Development of the Advanced Emitter Turn-Off (ETO) Thyristor

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By

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(ABSTRACT)

Advancements in the power electronics systems have been directly related to the availability of improved power semiconductor devices. The device performance greatly determines the efficiency, reliability, volume, and cost of the power electronics system. This dissertation is dedicated to develop an advanced high power semiconductor device, the emitter turn-off (ETO) thyristor, which is targeted to improve the limitations of the present high power devices.

Major improvements in electrical and mechanical designs of the ETO for high power and high frequency operation are proposed which result in improved snubberless turn-off capability, low conduction loss, and low gate drive power consumption of the new generation ETO.

A revolutionary self-power generation method of the ETO is proposed. Different from the conventional high power devices which require the external power input for their gate drivers, ETO achieves complete optically controlled turn-on and turn-off and all the internal power required is self-generated. This advancement will have a major impact to high power converter designs.

A novel integrated method to eliminate the dead-time requirement is proposed for ETO. This method not only improves the output waveform quality but also increases the reliability and reduces the cost of the high power PWM voltage source converters. With this unique function, the upper and the lower ETO's within a converter phase leg can receive the ideal complementary (without dead-time) PWM signals and solve shoot-through problems.

Method to measure the ETO current and transfer the current information to a PWM signal is proposed. Based on the ETO's built-in current sensor, the over-current protection function of the ETO is designed as well. The experimental results show that the built-in current sensor has a very high precision, and the over-current protection function can effectively protect the ETO during the short circuit faults.

In order to improve ETO's turn-off capability, a comprehensive investigation of the turn-off failure mechanism of the ETO was performed. A series of simulations and experiments are carried out to study the ETO turn-off operation. The detail turn-off failure mechanisms are presented. The conditions to cause the ETO failure are addressed. The approaches to improve the ETO's turn-off capability are discussed.

To my parents

And my wife, Sha Wu

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Chapter 1. Introduction

1.1. The Present State of the Art in High Power Semiconductor Devices

Energy in electrical form is one of the most important elements in modern industrial civilization. In the modern world an increasingly significant portion of the generated electrical energy is processed through power electronic systems for various applications in industrial, commercial, residential, aerospace, and military environments [A 1].

Power semiconductor device is the key element of the power electronic systems. Historically, the evolution of power electronics has generally followed the evolution of power semiconductor devices, although some generic power converter topologies have been in existence from the early gas tube age. The majority of the power electronic systems in the world today by volume are in the low and medium power range from hundreds of milliwatts to tens of kilowatts. However, a significant amount of power is processed by very high power level power electronic systems ranging from hundreds of kilowatts to gigawatts. This trend is increasing rapidly with the development of the flexible AC transmission systems (FACTS), high voltage DC (HVDC) transmission systems, and high power traction applications [A 2], [A 3]. The present widely used high power semiconductors to build the high power electronic systems are thyristor, gate turn-off thyristor (GTO), high voltage insulated gate bipolar transistor (HVIGBT), and integrated gate commutated thyristor (IGCT). Fig. 1.1 shows the development time line of high power semiconductor devices [A 4], [A 6], [A 7]. Fig. 1.2 shows the power range of commercially available high power semiconductors [B 1]-[B 6], [C 1]-[C 3]. In Fig. 1.2

the maximum collector-emitter voltage and DC-collect current are shown for IGBT's. Repetitive peak off-state voltage and maximum RMS on-state current are shown for Thyristors, GTO's, and IGCTs.

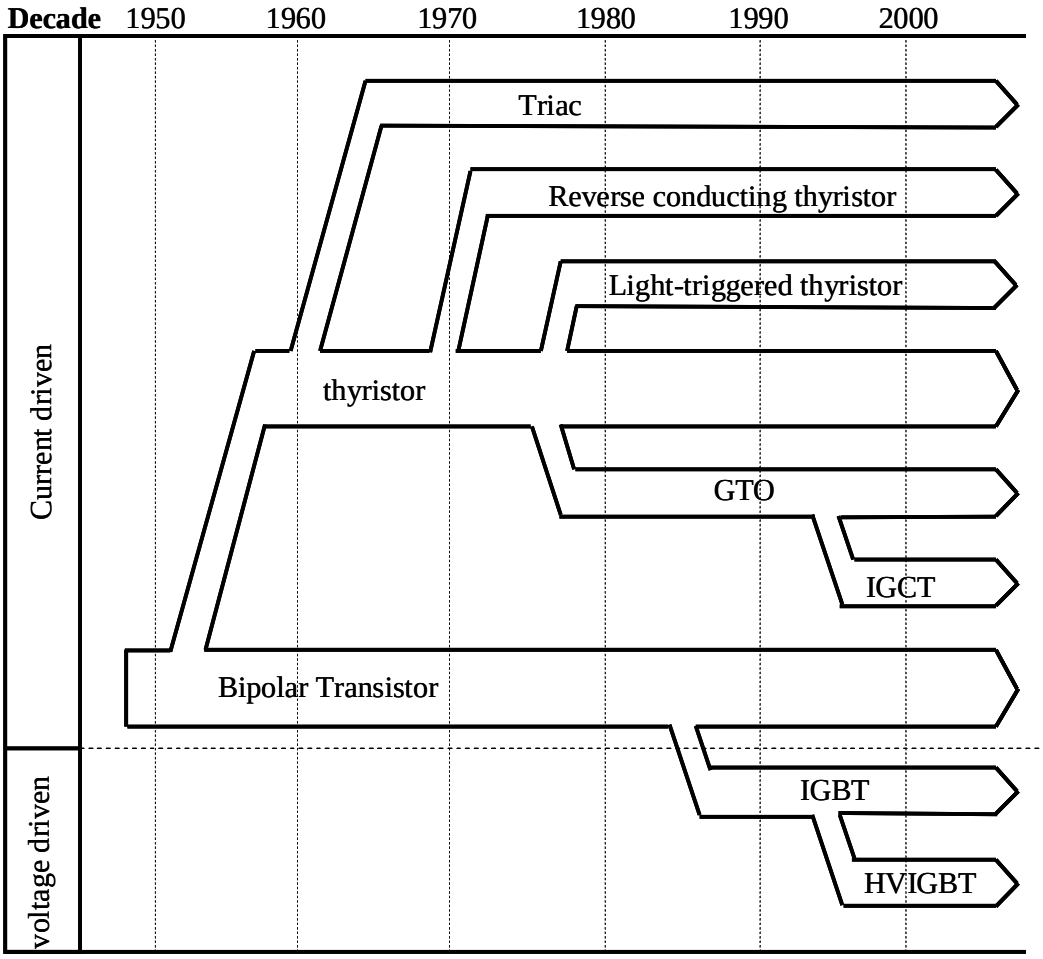


Fig. 1.1 The development time line of high power semiconductor devices

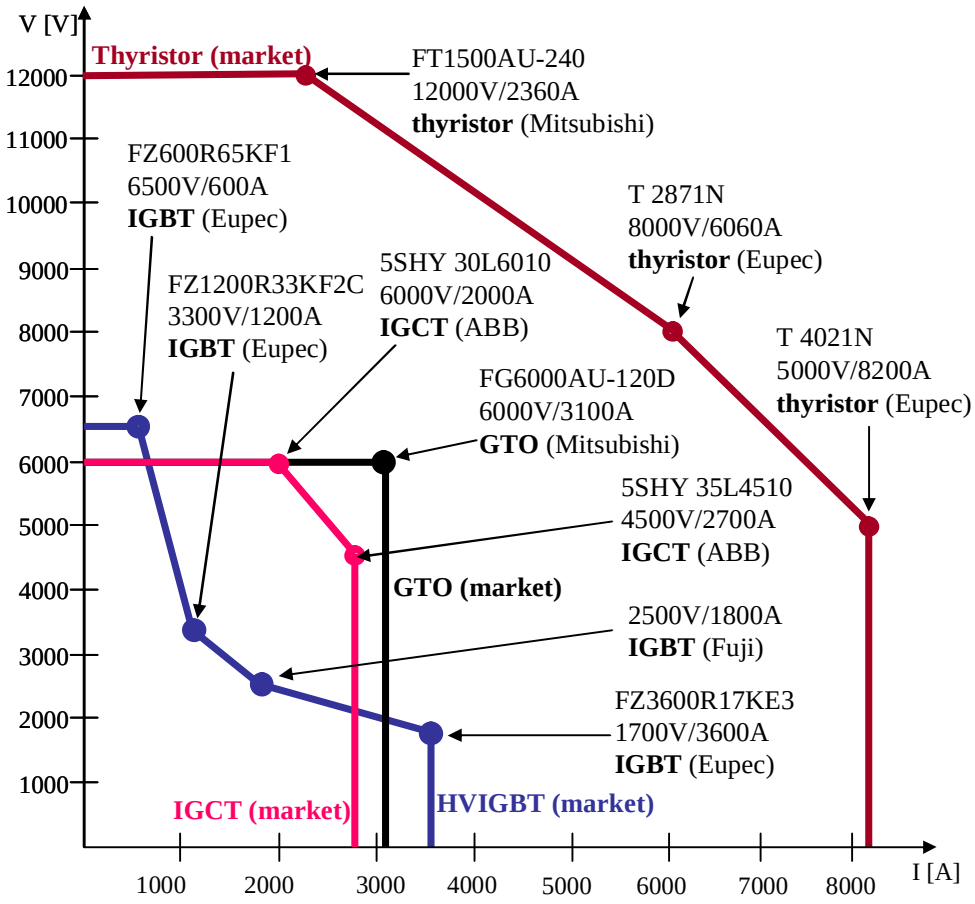


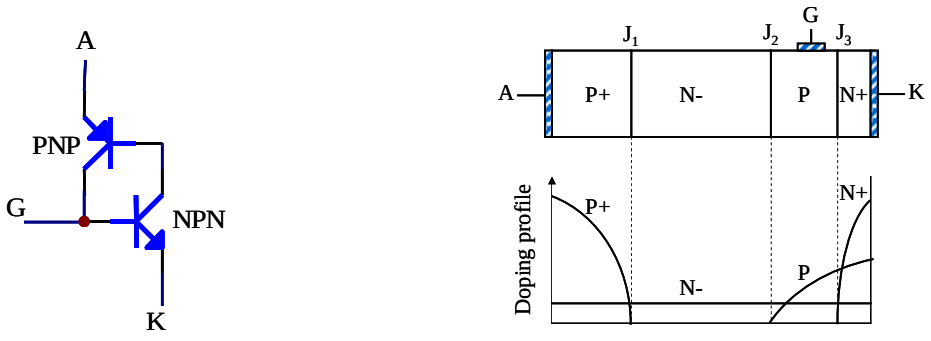
Fig. 1.2 Power range of commercially available high power semiconductors

1.1.1. Thyristor

The age of modern power electronics began by the invention of the thyristor (also called silicon-controlled rectifier (SCR)) in the 1950s, and it reigned almost supreme for the first two decades.

The thyristor is four-layer three junction device of the structure of PNPN [A 5], where PNP and NPN transistors are connected in regenerative feedback mode. The thyristor usually fabricated in a single die up to six inches in diameter. The equivalent circuit and basic structure are illustrated in Fig. 1.3. The thyristor has the capability of supporting

voltage in both directions and can be triggered into a current conduction mode by a small current pulse into the gate when the anode voltage is positive. In the on state there is very strong minority-carrier injection in all four regions, junction J_2 is forward biased, and the BJT's are saturated. In this saturation the large conductivity modulation is represented by the stored charge distribution.



(a) (b)

Fig. 1.3 The power thyristor: (a) the equivalent circuit and (b) the structure and doping profile

The thyristor is the best switch in on-state and off-state among all the high power semiconductor devices. It has the highest voltage blocking and current conducting capabilities: in off state it can block high voltage with very small leakage current, and in on state it can conduct very large current with very low voltage drop. Additionally, once the thyristor is turned on, the two coupled transistors within the thyristor can provide the base drive currents for each other and no gate current injection is required to maintain the on state.

The main disadvantage of the thyristor is that it can not be turned off by its gate and it only returns to the off state if the anode current falls below a certain minimum value or if the direction of the anode current is reversed.

Since its introduction, the thyristor has been widely used in phase controlled DC drives, AC drives, lighting and heating control, welding control, HVDC, static VAR compensation (SVC), and Solid state circuit breakers [A 4]. They are mostly used today in very large power applications, mainly power systems and very large motor drives.

The light triggered thyristor (LTT) can be triggered on by light applied to the gate area rather than by the electrical impulse [B 7]-[B 9]. Now LTT with 8000V/5000A power rating is commercially available. Fig. 1.3 shows the picture of the light triggered thyristor T2563N, produced by Eupec. LTT greatly simplifies the thyristor gate control unit, saves gate control energy, improves the reliability, and electromagnetic immunity. More and more LTT's are being used in the high voltage power electronic systems such as HVDC and SVC.

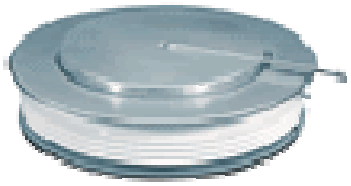


Fig. 1.4 Picture of the light triggered thyristor T2563N

1.1.2. GTO

Thyristor is typically used as phase-controlled current valves for AC circuits, operating at low frequencies (most often around AC line frequency). Since thyristor can not be turned off by its gate, it is not suitable for applications with DC power sources.

This has motivated the development of power thyristors that can be switched from the on-state to the off-state under gate bias control. Such devices are referred to as gate turn-off thyristors, or GTO's.

GTO is a thyristor type device that not only can be turned on by a positive gate current pulse but also has the capability of being turned off by a negative gate current pulse. With its high power handling capability and gate turn-off capability, GTO has been the dominant fully controllable semiconductor devices in the high power conversion areas, since it was introduced to the industry in the 1970s.

The gate turn-off capability is obtained by increasing the turn-off gain [A 5], which is achieved by making the gain of the NPN transistor close to unity and the gain of PNP transistor small. A low gain for the PNP transistor is obtained by reducing the minority carrier lifetime in the N-base region, forming anode shorts, or including a highly doped N-type region (buffer layer) at the anode regain. Using the anode short or buffer layer structure, GTO will lose the reverse blocking capability, becoming the so called asymmetrical GTO (the GTO without the anode short and buffer layer is called symmetrical GTO). Fortunately, in voltage-fed converters, which dominate the present power converters, there is always a diode connected in anti-parallel with each of the GTO's, and the reverse blocking capability is not required. The symmetrical GTO has reverse blocking capability, finding applications in current source converters. By the buffer layer structure the wafer thickness of the asymmetrical GTO can be thinner than that of the symmetrical GTO with the same voltage blocking capability, leading to benefits such as lower voltage drop and lower turn-off loss. The doping and electrical field profiles of the symmetrical GTO and asymmetrical GTO are shown in Fig. 1.5.

Besides anode short, the transparent anode technology was introduced [B 10], [B 11], [A 9]. A transparent anode structure has thin p-base layer and brings high trigger characteristics without sacrificing turn-off performance. The cross-section structure of the anode short GTO and transparent GTO is shown in Fig. 1.6.

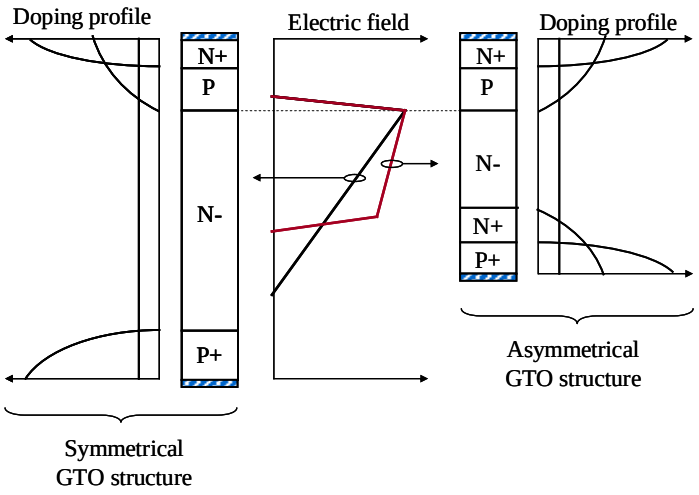
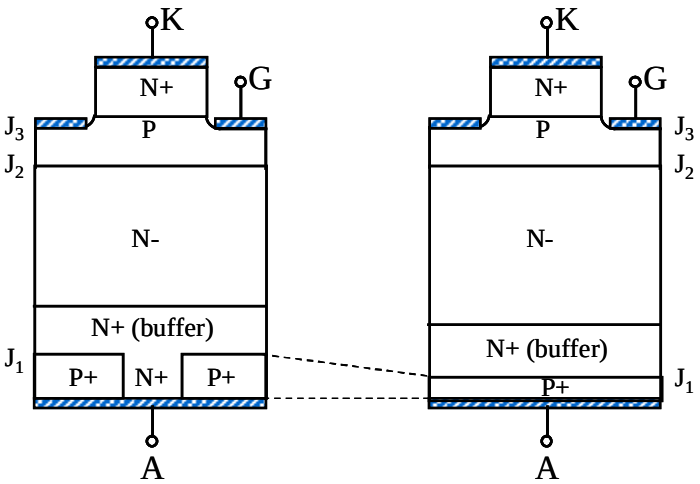


Fig. 1.5 The doping and electrical field profiles of the symmetrical GTO and asymmetrical GTO



(a) (b)

Fig. 1.6 The cross-section structure of the (a) anode short GTO and (b) transparent GTO

To improve the turn-off homogeneity of all cathode regions, the highly interdigitated gate and cathode geometry structures are used to lay out the gates and cathodes. The basic goal is to maximize the periphery of the cathode and minimize the distance from the gate to the center of the cathode region.

The main disadvantage of the GTO is that it requires a switching stress reduction network (snubber) for safe turn-on and turn-off [A 10], [B 13], and the snubber heavily limits the performance of the GTO and further, the GTO based power converter. Fig. 1.7 shows a two level GTO voltage source converter phase leg with di/dt and dv/dt snubbers.

In Fig. 1.7, D_p and D_n are anti-parallel diodes of the GTO's. Those diodes have the same rating as the GTO's and those high power diodes have relatively slow reverse recovery. Each time when a GTO is turned on is always associated with a diode being turned off. Take Fig. 1.7 for example, if the output current is flowing out of the phase leg, turning on of ETO_p will force D_n to turn off. During turn-on, the GTO will have a fast turn-on current rising time compared with diode's reverse-recovery time, due to GTO's latch mechanism and the highly interdigitated gate-cathode structure. If without the di/dt snubber limiting the turn-on rising current, very large over current will flow in both the GTO and the diode, may leading to the diode's turn-off failure or GTO's turn-on failure. The di/dt snubber shown in Fig. 1.7 is commonly used in the GTO based converters.

When a GTO is being turned off, the segments close to the gate contact tend to turn off first, while the turn-off of those remote segments from this contact are delayed due to the p-base lateral resistance. If the total GTO anode current is kept constant, the current in these remote regions will increase. The current inhomogeneous distribution of the

GTO during turn-off may cause the current crowing regions of the GTO overheat or being retriggered back into the on-state, leading to a turn-off failure. To prevent this from happening, a portion of the GTO current must be diverted to the dv/dt snubber to reduce the total GTO anode current of the GTO during its turn-off. Normally, the dv/dt snubber is designed to limit the rising rate of the anode-cathode voltage to about 500V/μs to 1000V/μs [B 14]. A commonly used dv/dt snubber is illustrated in Fig. 1.7. The power dissipation by the dv/dt snubber can be calculated by (1-1)

$$W_{dv/dtsnubber} = \frac{1}{2} \cdot C_s \cdot V_{dc}{}^2 \cdot f_s \qquad (1\text{-}1)$$

The dv/dt snubbers greatly reduce the system efficiency. For example, if the GTO switches at 500Hz with 6μF snubber capacitor under a DC link voltage of 2.5kV, the loss is about 9.4kW.

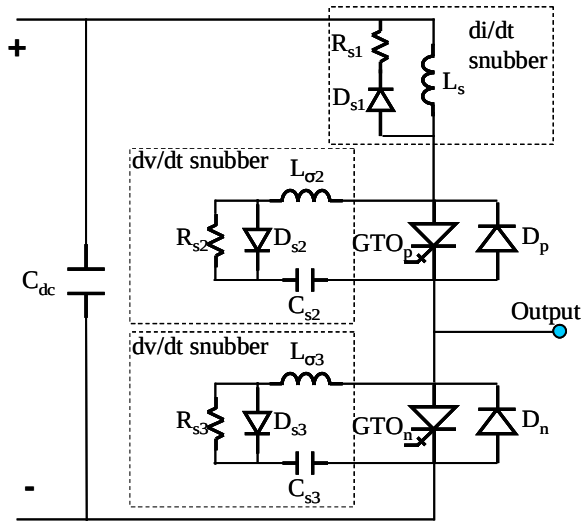
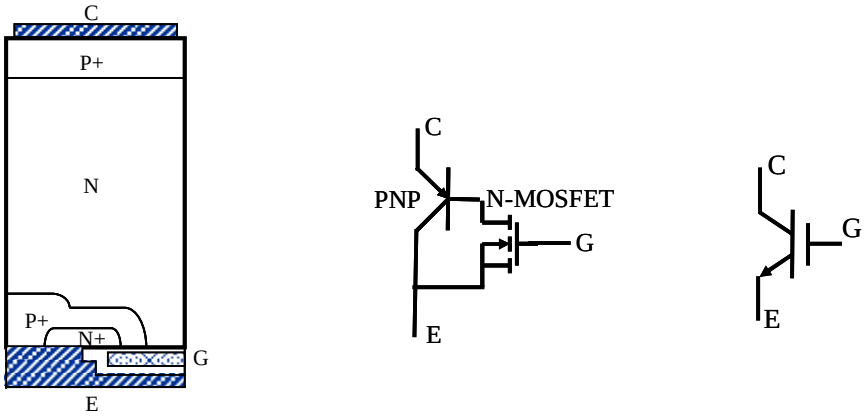


Fig. 1.7 A two level GTO phase leg with di/dt and dv/dt snubbers

1.1.3. IGBT

The supremacy of the GTO in the high power conversion area is increasingly being challenged by IGBT's, whose voltage and current handling capabilities are constantly improving with the advance of fabrication technology [C 4]. HVIGBT's refer to the IGBT's whose voltage block rating is over 3300V.

The IGBT is essentially a MOSFET with an additional p-layer to improve the conduction capability by injecting minority carriers. The structure and the equivalent circuit are illustrated in Fig. 1.8. Due to the injection of a high concentration of holes from the P^+ substrate in the N-drift region, the IGBT has a much lower forward voltage drop as compared to a power MOSFET structure. Since the input signal of the IGBT shares the high impedance advantage of the power MOSFET, the IGBT is also classified as MOS-controlled device. However, compared to MOSFET, the switching speed of IGBT is limited by the time taken for removing the stored charge from the drift region due to the injection of the holes during the on-state current conduction. The turn-off time, especially the tail current, is strongly determined by the minority lifetime. The tail current is the main cause of the IGBT's turn-off loss (E_{off}). Reducing minority lifetime can decrease the turn-off time and the tail current but increase the on-state voltage drop (V_F). Therefore, a trade-off has to be made for the switching speed vs. the on-state voltage drop.



(a) (b) (c)

Fig. 1.8 IGBT: (a) the cross section, (b) the equivalent circuit, and (c) circuit symbol

IGBT's have been improved to realize high blocking capability, high switching speed and low loss by microfabrication and technologies such as local lifetime control, punch-through structure, etc. Additionally, the press-package HVIGBT's are developed to further improve the reliabilities, and are favorable to the applications where fail-short is desirable [A 9]. The picture of the standard IGBT and the press-pack IGBT [C 5] are shown in Fig. 1.9.

(a) (b)

Fig. 1.9 The IGBT pictures: (a) standard IGBT and (b) press-pack IGBT

IGBT turns off as the open-base transistor mode and does not have the latch mechanism as the GTO. Thus dv/dt snubber is not required for the turn-off of IGBT.

Another important characteristic making the IGBT different from the latch type devices is its current saturation feature, which is illustrated in Fig. 1.10. IGBT can be used in the voltage converters without di/dt snubber. IGBT's current saturation capability effectively limits the over-current caused by the reverse-recovery of the diode. Additionally, when over-current fault happens, IGBT can limit the rising rate of the fault current by increasing collect-emitter voltage, making the over-current protection much easier than the latch type devices. Fig. 1.11 shows a two level IGBT voltage source converter phase leg. Compared with the GTO phase leg shown in Fig. 1.7, IGBT converter eliminates the bulky dv/dt and di/dt snubbers. The converter construction is highly simplified.

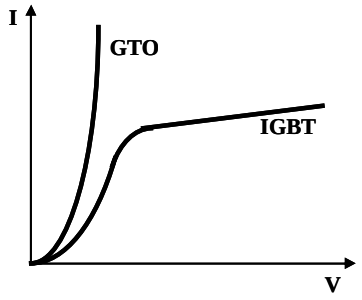


Fig. 1.10 the forward I-V characteristics of GTO and IGBT

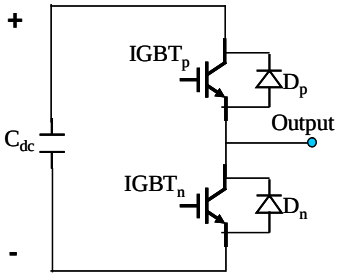


Fig. 1.11 A two level IGBT phase leg

1.1.4. Hard-driven GTO

In the late 1990s, the GTO and an innovative gate drive method were merged and formed the hard-driven GTO concept. By combining the advantages of the low on-state voltage drop of the thyristor and the uniform turn-off mechanism of the transistor, hard-driven GTO's have made inroads into a future that was firmly believed to belong to MOS-controlled devices.

The concept of the hard-driven GTO is turning off the GTO by driving the GTO's gate current quickly to equal to the anode current before the anode voltage starting to rise. In this condition, referred to as unity-gain turn-off or hard-driven, the NPN transistor turns off first and the main GTO turns off in the rugged open-base PNP transistor mode, eliminating any possibility of latching [B 13], [B 15].

Supposing the GTO's storage time, the time interval between the GTO starting to be turned off by the negative gate current to the anode voltage starting to rise, is t_s, the gate loop total inductance is L_{gt}, and the gate voltage applied to turn off the GTO is V_d, then the maximum GTO anode current I_{TGQM} can be turned of through the unity turn-off gain can be calculated in (1-2).

$$I_{TGQM} = \frac{V_d \cdot t_s}{L_{gt}} \qquad (1\text{-}2)$$

Fig. 1.12 shows the standard GTO and its turn-off circuits [E 1]. To turn off the GTO, switch S_1 is closed to apply negative voltage V_d to GTO's gate. L_g is the GTO gate inductance which is about 10nH, L_c is the coaxial cable inductance which is about 200nH, L_d is the gate driver inductance which is about 100nH. So the gate loop total inductance L_{gt} is about 310nH.

In order to obtain high emitter efficiency at the cathode end, desirable for good turn-on characteristics, the n+ emitter layer of the GTO must be high doped, giving a gate-cathode reverse breakdown voltage, V_{GRM}, to the adjacent p-base of typically 20-24V. V_d must be designed to be low than V_{GRM} to guarantee the GTO gate-cathode junction will not constantly break down, destroying the GTO.

The storage time t_{st} of the GTO in the unity turn-off gain condition is about 1μs.

Suppose V_d is 18V. Then according to (1-2), the maximum unity gain turn-off current I_{TGQM} of the standard GTO is about 60A, which is much lower than the GTO's current rating.

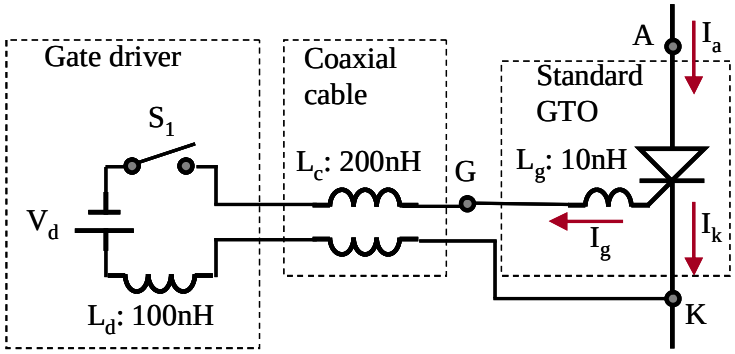
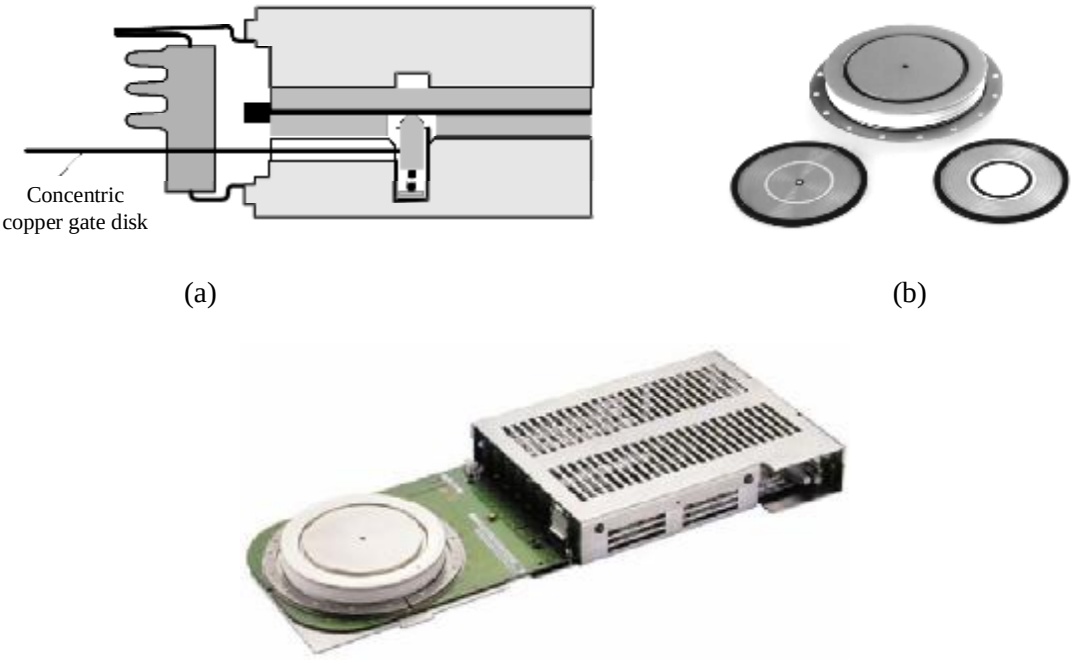


Fig. 1.12 The standard GTO and its gate drive circuit

(1-2) indicates that to increase the maximum unity gain turn-off current, one can increase V_d, increase t_s, or decrease L_{gt}. Based on the present GTO technology, V_d and t_s is difficult to be further increased. So decreasing L_{gt} seems to be the only solution. According to (1-2), to increase the gain turn-off current I_{TGQM} to over 4000A, L_{gt} should be as low as about 4.5nH. For a long time, it was believed that the only way to achieve such a low gate loop inductance is by integrating the gate-drive into the GTO's ceramic housing. Although possible in principle, cost and reliability goals finally rule this out.

In the middle of the 1990s, IGCT, a low cost approach to highly reduce the gate loop inductance, was introduced [B 16]. By using the coaxial GTO housing and interconnecting gate drive with power semiconductor device by a printed circuit board, IGCT dramatically reduces the total gate loop inductance to less than 3nH. Fig. 1.13 (a) illustrates the cross section of the low inductance gate contact. Fig. 1.13 (b) shows the housing and wafers. Fig. 1.13 (c) shows the picture of IGCT 5SHY 35L4511 produced by ABB.



(a) (b)

(c)

Fig. 1.13 IGCT: (a) low inductance gate contact, (b) housing and wafers, and (c) the picture of 5SHY 35L4511

Calculating (1-2) using 2nH of L_{gt}, it can be seen that IGCT has about 6000A unity gain turn off capability. Additionally, since the gate loop inductance is reduced, the turn-

on characteristics are improved as well. The turn-on di/dt capability is improved and turn-on delay time is reduced. IGCT has the following major advantages over the standard GTO:

- By eliminating the current inhomogeneous distribution during turn-off, IGCT can be safely turned off without dv/dt snubber. IGCT dramatically simplifies the converter construction, increases the converter efficiency, and reduces the cost.
- Turn-off and turn-on delay time is highly reduced, making it much easier for the device series connection applications.
- Power consumption of the gate driver is greatly reduced.

At present, the IGCT's with peak off state voltage/maximum turn-off current of 4500V/4000A and 6000V/3000A are commercially available. Fig. 1.14 shows a two level IGCT voltage source converter phase leg. Compared with the GTO phase leg shown in Fig. 1.7, IGCT converter eliminates the bulky dv/dt snubbers. Instead, only one capacitor C_{clamp} is used to clamp the peak voltage across the IGCT's.

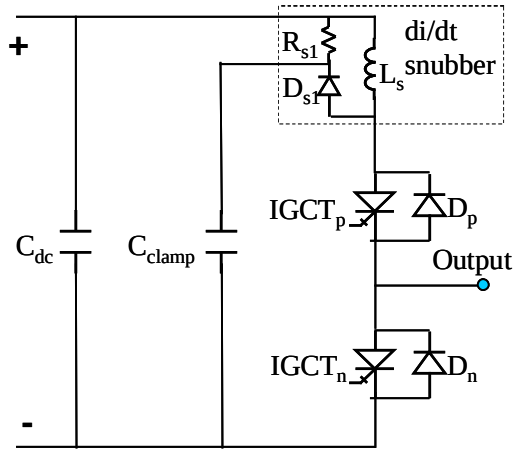


Fig. 1.14 A two level IGCT phase leg

1.2. The Limitations of the Present High Power Device Technologies and the Developing Trend of the Future Device Technologies

The performance of the semiconductor devices is paramount to power converter design. The power semiconductor device is the most complex, delicate, and fragile element in a power converter. Although the cost of the power semiconductor device in a typical power converter may not exceed typically 20% to 30% [A 4], the total power converter performance, reliability, volume, and cost is highly influenced by the performance of the semiconductor device.

The engineers always dream that there are ideal high power switches available to build the power electronic systems.

An ideal high power switch should have at least the following characteristics:

- Infinite large current conduction capability in the on-state with zero voltage drop
- Infinite large voltage block capability in the off-state with zero leakage current
- No turn-on and turn-off delay time
- The on/off of the switch are fully controlled by the optical signal. No isolation for the drive signal is required to deliver to the switches which are at the different voltage potentials.
- Current sensing capability
- Over-current limit and protection capability
- Low Cost

Unfortunately, the characteristics of the present power semiconductor devices are much inferior to the ideal high power switches, and the performance of the power converters is degraded to compromise the limitations of the power semiconductor devices. The main develop trench and the limitations of the present high power device technologies are discussed in the following sections.

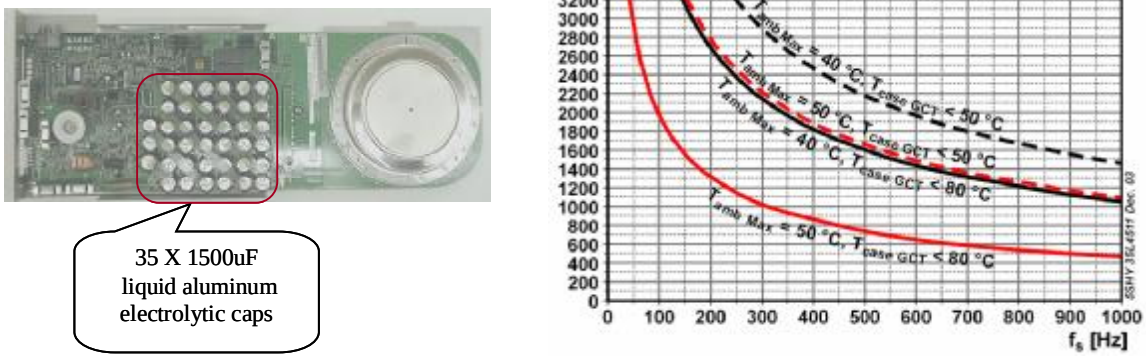
1.2.1. The Development of the New High Power Device with High Power Handling Capability is Necessary

By combining the advantages of the low on-state voltage drop of the thyristor and the uniform turn-off mechanism of the transistor, IGCT is believed to have low conduction loss and switching loss. However, IGCT has high gate drive power consumption due to its current turn-on and current turn-off mechanism. To turn on the IGCT, a firing pulse is injected into the GTO's gate. While the IGCT is on, a small DC current is provided for the GTO's gate in order to ensure that the GTO remains in a low conduction loss state. To turn off the IGCT, a large turn off current, whose peak value is equal to the total anode current, need to be drawn from GTO's gate to achieve unity turn-off gain. Large energy is required to provide the turn-on and turn-off current. A large amount of low lifetime liquid aluminum electrolytic caps are required to reduce the gate loop inductance and deliver the huge turn-off current. The picture and maximum turn-off current vs. frequency for lifetime operation of the caps of the IGCT 5SHY 35L4511 [B 18] are shown in Fig. 1.9. It can be seen that IGCT is able to conduct 2000A at 1kHz switching frequency, however, due to the reliability issue caused by the caps, the current capability

has been reduced to about 500A when T_{amb}=50°C and T_{case}=80°C. Those liquid aluminum electrolytic caps greatly limit the output power capability of IGCT.

IGBT is a voltage controlled device, and has low gate drive power consumption. However, IGBT works in a transistor mode during on-state, and has a high conduction loss comparing with the GTO type devices

Therefore, it is necessary to develop a new type of high power device which has both low conduction loss and low gate drive power consumption to further increase the power handling capability.



(a) (b)

Fig. 1.15 The on-board capacitors of IGCT: (a) picture and (b) maximum turn-off current vs. frequency for lifetime operation of the caps

1.2.2. The Present Power Devices Demands the Isolated Gate Driver Power Inputs.

The present fully controllable semiconductor devices are controlled/triggered by the electrical signals. Isolation for the gate drive power and signal is required to control the devices at the different voltage potentials. The external power supplies for the device gate

drivers needs to be individually designed. The power for each device gate driver is normally provided from low voltage potential (normally ground potential), as shown in Fig. 1.16. The insulation transformer is required to deliver the power to the device gate driver which is at the different voltage potential. In a high voltage converter, those insulation transformers have large sizes and are often difficult to implement the reliable insulation design. These external power supplies for the gate drivers increase the cost, decrease the efficiency, and reduce the reliability of the total system. As an example, Fig. 1.17 shows an IGCT with the power supply for its gate driver.

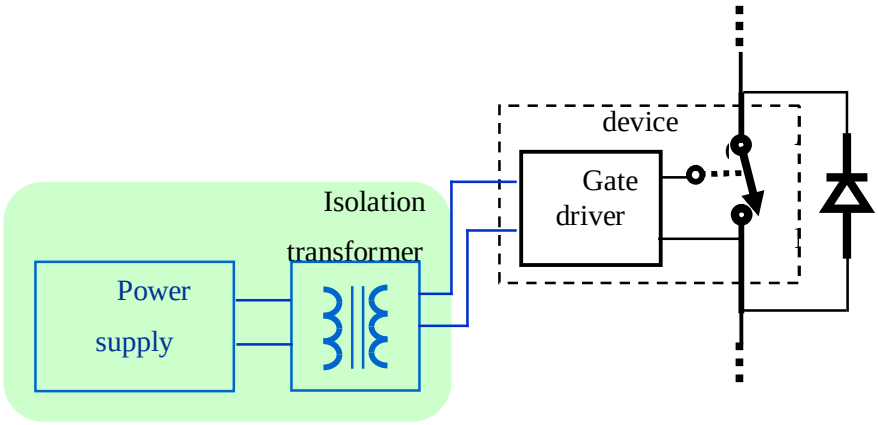


Fig. 1.16 Getting gate drive power from low voltage potential (ground) through insulation transformer

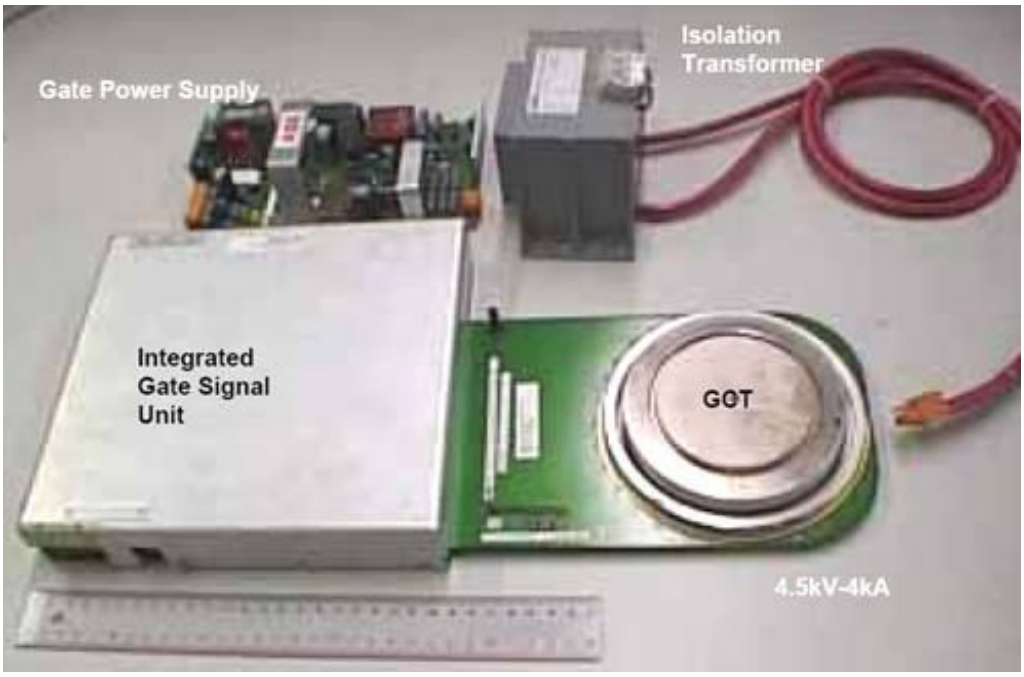


Fig. 1.17 An IGCT with the power supply for its gate driver

1.2.3. The Dead-time Effect Causes Output Distortion and the Fundamental Voltage Loss.

In the voltage source PWM converters, if the upper and lower devices within a phase leg are fed with the fully complimentary PWM commands, the current shoot through in the DC link will happen because of the turn-on and turn-off delay of the devices. Therefore the dead-time, which is a short time period during which both the upper and lower devices of the inverter phase leg are off, needs to be inserted in the PWM commands to prevent such a fault condition. The dead-time causes such problems as the waveform distortion and the fundamental voltage loss of the converter. Many dead-time compensation methods were proposed [E 2], [E 3], [E 4]. However, these methods require current sensors or voltage sensors to obtain the output current or output voltage

information. The current sensors or voltage sensors increase the cost of the system, especially in the open loop controlled converters, where the current sensor and voltage sensor are not necessary for the control purpose. In addition, the conventional dead-time compensation methods are often not effective during the time period when the load current is cross zero.

Therefore the converter construction and control would be greatly simplified if the devices within the converter have the capability of receiving fully complementary PWM commands and preventing the shoot through faults from happening.

1.2.4. The Present High Power Devices Lack Current Sensing Capability

In a power converter, the load current information is often used for the current close loop control. Although the load current always flows through one or more semiconductor devices, the present devices do not have the current sensing capability. Instead, the expensive and complicated external current sensors are necessary to sense the load current. Therefore, a new high power device with the current sensing capability will reduce the cost and increase the reliability of the system.

1.2.5. The Present Hard-Driven GTO Technology Lacks the Over-Current Protection Capability

The present hard-driven GTO technology has such advantages as low conduction loss and high voltage block capability. However, the reliability of the hard-driven GTO technology is heavily limited by its lacking of the over-current protection capability.

The over-current caused by the short circuit, malfunction, or the component failure is severe fault situation that can result in further failure of the power converter if appropriate remedial action is not taken in time. The over-current protection of the GTO technology based converter is more complicated and difficult than that of the MOSFET, BJT, or IGBT based converters. For the MOSFET, BJT, or the IGBT, the accidental over-current can cause the device to go out of the saturation region and enter the active region, and the rising voltage of the device will limit the current. In this situation, the converter can be protected if the device is commanded to shut down quickly. However, the latching devices such as IGCT cannot enter such active region to limit the current. In contrary, the large fault current will make the IGCT latch more strongly. IGCT can only be protected if the over current is detected by an external current sensor, and the controller turns off the IGCT immediately. Fig. 1.18 shows an IGCT based three phase converter, where S_{ap}-S_{cn} are IGCT's. If the short circuit happens between point A and point B, the fault current will flow through current sensor A and current sensor B. If current sensor A and current sensor B send current signal to the controller, the controller can turn off all the IGCT's. If the rising rate of the fault current is limited, the IGCT's can be protected. However, if the short circuit happens between point A' and point B', or between point A' and V_{DC}, the fault current will not flow through any current sensor. In this situation, the over current can not be detected and protected. If the IGCT are still commanded to switch, one or more IGCT will be destroyed.

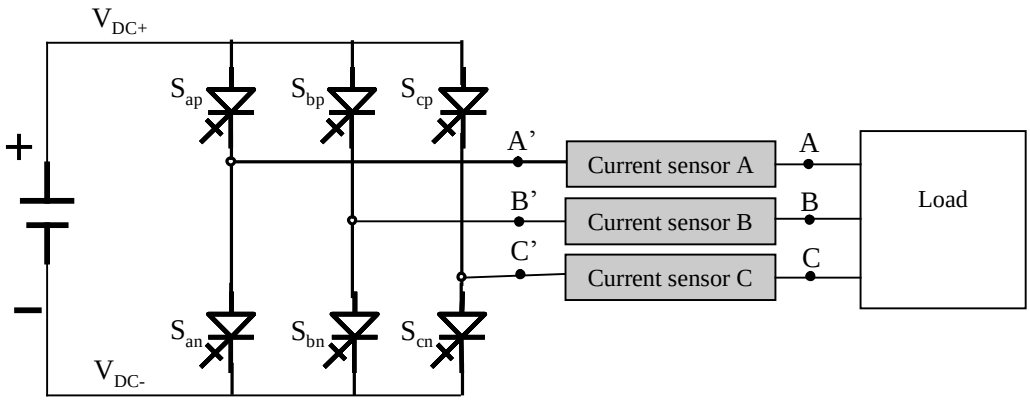


Fig. 1.18 An IGCT three phase converter

If the device can detect the fault conditions and turn off by itself, the device and the system will be protected as long as the rising rate of the fault current is limited. Therefore, the development of a new hard-driven GTO with the built-in over current protection capability will greatly improve the reliability of the devices and the converter.

1.2.6. The Turn-Off Failure Mechanism of the Hard-Driven GTO is still not Well Understood.

The turn-off failure mechanism of the conventional GTO with dv/dt snubber has been the subject of many experimental and simulation studies [B 19]-[B 22]. The studies show that due to the lateral voltage drop in the gate metallization and variations in the carrier lifetime or emitter efficiencies among the GTO cells, the GTO current will redistribute during the turn-off operation from the whole device into one or several singular current filaments situated in the last unit cells that turns off, leading to the device being retriggered on locally.

The turn-off mechanisms of the hard-driven GTO are quite different from the conventional GTO. A hard-driven GTO cuts off electron injection from the cathode emitter before anode voltage starts to increase [B 23]. The hard-driven GTO turns off in a transistor mode. So GTO cells being retriggered on, which is the main reason leads to conventional GTO turn-off failure, not likely happens in the hard-driven GTO. The exact failure mechanism of the hard-driven GTO is still not well understood. According to [B 24], IGCT's have turn-off failed at 200kW/cm^2~300kW/cm^2 power density. However, this power density is still relatively low for the silicon material [B 25], [B 26].

[B 27]- [B 30] shows that there is currently non uniform distribution among the GTO cells during turn-off. However, this only causes small temperature inhomogeneity. And in their simulation, the current distribution becomes uniform again when the voltage starts to rise. In [B 24], the authors attributed the turn-off failure to the on-set of dynamic avalanche. After dynamic avalanche, the anode voltage can still rise and the device may still be turn off. Actually, dynamic avalanche alone may not cause the turn off failure. The literatures did not precisely explain the failure mechanism.

It is therefore very important to investigate the exact failure mechanism and propose the way to improve the turn-off rating of the hard-driven GTO, and further increase the reliability of the high power converter.

1.3. Dissertation Outline

Besides IGCT technology, another approach to realize the unity turn-off gain of the GTO, the MOS-GTO hybrid configuration, was proposed in the later 1990s [B 31]-[B 34], [D 1]-[D 3]. One of such technologies is the emitter turn-off (ETO) thyristor, which is

based on mature technologies of the GTO and power MOSFET. The ETO concept provides the potential to develop a new generation high power devices with high performance, high functionality, and low cost.

This dissertation is dedicated to develop the advanced ETO which is targeted to solve the limitations of the present high power devices. This dissertation investigates the following topics related to the development and analysis of the ETO:

1.3.1. The Major Electrical and Mechanical Improvements in the Advanced ETO

This chapter presents the development of the new generation ETO with high performance, high reliability, and low cost [D 4], [D 5]. After a briefly introduction of the ETO concept, the limitations of the first generation ETO are discussed. Then the innovative electrical and mechanical designs are introduced. The design to improve its manufacturability is addressed as well. Based on the new design, the new generation ETO was developed. The snubberless turn-off capability, low conduction loss, and low gate drive unit power consumption of the new generation ETO are experimentally demonstrated.

1.3.2. The Innovative Self-Power Generation Method of the ETO

This chapter presents the design and experimental demonstration of the innovative self-power generation function of the ETO [D 6]. Different from the conventional high power devices which require the external power input for their gate drivers, ETO achieves complete optically controlled turn-on and turn-off and all the internal power

required is self-generated. The Innovative self-power generation method of the ETO is demonstrated by the experiment.

1.3.3. A Novel Integrated Method to Eliminate the Dead-Time Requirement of the ETO

This chapter introduces the novel integrated method to eliminate the dead-time requirement. This method not only improves the output waveform quality but also increases the reliability and reduces the cost of the high power PWM voltage source converters [D 7]. With this unique function, the upper and the lower ETO's within a converter phase leg can receive the ideal complementary (without dead-time) PWM signals and solve shoot-through problem. In this chapter, the principle of the new generation ETO is described, and the experimental results of the ETO based PWM voltage source converters are presented.

1.3.4. The Built-in Current Sensor and Over-Current Protection of the ETO

This chapter introduces a method to measure the ETO current and transfer the current information to a PWM signal whose duty cycle is proportional to the current value [D 8]. Based on the ETO's built-in current sensor, the over-current protection function of the ETO is designed as well.

1.3.5. Investigation of the Turn-Off Capability of the ETO

The high-current turn-off capability is very important for ETO's safe operation, especially in the over-load and fault conditions. Both ETO and IGCT are based on hard-

driven GTO concept, and they share the same turn-off failure Mechanism. In this chapter, the methods to improve the ETO's turn-off capability are investigated. A comprehensive investigation of the turn-off failure mechanism of the hard-driven GTO was performed. A series of simulations and experiments are carried out to study the large area hard-driven GTO turn-off operation. The detail turn-off failure mechanisms are presented. The conditions to cause the hard-driven GTO failure are addressed. The approaches to improve the ETO's turn-off capability are discussed.

1.3.6. Summary and Future Work

This chapter summarizes the entire dissertation, and proposes possible future work.

Chapter 2. The Major Electrical and Mechanical Improvements in the Advanced ETO

Firstly, this chapter introduces the ETO concept, which was proposed in the later 1990s. The limitations of the first generation ETO are discussed. Then the innovative electrical and mechanical designs, which are concentrated on the improvements of the ETO's turn-off, turn-on and high frequency switching capabilities, are introduced. The design to improve its manufacturability is addressed as well.

Based on the new design, the new generation ETO was developed. The new ETO's were firstly tested in the boost pulses tester. The experimental results are presented and analyzed. The homogenous switching due to the unity turn-off gain and high turn-off gate current rising rate enlarges the ETO's SOA to full dynamic avalanche, approaching the physical limits of silicon. The short turn-off storage time, the high turn-on di/dt capability, low switching and conduction losses, and the low gate drive unit power consumption allow the ETO's to operate at high power and high frequency (kHz range).

Based on ETO's switching loss, conduction loss, thermal impedance, and the system's thermal dissipation, an ETO H-bridge voltage source converter's output current and output power capabilities were calculated. An ETO based H-bridge converter was built, and 1000 A_{RMS} output current at 2000V DC bus voltage and 1kHz switching frequency was demonstrated.

2.1. The Basic Concept of the ETO

ETO is a MOS-GTO hybrid high power device. Fig. 2.1 shows the ETO's equivalent circuit. An emitter switch Q_e is connected in series with the GTO, and a gate switch Q_g is connected to the GTO's gate. Each of Q_e and Q_e is consisted of many parallel connected MOSFET's to ensure the large current capability. ETO is turned on by turning on Q_e, turning off Q_g, and injecting current into the GTO gate (G_{GTO}). ETO is turned off by turning off Q_e and turning on Q_g. At this time, there is a voltage V_{Qe} applied across the cathode and the gate of the GTO, forcing GTO's cathode current divert to GTO's gate. V_{Qe} can be as high as the avalanche voltage of the MOSFET's, which can be much high than the GTO's gate-cathode reverse breakdown voltage, V_{GRM}. So if an ETO turns off a same current as an IGCT, a higher gate loop inductance L_{gt} can be tolerated to achieve the unity turn-off gain. The special low inductance GTO gate design is not required for ETO.

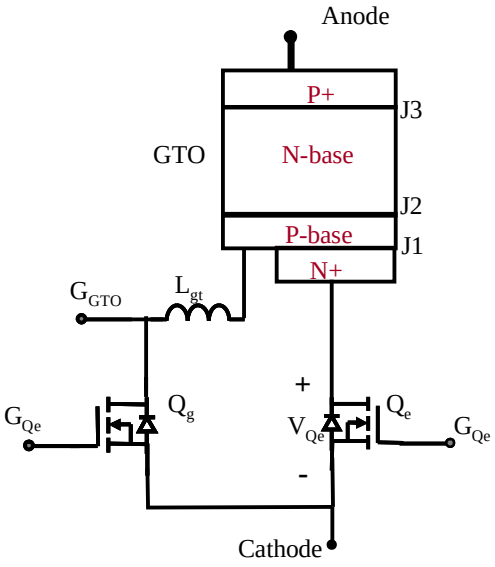


Fig. 2.1 The ETO equivalent circuit

The maximum ETO anode current I_{TGQM} can be turned off through the unity turn-off gain can be calculated in (2-1).

$$I_{TGQM} = \frac{V_{Qe} \cdot t_s}{L_{gt}} \qquad (2\text{-}1)$$

2.2. The Limitations of the First Generation ETO

The first generation ETO was developed in Center for Power Electronics (CPES), Virginia Tech, in 1999 [A 11], [A 12]. The picture of the first generation ETO is shown in Fig. 2.2. Although the ETO concept was demonstrated, the first generation ETO has limitations which prevent it from handling the real high power.

Fig. 2.2 The picture of the first generation ETO

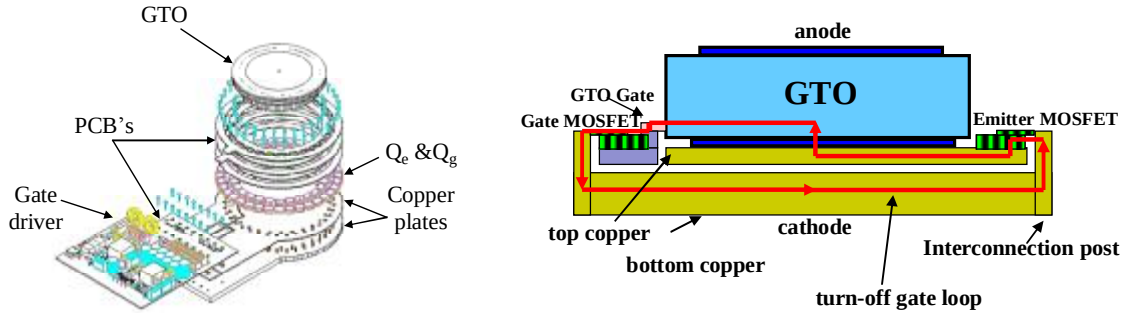
2.2.1. The Old Mechanical Design Leads to Large Parasitic Gate Inductance and Low Manufacturability

According to (2-1), the maximum unity-gain turn-off current is limited by MOSFET voltage, and gate loop inductance. Fig. 2.3 shows the assembling drawing and the cross section of the mechanical design of the old generation ETO. For the old design, the avalanche voltage of Qe MOSFET's is 55V. Q_e and Q_g are placed on two copper plates,

leading to a large gate loop inductance. According to measurement, the total gate loop inductance L_{gt} is about 27nH. The turn-off storage time of the GTO t_s is about 1μs. From (2-1), the ETO maximum unity-gain turn-off current I_{TGQM} is about 2000A, which is only half of the GTO maximum turn-off current (4000A).

From Fig. 2.3 (b) it can be seen that the old design includes many copper plates, discrete components, and many PCB boards. The emitter switch MOSFET's and gate switch MOSFET's are soldered on the multi-layer copper plates and connected by multiple PCB boards. The gate driver is on another PCB board. The emitter switch, gate switch and gate driver board are connected by the copper plates and the screws.

The mechanical design of the old generation ETO has poor manufacturability and reliability.



(a) (b)

Fig. 2.3 The mechanical design of the old generation ETO: (a) assembling drawing and (b) the cross section

2.2.2. The Abnormal Failure Issue Caused by the GTO Parasitic Diode

To reduce the turn-off switching loss of ETO, the anode short type GTO [B 11],[B 38]-[B 40] is used to build the ETO. Inside the anode short GTO, there is a parasitic diode D_{pa} from GTO's gate to anode, as shown in Fig. 2.4.

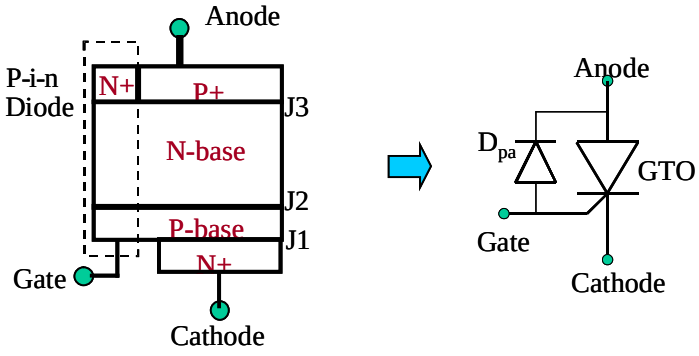


Fig. 2.4 Anode short GTO: (a) device model and (b) circuit model

In the voltage source converter applications, there is a diode connected in anti-parallel across the device. Fig. 2.5 shows the equivalent circuit with the anti-parallel diode D_1 of the old generation ETO. It can be seen that when D_1 is conducting current, there are two additional current paths, I_1 and I_2, from the ETO's cathode. I_1 and I_2 can easily reach ETO's anode through the GTO's parasitic diode. When ETO starts to block voltage, there will be reverse recovery current, which is caused by the parasitic diode, flowing through the ETO. The parasitic diode of the GTO has very poor reverse recovery performance since the junction J_2 is optimized for the thyristor performance instead of the diode performance [D 9]. Since the anode short part is a small portion of the anode side, even a small reverse recovery current may result in a current density that is high enough to destroy the GTO.

The abnormal failure issue of the old generation ETO strongly limits its capability for high power and high switching frequency applications.

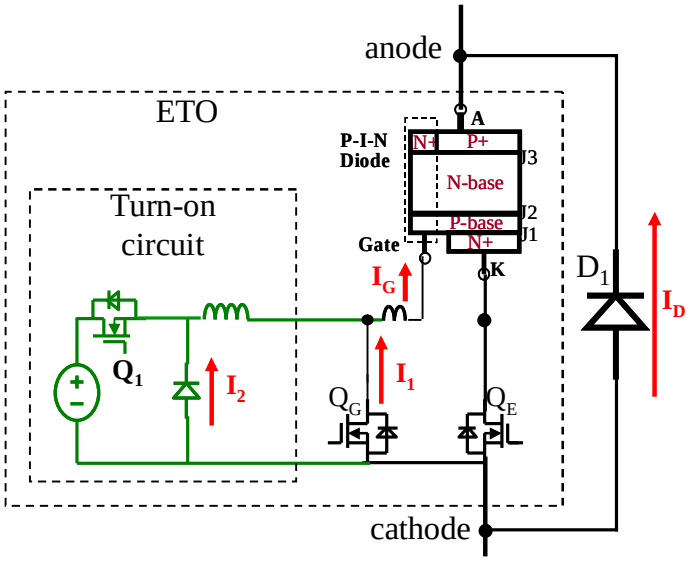


Fig. 2.5 The equivalent circuit with the anti-parallel diode of the old generation ETO

2.3. The Mechanical and Electrical Design of the New Generation ETO

The new Generation was designed to improve the ETO's turn-off, turn-on and high frequency switching capabilities. The design was targeted to increase the manufacturability and reduce the cost as well.

2.3.1. The Mechanical Design of the New Generation ETO to Minimize the Gate Loop Inductance, Increase the Reliability, and Improve the Manufacturability

Fig. 2.6 shows the picture of the new generation ETO. Fig. 2.7 and Fig. 2.8 show the mechanical assembly drawing and the cross-section drawing of the new generation ETO respectively. In the new design, all the components except GTO are put on a PCB circuit

board. The GTO and the circuit board are connected by copper plates. The heat generated by the GTO can be easily removed by double side cooling. The Q_e MOSFET's are arranged in a ring shape around the GTO to reduce the gate loop inductance and also allow easy conduction of heat generated by the Q_e. The ETO turn-off current gate loop is shown in Fig. 2.8. By these approaches, the gate loop inductance is greatly reduced. According to measurement, the total gate loop inductance L_{gt} is about 15nH. In the new design, 100V MOSFET is used for the emitter switch. Recall that the turn-off storage time of the GTO t_s is about 1μs. From (2-1), the new generation ETO maximum unity-gain turn-off current I_{TGQM} is about 6700A. The turn-off gate commutated current rising ratio di_{GQ}/dt=6700A/μs. The snubberless turn-off capability of the ETO is highly improved. Since the gate drive circuits, emitter switch, and gate switch are all put on the PCB board, the manufacturability and reliability is improved. A comparison between Fig. 2.7 and Fig. 2.3 (a) shows that the new design has a much simper mechanical design.

Fig. 2.6 The picture of the new generation ETO

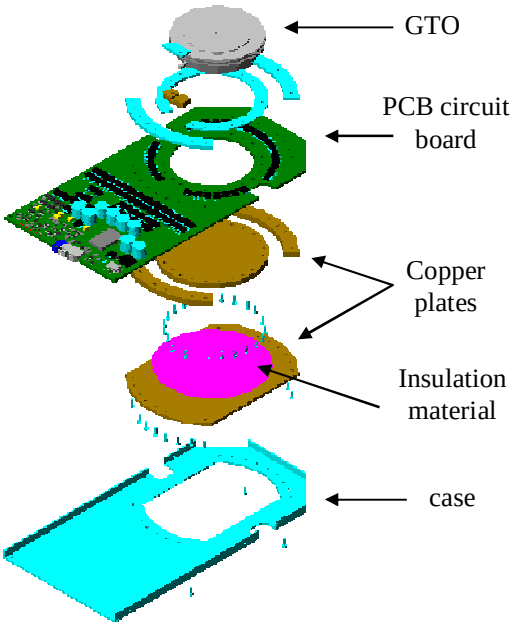


Fig. 2.7 The mechanical assembly drawing of the new generation ETO

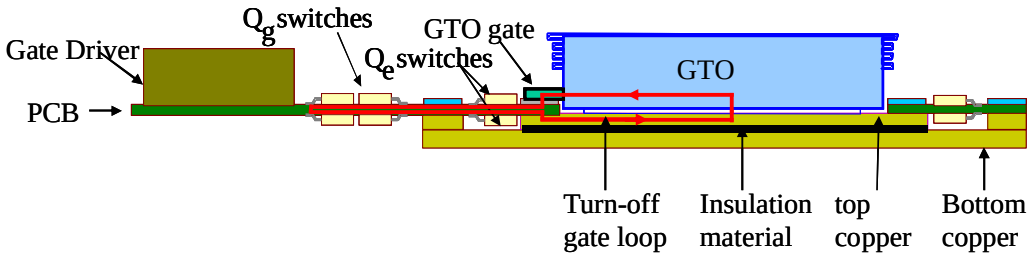


Fig. 2.8 The cross-section drawing of the new generation ETO

2.3.2. The Electrical Design of the New Generation ETO to Increase the Turn-Off and Turn-On Capability and High Power Switching Capability

Fig. 2.9 illustrates the circuit diagram of the new generation ETO including DC current injection, pulse current injection and clamp circuit.

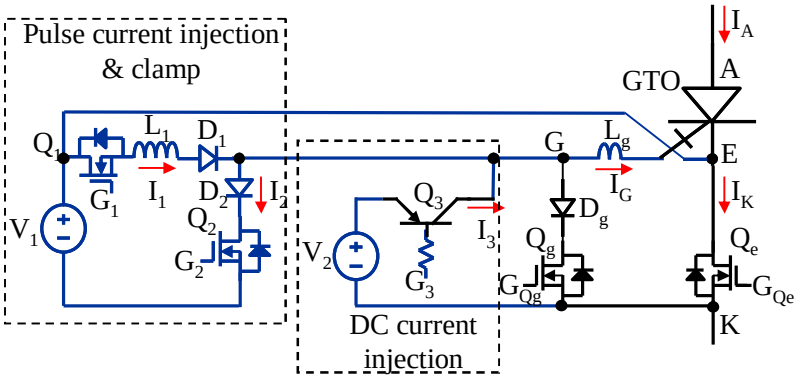


Fig. 2.9 The circuit diagram of the new generation ETO

To illustrate the work principle of the ETO, suppose ETO is working in a boost converter shown in Fig. 2.10. In this circuit, the ETO turn-on di/dt is limited by the di/dt snubber. There is no dv/dt snubber. A RCD clamp is used to limit the voltage spike during turn-off.

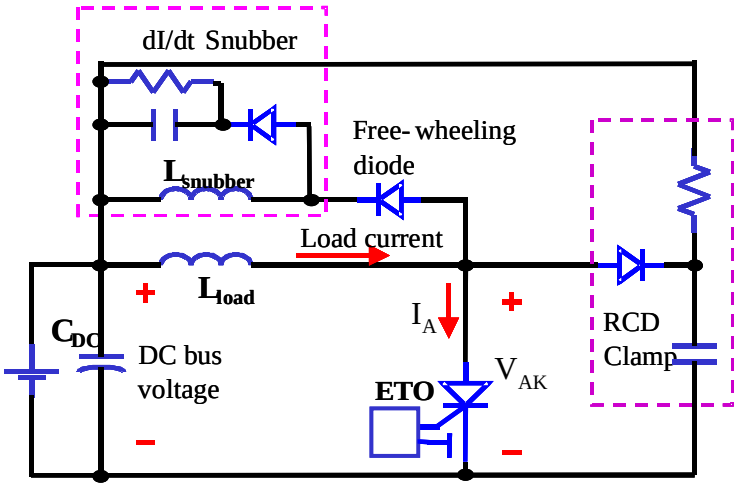


Fig. 2.10 A boost converter to test ETO

Fig. 2.11 shows the drawing of the operational waveforms during ETO turn-on and turn-off.

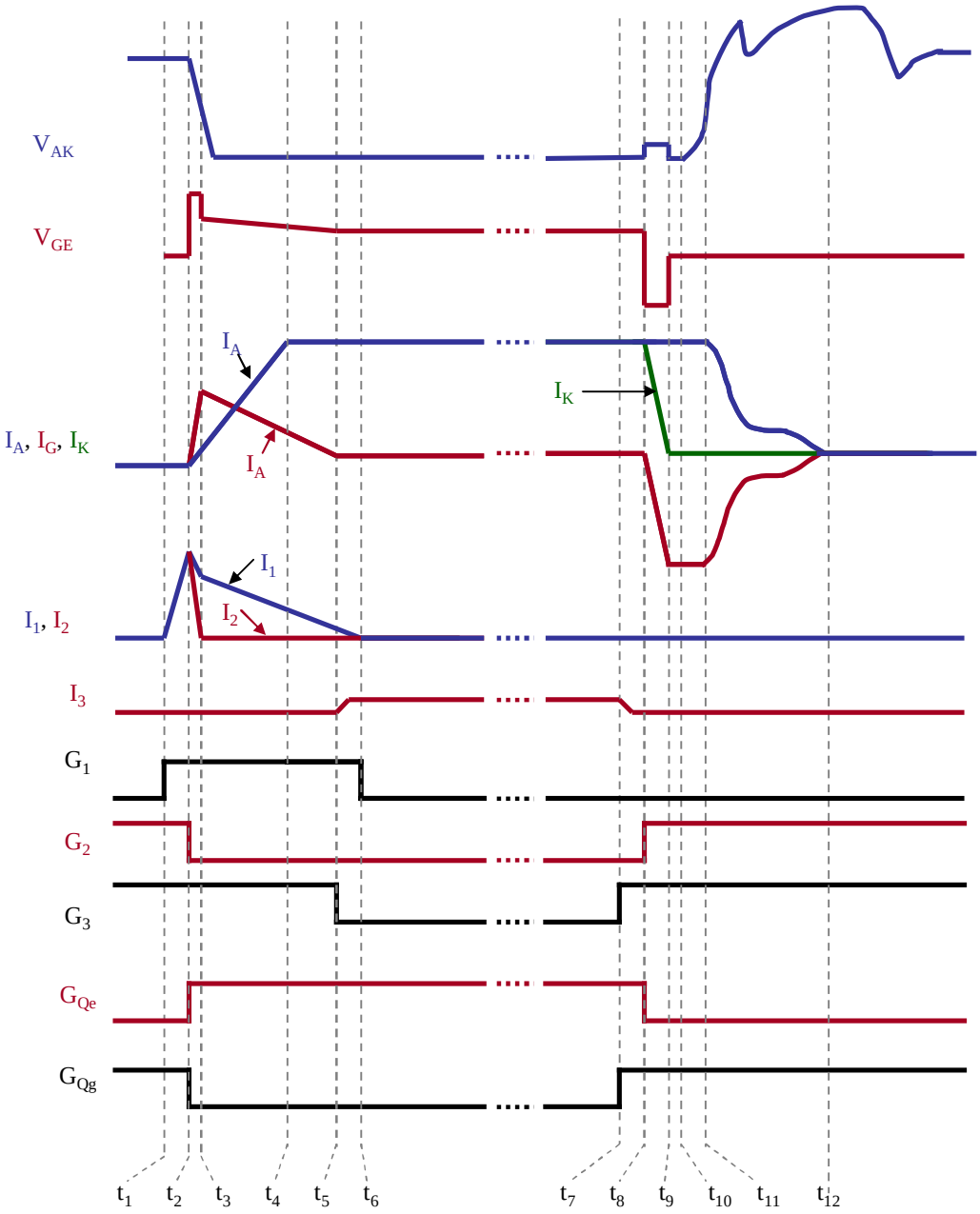


Fig. 2.11 The drawing of the operational waveforms during ETO turn-on and turn-off

As can be seen in Fig. 2.11, the turn-on and turn-off operation of the ETO consists of the following events.

Before t_1: The ETO is in off state before t_1. When ETO is in off-state, all the devices are off, except that Q_g and Q_2 are in on-state. Q_g is kept on to short the GTO's gate to ETO cathode, and Q_2 is kept on to reverse bias the GTO's gate-cathode junction. These approaches are used to prevent ETO from falsely triggering on by any kind of noise.

t_1-t_2: At time t_1, Q_1 is turned on. Since both Q_1 and Q_2 is on, V_1 is applied across L_1, I_1 and I_2 increase linearly (I_1 is equal to I_2), as shown in Fig. 2.12 (the bold drawing part of the circuit indicates that it is conducting current).

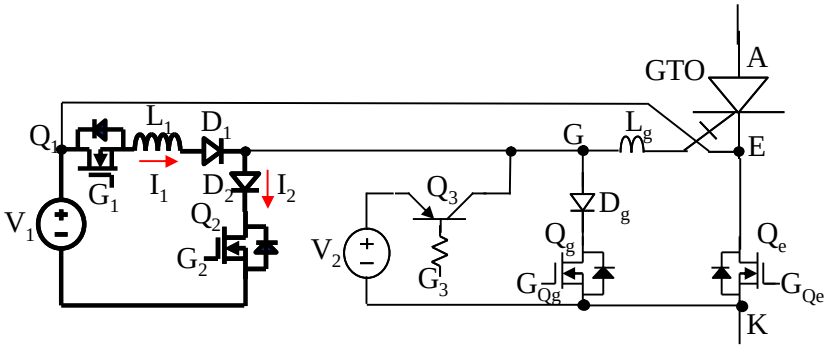


Fig. 2.12 The ETO operation from t_1 to t_2

t_2-t_5: When I_1 increases to the a desired value at time t_2, Q_2 is turned off, forcing the current I_1 to inject to the GTO's gate, and the GTO starts to turn on. Since now the inductor current I_1 has already built up, the di/dt of the gate current injection I_G can be extremely high, which is very important for the ETO's uniform turn-on [D 10]. At the same time, Q_g is turned off and Q_e is turned on. I_A and I_K start to increase, and ETO voltage V_{AK} drops very fast. At time t_3, I_2 decreases to zero, indicating that Q_2 is fully off and I_1 is equal to I_G from now on. The GTO gate injection current I_G is maintained by the energy stored in L_1. At time t_4, ETO current I_A is

increased to equal to the load current. ETO is fully on. The circuit operation during this period is shown in Fig. 2.13.

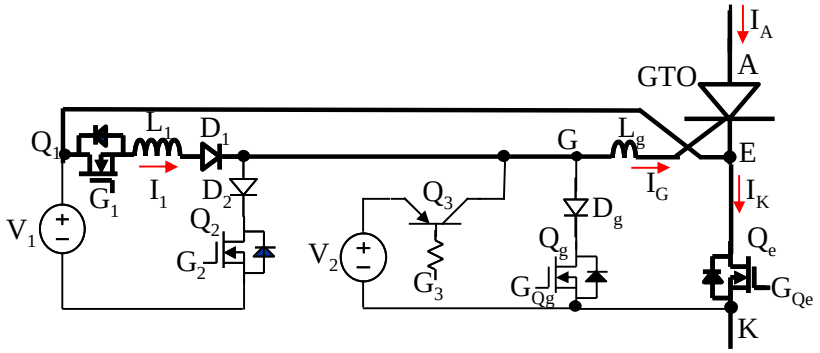


Fig. 2.13 The ETO operation from t_2 to t_5

t_5-t_7: At time t_5, I_G decreases to a very low value. Q_3 is turned on to supply a small DC current to GTO's gate, in order to ensure that the GTO remains in a low conduction loss state. At time t_5, I_G decreases to zero and Q_1 is turned off. The circuit operation during this period is shown in Fig. 2.14. The ETO is kept on until it is commanded to turn off at time t_7.

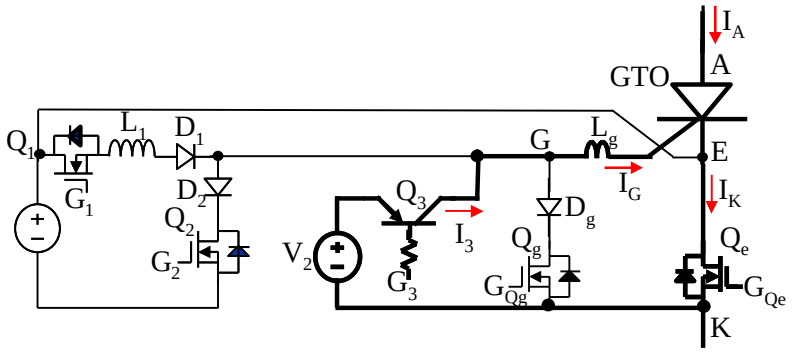


Fig. 2.14 The ETO operation from t_5 to t_7

t_7-t_8: At time t_7, Q_G is turned on and Q_3 is turned off to cut off the DC current injection. The ETO is ready to be turned off.

t_8-t_9: At time t_8, Q_e is turned off and Q_2 is turned on. The turn-off operation starts. Since Q_e is turned off and Q_g is on, there is a high voltage V_{EK} applies across the GTO's cathode-gate junction, forcing the cathode I_K divert to GTO's gate. V_{EK} can be as high as Q_e MOSFET's avalanche voltage. As a result, I_k starts to decrease and a negative I_G starts to increase in absolute value. The circuit operation during this period is shown in Fig. 2.15.

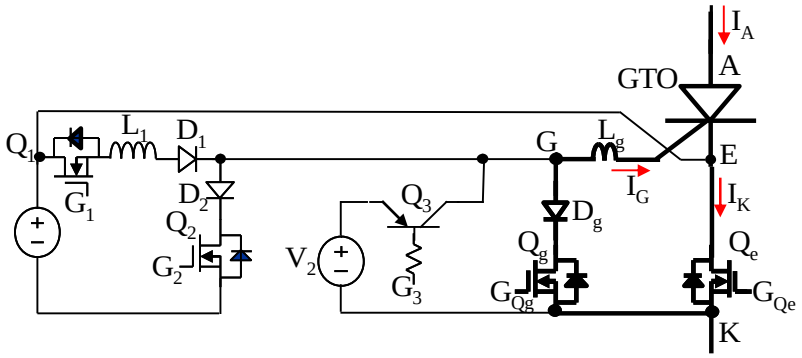


Fig. 2.15 The ETO operation from t_8 to t_9

t_9-t_{12}: At time t_9, I_K decreases to zero, and I_A is equal to negative I_G. ETO achieves so-called unity turn-off gain. The minority carriers in the P-based region of the GTO are pulled out by the negative gate current I_G until time t_{10} when the main junction J_2 is recovered. The storage time ends. From time t_{10}, the minority carriers in the n^- region are swept out while the voltage increases to the DC link voltage value at time t_{11}. Then the ETO current I_A starts to divert to the RCD clamp circuit and di/dt snubber (refer to Fig. 2.10). So I_A starts to decrease. I_A fails to its tail value rapidly and voltage spike appears due to the di/dt applied to stray inductances. Finally the anode voltage remains high while the anode current decreases slowly, determined

by the minority carrier recombination in the undepleted n^- region, and until at time t_{12}, I_A decreases to zero and ETO is fully off. . The circuit operation during this period is shown in Fig. 2.16.

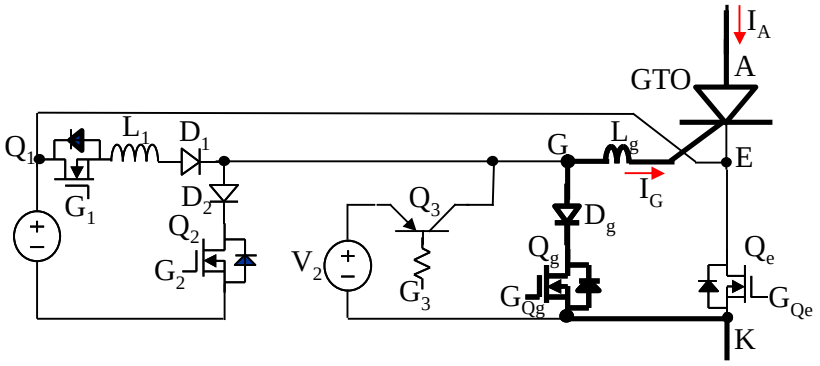


Fig. 2.16 The ETO operation from t_9 to t_{12}

An important improvement of the new generation ETO is that all the reverse current conduction path, which is from cathode of the ETO to the anode of the ETO, are blocked or limited. The reverse current through Q_g is blocked by D_g, and through the DC current injection circuit is limited by the PNP transistor Q_3. There is no reverse current path existing in the pulse current injection and clamp circuit. The abnormal failure issue caused by the GTO parasitic diode is solved.

2.4. The Experimental Demonstration of the New Generation ETO in the Boost Double Pulse Tester

2.4.1. Tester Set Up

According to the circuit schematic shown in Fig. 2.10, a boost converter was built to measure the characteristics and performance of the new generation ETO. In the test, the

ETO is initially off, and the high voltage capacitor bank C_{DC} is charged to the voltage at which the ETO will experience during switching. The double-pulse test which consists of two turn-on and turn-off events is adopted to test the ETO's switching characteristics. Fig. 2.18 shows the testing waveforms.

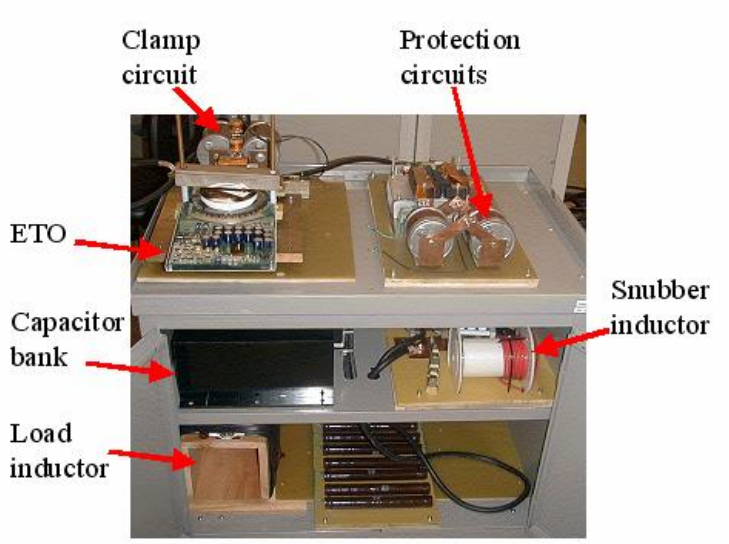


Fig. 2.17 The picture of the boost test converter for ETO

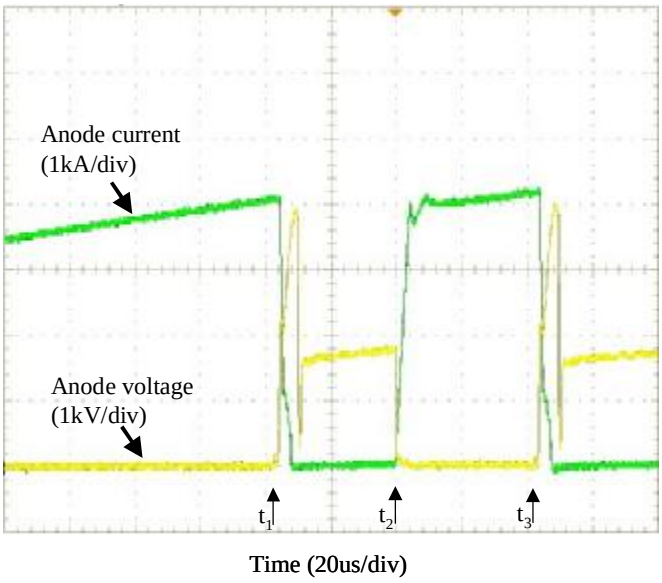


Fig. 2.18 The double pulses switching waveforms

As shown in Fig. 2.18, when the testing begins, the ETO is turned on and C_{DC} charges the load inductor L_{Load}. The anode current of the ETO increases linearly. When anode current reaches the desired value at t_1, the ETO is command to turn off. The total load current will still go through the ETO until its anode voltage reaches the bus voltage. Then the ETO's anode current begins to be commutated to the free-wheeling diode and the clamp circuit. The ETO will see a voltage spike due to the stray inductance of the circuits. However this spike is limited to a safe value by the clamp circuit. The ETO has the highest stress during the interval when the current and voltage are simultaneously high.

After the ETO's turn-off process ends, the ETO will block a voltage equal to the DC bus voltage. The current is still free-wheeling through the load inductor, the free-wheeling diode and the snubber inductor $L_{snubber}$. Then the ETO is turned on again at t_2 in order to test its turn on characteristic. Then the load current begins to commutate into the ETO from the free-wheeling diode. The di/dt snubber inductor $L_{snubber}$ determines the rate of current transfer. So by choosing the value of $L_{snubber}$, the desired turn-on di/dt of the ETO can be obtained for characterization of its turn-on performance. Shortly after the total current of the load inductor commutated into the ETO, the ETO is commanded to turn-off at t_3. Then the process of the double test ends.

2.4.2. The turn-off and turn-on performance

Fig. 2.19 shows the turn-off waveform of the ETO at 5000A load current and 2200V DC bus voltage without dv/dt snubber.

From the Fig. 2.19, it can be calculated that the maximum power P_{max} of the ETO during turn-off is about 12MW. The diameter of the effective area of the GTO wafer is about 8cm. So it can be calculated that from (2-2) the maximum power density during turn-off of the Gen-3 ETO reaches about:

$$\frac{P_{\max}}{p*(\frac{8cm}{2})^2} = 239 \cdot 10^5 W/cm^2 \qquad (2–2)$$

The current density reaches:

$$\frac{5000A}{p*(\frac{8cm}{2})^2} = 100A/cm^2 \qquad (2-3)$$

These data show that the ETO's Safe Operation Area (SOA) is basically enlarged to that of an open base PNP transistor and is only limited by the dynamic avalanche [B 24]. This test also shows that the ETO turn-off storage time is about 1.2μs, which is reduced to about one twentieth of that of GTO (25μs).

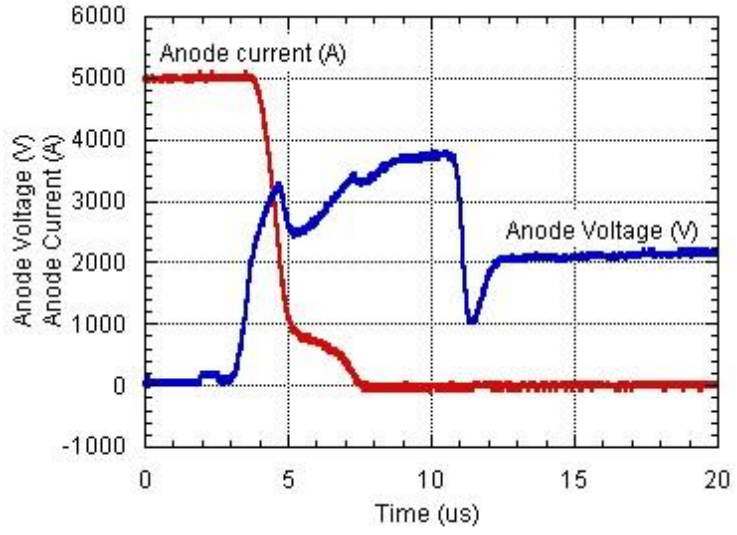


Fig. 2.19 The 5000V/2200A snubberless turn-off waveform of the ETO at Tj=25℃

Fig. 2.20 shows the turn-off waveform of the ETO at 4200A load current and 2500V DC bus voltage without dv/dt snubber.

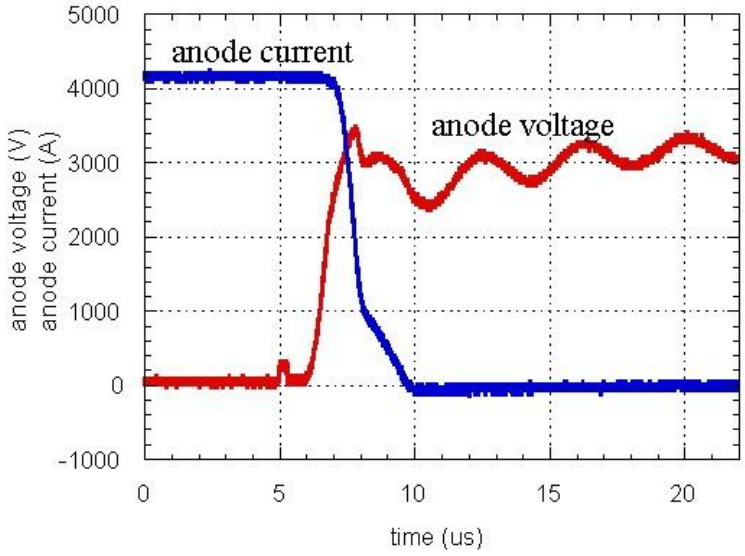


Fig. 2.20 The 4200A/2500V snubberless turn-off waveform of the ETO at Tj=25°C

Fig. 2.21 summarizes the turn-off switching loss of the ETO at 2000V DC bus voltage. These data can be used to calculate the ETO converter output capability.

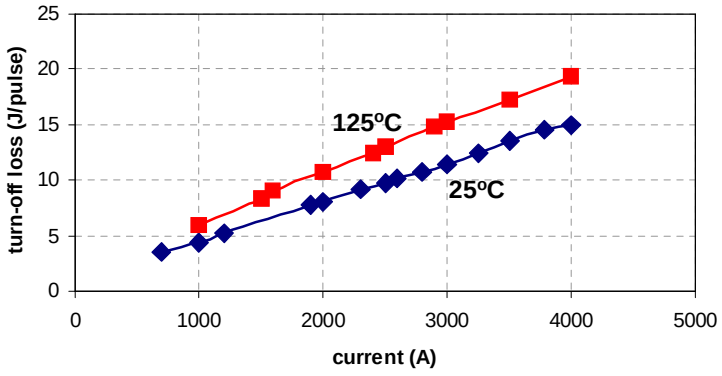


Fig. 2.21 The turn-off switching loss of the ETO

The new generation ETO has a relatively low inductance gate loop (about 15nH) due to its housing design. Combining low gate loop inductance with the improved turn-on circuit, the ETO can achieve the turn-on rising rate of gate current about 2000A/us. The peak current is controlled to be about 150A. The measurement result of the gate current injection is shown in Fig. 2.22. With such an efficient turn-on function, the anode current of the new generation ETO can safely be turn-on to 4000A with 1000A/us di/dt. Therefore the turn-on speed is greatly improved and the turn-on loss is also reduced. Fig. 2.23 shows the turn-on waveforms of the new generation ETO.

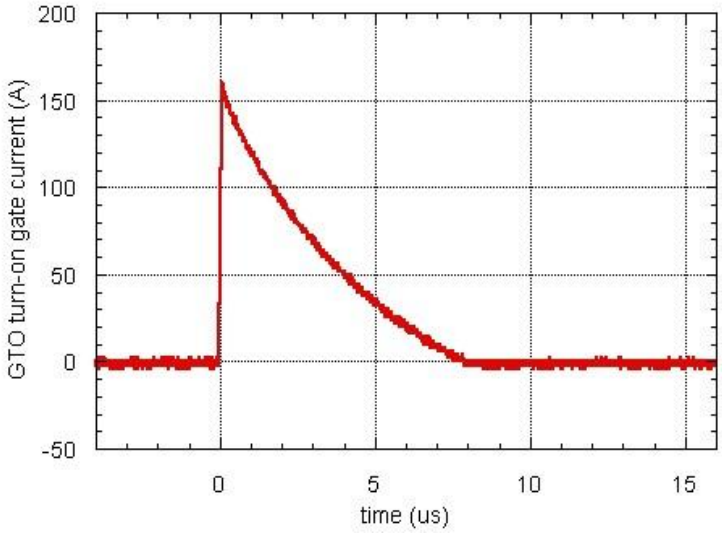


Fig. 2.22 The ETO turn-on pulse current injection

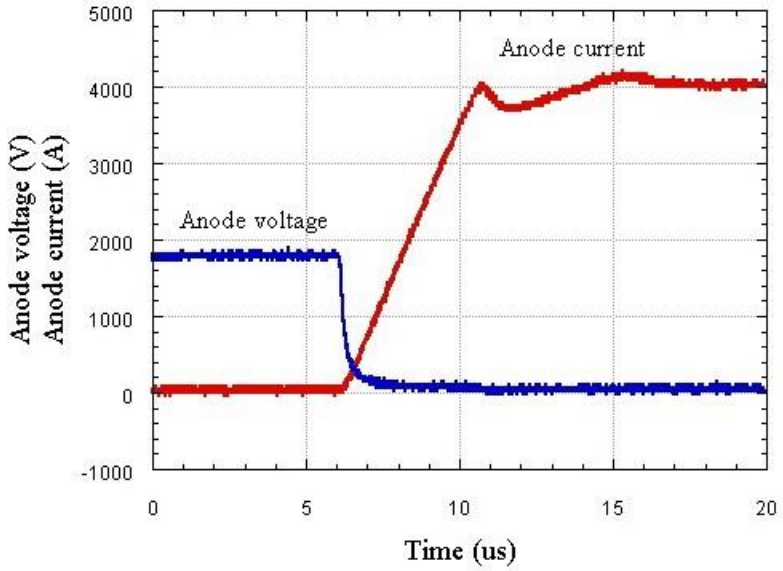


Fig. 2.23 The ETO turn-on waveforms

Although the ETO can be turned on at high di/dt [4], the di/dt is normally maintained at a relatively low value to keep the turning-off diode within its safe operating area. Taking ABB 5SDF 10H4502 diode [B 37] for example, its turn-off di/dt is limited to less than 650A/μs. Under low turn-on di/dt condition, the ETO's turn-on loss is very small.

2.4.3. On-state Characteristics

The on-state characteristics of the ETO were measured by discharging a charged capacitor through the ETO. Fig. 2.24 shows a typical ETO on-state characteristic test waveform.

Fig. 2.25 shows the on-state characteristics of the GTO used in the ETO. Fig. 2.26 shows the on-state characteristics of the emitter switch Q_e of the ETO. Fig. 2.27 shows the on-state characteristics of the ETO.

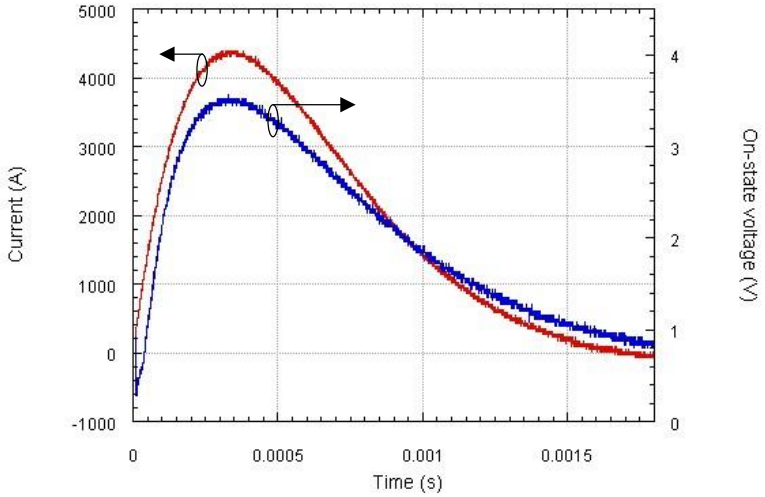


Fig. 2.24 The typical on-state characteristics test waveform of the ETO

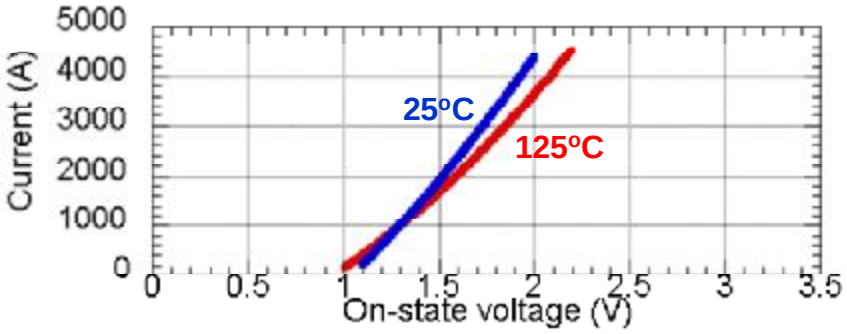


Fig. 2.25 The on-state characteristics of the GTO

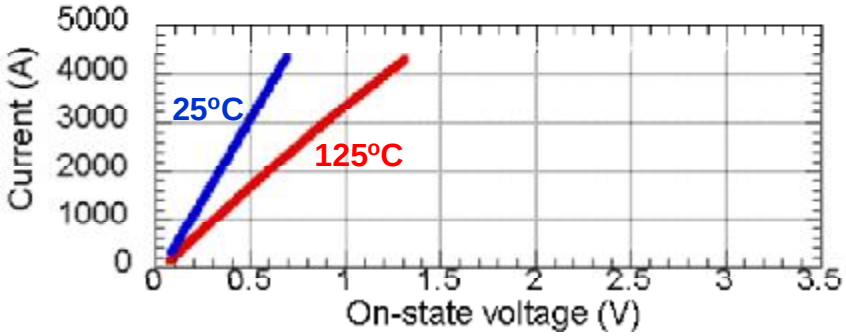


Fig. 2.26 The on-state characteristics of the emitter switch MOSFET's

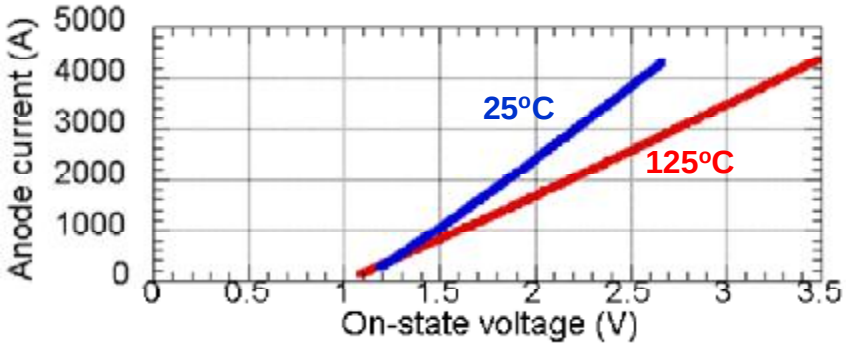


Fig. 2.27 The on-state characteristics of the ETO

From Fig. 2.25, Fig. 2.26, and Fig. 2.27, it can be seen that the ETO has more resistive I-V characteristic than that of the GTO. So ETO is better for current sharing in the parallel connection application than that of the GTO due to the resistive I-V characteristic of the emitter switch. Furthermore, the positive temperature coefficient I-V is very important to avoid the positive feedback of current crowding. Fig. 2.25 shows that the GTO tested has a positive temperature coefficient I-V above a critical current value (1200A). Due to the strong positive temperature coefficient of the emitter switch, the critical current value of the ETO moves much lower (below 300A) than that of the GTO. ETO also has a stronger positive temperature coefficient than that of the GTO. Combining with the much fast switch speed, the ETO has a highly improved performance in the parallel and series application than that of the GTO.

A summary of the rating and the characteristics of the new generation ETO are listed in Table 2.1.

Table 2.1 Main rating & characteristics of the new generation ETO

Parameters (operation at 2000V DC bus and 4000A anode current)	**Ratings & Characteristics**
Repetitive peak off-state voltage	4500 V
On-state voltage	3.3 V
Rate of rise of on-state current	1000A/us
Risig rate of gate current during turn-on	2000A/us
Turn-on delay time	3us
Turn-on Rise time	0.4us
Turn-on loss per pulse	0.38J
Peak on gate current	200A
DC on gate current	3A
Snubberless turn-off current	5000A
Storage time	1.4us
Turn-off delay time	4us
Turn-off Fall time	0.8us
Rising rate of gate current during turn-off	7000A/us
Turn-off loss per pulse	13.5J

2.5. The High Frequency Multi-Pulses Sequence Snubberless Testing

To demonstrate ETO's transient thermal handling capability, a 10 kHz 12-pulse sequence snubberless switching test was conducted. Fig. 2.28 shows the anode voltage, anode current, and the ETO loss waveforms of the test results. The DC link voltage is 2500V, and the switching current rises from 1000A to 4000A. The duty cycle of the pulse

sequence is 50% (50μs on and 50μsoff). The power loss, mainly caused by the snubberless turn-off, reaches 130J at the end of the last pulse.

For the traditional GTO, its minimum on-time and off-time is long due to its non-uniform current distribution during switching. The non-uniform current distribution can cause non-uniform temperature distribution, leading to hot spots and thermal runaway [B 41]. ETO achieves the uniform current distribution during switching through its unity gain turn-off. The heat generated during the switching is evenly distributed across the ETO. In addition, the transient thermal impedance of the ETO is very low in short time pulses, therefore, ETO can endure very high power in a short time period without causing its junction temperature to exceed the safe operation area. In the test shown in Fig. 2.28, 130J was generated within 1ms and did not destroy the ETO due to the ETO's even thermal distribution and low transient thermal impedance. This capability sets a large safety margin during ETO's normal operation condition, and is very important for ETO when working at over-load and fault condition. This test shows that the ETO's switching frequency is limited by the thermal handling capability of the package, rather than by the electrical capability. The ETO can operate at extremely high power and in high frequency condition as long as the heat can be removed.

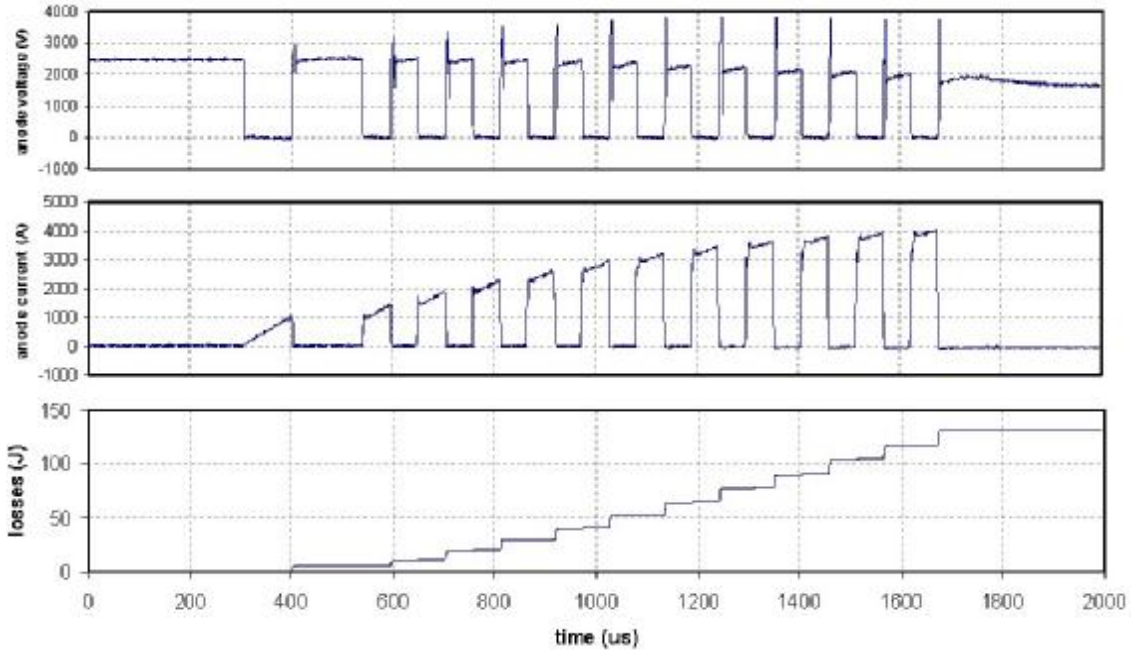


Fig. 2.28 The 10kHz, 12-pulse sequence test results of the ETO at T_j=25°C

2.6. The Experimental Demonstration of the High Power, High Frequency Operation of the ETO

2.6.1. ETO Phase Leg Output Capability Determination

The ETO converter's power handling capability is greatly determined by the characteristics of the ETO being used. Based on ETO's switching loss, conduction loss, thermal impedance, and the system's thermal dissipation, the ETO phase leg's output current and output power capabilities can be calculated, which is important to indicate the ETO's actual power handling capability for practical applications.

The ETO's junction to case thermal impedance with double side cooling is about 12.6K/kW, and the case to heat sink thermal impedance with double side cooling is about 2.5K/kW. The heat sink to cooling water thermal impedance is determined by the thermal

impedance of the heat sink and the flowing rate of the cooling water. In our test, the temperature of the cooling water is about 55 ^{o}C. The heat sink to water thermal impedance is about 5.5K/kW. Assuming the ETO junction temperature is 125^{o}C, and then the allowable power dissipation of each ETO, P_{max}, is about 3.4kW.

From the test results shown in Fig. 2.21, one can express the turn-off loss using equation (2-4) at 125^{o}C junction temperature, and 2000V DC bus voltage.

$$E_{off}(I) = 0.00444 \cdot I + 1.81 \qquad (2\text{-}4)$$

From the test results shown in Fig. 2.27, one can get the ETO's on-state voltage equation (2-5) at 125^{o}C junction temperature.

$$V_{on}(I) = 0.00057 \cdot I + 1.03 \qquad (2\text{-}5)$$

Suppose the ETO converter has a sinusoidal output, and each ETO only works for half a cycle: the current flows through an ETO for half cycle and the ETO current is zero for the other half a cycle. The ETO turn-on loss is neglected since it is very small compared with the turn-off loss. Then the switching loss of the ETO is given by (2-6).

$$P_{sw}(I_{pk}) = f_{sw} \cdot \frac{1}{2p} \int_0^p E_{off}(I(a))da \qquad (2\text{-}6)$$

Where f_{sw} is the switching frequency;

$$I(a) = I_{pk} \cdot \sin(a) \qquad (2\text{-}7)$$

The switching duty cycle of the ETO is given by the following expression:

$$D(a) = \frac{1}{2} \cdot [1 + M \cdot \sin(a + j)] \qquad (2\text{-}8)$$

Where M is the modulation depth; a is the angle within the sine wave; j is the angle of the load impedance. Then the conduction loss is given by (2-9).

$$P_{cond}(I_{pk}) = \frac{1}{2p} \cdot \int_0^p I(a) \cdot V_{on}(I(a)) D(a) \cdot da \qquad (2\text{-}9)$$

The total power dissipation on the ETO is:

$$P_{loss}(I_{pk}) = P_{cond}(I_{pk}) + P_{sw}(I_{pk}) < P_{\max} \qquad (2\text{-}10)$$

We can assume M=0.9, and j =0, in the situation when the highest conduction loss occurs. Based on (2-4)-(2-10), the ETO output RMS current as a function of the switching frequency can be calculated, and the result is shown in Fig. 2.29.

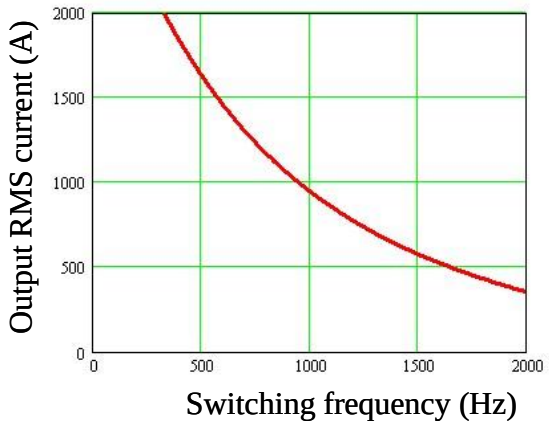


Fig. 2.29 The ETO output current versus frequency

In this calculation, the DC link voltage is 2000V, the maximum peak output voltage of the fundamental frequency is given by (2-11), and the maximum RMS output voltage is given by (2-12).

$$V_{out\_peak} = V_{dc} \cdot M = 1800V \qquad (2\text{-}11)$$

$$V_{out\_RMS} = \frac{V_{out\_peak}}{\sqrt{2}} = 1273V \qquad (2\text{-}12)$$

The output power of an ETO H-bridge phase leg is:

$$S_{out\_RMS}(f_{sw}) = V_{out\_RMS} \cdot I_{out\_RMS}(f_{sw}) \qquad (2\text{-}13)$$

(2-13) is plotted and shown as Fig. 2.30.

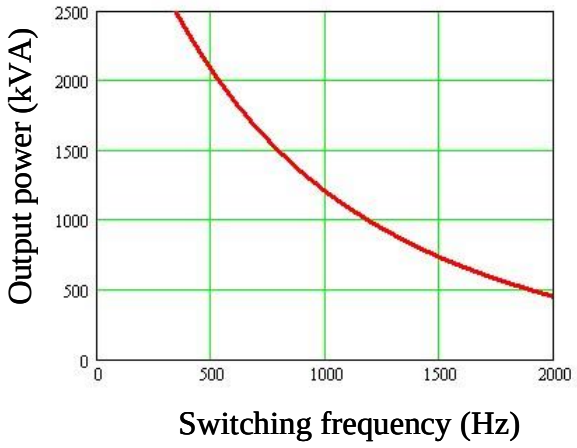


Fig. 2.30 The ETO phase output power versus frequency

2.6.2. The ETO H-Bridge Converter

Based on the calculation above, an ETO based H-bridge voltage source converter is built and tested. Fig. 2.31 shows the schematic of the converter system. Fig. 2.32 shows the picture of the H-bridge converter. The input cap bank C_{dc} is built using seven paralleled film capacitors, the rating of each is 850uF, 2.5kV, and 740 A_{RMS}. The load is built using three paralleled adjustable water-cooling inductors. The pictures of the input cap bank and the load are shown in Fig. 2.33.

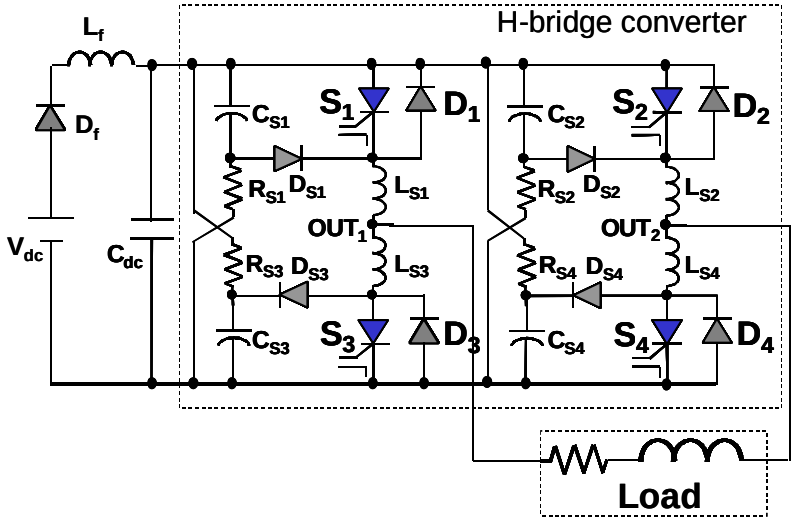


Fig. 2.31 The schematic of the ETO based H-bridge voltage source converter system

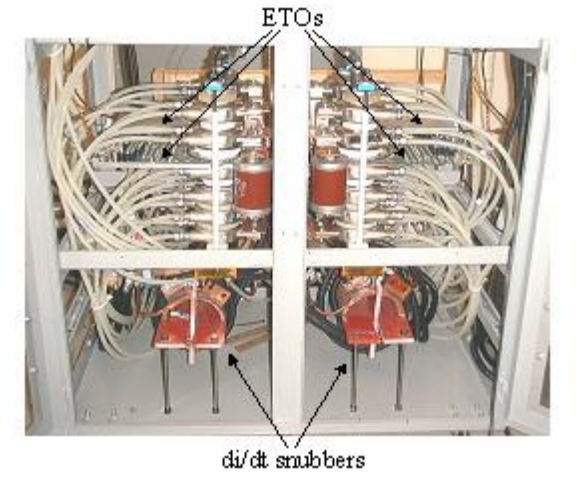


Fig. 2.32 The picture of the ETO based H-bridge converter

(a) (b)

Fig. 2.33 The picture of the passive components: (a) input cap bank and (b) inductive load

Table 2.2 summarizes the parameters of the ETO based H-bridge voltage source converter.

Fig. 2.34 shows the test results. The output current peak value is about 1400A, and the RMS value is about 1000A. The output power of the H-bridge is about 1.2MVA.

Table 2.2 The parameters of the ETO converter

The components of the converter	The parameters of the components
Main switch	ETO
Anti-parrallal diodes D_1- D_4	ABB 5SDF 10H4502
Snubber diodes Ds_1- Ds_4	ABB 5SDF 10H4502
V_{dc}	2000 V
Snubber inductors L_{s1}- L_{s4}	3.5 μH
Clamp resistors R_{s1}- R_{s4}	0.5 Ohm
Clamp capacitors C_{s1}- C_{s4}	1.5 μF

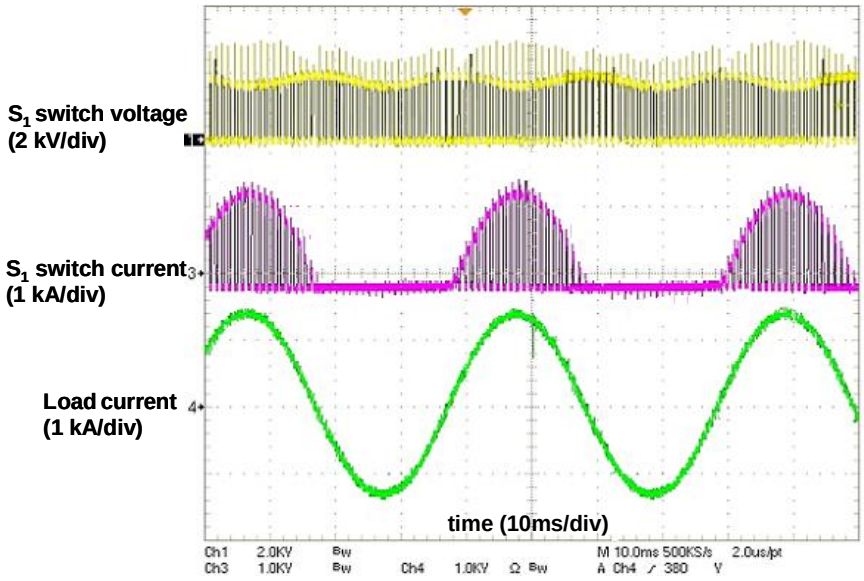


Fig. 2.34 The test results of the ETO based H-bridge voltage source converter

2.7. Conclusions

This chapter presents the design, analysis, and experimental demonstration of the new generation ETO. The new generation ETO has high performance, high reliability, and high manufacturability.

ETO's homogenous switching due to the unity turn-off gain and high turn-off gate current rising rate enlarges the SOA to full dynamic avalanche, and enables the ETO to operate at extremely high power and high frequency conditions as long as its junction temperature is kept at a safe value. The ETO's switching frequency is limited by the thermal dissipation, rather than the electrical capability. ETO's short turn-off storage time, high turn-on di/dt capability, low switching and conduction losses, and the low gate drive unit power consumption allow the ETO converter to operate at much higher power and higher frequency than that of the traditional GTO. Since the di/dt snubber is greatly reduced, the dv/dt snubber is not required, and the power consumption of the gate drive is very low, the system's cost can be significantly reduced, and the reliability can be greatly improved. ETO's high power high frequency operation is successfully demonstrated in a megawatt H-bridge voltage source converter.

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Chapter 3. The Innovative Self-Power Generation Method of the ETO

This chapter presents the design and experimental demonstration of the innovative self-power generation function of the ETO. Different from the conventional high power devices which require the external power input for their gate drivers, ETO achieves complete optically controlled turn-on and turn-off and all the internal power required is self-generated. ETO has a simple and low power loss circuit to get its start-up power. ETO obtains power for gate drive through its turn-on operation. This chapter also introduces a novel gate drive circuit to realize unnecessary turn-on suppression to minimize the gate drive power loss for ETO. ETO greatly reduces the cost and increase the reliability of the power converters since no external power supply for device gate drive is required.

3.1. Introduction

The conventional high power semiconductor device requires the external power input for its gate driver. In the voltage source converter applications, the external power supplies for the device gate drivers need to be individually designed. The power for each device gate driver is normally provided from low voltage potential (normally ground potential). The insulation transformer is required to deliver the power to the device gate driver which is at the different voltage potential. In a high voltage converter, the insulation transformer has a large size and it is often difficult to implement the reliable

insulation design. These external power supplies for the gate drivers increase the cost and reduce the reliability of the total system.

Several gate drive power supply methods [E 5], [E 6], [E 7] by which the gate drive power is not provided from the low voltage potential through insulation transformer are proposed. However, each of these methods obtains the gate drive power through the dv/dt snubber circuit, and has low efficiency. A typical implementation of such methods is shown in Fig. 3.1. The power supplies for the gate drives need to be individually designed according to the operation voltage and switching frequency of the device. For the high power converters using the hard-driven GTO devices such as IGCT's and ETO's, the dv/dt snubbers are not required and these methods are difficult to apply.

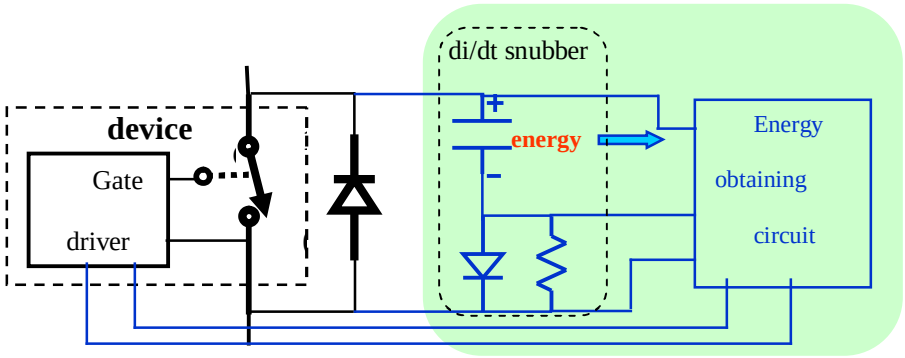


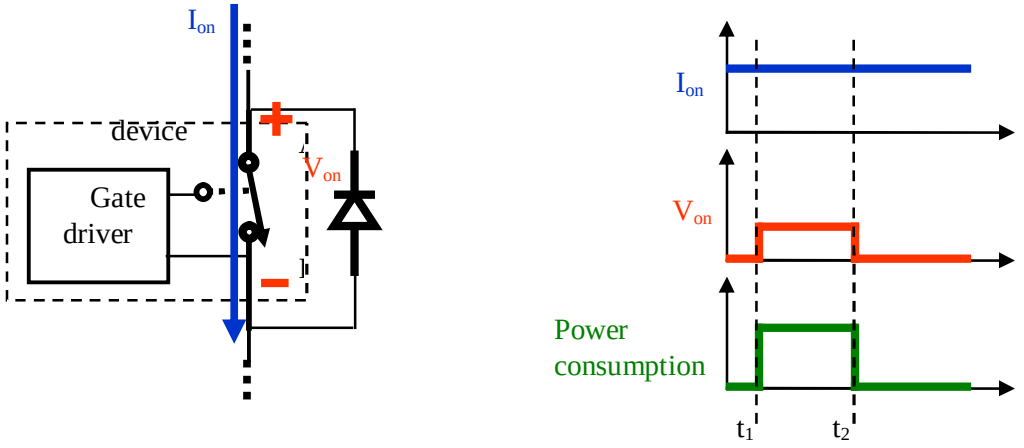
Fig. 3.1 A typical implementation to get gate drive power through dv/dt snubber

In this chapter, a novel self-power generate method is proposed. Different from the conventional high power devices which require the external power input for their gate drivers, ETO achieves complete optically controlled turn-on and turn-off, and all the internal power required is self-generated.

3.2. Design and Operation Modes of the Self-Power Generation Method

3.2.1. Novel Method to Get Power for Device Gate Drive

A new method to get power for device gate drive is proposed, as shown in Fig. 3.2. When a device is in on-state, there is current going through the device and the voltage drop is low. If the voltage drop of the device can be increased in a controllable period, there will be controllable large power dump on the device. As shown in Fig. 3.2 (b), at beginning, I_{on} is large, and the device's voltage drop V_{on} is low. When V_{on} increases at t_1, the power consumption on the device increases. The idea is that if the power can be collected and stored power in a capacitor, this energy can be high enough for gate drive. When enough power is obtained, the device changes back to a low voltage drop. Then the device behavior likes a normal device.



(a) (b)

Fig. 3.2 Novel method to get power for device gate drive: (a) the circuit diagram and (b) operation waveforms

Fig. 3.3 shows the implementation of such method into the ETO, where there is a diode and capacitor across the emitter switch. Normally, in the on-state, both the GTO and Q_e switch are on, the current goes through both the devices, and the total voltage drop is very low. To get power, the emitter switch is turned off but the GTO is kept on, then the current will charge the capacitor. When the capacitor receives enough power, the emitter switch turns on again. Compared to the converter DC-link voltage, the voltage across the capacitor is designed to be very small. Then the ETO behaves like increasing a little bit voltage drop, then the voltage drop changes back as it is before the increasing.

This method has many advantages. Firstly, high voltage is blocked by GTO, so there is no high voltage across Q_e and C_1. Second, the grounds of the DC-DC converter and ETO are shared, so DC-DC converter is easy to design. Third, the energy to charge C_1 is easily controlled by controlling the off time of Q_e. Fourth, voltage across Q_e is clamped to controllable voltage, so that the emitter switch Q_e is prevented from avalanche break down, which is favorable to the device's long term reliability.

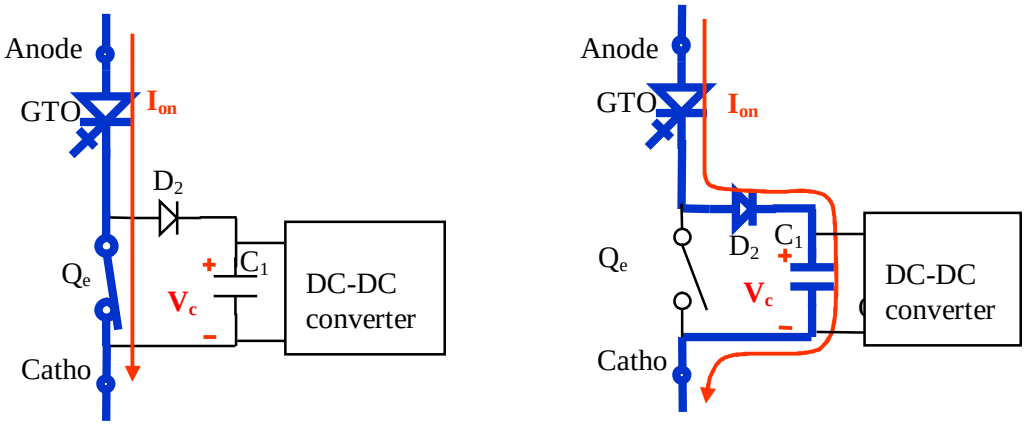
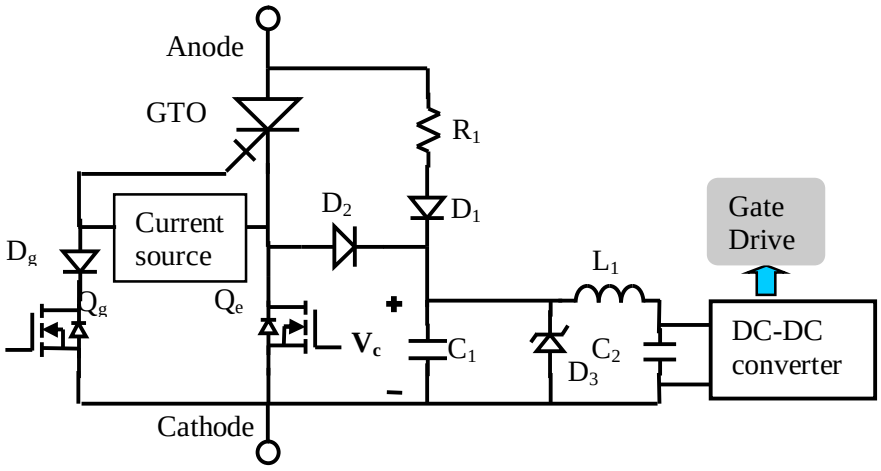


Fig. 3.3 The implementation of the method in the ETO: (a) normal on state mode and (b) power obtaining mode.

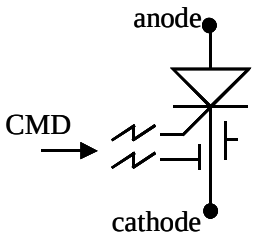
3.2.2. Design and Package

Fig. 3.4 shows the circuit diagram and circuit symbol of the ETO with the self-power generation function. R_1, L_1, $C_{1\text{-}2}$, and $D_{1\text{-}3}$ are used to obtain power and store the energy into cap bank C_1. Then the power from C_1 is supplied to the input of a DC-DC converter. The DC-DC converter generates the power for the internal control and gate drive of ETO. ETO does not require the external power input for gate drive. Turn-on and Turn-off commands to the ETO are transferred through an optical fiber. Based on such implementation, ETO can be seen as a two electrical terminal device with an optical command input (CMD) as shown in Fig. 3.4 (b).

Fig. 2 shows the picture of the ETO. Fig. 3 shows the cross section of the ETO, indicating the various components of the integrated device. The ETO utilizes double side press-pack cooling package and achieves small thermal resistance. The power resistor R_1 is put on the bottom copper, so that the heat of the R_1 is easily transferred to the heat sink.



(a)



(b)

Fig. 3.4 The Circuit of the ETO with the self-power generation function: (a) The circuit diagram of ETO and (b) The circuit symbol of ETO.

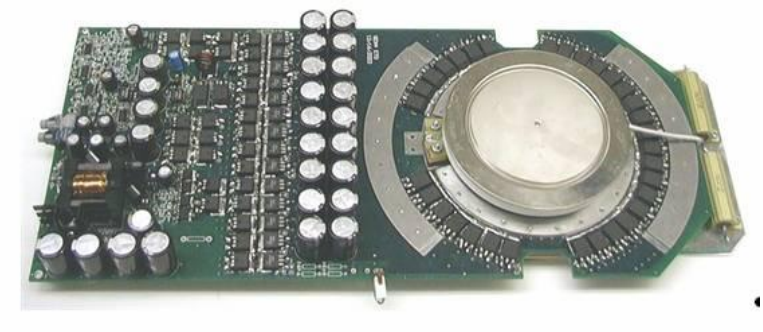


Fig. 3.5 The picture of the ETO.

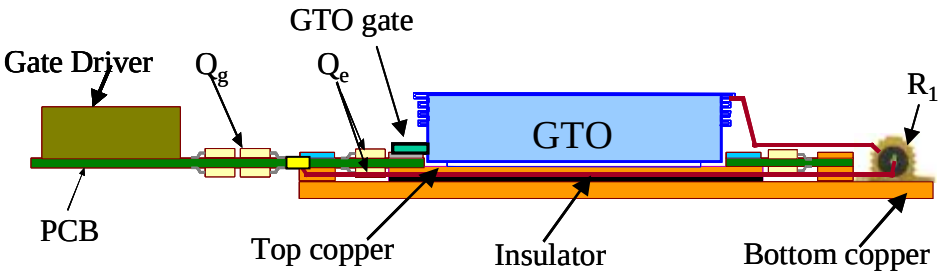


Fig. 3.6 The cross section of the ETO.

3.2.3. Three operation modes of ETO with the self-power generation function

When ETO works in a PWM voltage source converter, it has three operation modes: start up mode, active switching mode, and inactive switching mode. Fig. 3.7 shows a two level voltage source converter phase leg. ETO_p and ETO_n are the upper switch and the lower switch respectively of the phase leg.

Fig. 3.7 shows that the ETO's are working at start up mode. ETO's work at start up mode when the converter is first powered on. In this mode, both ETO_p and ETO_n are in off state. The DC-link voltage rises gradually from zero to the rated voltage.

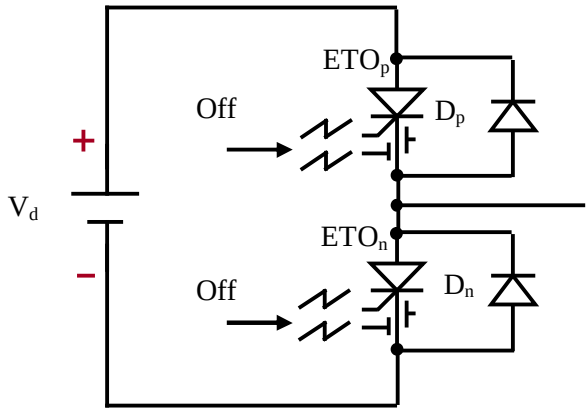
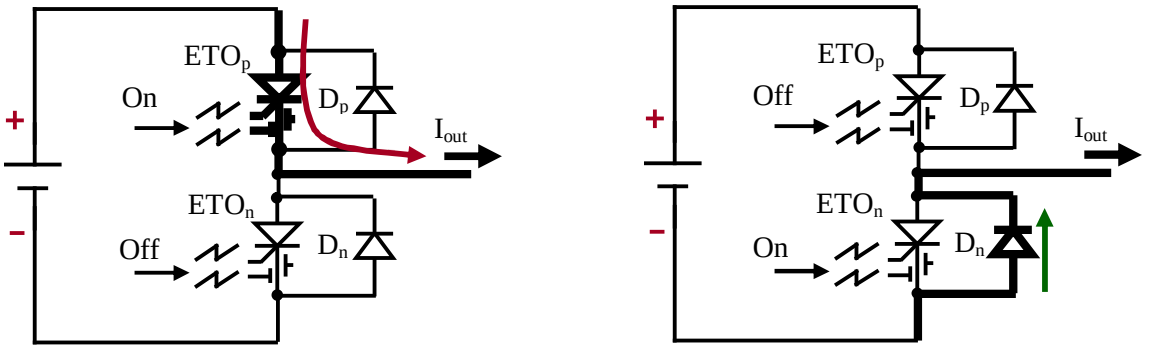


Fig. 3.7 The ETO's work at start up mode

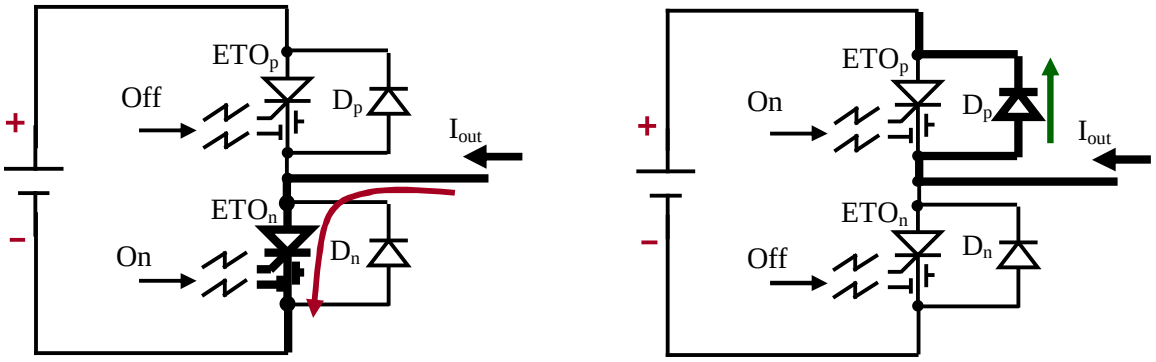
Assuming the output current I_{out} of the phase leg is positive when it flows out of the phase leg. When I_{out} is positive, the upper switch ETO_p works in the active switching mode as shown in Fig. 3.8. From Fig. 3.8 it can be seen that I_{out} will flow through ETO_p if ETO_p is on and ETO_n is off; I_{out} will flow through D_n if ETO_p is off and ETO_n is on.



(a) (b)

Fig. 3.8 The ETO_p works in active switching mode: (a) ETO_p is on; ETO_n is off and (b) ETO_p is off; ETO_n is on.

When I_{out} is negative, the upper switch ETO_p works in the inactive switching mode as shown in Fig. 3.9. From Fig. 3.9 it can be seen that, I_{out} will flow through ETO_n if ETO_p is off and ETO_n is on; I_{out} will flow through D_p if ETO_p is on and ETO_n is off. It can be known that I_{out} will never flow through ETO_p when it works in the inactive mode, no matter ETO_p is on or off.



(a) (b)

Fig. 3.9 The ETO_p works in inactive switching mode: (a) ETO_p is off; ETO_n is on and (b) ETO_p is on; ETO_n is off.

The lower switch ETO_n has the same working principle as that of the ETO_p. When I_{out} is negative, ETO_n works in the active switching mode. When I_{out} is positive, ETO_n works in the active switching mode.

Fig. 3.10 shows the summary of the three working mode waveforms of the upper ETO S_p.

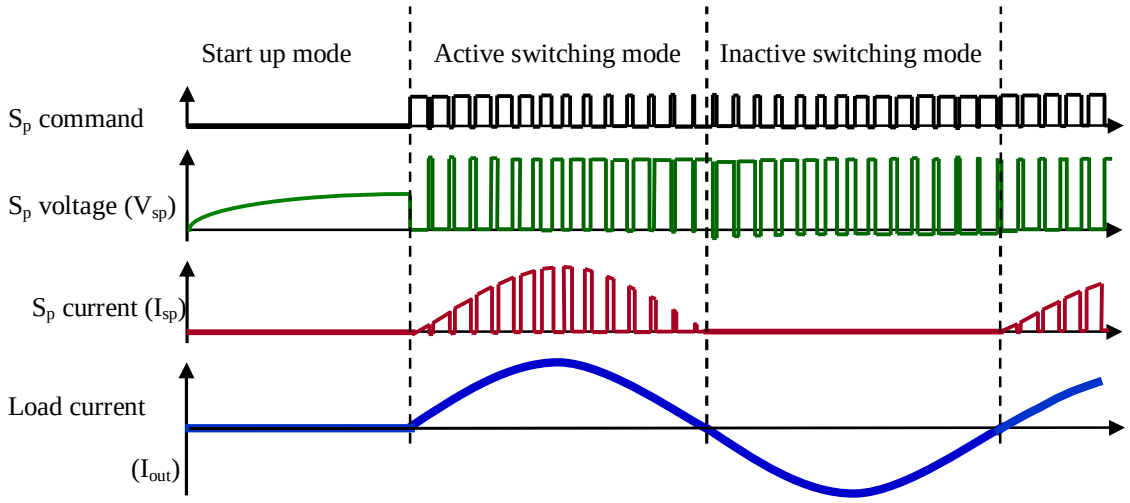


Fig. 3.10 A summary of the three working mode waveforms of the ETO

3.2.4. The power consumption of ETO in off state and during switching

The power consumptions of ETO in off state and during switching are quite different. During off state (no switching), the power consumption of the ETO is its control IC's quiescent power consumption.

When the ETO is commanded to turn on, the emitter switch MOSFET's are turned on and the gate switch MOSFET's are turned off. At the same time, a firing current pulse is injected into the GTO's gate by a current source to turn on the GTO. While the ETO is on, a small DC current is provided for the GTO's gate. When the ETO is commanded to

turn off, the emitter switch MOSFET's are turned off and the gate switch MOSFET's are turned on. During switching, current pulse injection, MOSFET's gate drive, and DC current injection will consume power. The power consumptions of current pulse injection and MOSFET's gate drive are also proportional to the switching frequency.

Fig. 3.11 shows the power consumptions of ETO in off state and during switching at different frequencies. In Fig. 3.11, P_GTO_DC denotes ETO's DC current injection power consumption. P_GTO_pulse denotes ETO's pulse current injection power consumption. P_MOSFET denotes ETO's MOSFET's gate drive power consumption. It can bee seen that ETO's gate drive power consumption in off state is very small (below 0.5W). ETO's gate drive power consumption increases dramatically from off state to switching state and also increases with the switching frequency.

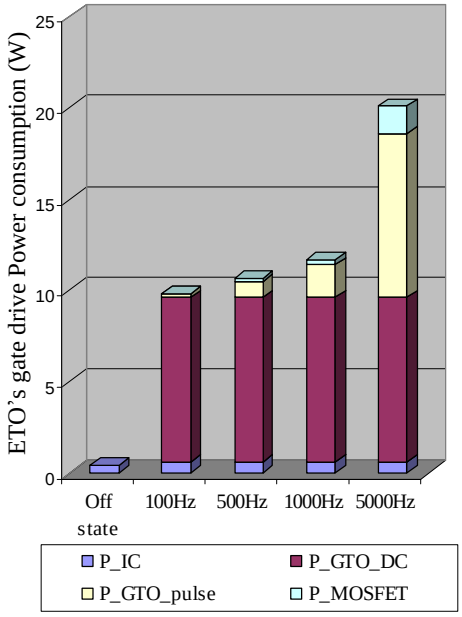


Fig. 3.11 The ETO's gate drive power consumptions in off state and during switching at different frequencies

In the following sections, ETO's operation principle and experimental results in three working modes is described.

3.3. The Operation Principle and Implementation of the ETO in Start-Up Mode

At power up of the ETO, the power for gate drive is received through R_1 by the ETO's anode voltage V_{anode}, as shown in Fig. 3.12 (the circuits with the bold line indicating current flowing). The charge current I_{c1} charges capacitor bank C_1 and then provides the power input to the DC-DC converter through filter L_1 and C_2. The power that is delivered to DC-DC by R_1 is expressed by (3-1).

$$P_1 = V_c \cdot \frac{(V_{anode} - V_c)}{R_1} \qquad (3\text{–}1)$$

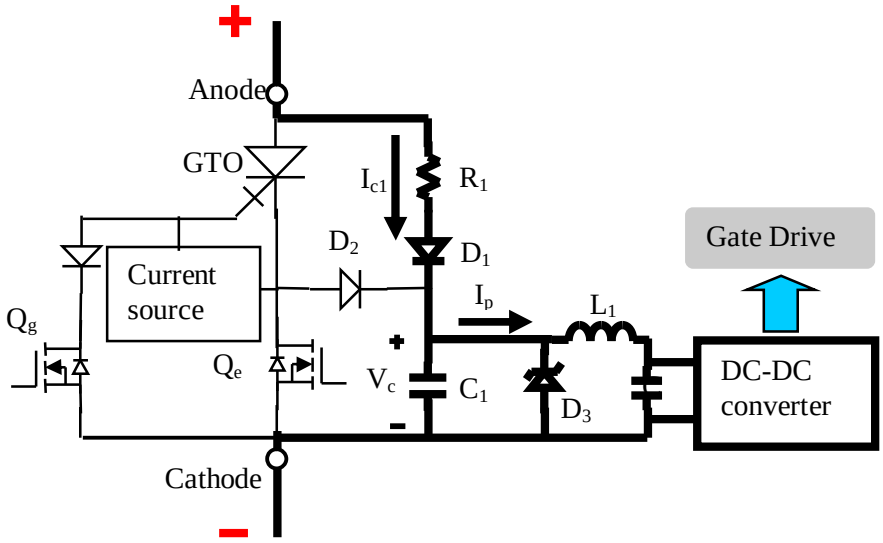


Fig. 3.12 The start-up operation of the ETO

From (3-1), it can be known that the higher V_{anode} the more power can be obtained by the DC-DC converter, and at a given V_{anode}, the maximum power can be obtained by DC-DC converter when

$$V_c = \frac{V_{anode}}{2} \qquad (3\text{–}2)$$

During start up, ETO works at off state. From Fig. 3.11 it can be known that the ETO's gate drive power consumption P_1 is less than 0.5W. The minimum V_{anode} for the ETO to get enough power for start-up is set at 500V. A DC-DC converter with line under-voltage detection function (UV) is designed for the DC-DC. At power up, UV keeps DC-DC converter off until V_c reach the under-voltage threshold, which is set at 250V according to (3-2). Then from (3-1), the value of R_1 is designed to be 125 kΩ.

Once DC-DC converter powers up, UV is disabled to extend input voltage operation range: DC-DC can still work even when V_c drops to 20V. A zener diode D_3 is used to limit the V_c to be below 300V.

Suppose the ETO's maximum anode voltage during operation is 2800V. The maximum power consumption of R_1 is about 24W. R_1 is mounted at the heat sink of ETO as shown in Fig. 3.6. The capability of the water cooling system for each ETO is normally designed around several kilo-watts. So R_1 adds only a very small burden to ETO's cooling system.

3.4. The Operation Principle and Experimental Demonstration of the ETO in Active Switching Mode

3.4.1. The Operation Principle

The power consumption of the gate driver of the ETO is much larger during switching operation as shown in Fig. 3.11. Apparently, the power obtained through R_1 is not enough to support ETO's gate drive power consumption in switching mode. Then V_c, the voltage of the capacitor bank C_1, will gradually decrease during the ETO's switching. Another method was proposed to maintain V_c to a certain range. The objective of the method is to control V_c to be between V_{ref1} and V_{ref2}:

$$V_{ref1} < V_c < V_{ref2} \qquad (3\text{–}3)$$

V_c is constantly monitored by the control circuit. When the ETO is commanded to turn-on, the gate switch Q_g is turned off, and a firing pulse I_{g_on} is injected into the GTO's gate by a current source and the GTO is turned on. At the same time, the control circuit will check V_c.

If V_c is lower than V_{ref1}, the ETO will enter into the charging turn-on mode, as shown in Fig. 3.13. Supposing ETO is commanded to turn on at t_1, the turn-on of Q_e will be delayed. Since GTO is turned on and Q_e is still off, the GTO current I_a will be forced to charge capacitor bank C_1 through D_2, as shown in Fig. 3.13 (a). As a result, V_c will increase, as shown in Fig. 3.13 (c). The V_c increasing rate is depended on both I_a and the capacitance of C_1. When V_c increases to V_{ref2} at t_2, Q_e is turned on, D_2 is reverse biased and I_a will be diverted to Q_e from D_2, as shown in Fig. 3.13 (b). Then V_c stops increasing,

and the input power of DC-DC is provided by the energy stored in C_1, as shown in Fig. 3.13 (c).

If V_c is higher than V_{ref1} when the ETO is commanded to turn on, Q_e will be turned on immediately. The ETO operation will directly goes to Fig. 3.13 (b), and the operation shown in Fig. 3.13 (a) will be bypassed. C_1 is a large capacitor bank and it can store a large amount of energy. Once it is charged to or above V_{ref2}, the energy stored in C_1 is large enough to maintain the gate drive power of ETO for a fairly long time before V_c is discharged to V_{ref1}. The operation shown in Fig. 3.13 (a) happens once in several thousand switching cycles.

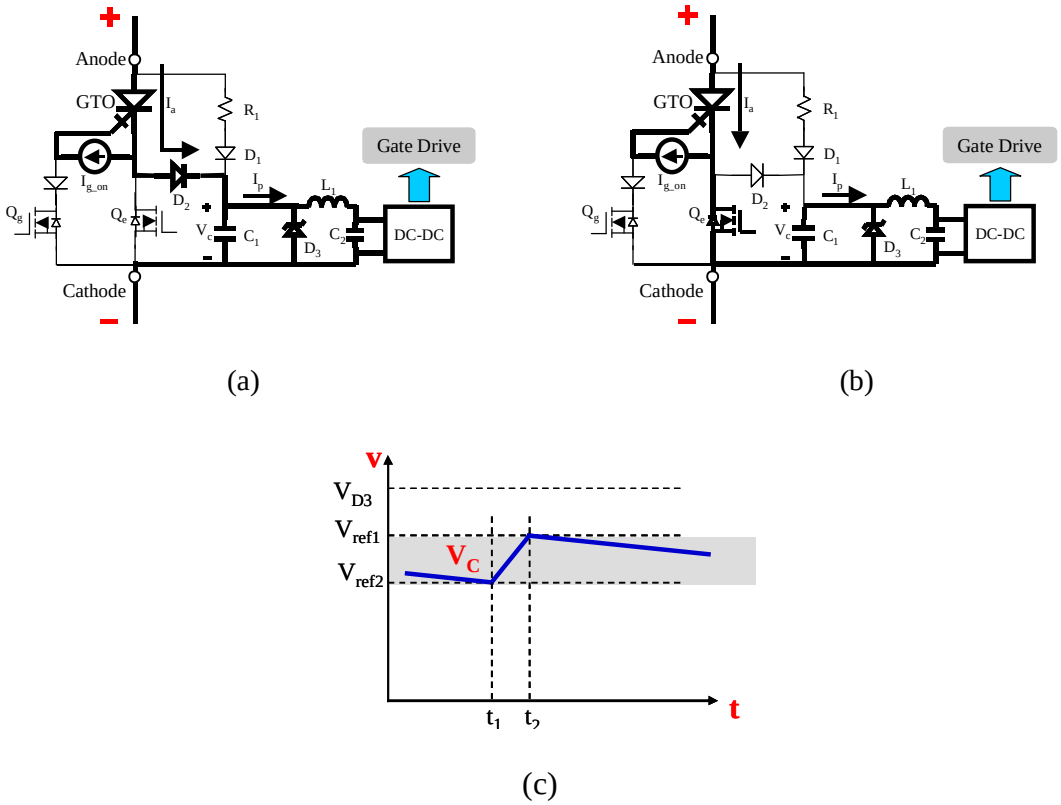
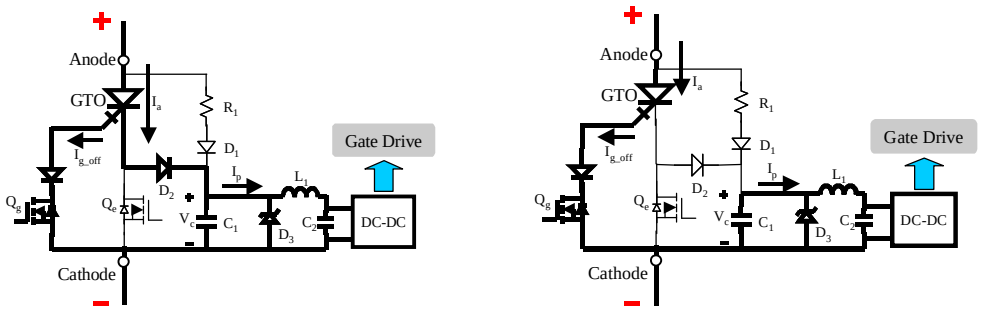


Fig. 3.13 The charging turn-on operation of ETO: (a) the operation circuit at t_1, (b) the operation circuit at t_2 and (c) the operation waveform.

When the ETO is commanded to turn off, Q_e is turned off and Q_g is turned on. V_{Qe}, the voltage between Q_e's drain and source, begins to increase, forcing cathode current commutate to Q_g via the GTO's gate. If I_a is large enough, V_{Qe} will reach V_c and forward bias D_2, as shown in Fig. 3.14 (a). Then V_{Qe} will be clamped to V_c and stop increasing. V_c is designed to be lower than the break down voltage of the Q_e MOSFET's. Therefore the drain voltage of the MOSFET's will never reach break down voltage, and this is favorable for the MOSFET's long-term reliability. After the total GTO cathode current is diverted to GTO's gate, there will be no current go through Q_e as shown in Fig. 3.14 (b), and V_{Qe} will drop. In the off state the GTO supports the whole voltage applied on the ETO. C_1 obtains energy from R_1 in off state.



(a) (b)

Fig. 3.14 The turn-off operation of ETO: (a) before unity turn-off gain achieved and (b) after unity turn-off gain achieved.

3.4.2. The Experimental Demonstration of the ETO in Active Switching Mode

The characteristics and performance of the ETO are measured in a boost converter shown in Fig. 3.15. In this circuit ETO is turned off without dv/dt snubber. The DC-link voltage is 2000V. The operation circuits and experimental results are shown in Fig. 3.16.

V_{ref1} and V_{ref2} are set to be 100V and 150V. V_c is 95V when ETO is commanded to turn on.

At time t_1, ETO is commanded to turn on. Since V_c is lower than V_{ref1}, the turn-on of Q_e is delayed. Then V_{Qe} begins to rise very fast and eventually is clamped to V_c. I_a starts to charge C_1 and V_c starts to rise. At time t_2, V_c reaches V_{ref2}. Then Q_e is turned on. V_{Qe} drops to nearly zero, and I_a is diverted to Q_e immediately. D_2 is reverse biased and V_c stop increasing. At time t_3, ETO is commanded to turn off. Q_e is turned off first. Then V_{Qe} starts to rise rapidly and clamped to V_c. V_{Qe} drops down when the unity turn-off gain achieved. Eventually V_a rises to above DC-link voltage and I_a decreases to zero. ETO turns off 2000A to the 2000V DC bus. During this switching cycle, V_c is charged from 95V to about 135V. C_1 is designed to be 1200μF. ETO successfully obtains about 10.1J energy in this switching cycle. The energy can provide the ETO's gate drive for about one second when switching at 1000 Hz.

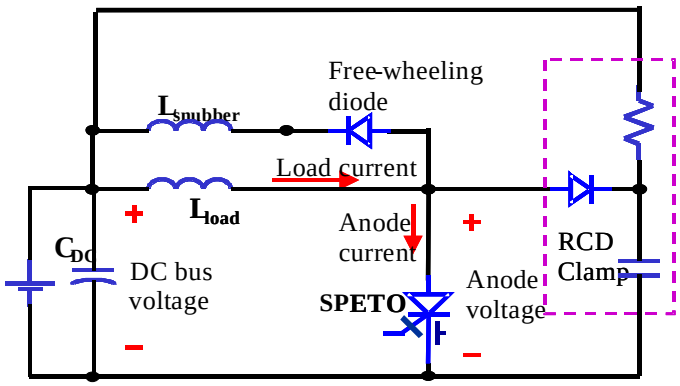
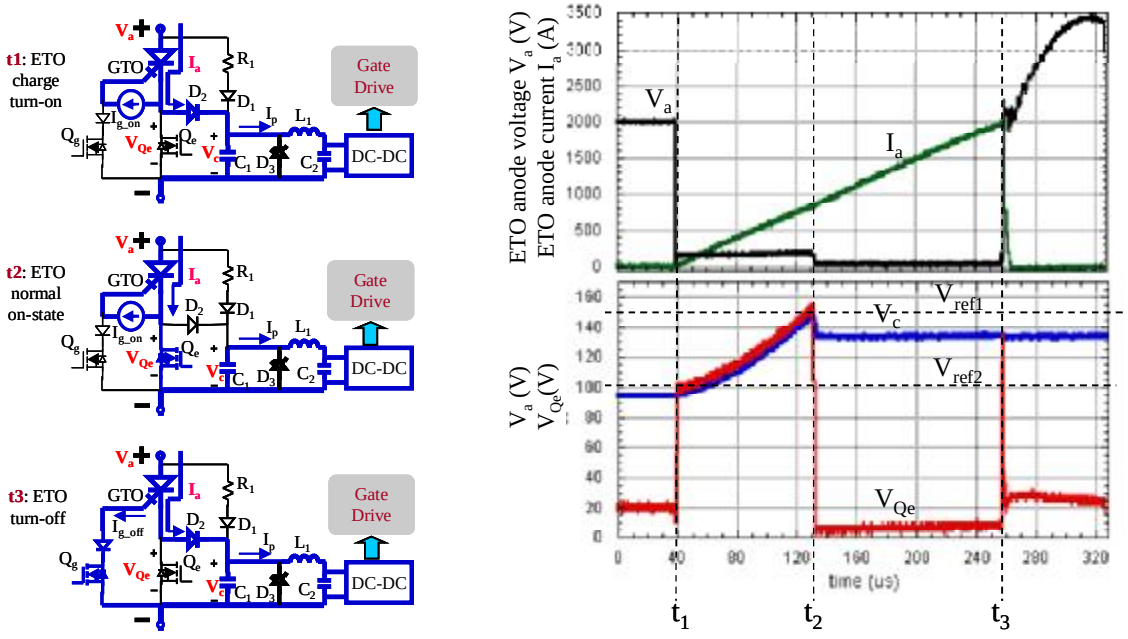


Fig. 3.15 The test circuit for the ETO in active switching mode



(a) (b)

Fig. 3.16 The experimental results of the SETO in active switching mode

3.5. The Operation Principle and Experimental Demonstration of the ETO in Inactive Switching Mode

3.5.1. The Operation Principle

When designing a voltage source PWM converter, the gate drivers of the upper switch and the lower switch of a phase leg are usually fed with complementary on/off commands with dead-time inserted, and no matter they are working in active switching mode or inactive switching mode. In section 3.2.3., it can be known that when ETO works in the inactive mode, I_{out} will never flow through ETO (I_{out} flows through its anti-parallel diode or the other ETO), no matter ETO is on or off. So in inactive switching mode, ETO is not able to obtain power through charging turn-on operation which is shown in Fig. 3.13 (a).

From Fig. 3.11 it can be known that the gate drive power consumption of ETO is much larger in switching modes than that in off state. So in inactive switching mode, the ETO gate driver consumes large power and can not obtain power through charging turn-on operation. As a result, V_c will decrease in the inactive switching mode.

In order to keep ETO work well, the output current line frequency has to be high enough to ensure that ETO comes back to active switching mode from inactive switching mode (current changes direction) before V_c decreases to a so low value that the DC-DC converter within the ETO gate driver runs out of regulation.

When device works at inactive switching mode, it does not conduct current. So the turn-on of the device is unnecessary. In this situation, the turn-on operation of the device can be suppressed to save the gate drive power [E 4]. The conventional methods are implemented within the PWM controller and need the output current direction detection: when the device is detected to be in the inactive switching mode according to the load current direction, the turn-on of this device is suppressed. To implement the unnecessary device turn-on suppression within the device, the device gate driver needs to obtain the load current information. Fig. 3.17 shows that when both upper and lower devices are commanded to be off (during dead-time), the polarities of the voltage drops across the devices will indicate whether or not the devices are in inactive switching mode. As shown in Fig. 3.17 (a), when the load current is positive, the load current will flow through D_n. At this time, V_{AK_p}, which is the voltage drop across the active switching switch ETO_p, is positive, and V_{AK_n}, which is the voltage drop across the inactive switching switch ETO_n, is negative. Similarly as shown in Fig. 3.17 (b), when the load current is negative, V_{AK_p}, which now is the voltage drop across the inactive switching

switch ETO_p, is negative, and V_{AK_n}, which now is the voltage drop across the active switching switch ETO_n, is positive.

Therefore, it can be known that when both the upper and lower switches within a converter phase leg are off, the negative voltage drop across the device indicates that the device is in inactive switching mode, in which mode the turn-on action need to be suppressed to save the gate drive power. However, the detection of the voltage drop polarity across the device in a high voltage converter is very difficult because the voltage drop will be the DC-link voltage (several kilo-volts) when the device is block voltage and negative 1~3 volts when its anti-parallel diode is conducting current. This means that the voltage polarity detection circuit need to not only block several kilo-volts when the voltage polarity is positive but also be precise enough to detect the negative voltage polarity of negative 1~3 volts.

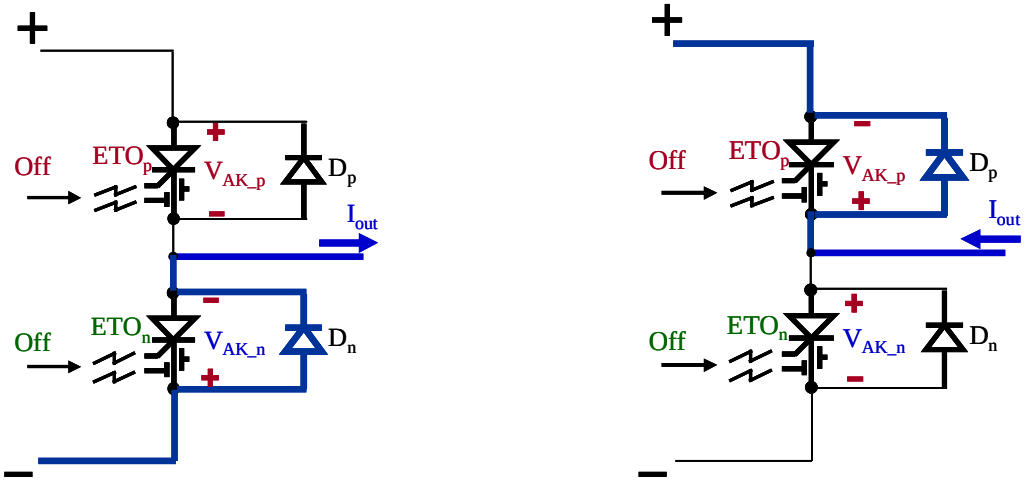


Fig. 3.17 The polarities of the voltage drops across the devices when both upper and lower devices are off: (a) the load current is positive and (b) the load current is negative.

A novel ETO gate drive suppression function which is implemented within the ETO gate driver is presented. The ETO gate driver monitors the on/off state of the ETO's anti-parallel diode and suppresses the ETO turn-on command if its anti-parallel diode is conducting current.

As shown in Fig. 2.4, the anode short type GTO is used to build the ETO. Inside the anode short GTO, there is a parasitic diode D_{pa} from GTO's gate to anode. In our design, D_{pa} is utilized to implement this novel ETO gate drive suppression function.

Fig. 3.18 shows the circuit diagram of ETO's gate drive suppression function. Fig. 3.18 shows the detail circuit diagram of the gate drive suppression function for the lower switch ETO_n, and for the higher switch ETO_p only the circuit symbol is shown. The gate drive suppression circuit includes reference voltage V_1, V_2, and a resistor R_2. Suppose the load current is positive and ETO_n is in the inactive switching mode. When ETO_p is on and ETO_n is off, there will be a small current flowing through R_2, D_4, and Q_g, as shown in Fig. 3.18 (a). V_2 is set to be smaller than V_{KG}. Then VC_0, the output of COMP, will be high, as shown in Fig. 3.18 (c). During dead-time when both ETO_p and ETO_n are off, D_p conducts current and leads to a negative polarity of V_{AK_n}. The forward voltage drop of D_4 is designed to be equal or larger than that of D_{pa} if they conduct same current. Then the current originally flowing through D_4 and Q_g will be diverted to D_{pa}, making V_{KG} lower than V_2, as shown in Fig. 3.18 (b). Then VC_0 will be low logic level, which can be used to suppress ETO_n's turn-on command. As a result, ETO_n is kept off even it is commanded to turn on, as shown in Fig. 3.18 (c). By this approach, ETO_n will not be turned on when its anti-parallel diode is conducting current. Same principle applies for ETO_p.

When Da_p is conducting current, the magnitude of the current is limited to a small value by R_2. So the current flowing through Da_p will not cause any abnormal failure problems [D 9].

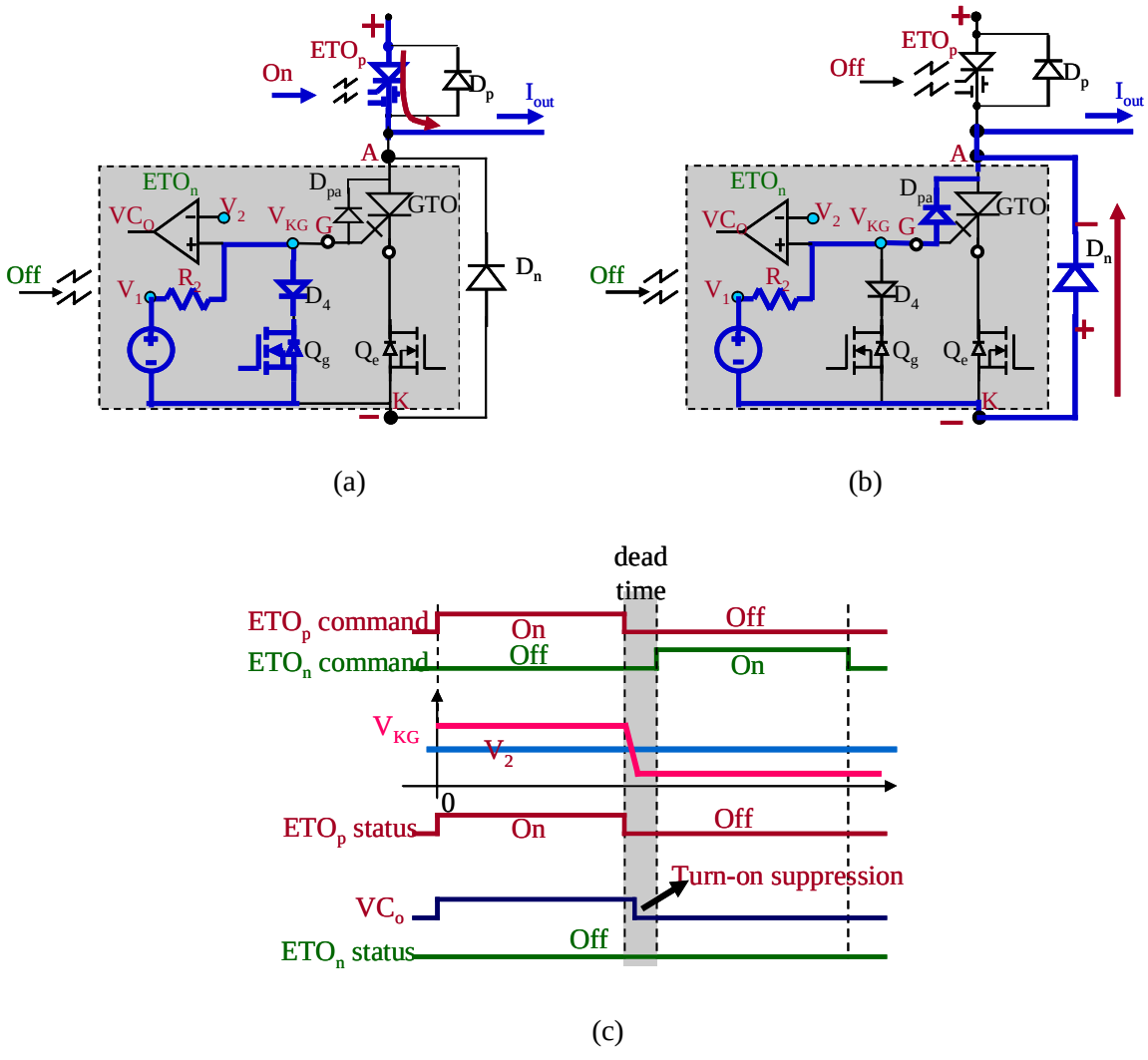
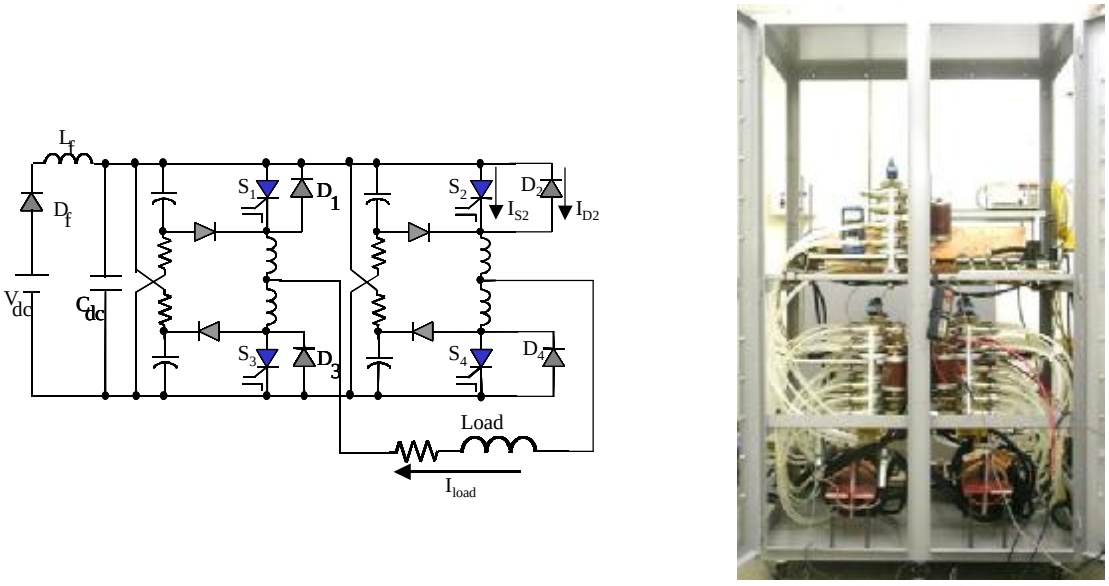


Fig. 3.18 The circuit diagram of ETO's gate drive suppression function: (a) ETO_n is off and ETO_p is conducting current; (b) During dead-time, D_n is conducting current; (c) the operation waveforms.

3.5.2. The Experimental Demonstration of the ETO's Gate Drive Unnecessary Turn-On Suppression Function

The ETO's gate drive suppression function is tested in an ETO based high power H-bridge converter as shown in Fig. 3.19. S_1, S_2, S_3, and S_4 are four ETO's. In this test, the upper and lower ETO's are fed with continuous complementary PWM signals with dead-time inserted. Each ETO's gate drive unnecessary turn-on suppression function will suppress the turn-on command when its anti-parallel diode is conducting current. Each ETO also sends out its on/off status feedback signal through optical fibers.



(a) (b)

Fig. 3.19 The ETO based high power H-bridge converter: (a) circuit schematic and (b) picture of the converter.

The ETO S_2's input switching command, on/off status feedback signal, S_2's current plus D_2's current, and the load current I_{load} are measured and shown in Fig. 3.20. From Fig. 3.20 it can be seen that although S_2 is fed with continuous PWM command signal, it

suppresses the turn-on command when its anti-parallel diode D_2 is conducting current (when I_{S2} plus I_{D2} is negative). The ETO's gate drive suppression function is successfully demonstrated.

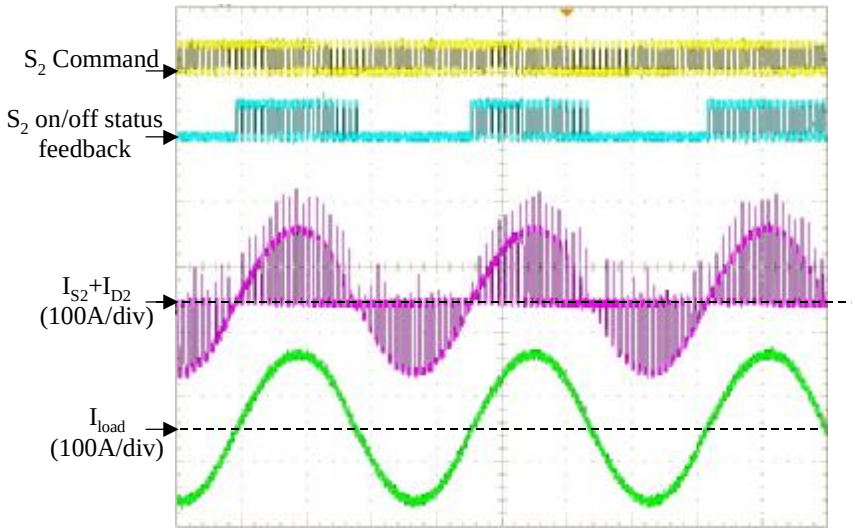


Fig. 3.20 The experimental results of the ETO's gate drive unnecessary turn-on suppression function

3.6. A Summary of the ETO Operations in Three Work Modes

Fig. 3.21 shows a summary of the ETO operations in three work modes. Taking the lower switch ETO_p of a two level voltage source converter phase leg for example, Fig. 3.21 shows the on/off command to ETO_p, the anode to cathode voltage across ETO_p, the ETO_p current and load current, and V_c which is the voltage across C_1 of ETO_p (refer to Fig. 3.4).

During power on, both ETO_p and ETO_n are off. The energy storage capacitor C_1 is charged up slowly, when V_c reaches under-voltage threshold at time t_0, the DC-DC converter is activated.

At time t_1, the switching commands are transmitted to ETO_p and ETO_n. Each ETO begins to consume more power, and the V_c will decrease gradually. After hundreds of switching cycles, at t_3, the V_c dropped below the lower threshold voltage V_{ref2}. Then the charging turn-on function during the active switching mode is activated, and V_c is charged to the upper threshold voltage V_{ref1}.

During the ineffective switching mode, the device is kept off to save the power consumption.

The voltage V_c is always controlled to be within the shadow region during the switching.

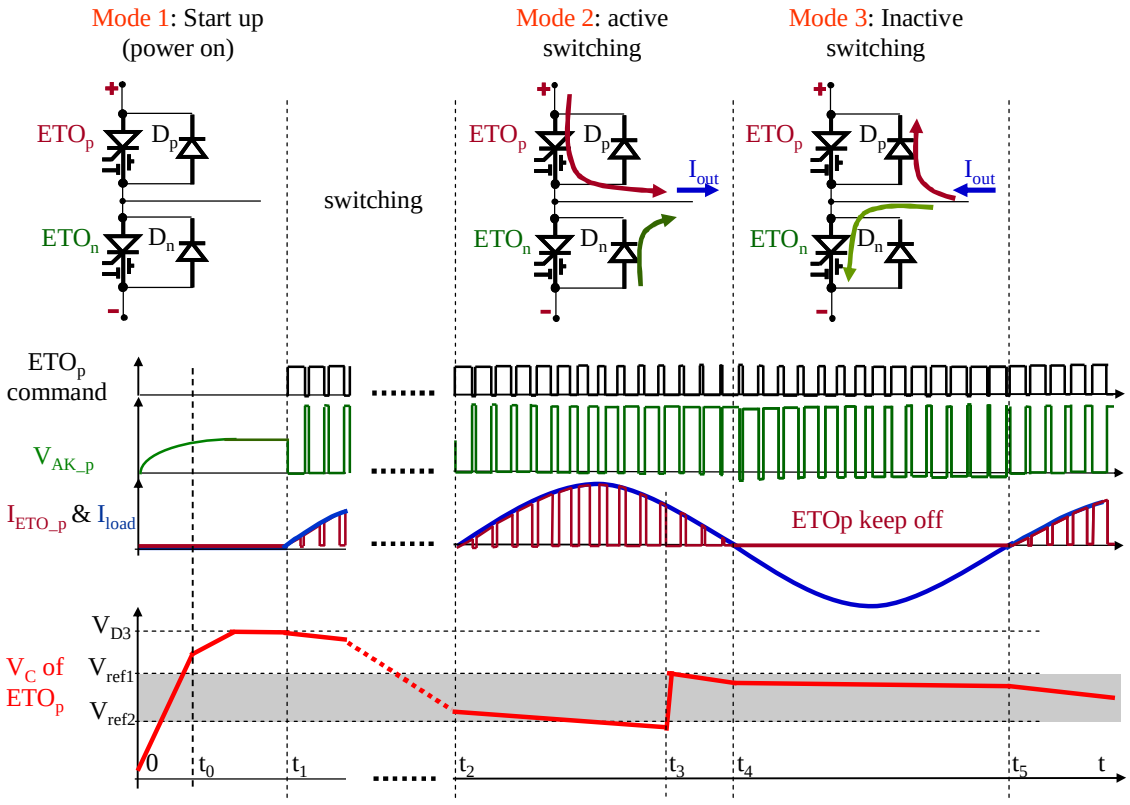


Fig. 3.21 A summary of the ETO operations in three work modes

3.7. Conclusion

This chapter presents the design and experimental demonstration of the ETO's self-power generation method. ETO achieves complete optically controlled turn-on and turn-off, and all the internal power required is self-generated.

ETO has three working modes: start up mode, active switching mode, and inactive switching mode. ETO has a simple and low power loss circuit to get power for start-up. In active switching mode, ETO obtains gate drive power through its charging turn-on operation. In inactive switching mode, ETO suppresses its unnecessary turn-on when its anti-parallel diode is conducting current to save gate drive power.

The internal power generation, unnecessary turn-on suppression, and snubberless turn-off functions are demonstrated through the experiments. ETO's self-power generation function can greatly reduce the cost and increase the reliability of the power converters since no external power supply for device gate drive is required. With self-power generation, ETO is very suitable for the high voltage converter applications such as devices series-connected and multilevel converters.

Chapter 4. A Novel Integrated Method to Eliminate the Dead-Time Requirement of the ETO

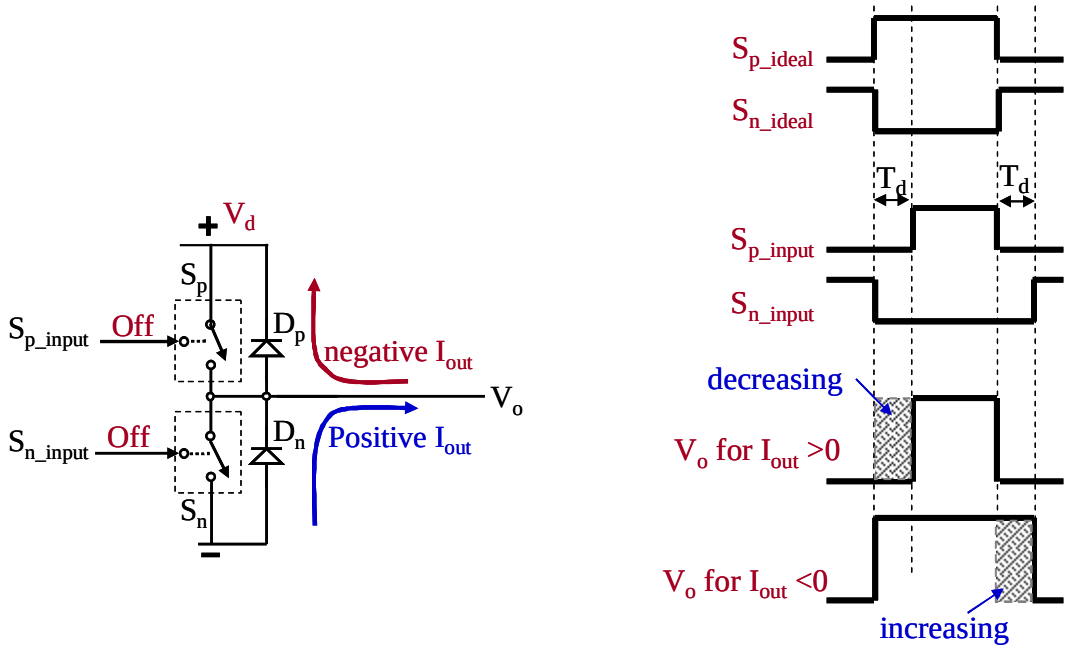
This chapter introduces the novel integrated dead-time requirement elimination method which not only improves the output waveform quality but also increases the reliability and reduces the cost of the high power PWM voltage source converters. With this unique function, the upper and the lower ETO's within a converter phase leg can receive the ideal complementary (without dead-time) PWM signals and solve shoot-through problem.

In this chapter, the principle of the new generation ETO is described. The simulation and experimental results of the ETO based PWM voltage source converters are presented.

4.1. Introduction

In the voltage source PWM converters, due to the turn-on and turn-off delay of the devices, the dead-time, which is a small time period during which both the upper and lower switches of the inverter phase leg are off, needs to be inserted in switching signals to prevent a short circuit in the DC link. Fig. 4.1 (a) shows a voltage source converter phase leg, where both the upper switch G_p and lower switch G_n are commanded to be off during dead-time. Fig. 4.1 (b) shows the dead-time effect to the output voltage. The ideal commands to G_p and G_n are ideal complementary pulses. After dead-time is inserted, the turn-on of both G_p and G_n will be delayed for dead-time T_d. If the output current is positive, during dead-time the output voltage is zero, leading to an output voltage loss

comparing to the ideal output voltage. Similarly, if the output current is negative, during dead-time the output voltage is V_d, leading to an output voltage gain comparing to the ideal output voltage. Apparently, the dead-time causes such problems as the waveform distortion and the fundamental voltage loss of the converter.



(a) (b)

Fig. 4.1 the dead-time effect: (a) a voltage source converter phase leg during dead-time and (b) the dead-time effect to the output voltage.

To reduce the dead-time effect, many dead-time compensation methods were proposed [E 2], [E 3]. The conventional compensation method is to increase the voltage output when the output current is positive and decrease the voltage output when the output current is negative.

Meanwhile, the base/gate drive suppression methods [E 4], which eliminate the dead-time requirement by inhibiting the unnecessary device switching, were proposed. As analyzed in Chapter 3, when I_{out} is positive, S_n will never conduct current. Similarly, When I_{out} is negative, S_p will never conduct current. The base/gate drive suppression methods are to keep S_n off when I_{out} is positive, and keep S_p off when I_{out} is negative, as shown in Fig. 4.2. Since either upper switch or lower switch is always off, the shoot-through will never happen. So no dead-time is required to insert to the converter.

Most of conventional dead-time compensation methods and base/gate drive suppression methods are implemented within the PWM controller and need the output current direction detection.

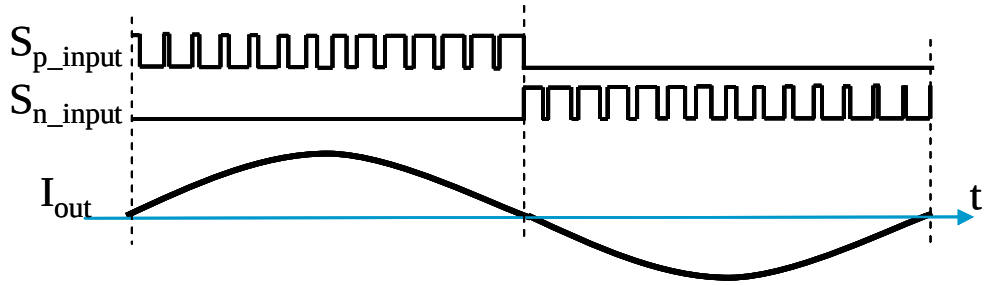


Fig. 4.2 the base/gate drive suppression method

In the GTO based high power PWM voltage source converters (VSC's), the GTO's have fairly long switching (turn-off and turn-on) period due to their long storage time, and require the huge dv/dt and di/dt snubbers for the safety operation. The long switching period requires a long dead-time, which causes severe harmonic distortion and fundamental voltage loss of the converter output. It is difficult to design the dead-time compensation for the GTO based VSC's, because the output voltage is not constant and

its changing rate depends on both the snubbers and the output current which is very hard to predict.

The ETO can be safely turned off without any dv/dt snubber due to the much more uniform turn-off process. Furthermore, the di/dt snubber is highly reduced by increasing the turn-on gate current's amplitude and rising rate. ETO has very short storage time (around 1μs). The dead-time of the ETO based VSC can be greatly reduced compared with those of the GTO based VSC's and the dead-time compensation is also much easier to design.

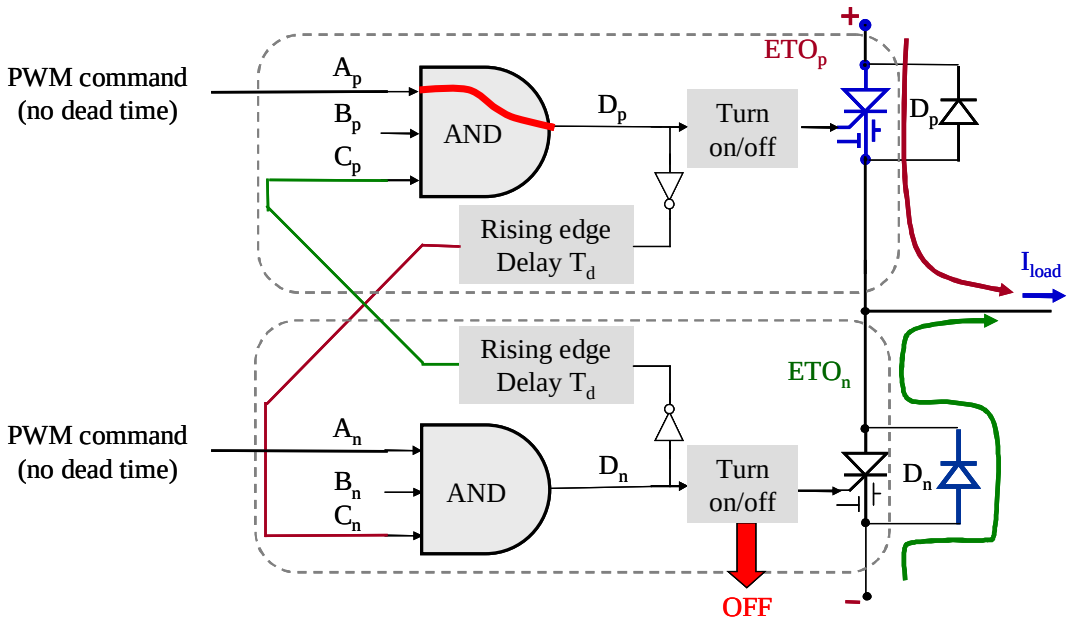
In Chapter 3, we introduced the ETO unnecessary turn-on suppression method: during dead-time (both upper and lower switch are off) the ETO gate driver monitors the on/off state of the ETO's anti-parallel diode and suppresses the ETO turn-on command if its anti-parallel diode is conducting current. Based on this method, in this chapter a novel integrated ETO gate drive method to suppress the unnecessary ETO turn-on and eliminate the dead-time requirement is presented.

4.2. Principle of the ETO's Dead-time Requirement Elimination Method

4.2.1. The ETO's Dead-time Requirement Elimination Method

Suppose the upper and lower ETO's within a VSC phase leg are fed in the fully complementary (with no dead-time) PWM commands. According to Fig. 4.2, if the load current is positive, the lower ETO should be keep off and suppress the turn-on command; if the load current is negative, the upper ETO should be keep off and suppress the turn-on command. So if ETO is originally off and the turn-on command comes, the key for the

ETO gate driver to decide whether or not to turn-on the ETO is to have the load current direction information. The method shown in Fig. 4.3 is used to realize the dead-time requirement elimination function without using external current sensor to detect the load current direction.



A_p, A_n: the fully complementary PWM command (with no dead time).

B_p, B_n: Anti-parallel diode NOT conducting.

C_p: The lower ETO is completely off.

C_n: The upper ETO is completely off.

D_p, D_n: the outputs of the AND gates.

Fig. 4.3 The principle of ETO's dead-time requirement elimination method

Fig. 4.3 shows two ETO's with their gate drivers in a two level voltage source converter phase leg. It can be seen that each ETO has an AND logic gate. Take the upper

ETO for example, the three input conditions are: A_p (input command logic), B_p (anti-parallel diode NOT conducting), and the C_p (lower device being completely off). The circuit to detect whether or not anti-parallel diode is conducting current is described in Chapter 3. The rising edge delay is set to be a litter larger than the ETO turn-off delay time. Then the output logic high of C_n indicates that the upper ETO is completely off. D_p is the output of the AND logic gate. D_p is used to control the turn-on and turn-off of the ETO.

The upper and lower ETO's are connected by two optical fibers as shown in Fig. 4.3.

Assume the load current is positive as shown in Fig. 4.3. The operation waveforms are shown in Fig. 4.4. For the lower ETO, it can be seen that these following two conditions will never be true at same time: C_n (the upper ETO being completely off), and B_n (anti-parallel diode NOT conducting), because if the upper ETO is completely off the anti-parallel diode must conduct load current, and if anti-parallel diode is not conducting load current the upper ETO must conduct load current (the upper ETO must be on). So the output of the AND gate D_n is always low. Then the lower switch is always off.

For the upper ETO, the condition C_p (the lower ETO is completely off) is true, and the condition B_p (anti-parallel diode NOT conducting) is also true because the I_{load} is positive and it can not flow through D_p. Therefore, the PWM command logic A_p (without dead-time) will become the effective command. As a result, the lower ETO is kept off, ignoring its PWM command, and the upper ETO is controlled by the PWM command with no dead-time.

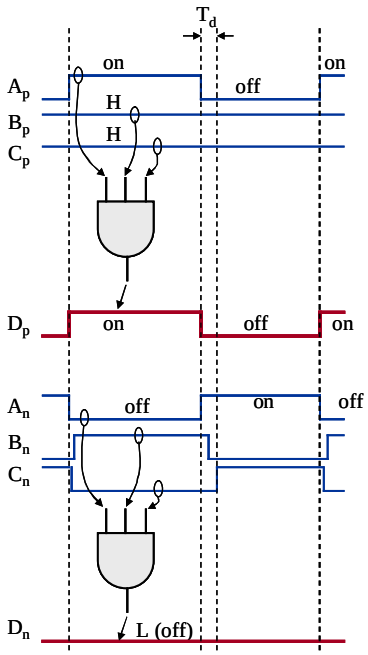


Fig. 4.4 The operation waveforms when the load current is positive

Similarly, when the load current is negative, the lower ETO is controlled by the PWM command with no dead-time, and the upper ETO is kept off, ignoring its PWM command.

Interestingly, the rising edge delay of each ETO does not cause dead-time effect when the load current keeps positive or negative (does not change direction) during the switching. Suppose the load current is positive, as shown in Fig. 4.4. Since D_n is always low (no rising edge), there is no rising edge delay effect on C_p. Therefore there is no rising edge delay effect on the active switch ETO_p. Although there is rising edge delay effect on C_n, since ETO_n is always kept off, there is no rising edge delay effect on ETO_n. Similarly, when the load current is negative, the rising edge delay of each ETO does not cause dead-time effect either.

However, when the load current is cross zero, the rising edge delay of each ETO may cause output current error. This output current error does not change with the variation of the output current. When the output current is large, the output current error is relatively small comparing with the output current and can be neglected. When the output current is very small, the output current error may cause obviously distortion, and may even cause the output current clamped to zero.

A new approach to correct the output voltage error during zero current crossing is proposed.

4.2.2. A New Approach to Correct the Output Current Error during Zero Current Crossing

Consider an H-bridge ETO converter shown in Fig. 4.5. This converter has a pure inductor load. D_{ap}, D_{an}, D_{bp}, are D_{bn} are the effective on/off command from the gate drivers.

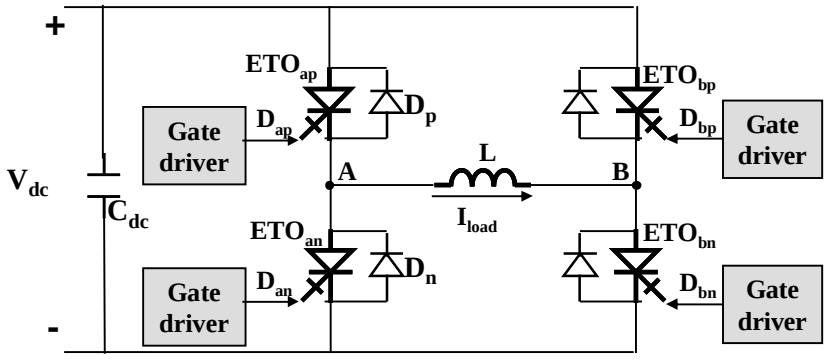


Fig. 4.5 Schematic of a H-bridge ETO converter

Fig. 4.6 shows the operation waveforms during zero crossing. At time t_2, the load current I_{load} reaches zero. From time t_2 to t_3, both ETO_{an} and ETO_{bn} are in on-state. I_{load} keeps zero since zero voltage V_{AB} is applied on the inductor L. At time t_3, ETO_{bn} is turned off.

In the ideal condition, ETO_{bp} should be turned on immediately. Then a negative V_{AB} is applied on L, forcing the current to go to negative, until ETO_{an} is turned off at time t_5. This period of time is $t_i=t_5-t_3$.

However, due to the rising edge delay, the turn-on of ETO_{bp} is delayed. ETO_{bp} is turned on at time t_4 instead of time t_3. The time delay is $t_d=t_4-t_3$. If $t_i > t_d$ as shown in Fig. 4.6, there will be a negative V_{AB} is applied on L from time t_4 to t_5 forcing the current to go to negative. This period of time is $t_e=t_i-t_d$. As shown in Fig. 4.6, the time delay t_d causes output current error:

$$\Delta I_{load} = \frac{V_{dc} \cdot T_d}{L} \qquad (1)$$

The worst case is $t_i < t_d$. In this condition, there will be no negative V_{AB} applied on L to force the current to go to negative. The I_{load} will be clamped to zero, until $t_i > t_d$.

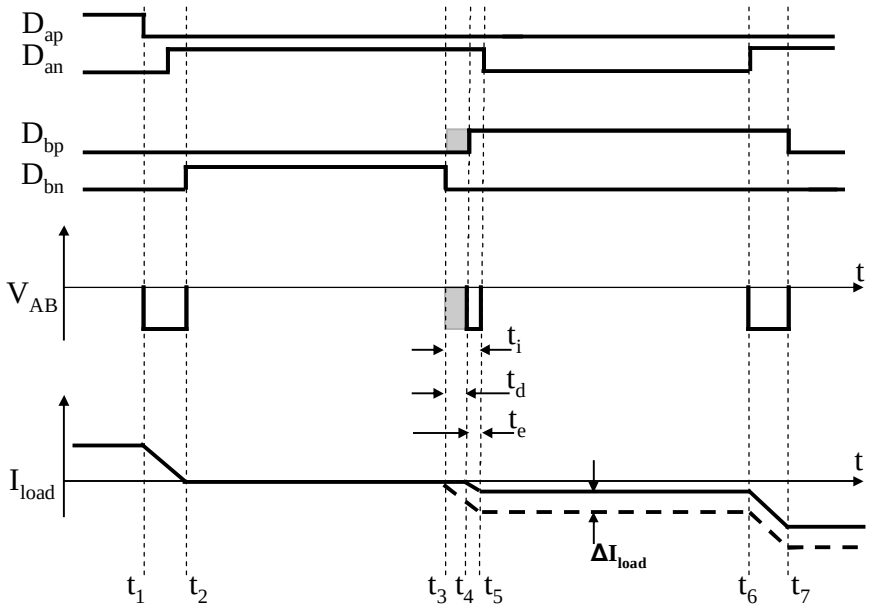


Fig. 4.6 The operation waveforms during zero crossing

A new approach to correct the output current error during zero current crossing is proposed, as illustrated in Fig. 4.7. When the load current keeps positive or negative (is not crossing zero), one of the upper and the lower ETO within a phase leg is always off. Therefore the turn-off of one of the ETO will not be followed by the turn-on of the other ETO. Only when the current is crossing zero, the turn-off of one of the ETO will be followed by the turn-on of the other ETO. As shown in Fig. 4.7, the turn-off of ETO_{bn} at time t_3 is followed by the turn-on of ETO_{bp} at time t_5. This condition indicates to the controller that the load current is crossing zero. The approach is compensating t_d by increasing the ETO's on time by t_d, as shown in Fig. 4.7. The t_d compensation only needs to execute once when the current is crossing zero. As shown in Fig. 4.7, the current error is corrected at time t_7 due to the t_d compensation.

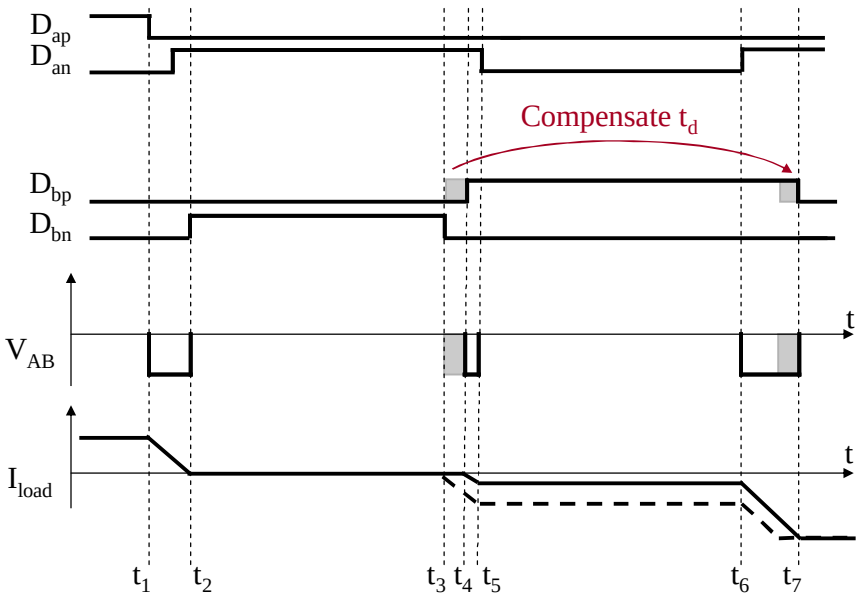


Fig. 4.7 a new approach to correct the output current error during zero current crossing

This approach is more important during the worst case: $t_i < t_d$. The t_d compensation will help the load current coming out of the zero current clamping.

4.3. The Design of ETO's Dead-time Requirement Elimination Function

Fig. 4.8 shows the circuit diagram of the ETO and the ETO symbol. In Fig. 4.8 (a), VC_o indicates whether or not the ETO's antiparrallel diode is conducting current. The circuit realization is described in Chapter 3. ETO's input signal CMP is the switching command from the PWM controller. ETO's input signal FI is the feedback signal from another ETO in the same phase leg. CMP and FI are delivered by the optical fibers. The "falling edge trigger turn-off delay" function block is used to correct the output current error during zero current crossing. This function block increases the on-time of the ETO

by time t_d if this ETO is turn-on is followed by the turn-off of the other ETO within the same phase leg.

FO is the feedback of the ETO, indicating the on/off state of this ETO. Fig. 4.9 shows the relationship between CMD_E and FO. In Fig. 4.9, FO is logically inverted with CMD_E except that there is a time delay T_d between the falling edge of CMD_E and the rising edge of FO. If FO is high, it is indicating that this ETO is in off state, and if FO is low, it is indicating that this ETO is in on state.

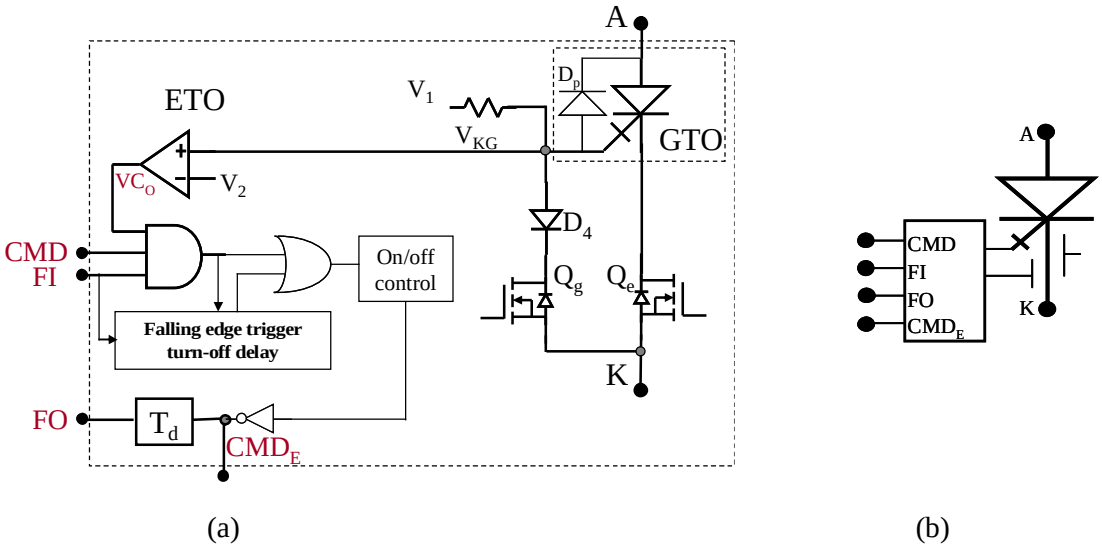


Fig. 4.8 The circuit diagram of the ETO with the dead-time requirement elimination method: (a) circuit diagram and (b) circuit symbol

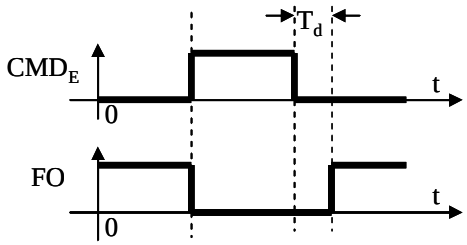


Fig. 4.9 The relationship between CMD_E and FO.

Fig. 4.10 shows the ETO configuration in a two level voltage source converter phase leg (di/dt snubber is not included in the drawing). In this structure, ETO_p is the upper switch, and D_p is ETO_p's anti-parallel diode. ETO_n is the lower switch, and D_n is ETO_n's anti-parallel diode. Two optical fibers OF3 and OF4 are used to connect ETO_p and ETO_n. Optical fiber OF1 and OF2 transfer switching command to ETO_p and ETO_n from the PWM controller. I_{out} is the current output of the phase leg.

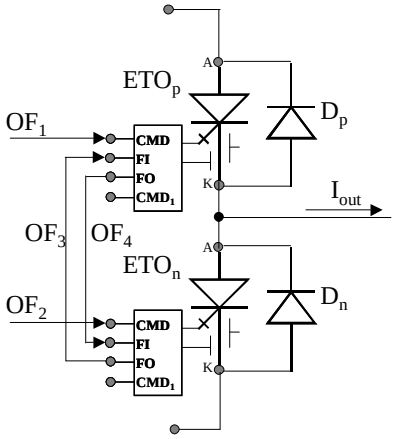


Fig. 4.10 ETO based two-level VSC phase leg

4.4. Simulation and Experimental Results

The ETO with dead-time requirement elimination method is simulated and tested in a H-bridge ETO converter shown in Fig. 4.11. A high power inductor and resistor are connected in serial as the load. The load is connected between OUT_1 and OUT_2.

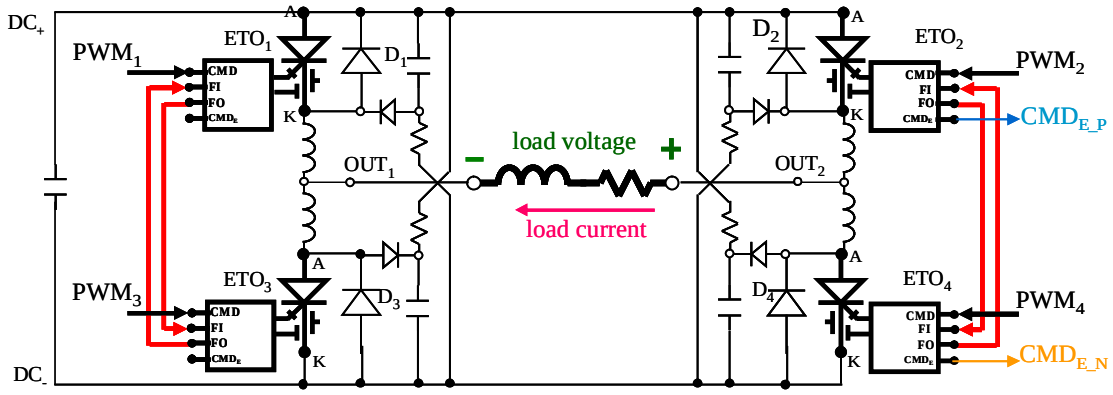


Fig. 4.11 The schematic of the ETO based H-bridge VSC.

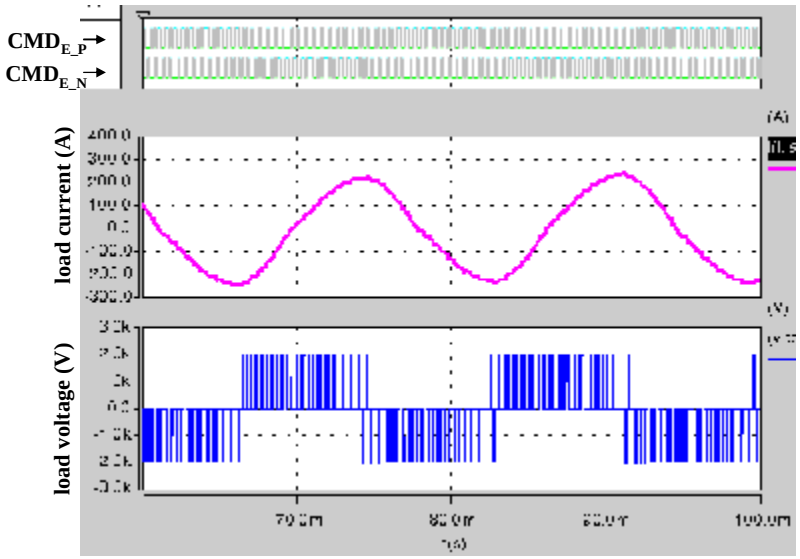
4.4.1. Simulation Results

The parameters of the converter for simulation are shown in table 4.1.

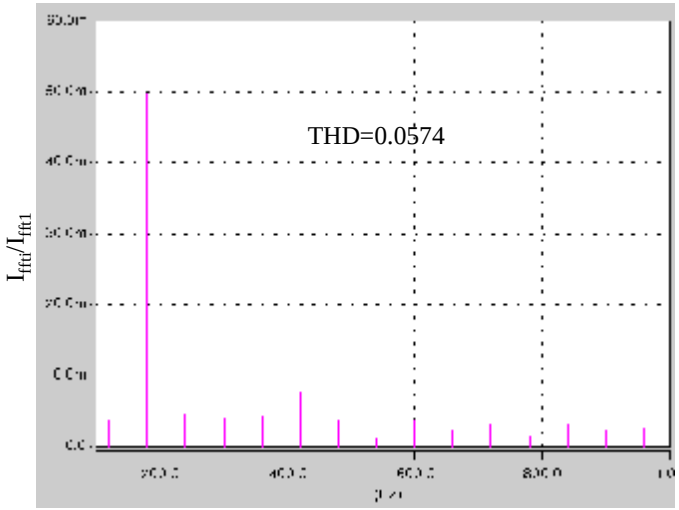
Table 4.1. The parameters of the H-bridge PWM voltage source power stage used for test

V_{dc}	Load inductor	Load resistor	Switching frequency	Line frequency
2000 V	10mH	0.5Ω	2 kHz	60Hz

Fig. 4.12 (a) shows the simulation results of the output current and output voltage using the conventional PWM strategy with 2kHz and 15μs dead-time. It clearly shows the current distortion caused by the dead-time effect. Fig. 4.12 (b) shows the harmonic frequency spectrum. The current THD is 5.74%.



(a)

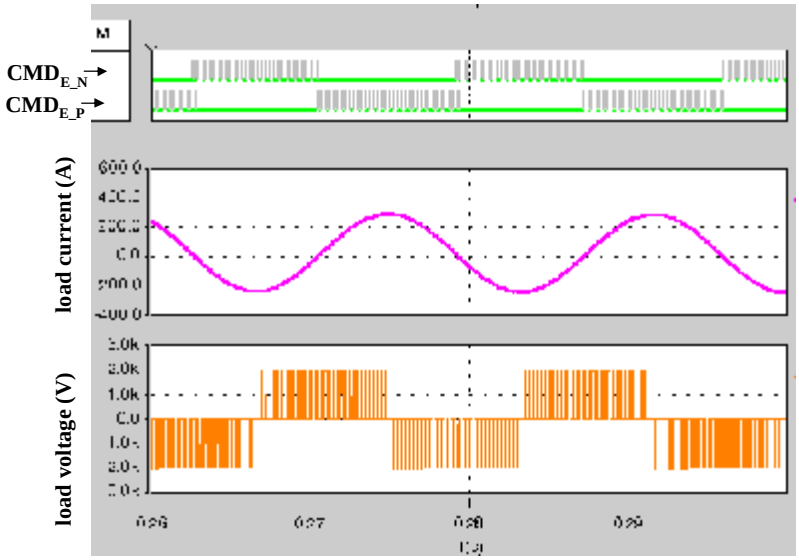


(b)

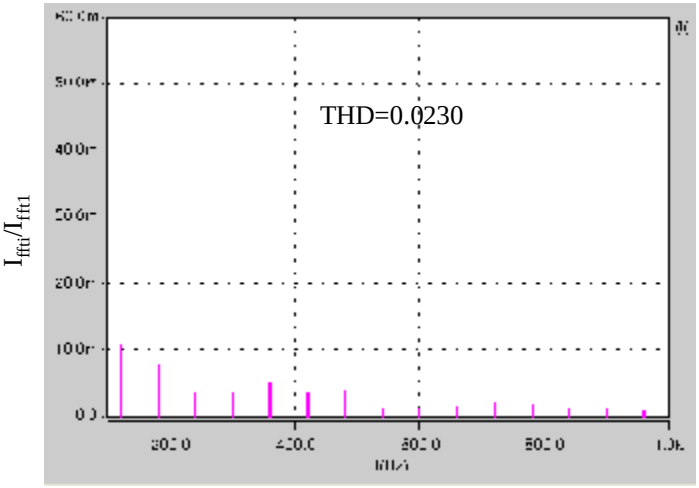
Fig. 4.12 The simulation results of the converter with 2kHz switching frequency and 15us PWM dead-time: (a) simulation waveforms and (b) Output current harmonic frequency spectrum

Fig. 4.13 shows the simulation results of CMD_{1_1}, CMD_{1_2}, output current and the output voltage using the ETO with the proposed method. From Fig. 4.13 (a), it can be seen that when output current is negative CMD_{1_1} is always low. When output current is

positive, CMD_{1_2} is always low. Fig. 4.13 (b) shows the harmonic frequency spectrum. The current output is highly improved comparing to the current output of the conventional PWM strategy with dead-time. The THD is 2.3%.



(a)



(b)

Fig. 4.13 The simulation results of the converter with 2kHz switching frequency and using ETO's with the dead-time requirement elimination method: (a) simulation waveforms and (b) output current harmonic frequency spectrum

When the load current is very small, the output current error caused by the rising edge delay becomes obvious. Fig. 4.14 (a) shows that when the output current decreases to about 30A, we can clearly notice the output current distortion caused by the rising edge delay. After applying the rising edge delay compensation approach, the output current quality is highly improved, as shown in Fig. 4.14 (b).

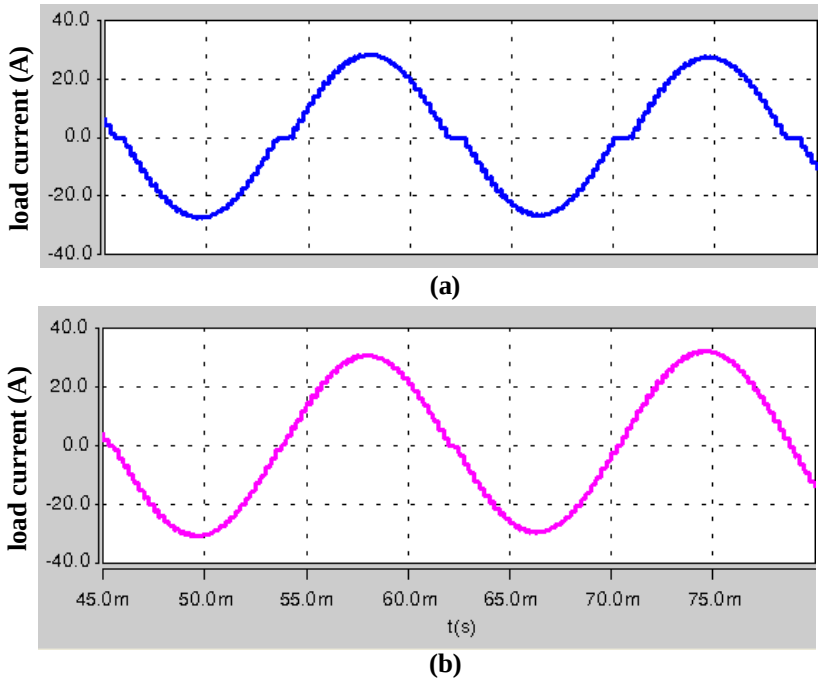


Fig. 4.14 the simulation results during zero current crossing: (a) without T_d compensation and (b) with T_d compensation

4.4.2. Experimental Results

The ETO with dead-time requirement elimination method based on the circuit shown in Fig. 4.8 was developed. The picture of the ETO is shown in Fig. 4.15. Fig. 4.15 also shows the input and output signals, which is carried by optical fibers, of the ETO. Based

on Fig. 4.11, an ETO based H-bridge voltage source converter is built and tested. Fig. 4.16 shows the picture of the H-bridge converter. The parameters of the converter for the test are shown in table 4.2.

Fig. 4.15 The picture of the developed ETO

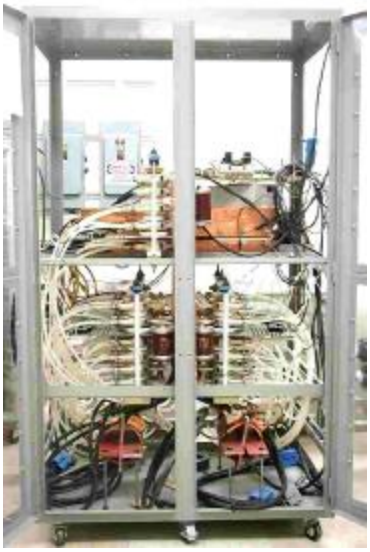


Fig. 4.16 The picture of the ETO based H-bridge VSC

Table 4.2 The parameters of the H-bridge PWM voltage source power stage used for test

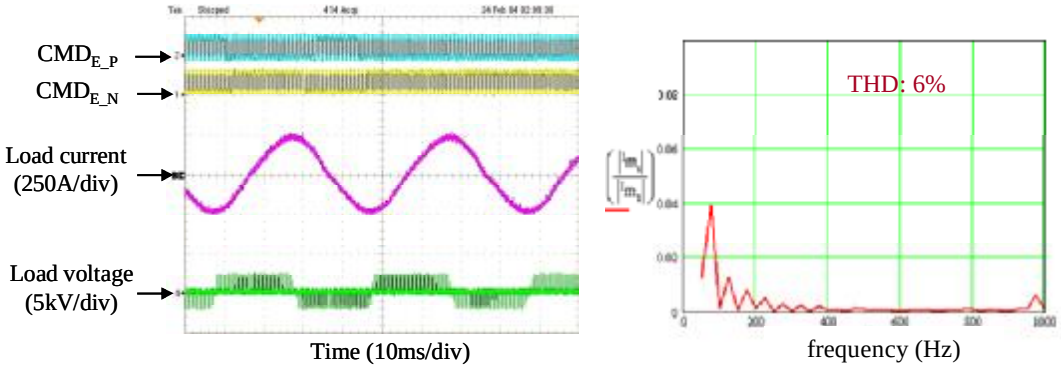
V_{dc}	Load inductor	Load resistor	Switching frequency	Line frequency
2000 V	3.3mH	21mΩ	1&2 kHz	25Hz

Fig. 4.17 shows the experimental waveforms of the output current and output voltage using the conventional PWM strategy with 1kHz and 15μs dead-time. It clearly shows the

current distortion caused by the dead-time effect. Fig. 4.17 (b) shows the harmonic frequency spectrum. The current THD is 6%. Fig. 4.18 shows the experimental waveforms of the output current and output voltage using the conventional PWM strategy with 1kHz and 25us dead-time. It has a more serious current distortion caused by the longer dead-time. Fig. 4.18 shows the harmonic frequency spectrum. The current THD is 10.3%.

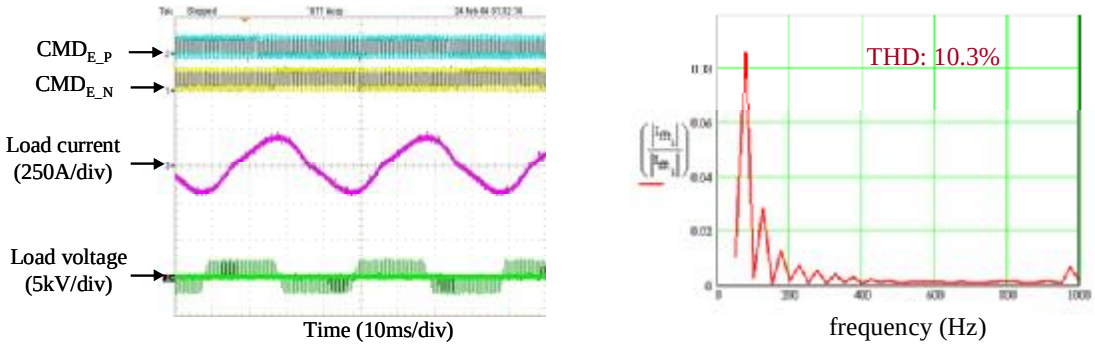
Fig. 4.19 shows the experimental results of CMD_{1_1}, CMD_{1_2}, output current and the output voltage using the ETO with the proposed method. From Fig. 4.19 (a), it can be seen that when output current is negative CMD_{1_1} is always low. When output current is positive, CMD_{1_2} is always low. Fig. 4.19 (b) shows the harmonic frequency spectrum. The current output is highly improved comparing to the current output of the conventional PWM strategy with dead-time. The THD is 3.3%.

It also can be seen from the test results that the VSC using the new generation ETO reduces the output voltage loss.



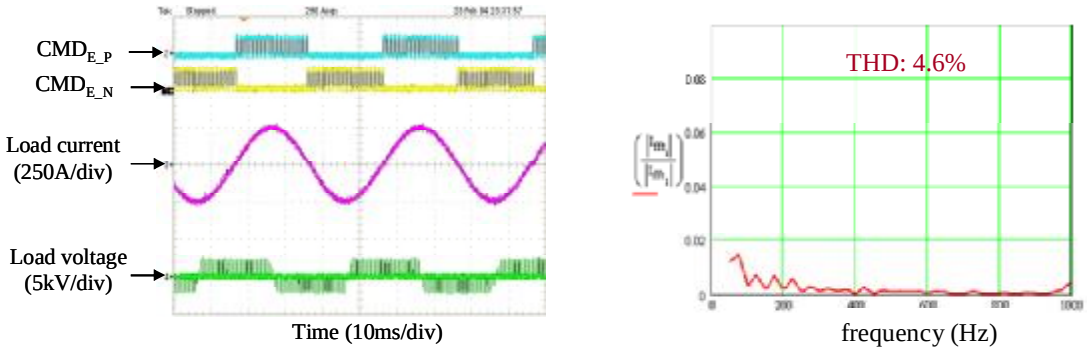
(a) (b)

Fig. 4.17 The experimental results of the converter with 1kHz switching frequency and 15us PWM dead-time: (a) experimental waveforms and (b) Output current harmonic frequency spectrum



(a) (b)

Fig. 4.18 The experimental results of the converter with 1kHz switching frequency and 25us PWM dead-time: (a) experimental waveforms and (b) Output current harmonic frequency spectrum



(a) (b)

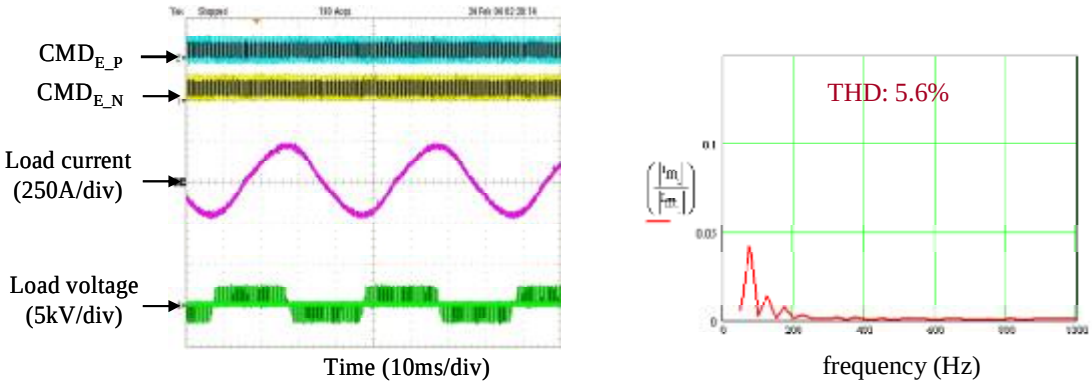
Fig. 4.19 The experimental waveforms of the converter with 1kHz switching frequency and using ETO's with the dead-time requirement elimination method: (a) experimental waveforms and (b) Output current harmonic frequency spectrum

The experiment of the converter with 2 kHz switching frequency was also performed. Fig. 4.20 (a) shows the experimental waveforms of the output current and output voltage using the conventional PWM strategy with 2 kHz and 15us dead-time. It clearly shows the current distortion caused by the dead-time effect. Fig. 4.20 (b) shows the harmonic

frequency spectrum. The current THD is 5.6%. Fig. 4.21 (a) shows the experimental waveforms of the output current and output voltage using the conventional PWM strategy with 2 kHz and 25us dead-time. Fig. 4.21 (b) shows the harmonic frequency spectrum. The current THD is 13%.

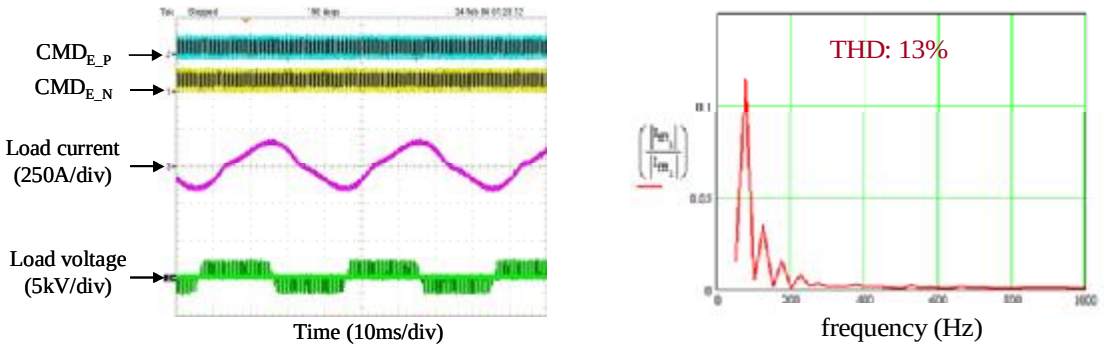
Fig. 4.19 shows the experimental results of CMD_{1_1}, CMD_{1_2}, output current and the output voltage using the ETO with the proposed method. Fig. 4.19 (b) shows the harmonic frequency spectrum. The THD is improved to 3.3%.

Fig. 4.23 shows the waveforms when current is cross zero. It can be seen that the switching mode is transferred from ETO_1 to ETO_3 smoothly when the load current is cross zero from positive value to negative value. The tests of Fig. 4.17 to Fig. 4.22 have exactly the same PWM command to the ETO's. It can also be seen from the test results that the VSC using the new generation ETO reduces the output voltage loss.



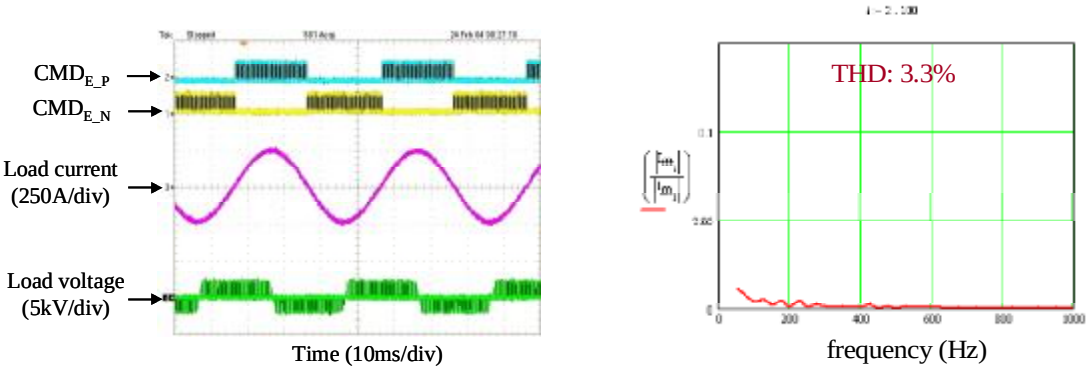
(a) (b)

Fig. 4.20 The experimental results of the converter with 2kHz switching frequency and 15us PWM dead-time: (a) experimental waveforms and (b) Output current harmonic frequency spectrum



(a) (b)

Fig. 4.21 the experimental results of the converter with 1kHz switching frequency and 25us PWM dead-time: (a) experimental waveforms and (b) Output current harmonic frequency spectrum



(a) (b)

Fig. 4.22 The experimental waveforms of the converter with 2kHz switching frequency and using ETO's with the dead-time requirement elimination method: (a) experimental waveforms and (b) Output current harmonic frequency spectrum

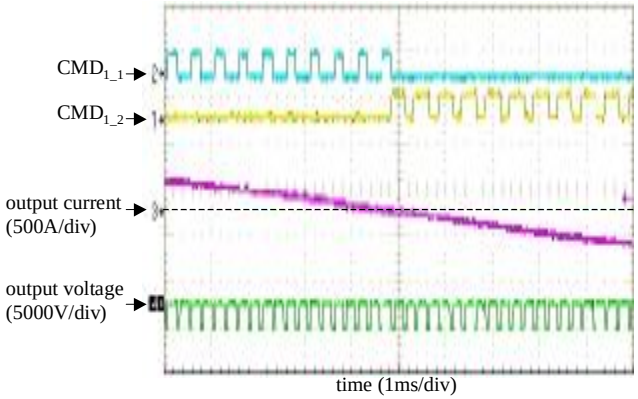


Fig. 4.23 the waveforms when current is cross zero using the ETO with the proposed method

4.5. Conclusions

In this chapter a novel integrated ETO gate drive method to suppress the unnecessary ETO turn-on and eliminate the dead-time requirement is presentd. By this method, when the upper and the lower ETO's within a converter phase leg are connected with two optical fibers, the ETO's can receive the ideal complementary (without dead-time) PWM signals and solve shoot-through problem. Compared with the conventional high power devices, the ETO reduces the output waveform distortion and the fundamental voltage loss of the converter. This method implements the base/gate drive suppression function within the ETO gate driver, and no current sensor and complex control are required.

By this novel method, ETO not only reduces harmonic distortion of VSC, but also reduces the cost since no current sensor is required. Additionally, since the switch action of the gate driver is reduced, the gate driver loss is also reduced. With this function, the ETO can be used in the high power voltage source PWM converters to improve the output waveform quality, increase the reliability, and reduce the cost.

Chapter 5. The Built-in Current Sensor and Over-Current Protection of the ETO

This chapter introduces a method to measure the ETO current and transfer the current information to a PWM signal whose duty cycle is proportional to the current value. The temperature effect on the MOSFET's on-resistance is eliminated. The sensed current information is sent out through an optical fiber. So it is very easy to be received and used for control purpose. The sensed current information is also used for the built-in over-current protection purpose. The ETO's built-in current sensor, fast turn-off speed, and high current turn-off capability enable the ETO to shut down the fault current very fast in the over-current fault situation.

5.1. Introduction

The current sensor is an important element in the power electronics systems for the measurement, protection, and control purposes. In the high power application, current transformers, Hall Effect devices, and current shunts are widely used. The current transformer and Hall Effect device are convenient to use. But they require expensive and bulky magnetic cores. The shunts are cost effective, but they usually need the complicated signal isolation and amplifier, and also suffer from the noise problems.

This chapter introduces an ETO built-in current sensor, which can measure the ETO current during its on-state. The sensed current information is sent out by an optical PWM signal which can be easily received and used for control purpose.

The built-in current sensing function can also be used in the over-current protection purpose.

The over-current caused by the short circuit, malfunction, or the component failure is severe fault situation that can result in further failure of the power converter if appropriate remedial action is not taken in time. The over-current protection of the conventional GTO based converter is more complicated and difficult than that of the MOSFET, BJT, or IGBT based converters. For the MOSFET, BJT, or the IGBT, the accidental over-current can cause the device to go out of the saturation region and enter the active region, and the rising voltage of the device will limit the current. In this situation, the converter can be protected if the device is commanded to shut down quickly. However, the latching devices such as GTO cannot enter such active region to limit the current. On contrary, the large fault current will make the GTO to latch more strongly. GTO takes relatively longer time to turn off due to its longer storage time, which also increases with the current. If the rising rate of the fault current is too fast, the current will exceed the maximum controllable current of the GTO during the storage time, and cause the GTO turn-off failure. In conventional technology, when over-current situation happens, the GTO will be kept on and let the fault current be cut off by the protection elements such as fuses. To protect the GTO, an additional thyristor, so-called crowbar, is often connected in parallel with the GTO. In the over-current situation, the crowbar will be trigged on to divert the current from the GTO. Obviously, those approaches are expensive and not reliable.

The ETO dramatically reduces its storage time to about 1μs through the unity gain turn-off. Therefore, the ETO has a much faster turn-off speed than that of the

conventional GTO. Combining with the built-in current sensor, the ETO can detect the over-current and trigger the turn-off very fast and shut down the ETO before the fault current reaches the maximum ETO controllable turn-off value.

5.2. The ETO Built-in Current Sensor

The emitter turn-off (ETO) thyristor is a MOS-GTO hybrid high power device. Inside the ETO, the GTO is connected in series with the MOSFET's. When ETO is conducting current, the total current will go through both the GTO and the MOSFET's. In this situation, the MOSFET's act as a small linear resistor whose voltage drop is proportional to the current through it. Based on this principle, the ETO's built-in current sensor is designed.

5.2.1. The Design of the ETO Built-in Current Sensor

Fig. 5.1 Shows the ETO equivalent circuit and the circuit symbol. The emitter switch consists of many MOSFET's in parallel. These MOSFET's have very good current sharing capability due to their strong positive temperature coefficient. As shown in Fig. 5.1, the parasitic resistance and inductance R_1, C_1, R_2, C_2, etc, which caused by the layout of the MOSFET's and the circuit routing, may affect the current sharing of the MOSFET's and increase the ETO current conduction loss. To reduce these parasitic effects, the circuits are put in a multi-layer PCB, and these MOSFET's are arranged in a ring shape and put very close around the GTO. By following this approach, the parasitic effects are minimized and can be ignored for the current sensing. So we can get the

simplified equivalent circuit shown in Fig. 5.2. During the on-state as shown in Fig. 5.2 (a), the gate switch is off and the emitter switch is on. The ETO current will go through both the GTO and the emitter switch MOSFET's, which are also used for the current sensing purpose. In the off-state as shown in Fig. 5.2 (b), the emitter switch is kept off.

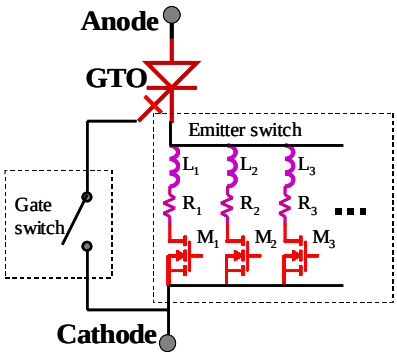
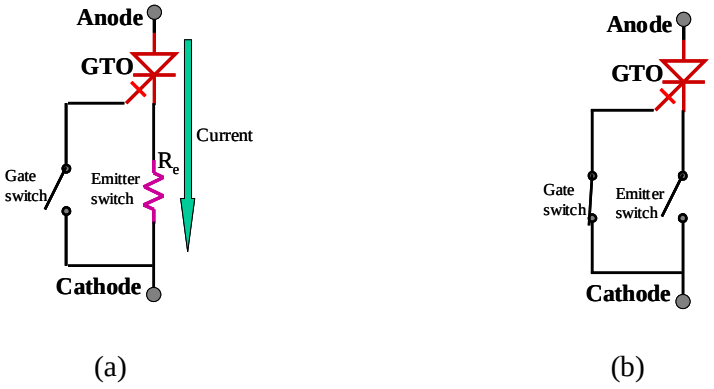


Fig. 5.1 ETO circuit equivalent circuit



(a) (b)

Fig. 5.2 The simplified equivalent circuit of the ETO: (a) On-state. (b) Off-state

Fig. 5.3 shows the block diagram of the ETO built-in current sensor and over-current protection. The voltage across the emitter switch V_e is sensed, and sent across a resistor R_1 to the PWM generator (PG) and the comparator and latch (CL). There is a switch S_1 connecting R_1 and electrical ground. In addition, the temperature of the ETO emitter

switch is also sensed and transferred to a voltage signal V_t. V_t is also sent to the PG and the CL. In the ETO on state, S_1 is opened and the V_e, which is proportional to the current through the emitter switch, equals to V_i. In the ETO off state, S_1 is closed and the zero voltage, which means that the current through the emitter switch is zero, equals to V_i. V_i is received by PG and CL. The PG generates a PWM signal whose duty-cycle is proportional to V_i. Then the PWM signal is transformed to the optical signal and sent out through the optical fiber.

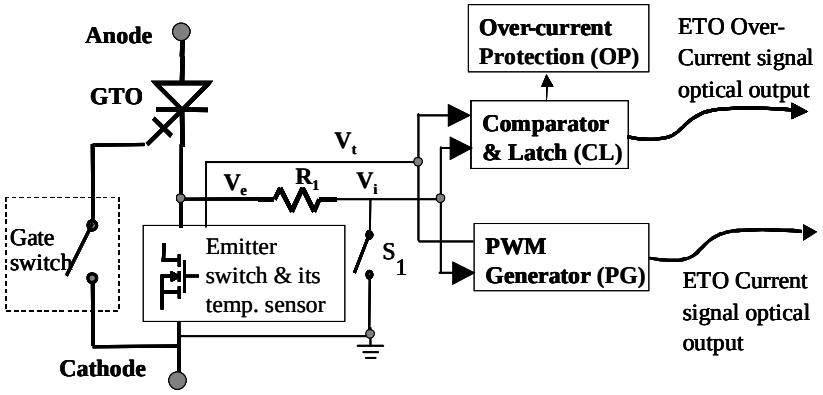


Fig. 5.3 The block diagram of the ETO built-in current Sensor and over-current protection.

5.2.2. The Static Performance of the ETO Built-in Current Sensor

Fig. 5.4 shows the V_e vs. the ETO current in the ETO on-state, and demonstrates their linear relationship in 20°C as shown in (5-1).

$$V_e = I \bullet 0.000083 \qquad (5\text{-}1)$$

Based on this relationship, the PG is designed. Assuming the ETO switch frequency is 1 kHz, and the duty-cycle is between and 5% and 95%, then the minimum on time is

about 50us. To make sure that the current sensor can catch at least one point during the ETO minimum on time situation, the period of PG is chosen as 25us. So the switching frequency of PG is set to 40 kHz. Although the ETO is capable of turning off 5000A without dv/dt snubber, its operating current, which is rather limited by ETO's thermal resistance, is usually below 3000A. So the PG duty cycle is set from 50% to 90% according to the 0A and 3000A ETO current. So the voltage-duty cycle relationship of PG is

$$Dutycycle = \frac{I}{7500} + 0.5. \qquad (5\text{-}2)$$

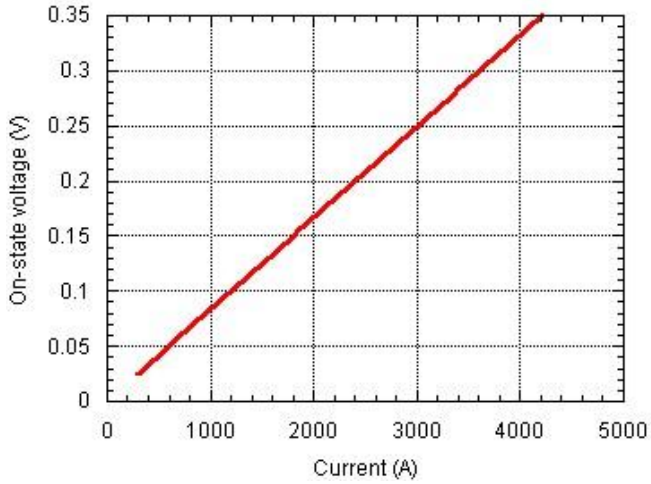


Fig. 5.4 The on-state characteristic of the emitter switch.

Fig. 5.5 shows the experiment results of the built-in current sensor output PWM duty cycle vs. the current. As can be seen, the test results meet the design requirement very well. The measurement error of ETO built-in current sensor is less than 1%.

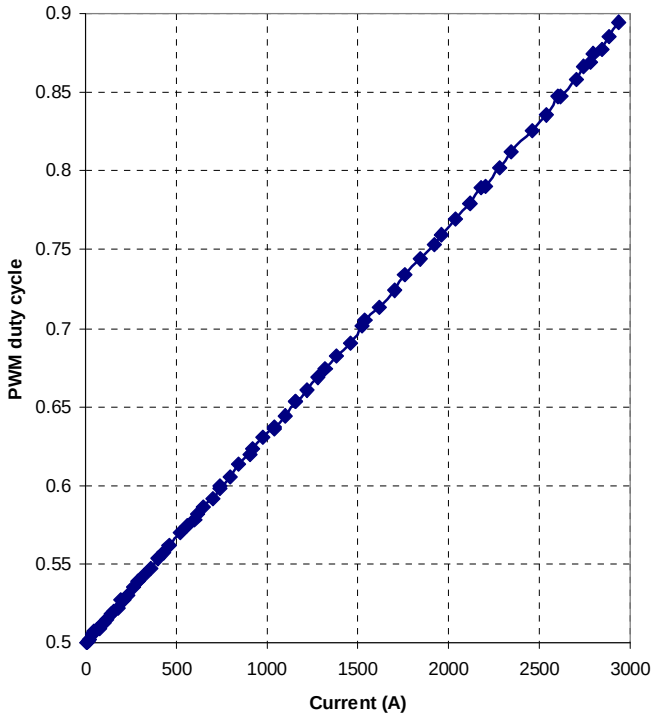


Fig. 5.5 Measured current sensor output PWM signal duty cycle vs. the ETO current

5.2.3. The Dynamic Performance of the ETO Built-in Current Sensor

The ETO with the built-in current sensor was tested in a boost type PWM converter. In this converter, the ETO built-in current sensor measured the ETO current on-line during the ETO switching. The output PWM optical signal of the ETO built-in current sensor was received by another circuit board and transformed back to the electrical PWM signal for measurement. Fig. 5.6 shows the experimental test result of the current sensor output (bottom curve) and the ETO current measured by the rogowski coil (top curve) during one PWM pulse. The accuracy of the ETO built-in current sensor can be seen more clearly in Fig. 5.7. Fig. 5.7 shows a reconstructed current whose value is proportional to the built-in current sensor output duty cycle. It can be seen that the built-

in current sensor output meets very well with the current measured by the rogowski coil. And the measurement delay is less than 25us (the period of the PWM signal).

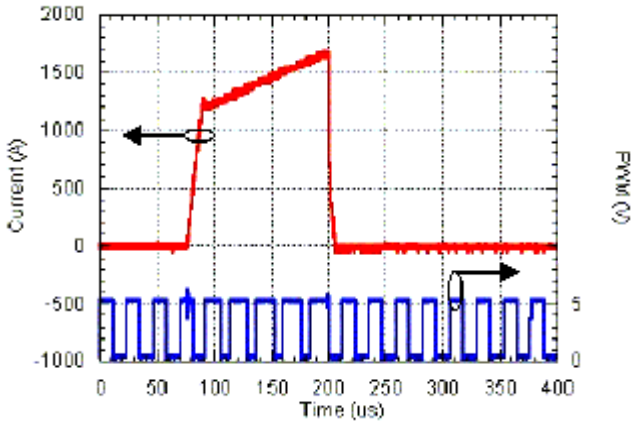


Fig. 5.6 Measured current and current sensor output PWM signal during a PWM pulse.

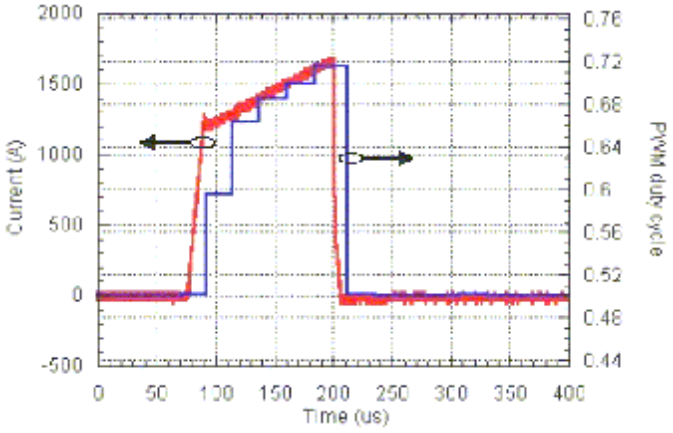


Fig. 5.7 Measured current and reconstructed current

5.2.4. The Temperature Compensation of the ETO Built-in Current Sensor

The on-resistance of the MOSFET increases with the increasing temperature. Fig. 5.8 shows the emitter switch on-resistance vs. the temperature. The on-resistance of the

MOSFET at 100^{o}C is about 50% bigger than that at 20 ^{o}C. So if the temperature effect is not compensated, built-in current sensor will have large measurement error during temperature changing. We linearized the data in Fig. 5.8 and get the following relationship between the emitter switch on resistance R_{on} and its junction temperature T_j.

$$R_{on} = T_j \bullet 0.00052 + 0.07118 \qquad (5\text{-}3)$$

As shown in Fig. 5.3, the case temperature of the MOSFET's is measured by a linear current sensing IC. Since many MOSFET's connected in parallel to form the emitter switch, each MOSFET's consumes only a small amount of power even in the ETO heave load. The temperature difference between the MOSFET's case and junction is small (less than 3^{o}C). So the case temperature, T_c, can be measured and used for the temperature compensation purpose.

From (5-3) one can get the ETO current

$$I_{on} = \frac{V_i}{T_j \bullet 0.00052 + 0.07118}. \qquad (5\text{-}4)$$

From (5-4) it can be seen that the proportion, addition, and division are needed to eliminate the temperature effect. This approach is too complicated for the analog circuit to realize within the ETO gate driver. And the calculation error can also be a problem.

Another approach is to send out the temperature information to the converter controller. And (5-4) is very easy to calculate by the microprocessor controller. In our design, the MOSFET temperature information is carried by the PWM switching frequency of the built-in current sensor. So the duty cycle of the PWM output of PG is proportional to V_i, and the frequency is proportional to T_c. With this approach, both the voltage and temperature of the MOSFET's are sent out by one PWM signal.

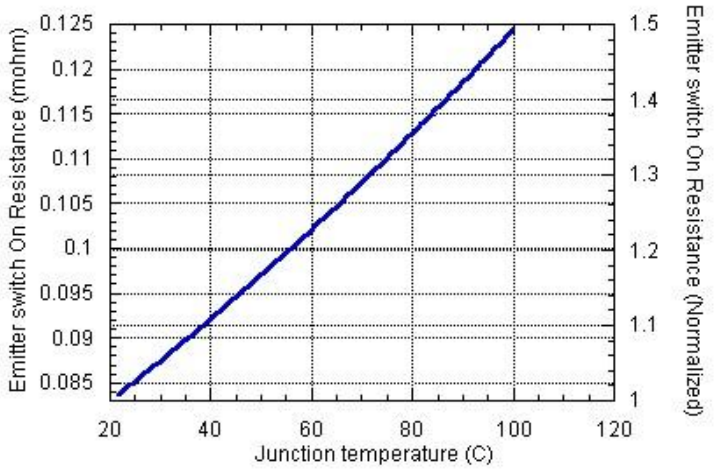


Fig. 5.8 Emitter switch on-resistance vs. temperature

5.2.5. Calculating the Converter Load Current from the Output of the ETO Built-in Current Sensor

The output of the ETO built-in current sensor can be used for the current control purpose. Fig. 5.9 shows a simplified circuit of an ETO phase leg for voltage source converter. Usually the load current sensing is needed for the current control of the converter. The ETO current I_{ETOP} and I_{ETON} can be measured by the ETO built-in current sensor. Fig. 5.10 shows a small period of the typical ETO current and diode current when the load current direction is positive (current going out of the phase leg). In this situation, the load current goes through the top ETO S_p and the bottom diode D_n alternatively. I_{ETOP} is the load current when it goes through the ETO. And the I_{DP} is the load current when it goes through the diode. I_{ETOP} can be measured by the ETO. I_{DP} can not be measured. However, because of the inductor filter and the load inductance, the load current changing rate dI_{load}/dt is limited. As can be seen in Fig. 5.10, it can be assumed that I_{DP} is equal to I_{ETOP} in the same switching cycle. There will be error caused by this assumption.

If the load and the inductors in the circuit are taken into account, the changing rate of the I_{DP} can be calculated. And the more accurate I_{DP} can be obtained. These methods will not be discussed in this chapter. When the load current is negative, the load current goes through the bottom ETO S_n and the top diode D_p alternatively. The situation is similar to that of the positive load current.

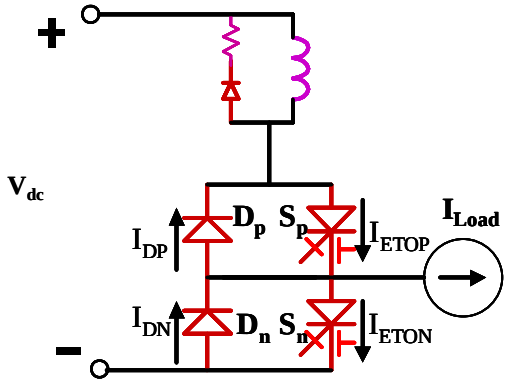


Fig. 5.9 Simplified circuit of an ETO phase leg.

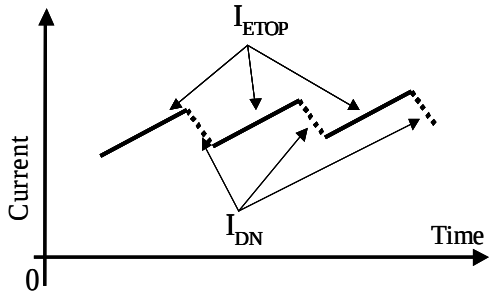


Fig. 5.10 The ETO current and the diode current.

Fig. 5.11 shows the flowchart of the load current calculation for one ETO phase leg. The ETO has an on/off status output though optical fiber, indicating the on and off status of the ETO. Both the built-in current sensor outputs and the on/off status output of the top

and bottom ETO's are received by the microprocessor controller through the optical fibers.

The first step is to find which ETO is in the on-state from the on/off status output. The second step is to calculate output PWM signal's duty cycle and the frequency of the ETO which is in on-state. If the duty cycle is equal to 50%, it can be known that the ETO is not conducting current- either the antiparallel diode is conducting current or the load current is zero. Otherwise, the ETO is conducting current. The current can be assumed to remain unchanged in within a switching cycle period. At the same time the load current direction can be known. The next step is the load current calculation base on the current-duty relationship shown in Fig. 5.5, and temperature compensation shown in (5-4). At last, the load current is updated.

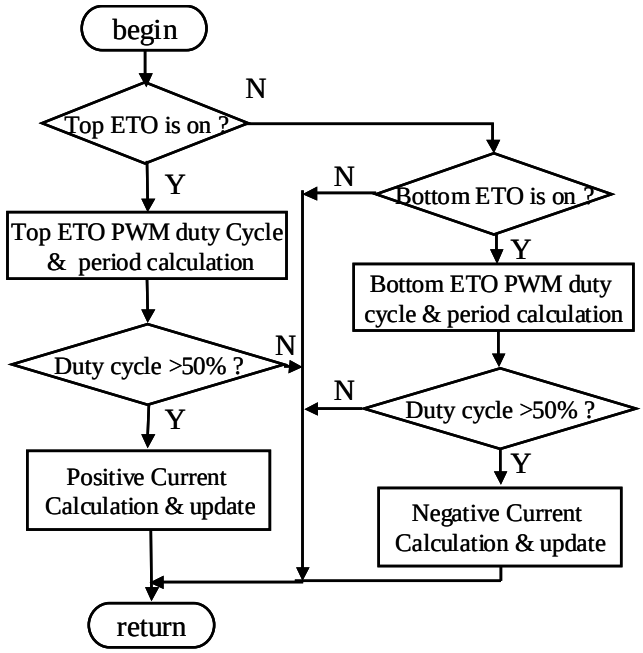


Fig. 5.11 The flowchart of the current calculation.

5.2.6. The Built-in Current Sensor of the Reverse Conducting ETO

If the reverse conducting GTO [B 35] is used, a reverse conducting ETO, RCETO, can be built. The RCETO equivalent circuit and circuit symbol are shown in Fig. 5.12. The reverse conducting ETO can conduct both the positive current whose direction is from anode to cathode, and the negative current whose direction is from the cathode to anode. During each situation, the emitter will be turned on and conduct current. Obviously, the voltage across the emitter switch will be positive when it is conducting positive current and negative when it is conducting negative current. With the same built-in current sensor, the output PWM duty cycle will cover from 0% to 100%. A duty cycle bigger than 50% indicates a positive current and lower than 50% indicates a negative current.

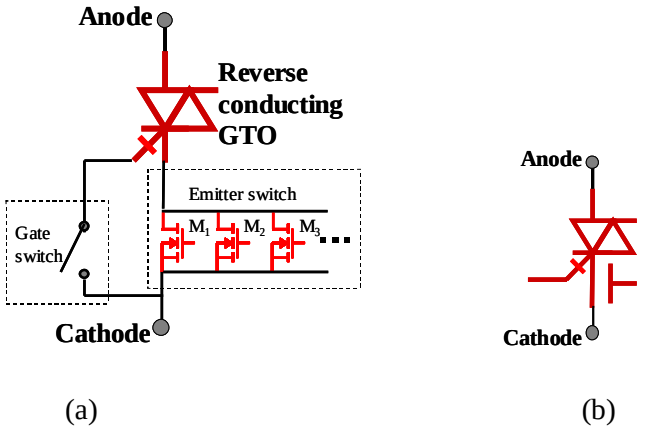


Fig. 5.12 The RCETO: (a) Equivalent circuit and (b) circuit symbol.

Fig. 5.13 shows a simplified circuit of a RCETO phase leg. Compared to the circuit shown in Fig. 5.9, the RCETO not only simplifies the phase leg circuit, but also simplifies the built-in current sensor. With the RCETO built-in current sensor, the load current can be easily calculated by (5-5).

$$I_{load} = I_{RCETOP} - I_{RCETON} \qquad (5\text{-}5)$$

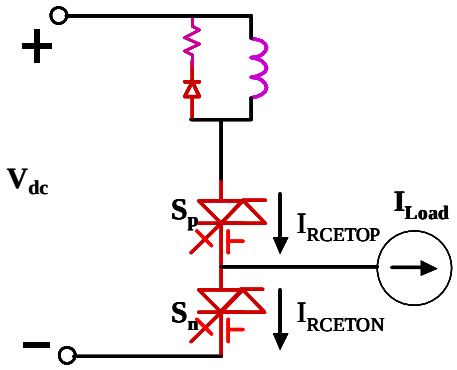


Fig. 5.13 Simplified circuit of a RCETO phase leg.

5.3. The ETO Over-Current Protection

The ETO can shut down the over-current fast and automatically due to its built-in current sensing function, fast turn off speed, and high current turn off capability. Based on the ETO built-in current sensor, the ETO over-current protection circuit was built. As can be seen in Fig. 5.14, the voltage signal V_i is also sent to a comparator and latch block (CL). In CL, V_i is constantly compared to a trigger voltage by a fast comparator. Once this voltage is bigger than the trigger voltage, the comparator will trigger the latch, and an over-current warning signal will be generated and locked. This signal is also sent to the over-current protection block to turn off the ETO. The ETO emitter switch temperature information V_t is also sent to CL. The trigger voltage can be adjusted by V_t. Then the over-current trigger value will not be affected by the temperature. The over-current warning signal is also sent out by the optical fiber. In some applications, the ETO may not be desired to turn off when over-current happens. In these situations, the over-current

warning signal can be used by the controller to freeze all the ETO's or trigger the circuit breaker to shut down the fault current.

It takes less than 500ns between the over-current triggering and the ETO emitter switch being turned off. The ETO storage time and the turn-off voltage rising time greatly depend on the main switch—the GTO being used. Normally, the ETO storage time is about 1us, and the turn-off voltage rising time is about 1μs. So it takes less than 3us between the over-current triggering and the ETO anode current starting to decrease, in another word, the ETO over-current protection delay is less than 3us.

The device over-current is usually caused by the short circuit, the malfunction, or the component failure. When these fault conditions happen, the current will lose control and rise until the over-current protection of the ETO triggers. In fault conditions, the current rising rate is limited by the di/dt snubber or the stray inductors of the circuit. If the current is below the maximum ETO turn-off current after the over-current protection delay, the ETO and the system can be safely protected.

Fig. 5.14 shows the over-current protection experimental relsults. Fig. 5.15 shows the protection waveform in detail. In this test, the ETO over-current trigger value was set to 3800A. The current rising rate was limited to 200A/us by the di/dt snubber. As shown in Fig. 5.15, when the ETO current rose to the trigger value at t_1, the ETO over-current protection was triggered. The ETO started to turn off. After about 200ns, the over-current warning signal was sent out by the optical fiber. Then the optical signal was transferred to electrical signal by another circuit for measurement. The signal is show in Fig. 5.14 and Fig. 5.15.

After the ETO gate driver turn-off delay time which is about 1us, the emitter switch starts to be turned off at t_2. Then the GTO turn-off process starts. When the ETO storage time finished at t_3, the ETO anode voltage started to rise. The ETO current continued rising until its anode voltage reached the DC link voltage at t_4. Fig. 5.15 shows that the ETO current began to decrease at about 4200A, at 2us after the over-current triggering. Then the ETO current decreased to zero in about 4us.

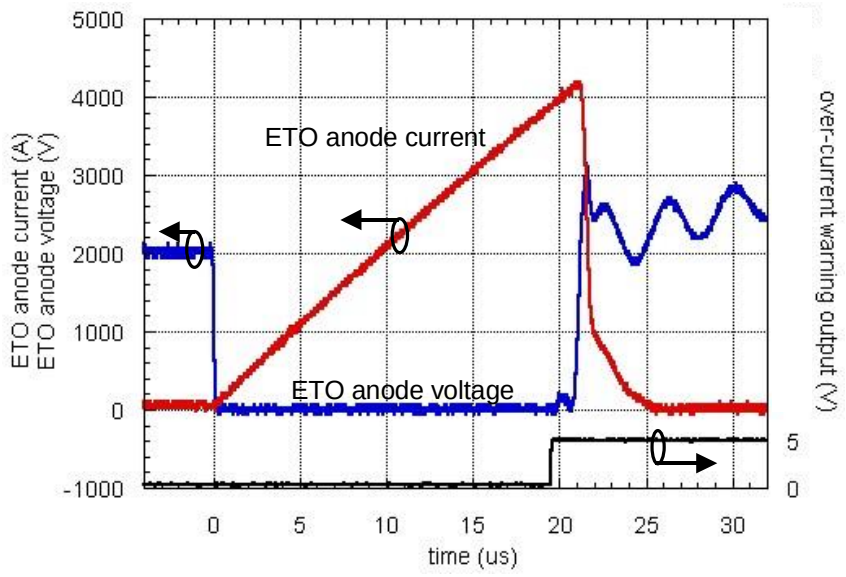


Fig. 5.14 The over-current protection waveform

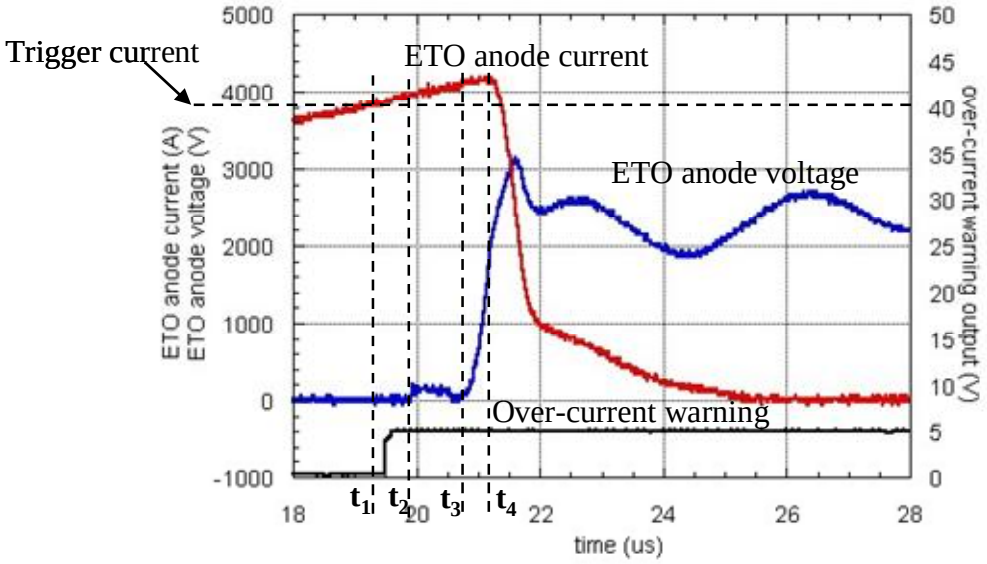


Fig. 5.15 The over-current protection transient waveform

5.4. Conclusion

The ETO built-in current sensor is a low cost, high precision, and convenient to use function. Experimental results show that the measurement error is below 1%. And the measurement delay is less than 25μs. This function can be easily used for the current control purpose. Due to its built-in current sensor, fast switching speed, and high current turn off capability, the ETO can shut down the fault over-current within a very short time. Test results show that it takes less than 3μs between the over-current triggering and the anode current stopping rising. The ETO's built-in current sensor and over-current protection function can be used to improve the performance, and reliability, as well as reduce the cost of the high power electronics systems.

Chapter 6. Investigation of the Turn-Off Capability of the ETO

The high-current turn-off capability is very important for ETO's safe operation, especially in the over-load and fault conditions. Both ETO's and IGCT's are based on hard-driven GTO concept, and they share the same turn-off failure mechanism. Until now, the exact failure mechanism of the hard-driven GTO is still not well understood.

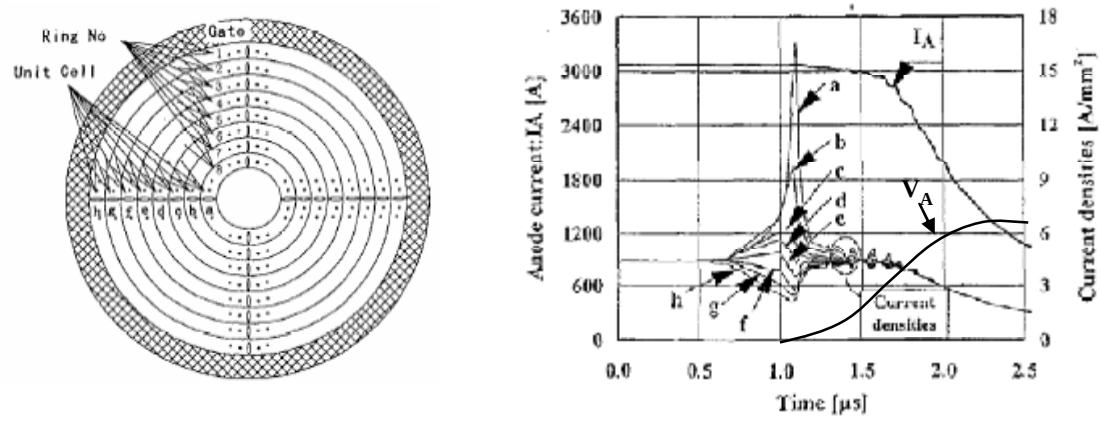
In this chapter, the methods to improve the turn-off capability of the ETO are investigated. Firstly, a comprehensive investigation of the turn-off failure mechanism of the hard-driven GTO is performed. A series of simulations are carried out to study the large area hard-driven GTO turn-off operation. The simulations show that the GTO will first reach on-set of dynamic avalanche and then enter the sustain mode avalanche if the anode voltage keeps increasing. Then a simplified approach using two parallel GTO's with different areas and different parameters is used to study the multi-cell GTO turn-off failure mechanism due to inhomogeneities. Based on the simplified approach, both the simulations and the experiments are carried out to investigate the hard-driven GTO failure mechanism. The conditions to cause the hard-driven GTO failure are presented. The approaches to improve the ETO's turn-off capability are discussed.

6.1. Introduction

The turn-off failure mechanism of the conventional GTO has been well studied. However, the exact failure mechanism of the hard-driven GTO is still not well understood. Since both ETO's and IGCT's are based on hard-driven GTO concept, they share the same turn-off failure Mechanism. According to our experiments, ETO's have

turn-off failures at 200kW/cm^2~300kW/cm^2 power density, similar to the IGCT failures reported in [B 24]. Such power density is still relatively low for the silicon material [B 25].

[B 27]- [B 30] shows that there is current non-uniform distribution among the GTO cells during turn-off. One of the authors' simulation results is shown in Fig. 6.1 [B 27]. In this simulation, GTO wafer was divided in to eight ring shape cells. Fig. 6.1 shows the current distribution inhomogeneity among the cells during the turn-off transient. In this simulation, the current distribution became uniform again when the voltage start to rise. So this inhomogeneity only causes small temperature inhomogeneity and will not likely lead to a turn-off failure directly.



(a) (b)

Fig. 6.1 GCT failure mechanism simulation: (a) simulation model and (b) anode current and current density on each unit cell waveforms

In [B 24], the authors attributed the turn-off failure to the on-set of dynamic avalanche. However, after dynamic avalanche, the anode voltage can still rise and the device may still be turn off. This phenomenon can be seen from their experimental results shown in

Fig. 6.2. Fig. 6.2 shows a successful GCT turn-off. At time t_1, it can be seen a decrease of the dV_{AK}/dt when I_A keeps constant. This phenomenon clearly indicates that the dynamic avalanche happens at time t_1. Since electrons start to be injected to the depletion region due to dynamic avalanche, the expanding speed the depletion region slows down, and as a result, the anode voltage increasing rate dV_{AK}/dt decreases. However, the anode voltage V_{AK} can still increase, because density caused by the dynamic avalanche is still less than the required GTO gate current. Therefore, the dynamic avalanche may not sufficiently cause the turn-off failure. This literature does not provide a further explanation.

The objective of this study is to provide a better understanding of the hard-driven turn-off failure mechanism and propose the way to improve the turn-off capability of the ETO, and further increase the reliability of the high power converter.

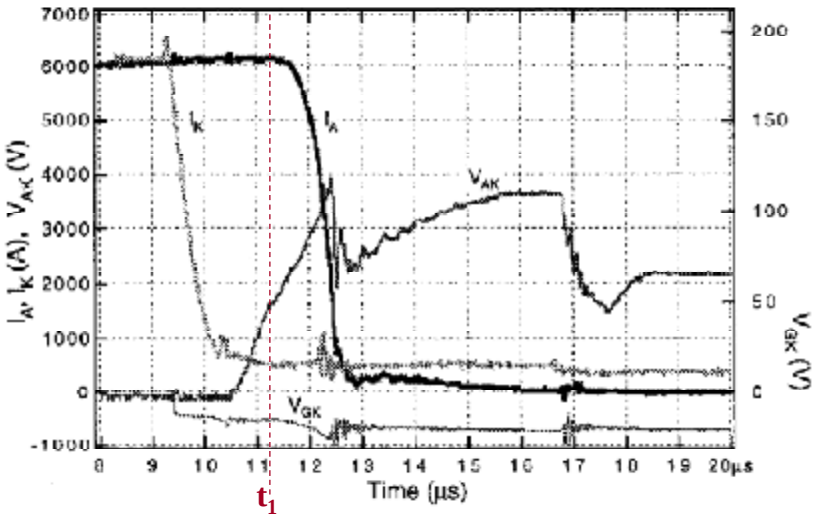
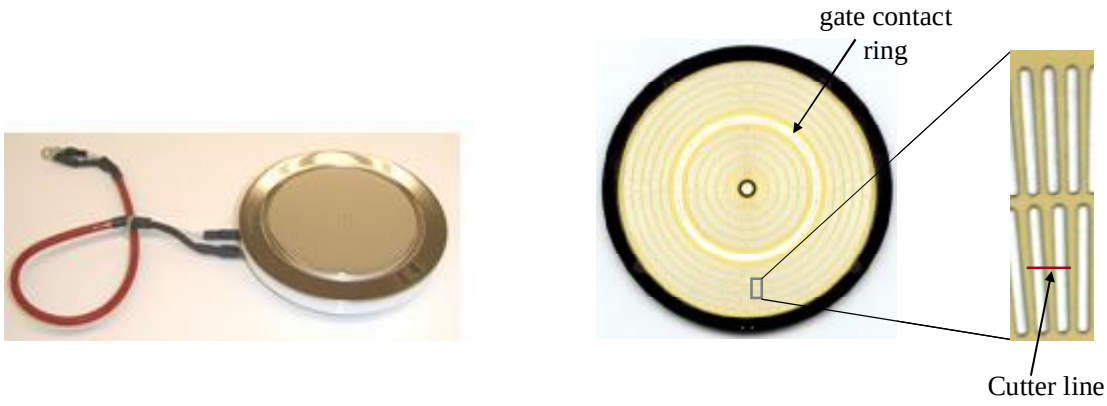


Fig. 6.2 GCT turn-off waveforms

6.2. GTO Structure and Static Avalanche Characteristics

Fig. 6.3 shows the picture, the wafer, and the details of cathodes islands of the transparent GTO (TGTO) 5SGT40L4502, which is used to build the ETO. This GTO has 4500V peak off-state voltage and 4000A maximum controllable turn-off current rating. In order to achieve the high current turn-off capability, a strongly interdigitated structure is used on the cathode side of the wafer. The purpose is to minimize the distance from the center of a cathode finger, which conducts large current in the conduction on-state, to the gate, which is used to extract the charge from the cathode region during turn-off. There are about 2700 cathode islands on the wafer. The wafer is about 8.5 cm in diameter. The cathode area islands are formed by etching away the surrounding silicon. The cathode islands contact directly to the metal, which serves as the cathode electrode. The cathodes islands are arranged in concentric rings around the device centre. The common gate contact is in the middle of the wafer in a ring shape.



(a) (b)

Fig. 6.3 The TGTO 5SGT40L4502 (a) the picture and (b) the wafer and a detail of cathodes islands

Fig. 6.4 shows the cross-section through two cathode islands along the GTO cutline indicated in Fig. 6.3 (b). Fig. 6.4 defines the locations and names of the contacts. The device consists of the four layers P1-N1-P2-N2, where P1 and N2 are the anode and cathode emitter regions respectively. N1 and P2 are the n-base and p-base. The transparent GTO is a type of punchthrough (PT) device [B 11]. There is an N-buffer layer located between the substrate region and the anode region. In the high voltage blocking state, the electric field is reduced to zero not in the lightly doped substrate region, but in the buffer layer. This buffer layer prevents the electric field from reaching through into the anode region. A PT device greatly reduces the wafer thickness than a non-punchthrough (NPT) device. Since the stored charge during conduction on-state decreases with decreasing wafer thickness, a PT GTO has much lower conduction and switching losses than the NPT GTO. One unique characteristic of the TGTO is its shallow low-efficiency anode emitter, which is different from the anode short type GTO. This gives TGTO such advantages as low turn-off loss and low trigger gate current [B 43], [B 44].

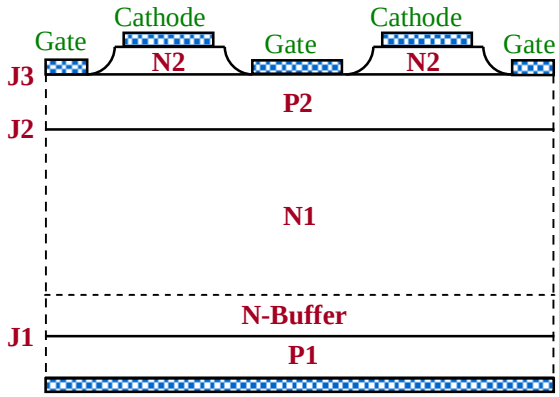


Fig. 6.4 The cross-section through a GTO along the cutline

Numerical simulations using ISE [A 14] were performed on a TGTO device. The GTO structure and the doping concentration are shown in Fig. 6.5. The GTO parameters are listed in Table 6.1. Default physical models for impact ionization, field dependant mobility, carrier-carrier scattering, Auger recombination, Fermi-Dirac statistics and band-gap narrowing are used. The carrier lifetime is fixed at 16μs for electrons and 4μs for holes by matching the simulated forward I-V with the experimental device. The length of the GTO is set to be 14700mm to match the area of the GTO 5SGT40L4502.

Fig. 6.6 shows the experimental result and simulation result of the GTO on-state characteristics. It can be seen that the simulation result meets the experimental results very well.

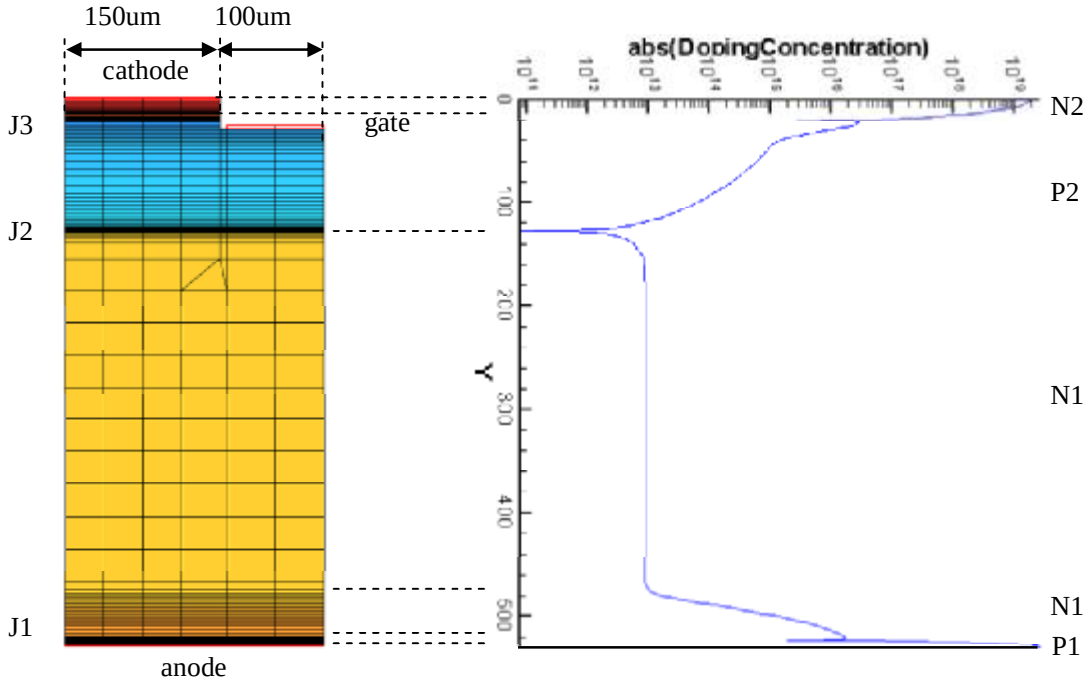
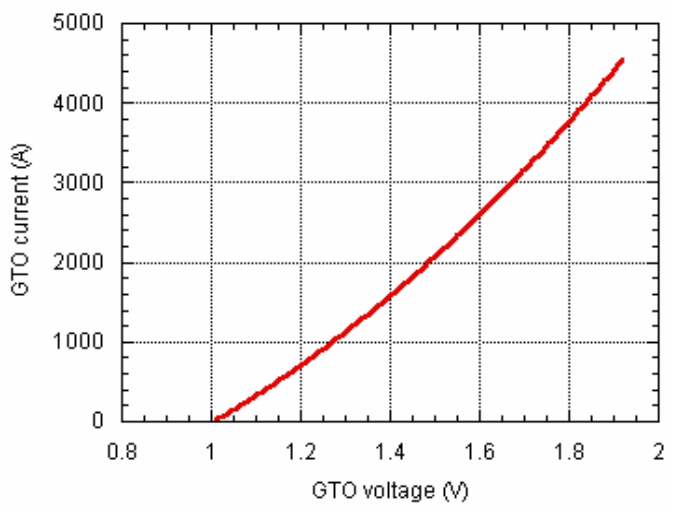


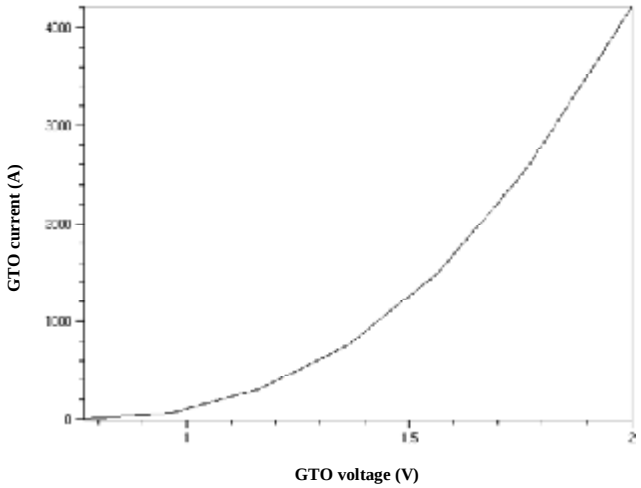
Fig. 6.5 The GTO structure and the doping concentration

Table 6.1 The parameters of the GTO

	Baseline (x0 y0 x1 y1) (μm)	diffusion	Peak concentration	Junction value	Depth (μm)
N+ emitter	0,0,150,0	Gauss	2e+19	1.4e+17	20
P+ base	0,0,250,0	Gauss	4.5e+17	1.8e15	45
P base	0,0,250,0	Gauss	2e+15	9e+12	128
substrate	-7.3,-14.7,258.4,600		9e+12		
N-buffer	0,530,250,530	Gauss	2.5e+16	9e+12	50
P+ emitter	0.2,530,250,530	Gauss	2.7e+19	1.6e+16	8



(a)



(b)

Fig. 6.6 The on-state characteristics of the GTO: (a) experimental result (b) simulation result by ISE.

Doping concentration and electric field of the studied GTO at static voltage blocking are shown in Fig. 6.7. Such a trapezoidal field profile is typical for PT GTO. Fig. 6.8 shows the static avalanche breakdown of the studied GTO obtained by ISE. Fig. 6.8 (a) shows the circuit for simulation. V_A is gradually until GTO is break down. Fig. 6.8 (b) shows the simulation result. The break down voltage of the GTO model is about 5200V, which meets the real GTO very well.

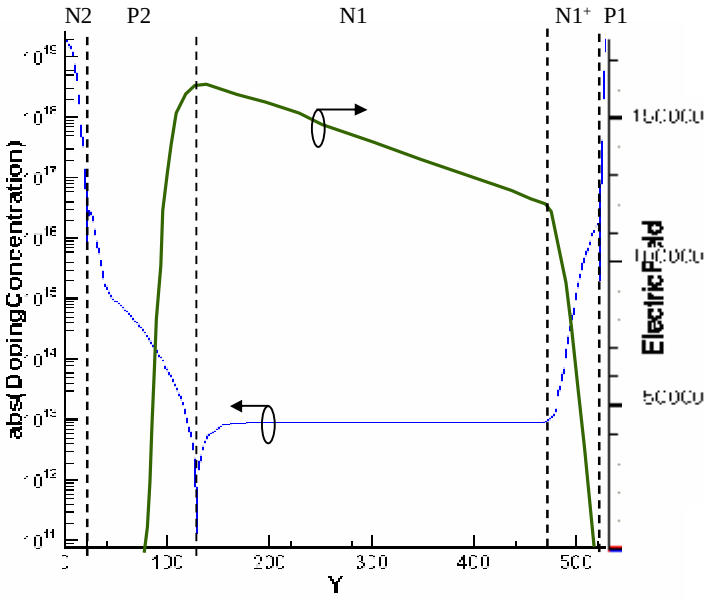
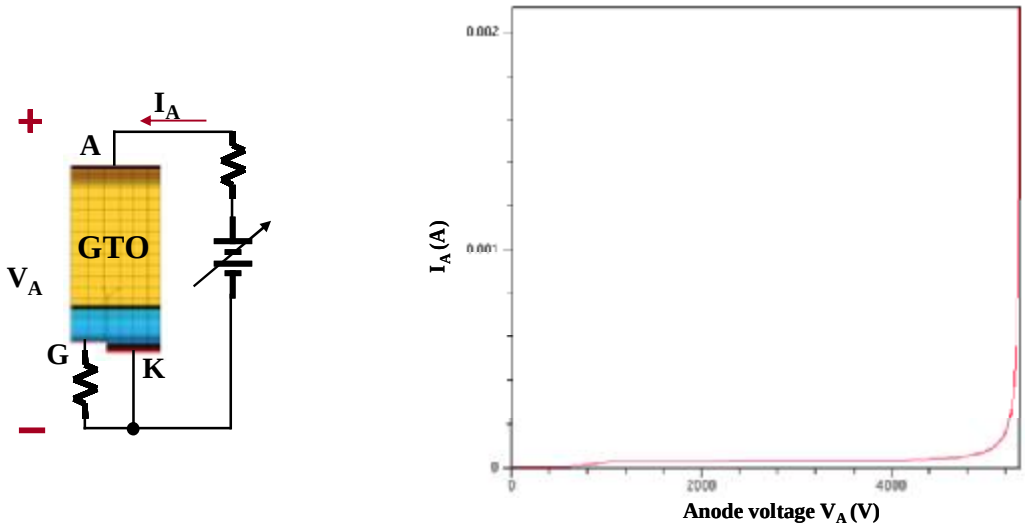


Fig. 6.7 Doping concentration and electric field at static voltage blocking



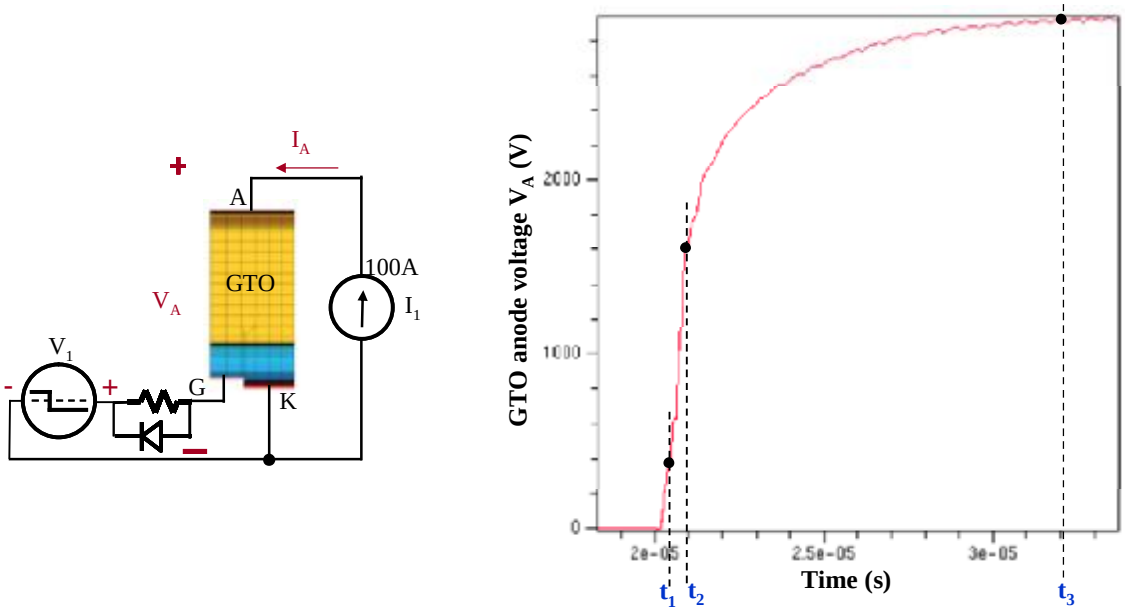
(a) (b)

Fig. 6.8 The static avalanche breakdown of the studied GTO obtained by ISE: (a) circuit diagram and (b) simulation result

6.3. The Turn-Off Operation of the Hard-Driven GTO

Based on the GTO model developed in Fig. 6.5 and Table 6.1, GTO turn-off operation is studied. In this simulation, the area of the GTO is set to be $1cm^2$. Firstly, the GTO is turned off with a constant current source, which is equivalent to an inductive load, applied across its anode and cathode. The circuit diagram is shown in Fig. 6.9 (a). The simulation result of the GTO anode is shown in Fig. 6.9 (b).

After studying the anode voltage changing slope dV_A/dt of the in Fig. 6.9 (b), it can be seen that before time t_2 dV_A/dt is almost kept constant. At time t_2, dV_A/dt starts to decrease. At time t_3, dV_A/dt reaches zero, and the anode voltage stops rising. Time t_1 is chosen between the time when anode starts to rise and time t_2. The simulation results of the electron concentrations and electric field evolution at t_1, t_2, t_3 are shown in Fig. 6.10.



(a) (b)

Fig. 6.9 The GTO turn-off operation: (a) the circuit diagram, and (b) the simulated GTO anode voltage during turn-off

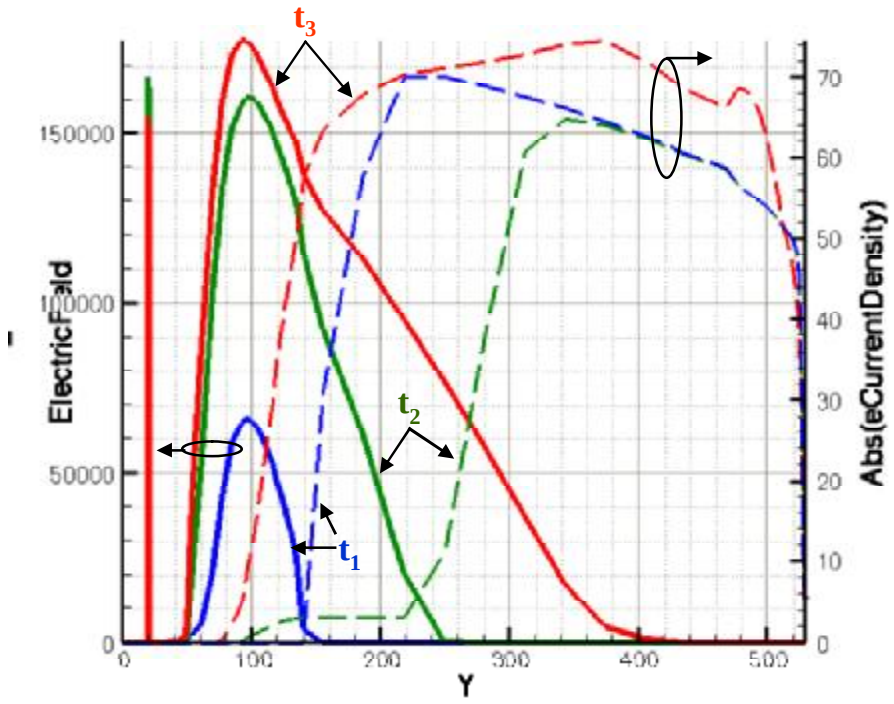


Fig. 6.10 The electron concentrations and electric field evolution during the GTO turn-off

6.3.1. The Operation of the Anode Voltage Rising Period before Time t_2

When unity turn-off gain is established, the electron injection at the cathode emitter stops, and the hard-driven GTO is turning off as an open base transistor mode. Anode current flows through the n-base and p-base and then flows out of the gate. The absence of the electron injection from the cathode emitter results in net extraction of minority carriers from the n-base, since a constant load current has to be maintained due to the inductive load characteristics. The net carrier extraction results in an expansion of the depletion region. Then the open base PNP transistor voltage rise at a very rapid rate to support the expansion of the depletion region at the p-base /n-base junction. The other current component that can be sustained without depletion region expansion is the normal

PNP collect diffusion current. This operation refers to the time when anode voltage starts to rise shown in Fig. 6.9 (b). Fig. 6.11 illustrates the schematic diagram showing the electrical field and carrier distributions at time t_1.

As shown in Fig. 6.11, a highly modulated boundary layer exists between the depletion region and the quasi-neutral region. The carrier profile in the quasi-neutral region is the same as the GTO in the forward conduction state. A linear carrier distribution approximation can be used in the boundary region [B 23]. At the left hand side of the boundary layer, holes are extracted away from the modulated boundary region. Due to the high electric field prevalent in the depletion region, the holes pass through the depleting region to the p-base at their saturation velocity, v_{sat}. The electron current at the left hand side of the boundary layer is almost zero, which is proved by the simulation results shown in Fig. 6.10. As can be seen from Fig. 6.10 that, at time t_1, the electron current density at the depletion region, where the electric field exists, is almost zero. Therefore, the current component in the depletion region is almost only the hole diffusion current:

$$q \cdot p \cdot v_{sat} = J_p + J_n \approx J_p \qquad (6\text{-}1)$$

At the right hand side of the boundary layer, electron current flows out of the boundary layer, results in the net carrier extraction from the boundary layer and expansion of the depletion region, as shown in Fig. 6.11. The boundary layer moves toward the GTO anode with the expansion of the depletion region. The carrier distribution keeps unchanged inside the boundary layer because the linear carrier distribution is assumed in the boundary layer.

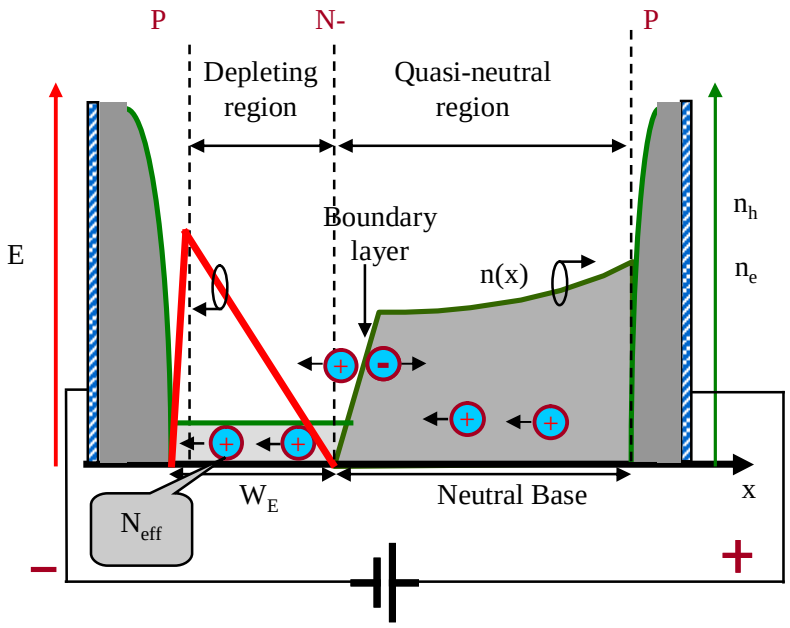


Fig. 6.11 Schematic diagram showing the electrical field and carrier distributions at time t_1.

The holes which are passing through the depleting region to the p-base at their saturation velocity strongly determines the current density controlled effective doping, N_{eff}. (6-2) shows the relationship between N_{eff} and the GTO anode current density J_A.

$$N_{eff} = N_D + p - n = N_D + \left(\frac{J_p - J_n}{q \cdot v_{sat}} \right) \approx N_D + \left(\frac{J_p}{q \cdot v_{sat}} \right) \approx \frac{J_A}{q \cdot v_{sat}} \qquad (6\text{-}2)$$

where J_p and J_n are hole and electron current density in the PN junction depletion region.

The electric field distribution in the drift region is determined by effective doping N_{eff}. Poisson's equation in the drift region is

$$\frac{dE(x)}{dx} = -\frac{q}{e} N_{eff} \approx -\frac{q}{e} p \qquad (6\text{-}3)$$

The presence of the holes in the drift region alters the electric field distribution in the drift region. As shown in Fig. 6.11, the slope of the electric field profile is greatly

increased, leading to a triangular electrical field profile, quite different from the trapezoidal field profile during the static voltage block shown in Fig. 6.7.

6.3.2. The Operation of the Dynamic Avalanche Period between Time t_2 and Time t_3

As the anode voltage increases with the expansion of the depletion region, the peak value of the electric field profile increases as well. When the peak electric field reaches a certain value, dynamic avalanche occurs, creating electron-hole pairs within the depletion region.

After the onset of avalanche in the drift region of the open-base transistor, the peak electric field can be assumed to be a roughly fixed value E_c.

$$E_c = 2 \cdot 10^5 V / cm \tag{6-4}$$

Since the voltage is supported by the depletion region, it reaches a critical value when the maximum depletion region width is

$$W_E = \frac{e_s E_c}{qN_{eff}} \tag{6-5}$$

where

$$e_s = 11.7 \cdot 8.85 \cdot 10^{-14} F / cm \tag{6-6}$$

$$V_{sat} = 10^7 cm / s \tag{6-7}$$

So the on-set voltage for dynamic avalanche

$$BV_{dy} = \frac{1}{2} E_c W = \frac{1}{2} E_c \frac{e_s E_c}{qN_{eff}} \tag{6-8}$$

For large J. using (6-2) and neglect N_D, one gets

$$BV_{dy} = \frac{1}{2}\frac{e_s E_c^{\,2} v_{sat}}{J} \qquad (6\text{-}9)$$

And, the power density at the on-set point is

$$P_{dy,onset} = BV_{dy} J = \frac{1}{2} e_s E_c^{\,2} v_{sat} \qquad (6\text{-}10)$$

From (6-4), (6-6), (6-7), and (6-10) we can get

$$P_{dy,onset} = 206 kW / cm^2 \qquad (6\text{-}11)$$

So the peak power density of about 200kW/cm^2 is power density required to cause the on-set of the dynamic avalanche. The high N_{eff} results in a triangular electrical field profile, making the on-set of dynamic avalanche well below the static breakdown voltage.

The diagram showing the electrical field and carrier distributions at the on-set of the dynamic avalanche is shown in Fig. 6.12. The electron-hole pairs are created by the dynamic avalanche. Now at the left hand side of the boundary layer, there are electrons passing through the depleting region to the n-base at their saturation velocity. The electron current at the left hand side of the boundary layer can be seen from the simulation results shown in Fig. 6.10. It can be seen from Fig. 6.10 that, at time t_2, the electron current density at the depletion region, where the electric field exists, is not zero. Therefore, now the current component in the depletion region consists of both the hole diffusion current and the electron diffusion current.

After on-set of dynamic avalanche, the GTO is normally not in the sustain-mode dynamic avalanche, because the carriers generated by the dynamic avalanche are not enough to form a sustainable current, and hence, the depletion region will continue to expand. Then the carriers generated by the dynamic avalanche plus the carriers extracted

due to the expansion of the depletion region support the load current. The depletion region expands at a slower rate because the electrons and holes generated by the avalanche contribute to the load current. Then the voltage increases at a lower dV_A/dt. The on-set of the dynamic avalanche is clearly indicated by the anode voltage changing slope dV_A/dt, shown in Fig. 6.9 (b). At time t_2, dV_A/dt starts to decrease, indicating the dynamic avalanche occurs.

An important phenomenon is the electron current density at the depletion region alters the effective doping N_{eff}, and further alters the electric field profile.

Now Poisson's equation in the drift region is

$$\frac{dE(x)}{dx} = -\frac{q}{e} N_{eff} \approx -\frac{q}{e}(p-n) \qquad (6\text{-}12)$$

Compared with (6-3), it can be seen that the slope of the electric field profile is decreased, which means higher voltage can be support given the same peak electric field.

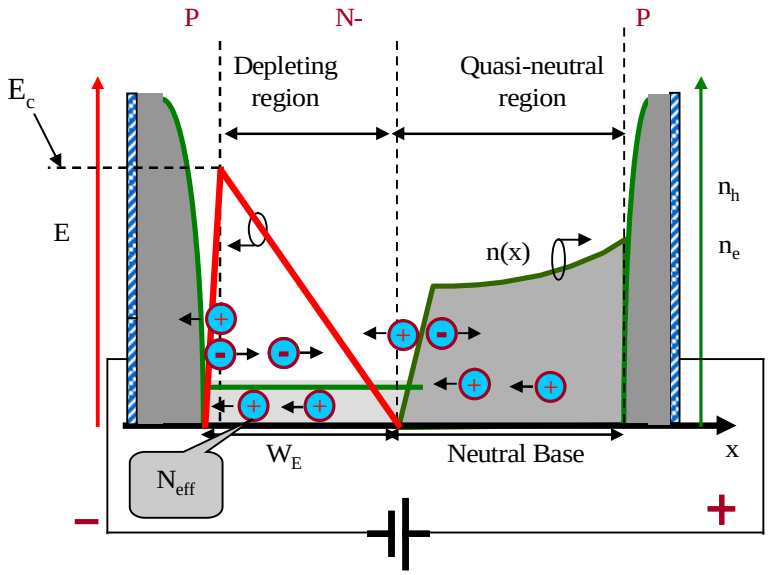


Fig. 6.12 diagram showing the electrical field and carrier distributions at time t_2.

6.3.3. The Operation of the Sustain Mode Dynamic Avalanche Period after Time t_3

As the anode voltage keeps increasing, more and more electron-hole pairs are generated, and eventually the avalanche generated carriers will be enough to provide the total anode current. The depletion region will stop expanding. Then the anode voltage will not increase and the GTO enters its sustain mode dynamic avalanche. The stable anode voltage is therefore the sustain mode dynamic avalanche voltage. The sustain mode dynamic avalanche is clearly indicated by the anode voltage's changing slope dV_A/dt, shown in Fig. 6.9 (b). At time t_3, dV_A/dt decrease to zero, indicating the sustain mode dynamic avalanche occurs. The diagram showing the electrical field and carrier distributions at time t_3 is shown in Fig. 6.13.

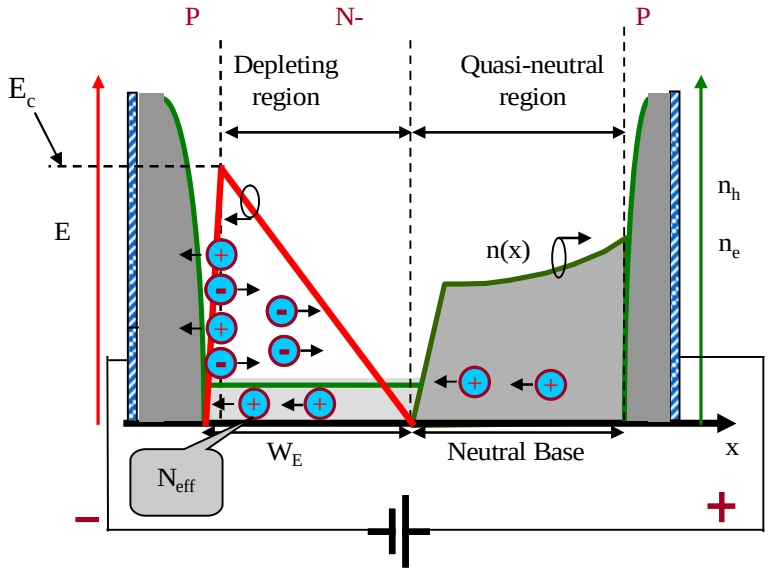


Fig. 6.13 diagram showing the electrical field and carrier distributions at time t_3.

The sustain mode dynamic avalanche is a stable situation and the GTO can stay in that condition if there is no temperature rise and the GTO wafer is ideally homogeneous.

Therefore the sustain mode of dynamic avalanche boundary in the J-V plane can be considered as the theoretical Reverse Bias Safe Operating Area (RBSOA) of the GTO.

Altering the current source I_1 value and repeating the simulations, we obtain the simulated dynamic avalanche voltage and sustain mode dynamic avalanche voltage at different current density, as shown in Fig. 6.14.

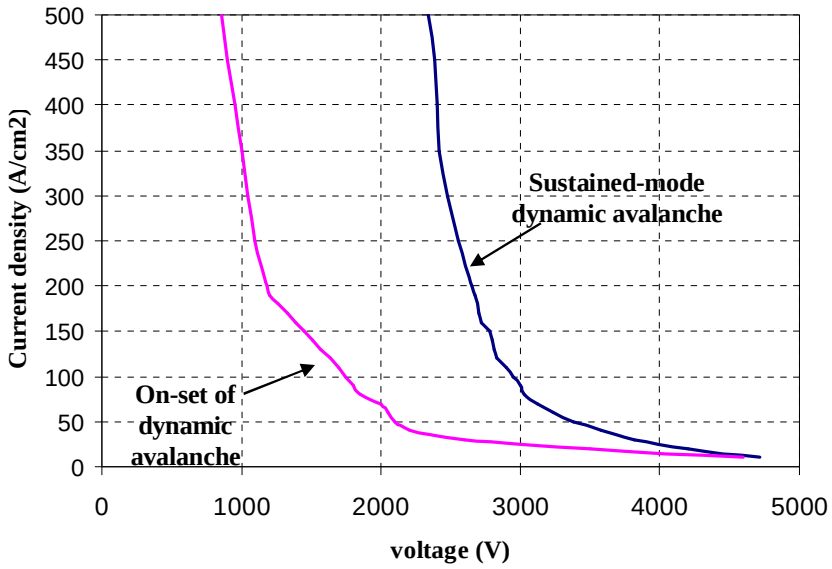


Fig. 6.14 the simulated dynamic avalanche voltage and sustain mode dynamic avalanche voltage at different current density

After reaching sustain mode dynamic avalanche, both the holes and electrons are passing through the depleting region to the p-base at their saturation velocity.

The hole current density (J_p) at the depletion region is

$$J_p = a_{PNP} \cdot J_A \tag{6-13}$$

where α_{PNP} is the current gain of the PNP transistor of the GTO.

The electron current density (J_n) at the depletion region is

$$J_n = (1 - a_{PNP}) \cdot J_A \tag{6-14}$$

Then the current density controlled effective doping, N_{eff}, is

$$N_{eff} = N_D + p - n = N_D + \left(\frac{J_p - J_n}{q \cdot v_{sat}} \right) = N_D + \left(\frac{2a_{PNP} - 1}{q \cdot v_{sat}} \right) \cdot J_A \approx \left(\frac{2a_{PNP} - 1}{q \cdot v_{sat}} \right) \cdot J_A \tag{6-15}$$

Substituting (6-15) into (6-8), we can get the sustain mode dynamic avalanche voltage

$$BV_{sutain\_dy} = \frac{1}{2} E_c W = \frac{1}{2} E_c \frac{e_s E_c}{q N_{eff}} = \frac{1}{2} \cdot \frac{e_s E_c^2 v_{sat}}{J_A} \cdot \frac{1}{(2a_{PNP} - 1)} \tag{6-16}$$

(6-16) indicates that the sustain mode dynamic avalanche voltage will be increased with the decreasing of the gain of the PNP transistor, α_{PNP}. This effect is shown in Fig. 6.15.

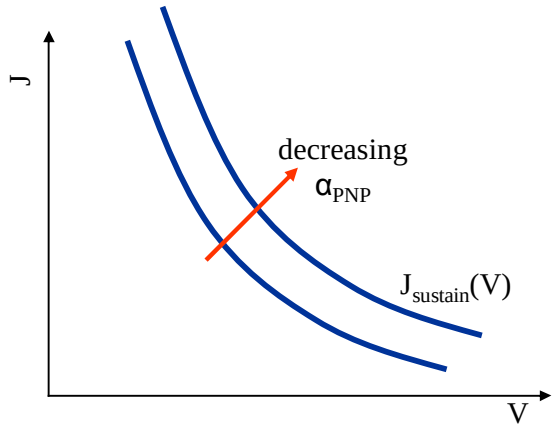


Fig. 6.15 The sustain mode dynamic avalanche voltage with α_{PNP} being decreased

6.4. The Multi-Cell GTO Turn-Off failure Mechanism Due to Inhomogeneities

6.4.1. Modeling Approach

The above theoretical RBSOA is only realizable under isothermal and homogeneous condition. This is almost impossible to realize in reality. To study hard-driven GTO turn-off stress, especially the localized high power stress existing in large area GTO, the inhomogeneity within the GTO must be included. Local differences such as edge current fringing, non-uniform carrier lifetime and/or doping between the GTO segment (cells) lead to current density inhomogeneity in the large area GTO which in turn results in local areas of higher stress during turn-off.

Inhomogeneities in large area GTO are caused probably by the following mechanisms. Firstly, in order to control the GTO on-state conduction or switching characteristics, deep level recombination centers are introduced. If those recombination centers or impurities are introduced nonuniformly, non-uniform lifetime will be generated. Non-uniform lifetime will cause non-uniform initial carrier distribution in the GTO wafer, and further cause the current density inhomogeneity during the GTO on-state current conduction. Secondly, non-uniform P^+ anode region doping can cause inhomogeneity in carrier plasma because of the differences in injection efficiency. The edges and corner regions of the GTO may have higher initial plasma concentration than the rest of the device due to the two-dimensional current spreading effect. Third, the field crowding at the edge of the diode may introduce lower breakdown voltage [B 25].

Ideally, the above inhomogeneities should be studied by directly simulating the multi-cell GTO. The direct multi-cell model should include small parts which have different

characteristics from the normal region such as different doping concentration, different lifetime, or different avalanche voltage. Those small regions and the normal region should be connected through joining regions which make the parameters variation continuous. However, because of the huge number of finite elements needed to describe such a multi-cell device, a complete simulation of the multi-cell device is virtually impossible considering the capability and simulation efficiency of the current available numerical simulators. A simplified modeling approach is necessary. The objective of the investigation is focused on the fundamental failure mechanisms of the hard-driven GTO, not trying to exactly match the simulation results with the experimental data. Our approach is to use two paralleled 1-D GTO's structures with different areas. The large GTO represents the normal uniform portion of GTO, and the small GTO represents the special region. The area ratio N determines the final current filament density in the special region, because the worst case is that the small GTO carries the total current. So the maximum current density of the small GTO is

$$J_{S,\max} = N \cdot J_L \tag{6-17}$$

where J_L is the current density of the large GTO.

The inhomogeneity that causes the current filament can be introduced by varying parameters of the small GTO, such as lifetime, ionization rate, or doping concentration.

Fig. 6.16 shows the circuit diagram used to study the hard-driven GTO turn-off failure mechanism. The GTO model developed in Fig. 6.5 and Table 6.1 is used for the large GTO and small GTO. For the large GTO, the carrier lifetime is fixed at 16μs for electrons and 4μs for holes. The area factor is about 14500mm for the large GTO and 1450mm for the small GTO. The area is about $40cm^2$ for the large GTO, which matches the real GTO.

The area is $4cm^2$ for the small GTO. So a total current of 4000A indicates the current density of the large GTO is about $100A/cm^2$.

Voltage source V_1 is used to control the turn-on and turn-off of the large GTO and small GTO. Initially, both of the GTO's are off, and V_1 is -18V. $V_A=V_{dc}=2000V$. Then V_1 is changed to 30V, applying 3A to the GTO gates to turn on the GTO's. After GTO's are on, V_{dc}, a 2000V voltage source, applies across the inductor L_1, causing current I_A increasing linearly. After 100μs, I_A increases to 4000A. V_1 is changed to -18V to turn off the GTO's with $dI_G/dt=-6000A/\mu s$, which is similar to the ETO's turn-off dI_G/dt. Then V_A starts to increase, forcing L_1's current to flow to the clamp circuit C_1 and D_1. Then V_A has a voltage peak caused by the parasitic inductor L_2 and C_1's voltage. Finally the current through L_1 decreases to zero. And V_A returns to 2000V.

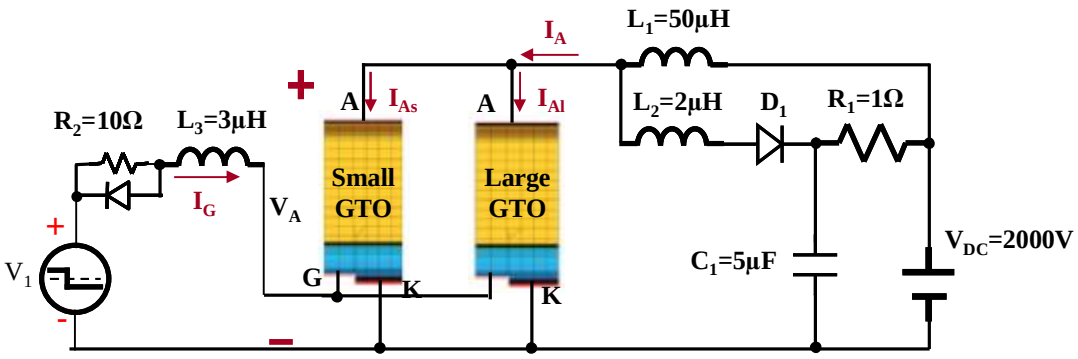


Fig. 6.16 Paralleled 1-D GTO model used in the simulation to study the GTO turn-off failure mechanism.

6.4.2. Simulation Results and Analysis

Firstly, we run the simulation by setting the parameter of the small GTO same as the large GTO. Fig. 6.17 shows the simulation results. The GTO's successfully turn off at 4000A. The waveforms of the simulation results meet very well with those of the experimental data shown in Fig. 2.19 and Fig. 2.20.

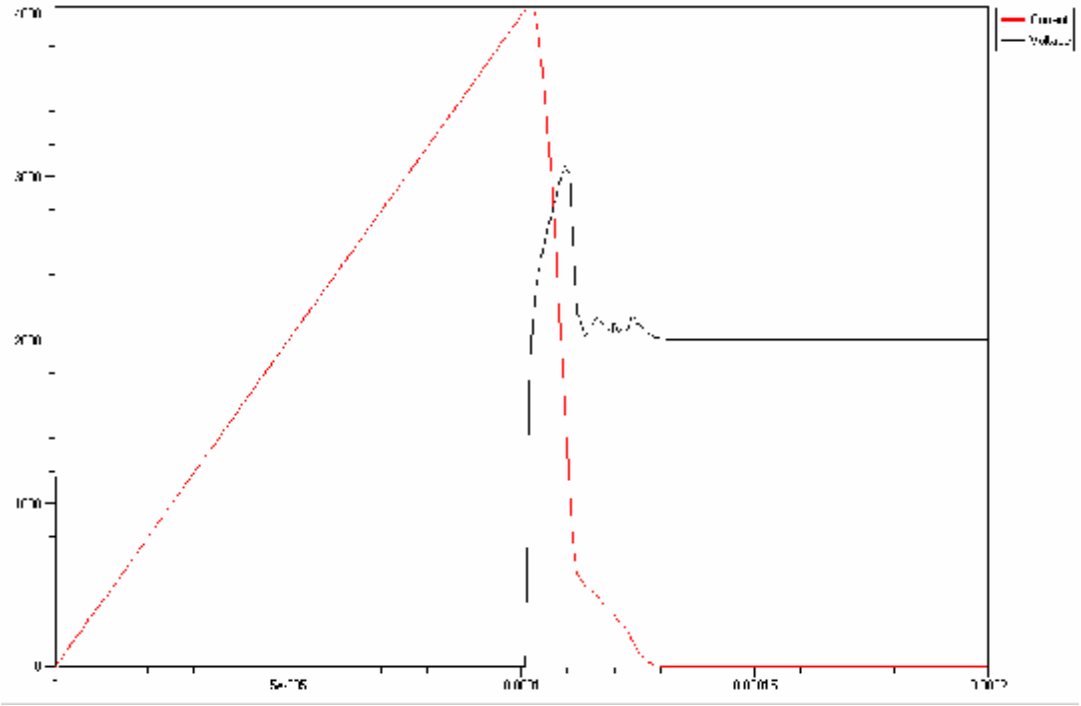


Fig. 6.17 The simulated turn-off waveforms when the large GTO and small GTO have the same parameters

In the next simulation, the small GTO's lifetime is increased from 16μs to 18μs for electrons and from 4μs to 6μs for holes. Fig. 6.18 shows the simulated turn-off waveforms. The longer lifetime makes the initial forward current density in small diode almost two times larger than that of the large GTO. As can be seen from Fig. 6.18 (a), before the GTO's turning off, the large GTO's current density is about 100A/cm^2 while

small GTO's current density is about 200A/cm^2. The difference of the current density results in large inhomogeneity in initial carrier plasma. The onset of dynamic avalanche voltage is therefore significantly changed. As the anode voltage reaches the dynamic avalanche voltage of the small device, the current in the small GTO increases quickly.

After a very short time, there is a sudden anode voltage drop, as can be seen in Fig. 6.18 (c). It can be seen that when the anode voltage decreasing occurs, the anode voltage is still below DC-link voltage, V_{DC}, indicating that the total current through GTO is still kept constant.

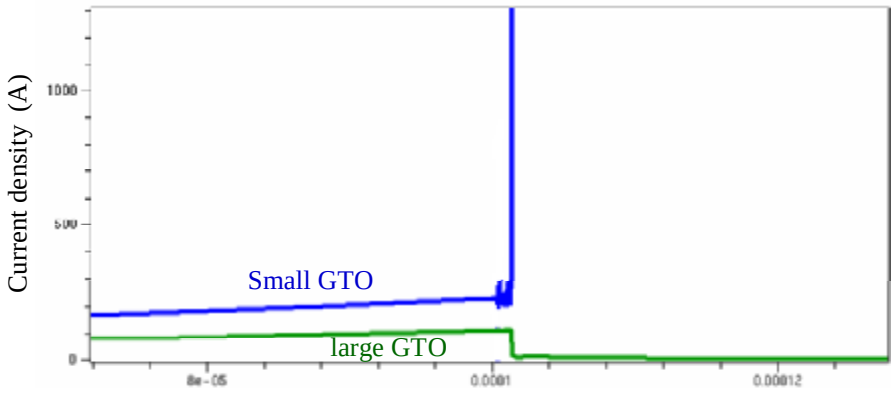
If GTO is turned off as open-base transistor mode and the GTO anode current is kept constant, two conditions must be satisfied to have an anode voltage decrease.

First, one or several small regions of the GTO must reach sustain mode dynamic avalanche. We know after on-set of dynamic avalanche, the carriers generated by the dynamic avalanche are not enough to support the total anode current and the space charge region will continue to expand (although at a slower rate) and the voltage will increase at a lower dV/dt. Only when GTO reach sustain mode dynamic avalanche the avalanche generated carrier can support the total anode current and the anode voltage will stop increasing.

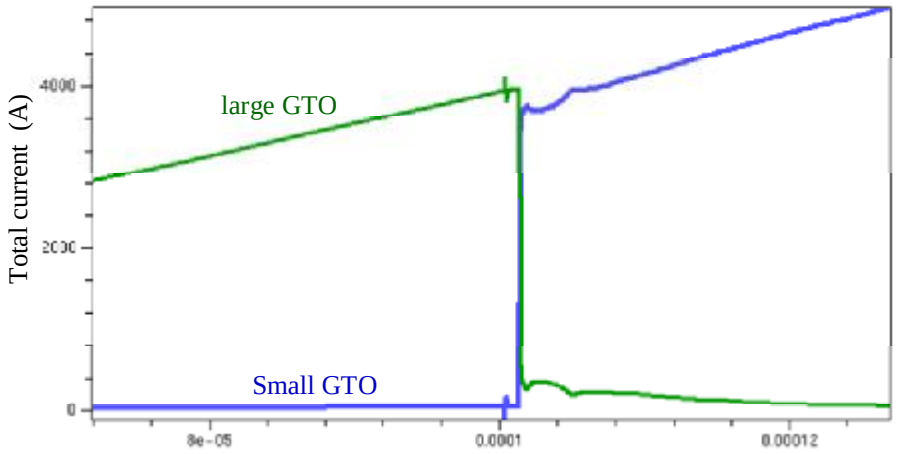
Second, negative differential resistance (NDR) exists in sustain mode dynamic avalanche voltage. When one or several small regions of the GTO must reach sustain mode dynamic avalanche, the anode voltage of those regions will stop increasing. More current will tend to flow through those regions. If NDR exists, the anode voltage will decrease, making current further crowd toward those regions. Such a positive feedback

will eventually cause the total current flowing through those small regions. As shown in Fig. 6.14, such an NDR characteristic always exists in the GTO devices.

When the small GTO reaches the sustain mode dynamic avalanche, the current density increases very fast until the total current of the large GTO diverts to the small GTO. Finally, the current of the large GTO decreases to zero, and the small GTO takes the total current, as shown in Fig. 6.18 (b). The anode voltage decreases to a very small voltage, indicating that the turn-off operation is not successful. The total GTO current keep increasing, and its rising slop is only limited by the inductor L_1. Since the area of the small GTO is 100 times smaller than that of the large GTO. The current density of the small GTO is increased 100 times, leading to a very large power stress. If the temperature effects are included, the temperature of the small GTO will rise to a very high value (larger than 1800 K). The high temperature will form hot spots in the GTO and destroy the device permanently in the form of a melted through holes. The end result of such failure is frequently referred as thermal runaway or thermal instability.



(a)



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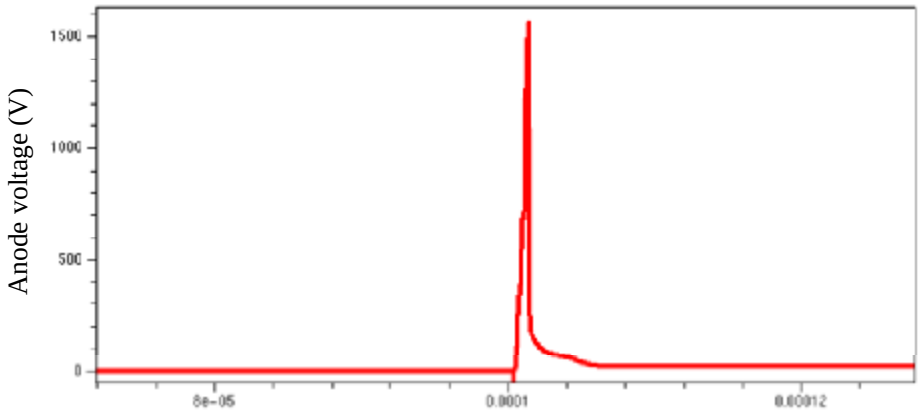

(c)

Fig. 6.18 The simulated turn-off waveforms when the small GTO has longer lifetime than the large GTO: (a) current density, (b) total current and (c) GTO anode voltage

Fig. 6.19 illustrates the GTO total anode current, anode voltage, and the trajectories of the small GTO and large GTO during turn-off. Suppose the initial current is J_{O_S} for the small GTO and J_{O_L} for the large GTO. J_{O_S} is larger than J_{O_L} due the inhomogeneity of the GTO.

At time t_1, GTO starts to turn off, and the anode voltage starts to increase.

At time t_2, the current density of the small GTO, $J_{small}(V)$, reaches the on-set dynamic avalanche trajectory $J_{d\_avalanche}(V)$ before the large GTO, since J_{O_S} is larger than J_{O_L}. Then the depletion region of the small GTO tends to expand at a slower rate because the electrons and holes generated by the avalanche contribute to the anode current. However, since the large GTO conducts most of the current, the anode voltage is determined by the large GTO. So the expansion of the depletion region of the small GTO does not slow down. As a result, more current will flow through the small GTO due to the carriers generated by the avalanche plus the carriers generated by the depletion region expansion. The current density of the small GTO starts to increase as shown in Fig. 6.19.

At time t_3, the large GTO reaches $J_{d\_avalanche}(V)$, and the anode voltage rising rate slows down. The current density increasing rate of the small GTO is decreased because the depletion region expansion speed is decreased.

At time t_4, the GTO anode voltage reaches the DC bus voltage, and the anode current starts to decrease. The current density of both the small GTO and large GTO starts to decrease. However, the GTO anode voltage continues increasing due to the parasitic inductance of the clamp circuit.

After time t_5, both GTO anode voltage and anode current decrease. The current density trajectories of both the small GTO and large GTO start to move far away from the sustain mode dynamic avalanche trajectory $J_{sustain}(V)$.

From Fig. 6.19 it can be seen that from time t_2 to time t_5, $J_{small}(V)$ strongly move toward $J_{sustain}(V)$. It is necessary to prevent $J_{small}(V)$ from reaching $J_{sustain}(V)$ for the successful turn-off.

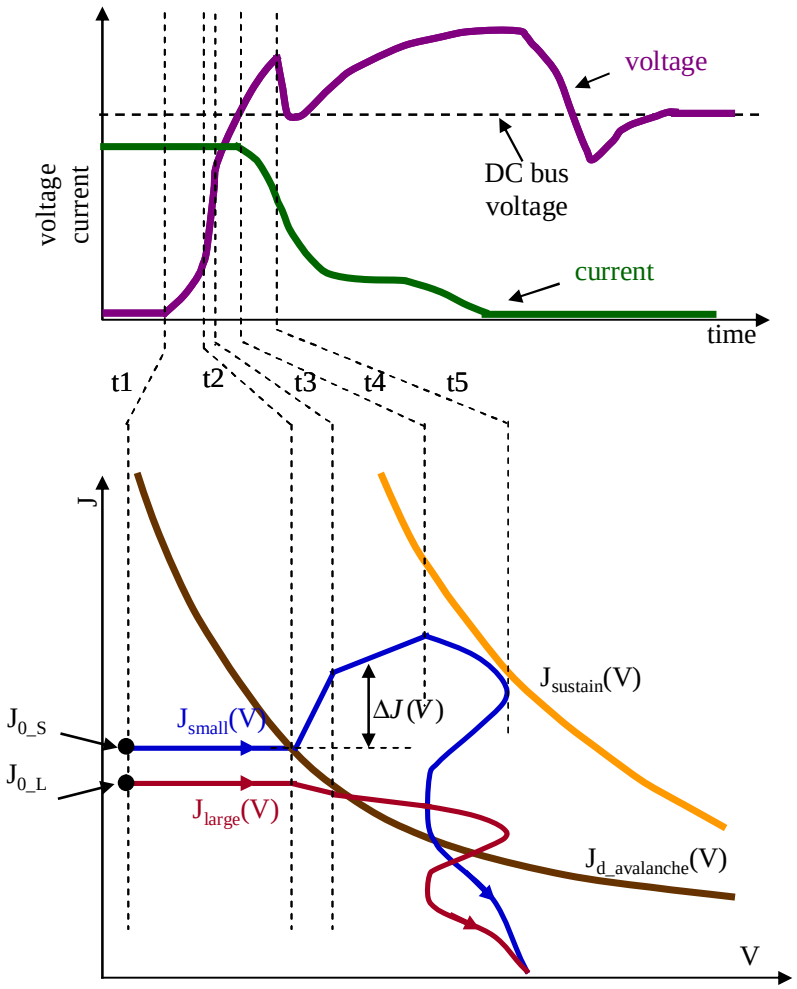

Fig. 6.19 The anode voltage, total anode current waveforms and the trajectories of the small GTO and large GTO during turn-off

6.4.3. Experimental Results and Discussions

Fig. 6.20 shows the experiments to study the hard-driven GTO turn-off failure mechanism. The circuit diagram for the experiment is the same as that in the simulation shown in Fig. 6.16, except that V_{DC}=2500V. The ETO is used to study the failure mechanism.

At time t_1, the anode current reaches about 4300A. Emitter switch is turned off to turn-off ETO. The emitter switch voltage rises to about 110V immediately, forcing the GTO cathode current divert to GTO gate.

At time t_2, emitter switch voltage drops to a low value, indicating that GTO cathode current decreases to zero and gate current equals to the anode current. The unity turn-off gain is achieved.

At time t_3, the GTO storage time ends, and the anode starts to rise.

At time t_4, dV_A/dt starts to decrease, indicating that the majority of the GTO regions reach the on-set of the dynamic avalanche.

At time t_5, the ETO anode voltage reaches the DC bus voltage. The load current starts to be diverted to the clamp circuit, and ETO anode current starts to decrease.

At time t_6, the ETO anode voltage has a sudden decrease. It is believed that several small GTO regions reach the sustain mode dynamic avalanche. The total anode current flows through those small GTO regions, leading to a very large power stress. The temperature of those small GTO regions rises very fast to a very high value and generates hot spots within a few microseconds. The hot spots destroy the GTO permanently in the form of melted through holes, leading to short circuits among all the GTO terminals. Then GTO draws all the current back from the clamp circuit. An anode current peak due to the reverse recovery of the clamp diode is observed. The voltage spike of the emitter switch is caused by the anode current spike with a high di/dt flowing through the gate parasitic inductor. Eventually, ETO conducts the total current with a very low voltage drop due to the GTO short circuit. The ETO turn-off operation fails. Fig. 6.21 shows the

picture of the GTO wafer and the failure points. It can be clearly seen the melted-through holes on the GTO wafer.

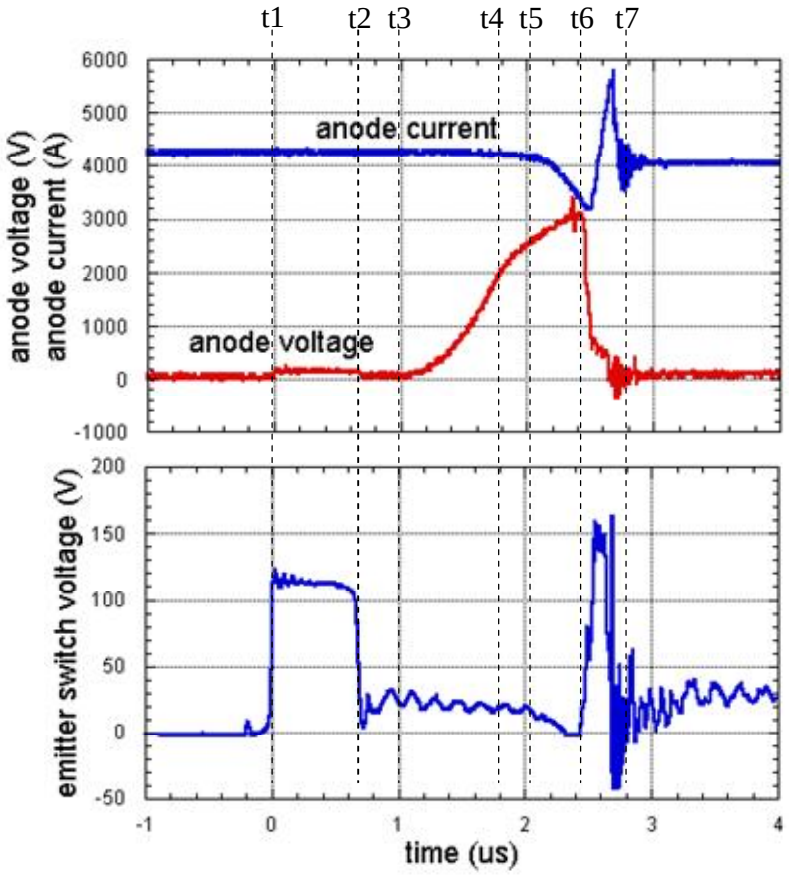

Fig. 6.20 The experimental results during a hard-driven GTO turn-off failure

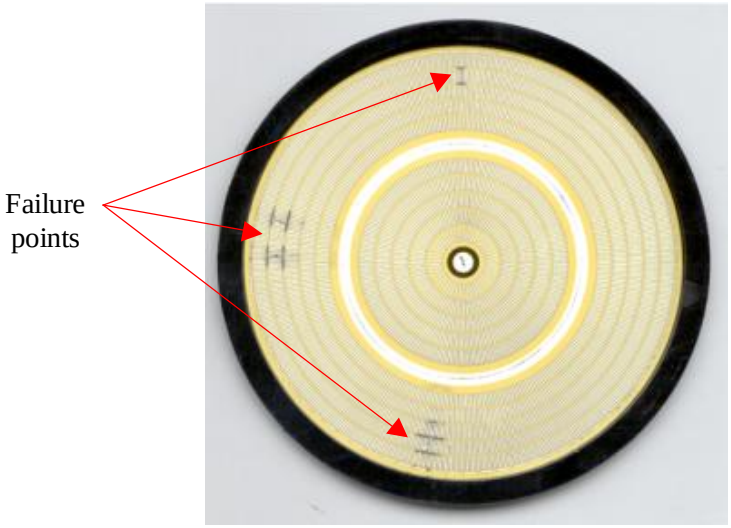

Fig. 6.21 The picture of the GTO wafer with failure points

From the above simulations and experiments, it is concluded that the hard-driven GTO turn failure would happen if the following conditions are satisfied

Condition (1): $N \cdot J_{O\_S} > J_{sustain}(V)$

Condition (2): $\Delta J(V) \geq J_{sustain}(V) - J_{0\_S}$

Condition (3): NDR exits in sustain mode dynamic avalanche voltage

Condition (1) means that there is enough current to push the small cell to the sustain mode dynamic avalanche. This condition is typically true in large GTO if N is also large. Condition (2) means the inhomogeneity within the GTO must be large enough to cause the small cell to reach the sustain mode dynamic avalanche. The current filament always happens between time t_2 to time t_5 shown in Fig. 6.19. Condition (3) means that negative differential resistance must exist to cause a positive feedback for the current crowing

when the small cell reaches sustain mode dynamic avalanche, so that the total current is squeezed into the small cell and causes the over stress of the small cell.

There are two main approaches to enlarge the RBSOA.

The first approach is to enlarge the sustain mode dynamic voltage. From (6-16) it can be seen that we can decrease the current gain α_{PNP} of the PNP transistor to increase the sustain mode dynamic avalanche voltage. This approach mainly targets to the condition (1). Apparently, if $J_{sustain}(T)$ is increased, more current can be safely turned off without reaching the sustain mode dynamic avalanche. α_{PNP} can be decreased by reducing the anode doping concentration or increasing the n-base buffer doping concentration. However, reducing α_{PNP} will increase the GTO's trigger current and the on-state voltage drop [A 15]. Therefore, tradeoffs have to be made among the ETO characteristics.

The second approach is to increase the homogeneity among the GTO cells. This approach is achieved by the following aspects.

- Increase the homogeneity of the carrier lifetime and doping concentration among the GTO cells

As we discussed in the simulations, increasing the homogeneity of the carrier lifetime and doping concentration will cause the current more uniformly distributes among the GTO cells during turn-off $\Delta J(V)$ in condition (2) will decrease, leading to a higher RBSOA.

- Increase the dI_G/dt of turn-off gate current.

As shown in Fig. 6.3, the GTO wafer consists of several thousands of small GTO cells, each of which has a cathode island. The cathodes islands are arranged in concentric rings around the device centre. The common gate contact is in the middle of the wafer in a ring

shape. The GTO cells closer to the gate contact ring have smaller parasitic gate resistance and inductance than those of the GTO cells further to the gate contact ring.

During a hard-driven GTO's turn-off transient, the GTO cells nearer to the gate contact ring transfer earlier into transistor mode with the recovery of the gate-cathode junction, because the negative gate current through those GTO cells rises faster due to their smaller parasitic gate resistance and inductance. The GTO cells nearer to the gate contact ring are turned off earlier than those GTO cells further to the gate contact ring. Therefore during turn off, current tends to crowd into those GTO cells remote to the gate contact ring. If the turn-off current is not very large, the current distribution inhomogeneity can be corrected by hard-driven GTO's transistor mode turn-off. In the transistor mode turn-off, the GTO cells with higher current turn off faster because higher carrier extraction results in faster expansion of the depletion region. Eventually the turn-off operations of all the GTO cells tend to become homogenous. However, when turn-off current approaching RBSOA, the GTO cells with the highest current density may reach the sustain mode dynamic avalanche, leading to a turn-off failure. So it is still important to improve the current distribution homogeneity during the turn-off transient. The most efficient way to improve the current distribution homogeneity among the GTO cells is to increase rising rate of the gate current, because the time difference to transfer into transistor mode among all the GTO cells will be decreased.

For IGCT, increasing rising rate of the gate current can be achieved by decrease the gate loop inductance. However, this approach is finally limited by the GTO gate structure. ETO does not have such limit, since rising rate of the gate current can be increased by increase the voltage block rating of the emitter switch. Therefore, ETO has

higher potential than IGCT to improve the current distribution homogeneity among the GTO cells during turn-off.

6.5. Conclusions

The high-current turn-off capability is very important for ETO's safe operation, especially in the over-load and fault conditions. Both based on hard-driven GTO concept, ETO's and IGCT's share the same turn-off failure mechanism. In this chapter, methods to improve the turn-off capability of the hard-driven GTO's are investigated. Firstly, numerical and experimental analyses of the hard-driven GTO turn-off failure mechanism are preformed. The simulations show that the GTO will first reach on-set of dynamic avalanche and then enter the sustain mode avalanche if the anode voltage keeps increasing. The dynamic avalanche and the sustain mode avalanche of the GTO are studied. The sustain mode of dynamic avalanche boundary in the J-V plane can be considered as the theoretical RBSOA of the GTO. Because of the inhomogeneity and thermal consideration existing in the real GTO, the turn-off failure will occur at a power density which is much lower than the RBSOA determined by the sustain mode dynamic avalanche. A simplified approach using two parallel GTO's with different areas and different parameters is used to study the multi-cell GTO turn-off failure mechanism due to inhomogeneities. After introducing inhomogeneity between the large and small GTO's, a current bump occurs in the small GTO. It is shown that the current bump happens because the small GTO reaches the on-set of the dynamic avalanche before the large GTO does. Such current bump rises from current filament formation. If the current density of the filament reaches the sustain mode dynamic avalanche, a current crowing

with a positive feedback will occur, leading to the thermal running away and GTO turn-off failure.

The RBSOA of the hard-driven GTO can be enlarged by decrease the gain of the PNP transistor of the GTO. However, this approach has to trade off with GTO turn-on trigger current and on-state voltage drop. Increasing the homogeneity of the carrier lifetime and doping concentration among the GTO cells will improve the RBSOA. RBSOA can also be enlarged by increasing the turn-off gate current dI_G/dt.

Chapter 7. Summary and Future Work

7.1. Summary

Advancements in the power electronics systems have been directly related to the availability of improved power semiconductor devices. The device performance greatly determines the efficiency, reliability, volume, and cost of the power electronics system. This dissertation is dedicated to develop an advanced high power semiconductor device, the emitter turn-off (ETO) thyristor, which is targeted to improve the limitations of the present high power devices.

This dissertation investigates the following topics related to the development and analysis of the ETO:

- The Major Electrical and Mechanical Improvements in the Advanced ETO

The first generation ETO has a low current turn-off capability, low manufacturability, and the abnormal failure issue caused by the GTO parasitic diode. The new electrical and mechanical designs are proposed improve those limitations. The new generation ETO has 5000A snubberless turn-off capability, improved turn-on capability, low conduction and switching loss, high reliability, high manufacturability, and low cost. The abnormal failure caused by the GTO parasitic diode is eliminated as well. ETO's high power high frequency operation is successfully demonstrated in a megawatt H-bridge voltage source converter.

- The Innovative Self-Power Generation Method of the ETO

An innovative self-power generation method of the ETO is presented. ETO has three operation modes: start up mode, active switching mode, and inactive switching mode. ETO has a simple and low power loss circuit to get power for start-up. In active switching mode, ETO obtains gate drive power through its charging turn-on operation. In inactive switching mode, ETO suppresses its unnecessary turn-on when its anti-parallel diode is conducting current to save gate drive power. By this approach, ETO achieves complete optically controlled turn-on and turn-off and all the internal power required is self-generated. The Innovative self-power generation method of the ETO is demonstrated by the experiment.

- A Novel Integrated Method to Eliminate the Dead-Time Requirement of the ETO

A novel integrated method to eliminated the dead-time requirement is introduced and experimentally demonstrated. By this method, the turn-on operation of the ETO which works in inactive mode is suppressed. If the load current does not change direction, only one of the upper ETO and lower ETO within one phase leg keeps switching and the other ETO is kept off. Therefore, the shoot-through problem will not happen. By connecting two optical fibers between the upper and lower ETO within a phase leg, ETO's can receive the fully complementary PWM commands (without dead-time). This method the which not only improves the output waveform quality but also increases the reliability and reduces the cost of the high power PWM voltage source converters.

- The Built-in Current Sensor and Over-Current Protection of the ETO

During on-state, The ETO current will go through both the GTO and the emitter switch MOSFET's. These MOSFET's can be used for the current sensing purpose since voltage drop across the MOSFET's reflects the current through them. Based on this principle, a method to measure the ETO current and transfer the current information to a PWM signal whose duty cycle is proportional to the current value is proposed. Experimental results show that the measurement error is below 1%. And the measurement delay is less than 25μs. Based on the ETO's built-in current sensor, the over-current protection function of the ETO is designed as well. Due to its fast switching speed and high current turn off capability, the ETO can shut down the fault over-current within 3μs.

- Investigation of the Turn-Off Capability of the ETO

The high-current turn-off capability is very important for ETO's safe operation, especially in the over-load and fault conditions. Both ETO and IGCT are based on hard-driven GTO concept, and they share the same turn-off failure mechanism. A comprehensive investigation of the turn-off failure mechanism of the hard-driven GTO was performed. The simulations show that the GTO will first reach on-set of dynamic avalanche and then enter the sustain mode avalanche if the anode voltage keeps increasing. The sustain mode of dynamic avalanche boundary in the J-V plane can be considered as the theoretical RBSOA of the GTO. Because of the inhomogeneity and thermal consideration existing in the real GTO, the turn-off failure will occur at a power density which is much lower than the RBSOA determined by the sustain mode dynamic avalanche. The RBSOA of the hard-driven GTO can be enlarged by decreasing the gain

of the PNP transistor of the GTO. However, this approach has to trade off with GTO turn-on trigger current and on-state voltage drop. Increasing the homogeneity of the carrier lifetime and doping concentration among the GTO cells will improve the RBSOA. RBSOA can also be enlarged by increasing the turn-off gate current dI_G/dt.

7.2. Future Work

- Reduce the start-up voltage of the ETO's self-power generation function

According the design presented in Chapter 3 of this dissertation, the start-up voltage of the ETO is about 500V. In some applications, a lower start-up voltage may be desirable. Of course we can reduce R_1 in Fig. 3.12 to reduce the start-up voltage. However, this approach will increase the power consumption of R_1. Therefore a more efficient approach to achieve a lower start-up voltage is necessary.

- Investigation the dead-time elimination function in the multi-level converters

This dissertation proposed a dead-time elimination function which is very successful in the two level converters. However, this approach can not be directly applied in the multi-level converters such as neutral point clamped (NPC) converter, since in NPC converter the upper and lower ETO's do not operate in fully complementary mode any more. Therefore a further investigation of this method in multi-level converter is important.

- Further investigation of the ETO's failure mode and reliability

It is believed that GTO's will safely short circuit under all worst case failure conditions. Although according to our experiments ETO's always fail in short circuit, a

comprehensive study of how the MOSFET's which are connected in series with the GTO affect the ETO's failure mode is still necessary. In addition, the study of the failure in time (FIT) of the ETO is valuable to provide a better understanding of ETO's reliability.

Appendix. A Comparison of ETO's, IGCT's, and HVIGBT's for High-Power Converters

In the Appendix, a comprehensive comparison and evaluation of ETO's, IGCT's, and HVIGBT's for high-power converters are performed.

Firstly, the loss characteristics of the three devices are compared. A comparison of the IGBT and hard-driven GTO in terms of the forward conduction voltage drop (V_F) vs. turn-off loss (E_{off}) tradeoff based on the device structure is performed. Then a comparison of the total losses of ETO, IGCT, and IGBT in three voltage source converter phase legs is conducted.

Based on three voltage source converter phase legs, the device's impacts on the converter construction and design are discussed. Then the comparisons of ETO's, IGCT's, and IGBT's based on voltage and current scalability, device gate drivers, protection, reliability, and cost are performed.

A.1. Introduction

The previous chapters, the advanced ETO is developed and the failure mechanism of the hard-driven GTO's is performed. It is imperative to compare the ETO with the other state of the art power devices.

Although GTO's have been the dominated fully controllable devices the high power conversion area, it is being increasingly replaced by IGCT's and HVIGBT's. Therefore, IGCT's and HVIGBT's are chosen to do the comparison with ETO's. 5SHY 35L4511 [B

36] IGCT produced by ABB and CM900HB-90H [C 6] IGBT produced by Mitsubishi are selected for the comparison. The ETO, 5SHY 35L4511 IGCT, and CM900HB-90H IGBT all have 4500V voltage blocking capability. The silicon areas of all of the three devices are also similar.

To perform a comprehensive comparison and evaluation of the devices, not only the three devices' characteristics are compared, but also three two-level voltage source converter phase legs, which use the ETO's, IGCT's, and IGBT's as the main switches respectively, are compared and evaluated.

Fig.A. 1 shows the circuit diagram of the two-level voltage source converter phase leg using IGBT's as the main switches. The IGBT converter phase leg operates without any snubber to minimize the part count. The freewheeling diodes (D_p and D_n) are imbedded within the IGBT modules. The DC-link voltage is 2500V. The auxiliary power supply, transformer, and the rectifiers are used to provide the isolated power inputs for the IGBT gate drivers. A current sensor is required for the current control. The controller provides PWM signals with dead-time to the gate drivers of the upper and lower IGBT's ($IGBT_p$ and $IGBT_n$). The dead-time compensation function is implemented within the controller to reduce the output harmonics caused by the dead-time. IGBT's have over-current protection function. When over-current occurs, warning signals are generated by the IGBT gate drivers and then deliver to the controller through optical fibers.

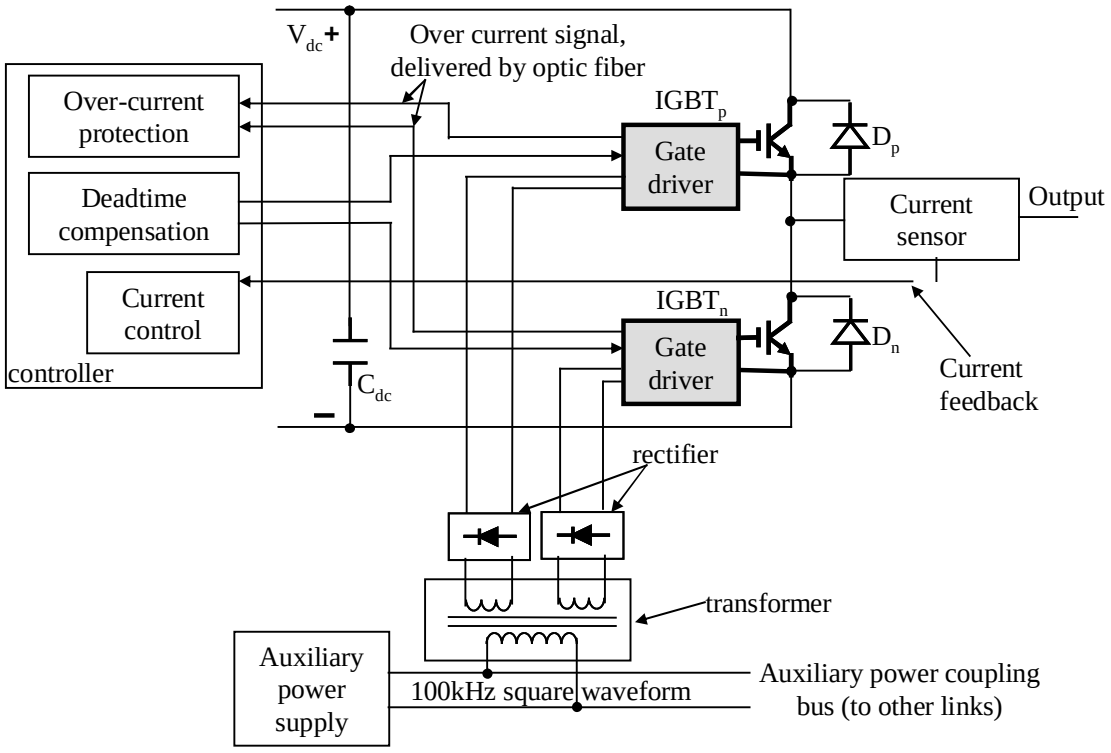

Fig.A. 1 The circuit diagram of the two-level voltage source converter phase leg using IGBT's as the main switches

Fig.A. 2 shows the circuit diagram of the two-level voltage source converter phase leg using IGCT's as the main switches. The DC-link voltage is 2500V. The fast recovery diode 5SDF10H4502's [B 37] are used for the freewheeling diodes (D_p and D_n). The current rising rate of IGCT's is limited to about di/dt=600A/μs by a di/dt snubber to protect the freewheeling diodes. L_c of di/dt snubber is about 4μH. dv/dt snubbers are not included due to IGCT's snubberless turn-off capability. The auxiliary power supply and transformer are used to provide the isolated power inputs for the IGCT gate drivers. A current sensor is required for the current control. The controller provides PWM signals with dead-time to the gate drivers of the upper and lower IGCT's ($IGCT_p$ and $IGCT_n$). The dead-time compensation function is implemented within the controller to reduce the

output harmonics caused by the dead-time. The over-current protection function is implemented within the controller.

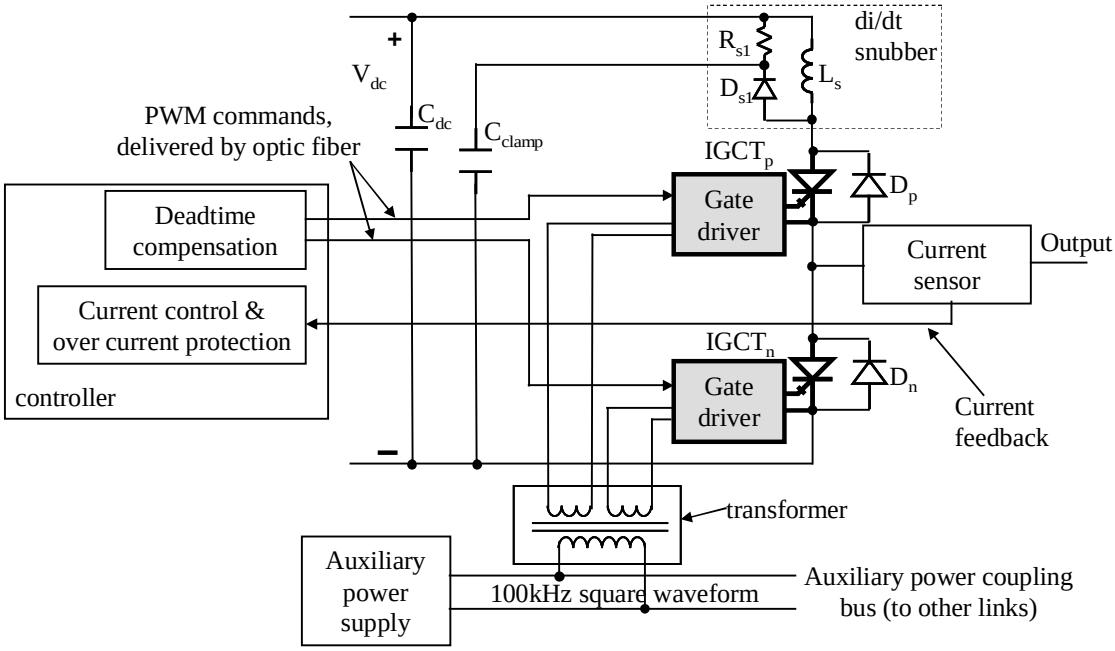

Fig.A. 2 The circuit diagram of the two-level voltage source converter phase leg using IGCT's as the main switches

Fig.A. 3 shows the circuit diagram of the two-level voltage source converter phase leg using ETO's and the main switches. The DC-link voltage is 2500V. The same diodes as IGCT converter phase leg are used for the freewheeling diodes (D_p and D_n). The same di/dt snubber is used as well. dv/dt snubbers are not included due to ETO's snubberless turn-off capability. The power for the ETO's gate driver is self-generated by the self-power generation function. Therefore, the auxiliary power supply and transformer are not required for ETO converter. Since ETO has built-in current sensor, the external current sensor is not required for the current control. Instead, two optical fibers are connected

between the controller and ETO to deliver current information to the controller. ETO's also have over-current protection function. When over-current happens, ETO can automatically shut down, and send the warning signal to the controller through optic fiber. By connecting two optical fibers between the ETO_p and ETO_n, ETO's can receive fully complementary PWM signals and will not cause shoot-through problem. Therefore, the dead-time compensation is not required for the controller.

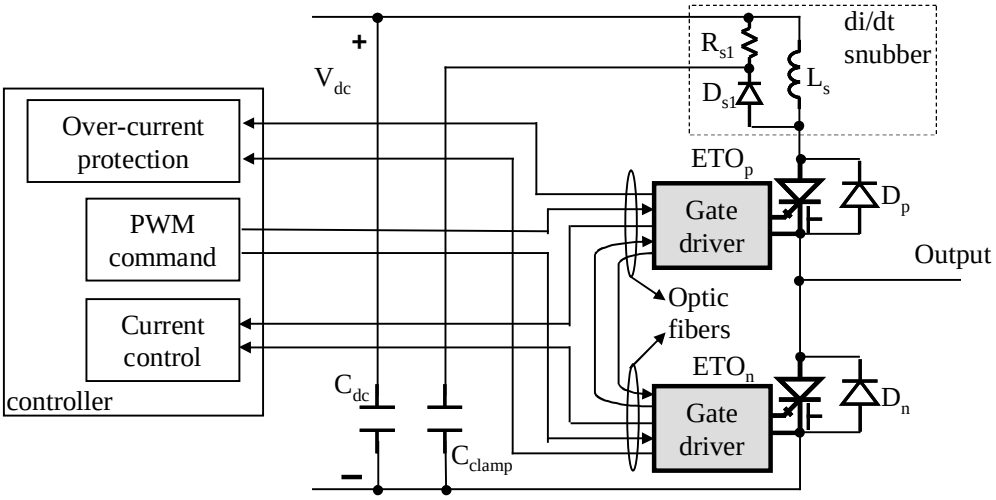

Fig.A. 3 The circuit diagram of the two-level voltage source converter phase leg using ETO's as the main switches

A.2 The Loss Characteristics of ETO's, IGCT's, and IGBT's

The device loss is the most important characteristics impacting the performance of the converter. The total device loss includes the conduction loss and the switching loss, between which there are always tradeoffs [A 13]. Both ETO and IGCT are based on hard-driven GTO technology. They share the similar loss characteristics.

Firstly, a comparison of the IGBT and hard-driven GTO in terms of the forward conduction voltage drop (V_F) vs. turn-off loss (E_{off}) tradeoff based on the device structure is performed. Then a comparison of the total losses of ETO, IGCT, and IGBT in three voltage source converter phase legs is conducted.

A.2.1 A Comparison of the IGBT and Hard-driven GTO in Terms of the V_F vs. E_{off} Tradeoff Based on the Device Structure

Fig.A. 4 shows the basic unit-cell structures of an IGBT and a GTO. The on-state carrier distribution profiles are shown above the cross-section view of the unit-cell structures to illustrate the main difference in the carrier modulation levels in the IGBT and the GTO. As shown in Fig.A. 4, the modulated carrier density falls exponentially as it moves away from the emitter junction. The fall-off rate of the carrier modulation level is characterized by the ambipolar diffusion length [A 5]:

$$L_a = \sqrt{D_a t_{HL}} \qquad \text{(A-1)}$$

where D_a is the ambipolar diffusion length and τ_{HL} is the high-level carrier lifetime.

Among the carriers injected from one emitter, about 1/e portion of them will reach the point that is L_a away from the emitter.

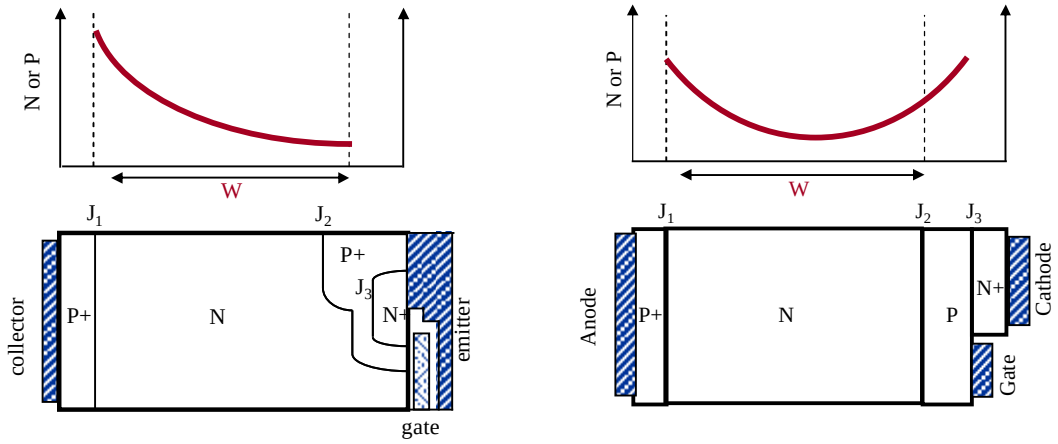

Fig.A. 4 Basic unit-cell structures and on-state conduction carrier distribution profiles: (a) IGBT and (b) GTO

When blocking voltage in the off state, both IGBT and hard-driven GTO block voltage by junction J_2. Supposing both IGBT and hard-driven GTO have the punch-through structure, they will have the similar electric field profile. Since we are compare IGBT and hard-driven GTO with the same voltage block rating, we can assume both devices have the same thickness (W) of the N-drift region.

During on-state conduction of IGBT, carriers are injected into the N-drift region from the collect P+/N junction (junction J_1). During on-state conduction of GTO, carriers are injected into the N-drift region from both ends of the thyristor structure (junction J_1 and J_3). The carrier modulation level determines the device's on-state voltage drop. The carrier lifetime determines the device's turn-off speed. From Fig.A. 4 it can be seen that to maintain a similar carrier modulation level, the ambipolar diffusion length (L_a) of GTO only need to be half comparing with that of the IGBT. Then from (A.1) it can be seen that

the high-level carrier lifetime (τ_{HL}) of the GTO will be lower than that of the IGBT. One the other hand, if τ_{HL} are the same for both IGBT and GTO, GTO will have a higher carrier modulation level than that of the IGBT. Therefore, to have a similar on-state voltage drop, hard-driven GTO can have a lower τ_{HL}.

Both IGBT and hard-driven GTO turn off as open-base transistor mode. When a device turn-off an inductive load, the current through the device remains constant before the device voltage reaches the DC-link voltage. The constant current is maintained by extracting stored carriers out of the N-drift region. After the voltage reaches the DC-link voltage, the depletion region will no longer expand, and the residue carries stored in the N-drift region near the anode end will be removed through the recombination process. The recombination process accounts for the current tail in the turn-off current waveform [A 13]. The turn-off current tail greatly increases the overall turn-off loss.

The IGBT's on-state carrier distribution profiles shown in Fig.A. 4 indicates that the highest carrier concentration locates near the collect end. For the GTO, on-state carrier distribution profiles are quite even, since the carrier concentration at its highest at both junctions. With a similar carrier modulation level, IGBT will have a higher carrier concentration locates near the collect end than that of GTO. Therefore, IGBT will have a larger current tail due to the higher carrier concentration near the collect end, and will have a longer current tail due to its high-level carrier lifetime, compare to GTO.

From the above analysis, it can be conclude that giving the similar on-state voltage drop, hard-driven GTO will have less turn-off loss than that of IGBT. On the other hand, with the similar turn-off loss, hard-driven GTO will have lower on-state voltage drop. Therefore, hard-driven has a better V_F vs. E_{off} tradeoff than that of IGBT.

A.2.2 Comparison of the Device Losses in a Three Voltage Source Converter Phase Leg

Based on the converter phase legs shown inFig.A. 1, Fig.A. 2, and Fig.A. 3, the total losses can be obtained and compared.

Fig.A. 5 shows the on-state voltages of IGBT, IGCT, and ETO with the junction temperature T_j=125°C. In Fig.A. 5, data of ETO is from the experimental results shown in Fig. 2.24. Data of the IGCT and IGBT are from the datasheets.

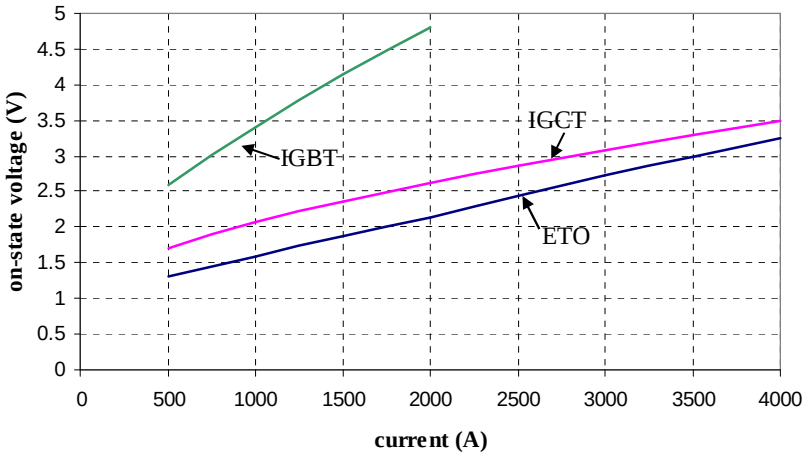

Fig.A. 5 The on-state voltages of IGBT, IGCT, and ETO at T_j=125°C

By applying curve fitting of the curves in Fig.A. 5, we can obtain the on-state voltage equations for all the devices.

$$V_{on\_ETO}(I) = 0.00057 \cdot I + 1.03 \qquad \text{(A-2)}$$

$$V_{on\_IGCT}(I) = 0.00050 \cdot I + 1.56 \qquad \text{(A-3)}$$

$$V_{on\_IGBT}(I) = 0.00147 \cdot I + 1.90 \qquad \text{(A-4)}$$

Fig.A. 6 shows the on switching loss characteristics of IGBT, IGCT, and ETO with the junction temperature T_j=125°C. In Fig.A. 6, data of ETO is from the experimental results [D 4]. Data of the IGCT and IGBT are from the datasheets.

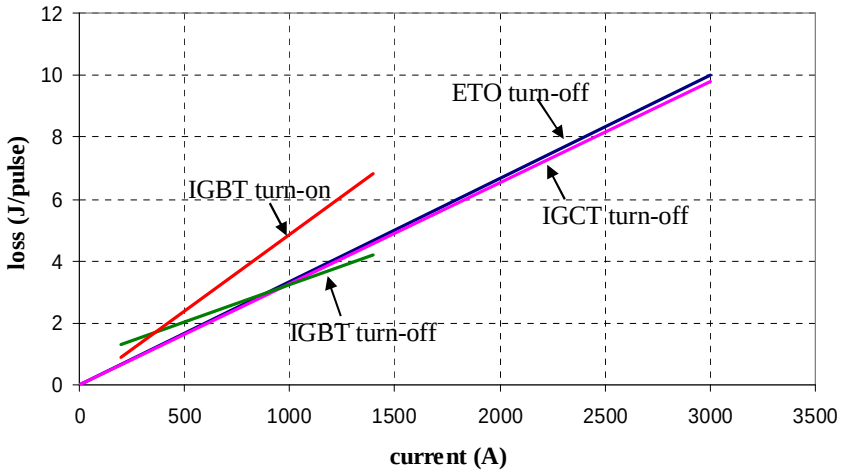

Fig.A. 6 The switching loss characteristics of IGBT, IGCT, and ETO at T_j=125°C

By applying curve fitting of the curves in Fig.A. 6, we can obtain the loss equations for all the devices.

$$E_{off\_ETO}(I) = 0.00333 \cdot I \qquad \text{(A-5)}$$

$$E_{off\_IGCT}(I) = 0.00327 \cdot I \qquad \text{(A-6)}$$

$$E_{off\_IGBT}(I) = 0.0024 \cdot I + 0.8167 \qquad \text{(A-7)}$$

$$E_{on\_IGCT}(I) = 0.0049 \cdot I - 0.0833 \qquad \text{(A-8)}$$

Due to the di/dt snubber, the turn-on losses of IGCT and ETO are very small and can be neglected:

$$E_{on\_ETO}(I) = E_{on\_IGCT}(I) = 0 \qquad \text{(A-9)}$$

Suppose all the converter phase legs have sinusoidal current output, and each of the upper and lower devices works for half a cycle. Also assume the modulation depth M=0.9, and the load impedance angle φ=0.

From (A-6) and (A-9) we can obtain the total device loss in the voltage source converter phase leg:

$$P_{loss}(I_{RMS}) = P_{cond}(I_{RMS}) + P_{sw}(I_{RMS}) \tag{A-10}$$

where

$$P_{cond}(I_{RMS}) = \frac{1}{2p} \cdot \int_0^p \sqrt{2} \cdot I_{RMS} \cdot \sin(a) \cdot V_{on}\left(\sqrt{2} \cdot I_{RMS} \cdot \sin(a)\right) \cdot \frac{1}{2} \cdot [1 + 0.9 \cdot \sin(a)] \cdot da \tag{A-11}$$

$$P_{sw}(I_{RMS}) = f_{sw} \cdot \frac{1}{2p} \int_0^p \left[E_{off}(\sqrt{2} \cdot I_{RMS} \cdot \sin(a)) + E_{on}(\sqrt{2} \cdot I_{RMS} \cdot \sin(a))\right] da \tag{A-12}$$

where f_{sw} is the switching frequency.

Substitute (A-5)-(A-9) into (A-10), we can obtain the total device losses of ETO, IGCT, and IGBT. Fig.A. 7 shows the device total losses at 500Hz switching frequency, and Fig.A. 8 shows the device total losses at 1 kHz switching frequency.

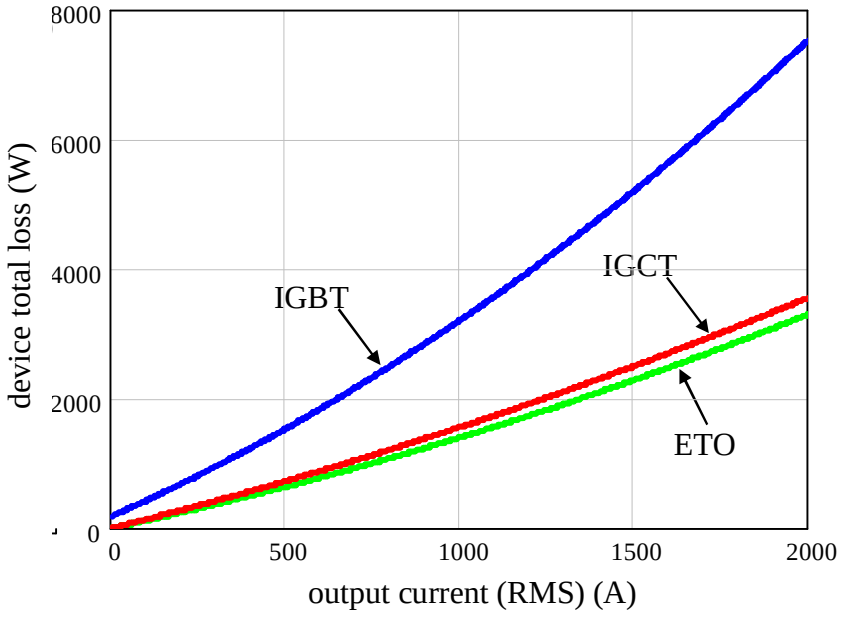

Fig.A. 7 The device total losses at 500Hz switching frequency

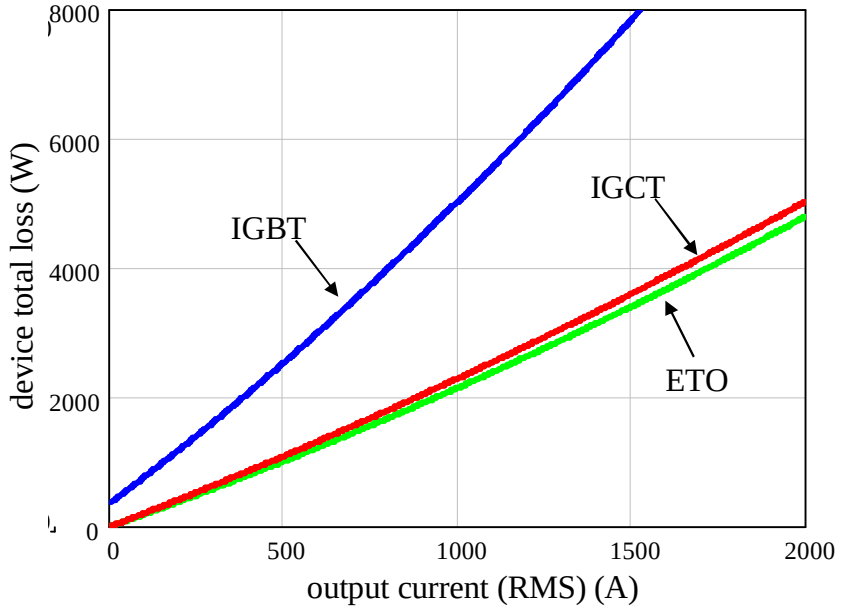

Fig.A. 8 The device total losses at 1 kHz switching frequency

From Fig.A. 7 and Fig.A. 8, it can be seen that ETO and IGCT have the similar total losses, and the total losses of the hard-driven GTO's (ETO and IGCT) are lower than that of IGBT.

A.3 The Device's Impact on the Converter Construction and Design

Comparing the voltage source converter phase leg shown in Fig.A. 3 with those shown in Fig.A. 2 and Fig.A. 1, it can be seen that ETO greatly simplify the converter construction and design.

For the IGBT and IGCT converters, the auxiliary power supply and the isolation transformers are required to provide power for the device gate drivers. Those auxiliary power supplies, transformers, and their wiring greatly increase the complexity and cost of the system. In high voltage applications, multilevel topology and device series connection may be employed. In those situations, tens or even hundreds of high power devices are required to build the system. Auxiliary power supplies, transformers, and their wiring for the device gate drivers will be very complex. The total power consumption of all the gate drivers will be very large, especially for the IGCT's whose gate drivers require large power to turn off and turn on the device. It is also difficult to implement the reliable insulation design for the transformers in the high voltage applications. Therefore, the auxiliary power supplies, transformers, and their wiring greatly increase the cost and reduce the reliability of the system. For the ETO converter, those challenges are dramatically relieved by the ETO's self-power generation function. As described in Chapter 3, ETO obtains the power for its gate drive directly for the DC-bus. The auxiliary power supplies and transformers are not required.

The IGBT and IGCT converters require the expensive external current sensors for the close loop current control. The current measurement often suffers from the noise problem, since those current sensors are always installed in the power stage, and long wires need to connect between the current sensor and the controller to deliver the current information. For the ETO converter, the external current sensor can be replaced by the ETO's built-in current sensor, which measure the device current and sent it to controller for the current control. Since the current information is delivered by optical fiber, the ETO current sensor has much less noise problem. The converter design is also simplified by ETO's dead-time requirement elimination function, which reduces the ETO converter's output current harmonics. The dead-time compensation is not required for the ETO converter.

A.4 Voltage and Current Scalability

The voltage blocking capability of the present fully controllable devices are below 6.5kV. The maximum achievable converter output voltage of a three-level neutral point clamped voltage source converter using 5.5kV device is limited to 4.16kV [B 45]. As the development of HVDC and FACTS applications, the converter with higher output voltage are demanded. To achieve higher output voltage, the series connection of devices is necessary. The most important aspect in device series connection is to balance the static and dynamic device voltages. The static voltage balancing can be simply achieved by connecting small resistor in parallel with each device. The dynamic voltage balancing during turn-on and turn-off transients are more difficult to achieve. Two dynamic voltage balancing techniques are currently widely used: the load side balancing and the gate side

balancing, also called active gate control. The load side balancing uses snubber circuit and/or clamp circuit to limit the voltage rising dv/dt and/or clamp the peak voltage. The main disadvantage of the load side control is the additional loss involved in the snubber and clamp circuits. The active gate control is to use the control function of the gate drive to achieve the voltage balancing. The active gate control approach is more attractive due to its high efficiency.

It is impossible for ETO and IGCT to achieve voltage balancing by the active gate control approach, because of their latching thyristor structure. Load side balancing approach is necessary for the series connection of ETO and IGCT. Fortunately, their transistor mode turn-off operation greatly reduces the turn-off delay and results in very well defined fast switching transients compared with GTO. Thus, comparing with GTO, a much smaller snubber and/or clamp capacitor can be used to achieve the voltage balancing, leading to a relatively small additional loss.

For the series connection of IGBT, many active gate control approaches are proposed to realize the low loss series connection operation [C 7], [C 8], [C 9]. Although the active gate control approach has difficulties such as balancing the voltage during the turn-off current tail period, it is still proved to be a more efficient approach than the load side balancing.

To increase the output current capability of a converter, the parallel operation of the devices is necessary. Due to the emitter switch MOSFET's, ETO has very strong positive temperature coefficient than IGCT and IGBT. Therefore, ETO has the best current sharing in the parallel operation than that of IGCT and IGBT.

A.5 Device Gate Drivers

IGCT has complex gate drive circuit. The turn-on pulse gate current injection, the constant gate current injection during on-state, and the turn-off current injection require to be precisely controlled. The minimum on/off time need to be controlled as well.

IGCT gate drive has large power consumption because it delivers the required gate current for turn-on and turn-off GTO. Its power consumption increases almost proportionally with the switching current and switching frequency. IGCT requires a large amount of low lifetime liquid aluminum electrolytic caps to reduce the gate loop inductance and deliver the huge turn-off current. Due to the reliability issue caused by the caps, the current capability has to be reduced [B 18].

ETO gate drive circuit is complex as well. Gate driver circuit is carefully designed to control the turn-on and turn-off GTO very precisely, as presented in the previous chapters. To implement the multiple functions, additional circuit is included within the circuit board.

ETO gate drive power consumption is much lower than that of IGCT. ETO's turn-off is achieved by turning off the emitter switch and ETO gate driver does not provide the turn-off current. ETO gate driver only provides the GTO turn-on current. ETO gate drive power consumption almost keeps constant with the increasing of switching current and switching frequency.

IGBT gate drive circuitry would be very simple if it is only designed to control the turn-on and turn-off of the IGBT. However, much more advanced circuit is often implemented in the real design. di/dt and dv/dt are precisely controlled during the switching transients. The power supply under-voltage protection, short-circuit protection,

as well as the generation of the error signals are designed. The above multi-functions require sophisticated gate drives with substantial part count of electrical components [A 16].

IGBT gate driver has very low power consumption, since it only need to charge and discharge the input capacitance of IGBT to turn on and turn off IGBT.

A.6 Protection

The over-current caused by the short circuit, malfunction, or the component failure is severe fault situation that can result in further failure of the power converter if appropriate remedial action is not taken in time.

Both IGBT and ETO have over-current protection capability. IGBT and ETO can detect the fault current condition and turn off automatically. For IGBT, over-current can cause the device to go out of the saturation region and enter the active region, and the rising voltage of the device will limit the current. For ETO, the rising rate of the fault current is limited by the di/dt snubber. IGCT does not have over-current protection capability. If the fault current flow through the external current sensor, IGCT may be turned off by the controller. However, when converter shoot-through happens, the fault can be detected by the current sensor. In this situation, IGCT converter can not be protected, and further failure of the IGCT and/or converter will happen.

If the over-current does not be turned off for any reason, device will be destroyed by the occurring large over-current. IGCT will short circuit under all worst case failure conditions due to its press pack package. On contrary, IGBT will act as an open circuit due to its wire bond package. In device series connection applications, short circuit after

destruction is desirable, since the converter may still able to operation properly after one or more devices fail in short circuit. According to our experiments, ETO always fails in a short circuit. The detail failure mode of the ETO needs to be further investigated.

A.7 Reliability

Since IGBT module provides insulation between the power circuits and cooling systems, the durability of the insulator is one major aspect of reliability. Another serious source of failure is the increase of the thermal resistance after power cycling tests. IGCT has only one silicon wafer in the proven reliable press pack. It is believed that IGCT has a higher reliability than that of IGBT [A 16]. ETO uses GTO as the main switch, which is the same with IGCT. So ETO also has high reliability. Although the ETO current also flow through the emitter switch MOSFET's, those MOSFET's are all low voltage devices and their temperature rising is much lower than that of the GTO during switching. Therefore, those MOSFET's do not have much reliability issue. A further investigation of the reliability of those MOSFET's is necessary to provide a fully understanding of the ETO reliability.

A.8 Cost

Today's high power IGBT's consist of many parallel chips, and the maximum chip size of IGBT's is limited to 2.6cm^2. The connections of the chips are realized by aluminum wires which are bonded to the chip metallization. IGCT is the combination of a GTO with special designed concentric gate disk and an extremely low inductive gate

driver. IGCT consists of only one silicon wafer, a few mechanical parts, and an integrated gate driver. IGCT is believed to have a substantial cost advantage compared to the IGBT due to its high silicon utilization and high yield [A 16]. ETO has an even lower cost than that of IGCT. With all the cost advantage of IGCT, ETO further reduces the cost of the GTO, since the special GTO gate concentric gate disk design is not required. The common commercially available GTO is used to build the ETO.

From the system point of view, the cost saving by ETO is very large. The auxiliary power supply, isolation transformers, and the current sensors are saved by ETO's self-power generation function and built-in current sensor.

A.9 Conclusion

ETO and IGCT have better on-state voltage drop vs. turn-off losses tradeoff than that of IGBT. Comparing ETO, IGCT and IGBT in the voltage source converters with the same switching frequency and output power, ETO and IGCT have lower total power losses than that of IGBT.

With ETO's self-power generation function, built-in current sensor, and dead-time elimination function, ETO greatly simplifies the converter construction and design.

ETO's and IGCT's are much easier than GTO to achieve the voltage balancing in series operation by the low loss load side balancing methods. High power IGBT offers the active control of dv/dt and di/dt features, which make IGBT very easy for the series connection operation. ETO has better current sharing in the parallel operation than that of IGCT and IGBT.

Both IGCT and ETO have complex gate driver. IGCT gate drive has large power consumption. ETO's gate driver power consumption is much lower than that of IGCT. The dv/dt and di/dt control as well as the protection circuit makes the advanced IGBT gate drive also sophisticated. IGBT gate driver has very low power consumption.

ETO and IGBT offer built-in over current protection, which enable them to protect the system even in the worst case shoot-through fault conditions.

ETO and IGCT have higher reliability than that of IGBT. ETO has the lowest cost.

Table A-1 summarizes the important characteristics of the ETO's, IGCT's and IGBT's for comparison.

Table A-1 Comparison of Characteristics of ETO, IGCT, and IGBT

Characteristics	ETO	IGCT	IGBT
Total loss	low	low	high
Auxiliary power supply and isolation transformers for gate driver	Not require	require	require
Current sensing capability	Yes	No	No
Dead-time to prevent shoot-through	Not require	require	require
Voltage Scalability	Good	Good	Best
current Scalability	Best	Good	Good
Gate driver power consumption	Medium	High	Low
Gate driver complexity	High	High	Medium
Built-in over-current protection	Yes	No	Yes
Reliability	High, need further investigation	High	Medium
Behavior after destruction	Short circuit, need further investigation	Short circuit	Open circuit
Cost	Lowest	Low	High

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