The Dual Use of Power Distribution Networks for Data Communications in High Speed Integrated Circuits

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Dissertation submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical and Computer Engineering

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January 27, 2006
Blacksburg, VA

Keywords: Ultra Wideband, Power Distribution Networks, Power Line Communications, Integrated Circuits

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(ABSTRACT)

This thesis investigates a new data communication method in high speed integrated circuits using power distribution networks (PDNs). The conventional purpose of PDNs in integrated circuits (ICs) is to deliver power to internal nodes of an IC while meeting a level of power integrity. As the power consumption increases for very large scale integration (VLSI) systems, the number of power/ground pins increases as well. In this thesis, we propose to use PDNs for dual purposes, delivery of power and one-/two-way data communications, which is highly beneficial for pin-limited high performance ICs. To this end, we investigate signaling methods for a microscopic communication channel. Impulse-based ultra wideband (UWB) signaling is selected due to its robustness to noise and wideband characteristics. Next, we study a planar structure IC package based on the cavity resonator model (CRM) as a communication channel. Impedance characteristics of a planar structure IC package and other relevant components of an IC are important, and they are investigated for data transmission over power distribution networks. Another important aspect of the study is data transmission and reception, which we investigate through simulations. Finally, we study one possible application for one way communications, massive parallel scan design, which greatly shortens the testing time at moderate overhead. The performance is measured with eye diagrams and bit error rates (BERs) under the presence of voltage drop, simultaneous switching noise, and thermal noise.

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Title: Professor of Electrical and Computer Engineering

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Kids: “Dad, will you go to school, tonight?”

Dad: “Yes, I have something to do.”

Dedication

To my loving God

To my parents and parents-in-law

To my bride, Kyung Ah Roh
To my daughters, Rosa (Soo Young) and Hye Sim

Acknowledgements

First of all, I would like to express my sincere thanks to my advisor, Dr. Dong S. Ha for his insights in research, guidance on this interesting research thesis, patience, financial support, and out of the academic activities as well. I would also like to thank my Ph.D. dissertation committee, Dr. James R. Armstrong, Dr. Michael S. Hsiao, Dr. Amitabh Mishra, and Dr. Jeffrey H. Reed for their valuable advice and constructive suggestions on my doctorate research.

For technical discussions and collaborations, I thank my colleagues at Virginia Tech VLSI for Telecommunications (VTVT) Laboratory. I would never forget the technical sessions on Ultra Wideband (UWB) with my colleagues in early 2002. All the current students and alumni of the VTVT group – Hyung-Jin Lee, Jina Kim, Rajesh Thirugnanam, Jong Suk Lee, Shen Wang, Sweta Kalantri, Jonathan Perry, Sajay Jose, Venkat Srinivasan, Chad Pelino, Kevin Marsden, Dr. Jos Sulistyo, Dr. Nathaniel J. August, and Dr. Suk Won Kim.

I want to present special thanks to Dr. Donald McKeon, Dr. Joseph G. Tront, Dr. Boo Hee Nam, Mr. Hiromitsu Yagi, and Dr. Jae-Hong Park for their kind advice and considerations for many concerns as a senior in life. My old peer at Samsung Electronics, Dr. Woo Jin Kim at AMD, old peer at IBM, Ms. Deborah A. Dyson, and Dr. Chan K. Park at Broadcom deserve my thanks for their helping me launch my career at Qualcomm. I also thank all the members of the Korean Catholic Community of Blacksburg (KCCB), Korean ECE Student Association (KECESA), and Korean Student Association (KSA) at Virginia Tech for providing me with extra curricular activities with close fellowships.

I would like to thank Master Solutions, Samsung Electronics, and Intel Corporation for their financial support via several research projects. I thank my family - particularly my sister, Hae-Kyong, my parents, and my parents-in-law - for their support, prayers, and good wishes throughout my doctorate study.

Lastly but not least, I would really appreciate my kids, Rosa and Hye Sim for their sound belief on Dad, and my bride, Kyung Ah Roh, for her dedicated support with consistent love. Without her prayers, support, and good wishes, this thesis would not be completed.

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Chapter 1

Introduction and Scope

The number of pins on a VLSI chip seems to grow boundlessly with advancement of VLSI technology into a deeper submicron technology. The increasing pin count results not only from additional signal pins but also from additional power and ground pins. For example, the Intel Pentium 4 processor has a total of 775 pins (lands), of which 226 pins are for power and 274 pins for ground. Additional pins increase the cost of a chip and lead to a larger footprint. We propose to investigate the possibility of using power pins to carry data signals while serving their intended purpose, supply of power. The dual use of the power pins can significantly reduce the pin count, size, and hence the cost of a chip.

Power line communications, which was patented in the 1920's, uses power lines for the dual purposes of data communications and power delivery [1]-[6]. Even when scaled for integrated circuits (ICs) or printed circuit boards (PCBs), the environment is essentially the same as the lines that deliver power to the home. However, power line communication has never been considered for communications in ICs and PCBs so far, mainly due to the low operating voltage and the tight electromagnetic compatibility (EMC) requirements. In this dissertation, we propose to use the power distribution networks of ICs and PCBs to simultaneously carry data signals while delivering power. The power distribution networks are used for both inter-chip and intra-chip data communications. We investigate the feasibility for dual use of power distribution networks in high speed integrated circuits through a case study. A direct superposition of a data signal on a power pin would fail due to the inherently high noise level on power distribution networks and the limited additional power that can be applied to power distribution networks. Further, this would preclude the possibility for multiple data channels. To address the problem, we suggest adoption of

UWB (Ultra Wideband) and direct sequence code division multiple access (DS-CDMA) communication technologies.

Since the FCC's allocation of a UWB spectrum in 2002, UWB has gained phenomenal interest in academia and industry. Compared to traditional narrowband communication systems, UWB has several advantages such as high data rate, low average power, and simple RF circuitry. Many of these potential advantages are a direct consequence of the large instantaneous bandwidth, which is on the order of several GHz. UWB signals overlay existing spectrum, but their low power limits the impact to the underlying signals. UWB signaling can be carrier-based or impulse-based, and the impulse-based signaling is more suitable for the proposed application due to its simple hardware.

Two representative UWB systems – impulse-based UWB (I-UWB) systems [7]-[13] and multi-carrier UWB (MC-UWB) systems [14], [15] – have been recently investigated in the literature. For this dissertation, I-UWB has advantages over multi-carrier systems including low complexity of demodulation/detection, low sensitivity to simultaneous switching noise, and low-cost, low-power hardware. The carrierless nature of I-UWB results in simple RF circuitry, which does not require intermediate mixers and oscillators.

Different from a narrowband signal, a short pulse for I-UWB signaling occupies a wide spectrum which may range over several GHz. Typically, I-UWB signaling appears in the time domain as shaped sub-nanosecond pulses in a low duty cycle – the pulse repetition interval (PRI) ranges from nanoseconds to microseconds. For this dissertation, high rate I-UWB pulse transmission would be preferred to secure high data rate multichannel data transmission.

1.1 Power Line Communications (PLC)

Figure 1.1 shows the Voltage Layers (VLs) that have been widely accepted in the conventional power line communications arena [2]. The VL model has four voltage layers, EHV, HV, MV, and LV (Extremely High Voltage, High Voltage, Medium Voltage, and Low Voltage) with intermediate transformers. The High Voltage power lines or even Extremely High Voltage power lines emanate from power plants and represent a wide-

meshed long-distance nationwide network. The term HV applies to voltage over 36 kV, EHV to voltage over 300 kV. The next lower level is constructed for delivering power into cities, towns, and villages. The term Medium Voltage covers the range from 1 kV to 36 kV. Eventually, MV is transformed down to Low Voltage with levels below 1 kV for distribution to customer premises as shown in Figure 1.1 [1]. The LV varies depending upon the consumer load [1]. Here, we introduce the new term 'Extremely Low Voltage' (ELV) for naming our proposed research. The ELV concept is not just an addition or extension of the existing concepts, but it opens a new approach for interconnect technology in a highly integrated SoC environment. ELV typically covers voltage ranges on the order of single digit volts with voltage regulator modules on modern electronic systems.

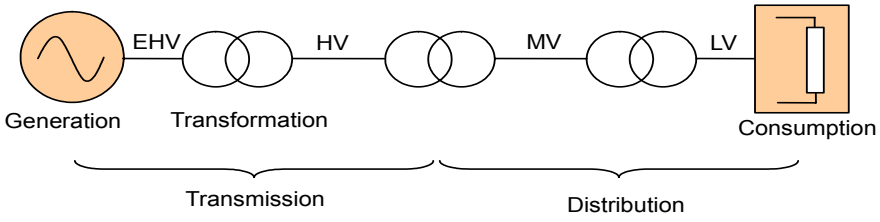


Figure 1.1: Voltage Layers.

1.1.1 Background

The idea of digital communications over power lines is not new in that it was patented in the early 1920s. Since then, power line communications (PLC) have been mainly used by utility companies for remote metering and control [3]. Recently, it has been revived for broadband internet access over existing power lines under the name Broadband over Power Lines (BPL). PLC also applies to narrowband applications within the frequency range of few kilohertz. The basic idea behind PLC is to utilize the existing resources for communication purposes; that is, "no new wires" for data transmission is the fundamental essence of PLC.

1.1.2 Channel Model

For a communications channel, the appropriate channel model is crucial for the evaluation of its performance. However, there has been no standardized channel model for PLC channels due to the difficulties of characterizing the power supply network. PLC channels suffer from a number of technical challenges [6]:

- Frequency-varying and time-varying attenuation
- Dependence on location, network topology, and connected loads
- High interference due to noisy loads
- Highly colored background noise
- Various forms of impulse noise
- Electromagnetic compatibility (EMC) issues that limit available transmitted power

The most widely known channel model for the frequency response transfer function $H(f)$ of the PLC channel would be the multipath model proposed by Philipps [4], and by Zimmermann and Dostert [5], which is expressed as follows in the frequency range from 500 kHz to 20 MHz:

$$H(f) = \sum_{i=1}^{N} g_i e^{-(a_0 + a_1 f^k) d_i} e^{-j 2\pi f \tau_i} \quad . \tag{1.1}$$

N is the number of propagation paths, a_0 and a_1 are the link attenuation parameters, k is an exponent (with its typical values from 0.5 to 1), g_i is the weighting factor for path i, d_i its length, and τ_i its delay [6].

1.1.3 Advantages and Challenges

The main advantages of PLC would be the "**no new wires**" concept for high-rate data communications. Another possibility is the extension to wide area networks, since power lines offer a convenient and inexpensive shared medium for data transmission.

Although the advantages of PLC are apparent in nation-wide power supply networks, there are still possible challenges for the deployment of PLC. They mainly result from the fact that data transmission should not disturb the main function of power delivery

for power supply networks. In addition, as the shared wired medium, power lines have several challenges as described in Section 1.1.2.

1.2 Data Communications in Integrated Circuits

Major research topics for VLSI systems include 1) reducing power consumption, 2) enhancing performance, and 3) reducing silicon area for low cost manufacturing. The unique assumption of these research activities is to use existing on-chip metal wires to form separate data communication channels per signal. Thus, as the integration level increases per the demand of markets, more metal wires should be routed for data communications in ICs. In addition, due to the low power consumption and small area constraints, the process technology has been decreasing to deeper submicron. Finally, maintaining signal integrity in densely integrated VLSI systems will be a critical issue with the limited number of pins of an IC. For example, crosstalk among the adjacent signal lines (metal wires) should be reduced within a tolerable range which enables the resources to be used as a sufficient data communication channel between a transmitter (a driver or source node) and a receiver (a sink or destination node) on chip. In addition to this interference, parasitics resistance and capacitance also impact signal integrity based on the metal geometry. As the performance of VLSI systems increases beyond the Gigahertz range, the switching noise becomes another concern.

1.3 New Approach for Data Communications in ICs

As processes advance to deeper submicron technologies per the demands of decreasing supply voltage and increasing operating frequency, signal integrity plays a crucial role. Most research activities have focused on the reduction of detrimental effects in energy efficient on chip data communications. In this dissertation, we propose to use the power distribution networks (PDNs) for data communications while endeavoring to meet the traditional needs in VLSI systems. The proposed idea can be categorized into two classes – one-way and two-way data communications in high-speed integrated circuits.

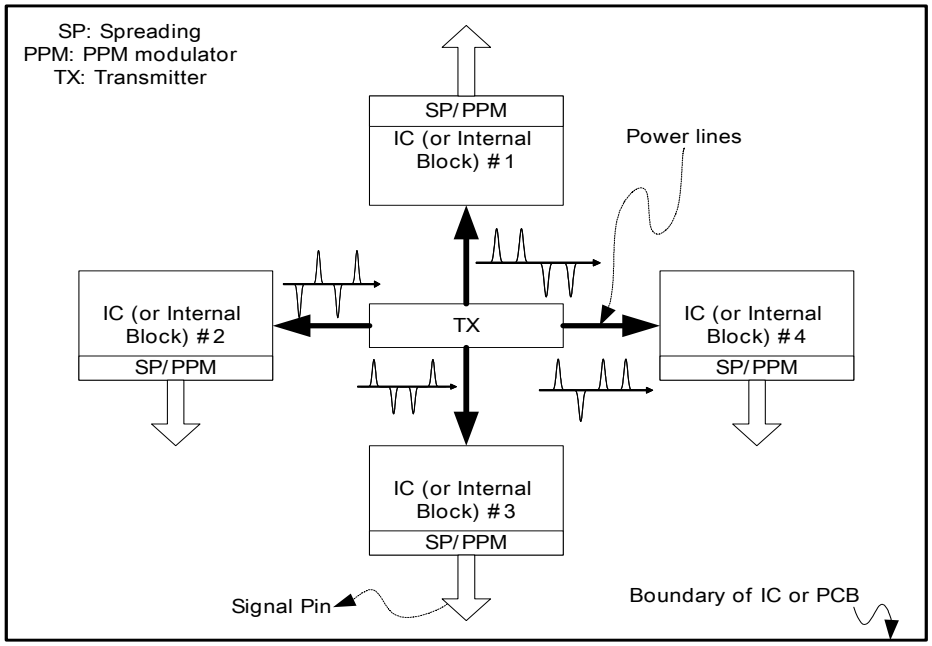
1.3.1 One-Way and Two-Way Data Communications

The dual use of power lines for data communications in a system-on-chip environment was proposed for the first time in 2005 [16]. As the number of required pins increases with the number of devices on a chip, the cost for the pins increases as well. The bottom line of the thesis is to utilize the existing resources[1] on chips and/or on boards – power lines (or power buses) – for data communications purposes; and at the same time we can achieve multiple data transmissions and/or reduced pin count with moderate hardware complexity.

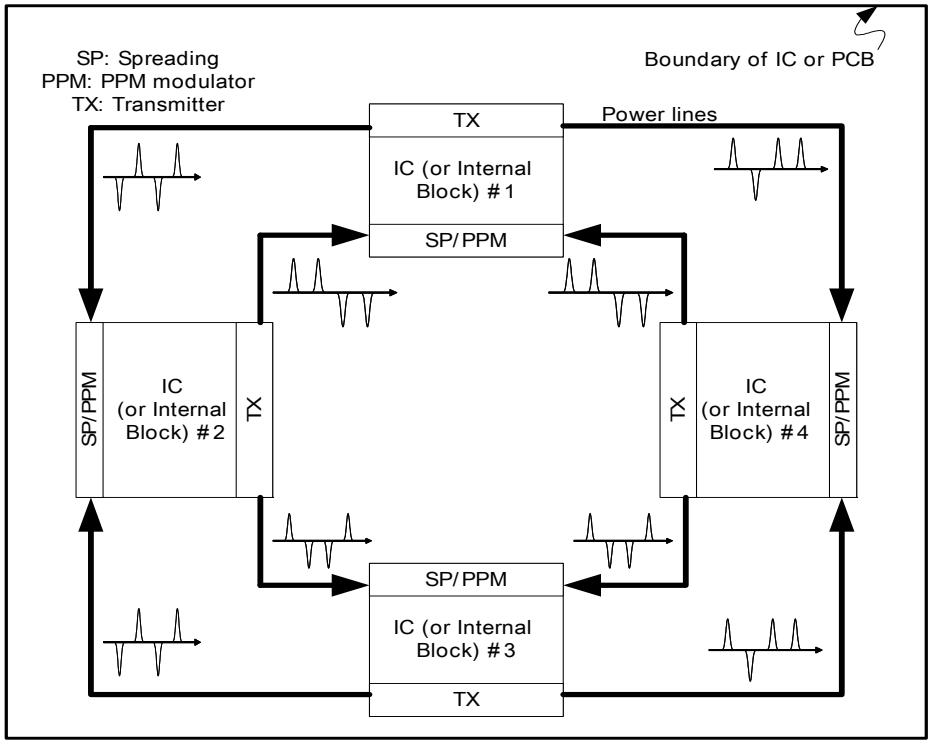
Figure 1.2 shows the overview of our proposed data communications through on-chip/on-board power lines (power distribution networks; PDNs). The proposed method can be applied for either 1) one-way communications such as a massive parallel scan design applications [17] or for 2) two-way communications such as inter-/intra- chip data communications [16]. The reference for the distinction between one-way and two-way communications is determined by the hardware resources supporting the architecture. One-way communications can be constructed with an impulse-based ultra wideband (I-UWB) transmitter as a source node and several receivers, which receive I-UWB pulses via power pins and transmit via normal output pins for signals. One promising application is in massive parallel scan design. Two-way communications is a generalized version of the proposed architecture. It uses power distribution networks for both transmission and reception of signals. Thus, the I-UWB transmitter and the simple data recovery unit (which consists of a one bit comparator and a digital accumulator) are necessary on a chip for two-way communications.

As shown in Figure 1.2 (a), one-way communications can be done among internal blocks of an IC or among several ICs in a printed circuit board (PCB). The large rectangle indicates the border of an IC or a PCB. Inside the large rectangle, there are four receivers and one transmitter. For multiple access, we consider the direct sequence code division multiple access (DS-CDMA) principle.

[1] This essentially conforms to the idea of "no new wires" for the power line communications in the literature.



(a) One-Way Communications



(b) Two-Way Communications

Figure 1.2: Overview of Proposed Data Communications in Integrated Circuits.

The transmitter will be a UWB pulse generator, and the receiver will be the above mentioned 1-bit comparator. Both are based simple hardware. In this case, the transmitter and the receiver use the PDNs for data communications. Optionally, the receivers can transmit the received data to certain destinations via signal lines using a pulse position modulation (PPM) modulator for application specific needs.

As shown in Figure 1.2 (b), two-way communications can also be performed among the internal blocks of an IC or among several ICs in a PCB. The large rectangle indicates the border of an IC or among several ICs in a PCB. Inside the large rectangle, there are five transceiver blocks (or ICs). Each transceiver has a transmitter (UWB pulse generator) and the comparator-based receiver used in the one-way communications.

1.3.2 Advantages and Challenges

The proposed method of data communications provides the benefits of utilizing the existing PDNs, and the potential advantages can be summarized as follows.

- Reduced pin count
- Efficient utilization of metal resources in an IC or on a PCB
- Complete/selective use of PDNs for data communications
- More resources for the routing of critical signals
- Reduced crosstalk for the critical path
- Low cost implementation/manufacturing
- No harmful effects on the target signal/power integrity
- Application specific benefits (*e.g.*, on chip diagnosis, at speed testing with massive parallel scan design, etc.)

As most of the advantages of the improved technology have challenges, the proposed communication method has also the following challenges as well.

- Feasibility considering impedance characteristics on the state-of-the-art IC packages
- Performance of the I-UWB signal detection

- Silicon area cost for a transceiver (a UWB pulse generator and a simple receiver which consists of a 1-bit comparator and an accumulator)
- Additional power consumption for the above transceiver

The above advantages and challenges are discussed in the following chapters of this dissertation, focusing on the feasibility in a realistic high speed integrated circuit environment with appropriate models. The advantages and challenges can be traded off constructively. The sole purpose of this thesis is to provide a systematic approach for one- and two-way data communications over microscopic power lines – or PDNs in an IC.

1.4 Summary of Contributions

In the above sections, we present the overview, benefits, and challenges of the proposed method of data communications in ICs. The contribution of this thesis can be summarized as follows.

- It provides a new approach for data communications on the existing resources – namely the power distribution networks in ICs. The benefits of the proposed method are illustrated in the above section.
- It presents a systematic approach for showing the feasibility of the proposed approach by providing a simulation environment which consists of PERL scripting, SPICE, and MATLAB.
- It will provide a significant role in future high-speed interconnect in most high performance electronic systems which employ several ICs on a PCB or a backplane.
- It envisions new paradigm of data communications applicable to most high performance digital electronic systems.

1.5 Organization of the Thesis

As the integration level in an IC or a PCB increases, the importance of the design of the power distribution networks increases as well. The actual design of power distribution networks is frequently over-estimated with respect to the possible adverse effects due to

voltage drop, simultaneous switching noise, and thermal noise. That is, power distribution networks have been frequently over-designed to be robust to these adverse affects. Assuming we are constrained to use existing power distribution network designs, several questions may arise on the feasibility of the dissertation.

1) How does the unique signaling of I-UWB affect existing power distribution networks in an integrated circuit?

2) How do we transmit I-UWB signals over noisy power distribution networks without incurring harmful effects on the existing power distribution networks?

3) How can the impacts of the propagation of I-UWB pulses on realistic IC package and on-chip metal wires be estimated and properly considered?

4) How can I-UWB pulses overlaid with the power supply voltage be detected with high accuracy and low cost hardware?

5) How can the feasibility be justified within a comparable environment to the existing ICs?

As an end result, the dissertation intends to show the feasibility of dual use of power distribution networks in high speed integrated circuits for single/multiple channel data communications using appropriate I-UWB signaling.

Chapter 1 starts with an overview of the dissertation consisting of one-way and two-way communications with their advantages and challenges. Then it provides contributions and organizations of this thesis.

Chapter 2 provides answers for the first question, and it reviews power distribution networks and I-UWB. The chapter starts with an overview of power distribution networks, packages, and power pads. Next, it presents the basics of I-UWB, including signaling, transceiver architectures, and multichannel data transmission. Finally, it examines multiple access schemes for multichannel data transmission with an emphasis on the specific requirements of I-UWB and the power integrity of power distribution networks.

Chapter 3 answers the three questions 2-4, and it investigates the major components in the power distribution systems of a high speed IC focused on the impedance characteristics. Impedance characteristics will predict the signal propagation over a power distribution network used as a communication channel. Chapter 3 starts with Section 3.1, which presents an overview of our modeling philosophy including the simulation methodology. Section 3.2 briefly introduces a planar structure IC package model based on the cavity resonator model shows the various impedance characteristics investigated. Section 3.3 investigates realistic models for solder ball and C4 bump, and it discusses the parasitics for the proposed data communication schemes. Sections 3.4 and 3.5 investigate the power distribution networks and decoupling capacitors. Section 3.4 starts with a generic second order system model for the on-chip power distribution network. The model is a lumped element model that represents the channel for signal transmission. Next, Section 3.5 describes the realistic distributed RLC models with a reasonable number of stages.

Chapter 4 answers the fourth question with comparisons of possible architectures for the proposed data communications scheme. As opposed to such existing methods as correlation or matched filtering, we propose a simple architecture for the detection of signals that emphasizes low power and low cost. We explore the effect of sampling speed on signal quality and the effect of spreading on multichannel data transmission. The simulation results present the impact of port location considering interference and performance.

Chapter 5 answers the last question and justifies the feasibility of the dual use of power distribution networks for power and communications. In Chapter 5, we present a case study that employs the results from the previous chapters in a realistic simulation environment with parameters comparable to those of a PowerPC 750 processor for electrical parameters and an Intel Pentium III processor for a package model. The case study provides a new approach to massive parallel scan design. Our approach emphasizes multichannel data transmission at different power pins via I-UWB signaling and DS-CDMA. Next, it considers the voltage drop from the resistive IR-drop and inductive loss due to the simultaneous switching noise. The simulation results prove the feasibility of the

proposed data communications over power distribution networks in high speed integrated circuits.

Finally, Chapter 6 concludes the dissertation with discussions.

Chapter 2

Preliminaries

In this chapter, we investigate the major components in power distribution systems and the equivalent resistor-inductor-capacitor equivalent circuits in power distribution networks. Based on the IO locations, we present two IC packaging methods – peripheral IO type and array IO type packages. We explain the pad cells that supply power, and finally we review some relevant fundamentals of UWB.

2.1 Scope of Applications: ICs on PCB

Even though we introduce general applications of the dual use of power distribution networks both in a PCB and in an IC, in this thesis, we focus of our investigation on an IC which has a miniaturized power distribution networks in a microscopic environment.

2.2 Power Distribution Networks

2.2.1 Definition [18]

A power distribution system consists of interconnect networks with decoupling capacitors on a printed circuit board, an integrated circuit package, and a circuit die. It supplies power depending on the performance, size, and cost characteristics of the overall electronic system.

Figure 2.1 shows a cross-sectional view of a power distribution system in a system-on-chip environment [18]. The components in the power supply system are connected through several layers of packaging hierarchy. First, we consider the voltage switching regulator module, which is usually an off-chip component. The voltage regulator module

converts the high DC voltage level into the appropriate lower voltage level for the integrated circuit. The regulator functions as the power source and the integrated circuit will be the power load (or sink). Then, decoupling capacitors minimize impedance for both the integrated circuit and the board, thus avoiding resonance.

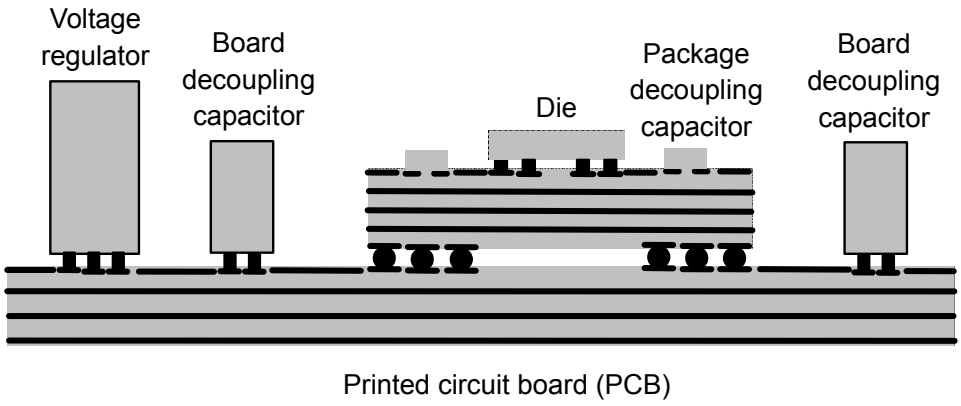


Figure 2.1: Hierarchical View of a Power Distribution System.

The overall power distribution system consists of a hierarchical structure, which spans the voltage regulator, printed circuit board, packages, and integrated circuits. The overall characteristics of the power distribution networks of the power distribution system depend on the operating frequency range. As the frequency increases, the current loop dominates in the inner-loop. The inner current loop is formed through the power load and the modeled parasitics of integrated circuits. The parasitics of the power (ground) plane include resistance and inductance. As the number of planes increases, the parasitics of resistance and inductance decrease because of the shunt connections among planes. The other parasitics include the equivalent series resistance (ESR; R_y^c), the equivalent series inductance (ESL; L_y^c), and the capacitance (C; C_y) of the decoupling capacitors between power and ground lines[2]. Figure 2.2 displays an exemplary circuit model for characterizing a power supply system [18]. The subscript *r*, *b*, *p*, and *c* denote regulator, board, package, and chip, respectively. The superscript *p*, *g*, and *c* denote the power, ground, and decoupling capacitors. The power and ground planes have parasitics of resistance and

[2] *Lines* can be interchangeable with *nodes* and *planes*.

inductance of $R_x^{p(g)}$ and $L_x^{p(g)}$, respectively. The superscript p (g) denotes the power (ground) plane and the subscript x represents r, b, p, or c. The ESR, ESL, and C in a decoupling capacitor can be represented by R_y^c, L_y^c, and C_y, respectively. The superscript c denotes decoupling capacitors and the subscript y represents b, p, or c.

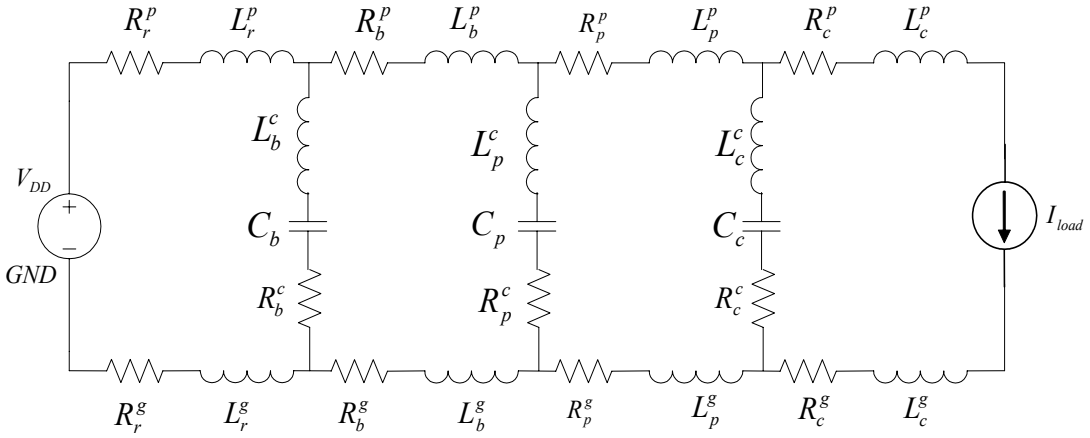


Figure 2.2: The Circuit Model for a Power Distribution System.

2.2.2 Parasitics

2.2.2.1 Resistance (R) [22]

The resistive components of metal wires (or traces in case of printed circuit board) affect the signal integrity. The dominant effect is the delay and attenuation from the time constant (which is the product of resistance and capacitance), since the on-chip inductance is usually ignored. The estimation of resistance of metal wires is as follows [19]. For a uniform conducting slab whose dimension is in w (width) × l (length) × t (thickness), the resistance can be estimated as

$$R = \left(\frac{\rho}{t}\right) \cdot \left(\frac{l}{w}\right) \qquad [\Omega] \tag{2.1}$$

where ρ = resistivity

t = thickness

l = conductor length

w = conductor width

The expression in (2.1) can be rewritten as

$$R = R_s \cdot \left(\frac{l}{w} \right) \qquad [\Omega] \tag{2.2}$$

where R_s is the sheet resistance having units of Ω/square. Thus, to obtain the resistance of a metal wire, we only need to know the length, width, and sheet resistance. Typically, the sheet resistance is provided with the technical library of any ASIC processes.

The upper metal layers have reduced resistivity and delay, since they are usually thicker. Typically for effective distribution of power and ground, the thicker metal layers have been used, and frequently more than necessary are used. This overestimation results in the waste of a valuable resource (the upper metal layers) in an integrated circuit. The determination of the metal width depends on the requirement of voltage drop, die size, and the number of power pins. It will be covered in more detail in Chapter 5 through a case study.

2.2.2.2 Inductance (L) [22]

As technology advances, the integration level and operating frequency of an integrated circuit increases, so the inductive loss of on-chip metal wires cannot be ignored as before. The inductance of a power distribution system mainly results from the bond wires in a package, which can have a significant impact on signal integrity. It is difficult to model the inductance accurately (yet simply) because of non-locality effects and an unknown return path. Inductance of a conductor on the silicon substrate can be obtained from the following equation under the assumption of negligible thickness of the conductor (*e.g.* a metal wire) and $w < h$.

$$L = \frac{\mu}{2\pi} \ln \left(\frac{8h}{w} + \frac{w}{4h} \right) \tag{2.3}$$

where μ = permeability, h = thickness of the substrate and the conductor on it (which can be approximated as the thickness of substrate due to the large difference in the order of the thickness of a substrate and a conductor), and w = width of the conductor [20], [21]. Although the thickness of the silicon substrate varies based on the process and

manufacturing company, the order of the thickness of a substrate is much greater than that of a conductor. Thus, the thickness h in (2.3) will be approximated as the thickness of the silicon substrate, which ranges from 250 μm to 1000 μm. In the case of package inductance, manufacturers usually provide values (normally in the range of 3-15 nH for the peripheral I/O type packages [22] and 0.5-2 nH for the array I/O type packages). The inductance of a bond wire is an important consideration for inductive spikes, when a large current is drawn through a wire in a short period of time. Recently, on-chip inductance has also been a focus due to increased chip dimensions (number of devices) and thus, increased chances of the simultaneous switching of the increased number of devices.

2.2.2.3 Capacitance (C) [22]

Capacitive parasitics result from the routing conductors on the substrate, and the basic principle is the parallel-plate capacitor model ($C = \varepsilon S/d$), where S is the area of the parallel-plate capacitor, d is the insulator thickness, and ε is the permittivity of the insulating material between the plates. However, the parallel-plate capacitor model ignores the fringe effect at the edges of the conductor due to its finite thickness. The fringing field increases the effective area beyond that of the parallel plates of the adjacent conductors [22]. Due to the computational complexity for finding the capacitances of many conductors, many research activities have explored approximations to this calculation [23].

An empirical formula that is computationally efficient with reasonable accuracy is provided by [24]

$$C = \varepsilon\left[\left(\frac{w}{h}\right) + 0.77 + 1.06\left(\frac{w}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5}\right]. \qquad (2.4),$$

where ε is the permittivity, w is the width, h is the height, and t is the thickness of the geometry of a conductor of interest. Methods for more accurately computing the fringing factor can be referred to [24]. For multiple conductors' capacitance, one research study shows the general tendency of typical conductor capacitance as a function of spacing and width. As the spacing increases, the capacitance decreases; as the width increases, the

capacitance increases [26]. Other approaches to capacitance modeling may be referred to [27]-[31].

2.3 Noise

2.3.1 Simultaneous Switching Noise

Continuing advances in VLSI process technology have resulted in many new challenges to interconnect package design. The number of devices on an integrated circuit increases, while they become more sensitive to the power/ground noise [32]. In power distribution networks, the noise mainly results from simultaneous switching noise (SSN), which comes from the large current drawn from a large number of simultaneously switching devices. The SSN is related to the inductive parasitics and the switching characteristics. The impact of the SSN is represented as a voltage drop by the multiplication of the inductance (L) and the current variation per certain time duration (dI/dt), thus, it is frequently known as delta-I noise or dI/dt noise. As expected, SSN can cause logic circuits to switch state falsely, if it is uncontrolled [33]. Signal integrity issues have significant impacts on the performance of high-speed digital systems [34], [35]. Further research on a simplified model for delta-I noise simulation is referred to in [36].

The slope of transient current is on the order of magnitude of 10-1000 mA/ns [37], [38]. In one case, a 3.3 V LVCMOS off-chip driver's are source terminated with an output of 20 Ω and 65 Ω with dI/dt of 60 and 15 mA/ns, respectively [39].

2.3.1.1 Thermal Noise

Thermal noise at resistors was measured by Johnson and reported as a consequence of Brownian motion by Nyquist in 1928 [40], [41]. Thermally agitated charge carriers in a conductor constitute a randomly varying current that results in a random voltage (via Ohm's law). In honor of Johnson and Nyquist, thermal noise has been frequently called Johnson noise, or less frequently, Nyquist noise [42]. Due to the thermal origin, thermal noise power is directly proportional to temperature. Specifically, a quantity called the available noise power is given by

$$P_{NA} = kT\Delta f \tag{2.5}$$

where k is Boltzmann's constant (about 1.38×10^{-23} J/K), T is the absolute temperature in Kelvins, and Δf is the noise bandwidth in Hertz (equivalent brickwall bandwidth) over which the measurement is made. The available noise power over a 1 Hz bandwidth at room temperature can be computed using (2.5) as 4×10^{-21} W (or -174 dBm, which is a number very familiar to those who analyze link budgets in communication channels). The available noise power considers only the frequency bandwidth, and hence it is described as white noise. In reality, white light consists of constant energy per *wavelength*, but white noise has constant energy per *Hertz* [42]. The original works on thermal noise were done for resistors, but FETs (Field Effect Transistors) are essentially voltage-controlled resistors so they too exhibit thermal noise. Particularly, there has been significant interest in CMOS devices in VLSI systems. For MOSFET devices, drain current noise and gate noise can be considered as thermal noise with additional channel parameters that account for both short and long channel devices.

2.3.2 Impacts of Parasitics and Noise on Power Integrity

Signal integrity is affected by several causes such as electromigration, voltage drop from either resistive IR drop or inductive loss, and thermal noise. The main concerns for signal integrity in power distribution networks with data transmission would be attenuation and delay over the power lines. The closed-form expressions for the delay, capacitive coupling, and crosstalk of RC interconnect in VLSI systems is referred to in [43].

2.3.2.1 Attenuation

Since a power distribution system can be considered as a high-order low pass system, the signal attenuation through it is manifest. For the analog I-UWB signals used in the proposed research, the peak voltage level would be restricted within a certain amount of the voltage drop margin. If we pick a relatively large amplitude for an I-UWB signal overlaid with the power supply voltage, it may degrade overall signal integrity for the power supply's intended purpose – delivery of clean power supply voltage. On the other hand, if we pick a relatively small amplitude for an I-UWB signal overlaid with the power

supply voltage, the I-UWB signal might not be detected without increased hardware complexity and/or difficulty. With appropriate I-UWB signaling schemes and power distribution network design, which concerns the package inductance and resistance parasitics, signal attenuation can be overcome.

2.3.2.2 Delay

For high-speed interconnect in VLSI systems, delay has been a dominant factor for deciding the maximum operating speed. With the I-UWB signals in the proposed research, the delay of the peak of the I-UWB pulses is critical for determining the maximum data rate for communications purposes. The delay characteristics of a signal on metal wires have been widely represented by a function in terms of R and C. For very long wires with considerable sheet resistance, propagation delays resulting from the distributed resistance capacitance (RC) on the metal wire can dominate and can be calculated using the Elmore delay model [44].

2.3.3 Signal Transmission Model

2.3.3.1 Lumped Circuit Model

The lumped circuit model consists of representative lumped elements, such as resistors, inductors, and capacitors. In a lumped circuit model, the characteristics are lumped into idealized discrete components with no (or negligible) spatial extent. Thus, for the purpose of the proposed research, we would rather consider the distributed circuit model for on-chip power distribution networks.

2.3.3.2 Distributed Circuit Model

For a dynamic simulator such as SPICE (Simulation Program for Integrated Circuits Emphasis), the simplest model to represent an RC interconnect impedance is a lumped RC circuit. This model suffers from high error since the lumped model does not accurately model the distributed nature of the interconnect impedance. Modeling a distributed RC network as a lumped RC network can produce up to 50 % error [45]. Figure 2.3 shows the

various circuit models of (a) lumped model, and (b)-(h) π/T-type distributed circuit models [46].

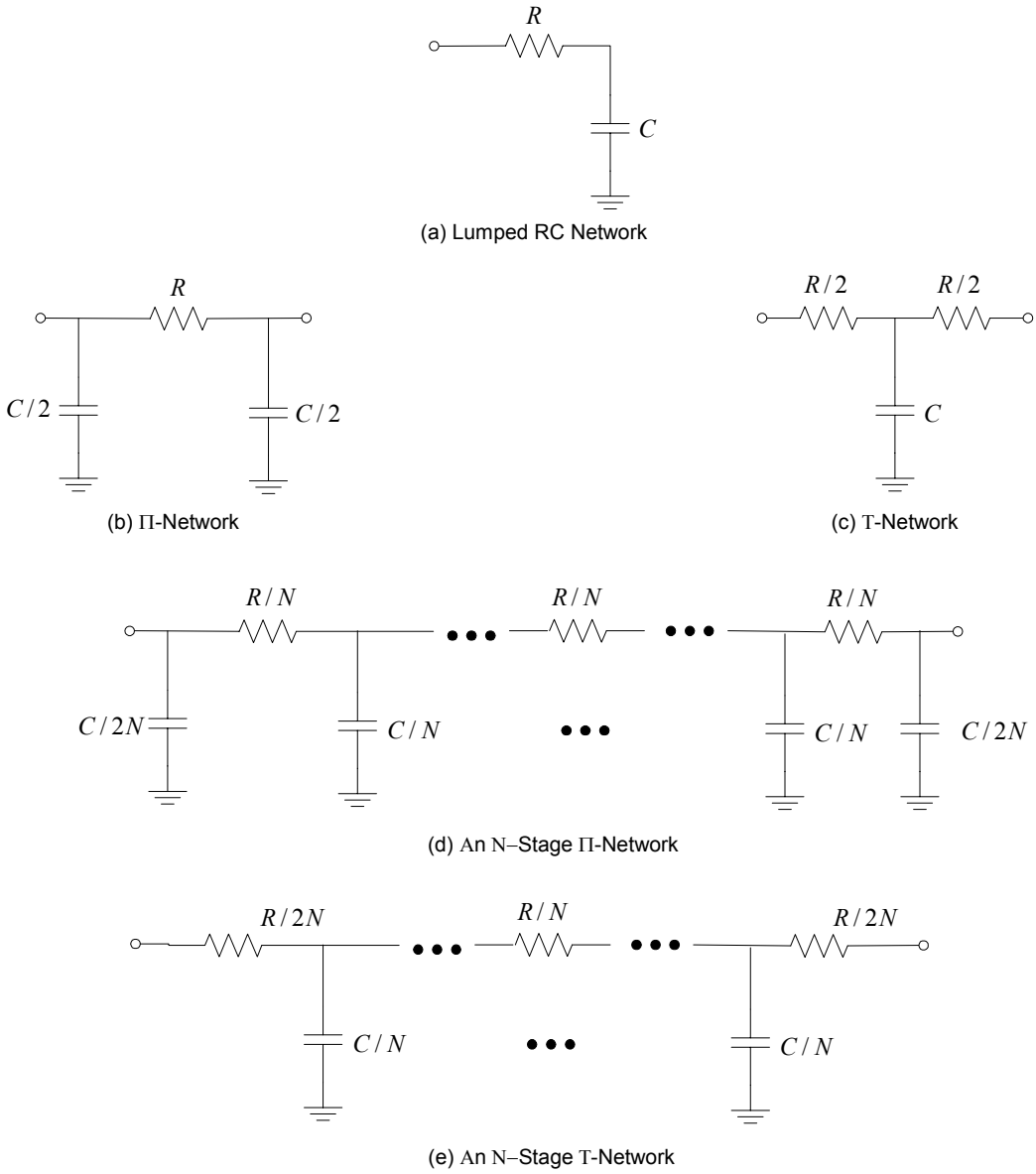


Figure 2.3: Various Circuit Models for an RC Interconnect.

2.4 Packages

Electronic packages contain many electrical circuit components – up to tens of millions – mainly transistors assembled in integrated circuit (IC) chips, but also resistors, diodes, capacitors, and other components as discrete or integrated in a single package. With

the mechanical support of IC packaging and the electrical support of energy, an IC functions well within a certain operating range of temperature. Thus, packaging should provide an adequate means for heat removal. In this context, the main functions of integrated circuits are can be summarized as follows [47]

- Signal distribution, involving mainly topological and electromagnetic considerations
- Power distribution, involving electromagnetic, structural, and materials aspects
- Heat dissipation (cooling), involving structural and materials considerations
- Protection (mechanical, chemical, electromagnetic) of components and interconnections.

Out of the above four major functions of IC packaging; we focus on the second function of power distribution for the proposed research.

There are two different categories of IC packaging – the perimeter I/O type and the area array I/O type packaging. Figure 2.4 shows the two categories of IC packaging. The area array package provides two advantages – 1) higher density of I/Os, and 2) full use of Surface Mount Technology (SMT). The use of SMT is important since it allows area array packages to fit into modern mainstream assembly processes [50].

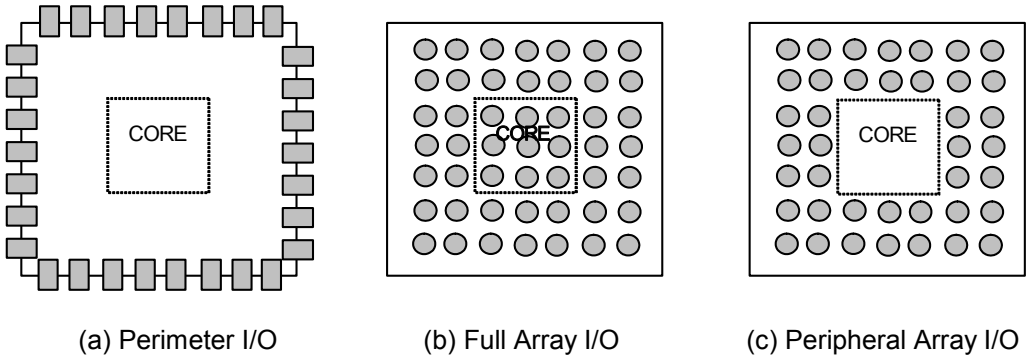


Figure 2.4: Perimeter versus Area Array I/O Package Layout.

2.4.1 Perimeter I/O

2.4.1.1 Quad Flat Package (QFP)

Even with the many advantages of area array packages as mentioned above, the Plastic Quad Flat Package is the most common package in use today, exceeding 10 billion units worldwide in 1995 and doubling that in the year 2000 [47].

2.4.2 Area Array I/O

2.4.2.1 Wire Bonded-Ball Grid Array (WB-BGA)

A wire-bonded BGA package is an area array I/O package which employs the connection via bond wires from the solder ball to the I/Os of a die. Since this type of package uses the bonding wires for electrical and physical connections between the pins and pads, the parasitics of inductance and resistance would be larger than those of flip chip type packages.

2.4.2.2 Flip Chip-Ball Grid Array (FC-BGA)

A flip-chip BGA package is an area I/O package which provides a short distance connection between the package I/Os and the die (chip) I/Os and thus reduced parasitics by flipping the chip inside a package. Figure 2.5 shows the structural difference between the WB_BGA and FC_BGA [51]. Note that the difference between the two packages in length of electrical contact. This difference impacts the inductive loss, and thus voltage drop of an integrated circuit.

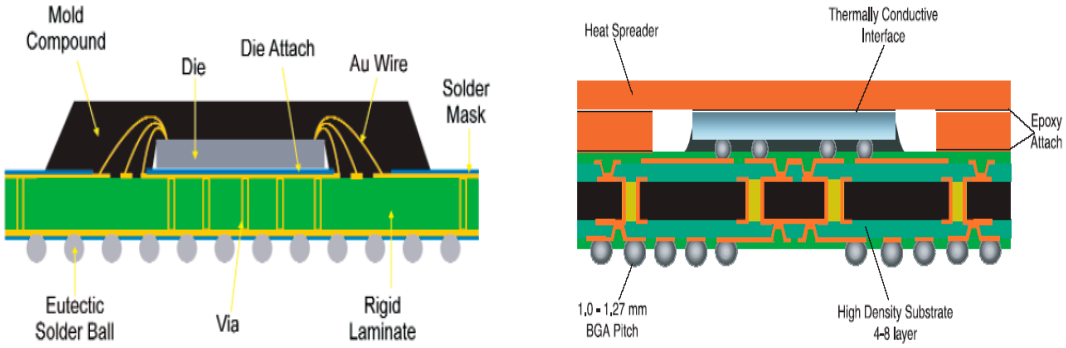


Figure 2.5: Cross-Sectional Views of WB_BGA and FC_BGA packages.

2.5 Pad Cell for Power Supply

2.5.1 Structure

The V_{DD} and Vss (power supply and ground) pads are easily designed and consists of a conjunction of the metal pad layers connected with an appropriate bus, since power is supplied and distributed via bus-like physical routing. Power/ground bus width may be calculated from the power consumption of a chip and its power supply voltage. Multiple power ground pads may be helpful for reducing noise. Placement of the pads can be supported by a pad frame generation program.

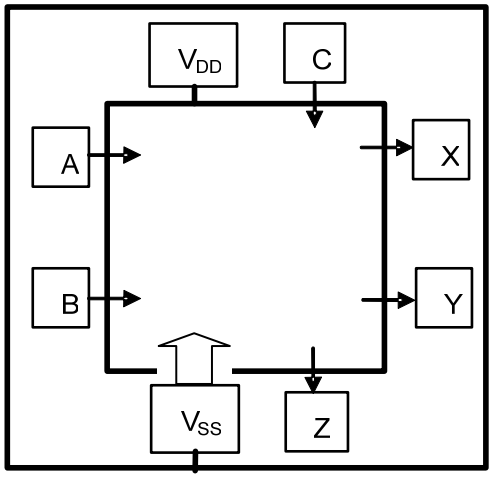
```
LEFT:
INPUT A;
INPUT B;

TOP:
VDD VDD;
INPUT C;

RIGHT:
OUTPUT X;
OUTPUT Y;

BOTTOM:
OUTPUT Z;
VSS VSS;
```

(a) An Pad Frame Description



(b) Generated Pad Frame

Figure 2.6: A Pad Frame Generation.

As illustrated in Figure 2.6, pad frame generation requires a description of the desired location of pads including power and ground pads as well [22]. The figure (a) is a description for I/O frame generation and its resultant placement of I/Os are shown in the figure (b). A generic power pad can be implemented using RC series clamp circuitry and buffers in parallel between power and ground nodes.

2.5.2 ESD (Electro-Static Discharge) Protection

Usually, a combination of a resistance and diode clamps are used to limit potentially destructive voltages. Figure 2.7 shows a typical ESD protection circuit for an input pad [22]. Clamp diodes *Diode 1* and *Diode 2* turn on if the voltage at node N rises above V_{DD} or below V_{SS}. Resistor *R* limits the peak current that flows in the diodes in the event of an unusual voltage excitation. The resistance of the resistor *R* ranges from 200 Ω to 3 kΩ [22]. In the case of a power (ground) pad, the clamp diode *Diode 1* (*Diode 2*) is used for ESD protection using several parallel NMOS (PMOS) transistors.

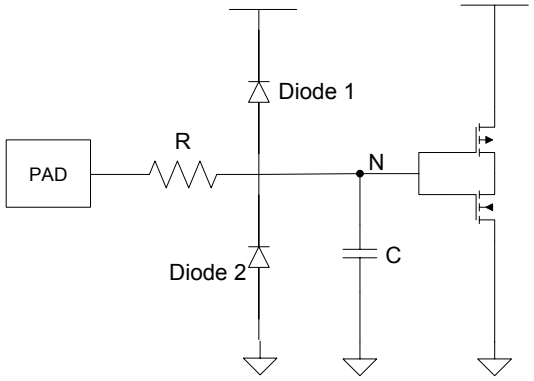


Figure 2.7: Typical ESD Protection Circuit for an Input Pad.

2.6 UWB (Ultra Wideband)

2.6.1 Background

2.6.1.1 Definition

UWB uses scarce frequency resources efficiently, since it coexists with existing systems under a strict regulatory spectral mask. The low power spectral density of UWB is intended to avoid interference to/from the underlying narrowband signals.

Traditionally, all RF signals with a high frequency bound, f_h, and low frequency bound, f_l, have a corresponding index of breadth of band, μ_b, or relative bandwidth (or called as "fractional bandwidth" later) [52]-[54],

$$\mu_b = \frac{f_h - f_l}{\left(\frac{f_h + f_l}{2}\right)} \tag{2.6}$$

The fractional bandwidth is defined as {absolute bandwidth/center frequency} as in (2.6), and the center frequency is defined as the arithmetic mean of two cutoff frequencies. The absolute bandwidth is defined as the difference between two 10 dB[3] cutoff frequencies with respect to the maximum magnitude in the spectrum.

Figure 2.8 compares the power spectral density of UWB to narrowband (NB) and wideband (WB). The definition of bandwidth can vary based on the applications – communications, radar, electromagnetic interference (EMI) and electromagnetic compatibility (EMC) etc. Here, we use the terminology of bandwidth as the ratio of bandwidth relative to the carrier frequency as in RF engineering [55].

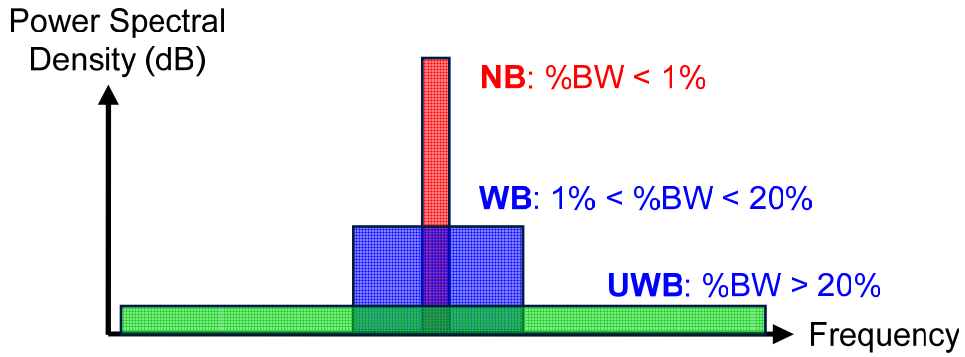


Figure 2.8: Power Spectral Density of NB, WB, and UWB.

Based on the definition of percentage bandwidth (% BW) which is the fractional bandwidth in percent, there are three categories of bandwidth of electromagnetic (EM) waves [56]:

[3] In case of UWB signals, the cutoff frequency is defined to be measured at -10 dB from the maximum in magnitude.

- If EM waves whose instantaneous bandwidth is less than 1% of center frequency, the EM waves are classified as narrow band (NB) signals.
- If the instantaneous bandwidth of EM waves is greater than 1 % but less than 25 %, the EM waves are classified as wideband (WB) signals.
- If the instantaneous bandwidth of EM waves is greater than 25 %, the EM waves are classified as ultra wideband (UWB) signals.

The threshold bandwidth of 25 % in the above classification of an UWB signal is changed into 20 % based on the FCC definition on UWB [57].

$$\%BW = \frac{f_h - f_l}{\left(\frac{f_h + f_l}{2}\right)} \times 100 . \tag{2.7}$$

The FCC defines spectral limitations for UWB but does not specify a signal type, *e.g.* I-UWB or MC-UWB. The FCC classifies a device as UWB if the signal bandwidth is greater than either 0.2*center frequency in fractional bandwidth or 500 MHz in absolute bandwidth [57]. UWB communications systems operate in the band from 3.1 GHz to 10.6 GHz, and the FCC limits the radiated power to -41.3 dBm/MHz over this frequency band.

2.6.1.2 *Advantages* [52], [81]-[83]

Compared with narrowband systems, UWB has several advantages. First, one representative characteristic of UWB is that its radiated power is at least an order of magnitude less than narrowband radios [58]-[61]. This enables the advantages of low probability of detection and intercept, reuse of existing spectrum, minimal impact to existing users, and energy efficient transmitters [60], [62]-[64]. Next, the wide bandwidth provides an extremely high data rate, which can be traded for longer range or robustness [65]-[71]. High data rate can be achieved by either the increase of bandwidth or signal-to-noise ratio in AWGN. The direct benefit of UWB is to significantly increase data rate due to the ultra wide bandwidth, if we recall the Shannon-Hartley channel capacity theorem. Figure 2.9 shows the computed channel capacity over a range of signal-to-noise ratios

(SNRs) and bandwidths. In order to achieve a data rate of 500 Mbps, a UWB signal whose bandwidth is 500 MHz can achieve the data rate with an SNR of 0 dB, but a NB (narrow band) signal whose bandwidth is 40 MHz can achieve the data rate only with SNR of 37 dB.

The wide bandwidth also gives UWB relative immunity to multipath fading effects [70], [65]. With an appropriate receiver, a UWB system may even rake energy from the resolvable multipaths to enhance the channel capacity in terms of data rate. The wide instantaneous bandwidth provides fine time resolution for use in radar and imaging applications. Finally, the carrierless nature of I-UWB enables the simple, low-power, low-cost hardware implementations via direct conversion and other techniques that differ from the traditional narrowband/wideband approaches of using intermediate oscillators and mixers [65]-[67].

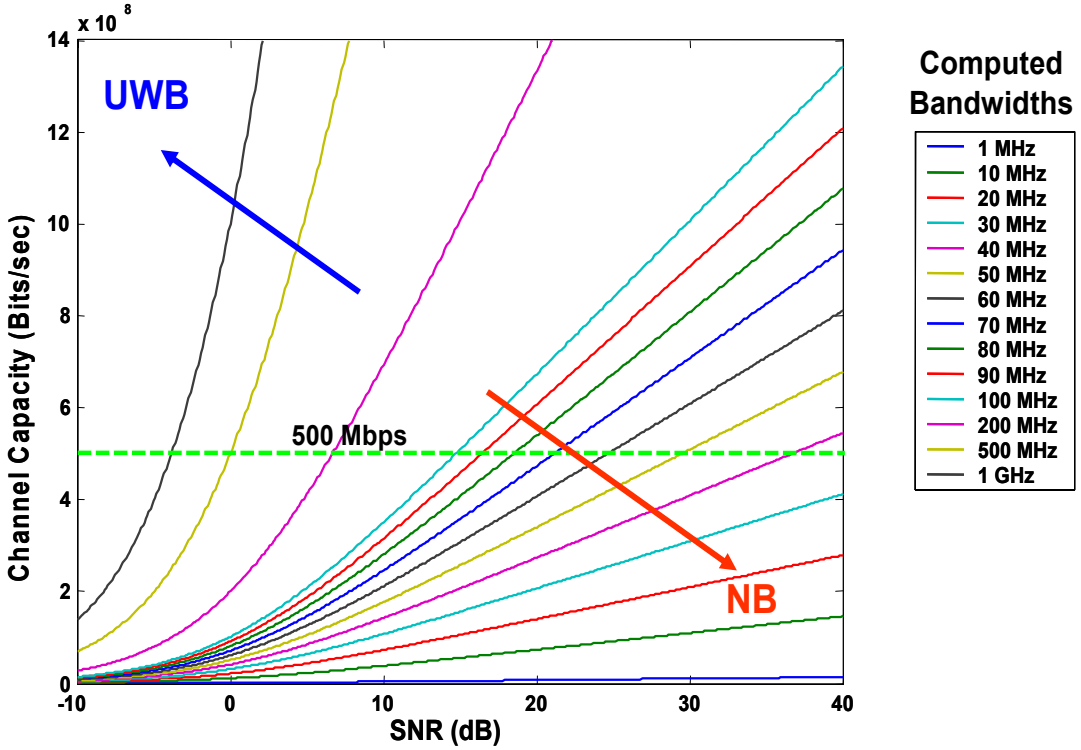


Figure 2.9: Computed Channel Capacity vs. SNR with Bandwidth.

2.6.1.3 *Signaling* [52], [81]-[83]

Two representative forms of UWB signaling have been investigated, which differ in the method used to occupy the spectrum. At one extreme, a sharp impulse occupies the band as in impulse-based UWB (I-UWB); and at the other extreme, many simultaneous narrowband tones occupy the band as in multi carrier UWB (MC-UWB) [13], [15]. Several solutions exist in between these extremes. Due to the advantages of I-UWB for power distribution networks to provide clean power and data transmission, this section focuses on I-UWB signaling.

A narrow pulse of I-UWB signaling may occupy several GHz of spectrum, but it may last less than a nanosecond. The pulse is repeated at a low pulse repetition interval (PRI) that lasts from nanoseconds to microseconds, and thus transmitted I-UWB signal is

$$s(t)=\sum_{i=-\infty}^{\infty} A_i(t)\, p\left(t-iT_f\right) \tag{2.8}$$

where $A_i(t)$ is the amplitude of the pulse, $p(t)$ is the received pulse shape with normalized energy, and T_f is the frame time or the PRI. The PRI is generally much longer than the pulse width, which results in low duty cycle (~1%) [72].

Common pulse shapes for UWB use the Gaussian pulse [73]-[75]. A Gaussian doublet (second derivative) is described in (2.9) in terms of t_n, which is the time difference between the minimum and maximum signal values. For the Gaussian doublet, the pulse width = 4*t_n, the center frequency = 0.8/t_n, and the bandwidth = 1.2/t_n.

$$p(t)=\left(1-4\pi\left(\frac{t}{t_n}\right)^2\right)\cdot exp\left(-2\pi\left(\frac{t}{t_n}\right)^2\right) \tag{2.9}$$

Two representative modulation schemes for I-UWB are orthogonal (non-overlapping) pulse position modulation (PPM) and binary antipodal amplitude modulation, which are equivalent to the same signal constellation as frequency shift keying (FSK) and binary phase shift keying (BPSK) in narrowband systems, respectively. For BPSK, the pulse train of (2.8) becomes

$$s(t)=\sum_{i=-\infty}^{\infty} A_i(t)\, p\left(t-iT_f\right) \tag{2.10},$$

where $A_i(t) = d_i(t)$ is the amplitude of the i^{th} pulse modulated by data bit $d_i(t) \in [-1,1]$.

For PPM, the pulse train of (2.8) becomes

$$s(t) = \sum_{i=-\infty}^{\infty} Ap\left(t - iT_f - \delta d_i(t)\right) \qquad (2.11),$$

where $d_i(t)$ shifts the pulse in time by some multiple δ, which is larger than the pulse width to assure an orthogonal signal set. For PPM, a single pulse can represent multiple bits or chips.

Figure 2.10 shows (a) BPSK and (b) 4-ary PPM, in which the polarity of the pulse and four different orthogonal (non-overlapping) pulse positions modulate the data.

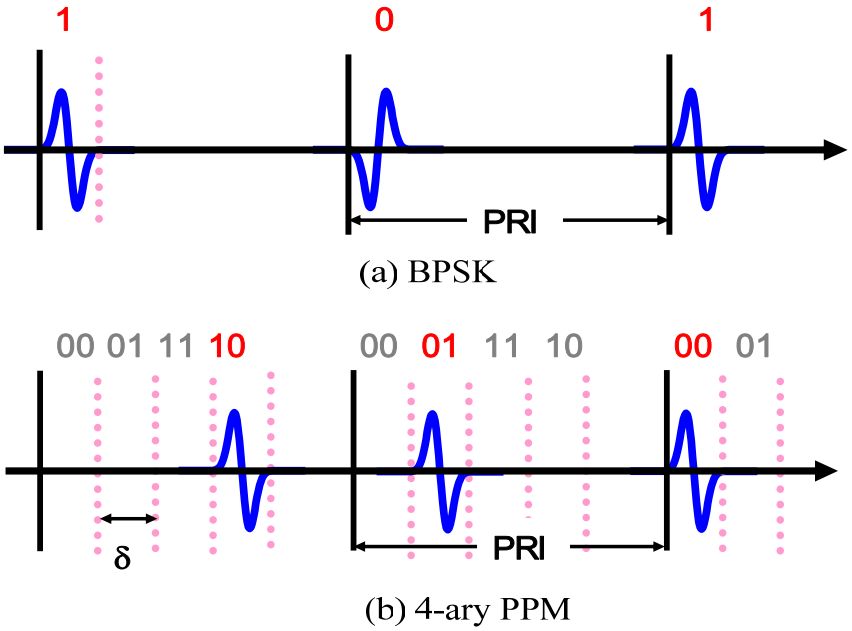


Figure 2.10: Modulation Schemes for I-UWB.

2.6.1.4 *Channel Model* [52], [89]

As a signal propagates through a channel, it experiences reflection, scattering, and diffraction, and these effects result in large-scale propagation and small-scale fading characteristics. The model proposed in the IEEE 802.15.3a standardization process for high rate UWB applications is widely used as an indoor UWB channel model [76], [77]. It is based on the Saleh-Valenzuela model, and it considers four scenarios that depend on link

distance and the existence of a line of sight (LOS) path. The channel is modeled as a finite impulse response (FIR) filter.

$$h(t) = \sum_{i=1}^{N_p} \beta_i \delta(t - \tau_i) \tag{2.12}$$

where β_i is the amplitude and polarity of the i^{th} reflection, τ_i is the delay of the i^{th} reflection, $\delta(t)$ is an impulse function and N_p is the number of reflections. The channel model gives these parameters random values whose statistics are determined from observation [76], [77]. A typical channel may incur 30-60 resolvable reflections that continue for less than 100 ns after the first path arrives. Other channel models are currently under development for UWB radios in environments such as warehouses, human bodies, and sports stadiums.

Considering the possibly harmful effects of multipath fading, I-UWB systems maintain their performance much better than narrowband systems. One study found that I-UWB signals required a fading margin[4] of only 1.5 dB [78] compared to about 35 dB for a narrowband signal in a Rayleigh fading environment [79].

However, the channel impulse response obtained in the indoor radio channel environment cannot be used for the proposed research since the channel environment for power distribution networks is quite different from the radio environment. That is, there would be a greatly reduced number of multipaths for the power distribution networks. Further, the power distribution network would experience ringing and resonance within a drastically shorter period of time compared to the indoor UWB radio channel. The channel response for our experiments will be considered in relation to the actual parameters of power distribution networks. We consider the power distribution network as a distributed RLC mesh network as discussed in Section 2.2.5.

2.6.1.5 Impact of I-UWB Signaling

Since our communication signals overlay the power supply voltage level for the proposed approach, they should not increase the noise level of power supply voltage. If we consider rectangular pulses with a raised cosine filter or other traditional signaling methods

[4] *Fading margin can be defined the link budget allowance that accommodate expected fading, for the purpose of ensuring that the required quality of service is maintained.*

with carrier (as in continuous wave modulations), it would increase the possibility for the signals to disturb the power lines, which require the noise level as low as possible. Whereas rectangular pulses or sinusoidal waves would definitely disturb the power supply, I-UWB pulses would look like noise spikes and blend in with the existing noise. Figure 2.11 shows the waveforms of the two signals; 1) I-UWB and 2) Monotone overlaid on the power lines for comparison purposes. In the figure, the carrier frequency is 10 times faster than the PRI of I-UWB signal. In addition, the hardware complexity for the continuous wave modulated signaling would not be reasonable due to the requirement of more elaborate demodulation circuits than that of I-UWB.

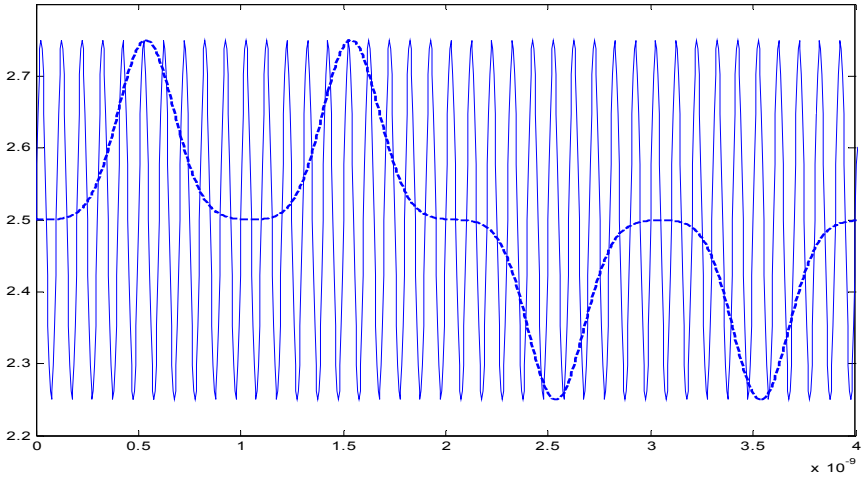


Figure 2.11: I-UWB and Monotone Signal Overlaid on the Power Supply Voltage.

2.6.1.6 Applications

2.6.1.6.1 New Application

Due to the many advantages of ultra wideband signaling such as high data rate, low transmitted power, low probability of detection/intercept, and imaging capabilities, UWB is an attractive radio technology for numerous applications including short-range high data rate wireless communications [80], indoor tracking, location, surveillance, automotive, body area network, and wireless sensor networks. To our knowledge, there has been no research of UWB data communications over power distribution networks in a system-on-

chip environment. The following four sections present the major applications of UWB in the literature.

2.6.1.6.2 *Radar* [52], [84], [82]

From the long history of UWB, I-UWB has been naturally suitable to radar applications with wide bandwidth and a low duty cycle [85]. The wide bandwidth identifies more target information, improves range accuracy, improves resilience to passive scatterers, mitigates destructive multipath effects from ground reflection, and enables a narrow antenna beam pattern [65]. The low radiation power under the spectral mask provides low probability of intercept and detection. Pulses with a low center frequency (and thus a significant proportion of power in the large wavelengths) can be used to penetrate solid structures such as concrete walls. I-UWB can provide one low-cost interface for both a sensor and a communications system.

With these advantages, I-UWB can be applied for vehicular radar [86], ground penetrating radar (GPR) [87], through-walls imaging, and medical imaging [88].

2.6.1.6.3 *Communications* [52], [89], [82]

More recent applications focus on short-range, high-rate wireless communications such as wireless personal area networks (WPANs), which construct a network with a limited number of devices in a small coverage area (within 10m) [91]. The proposals for the IEEE 802.15.3a standard define medium access and physical layers with extremely high data rates (up to Gbps range) for multimedia applications [92]. The most common application for WPAN is cable replacement for high-speed devices such as video players and PC wireless USB devices. Another cable replacement application is wearable peripherals for health, entertainment, or military purposes with the support of body area networks (BANs).

2.6.1.6.4 *Communications with Location Awareness* [52], [89], [90], [82]

With the dual use of the above two conventional applications of radar and communications, I-UWB offers communications with location awareness [71], [94], [95]. I-

UWB can have ranging capability with sub-centimeter accuracy even at low SNR with possibly one transceiver. Nodes can also share distance estimates to cooperatively compute location information, which is an important feature for many sensor network applications and network protocols [96], [97].

The IEEE 802.15.4a standard [93], as a potential example for communications with location awareness, focuses on a UWB physical layer to achieve low power, flexible link distances, and precision ranging particularly for outdoor applications such as wireless sensor networks in wide open areas. The standard provides simple, pervasive, and seamless wireless connectivity among devices. Suggested application spaces include sensors, controllers, and logistical devices [94], [95].

2.6.1.6.5 *Sensor and Ad Hoc Networks* [89], [82]

Many recent applications of UWB are in the area of ad hoc and sensor networks, while ad hoc and sensor networks have been steadily investigated in the literature for several years from a narrowband perspective. Ad hoc and sensor networks can utilize the location awareness of UWB for networking in a sensor field without existing infrastructure, *i.e.*, the network is responsible for self-configuration [98]. For sensor networks, power consumption, cost, and Quality of Service (QoS) are crucial design factors for the Physical layer (PHY) and Medium Access Control (MAC) protocol [98]-[100], [101], [102].

2.6.2 Impact of I-UWB on Power Distribution Networks

2.6.3 Transceiver Architecture

This section reviews prior work on an I-UWB transmitter/PPM modulator and receiver for the proposed research. This work builds upon these components, but it may use others [103]-[107].

2.6.3.1 Transmitter

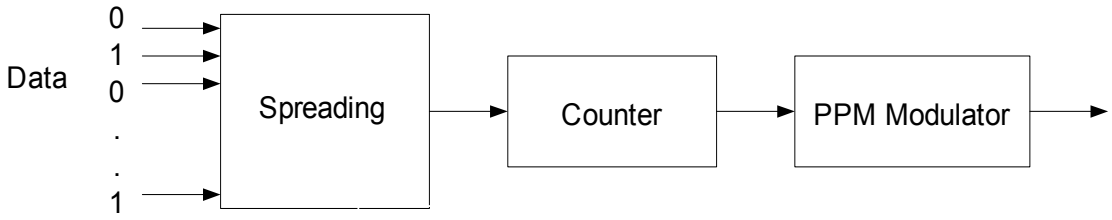
The transmitter can be either 1) a modulator or 2) a generic I-UWB transmitter which consists of a pulse generator, a corresponding filter, and a control block. The

transmitter assumes the DS-CDMA (Direct Sequence Code Division Multiple Access) principle for data transmission.

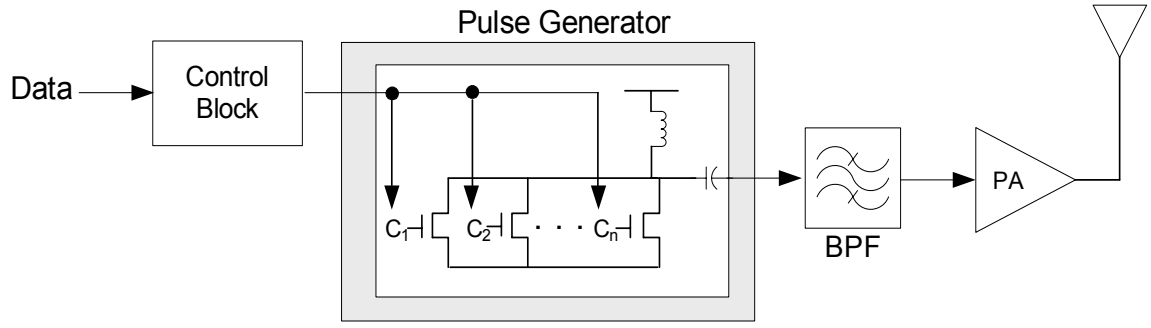
A modulator can provide appropriate modulation schemes. For the one-way communication in the proposed research, Pulse Position Modulation (PPM) with the DS-CDMA principle is selected. PPM would not increase the voltage amplitude over the power supply voltage level, which in turn might increase the voltage drop. An IC with this type of transmitter can be used for VLSI testing in massive parallel scan designs. The parallel scan-out data can be spread, and each bit of spreading code is added and transmitted via PPM within a subsection in time. For example, if 4-bit spreading codes were used, at each chip[5] period, the spread bits are added and transmitted via PPM as in Figure 2.12(a). Further details will be investigated through the case study presented in Chapter 5.

A generic I-UWB transmitter is based on the pulse generator in Figure 2.12(b) [67], which can generate various pulse shapes and data rates through a configurable control block. Depending on the desired data rate and pulse shape, the control block provides the appropriate control voltage for the gate of each NMOS transistor connected in parallel to control the direction of current flow and output voltage. The band pass filter limits the output to the FCC regulated -41.3 dBm/MHz over its bandwidth from 3.1 GHz to 10.6 GHz. Digital timing control determines the PRI. The total power from the circuitry is less than 10 μW.

[5] Typically the bit in each codeword can be considered as chip as in spread spectrum communications. The one cycle period consists of several chip periods (four chip periods in this example).



(a) A PPM Modulator w/ Spreading.



(b) A Generic I-UWB Transmitter w/ Programmable Pulse Generator.

Figure 2.12: Transmitters for the Proposed Data Communications.

2.6.3.2 Receiver

The receiver receives the spread data, so it simply needs to recover each chip data and decide the final information bit within a system clock period. The receiver can be constructed with a simple data recovery unit which consists of a one-bit comparator and an accumulator. A matched filter or a correlator may be used for the enhancement of performance with increased hardware complexity. Three times of over-sampling is enough for reasonable signal integrity according to our simulation results from a case study.

Figure 2.13 shows the proposed receiver architecture. It displays the overall circuit diagram consisting of a one-bit comparator (or a correlator) for hard decision and a data recovery unit. The data recovery unit receives the decided bit (r_i) from the one-bit comparator for each chip duration, compares it with the reference codeword (c_i), adds the number of differences, then decides the final bit value in one clock cycle. A one-bit comparator can be implemented based on two cascaded, capacitively coupled, auto-zeroed

inverters followed by a dynamic register [22], [108]. Further details of the data recovery schemes will be investigated in Chapter 4.

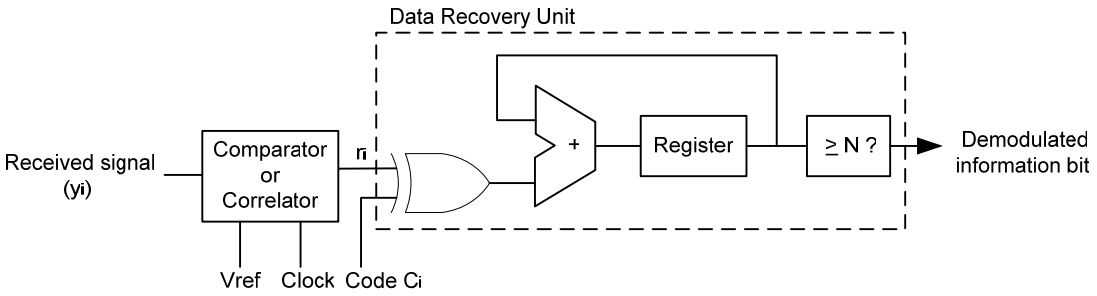


Figure 2.13: Proposed Receiver Architecture.

2.6.4 Multichannel Data Transmission

2.6.4.1 Time Division

The time division multiple access (TDMA) scheme is a transmission technology that allows a number of users to access a single channel (originally radio frequency channel) without interference by allocating unique time slots to each user within a channel. TDMA can fail to transmit or receive due to the occupancy problem, sensitivity to multipath interference, and high cost compared with that of CDMA (Code Division Multiple Access).

2.6.4.2 Code Division [89]

CDMA is a digital cellular technology that uses spread spectrum techniques. Unlike competing systems, such as GSM (Global Systems for Mobile Communications), that use TDMA, CDMA does not assign a specific time or frequency channel to each user. Instead, every channel uses the full available spectrum. Individual communications are encoded with a pseudo-random digital sequence. Different code channels, ideally orthogonal to each other, allow simultaneous transmission for multiple users. With this structural support for no collisions, users avoid the overhead of handshaking and detecting medium activity. In I-UWB, the channel may be divided into code spaces by employing time hopping codes [109]-[116] or direct sequence codes [117]-[120].

Time-hopping is the most well-known form of code division for I-UWB signals. The k^{th} user transmits the signal

$$s^{(k)}(t) = \sum_{i=-\infty}^{\infty} A_p \left(t - iT_f - c_i^{(k)} T_c - \delta d_{\left\lfloor \frac{i}{N_c} \right\rfloor}(t) \right) \tag{2.13}$$

with time-hopping code $c_i^{(k)}$ and chip duration T_c. Figure 2.14 shows time hopping for a length N_c = 3 code, which could support up to eight users sub-optimally. The figure (a) shows the spreading over the hopping codes for both users; User 1 transmits a data '0' and User 2 transmits a data '1'. The time hopping code determines the slot number and the data determines the pulse position within that slot. Note that pulses from two different users may interfere with each other in the same slot (as in the second chip), but spreading multiple data chips over a code mitigates such multiple access interference.

Direct sequence UWB (DS-UWB) is similar to well-known narrowband direct sequence spread spectrum techniques, but I-UWB communication systems spread the signal in time as opposed to frequency. A user transmits a continuous train of data with the amplitudes of the chips modulated by the spreading code. The DS-UWB waveform for the k^{th} user in Figure 2.14 can be represented as

$$s^{k}(t) = \sum_{i=-\infty}^{\infty} \sum_{j=1}^{N_c} A_p \left(t - iT_f - jT_p \right) \left(c_j^{(k)} \right) d_i(t) \tag{2.14}$$

with spreading code $c_j^{(k)}$ for the j^{th} pulse in a length N_c code.

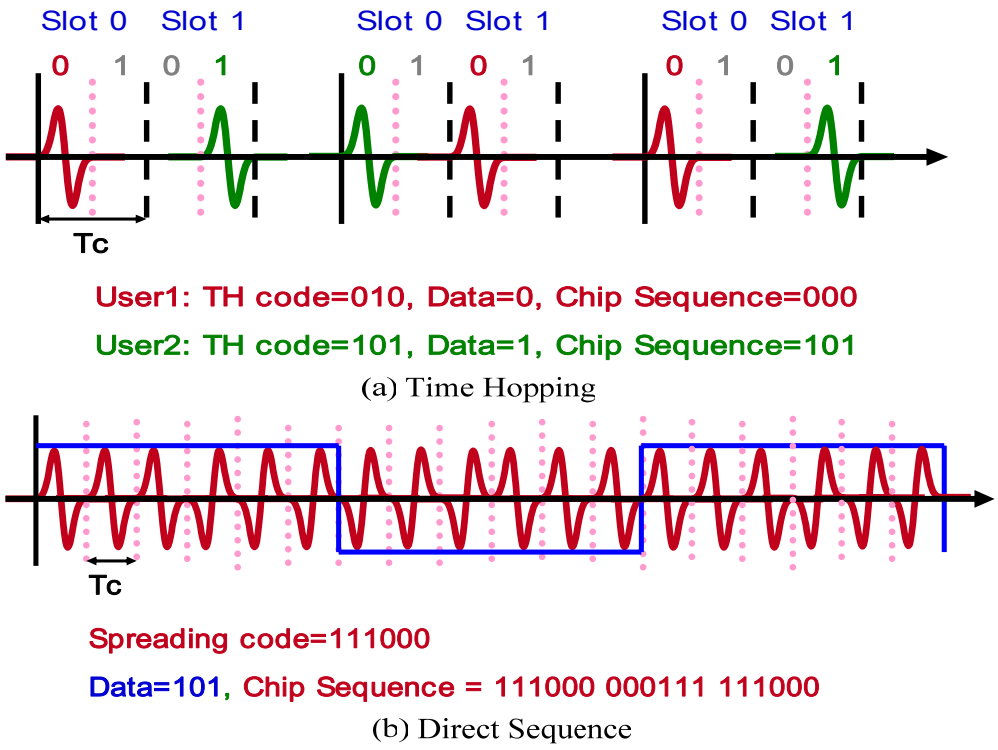


Figure 2.14: Time Hopping vs. Direct Sequence Multiple Access.

2.7 Summary

In this chapter, we presented an overview of power line communications, power distribution networks, packages, pad cells of a power IO, and ultra wideband communications.

Section 2.1 briefly presents the scope of the application for the proposed data communications schemes over the existing power distribution networks.

Section 2.2 investigates power distribution networks, noise, the impacts of parasitics, and the signal transmission model.

In Section 2.3, we investigated the representative packages of integrated circuits, including perimeter IO type packages and area array IO type packages. With array IO type packages, we can support an increased number of IOs with reduced parasitics. The proposed research would reduce the number of power pins and signal pins as well.

Section 2.4 discusses the power pad structure, including the diode for ESD protection. Although the circuit and function of power pads are not complex, the design for

high performance IO is dominant for high-speed interconnect in high performance VLSI systems.

In Section 2.5, we investigated ultra wideband communications, including the background, the applications, the transceiver architecture for the proposed research, and multichannel data transmission schemes. The direct-sequence code division multiple access for impulse-based ultra wideband (DS-UWB) is our baseline scheme for data communications over power distribution networks.

Chapter 3

Microscopic Channel Model

In this chapter, we investigate a microscopic [6] channel model. A microscopic channel consists of an IC package, power distribution network, solder ball, C4 bump, and decoupling capacitor. The main component of the microscopic channel model is the IC package. We focus on the modeling of the planar structure IC package. We develop this microscopic channel model based on the cavity resonator model (CRM). Then, we present the impedance matrix method for solving a transient response at a specific location within the power distribution network of an IC.

3.1 Modeling Philosophy

The philosophy behind the overall modeling uses the three major tools of Matlab, PERL, and SPICE. Matlab is used for modeling a CRM-based planar IC package. PERL is used for generating power distribution networks which will be used for circuit simulations in SPICE. SPICE is a well known circuit simulator and accepts netlist or circuit description which is possible via PERL (Practical Extraction and Report Language) scripting for a large power distribution network without directly making the actual circuit.

3.1.1 Impedance Matrix Method

We use a simple and convenient method for finding channel responses in the time domain. The main idea is to use the frequency domain impedance characteristics of the channel model based on the CRM. If we have N-ports for a planar structure IC package, we can construct an N/2-channel N-port network for it. Each transmission port (source) has a UWB signal overlay DC power supply source, and each receiver port (load, current sink, or

[6] Hereby we coin the term *microscopic* for differentiating the channel from the conventional communications channel through the air.

destination) has a current consumption. Since the CRM (that will be presented in detail in Section 3.2) is based on the N-port network and provides the impedance matrix of the N-port networks, we use the matrix for obtaining a transient response based on Ohm's law [V]=[Z][I] where [V] is Nx1 column vector, [Z] is NxN square matrix, and [I] is Nx1 column vector in frequency domain. For the final transient responses, we need an inverse Fourier transformation.

3.1.2 Methodology

We use three major modeling tools of MATLAB, PERL, and SPICE for channel modeling and simulations. The overall methodology for modeling and simulation is shown in Figure 3.1. As shown in the figure, the light blue, cyan, and green indicates the tasks in MATLAB, PERL, and SPICE. First, we develop a model for an IC package with the geometry, number of ports, and port locations of planar structure package. At the same time, the power distribution network (PDN) is designed by considering the number of metal layers, metal wires, metal width, and maximum tolerable IR drop.

We used PERL for PDN generation rather than an actual equivalent circuit for efficiency. For example, if we want to construct a 2-dimensional single layer N-stage Π-type distributed RLC circuits for a PDN, we need to describe (or input) $(N+1)^2$ + 2*2N(N+1) actual components (more precisely, $(N+1)^2$ capacitors, 2N(N+1) resistors, and 2N(N+1) inductors. In addition, with this direct implementation of the PDN into equivalent circuits, it requires more effort and takes more time to change the PDN. With the use of PERL, we can save time and be more flexible for changing the PDN. With inputs from a SPICE output (AC frequency simulation results at some PDN inputs), the impedance matrix for the IC package of interest will be constructed. Once the impedance matrix is built, its inversion should be obtained to derive currents at particular locations. We obtain the voltage response at certain location by multiplying the inverse of the impedance matrix ($[Z]^{-1}$) by voltage matrix ([V]). With the currents, we can obtain the voltage response of the specific port based on Ohm's law in frequency domain. Using an inverse fast Fourier transformation (I-FFT), we can obtain the target transient response at the specific port

location which is the input of the PDN. We use the temporal characteristics for SPICE input for measuring waveforms at various locations in the PDN.

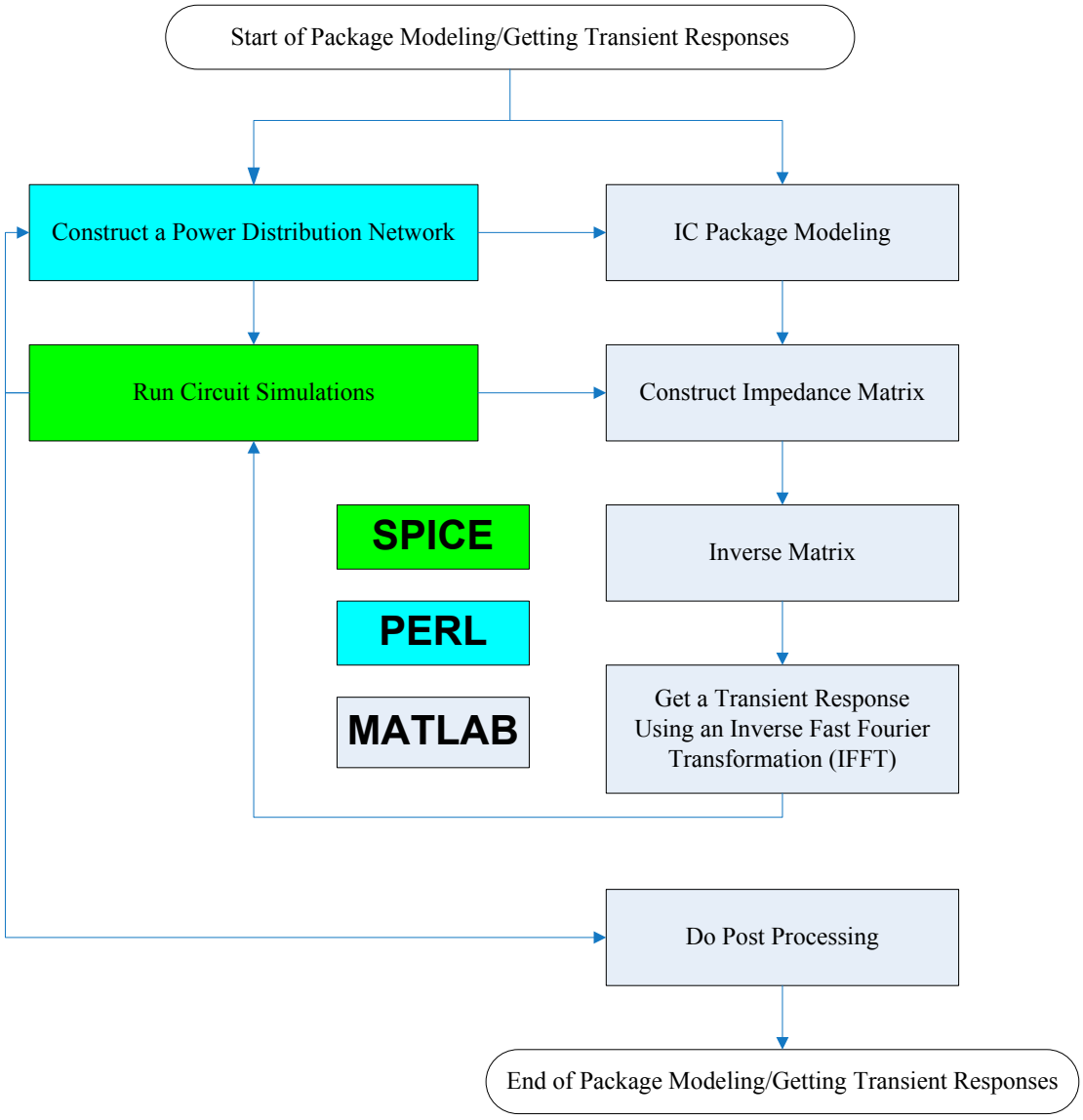


Figure 3.1: Overview of Modeling and Simulation Methodology.

An impedance matrix for an N-port networks can be represented by an NxN matrix (3.1) based on [121]. Each impedance component of self- and trans-impedance can be obtained by the cavity resonator model for a planar structure IC package. N-port networks can be modeled and treated by rank (N) matrices. The main inputs for the network are

current and voltage. The representative impedance (Z) matrix for an N-port network can be expressed as follows (3.1).

$$\begin{bmatrix} V_1 \\ V_2 \\ . \\ . \\ V_N \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} & . & . & z_{1N} \\ z_{21} & z_{22} & . & . & z_{2N} \\ . & . & . & . & . \\ . & . & . & . & . \\ z_{N1} & z_{N2} & . & . & z_{NN} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ . \\ . \\ I_N \end{bmatrix} \tag{3.1}$$

Equation (3.1) can be written as a simpler vector notation of $V = Z \cdot I$ with two Nx1 column vectors and an NxN square matrix. With the N-port network voltages, input voltages, and current sources, we can obtain the output voltage (V_N) at particular port location with the load resistor R_L, which consists of the parallel impedance of Z_{pdn} and Z_{decap}.

With the current/voltage relationship and the circuit configurations, (3.1) can be modified as (3.2) and it is illustrated in Figure 3.2.

$$\begin{bmatrix} V_0 - I_1 \cdot R_s \\ V_0 - I_2 \cdot R_s \\ . \\ . \\ -I_N \cdot R_L \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} & . & . & z_{1N} \\ z_{21} & z_{22} & . & . & z_{2N} \\ . & . & . & . & . \\ . & . & . & . & . \\ z_{N1} & z_{N2} & . & . & z_{NN} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ . \\ . \\ I_N \end{bmatrix} \tag{3.2}$$

(3.2) can be expressed as (3.3).

$$\begin{bmatrix} V_0 \\ V_0 \\ . \\ V_0 \\ 0 \end{bmatrix} = \begin{bmatrix} z_{11} + R_s & z_{12} & . & . & z_{1N} \\ z_{21} & z_{22} + R_s & . & . & z_{2N} \\ . & . & . & . & . \\ . & . & . & z_{N-1,N} + R_s & . \\ z_{N1} & z_{N2} & . & . & z_{NN} + R_L \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ . \\ I_{N-1} \\ I_N \end{bmatrix} \tag{3.3}$$

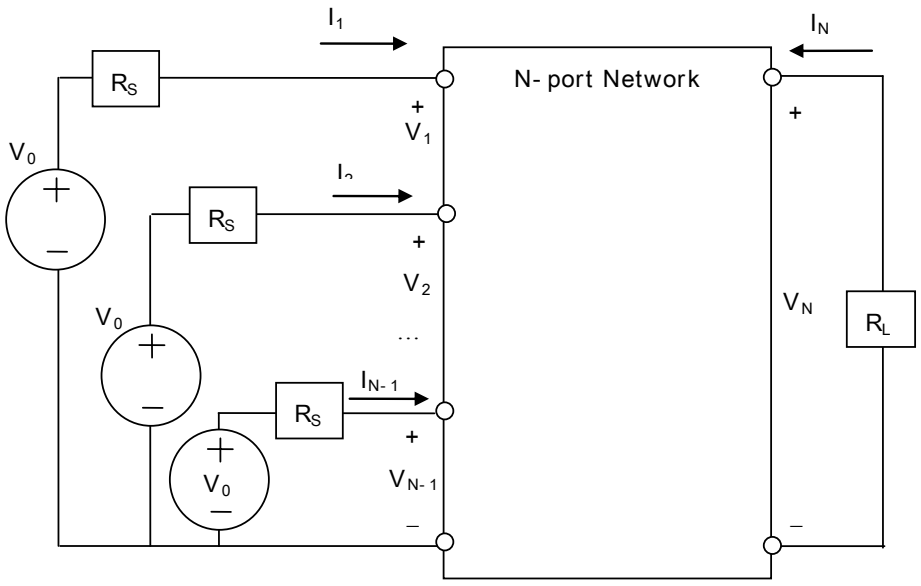


Figure 3.2: N-port Network and its Application Models for the Experiments.

(3.3) can be written as in a simpler vector notation of $V_{\text{mod}} = Z_{\text{mod}} \cdot I$. If we want to know the voltage waveform at particular port location N (or any arbitrary location r), we can do this by inputting any other ports with voltage/current inputs. First, we find the inverse matrix of Z_{mod}, and then we do the multiplication of the inverse matrix of Z_{mod} by V_{mod}. Thus, the currents at all the port locations are obtained. Once the current at the port location of interest is obtained, the voltage waveform at the port location can be obtained by the relationship $V_N = -I_N \cdot R_L = -I_N \cdot \left(Z_{pdn} \| Z_{decap}\right)$. V_0 may be either V_0 or V_{dc} dependent on the applications.

3.1.3 Advantages of the Methodology

The primary objective of a power integrity designer is to select the appropriate type and location of components to meet the impedance target for a given system. A majority of the power delivery system design factors, such as the number of power/ground layers and the location of capacitors, is made before actual fabrication. Conventional validation for the power distribution systems has been carried out in the time domain by monitoring the noise on the die sense lines while a high activity program is run on the IC of interest. Due to the

uncertainty associated with the die excitation model, it is inconvenient to use the time domain measurement data to calibrate the simulation models. In order to overcome this uncertainty, a frequency domain scheme is used to measure the impedance profile of the power distribution system as a function of frequency. In addition to this requirement for the calibration, note that with the frequency domain modeling and processing with MATLAB, the computation will be much faster than the time domain simulation with SPICE.

3.1.4 Scope: Planar Structure

In this thesis, the channel model is primarily confined to the planar structure IC package and for the non-planar structure IC packages, the PDN-package can be considered as a whole in the time domain by constructing the whole equivalent circuit and running SPICE.

3.2 Planar Structure IC Package Model

In this section, since power-ground planes and PDN are major components[7] contributing to work as a channel for communications, we investigate an efficient channel model in the literature in terms of its accuracy and computational complexity. Then we develop a planar structure IC package model using MATLAB™ and incorporate it with a power distribution network model in SPICE. Several impedance characteristics are provided as representative channel characteristics of the proposed data transmission. Prior to mentioning the modeling the power-ground planes, note that there is no need to apply UWB signals to all the power pins; only required power pins in their optimal locations receive UWB pulses with method illustrated in Figure 3.3.

[7] Parasitics of solder balls and C4 bumps can be ignored due to their RLC parasitics and transfer characteristics; See Section 3.3.

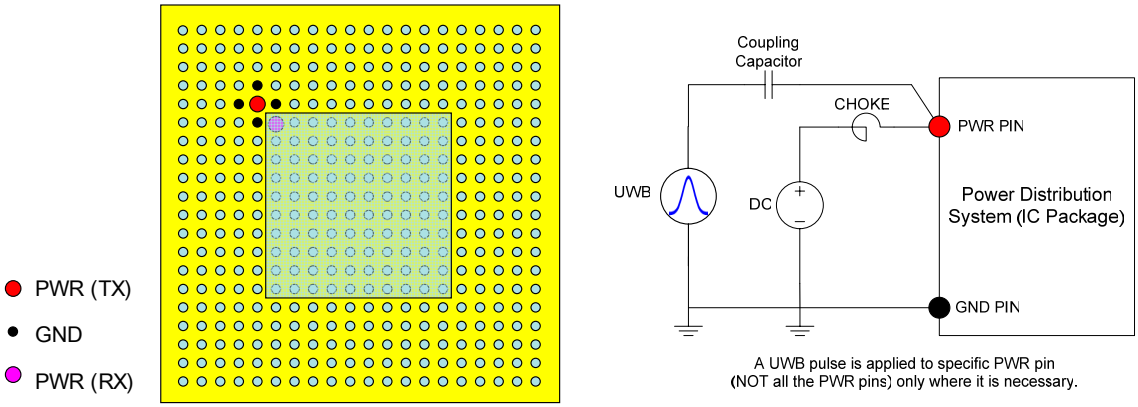


Figure 3.3: Illustration for a UWB Signal Input on a Specific Power (PWR) Pin.

3.2.1 Cavity Resonator Model (CRM)

The most important element of the PDN in high speed packages running over GHz are planes [121]. Recent publication shows the computational efficiency and its accuracy for the modeling and simulations of a planar structure IC package based on the cavity resonators [121]. Differing from the past approaches based on a lumped circuit or an inductive network, the CRM considers wave propagation, which is far more accurate for current high speed VLSI systems [121]. The power-ground plane pairs work as cavity resonators supporting radial waves which propagate into the space between the plane pairs. At the edges of the planes, the radial waves are reflected and cause resonance in the steady state. This behavior can be represented by computing the impedance characteristics seen by an arbitrary location of ports on the planes. In this thesis, we adopt this planar package model which secures accuracy with computational efficiency.

3.2.2 Impedance Characteristics of Power–Ground Planes

Based on [121], for a single plane pair, we have impedance characteristics represented by following equation, which represents the equivalent circuit formed by using parallel resonant circuits and ideal transformers. The impedance between port *i* and port *j* is given by

$$Z_{ij}(\omega)=\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{N_{mni}N_{mnj}}{1/\,j\omega L_{mn}+j\omega C_{mn}+G_{mn}}$$

where

$$L_{mn}=d/\left(\omega_{mn}^2 ab\varepsilon\right),\ C_{mn}=ab\varepsilon/d,\ G_{mn}=\left(ab\varepsilon/d\right)\omega_{mn}\left(\tan\delta+\left(\sqrt{2/\omega_{mn}\mu\sigma}\right)/d\right)$$

[8]

$$N_{mni}=\varepsilon_m\varepsilon_n\cos\left(\frac{m\pi x_i}{a}\right)\sin c\left(\frac{m\pi t_{xi}}{2a}\right)\cos\left(\frac{n\pi y_i}{b}\right)\sin c\left(\frac{n\pi t_{yi}}{2b}\right),\quad \sin c(x)=\frac{\sin(x)}{(x)}.$$

L_{mn}, C_{mn}, and G_{mn} form a parallel resonator R_{mn} and the entire SPICE equivalent circuit is shown in Figure 3.4 as in Fig. 3 of [121].

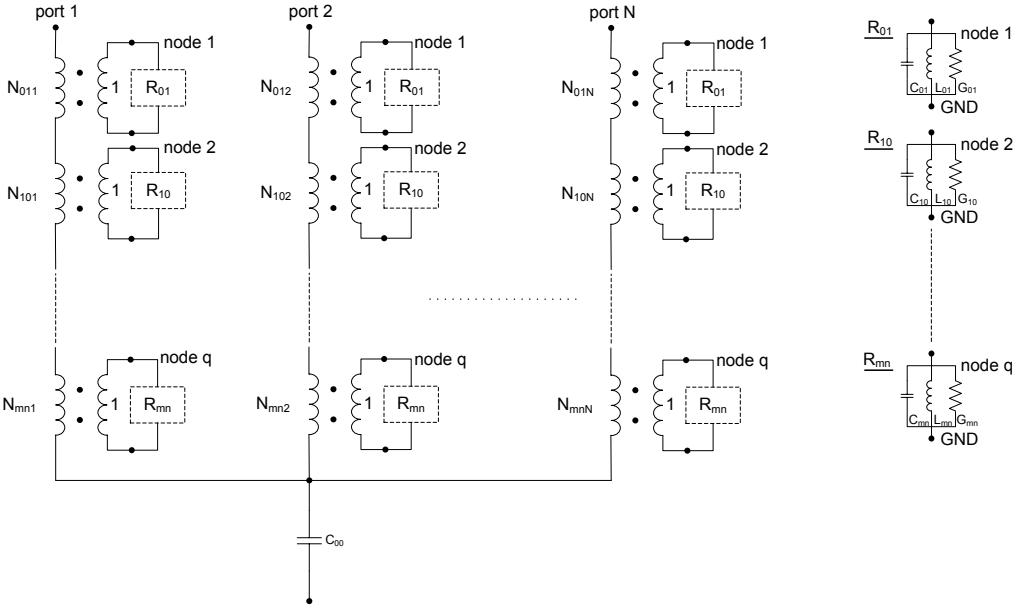


Figure 3.4: SPICE Equivalent Circuit for "N" Ports and "q" Modes.

The impedance expression results from the assumptions that a, b >> d where d << λ (wavelength) and $k'>>k''$. The dimension of the planes is a×b, and d is the height in the z direction as in Figure 3.5.

[8] In [121], the equation of L_{mn} is presented as a function of ω_{mn} ; it is a typo for the function of ω_{mn}^2 .

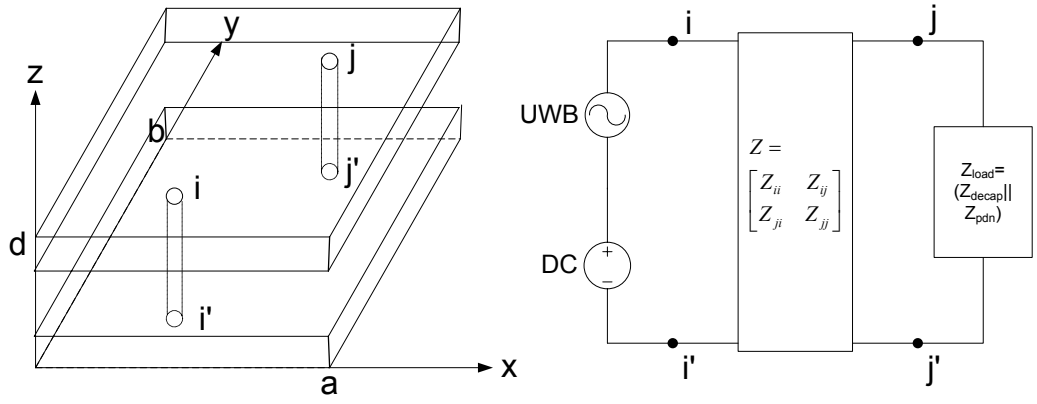


Figure 3.5: Two Port Locations at Power-Ground Planes and Their Network Model.

The $k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2$ with propagating modes of m and n. The skin depth is given as $r = 1/\sqrt{\pi f \mu \sigma}$, δ is the dielectric loss angle, and ε_m, ε_n = 1 for m, n = 0 and $\sqrt{2}$ otherwise. The (x_i, y_i) and $(x_{j,} y_j)$ are the coordinates of the port locations and the (t_{x_i}, t_{y_i}) and (t_{x_j}, t_{y_j}) are the dimensions of ports *i* and *j*. The $\omega_{mn} = 2\pi f_{mn}$, and f_{mn} is the resonant frequency of each mode. Note that the impedance characteristic is computed in the frequency domain and needs to be translated in order to obtain the time domain transient response using an inverse Fourier transform.

We consider a test structure with dimension of 10 mm × 10 mm, distance between planes of 8 mils[9], and dielectric constant of 4.3. Figure 3.5 shows the two ports *i* and *j* on the plane pair and its model with a source power supply and a load resistor in view of UWB signal transmission. For the adjacent two ports *i* and *j* at (5.04, 1000) μm and (530.82, 1000) μm, the magnitude of impedances ($|Z_{ii}|$, $|Z_{ij}|$, $|Z_{ji}|$, $|Z_{jj}|$) are obtained as shown in Figure 3.6.

[9] 1 mil is defined as 1/1000 inch = 2.54×10^{-5} m.

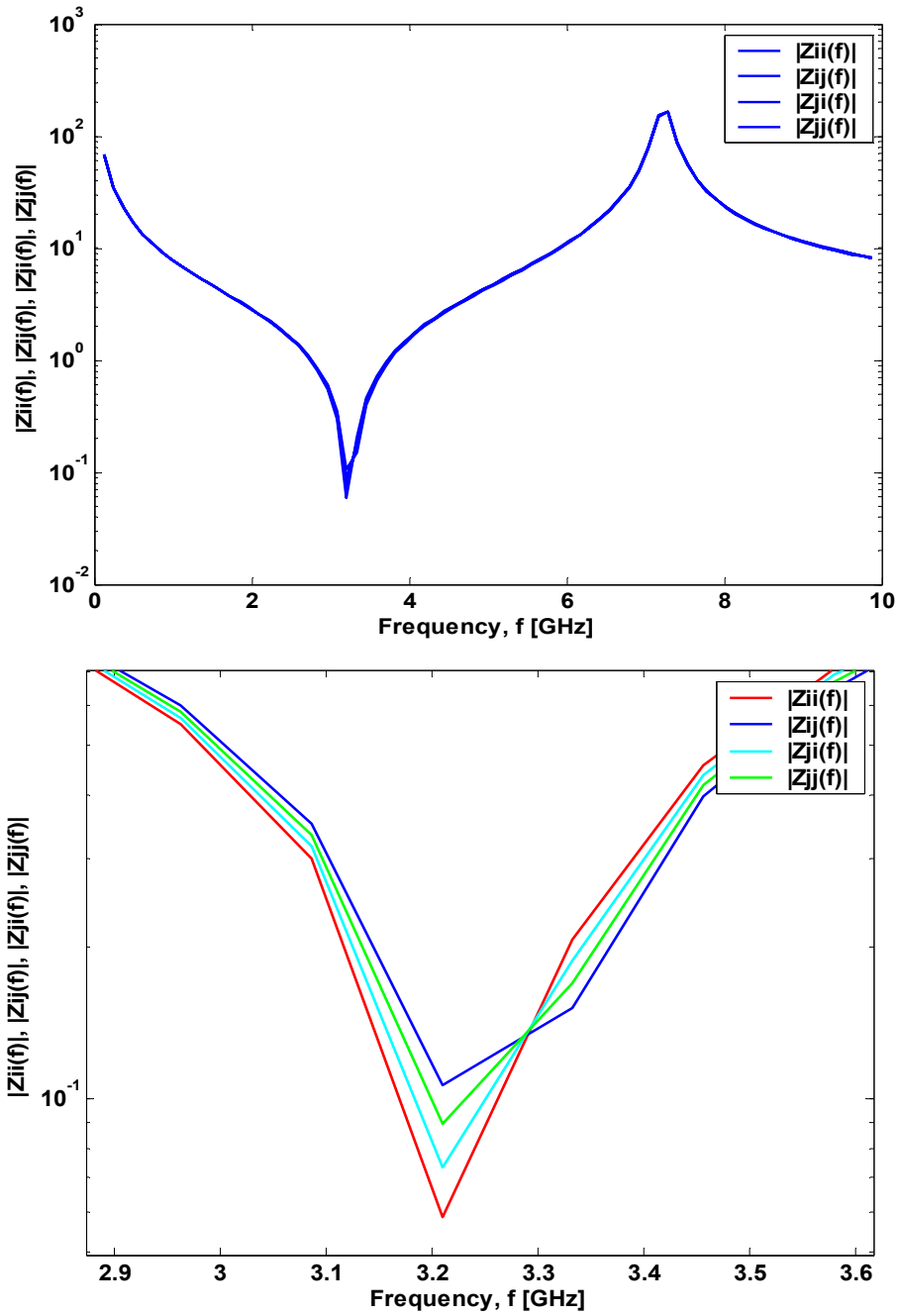


Figure 3.6: Impedance Characteristics of the Two-Port Network (**$|Z_{ii}|$, $|Z_{ij}|$, $|Z_{ji}|$, $|Z_{jj}|$**) in the Frequency Domain (Top: Overall View, Borttom: Detailed View).

As shown in the figure, the four impedances are almost the same with little difference. We adopt a decoupling capacitor whose effective series resistance (ESR), effective series inductance (ESL), and capacitance are 1.49 Ω, 300 pH, and 270 pF, respectively [122]. The impedance characteristics of the chosen decoupling capacitor (Z_{decap}) is shown with respect to frequency in Figure 3.7.

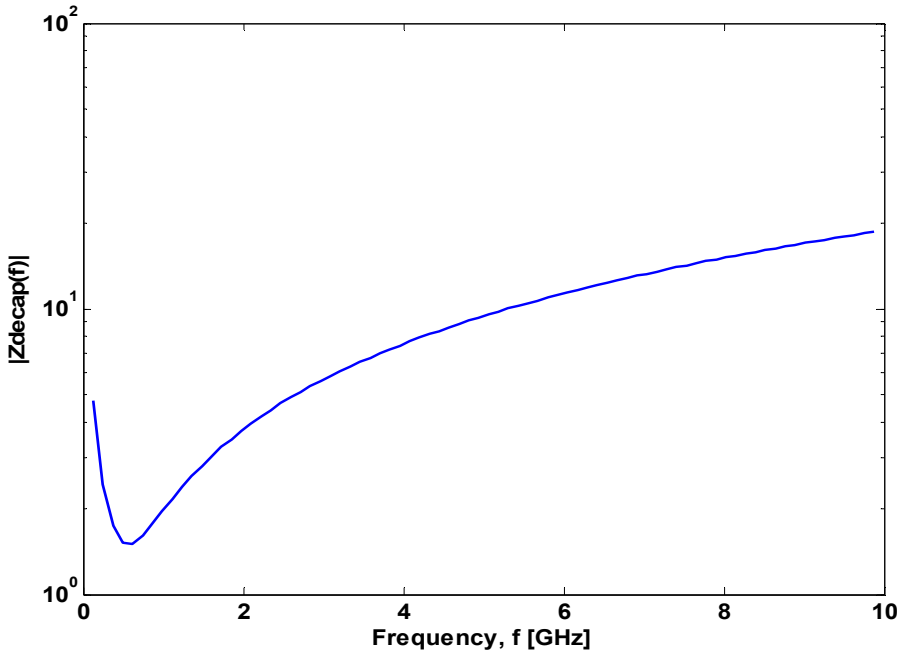


Figure 3.7: Impedance Characteristics of a Decoupling Capacitor.

In order to obtain the impedance of a PDN as seen at port *j* (or load) (Z_{pdn}), we use SPICE AC simulation sweeping from 0 to 10 GHz which is shown in Figure 3.8.

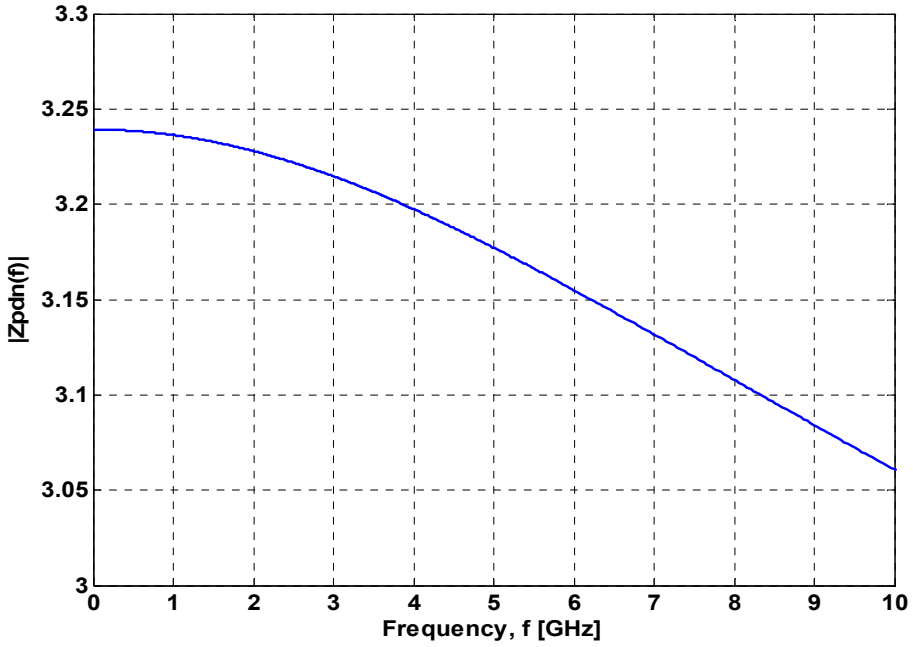


Figure 3.8: Impedance Characteristics of the Power Distribution Network.

The resultant impedance at the load is the parallel impedance ($Z_{pdn} \parallel Z_{decap}$) of Z_{pdn} and Z_{decap} as shown in Figure 3.9. The figure shows that the impedance has a notch around 0.5 GHz and increases after that point as frequency increases.

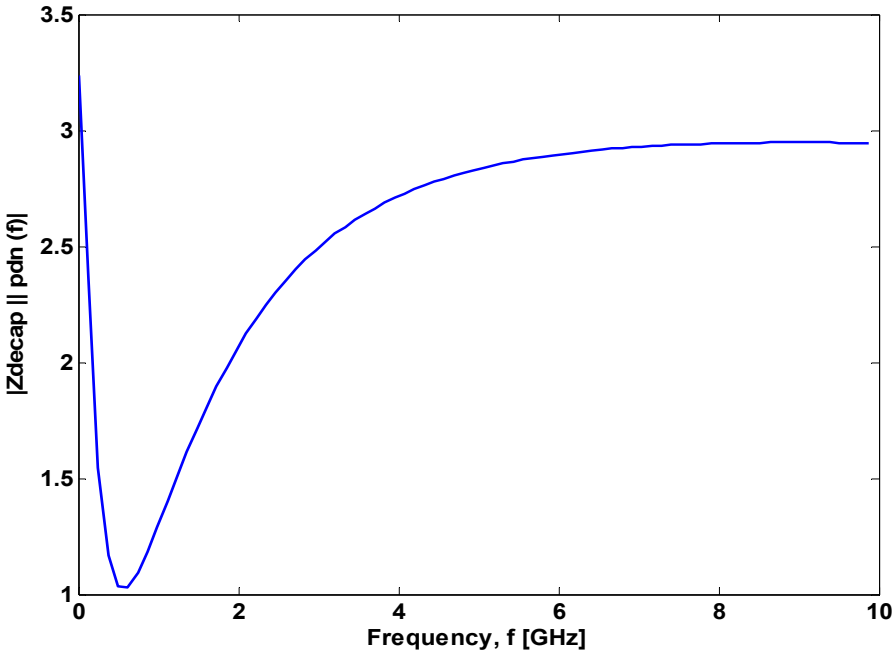


Figure 3.9: Frequency Response of the Impedance of the Parallel Loads ($Z_{pdn}||Z_{decap}$).

The transfer function for the two port network model is shown in Figure 3.10. It indicates that the two ports at the power-ground planes can transfer signals with little loss of energy within a certain range of frequency. The transfer characteristics of 0-2, 8-10, and 3.5-6.5 GHz ranges show that the three bands are useful for data transmission in view of the flat frequency response with the gain close to unity.

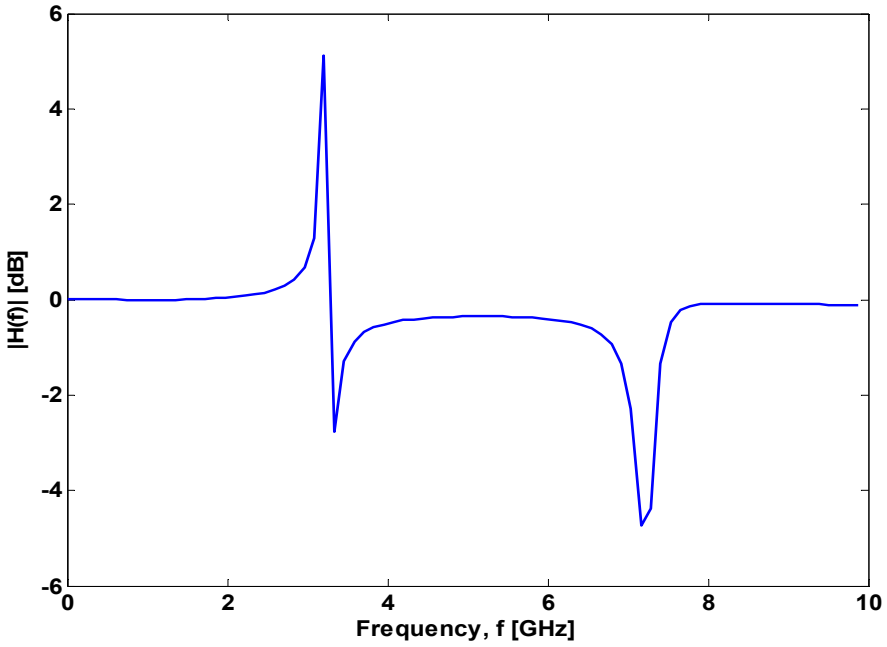
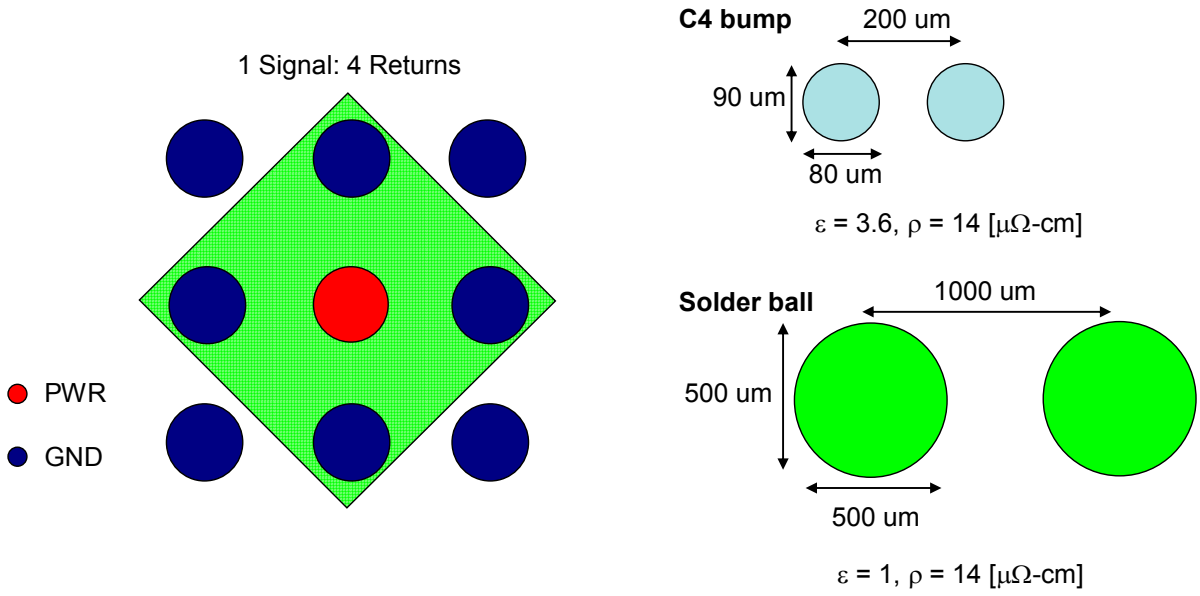


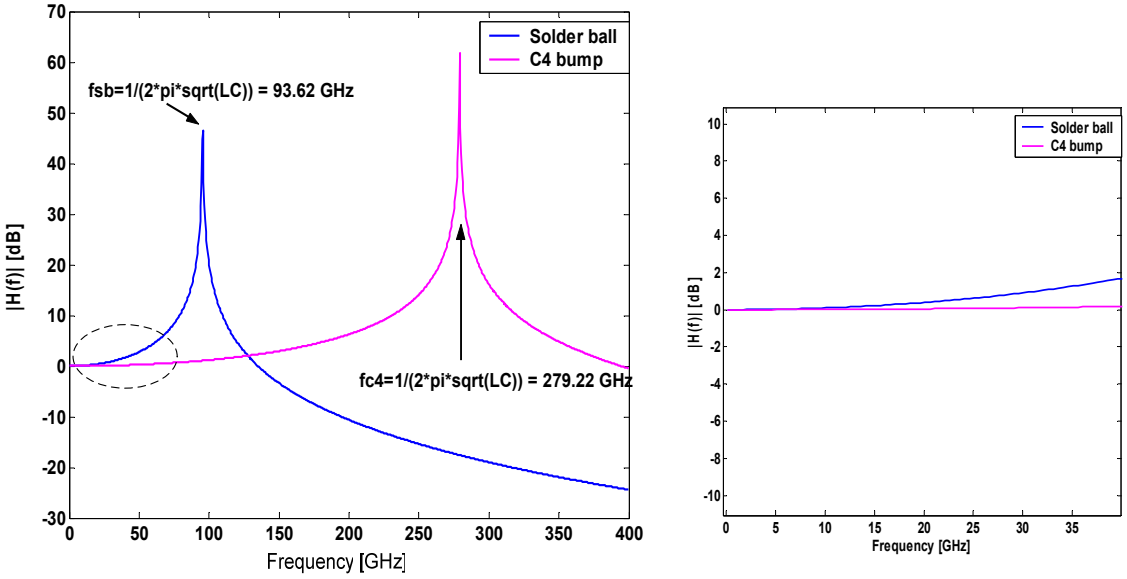
Figure 3.10: Frequency Response of the Two-Port Network.

3.3 Solder Ball and C4 Bump: Generic Model

Solder ball (IC package to PCB) and C4 bump parasitics are estimated using the Ansoft Maxwell two dimensional field solvers. Resistance values are computed based on the formula of $\rho\frac{l}{S}$ (where ρ: resistivity, l: length, S: cross-sectional area). The basic geometry is shown in Figure 3.11. A four-return-path configuration can be the most relevant benchmark values for typical designs since four nearest neighbors effectively shield the next set of neighbors [123]. We obtained the values of {0.45 mΩ, 102 pH, 27.3 fF} and {3.1 mΩ, 28.8 pH, 11.3 fF} as RLC parasitics for the solder balls and C4 bump, respectively. Their dimensions and parameters are as shown in Figure 3.11.



(a) Illustration of four return paths per signal, (b) Dimensions of C4 bump and solder ball



(c) Frequency responses of C4 bump and solder ball, (d) Detailed view (0 – 40 GHz)

Figure 3.11: Geometry and Characterization of Solder Ball and C4 Bump.

Based on these RLC values, we can construct an RLC circuit (series R-L and shunt C connection). The filter characteristics on the shunt capacitor C are represented by the transfer function H(s)

$$H(s) = \frac{\frac{1}{sC}}{R + sL + \frac{1}{sC}} = \frac{1}{1 + sRC + s^2 LC}$$

$$H(j\omega) = \frac{1}{(1 - \omega^2 LC) + j\omega RC}$$

Then, the magnitude of filter response will be

$$|H(\omega)| = \frac{1}{\sqrt{(1 - \omega^2 LC)^2 + (\omega RC)^2}}$$

Taking the logarithm and derivative on both sides, we can obtain the resonance frequency of ω_0 as follows:

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{R^2}{2L^2}}$$

If $\frac{1}{LC} >> \frac{R^2}{2L^2}$, the resonant frequency of ω_0 will be

$\omega_0 \cong \sqrt{\frac{1}{LC}}$.

At this resonant frequency, the magnitude of frequency response will be

$$|H(\omega_0)| = \frac{1}{R}\sqrt{\frac{L}{C}}$$

Figure 3.11 (c) and (d) show that solder ball and C4 bump will have resonance at a frequency far higher than that of our interest (on order of several GHz). According to the exact computation, the frequency response indicates that we can ignore the potential impacts of the solder balls and C4 bump for the chosen dimensions and the frequency due to the 0 dB magnitude of frequency response. The dimensions used in this analysis are from generic and widely accepted representative solder balls and C4 bumps.

3.4 Models of Power Distribution Networks

In order to investigate the characteristics of signal propagation, we need to see the environment that signals pass through – that is the channel. Since the channel in an integrated circuit, including the on-chip power grid, is determined by specific parameters, we have to obtain realistic parameters for our models. The parameters include the parasitics (R, L, C) of a package, the power consumption, the number of power pins, the voltage drop due to the on-chip resistive IR drop, and the inductive loss based on the operating frequency and the chip dimension. The most general and simplest model for power distribution networks, including on-chip power grids, is a second order system model.

3.4.1 Generic 2nd Order Lumped RLC Model

A generic model for the impedance characteristics of a power distribution network (or a current consumption model at the power loads) can be represented by a second order system model. As shown in Figure 3.12, the model consists of the lumped elements of a resistor and an inductor in series for the loss of metal wires and a shunt capacitor for modeling the charges stored in devices.

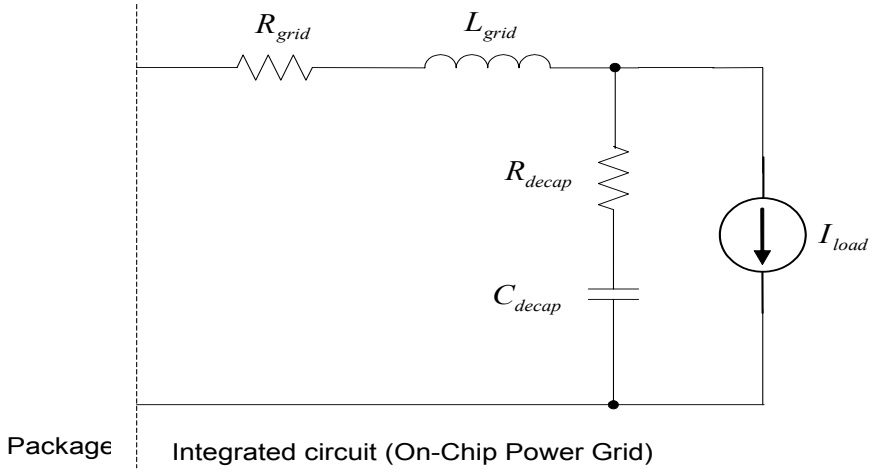
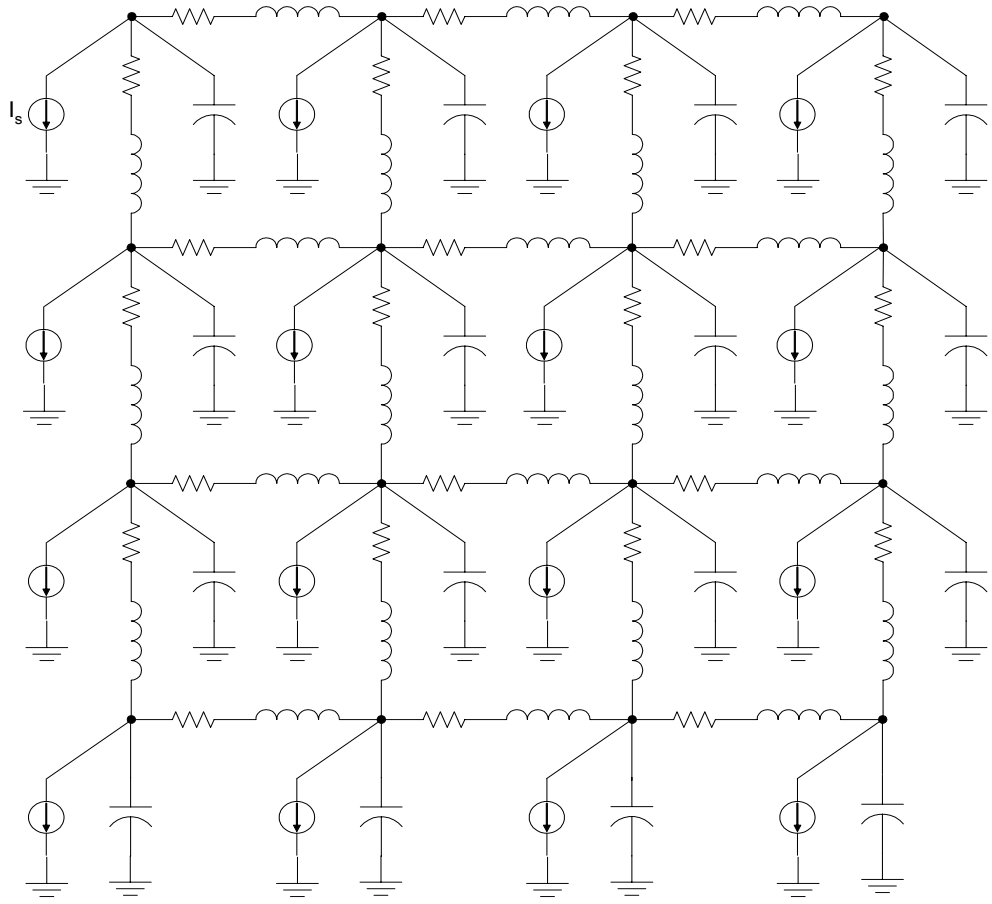


Figure 3.12: A Second Order Model for a Power Distribution Network.

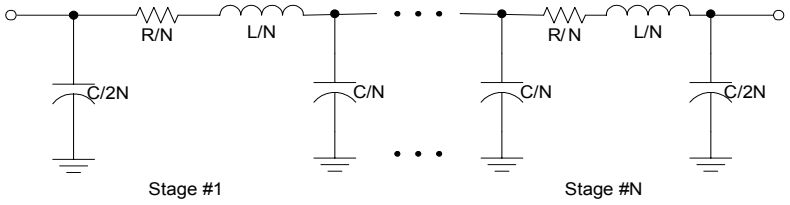
3.4.2 Distributed Π-Type RLC Model

The lumped second order model does not give insight for estimating the desired characteristics of delay and attenuation at several locations on a metal wire, as discussed in

Section 2.3.3.2. A simple distributed RLC model is appropriate for the investigation of pulse propagation through an on-chip metal wire. First, we consider a π-type distributed RC model for a metal wire based on the observation in [46]. Then, a π-type distributed RC model is incorporated into a distributed RLC model, which forms power mesh grids. The parasitics of R, L, and C are explained in 2.2.2. This RLC model can be referred to in [124]. In the RLC model, the die area is divided into a grid of M×N cells. The power and ground distribution networks within each cell are reduced to a simplified macromodel. These macromodels form an RLC grid model of an on-chip power distribution network, as shown in Figure 3.13(a). A row or column in the figure is considered as a π-type distributed RLC model for an on-chip wire as shown in Figure 3.13(b).



(a) (3X3) Π-Type Distributed RLC Power Mesh Grid



(b) N-stage Π-Type Distributed RLC Model

Figure 3.13: A Distributed RLC Model of an On-Chip Power Distribution Network.

3.5 Decoupling Capacitors

As the number of transistors increases along with operating frequency, the noise becomes a more significant issue for signal/power integrity in high performance VLSI systems. For alleviating this noise whatever it is from (or for achieving lower impedance power distribution system), decoupling capacitors have been used. For overall power

distribution system to maintain a certain power integrity with a low target impedance over a wide bandwidth of interest, multistage decoupling is a reasonable approach. Multistage decoupling adds decoupling capacitors at various abstractions of components – voltage regulator module on a PCB, power/ground pin pairs of ICs, and power/ground nodes in an IC. In this thesis, we focus on the environment of high speed integrated circuits. The original intention of using decoupling capacitors is not changed for the proposed data communications.

Different from ideal capacitors, an actual capacitor is typically decomposed into an equivalent circuit of three components in series – an ESR (Equivalent Series Resistor), an ESL (Equivalent Series Inductor), and C (Capacitor) as shown in Figure 3.14. With simple mathematics in the Laplace domain, we can obtain the impedance characteristics of a decoupling capacitor in the frequency domain. Simply, there is a resonance at $f_0 = \frac{1}{2\pi\sqrt{L \cdot C}}$ and infinite impedance at DC (f = 0 Hz) and at infinite frequency. An exemplary frequency response of a decoupling capacitor is shown in Figure 3.7.

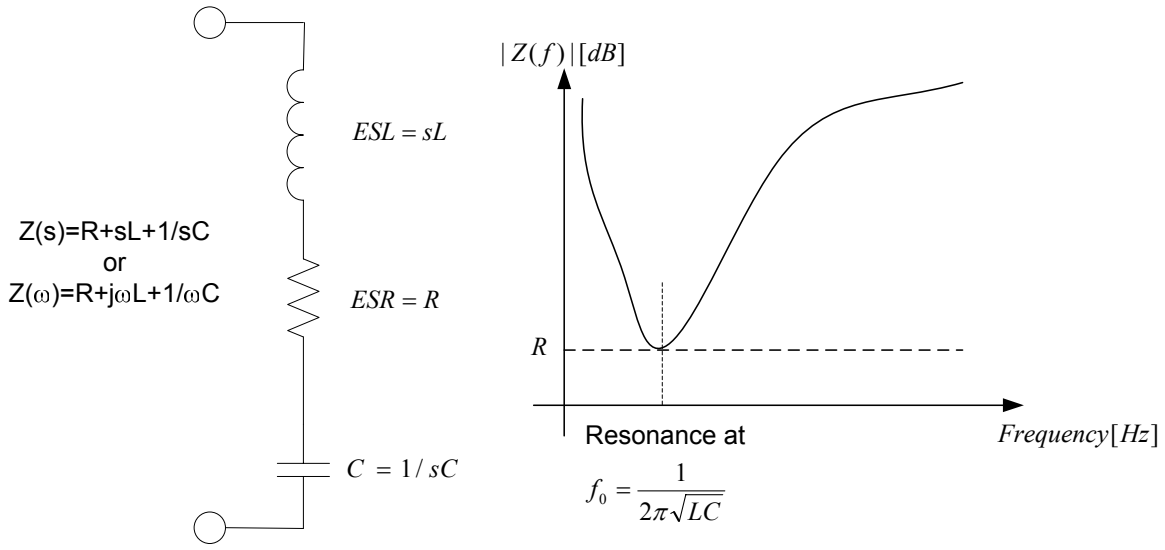


Figure 3.14: Equivalent Circuit of a Decoupling Circuit and its Response.

There are two characteristics that function in the resonance of a capacitor. First, there is a series resonance where its impedance is minimum at the ESR. This is desired since it

provides a low impedance path from the power plane to the reference plane at the resonant frequency. The second characteristics is a parallel resonance which results from the interaction between capacitors in an anti-resonance form which shows itself as high impedance. As the ESR of a capacitor decreases, the magnitude of this anti-resonance will increase. The design goal should be the reduction of impedance for frequency band of interest while minimizing the effect of anti-resonance responses. The design of broadband, low impedance characteristics in high performance VLSI systems has been widely accepted and proved with great success in industry [142]. In this thesis, the series decoupling capacitors are considered.

3.6 Summary

In this chapter, we investigate a microscopic channel model for the power distribution networks starting from the overall methodology for modeling and simulation. The chapter also discusses planar structure IC package models, solder ball and C4 bump models for flip chip IC packages, and accurate models for the power distribution networks. The chapter ends with the considerations for decoupling capacitors.

In Section 3.1, we present modeling philosophy of accuracy with efficiency in simulation speed. As our simulation method, we used the impedance matrix method for finding a transient response for the UWB signals overlaid on the DC power supply voltage. Since the overall computation is done in frequency domain, we need to convert the frequency domain response into time domain using an inverse fast Fourier transformation. We also presented the methodology in a flow chart for visualization of the modeling and simulation using PERL, SPICE, and MATLAB.

In Section 3.2, we investigate a computationally efficient modeling method for a realistic planar structure model – cavity resonator model (CRM) and obtained a frequency response for an exemplary two-port network.

Section 3.3 provides an investigation of the generic models for solder ball (between PCB and IC) and C4 bump (between die or chip and substrate in an IC package for a flipchip connection). The investigation shows insight to the possibility of approximating

the two components in power distribution networks based on the frequency response and the frequency band of interest.

Section 3.4 investigates the power distribution networks for finding an appropriate model, which will be a π-type distributed RLC network. The number of stages in this RLC network will be chosen based on the physical parameters, and accuracy will be achieved with at least 13 stages [46].

Section 3.5 presents the model for a decoupling capacitor and its equivalent circuit and analyzes the impacts of the ESR, ESL, and C with the frequency response of the impedance. In brief, the series capacitance resonance will provide the lowest impedance (equivalent to ESR) at $f_0 = \frac{1}{2\pi\sqrt{L \cdot C}}$.

Chapter 4

Transmission and Recovery of I-UWB Pulses in a Power Distribution Network

4.1 Overview

We proposed the dual use of power lines for data communications in a system-on-chip environment in [16]. As the number of required pins increases with the number of devices on a chip, the cost for the pins increases as well. The bottom line of this thesis is to utilize the existing resources[10] on chips and/or on boards – power lines (or power buses) in power distribution networks – for data communications purposes; and at the same time we can achieve multiple data transmissions and/or reduced pin count with moderate hardware complexity.

Figure 1.2 in Chapter 1 shows the overview of the proposed on-chip/on-board power line communications. The proposed data communications can be applied for either 1) one-way communications such as a massive parallel scan design [17] or 2) two-way communications such as inter-/intra- chip data communications [16]. The reference for the distinction between one-way and two-way communications is determined by the hardware resources supporting the architecture. One-way communications can be constructed with an I-UWB transmitter as a source node and several receivers, which receive I-UWB pulses via power pins and transmit via normal output pins for signals. One promising application is a new approach for massive parallel scan design. Two-way communications is a generalized version of our proposed data communications. It uses power lines for both transmission and reception of signals. Thus, the I-UWB transmitter and the simple data recovery unit (which

[10] This essentially conforms to the idea of "No new wires" for the power line communications in the literature.

consists of a one bit comparator and a digital accumulator) are necessary on a chip for two-way communications.

The methodology for the proposed data communications is investigated in three categories similar to those in the communications area. The first category is the signal transmission for incorporating one or two-way communications between chips in high speed integrated circuits, which will be discussed in Section 4.2. Section 4.3 discusses the second category of data recovery. Signal propagation in a power distribution network is covered in Chapter 3. Section 4.4 provides simulation results for exemplary parameters from a generic high speed integrated circuit. Section 4.5 summarizes this chapter.

4.2 Transmission

The transmission of an I-UWB signal for the proposed data communications is possible using either a generic I-UWB transmitter (suggested for two-way communications) or digital modulator (suggested for one-way communications) as indicated in Section 1.3.1. The basic principle is the same as that for I-UWB transmission in the literature [16], [17]. I-UWB pulses will be overlaid with the power supply voltage, and they can be spread following direct sequence-code division multiple access (DS-CDMA). Since we consider I-UWB signaling with DS-CDMA, the specific signaling can be called as DS-UWB as explained in Section 2.6. If we have four channels, each channel will transmit its unique orthogonal code sequence using I-UWB pulses as chips. The orthogonality can be achieved using the OVSF (Orthogonal Variable Spreading Factor) coding method, which provides high auto-correlation for each codeword (co-channel) and low cross-correlation for adjacent channels (codewords). Figure 4.1 (a) shows the derivation of four OVSF codewords, and Figure 4.1 (b) shows DS-UWB pulse sequences that follow the four codewords overlaid on a power line. For the recovery of transmitted I-UWB pulses using the DS-UWB modulation scheme, the de-spreading operation is necessary and will be discussed in Section 4.3.

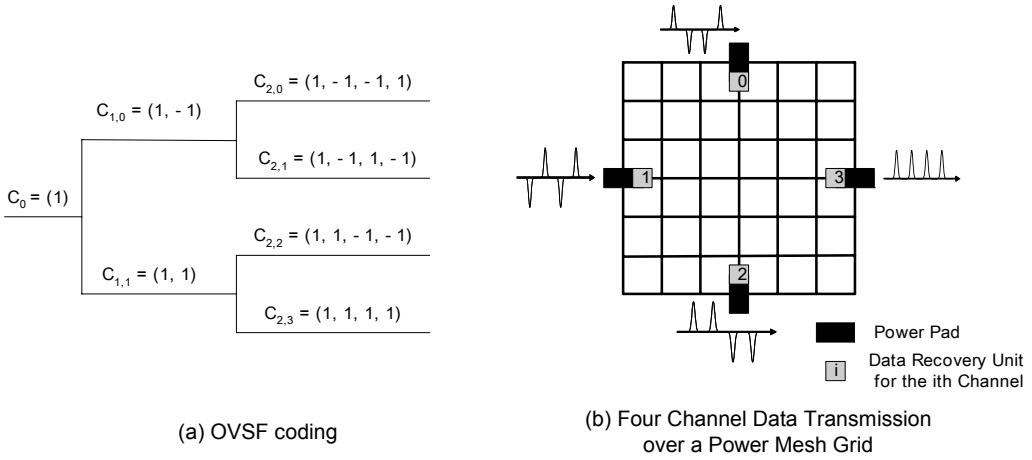


Figure 4.1: OVSF coding and Exemplary Four Channel Data Transmission.

4.3 Data Recovery

The most important part in communications is the receiver, so we characterize its performance for our transmission scheme and channel. The overall performance in a communication channel is determined by the receiver architecture as well as the transmission scheme and channel conditions. Since we presented an RLC distributed mesh grid as the channel in Chapter 3 and the transmission scheme in Section 4.2, this section discusses the data recovery scheme and its corresponding hardware architecture. We emphasize a low-power/low-area architecture for the proposed data communications. With simple data recovery units, which consist of a one-bit comparator for hard decision, a counter, and a decision unit, data recovery will be possible based on the literature survey.

4.3.1 Demodulation: Correlation/Matched Filtering vs. Others

It is convenient to subdivide the receiver into two parts – the signal demodulator and the detector in series. The function of the signal demodulator is to convert the received waveform $r(t)$ into an N-dimensional vector $\mathbf{r} = [r_1, r_2, \ldots, r_N]$, where N is the dimension of the transmitted signal waveforms. The function of the detector is to decode which of the M possible signal waveforms was transmitted based of the vector $\mathbf{r}$ [125]. Two realizations of the signal demodulators in an additive white Gaussian noise (AWGN) channel are based on the use of signal correlators and matched filters.

Correlation-based demodulators consist of N branches of correlators and samplers. Each correlator consists of a mixer (frequency down converter in case of narrowband signals) and an integrator (a low pass filter) for recovering the corresponding basis waveform in the received waveform contaminated by AWGN.

A matched filter operates similarly to a correlator-based demodulator, but it uses a bank of N filters instead of a bank of N correlators. A filter whose impulse response $h(t) = s(T-t)$, where $s(t)$ is assumed to be confined to the time interval $0 \le t \le T$, is called the matched filter to the signal $s(t)$. A matched filter has the interesting properties of 1) maximization of the signal-to-noise ratio (SNR), and 2) the dependence of the output SNR on the energy of the waveform $s(t)$ but not on the detailed characteristics of $s(t)$.

In fact, correlation or match filtering operations increase the SNR of the recovered data over use of comparators [125]. However, a correlator or a matched filter increases the hardware complexity as well as power consumption significantly. Also, analog correlators surrounded by digital blocks are sensitive to noise from digital circuits. Digital correlators and matched filters need a faster clock (by at least few times) than the system clock, which may be a problem for a high speed operation. Our SPICE simulation indicates that the proposed comparator approach with three times over-sampling for even severely aggravated signals has not experienced any error for 1000 data symbols, so it may be good enough for practical purposes. Note that correlators and matched filters can be readily incorporated into the proposed design at the cost described above.

4.3.2 Architecture

The receiver architecture for the proposed data communications focuses on low power design with a minimal area. Our design goal for the data recovery unit is to make it simple but efficient in view of accuracy and power consumption. As discussed in Section 2.6.3.2 and Figure 2.13, the receiver consists of a one-bit comparator to recover the chip value; a counter for counting the number of differences/agreements between the received chip and the reference chip in a codeword; and a decision unit for the finally recovered information bit. The spreading operation makes multiple channel data transmission

possible, but without the spreading operation, the receiver reduces to a one-bit comparator. That is, one channel can be implemented with the least area overhead.

Figure 4.2 shows the data recovery scheme of the proposed receiver architecture which is discussed in Section 2.6.3.2. Recall Figure 2.13 for the hardware architecture for the proposed research. Figure 2.13 (a) displays the overall circuit diagram; and Figure 2.13 (b) displays a representative one-bit comparator for a hard decision. The data recovery unit receives the decided chip (r_i) from the one-bit comparator, compares it with the reference chip in a codeword (c_i), adds the number of difference/agreements, and then decides the final bit value in a clock period (or a pulse repetition interval (PRI) for an I-UWB signal). The one-bit comparator can be implemented using two cascaded, capacitively coupled, auto-zeroed inverters followed by a dynamic register[11] [22], [108].

If we have 4-bit chip sequence of (1, 1, -1, 1) as a reference codeword for bit 1 and the demodulated codeword (from the one-bit comparator) of (1, 1, -1, 1) in a noise free environment, the output of the exclusive-OR gate would be (0, 0, 0, 0) and the output of the counter would be *zero*. For the same reference codeword and the demodulated codeword of (-1, -1, 1, -1), the output of the exclusive-OR gate and the output of the counter will be *four*. The output value *zero* (*four*) of the counter would be detected as information bit of 1 (0) as illustrated as in Figure 4.2. As we will see in Section 4.3.4, the benefit of spreading gain can be observed via this increased decision region.

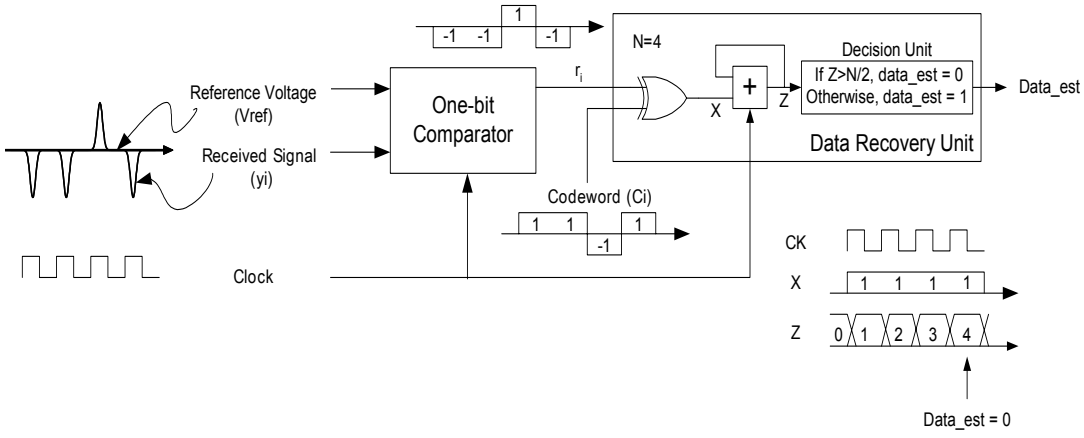


Figure 4.2: Proposed Data Recovery Scheme.

[11] It can be considered as a D-type latch consisting of two back-to-back tri-state inverters.

4.3.3 Over-Sampling

The time instant for sampling is crucial for the accuracy of data recovery. We assumed a precisely controlled system clock. With the clock, we can estimate the delay between the peak of the input I-UWB pulse and that of the pad output inside a chip by transmitting a train of I-UWB pulses with known PRI. Even though we know an accurate delay estimate for the peak of the I-UWB pulse at the input of the data recovery units, one sample per PRI is not enough due to the sensitivity of a power distribution network to the thermal noise assumed in our initial research. The bit error rate for one-time sampling was about 10^{-1} for the 1000 data bits transmission. Thus, we increased the sampling rate to three samples per PRI. With this increased number of samples, our SPICE simulation indicates that the proposed comparator approach with three times over-sampling has not experienced any error for 1000 data bits, so it may be good enough for practical purposes. The time for over-sampling was set to 100 ps before/after the estimated time for the peak of an input of a data recovery unit.

4.3.4 Spreading Factors

The DS-CDMA technique assigns a codeword to each bit of information, and the bit is spread over the codeword. Orthogonal codewords are assigned to different users. We describe the spreading operation and benefits of the DS-CDMA technique in more detail. The spreading operation represents one bit of data as a series of binary (positive and negative) pulses spread over a codeword. For example, a codeword of (1, 1, -1, -1) represents a data bit 1 and the opposite, (-1, -1, 1, 1), a data bit 0. To send one bit of information, we have to send four pulses, which either reduces the data rate or increases the pulse repetition frequency. The benefit of the spreading operation is the processing gain, which is *10*log10* (*spreading_factor*) in dB added to the link budget. For the example 4-bit codeword, the spreading factor is 4, which yields a processing gain of 6 dB. This implies that the signal power of the pulses can be reduced by 6 dB, while maintaining the same signal-to-noise ratio. Thus, DS-CDMA further reduces the impact of UWB pulses on power line fluctuations, and the de-spreading operation permits better recovery of the signal.

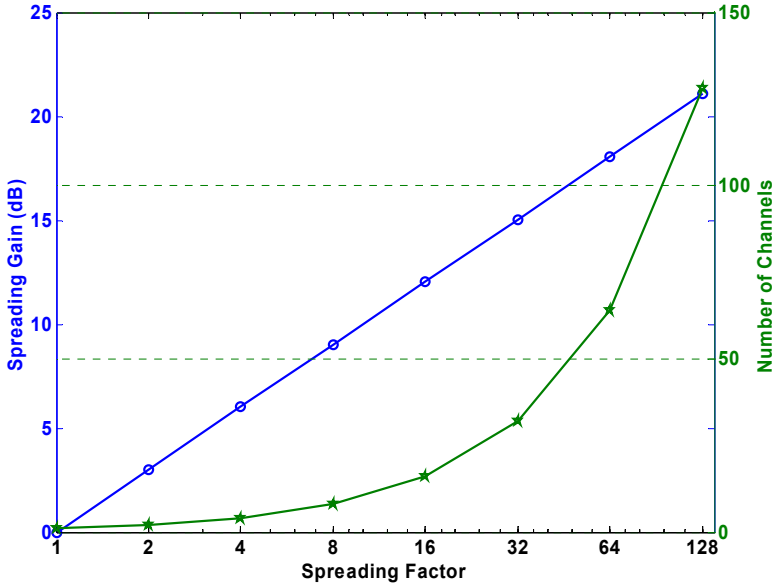


Figure 4.3: Computed Gain and Number of Channels versus Spreading Factors.

However, the data rate decreases as the spreading factor increases. Figure 4.3 shows the need for deciding an appropriate spreading factor for specific applications. In certain applications, an adaptive spreading factor may be feasible for enhanced quality of service.

The spreading factors vary from 1 to 128 by a step of a power of 2 and the number of channels follows the spreading factor. As the spreading factor increases, the number of channels (with the same data rate) increases, as shown in the green waveform with the y-axis at the right-hand side of the figure. In addition, the spreading gain increases with the spreading factor, as shown in the y-axis at the left-hand side of the figure, and thus better quality of service (signal integrity such as BER) is guaranteed. For a CDMA environment like cellular communications, a large number of channels can maintain the same aggregate data rate, and this is a distinctive benefit of the CDMA.

4.4 Simulation

In this section, we set up a simulation framework which consists of a planar structure IC package model and a power distribution network model in MATLAB and SPICE, respectively. We will present the design parameters for the package and PDN,

voltage drop design, and simulation results with observations in this section. We use PERL for generating the π-type distributed RLC circuits which is used as an input for SPICE.

4.4.1 Design Parameters

We select the design parameters of chip dimension, number of power pins (or balls), package selection, and the pad cell for power supply for constructing a generic integrated circuit whose specification is comparable to high performance processor. Our power distribution networks are modeled for a generic IC based on a PowerPC750 processor in a BGA (Ball Grid Array) package and also on a Pentium III processor in a FCPGA (Flip Chip Pin Grid Array) package.

Package model parameters:

- Package dimension: 20 mm × 20 mm
- Number of balls: 400
- Number of power balls: 100
- Number of ground balls: 100
- Number of signal balls: 200

PDN model parameters:

- Chip dimension: 10 mm × 10 mm (More accurately, 9999.96 μm × 9999.96 μm)
- Number of power cross points: 400 (20 and 20 wires in M4 and M5, respectively)
- Metals for power bus: M4 and M5
- Sheet resistance for M5: R = 0.04 Ω/□
- Sheet resistance for M4: R = 0.07 Ω/□
- Via resistance (R_{via}) for the interconnection between M4 and M5 = 8.68 Ω

We use the necessary parameters from the TSMC 0.25 μm deep submicron process. The resistances for metal wires are calculated using the sheet resistance model [19], and the inductance is computed based on the formula (2.3). The capacitive parasitics of metal wires are extracted from their layouts using the NCSU design kit.

4.4.2 Voltage Drop Consideration

The dynamic power consumption of the processor (a PowerPC750 processor) is 7.3 W @ 300 MHz with a supply voltage of 2.5V. The current source I_s at each cross point sinks 7.3 mA to result in the total power consumption of 7.3 W. The maximum resistive IR drop is set to 10 percent of the power supply voltage, which is 0.25 V at the center point of the series connection of R and L in a grid. The 10 percent is provided as a guide for IR drop in a power distribution network design in the literature [126]. Efficient power/ground network design and analysis were investigated in [127], [128]. We computed the width of a power line w to achieve the maximum allowable IR drop based on the iterative procedures in a flow chart as shown in Figure 4.4.

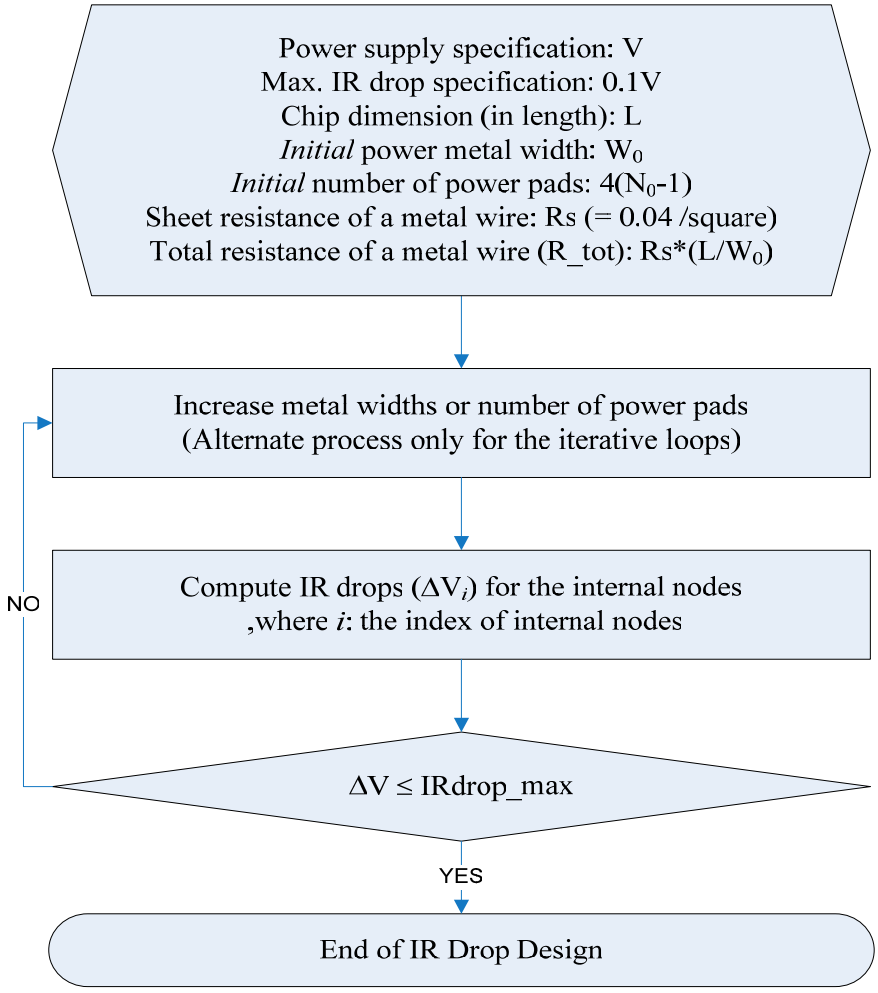


Figure 4.4: A Flow Chart for IR Drop Design.

Another reason for voltage drop is the inductive loss resulting from the simultaneous switching noise (SSN) of current consuming devices. Since the voltage drop due to this inductive loss results from either the inductance of wires or the SSN of internal devices, any method for reducing either of the two factors would work. There is a good reference which provides insight on the challenges in power-ground integrity [129].

The inductance of a flip-chip array IO package is much less than that of a wire-bonded package due to its structural distance as shown in Figure 2.5. The inductance of an on-chip metal wire is computed using (2.3) in Section 2.2.2.2. The di/dt measure of an IC is derived as $di/dt \cong P \cdot f_c / V_{dd}$ in [129] and in our case it is 1 A/ns at each cross point. The internal circuits are typically modeled as current sources from power supply to ground [124]. For a typical CMOS chip, these currents are shaped as a saw tooth waveform and different circuit families have different current signatures [130]. Another approach for modeling the SSN more realistically using modeling parameters from three PowerPC processors is found in [131]. We model the di/dt with the rising slope of 1 A/ns for 100 ps followed by a symmetrical falling slope to each current source at every node in a power distribution network.

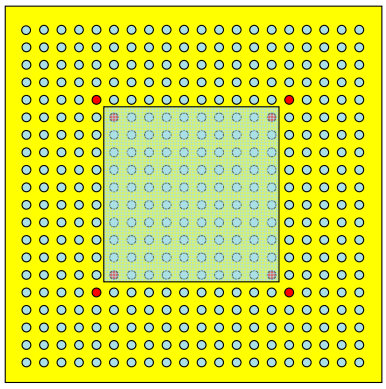
The signal-to-noise ratio (SNR) is considered from the ratio of average current (I_{avg}) to absolute magnitude of current fluctuation ($I_{thermal}$) in percent as suggested as 5 % of the average current [132]. Since the infinite bandwidth of noise was assumed, it is generated using a normal distribution of zero mean and a variance which is equal to the energy of the current noise ($I_{thermal}^2$). The current noise at the SNR of 5 % variation is modeled in our case study using MATLAB and then incorporated into the SPICE simulation.

4.4.3 Simulation

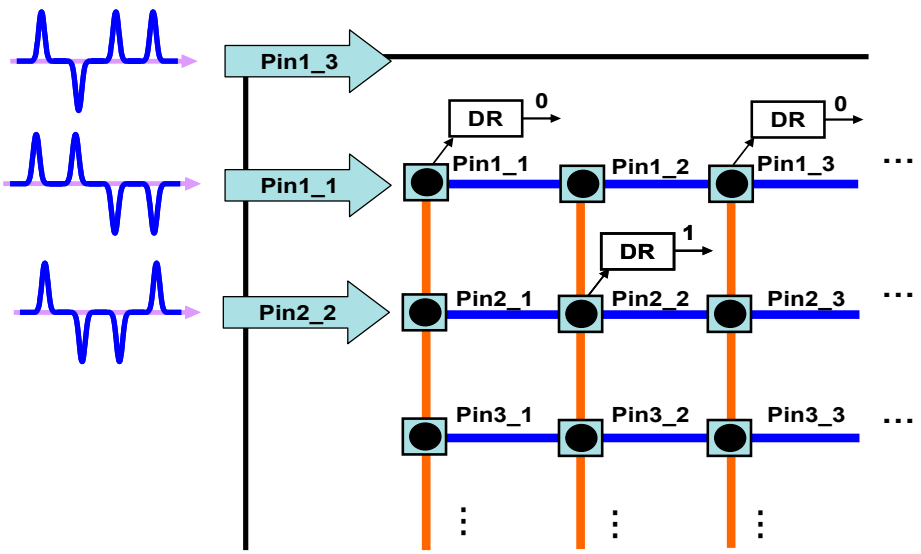
Gaussian UWB pulses with peak amplitude of 0.125 V, (*i.e.*, 5 percent of the supply voltage), a width of 1 ns, and PRI of 1 ns were considered for our simulation. The maximum chipping rate (*i.e.*, the raw pulse rate) for the Gaussian pulses is 1 GHz. Two noise sources, simultaneous switching noise (SSN) and thermal noise, are the most important issues for power distribution networks. We added SSN with the rising slope of 1

A/ns for 100 ps followed by a symmetrical falling slope to each current source, and the repetition frequency of the SSN is 1 GHz. The output waveform may have a notch at the occurrence of the SSN depending on the amount of SSN. So the output waveform should not be sampled at the vicinity of the occurrence of the SSN.

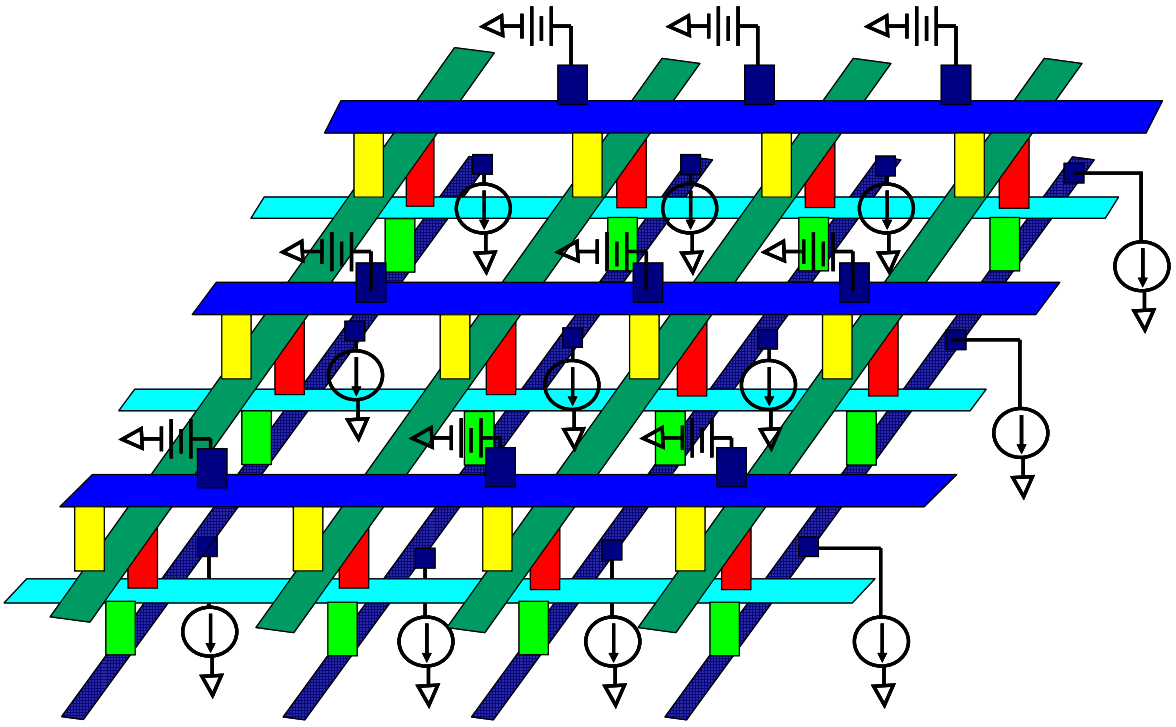
The first and most critical experiment is to examine whether I-UWB pulses propagate through power pins/balls. We applied I-UWB pulses at several locations (refer to Figure 4.5), while the rest of the power pads (C4 bumps) remain at VDD = 2.5 V. We also measured the waveforms at different locations. We considered the two top most metal layers of the TSMC 0.25 μm process. For single channel data transmission in a flip-chip type IC package environment, area overhead for the data recovery block will be drastically reduced with its flexible locations.



(a) Transmitters and Receiver Locations for Four Channels in an IC Package (outer square) and Chip (inner square) boundary (Bottom View of an IC Package).



(b) Top View (Corner of an IC die; Signal pads are omitted for brevity)



(c) Multilayer Power Grid

Figure 4.5: Overview of the Channel Environment in an Array IO Package.

Based on the impedance matrix method in Section 3.1.2, we obtain following equation for N-port network of which inputs has R_s and output has a load resistor R_L. I_i ($i=0, \ldots, N-1$) is the current at port i and V_i ($i=0, \ldots, N-1$) is the voltage at port i. We assume the same power supply for between all the source nodes and ground node in the following equation. However, the voltage source can be varied according to the actual power supply voltage levels.

$$\begin{bmatrix} V_0 \\ V_0 \\ . \\ V_0 \\ 0 \end{bmatrix} = \begin{bmatrix} z_{11}+R_s & z_{12} & . & . & z_{1N} \\ z_{21} & z_{22}+R_s & . & . & z_{2N} \\ . & . & . & . & . \\ . & . & . & z_{N-1,N}+R_s & . \\ z_{N1} & z_{N2} & . & . & z_{NN}+R_L \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ . \\ I_{N-1} \\ I_N \end{bmatrix} \tag{4.1}$$

(4.1) can be written as in a simpler vector notation of $V_{\text{mod}} = Z_{\text{mod}} \cdot I$. If we want to know the voltage waveform at particular port location N (or any arbitrary location r), we can input any other ports with voltage/current inputs. First, we find inverse matrix of Z_{mod}, and then we perform the multiplication of the inverse matrix of Z_{mod} by V_{mod}, and thus, the currents at all the port locations are obtained. Once the current at the port location of interest is obtained, the voltage waveform at the port location can be obtained by the relationship $V_N = -I_N \cdot R_L = -I_N \cdot \left(Z_{pdn} \| Z_{decap}\right)$, where Z_{pdn} and Z_{decap} are impedance matrices of power distribution network and decoupling capacitor of interest, respectively. V_0 may be either V_0 or V_{dc} dependent on the applications.

4.4.4 Simulation Results and Discussion

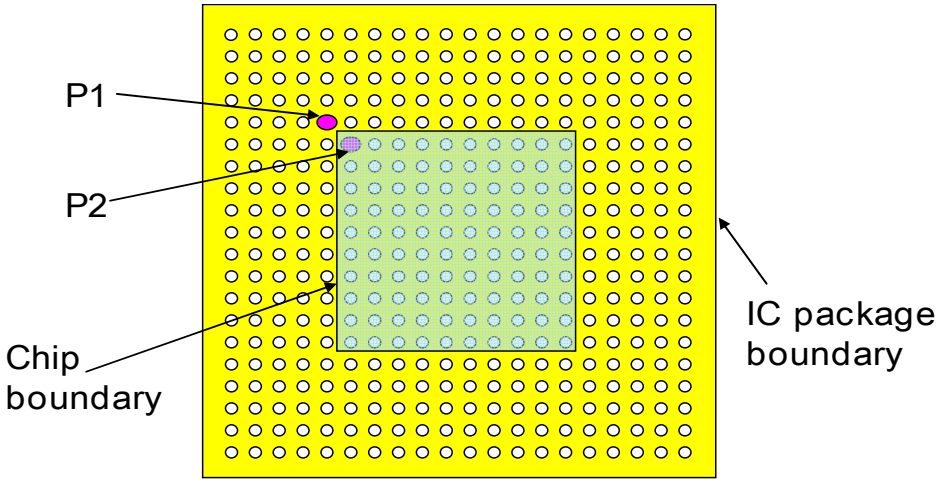
With the impedance matrix method, several representative cases of simulations are run and summarized in Table 4.1. The peak-to-peak voltages are measured in mV units at four receiver locations according to the variations of P5 location.

Table 4.1: Peak-to-Peak Voltage measured at Four Internal Nodes close to the Four Receiver Locations for Various P5 Locations. [Unit: mV].

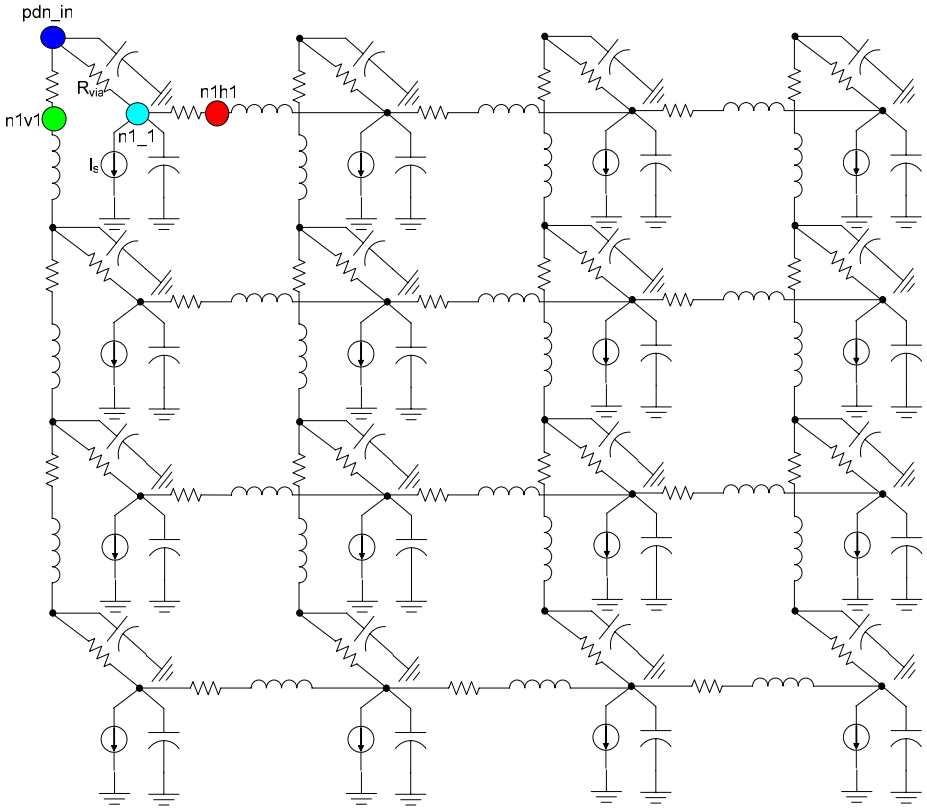
Test Set	V(pdn_in*)	V(n1v1*)	V(n1_1*)	V(n1h1*)
SET1P5	**175.0**	**175.0**	**180.2**	**180.2**
SET1P6	169.6	169.6	183.6	183.6
SET1P7	193.6	193.6	194.8	194.8
SET1P8	96.3	96.3	83.3	83.3
SET3P5	**106.0**	**106.0**	**117.3**	**117.3**
SET3P6	177.3	177.3	185.2	185.2
SET3P7	188.7	188.7	193.9	193.9
SET3P8	97.5	97.5	85.7	85.7
SET5P5	**76.8**	**76.8**	**82.9**	**86.4**
SET5P6	182.7	182.7	189.0	189.0
SET5P7	180.5	180.5	188.9	188.9
SET5P8	97.2	97.2	86.1	86.1
SET7P5	**94.8**	**188.2**	**102.2**	**201.2**
SET7P6	189.5	189.5	206.6	206.6
SET7P7	175.5	175.5	187.9	187.9
SET7P8	102.0	102.0	95.3	95.3
SET9P5	**143.3**	**177.6**	**153.7**	**183.6**
SET9P6	177.8	177.8	185.0	185.0
SET9P7	183.3	183.3	191.1	191.1
SET9P8	100.4	100.4	88.7	88.7

*Please refer to Figure 4.6 (b) for the four locations of the first row in the table.

Figure 4.6 shows the distributed two-layered Π-type RLC model for PDN.



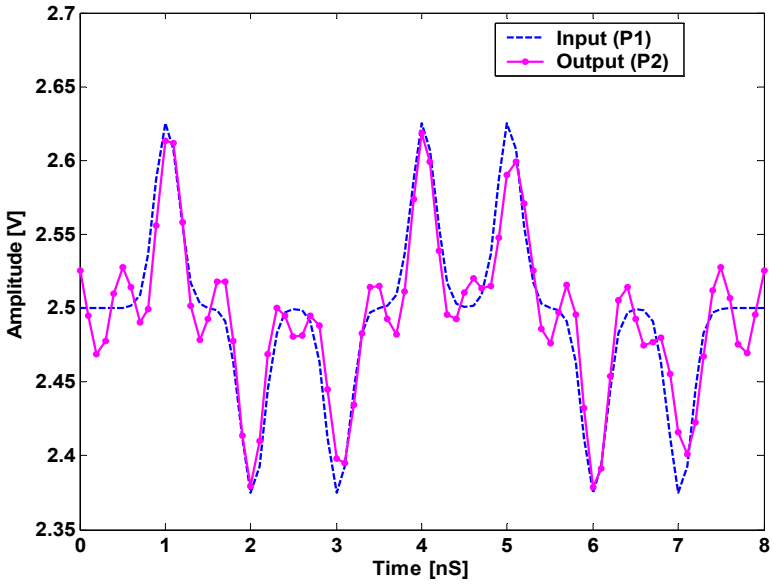
(a) Two-port locations in an IC chip on the plane in the package (Bottom View)



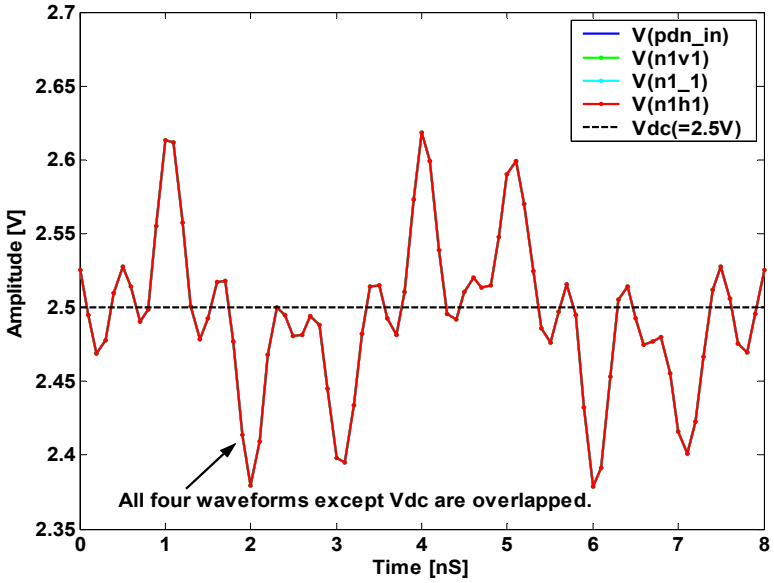
(b) Exemplary four locations in a PDN as a two-layered 3x3 Π-type distributed RLC network.

Figure 4.6: Locations of Ports and Internal Nodes in a PDN (Single Channel).

Figure 4.7 shows the single channel simulation results consisting of the voltage waveforms at planes (figure a) and a PDN with ideal via connections between M4 and M5 (Rvia=0) (figure b).



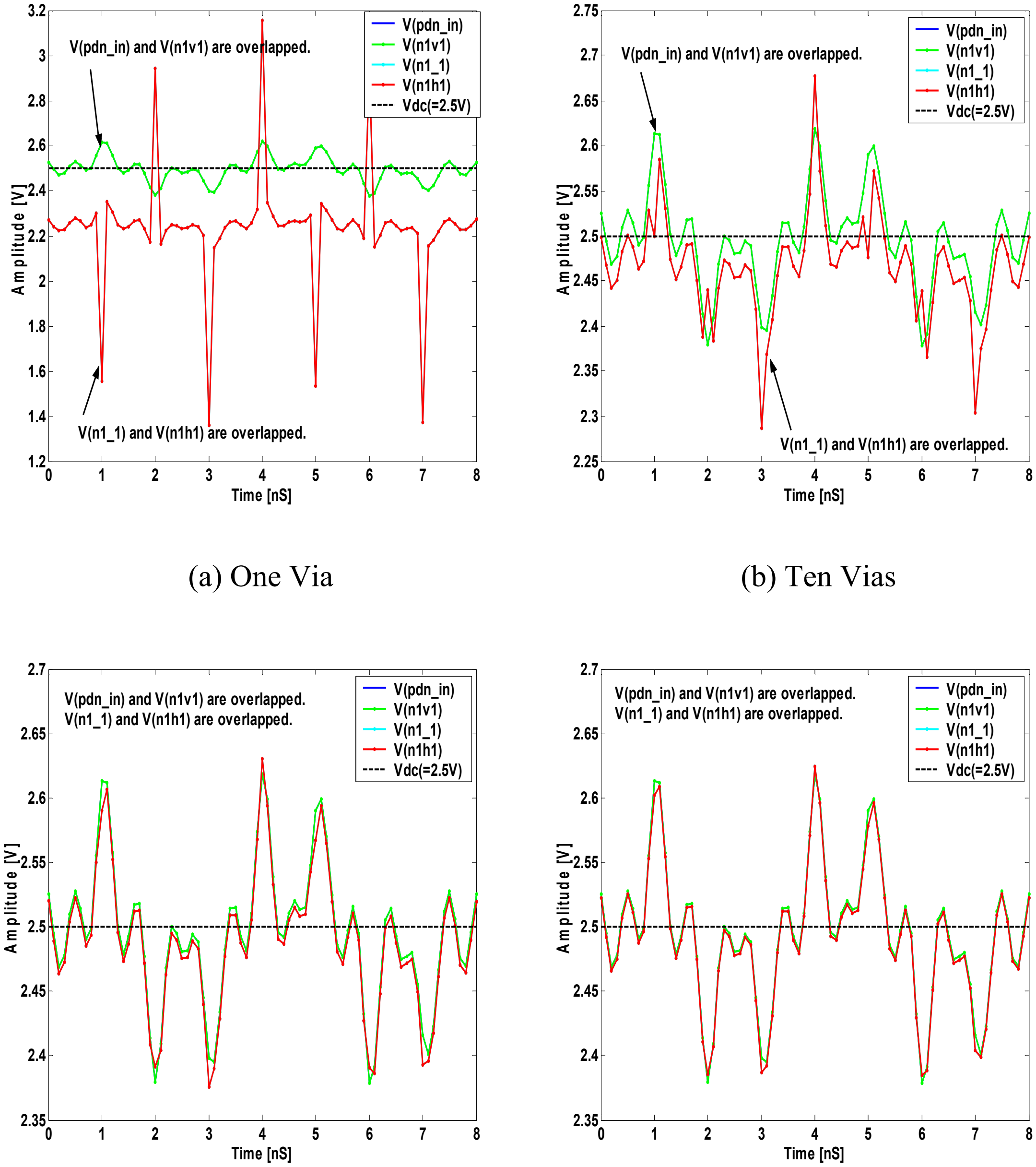
(a) Input and Output Waveforms at Two-Ports in Power-Ground Plane.



(b) Voltage waveforms at Various Locations in the PDN w/ infinite number of vias.

Figure 4.7: Simulated Waveforms at Two-Port Network (Single Channel).

However, if the impact of via is included, the results will be different with a certain amount of IR drop due to the resistive nature of via connections as shown in Figure 4.8.



(a) One Via (b) Ten Vias

(c) 50 Vias (d) 100 Vias

Figure 4.8: Simulated Waveforms with Various Numbers of Via at Single Channel.

Figure 4.8 (a) has distinct IR drop and Figure 4.8 (b) has reduced IR drop but still needs improvement. Figure 4.8 (c), (d) have negligible difference. Thus, from now on, unless otherwise specified, all the simulations results use 50 vias for a junction between M4 and M5.

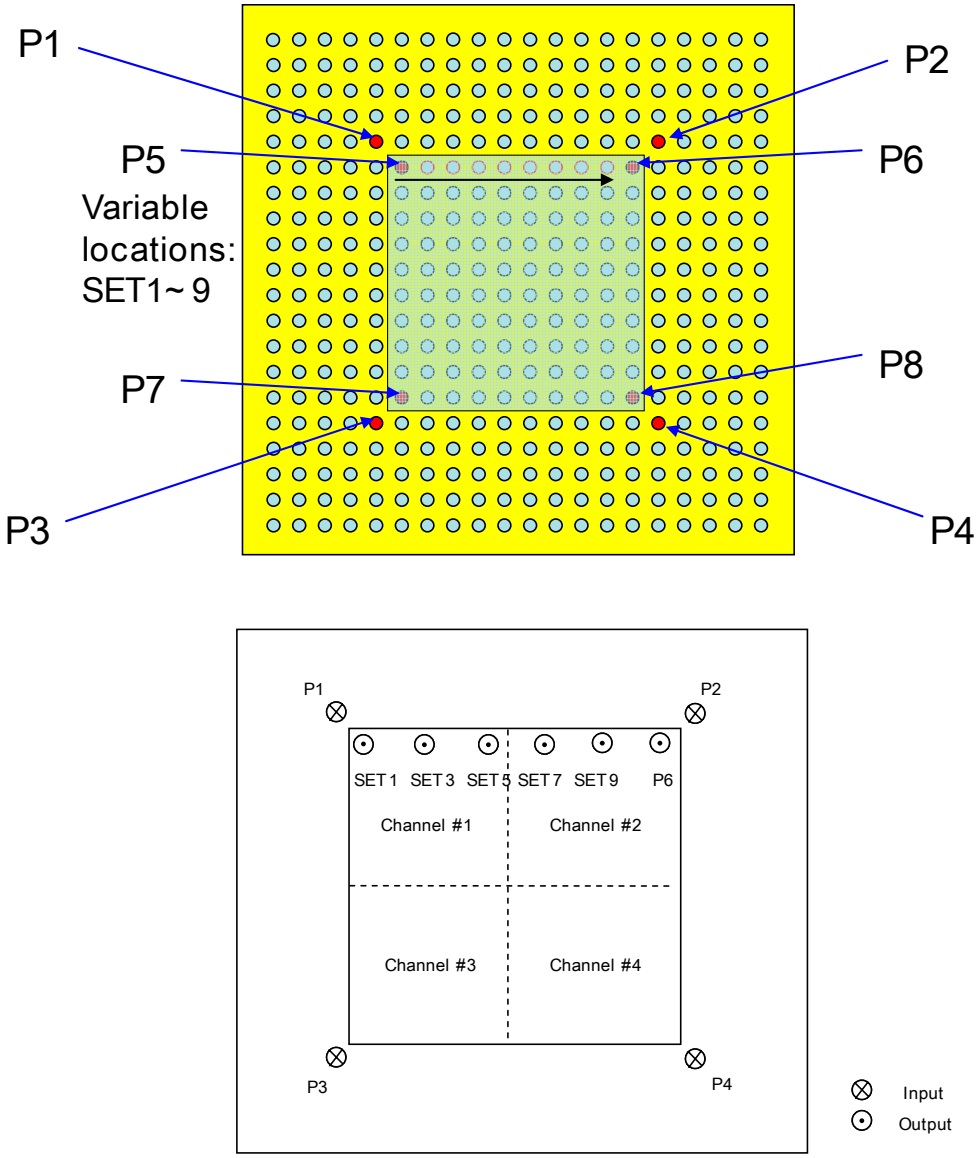
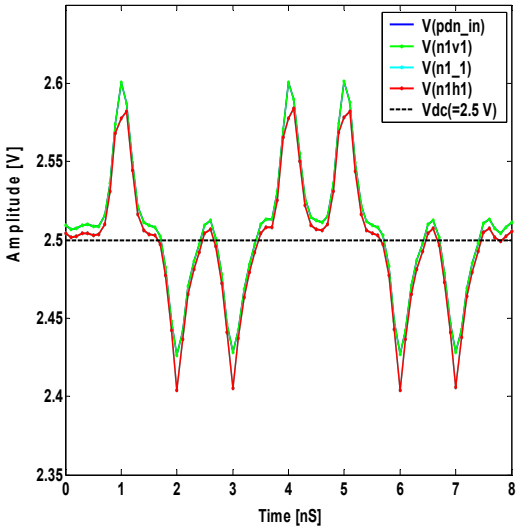


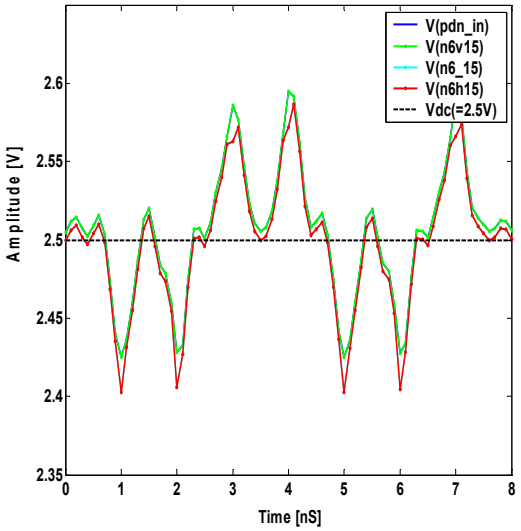
Figure 4.9: Port Locations and Channel Assignment of Four Channel (8 port) Simulations.

Figure 4.9 presents the port locations for four-channel simulations. The outer four ports of P1 – P4 are used as inputs, and the inner four ports of P5-P8 are used as outputs. Each set denotes a different P5 location in order to investigate the impact of interference on the multichannel data transmission. Four channels are assigned according to Cartesian coordinates in clockwise direction. Each channel assumes the use of orthogonal codes such as OVSF (orthogonal variable spreading factor) codes. In our simulations, channel #1, #2, #3, and #4 have {1001}, {0011}, {0101}, and {1111} as their corresponding OVSF codes. In addition, P5 is initially located at SET 1 and then moves to the neighbor cell (or channel #2) and finally reaches the SET 9 location, which is next to P6. As P5 approaches the cell border, the signal has more attenuation, and after passing through the border, it experiences phase inversion with decreased attenuation. However, all other channels (Channel #2, #3, #4 for P6, P7, P8) have good propagation properties which ensure the detection at the corresponding receiver port locations (See Figure 4.10 - Figure 4.14). P5, particularly for the proximity to the cell border, experiences more attenuation and phase flipping. Therefore, we need another method for securing detection – spreading. That is, even though the voltage waveform of P5 attenuates further, with the help of spreading, the required quality will be obtained with the sacrifice of data rate (PRI). If we employ a dummy channel, for example in this channel 1, the interference will be treated without sacrificing the data rate.

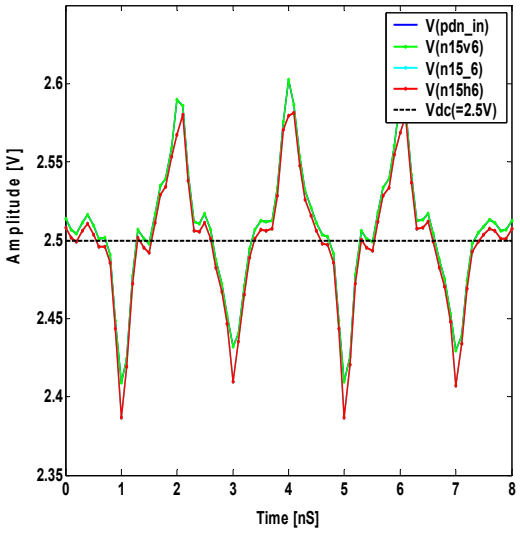
If we look at Table 4.1, particularly for P5 with five representative sets, the peak-to-peak voltage first decreases. Then once passing the border of channel #1, it will increase with phase inversion due to the different code sequence transmitted from channel #2 (P2).



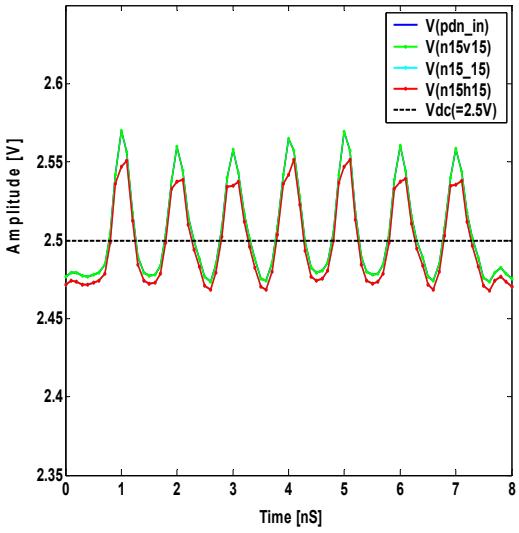
(a) Waveforms of P5 associated nodes



(b) Waveforms of P6 associated nodes

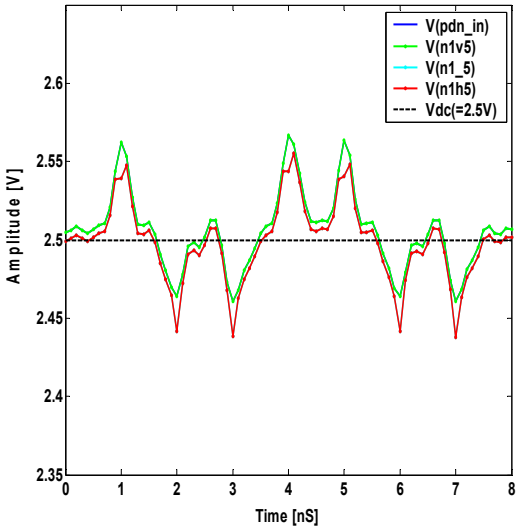


(c) Waveforms of P7 associated nodes

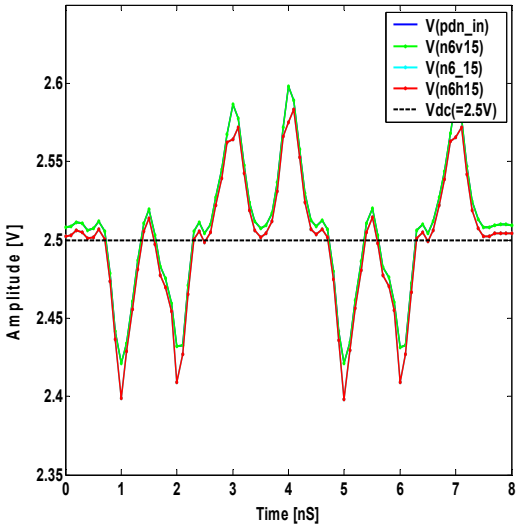


(d) Waveforms of P8 associated nodes

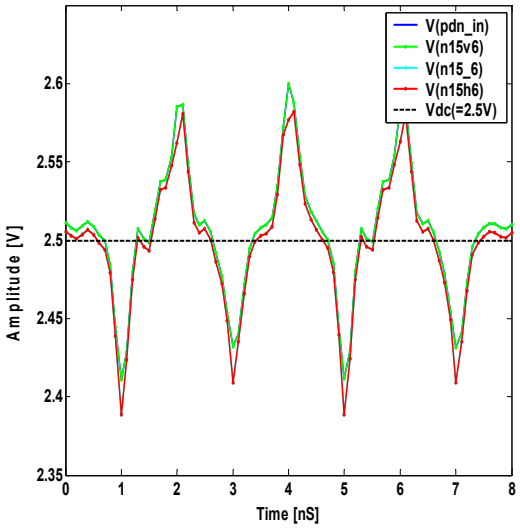
Figure 4.10: Four Channel Simulation (SET1; Symmetric Port Locations).



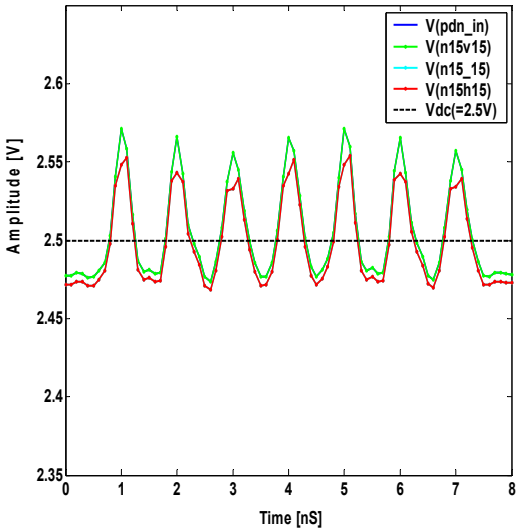
(a) Waveforms of P5 associated nodes



(b) Waveforms of P6 associated nodes

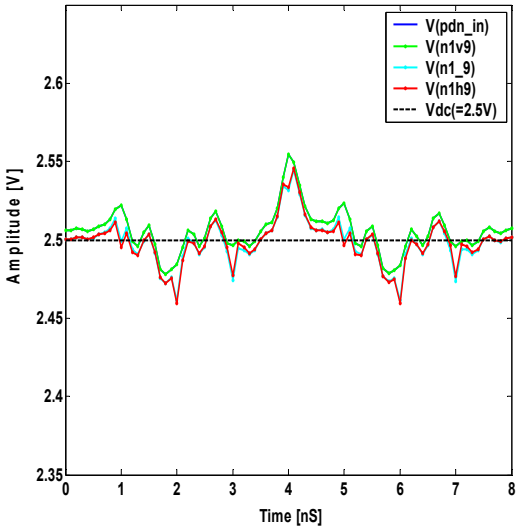


(c) Waveforms of P7 associated nodes

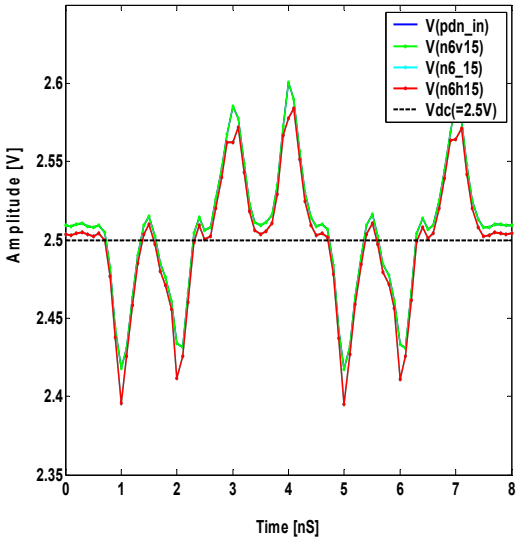


(d) Waveforms of P8 associated nodes

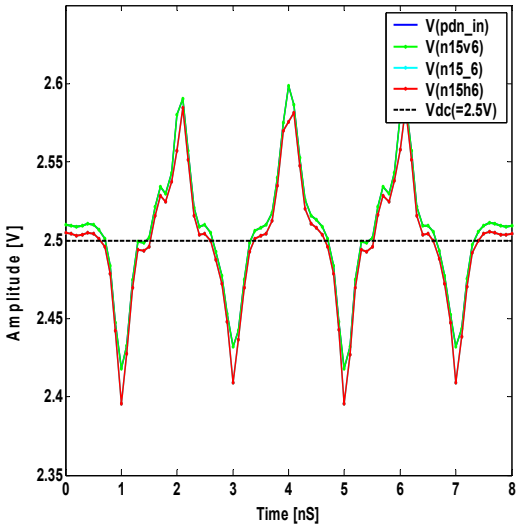
Figure 4.11: Four Channel Simulation Results (SET3).



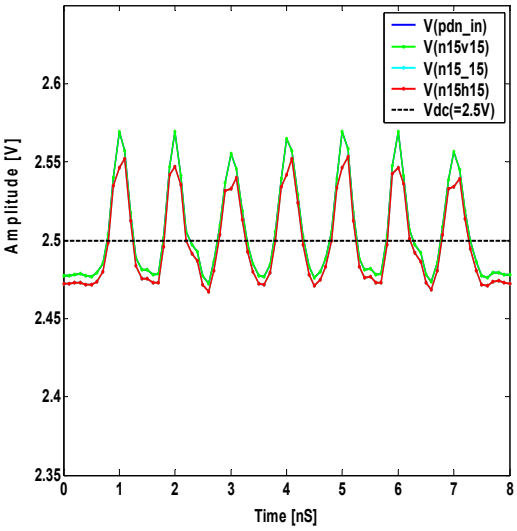
(a) Waveforms of P5 associated nodes



(b) Waveforms of P6 associated nodes

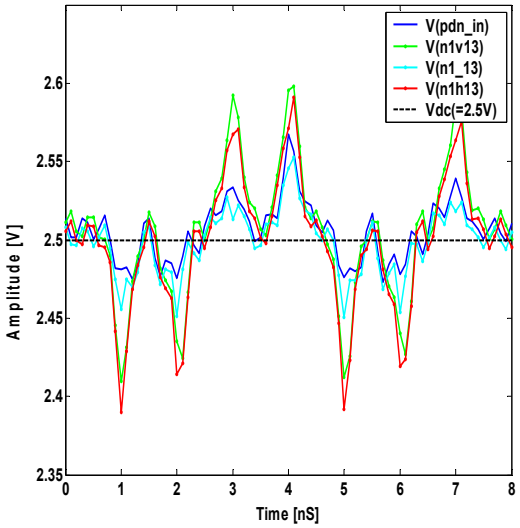


(c) Waveforms of P7 associated nodes

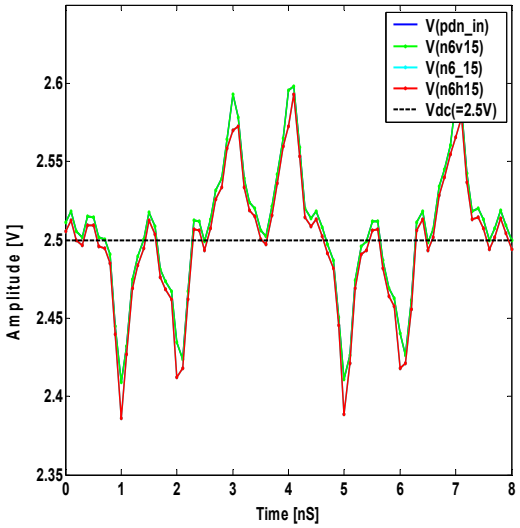


(d) Waveforms of P8 associated nodes

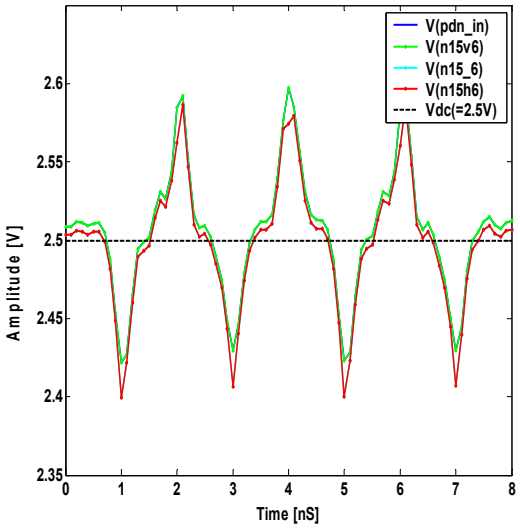
Figure 4.12: Four Channel Simulation Results (SET5).



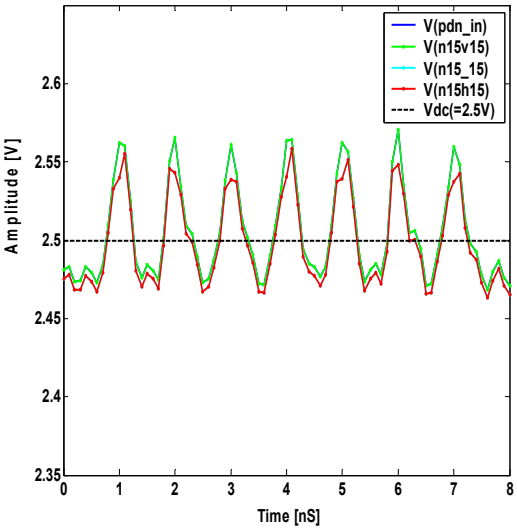
(a) Waveforms of P5 associated nodes



(b) Waveforms of P6 associated nodes

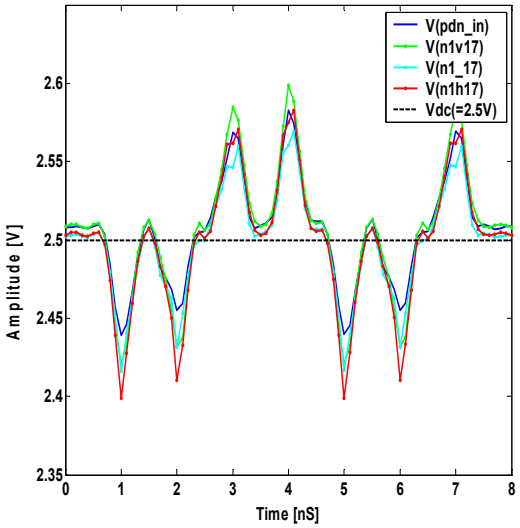


(c) Waveforms of P7 associated nodes

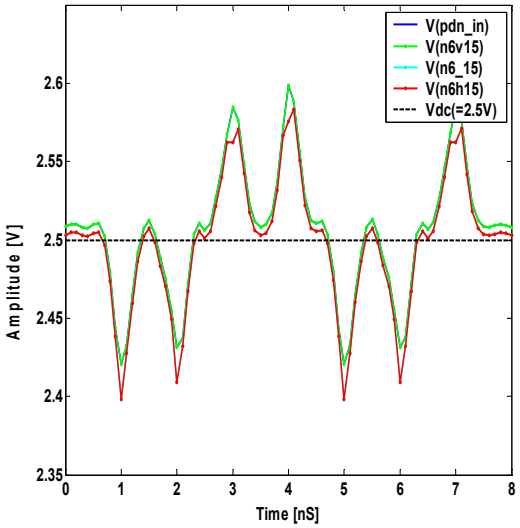


(d) Waveforms of P8 associated nodes

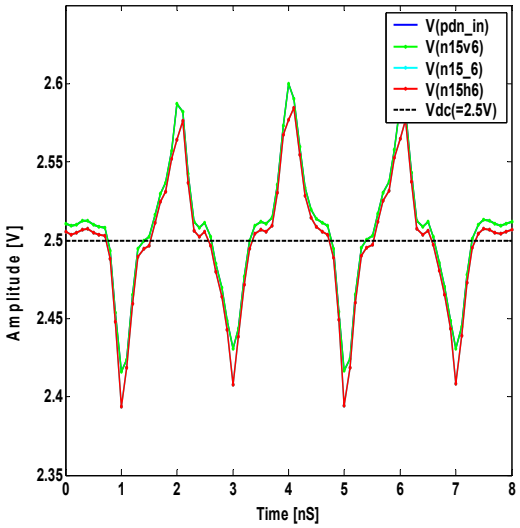
Figure 4.13: Four Channel Simulation Results (SET7).



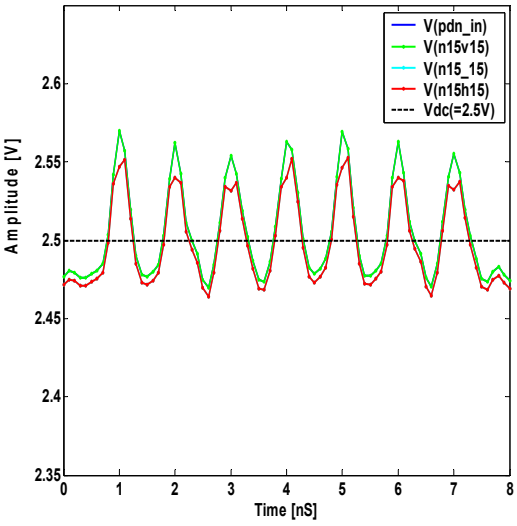
(a) Waveforms of P5 associated nodes



(b) Waveforms of P6 associated nodes



(c) Waveforms of P7 associated nodes



(d) Waveforms of P8 associated nodes

Figure 4.14: Four Channel Simulation Results (SET9).

4.5 Summary

In this chapter, we presented the chapter overview, the signal transmission method, the data recovery unit, and the simulations for the proposed data communications with realistic models in Sections 4.1, 4.2, 4.3, and 4.4, respectively.

In Section 4.1, we presented the overview of the proposed data communications over power distribution networks, which introduces the concept of dual use of power distribution networks for data communications in high speed integrated circuits.

In Section 4.2, we presented the basic principle behind the proposed communications. DS-UWB signaling incorporates the direct sequence-code division multiple access spread spectrum technology and impulse-based ultra wideband signaling for multiple channel data transmission with spreading gain at the receiver. The orthogonal variable spreading factor was explained.

In Section 4.3, we reviewed two realizations of the demodulator – the correlation method and the matched filter method – and discussed their impacts and properties. Then, we presented a simple architecture for the data recovery unit, which consists of a one-bit comparator, a counter, and a digital comparator. Next, we investigated the impacts of the number of samples in a pulse repetition interval and the impacts of the spreading factor. Three times of over-sampling is enough for practical purposes in the proposed communication scheme. As the spreading factor increases, the spreading gain increases but the link data rate decreases. Thus, we must decide the optimum spreading factor considering the spreading gain, data rate, and hardware cost required for the specific application.

Section 4.4 provided simulation results considering a generic planar structure IC package and power distribution networks (PDNs) with a cavity resonator model and a three-dimensional π-type distributed RLC circuit, respectively. The three dimensions of the distributed RLC circuit result from the vias in the two layers of PDNs. With a 50 via connection, we can get high quality pulse detection/recovery for all the channels. Under certain cases such as SET5P5 and SET7P5, we need spreading for better performance. We showed pulse inputs and output locations based on N-port networks in an integrated circuit.

Chapter 5

Case Study: A New Approach for Massive Parallel Scan Design

Based on the preliminaries discussed in Chapter 2, the microscopic channel model presented in Chapter 3, and the transmission and recovery of I-UWB signals over the power distribution networks in Chapter 4, we will present a case study in a high-speed integrated circuit environment which is comparable to a PowerPC750 processor and a Pentium III processor. The case study covers a potential application of our proposed one-way data communications scheme. It provides a new approach for massive parallel scan design. The case study includes the common and core parts for both one-way and two-way communication – the data recovery unit and its low-cost hardware architecture.

Section 5.1 starts with the background of this case study. As process technologies advance and integration levels deepen, there is an increasing need for reducing the test application time and pin counts in integrated circuits testing. In Section 5.2, we provide the synopsis of the proposed research – challenges and scan-in/scan-out data processing. Section 5.3 discusses various design parameters for designing a realistic power distribution network, such as chip dimension, number of power pins, package type, and the pad cell for power supply. In Section 5.4, the voltage drop is determined by considering the resistive IR drop and the simultaneous switching noise. The process for determining the voltage drop will be summarized with a brief flow chart. In Section 5.5, we consider the thermal noise, which is directly proportional to the temperature and measurement bandwidth. Section 5.6 discusses simulation results for the various conditions and parameters. Section 5.7 summarizes this chapter.

With this case study on the dual use of power lines for data communication in a system-on-chip environment, the feasibility is manifest; and it opens a new research area for low-cost, high-performance interconnect technology in the VLSI/SOC arena.

5.1 Background

As the test set size grows, reduction of test time in scan design is a critical issue and has been widely investigated. A straightforward method to reduce the test application time is via parallel scan chains [126]-[131], [136]-[139]. However, a scan chain requires a pair of scan-in and scan-out pins, and the number of available I/O pins often limits the number of possible parallel scan chains. Recently, we have proposed the dual use of power lines for data communications in a System-on-Chip (SOC) environment [16]. We will extend its application to parallel scan design to enable massive parallel scan design.

We investigated the feasibility of using power pins and power distribution networks for simultaneously carrying scan data and delivering power. A direct superposition of a digital scan data signal on a power pin does not permit simultaneous use for scan and power. The digital scan data signal induces undesired fluctuations in the power line voltage, and high noise levels in the power lines corrupt the scan signal. Further, the direct superposition precludes the possibility of multiple digital scan data channels on power lines, which are electrically connected inside a chip.

5.2 Synopsis

Two major technical challenges exist for the proposed method. The first one is to reduce the impact of fluctuations caused by the scan data signal applied on a power pin, while the signal is still recoverable from the power distribution network. The second one is to enable multiple scan data transmissions on multiple power pins. As noted earlier, we propose to employ the UWB and DS-CDMA communication techniques to address the challenges. In addition to the two technical challenges, we have to devise a scheme to scan-out data.

5.2.1 Scan-In Data Processing

Figure 5.1 illustrates the proposed method on a package with 44 power pins with the i^{th} scan data recovery block SDR *i* connected to Pin *i*. One bit of scan-in data is spread over multiple, narrow UWB pulses (which are typically a few hundreds of picoseconds wide) called chips. Antipodal binary-phase modulation is adopted in the figure, in which a chip signal represents 1 (-1) as a positive (negative) pulse. UWB pulses are observed at the output of the power pad, which is in fact the input of a data recovery block. A data recovery block de-spreads the received signal to recover the scan-in data bit. More specifically, it accumulates the chips correlated with the code word over the spreading period. A simple comparator is necessary at the input of the data recovery block such as the one shown in Figure 2.13 (b) [22], [108].

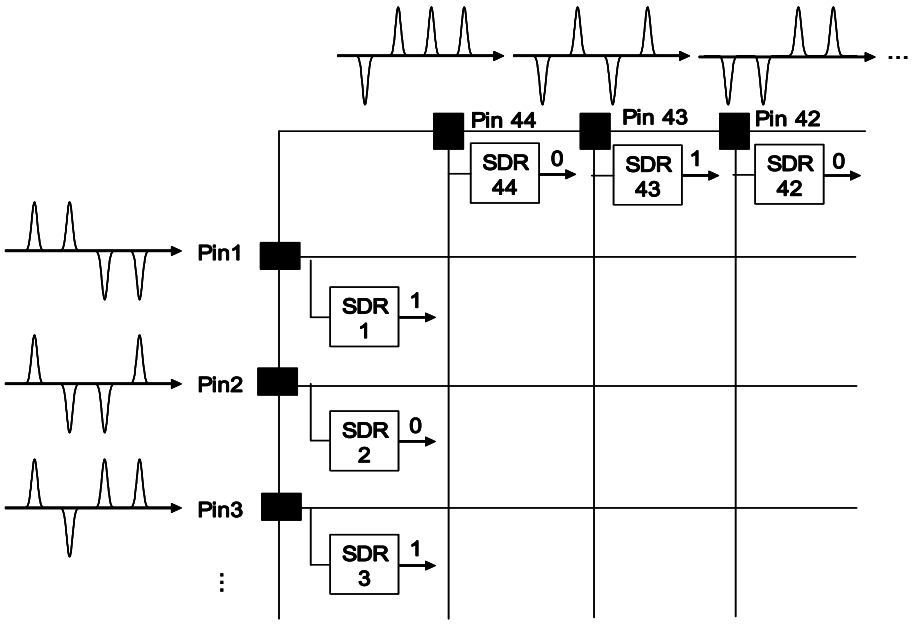


Figure 5.1: Overview of Dual Use of Power Pins.

The next challenge is to enable multiple scan data transmissions on power pins. Since all power lines are electrically connected inside a chip, multiple scan data signals on power lines interfere with each other. The DS-CDMA technique is employed to address this problem. When orthogonal codes are assigned to those multiple scan data channels, all the other scan data signals, except the intended one, behave as noise after the de-spreading

operation. For example, a codeword (1, 1, -1, -1) is assigned on pin 1, while a codeword (1, -1, -1, 1) on pin 2. The scan data recovery block associated with pin 1 de-spreads the received signal with the corresponding code (1, 1, -1, -1). When a scan data bit 1 is applied to pin 1, the de-spread value becomes 4 in a noise-free environment. When the scan data signal from pin 2 is de-spread by the same scan data recovery block, the de-spread value becomes 0, ignoring the slight difference in the propagation delays of the two signals. This means the data signals from other pins do not interfere with the scan-data recovery from a desired power pin. In reality, this is not quite true due to imperfect orthogonality caused by noise and propagation delay differences.

We suggest use of a comparator at the input of a data recovery block, which reduces hardware complexity. In fact, correlation or a matched filter operation increases the SNR (signal to noise ratio) of the recovered data over the use of comparators [125]. However, a correlator or a matched filter increases the hardware complexity as well as power consumption significantly. Also, analog correlators surrounded by digital blocks are sensitive to noise from digital circuits. Digital correlators and matched filters need a faster clock (by at least few times) than the scan clock, which may be a problem for a high speed scan-in operation. Our SPICE simulation indicates that the proposed comparator approach without over-sampling and spreading has a BER of 1.1×10^{-3} for 10 000 scan-in data. When the spreading factor increases to 4, we did not observe any error. In other words, the increase of the spreading factor by four times decreases the BER by at least a factor of 10.

Note that correlators and matched filters can be readily incorporated into the proposed design at additional cost.

5.2.2 Scan-Out Data Processing

We described a scheme to use power pins to scan-in test data. Use of power pins for scan-out data is not desirable, as the UWB pulse generators are expensive in hardware and power consumption. We propose a new scheme to multiplex parallel scan outputs to reduce the number of scan-out pins based on CDMA and PPM (Pulse Position Modulation).

The scan-out data of a scan chain shifts data out, one bit at a time, at the tick of every scan clock. Our objective is to share data pins among multiple scan chains, while the scan data shifts out at the chipping clock rate. Note that the chipping clock is available for the proposed system to de-spread the scan-in data. The process is illustrated in Figure 4.2. Each scan-out data signal s1, s2, …, s4, is spread through a unique orthogonal code in the horizontal direction at the chipping clock rate c_i. In this example, each bit is spread into a four-bit long code. Then, the chip values are added in the vertical direction, and the sum decides the pulse position in the time slot. For example, the sum of the first chip values is 2. Hence, the position of the pulse is 2 in the time slot c_1, which is displaced by two positions to the right. Similarly, the sum of the second chip values is -2, so that the pulse is displaced by two positions to the left. The scan-out data modulated in position is applied to the data pin. Note that there are 2N-3 distinctive positions in a time slot for N scan chains. A displacement of a pulse can be accomplished using a variable delay element such as the one in [125]. It is important to note that the pulse repetition rate is the same as the chipping rate, so *the proposed scheme operates at the chipping clock rate*, not any faster clock rate.

Now, let us consider recovery of the scan-out data, which is performed at ATE side or some dedicated external hardware. The ATE (Automatic Test Equipment) demodulates the PPM data for each code, *i.e.*, it detects the positions of pulses for the code. Then the demodulated PPM data is de-spread with the individual codes of the scan-out channels. For the example in Figure 5.2, the demodulated pulse sequence for the code is (2, -2, -2, -2).

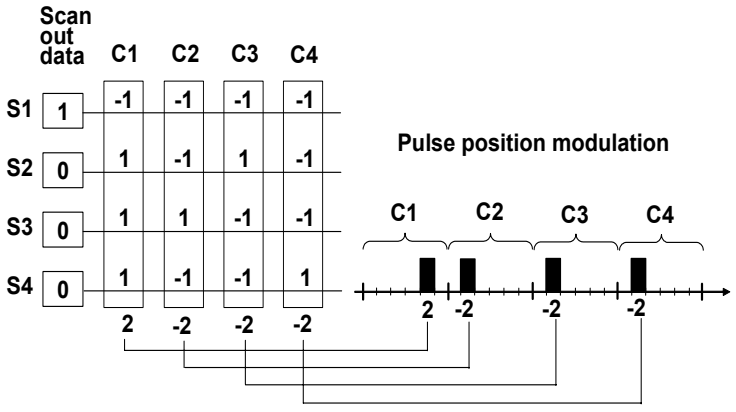


Figure 5.2: Overview of Scan-Out Data Processing.

The scan-out data for s1 is obtained by correlating with its assigned code (-1, -1, -1, -1). The correlated value is +4, which is interpreted as logic 1. Similarly, the assigned code for s2 is (-1, 1, -1, 1) (not its complement value.), and the correlated value is -4 to be interpreted as logic 0.

Finally, it is possible to multiplex scan-out data using the typical parallel-to-serial conversion and shift out with a faster clock. The clock speed limits the degree of multiplexing for this scheme. In contrast, the degree of multiplexing is bound by the number of possible pulse positions in a time slot, and it does not require a faster clock other than the chipping clock. Since PPM data are decoded by the ATE or other dedicated external hardware, it does not incur any hardware overhead to the circuit under test. Another point is that the spreading operation increases the resistance to noise. Since the spreading clock is readily available, the benefit of spreading operation would be far greater than a subtle increase in circuit complexity.

5.3 Design Parameters

We select the design parameters of chip dimension, number of power pins, package selection, and the pad cell for power supply.

5.3.1 Chip Dimension

Our power distribution network is modeled for an IBM PowerPC750 processor in a BGA (Ball Grid Array) package. The dimension of our power distribution network is set to 8.79 mm × 8.79 mm based on the area of the PowerPC chip (which is 7.56 mm × 8.79 mm).

5.3.2 Number of Power Pins

The PowerPC processor has 93 power/ground pins out of 360 pins, and the total number of power pins is set to 44 for this case study with SPICE simulations. As the number of power pins increases, the on-chip inductance and resistance decreases. That is the reason for the efforts for supporting the increased number of IOs for signal and power/ground as well. However, if the number of IOs increases, the cost for pins and the additional cost for testing would increase.

5.3.3 Package and Pad Cell

A widely adopted model for an IC package and a power pad is shown in Figure 5.3 [140]. V_i is the applied voltage of a pin, and V_o is the output voltage of the power pad. L_0, C_0, and R_0 are the parasitics of the package associated with wire bonds and lead frames, and C_1 and R_1 are the parasitics of the power pad. Z_L represents the impedance of the power distribution network, which is explained in detail in the following. Note that parasitics of L_0, C_0, and R_0 are usually provided by the packaging company. We considered an Amkor flexBGA 144 pin package for the case study due to the availability of its parasitic values in the public domain [51], and the following parameters are used.

- Parasitics of the package: L_0 = 0.25 nH, C_0 = 0.13 pF, and R_0 = 5 mΩ
- Parasitics of the power pad: C_1 = 203.62 fF and R_1 = 5 Ω
- ESD protection diode: (W/L=297/4), M=16.

The diode consists of 16 NMOS devices in parallel. The width of an NMOS diode is 35.64 μm and the length is 0.48 μm. The capacitive parasitics C_1 of a power pad are based on the TSMC 0.25 μm deep submicron process. The resistive parasitics R_1 are calculated from the sheet resistance model [19]. The capacitive parasitics of the ESD protection diode are extracted from the layout of the power pad.

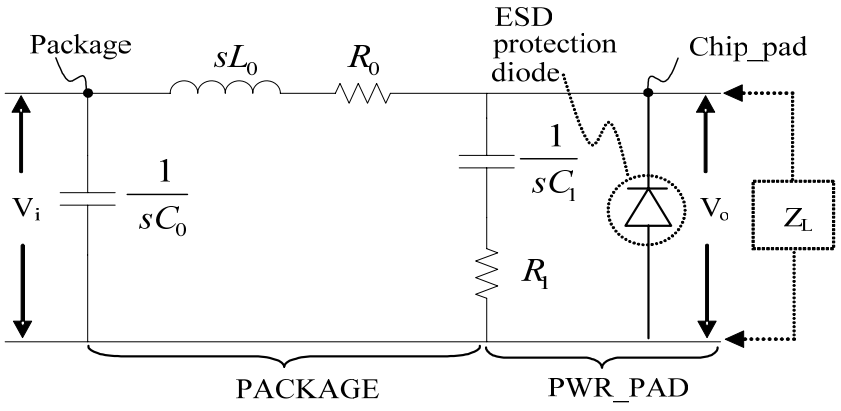


Figure 5.3: An Equivalent Circuit of a Package and a Power Pad.

5.4 Voltage Drop

5.4.1 Resistive IR Drop

The dynamic power consumption of the processor (a PowerPC750 processor) is 7.3 W @ 300 MHz with a supply voltage of 2.5V. The current source I_s at each cross point sinks 17.6 mA to result in the total power consumption of 7.3 W. The maximum IR resistive drop is set to 10 percent of the power supply voltage, which is 0.25 V at the center point of the grid. The 10 percent is provided as a guide for IR drop in a power distribution network design in the literature [126], [141]. Efficient power/ground network design and analysis were investigated in [127], [128]. We computed the width of a power line w to achieve the maximum allowable IR drop based on the iterative procedures in a flow chart as shown in Figure 4.4 in Section 4.4.2.

5.4.2 Inductive Loss

Another reason for voltage drop is the inductive loss resulting from the simultaneous switching noise (SSN) of current consuming devices. Since the voltage drop due to this inductive loss results from either the inductance of wires or the SSN of internal devices, any method for reducing either of the two factors would work. There is a good reference which provides the insights on the challenges in power-ground integrity [129].

The inductance of the wire bond in a package was given for two cases of the shortest and the longest paths. The shortest path is the path between the chip I/O in the center of an edge and the package I/O in the center of an edge. The longest path occurs at the path between the chip I/O in the corner of its dimension and the package I/O in the corner of corresponding dimension. We linearly interpolate the two extreme cases for intermediate values of inductive loss to the I/Os located between the two locations (the end and the center of an edge). The inductance of an on-chip metal wire is computed using (2.3) in Section 2.2.2.2. The inductance value of an on-chip metal wire is 59.867 pH and the total inductance of on-chip wires can be approximated as parallel connected inductors by analyzing the relationship between two metal planes connected in parallel [18]. For the given geometry, the total inductance is 2.3026 pH. If we assume a 2 % voltage drop, the

SSN can be obtained as 108 mA/ns from the equation of $L \cdot dI/dt = \Delta V_{SSN}$. Typically the internal circuits are modeled as current sources from power supply (VDD) to ground (GND) [124]. For a typical CMOS chip, these currents are shaped as a saw tooth waveform and different circuit families have different current signatures [130]. Another approach for modeling the SSN more realistically using modeling parameters from three PowerPC processors is found in [131]. We modeled the SSN with a rising slope of 108 mA/ns for 50 ps followed by a symmetrical falling slope to each current source at every node in a power distribution network.

5.5 Thermal Noise

Thermal agitation is another source of noise in a power distribution network. Mostly, it is from the devices on the power distribution network and is modeled as resistors or MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices (a kind of voltage controlled resistor). In the case of CMOS (Complementary Metal Oxide Semiconductor) devices, the thermal noise is analyzed and modeled depending on the gate voltage and drain current. In the case study, we generated thermal noise which is infinite in bandwidth.

The signal-to-noise ratio (SNR) is defined as the ratio of average current (I_{avg}) to absolute magnitude of current fluctuation ($I_{thermal}$) in dB as $10*\log_{10}(I_{avg}/I_{thermal})^2$ [dB]. Since the infinite bandwidth of noise was assumed, it is generated using a normal distribution of zero mean and a variance which is equal to the energy of the current noise ($I_{thermal}^2$). The current noise at the SNR of 10 dB is modeled in our case study using MATLAB and then incorporated into the SPICE simulation.

The average current is computed as {(P/V)/NIN}, where P is the total power consumption of 7.3 W, V is the power supply of 2.5 V, and NIN is the number of internal nodes on the power mesh, which is 165 for the designed power distribution network. The average current of 17.6 mA is obtained and added as current sources. The current source I_s at each cross point on the power distribution network sinks 17.6 mA to result in the total power consumption of 7.3 W.

5.6 Simulation Results

Gaussian[12] *UWB pulses with peak amplitude of 0.25 V, which is 10 percent of the supply voltage,* and a width of 1 ns were considered for our simulation. The maximum chipping rate, i.e., the pulse repetition rate, is set to 1 GHz.

The first and most critical experiment is to examine whether UWB pulses propagate through power pins. We applied UWB pulses only at power Pin 1 for the single channel environment (refer to Figure 5.1), while the rest of the 43 power pins are at VDD = 2.5 V Note that perfect impedance matching between UWB transmitter and power pins is assumed. Figure 5.4 shows the waveforms at the input of the power pin and at the output of the power pad *i.e.*, at the input of the scan-in data recovery block.

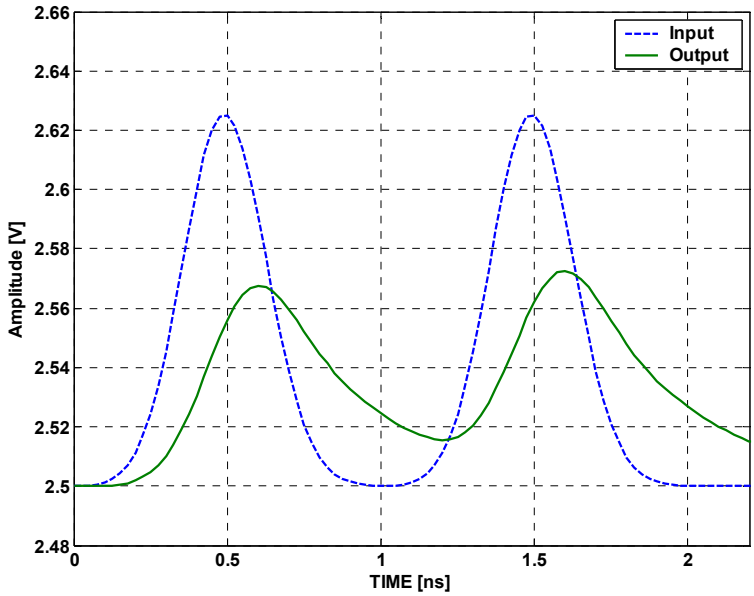


Figure 5.4: Noise Free Waveforms for the Single Scan Channel Environments.

The waveforms indicate that the attenuation of the peak of the pulses due to the package parasitics is in the range of 40 to 48 percents, and the propagation delay at the peak is about 100 ps. Although the peak is attenuated, pulses propagate through pins to open the possibility of using UWB pulses on power pins. The peak of the second output pulse is

[12] Refer to [116] for the shape of Gaussian pulses.

higher than that of the first output pulse. This is due to the tail of the first pulse causing inter symbol interference, and it can be mitigated by DC offset cancellation or simply a longer pulse repetition time.

The next experiment is to examine the interference level from a UWB pulse applied on an adjacent pin. We applied two consecutive positive pulses to Pin 5 and a positive pulse followed by a negative pulse at Pin 7. Note that Pin 6 is the center power pin on a side. Figure 5.5 shows the simulation results, and the output waveform is shown only for Pin 5.

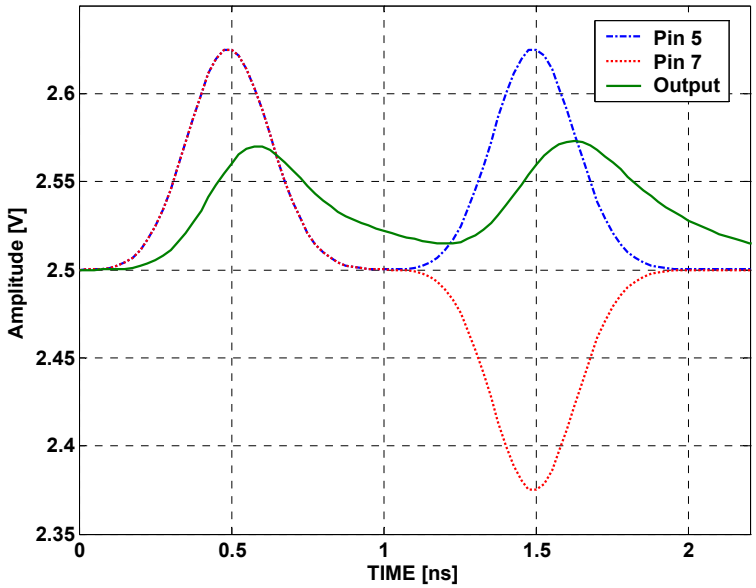


Figure 5.5: Noise Free Waveforms for the Two Scan Channel Environments.

As expected, when the two pulses add constructively, the output increases. When the two pulses have the opposite polarity, as in the case of the second pulses, they may add destructively to cause inter channel interference. However, the attenuation level due to the inter channel interference is negligible as shown in the figure. So the experiments indicate that the interference from other pins does not pose a problem. It is important to note that as a scan data recovery block moves away from the power pad toward the central point of a PDN, it will experience a higher level of inter channel interference to limit the number of parallel scan chains. In such a case, the power levels of individual UWB transmitters can be adjusted properly to maximize the number of scan chains.

Next, we added both Ldi/dt and the thermal noise to *each* current sink, *i.e.*, load. The Ldi/dt noise has a rising slope of 108 mA/ns for 50 ps followed by a symmetrical falling slope. The thermal noise has a Gaussian distribution limited to 5 percent[13] of average current at each current source. We set the level of the thermal noise intentionally high to account of variations of the L di/dt noise for real circuits. The waveforms under the two scan channels (Pin 5 and Pin 7) are shown in Figure 5.6 and the output waveform is shown only for Pin 5.

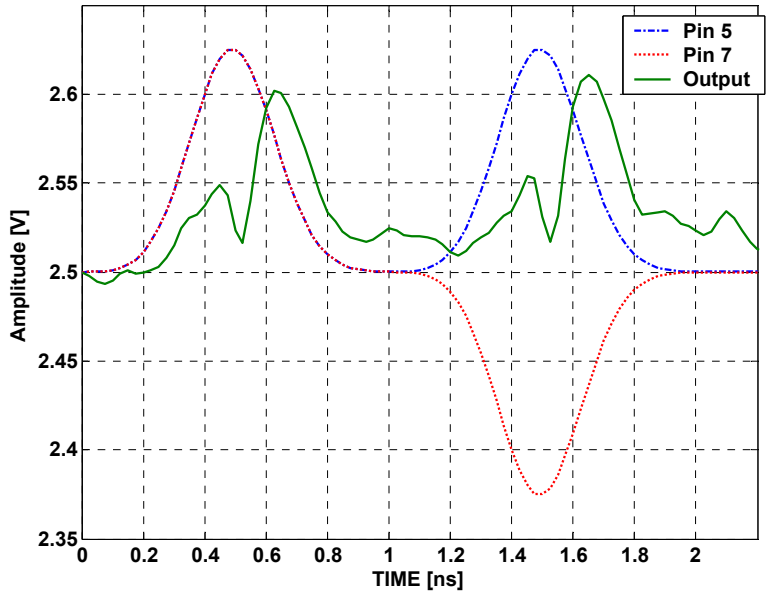


Figure 5.6: Waveforms with Ldi/dt and Thermal Noise.

The Ldi/dt noise incurs a dip notch slightly after the peak of the input, and the thermal noise distorts the output waveform for the entire period. The output waveform indicates that the sampling time of the output is critical when a comparator is used for a scan data recovery block. Note that it is not a problem for a correlator, which integrates the waveform for an entire clock period.

The next experiment examines the performance of the overall system in terms of BER (bit error rate). We considered a comparator (rather than a correlator) for the data

[13] More precisely, the 3σ value of the thermal noise is $0.05I_{avg}$.

recovery block in our simulation. We experimented with a single scan chain, in which we applied data to only one pin under the conditions of Ldi/dt and thermal noise mentioned above. We then compared the recovered data with the original data. After applying 100,000 scan-in data bits, we did not observe any errors – even without spreading, i.e., SF (spreading factor) = 1. Since the BER[14] is less than 10^{-5} for 100,000 scan data bits under SF=1, there is no need to experiment with a higher spreading factor. We then experimented with 44 scan channels, in which scan data is applied to all 44 pins. Again, we did not observe any errors even under SF=1. Although we have not experimented with a sufficiently large number (such as on the order of 10^{11}) of data due to long simulation time, we believe that the proposed method could be used for parallel scan chains without employing the spreading operation.

Finally, in order to see the impact of spreading, we experimented with an artificially inflated (and hence unrealistic) level of the thermal noise. We set the thermal noise level to 10 percent of average current and considered two different spreading factors, SF=1 and SF=4, under four scan channels. We adopted OVSF (Orthogonal Variable Spreading Factor) codes, which are employed in Third Generation CDMA standards [132]. The center power pin on each side is selected to maximize the distance between pins. Under the application of 10,000 data bits, we obtained the BER=1.1×10^{-3} for SF=1. When the spreading factor increases to 4, we did not observe any errors. In other words, the increase of the spreading factor by four times decreases (or improves) the BER by at least a factor of 10.

Before we close this section, we describe the method of determining the sampling instant of the received signals for the data recovery blocks. The sampling instant may significantly affect the performance of the proposed system, especially when a comparator is used for a data recovery block. An eye diagram is a useful tool to determine the effects of the sampling instant and jitter for the received signals since eye diagrams have been frequently used in communication systems for the evaluation of channel imperfections [133]. Unlike wireless communication systems, the UWB signal generators on the ATE

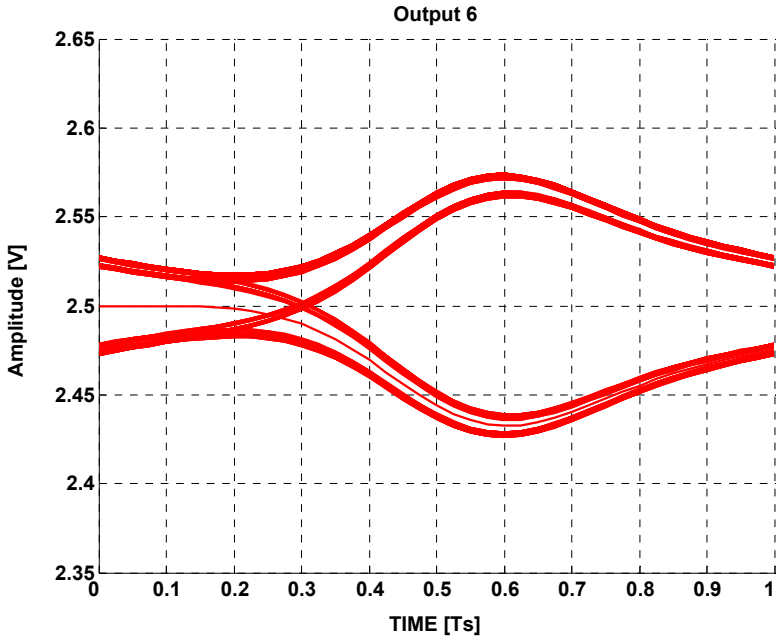
[14] In this case, we did not observe any errors for 100,000 scan data bits.

side and the data recovery blocks for the proposed system are synchronized through a dedicated clock signal line. So, clock jitter has insignificant impact on an eye diagram for the proposed system. The major sources of error in the eye diagram for the proposed system are Ldi/dt and thermal noise.

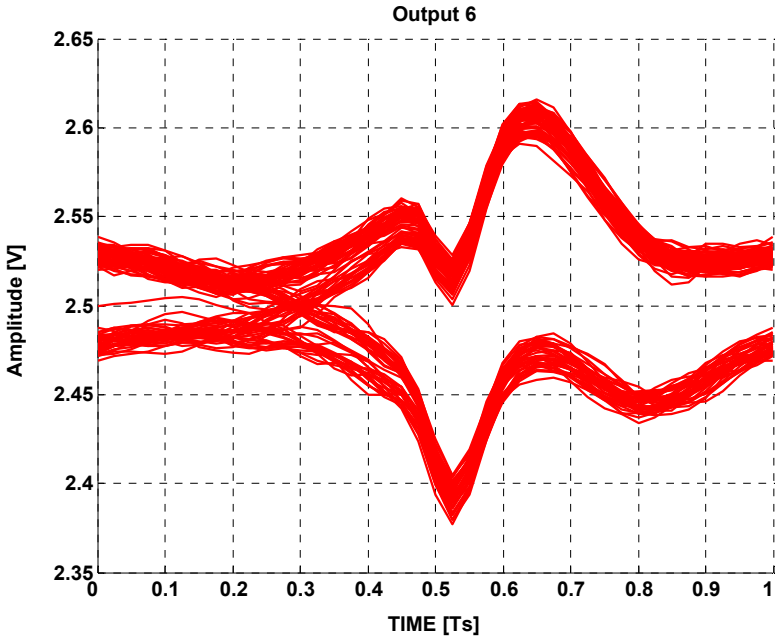
Figure 5.7 shows the observed eye diagrams for 100 data bits under a single scan channel.

Figure 5.7 (a) shows the eye diagram without considering Ldi/dt and the thermal noise. In this case, the optimal sampling instant would be at 0.6Ts for both a data bit 1 and a data bit 0.

Figure 5.7 (b) shows the observed eye diagram with the Ldi/dt and the thermal (5 percent) noise mentioned above. As shown in the figure, the optimal sampling instants are different for a data bit 1 and a data bit 0. The sampling instant at 0.52Ts, where Ts is the symbol duration, is the best for a bit 0, but the worst for a data bit 1. It is the opposite for the sampling instant at 0.63Ts. As a compromise, we set the sampling instant to 0.60Ts in our simulations. The possible performance degradation would be overcome by considering over-sampling.



(a) Without Ldi/dt and thermal noise



(b) With Ldi/dt and Thermal Noise

Figure 5.7: Observed Eye Diagrams at Pin 6.

5.7 Summary

In this chapter, we presented a case study with a realistic power distribution network, which is comparable to that of a PowerPC750 processor [135].

In Section 5.1, we discuss the background and the meaning of the case study, which is the proof of concept showing the feasibility of the proposed data communications scheme. Section 5.2 presents an overview of the proposed communications scheme with respect to the massive parallel scan design.

Section 5.3 discusses various design parameters for a power distribution network, including chip dimension, number of power pads, package selection, and pad cell of a power IO. In Section 5.4, the most important design consideration in power distribution networks – voltage drop – is discussed. First, we presented a resistive IR drop determination procedure in a flow chart. The IR drop design is basically an iterative procedure, and its inputs are the number of power pins, the width of a power bus, and the specification of the IR drop. Available resources for the design process are the number of

power pins and the width of a power bus. Next, we covered voltage drop due to the inductive loss. In order to reduce the impact of the inductive loss, we need to elaborate the package design, which incorporates the length of wire bonds and/or the power bus design, which reflects potential design parameters such as the optimum width of the power bus. In Section 5.5, the generation of thermal agitation in devices on a chip is investigated and the SNR of 10 dB was considered in our case study.

Section 5.6 provides various simulation results of I-UWB pulse propagation in a single channel that includes the switching noise, the thermal noise, various spreading factors, and their corresponding waveforms at the input of a data recovery unit. In this section, we proposed a new approach for massive parallel scan design through dual use of power pins. UWB and CDMA are employed to address noise and multiple access problems associated with power pins. To investigate the feasibility of the proposed design, we presented SPICE simulation results for a wire-bonded BGA type package and power pad cells in a 0.25 μm CMOS process. The chip dimension is comparable to that of a PowerPC750 processor. The simulation results include the pulse propagation delay and attenuation with/without IR drop, simultaneous switching noise, and thermal noise. We also simulated the impacts of spreading factors on the BER performance.

In existing scan designs, each scan chain requires a pair of scan-in and scan-out pins, and the number of available I/O pins often limits the number of possible parallel scan chains. We proposed a new approach to address this problem. The key idea employed for our approach is the dual use of power pins for scan-in data communications as well as for delivery of power. Specifically, we proposed to use DS-CDMA combined with UWB signaling to avoid degrading power delivery. We also proposed a new scheme to multiplex scan-out data using PPM and CDMA.

Our SPICE simulations indicate that the proposed method is indeed feasible for parallel scan design. Scan-in test data are recovered correctly at power pads for 44 scan channels under a realistic PDN and a realistic noise model. However, to deploy our method in the real world, further study is necessary, especially into the load boards of ATE. Finally,

the proposed method offers the possibility for monitoring the internal logic values through a PDN and power/data pins, which opens many new applications in testing and diagnosis.

Chapter 6

Discussion and Conclusion

Power lines are ubiquitous and an essential part of our every day lives. The concept of power line communications was introduced in patents in the 1920's, and since then there has been much research activity on power line communications. Recently in the 2000's, power line communications has been revived for broadband network service over power lines. Power line communications has a fundamental benefit of "no new wires," but at the same time it has several challenges, such as a noisy channel environment and regulations for electromagnetic compatibility.

Current power distribution networks in most of the high performance digital systems - whether they are on an integrated circuit or on a printed circuit board – are used only for their original purposes, which are the delivery of clean power supply voltage with an optimum metal width. The ubiquitous resources in power distribution networks are power lines and pins, which have never been used for data communications.

We, for the first time, proposed to use microscopic power distribution networks, which are microscopic in both supply voltage level and physical dimension of the channel. This thesis investigates **the dual use of power distribution networks for data communications in high speed integrated circuits**. The proposed data communications over power distribution networks provides a paradigm shift from the use of many IOs for signals and power delivery to the use of a minimum number of signal IOs and required number of power IOs [16], [17]. Our proposed communication scheme inherits challenges from macroscopic power line communications. Communications over *noisy power line channels* would require a novel signaling, which is robust in such a noisy environment. In addition, *multichannel data transmission* can enhance the benefits of the proposed method,

since it can be applied for useful applications in high-speed integrated circuits, including massively parallel scan design and inter- and intra-chip data communications. I-UWB can overcome the first challenge of the noisy power line channels in power distribution networks, and the DS-CDMA principle can make multichannel data transmission possible. Thus, we adopted the DS-UWB signaling as a potential methodology for the proposed data communications.

The purpose of this thesis is to investigate the I-UWB with DS-CDMA signaling over power distribution networks for data communications in an integrated circuit.

First, Chapter 1 introduces advantages and the challenges of power line communications, and provides an overview of the proposed microscopic data communications in two categories – one-way and two-way communications.

Chapter 2 provides the necessary background for this thesis, and it includes the power distribution networks, packages, pad cell of power supply, and ultra wideband signaling. We investigate the power distribution network from its definition; parasitics of resistance, inductance, and capacitance; noise; and signal transmission models. A power distribution network is a hierarchy of voltage regulator modules, on-board decoupling capacitors, packages of integrated circuits, and on-chip decoupling capacitors. Typically the higher layer of on-chip metal wires is preferred for power bus routing, since it has low resistive loss. Recently, inductance has been an important factor, since it impacts the signal integrity due to its high speed operation and increased on-chip inductance. These overall parasitics and noise (both thermal and simultaneous switching noise) cause delay and the attenuation of UWB signals. In addition, the package and its RLC parasitics affect the signal delay and attenuation for the same reason. We also investigate packages and pad cells for a 0.25 um process. In Section 2.6, we investigate the fundamentals of ultra wideband radio technology, including definition, applications, transceiver architecture, and multichannel data transmission scheme. Section 2.6.2 proposes a method to overcome the challenges of applying I-UWB to power distribution networks. We need a low cost transmitter/receiver architecture to facilitate the adoption of DS-UWB.

Chapter 3 investigates the microscopic channel model and its modeling philosophy

with an overview of simulation methodology. The channel is considered as a cavity resonator model for the planar structure IC package. All other components of this channel are power distribution networks including pads and package pins (or balls). Based on the frequency domain impedance matrix method for the cavity resonant model, we obtained the time domain responses for various port locations in an IC package.

Chapter 4 discusses the transmission and data recovery scheme with its hardware architecture. As a communication channel, metal wires have been analyzed and modeled with generic lumped RLC circuits. For more accurate results for the delay and attenuation, we suggest to use the distributed π-type RLC model. Data recovery is possible by overlaying spread I-UWB pulses on the power supply voltage. For this, we devise a simple, low-cost data recovery unit, which requires a one-bit comparator and an accumulator. As the spreading factor increases, the spreading gain and the number of channels increase without incurring any reduced channel capacity in terms of aggregate data rate.

Chapter 5 investigates a case study that exploits the unique signaling of I-UWB to benefit power distribution networks. Section 5.1 provides the background of the case study. Section 5.2 presents the proposed data communications for a representative one way communication – massive parallel scan design in views of Scan-In and Scan-Out Data Processing. In Sections 5.3, 5.4, and 5.5, various design parameters, including chip dimension, number of power I/Os, voltage drop design, and thermal noise are discussed. In Section 5.6, we provide SPICE simulation results with relevant observations. First, we consider the pulse propagation and detection in a realistic π-type distributed RLC circuit model. The scan data recovery scheme is illustrated using single bit and 4-bit codewords. In addition, spreading factors (SFs) are considered as a means of multichannel transmission and spreading gain as an enhancement of the signal-to-noise ratio. We obtained the BER=1.1×10^{-3} for SF =1 and BER < 10^{-4} for 10,000 scan data bits applied for SF=4 (When the spreading factor increases to 4, we did not observe any errors for the 10,000 scan data bits). We observed the optimal sampling instant is 0.60Ts (60 percent of symbol duration) for both the ideal channel and the noisy channel from the observed eye diagrams.

The thesis quantitatively differentiates the power line communications into

application scenarios. It is expected that one-way communication schemes are more attractive in cost saving since it needs only a data recovery unit and a PPM transmitter; whereas two-way communication schemes offer a more costly solution due to the use of a UWB transmitter on chip. The communication scheme would be decided in an application-specific manner.

In summary, the unique signaling of I-UWB overcomes the challenges of implementing communications over a power distribution network. I-UWB signaling overcomes the challenge of not perturbing the voltage drop of a power distribution network. DS-UWB signaling also overcomes the challenge of implementing multi-channel communications.

This thesis investigated 1) a new approach of high performance interconnect, 2) an IC package such as the flip-chip type ball grid array package, 3) a plane structure for power distribution and its modeling, 4) evaluation of bit error rate performance, and 5) computationally efficient simulation methodology based on MATLAB, PERL, and SPICE.

Physical design for the data recovery unit remains for future challenge. It is expected the dual use of power distribution networks for data communications in high-speed integrated circuits will improve performance and cost over traditional interconnect technology without the hardware overhead of a correlator or a matched filter. The optimization of design parameters of the package, pad cell, and power distribution networks should further improve performance.

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