Chapter One

Introduction

1.1. RESEARCH BACKGROUND

The advances in VLSI (very large scale integration) technologies impose a new challenge for delivering high-quality power to modern microprocessors [A1, A2, A3].

As Moore's Law predicts that transistor density "… doubles every eighteen months," the number of transistors per die in microprocessors has increased steadily in the past decade, as shown in Figure 1.1 [E1, E2, E3, E4]. Correspondingly, the clock frequencies of microprocessors have also greatly increased.

The increases in the microprocessors' speed and transistor number have resulted in an increase in current demands and transition speeds. The supply voltages of the microprocessors have been decreased in order to reduce power consumption.

As Intel predicted (Figures 1.2 and 1.3), with the continuous increase in the speed and transistor number within the chips, the microprocessors operate at significantly low voltages, high currents and high slew rates [E1, E2, E3].

These low voltages, high currents and high slew rates are the challenges imposed on power supplies for microprocessors. The centralized silver box is the typical power source in computer systems. However, with the lower voltage and higher current

demands, the parasitic resistance and inductance between the centralized silver box and the microprocessor have a severe, negative impact on power quality. It is not practical to use the centralized silver box to provide power directly to the microprocessor.

The power supply architecture must be changed. The point-of-load regulation system is used to deliver a highly accurate supply voltage to the microprocessor, where a dedicated DC/DC converter, the voltage regulator module (VRM), is placed in close proximity to the microprocessor in order to minimize the parasitic impedance between the VRM and the microprocessor.

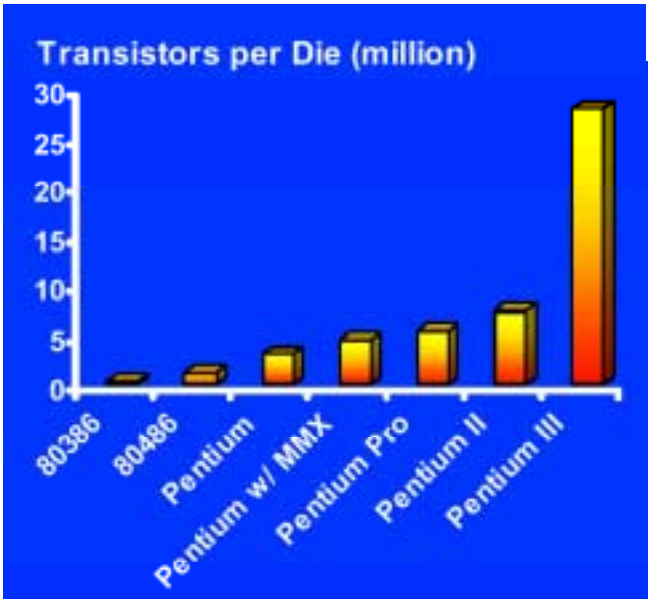

Figure. 1.1. Total number of transistors in the microprocessors has increased exponentially (Source: Intel Technology Symposium 2000, by Jerry Budelman).

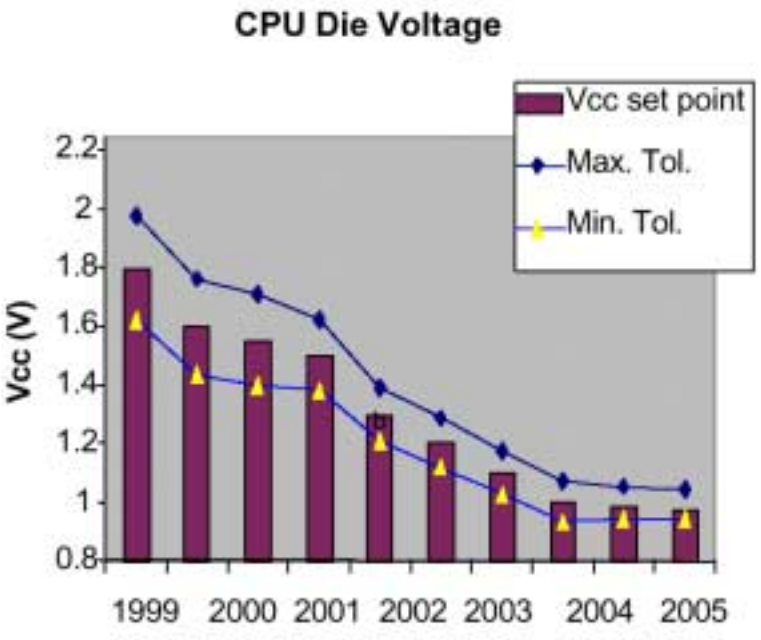

Figure 1.2. Microprocessor roadmap for supply voltages (Source: Intel Technology Symposium 2001, by Ed Stanford).

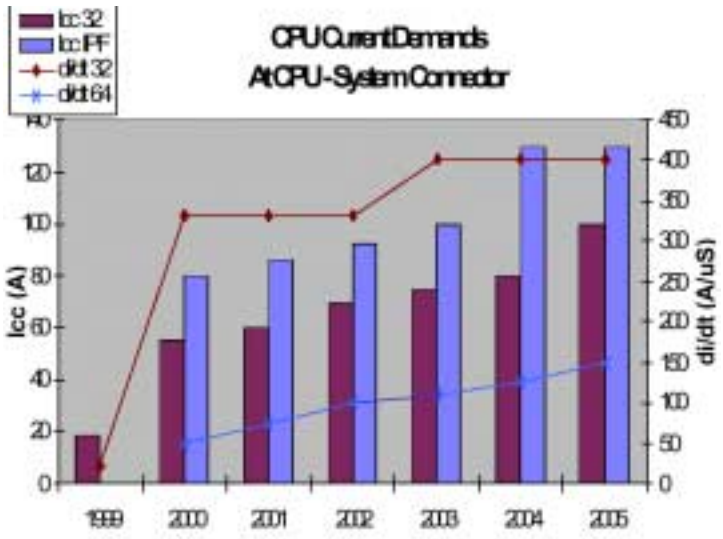

Figure 1.3. Microprocessor roadmap for current demands and transition slew rates (Source: Intel Technology Symposium 2001, by Ed Stanford).

For low-end computer systems, such as desktops, workstations and low-end servers, Figure 1.4's power delivery architecture is adopted. The silver box provides +5 V and +12 V, which feeds the disk drives and other devices as well as the VRMs. In close proximity to the CPU, the VRMs step down the voltage to the CPU.

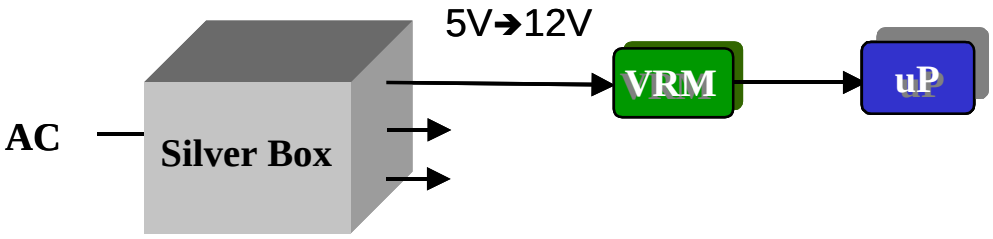

Figure 1.4. Power delivery architecture for low-end computer systems.

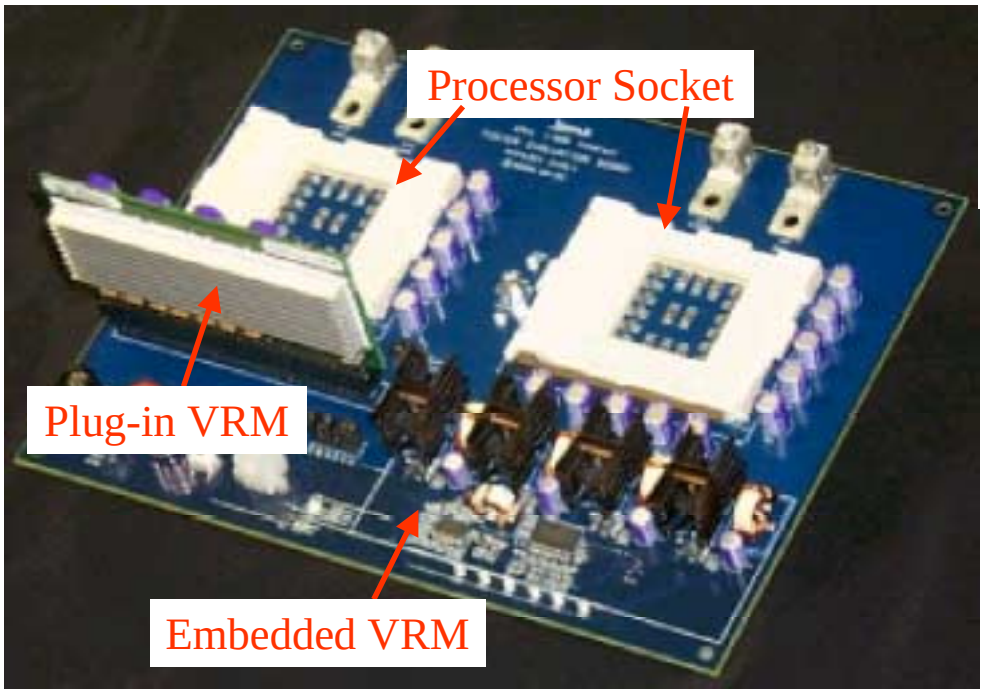

Figure 1.5. Plug-in VRM and embedded VRM [E2].

VRMs are either plugged into the sockets on the motherboard or are integrated directly onto the motherboard. Figure 1.5 shows both the plug-in VRM and the on-board VRM. The plug-in VRM is a power module that can be plugged into the socket on the motherboard. The on-board VRM, also called the VR-down (VRD), is built directly onto the motherboard. The benefit of plug-in VRMs is their exchangeability. The benefit of on-board VRMs is that they can eliminate the problematic and costly connector that comes with plug-in VRMs. Most of today's low-end computer systems use on-board VRMs.

For high-end computer systems with multi-processors, such as high-end servers, the distributed power architecture is often used, as shown in Figure 1.6. The paralleled front-end converters provide a single DC distribution bus around the system, which is often +48 V and which feeds VRMs and other DC/DC converters. Each processor has its own VRM in close proximity. Figure 1.6 shows the four-processor server system from Intel [E3]. The VRM, also called the Power POD, is directly connected to the processor through power tabs.

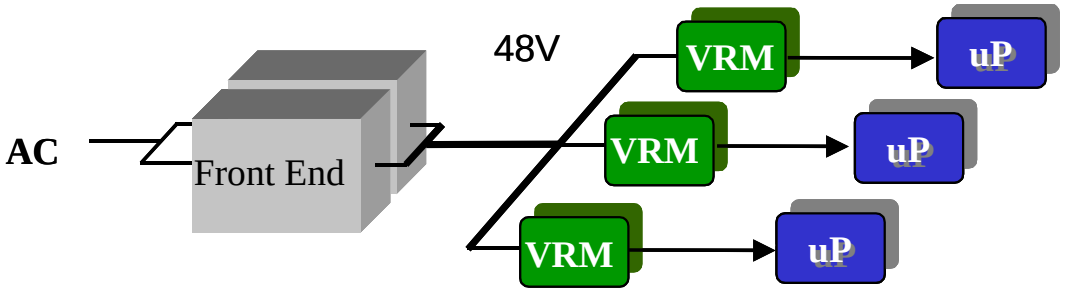

Figure 1.6. Power delivery architecture for high-end computer systems.

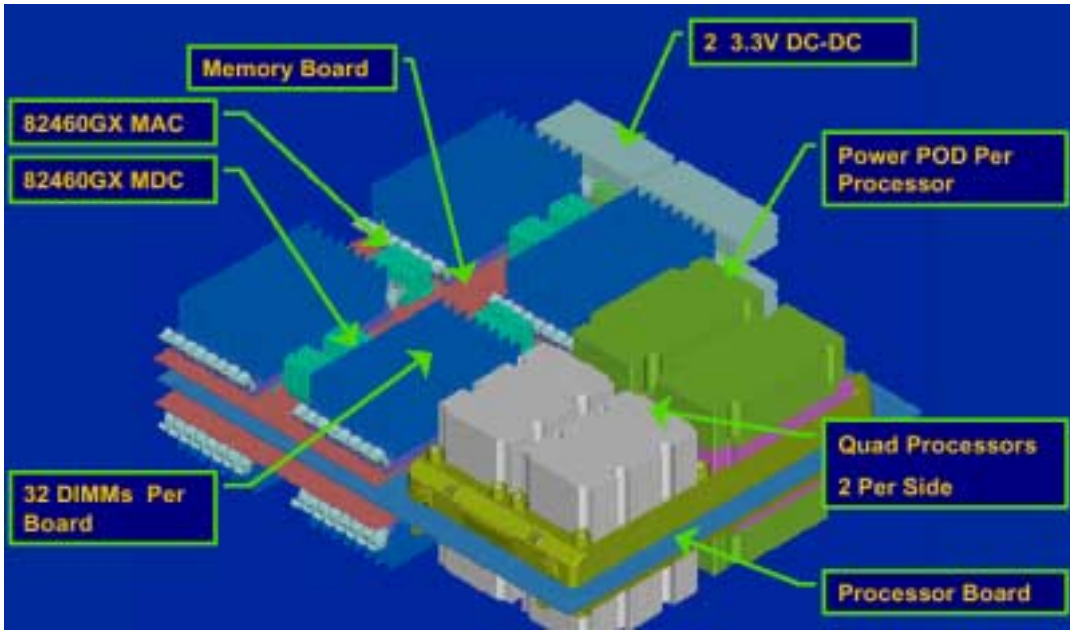

Figure 1.7. Power POD in Intel high-end servers [E3].

Although VRMs take a variety of forms for different computer systems, the fundamental requirements for VRMs are generally the same. The fast dynamic transients happen when the microprocessor chip operates from sleep mode to active mode and viceversa. The small transient voltage deviation under high currents and high slew rates is the most stringent requirement. As the operating voltage is reduced to below 1V, the transient voltage tolerance is also expected to decrease and to become much tighter. Because of the high cost of space in the motherboard, the power density and efficiency are also very important for VRMs. These performance requirements pose serious design challenges for the VRM design.

1.2. MULTIPHASE TECHNOLOGY

Earlier VRMs use a single conventional buck or synchronous buck topology for power conversion [A4, A5, A7]. They operate at a lower switching frequency with a higher filter inductance that limits the transient response [A32, A33, A35].

Figure 1.8 shows a single-phase VRM. The large output-filter inductance limits the energy transfer speed. In order to meet the microprocessor requirements, huge output-filter capacitors and decoupling capacitors are needed to reduce the voltage spike during the transient.

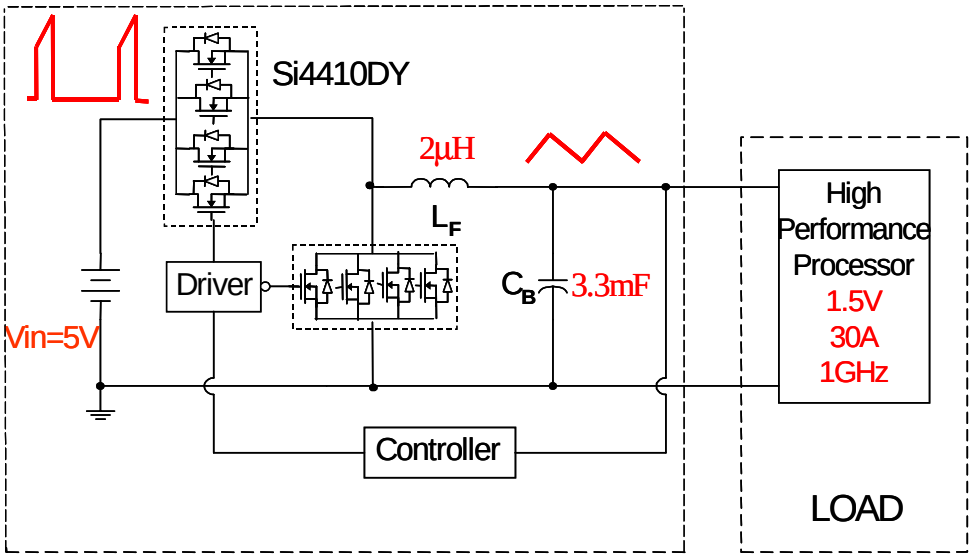

Figure 1.8. Single-phase VRM.

In order to reduce the VRM output capacitance, a large inductor current slew rate is preferred. Smaller inductances give larger inductor current slew rates; therefore, a smaller VRM output capacitance can be used to meet the transient requirements. In order to

greatly increase the transient inductor current slew rate, the inductances need to be reduced significantly, as compared with those in conventional designs.

However, small inductances result in large current ripples in the circuit's steady-state operation. The large current ripples generate large steady-state voltage ripples at the VRM output capacitors. The steady-state output voltage ripples can be so large that they are comparable to transient voltage spikes. It is impractical for the converter to work this way.

In 1997, VPEC (CPES) proposed using interleaving technology to solve the large current ripples in quasi-square-wave (QSW) VRMs [A12, A13, A15, A19]. Interleaving greatly reduces the current ripples to the output capacitors, which in turn greatly reduces the steady-state output voltage ripples, making it possible to use very small inductances in VRMs to improve transient responses. Interleaving VRMs with small inductances reduces both the steady-state voltage ripples and the transient voltage spikes, so that a much smaller output capacitance can be used to meet the steady-state and transient voltage requirements. The power density can be significantly improved. Moreover, interleaving makes the thermal dissipation more evenly distributed. Studies show that in high-current applications, the overall cost of the converter can be reduced using this technology. The concept of applying interleaving to VRMs is so successful that it has become the standard practice in VRM industry.

The topology of a multiphase buck converter is shown in Figure 1.9. It consists of n identical converters with interconnected inputs and outputs. The duty cycles of adjacent channels have a phase shift of $\frac{360^o}{Nc}$, where Nc is the total channel number.

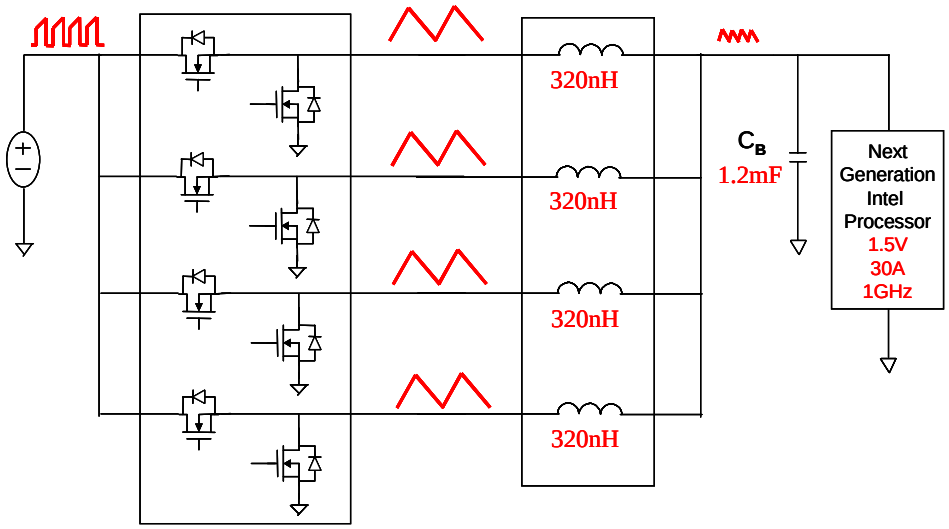

Figure 1.9. Multiphase VRM.

The main benefit of multiphase technology is the ripple cancellation effect, which enables the use of small inductances to both improve transient responses and minimize the output capacitance.

Multiphase converters interleave the inductor currents in individual channels, and therefore, greatly reduce the total current ripple flowing into the output capacitors. With the current ripple reduction, the output voltage ripples are greatly reduced, which enables the use of very small inductances to improve the transient response, and therefore, a small output capacitance can be used to meet the transient requirements. The reduced output

voltage ripple also allows more room for voltage variations during the load transient because the voltage ripple will consume a smaller portion of the total voltage tolerance budget. Consequently, the multiphase converter helps improve the load transient performance and minimize the output capacitance.

In multiphase converters, the current ripple cancellation effect can be defined as the ratio of the magnitudes of output current ripple and inductor current ripple. Figure 1.10 shows the ripple reduction effect as a function of duty cycle.

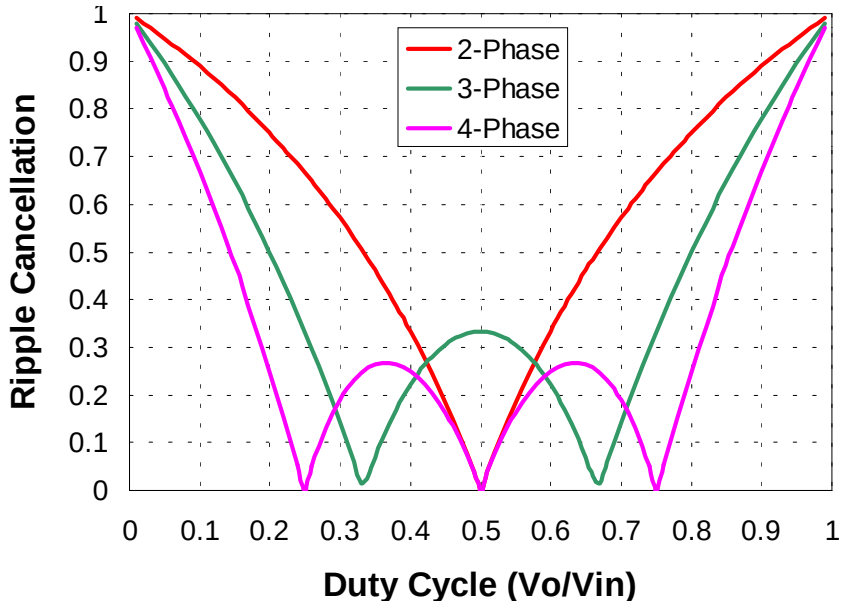

Figure 1.10. Current ripple cancellation in multiphase VRMs.

The benefits of the multiphase approach can be summarized as follows. This approach allows a small output inductance to be used in order to increase the energy transfer speed. This small inductance makes the VRM transient response much faster. The interleaving approach can reduce the ripple current and increase the ripple frequency,

which makes it possible in order to reduce the output capacitance to improve the transient response, as well as to increase the VRM efficiency. The interleaving techniques also make it possible to parallel the output inductors of the individual modules during the transient. Therefore, the effective output inductance can be further reduced in order to improve the transient response. Other benefits of interleaving include better thermal management and better mechanical performance.

Recently, multiphase converters have been widely used for 12V-input VRMs as a standard practice [A16, A39, E3]. The interleaving technique has also been investigated as a possible way to improve power density and transient response for 48V-input VRMs [B22, B42]. Correspondingly, many semiconductor companies, such as Intersil, Semitech, National Semiconductor, On Semiconductor, Analog Devices and Voltera, have produced dedicated control chips for multiphase VRMs.

1.3. STATE-OF-THE-ART VRM DESIGN

1.3.1. 12V-Input VRM

Today's 12V-input VRMs are almost universally based on the multiphase synchronous buck converter, as shown in Figure 1.11. They consist of N_C identical converters with interconnected inputs and outputs. The duty cycles of adjacent channels have phase shifts of $360/N_C$ degrees. Table 1.1 lists some commercial designs for the latest Pentium 4® microprocessors.

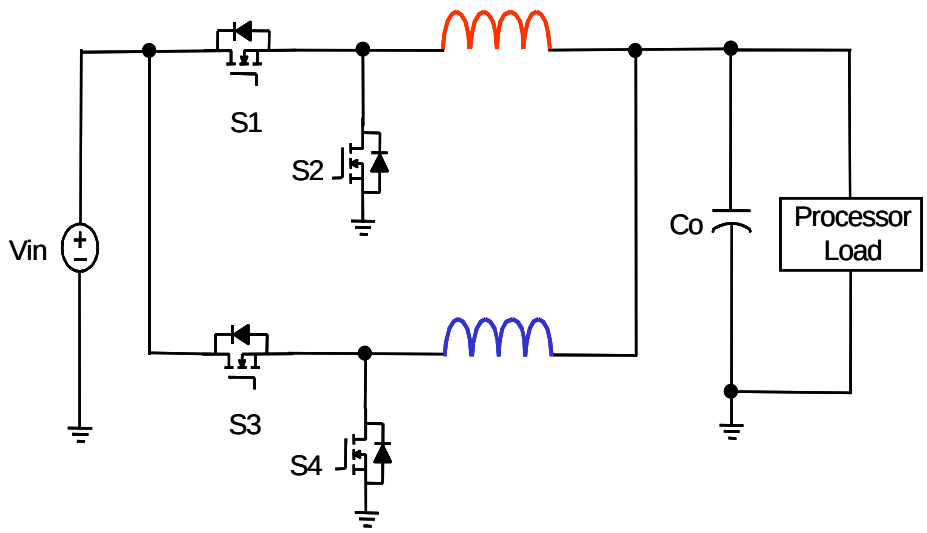

Figure 1.11. Multiphase buck converter (two-phase as an example).

Table 1.1. State-of-the-Art 12V VRM Design.

	Channel Number	Switching Freq. (kHz)	Inductance Per Channel (nH)	Output Bulk Capacitor
ADI	2	200	600	8x1200uF (OSCON)
Intersil	3	200	850	6x1000uF (OSCON)
On-Semi	3	250	500	14x1200uF (Aluminum)
Semtech	4	250	600	6x820uF (OSCON)
Voltera	10	800	200	20~40x22uF(Ceramic)

For 12V VRMs, the multiphase buck converter runs at a very small duty cycle. With a very small duty cycle, the current ripple reduction is very little, as shown in Figure 1.10. Therefore, the benefit of multiphase converters for improving the transient response is compromised. The small duty cycle also impairs the efficiency of the multiphase buck converter. Experimental results show that the efficiency of the 12V VRM is about 6%

lower than that of the 5V VRM. The measurement is based on the same four-phase buck VRM [A51].

Many output inductors are required in the multiphase buck converter. Integrated magnetic components can reduce the flux ripple in the center leg of the core. As a result, the core loss can be reduced and the overall efficiency can be improved. It has been demonstrated that 1% to 2% efficiency improvement can be achieved by using integrated inductors [C19, C24]. By using properly designed coupling inductors, one can further reduce the steady-state current ripple while maintaining the same transient response [C21, C22, C27]. The efficiency of the converter can be improved by an additional 3% [C21, C22].

As listed in Table 1.1, all the designs are focused on the same VRM 9.0 specifications for the latest Pentium 4® microprocessors, but the selection of channel number is quite different. The minimum phase is two, and the maximum channel number is ten. Most of them are around three to four. Obviously, all of them can meet the design requirements, but their size and cost are different.

A great amount of work has gone into analyzing and designing the synchronous buck VRM. The main focus was to optimize the devices [A27-A31], the output filter [A39-A47], and the input filter [A48].

Device optimization is more important in the 12V-input VRM. In the top MOSFET, the switching and gate drive losses are much larger than the conduction loss. The bottom

MOSFET conducts the load current most of the time. The conduction loss is a major concern. A device with low gate charge is suitable for the top switch, while a device with low on-resistance is suitable for the bottom switch. The commercially available low voltage power devices are currently constructed based on the vertical trench technology, and most of them are rated at 30 V [A27, A28, A29]. Because of these devices' large figures of merit (FOM), defined as the product of the on-resistance multiplied by the gate charge (R_{ON} x Q_G), most of today's VRMs run at about 300 kHz switching frequency. Low-voltage lateral devices can offer much smaller FOM [A27, A28]. Some semiconductor companies, such as Voltera, have come out with such devices, which allow the VRM to run at a MHz-level switching frequency. This is promising technology for future multi-MHz VRMs.

For a certain power device technique, die size can be optimized to improve the efficiency. The on-resistance of the MOSFET, which is related to the conduction loss, is inversely proportional to the die size. The charge of the MOSFET, which is related to the switching and gate driver loss, is directly proportional to the die size. Die size optimization is basically a tradeoff between the conduction loss and the switching and gate drive losses.

The most effective way to reduce the transient voltage spikes is to reduce the output inductance of the VRM. The concept behind the QSW is to greatly increase the inductor slew rate by reducing the output inductance of the VRM. Experimental results show that the multi-phase QSW buck VRM can achieve 5X faster transient response, 6X better

power density, 10X smaller inductance, and 6X smaller capacitance compared with the conventional VRM [A17, A19]. However, the large ripple current caused by the smaller output inductor in the QSW increases the conduction losses of the devices and the inductor windings.

Studies also show that the transient response is not only determined by the output inductance but also by the control loop bandwidth [A40]. Higher control loop bandwidth results in faster current response. For a fixed control bandwidth, reducing output inductance cannot further increase the VRM output current slew rate. There exists a critical inductance value for a certain bandwidth [C30]. If the VRM output inductance is smaller than the critical inductance value, the transient response will remain unchanged. If the VRM output inductance is larger than the critical inductance, the transient response will slow down as the output inductance increases. The critical inductance helps to reduce the conduction and switching losses and, therefore improves the efficiency, while maintaining the same transient response.

1.3.2. 48V-Input VRM

High efficiency and high power density are the general requirements for 48V-input VRMs. Because of similar input and output specifications, substantial research efforts made for low-voltage DC/DC converters can be extended to 48V VRMs.

Synchronous rectification with specifically designed low-voltage MOSFETs is widely used to dramatically improve the efficiency of low-voltage DC/DC converters [B15-B30]. For 48V VRM, synchronous rectification technology is a must.

The active-clamped forward converter has become the prevailing topology in low-voltage DC/DC converter applications because it recovers the magnetizing energy of the transformer and minimizes the voltage and current stresses of the primary switches as well as those of the rectifiers [B1, B2, B3, B4]. However, this topology is a fourth-order system. For 48V VRMs, it is difficult to achieve a higher bandwidth design to improve transient responses [B36, B40].

Recent research proves that the symmetrical half-bridge topology with the synchronous rectifier is a suitable approach for this application [B34, B41]. Major power supply vendors such as Delta and Celestica have already used this technology in their latest 48V VRM designs.

In 1998, VPEC (CPES) proposed a novel push-pull forward topology for 48V VRMs, as shown in Figure 1.16. It has an improved transient response, improved efficiency, and increased package density. This topology is essentially a modified push-pull converter topology with a clamp capacitor. One can clamp the voltage overshoot and recover the leakage energy. This topology also provides a reduced input current ripple and requires a smaller input filter. Experimental results show that the push-pull forward topology can demonstrate 3% better efficiency compared to either a symmetrical or an asymmetrical half-bridge converter [A15, B36].

The secondary-side power losses have a major impact on efficiency for low-voltage and high-current applications. They can be reduced by the proper selection of secondary-side topologies. Because of its simpler transformer structure and two-times-lower inductor currents and transformer secondary currents, the current-doubler topology can offer lower conduction losses than the conventional center-tapped topology [B9-B14]. Besides the efficiency, the transient response is another major concern for VRMs. The transient response can be improved by reducing the output filter inductance. With the current doubler running in QSW mode, fast transient response can be obtained. Due to the ripple cancellation in the current-doubler rectifier, the large current ripple caused by the small output inductances can be canceled at the VRM output.

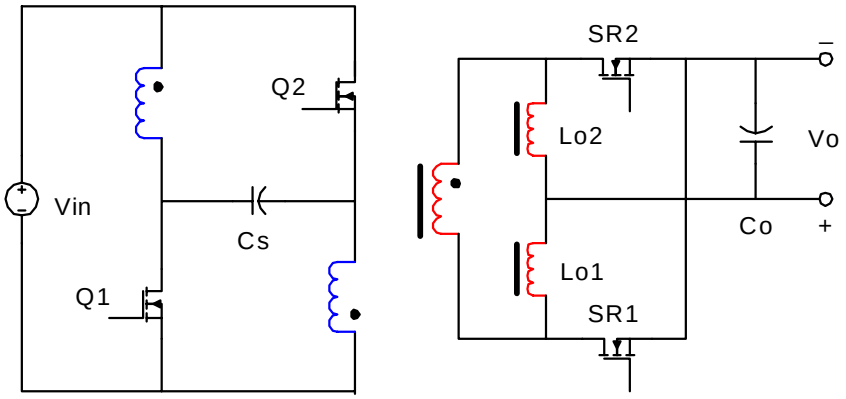

Figure 1.12. Push-pull forward converter with current-doubler rectifier.

To achieve high efficiency and high power density in 48V VRMs, the magnetic design is also a key issue. The magnetic-related effects, including core loss, winding loss and leakage inductance, become more severe at high frequencies. Another advantage of the current-doubler rectifier is that all its magnetic components can be integrated into a

single core [C15, C16, C18, C19]. It is possible to further improve the efficiency and cut the cost and size. Figure 1.13 show the integrated magnetics for the current-doubler topology, in which the windings are wound around the center leg and the air gaps are placed on the two outer legs. Both core and winding integration are realized in this structure. Only two high-current windings and three high-current interconnections are needed, resulting in lower interconnection loss and lower conduction loss. As a result, this integrated magnetic structure allows for lower overall system cost and size, as well as higher efficiency [C19].

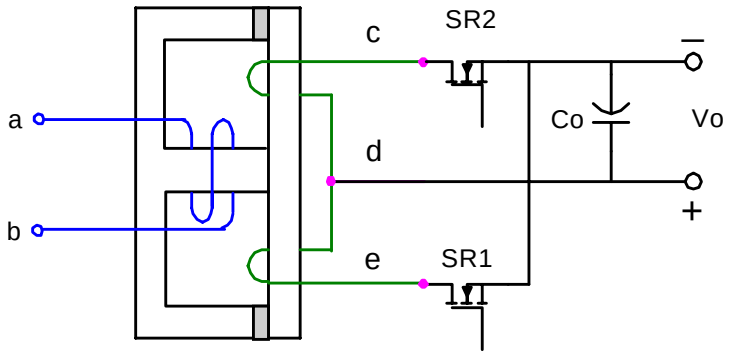

Figure 1.13. Integrated magnetics for the current-doubler rectifier.

Despite all its advantages, the integrated magnetics have not been successfully used for the current-doubler rectifier in commercial products. Some issues must be addressed. The core structure requires precise adjustment and is not mechanically stable. This makes mass production difficult and costly. The existence of air gaps on the two outer legs also causes electromagnetic interference (EMI) issues. A significant level of leakage exists in

the integrated magnetics, causing severe parasitic ringing, decreasing the duty cycle, and impairing the efficiency [B37].

1.4. TECHNICAL CHALLENGES FOR VRM DESIGN

As discussed in Section 1.1, power management-related issues become much more critical for future microprocessors and much more difficult to handle. To meet future specifications, high-efficiency, high-power-density, fast-transient VRMs are required. To achieve this target, the following technology challenges should be addressed.

1. Advanced VRM topologies: high efficiency, high power density and fast transient response for low-voltage, high-current applications.

2. Efficient synchronous rectification: new driving means or topologies to eliminate the body diode loss for high-frequency operation.

3. Innovative integrated magnetics: low core loss, low winding loss and easy manufacturability for high efficiency and high power density.

4. Advanced power devices: using lateral power devices for low-voltage, high-current, high-frequency applications instead of the-state-of-art vertical power devices.

5. Optimization of multiphase VRM: a methodology for determining the appropriate number of channels and value of output inductance for the optimal design of multiphase VRMs.

6. Advanced packaging technology: minimizing parasitics for high-frequency operation.

The first, third and fifth preceding challenges have been addressed in this dissertation. The primary objectives of this dissertation are to develop advanced topologies and innovative integrated magnetics for high-efficiency, high-power-density, fast-transient VRMs. The optimization of multiphase VRMs has also been discussed.

1.5. DISSERTATION OUTLINE

This dissertation consists of five chapters. They are organized as follows.

Chapter 1 is the background review of existing VRM technologies and the technical challenges for VRM designs. In order to improve the transient response, small inductances must be used. The ripple cancellation in the multiphase converter makes it possible to use very small inductances in VRMs. Multiphase converters have become the standard practice for 12V VRMs in industry. Today's multiphase VRMs are almost universally based on the synchronous buck topology. A great amount of work has gone toward analyzing and designing the synchronous buck VRM. Integrated inductors are

used to improve the efficiency of multiphase buck converters. The 48V VRMs are often based on isolation topologies using the current doubler and synchronous rectifier. Magnetic design is the key issue for 48V VRMs to achieve high levels of efficiency and power density. The technical challenges for VRM design can be summarized as advanced VRM topologies, efficient synchronous rectification, innovative integrated magnetics, advanced power devices, multiphase optimization and advanced packaging technology. The primary objectives of this dissertation are to develop advanced topologies and innovative integrated magnetics for high-efficiency, high-power-density, fast-transient VRMs. The optimization of multiphase VRMs has also been discussed.

Chapter 2 explores suitable multiphase topologies for VRMs with large step-down conversions, such as from 12 V to 1.5 V. Currently, the multiphase buck converter is the most popular topology for such applications. With increased input voltages and decreased output voltage, the multiphase buck converter suffers from a very small duty cycle. It is very difficult for the multiphase buck converter to achieve a desirable efficiency while providing a fast transient. The loss analysis shows that its efficiency drop is mainly caused by the switching losses of the top switches when the duty cycle is reduced.

In order to improve the efficiency without compromising the transient performance, the multiphase tapped-inductor buck converter is investigated, which employs multi-winding coupled inductors to extend the duty cycle. Under the same transients, the multiphase tapped-inductor converter has a much larger steady-state duty cycle, and therefore it can offer a higher efficiency than the multiphase buck converter. However,

the multiphase tapped-inductor buck converter suffers from a voltage spike problem caused by the leakage inductance between the coupled windings.

An improved topology, named the multiphase coupled-buck converter, is proposed. This topology enables the use of a larger duty cycle with a clamped and coupled structure. Therefore, the leakage energy can be recovered and the voltage spike across the device can be clamped. With the extension of the duty cycle, the multiphase coupled-buck converter has switching losses for the top switches that are significantly lower than those of the multiphase buck converter. Both analyses and experiments demonstrate that the multiphase coupled-buck converter can offer an efficiency that is significantly better than the conventional buck converter that uses a very small duty cycle under the same transients.

The proposed concept in the multiphase coupled-buck converter can be extended to other applications. The isolated counterpart of the multiphase coupled-buck converter is the push-pull forward converter with the current-doubler rectifier. Correspondingly, the benefits of the multiphase coupled-buck converter can also be extended. Compared to the isolated counterpart of the multiphase buck converter that is the push-pull converter, the push-pull forward converter has clamped device voltage and recovery leakage, and therefore a higher efficiency.

Chapter 3 discusses the use of integrated magnetic techniques in multiphase VRMs in order to reduce the number of the magnetics, and to improve the efficiency. All the

magnetic components can be integrated into a single core, in which the windings are wound around the center leg and the air gaps are placed on the two outer legs. However, the core structure of the integrated magnetics requires precise adjustment and is not mechanically stable. The existence of air gaps on the two outer legs also causes EMI issues. A large amount of leakage inductance exists in the integrated magnetics, causing severe parasitic ringing, decreasing the duty cycle, and impairing the efficiency.

This chapter proposes a novel integrated magnetics solution to solve these problems. In the proposed structure, all the windings are wound on the two outer legs, the core structure has an air gap in the center leg, and there are no air gaps in the two outer legs. This kind of core is easier to manufacture. The windings are physically located on the same legs. The interleaved winding technique can be used to minimize the leakage inductance.

In the proposed integrated magnetics, the air gap in the center leg introduces inverse coupling between the two output filter inductors. With the inversely coupled output inductors, both the steady-state and dynamic performances of the converter can be improved. Another benefit of the proposed structure is the flux ripple cancellation effect in the center leg. With the small flux ripples in the center leg, the core loss can be reduced. Because only the center leg has an air gap and the flux ripples are cancelled in the center leg, the fringe effect of the air gap becomes insignificant and the winding loss can also be reduced.

Unlike conventional magnetic integrations, the proposed solution also considers the integration of the input filter. In the proposed integrated magnetic structure, the input inductor is formed by the leakage inductance between the transformer's primary windings. This leakage can be controlled by proper winding design. With the proposed integrated magnetics, it is possible to use only a single magnetic core for the whole converter.

Chapter 4 proposes an optimization methodology for multiphase VRMs in order to determine the appropriate number of channels for an optimal design.

The problem formulation for the optimization is discussed. Two constraints exist, corresponding to the requirements of the transient responses and the minimum efficiency. Four design variables need to be traded off; they are the channel number, switching frequency, control bandwidth and output inductance. The selection of the objective function depends on the preference of individual manufacturers or designers. Minimized weighted volume and cost could be the objective function for most of today's multiphase VRMs.

The general method of optimization is proposed. As a dependent variable, the control bandwidth is eliminated from the four design variables. The optimization problem can be illustrated by a series of surfaces in a three-dimensional space, with the objective function as the vertical axis, the switching frequency and the output inductance as two horizontal axes, and the channel number as the parameter. The proposed optimization method first looks for the lowest points of these surfaces, which represent the optimal designs for the

given channel numbers. For most of today's multiphase designs, these lowest points correspond to the design of the minimum efficiency and the critical inductance. Connecting these lowest points together forms a curve, and the optimization solution is located at the lowest point of this curve.

Two examples are performed step by step to demonstrate the proposed optimization methodology. Both are targeted on typical VRM 9.0 designs for the latest Pentium 4® microprocessors and their results are compared with the industry practice. The first example has a simple objective function, to minimize the number of output capacitors. A more realistic objective function is used for the second example, to minimize the cost of multiphase VRMs. The optimization results provide not only the appropriate channel number, but also the complete design, including the output inductance value, the switching frequency and total number of input and output capacitors required. The more generalized formulation has been discussed. Its objective function could be to minimize the weighted volume and cost of multiphase VRMs.

Chapter 5 summarizes the work and proposes some ideas for future work.