Chapter 1. Introduction

1.1 Background

One of the most active research and development areas in the power electronics field is variable speed drives (VSDs). As power semiconductor devices become cheaper, faster and more reliable, the use of energy saving VSDs in industry and residential applications has been increasing. VSDs utilizing induction and dc motors make up the majority of industrial and domestic drives. Although these VSDs require an initial investment and generate current harmonics, they provide significant improvements in performance such as better control, wider speed ranges, soft start, and enormous energy savings in various kinds of applications. The selection of VSDs is an application-specific matter. There are many factors to be considered when we select VSD systems, including cost, output torque, speed ranges, performance, and power ratings.

There have been tremendous development efforts of various kinds of brushless motor drives over the past decades [1-17]. These are induction motor (IM), permanent magnet brushless dc motor (PMBDC), permanent magnet synchronous motor (PMSM) and switched reluctance motor (SRM) based drives. The use of PMBDC drives is increasing for three reasons. The first reason is the improving performance of drive electronics. The other reasons are the cost reduction of rare earth permanent magnet materials and a huge investment in manufacturing facilities. The SRM is the newest among the brushless motor family, although its concept was announced more than one hundred years ago [13]. SRM drives are not widely available in the motor drive market in these days, but this motor has been studied and developed since the late '70s. It has no windings or magnets on the rotor, thus it can be mass produced at the lowest cost compared to other motor types. Furthermore, the SRM has the additional advantages of low inertia, minimal losses on the rotor and mechanical robustness, which allows it to be driven at high speeds. The stator windings are concentrated, making it easier to wind compared to ac or dc machines. But despite its simple appearance, it is more difficult to design due to its nonlinearity [2, 9].

The increasing interest today is to find compact and inexpensive VSDs to meet the continuing demands of high volume, low cost, and low performance applications such as fans, pumps, process drives, appliance drives and many others in the range of fractional to one horsepower ratings. All off-line VSDs have rectifiers and storage capacitors in their front-end to get dc voltage from an ac power source. This input circuitry lowers the power factor (PF) of the VSD systems and pollutes ac power systems. The PF is the ratio of real power in watt to apparent power in volt-ampere (VA). When the input ac current and voltage are sinusoidal and in phase, the power factor is unity. In off-line VSD systems, the input current is distorted and out of phase with the input voltage. In this case, the power factor is less than unity and less real power is transmitted to the load. However, the rms input current is increased, due to the harmonic currents. Plus, the current required by the load must still be carried, requiring the wiring of the ac power system to be heavier and more expensive than necessary [37, 38, 46]. The most common problem that disturbs ac power systems is caused by electric motors operating in industries. The inductive component of the motors causes the ac current to lag the ac voltage. This results in a low power factor. Assuming loads are linear, the power factor can be corrected to near unity by connecting a bank of capacitors across the ac power line. Low power factor gives rise to a

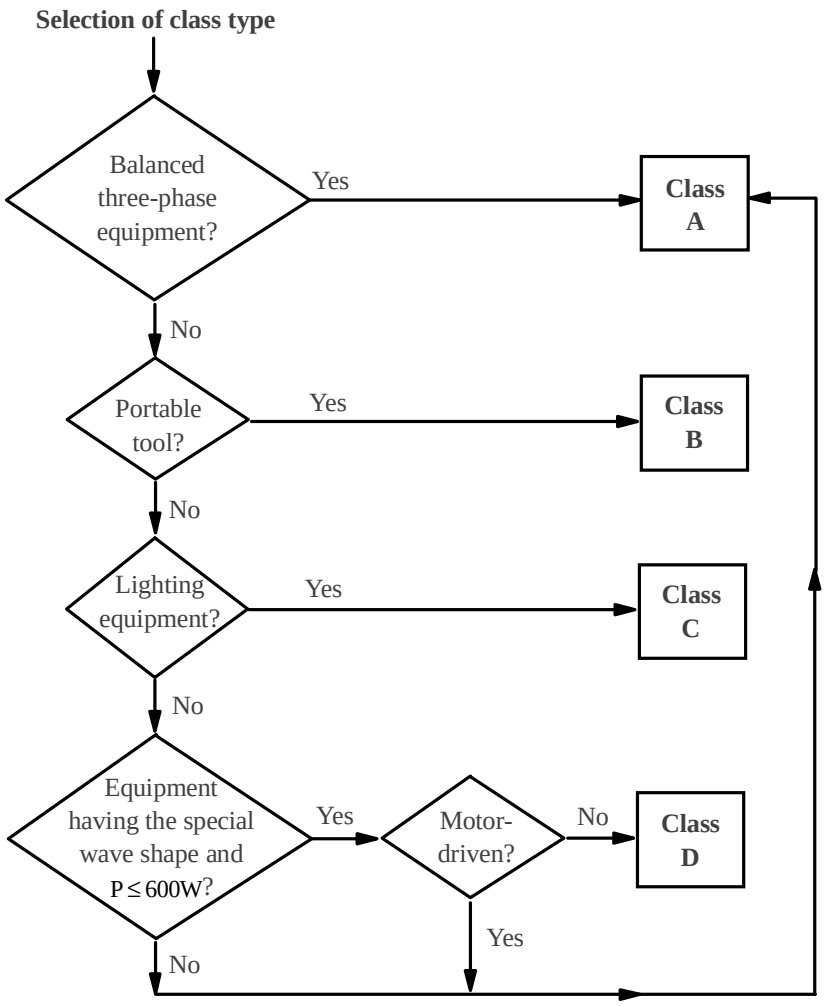
number of serious problems in VSD systems. The size of the input fuses and circuit breakers of the input circuitry must be increased. The distorted current waveform, which causes interference with other equipment, must be filtered to reduce magnitudes of harmonic frequencies. Consequently, to increase the output power from ac power systems, it is necessary to correct the power factor. This substantially reduces peak and rms input current and makes it possible to achieve higher output power.

With the proliferation of nonlinear loads, such as switched mode power converters, standards agencies around the world are developing requirements for harmonic contents of electronic power conversion systems to reduce the overall distortion on main supply lines. One standard is IEC 1000-3-2 (published in 1995) (latest version of IEC 555-2 / 1982) [24] from the International Electrotechnical Commission (IEC). This standard limits for input harmonic currents in electrical equipment, such as heating, ventilating, and air conditioning (HVAC) equipment, blenders, washing machines, electrical power tools, cookers, etc. The standard describes general requirements for testing equipment, as well as the limits and the practical implementations of the test. For the purpose of harmonic current limitation, the standard divides electrical equipment into four classes, shown in Figure 1.1. Each class has different harmonic current limit. Balanced three-phase equipment and other electronic apparatus, excluded from the other three classes, are included in the Class A classification. To apply Class D limit, the following two requirements should be satisfied:

(i) Input power should be less than 600W, and
(ii) Input current waveshape of each half cycle is within the envelope shown in Figure 1.2 for at least 95% of the duration of each half period.

The center line in Figure 1.2 coincides with the peak value of the input current. The second requirement implies that waveforms having a small peak outside the envelope is considered to fall within the envelope. For equipment with input power greater than 75W, relative limits (mA/W) are applied. The specified limits of the IEC 1000-3-2 standards are applicable to electrical equipment having an input current up to 16A per phase, nominal voltages of 230V at 50Hz single-phase, and harmonic currents from the 2^{nd} to the 40^{th} harmonic.

Appliance VSDs fall into the Class A or D category depending on whether they use a phase-angle controlled VSD or not, and if their input power range is less than or greater than 600W. The VSDs investigated in this study have a front-end rectifier circuit to convert ac voltage into dc voltage. The ac input current of these VSDs, have a pulse type waveform, which falls into Class D envelope regardless of the magnitude of its input power. This is because the pulse current is normalized based on its peak value. This relationship shown in Figure 1.3, is obtained by PSpice simulation of a single-phase diode rectifier circuit is normalized to the peak value. If the input power of a VSD is over 600W, Class A limit is applied. Otherwise Class D limit is applied. Therefore, in this study, only the Class A and D limits are employed to verify the effects of PFC according to the IEC 1000-3-2 standard shown in Table 1.1. Even though this standard does not directly fit into the 120V system, the permissible harmonic current limit for the 120V system is obtained by multiplying the limits for the 230V system by a scaling factor of 1.92 [36]. It is employed as a reference for the 120V system, and used to compare the magnitudes of the input current harmonic components in this study. To validate the scaling on harmonic current limits, a typical comparison example of the magnitude of the input current harmonics of a single-phase



Note. Motor-driven: Phase Angle Controlled

Figure 1.1 Flowchart for class determination of electrical equipments by IEC 1000-3-2 standard.

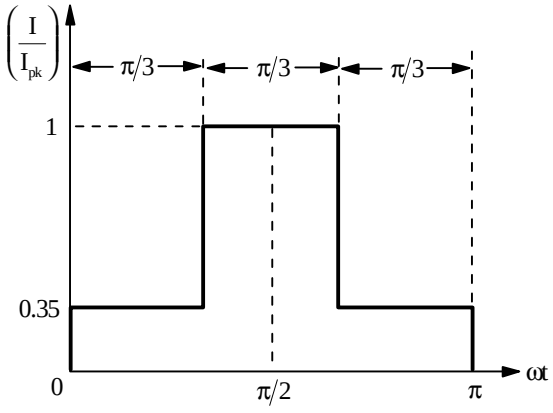


Figure 1.2 Class D waveform envelope.

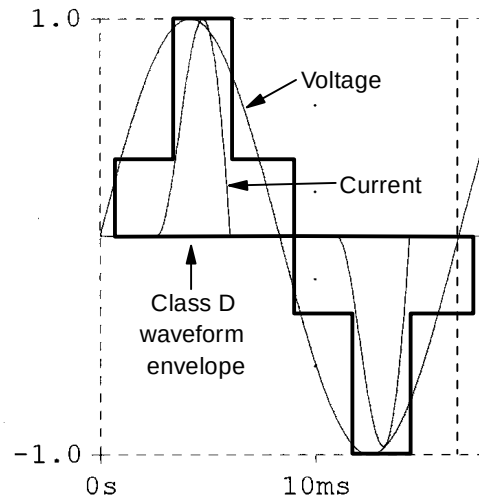


Figure 1.3 Application of the Class D waveform envelope
to input current of a single-phase diode rectifier circuit.

Table 1.1
Original harmonic current limits for Class A and D equipments
by IEC 1000-3-2 standard.

Harmonic order (n)	**Class A**	**Class D**	
	Absolute limit (P > 600W)	Relative limit (600W ≥ P > 75W)	Absolute limit (600W ≥ P > 75W)
	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
Odd Harmonics			
3	2.30	3.4	2.30
5	1.14	1.9	1.14
7	0.77	1.0	0.77
9	0.40	0.5	0.40
11	0.33	0.35	0.33
13	0.21	Use following equations	
15 ≤ n ≤ 39 (Class A)	2.25/n		
13 ≤ n ≤ 39 (Class D)		3.85/n	2.25/n
Even Harmonics			
2	1.08	Not Applicable	
4	0.43		
6	0.30		
8 ≤ n ≤ 40 (Class A)	1.84/n		

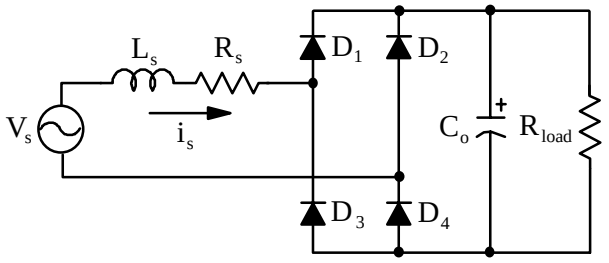


Figure 1.4 A single-phase diode rectifier circuit with capacitor.

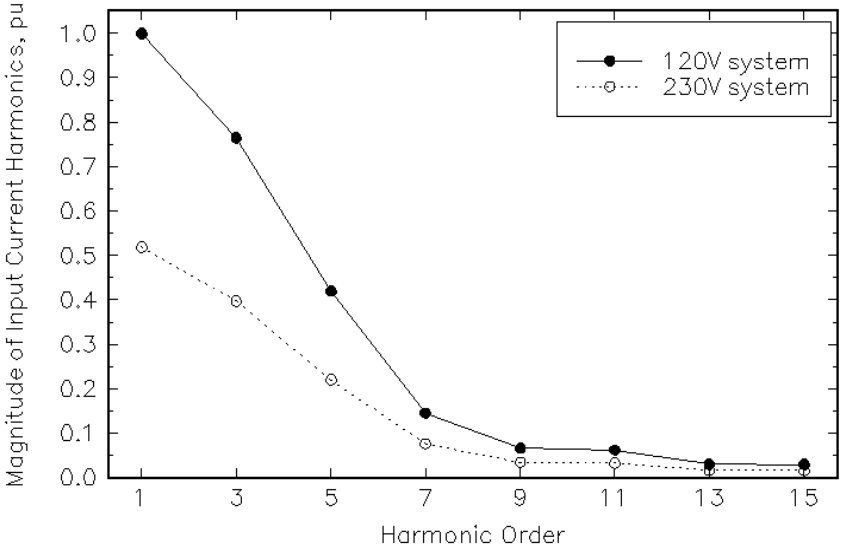


Figure 1.5 Comparison of the input current harmonic magnitudes with two different input voltages.

diode rectifier circuit shown in Figure 1.4 with two different input voltages is illustrated in Figure 1.5. These values are obtained by PSpice simulation of a full-bridge diode rectifier circuit with 120V and 230V ac input voltages having identical load. The magnitude of the input current harmonic is normalized to the fundamental input current component with a 120V source voltage since it has the highest magnitude. Figure 1.5 shows the overall input harmonic current magnitudes of the 120V input voltage is approximately 1.92 times bigger than one with 230V. Table 1.2 shows the modified IEC 1000-3-2 harmonic current limit for the 120V system. The even harmonics are not considered because of the single-phase full-wave bridge rectifier generates only odd harmonic currents [23]. Table 1.2 is utilized as a reference to compare the magnitudes of harmonic components in the input current of various VSD systems with and without the PFC preregulator. Although IEC 1000-3-2 standard has different designations, such as EN 61000-3-2 for the European Union published by CENELEC (Comité Européen de Normalization Electrotechnique) and BSEN 61000-3-2 for the United Kingdom, those versions have the same IEC standard. Another important standard is the IEEE Std 519-1992 - IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems

(revision of IEEE Std 519-1981) [25] which specifies the steady-state limitation in the harmonic current at the point of common coupling (PCC). This standard addresses the following two important facts.

(i) The customers are responsible for maintaining current distortion to within acceptable levels, while the utility companies are responsible for limiting voltage distortion.
(ii) The limits are only applicable at PCC between the utility and the customers.

Since appliance VSDs are not connected to the PCC, this standard is not utilized as a reference in this study. Instead, current limits proposed by the IEC 1000-3-2 standard are used to probe the results of the experimental harmonic measurements.

Table 1.2
Modified harmonic current limits for Class A and D
equipments with 120V power source.

Harmonic order (n)	**Class A**	**Class D**
	Absolute limit (P > 600W)	Relative limit (600W ≥ P > 75W)
	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)
3	4.42	6.53
5	2.19	3.65
7	1.48	1.92
9	0.77	0.96
11	0.63	0.67
13	0.40	Use following equation
15 ≤ n ≤ 39 (Class A)	4.35/n	
13 ≤ n ≤ 39 (Class D)		7.39/n

1.2 Overview of Previous Research

The summary of survey results on previous research related to PFC techniques and input PF corrected VSD systems is introduced in this section. Numerous single-phase PFC topologies are classified and various VSD systems with input PFCs are reviewed.

1.2.1 Single-Phase PFC Topologies

The study of PFC topologies is limited to single-phase systems since most appliance VSDs are powered by a single-phase utility source. The classification of single-phase off-line PFC topologies for VSDs is shown in Figure 1.6. Among these PFC topologies, low-frequency active, resonant, and isolated types are not considered in this study.

A passive PFC [36, 37] is more reliable than an active PFC because no active devices are utilized. However, it contains bulky capacitors and inductors operating at the line frequency, and it is sensitive to the line frequency, line voltage, and load. Therefore this method is not suitable for appliance drives.

The most popular active PFC method is the boost topology [38-41]. This topology is a universal solution from switch-mode power supply (SMPS) to small-motor drive applications. It has a smooth input current because an inductor is connected in series with the power source, showing a low level of conducted electromagnetic interference (EMI) noise. This topology has a high output voltage which is greater than the peak input voltage. The overload and start-up current cannot be controlled in this topology because there is no series switch between the input and output path. Also, isolation between input and output cannot be easily implemented.

The buck type PFC [42, 43] has a lower output voltage than input voltage, and it has a pulsating input current generating high harmonics onto the power line. This circuit is not practical for low-line input because it does not draw the input current when input voltage is lower than the output voltage. Therefore it has a relatively low power factor compared to the boost PFC circuit. The buck type PFC is suitable for charger applications due to its voltage step down nature.

The SEPIC (single-ended primary inductor converter) PFC [44] circuit has a single power switch driven at high frequency, as in the boost PFC topology. But it requires extra inductive and capacitive components for energy storage and transfer. The input current of the SEPIC is smoothed by employing an inductor in a series with the power source. This circuit is easily modified to the isolated version [50, 51].

A cascaded converter, which has a buck circuit in the front and boost circuit in the second stage, is introduced in [45]. The boost switch is turned on when the input voltage is below the output voltage. This causes the circuit to operate as a boost converter. When the input voltage is higher than the output voltage, the boost circuit stops and the buck circuit restarts. This converter

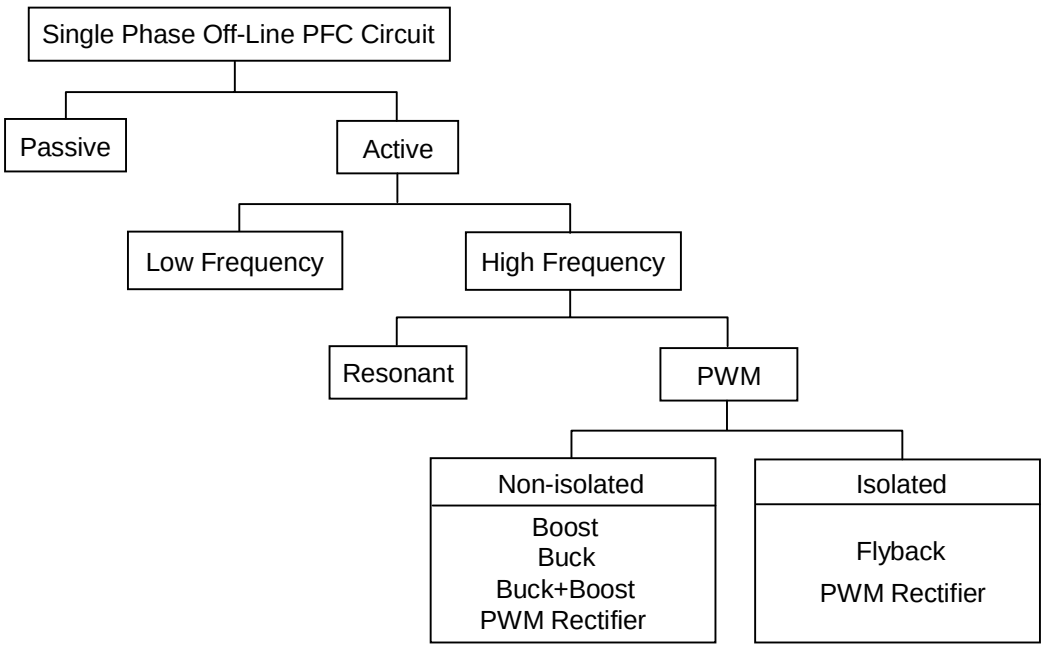


Figure 1.6 Classification of single-phase input PFC topologies for VSD systems.

can supply step-up or step-down outputs, allowing it to operate over a wide range of inputs. There is no inrush current due to the buck switch, which is in series with the power source. But it has a pulsating input current, which requires more filtering.

Another non-isolated PFC topology is the PWM rectifier [46, 47]. The topology in [46] can supply the step-up or step-down outputs like the buck-boost circuit. A full-bridge PWM recitifier in [47] provides the step-up output. The PWM rectifier circuit needs two [46] or four [47] power switches to achieve the unity power factor because it employs a half- or full-bridge configuration. It also needs more complicated control than the boost topology. But for high power applications, it may be a good candidate.

1.2.2 Input PF-Corrected VSD Systems

With Unidirectional Front-end PFC Preregulator

The endeavor to apply PFC circuits to converters for VSD systems focuses mainly on low harmonic pollution to power systems, low cost, and efficient implementation. There are several different approaches to improve the power factor and the input current harmonics of VSD systems [56-63]. These approaches employ a front-end converter for PFC and an inverter for the three-phase IM or a converter for PMBDC and SRM. These topologies may be classified into non-isolated and isolated type.

The boost topology with a high frequency inverter is introduced in [56, 57]. This circuit consists of a boost converter in the front-end, a full-bridge inverter isolated by a high frequency transformer, and a secondary rectifier circuit. The front-end boost converter corrects the power factor, and the inverter in the second stage provides high frequency ac voltage which is converted into dc output voltage. This multistage power conversion topology lowers the overall converter efficiency, and the requirement of additional hardware decreases the reliability of the converter. This topology is useful for applications requiring isolation between input and output, such as chargers for electric vehicles.

Chibani [54] and Rim [55] proposed high frequency inverters providing isolation by utilizing high frequency transformer-based ac to dc converters. Chibani's converter is a boost-derived topology where an inductor lies in a series with the input power source. It uses the boost mode and inverter mode operations to generate an amplitude modulated voltage. Rim's converter is not a boost derived one and needs bilateral power switches which may degrade the reliability and increase the complexity of the converter. This topology provides a wide range of dc output voltage. Both topologies are suitable for high frequency link UPS systems.

The non-isolated drive system employs a non-isolated boost PFC converter as an input to the PWM inverter as proposed in [56, 60, 62, 63]. It provides input PFC and high, stable, dc bus voltage, widening the field-weakening range in drive systems. The buck-boost cascaded converter based PWM inverter is proposed in [59]. The buck front end converter limits the input current to charge up the output capacitor smoothly and corrects the input power factor. The boost stage ensures inverter operation at low input voltages by a voltage step-up operation. The overall efficiency of the variable speed drive system with one of these multi-stage converters is relatively low compared with the single stage converter based drive system.

Isolated drive systems, which have a full-bridge PWM rectifier [57] and a half-bridge PWM rectifier [58], are proposed. A full-bridge PWM rectifier requires 10 power switches for a 1.5kW

input PFC and a three-phase inverter. A half-bridge topology needs only 6 switches for 3kVA PFC and a three-phase inverter. Both converters require complicated controllers to achieve high input power factors and inverter operations. A flyback PFC converter is proposed in [61]. This inverter combined with a step-down converter provides the PFC operation, electrical isolation, and controllable dc output. Its feasibility is demonstrated with a 400W IM drive system.

All of the above PF corrected VSD-related papers introduce only a basic attempt to improve input PF of the drive system. There is no variety of motor types, that is, most of the power factor corrected VSD study was accomplished with the IM. Also, the comprehensive analytical process in order to predict overall VSD system efficiency was not provided.

With Bi-directional Front-end PFC Preregulator

When a motor decelerates rapidly or stops and starts frequently, the power flows from the motor and the net average value of bus current becomes negative. Reverse power flow to the ac mains through the rectifier bridge is not possible. The excessive regenerative energy from the motor increases the dc bus voltage. One of the simplest schemes to reduce the increased bus voltage is dynamic braking which uses a power resistor in series with a switching device across the bus. The level of bus voltage is regulated by dissipating the excessive energy through this resistor by switching. This braking resistor is bulky and inefficient in terms of energy usage. Thus it is not desirable to use in appliance VSD applications. Another alternative is regenerative braking which utilizes the bi-directional (two-quadrant) converter topologies which improves the input power factor and recovers the regenerative energy to the source at the same time. The various kinds of bi-directional converter topologies are presented in [18-20]. The further investigation of bi-directional converter is beyond the scope of this study and hence will not be discussed in this dissertation.

1.3 Motivation and Objective

The motivation and main objective of this study have been established from the result of previous literature research on single-phase PFC topologies and input PF-corrected VSD systems for appliance applications.

Motivation

Three factors which motivated this study are given as follows:

(i) The first motivation is the emerging high volume fractional horse power VSD applications, such as white goods, air circulation blowers for HVACs, power tools, spa and whirlpool equipments and exercise equipments.

(ii) The second one is the growing awareness for drawing sinusoidal current at high power factor from utility for better utilization of installed generation capacity and minimization of harmonic injection into the power distribution lines.

(iii) The third motivation is the mandatory federal regulations regarding power quality, such as IEC 1000-3-2 for limiting the input current harmonics.

Therefore the study of the effects of input PFC in appliance VSD system is timely appropriate.

Objective

The objectives of the study of the effects of input PFC on VSD systems are summarized as follows:

(i) Inclusion of input PFC in the VSD systems:

The solution for drawing the sinusoidal current at high PF from the utility is addition of a PFC means to the VSD systems. An active high frequency PFC topology based on boost converter has been selected as the PFC preregulator due to its simple power circuit and availability of the dedicated PFC controller chip. The inclusion of the PFC preregulator in appliance VSD systems not only reduces the magnitudes of input current harmonics, but it lowers the overall VSD system efficiency. Therefore the study of the system level efficiency is inevitable to justify the inclusion of the input PFC. The system level efficiency study was performed with various VSD systems with and without a PFC preregulator. The measured and predicted efficiencies are compared to each other to evaluate the effects of the input PFC to the VSD system. The predicted efficiency of a VSD system with and without a PFC preregulator is obtained with loss models which are derived from the summation of individual power losses of major power components in a VSD system and PFC preregulator. It should be mentioned that the derived loss models are unique to the given power ratings of PFC preregulators and VSD systems. Therefore the derived loss models are not directly applicable to other VSDs with different configurations, but the procedures to derive the power ratings and loss expressions for major power components can be referred to derive the loss models of other types of VSDs.

(ii) Incorporation of a low cost and high reliability power converters for the VSD systems:

Almost all of the input PF corrected VSDs in previous studies have been restricted to induction motors only. Therefore the investigation of input PF-corrected VSDs based on SRM, PMBDC and DCM motors has been taken up in this study. The brushless motors such as SRM and PMBDC are becoming popular in appliance VSD applications. The SRM is the newest motor even though it originated more than one hundred years ago. With emerging low cost magnets and electronic components, the PMBDC motor only recently gained its popularity for appliance applications. The DCM motor is one of the conventional motors for VSD applications. Among the three motors selected for this study, the DCM is the most popular motor in appliance applications due to its easy control and long proven history in the market.

The SRM-based VSD has been presented with the C-dump converter which is one of the most cost effective and reliable power converters. In particular, the application of the SRM-based VSD to appliance is growing due to its simple motor construction which lowers the overall VSD system cost. Further the cost of the SRM-based VSD system can be reduced by selecting a low cost converter topology. The most cost effective converter topology for SRM drive is a single-switch-per-phase type. One of this topology, C-dump converter is selected to implement the SRM-based VSD for this study. Previous study on C-dump converter based SRM drive is restricted to extremely low power application. The developed SRM-based VSD was tested over a 100W input power range. The systematic analysis and design of this topology were not presented in the previous literatures. The five operational modes are identified and based on this systematic

design procedures were developed. The SRM-based VSD system has been considered with and without the input PFC as the PFC will become mandated in the future. Overall system efficiency is obtained with experiment and analysis to study the efficiency variation with integration of front-end PFC preregulator in the VSD system.

While the application of C-dump converter to SRM already has been reported in the previous literatures, its application to the PMBDC motor is novel. Many of the emerging high volume VSD applications, mostly in the fractional to 1hp rating, face stiff low cost and compact packaging requirements to make it to the market. One of the obvious places to look for the reduction in the cost of the VSD systems is in the converter and control circuits. The C-dump converter, which is one of single-switch-per-phase converter topologies, has the advantages of a low number of power switches hence reduction in the number of logic power supplies and gate drive circuits, elimination of shoot-through fault and enhancement of reliability of the VSD system. In addition to that, the C-dump topology lends itself to four-quadrant operation. These advantages seem to match the high reliability and dynamic performance requirements of the emerging high volume, but low cost, appliance VSD applications. Also it has the disadvantage of requiring an additional step-down converter. A low cost four-quadrant controller based on discrete components is developed for evaluation of dynamic performance of the C-dump converter based PMBDC drive. The system design equations are derived from the detailed analysis. The analysis includes identification of operational modes of the proposed VSD systems and analytical derivations of design procedures for each mode to evaluate the drive system performances with and without an input PFC preregulator.

(iii) Investigation of the UMD concept for VSD systems:

The novel concept of the UMD has been developed and verified experimentally with a C-dump converter based SRM drive system intended for appliance application. This concept provides the uninterrupted source power to the appliance VSD system. Even though this concept is particularly suitable to the critical applications, such as medical equipments and semiconductor process equipments, etc., the advent of low cost high power switching devices and control circuits makes it possible to elaborate many appliance applications. Various charger and discharger topologies for UMD have been reviewed and one such topology has been selected for prototype implementation. The system performances during the steady-state and transients have been considered. The overall system efficiencies of the appliance SRM-based VSD during the charging and discharging modes have been experimentally measured and analytically predicted.

1.4 Dissertation Outline

The boost PFC circuit is introduced and the principle of operation is discussed in Chapter 2. Analytical expressions of power ratings and the losses for power components in the boost PFC converter are derived. With these derivations, the predicted efficiencies at different output power levels of the boost PFC circuit are shown. Furthermore, the predicted efficiency is compared with the experimental one. The statistical analysis of the predicted efficiency error is provided to evaluate the developed loss models for 300W and 2kW PFC preregulator. The magnitude of the input current harmonics are compared with the modified IEC 1000-3-2 Class A limit with a 1.4kW load.

In Chapter 3, the operational principles and single switch per phase converter topologies of the SRM are explained. One of the minimum switch per phase converters, the C-dump converter, has not been tested for practical levels and has not been analyzed completely. The comprehensive analysis, design and test results for the C-dump converter at significant power levels is provided. The proposed SRM-based VSD is experimentally verified with and without a PFC circuit. The experimental results are compared with the analytical one. The main comparison factors are efficiency, input power factor, and magnitude of input current. The effects of the PFC circuit is investigated with the modified IEC 1000-3-2 Class D relative limit. The SRM phase current and recovery current are simulated to confirm the operational performance of the drive. A comparative study of the magnitude of the input power factor and the input ac current is performed to verify the effectiveness of the input PFC. The predicted error of the overall system efficiency is presented to validate the derived loss models with and without input PFC.

The uninterruptible motor drive (UMD) concept is introduced in Chapter 4. The study investigates the various power converter topologies for UMD implementations and illustrates the concept with SRM-based VSD systems. The power ratings of the UMD are derived and compared to the conventional VSD systems. The efficiency study with and without the PFC circuit is provided. The predicted efficiency with and without input PFC is obtained by the derived loss models. A statistical comparison is performed to validate the derived loss models.

A PMBDC drive system employing a C-dump converter is introduced in Chapter 5, along with the principle of operation. The C-dump converter topology for the SRM is applied to PMBDC drive, its performance is verified with experiment and simulation. Analysis and design guidelines are introduced. A four-quadrant controller for the PMBDC is developed and experimentally verified. A two-stage PFC is employed, not only to correct the input power factor, but to meet the converter input voltage level for the PMBDC. For the prediction of the overall system efficiency, duty cycles for the main phase switch and the recovery switch are analytically derived. The analytical expressions of the power ratings and losses of the major power components are also derived. Comparative results between the predicted and measured efficiency are presented with and without a PFC circuit. Statistical analysis of the system efficiency shows the correlation between the measured and predicted efficiencies. The magnitude of the harmonic content in the input ac current with and without input PFC is compared with the modified IEC 1000-3-2 Class A absolute limit to validate the effectiveness of the input PFC.

A DCM-based VSD system with and without the PFC circuit is explained in Chapter 6. A four-quadrant controller is developed and experimentally verified. The dynamic speed loop simulation is performed to evaluate the developed controller. The analytical expression for the duty cycle at steady-state is derived. The power ratings and losses of power components are analytically derived. Analytical and experimental results are compared. The input current harmonics are compared with the modified IEC 1000-3-2 Class D relative limit. The magnitude of input power factor and the input ac current are investigated with and without the PFC. The predicted efficiency is compared with the measured one, with and without the PFC preregulator. The statistical analysis shows the accuracy of the derived loss models.

In Chapter 7, conclusions and recommendations are introduced to summarize the entire work.