Chapter 5. Input PF-Corrected PMBDC-Based VSD System

5.1 Introduction

With the growing potential for widespread use of PMBDC drives in many low-cost applications such as in HVAC (Heat, Ventilation and Air Conditioning), refrigerators, and freezers in houses and small velocity servos in process industries, it has become important to minimize costs. Due to the high volume nature of these applications, cost minimization is of paramount importance not only to save materials, labor, and possibly parts reduction to enhance the reliability of the product, but also because without such a cost minimization many of these applications with VSDs may not be realized. One obvious place for cost reduction is in the cost of the inverter and its associated controller.

The half-wave and full-wave (H-bridge) converter topologies are invariably associated with very low performance and high performance applications, respectively. The half-wave converter topology with one switch per phase has half the number of switches of the full-wave topology but could only deliver motoring in both directions with no regenerative control. This fact precludes its use where high performance is a requirement. This could be resolved if topologies with more than one switch per phase but less than two switches per phase are used [6]. Such topologies [2, 8, 9, 21, 32] have been developed for SRM drives with considerable success. One such topology is the C-dump converter with (n+1) switches for a n-phase machine [27, 33, 35] as explained in Chapter 3. With that perspective, a novel application of the converter topology for the PMBDC known as C-dump converter in the SRM drives is proposed in this study. Design considerations for the PMBDC-based VSD are derived for use with the proposed converter topology. The operational and design characteristics of the C-dump converter driven PMBDC drive are derived for four-quadrant performance. Guidelines for the design of the proposed topology are derived and presented in this chapter. Experimental results from a laboratory prototype are presented to validate the feasibility of the proposed PMBDC drive system.

The input power factor correction is applied to the developed C-dump converter based PMBDC drive. The two-stage power conversion which consists of the boost PFC converter for ac-dc conversion and the buck converter for dc-dc conversion is employed. The front-end boost PFC converter is for the input PFC and the buck step-down converter is to match the output voltage of the PFC converter with the terminal voltage of the PMBDC. The analytical expressions of the duty cycle and loss model of the 2kW buck converter are derived. Based on these analytical results, converter efficiency is predicted and compared with the measured ones. The duty cycles of both the main phase switch and the recovery switch are analytically derived. The predicted and measured overall system efficiencies of the PMBDC-based VSD are compared with and without PFC circuit.

This chapter is organized as follows. Section 5.2 contains the principle of operation of the C-dump topology based PMBDC. Section 5.3 presents the design considerations for the PMBDC motor for use with the proposed converter topology. Analysis of the proposed drive system is also given in this section. Development of a four-quadrant controller for C-dump converter based PMBDC drive is explained in Section 5.4. Experimental verification of the developed controller is introduced in this section. Experimental setup and verification of the proposed PF corrected

PMBDC drive system with and without the PFC circuit are given in Section 5.5. Section 5.6 contains the key conclusions of the study.

5.2 Principle of Operation of the Proposed C-Dump Converter-Based PMBDC Drive System

The definition of the operational quadrant is given in Figure 5.1 [1, 34, 35]. The defined operating quadrants are applied to all VSDs in this study. The four different combinations of the polarities of speed and torque contribute to decide the adequate operating quadrant. The relationship between four different combinations of the polarities of speed and torque is summarized in Table 5.1.

The C-dump converter for a three-phase system, shown in Figure 5.2, is considered for this study [34, 35]. It has four power switches and four power diodes with one of each for each phase winding and one set for energy recovery from the capacitor, C_o.

The key waveforms of this circuit is similar to Figure 3.7(ii). Since the phase has only one switch, the current in it could be only unidirectional and hence it is very similar to the half-wave

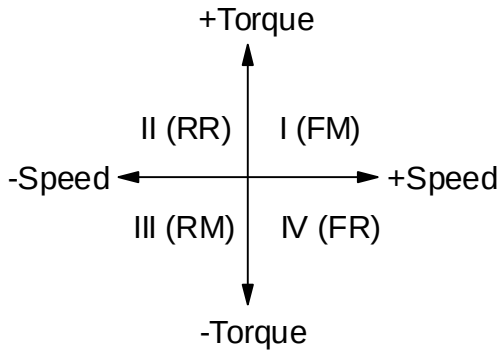


Figure 5.1 Definition of four operational quadrants.

Table 5.1
Definition of four operational quadrants.

Mode of Operation	Quadrant	Speed	Torque	Phase Sequence
Forward Motoring (FM)	I	+	+	a-b-c
Forward Regeneration (FR)	IV	+	-	a-b-c
Reverse Motoring (RM)	III	-	-	a-c-b
Reverse Regeneration (RR)	II	-	+	a-c-b

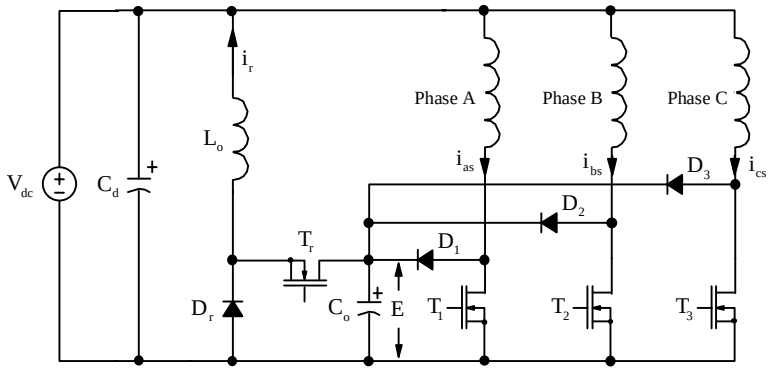


Figure 5.2 C-dump converter topology for three-phase PMBDC.

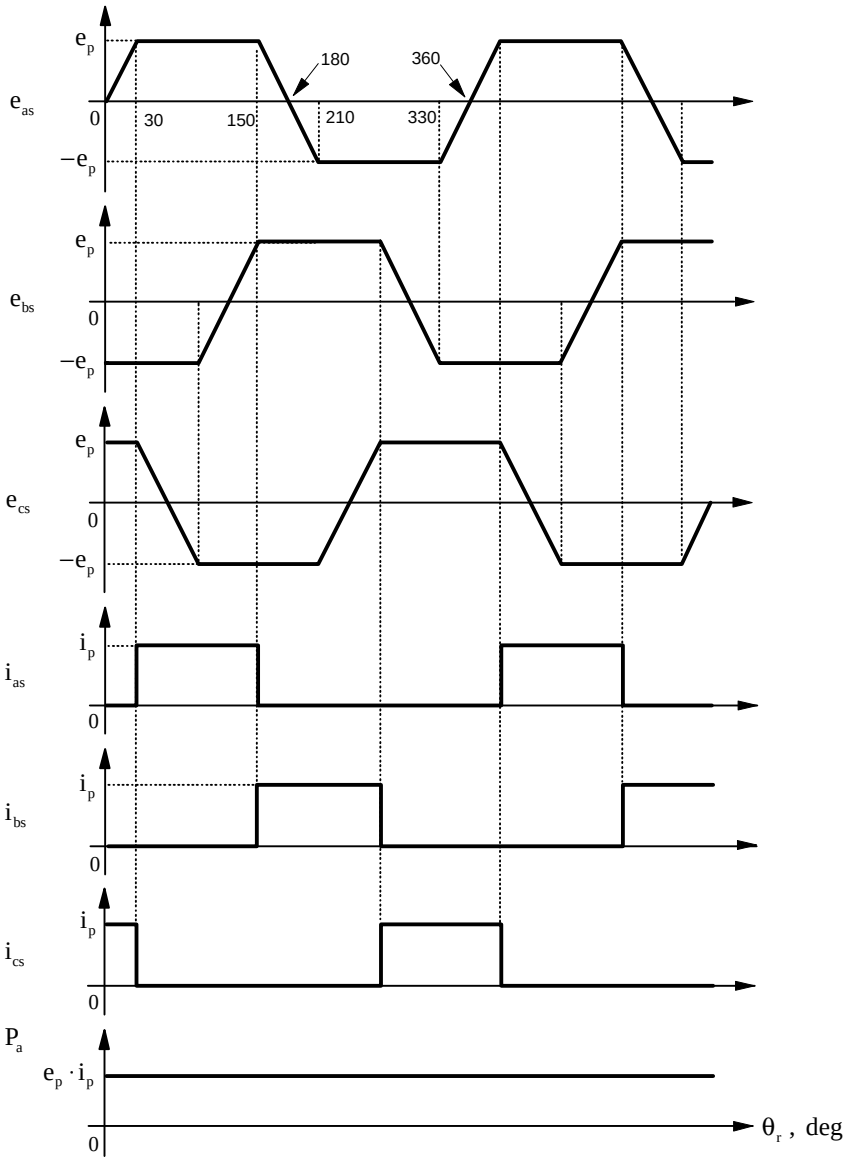


Figure 5.3 Voltage, current and airgap power waveforms of the proposed C-dump based PMBDC.

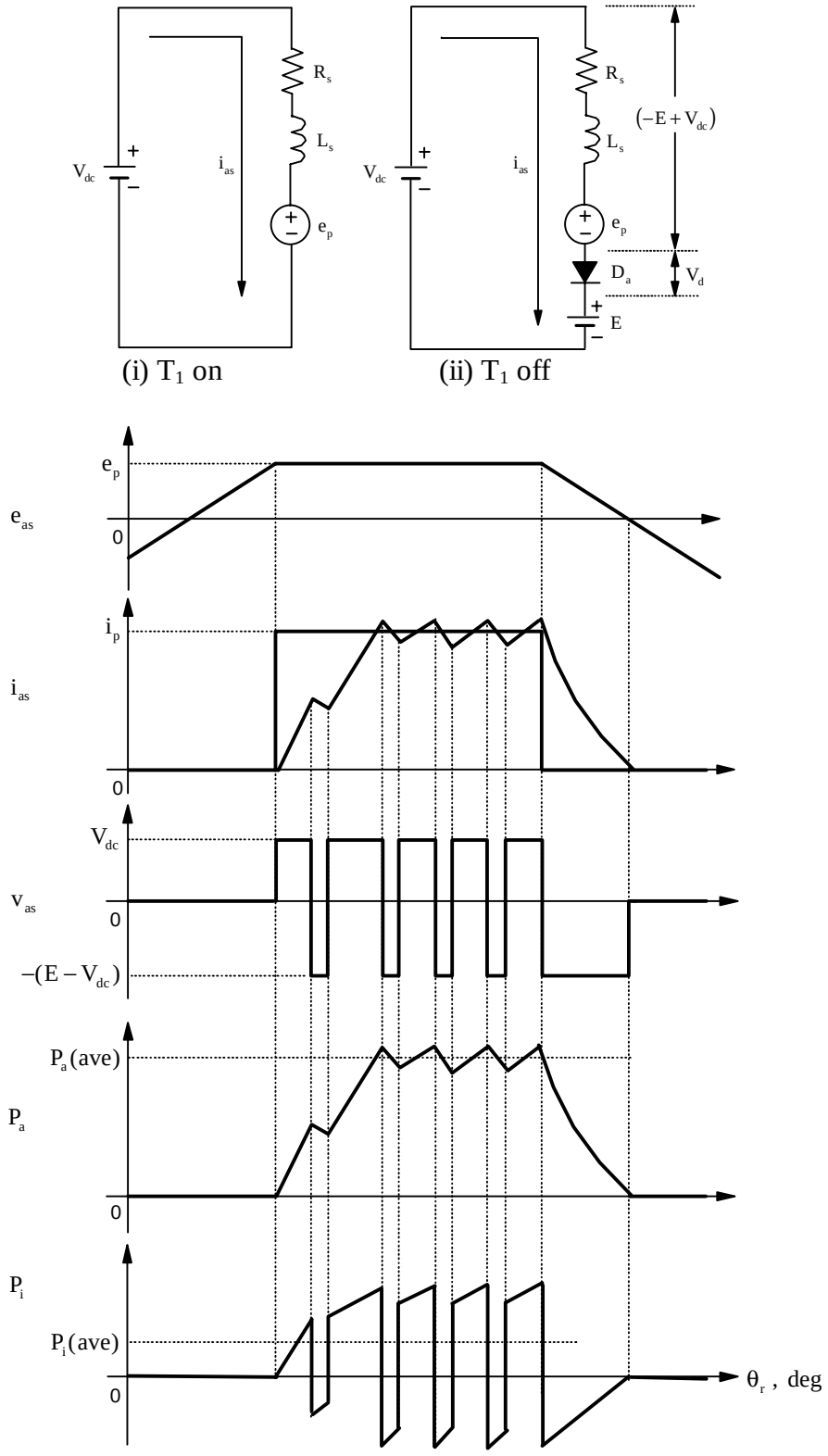
converter driven PMBDC in operation. The operation of the various phases could be simply shown as in Figure 5.3 for a phase sequence of *a-b-c*. The duty cycle of each phase is only 1/3 and, in spite of it, note the airgap power and hence the electromagnetic torque are both continuous.

5.2.1 Motoring Operation

The forward motoring (first-quadrant) and reverse motoring (third-quadrant) operations of the C-dump converter-based PMBDC are briefly described in this section. Assume the direction of the motor is clockwise, which may be considered as positive with a phase sequence of *a-b-c* of the motor phase windings for this discussion. The motoring operation is initiated when the phase voltage is in the flat region, i.e., at constant magnitude for a fixed speed and with the duration of 120 electrical degrees. Phase A is energized when the phase current is commanded by turning on switch T_1 and the input power is positive, giving a positive electromagnetic torque. This indicates that the operation is firmly in the first-quadrant of the torque speed as shown in Figure 5.4. When the current error is negative, switch T_1 is turned off and the current in the Phase A winding is routed through the diode D_1 to the energy recovery capacitor, C_o shown in Figure 5.4(ii). During this time, a negative voltage to the magnitude of $(E - V_{dc})$ is applied across the machine winding, reducing the current and bringing the current error to positive. Waveforms of key variables such as the induced emf, stator current, stator voltage, airgap power and input power are shown in Figure 5.4(iii) for the motoring operation. The reverse motoring operation in the counter clockwise direction of rotation of the motor is similar, except the phase sequence will be *a-c-b* in the energization of the motor phase windings. This corresponds to the third-quadrant of the torque speed characteristics.

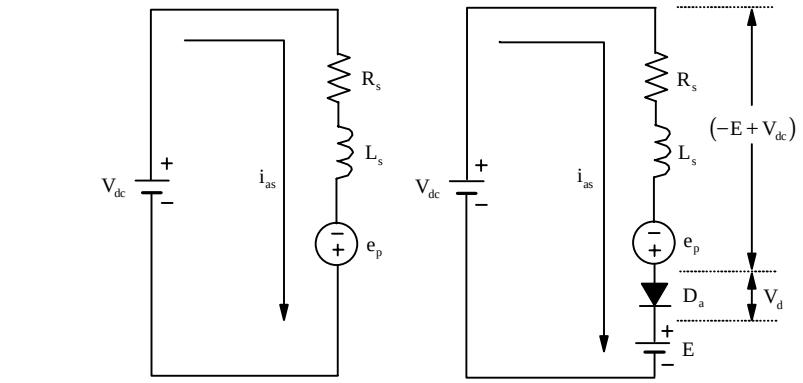
5.2.2 Regenerative Operation

Whenever the energy has to be transferred from the load to the supply, the PMBDC is to be operated as a generator, i.e., by providing a negative torque to the machine against the positive torque for the motoring operation. It is usual to provide a current of opposite polarity to that of the induced emf in the full-wave converter operated PMBDC to generate a negative torque. It is not feasible in this C-dump operated PMBDC due to its unidirectional current feature for the positive half cycle of the induced emfs. Then the only alternative is to exploit the negative cycles of the induced emf where only positive currents are required to obtain the negative torque. Such an operation for Phase A involves turning on T_1 during the negative constant emf period and when the error current becomes negative turning off T_1 enabling the conduction of D_1,which results in the energy transfer from the machine Phase A to the energy recovery capacitor shown in Figure 5.5. Key variable waveforms are also shown in Figure 5.5 for this mode of operation. Note that the airgap power and the average input power to Phase A are negative indicating that the power has been transferred from the machine to the energy recovery capacitor, C_o. The energy from C_o is recovered by a step-down chopper using switch T_r and diode D_r, shown in Figure 5.2. Note that this regenerative operation corresponds to the fourth-quadrant for a phase sequence of *a-b-c* and is similar to the regenerative operation for reverse rotational direction of the PMBDC corresponding to the second-quadrant.

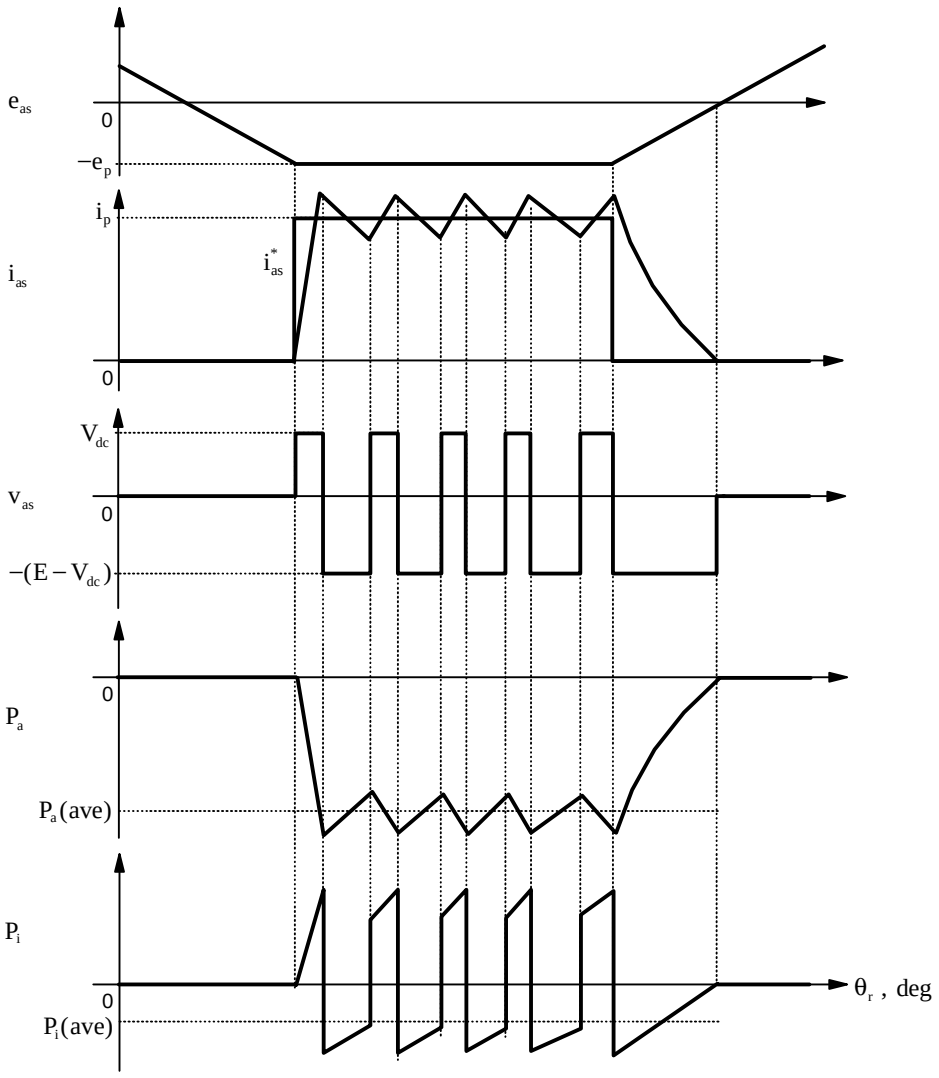


(iii) Waveforms of variables

Figure 5.4 First-quadrant motoring operation of PMBDC drive.



(i) T_1 on (ii) T_1 off



(iii) Waveforms of variables

Figure 5.5 Fourth-quadrant regenerative operation of PMBDC drive.

5.3 Analysis and Design of the C-Dump Converter-Based PMBDC Drive

The analysis of the drive system with the proposed topology is presented in this section. Effort is primarily made to obtain the maximum speed of the motor in terms of the duty cycle of the phase switches and the energy transferred to the energy recovery capacitor and hence, an estimate of the power to be handled by the recovery chopper for a given motor rating. For this study, it is assumed the commutation pulses are available through Hall sensors or encoders or resolvers.

5.3.1 Maximum Speed

Consider the machine voltage equation in steady-state for a rated stator current given by I_b and it is given as follows :

$$v_{as} = R_s \cdot I_b + K_b \cdot \omega_m \quad \text{, V.} \tag{5.1}$$

and the speed is obtained from this as,

$$\omega_m = \frac{v_{as} - R_s \cdot I_b}{K_b} \quad \text{, rad/s.} \tag{5.2}$$

For a faster current loop and hence higher torque and faster speed response, it is necessary to set aside some voltage which is a fraction of the rated stator voltage given as $K_a v_{as}$. Including this factor, the rotor speed is modified to,

$$\omega_m = \frac{1}{K_b}\left[v_{as}\left(1 - K_a\right) - R_s \cdot I_b\right] \text{, rad/s.} \tag{5.3}$$

If an average duty cycle of the phase switches is denoted as d, then the stator phase voltage in terms of the dc link voltage is written as,

$$v_{as} = d \cdot V_{dc} \text{ , V.} \tag{5.4}$$

which when combined with the speed equation and normalization yields the normalized rotor speed as,

$$\omega_{mn} = d \cdot \left(1 - K_a\right) \cdot V_{dcn} - R_{sn} \quad \text{, pu.} \tag{5.5}$$

where,

$$\left.\begin{aligned} \omega_{mn} &= \frac{\omega_m}{\omega_b} \ , \ pu \\ V_{dcn} &= \frac{V_{dc}}{V_b} \ , \ pu \\ R_{sn} &= \frac{R_s}{Z_b} \ , \ pu \\ Z_b &= \frac{V_b}{I_b} \ , \ \Omega \end{aligned}\right\} \tag{5.6}$$

The additional subscript n denotes the normalized values of the variables and parameters. K_a is typically in the range of 0.2 to 0.4 and d varies from nearly zero to one. This relationship explicitly gives speed in terms of the duty cycle, dc link voltage, stator resistance, and dynamic voltage reserve. This expression allows the determination of range of d variation for the desired variation of speed range. Determination of d is crucial in the evaluation of the average energy recovery current and hence in the rating of that circuit.

5.3.2 Peak Recovery Current

The energy transferred to the energy storage capacitor, C_o, during the turn-off intervals of phase switches has to be recovered through the energy recovery circuit if losses are neglected. The average duty cycle of energy transfer from the dc link and machine phase into the capacitor C_o is *(1-d).* Assuming this stored energy is recovered through the chopper in a duty cycle of d, as is essential to keep the separation of energy storage and recovery circuits, the powers can be equated as,

$$E \cdot (1-d) \cdot I_p = E \cdot d \cdot I_r \, , \tag{5.7}$$

where I_r is the peak recovery current through the chopper and could be written as,

$$I_r = \frac{(1-d)}{d} \cdot I_p . \tag{5.8}$$

As d increases, note the energy recovered through the chopper reduces as I_r goes down, which in turn reduces the volt-ampere rating of the energy recovery chopper circuit.

5.3.3 Design Guidelines for the C-Dump Converter for PMBDC Drive

The guidelines for the rating of the various passive and active components of the C-dump topology driven PMBDC drive are presented in this section based on the analysis of the drive scheme in the previous section. The rated current and voltage of the PMBDC motor are I_b and V_b, respectively and hence the base power is $(V_b \cdot I_b)$. These values form the base values for the determination of the component ratings.

Dc Link Voltage

The minimum dc link voltage, V_{dc}, required is

$$V_{dc} = \left(E_b + I_b \cdot R_s + L_s \frac{dI_b}{dt} \right), \text{V.} \tag{5.9}$$

Here the rate of the change of current should correspond to the base current when the machine is running at rated speed, ω_b, which is related to the emf E_b by,

$$E_b = K_b \cdot \omega_b \quad , \text{V.} \tag{5.10}$$

Determination of this dc link voltage leads to the rating of the capacitor, *C*.

Phase Switches

Its minimum voltage is given by,

$$V_{sw} = E \quad , \text{V.} \tag{5.11}$$

where *E* is the voltage across the energy recovery capacitor. Its current ratings are given by,

$$I_{sw}(pk) = I_b \cdot x \quad , \text{A.} \tag{5.12}$$

$$I_{sw}(rms) = \frac{I_b \cdot x}{\sqrt{3}} \quad , \text{A.} \tag{5.13}$$

where *x* is the number to find the transient torque in terms of the base torque which usually is much greater than one for high performance applications, say in the order of two or so, and for low performance applications it is around 1.25.

Phase Diodes

The voltage rating is the same as that of the phase switches, i.e., *E*, but their current ratings vary from that of the phase switches. Its peak current rating has to be equal to that of the phase switch, but its rms value could be smaller than that of the phase switches. Assuming a maximum duty cycle of 0.5,

$$I_d(rms) = (0.7) I_{sw}(rms) \quad , \text{A.} \tag{5.14}$$

Energy Recovery Capacitor

The minimum voltage on this capacitor, C_o, is given by,

$$E(min) = V_{dc} + E_p + \Delta E \ , \text{V}. \tag{5.15}$$

where E_p is the maximum induced voltage at maximum speed and ΔE is the voltage magnitude to be provided for in design to prevent the conduction of diodes D_1, D_2 and D_3 during the negative half cycles of the induced emf generation in the machine.

Energy Recovery Chopper

The voltage rating is equal to *E* but its current rating is based on the power transfer from the energy recovery capacitor to the dc link. It is based on the speed of operation and load which is a function of the duty cycle of the phase switch. The inductor L_o is rated based on the switching frequency of the chopper.

5.4 Four-Quadrant Controller Development for C-Dump Converter-Based PMBDC Drive

The design process of the four-quadrant controller for the C-dump converter based PMBDC drive is introduced in this section. The definition of the operational quadrant based on the relationship between the polarities of speed feedback and torque command signals is explained. The developed commutation logic circuit with this principle along with its key waveforms are presented.

5.4.1 Definition of Operational Quadrant

The same definition of the operational quadrant with the polarities of speed and torque which is given in Figure 5.1 and Table 5.1 [1, 34, 35] is applied to the PMBDC-based drive system. The four different combinations of the polarities of sensed speed response, ω_r, and torque command, T_e^*, contribute to decide the adequate operating quadrant as illustrated in Figure 5.6. The mode of operation and phase sequence for each defined quadrant is summarized in Table 5.2. The forward phase sequence, *a-b-c*, is associated to the operational quadrants I and IV. Both quadrants II and III are related to the reverse phase sequence, *a-c-b*. This definition will also be applied to the DCM-based VSD in this study.

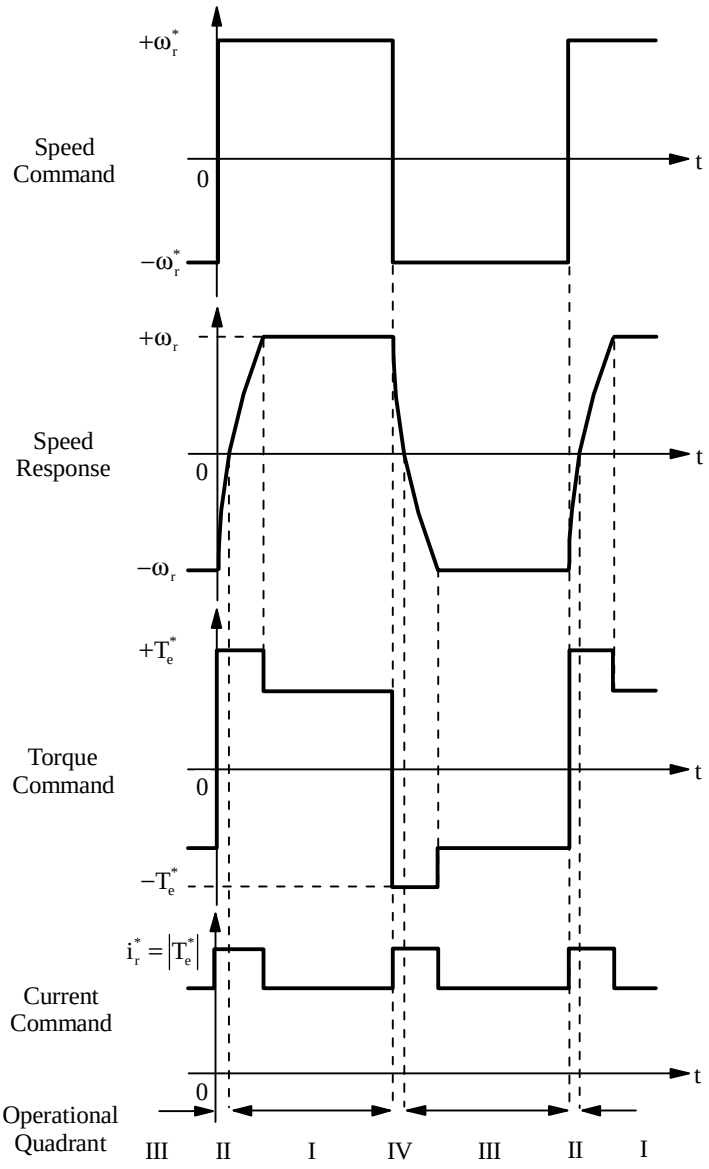


Figure 5.6 Determination of operating quadrant with polarities of speed response and torque command.

Table 5.2
Decision of operational quadrant with polarities of speed and torque.

		Speed	**Torque**	
Mode of Operation	**Quadrant**	ω_{rp}	T_{ep}^{*}	**Phase Sequence**
Forward Motoring (FM)	I	+	+	*a-b-c*
Forward Regeneration (FR)	IV	+	-	*a-b-c*
Reverse Motoring (RM)	III	-	-	*a-c-b*
Reverse Regeneration (RR)	II	-	+	*a-c-b*

5.4.2 Implementation of Four-Quadrant Controller

The Hall effect sensors provide the rotor position informations and their outputs are represented as H_a, H_b and H_c in Figure 5.7(i). The output signals of the Hall effect sensors are processed through a commutation logic circuit to decide the duration of commutation cycle of each phase. The output of commutation circuit is applied to the corresponding phase switch. The firing sequence of the phase switch according to the forward or reverse phase sequence are also shown in Figure 5.7(i). When the reverse phase sequence required in II- or III-quadrant, the outputs of AND2 and AND3 will be applied to T_3 and T_2, respectively. The analog switch is utilized to route the output signal of the commutation logic circuit.

The key waveforms of the commutation logic circuit are shown in Figure 5.7(ii). The output of the commutation circuit will be combined with a PWM signal and be distributed to the gate drive circuit for driving the phase switch. An OC (overcurrent) detection circuit is implemented with one current transducer that senses the current in common power return path in the dc bus. OC fault is presumed when the peak motor current exceeds 20A. The output of OC detection circuit is combined with the gate drive signal to protect the phase switch against the fault current.

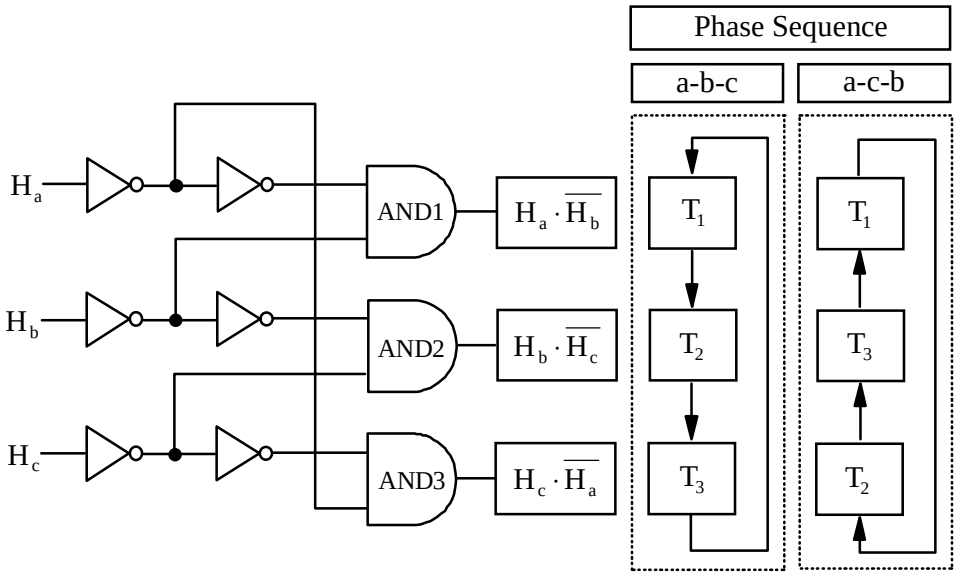


Figure 5.7(i) Commutation logic diagram for phase sequences a-b-c and a-c-b.

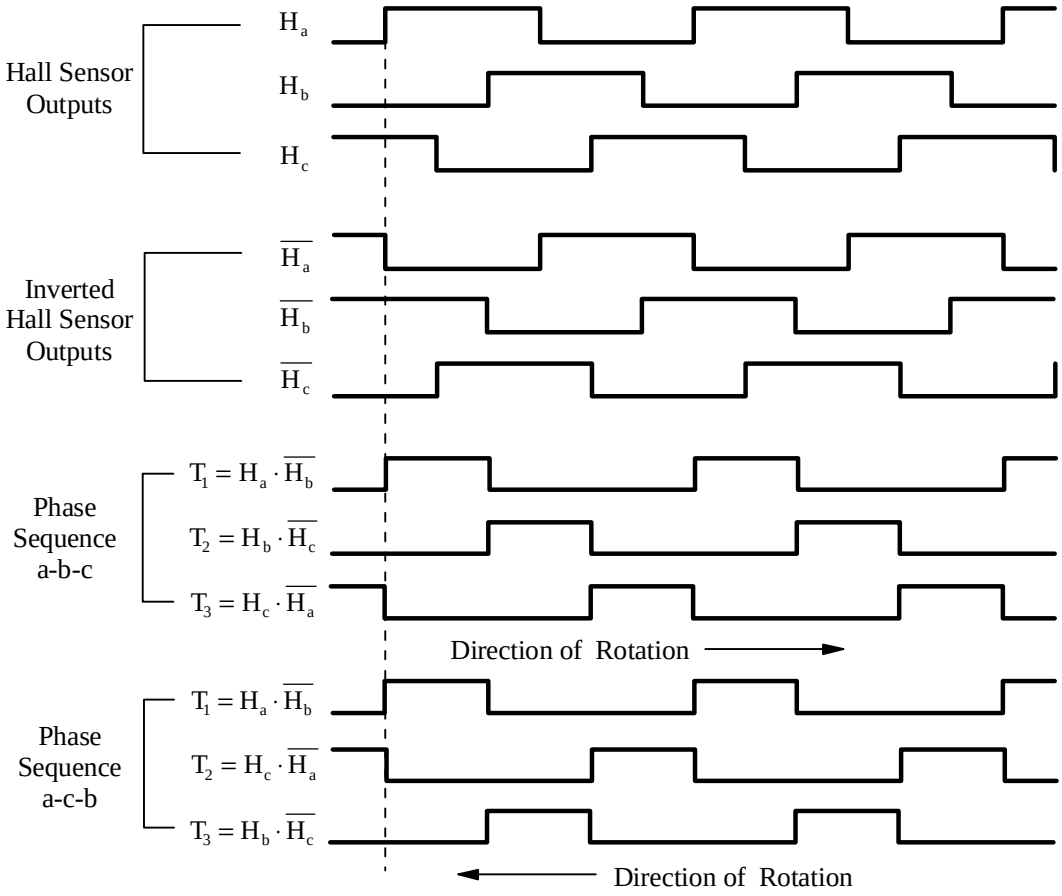


Figure 5.7 (ii) Waveforms of commutation logic circuit.

5.4.3 Experimental Verification of the Developed Controller

The simplified block diagram of the proposed four-quadrant PMBDC drive is shown in Figure 5.8. The C-dump converter-based PMBDC drive is realized with the MOSFET-based converter fed from a rectified 115V ac utility supply with an approximate dc link voltage of 100V. For the purpose of load, a permanent magnet brush dc machine has been coupled to run as a generator driven from the PMBDC drive system. The ratings and characteristics of the PMBDC and the load dc machine are given in the Appendix B.

The actual speed is sensed by a tachogenerator. The speed feedback signal is compared with the commanded speed signal, producing the speed error. The speed error signal is fed into a PI speed controller. The output of the PI speed controller becomes the torque command signal. The torque command signal is applied to a precision fullwave rectifier circuit and then becomes the current command. The difference between the commanded current and current feedback signal is applied to the current PI controller. The output of the current PI controller is compared with the triangular waveform to produce a PWM signal. The polarities of the speed feedback and the torque command signals are detected through speed and torque polarity detectors which consist of two zero crossing detector circuits. The C-dump controller is provided to control the auxiliary switch in a recovery circuit. This circuit is the same as the one in SRM-based VSD which is explained more in Section 3.4.2.

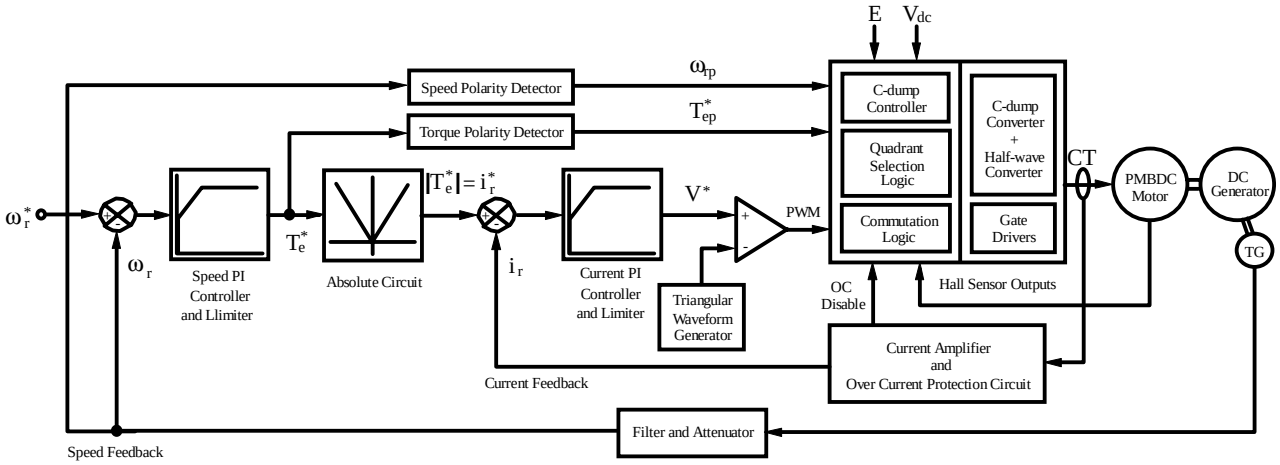
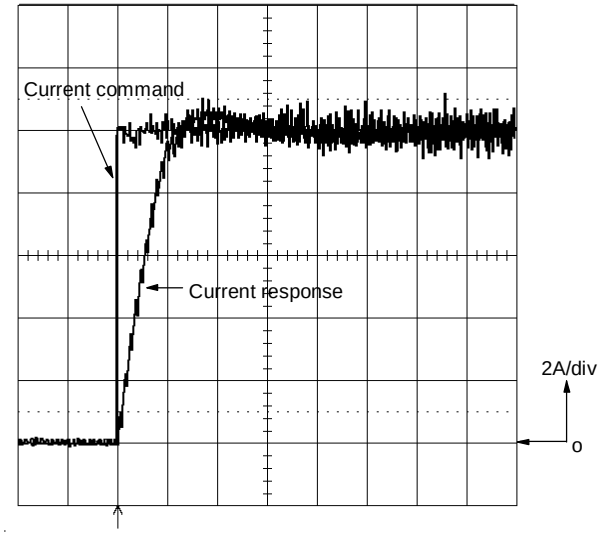


Figure 5.8 Simplified block diagram of the proposed four-quadrant PMBDC drive.

The experimental verification of the developed four-quadrant controller is performed with a PMBDC and DCM set from A.O. Smith and Electro Craft, respectively and details of PMBDC and DCM are listed in Appendix B. A DCM is used as the generator along with the variable resistor bank.

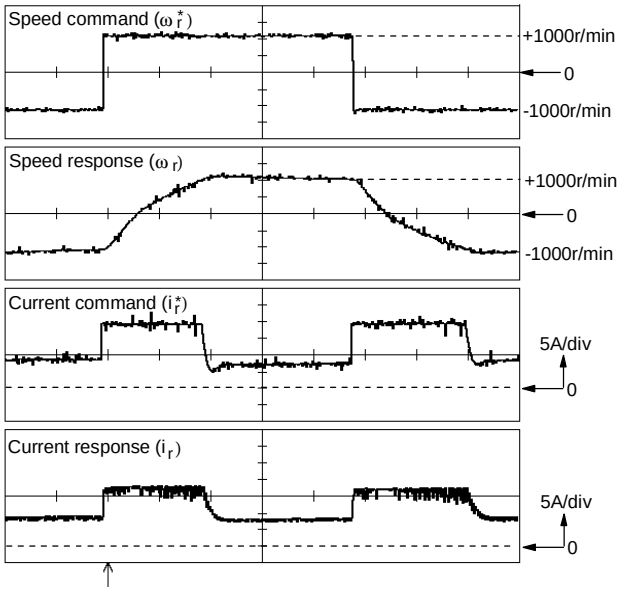
Figure 5.9 shows the step current response in one phase of the proposed PMBDC drive with the machine running at 1000r/min. The response time is 0.6 ms to reach the commanded value, 10A. It shows the current loop bandwidth of 1kHz. The step current response is simulated based on current loop equations in section 3.4.1. The simulated waveform is closely matched with the experimental result. The response of the speed loop is shown in Figure 5.10 for a speed command of ±1,000r/min. The speed response time to change between -1,000r/min to +1,000r/min is 1s.

The current command and response signals are also shown in this figure. The slight difference between the two signals is due to the low pass filter in the current feedback path.



(Time: 0.5 ms/div)

Figure 5.9 Current loop response of the experimental prototype drive.



(Time: 500 ms/div)

Figure 5.10 Speed and current loop responses of the experimental prototype drive.

5.5 Input PF-Corrected PMBDC Drive

The effectiveness of the front-end PFC for PMBDC-based VSD system is investigated in this section. The analysis and implementation of such a drive system in respect of efficiency and magnitude and harmonic contents of input currents are introduced. For efficiency prediction, a loss model for PMBDC-based VSD drive system is derived. The two-stage power conversion is employed to correct the input PF and to match the motor voltage of the PMBDC-based VSD system. The proposed PF corrected PMBDC-based VSD system is similar to the PF corrected SRM-based system shown in Figure 3.17 except that it has a two stage dc-dc conversion and its controller. The output power rating of both the front-end PFC preregulator and step-down buck converter is 2kW which is sufficient to supply power to the proposed PMBDC-based VSD system.

5.5.1 Analysis and Design of the Input PF Corrected PMBDC Drive

Derivation of Switch Current and Duty Cycle

It is very important to derive the analytical expressions in terms of switch current and duty cycle to develop the relevant loss models. The analytical expressions of PMBDC phase current and duty cycle for main phase switch and auxiliary switch are derived in this section.

The peak current in PMBDC is obtained from the following equations [3],

$$P_a = E_p \cdot I_p = K_b \omega_r \cdot I_p \ , \text{W}. \tag{5.16}$$

or in terms of output power and friction and windage losses,

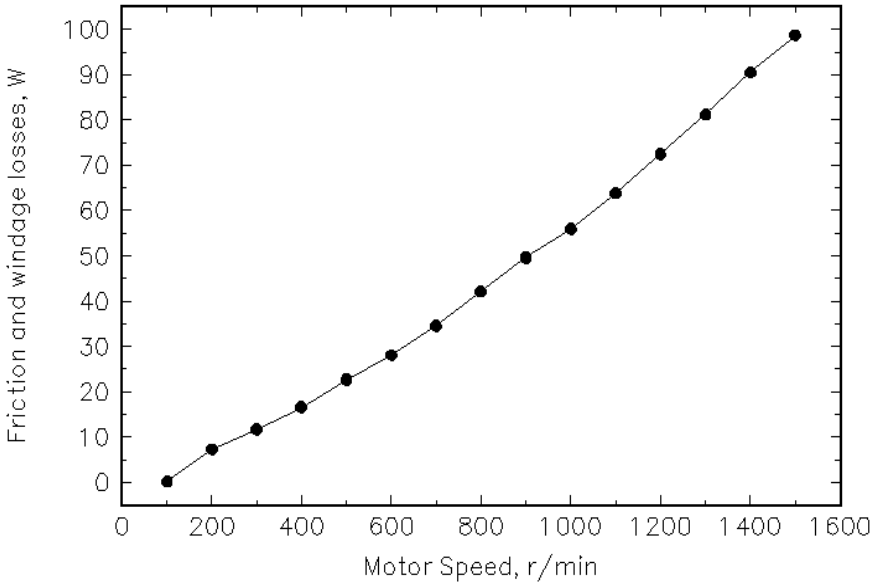


Figure 5.11 Friction and windage losses of a 4hp PMBDC motor from Kollmorgen and 1hp separately excited DCM from Integrated Electric.

$$P_a = P_{ro} + P_{fw} \text{ , W.} \tag{5.17}$$

where

P_a	=	airgap power, W
E_p	=	peak emf, V
I_p	=	peak phase current of PMBDC
K_b	=	emf constant, V/(rad/sec)
ω_r	=	motor speed, rad/sec
P_{fw}	=	friction and windage losses, W

and P_{ro} is the rated output power in W defined in equation (3.59).

The measured friction and windage losses of 4hp PMBDC motor coupled with 1hp DCM generator set is shown in Figure 5.11. The maximum speed is limited to 1,500r/min to match the rated speed of DCM which serves as a load.

By combining equations (5.16) and (5.17), and then rearranging them in terms of phase current, we have

$$I_p = \frac{P_{ro} + P_{fw}}{K_b \omega_r} \text{ , A.} \tag{5.18}$$

The duty cycle of the main phase switch, d is calculated by rearranging the equation (5.5) as,

$$d = \frac{\omega_{mn} + R_{sn}}{(1 - K_a) \cdot V_{dcn}}. \tag{5.19}$$

The duty cycle of the recovery switch, d_r is predicted with following relationship,

$$d_r \cong \frac{V_{dc}}{E}. \tag{5.20}$$

The measured duty cycles of the main phase switch and recovery switch are shown in Figure 5.12. The predicted duty cycle of the main switch and recovery switch with equations (5.19) and (5.20) are compared with the measured values in Figures 5.13 and 5.14, respectively. The predicted values are closely matched with the measured one. The prediction of the main phase switch duty cycle has better correlation with the measurement than the recovery switch duty cycle. In the high speed region, the measurement values of the recovery switch duty cycle show significant deviation from the predicted one. This may be due to the combination of measurement error and the use of a concise analytical equation for d_r defined as equation (5.20). The prediction error of the duty cycle is summarized in Figure 5.15 and Table 5.3. The error is within ±10% over the entire speed range for the main switch duty cycle and below 1,000r/min for the recovery switch duty cycle.

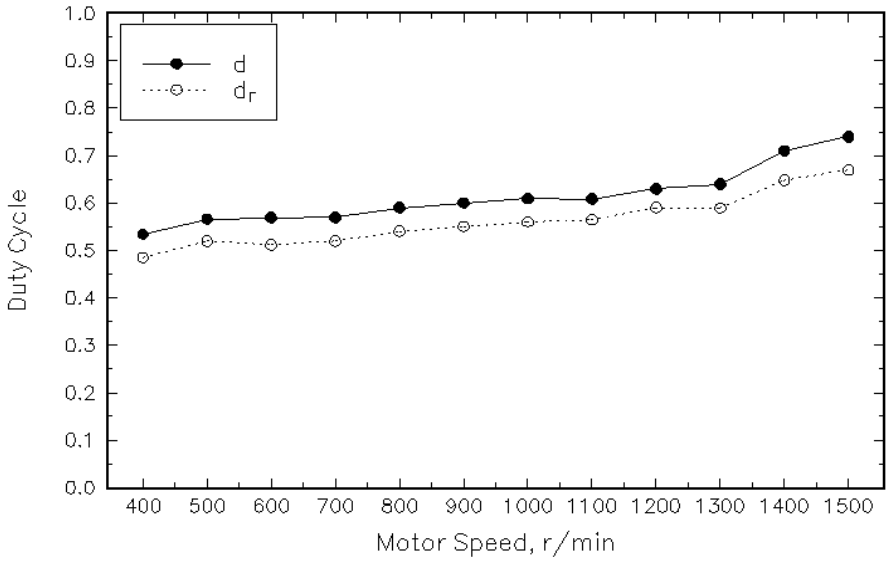


Figure 5.12 Measured duty cycle of main phase switch, d and recovery switch, d_r.

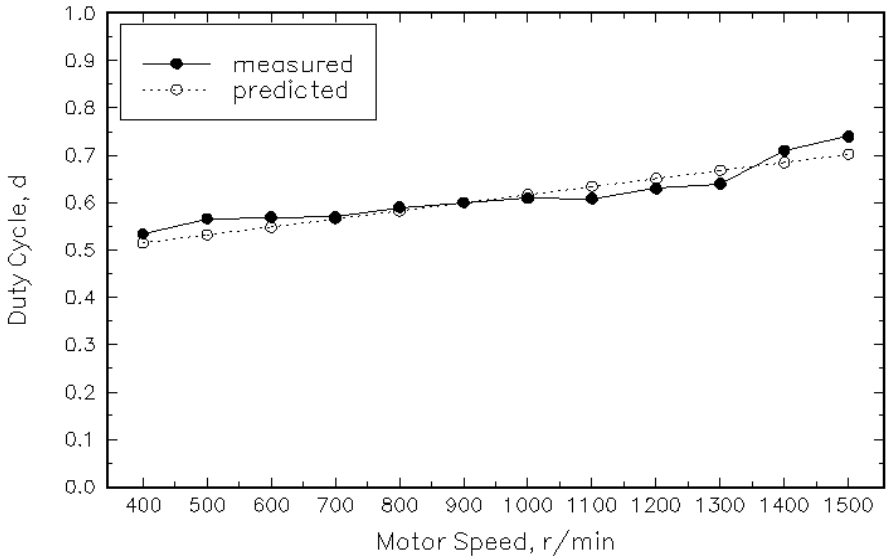


Figure 5.13 Measured and predicted duty cycle of main phase switch.

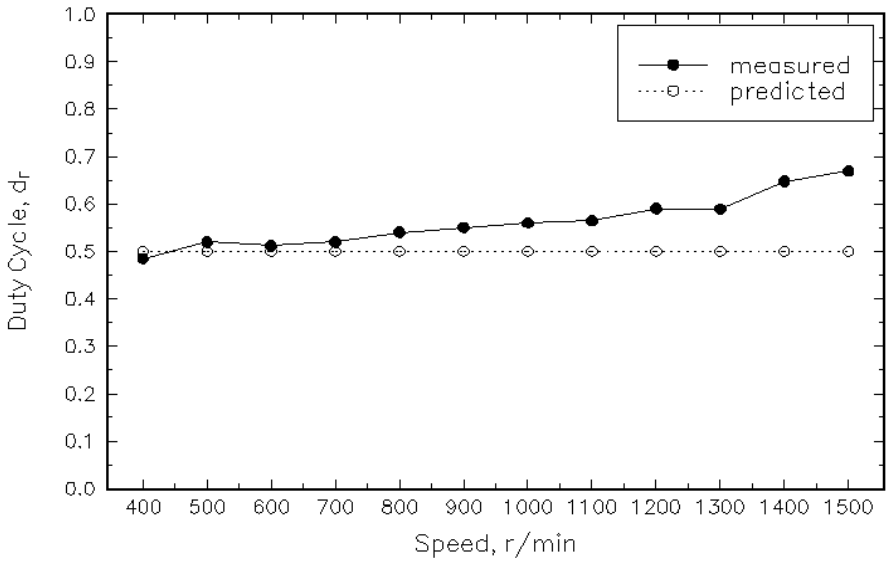


Figure 5.14 Measured and predicted duty cycle of recovery switch.

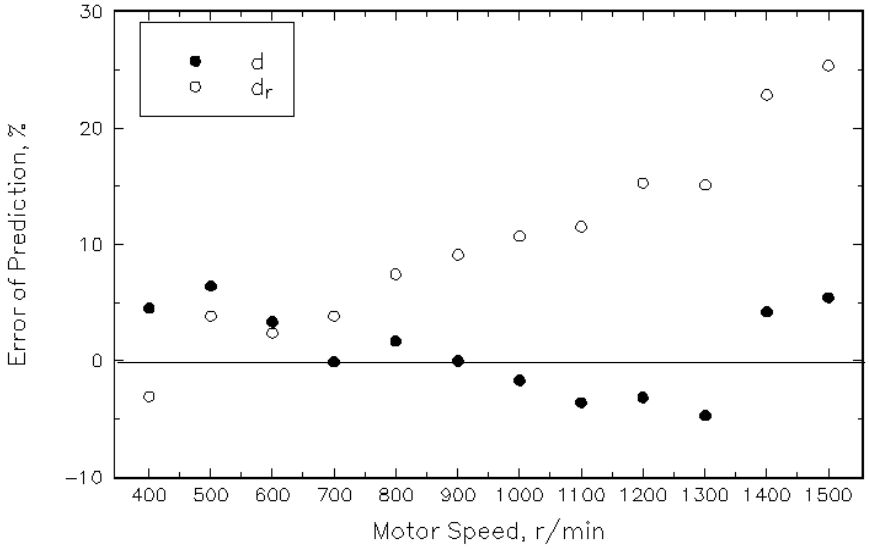


Figure 5.15 Prediction error versus PMBDC speed for duty cycles for main and auxiliary switches.

Table 5.3
Statistical analysis results of prediction errors for main and auxiliary switch duty cycles.

	Fig. 5.14 d	Fig. 5.15 d_r
Total Observation	12	12
Minimum Error	-4.69	-3.08
Maximum Error	6.42	25.37
Mean	1.03	10.35
Median	0.85	9.90
Variance	14.35	69.90
Standard Deviation	3.79	8.36
Standard Error	1.09	2.41

Derivation of Loss Models of 2kW PFC and buck converters and PMBDC drive

The loss model of 2kW PFC preregulator is derived as equation (2.15). The predicted efficiency of the 2 kW PFC preregulator is obtained based on the loss model. The intermediate stage is a buck step-down converter which converts 230V dc output of PFC preregulator into 130V dc. This voltage is supplied to the C-dump converter-based PMBDC drive.

The measured efficiency is obtained from the ratio between output power and input power of the 2kW buck converter. The voltage and current in the input and output side are measured and multiplied to obtain input and output power.

The loss model of 2kW buck converter is derived in terms of switch duty cycle d_1 and d_2 based on Table 4.6 as,

$$P_{2kW}(buck) = (16.75)(d_1 + d_2)d_2^2 + \left[30.22 + (68.17)\sqrt{d_1} + (1.04)\sqrt{d_2}\right]d_2 + 6.99 \text{ , W.} \quad (5.21)$$

It should be noted that the constant term in the loss model is the sum of the switching loss of a freewheeling diode and the R-C-D type snubber loss of a buck switch device.

The ratings for major power components of C-dump converter based PMBDC drive are summarized in Table 5.4. Based on this table, the loss models of the major power components are derived and tabulated in Table 5.5. The loss models in Table 5.5 will be used to evaluate the overall efficiency of the drive system.

The loss model in terms of d, I_p, d_r and I_r in C-dump converter based PMBDC drive is obtained based on loss equations in Table 5.5.

$$P_{PMBDC} = \left[0.65 - (0.04)d\right]dI_p^2 + \left[0.36 + (0.87)(1-d)\sqrt{1-d}\right]I_p - (3.96)d + \left[0.63 - (0.11)d_r\right]d_r I_r^2 + \left[2.32 - (1.50)d_r + (2.40)d_r\sqrt{d_r}\right]I_r + 69.32 \text{ , W.} \quad (5.22)$$

It should be also noted that the motor winding loss is also included in this model in addition to the loss equations defined in Table 5.5. The constant term in the obtained loss model consists of the switching losses of three main phase diodes and a recovery diode, the R-C-D type snubber losses of three main phase switches and a recovery switch and the R-C type snubber losses of three main phase diodes and a recovery diode.

Table 5.4
Ratings for key power components in C-dump PMBDC drive.

Device	**Duty cycle**	**Ratings**		
		Voltage	**Current**	
			Peak	**RMS**
Phase switch	d	$E+\Delta V_o$	I_p	$I_p\sqrt{\frac{d}{m}}$
Phase diode	1-d	$E+\Delta V_o$	I_p	$I_p\sqrt{\frac{1-d}{m}}$
Recovery switch	d_r	$E+\Delta V_o$	I_r	$I_r\sqrt{d_r}$
Recovery diode	1-d_r	$E+\Delta V_o$	I_r	$I_r\sqrt{1-d_r}$
$\boldsymbol{C_o}$	1	$E+\Delta V_o$	I_r	$I_r\sqrt{d_r}$
$\boldsymbol{L_o}$	d_r	$E+\Delta V_o$-V_{dc}	I_r	$I_r\sqrt{d_r}$

Table 5.5
Losses for key power components in C-dump PMBDC drive.

Device	Duty cycle	Losses	
		Conduction	Switching
Phase switch	d	$I_p^2 \cdot \frac{d}{m} \cdot R_{ds}(on)$	$\frac{1}{2} E I_p f_c (t_r + t_f)$
Phase diode	1-d	$\frac{(1-d)}{m} \cdot I_{pd} V_{fp}$	$\frac{(1-d)}{m} \cdot E_{rr} f_c$
Recovery switch	d_r	$I_r d_r V_{CE}(sat) \sqrt{d_r}$	$\frac{1}{2} E I_r f_c (t_r + t_f)$
Recovery diode	1-d_r	$I_r (1-d_r) V_{fr}$	$E_{rr} f_c$
$\boldsymbol{C_o}$	1	$I_p^2 \cdot \frac{d(1-d)}{d} \cdot ESR$	$I_r^2 d_r (1-d_r) \cdot ESR$
$\boldsymbol{L_o}$	d_r	$d_r I_r^2 R_o$	-

where,

$R_{ds}(on)$ = drain-to-source on-resistance of a MOSFET switch, Ω

$V_{CE}(sat)$ = collector-to-emitter saturation voltage of an IGBT switch, V

ESR = equivalent series resistance of energy recovery capacitor, Ω

R_o = dc resistance of energy recovery inductor, Ω

5.5.2 Experimental Setup and Method

The simplified block diagram of the test setup is shown in Figure 5.16. The efficiency tests are performed with and without the PFC preregulator. The front-end converter consists of either a combination of a PFC preregulator and a buck step-down converter or bridge rectifier. The output voltage of the PFC preregulator is greater than the peak input voltage as explained in Chapter 2. The terminal voltage of the PMBDC is 130V. A step-down converter is necessary to match the output voltage of the PFC preregulator with PMBDC voltage. Without a PFC preregulator, the variable input source voltage is utilized to maintain 130V dc bus voltage. The same MOSFET-based C-dump converter which is explained in section 5.4.3 is used for a PF corrected PMBDC drive. A 4hp PMBDC from Kollmorgen is selected to implement the VSD system. For the load generator, an 1hp separately excited dc motor from Integrated Electric is used. The ratings of these machines are given in the Appendix B. The four-quadrant controller developed and tested in section 5.4 is modified to drive 4hp PMBDC. Even though the 4hp PMBDC is used for this experiment, the test power is limited to 280W due to the lower power rating and speed of the load generator.

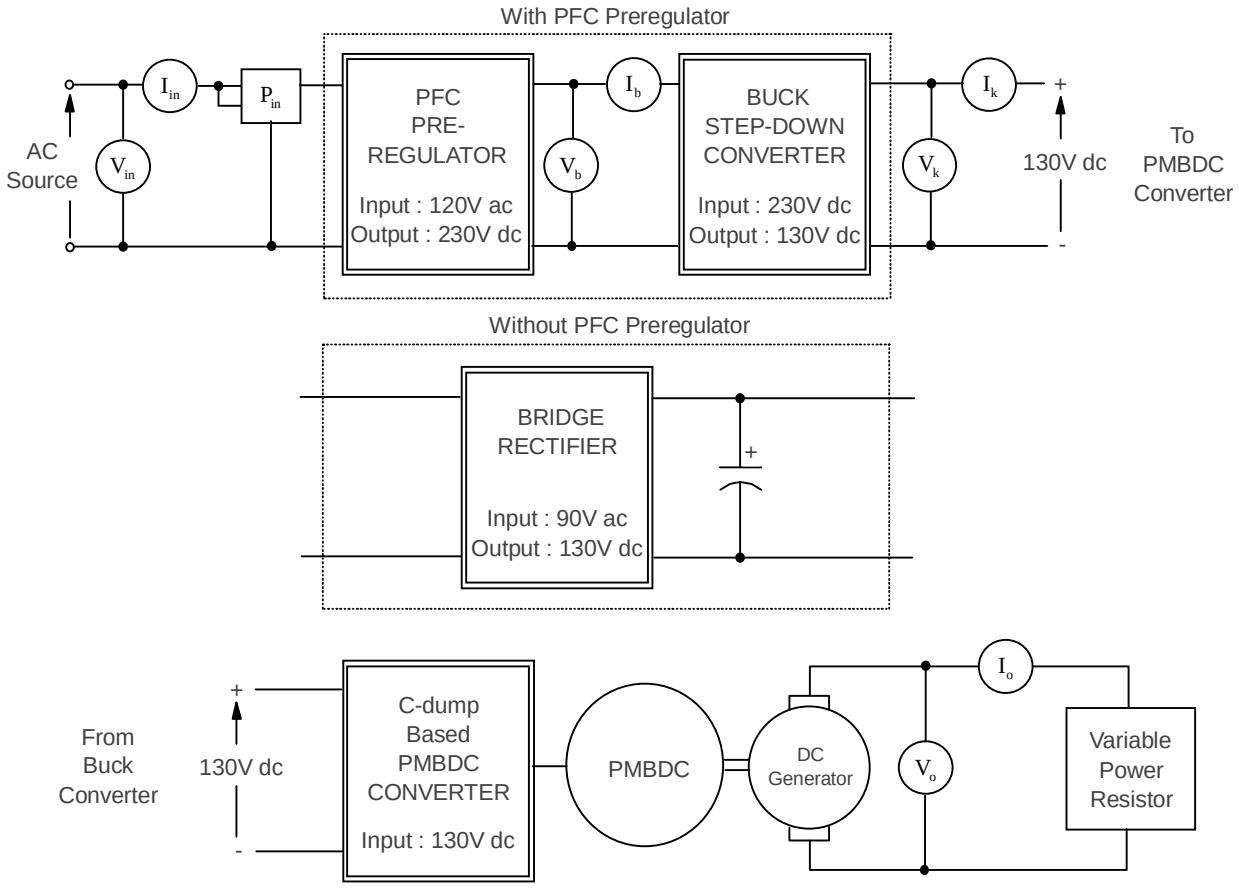


Figure 5.16 Test setup for the input PF-corrected PMBDC-based VSD system.

5.5.3 Discussion on Experimental Results

Efficiency evaluation of the developed 2kW buck converter

The predicted and measured efficiencies of 2kW buck converter are shown in Figure 5.17(i). The tested output power is from 100W to 1.5kW due to the limitation of the maximum power rating of the instrument. Both efficiencies are closely matched over the entire output power range and therefore the derived loss model is validated. The efficiency prediction error of 2kW buck converter is evaluated and illustrated in Figure 5.17(ii) . The error is within +1 to -3.5% over the entire output power range. The statistical analysis of the prediction error is tabulated in Table 5.6 shows excellent match between the measured and predicted efficiencies.

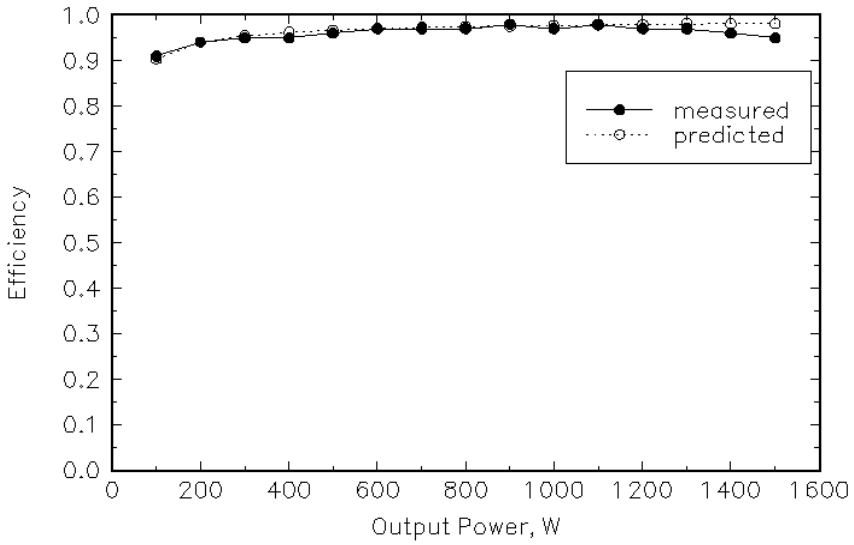


Figure 5.17(i) Efficiency of a 2kW buck converter.

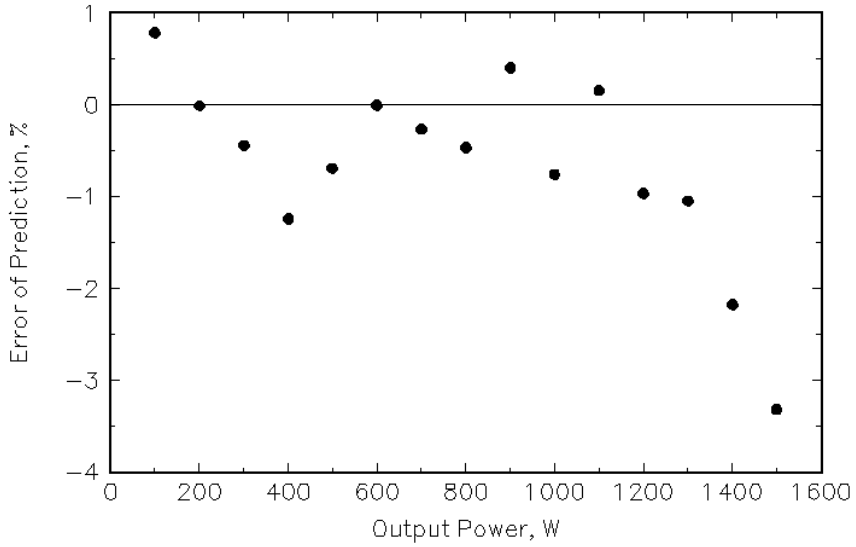


Figure 5.17(ii) Error of prediction versus output power for 2kW buck converter efficiency.

Table 5.6
Statistical analysis of efficiency prediction errors for 2kW buck converter.

	Fig. 5.12(i)
Total Observation	15
Minimum Error	-3.32
Maximum Error	0.79
Mean	-0.67
Median	-0.46
Variance	1.07
Standard Deviation	1.03
Standard Error	0.27

Efficiency of the PMBDC drive system

The predicted efficiency of the PMBDC drive system is obtained from considering conduction and switching losses in the main power components using equations given in Table 5.7. The predicted and measured efficiency with and without the input PFC are shown in Figures 5.18(i) and (ii) with friction load, respectively. The output power and speed ranges are determined according to the ratings of the dc generator whose specification is shown in Appendix B. The maximum speed is limited to 1,500r/min to match the rated speed of DCM which serves as a load. The friction type load is used and the maximum tested output power is limited to about 280W at 1,500r/min. The normalized maximum tested output becomes 0.1pu with considering the rated output power of PMBDC, 4hp at 4,900r/min, as the base power. The low efficiency in both cases is due to the reduced operational power of PMBDC drive. The efficiency with the PFC and step-down converter is lower than without the PFC because of the two-stage power conversion.

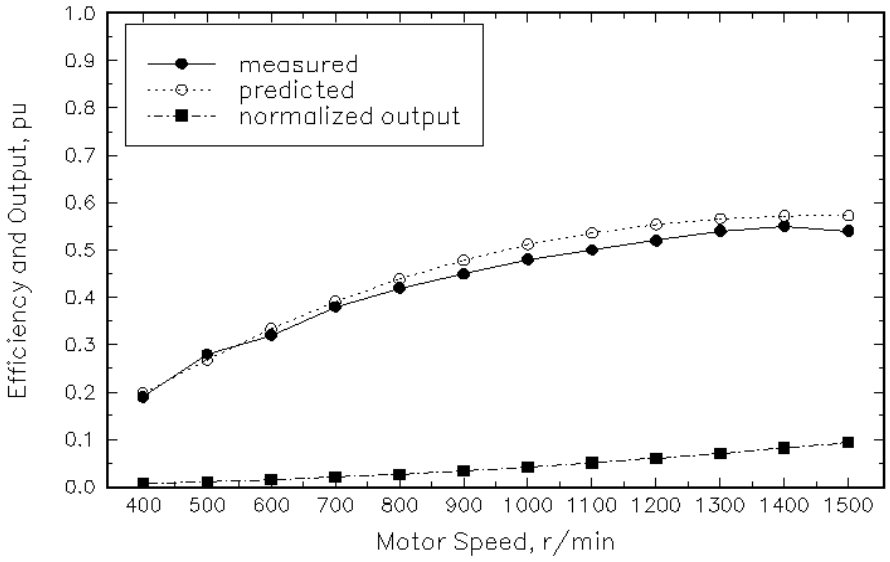
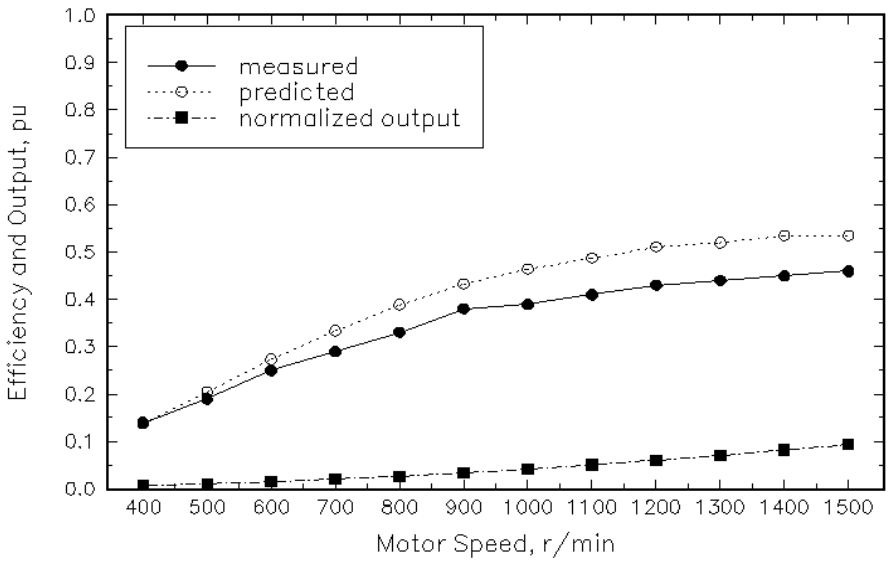


Figure 5.18 (i) without PFC



(ii) with PFC

Figure 5.18 Predicted and measured overall system efficiency and normalized tested output of the PMBDC drive with and without PFC.

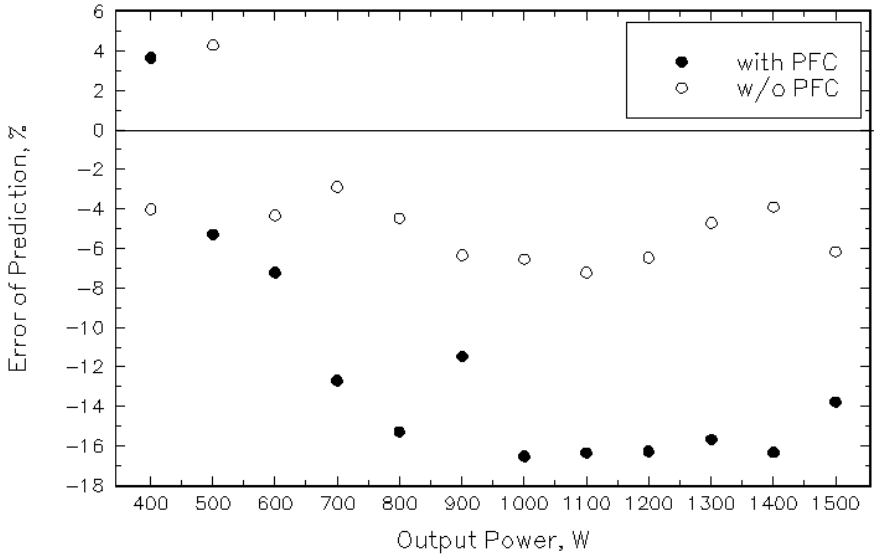


Figure 5.19 Efficiency prediction error versus PMBDC speed with and without PFC preregulator.

Table 5.7
Statistical analysis of efficiency prediction errors for PMBDC drive system with and without PFC preregulator.

	Fig. 5.20(i) without PFC	Fig. 5.20(ii) with PFC
Total Observation	12	12
Minimum Error	-7.22	-16.53
Maximum Error	4.29	3.64
Mean	-4.40	-11.95
Median	-4.59	-14.54
Variance	9.29	37.94
Standard Deviation	3.05	6.16
Standard Error	0.88	1.78

The efficiency prediction error is illustrated in Figure 5.19 to evaluate the derived loss model. The error settles within +5 to -8% without the PFC preregulator. With PFC preregulator, the error becomes -18% after 600r/min due to the error in d_2 measurement. Table 5.7 shows the statistical analysis results of the prediction error. The prediction error without the PFC has a narrower dispersion than the one with the PFC.

Input ac current

The input current harmonics are much improved with the input PFC preregulator as shown in Figures 5.20(i) and (ii). The modified IEC 1000-3-2 Class D relative limit is applied to compare both cases and the results are shown in Figure 5.21. The magnitudes of the input current harmonics with the PFC lay well within the limit. The magnitude of the input ac current is shown

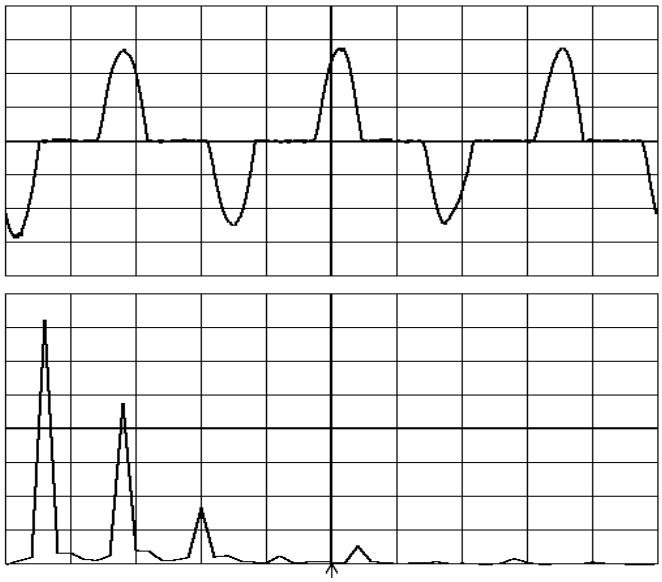
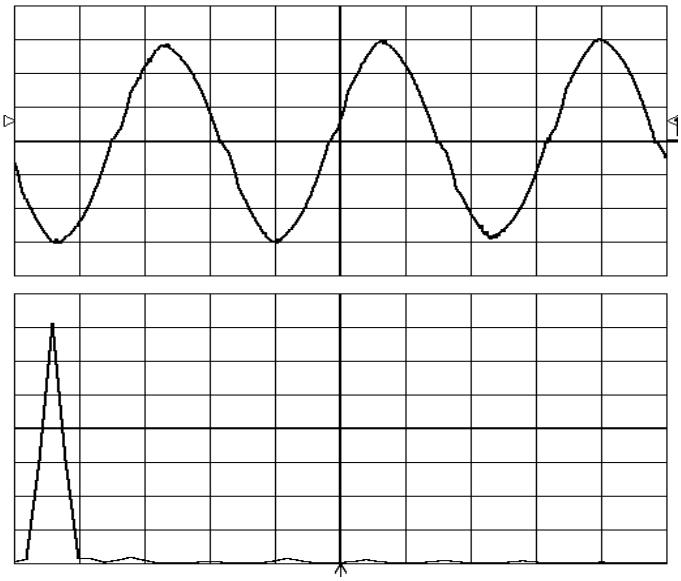


Figure 5.20 (i) without PFC



(ii) with PFC

Figure 5.20 Input current and its harmonic spectra without and with
PFC preregulator at 1500r/min.
Input current(top): 5A/div, 5ms/div / FFT (bottom): (i) 1A/div (ii) 2A/div, 100Hz/div

in Figure 5.22. The magnitude of the input current without PFC circuit is growing bigger than the one with the PFC as power output level increasing. This is due to the increase of harmonic components in the ac current which yields the increase of the rms current as explained in Chapter 2.

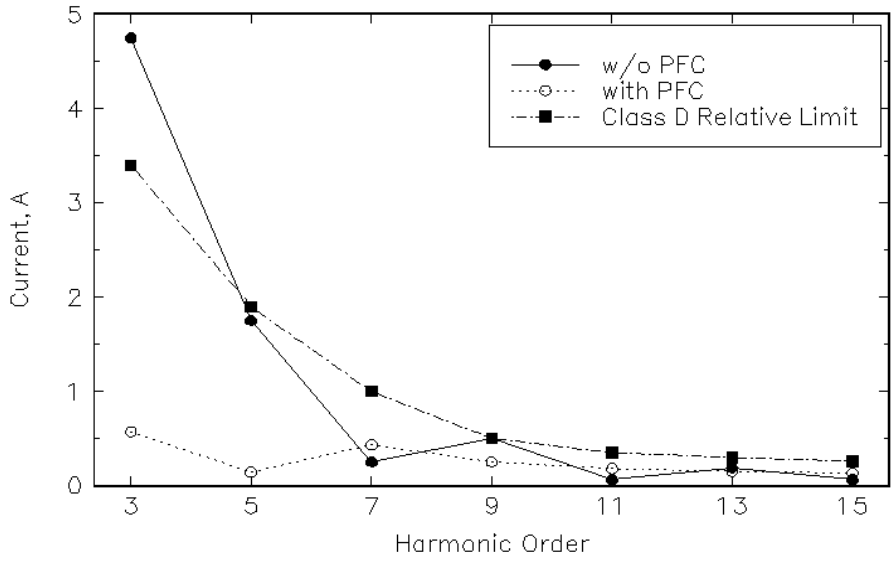


Figure 5.21 Comparison of measured input current harmonics from Figure 5.20
with modified IEC 1000-3-2 Class D harmonic current limits.

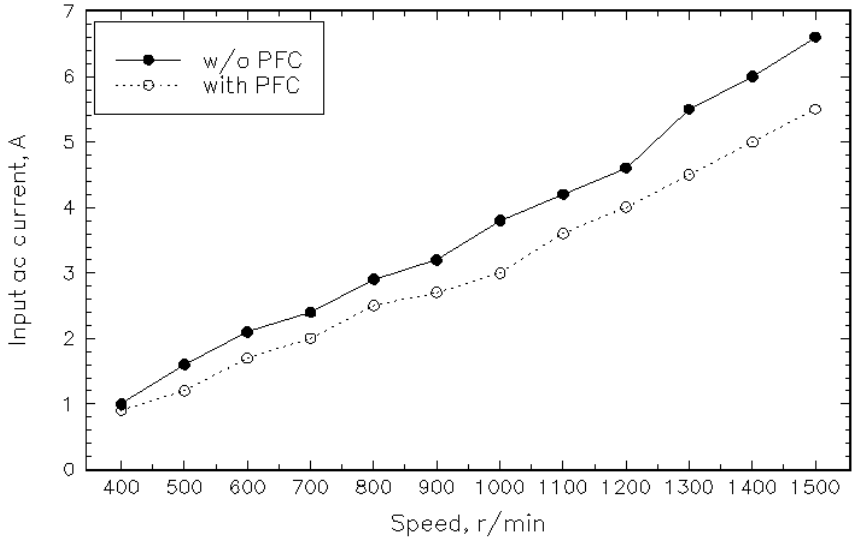


Figure 5.22 Magnitude of the input ac current with and without PFC.

5.6 Conclusions

The C-dump converter which has one switch per phase has been identified for use in the control of a PMBDC motor in this study. The identified topology lends itself to the four-quadrant operation, compact packaging, elimination of shoot-through fault, low number of power supplies and gate drive requirements, making it a low-cost PMBDC-based VSD system. The proposed drive system has been analyzed and design guidelines have been developed for the given PMBDC motor ratings. The design considerations for the PMBDC motor for use with the proposed topology have been derived in terms of maximum motor speed and peak recovery current. The feasibility of the proposed drive scheme is verified with an experimental laboratory prototype.

The PFC is employed in PMBDC-based VSD system to improve the input PF. The magnitude of the input current harmonics and overall system efficiency are investigated in the proposed power factor corrected PMBDC-based VSD. The four-quadrant controller for the PMBDC-based VSD is developed. The feasibility of the drive scheme is verified with an experimental laboratory prototype PMBDC motor. The input current harmonics are greatly reduced with the PFC and meet the IEC 1000-3-2 limits. The overall drive system efficiency is decreased due to the cascaded front-end converters. The magnitude of the input ac current with PFC is smaller than the one without a PFC, because of the less harmonic contents in the current.

The advantages of the proposed drive seem to match the stiff high reliability, compact packaging and dynamic performance requirements of the emerging, high volume, but low cost appliance VSD applications.