Chapter 6. Input PF-Corrected DCM-Based VSD System

6.1 Introduction

The effects of the input PFC for the DCM-based VSD are presented in this chapter. The analytical expressions to predict the overall drive system efficiency are developed with and without the input PFC preregulator. Other important benefits with the input PFC are investigated such as a reduction of magnitude of input current and high input power factor. A low-cost, four-quadrant controller for the DCM-based VSD is developed and its performance is verified with experiment and simulation.

VSD utilizing the DCM is predominant in industrial and domestic applications. The low- to medium-power level VSDs using the DCM are numerous in home appliances, automobile applications and so on. The dc power for the DCM-based VSD for home appliance application is supplied mainly by a full-wave rectifier circuit with filter capacitors. This type of power supply is simple to implement but there are some drawbacks as explained in Chapters 1 and 2. The most significant disadvantage is the generation of odd numbered current harmonics. These harmonics propagate into the main ac power source line, generating problems such as an increase of EMI, distortion of current, transfer of less real power to the load, requirement of heavy wire size and so on. Almost all of the currently available VSDs do not have any means for input PF improvement in their circuit. For a very low power VSD, an insertion of a small inductor may reduce the magnitude of current harmonics [36], but the size of a low frequency inductor may be big and it does not eliminate current harmonics effectively. The boost active PFC preregulator circuit analyzed and tested in Chapter 2 will be employed to improve the input PF of the DCM-based VSD.

The selection of a power converter topology for the DCM-based VSD mainly depends on the requirements of the specific operating quadrants. The simplest topology is the single switch dc-to-dc chopper [1]. The operation of the single switch chopper is limited to the single-quadrant. The versatile power converter topology for the DCM-based VSD is a full-bridge (H-bridge) converter which can operate in all four operational quadrants. The definition of an operational quadrant is based on the explanation in Chapter 5, where the torque and the speed corresponds to the motor armature current and voltage, respectively. In full quadrant operation, a motor requires the rapid deceleration. The fast deceleration of a motor generates enormous energy because it operates as a generator. This causes the rising of the dc bus voltage. The dynamic braking [1] can help a motor to decelerate quickly by dissipating the excessive energy as heat through a resistor. The drawback of dynamic braking is the requirement of an additional switch device, control circuit and power resistor, which may reduce the overall drive system efficiency. The regenerative braking method can be employed when the efficiency is of high concern. This method recovers the excessive energy to the source by using a two-quadrant front-end converter. Although the control complexity will be increased, both the energy recovery and PFC can be implemented into the two-quadrant ac-to-dc converter [44, 46]. Neither the dynamic braking nor regenerative braking are considered in DCM-based VSD study mainly because the steady-state system efficiency and input current harmonics were studied. But the dynamic response of the developed four-quadrant controller when the direction of rotation of the motor is changed is investigated to verify the performance of the controller.

This chapter is organized as follows: in Section 6.2, analytical derivation of switch duty cycle is discussed. A four-quadrant controller development is explained in Section 6.3. In Section 6.4, the experimental setup is explained and the results of experiment and simulation are discussed. The PF corrected DCM drive is introduced in Section 6.5. The conclusions on DCM-based VSD system will be followed in Section 6.6.

6.2 Analysis of DCM-Based VSD System

6.2.1 Derivation of Duty Cycle

The simplified schematic diagram of the implemented MOSFET-based H-bridge power circuit in this study is shown in Figure 6.1. The equivalent circuit of the armature winding of a dc motor is shown in the dotted box [1]. R_a and L_a are the armature resistance and inductance, respectively. The motor back emf voltage is expressed as e_b. The analytical expressions at steady-state are derived only at the first quadrant operation. The normalized expression of the switch duty cycle is obtained in terms of motor speed, torque and V_{dc}. The duty cycle of the switch is utilized to predict the current and losses in switches and freewheeling diodes. The parasitic elements are not considered in all the derivations.

The operational waveforms of the first-quadrant operation in the continuous conduction mode are shown in Figure 6.2. There are two distinct operational modes in the first-quadrant operation. Mode I corresponds to the state when both T_1 and T_2 switches are turned on. The armature current is increased exponentially in this mode. It is decreased exponentially in Mode II which relates to T_1 is turned off and T_2 remains on state. The armature current keep flowing in the same direction through D_4 and T_2. The equivalent circuits of two operational modes in the first quadrant operation are shown in Figure 6.3.

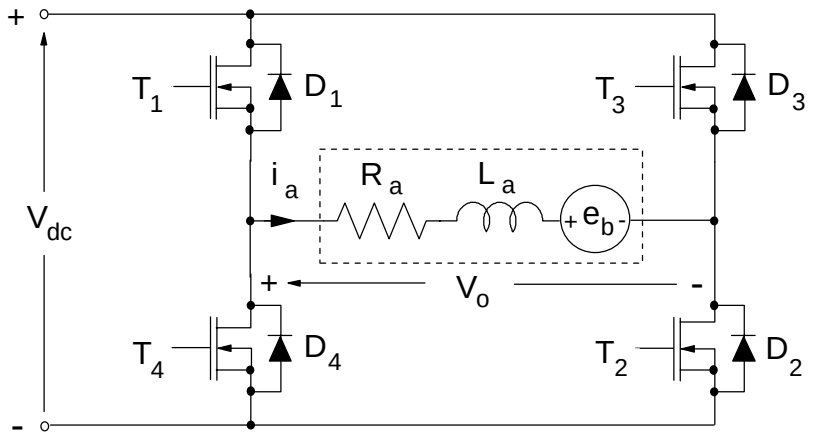


Figure 6.1 MOSFET-based H-bridge converter configuration for DCM drive.

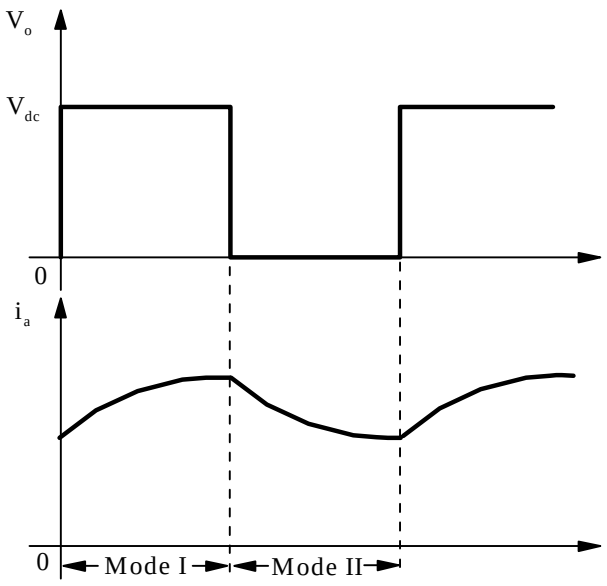
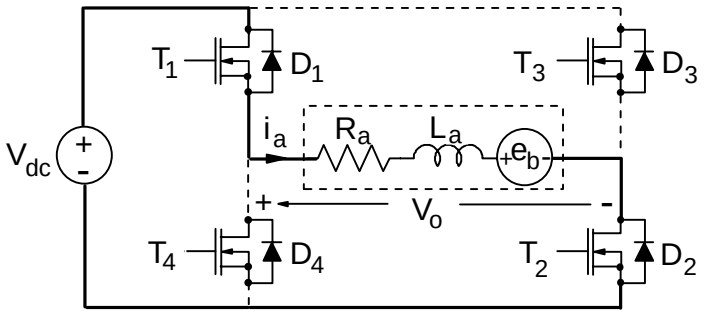
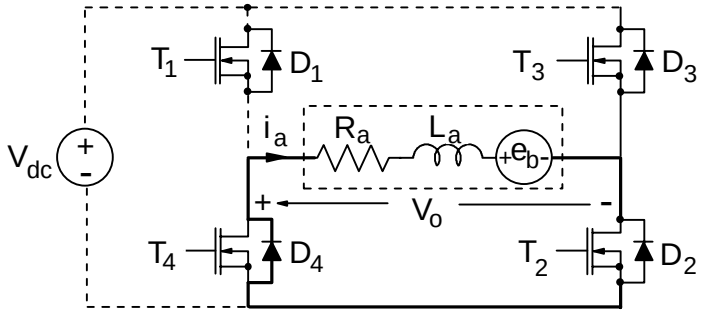


Figure 6.2 Operational waveforms of V_o and i_a in first-quadrant.



Mode I. T_1 and T_2 on



Mode II. T_1 off, T_2 on

Figure 6.3 Equivalent circuits of two operational modes in first-quadrant operation.

From Figure 6.3, the average armature current is expressed as [1],

$$I_{ave} = \frac{V_o - e_b}{R_a} \text{ , A.} \tag{6.1}$$

where,

$$V_o = d \cdot V_{dc} \text{ , V.} \tag{6.2}$$

$$e_b = \omega_m \cdot K_b \text{ , V.} \tag{6.3}$$

and d is the duty cycle, e_b is the induced emf, ω_m is the motor speed, and K_b is the emf constant.

The average electromagnetic torque, written in terms of duty cycle and motor speed, is as follows,

$$T_{ave} = K_b \cdot I_{ave}$$

$$= \frac{K_b(d \cdot V_{dc} - K_b \cdot \omega_m)}{R_a} \text{ , N·m.} \tag{6.4}$$

The normalized expression of the electromagnetic torque is obtained as,

$$T_{en} = \frac{d \cdot V_{dcn} - \omega_{mn}}{R_{an}} \text{ , pu.} \tag{6.5}$$

where,

$$R_{an} = \frac{I_b \cdot R_a}{V_b} \text{ , pu.}$$

$$V_{dcn} = \frac{V_{dc}}{v_b} \text{ , pu.}$$

$$\omega_{mn} = \frac{\omega_m}{\omega_b} \text{ , pu.}$$

Rearranging equation (6.5) in terms of the duty cycle we have

$$d = \frac{\omega_{mn} + R_{an} \cdot T_{en}}{V_{dcn}}. \tag{6.6}$$

6.2.2 Development of Loss Model

The duty cycle expression plays an important role to estimate the currents in switch and diode. The estimated current in switching device is utilized to predict the conduction and switching losses in it. The ratings and losses of key power components are shown in Tables 6.1 and 6.2. The loss expressions presented in this table are for the single device. In Table 6.2, I_{sw} represents rms switch current and I_d is rms diode current, and I_{bd} is rms current in bridge rectifier.

The actual H-bridge power circuit is implemented with MOSFET power switching devices as illustrated in Figure 6.1. The suppression of the conduction in the body diode is considered because the slow recovery intrinsic body diode of the MOSFET switching device is not suitable to high frequency switching [4]. The drawback of the suppression circuit is that the single diode voltage drop is added to the total switch conduction loss. The R-C-D snubber network is added to improve turn-off characteristics of the switching device.

Based on the derived conduction and switching loss equations in Table 6.2, the model of the total losses in the DCM-based VSD system which employed the H-bridge power circuit is obtained in terms of the rated output power, P_{ro} and the duty cycle, d as follows;

Table 6.1
Ratings of power components in DCM drive.

Device	**Duty Cycle**	**Ratings**		
		Voltage	**Current**	
			Peak	**rms**
Bridge Diode	1	V_{dc}	I_{pk}	$\frac{I_{pk}}{2}$
Switch	d	V_{dc}	I_{pk}	$I_{pk}\sqrt{\frac{1+d}{2}}$
Diode	1-d	V_{dc}	I_{pk}	$I_{pk}\sqrt{\frac{1-d}{2}}$

Table 6.2
Losses of power component in DCM drive.

Device	**Duty Cycle**	**Losses**	
		Conduction	**Switching**
Bridge diode	1	$I_{bd}\cdot V_{fb}$	-
Switch	d	$I_{sw}^2\cdot R_{ds}(on)$	$\frac{1}{2}V_{dc}\cdot I_{sw}\cdot f_s(t_r+t_f)$
Diode	1-d	$I_d\cdot V_f$	$E_{rr}f_s$

$$P_{DCM}=\left[9.99-(7.29)d+(17.28)d^2\right](10^{-5})P_{ro}^2 +\left[0.02+(0.02)(\sqrt{1+d}+\sqrt{1-d})\right]P_{ro}+54.64 \text{ , W.} \quad (6.7)$$

The constant term consists of the switching losses in two freewheeling diodes and the two conventional R-C-D snubber circuits. The diode bridge conduction losses should be added to this loss model when the overall system efficiency without an input PFC preregulator is evaluated. This equation is utilized to predict the overall VSD system efficiency and the obtained predicted efficiency will be compared with the experimental result.

6.3 Implementation of Four-Quadrant Controller

The definition of the operational quadrant is based on Figure 5.5(i) in Chapter 5. It should be noted that the operational quadrant of DCM-based VSD is determined by the polarities of the current command signal, i_{ap}^{*}, and the voltage command signal, v_{cp}^{*}, which corresponds to the motor torque and motor speed, respectively. The relationship between these polarities, operational quadrants and switching status of the switching device in the developed DCM-based VSD system is summarized in Table 6.3. For example, the first-quadrant operation is presumed when the polarities of v_{cp}^{*} and i_{ap}^{*} are positive. In this case, switches T_1 and T_2 are turned on. Other operations follow the defined switching sequences in the table.

Table 6.3
Switching logic for four quadrant operation of DCM-based VSD.

		Speed	Torque	Switches			
Mode of Operation	**Quadrant**	v_{cp}^{*}	i_{ap}^{*}	T_1	T_2	T_3	T_4
Forward Motoring (FM)	**I**	**+**	**+**	**ON**	**ON**	OFF	OFF
Forward Regeneration (FR)	**IV**	**+**	**-**	OFF	OFF	OFF	**ON**
Reverse Motoring (RM)	**III**	**-**	**-**	OFF	OFF	**ON**	**ON**
Reverse Regeneration (RR)	**II**	**-**	**+**	OFF	**ON**	OFF	OFF

The simplified block diagram of the implemented DCM-based VSD with a four-quadrant controller is shown in Figure 6.4. The fixed dc voltage source supplies the power to the field winding of the motor. The unipolar speed command signal is applied to operate in all four

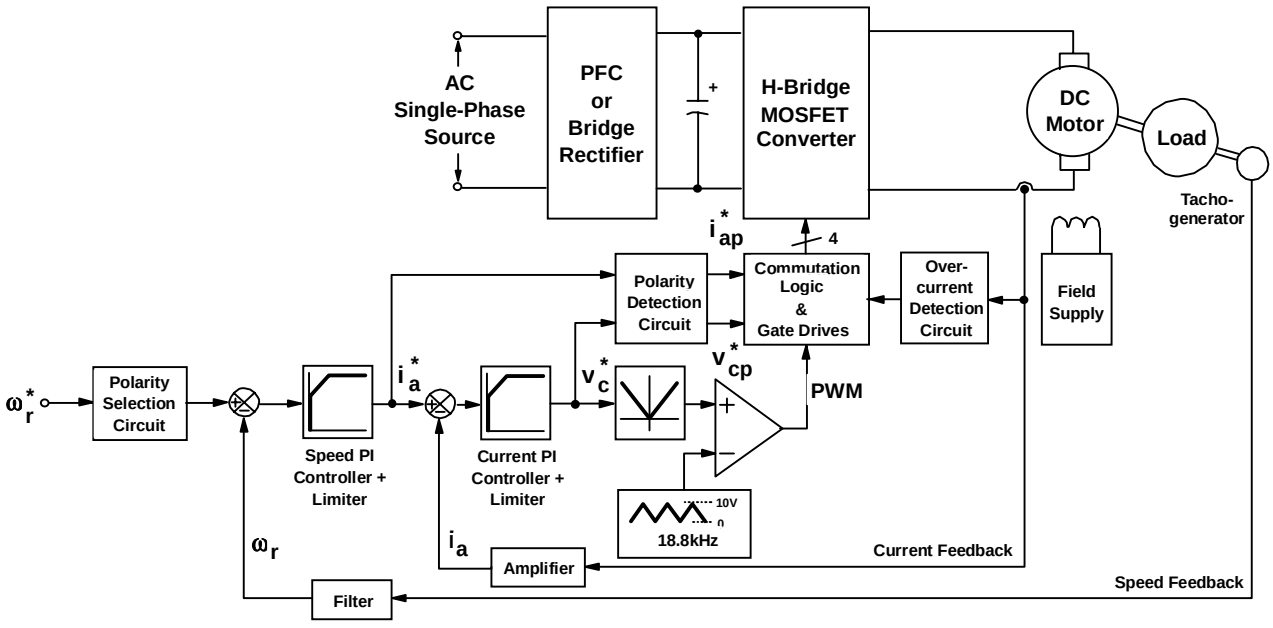


Figure 6.4 Simplified block diagram of the developed DCM-based VSD with four-quadrant controller.

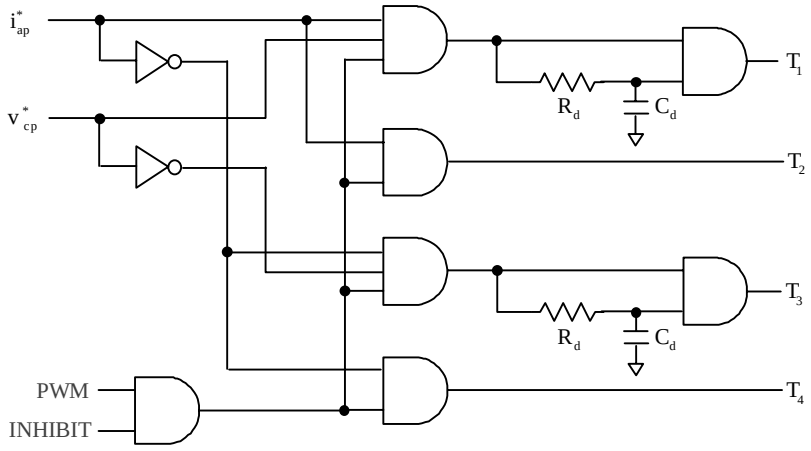


Figure 6.5 Simplified commutation logic diagram of the developed four-quadrant controller for DCM-based VSD system.

quadrants. The commanded speed signal goes to the polarity selection circuit which decides the direction of rotation of the DCM. The polarity of the unipolar speed command signal is inverted through an inverting amplifier to operate in negative speed regions - second- or third-quadrant. The speed feedback is obtained from a dc tachogenerator. The sensed speed feedback signal is applied to a low pass filter to remove the high frequency noise. The speed error signal which is the difference between the commanded and sensed speed signals is applied to the speed PI controller circuit. The output of the speed PI circuit is the armature current command signal, i_a^* which corresponds to the torque. The commanded armature current signal is compared with the sensed armature current signal and applied to the current PI controller circuit. The output of the current PI controller is the voltage command signal, v_c^*. The polarities of i_a^* and v_c^* are identified through the polarity detection circuit. The polarity detection circuit consists of two voltage comparator circuits to detect the polarity of the commanded signals for the armature current, i_a^* and voltage, v_c^*. The armature voltage command signal is applied to the precision full-wave rectifier circuit to get the absolute value, $\left|v_c^*\right|$. The absolute value of the voltage command signal is compared with a 18.8kHz triangular waveform to generate a PWM signal. The generated PWM signal and identified polarity informations, i_{ap}^* and v_{cp}^*, are applied to the commutation logic circuit. The implemented steering logic diagram for a four-quadrant DCM-based VSD is shown in Figure 6.5. The INHIBIT signal is the output of the overcurrent detection circuit and R_d and C_d provide dead-time for the two upper switches, T_1 and T_3, to prevent shoot-through fault in each phase leg which consists of T_1 and T_4 or T_3 and T_2. The commutation logic circuit distributes the PWM signal to the appropriate switching device based on the switching strategy tabulated in Table 6.3. The load motor is a PMBDC motor which operates as a dc generator which generates three-phase sinusoidal voltages, thus they are rectified by a three-phase full-wave bridge rectifier circuit and filtered through capacitors. The rectified dc voltage is applied to the variable resistor bank. The friction type load is used for a test. The range of the test power is decided based on the rated speed and output power of the DCM and PMBDC. The details of the DCM and PMBDC is listed in Appendix B.

6.4 Design Verification of the Developed Controller

The experimental verification of the developed four-quadrant controller is presented in this section along with the simulation. PI gains of the speed and current control loops are summarized in Table 6. 4.

The response of the speed reversal in the implemented DCM-based VSD system is shown in Figure 6.13. The rise time of the speed response is 0.4s for speed changes between -1,000r/min and +1,000r/min. The implemented four-quadrant controller shows a good control performance.

Table 6.4
PI gains of the speed and current control loops.

Gain	Speed Loop	Current Loop
Proportional	16.67	293.33
Integral	10.64×10^{-3}	66.84

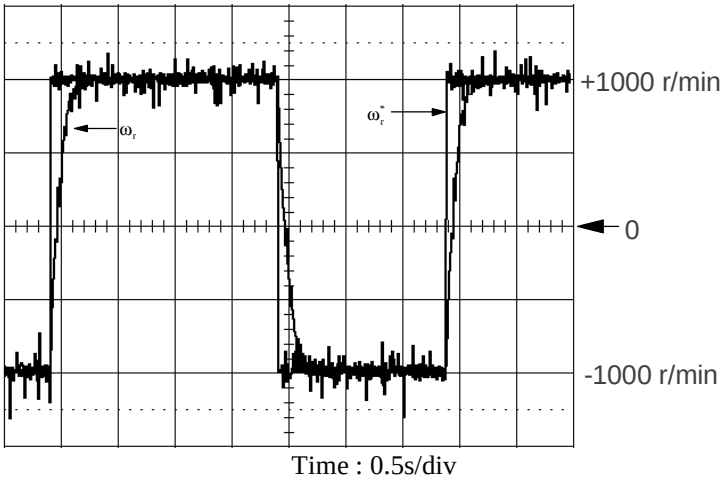


Figure 6.6 Speed loop response at ±1,000r/min.

The modeling of the DCM-based VSD system includes PI speed and current control loops, DCM and load [1]. The armature current, i_a, and motor speed, ω_m, are selected as the state variables, because the DCM-based VSD in this study is operating in constant torque mode. The mathematical models of DCM and load in differential equation form are [1]

$$\frac{di_a}{dt} = -\frac{R_a}{L_a}\cdot i_a - \frac{M}{L_a}\cdot i_f \cdot \omega_m + \frac{1}{L_a}\cdot V_a . \tag{6.8}$$

$$\frac{d\omega_m}{dt} = \frac{M}{J}\cdot i_a \cdot i_f - \frac{B}{J}\cdot \omega_m - \frac{T_l}{J} . \tag{6.9}$$

The transfer functions of subsystems, such as PI current and speed controllers, are based on equations in Section 3.4. The flowchart for simulation of DCM-based VSD is shown in Figure 6.7. The simulated speed response is shown in Figure 6.8. The speed response shows good match with the experimental result in Figure 6.6.

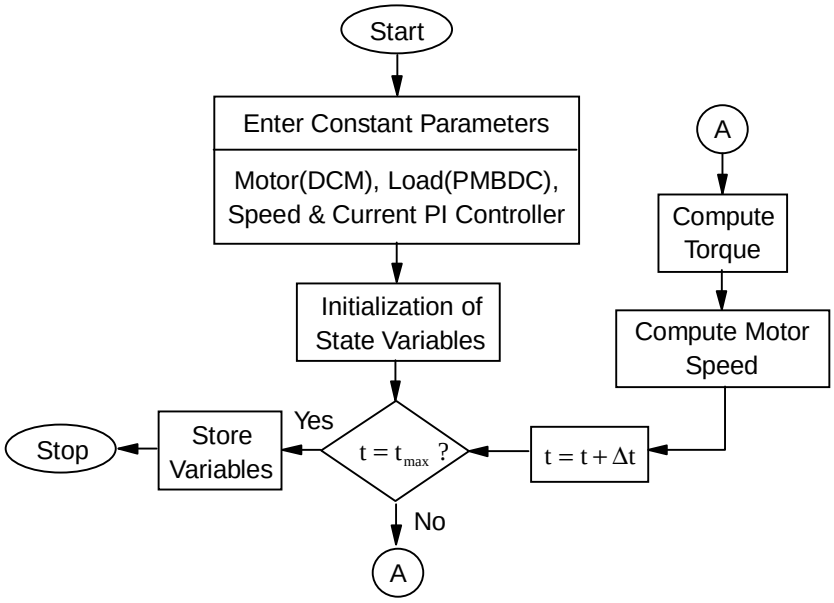


Figure 6.7 Flowchart for simulation of DCM-based VSD system.

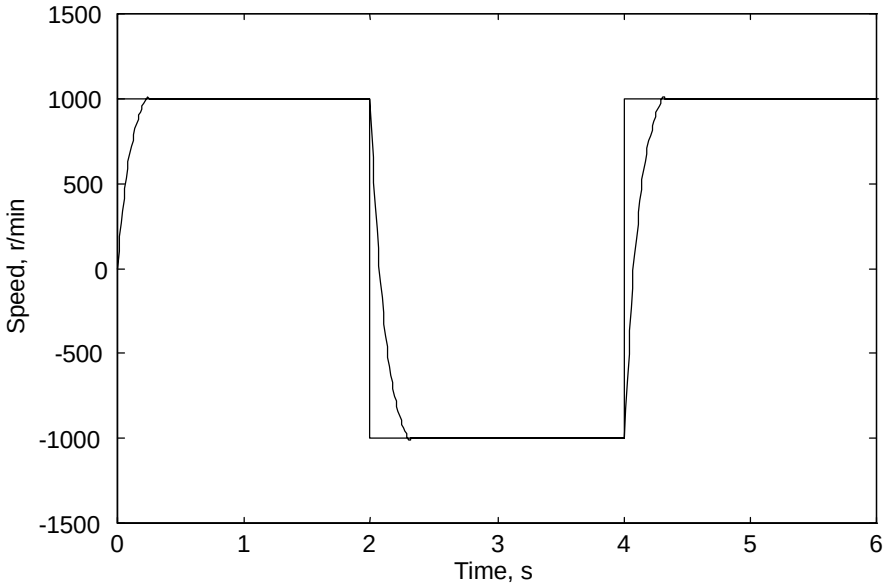


Figure 6.8 Simulated speed response at ±1,000r/min.

6.5 Input PF-Corrected DCM Drive

The input PFC for the developed four-quadrant DCM-based VSD are introduced in this section. The effects of the input PFC, such as input current harmonics, input power factor, magnitude of input current and overall drive system efficiency are investigated. The experimental verification of the input PFC is followed by the efficiency evaluation. The predicted efficiency of the drive system is obtained with loss equations in Section 6.2.2. Various input variables are studied with and without input PFC preregulator.

6.5.1 Experimental Setup

The experimental setup for the four-quadrant DCM-based VSD is shown in Figure 6.9. The input variables, such as the ac input current, voltage and power are measured with an ac ammeter I_{in}, voltmeter V_{in} and power meter P_{in}, respectively. For the experiment without the PFC preregulator, the PFC preregulator is replaced with a bridge rectifier module. A 2kW PFC preregulator which is fully analyzed and tested in Chapter 2 is used for the experiment with PFC and its details are given in Appendix A. A DCM tested in this experiment is a separately excited type. A 300W PFC preregulator is used for the constant 200V dc field power supply. In this experiment, a three-phase PMBDC motor from Kollmorgen, which was also utilized for efficiency studies in Chapter 5, operates as the generator. The generated three-phase ac voltage is converted into dc by a three-phase bridge rectifier and filter capacitor. The friction type load is presumed and the variable resistor bank is served as the load. With this type of load, the tested speed range is set from 400r/min to 1,500r/min. The maximum tested output power of the DCM-based VSD system is limited to about 280W at 1,500r/min because of the reduced power of PMBDC generator at 1,500r/min with friction type load.

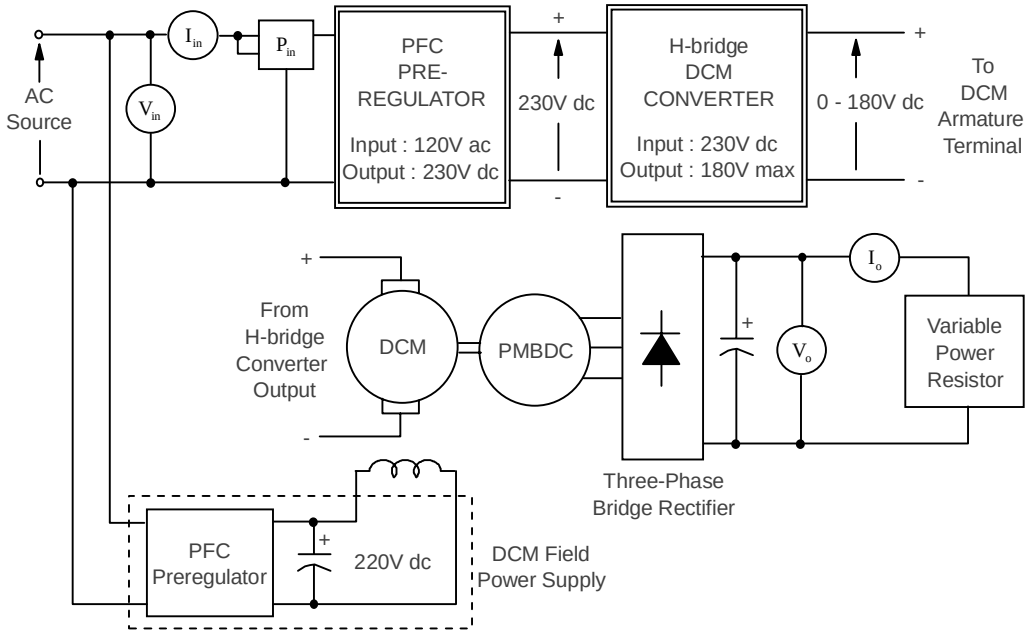


Figure 6.9 Test setup for the input PF-corrected DCM-based VSD system.

6.5.2 Efficiency Evaluation

The rated output current of the PMBDC generator is estimated with the following equation.

$$I_{ro} = \frac{P_{ro} - P_{fw}}{nK_b + 2V_f} \text{ , A.} \tag{6.10}$$

where,

P_{ro}	=	rated output power, W
P_{fw}	=	friction and windage losses of DCM and PMBDC, W
n	=	motor speed, r/min
K_b	=	emf constant of PMBDC, V/(r/min)
V_f	=	forward diode voltage drop in three-phase bridge rectifier.

The rated output current at a particular motor speed is set by adjusting the variable load resistor. The rated output current is monitored with a dc ammeter I_o. A dc voltmeter is used to measure the output voltage as shown in Figure 6.9.

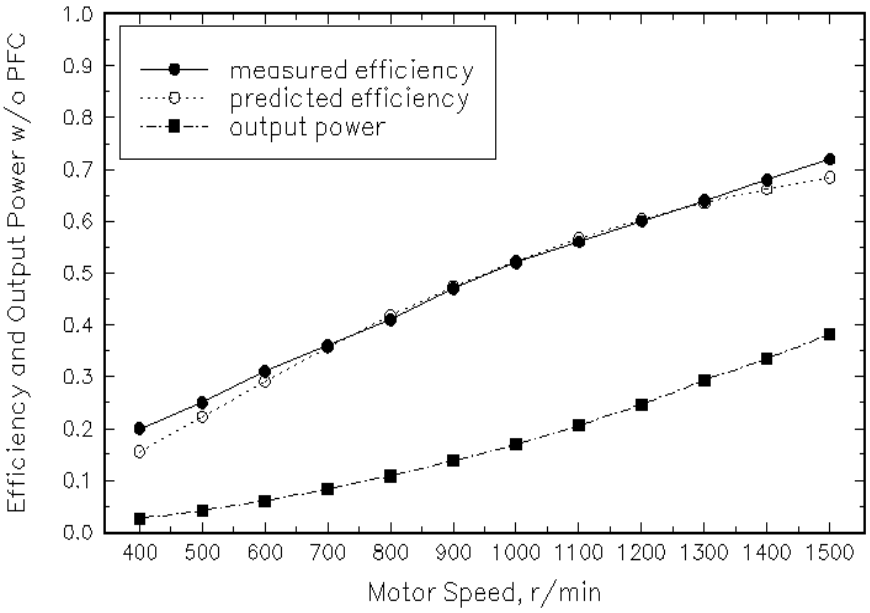
The output power of the DCM is estimated as the sum of the PMBDC generator output and its losses as follows,

$$P_o = \left(V_o + 2V_f\right)I_o + P_{fw} \text{ , W.} \tag{6.11}$$

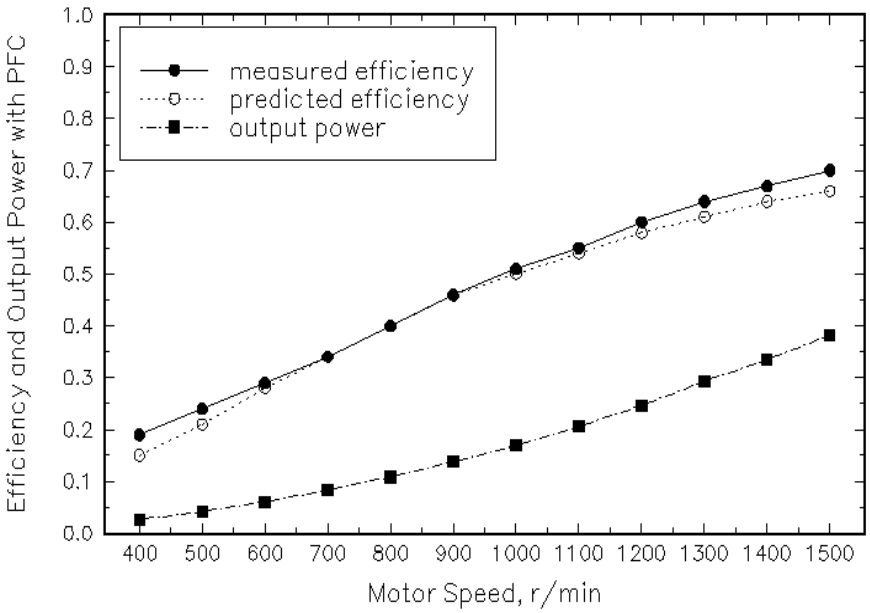
where I_o is the measured output current which is equal to I_{ro}. V_o is the measured output voltage and P_{fw} is the friction and windage losses of DCM and PMBDC set. The friction and windage losses of DCM and PMBDC set is shown in Figure 5.11.

The predicted efficiency of the DCM drive system is obtained from considering loss model shown in equation (6.7). The overall input PF-corrected DCM drive system efficiency is evaluated as the product of the 2kW PFC effciency and the DCM drive system efficiency.

The measured and predicted efficiencies are shown in Figures 6.10(i) and (ii) without and with the PFC, respectively. The efficiency prediction error with and without the input PFC preregulator is illustrated in Figure 6.11. The error becomes large at less than 500r/min, but beyond this speed, it settles down within ±5%. As shown in Table 6.5, the prediction error with the PFC is slightly smaller than without the PFC case. The predicted efficiency is well matched with the measured one over the entire speed range.



(i) without PFC



(ii) with PFC

Figure 6.10 Measured and predicted overall system efficiency and normalized tested output power of DCM drive without and with PFC preregulator.

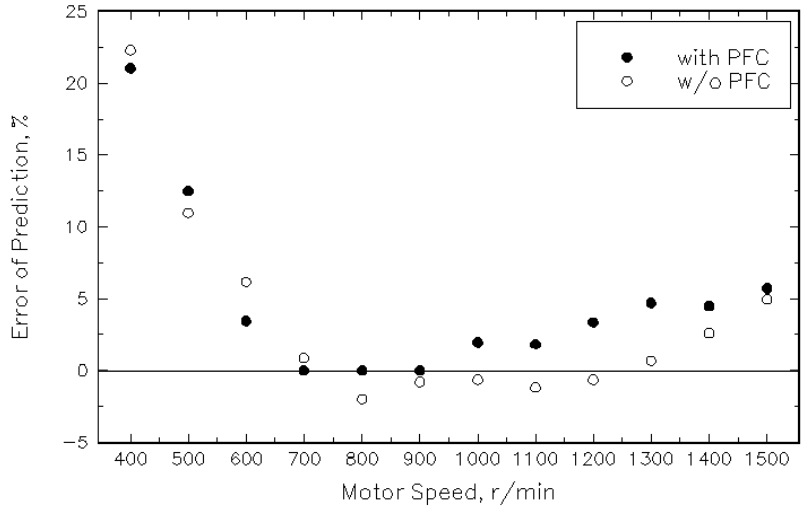


Figure 6.11 Error of prediction versus speed for DCM-based VSD system with and without PFC preregulator.

Table 6.5
Statistical analysis results of efficiency prediction errors for DCM drive system with and without PFC preregulator.

	Fig. 6.10(i) without PFC	Fig. 6.10(ii) with PFC
Total Observation	12	12
Minimum Error	-2.00	0.00
Maximum Error	22.30	21.05
Mean	3.60	4.92
Median	0.77	3.39
Variance	49.01	37.66
Standard Deviation	7.00	6.14
Standard Error	2.02	1.77

6.5.3 Input Variables

Input Current Harmonics

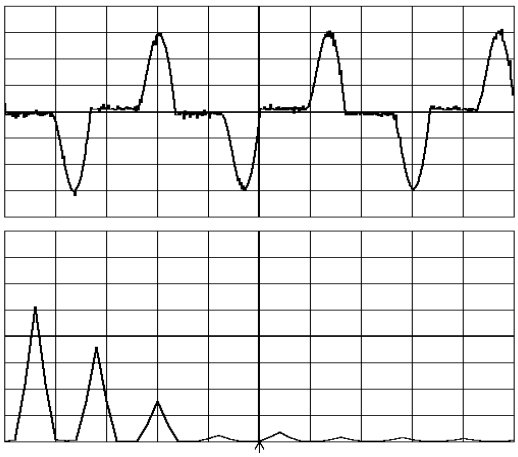
The input current and its harmonic spectra are shown in Figures 6.12(i) and (ii) without and with PFC, respectively. The rich harmonics in the input ac current are greatly reduced with the PFC preregulator. The modified IEC 1000-3-2 Class D relative harmonic current limit shown in Table 1.2 is applied to validate the effectiveness of the PFC. The comparison between the input current harmonics with and without a PFC front-end and IEC 1000-3-2 Class D relative harmonic current limit is illustrated in Figure 6.13. The input current harmonics are improved with significant margin with the PFC preregulator.

Input Power Factor

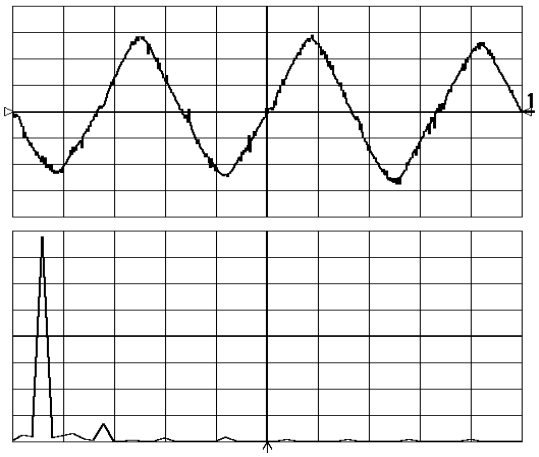
Figure 6.14 shows the comparison of the input power factor between with and without the PFC preregulator in DCM-based VSD system. The input power factor is also significantly improved with the PFC circuit because of the substantial reduction of harmonic contents in the input ac current.

Magnitude of input current

The measured magnitudes of the input ac current with and without the PFC circuit are shown in Figure 6.15. The input current without the PFC circuit increases due to the increase of the harmonic contents as output power increases.



(i) without PFC



(ii) with PFC

Figure 6.12 Input current and its harmonic spectra of DCM drive
at 1,500r/min without and with PFC preregulator.
(Top) Input current: 2A/div, 5ms/div (Bottom) Harmonic spectra: 0.6A/div, 100Hz/div

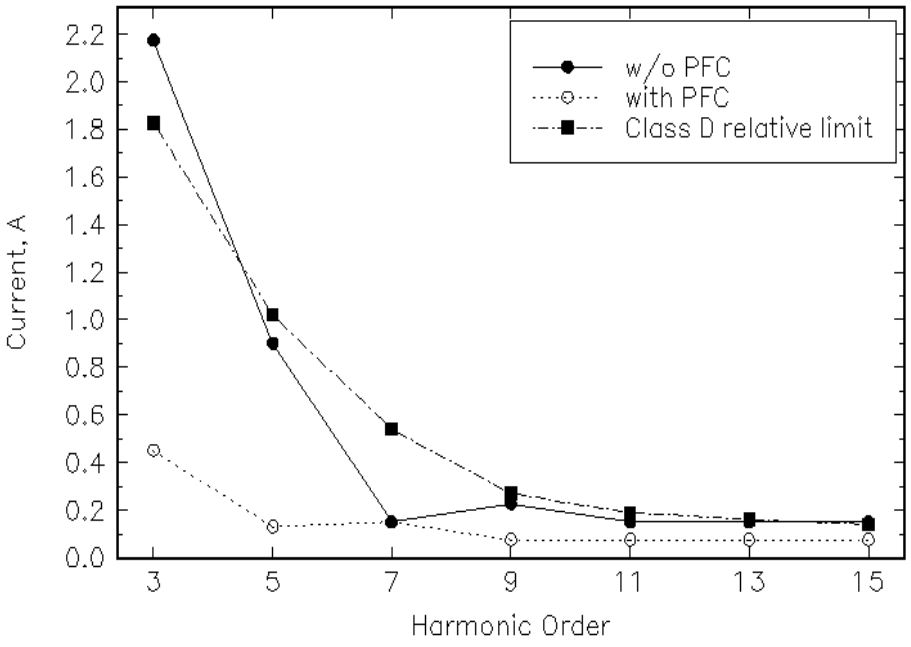


Figure 6.13 Comparison of measured input current harmonics from Figure 6.12 with modified IEC 1000-3-2 Class D harmonic current limit.

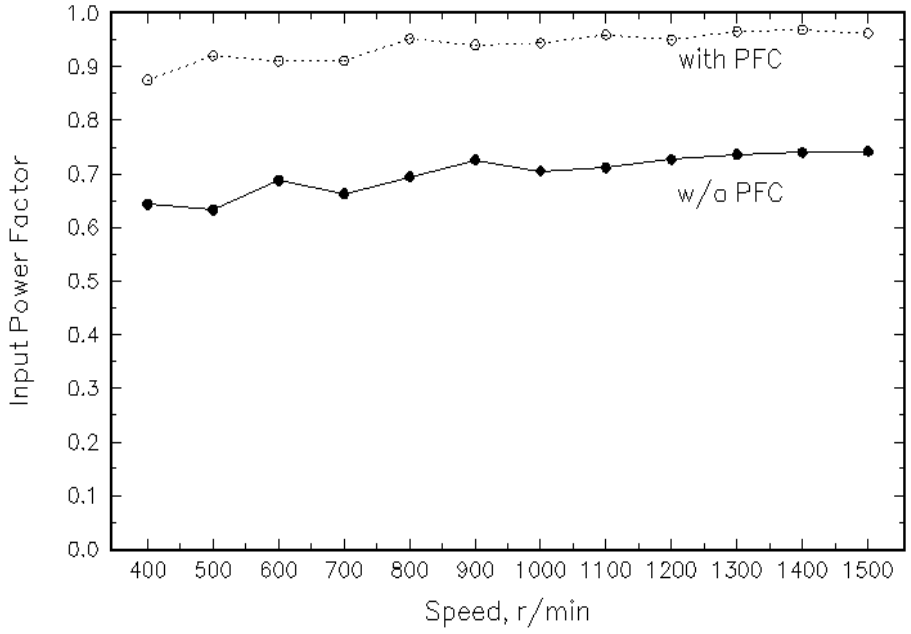


Figure 6.14 Input power factor with and without PFC preregulator.

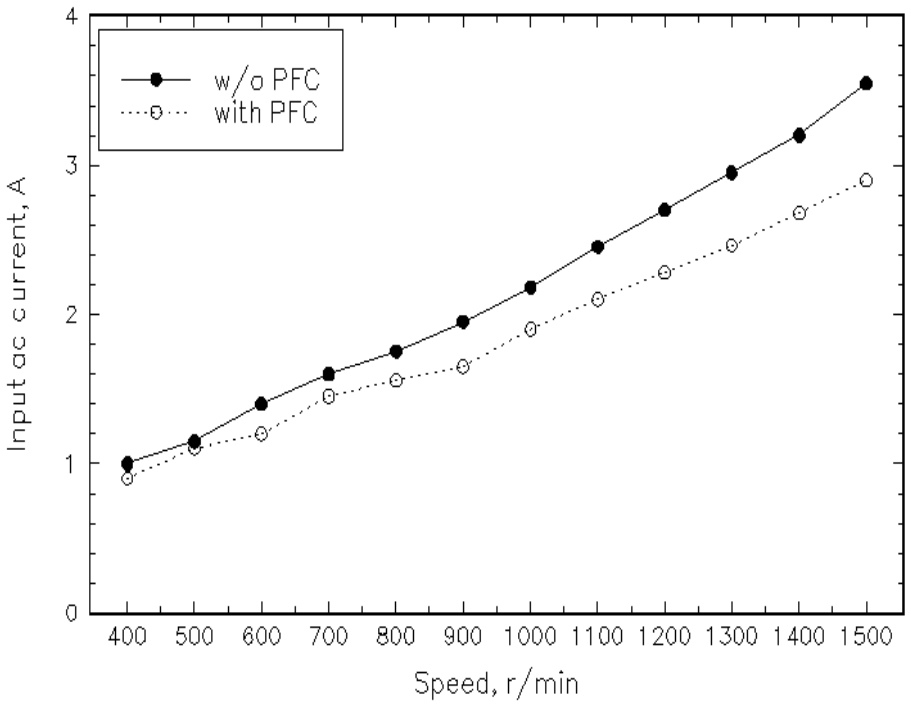


Figure 6.15 Magnitude of input ac current with and without PFC.

6.6 Conclusions

The input power factor corrected DCM-based VSD system is introduced in this chapter.

The duty cycle of the switch is derived to analyze the proposed DCM-based VSD system. Loss models of the major power components are developed for efficiency prediction of the drive system.

A four-quadrant controller for the DCM-based VSD system is developed. The performance of the controller is experimentally verified. MATLAB simulation of the speed reversal enhances the verification of the controller performance. The implemented low-cost, four-quadrant controller shows a good control performance.

A two stage power conversion is implemented with a 2kW front-end PFC preregulator and the MOSFET-based H-bridge down converter. The field voltage of the DCM is kept constant with 300W PFC preregulator.

The effectiveness of the PFC regards to improvement of the input current harmonics and the input power factor, and decreasing of the input current is verified with the experiment. The magnitude of the input current harmonics lies within the IEC 1000-3-2 Class D limit with a significant margin with the input PFC preregulator. The derived analytical calculations lead to a reasonable prediction of overall drive system efficiency in both with and without PFC cases. The prediction error becomes larger below 500r/min, but beyond this speed, it settles down within ±5%. This indicates that the derived loss model is useful to predict efficiency in high speed regions.