APPENDIX A

Direct Bond Copper (DBC) Ceramic Substrate*

DBC means Direct Bond Copper and denotes a process in which copper and a ceramic material are directly bonded. Normally, DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) or aluminum-nitride (AlN) ceramic base. The DBC process yields a super-thin base and eliminates the need for the thick, heavy copper bases that were used prior to this process. Because power modules with DBC bases have fewer layers, they have much lower thermal resistance values and because the expansion coefficient matches silicon, they have much better power cycling capabilities (up to 50,000 cycles).

Properties of DBC ceramic substrates:

- Good mechanical strength; mechanically stable shape, good adhesion and corrosion resistant;
- Excellent electrical insulation;
- Very good thermal conductivity;
- Superb thermal cycling stability;
- The thermal expansion coefficient is close to that of silicon, so no interface layers are required;
- Good heat spreading;
- May be structured just like printed circuit boards or "IMS substrates";
- Environmentally clean.

Advantages to the user:

- The 0.3 mm thick copper layer permits higher current loading for the same conductor width. Assuming the same copper cross-section the conductor needs to be only 12 % of that of a normal printed circuit board;

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- The excellent thermal conductivity provides the possibility of very close packaging of the chips. This translates into more power per unit of volume and improved reliability of systems and equipment;
- The high insulation voltage results in improved personnel safety;
- DBC ceramic is the basis for the "chip-on-board" technology which represents the packaging trend for the future.

DBC ceramic substrates are the base materials of the future for both the construction and the interconnection techniques of electronic circuits. They will be employed as base material for electronic components with high values of power dissipation and demanding requirements concerning their thermal shock behavior as well as their failure rate, whenever normal printed circuit boards are no longer adequate. Examples:

- Power hybrids and power control circuits;
- Power semiconductor modules;
- Smartpower building blocks;
- Solid state relays;
- High frequency switch mode power supplies (SMPS);
- Electronic heating devices;
- Building blocks for automobile electronics, the military as well as aerospace technology.

Properties and parameters of commonly available DBC substrates:

Uncladed ceramic	Aluminum Oxide Al_2O_3	Aluminum Nitride AlN
Purity	≥ 96 %	≥ 97 %
Dielectric strength	10 kV/mm	~14 kV/mm
Electrical resistivity	>10 14 Wcm	>10 14 Wcm
Thermal conductivity	24-28 W/mK	≥ 150 W/mK
Dimensions	max. 138 x 178 mm / 5.4" x 7.0"	75 x 57 mm / 2.95" x 2.24" (Example)
Thickness	Standard: 0.63, 0.38, 0.25 mm 25, 15, 10 mil	Standard: 0.63 mm 25 mil

Claded ceramic	Aluminum Oxide Al_2O_3	Aluminum Nitride AlN
Surface finish	Cu or (electroless) nickel plated Cu	Cu or (electroless) nickel plated Cu
Cu thickness	Standard: 0.3 mm / 12 mil	Standard: 0.3 mm / 12 mil
Ni thickness	max. 7 µm / 0.28 mil	max. 7 µm / 0.28 mil
Usable metallized area	max. 127 x 169 mm / 5.00" x 6.65"	73 x 55 mm / 2.87" x 2.17" (Example)
Total thickness resp. (Cu-AlN-Cu)	Standard: 1230 µm / 48 mil	Standard: 1230 µm / 48 mil
Cu bonding strength	≥ 6 N/mm; 34.3 lb/inch (in accordance with DIN 53 289)	≥ 3 N/mm; 17.2 lb/inch (in accordance with DIN 53 289)
Thermal expansion coefficient	Standard: 7.4 x 10 -6 K -1 @ (50 - 200)°C	Standard: 5 x 10 -6 K -1 @ (25 - 500)°C
Application temperature (inert atmosphere)	-55 ... +850°C	-55 ... +850°C
Hydrogen embrittlement	up to 400°C	up to 380°C

Design Rules for DBC substrates:

Dimensions	Application dependent	Application dependent
Min. width of Cu pattern	0.5 mm / 19.7 mil	0.5 mm / 19.7 mil
Min. spacing between Cu patterns	0.5 mm / 19.7 mil	0.5 mm / 19.7 mil
Minimum spacing between Cu patternand ceramic edge	0.35 mm / 13.8 mil	0.35 mm / 13.8 mil