CHAPTER VII

Summary and Conclusions

Power chip interconnection is extremely important in power electronics packaging since chip interconnection technology is the limiting factor for electrical performance, thermal management, size reduction, reliability and cost of power systems. The state-of-the-art wire bond interconnection technology for power chips can not meet the future power electronics requirements due to its inherit limitations. A new generation of advanced interconnection technologies for power chips is highly demanded. This study is specifically focused on the designing, processing, and reliability evaluation of solder joint interconnection for power chips and the application of solder joint interconnects in developing chip-scale power packages as well as three-dimensional integrated power electronics modules. A new stacked solder bumping process has been designed and developed for fabricating high standoff hourglass-shaped solder joints to meet the reliability requirement for power chip interconnection. Solder joint reliability has also been improved by underfilling flipped power chip and utilizing compliant substrate. Solder joint fatigue life is evaluated by accelerated temperature cycling as well as tensile and shear tests, and failure mechanisms has been studied. Furthermore, chip-scale power packaging concept has been put forward and two chip-scale power packages have been developed in this study. Ultimately, we have designed and implemented a three-dimensional integrated power electronics module structure.

In the following paragraphs, conclusions and significance for the above-mentioned areas of this study are summarized.

7.1 Process Development of Solder Joints for Power Chip Interconnection

Solder joint area array interconnection for power chips has been designed with the considerations of parasitic resistance and inductance reduction, current handling capability, thermal management, reliability improvement and manufacturability. The solder joint fabrication process development is based on the low cost stencil printing technique. In current industrial practice, the solder joints take on the shape of a spherical segment which is known to have high stress concentrations at the corners of the solder joint. A new solder joint fabrication

process, which is able to produce high standoff hourglass-shaped solder joint that consists of an inner cap, middle ball and outer cap, has been successfully developed for power chips. The triple-stacked solder joints have greater compliance than conventional solder joints and are able to relax the stresses caused by the coefficient of thermal expansion (CTE) mismatching between the silicon chips and substrates since it has a greater height. Moreover, the hourglass-shaped solder joints have a much lower stress/strain concentration at the interface between the solder bump and the silicon die as well as at the interface between the solder bump and substrate than barrel-shaped solder joints, especially around the corners of the interfaces. All these characteristics are important in improving solder joint fatigue resistance.

Solder joint fatigue failure is a major concern for solder joint area array technologies, such as flip chip and ball grid array. Researchers in industries, such as IBM and AT&T Bell Labs, have been pursuing alternative solder joint fabrication technologies to improve solder joint interconnection reliability and some approaches have been developed. However, solder joints made by some of the developed processes still have joint geometries that concentrate stresses and strains at the package and substrate metallization interfaces and require large joint-to-joint separation to obtain reliable joint heights, some of these technologies are not easily implementable in a manufacturing environment and some of them have yet to prove their cost-effectiveness. The solder joint fabrication process, called stacked solder bumping process, developed in this work can easily control the solder joint shape and height and is compatible with the existing surface-mount assembly operations and potentially low cost. This solder joint fabrication process is not only applicable to power chips, but also has its significance in other solder joint area array applications.

7.2 Solder Joint Reliability Evaluation

The reliability of fabricated solder joints including low standoff barrel-shaped solder joints and high standoff stacked solder joints with barrel and hourglass/column shapes was evaluated by accelerated temperature cycling test and adhesion tests. In-process electrical resistance measurement and nondestructive evaluations such as scanning acoustic microscopy and optical microscopy were conducted to monitor solder joint failure behaviors during thermal cycling. Tensile and shear tests were performed on as-processed solder joint assembly samples as well as temperature cycled samples to investigate the adhesion strength of different solder

joint configurations and study the adhesion strength change and fracture behavior of these solder joint configurations as a result as temperature cycling.

Accelerated temperature cycling test results clearly show that high standoff hourglass-shaped solder joint has the highest fatigue lifetime, with high standoff barrel-shaped solder joint in between and low standoff barrel-shaped solder joint has the shortest fatigue lifetime. Solder joint fatigue damage process can be divided into three phases corresponding to crack initiation, crack propagation and catastrophic failure. It has been found in this study that fatigue cracks in solder joints usually are initiated at a free surface, especially at the corners of the solder joints in the cooling process of a temperature cycle. It has also been observed that high standoff hourglass-shaped solder joint could shift the fatigue failure location. Experimental results showed that about 30% of the total fatigue lifetime improvement of high standoff hourglass-shaped solder joint over low standoff barrel-shaped solder joint contributed from crack initiation time, while about 65% gained from crack propagation. It has been concluded in this study that solder joint shape is the dominant factor affecting crack initiation time, while solder joint height is major factor in determining crack propagation time. It has also been concluded that increasing solder joint height is a more effective way of improving solder joint reliability.

Tensile and shear tests experimentally verified that hourglass-shaped solder joint has less stress singularity than barrel-shaped solder joint. The tensile and shear loads of barrel-shaped solder joints during temperature cycling reduce faster than those of hourglass-shaped ones. It has been concluded that barrel-shaped solder joints degrade earlier and faster and thus have lower fatigue lifetime.

Temperature cycling results showed that the thermal fatigue lifetimes of both single bump barrel-shaped and stacked hourglass/column-shaped solder joints were improved by using flex substrate. Experiments showed that flex substrate buckles during temperature cycling and it was indicated that the thermal strain and stress in solder joints could be reduced by flex buckling or bending. It has been concluded that the reliability improvement of flip chip on flex assembly is due to the flex buckling or bending under temperature cycling.

Solder joint fatigue models in the literature only characterize and emphasize one aspect of the solder joint fatigue process, for examples, both strain-based approach and energy-based approach only describe and predict crack initiation life; fracture mechanics-based approach predicts only crack propagation life. This research indicated that each of the crack initiation,

crack propagation and catastrophic failure stages need to be considered in order to fully study the solder joint fatigue behavior and accurately predict fatigue lifetime.

It is not clear in literature whether solder joint shape is the dominant factor or standoff height is more effective in improving solder joint reliability in the hourglass-shaped solder joints. Some studies in literature may even mislead readers by mixing the effects of shape and height on solder joint reliability and give readers the impression that solder joint shape is the only factor affecting reliability in their specific studies. The effects of solder joint shape and standoff height on reliability have been systematically studied experimentally for the first time in this research. This research provides engineers a useful guideline for designing and processing solder joint area array interconnects.

Flex circuitry is gaining increasing interest and has been found a lot applications in electronic industry. However, the effect of flex substrate on solder joint reliability has not yet been paid attention to and studied. To our knowledge, for the first time, it is reported in this study that flex substrate could improve solder joint reliability. This finding has its application significance. In some applications, higher solder joint reliability could be achieved by using flex substrate that otherwise would require underfill encapsulation or other means to improve reliability which are costly and need additional equipments.

7.3 Chip-Scale Power Packaging

Chip scale packaging (CSP) of integrated chips is gaining acceptance widely because of its intrinsic size advantages, the promise of highly favorable cost/performance trade-offs and reliance on existing materials and assembly infrastructures. However, CSP concept has yet to be realized in power electronics packaging area. In this research, two types of chip-scale power packages have been developed. One is called cavity down flip chip on flex; the other is termed Die Dimensional Ball Grid Array (D^2BGA). Both utilize solder joint as chip-level interconnection. These CSPs make high-density packaging and module miniature possible, enable the power chip to combine excellent thermal transfer, high current handling capability, improved electrical characteristics, and ultra-low profile packaging. Electrical tests show that the V_{CE}(sat) of the high speed IGBT chip-scale packages is improved by 20% to 30% by eliminating the device's wirebonds and other external interconnections, such as leadframe.

Double-sided cooling is realized in these CSPs. Temperature cycling test shows that the CSPs are reliable.

Chip scale packaging can enable a few very important concepts and advantages in power electronics packaging. It offers high silicon to package footprint ratio, provides a known good die solution to power chips, improves electrical as well as thermal performance and creates an opportunity for power component standardization.

7.4 Packaging of Three-Dimensional Multichip Power Modules

Integrated power electronics modules (IPEMs) are envisioned as integrated power modules consisting of power semiconductor devices, power integrated circuits, sensors, and protection circuits for a wide range of power electronics applications, such as inverters for motor drives and converters for power processing equipment. We have developed a three-dimensional approach, termed flip chip on flex (FCOF), for packaging high-performance IPEMs. The new concept is based on the use of solder joint (D^2BGA chip scale package) to interconnect power chips. We have demonstrated the feasibility of this approach by constructing half-bridge converters (IGBT and diode ratings: 1200 V, 70A) which have been successfully tested up to 800 V and 90 A. Switching tests have shown that parasitic inductance of the FCOF module has been reduced by 40% to 50% over conventional wire bond power modules. Better thermal management can be achieved in this three-dimensional power module structure. Compared with the state-of-the-art half-bridge power modules, the volume of the half-bridge FCOF power module is reduced by at least 65%. Reliability test shows that this flip chip on flex power module structure is potentially more reliable than wire bond power module.

In power electronics, it is generally believed that advancement can be achieved only through a systems-level approach by developing intelligent, integrated power electronics modules (IPEMs) that enable greater integration within power electronics systems and their end-use applications. The state-of-the-art power system packaging offers a hybrid structure, with switching devices assembled in planar structures and the gate drivers and controls and protection circuits being put together in a subassembly and incorporated in a single module. This kind of packages increases the size and cost of the module, introduces undesirable degrading parasitics, and is prone to failure. Also heat dissipation is still limited by the planar structure and the problems with wire bond still exist. Several new technologies for fabrication multichip power

modules are under development by the module manufacturers and research institutes in the area of power electronics. However, the technologies have yet to prove their manufacturability, reliability, and cost effectiveness. This three-dimensional high-density multichip power module packaging structure could be a solution to the future power electronics systems.