Processing and Reliability Assessment of Solder Joint Interconnection for Power Chips

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(ABSTRACT)

Circuit assembly and packaging technologies for power electronics have not kept pace with those for digital electronics. Inside those packaged power devices as well as the state-of-the-art power modules, interconnection of power chips is accomplished with wirebonds. Wirebonds in power devices and modules are prone to resistance, noise, parasitic oscillations, fatigue and eventual failure. Furthermore, there has been an increase demand for higher power density and better efficiency for power converters. Power semiconductor suppliers have been concentrating on improving device structure, density, and process technology to lower the on-resistance of MOSFETs and voltage drop of IGBTs. Recent advances made in power semiconductor technology are pushing packaging technology to the limits for performance of these power systems since the resistance and parasitics contribution by the package and the wirebonds are roughly the same as that on the silicon. In recent years, an integrated systems approach to standardizing power electronics components and packaging techniques in the form of power electronics building blocks has emerged as a new concept in the area of power electronics. As a result, it has been envisioned that the packaging of three-dimensional high-density multichip modules (MCMs) can meet the requirement for future power electronics systems. However, the conventional wirebond interconnected power devices are excluded from three-dimensional MCMs because of their large size, limited thermal management, and incompatible processing techniques. On the other hand, advanced solder joint area-array technologies, such as flip-chip technology, has emerged in microelectronics industry due to increased speed, higher packaging density, and performance, improved reliability and low cost these technologies offer. With all these benefits to offer, solder joint area-array technology has yet to be implemented for power electronics packaging. Therefore, the first objective of this study is to design and develop a solder joint area-array interconnection technique for power chips. Solder joint reliability is a major concern for area array technologies and power chip interconnection, thus the second objective of this study is to evaluate solder joint reliability, investigate the fatigue failure behavior of solder joint and improve solder joint reliability by developing a new solder bumping process for improved solder joint geometry, underfilling solder joint with encapsulant and applying flexible substrate in the assembly. The third objective is the implementation of solder joint interconnection technique in developing chip-scale power packages and a three-dimensional integrated power electronics module structure.

Solder joint area array interconnection for power chips has been designed with the considerations of parasitic resistance and inductance reduction, current handling capability, thermal management, reliability improvement and manufacturability. A new solder joint fabrication process, which is able to produce high standoff hourglass-shaped solder joint that consists of an inner cap, middle ball and outer cap, as well as the conventional solder bumping process have been successfully developed for power chips by using stencil printing. This solder

bumping technology is compatible with the existing surface-mount assembly operations and potentially low cost. The fabricated solder joints have been characterized for their structure integrity, mechanical strength and electrical performances.

Solder joint reliability has been improved by optimizing solder joint geometry, underfilling flipped power chip and utilizing compliant substrate. Solder joint reliability was evaluated using accelerated temperate cycling and adhesion tests. The interfaces of the triple-stacked solder joints were examined using scanning electron microscopy (SEM) and energy dispersive X-ray analysis (EDX) for the integrity of the joint. Acoustic microscopy imaging (nondestructive evaluation) was utilized to examine the quality of the bonded interfaces and to detect cracks and other defects before and during accelerated fatigue tests. Adhesion strength of both single bump barrel-shaped and stacked hourglass-shaped solder joints to bonding pads was characterized and analyzed. It was found that stacked hourglass-shaped solder joint have higher fracture stress than barrel-shaped solder joint. This verifies that hourglass-shaped solder joint has lower stress singularity at the interface between the solder bump and the silicon die as well as at the interface between the solder bump and substrate than barrel-shaped solder joint, especially around the corners of the interfaces. Furthermore, the adhesion strength of barrel-shaped solder joint decreases much faster than that of high standoff hourglass-shaped solder joint under temperature cycling, which indicates that the latter has high reliability than the former. Our accelerated temperature cycling test clearly shows that solder joint fatigue failure process consists of three phases: crack initiation, crack propagation and catastrophic failure. Solder joint geometry, underfilling and substrate flexibility were proved to affect solder joint reliability. The effects of solder joint shape and standoff height on reliability have been systematically studied experimentally for the first time. Our experimental results indicated that both hourglass shape and great standoff height could improve solder joint fatigue lifetime, with standoff height being the more effective factor. The fatigue lifetime of high standoff hourglass-shaped solder joint is improved mainly by prolonged crack propagation time, with slight improvement in crack initiation time. Experimental data suggested that shape is the dominant factor affecting crack initiation time while standoff height is the major factor influencing crack propagation time. Underfilling and flexible substrate improved the lifetime of both barrel and hourglass-shaped solder joints. The effect of underfill on solder joint reliability is well known in microelectronics packaging field. However, for the first time, it is reported in this study that flex substrate could improve solder joint reliability. It has been found that flex substrate bucks during temperature cycling and thus reduces thermal strain in solder joints, which in turn improves solder joint fatigue lifetime.

Chip scale packaging can enable a few very important concepts and advantages in power electronics packaging. It offers high silicon to package footprint ratio, provides a known good die solution to power chips, improves electrical as well as thermal performance and creates an opportunity for power component standardization. Two kinds of chip-scale power packages have been developed in this research. One is called cavity down flip chip on flex; the other is termed Die Dimensional Ball Grid Array (D^2BGA). Both utilize solder joint as chip-level interconnection. Electrical tests show that the V_{CE}(sat) of the high speed IGBT chip-scale packages is improved by 20% to 30% by eliminating the device's wirebonds and other external interconnections, such as leadframe. Double-sided cooling is realized in these CSPs. Temperature cycling test shows that the CSPs are reliable.

Integrated power electronics modules (IPEMs) are envisioned as integrated power modules consisting of power semiconductor devices, power integrated circuits, sensors, and

protection circuits for a wide range of power electronics applications, such as inverters for motor drives and converters for power processing equipment. We have developed a three-dimensional approach, termed flip chip on flex (FCOF), for packaging high-performance IPEMs. The new concept is based on the use of solder joint (D^2BGA chip scale package), not bonding wires, to interconnect power devices. This packaging approach has the potential to produce modules having superior electrical and thermal performance and improved reliability. We have demonstrated the feasibility of this approach by constructing half-bridge converters (consisting of two IGBTs, two power diodes, and a simple gate driver circuitry) which have been successfully tested at power levels over 30 kW. Switching tests have shown that parasitic inductance of the FCOF module has been reduced by 40% to 50% over conventional wire bond power modules. Better thermal management can be achieved in this three-dimensional power module structure. Compared with the state-of-the-art half-bridge power modules, the volume of the half-bridge FCOF power module is reduced by at least 65%. Reliability test shows that this flip chip on flex power module structure is potentially more reliable than wire bond power module.

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LIST OF ACRONYMS

AMI .... Acoustic Micrography Imaging
BGA .... Ball Grid Array
BLM .... Ball Limiting Metallurgy
C4 .... Controlled Collapse Chip Connection
CCGA .... Ceramic Column Grid Array
CCMD .... Chip Carrier Mounting Device
CGA .... Column Grid Array
CLASP .... Column Last Attach Solder Process
CPES .... Center for Power Electronics Systems
C-SAM .... C-mode Scanning Acoustic Microscope
CSP .... Chip Scale Packaging
CTE .... Coefficient of Thermal Expansion
DBC .... Direct Bond Copper
D^2BGA .... Die Dimensional Ball Grid Array
DCA .... Direct Chip Attach
DIP .... Dual-In-Line Package
DMA .... Dynamic Mechanical Analyzer
EDX .... Energy Dispersive X-Ray
FC .... Flipchip
FCOB .... Flip Chip on Board
FCOF .... Flip Chip 0n Flex
FEA .... Finite Element Analysis
FOM .... Figure of Merit
HDI .... High Density Interconnect
HTP .... Harris Thin Pack
IC .... Integrated Circuit
IGBT .... Insulated Gate Bipolar Transistor
IMS .... Insulated Metal Substrate
I/O .... input/output
IPEMs .... Integrated Power Electronics Modules
IR .... International Rectifier
JEDEC .... Joint Electron Device Engineering Council
KGD .... Known-good-die
MCM .... Multichip Module
MCM-L .... Multichip Module - Laminated
MMC .... Metal Matrix Composite
MOSFET .... Metal Oxide Semiconductor Field Effect Transistor
MPIPPS .... Metal Posts Interconnected Parallel Plate Structure
PCB .... Printed Circuit Board
PGA .... Pin Grid Array
PLCC .... Plastic Leaded Chip Carrier
POL .... Power Overlay
PWB .... Printed Wiring Board
QFP .... Quad Flat Pack

S^3 .... Solder Support Structure
SAM .... Scanning Acoustic Microscopes
SBB .... Stud Bump Bonding
SEM .... Scanning Electron Microscope
SIP .... Single-in-Line Package
SLAM .... Scanning Laser Acoustic Microscope
SMT .... Surface Mount Technology
SO .... Small Outline Package
SOIC .... Small Outline Integrated Circuit
SOT .... Small Outline Transistor
TAB .... Tape Automated Bonding
TAMI .... Tomographic Acoustic Micrography Imaging
TEM .... Transmission Electron Microscope
TMA .... Thermal Mechanical Analysis
TO .... Transistor Outline Package
TOF .... Time of Flight
TSSOP .... Thin Shrink Small Outline Packages
UBM .... Under Bump Metallurgy
UV .... Ultraviolet
VSI .... Voltage Source Inverter
XPS .... X-Ray Photoelectron Spectroscopy