

High Frequency, High Power Density Integrated Point of Load and Bus Converters

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Abstract

The increased power consumption and power density demands of modern technologies combined with the focus on global energy savings have increased the demands on DC/DC power supplies. DC/DC converters are ubiquitous in everyday life, found in products ranging from small handheld electronics requiring a few watts to warehouse sized server farms demanding over 50 megawatts. To improve efficiency and power density while reducing complexity and cost the modular building block approach is gaining popularity. These modular building blocks replace individually designed specialty power supplies, providing instead an optimized complete solution. To meet the demands for lower loss and higher power density, higher efficiency and higher frequency must be targeted in future designs. The objective of this dissertation is to explore and propose methods to improve the power density and performance of point of load modules ranging from 10 to 600W.

For non-isolated, low current point of load applications targeting outputs ranging from one to ten ampere, the use of a three level converter is proposed to improve efficiency and power density. The three level converter can reduce the voltage stress across the devices by a factor of two compared to the traditional buck; reducing switching losses, and allowing for the use of improved low voltage lateral and lateral trench devices. The three level can also significantly reduce the size of the inductor, facilitating 3D converter integration with a low profile magnetic by doubling the effective switching frequency and reducing the volt-second across the inductor.

This work also proposes solutions for the drive circuit, startup, and flying capacitor balancing issues introduced by moving to the three level topology.

The emerging technology of gallium nitride can offer the ability to push the frequency of traditional buck converters to new levels. Silicon based semiconductors are a mature technology and the potential to further push frequency for improved power density is limited. GaN transistors are high electron mobility transistors offering a higher band gap, electron mobility, and electron velocity than Si devices. These material characteristics make the GaN device more suitable for higher frequency and voltage operation. This work will discuss the fundamentals of utilizing the GaN transistor in high frequency buck converter design; addressing the packaging of the GaN transistor, fundamental operating differences between GaN and Si devices, driving of GaN devices, and the impact of dead time on loss in the GaN buck converter. An analytical loss model for the GaN buck converter is also introduced.

With significant improvements in device technology and packaging, the circuit layout parasitics begins to limit the switching frequency and performance. This work will explore the design of a high frequency, high density 12V integrated buck converter, identifying the impact of parasitics on converter performance, propose design improvements to reduce critical parasitics, and assess the impact of frequency on passive integration. The final part of this research considers the thermal design of a high density 3D integrated module; this addresses the thermal limitations of standard PCB substrates for high power density designs and proposes the use of a direct bond copper (DBC) substrate to improve thermal performance in the module.

For 48V isolated applications, the current solutions are limited in frequency by high loss generated from the use of traditional topologies, devices, packaging, and transformer design.

This dissertation considers the high frequency design of a highly efficient unregulated bus converter targeting intermediate bus architectures for use in telecom, networking, and high end computing applications. This work will explore the impact of switching frequency on transformer core volume, leakage inductance, and winding resistance. The use of distributed matrix transformers to reduce leakage inductance and winding resistance, improving high frequency transformer performance will be considered. A novel integrated matrix transformer structure is proposed to reduce core loss and core volume while maintaining low leakage inductance and winding resistance. Lastly, this work will push for higher frequency, higher efficiency, and higher power density with the use of low loss GaN devices.

To my family:

My parents: George III and Janet Reusch

My wife: Katelyn Reusch

My daughter: Paige Reusch

My sister: Jennifer Reusch

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Chapter 1

Introduction

1.1 Background of Point of Load (POL) Converters

Point of load converters are found in a variety of technologies used in everyday life, ranging from small handheld electronics to warehouse sized systems used to power server farms. As technologies have advanced over the years, so have the methods to power these complex systems. In 1965, Intel co-founder Gordon Moore established Moore's law by predicting that the number of transistors on an integrated circuit would double every two years [1]. This prediction has proved accurate and the number of transistors in the current Intel processor approaches 1 billion compared to 7.5 million ten years ago [2].

With growing processor speeds and transistor counts the power demands have also increased significantly [3][4]. In 1997, the Intel Pentium Pro processor used a single power supply to provide a maximum load current of 13.2 amperes. As the power demands of future processors grew, so did the power demands and transient response requirements of the voltage regulator (VR). The multi-phase VR was proposed by CPES to improve efficiency, transient performance, and power density [5]-[7]. As of 2011, every computer employs the multi-phase VR concept and the current multi-core server microprocessor can demand up to 180A which is supplied by as many as 8 multi-phase buck converters. The current multi-phase converters operate at lower switching frequencies, ranging from 200-600 kHz to maintain high efficiency. With lower switching frequencies, the passive components including the inductors and capacitors

become bulky and occupy a large amount of motherboard real estate. Shown in figure 1.1 is a current server mother board, the space occupied on the mother board by power supplies is up to 30% of the overall real estate [8]. With future demands calling for higher output currents and smaller sizes, power supplies must improve power density while maintaining high efficiency.

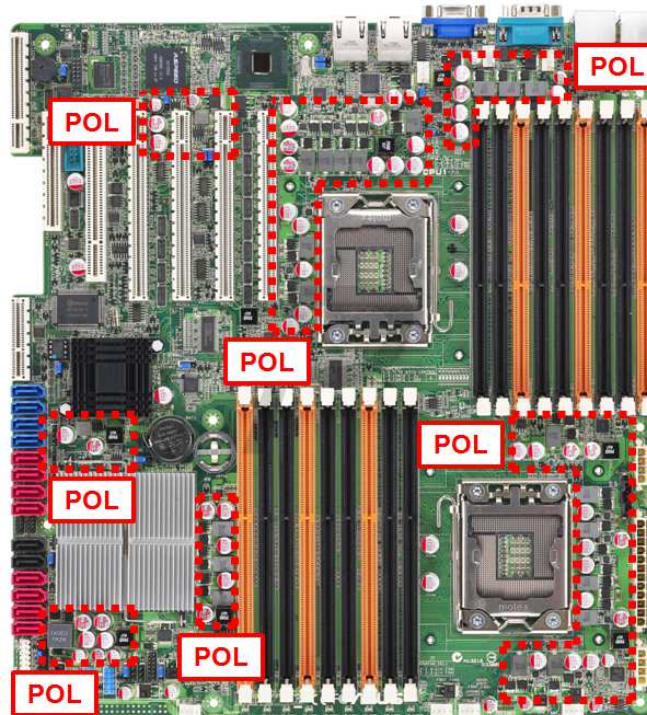


Figure 1.1. Server motherboard and POL converters on board

The current computer and telecom applications require a large number of POL converters to power the various loads which have a wide range of currents and voltages. To simplify the design of the power management, industry leaders are migrating to a solution that does not require the power management being embedded into the PCB. The proposed shift is to a modular power management solution built from individual power blocks designed by power supply manufacturers. The power block concept allows the designers to save board space by selecting from the optimized power blocks to meet their

power requirements. To achieve higher power levels the manufacturer can use multiple point of load (POL) modules in a multi-phase configuration, providing design flexibility.

The increase in power demands is not limited just to the microprocessor. Many everyday technologies such as cellular phones, mp3 players, etc. require low current switching power supplies to efficiently convert power to the processors, graphics units, and memory of these small handheld devices. In these applications small size is paramount and high density solutions are required.



Figure 1.2: Wide ranging applications for point of load converters

1.2 State of the Art POL Modules

1.2.1 Discrete POL Module

There are three different types of POL modules considered in this research. The first and most common POL available today is a discrete module. The discrete module generally contains two discrete semiconductors, a discrete driver, a discrete inductor, and

discrete output capacitors [9]. These components are connected electrically on a pcb board and connected to the mother board with external leads. These modules are available from currents as low as 3A to as high as 40A. The discrete solution operates at the lowest frequencies ranging from 200-600kHz, has the largest passive size, and offers the lowest power density in the 50-200W/in³ range. The limitations in switching frequency for the discrete converter are a result of the large parasitics introduced to the converter from the discrete packaged components. At lower switching frequencies, the size of the converter is dominated by the size of the passive components, with the output inductor being the largest component.

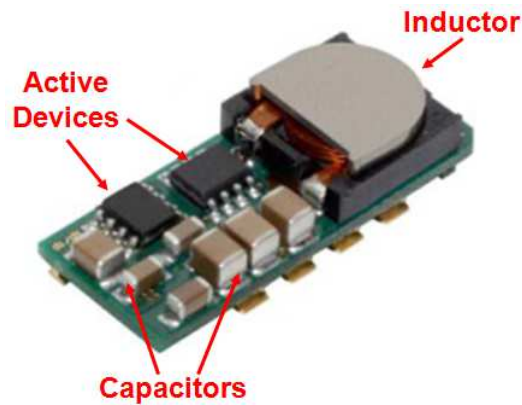


Figure 1.3: Typical 12V Discrete POL Module

1.2.2 Co-Packaged POL Module

The second type of POL module is a co-packaged solution. The co-packaged solution utilizes bare die for the power devices, driver, and control circuit to reduce parasitics compared to the discrete case. For the 12V input case, the active bare dies are generally trench based devices that are connected to the PCB substrate by direct die attachment and wire bonding. The passives remain discrete components and are connected to the active layers through the PCB substrate. Shown in figure 1.4 is a top and side view of a state of the art 12V/12A co-packaged module [10]. The drain of the

top device and synchronous rectifier (SR) are connected to the PCB substrate with a direct solder connection to the die. The gate and source pads of the two sided trench power devices are connected to the PCB substrate via wire bonding with multiple bonds used for the source to decrease parasitics. The 12V co-packaged solution offers lower parasitics than the discrete case and switching frequencies are increased to the range of 0.5MHz-1MHz allowing for smaller magnetic size leading to improved power density. From the top and side view of the converter it can be seen that the inductor's volume is still substantially larger than the other components and is the major bottleneck to higher power density.

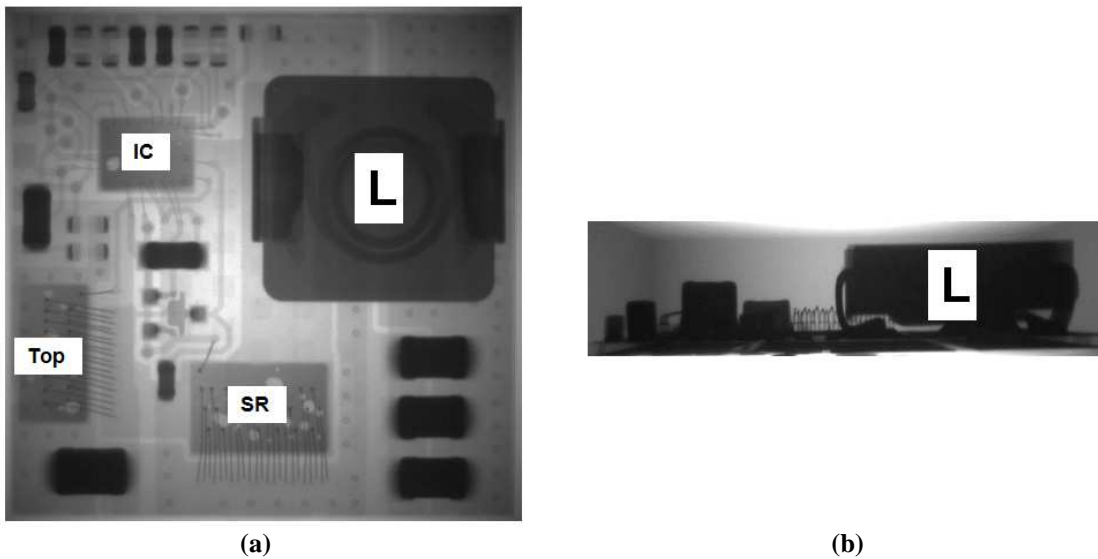


Figure 1.4: Linear Technology's co-packaged $V_{in}=12V$ $F_s=1MHz$ $I_o=12A$ POL converter LTM4601 (a) Top View (b) Side View. Images by author.

For lower voltage applications, i.e. portable electronics, a bus voltage of 5V or under is common, resulting in a large market for 3.3-5V power modules. For a co-packaged POL module with a 5V input, the design of the active stage changes to a monolithic solution for the active components. For the 12V case, the driver and control chips are lateral devices and the power devices are double sided trench devices. Since the

top and SR devices in a buck converter connect the source of the top switch to the drain to the SR a monolithic die cannot be used for a trench based module.

In the 5V case, the IC and power devices both use a low voltage lateral process allowing for monolithic integration of the driver and control with the power devices. Also, in a lateral semiconductor the device connections are all on a single side of the device, this allows for monolithic integration of the power devices as a result of the source of the top device and drain of the SR being contained on the same plane. Combining reduced parasitics of monolithic integration of the active stage, a lower input voltage, and better performing low voltage lateral transistors the switching frequency can be pushed to 5MHz with current levels up to 9A [11]. For the high frequency 5V co-packaged modules, the inductor size is greatly reduced, but at high currents remains a discrete component connected to the active layer through the pcb substrate. The inductor size still dominates module volume, limiting power density.

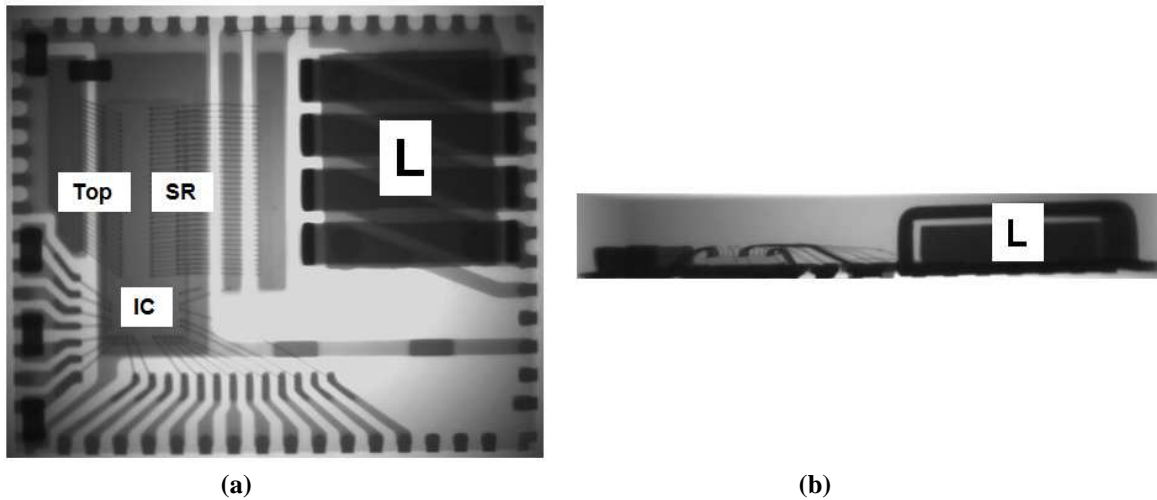


Figure 1.5: Enpirion's co-packaged $V_{in}=5V$ $F_s=5MHz$ $I_o=9A$ POL converter 5396QI (a) Top View (b) Side View. Images by author.

1.2.3 Integrated POL Module

The third type of POL module available today is a fully integrated solution. An integrated solution uses 3D integration to mount the inductor directly to the active stage, minimizing solution footprint and improving power density. The current 3D integrated products are confined to lower input voltages (3.3V,5V) and smaller output currents ($I_o < 1A$) to allow for monolithic active stage integration, yielding higher switching frequencies and smaller output inductors [12][13]. To minimize the inductor size a multi-turn inductor is used which reduces magnetic size but suffers from high winding resistance. Integrated converters operate with the highest switching frequencies ranging from 2-5MHz and offer the highest power density of all the POL modules. It should be noted however that the current integrated solutions do not integrate the input and output capacitors, which are co-packaged on the application motherboard with the module for a complete solution.

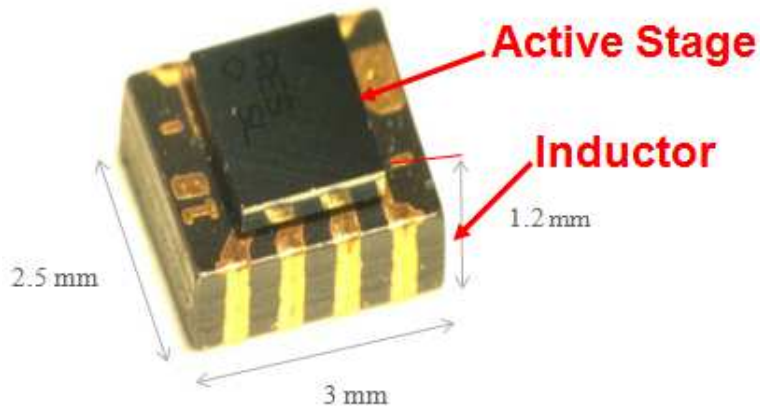


Figure 1.6: Integrated $V_{in}=5V$ $F_s=2MHz$ $I_o=1A$ POL converter

Having looked at the state of the art discrete, co-packaged, and integrated POL modules available today a trend emerges, increasing the level of integration can significantly increase converter performance and power density. To increase the level of integration, the switching frequency of the converter must be increased from the range of a couple hundred kHz to the range of multi-MHz to reduce the required passive size to a

level suitable for integration. The ability to increase switching frequencies requires the use of improved semiconductors, device packaging, converter layout, and inductor design. Figure 1.7 shows the power density map of today's POL converters. For the trench based 12V POL modules, there are no integrated and few co-packaged solutions currently available, limiting the frequency and power density. For the converters with a lower 5V input voltage, higher levels of integration can be achieved through the use of monolithic lateral solutions, resulting in high power density. From the roadmap it can also be noted that the level of integration reduces significantly at higher current levels, with no product integrating the inductor above 6A of output current and co-packaged solutions being limited to under 12A.

The objective of this dissertation is to explore methods to improve high frequency performance and power density for point of load applications. The following section will give an overview of relevant previous research on the subject matter.

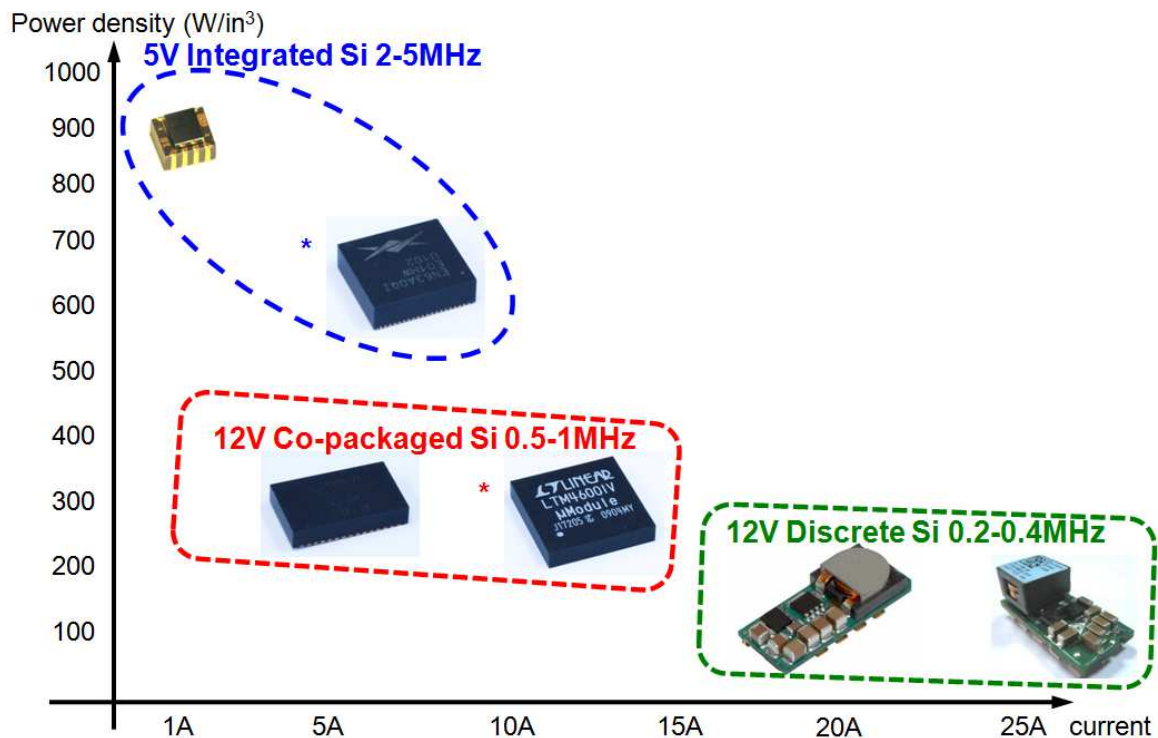


Figure 1.7: POL Power Density Roadmap. *: Images by author.

1.3 History of Integration in POL Modules

1.3.1 Active Layer Integration Techniques

The push for integration in the POL module has been pursued very aggressively in previous research. This section will outline the previous work done to integrate the POL module for low voltage, high current applications. A major barrier to higher power density can be seen by looking at the state of the art encapsulated modules in figures 1.4b & 1.5b. The inductor footprint and height make up the majority of module volume. To minimize footprint and maximize power density a 3D integration approach should be considered [14][15]. The concept of 3D integration proposes integrating a low profile inductor substrate to the active layer substrate to produce a low footprint, low profile solution. 3D integration can offer high power density and the concept is illustrated in figure 1.8.

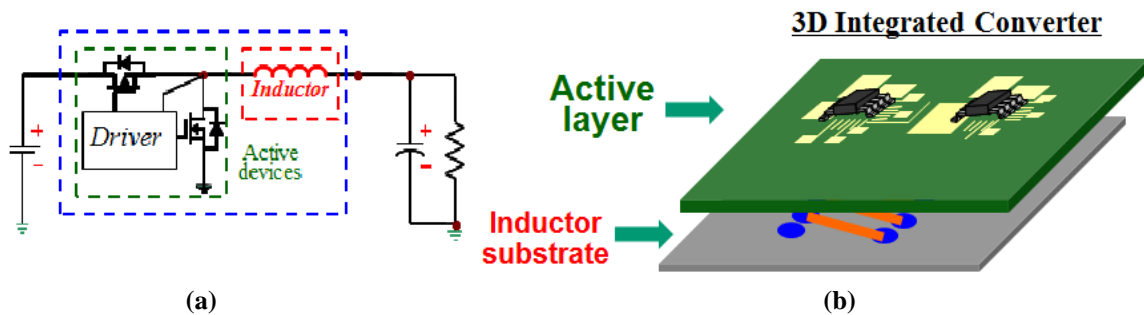


Figure 1.8: (a) Buck Converter Schematic (b) 3D Integrated Converter

The first CPES designed 3D integrated POL, shown in figure 1.9, employed the concept of integrating the active and passive layers by building the active layer directly onto a low temperature co-fired ceramic (LTCC) based inductor substrate [15]. A proposed benefit of using the LTCC inductor as the circuit substrate was that LTCC has 10x higher thermal conductivity than traditional PCB substrates which would help distribute heat, reducing thermal design concerns. Another proposed benefit of this

approach is that the coefficient of thermal expansion (CTE) of LTCC matches more closely to Si than the PCB substrate, limiting mechanical stress of the active stage.

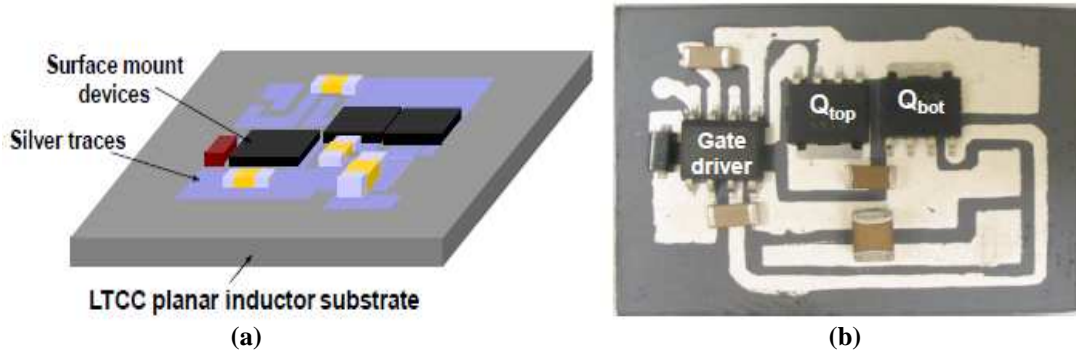


Figure 1.9: (a) 3D Integrated POL on LTCC Inductor Substrate (b) Hardware Design

The prototype of the 3D integrated converter built on a LTCC inductor substrate is shown in figure 1.9b. This converter was designed to run at an input voltage of 5V, output voltage of 1.1V, switching frequency of 1.3MHz, and an output current of 20A. The original experimental prototype for this design experienced low efficiency when compared to the performance of a buck converter built on a traditional PCB substrate. The cause of the low efficiency in this design was identified as interference between the inductor and the active power stage increasing the active stage parasitics. The results of increased parasitics were higher switching related losses and higher voltage ringing, increasing the voltage stress seen by the power devices.

To minimize parasitics and improve converter performance, isolation of the active and passive substrates was proposed. The isolation was achieved by using a Pyralux flex substrate to build the active layer, using an isolating copper shield layer in between the inductor and the active power stage to eliminate inductor interference on the power stage; the conceptual drawing is shown in figure 1.10a and the hardware design is shown in figure 1.10b.

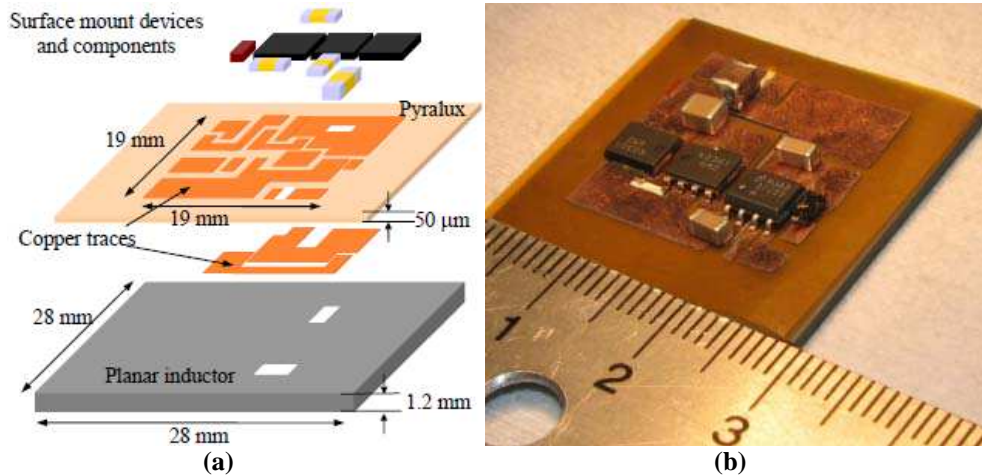


Figure 1.10: (a) 3D Integrated POL on Pyralux Substrate (b) Hardware Design

The impact of adding the shield layer to isolate the magnetic from the active layer was a reduction in active stage parasitics, reducing switching related losses, and improving high frequency performance. The experimental results showed a reduction in parasitic voltage ringing and a significant improvement in efficiency. The voltage ringing waveforms for the converter operated at 1.3MHz with and without the shield layers are shown in figures 1.11a&b. The ringing voltage in the design case with a shield isolating the inductor and active stage was reduced 80%, with the unshielded case having a 100% overshoot and the shielded case having a 20% overshoot.

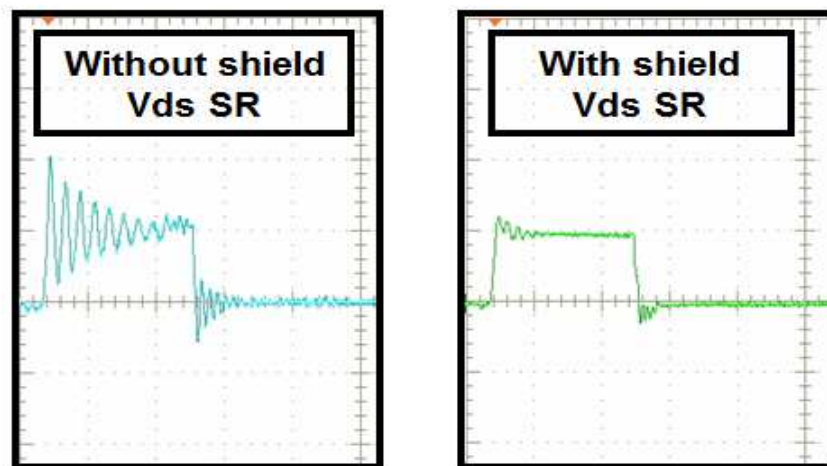


Figure 1.11: Voltage Ringing Waveforms for Design Without and With shield

The impact of the shield on efficiency is shown in figure 1.12. The design case with a shield had an efficiency gain of over 5% at 6A when compared to the original design with no isolating shield layer. While the shield improved performance, the efficiency was low when compared to the traditional PCB based designs, and the power density was limited by the use of a large inductor substrate and low output current.

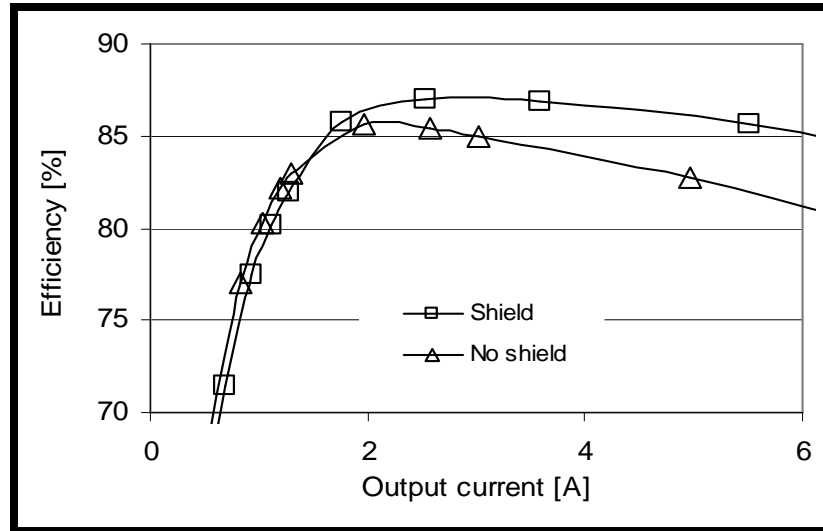


Figure 1.12: Converter Efficiency With and Without Shield for $V_{in}=5V$ $V_o=1.1V$ $F_s=1.3MHz$

In [15], circuit layout and device package parasitics were large, leading to low efficiency and thermal limitations for high output currents. In [16], integration of the POL concept was studied further to improve efficiency and thermal performance. The design in this work replaced traditional packaged devices with low parasitic, unpackaged bare die devices, and embedded the semiconductors into a highly thermal conductive aluminum nitride (AlN) substrate. The improved 3D integrated design's power loop is shown in figure 1.13a; the inductance of the power loop was reduced significantly paving the way for improved performance. The method used to reduce the loop inductance was to flip the top MOSFET device so that the source of the top device could be placed on the same layer as the drain of the SR. This also allowed for the drain of the top device and

source of the SR to be located on the same layer reducing loop size. Having the devices embedded in the substrate allowed for the capacitor to be located directly on top of the power devices. To maximize the power density a low profile LTCC inductor was designed to fit on the back of the active substrate; the final module design is shown in figure 1.13b. This 1.3MHz module achieved a $250\text{W}/\text{in}^3$ power density, which was the highest power density for a high current module at the time.

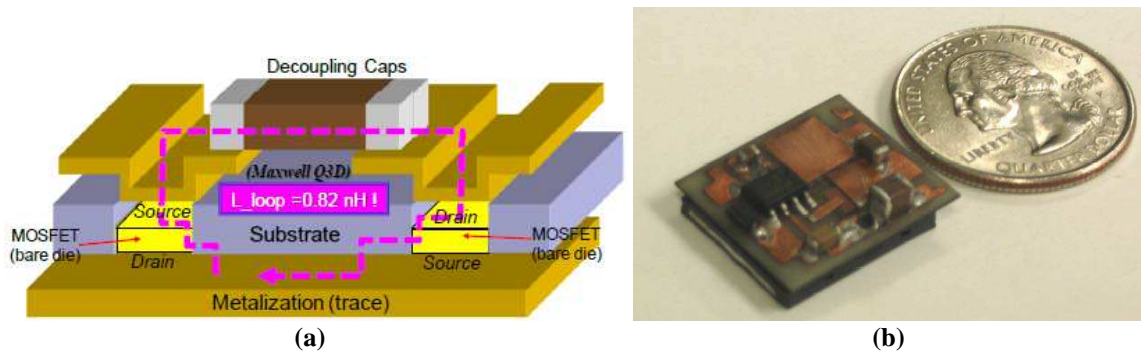


Figure 1.13: (a) Power Loop Design of 3D Integrated Module with Bare Die (b) Stacked Power Hardware for $V_{in}=5\text{V}$ $V_o=1.2\text{V}$ $I_o=20\text{A}$ $F_s=1.3\text{MHz}$

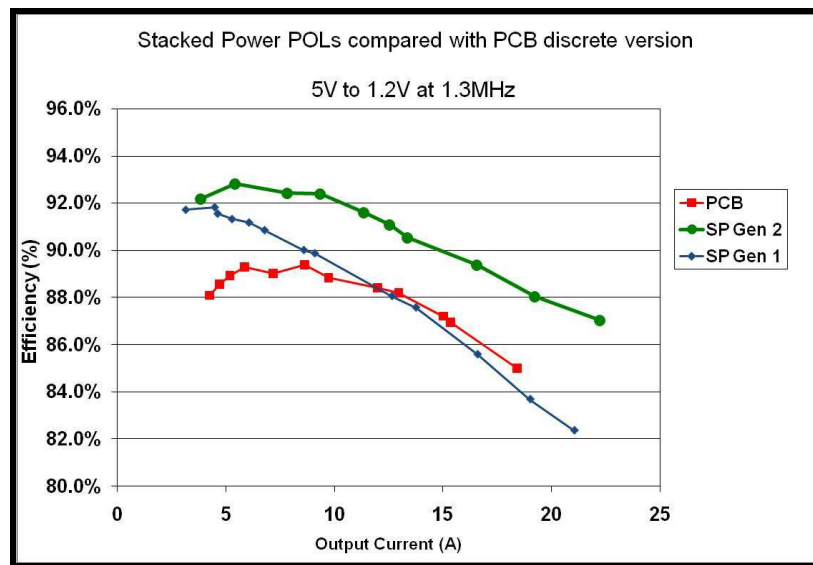


Figure 1.14: Efficiency comparison of improved 3D module

As the power density increases, thermal considerations of the module are critical. In [16], the substrate was chosen to be alumina nitride (AlN) which has a thermal conductivity much higher than the traditional PCB insulating layers. For the stacked

POL with embedded semiconductors, double sided cooling was used to further improve thermal performance. Figure 1.15 shows the traditional discrete POL design and the improved stacked power design utilizing a substrate with high thermal conductivity and double sided cooling. With the improved thermal design, the heat was spread evenly throughout the board avoiding the hotspots commonly seen in traditional PCB designs and eliminating the need for a heat sink.

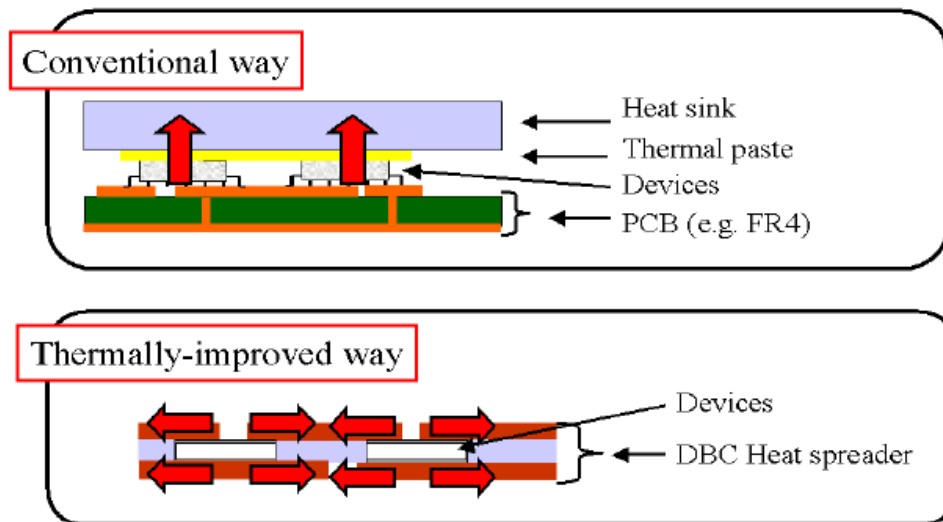


Figure 1.15: Conventional Cooling Method for PCB design and Improved Double Sided Cooling using AlN Heat Spreading Substrate

1.3.2 Passive Layer Integration Techniques

The previous section discussed the past research to create a high density, high frequency active power stage. This section will discuss the research related to the design of the low profile LTCC inductor for use in an integrated 3D POL module. The material used to create a LTCC comes in the form of thin sheets of magnetic material. To create an inductor, many layers of the magnetic material are stacked together. The process for building a LTCC inductor is discussed in [15]. This process is shown in figure 1.16; the first step in creating an inductor is to cut the LTCC sheets to the desired footprint. With the LTCC sheets, the bottom layer of the inductor was created using 7 layers of ferrite

tape; the layers were then laminated together using a temperature of 70°C and a pressure of 1500psi. The middle layer containing the inductor winding was created using 8 layers of LTCC tape laminated together and then laser cutting the c-shaped winding opening. The bottom and middle layers were then laminated together. The next step was to fill the conductor trace with silver paste and heat the structure to a temperature of 70°C to dry the paste. The top of the inductor was created in the same manner as the bottom layer and then laminated to the section of the inductor with the winding. The final step to create the inductor was to sinter the laminated inductor structure at 900°C.

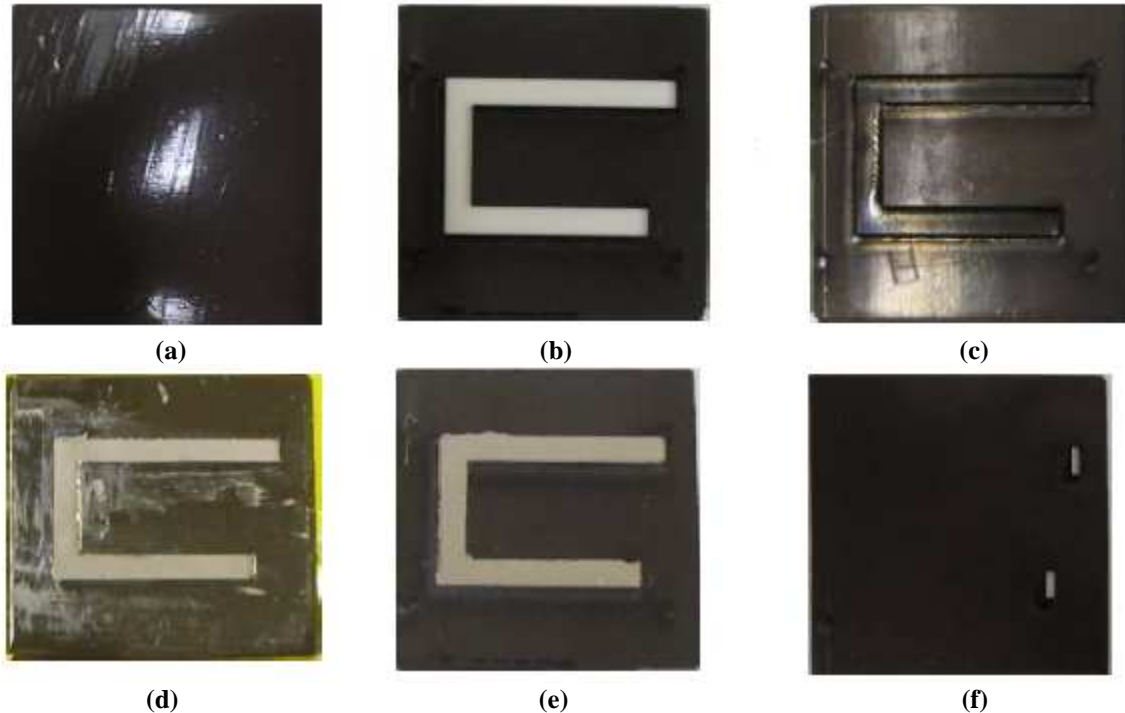


Figure 1.16: LTCC Inductor Fabrication Procedure: (a) Bottom inductor layer comprising 7 layers of ferrite tape (b) middle winding layer comprising 8 layers of ferrite tape, with C-shaped winding slot cut using laser (c) Result of laminating bottom layer and middle layer with winding (d) Conductor paste dispensed into slot, Kapton tape covering the rest of the surface (e) Bottom and middle layer with winding after conductive paste drying (f) Final inductor with top main layer comprising 7 layers of ferrite tape

The LTCC inductor and traditional inductor have a fundamental design difference in that the LTCC inductor has no air gap and parts of the core are purposely saturated. The ferrite sheet material has a lower permeability than traditional ferrites and the

permeability is very non-linear, changing with bias current. As a result of this property, for different biasing conditions the inductance value will vary, with lower inductance occurring at higher loads. The inductance vs load current for an LTCC inductor is shown in figure 1.17 for the design from [16], the inductance reduces by a factor of two from half load to full load. The designed LTCC inductor had a size of 18x18x1.75mm and achieved a full load inductance of 65nH. This inductor provided low profile but suffered from low inductor density, limiting the integration ability as a result of a large footprint.

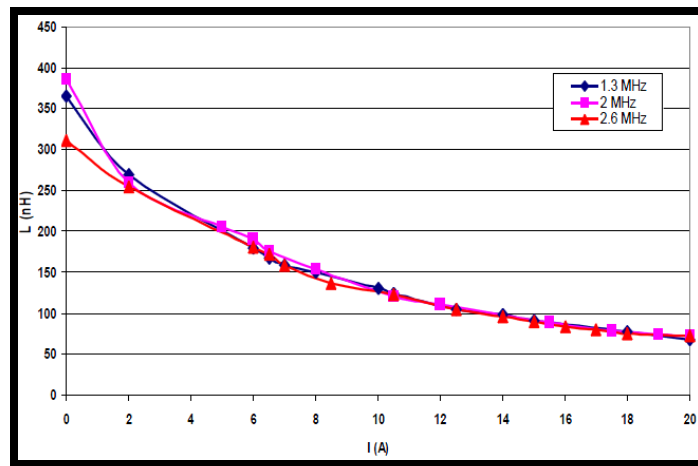


Figure 1.17: Inductance vs Load Current for LTCC Inductor

In the original LTCC inductor, also known as a vertical flux inductor, the winding was formed parallel to the substrate and the flux was generated perpendicular to the substrate. The drawbacks of this structure were that the magnetic interfered with the active stage and the ability to reduce core thickness was limited due to conductor thickness and low inductance density. To improve the performance of the LTCC inductor, an improved lateral flux LTCC structure was proposed in [17]. The lateral flux inductor changed the arrangement of the winding and core to make the flux travel parallel to the substrate. The benefits of having the lateral flux inductor are that the flux is parallel to the power stage reducing magnetic interference with the active layer and that

the core thickness could be reduced without sacrificing inductor volume density. In the vertical flux structure, the height was limited by the conductor sandwiched between the magnetic layers. In the lateral structure, the core height is independent of the conductor size allowing for lower profile. The two structures are shown in figure 1.18 with the plot of core thickness vs inductor density.

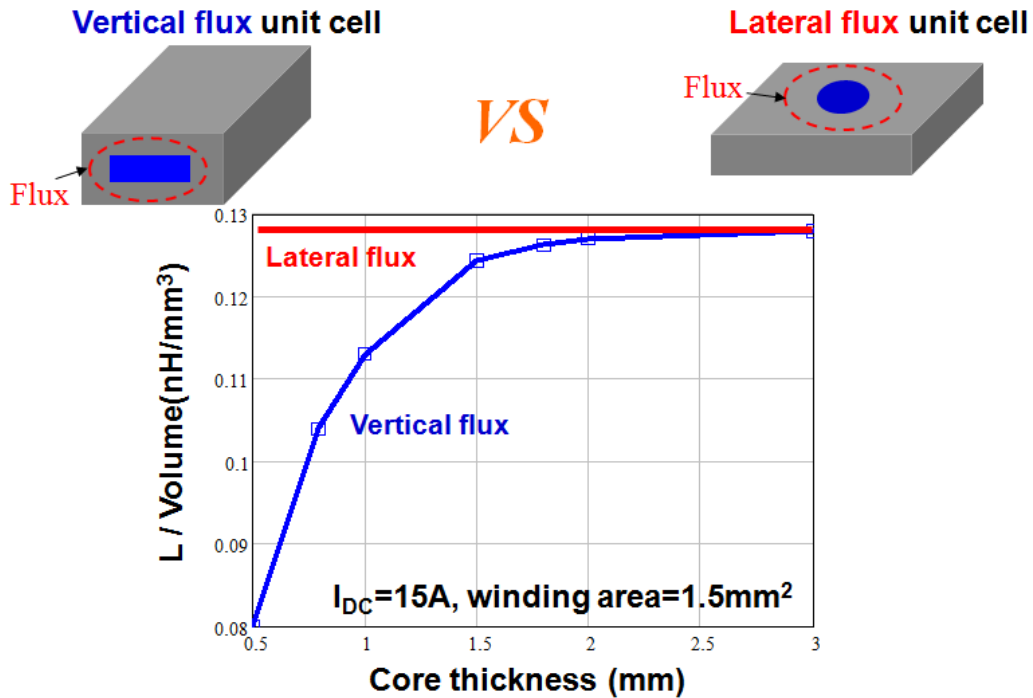


Figure 1.18: Inductance vs Core Thickness for Vertical and Lateral Flux LTCC Inductors

Figure 19a shows the hardware designs for the vertical and lateral flux inductors and figure 19b gives the inductance versus bias current. For the lateral flux inductor, the footprint was reduced by 30% while achieving similar full load inductance. The lateral flux inductor also offered higher light load inductance than the vertical flux case. Using the lateral flux inductor a power density of 300w/in³ was achieved with a switching frequency of 1.5MHz, $V_{in}=5V, V_o=1.2V, I_o=15A$. This was the highest power density for a high current module achieved at the time.

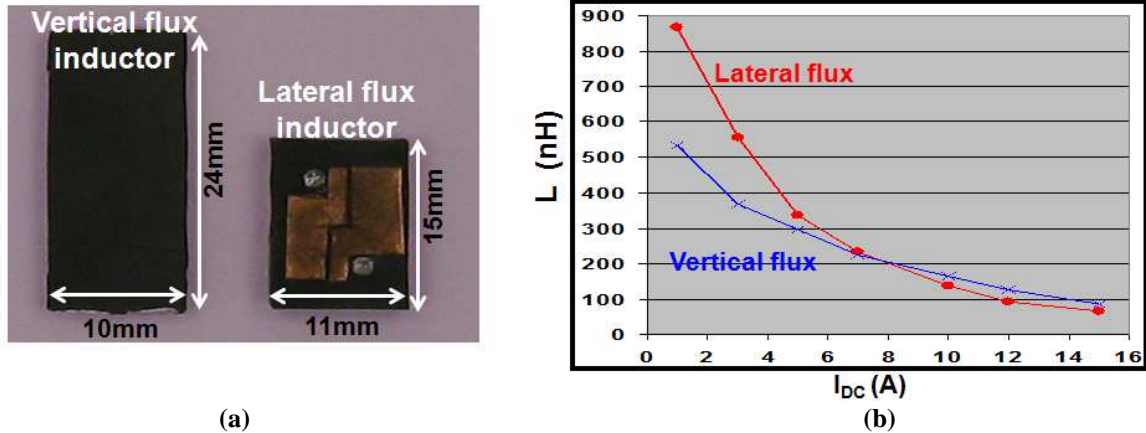


Figure 1.19: (a) Hardware Designs of Vertical and Lateral Flux Inductors (b) Inductance vs Bias Current for Vertical and Lateral Flux Inductor Designs [17]

1.4 Advanced Semiconductors for High Frequency Applications

1.4.1 Evolution of Power Semiconductors

The push for higher frequencies and higher levels of integration has been made possible by improved semiconductors. In the early 1980's, International rectifier introduced the planar power MOSFET which revolutionized the semiconductor industry. In the 1990's, the trench MOSFET rose to popularity improving upon the planar structure [18]. The trench device has seen improvements in switching speed and on resistances over the years. In recent years, the trench technology has become mature and the effort required to slightly improve switching performance has increased significantly.

For lower voltage applications ($V_{br} < 200V$) trench MOSFETs are preferred to planar technologies for their higher channel density and lower on resistances [19]. The trench FETs preferred operating voltage range is from 25V to 200V. For low voltages, $V_{br} < 15V$, the lateral MOSFET has proven superior to the trench device [20][21]. Si lateral devices offer performance improvements over trench devices but only in low

voltage applications. The majority of power semiconductor applications require devices capable of supporting a minimum of 25V.

Over the past five years two new device technologies have been introduced to improve performance in applications with higher voltage requirements. The first improved device is the lateral trench device, which was introduced in 2007 to offer superior performance in the voltage range between the lateral and trench device. The lateral trench device can provide superior performance in the voltage range of 12V to 25V. The comparison of the trench based devices figure of merit (FOM) vs. voltage rating is shown in figure 1.20. The figure of merit used for comparison is based on [22], where the FOM is a loss based formula derived for a low voltage buck converter. While the lateral trench technology can provide superior performance at a 12V voltage rating, the 12V input voltage applications require a 25-30V rated device and this technology offers modest improvements over the trench based devices at 25V. This technology is also Si based and faces the same difficulties with reducing FOM in the future.

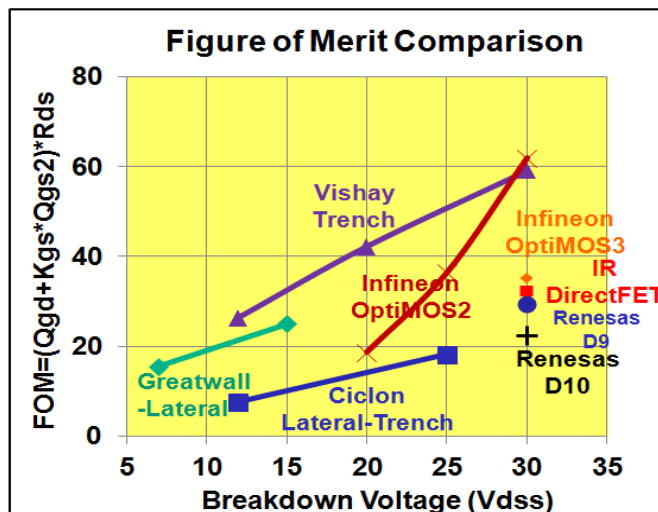


Figure 1.20: Figure of merit comparison between Si based devices vs breakdown voltages

The second new technology is Gallium Nitride (GaN), which was introduced 2010. Gallium Nitride transistors are high electron mobility transistors (HEMT) and

offer potential benefits for high frequency power conversion over a wide range of voltages. Shown in table 1 are the material characteristics for Si, SiC, and GaN [23]. GaN transistors have a higher band gap, electron mobility, and electron velocity than Si and SiC devices. These material characteristics make the GaN device more suitable for higher frequency and voltage operation. GaN devices are a new technology and project to offer significant performance gains in the future over a wide range of voltages [24].

	Si	SiC	GaN
Band Gap (eV)	1.1	3.2	3.4
Electron Mobility (cm ² /V-sec)	1450	900	2000
Electron Saturation Velocity (10 ⁶ cm/sec)	10	22	25

Table 1.1 Material Characteristics of Si, SiC, and GaN semiconductors

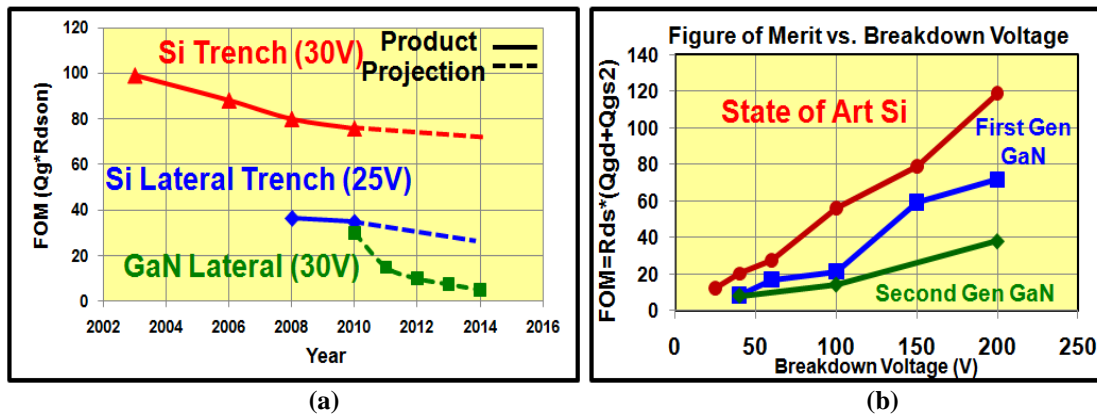


Figure 1.21: (a) FOM vs year for SI and GaN devices (b) FOM vs breakdown voltage for current Si and GaN devices

With gallium nitride transistors projecting to offer game changing performance compared to Si devices from as low as 30V to up to 600V, much higher switching frequencies can be targeted. Figure 1.22 shows the switching frequency capability of state of the art devices versus their voltage rating. The GaN semiconductor offers the ability for an order of magnitude increase in frequency over a wide range of applications within the next five years. A major focus of this dissertation will be the exploration of the GaN devices for use in high frequency, high density POL applications.

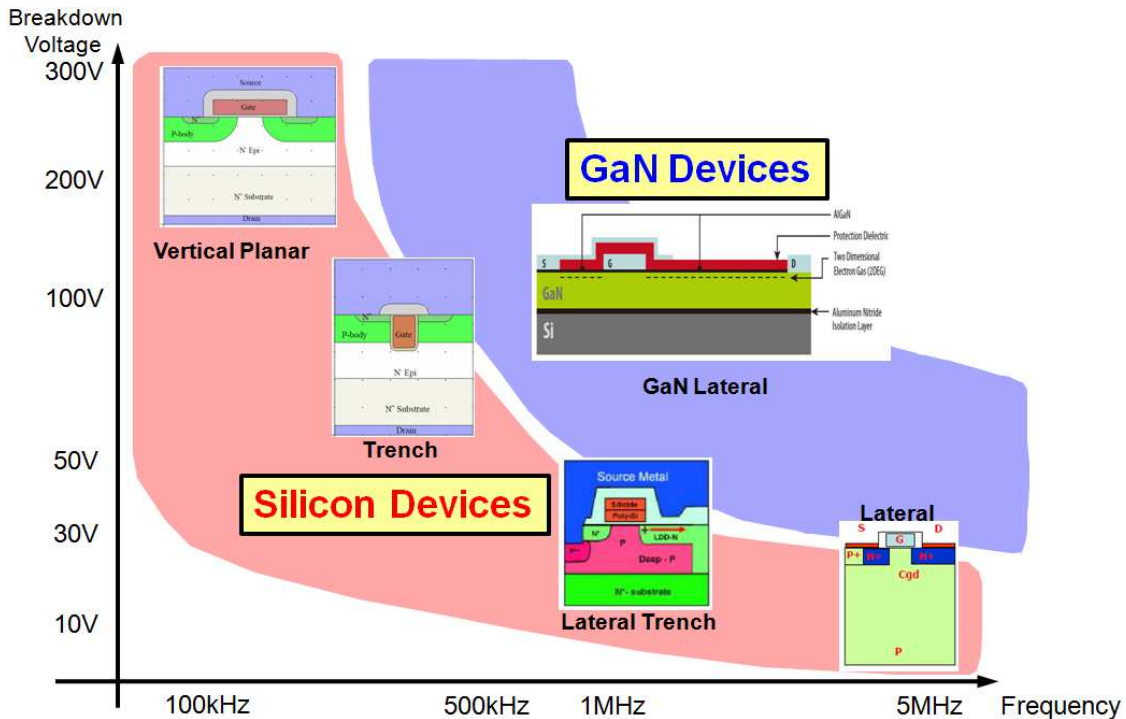


Figure 1.22: Map for Frequency vs Breakdown Voltage for Different Device Technologies

1.4.2 Evolution of Power Semiconductor Packaging

Semiconductor device packaging has had to evolve over the years to keep up with the improvements made in the die performance. Performance of the semiconductor die is improving to the level where the package is a major bottleneck to improved performance. Figure 1.23 illustrates the different packages for discrete power devices in the low voltage range. The earliest of the packages was the So-8; the So-8 package is used for a trench MOSFET and has the highest package parasitics resulting from the use of wire bonding to attach the die to the package. The loss free package (LFPAK) was introduced to improve on the So-8 package parasitics by removing the wire bonds and replacing them with a lower parasitic lead frame. The LFPAK still suffered from high gate and source inductance as a result of the source pad being connected to the package via an external connection. To reduce source and gate inductance, the IR DirectFET [25] flipped the orientation of the MOSFET die to allow for direct mounting of the gate and

source to the PCB substrate and connected the drain to the substrate with a large connection reducing the overall package parasitics.

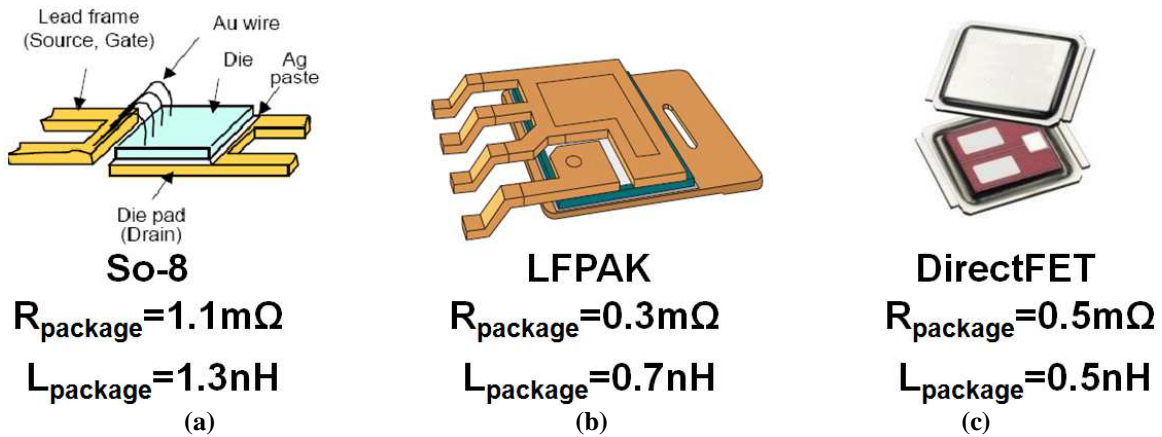


Figure 1.23: Different Commercial Trench Packaging Technologies (a) So-8 (b) LFPAK (c) DirectFET

To increase switching frequencies, the parasitics of the package must be reduced. The trench based devices are limited by having terminations on both sides of the die, requiring external connections for one side of the die. The lateral based devices have all of the terminals on the same side of the device, this allows for the devices to be used in the unpackaged form.

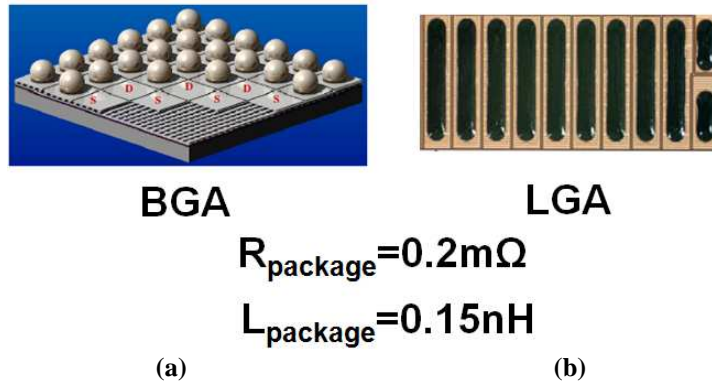


Figure 1.24: Different Commercial Lateral Packaging Technologies (a) Ball Grid Array (b) Linear Grid Array

Without packaging, the parasitics of the device can be reduced significantly. Shown in figure 1.24 are the two available lateral dies, the ball grid array (BGA) and linear grid array (LGA) GaN devices. These packages mount the die directly to the PCB

substrate and interleave the drain and source pads to minimize resistance and inductance. The reduced parasitics of the lateral die allow for higher frequency operation. Figure 1.25 maps the frequency operation range for the different packaged devices commercially available. The impact of packaging on high frequency performance is considered in this dissertation and high frequency designs with LGA packaged GaN devices is considered.

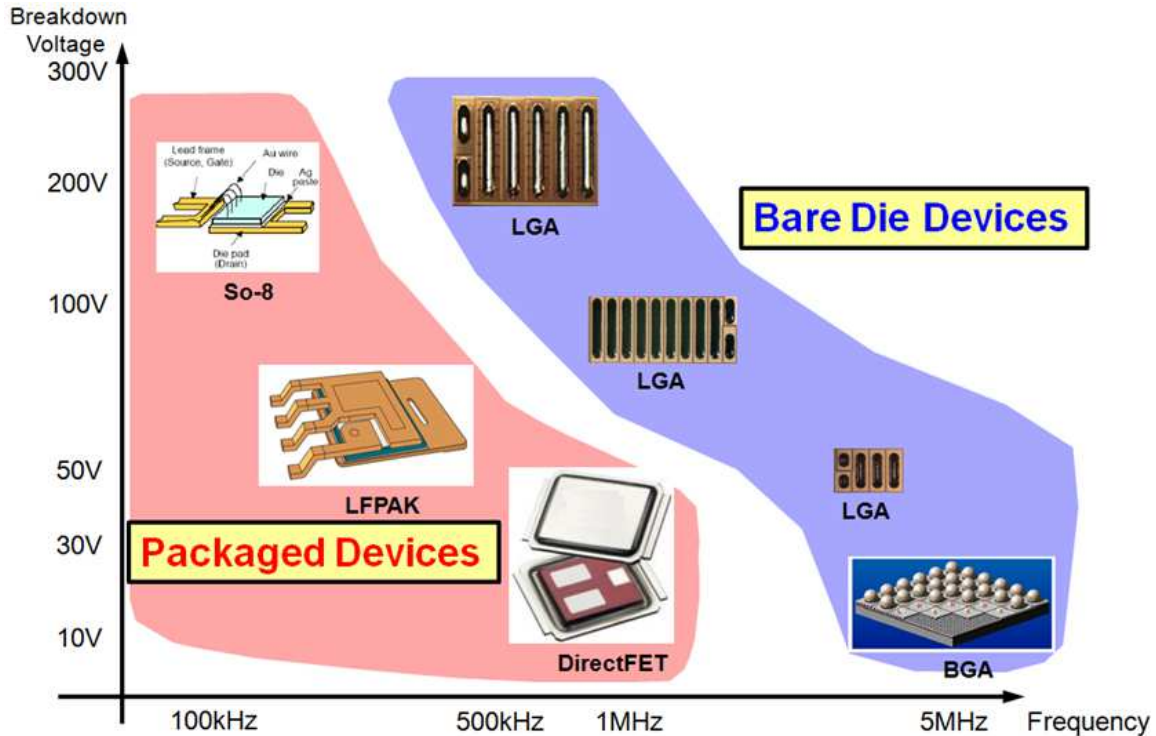


Figure 1.25: Map for Frequency vs Breakdown Voltage for Different Device Packaging Technologies

1.5 Background of Isolated Bus Converters

1.5.1 Distributed Power Architecture History

Distributed power systems are prevalent in communications, networking, and high end server applications and generally utilize a 48V bus voltage adopted from the telecom industry. From the 48V bus, a number of isolated point of load converters power the end loads, with isolation being required for safety. The traditional distributed power architecture (DPA), shown in figure 1.26, uses AC/DC front end converters to deliver the

48V bus voltage. From the 48V bus voltage, a number of isolated DC/DC regulated POL converters are used to deliver the required voltage and power to the individual loads. As communications, networking, and high end server systems have become more complex, the voltages and currents demanded by the ever increasing number of loads have increased significantly. Having a large number of regulated 48V isolated DC/DC POL converters to power these systems significantly increases the cost, volume, and complexity of the system.

Traditional Distributed Architecture Telecom and High End Server

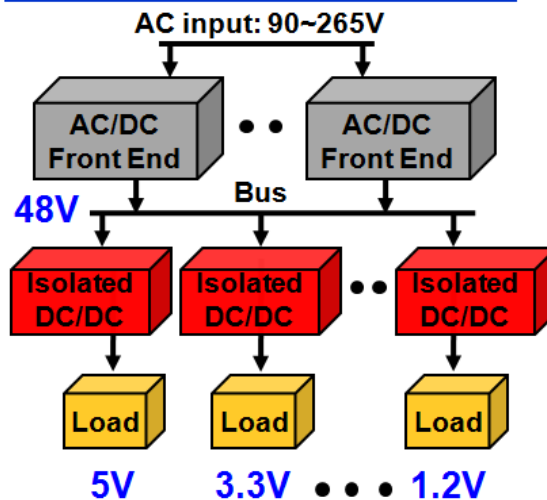


Figure 1.26: Traditional Distributed Power Architecture for Telecom and High End Servers

The limitation of the traditional distributed power architecture is that as the power demands of the loads increased so did the complexity of the isolated converters required. Fully regulated isolated POL converters are much larger, more complex, and more expensive than low voltage non-isolated POL converters. The isolated converters contain a bulky transformer, large filter inductor, and complex control due to the isolation requirements; this leads to lower efficiency and power density.

To simplify the design of these systems, the concept of intermediate bus architecture (IBA) was proposed to reduce the number of complex isolated POL converters required

in the system [26]-[29]. The IBA approach employs a lower number of 48V isolated converters that satisfy isolation requirements and supply an intermediate bus voltage ranging from 8-12V. The final regulation to the loads is done by smaller, more efficient regulated POL converters like those discussed earlier in the chapter. This concept is illustrated in figure 1.27, the IBA is widely used in the majority of distributed power systems today for better performance and lower overall system cost.

Intermediate Bus Architecture (IBA) Telecom and High End Server

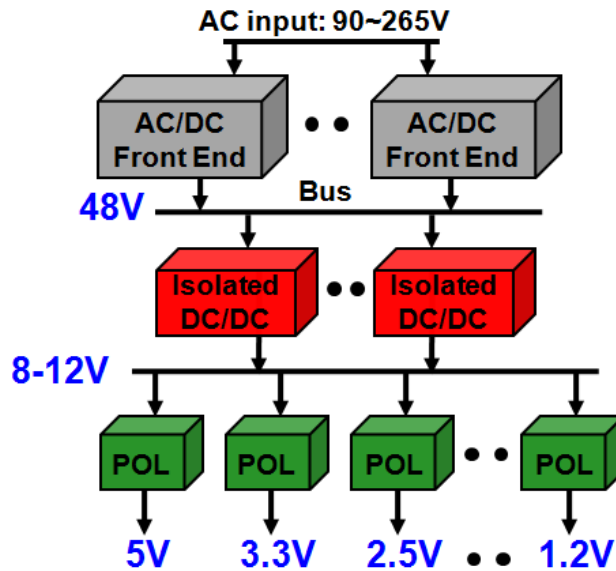


Figure 1.27: Intermediate Bus Architecture for Telecom and High End Servers

The IBA approach can use three different designs for the 48V isolated bus converter: a fully regulated, semi regulated, or unregulated design. The fully regulated converter supplies the output voltage to the controller to generate the gating signals, this provides a very accurate output voltage but results in the most complicated control structure as isolation is required for the voltage feedback. The semi regulated converters use the input voltage in a feed forward configuration [30] to regulate the gate signals; this provides less accurate voltage regulation as the losses in the converter are not taken into account. The semi regulated converter offers a simple control structure as no isolation is

required from the output to the controller. The unregulated converter is an open loop converter with no control in place. The unregulated converter leads to the largest variation in output voltage but offers the simplest design and most efficient power conversion as the switches are always operated close to a duty cycle of 100%. For high end server and some telecom applications, a narrow input voltage range is common, i.e. 38V-55V, and the downstream POL's can easily handle the small variations in output voltage making the unregulated IBA architecture the most efficient solution. In other applications with wider input voltage ranges, i.e. 36-72V, the fully or semi-regulated converters offer a more efficient solution.

1.5.2 State of Art Isolated Bus Converters

To improve the performance of the IBA, a highly efficient isolated converter must be designed. To achieve high efficiency and low loss the majority of current bus converters operate at lower switching frequencies. In the majority of current bus converters, there is no co-packaging or integration and discrete packaged devices and passive components are used. The frequency range of the current discrete unregulated converters is from 150-300 kHz [31]. The switching frequency of current designs is limited by the use of traditional hard switching topologies in combination with high parasitic, discrete packaged devices. The use of low switching frequencies results in bulky passives limiting power density; this includes the isolation transformer, output inductor, and filter capacitances.

A traditional bus converter design is shown in figure 1.28, the large transformer and inductors footprint occupy the majority of the footprint on the board. The second largest space occupiers on the board are the active devices, in particular the synchronous

rectifiers (SR). For a high current output, SR devices must be paralleled to reduce conduction loss. To improve power density, the size of the magnetic components and the footprint occupied by the active devices must be reduced without sacrificing efficiency.

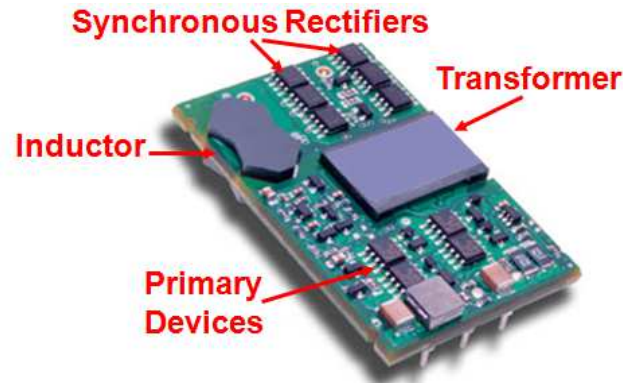


Figure 1.28: Typical industry discrete unregulated bus converter

To push for higher switching frequencies and reduce passive size, resonant topologies have been considered for IBA bus converters [32][33]. Resonant converters can utilize the parasitics in the converter to offer soft switching; reducing switching loss and improving performance. The resonant topologies can be operated at higher frequencies, eliminating the need for the large output filter inductor and significantly reducing the size of the transformer. Current resonant designs have been demonstrated at 1.7MHz with co-packaged devices.

Figure 1.29 shows the power density roadmap for the current unregulated bus converters from industry. It can be seen that there is a single product with high power density, far surpassing the power density of the other modules. This module is a co-packaged resonant solution, utilizing an advanced topology combined with low parasitic packaging techniques to push the switching frequency to 1.7MHz, a 4.7x increase over the highest frequency discrete hard switching converter available. The combination of high frequency and advanced packaging offers a 6x improvement in power density over a

similarly rated discrete module. To explore the design of a high frequency bus converter, the impact of high frequency on converter design must be considered, especially the impact of frequency on transformer size and performance.

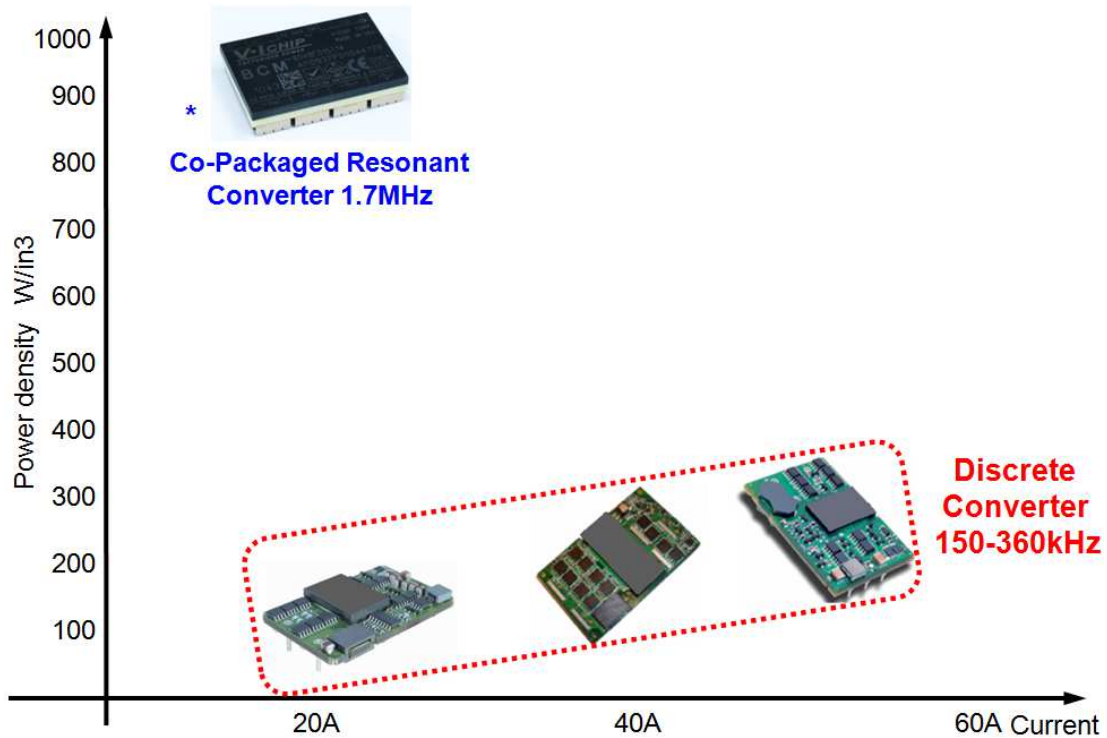


Figure 1.29: Unregulated Bus Converter Power Density Roadmap. *: Picture by author.

1.5.3 Distributed Matrix Transformers for High Frequency Applications

At higher frequencies the transformer design becomes critical to achieving high efficiency and power density. As frequency increases, the impact of the transformer's leakage inductance, core loss, winding loss, and transformer termination loss become a major barrier to efficient converter design. To minimize transformer loss at high frequency a distributed matrix transformer can be employed.

The distributed matrix transformer is defined as an array of elements interwired so that the whole functions as a single transformer [34][35]. Each element being a single transformer that contains a set turns ratio, i.e. 1:1, 2:1 ...:n:1. The desired turns ratio is

obtained by connecting the primary windings of the elements in series and the secondary's in parallel. The benefits of the matrix transformer are that it can reduce winding loss by splitting current between secondary windings connected in parallel, reduce leakage inductance, and improve thermal performance by distributing the power loss throughout the elements. The highest density product available today employs the distributed matrix transformer concept and this dissertation will assess the benefits and weaknesses of the matrix transformer and propose a novel improved structure.

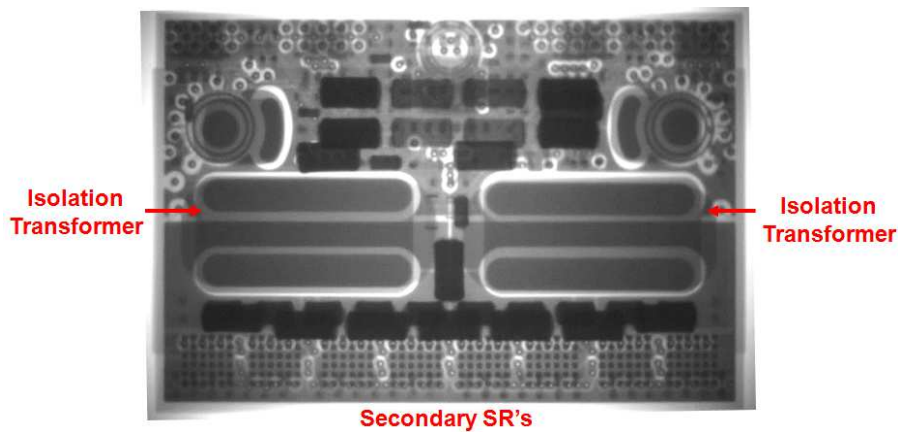


Figure 1.30: Vicor's B048F120T30 $V_{in}=48V$ $V_o=12V$ $I_o=25A$ $F_s=1.7MHz$ Co-Packaged Resonant Unregulated Bus Converter. Picture by author.

1.6 Challenges to High Density Integration

Point of load converters are found everywhere in modern technologies. As the capability and size reduction demands of electronic devices increase through the years, so does their power demands. Methods to supply higher power levels in a smaller solution size are not achievable with conventional technologies. The major bottleneck to improving power density is magnetic size and the major barriers to higher frequency are device technology, packaging of devices, module design, and magnetic design. To

achieve higher power density with improved performance, the following technological challenges will be addressed in this dissertation:

1. Inductor integration in non-isolated POL converters: To improve power density, the minimization of the inductor to facilitate the 3D integration of a low profile magnetic substrate will be targeted with the use of a three level topology for low current discrete Si applications and high current co-packaged GaN designs with the traditional buck topology for high current applications.
2. Utilization of advanced power transistors in high frequency designs: To reduce high frequency device switching loss, the exploration of superior Si lateral trench and GaN high frequency power devices will be considered. The ability of the three level topology to reduce voltage stress, allowing for the use of superior 12V lateral trench devices will be considered in low current non-isolated POL applications. For high current non-isolated POL's and isolated bus converters the use of GaN devices to increase switching frequency will be assessed.
3. Advanced packaging: The impact of device packaging on high frequency performance, the optimization of design parasitics to improve high frequency electrical performance, and the use of advanced substrates to improve high density thermal performance will be explored for non-isolated POL modules.
4. High frequency isolated transformer design: The ability to reduce the size of the transformer at high frequency, utilization of advanced topologies and power devices to achieve higher frequency, and methods to reduce the winding resistance, termination resistance, and leakage inductance for high frequency transformer designs will be considered.

1.7 Dissertation Outline

This dissertation consists of six chapters; the main objective of this work is improving power density and high frequency performance in non-isolated and isolated point of load converters. At higher frequencies, the reduction of magnetic size is possible, facilitating increased levels of integration. To achieve this objective the ability of different topologies, semiconductors, packaging techniques, and magnetic designs are explored for use in non-isolated point of load and isolated bus converters.

Chapter 1 discusses the background for this research. Combining the increasing power demands of modern power systems with the desire for smaller size has led to a push for improved power density. To improve power density, the passive components, which currently occupy the greatest real estate, must be made smaller. Many efforts have been made to improve density by the integration of the passive components, but have been limited by the large energy storage required at lower switching frequencies. To decrease the size of the passives the amount of energy they store must be reduced, either by using higher switching frequencies or different topologies. Improved topologies, power devices, packaging techniques, and circuit design must be utilized to provide higher frequencies, facilitating magnetic integration.

Chapter 2 will explore the use of a three level topology for use in a 12V input voltage, low current ($I_o < 12A$) discrete POL module design. The three level buck converter can significantly reduce the passive size compared to the traditional buck converter employed in the vast majority of currently available POL converters. Another benefit of the three level topology is the reduced voltage stress encountered by the active devices; this allows for the use of improved low voltage devices in a higher voltage

application. This chapter will also propose solutions for the drive circuit, startup, and flying capacitor balancing issues introduced by the three level topology.

Chapter 3 will discuss the use of gallium nitride (GaN) transistors for use in high frequency applications. GaN devices are high electron mobility devices that project to offer significant gains in switching performance in the future over a wide range of voltages. A survey of the current GaN technologies is conducted and the strengths and weaknesses of the currently available technologies will be compared. This chapter will cover the fundamentals of utilizing the GaN transistor in high frequency buck converter design; this will address the packaging of the GaN transistor, fundamental operating differences between GaN and Si devices, driving of GaN devices, and the impact of dead time on loss in the GaN buck converter. An analytical loss model for the GaN buck converter will also be introduced.

Chapter 4 will focus on the optimization of a 2MHz, $V_{in}=12V$, $I_o=20A$ non-isolated GaN POL buck module design. Considered in this chapter are the impact of layout parasitics on module performance, design layout improvement techniques to reduce critical parasitics for a high frequency buck module, the impact of frequency on passive integration, and the thermal design of a high density 3D integrated module. The final demonstration being a 2MHz, $900W/in^3$ co-packaged module, tripling the power density achieved by the current state of the art 12V modules. The final module utilizes GaN power devices, a low profile LTCC inductor, and a DBC based ceramic substrate for improved thermal performance.

Chapter 5 will examine the use of high frequency in unregulated 48V bus converters targeting IBA for use in telecom, networking, and high end computing

applications. This work will explore the impact of switching frequency on transformer core volume, the termination limitations of traditional transformer design at high frequencies, and the impact of leakage inductance and winding resistance at high frequency. The use of distributed matrix transformers to improve high frequency performance by reducing leakage inductance and winding resistance will be assessed. This work will propose a novel improved integrated matrix transformer structure to provide superior high frequency transformer performance. The use of GaN devices in high frequency converter design will also be considered and compared with Si designs. Lastly, a 1.6MHz, $V_{in}=48V$, $V_o=12V$, $I_o=30A$ GaN bus converter employing the proposed integrated transformer structure will be demonstrated, providing a power density of $900W/in^3$, doubling the power density of similar current state of the art bus converter modules.

Chapter 6 is the summary of this work and proposes future work.

Chapter 2

Three Level Buck Converter for High Frequency, Low Current POL Applications

2.1 Introduction

Many everyday technologies such as cellular phones, mp3 players, telecom, automotive, etc. require low current switching power supplies to efficiently convert small levels of power to the various loads. In these applications, small size is paramount and high density solutions are required. Originally, individual POL converters were custom designs for each voltage and current level and built on the main pcb board using discrete components. The active devices, capacitors, inductors, drivers, and controllers were purchased from various companies and were designed by the manufacturer to meet the specific demands of each system. This solution is very complex, with the manufacturer having to redesign the PCB each time the POL demands changed. These applications now generally operate off a standard internal bus voltage (12V, 5V) that can use standardized POL building blocks to power the loads.

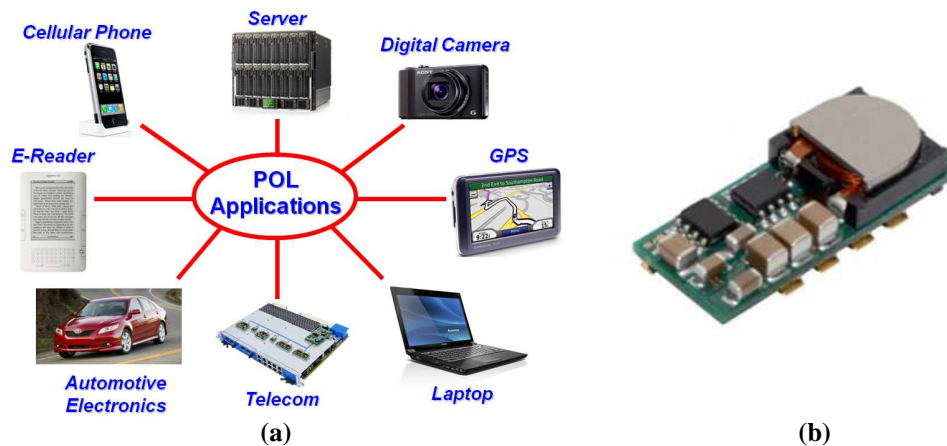


Figure 2.1: (a) Possible applications for point of load converters (b) Discrete point of load module

The POL module, shown in figure 2.1b, contains a complete power supply in a simple, single package form. The module is designed by a power supply company to optimize performance and fit the industry defined standards for footprint and pin outs [36]. These POL modules offer the benefits of design flexibility and scalability and are rapidly replacing the discrete custom designs. As the system demands in the applications change, the manufacturers can simply replace the POL module without having to completely redesign the entire PC board. The majority of POL modules today employ discrete components, limiting switching frequency and power density; this chapter will focus on the improvement of performance and power density for low current discrete POL modules employed in a wide variety of low current applications.

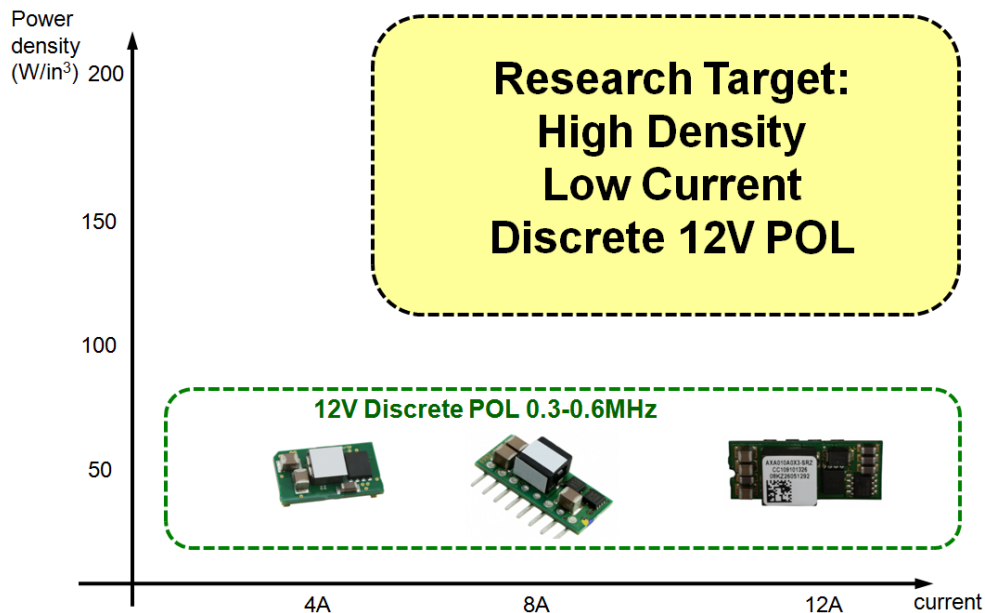


Figure 2.2: Power density comparison of current discrete 12V point of load modules

The majority of POL modules provide a step down conversion ratio and are non-isolated buck converters. The current discrete POL modules operate at frequencies ranging from 300-600kHz to offer high efficiency. Using lower switching frequencies results in an increase in passive size, with inductor size occupying a volume as much as

ten times the active components. Shown in figure 2.2 is the power density comparison of the current products; the power density is limited to the 50W/in³ range and the major barrier to higher power density is the output inductor.

This chapter will discuss the limitations of the traditional buck topology at higher frequencies, propose the use of a three level topology in low current (I_o<12A) V_{in}=12V applications to improve converter efficiency, allow the use of superior low voltage lateral trench devices, and reduce passive size allowing for the use of an integrated low profile magnetic. This chapter will also propose novel methods to solve control, driving, and startup for the three level converter. The final objective of this work is to demonstrate a high density 3D module with an integrated low profile magnetic.

Currently, the switching frequency of the discrete POL converters is decreased to the range of 300-600 kHz to offer higher system efficiency. To improve power density, the passive size must be decreased; for the traditional buck converter the inductance value is given by:

$$L_1 = \frac{V_{in} \cdot (1-D) \cdot D}{\Delta I_{Lph} \cdot f_s} \quad \text{for } D < 0.5 \quad (2.1)$$

Where V_{in} is the input voltage, D is the duty cycle (D=V_o/V_{in}), ΔI_{Lph} is the peak to peak current ripple, which is generally designed to be around 40% of the full load output current, and f_s is the switching frequency.

To decrease the passive size in a traditional buck converter, shown in figure 2.3a, the switching frequency must be increased. The impact of increased switching frequency on efficiency and inductance value is shown in figure 2.3; at higher frequencies the efficiency drops significantly due to switching related losses.

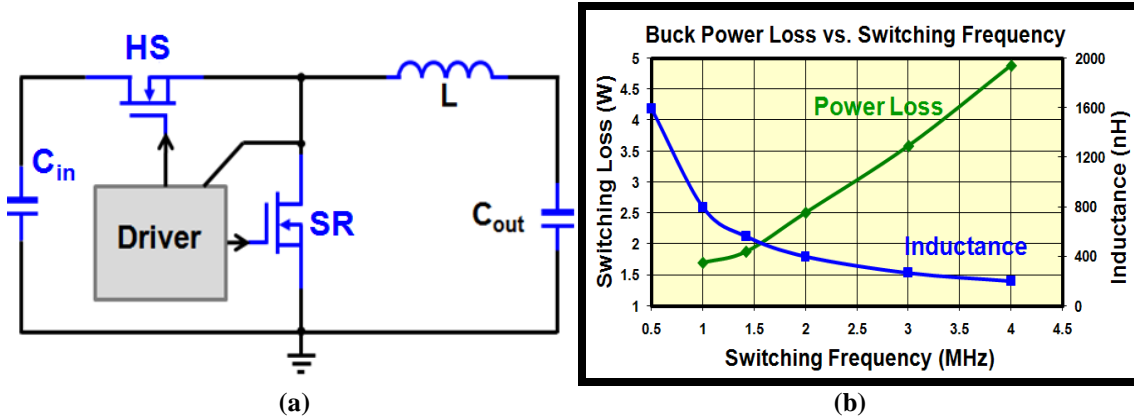


Figure 2.3: Traditional buck converter (a) schematic (b) Power loss and required inductance (40% ripple) for $V_{in}=12V$ $V_o=3.3V$ $I_o=7.5A$, Top switch:RJK0305, Bottom Switch:RJK0302, Driver:LM27222)

Figure 2.4a shows the impact of frequency on converter efficiency from experimental hardware. To quantify the impact of the different circuit parameters on switching loss an analytical model based on [37] is utilized. Using the loss model a detailed loss breakdown is performed and the results are shown in figure 2.4b. From the loss breakdown it becomes apparent that device turn off loss and reverse recovery are the two major barriers to pushing to higher switching frequency.

During the turn off transition of the buck converter, the loss can be roughly given as [38]:

$$P_{HS_Off} = 0.5 \cdot I_{HS_Pk} \cdot V_{HS} \cdot t_{off} \cdot f_s \quad (2.2)$$

Where I_{HS_Pk} is the current in the top device during turn off, V_{HS} is the device drain to source voltage at turn off, t_{off} is the duration of the turn off switching transition, and f_s is the switching frequency. I_{HS_Pk} is given by:

$$I_{HS_Pk} = I_o + \frac{V_{in} \cdot (1-D) \cdot D}{2 \cdot L_1 \cdot f_s} \quad (2.3)$$

Where I_o is the load current, D is the duty cycle, and L_1 is the output inductance. To reduce switching losses, the inductance value can be increased to limit the peak turn off

current. The option to decrease the turn off current to lower loss requires a larger inductance, increasing passive size and decreasing power density, which is undesirable.

For the reverse recovery loss it can be roughly given by:

$$P_{RR} = V_{in} \cdot Q_{RR} \cdot f_s \quad (2.4)$$

Where Q_{RR} is the reverse recovery of the SR body diode. When a diode is quickly reverse biased while it is conducting a high forward current, a finite amount of time is required to remove the charge carriers so that it can begin to block the reverse voltage.

The Q_{rr} of a diode represents its stored charge during this recombination period.

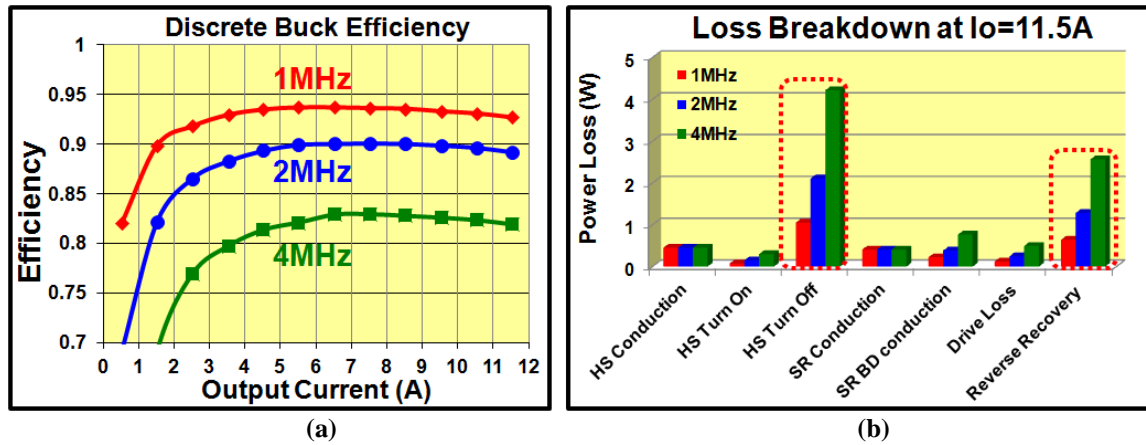


Figure 2.4: (a) Traditional buck converter efficiency and (b) Loss breakdown for $V_{in}=12V$ $V_o=3.3V$ $I_o=11.5A$, Top switch:RJK0305, Bottom Switch:RJK0302, Driver:LM27222)

From equations 2.2 and 2.4 it can be seen that decreasing the voltage across the device can reduce the total switching loss and reverse recovery loss. To lower the device voltage, the input voltage of the buck converter must be reduced. There have been methods proposed to reduce loss using this method for high frequency, high current multi-phase voltage regulators [39], using a highly efficient first stage to step down the input voltage of the multiple downstream POL's, improving high frequency performance. For general low current POL applications, a small number of POL's are employed and adding a first stage to step down the voltage to the buck is not practical.

2.2 12V Three Level Buck Converter

To offer higher power density while maintaining high efficiency the use of a three level non-isolated buck converter is proposed for use in low current 12V input applications. The multilevel converter was originally introduced for high power (kV) inverter applications [40] to allow for multiple superior performing lower voltage devices to be used connected in series to replace a single higher voltage device; for the 12V input applications in this work, the three level topology will allow for a single 25-30V switching at the full input voltage to be replaced with two superior 12V lateral trench devices switching at half the input voltage, improving performance. Another benefit of the original topology was the ability to reduce harmonic content by offering a larger number of available voltage levels; for the non-isolated DC-DC three level buck converter this translates to smaller filter inductance, allowing for reduction in inductor volume and improved power density.

There are two types of multilevel converter topologies: the diode clamped and capacitive clamped circuits. The diode clamped circuit uses clamping diodes to ensure voltage balance between the series connected semiconductors. The capacitive clamped converter uses a flying capacitor to clamp the semiconductor voltage. The capacitive clamped version is preferred at lower voltages because of the low part count. The three level buck converter with capacitor clamping was derived from a voltage chopper circuit in [41]. The balancing of the flying capacitor is critical to circuit operation [42][43]; a novel improved capacitor balancing concept will be proposed in this chapter.

This chapter will discuss the operating principles of the three level converter, the impact of lower switching voltage on performance and passive size, the gains possible by

utilizing superior performing low voltage devices, and the ability of the three level buck converter to integrate a small, high frequency output inductor to offer improved power density. This work will also propose solutions for the drive circuit, startup, and flying capacitor balancing issues associated with the three level topology.

2.2.1 Three Level Buck Converter Operating Principles

The three level buck converter, shown in figure 2.5, can offer improved performance and smaller passive size by reducing the effective voltage across the devices and the inductor. The topology has the same timing diagram as the traditional two phase buck converter where T1 and T2 are driven 180° out of phase and B1 and B2 are driven complimentary to T1 and T2 respectively. The operation of the converter starts at t_0 and ends at t_4 , ending a full period. The three level topology is capable of producing three voltages across the V_A node: $0V$, $0.5V_{in}$, and V_{in} .

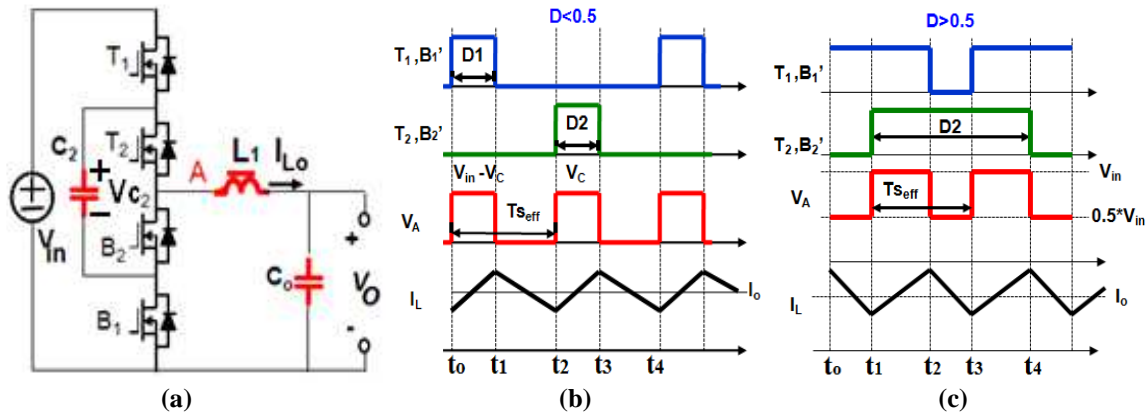


Figure 2.5: (a) Three level Buck Converter. Timing diagram for (b) $D < 0.5$ (c) $D > 0.5$

For $D < 0.5$ the converter operates at the $0V$ and $0.5V_{in}$ levels:

t_0 - t_1 : The switches T_1 and B_2 are on and the input voltage source V_{in} delivers power to the load and charges the capacitor C_2 resulting in a voltage of:

$$VC_{2(t_1)} = VC_{2(t_0)} + \Delta VC_2 = 0.5 \cdot V_{in} + \frac{0.5 \cdot I_o \cdot D_1}{C_2 \cdot f_s} \quad (2.5)$$

$$V_A = V_{in} - VC_2 \approx 0.5 \cdot V_{in} \quad (2.6)$$

Where $VC_{2(0)} = 0.5V_{in}$ at steady state, I_o is the output current, D_1 is the duty cycle for switch T_1 , C_2 is the capacitance of the flying capacitor, f_s is the switching frequency, and V_a in the node voltage at point A in figure 2.5a.

t_1 - t_2 : The switches B1 and B2 are on and the current freewheels, and the node voltage V_a is connected to ground. The flying capacitor voltage does not change as it conducts no current during this period.

$$V_A = 0V \quad (2.7)$$

t_2 - t_3 : The switches T2 and B1 are on and the flying capacitor C2 delivers power to power to the load and the capacitor discharges. The resulting voltage of C2 is given by:

$$VC_{2(t_3)} = VC_{2(0)} - \Delta VC_2 = 0.5 \cdot V_{in} - \frac{0.5 \cdot I_o \cdot D_2}{C_2 \cdot f_s} \quad (2.8)$$

$$V_A = VC_2 \approx 0.5 \cdot V_{in} \quad (2.9)$$

t_3 - t_4 : The switches B1 and B2 freewheel, and the operation is the same as t_1 - t_2 . The time t_4 represents the end of a switching cycle.

When the three level converter is operated over a duty cycle of 50%, the operation follows figure 2.5c and utilizes the $0.5V_{in}$ and V_{in} levels.

t_0 - t_1 : The switches T1 and B2 are on and the input voltage source V_{in} delivers power to the load and charges the capacitor C2 resulting in a voltage of:

$$VC_{2(t_1)} = VC_{2(0)} + \Delta VC_2 = 0.5 \cdot V_{in} + \frac{0.5 \cdot I_o \cdot (1 - D_2)}{C_2 \cdot f_s} \quad (2.10)$$

$$V_A = V_{in} - VC_2 \approx 0.5 \cdot V_{in} \quad (2.11)$$

t_1 - t_2 : The switches T1 and T2 are on and the input voltage is connected directly to the output. The flying capacitor voltage does not change as it conducts no current.

$$V_A = V_{in} \quad (2.12)$$

t_2 - t_3 : The switches T2 and B1 are on and the flying capacitor C2 discharges delivering power to the load. The resulting voltage of C2 is given by:

$$VC_{2(t_3)} = VC_{2(t_0)} - \Delta VC_2 = 0.5 \cdot V_{in} - \frac{0.5 \cdot I_o \cdot (1 - D_1)}{C_2 \cdot f_s} \quad (2.13)$$

$$V_A = VC_2 \approx 0.5 \cdot V_{in} \quad (2.14)$$

t_3 - t_4 : The switches T1 and T2 are on and the input voltage is connected directly to the output, and the operation is the same as t_1 - t_2 . The time t_4 represents the end of a switching cycle.

The voltage transfer relationship for the three level buck is the same as the traditional buck converter and given by:

$$\frac{V_o}{V_{in}} = D = D_1 = D_2 \quad (2.15)$$

Where D is the duty cycle of devices T1 and T2.

2.2.2 Passive Size Reduction of Three Level Buck Converter

The three level buck converter can greatly reduce magnetic size or reduce the switching frequency without suffering a bulky magnetic component. This makes this topology very attractive for low current point of load converters. By decreasing the

voltage across the inductor the inductor ripple current for the three level converter is given by:

$$\Delta i_{3Lpk-pk} = \frac{V_{in} \cdot (0.5 - D) \cdot D}{L_1 \cdot f_s} \text{ for } D \leq 0.5 \quad (2.16)$$

$$\Delta i_{3Lpk-pk} = \frac{V_{in} \cdot (1 - D) \cdot (D - 0.5)}{L_1 \cdot f_s} \text{ for } D > 0.5 \quad (2.17)$$

Where V_{in} is the input voltage, D is the duty cycle, L_1 is the filter inductance, and f_s is the switching frequency. The ripple currents are found using the assumption that $V_{c2}=0.5V_{in}$ and the capacitor voltage ripple is negligible. Figures 2.6 a&b show the inductance reduction offered by the three level buck converter over the traditional buck for the same switching ripple, which is four times at worst case, and the impact of inductance value on inductor volume.

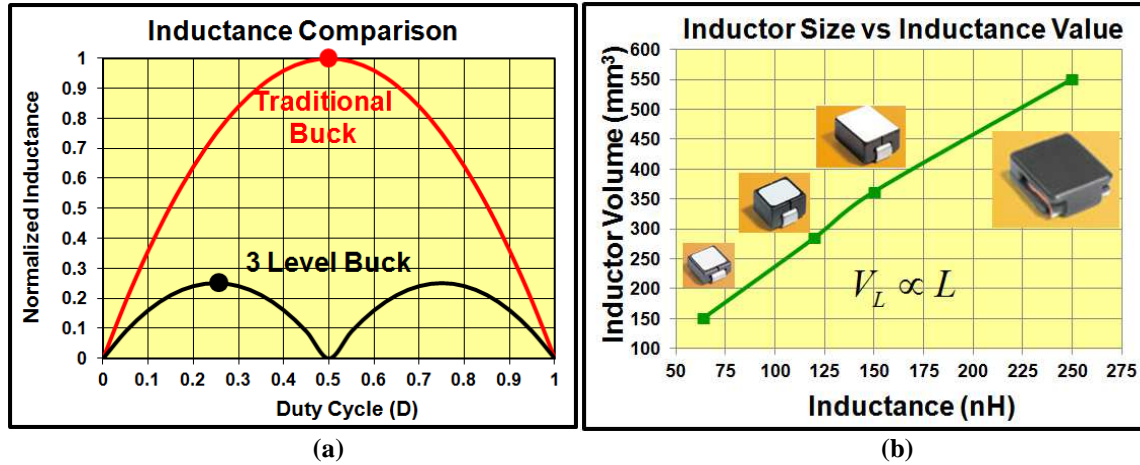


Figure 2.6: (a) Inductance comparison with same switching frequency and inductor ripple current (b) Inductor volume vs value for commercial discrete inductors

The ability to reduce the magnetic size over the traditional buck can offer significant improvements in power density. The three level buck converter also offers reduction in required output capacitance. The output voltage ripple for the traditional buck converter is given as [44]:

$$\Delta V_{Buck_pk_pk} = \frac{\Delta I_{Lph}}{8 \cdot C_o \cdot f_s} \quad (2.18)$$

Where ΔI_{Lph} is the peak to peak ripple of the buck converter found from equation 2.1, C_o is the output capacitance value, and f_s is the switching frequency.

For the three level buck converter, the effective switching frequency is doubled and the output voltage ripple is given as:

$$\Delta V_{3L_pk_pk} = \frac{\Delta i_{3Lpk-pk}}{16 \cdot C_o \cdot f_s} \quad (2.19)$$

From equations 2.18 and 2.19 it can be seen that the output voltage ripple is controlled by the inductor current ripple. For the POL applications the size of the filter inductor is significantly larger than the output capacitance. For this reason, the three level converter for this work is operated with the same current ripple, resulting in a two times reduction in output capacitance. In applications where minimizing the output capacitance or voltage ripple is critical the three level buck with a similar inductance can reduce the output capacitance by a factor of eight [42].

2.2.3 Flying Capacitor Selection

The basic operating principles discussed in the previous sections are based on the assumption that the flying capacitor is balanced to half of the input voltage and kept at a DC value. In practical designs, the flying capacitor adds physical size, introduces additional parasitics, and has a voltage ripple. The peak to peak capacitor voltage ripple is given by:

$$\Delta V_{Cf_pk_pk} = \frac{D \cdot I_o}{C_f \cdot f_s} \quad (2.20)$$

Where D is the duty cycle, I_o is the output current, C_f is the flying capacitance value, and f_s is the switching frequency.

To maintain a small voltage ripple, a large enough flying capacitance must be selected based on the design requirements. For higher duty cycles, output currents and lower frequencies the amount of capacitance required increases. For the design in this work, the maximum values for the flying capacitor occur at duty cycle of 0.5 and the highest output current considered is 12 amperes.

From figure 2.7 it can be seen that having a capacitance value of 60 μ F at 2MHz the voltage ripple of the flying capacitor can as low as 50mV. For a 12V input case, this corresponds to a capacitor voltage ripple of less than 1%. A small ripple voltage will ensure the devices do not exceed their low voltage rating and that the converter operates at its optimal conditions.

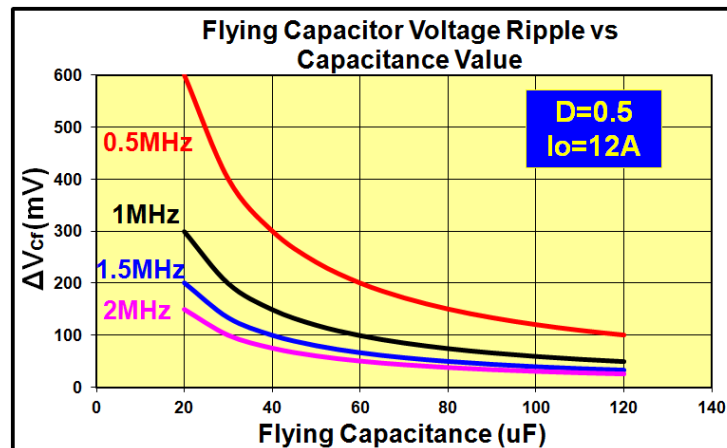


Figure 2.7: Flying capacitor voltage ripple vs flying capacitance for $D=0.5$, $I_o=12A$

Another concern with the flying capacitor is the current handling capability of the capacitor. To ensure long term reliability of the converter, the capacitor must be designed to handle a suitable amount of current. The dependence of the capacitance value of temperature on ripple current for a typical low voltage ceramic capacitor is shown in figure 2.8a [45]. As the frequency and rms current of the capacitor increase the

temperature of the capacitor rises. The impact of temperature rise on capacitance is shown in figure 2.8b. Above 45°C the capacitance value drops significantly with an increase in temperature and the maximum operating temperature is limited to 85°C. The rms value for the capacitor current is given by:

$$I_{Cf_RMS} = I_o \cdot \sqrt{2D} \cdot \sqrt{1 + \frac{(\Delta I_{3L_pk_pk})^2}{12 \cdot I_o^2}} \quad \text{for } D \leq 0.5 \quad (2.21)$$

$$I_{Cf_RMS} = I_o \cdot \sqrt{2(1-D)} \cdot \sqrt{1 + \frac{(\Delta I_{3L_pk_pk})^2}{12 \cdot I_o^2}} \quad \text{for } D > 0.5 \quad (2.22)$$

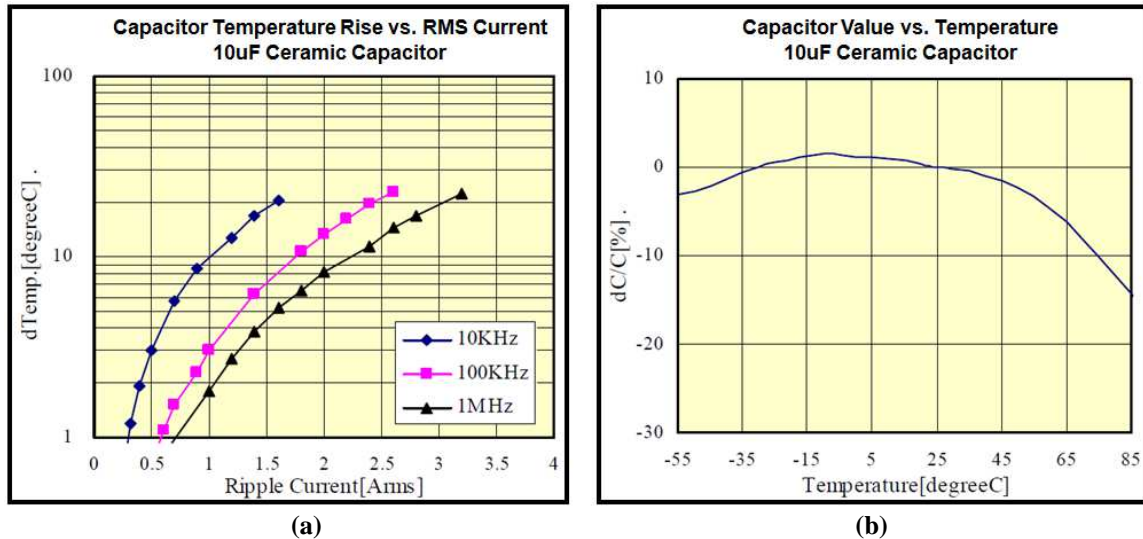


Figure 2.8: (a) Capacitor temperature rise vs. ripple current (b) Capacitance value vs. temperature

For the low voltage designs, multiple ceramic capacitors will be placed in parallel to reduce the equivalent resistance and inductance of the capacitor bank and to limit the maximum current flowing through each capacitor. Figure 2.9 shows the flying capacitor RMS current vs duty cycle for a 12A load current case, to keep the capacitor ripple below 2 ampere six capacitors were placed in parallel.

The capacitor selected for this design is a 16V 0805 10uF, the equivalent series resistance for this capacitor is given from the data sheet to be 3.3mΩ and the equivalent

series inductance is 0.46nH. Using six of these capacitors in parallel can reduce the effective ESR to 0.55mΩ and the effective ESL to 0.08nH. With the proper selection of the flying capacitor for an effective switching frequency of 2MHz, the worst case loss is limited to 79mW of conduction, the ripple is limited to 100mV, and the capacitor RMS is safely limited under 2A of current. The total volume occupied of the capacitor bank is 12.75mm³ which is only 3.5% of the volume occupied by a discrete 150nH inductor.

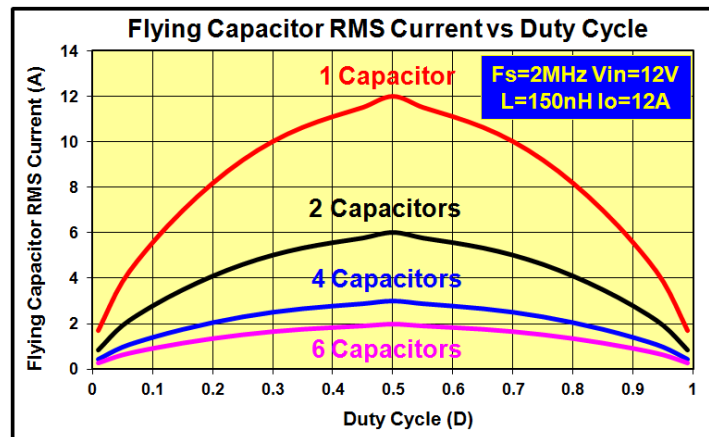


Figure 2.9: Flying capacitor RMS current vs duty cycle for $V_{in}=12V$, $L=150nH$, $I_o=12A$

2.2.4 Advantages of Low Voltage Devices

For this work, high efficiency is critical and the three level buck converter will be operated with the same effective frequency of the traditional buck converter, allowing for a 50% reduction in inductance value while offering improved performance. Operating at the same effective switching frequency as a traditional buck converter the three level topology can switch while seeing half of the voltage stress as shown in figure 2.10, this allows for lower switching losses, reverse recovery loss, and the use of lower voltage rated devices.

During all periods the voltage stress the devices must support is equal to:

$$V_{ds} = V_{in} - V_{c2} = V_{c2} = 0.5 \cdot V_{in} \quad (2.23)$$

Where V_{c2} is the voltage across the flying capacitor and assumed to be balanced to equal half the input voltage.

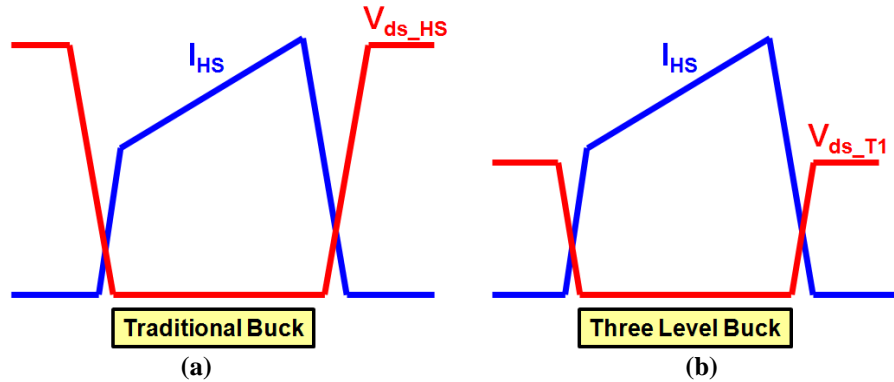


Figure 2.10: Current and voltage waveforms of top switch in (a) Traditional buck converter (b) Three level buck converter

The reduced voltage stress allows the three level converter to use low voltage devices for a higher voltage application. With the improvements in lateral and lateral trench devices they can offer major performance gains over trench devices in the 5-12V breakdown voltage range as well as provide superior packaging which will be discussed in detail in chapter 4. Fig. 2.11 shows the figure of merit (FOM) compared to the breakdown voltage for commercially available devices. The FOM is directly related to loss [46] and the low voltage devices available for three level converter offer superior performance over the traditional buck converter.

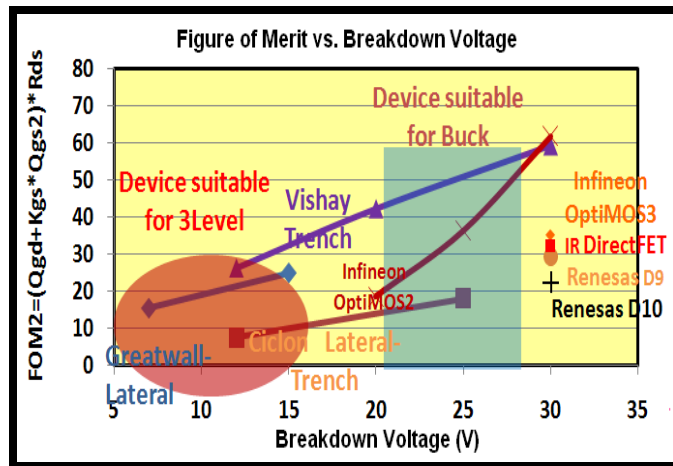


Figure 2.11: Figure of merit comparison vs. breakdown voltage

For the experimental verification, 30V devices were used for the traditional buck converter; for the three level buck converter the 12V lateral trench device from Ciclon was used to minimize loss. From table 2.1 it can be seen that the low voltage lateral trench device can offer superior performance when compared to the traditional trench device. Comparing devices with similar gate charges, the low voltage lateral trench can offer a 33% reduction in the miller charge, which contributes directly to turn off loss, and a 69% reduction in on state resistance. Due to the use of two devices in series in the three level converter, the effective resistance in the three level is doubled and the effective resistance is reduced by 37%. With the improved low voltage devices combined with lower switching voltage seen across the device, the three level converter can provide significant performance gains.

	Device	Voltage Rating (V)	Miller Charge Qgd (nC)	Gate Charge Qg (nC)	On Resistance Rdson (mΩ)
Traditional Buck	RJK0302	30	6.0	28	3.5
3 Level Buck	CSD13301	12	4.0	30	1.1

Table 2.1: Device comparison for traditional two level and three level buck converter

2.2.5 Experimental Results

To demonstrate the ability of the three level converter to offer superior performance over the single phase buck, hardware was built and tested. The three level converter used low voltage lateral trench devices from Ciclon (CSD13301) for the synchronous rectifier switches which had a breakdown voltage of 12V. At the time of this work no low voltage top switches were commercially available, and RJK0305 were used for the top switches. With low voltage top switches performance could be further improved; the top switch lateral trench device is in development in [47]. The gate driver for the three level converter was 2xLM27222, and the inductor was a coilcraft SLC1175.

The gate drive design details are discussed later in this chapter. The flying capacitor for the three level converter was 6x10uF ceramic capacitors. For the traditional buck converter 30V trench devices from Renesas were used with RJK0305 for the top switch and RJK0302 for the SR. The driver used was a single LM27222 and the inductor was a coilcraft MVR1251.

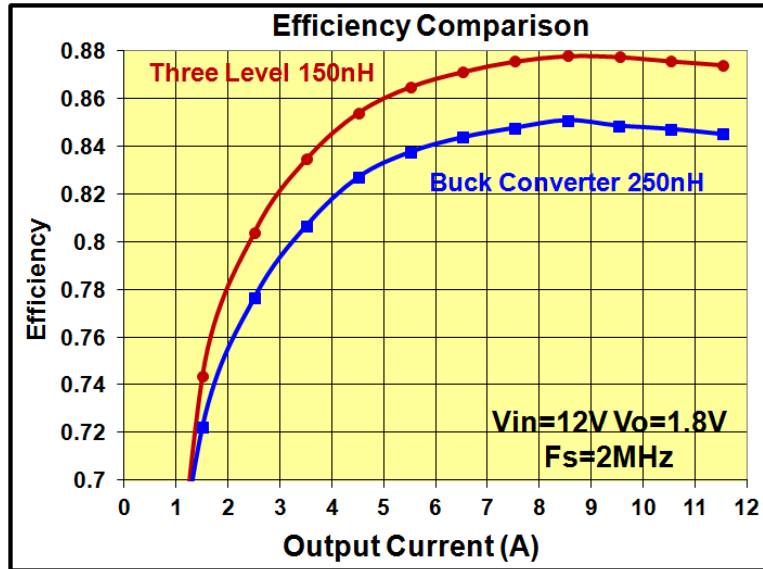
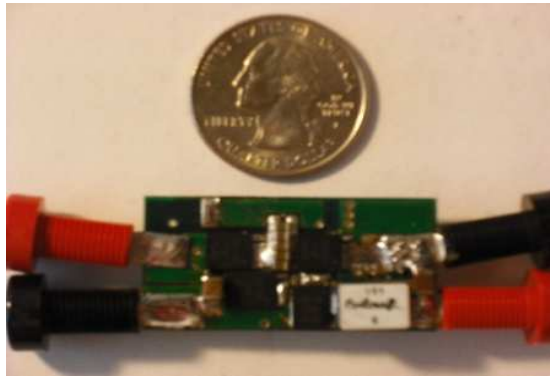
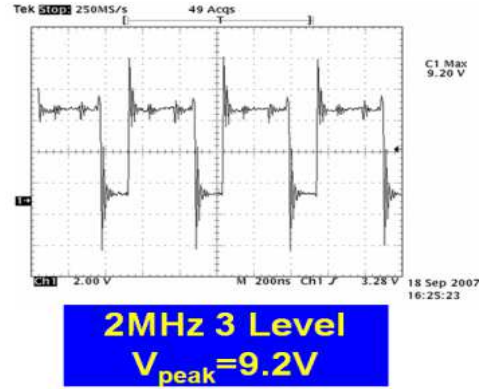


Figure 2.12: Efficiency comparison $V_{in}=12V$, $V_o=1.8V$, F_s effective= 2MHz

The operating frequency for the three level converter was 1MHz; resulting in an effective switching frequency of 2MHz, and an inductance of 150nH was selected. The traditional buck was operated at a switching frequency of 2MHz and an inductance value of 250nH was chosen to give similar current ripple as the three level converter. The efficiency curve shown in figure 2.12 shows that the three level converter achieves over 3% gain in peak efficiency and a 2.5% gain in full load efficiency when compared to the traditional buck converter while using an inductance 40% smaller. The hardware and voltage stress waveforms for the buck converter and three level converter are shown in figure 2.13. The three level converter experiences a peak voltage stress across the SR of 9.2V, giving a sufficient overvoltage margin while using a 12V rated device.



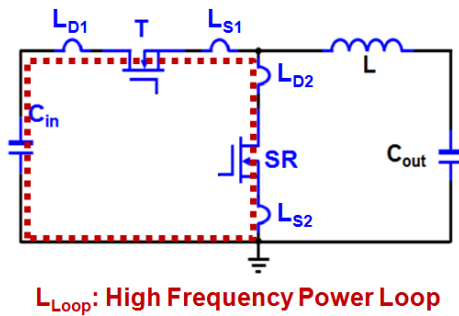
(a)



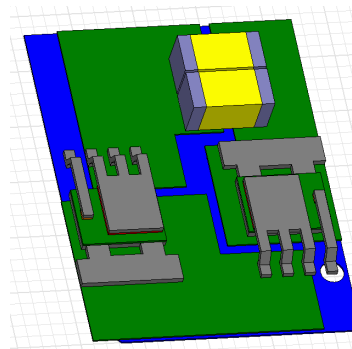
(b)

Figure 2.13: (a) Experimental hardware (b) Three Level Buck Peak MOSFET Voltage

To perform a detailed loss breakdown of the buck and three level converter to compare the topologies, the parasitics involved in the layout of each design must be considered. For the traditional buck converter the high frequency power loop, shown in figure 2.14a, L_{Loop} , is the parasitic inductance from the positive terminal of the input capacitance, through the top device, synchronous rectifier, and ground loop to the input capacitor negative terminal. A FEA model, shown in figure 2.14b, was created to model the PCB layout and device parasitics to extract the loop inductance of the traditional buck design.



(a)



(b)

Figure 2.14: (a) Synchronous buck converter parasitic loop (b) FEA model for traditional buck converter

For the three level buck converter, there are two different switching transitions, and two separate parasitic loops as shown in figures 2.15a and 2.15b. To achieve low

loss and capacitor voltage balance these two inductances should be as close as possible in value. For optimal efficiency, these loops are minimized in size. Table 2.2 shows the resulting parasitic loops for the traditional buck converter and the two separate loops for the three level buck converter. The loop inductances between the traditional buck converter and three level converter are similar in value as a result of the loops being similar in physical size and the same packages used for all of the power devices. For the three level converter the loop inductances vary only slightly, ensuring proper operation to help balance the flying capacitor.

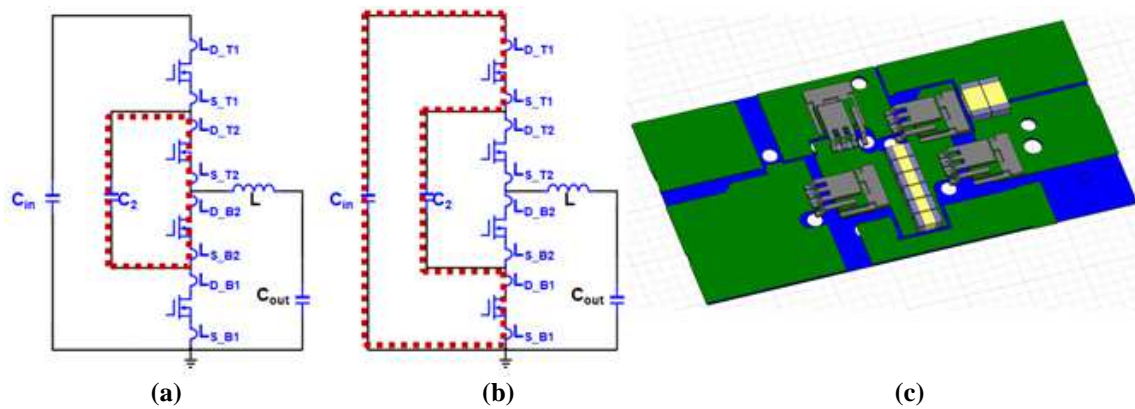


Figure 2.15: Three level buck converter parasitic loop (a) Loop 1 for t_2-t_3 (b) Loop 2 for t_0-t_1 (c) FEA model of experimental hardware

	Traditional Buck	3 Level Buck Loop 1	3 Level Buck Loop 2
Parasitic Inductance (nH)	2.91	2.87	3.02

Table 2.2. Parasitic comparison for traditional two level and three level buck converter

The loss breakdown for the two designs is shown in figure 2.16, the major gains in efficiency come from the reduction of turn off loss and reverse recovery losses. The turn off loss and reverse recovery loss are the barriers to high frequency in the traditional buck converter and the three level buck converter can significantly reduce these losses at high frequency with ability to reduce the voltage stress across the device by a factor of two, as shown in 2.24 and 2.25. The utilization of improved low voltage devices

provides a significant decrease in SR conduction loss. With proper design of the flying capacitor network, the additional loss from the flying capacitor is small.

$$P_{HS_Off} = 0.25 \cdot I_{HS_Pk} \cdot V_{HS} \cdot t_{off} \cdot f_s \quad (2.24)$$

$$P_{RR} = 0.5 \cdot V_{in} \cdot Q_{RR} \cdot f_s \quad (2.25)$$

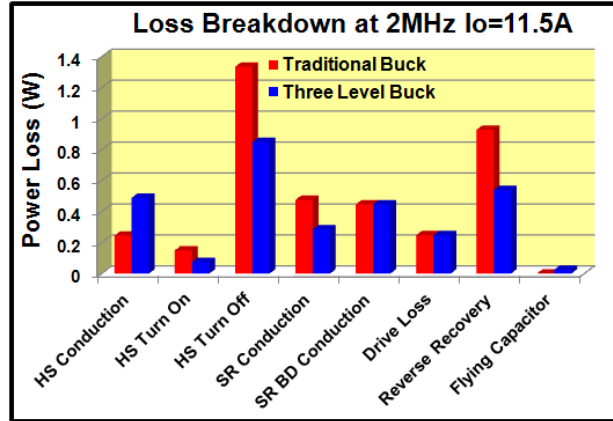


Figure 2.16: Comparison of 2MHz traditional buck and three level converter loss breakdowns

2.2.6 Gate Drive Design for Three Level Converter

The three level converter has a totem pole configuration that requires special care to provide a simple, effective gate drive solution [48]. The majority of low voltage buck converters are driven by commercial IC's utilizing a boot strap capacitor to drive the high side device due to their simplicity and small size. To simplify the circuitry of the three level converter, a drive structure, shown in figure 2.17, was created to drive the four three level devices using two bootstrap IC's.

The operation of the driver structure is that during the period t_0-t_1 the bootstrap capacitor CB2 is connected to the gate to source of switch T_2 , turning on the device. When device T_2 is on, the switching nodes V_{sw} and A are shorted. Diode DT1 turns on if the voltage of $CB1 < CB2$, connecting bootstrap capacitors CB1 and CB2 in parallel, allowing CB1 to be charged to the level of CB2. During period t_1-t_2 the converter is freewheeling with switches B_1 and B_2 on; the bootstrap capacitor CB2 is charged as it is

connected directly to ground. During period t_2 - t_3 the T1 device is turned on by the bootstrap capacitor CB1. Due to the floating ground of the T_2/B_2 driver, a diode is used to clamp the VSW2 voltage to ground to prevent false triggering.

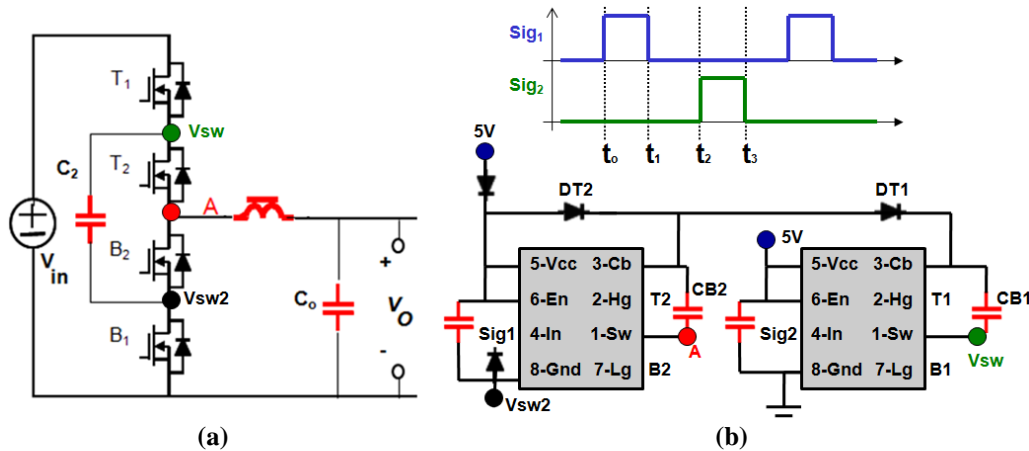


Figure 2.17: (a) Three level buck converter schematic (b) Driver scheme and timing diagram

2.2.7 3D Integration with Low Profile LTCC Inductor

With space at a premium in high density applications, the adoption of 3D integration is increasing rapidly to provide smaller footprint solutions [49]-[51]. An example of a 3D integrated product is shown in figure 2.18. Comparing this design technique to the 2D POL solution, shown in figure 2.18b, it can be seen that by fitting the magnetic footprint to the PCB size and mounting the inductor over the power stage the footprint and power density can be improved significantly. With the large magnetic component introduced by the traditional buck converter the inductor still remains very large and further limits the power density of the module.

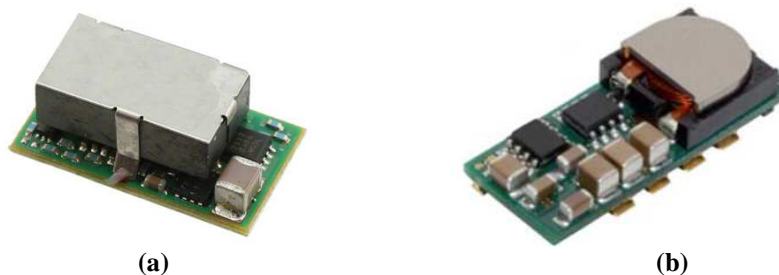


Figure 2.18: (a) 3D integrated point of load module (b) 2D point of load module

The three level buck converter has demonstrated the ability to improve efficiency at higher frequencies and significantly reduce the required inductance. At lower inductance values the ability to integrate a low profile magnetic structure is possible. Many efforts have been made to improve low profile magnetic substrates using low temperature co-fired ceramics (LTCC). To demonstrate high power density capability of the three level converter, an inductor designed in [52] was considered with the three level converter for a 12V application. A more detailed design process and inductor performance comparison for this case is discussed in the reference. The inductor conceptual drawing and experimental hardware is shown in figures 2.19 a&b. The final LTCC inductor had a thickness of 2mm, a via hole radius of 0.4mm, a distance of 0.5mm between the inductor vias, and a DCR of 1.5m Ω .

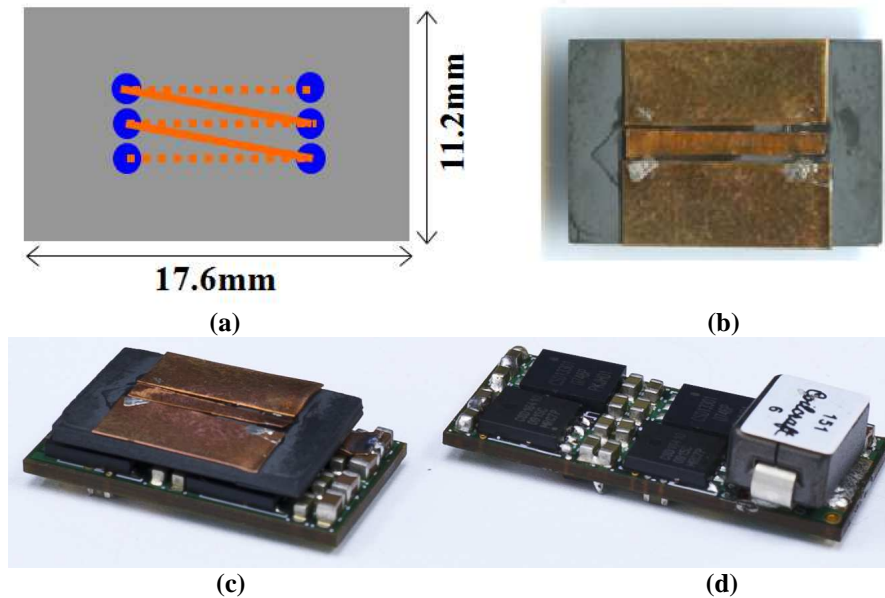


Figure 2.19: Low profile LTCC inductor (a) Conceptual view (b) Experimental prototype. Hardware designs: (c) 3D integrated converter with LTCC inductor (d) 2D design with discrete inductor

The low profile inductor, shown on circuit in figure 2.19c, can improve power density and reduce the required overall footprint of the module. The size and DCR comparisons of the inductors are shown in table 2.3, the LTCC inductor can provide low

profile and fit the footprint of the active area. The drawback is that the inductor DCR increases, decreasing high current performance slightly.

	Core Thickness	Footprint	Winding DCR
Discrete Inductor	7.2mm	84mm ²	0.25mΩ
LTCC Inductor	2mm	197mm ²	1.5mΩ

Table 2.3: Comparison between discrete and low profile inductor

The power density comparison of the three level designs demonstrated in this chapter and the discrete industry products is shown in figure 2.20. The ability of the three level converter to decrease inductor size significantly improves power density in 3D and 2D designs, increasing the power density by a factor of two when compared to the traditional buck converters. The $V_{in}=12V$, $I_o=11.5A$, $F_{\text{effective}}=2\text{MHz}$ three level buck converter with a 3D LTCC inductor can achieve a power density of $200\text{W}/\text{in}^3$. The three level buck has further potential to push frequency through the use of lateral based integration which is not possible for the traditional trench based buck converter, the advantages offered through integration for the three level can offer further improvements in power density and performance.

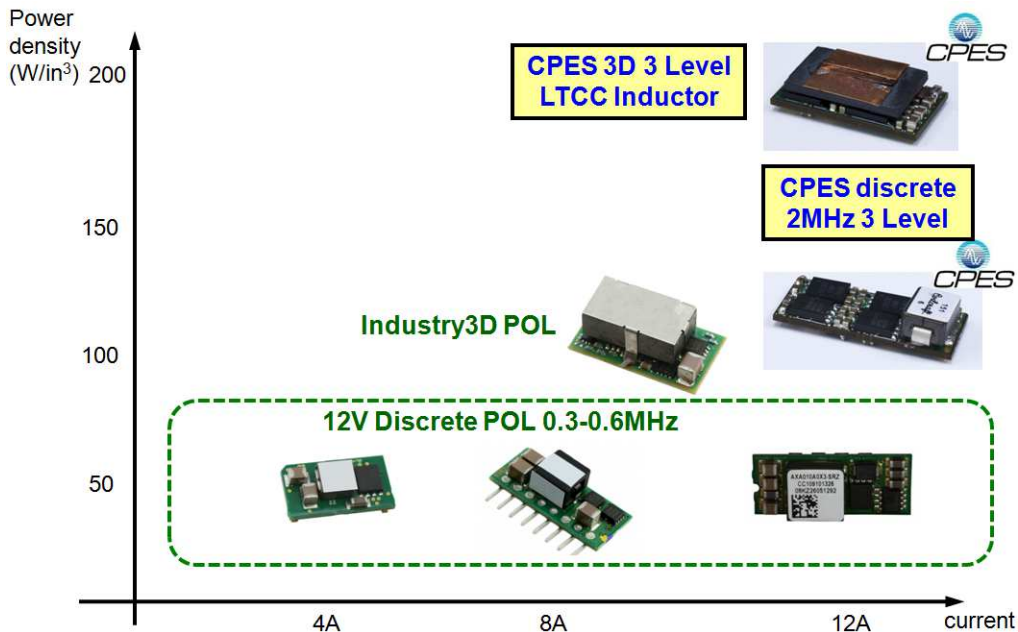


Figure 2.20: Power density map of discrete high density power modules

2.3 Flying Capacitor Balancing Methods

The three level converter's benefits are maximized when the flying capacitor voltage is balanced to half of the input voltage. In theory, if the duty cycles D1 and D2 remain the same the capacitor will naturally remain balanced. In practical circuit design, there are parasitics, device tolerances, and driver variations that make control necessary to balance the capacitor. Shown in figure 2.21 is hardware waveform for an unbalanced flying capacitor case.

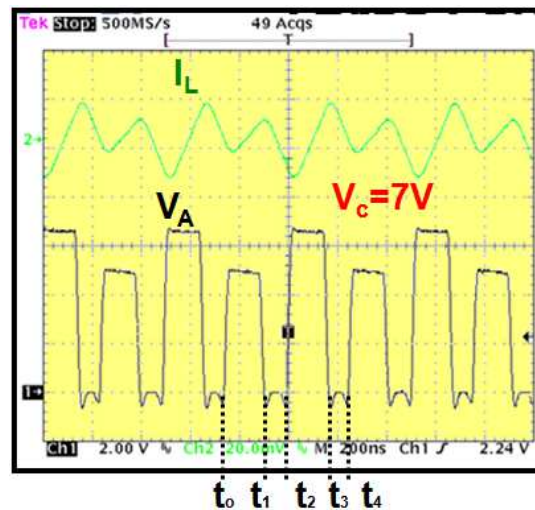


Figure 2.21: Circuit operation with capacitor unbalance

When the three level converter operates with an unbalanced flying capacitor, half the devices will see larger voltage stress, possibly damaging the device if a low voltage device is employed. Another side effect of capacitor unbalance is an asymmetrical current waveform with the current ripple increasing for the device experiencing the larger voltage stress, further increasing loss in the device. The current slope for the inductor current during the power delivery periods t_0-t_1 and t_2-t_3 is:

$$\frac{di_L}{dt} = \frac{V_A - V_o}{L_1} \quad (2.26)$$

In previous research, the capacitor voltage is directly measured using isolation [53] or by using digital timing controls [42][43] and complex networks balance the capacitor voltage. The isolation method requires an additional magnetic component which is unattractive in small power supplies and using digital timing controls requires additional measurements of the input and inductor node voltage; and both methods require an additional control loop. Another drawback of these methods is that they regulate the output voltage by controlling one duty cycle (charging period, t_0-t_1) and then alter the other duty cycle (discharging period, t_2-t_3) to balance the flying capacitor. This degrades the regulation capability and transient response because there is only one power delivery phase regulating the output.

2.3.1 Novel Flying Capacitor Balancing with Current Control

The method proposed in this work to regulate the flying capacitor without a separate capacitor balancing loop is by using self balancing current mode control. Current mode control is widely used in fast transient applications because of its ability to have good line regulation and to ease current sharing for multiple phases. Leading edge modulation can be adapted and naturally balance the capacitor in the three level converter by balancing the inductor current. This is possible because the inductor current contains the capacitor voltage information and is balanced when the inductor current is balanced. Figure 2.22 shows the unbalanced open loop operation on the left in pink, the right section in blue is the closed loop operation. When the control begins for the case $V_c < 0.5V_{in}$:

t_0-t_1 : The inductor current rises at a higher rate during the charging period as a result of increased voltage across the inductor, the slope is given by:

$$\frac{di_L}{dt} = \frac{V_{in} - V_{c2} - V_o}{L} > \frac{0.5 \cdot V_{in} - V_o}{L} \quad (2.27)$$

As a result of the high slope, the inductor current value at time t_1 is larger than the balanced case when the clock signal triggers the turn off of device T1.

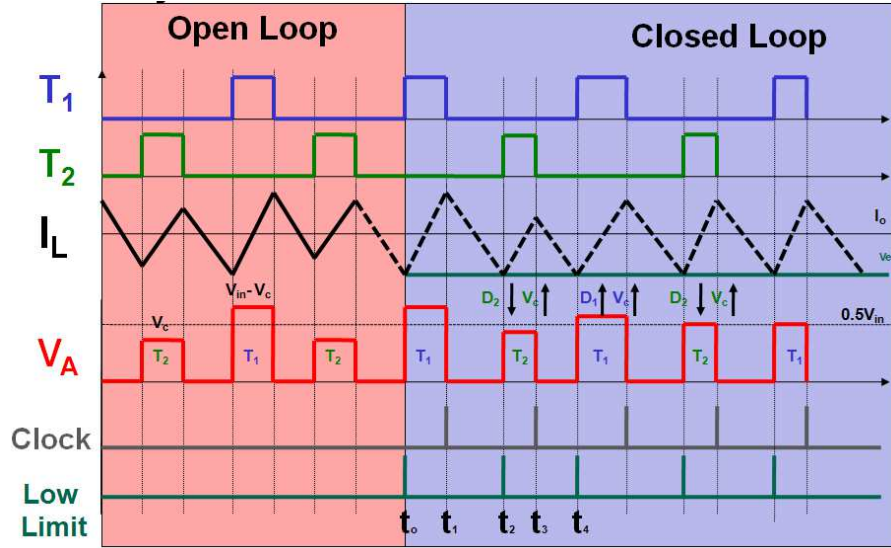


Figure 2.22: Unbalanced operation and closed loop balancing process for $V_c < 0.5V_{in}$

t_1 - t_2 : The inductor current falls during this period and ends when the low error signal is triggered by the inductor current. As a result of the high peak current at time t_1 , this period will be longer than the balanced case. The current slope is given by:

$$\frac{di_L}{dt} = \frac{-V_o}{L} \quad (2.28)$$

t_2 - t_3 : Due to the lengthening of the t_1 - t_2 period, the discharging period (t_2 - t_3) is shortened in duration. The inductor current begins to rise at a lower rate than t_0 - t_1 during this period and ends with the clock triggering turn off of T2.

$$\frac{di_L}{dt} = \frac{V_{c2} - V_o}{L} < \frac{0.5 \cdot V_{in} - V_o}{L} \quad (2.29)$$

The net effect of the shortening of the discharging period in relation to the charging period is an increase in voltage. The net rise in capacitor voltage will be related to the difference in D1 and D2 and is described in 2.31.

t_3-t_4 : During this period the current freewheels and the inductor current falls. This period is shorter in duration than the t_1-t_2 period because the inductor current reached a lower peak at t_3 . As a result of the short duration of this period, a longer charging period is set up in the next cycle.

This sequence repeats with the capacitor rising in voltage until it becomes balanced ($V_c=0.5V_{in}$) and the inductor currents become balanced:

$$\frac{di_L}{dt} = \frac{0.5 \cdot V_{in} - V_o}{L} \quad (2.30)$$

For the case when $V_c > 0.5V_{in}$ the operation is very similar. The high slope period now being the discharging t_2-t_3 period and the capacitor voltage dropping until the inductor current is balanced leading to capacitor voltage balance. For the case $D > 0.5$, trailing edge modulation should be used to control and balance the currents.

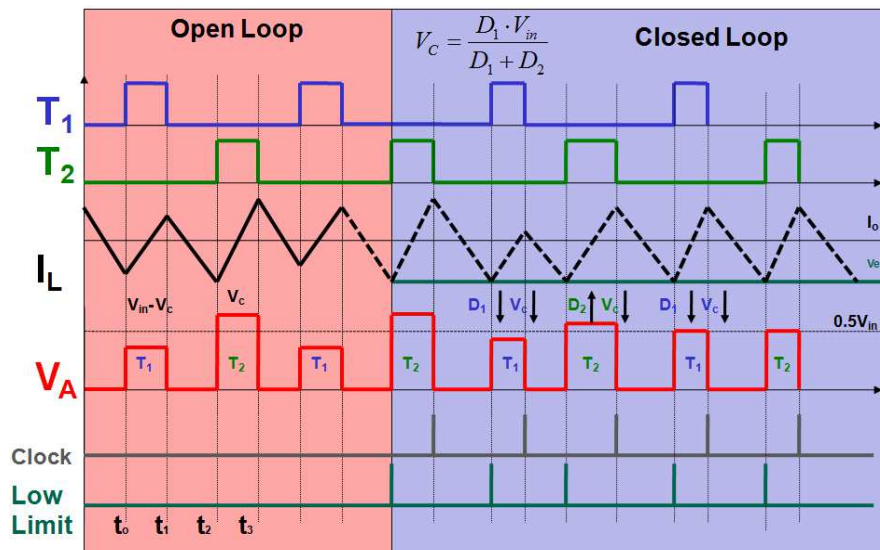


Figure 2.23: Unbalanced operation and closed loop balancing process for $V_c > 0.5V_{in}$

2.3.2 Simulation Verification of Control Method

To verify this control concept, the control method was simulated using SABER. This simulation would also test the control method during transient responses. The balance of the flying capacitor during load transients must be handled to ensure the use of lower voltage devices. The net change in voltage across the capacitor during a charging and discharging period is related to the difference in duty cycles, D1 and D2:

$$\Delta V_{c2_DC} = \frac{I_o \cdot \Delta D}{C_2 \cdot f_s} = \frac{I_o \cdot (D_1 - D_2)}{C_2 \cdot f_s} \quad (2.31)$$

The flying capacitor C2 should generally be chosen to be large enough that the ripple is very small. If this is done then the flying capacitor voltage deviation during a load transient should be also very small. Fig. 2.24 shows the simulation setup of the controller implemented in SABER.

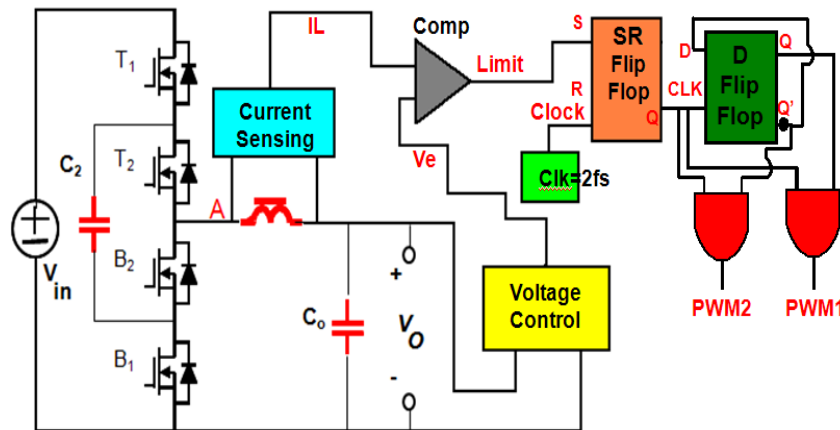
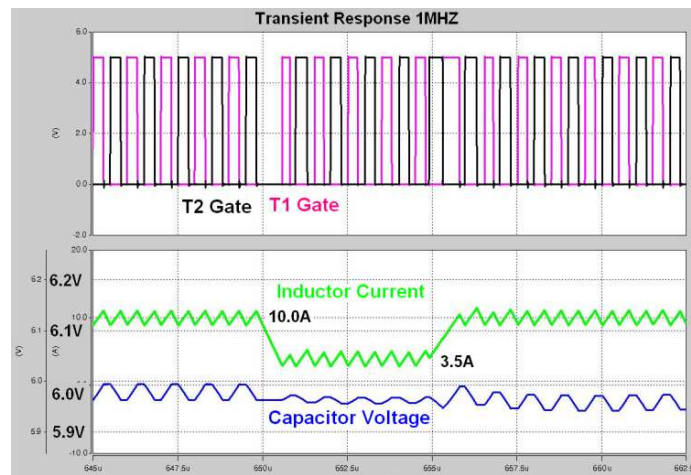


Figure 2.24: Proposed leading edge current control scheme applied to three level buck

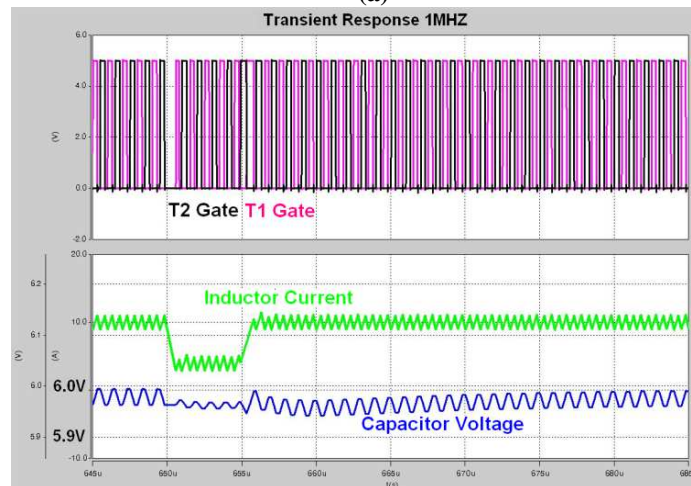
Figure 2.25 shows the response of the converter during a load step down from 10A to 3.5A. Both phases will be turned off until the error is triggered, which tracks the load current, and the capacitor voltage will not change while the phases are off. The voltage will change when the current reaches the new value and rebalance. During a load

step up the switches run at 50% duty cycle until the load current is reached. After this, the capacitor voltage will rebalance. During load transients, the two phases have at most one phase with different duty cycles resulting in little rebalancing required.

Once the load transient is completed the converter returns to steady state operation and the capacitor is rebalanced as shown in figure 2.25b. The total voltage deviation on the flying capacitor for a 60% load step is less than 100mV. Using a current control scheme to balance the capacitor provides a simpler, more effective control scheme than the previously proposed balancing schemes.



(a)



(b)

Figure 2.25: (a) Transient Response Zoomed to Load Transient (b) Transient Response with Capacitor Rebalancing Period

The gate voltages of these two devices is slowly ramped up so that they operate in saturation mode as voltage controlled current sources limiting the current while charging the capacitor to the voltage set by the resistive voltage divider ($0.5 \cdot V_{in}$). When the capacitor is charged to the level set by the resistive divider the comparator will go high turning off the start up devices. In figure 2.26c it can be seen that the peak charging current is 7A, if a slower ramp voltage is used the current can be decreased with the trade off being start up current vs. start up speed.

2.4 Conclusions

This chapter explored the ability of the three level buck converter to reduce passive size and increase efficiency over the traditional buck converter in low current point of load applications. This improved performance was achieved by doubling the effective switching frequency, reducing the voltage across the inductor, and reducing the voltage stress across the semiconductors to $0.5V_{in}$, reducing switching loss and allowing for the use of superior low voltage devices. The gain in efficiency and magnetic reduction is verified experimentally. To improve power density of the converter, the discrete inductor is replaced with a low profile LTCC inductor and packaged in a 3D arrangement.

To ensure the performance gains offered by the topology the flying capacitor voltage must be balanced. A novel control scheme that offers better performance, fast transient, and simplicity is proposed by modifying standard leading edge (valley mode) current control for the three level converter. The balancing of the flying capacitor voltage is achieved by balancing the inductor current as opposed to sensing the floating

flying capacitor voltage itself, which is difficult. This is possible because the inductor current contains the capacitor voltage information. Also proposed is a simple startup circuit that can quickly charge the flying capacitor to half of the input voltage allowing safe start up of the circuit, ensuring the safety of the low voltage power MOSFETs.

Chapter 3

Gallium Nitride Based Transistors for High Frequency, High Current POL Applications

The introduction of gallium nitride (GaN) transistors offers the potential to move to higher switching frequencies than capable with traditional Si devices while maintaining high efficiency. This chapter will explore the capability of GaN technology for use in high frequency POL converters. This chapter will give an overview of the current GaN technologies, compare the strengths and weaknesses of the currently available technologies, and discuss the fundamentals of utilizing the GaN transistor in high frequency POL converter design; this will address the packaging of the GaN transistor, fundamental operating differences between GaN and Si devices, driving of GaN devices, the impact of dead time on loss in the GaN buck converter, and an analytical loss model for the GaN buck converter will be proposed.

3.1 Emergence of Gallium Nitride Transistors

3.1.1 Introduction of Gallium Nitride Technology

Gallium Nitride transistors have recently emerged as a possible candidate to replace silicon and silicon carbide devices in various power conversion applications from 25V to 600V. Gallium Nitride transistors are high electron mobility transistors (HEMT) and offer potential benefits for high frequency power conversion. Shown in table 3.1 are the material characteristics for Silicon (Si), Silicon Carbide (SiC), and Gallium Nitride (GaN) [55][56]. GaN transistors have a higher band gap, electron mobility, and electron

velocity than Si and SiC devices. These material characteristics make the GaN device capable of superior performance for higher frequency and voltage operation.

	Si	SiC	GaN
Band Gap (eV)	1.1	3.2	3.4
Electron Mobility (cm ² /V-sec)	1450	900	2000
Electron Saturation Velocity (10 ⁶ cm/sec)	10	22	25

Table 3.1: Material characteristics of Si, SiC, and GaN semiconductors

The basic structure of the GaN is a lateral device [57][58]. The majority of GaN transistors are built on a silicon substrate, shown in grey in figure 3.1, to simplify fabrication and reduce cost. On top of the Si substrate lies an aluminum nitride transition layer to isolate the GaN from the Si substrate. On the next layer, shown in green, a thick layer of highly resistive un-doped GaN is grown and used as a base for the GaN transistor. On top of the thick un-doped GaN layer lies a thin layer of highly conductive AlGaN which is shown in black. The combination of the thin AlGaN layer on top of a high quality GaN surface creates a two-dimensional electron gas (2DEG) layer and makes the GaN transistor a high electron mobility transistor. Drain and source contacts are placed on the electron generating 2DEG and a gate is connected on top of the AlGaN.

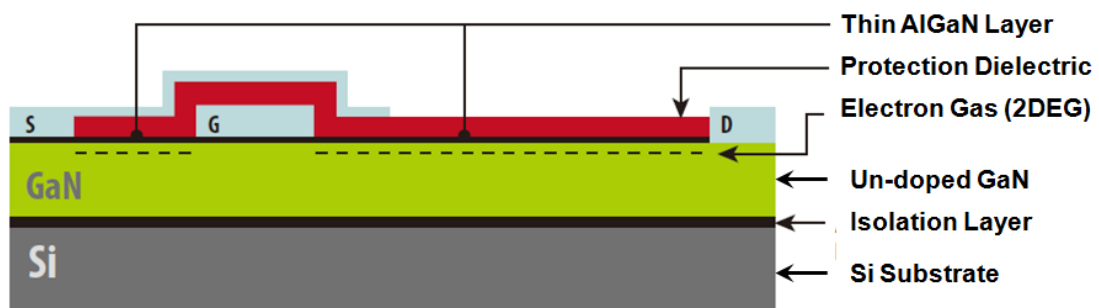


Figure 3.1: Typical GaN lateral power transistor structure

The comparison of currently available GaN and Si devices from 25V to 600V is shown in figure 3.2. From this figure, it can be seen that Si based devices, a mature technology, are closely approaching the theoretical limit regarding specific on resistance for a given breakdown voltage. Due to the significant improvements in Si devices over

the years, a large effort is now required to gain a small improvement in performance. Looking at the GaN theoretical limit for specific on resistance vs breakdown voltage, it can be seen that GaN has the potential to offer significant improvements over traditional Si technology. The first generation of GaN devices have been released by industry and can already outperform the state of the art Si devices by a factor of ten from 30-600V with regard to specific on resistance vs breakdown voltage. Being a new technology, GaN devices will improve rapidly in the first few years, moving towards the GaN limit as the technology matures and providing larger benefits when compared to Si devices.

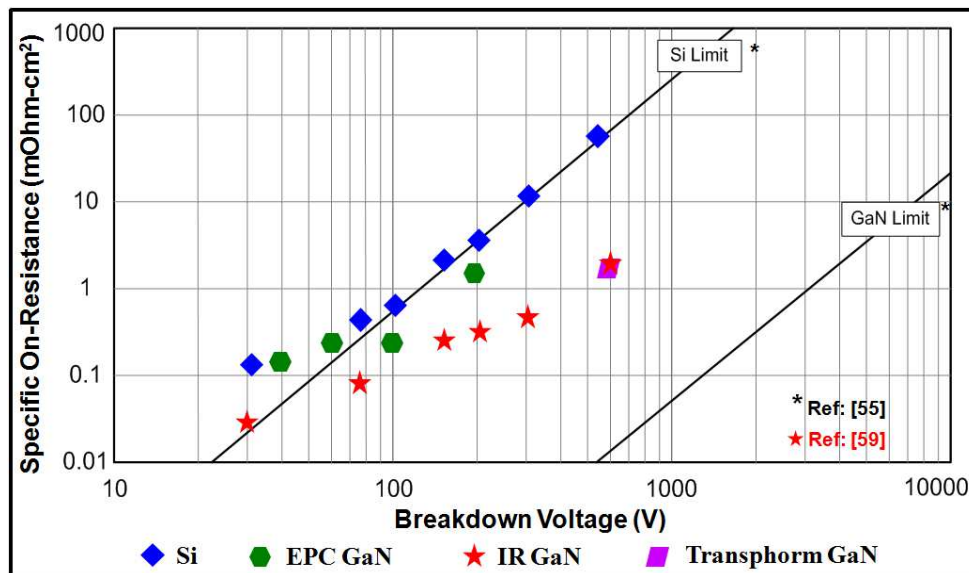


Figure 3.2: Comparison of specific on resistance for Si and GaN

When exploring the use of a device for high frequency, the specific on resistance vs breakdown voltage does not directly correlate to lower loss in an actual converter design. To assess the potential of GaN devices to improve converter efficiency, the FOM from [46] is used to compare the first generations of GaN devices vs the state of the art Si devices from 40V-200V, covering the possible device range for this work. Currently, the devices supported over 200V are in prototype evaluation, and the detailed device parameters are not publicly available. The first commercially available discrete GaN

devices are from Efficient Power Conversion (EPC) [57], the FOM of the first and second generation EPC devices are plotted in figure 3.3 vs the state of the art Si devices. From figure 3.3, it can be seen that the GaN device can offer reduced FOM and project to reduce switching losses over the best current Si based devices. Being a new technology, this figure, showing the significant FOM reduction from the first to second generation, can verify the trend for rapid FOM reduction in the near future for GaN power devices. Combining lower specific on resistance, yielding smaller device size, and smaller FOM, providing lower switching losses, the GaN power device has a potential to significantly increase the frequency and power density of POL modules.

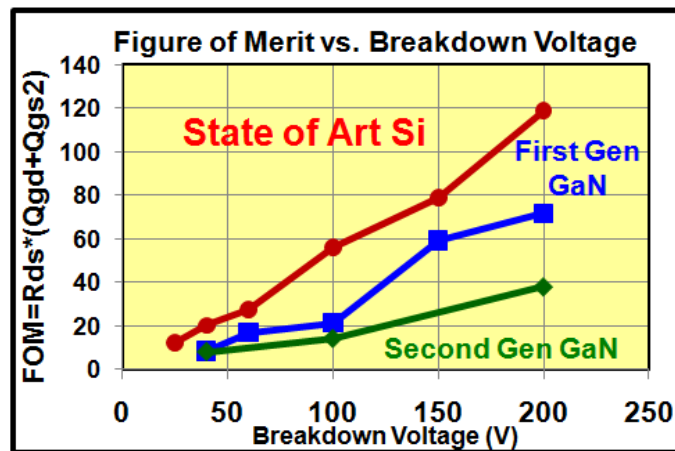


Figure 3.3: FOM vs breakdown voltage for current Si and GaN power devices

3.1.2 Gallium Nitride Transistor Characteristics

Today, there are two different low voltage ($V_{br} < 40V$) GaN devices available on the market. The first is an enhancement mode device from efficient power conversion (EPC) [57] and the second being a depletion mode module from International Rectifier (IRF) [59]. The devices from EPC share many similarities to standard Si MOSFET's as they are normally off enhancement mode components, ranging from 40V-200V, and come as a discrete device as shown in figure 3.4a. The solution from IRF comes as a

complete 30V buck converter module consisting of two GaN devices being built on a single wafer, a control IC for gate driving, and integrated input decoupling caps for high performance. The devices inside the module are normally on depletion mode GaN devices and the driver IC is a standard Si process. Both EPC and IRF GaN devices employ a linear grid array (LGA) pad connection to minimize packaging parasitics, which will be discussed in detail in this chapter.

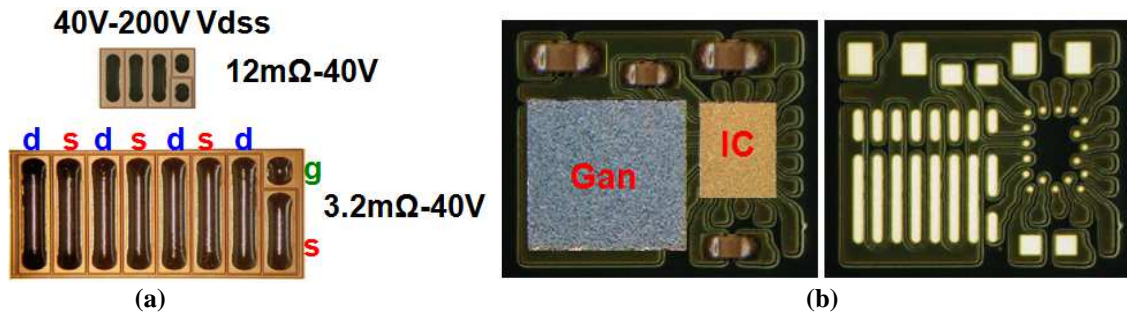


Figure 3.4: (a) Discrete enhancement mode transistors (b) Integrated depletion mode power module

To compare the device characteristics of the current low voltage GaN and Si devices, the 40V EPC2015 [60] is compared to a state of the art 40V Si device with similar on resistance in table 3.2. The GaN device shows a reduction of 60-78% when compared to the Si device for device footprint, gate charge Q_g , miller charge Q_{gd} , and input capacitance C_{iss} making the device attractive for high frequency, high density applications. The GaN reverse recovery, Q_{RR} , is reduced 100% but suffers a 265% increase in source to drain forward voltage, V_{SD} , when compared to the Si device. The large difference is a result of a fundamental difference in the GaN and Si technologies and will be discussed in detail in this chapter. Lastly, the GaN device sees a 70% reduction in drive voltage range, having breakdown limits from -5V to 6V; this is also due to the fundamental difference in the GaN transistor. From this information, it can be seen that a couple fundamental differences between the GaN and Si devices, the body

diode operation and gate drive voltage, must be explored in greater detail to fully identify the potential of GaN devices.

	40V GaN	40V Si	% Reduction
Device Footprint (mm ²)	6.6	30	78
R _{dson} (mΩ)	3.2	3.2	0
Q _g (nC)	10.5	26	60
Q _{gd} (nC)	2.2	6.6	67
C _{iss} (pF)	1100	4030	73
C _{oss} (pF)	575	650	12
Q _{RR} (nC)	0	30	100
V _{SD} (V)	2.2	0.83	-265
V _{gs} (V)	-5 to 6	-20 to 20	70

Table 3.2: Device parameter comparison between 40V GaN and Si enhancement power devices

The enhancement mode GaN IV curve of the EPC2015 [60] is shown in figure 3.5b, the device is designed to be driven on at 5 volts and driven off at zero volts, making the device very similar to the standard Si MOSFET's currently employed. The threshold voltage of the device is 1.4V, also very similar to traditional Si power devices. The enhancement mode GaN device is targeted to replace Si devices in a number of different applications with little change in design required to switch from Si to GaN power devices. The ability of the GaN device to simply replace Si devices in POL modules will be addressed in this chapter.

The depletion mode approach from [59] offers a complete solution with an optimized design for a specific application, a small duty cycle 12V application. The IV curve for a low voltage depletion mode GaN is shown in figure 3.5a, the device is driven on at zero volts and driven off at a voltage of -3.3V with a threshold voltage of -2V; this is very different from the standard enhancement mode device, requiring a specialized gate driver chip that is built into the module. With an internal driver, controller, and input capacitors, this module is designed as a black box solution to provide greater

performance without having to understand or redesign for the use of GaN transistors. An additional reason for the module form for the depletion GaN is the nature of a depletion device. A depletion device is a normally on device, which means the device is turned on in the absence of a negative gate voltage. This property makes the protection of the device much more difficult; the driver circuit must be functioning before the device experiences the input voltage and if there is a drive circuit failure, a short circuit is formed between the input and output, possibly damaging the application.

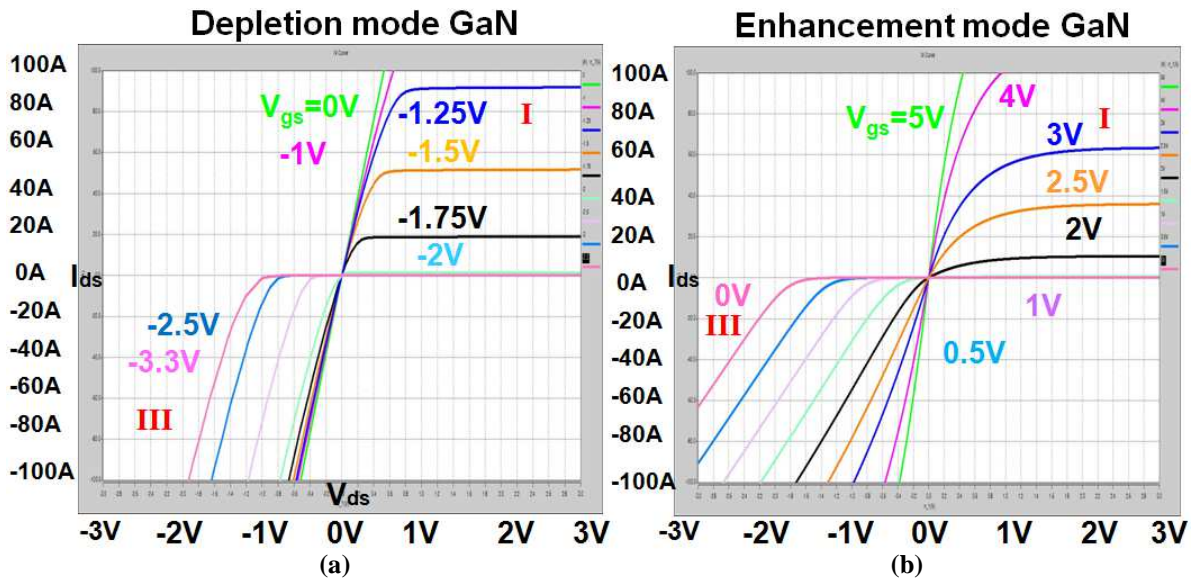


Figure 3.5: IV curve for (a) Depletion mode GaN (b) Enhancement mode GaN

3.2 Driving Gallium Nitride Transistors

3.2.1 Gate Drive Considerations for Gallium Nitride Transistors

From table 3.2, it was noted that the enhancement mode GaN transistor has a property that the device has a failure mechanism if the maximum gate voltage for the device exceeds 6V; this is also true for the depletion mode GaN device. Shown in Figure 3.6 is the resistance vs gate drive voltage for the currently available GaN devices and the standard enhancement mode Si device. The enhancement mode GaN and Si devices

require a gate voltage close to 5V to achieve optimal performance. The enhancement mode GaN device, unlike its silicon counterpart, experiences device failure above 6V. This leaves a very small margin of around 1V for driver overshoot to ensure safe operation. The depletion mode device achieves optimal performance around 0V, giving a 6V overshoot margin, allowing for safer driving than the enhancement mode GaN. For the depletion mode module, the gate signals were tested and shown in figure 3.6b; the module experiences gate overshoot of around 1V, leaving a 5V margin for safety.

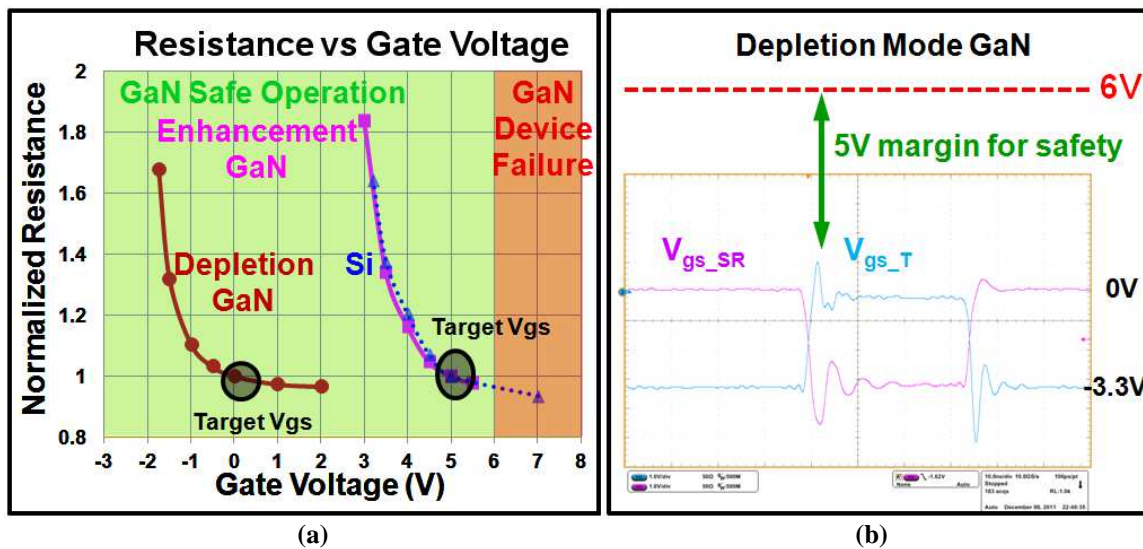


Figure 3.6: (a) Gate drive characteristics of GaN and Si transistors (b) Gate drive signals for depletion mode GaN devices

3.2.2 Over Voltage Issues for Enhancement GaN

To fairly compare the performance of GaN and Si devices and assess the driving challenges of the enhancement mode GaN devices, a hardware design was created using enhancement mode GaN transistors. For the first generation enhancement GaN design, shown in figure 3.7, a Si benchmark buck design was recreated with the Si devices replaced with EPC GaN transistors. This design was targeted for a switching frequency of 1MHz, an input voltage of 12V, an output voltage of 1.2V, and an output current of 20A. The top switch was selected to be the smaller die EPC1014 to provide lower

switching losses; the larger die EPC1015 was chosen for the SR for lower conduction losses. The driver was a so-8 packaged LM27222 single input two output drive structure and the inductor was a 150nH coilcraft SLC1175. For the benchmark buck design, the top switch was the CSD16410 and the SR was CSD16325.

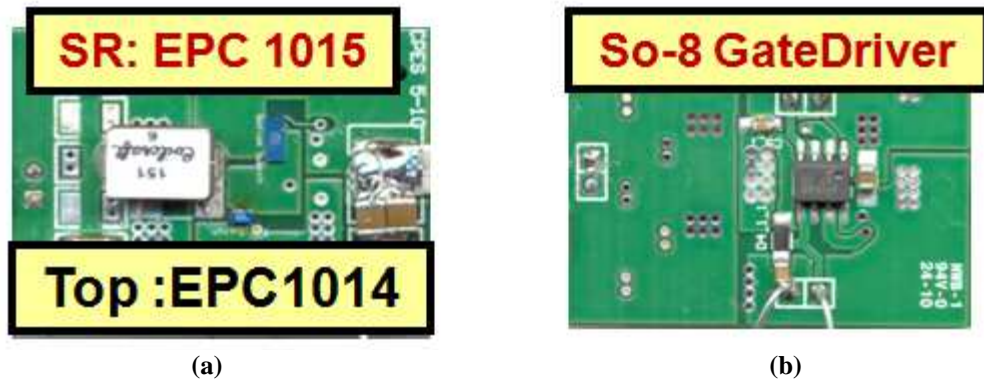


Figure 3.7: Generation 1 enhancement GaN design (a) top view (b) bottom view

The first generation GaN board experienced three issues that will be addressed in this chapter: gate driving over voltage compromising the safety of the devices during turn on, low efficiency when compared to the benchmark Si design, and mounting reliability problems with the GaN LGA package. To fully utilize the benefits of the GaN transistor, these issues must be overcome.

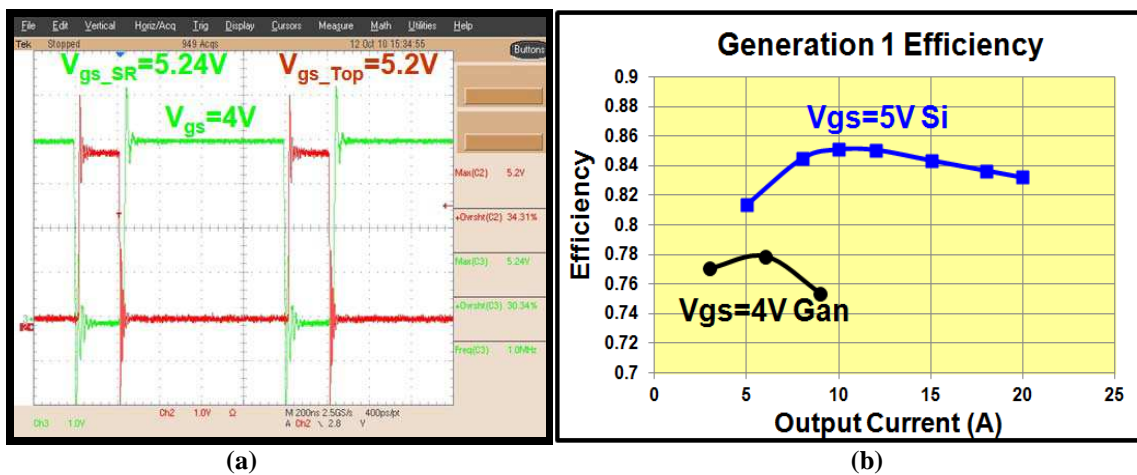


Figure 3.8: (a) Generation 1 GaN Gate Signals at 1MHz (b) Generation 1 GaN efficiency at $V_{in}=12V$, $V_o=1.2V$, $L=150nH$

Due to gate drive over voltage during turn on from gate ringing, shown in figure 3.8a, the design was limited to a 4V gate drive, resulting in non-optimal performance of the GaN devices. The overshoot of the gate drive signal was measured to be 1.24V and operating near a 5V gate drive led to device failure. The efficiency of the first generation design experienced a 10% drop in efficiency when compared to the Si benchmark. From the first generation design, it became apparent that simply replacing Si devices with GaN devices would not demonstrate the benefits of the GaN device. The optimization of the gate drive is critical to utilizing the enhancement mode GaN transistors. To indentify the major loss differences, the on state conduction and off state source to drain forward conduction losses were compared; the top switch conduction can be given by:

$$P_{HS_cond} = D \cdot \left(I_o \sqrt{1 + \frac{(\Delta I_{L_pk_pk})^2}{12 \cdot I_o^2}} \right)^2 \cdot R_{dson_HS} \quad (3.1)$$

Where D ($D=V_o/V_{in}$) is the duty cycle, I_o is the output current, $\Delta I_{L_pk_pk}$ is the peak to peak inductor current ripple, and R_{dson_HS} is the on resistance of the top device.

The conduction for the synchronous rectifier can be given by:

$$P_{HS_cond} = (1-D) \cdot \left(I_o \sqrt{1 + \frac{(\Delta I_{L_pk_pk})^2}{12 \cdot I_o^2}} \right)^2 \cdot R_{dson_SR} \quad (3.2)$$

The off state forward conduction, which occurs during the dead time is given by:

$$P_{BD} = 2 \cdot V_{dead}(I_o) \cdot I_o \cdot t_{dead} \cdot f_s \quad (3.3)$$

Where V_{dead} is the voltage drop across the SR during the dead time, I_o is the output current, t_{dead} is the dead time, and f_s is the switching frequency.

The loss breakdown of the Si and GaN generation 1 converters are compared in figure 3.9. Due to the inability to fully enhance the GaN devices due to overvoltage

concerns, the conduction loss increases significantly and the GaN device incur over twice the conduction loss of the Si devices. The traditional Si gate driver, the LM2722 in this design, has a built in dead time to avoid shoot through. As a result of the increased source to drain voltage of the GaN SR during off state, the loss during this dead time increases to over 0.4W, resulting in an efficiency drop of around 4%.

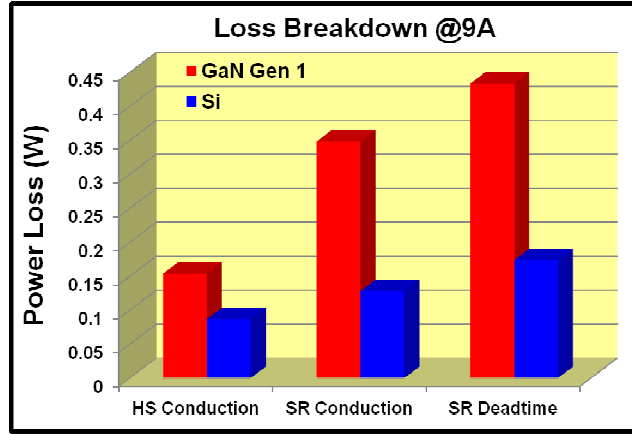


Figure 3.9: Loss breakdown of Generation 1 GaN and Si benchmark at $V_{in}=12V$, $V_o=1.2V$, $I_o=9A$, $L=150nH$

3.2.3 Gate Drive Design to Limit Enhancement GaN Over Voltage

From the first generation design it was learned that the design of a proper gate drive circuit is critical to the performance of enhancement mode GaN devices. The issues that need to be resolved for the gate driver are: gate voltage overshoot and dead time control. The gate voltage ringing is affected by the gate driver turn on resistance, parasitics from package and PCB layout, the GaN transistors gate resistance, and input capacitance. The simplified equivalent circuit for the gate drive is shown in figure 3.10. The gate voltage shape is that of an under damped resonant network formed by the gate drive circuit. The under damped step response can be described by [61]:

$$v_{gs}(t) = 1 + Ke^{-\alpha t} \cdot \cos(\omega_d \cdot t + \phi) \quad (3.4)$$

$$\alpha = \frac{R}{2L} = \xi \cdot \omega_o \quad (3.5)$$

$$\omega_d = \sqrt{\omega_o^2 - \alpha^2} = \omega_o \sqrt{1 - \xi^2} \quad (3.6)$$

$$\omega_o = \frac{1}{\sqrt{L \cdot C}} \quad (3.7)$$

$$K = -\frac{1}{\cos \phi} = -\frac{1}{\sqrt{1 - \xi^2}} \quad (3.8)$$

$$\phi = \tan^{-1}\left(\frac{\alpha}{\omega_d}\right) = \tan^{-1}\left(\frac{\xi}{\sqrt{1 - \xi^2}}\right) \quad (3.9)$$

$$\xi = \frac{R}{2} \sqrt{\frac{C}{L}} \quad (3.10)$$

Using equation 3.4 the overshoot can be solved and given as:

$$Overshoot = \frac{V_{Peak} - V_{Final}}{V_{Final}} = e^{\left(\frac{-\xi \cdot \pi}{\sqrt{1 - \xi^2}}\right)} \quad (3.11)$$

Where $R = R_{on} + R_g$ and $C = C_{iss}$, C_{iss} is equal to the input capacitance of the GaN transistor, R_{on} is equal to the turn on resistance of the gate driver, R_g is equal to the internal gate resistance of the GaN, and L is equal to the total inductance from the drive loop, bootstrap capacitor, and package parasitics of the driver. The inductance value for each generation design was extracted from Maxwell FEA Q3D simulations.

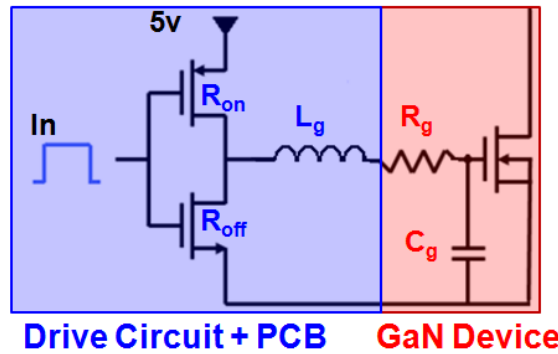


Figure 3.10: Equivalent Circuit for Gate Ringing

To minimize the overshoot of the gate voltage the drive loop inductance can be decreased, the turn on gate resistance can be increased, and/or the input capacitance can

be increased. Increasing resistance will reduce overshoot but slow down the turn on of the device which is not beneficial for high frequency. Increasing capacitance will lead to higher gate losses and slower switching speeds.

The changes for the second generation design were to use a two input, two output driver structure, allowing for control of dead time; and changing the top switch from the smaller die EPC1014, to the larger die EPC1015 to reduce high current conduction loss and driver overshoot. Two different gate drivers were tested in generation 2. With no commercially available two input two output drivers, the first driver was built using two individual ISL89163 gate drivers and a level shift for the top switch. The second driver was a prototype developed with National Semiconductor which has since been released as the first commercial gate driver for GaN, the LM5113 [62].

	Generation 1	Generation 2a	Generation 2b
Top Switch	EPC1014	EPC1015	EPC1015
Driver	1xLM2722	2xISL89163	1xLM5113
R _{on} (Ω)	0.9	1	2
R _{off} (Ω)	0.4	1	0.6
L _{gate} (nH)	11	10	5
R _g (Ω)	0.4	0.4	0.4
C _{iss} (nF)	0.28	1.1	1.1

Table 3.3. Gate Drive Parameters for Generations 1 and 2

Shown in figure 3.11 are the gate drive waveforms for generations 2a and 2b. For generation 2a, the overshoot of the driver was around 1.3V, leading again to device reliability concerns. The large overshoot was a result of using a small turn on resistance and having a large drive loop inductance from the use of two discrete drivers and a level shift. For generation 2b, the driver had a larger turn on resistance of 2ohms and a reduced drive inductance of 5nH, providing sufficient damping. The resulting gate drive is shown in figure 3.11b and it can be seen that by increasing turn on resistance and

decreasing drive inductance the GaN device can be safely driven near the optimal 5V level encountering only a 0.2V overshoot.

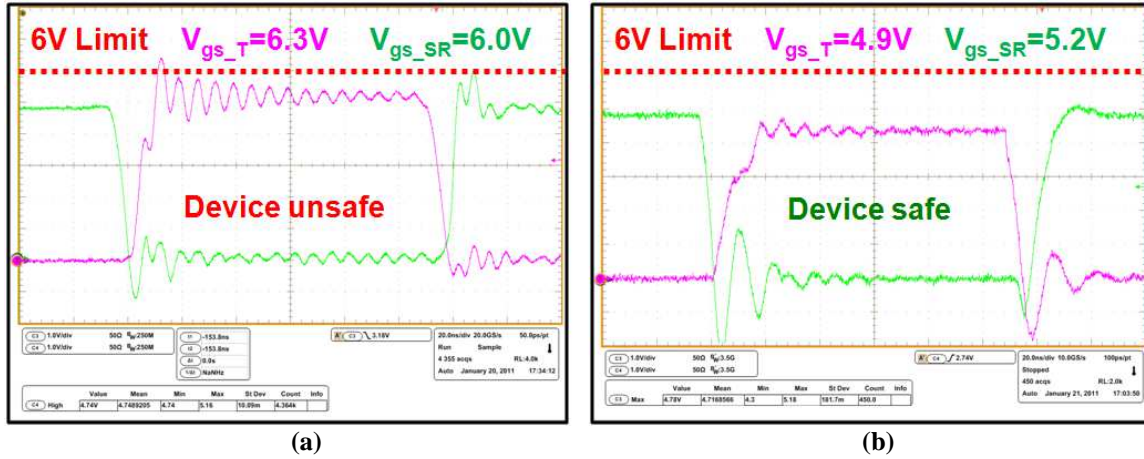


Figure 3.11: Gate waveforms for (a) Generation 2a (b) Generation 2b

To safely drive the enhancement mode GaN device in generation 2b, a larger turn on resistance was employed to increase damping and reduce voltage overshoot. The impact of increasing turn on resistance is a reduction in available driving current, resulting in slower turn on, the driving current can be given by:

$$I_{DR} = \frac{V_{DR}}{R_{DR} + R_g} \quad (3.12)$$

Where I_{DR} is the available driver current, V_{dr} is the effective driver voltage, R_{DR} is the driver resistance, and R_g is the GaN's internal gate resistance.

	Generation 2a	Generation 2b
Turn On Rise Time	10nS	16nS
Turn Off Fall Time	10nS	6nS

Table 3.4. Turn on and turn off times for Generation 2 designs

The approach of slowing down the switching turn on to limit overshoot can be utilized without sacrificing converter efficiency. In a buck converter the majority of the

loss is a result of turn off loss [37]. For improved performance, a gate drive can be designed with a larger turn on resistance to achieve low overshoot and a lower turn off resistance to achieve high efficiency.

Generation 2b employs this concept by having a 2ohm turn on resistance to limit gate overshoot and a 0.6ohm turn off resistance to reduce switching loss. The turn on and turn off times for the generation 2 designs are given in table 3.4, with turn on time being 10nS longer than turn off time for generation 2b. The impact of drive resistance selection on power loss and efficiency is illustrated in figures 3.12 a&b. The second generation GaN design improved efficiency over the discrete Si solution by 3% at 10A and 0.8% at 20A. The dead time was minimized for the GaN device in this design to focus on the driver overshoot issue.

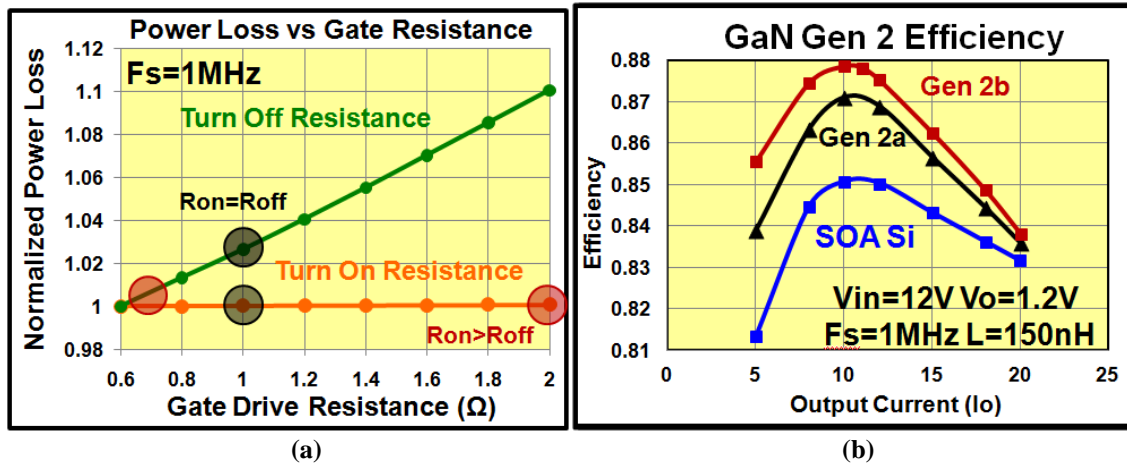


Figure 3.12: (a) Gate drive resistance vs power loss (b) Efficiency for generation 2 designs

3.2.4 Dead time optimization of Synchronous Rectifier

The GaN transistor shares many similar switching characteristics to the traditional Si MOSFET but also has a few key major differences in operation. One major difference from the traditional Si MOSFET is that the GaN transistor does not have a built in body diode, resulting in a different mechanism to conduct current in the SR during off time.

For Si devices in the third quadrant when the device is off the body diode conducts the reverse current. The circuit diagram for a Si MOSFET is shown in figure 3.13a, in SR mode the current flows from source to drain. When the device turns off the current first charges the output capacitor of the device at a rate of:

$$\frac{dv_{ds}}{dt} = \frac{-I_o}{C_{ds}} \quad (3.13)$$

When the output capacitor is charged to the voltage of the internal body diode, V_{df} , the body diode turns on and conducts the load current. The IV curve for a Si MOSFET is shown in figure 3.14a; the diode voltage drop is slightly dependent on load current. The voltage drop increases from 0.65V at no load to 0.82V at 20A.

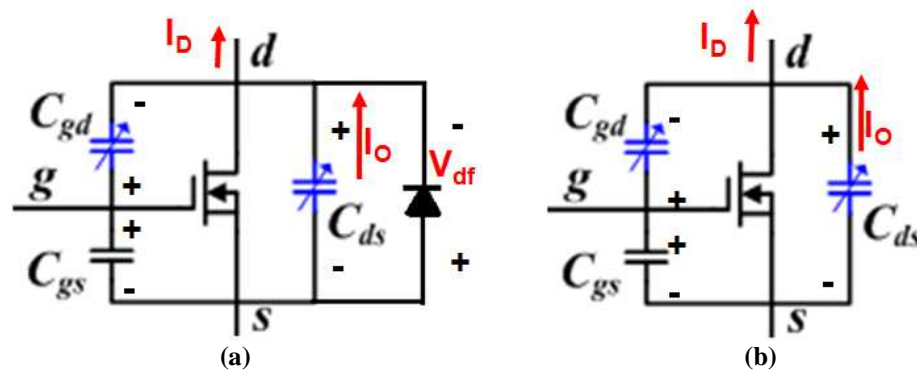


Figure 3.13: Device electrical model for (a) Si Trench MOSFET (b) GaN Transistor

The operation of the GaN in the third quadrant, when the device is off, is very different; the GaN has no built in body diode and has the ability to be driven bi-directionally with either a positive V_{gs} or V_{gd} . The electrical diagram of the GaN transistor is shown in figure 3.13b. During the third quadrant operation the reverse current will first flow from source to drain through the output capacitor as in equation 3.7, building up a voltage across the output capacitor. The voltage from gate to drain is given by:

$$V_{gd} = V_{gs} - V_{ds} \quad (3.14)$$

The drain to source capacitance voltage increases and the device turns on when:

$$V_{gd} = V_{th} \quad (3.15)$$

At this point the device weakly turns on and the IV curve for the third quadrant is shown in figure 3.14b. When compared to the Si MOSFET with the built in body diode, a large voltage drop equal to the threshold voltage is seen at no load (1.4V) and a larger increase in loss is encountered at higher loads with a voltage drop of 2.2V being seen at 20A. The loss of the GaN during dead time is around 2.5 times larger than the Si MOSFET.

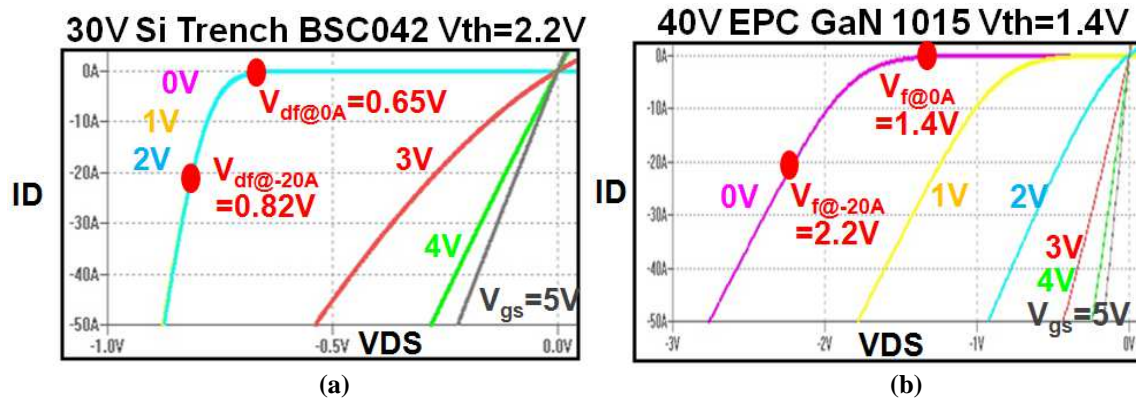


Figure 3.14: Third quadrant I-V curve for (a) Si Trench MOSFET (b) GaN Transistor

One benefit of the GaN during this third quadrant period is that the mechanism for reverse conduction contains no minority carriers eliminating the reverse recovery charge [57]. The internal Si body diode is a minority carrier which has a reverse recovery charge (Q_{rr}) that impacts high frequency performance as was seen in chapter 2. For the depletion mode GaN, the operation in the third quadrant is similar with the GaN seeing a voltage drop two to three times higher than the traditional Si MOSFET body diode.

The dead time in a buck converter, shown in figure 3.15, is defined as the time when both the top and SR devices are turned off. Dead time is used in the synchronous

buck converter to avoid simultaneous device conduction resulting in shoot through that can decrease efficiency significantly or damage the devices. During the dead time, the current freewheels through the SR's body diode. The loss is given by equation 3.3.

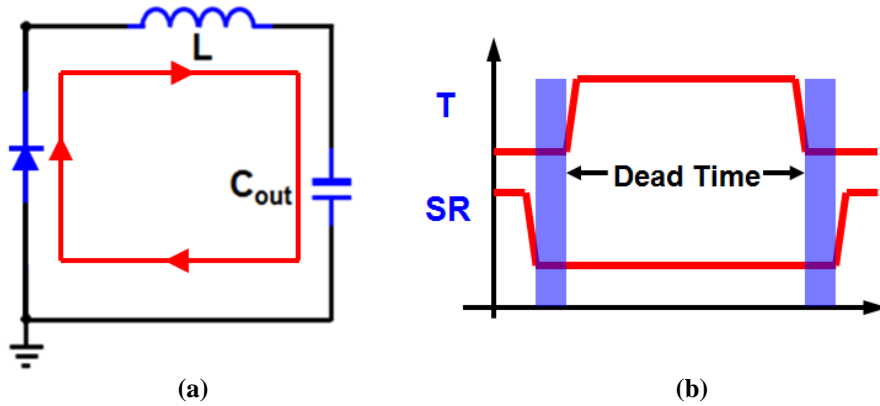


Figure 3.15: (a) Equivalent circuit for buck converter operating during dead time (b) Timing diagram of buck converter with built in dead time

For the GaN converter, the SR has no body diode, but due to its bidirectional driving capability has a mechanism to conduct current during dead time. The EPC1015 GaN SR source to drain voltage drop is given as:

$$V_{dead}(I_o) = 6.859 \cdot 10^{-5} \cdot I_o^3 - 4.060 \cdot 10^{-3} \cdot I_o^2 + 0.094 \cdot I_o + 1.401 \quad (3.16)$$

With the GaN device having around a 2.5x larger loss during the dead time period than the Si MOSFET with a built in body diode, the impact of dead time on the circuit performance must be quantified. The drive circuits in traditional Si buck converters employ a single input dual output structure with a built in dead time. The dead time is controlled by the driver chip and typical values of dead time are between 10-20nS.

For the GaN converter to be efficient, the control of dead time becomes critical to high efficiency. For the second generation drive scheme, a two input two output structure was chosen to allow for control of the dead time in the circuit. The effect of dead time on efficiency is compared using the driving schemes shown in figure 3.16a. In the first case

the gate signals overlap just below the threshold voltage resulting in almost no dead time conduction, the second case has a small 8ns dead time between the gate signals to provide a safety margin to avoid shoot through. Figure 3.16b shows the efficiency for the two cases, an efficiency drop of around 3% is encountered at full load without overlapping.

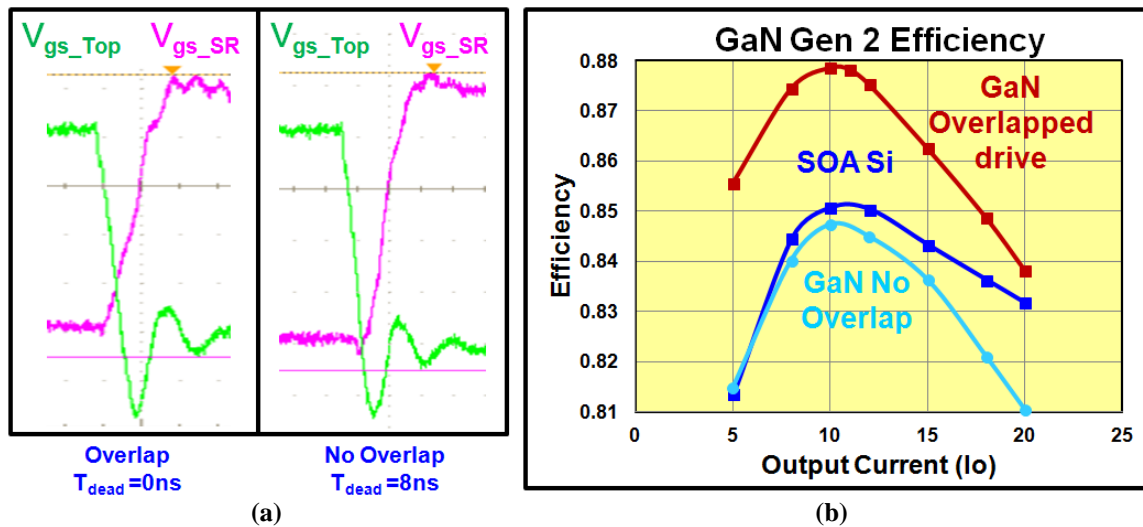


Figure 3.16: (a) Gate drive signals for dead time efficiency comparison (b) Impact of different gating signals on efficiency ($V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, $L=150nH$)

From 3.16b it can be seen that the GaN is very sensitive to dead time conduction. Controlling the gate timing to eliminate the dead time is very difficult and not preferred in practical design because of the possibility of shoot through if mismatch occurs, as shown in figure 3.17b. In shoot through operation, the short circuit current is controlled by the device saturation mode as a voltage controlled current source. In shoot through, the loss increases rapidly based on timing mismatch and will lead to low efficiency and possibly device failure.

To achieve a tradeoff of high efficiency and design safety it is proposed to place a low parasitic low voltage schottky diode in parallel to the synchronous rectifier (SR). The result will be a reduction in the dead time loss while allowing a timing mismatch safety margin to avoid shoot through conditions. The result, shown in figure 3.17a, is a

small efficiency drop over the overlapped case with no dead time and a 2.5% full load improvement over 8nS dead time case without a schottky diode.

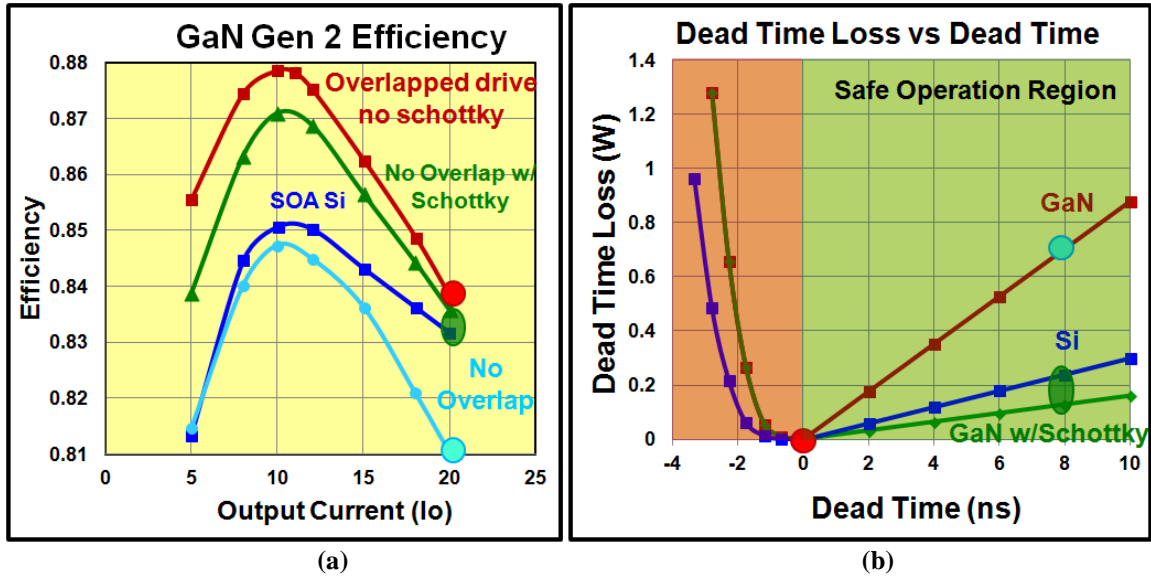


Figure 3.17: (a) Impact of different gating signals on efficiency ($V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, $L=150nH$) (b) Dead time loss vs dead time for 1MHz designs

To utilize a schottky diode in the GaN buck converter, a low parasitic inductance must be seen from the path of the SR to the diode. The parasitic inductance, L_{diode} , limits the current flow between the high loss SR to the low loss diode, the rate is given by:

$$\frac{di_{diode}}{dt} = \frac{V_{SD} - V_{DF}}{L_{diode}} \quad (3.17)$$

Where V_{sd} is the source to drain voltage of the GaN SR, V_{DF} if the forward voltage of the schottky diode, and L_{diode} is the sum of inductances of the GaN package, diode package, and the layout from the diode to the SR.

The schottky diode used in the generation 2 design was the MSS1P3L, a 30V, 1A diode in a low parasitic microSMP package. This package uses no wire bonding and mounts the cathode directly to the pad and uses a low parasitic copper strap to connect the anode to the package. The package inductance of the microSMP diode package was found to be 0.12nH. Combining low package parasitics of the GaN device and the

schottky diode, the result is similar to Si SR devices with built in schottky diode [63]; providing an effective solution to build in a small dead time to improve safety without sacrificing performance.

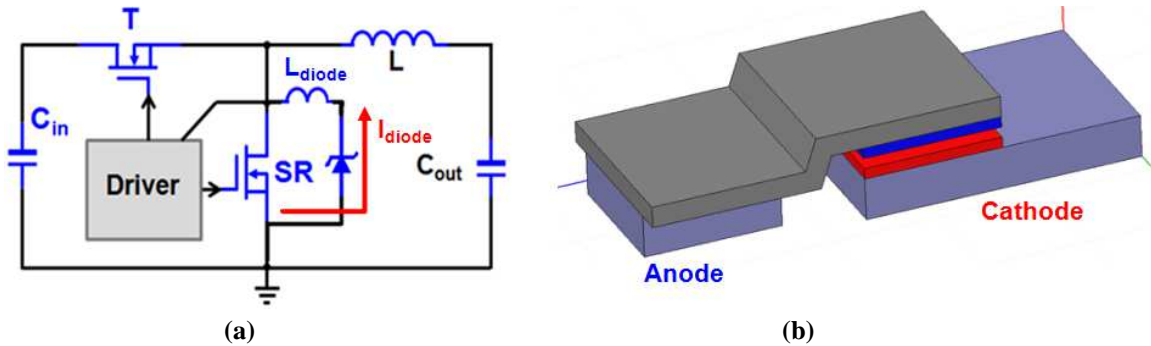


Figure 3.18: (a) Buck converter schematic with external schottky diode (b) Maxwell Q3D model of microSMP package

3.3 Packaging Analysis of High Frequency GaN Devices

3.3.1 Analytical Loss Model for Gallium Nitride Devices with Package Parasitics

In this section, the development of a GaN loss model to quantify the impact of the package and layout parasitics on performance and assess the benefits of the GaN LGA package at higher frequencies is discussed. The GaN device shares many similar switching characteristics with Si devices and there have been many different analytical loss models derived for Si buck converters in [37][64]-[66].

The Si based model from [37] is used to develop the GaN loss model in this work. The Si model was developed from a physics based semiconductor model to accurately estimate the switching loss in a converter by breaking down the switching waveform into the different operating modes of the device. Inside the different modes, equivalent circuits were created to represent the circuits operating conditions, the effects of the non-linear capacitances were considered, and the parasitic inductances impact on switching

were included. The total loss is found in a piecewise linear method by summing together the losses in each of these switching intervals. This analytical loss model is discussed in greater detail in appendix A.

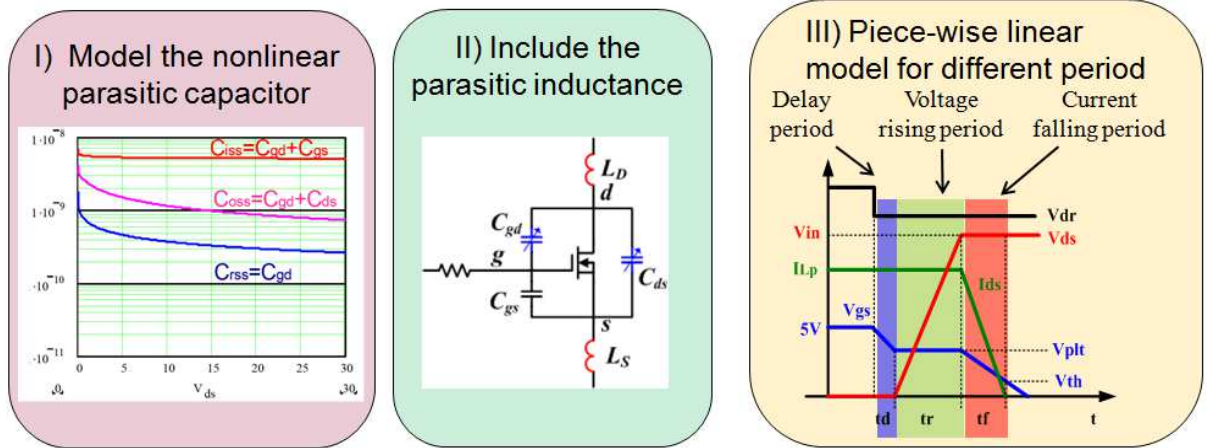


Figure 3.19: Accurate loss model process chart

To utilize this model and estimate the loss of the GaN transistor in high density GaN power designs some modifications were required. The non-linear capacitance of the GaN transistor has a different shape than the traditional MOSFET. To accurately model the increased non-linearity of the GaN capacitance, in particular the output capacitance, C_{ds} , more advanced curve fitting was used. C_{ds} is represented by a third order polynomial equation curve, the relationship for the EPC1015 GaN is:

$$C_{ds}(V_{ds}) = 5.244 \cdot 10^{-5} \cdot V_{ds}^3 - 2.220 \cdot 10^{-3} \cdot V_{ds}^2 + 1.244 \cdot 10^{-3} \cdot V_{ds} + 0.977 \quad (3.18)$$

The GaN gate to source capacitor, C_{gs} , can still be accurately estimated by a constant value. The gate to drain capacitor, C_{gd} , is represented by a second order polynomial. The relationship for C_{gd} is:

$$C_{gd}(V_{ds}) = 2.881 \cdot 10^{-4} \cdot V_{ds}^2 - 0.014 \cdot V_{ds} + 0.220 \quad (3.19)$$

Increasing the number of data points used to model the capacitances is necessary to model the greater non-linearity of the GaN capacitances. The capacitance equations are

derived from an increased number of data points, ranging 0V to 30V in 5V steps. Figure 3.20 shows the nonlinear capacitors curves from the EPC1015 datasheet and the curves obtained from the model.

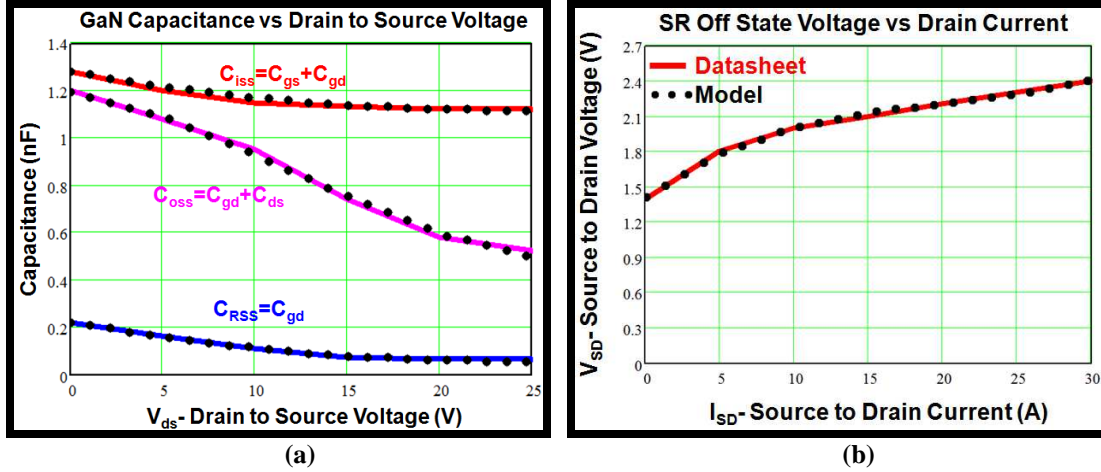


Figure 3.20: (a) Nonlinear capacitance comparison between the data from datasheet (solid lines) and data obtained from GaN model (dotted lines) (b) Reverse drain source characteristics from datasheet (solid lines) and data obtained from GaN model (dotted lines)

The dead time voltage of the GaN transistor was shown to have a large impact on loss earlier in the chapter. To accurately model the loss during the dead time; the source to drain off state voltage drop was modeled using a third order describing function given by equation 3.16, the dead time loss can be found by inserting 3.16 in equation 3.3:

$$P_{dead}(I_o) = 2 \cdot (6.859 \cdot 10^{-5} \cdot I_o^3 - 4.060 \cdot 10^{-3} \cdot I_o^2 + 0.094 \cdot I_o + 1.401) \cdot t_{dead} \cdot f_s \cdot I_o \quad (3.20)$$

The comparison of the loss model and data sheet values for off state source to drain voltage is shown in figure 3.20b. With improved modeling of the capacitances and dead time loss, the GaN loss model's accuracy can be improved.

3.3.2 Parasitic Inductance and Resistance Modeling

To accurately model the loss in a high frequency, high density module, the modeling of the parasitics is critical to accuracy. With low loss GaN devices, a greater majority of the loss is a result of the trace inductances and resistances of the PCB design.

The circuit layouts and devices were simulated using FEA analysis to accurately model the layout and device parasitics. Figure 3.21a shows the model based of the hardware designs for the generation 2 GaN design. Figure 3.21d shows the parasitics extracted to improve model accuracy for gen 2; the parasitics for all designs are in appendix A.

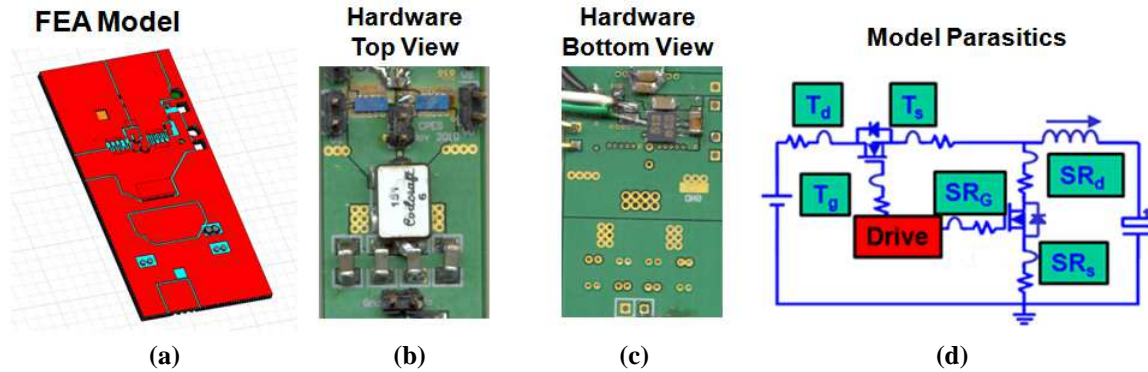


Figure 3.21: Generation 2 (a) FEA model (b) Hardware top view (c) hardware bottom view (d) circuit model with parasitics

	T_g	T_d	T_s	SR_g	SR_d	SR_s
L(nH)	6.24	0.57	0.16	4.60	1.37	0.77
R(m Ω)	10.9	0.40	0.20	8.87	0.87	0.59

Table 3.5. Parasitic inductances and resistances for generation 2 GaN design

3.3.3 Model Verification

To verify the accuracy of the analytical loss model, the efficiency and loss breakdown were compared to the simulation model and experimental hardware. The device spice models were supplied by the device manufacturer and the parasitics were derived from FEA analysis. Shown in figure 3.22 is the total loss for the experimental hardware, analytical model, and SABER simulation model. The losses match very closely after accurate parasitic extraction and GaN modeling.

By having an accurate loss model for the GaN based converter a detailed loss breakdown can be performed to identify the major sources of loss in the circuit and the

critical circuit parasitics giving insight into how to improve the design of a high frequency POL module.

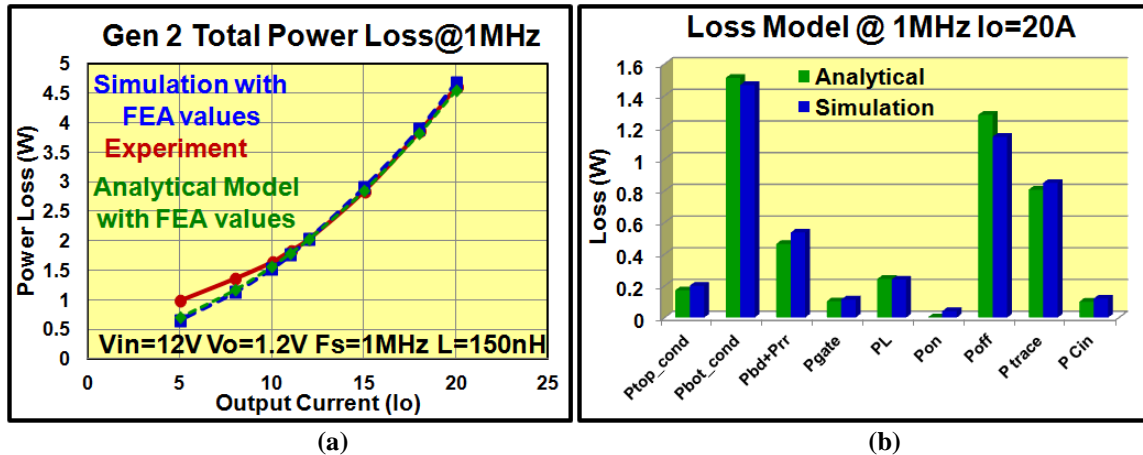


Figure 3.22. Generation 2 GaN design with $V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, Top switch:EPC1015, SR:EPC1015 (a) Loss comparison of simulation, experiment, and analytical model (b) loss breakdown comparison of analytical and simulated model

3.3.4 Evaluation of Device Package Parasitic Influence on Switching Loss

The GaN transistor package is very different than traditional Si devices due to the lateral nature of the device; it is mounted as a bare die with metalized bumps underneath in a linear grid array (LGA) with interleaving drain and source pads to minimize parasitics. The interleaved LGA structure shown in figure 3.23a will be compared to the traditional trench package structures in this section.

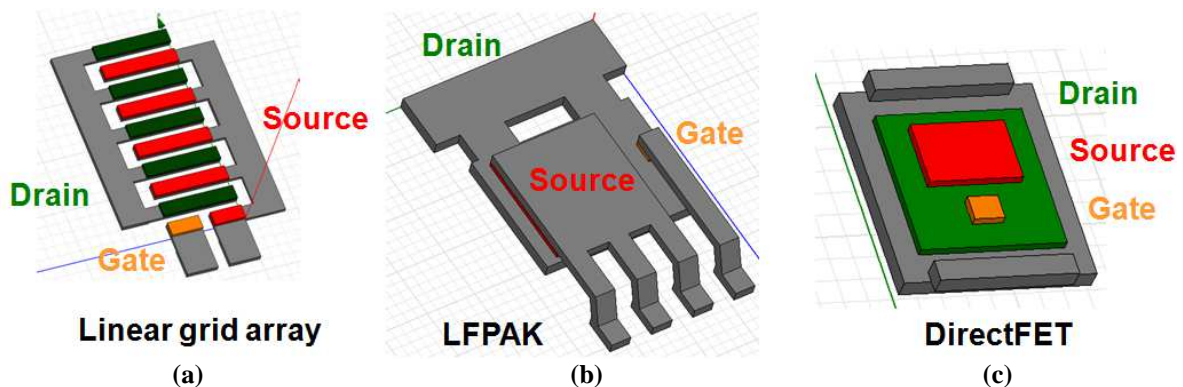


Figure 3.23: FEA package models for (a) Linear Grid Array (b) LFPACK (c) Si DirectFET

Shown in figures 3.23b&c are the loss free (LFPACK) and DirectFET packages; which are the most common discrete packages for low voltage Si devices. The LFPACK

orients the drain side of the die towards the PCB substrate and the drain pad is connected to a large tab that mounts to the PCB directly, minimizing drain parasitics and allowing for good heat transfer from the device to the PCB. The gate and source pads are connected to the board by external leads, introducing large parasitics to the source and gate of the device. The parasitic comparison between the packages was done using Maxwell 3D FEA simulations and the results are shown in table 3.6.

	Lg(nH)	Ld(nH)	Ls(nH)	Rg(mΩ)	Rd(mΩ)	Rs(mΩ)
So-8	2.06	0.48	0.83	9.44	0.13	0.96
LFPAK	1.64	0.10	0.54	0.73	0.10	0.14
DirectFET	0.09	0.44	0.09	0.22	0.39	0.23
GaN LGA	0.07	0.07	0.08	0.12	0.09	0.10

Table 3.6: Package inductances and resistances at 1MHz

The DirectFet orients the source and gate pads towards the pcb substrate, allowing for the mounting of the gate and source pads directly to the board, reducing gate and source parasitics. The drain of the device is connected to the board by the external can package, resulting in large parasitics for the drain connection. The drain can package is metalized to provide improved thermal performance [67]. For the synchronous buck converter, the common source inductance has the largest impact on the converter switching loss. The DirectFET offers minimal source parasitics, resulting in higher efficiency [68].

The lateral structure of the GaN device allows for a single sided LGA package with no external leads, as required for the two sided trench device. The LGA GaN structure mounts all of the pads directly to the PCB and interleaves the drain and source connections to further decrease parasitics. From table 3.6 it can be seen that the GaN offers low parasitics for the drain, source, and gate connection.

Using the loss model developed in this chapter, the impact of the package on performance is shown in figure 3.24a for the so-8, LFPAK, DirectFET, and LGA packages at 1MHz. The total switching loss is broken down into the switching loss contribution from the die and the contribution of the package. For the So-8 and LFPAK packages, the package is responsible for 82% and 73% of the total switching loss respectively due to the large source inductance. The DirectFET package offers the best performance for the trench packages, where 47% of the loss results from the package; with the improvement coming from the reduced source inductance. The GaN LGA package, having low parasitics for all device connections, reduces the package loss to only 18% of the total switching loss.

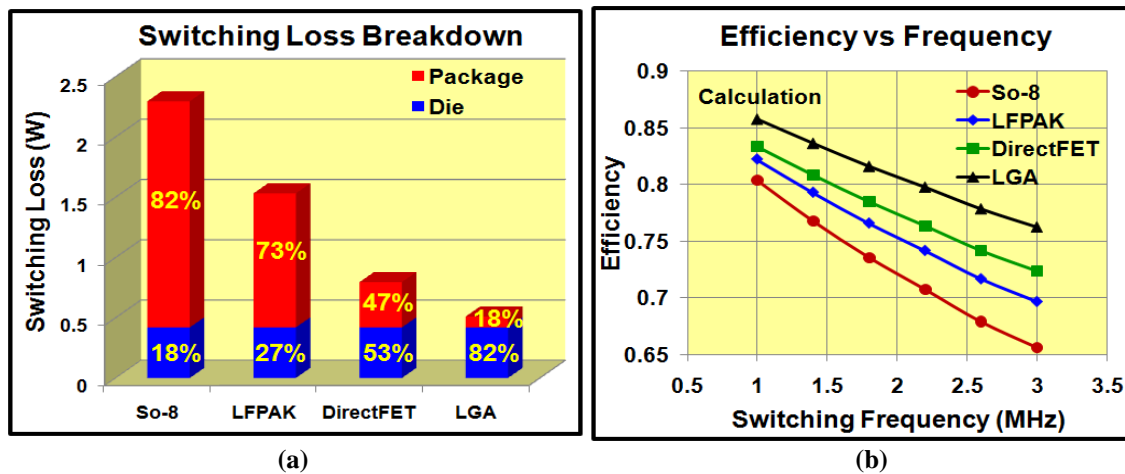


Figure 3.24: (a) Loss breakdown for different packages ($F_s=1\text{MHz}$, $V_{in}=12\text{V}$, $V_o=1.2\text{V}$, $I_o=20\text{A}$, $L=150\text{nH}$) (b) Package impact on efficiency for various frequencies ($F_s=1\text{MHz}$, $V_{in}=12\text{V}$, $V_o=1.2\text{V}$, $I_o=20\text{A}$, $\Delta I_L=40\%I_o$)

At higher frequencies, the reduction of switching loss is critical to high converter efficiency. The benefits of the GaN's reduced FOM combined with the low parasitic LGA package provide a device suitable to target higher frequency operation. Figure 3.24b explores the impact of the package parasitics on efficiency at higher switching

frequencies. At 3MHz, a 4% efficiency improvement is projected over the best packaged trench device.

With reduced loss resulting from the improved package of the device; the impact of the layout parasitics on performance is critical. For the benchmark discrete buck and GaN generation 2 designs the switching loss components for the PCB layout, package, and device are compared. Figure 3.25b shows that for a design with low packaging parasitics, the impact of PCB layout dominates the overall switching loss. This provides an opportunity to further improve performance through improved layout and the optimization of the power loop design will be explored in chapter 4 for a 3D module.

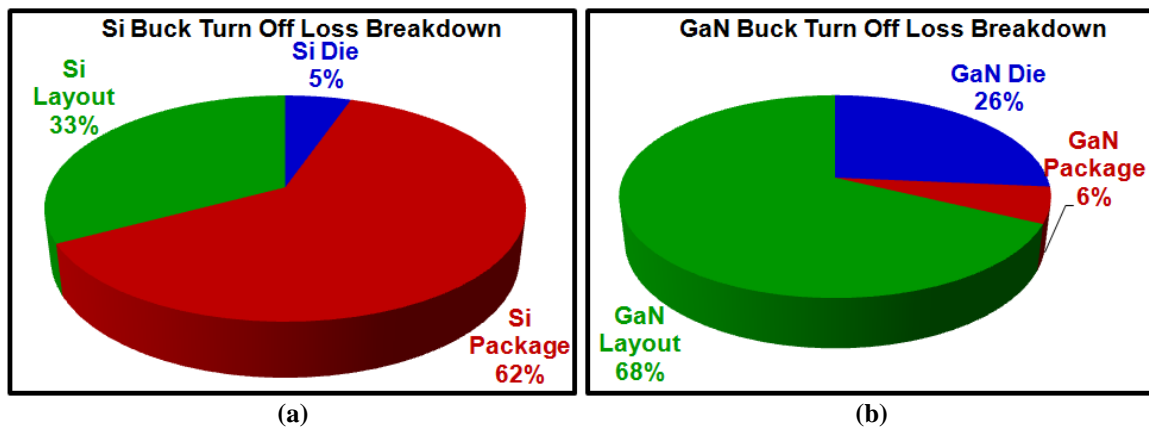


Figure 3.25: Turn off loss breakdown of PCB layout, die, and package of (a) Si benchmark using LFPACK devices (b) GaN generation 2 design

3.3.5 Mounting of GaN LGA Package

The GaN's reduced die size and interleaved LGA package provides performance benefits but introduces mounting challenges. The discrete Si devices have only three connections that need to avoid being shorted. These pads have over a 34mil separation distance and large surface area to ensure good solder connection. The GaN LGA package utilizes the interleaved structure, the separation distance of the pads measures 5.9mil and requires 11 small pads to avoid shorting and achieve good solder connection. This section will discuss the process of reliably mounting the GaN LGA device.

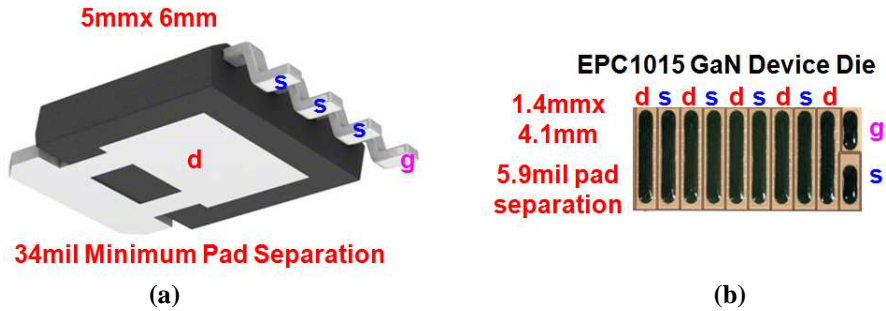


Figure 3.26: Mounting pads for (a) 5x6mm LFPAK (b) 1.4x4.1mm GaN LGA

The standard procedure for mounting devices onto a PCB board is to first supply solder paste to the board with a solder stencil outlining the pads and then placing the devices onto the board. The PCB board is then heated and the solder paste reflows, mounting the devices to the PCB board.

For the GaN device, the manufacturers recommend a similar process to make the GaN compatible with the standard reflow process [69]. The given solder paste profile is shown in figure 3.27; the GaN die comes with a 75um solder bump from the manufacturer. The combination of small pad separation distance, the die solder bump, and additional stencil solder results in frequent shorting between the pads causing the device to fail. The unreliability of the stencil method was verified internally and by external vendors.

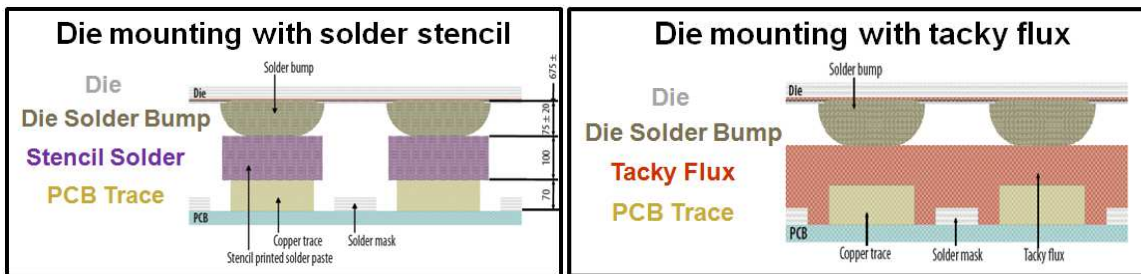


Figure 3.27: Cross-sectional view of a die placed on a PCB with (a) stencil-printed solder paste (b) Kester TSF6502 tacky flux

Since the GaN dies come with a small solder bump already attached the stencil solder layer was removed. To hold the devices mechanically in place a thin layer of

Kester Tacky Flux TSF6502 was used and the process is shown in figure 3.26b.

Mounting the GaN devices using the tacky flux resolved the major issue of device shorting. Using the tacky flux method, two issues presented themselves: device tilting and solder voiding. Because of the small physical size of the device and the pad surface area, the removal of residual flux during the reflow process is critical. An x-ray image of the mounted EPC1015 devices is shown in figure 3.28 and solder voiding was observed.

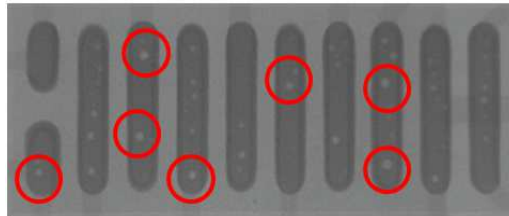


Figure 3.28: X-Ray of GaN device with solder voiding

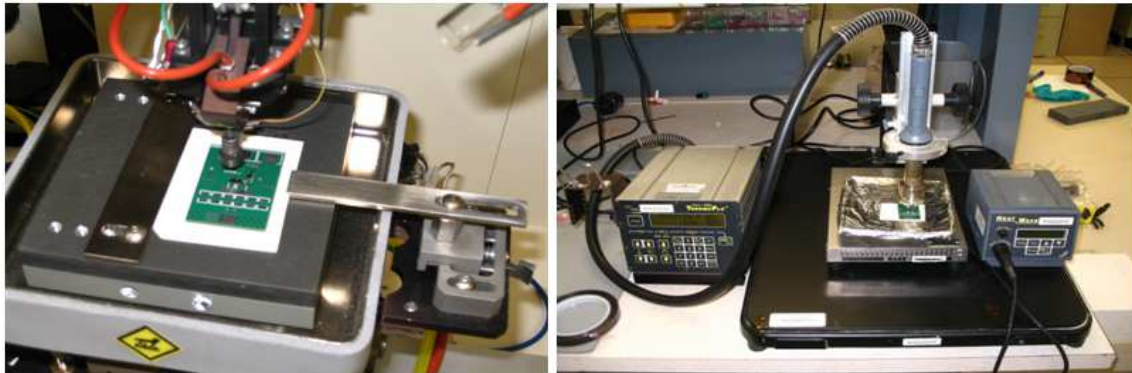


Figure 3.29: (a) Pick and place machine setup (b) Solder reflow station with 90° heat source

To ensure that the device could be mounted reliably: avoiding device tilting and solder voiding a different set up was developed to mount the GaN devices. A small amount of tacky flux was placed on the GaN pad; using an excess amount of flux will lead to part tilting and voiding. The pick and place machine, pictured in figure 3.29, was used to accurately place the device on the PCB board to avoid misalignment, when the device is placed on the board, the tacky flux will be leveled to a uniform height.

The final step in the device mounting procedure is to take the PCB board to the solder reflow station. The solder reflow station uses a heat gun with a perpendicular air flow and a bottom pre-heat source of 100° to ensure complete tacky flux burn off and that the device will remain level throughout the reflow process.

To determine the proper reflow profile, the device temperatures were measured using a thermocouple attached to the GaN devices with thermal grease. Figure 3.29a shows the final reflow profile and the measured device temperature.

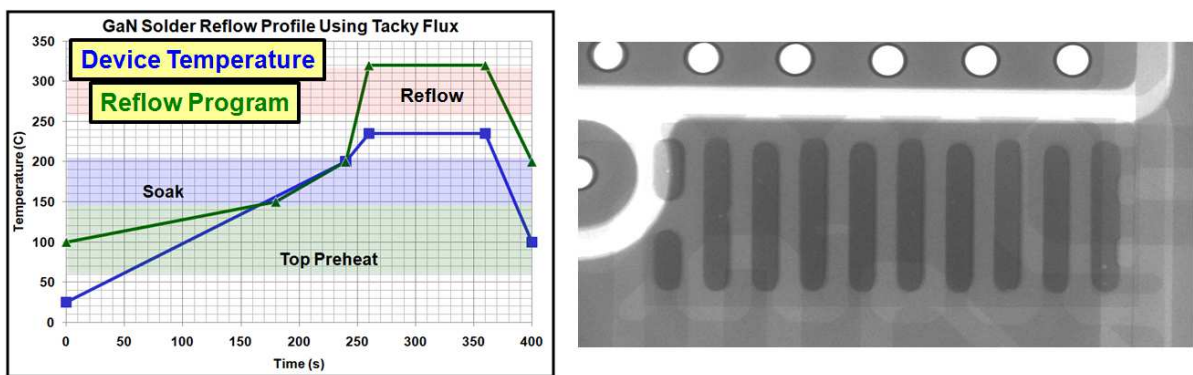


Figure 3.30: (a) Solder reflow profile for EPC GaN devices (b) X-Ray of GaN device with modified mounting procedure without solder voiding

There was a large difference between the programmed and measured reflow temperature and this value had to be modified to mount the devices properly. With the modified mounting procedure, reliable GaN device mounting without part tilting or solder voiding can be achieved. An x-ray of an EPC1015 using this procedure is shown in figure 3.30b.

3.4 Conclusions

The emerging gallium nitride device technology offers the potential to achieve higher frequency leading to higher levels of integration. First generation GaN technology already can provide improvements in switching FOM over the current state of the art Si

devices. As the GaN fabrication process matures and more companies begin entering the market, GaN device performance is projected to improve rapidly, with an order of magnitude improvement being projected in as little as five years.

To fully utilize the potential benefits of the GaN transistor, the fundamentals of the devices must be well understood. This chapter assessed the current depletion and enhancement mode GaN devices available today and compared their performance to Si devices. For enhancement mode GaN devices, the driving issues: gate over voltage, and increased dead time loss were discussed and solutions were proposed to provide high efficiency with limited gate ringing and conventional dead times. A GaN loss model was developed to quantify the losses in a high frequency GaN converter, assess the influence of package parasitics, and predict performance at higher frequencies. Lastly, the procedure to reliably mount the GaN LGA package with void less pad connections was discussed.

Chapter 4

Optimization of High Density 3D Non-Isolated Point of Load Module

4.1 Introduction

The demand for future power supplies to achieve higher output currents, smaller size, and higher efficiency cannot be achieved with conventional technologies. There are limitations in the packaging parasitics, thermal management, and layout parasitics that must be addressed to push for higher frequencies and improved power density. To address these limitations, the use of integrated 3D point of load converters utilizing GaN transistors, low profile magnetic substrates, and ceramic substrates with high thermal conductivity will be considered in this chapter.

The previous chapter addressed the fundamentals of using GaN transistors: Gate drive design for enhancement mode devices to limit over shoot while maintaining high efficiency, the use of a schottky diode to reduce dead time loss, and the impact of GaN packaging on high frequency performance.

This chapter will discuss the effect of layout parasitics on the performance of the high frequency GaN POL, methods to improve the circuit layout of a highly integrated 3D integrated POL module, the integration of a low profile LTCC inductor substrate, and the thermal design of a high density module using advanced substrates with improved thermal conductivity. The final objective of this work is to demonstrate a highly

integrated, high density $V_{in}=12V$, $I_o=20A$, 3D module approaching $1000W/in^3$, over three times the best state of the art design.

4.2 Evaluating Impact of Parasitics on Loss in GaN Synchronous Buck

The loss model in appendix A is used to evaluate the impact of parasitics on switching loss for the high frequency GaN module. Previous work has shown that reducing layout parasitics can improve high frequency performance [70],[71] when the device package parasitics are small. Shown in figure 4.1a is a synchronous buck circuit diagram illustrating the two major parasitic loops. The common source inductance, L_s , is the inductance shared by the drain to source current path and gate driver loop. The high frequency power loop, L_{Loop} , is the parasitic inductance from the positive terminal of the input capacitance, through the top device, synchronous rectifier, and ground loop to the input capacitor negative terminal. The parasitic inductances are defined as:

$$L_s = L_{S1} \quad (4.1)$$

$$L_{Loop} = L_{D1} + L_{D2} + L_{S2} \quad (4.2)$$

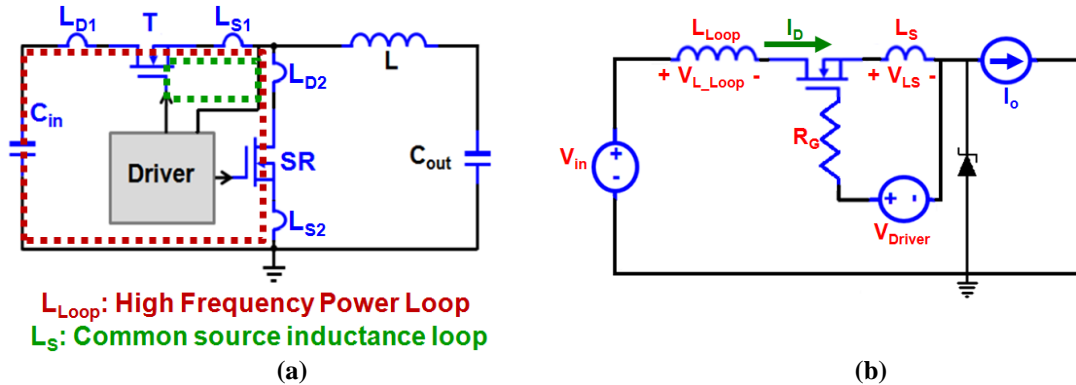


Figure 4.1: (a) Synchronous buck converter parasitic loops (b) Equivalent circuit for top switch

To design an efficient high frequency module, the impact of these circuit parameters on performance must be quantified. In a synchronous buck topology, the top switch is turned on and off with hard switching producing switching losses. The

synchronous rectifier has negligible switching loss because it operates with zero voltage switching due to the conduction of the body diode during the dead time. The impact of the parasitic parameters on switching loss of the top switch will be considered using the package parasitics and loss model verified and discussed in chapter 3.

The common source inductance, L_s , has been shown to be critical to performance because it directly affects the driving speed of the devices [72][73]. The common source inductance is mainly controlled by the package inductance. There has been significant effort related to reducing the common source inductance to minimize switching loss [68]. The previous chapter analyzed the GaN LGA package and quantified the reduction of package parasitics over the best available trench devices.

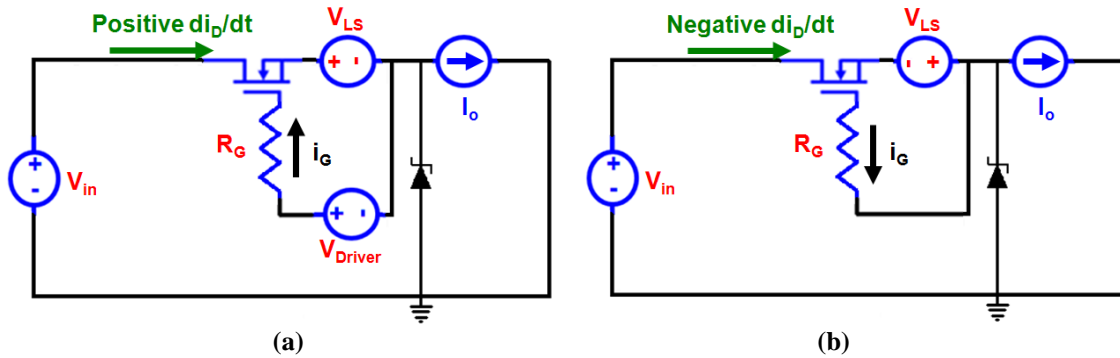


Figure 4.2: Impact of common source inductance during device (a) turn on (b) turn off

During the turn on transition, shown in figure 4.2a, the drain current is rising and a positive di_D/dt across the common source inductance induces a negative voltage. The induced voltage counteracts the driving voltage, reducing the available gate current, slowing the device turn on. The available driver current during turn on can be given by:

$$I_G = \frac{V_{Driver} - V_{gs(on)} - V_{LS}}{R_g} = \frac{V_{Driver} - V_{gs(on)} - L_s \cdot \frac{di_D}{dt}}{R_g} \quad (4.3)$$

$$V_{LS} = L_s \cdot \frac{di_D}{dt} \quad (4.4)$$

Where V_{Driver} is the driver voltage, $R_G = R_{G_GaN} + R_{on} + R_{ext}$, R_{G_GaN} is the GaN gate resistance, $V_{gs(on)}$ is the gate to source voltage during turn on, R_{on} is gate driver pull up resistance, and R_{ext} is external resistance.

During the turn off transition, shown in figure 4.2b, the drain current is falling and a negative di_D/dt across the common source inductance induces a positive voltage. The induced voltage again counteracts the driving voltage, slowing the device turn off:

$$I_G = \frac{-V_{gs(off)} + V_{LS}}{R_g} = \frac{-V_{gs(off)} + L_s \cdot \frac{di_D}{dt}}{R_g} \quad (4.5)$$

As a result, the common source inductance negatively impacts both the turn on and turn off losses. Figure 4.3a shows the switching loss vs. source inductance value, the common source inductance has a large effect of converter switching loss. This parasitic has been improved through device packaging and now reaches levels as low as 0.1nH [73].

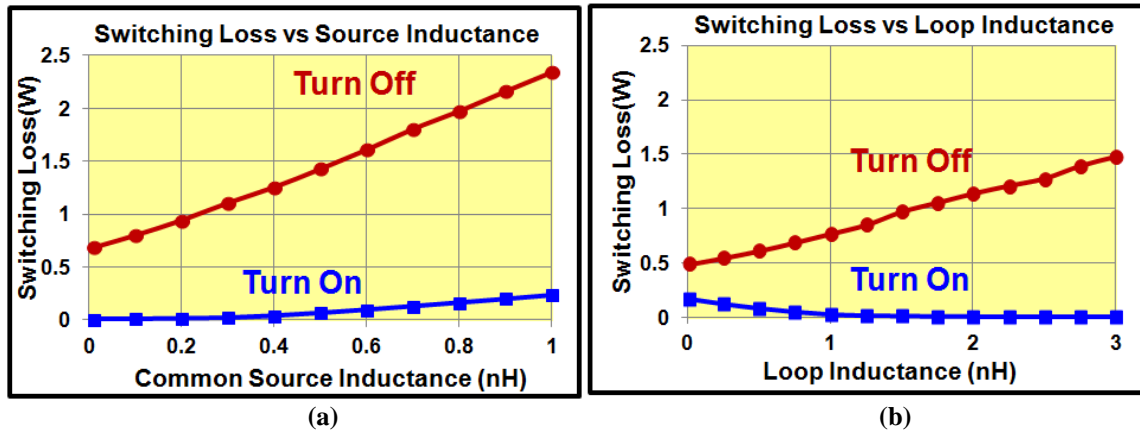


Figure 4.3: (a) Switching loss vs common source inductance for synchronous buck converter with $V_{in}=12V, V_o=1.2V, I_o=20A, L_{Loop}=1.35nH$, Device:EPC1015 (b) Switching loss vs loop inductance for synchronous buck converter with $V_{in}=12V, V_o=1.2V, I_o=20A, L_s=0.16nH$ Device:EPC1015

The loop inductance, L_{Loop} , impacts the switching speed of the devices and the peak drain to source voltage spike during turn off. The loop inductance is mainly controlled by the circuit layout. Figure 4.4 illustrates the impact of L_{Loop} for turn on and

off switching transitions. During the turn on transition, shown in figure 4.4a, the drain current is rising and a positive di_D/dt across the loop inductance induces a negative voltage. The induced voltage subtracts from the input voltage and limits the turn on speed. The reduction in the effective voltage across the device during turn on reduces switching loss. The voltage across the device is given by:

$$V_{L_Loop} = \frac{di_D}{dt} \cdot L_{Loop} \quad (4.6)$$

$$V_{DS} = V_{in} - V_{L_Loop} = V_{in} - \frac{di_D}{dt} \cdot L_{Loop} \quad (4.7)$$

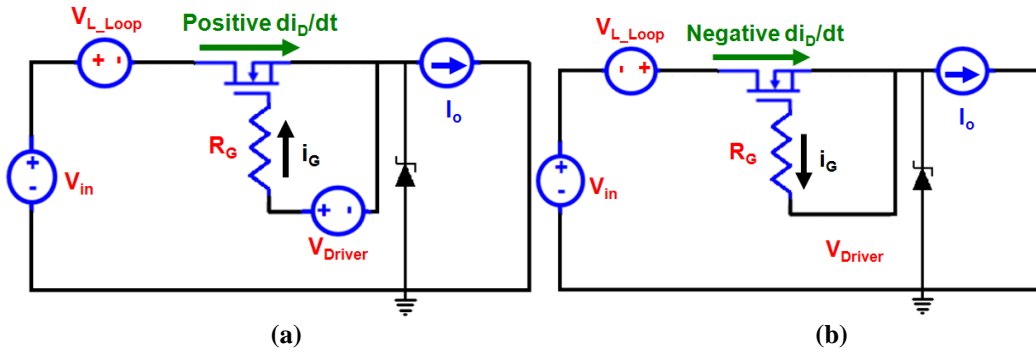


Figure 4.4: Impact of loop inductance during device (a) turn on (b) turn off

During the turn off transition, shown in figure 4.4b, the drain current is falling and a negative di_D/dt across the loop inductance induces a positive voltage. The induced voltage adds to the input voltage. The increase in the effective voltage across the device during turn on increases switching loss and lengthens the switching transition time.

$$V_{DS} = V_{in} + V_{L_Loop} = V_{in} + \frac{di_D}{dt} \cdot L_{Loop} \quad (4.8)$$

As a result, the loop inductance decreases the turn on loss and increases the turn off loss. With turn on loss contributing a significantly smaller amount to total switching loss than the turn off loss, loop inductance negatively impacts converter performance. Figure 4.3b shows the switching loss vs. loop inductance value, the loop inductance has a large effect of converter switching loss, especially when the source inductance is

minimal. While the common source inductance is controlled by the device packaging, the loop inductance is mainly controlled by the circuit layout. Methods to reduce loop inductance and its impact of performance will be covered in this chapter.

4.2.1 Generation 2 Design Comparisons

For generations 1 and 2, the focus was on the device selection, driver design, and dead time control; and the power loop was not optimized. The high frequency power loop, L_{Loop} , was made large to provide space for accurate device measurements. The second generation, without an optimized layout, achieved significant efficiency improvements over the Si benchmark design with optimal layout. A major contribution to the high efficiency was the reduced common source inductance of the device, which was minimized from the package of the GaN to be around 0.1nH.

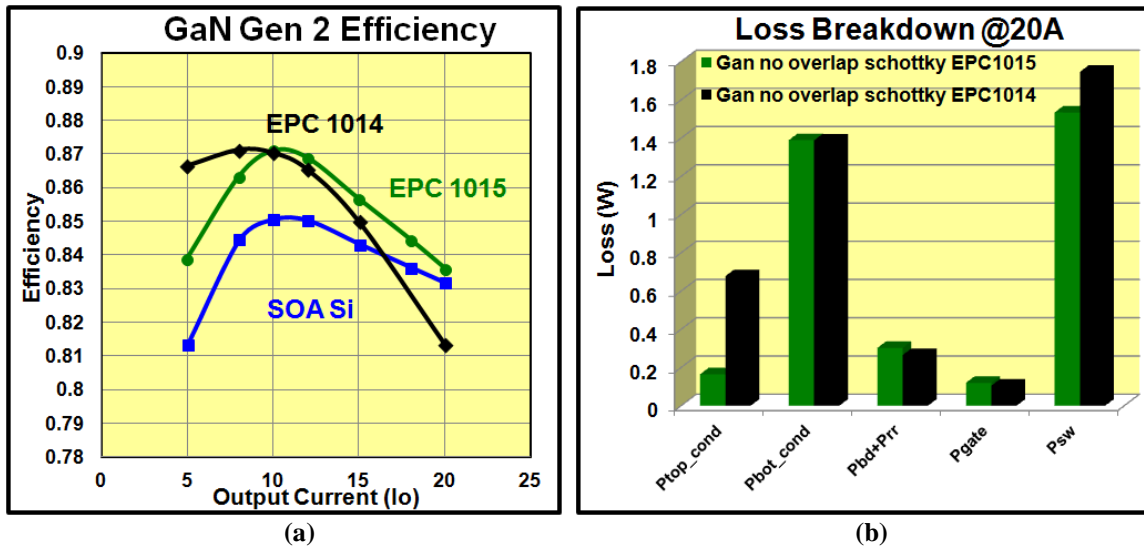


Figure 4.5: (a) Generation 2 efficiency comparison ($V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, $L=150nH$ Top device=EPC1014/5 SR=EPC1015) (b) Loss breakdown

While testing the second generation design, two different top switches were evaluated, the EPC1014 and EPC1015. The parametric comparison between the two devices is shown in table 4.1; from the datasheet, the smaller EPC1014 offered lower switching related charges. In experimental testing, using the EPC1015 top switch

provided superior results, as shown in figure 4.5a. The loss breakdown, shown in figure 4.5b, showed the EPC 1015 provided both lower conduction and switching losses than the smaller capacitance die. The reason for the higher switching loss in the smaller EPC 1014 die was a result of higher internal packaging inductance. Conferring with the device manufacturer, the smaller packaged device has fewer internal bussing connections, increasing the parasitic inductance over the larger device.

	Miller Charge Qgd (nC)	Gate Charge Qg (nC)	On Resistance Rdson (mΩ)	Total Inductance (nH)
EPC1014	0.55	3	12	0.38
EPC1015	2.2	11.6	3.2	0.16

Table 4.1: Device characteristics of EPC1014 and EPC1015

4.2.2 High Density Generation 3 Design

For the generation 3 design, the focus was on combining the knowledge gained from generations 1 and 2 into a low parasitic layout to improve overall efficiency and achieve the maximum power density. For the third generation design, all of the active components and capacitors were placed on the top layer of the PCB; to allow for a flat PCB bottom layer to accommodate 3D integration of a low profile LTCC inductor designed to fit the module footprint, maximizing power density.

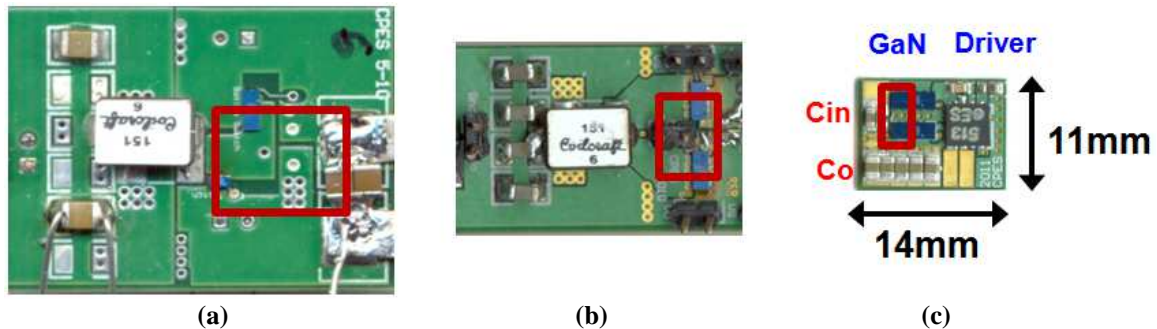


Figure 4.6: $V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, $L=150nH$ GaN designs (a) Generation 1 (b) Generation 2 (c) Generation 3

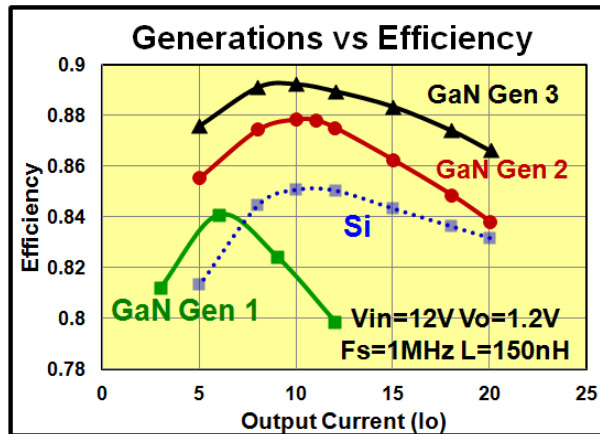
Shown in figure 4.6 are the three generations of designs with the high frequency power loops shown in red. The board footprint, power loop size, and high frequency

loop inductances are shown in table 4.2. The final values for the loop inductances for the three generations of designs were obtained from FEA Maxwell 3D simulations.

	Generation 1	Generation 2	Generation 3
Board Footprint	840mm ²	570mm ²	154mm ²
Power Loop Size	46mm	31mm	18mm
High Frequency Loop Inductance, L_{Loop}	6.30nH	2.90nH	1.19nH

Table 4.2: Parasitic loop inductances for generations 1,2 and 3 designs

The efficiency comparisons between the generations are shown in figure 4.7. The first generation design showed full load efficiency 5% below the benchmark Si buck converter design. The second generation with a proper driver and anti-parallel diode addition saw a 3% peak efficiency improvement over the benchmark design but had similar efficiency at 20A. For the third generation design with the lowest inductance layout, a 4% improvement in peak efficiency was seen and an efficiency gain of around 3% was seen at full load. Due to the low package parasitics of the GaN device, layout considerations are very critical to high performance, this is also true for Si lateral devices.



**Figure 4.7: Efficiency comparison between generations. $V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, $L=150nH$
Gen1 T:EPC1014, SR:EPC1015, Gen2&3 T:EPC1015, SR:EPC1015.**

Shown in figure 4.8 are the drain to source voltage waveforms for the second and third generation designs measured at 1MHz. The impact of minimizing the high frequency loop inductance lowers switching loss and the device ringing. For the third

generation design, the voltage overshoot was decreased over 25%. The final values for peak device voltage stress are given in table 4.3.

	Generation 2	Generation 3
Top Switch Peak Voltage	26.4V	19.9V
SR Peak Voltage	18.4V	13.1V

Table 4.3: Peak device voltages for generations 2 and 3 designs

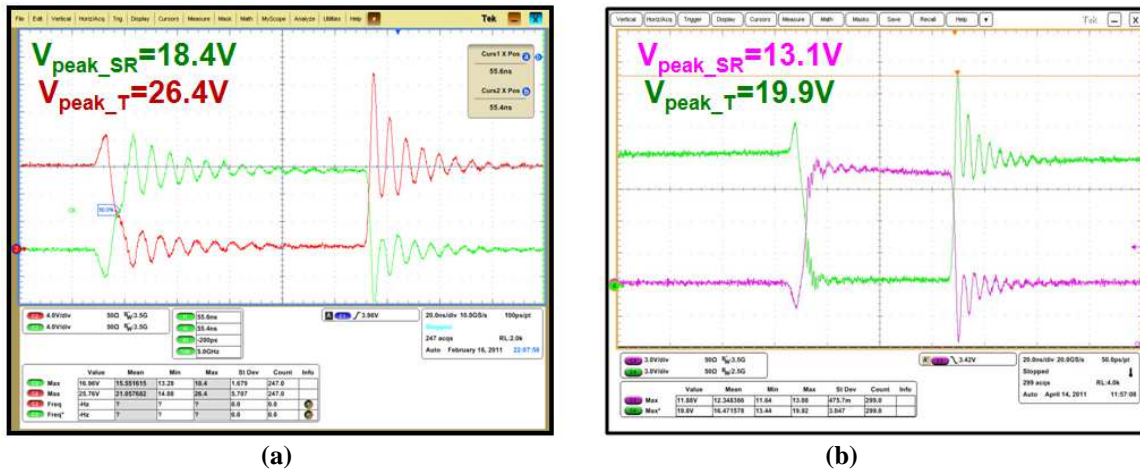


Figure 4.8: (a) Generation 2 voltage waveforms (b) Generation 3 voltage waveforms

Utilizing the GaN loss model developed in chapter 3 the loss breakdown was compared between generations 2 and 3. Figure 4.9a compares the power loss vs parasitic inductances; the common source inductance is minimal in both designs from the GaN package, resulting in similar L_s related losses for generations 2 and 3. With minimal common source inductance, the high frequency loop inductance becomes the major barrier to reduced loss.

Figure 4.9b shows the loss breakdown and it can be seen that for generation 3, the turn off loss and trace conduction losses were reduced 40% by improved layout. In high density modules with low loss GaN devices, the trace the layout conduction loss is critical for high efficiency. Compact layout will reduce the trace losses, as was evidenced by the loss breakdown in 4.9b. The largest loss in the generation 3 design is the SR conduction loss, which is currently limited by a non optimized GaN SR.

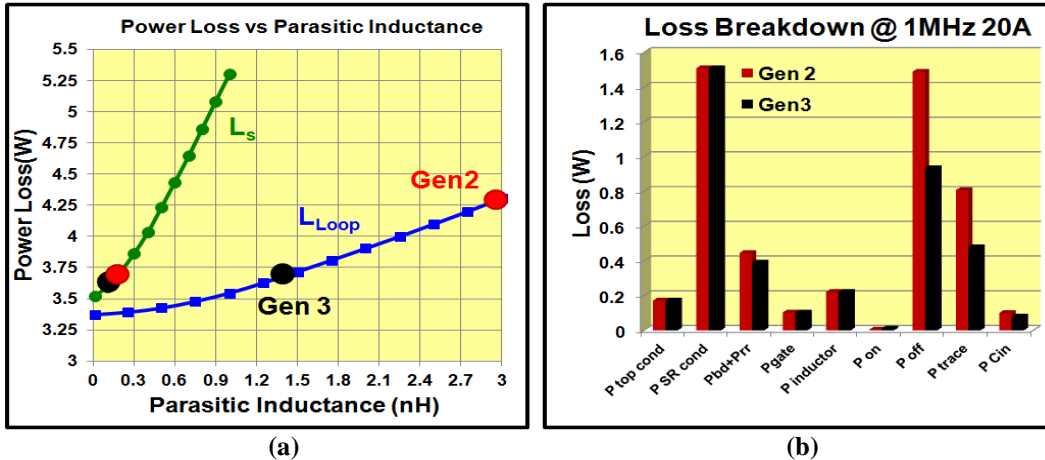


Figure 4.9: (a) Parasitic inductance impact on power loss ($V_{in}=12V$, $V_o=1.2V$, $F_s=1MHz$, $L=150nH$)
 (b) Loss breakdown for generations 2 and 3

With lower switching related losses, the third generation design allowed for the frequency to be increased. Shown in figure 4.10 is the impact of frequency on efficiency. Increasing the frequency from 1 to 2 MHz lowered the efficiency; but the design was able to match the full load efficiency of the benchmark 1MHz discrete buck converter while offering a percent increase in peak efficiency at twice the operating frequency. The ability to double the switching frequency while achieving low loss is a result of the ultra low parasitics in generation 3 combined with the low loss GaN devices. As a result of the higher switching frequency the size of the output inductance can be reduced facilitating integration using a low profile low temperature co-fired ceramic inductor.

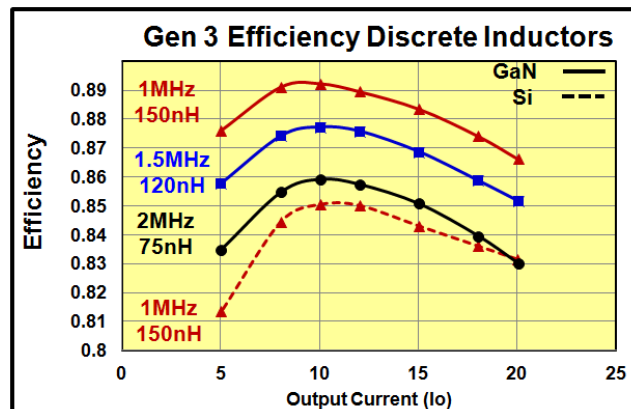


Figure 4.10: Efficiency of GaN generation 3 at 1, 1.5, 2MHz vs Si Buck at 1MHz. $V_{in}=12V$, $V_o=1.2V$,
 Si Buck: Top Device: CSD16410 SR:CSD16325 Driver:LM27222 GaN Gen 3 Devices:2xEPC1015,
 Driver:LM5113

4.2.3 Low Profile Inductor Integration

The integration of low-profile passive components, including the output filter inductor, is a key to the minimization of power supplies. By utilizing low temperature co-fired ceramic (LTCC) technology [75][76], the 3D integration concept can offer a compact design with the output inductor serving as the substrate. The 3D integrated module can save the inductor footprint and fully utilize the available space to achieve high power density. To maximize the power density and reduce converter footprint for the third generation converter an inductor was designed in [77] to fit on the backside of the generation 3 module.

The inductance analytical model for the LTCC inductor substrate with non-uniform flux and permeability distribution is proposed and validated in [76]. The inductance can be found from equation 4.9 with the parameters defined in figure 4.11.

$$L_{N=n} = 2 \int_0^g \frac{n^2 \cdot \mu_{r\Delta} (H_{DC_N=n}) \cdot h}{\sqrt{2} \cdot \sqrt{\left(n \cdot r_v + \frac{(n-1)d}{2} + r \right)^2 + (r_v + r)^2}} \cdot dr \quad (4.9)$$

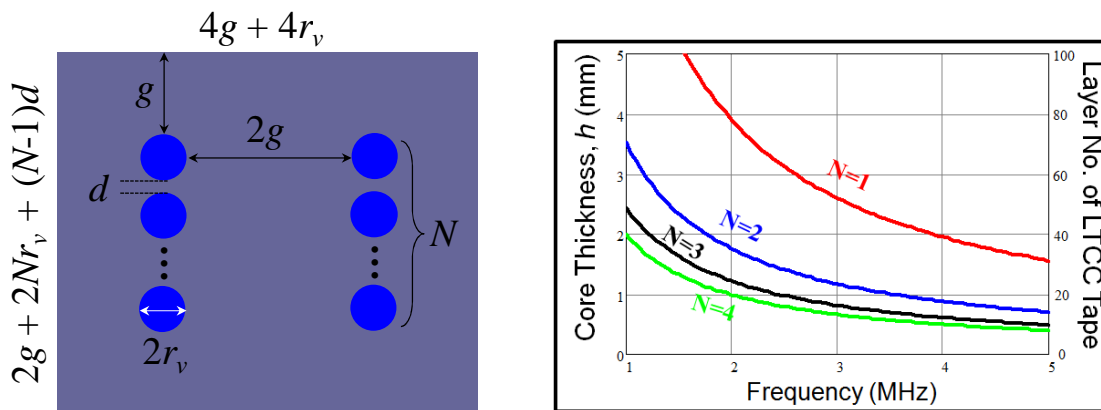


Figure 4.11: (a) LTCC inductor substrate structure with design parameters (b) Core thickness as a function of frequency for different number of turns

The core thickness for different frequencies and different turn numbers, with an inductance designed for 60% current ripple at 15A, is compared in figure 4.11b. The

LTCC inductor is built by sintering and co-firing a number of thin LTCC sheets together as described in chapter 1. Increasing core thicknesses beyond 3 mm is not possible due to process limitations [78]. To simplify the inductor design, reduce cost, and reduce thickness, the number of LTCC layers used to achieve the required core thickness should be minimized.

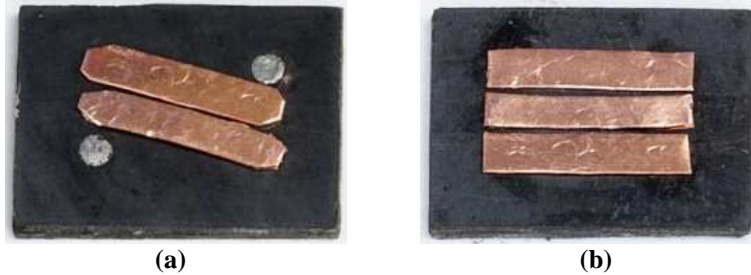


Figure 4.12: Three turn LTCC inductor with surface winding (a) Top view (b) Bottom view

	Discrete Inductor SLC1049-750ML	LTCC Inductor LTCC 50 material
Inductance @15A	75nH	60nH
Inductor DCR	0.3mΩ	1.2mΩ
Inductor Height	5.1mm	1.2mm
Inductor Volume	362mm ³	169 mm ³

Table 4.4: Comparison between discrete and LTCC inductor for 2MHz

Selecting the number of turns is a tradeoff between core thickness and inductor loss. Increasing number of turns reduces the core thickness but suffers from increased winding loss. For the generation 3 design, the three turn structure was chosen to achieve a good tradeoff of low profile, limiting the number of LTCC layers, vs. inductor winding loss. The final inductor is shown in figure 4.12 and the comparison between the low profile LTCC inductor and the standard discrete inductor are compared in table 4.4. The inductor is fabricated using LTCC50 material to provide low high frequency core loss, the performance of the different materials are compared in [79].

The LTCC inductor has non-linear inductance; with inductance increasing as current decreases. The increased light load inductance reduces current ripple, lowering

the turn off current, and reducing light load switching loss. The turn off current for a buck converter is given by:

$$I_{off} = I_o + \frac{V_{in}(1-D) \cdot D}{2 \cdot L \cdot f_s} \quad (4.10)$$

The inductance value vs DC bias current is shown in figure 4.13a, the inductance value increases from 60nH at 15A to 165A at no load. Figure 4.13b shows the efficiency of the generation 3 with discrete and LTCC inductors tested at 2MHz, the LTCC inductor provides light load efficiency gains from lower converter switching ripple, but suffers at heavy load to the higher winding DCR. With the reduced profile the power density of the converter was improved by a factor of two at 2MHz and the peak efficiency was improved 0.5 percent.

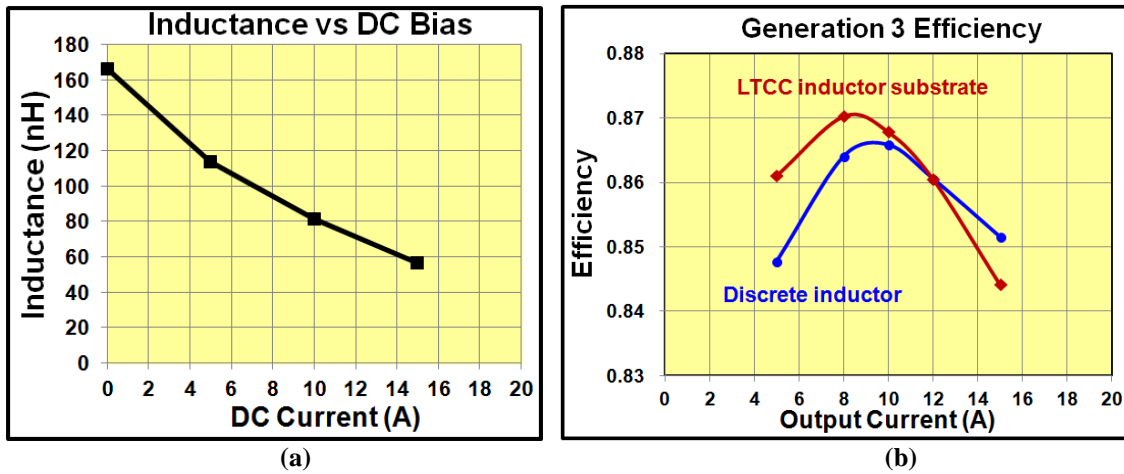


Figure 4.13: (a) Inductance vs. DC bias current for LTCC 50 inductor (b) Efficiency for generation 3 design with discrete and LTCC inductors $V_{in}=12V$, $V_o=1.2V$, $F_s=2MHz$

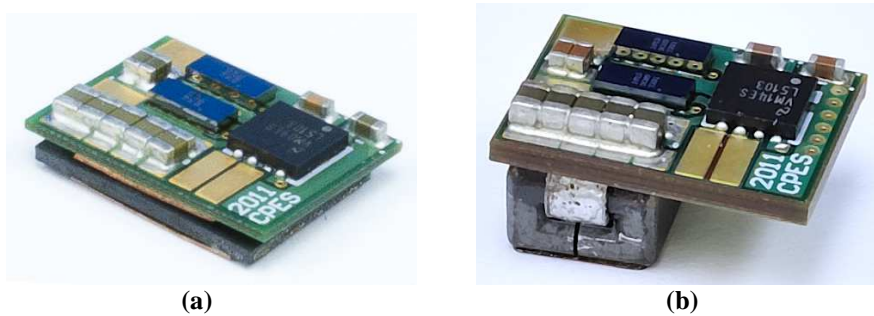


Figure 4.14: Experimental hardware for generation 3 with (a) LTCC inductor (b) Discrete inductor

4.3 Thermal Analysis of High Density POL Module

As the power density is increased in the third generation module, the thermal design becomes a critical aspect to consider; with thermal constraints often the bottleneck in power handling capability for high density modules. With GaN devices size shrinking in size, device current densities will increase almost an order of magnitude over current Si devices. This chapter will assess the impact of combining high frequency, small device size, and reduced footprint in the third generation module.

The comparison of 40V GaN and Si devices on resistance vs. temperature is shown in figure 4.15a for the EPC2015 and a Si device with the same gate charge. From figure 4.9b, it can be seen that the largest loss in the generation 3 design is SR conduction. For the GaN device, the maximum junction temperature is 150°C, but the resistance increases significantly with temperature, resulting in larger conduction losses. The relationship between temperature and resistance can be given by:

$$R_{ds_on}(m\Omega) = 2.8e^{0.0055T(C^\circ)} \quad (4.11)$$

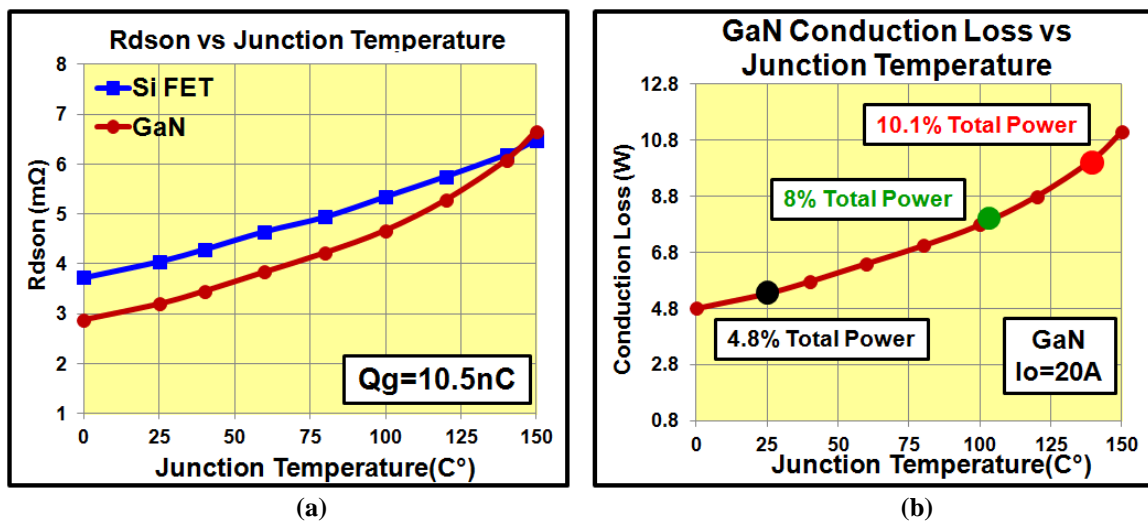


Figure 4.15: (a) On resistance vs junction temperature for GaN and Si devices (b) Conduction loss for GaN buck converter at 20A vs junction temperature

For the third generation PCB design, a thermal camera was used to evaluate the temperature of the GaN devices and the module. The traditional PCB has an epoxy isolating the copper layers which has a very poor thermal conductivity of around $0.3\text{W/m}^{\circ}\text{K}$. As a result of the low thermal conductivity of the fr4 substrate, there is little heat distribution in the module and heat crowding is experienced on the edge of the board near the top device. Due to the small pad size and pitch of the GaN pins thermal vias could not be placed underneath the pads to alleviate the thermal strain. In the third generation PCB design there is little heat distribution, with the temperature varying over 40°C from the hot spot to the corner of the PCB board, increasing device loss.

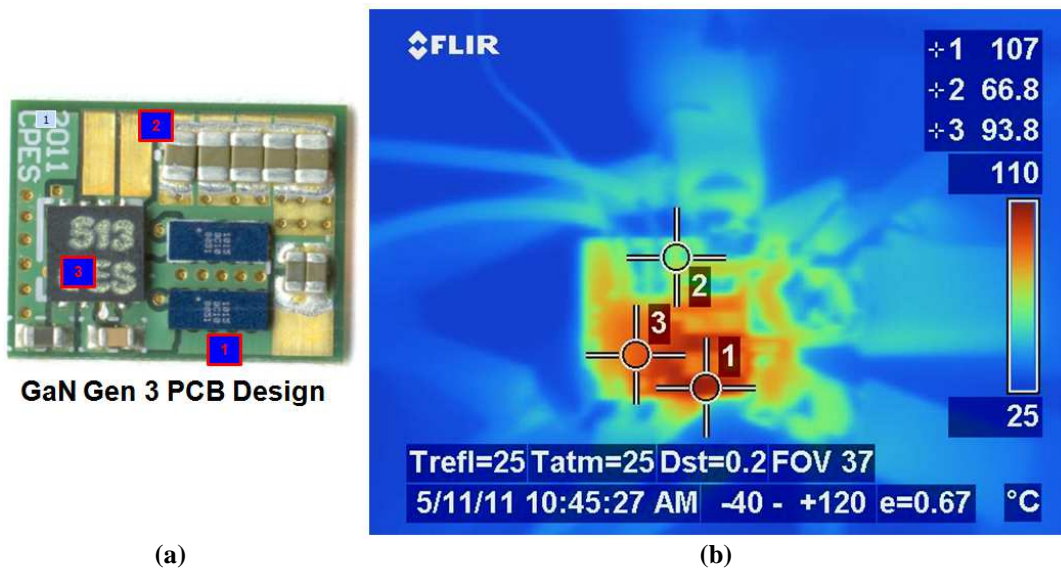


Figure 4.16: (a) Generation 3 PCB design with corresponding temperature measurement points (b) Thermal image of generation 3 @Ta=25C Fs=2MHz Ploss=4W under natural convection

To improve the thermal performance of the third generation design, another module was created using a direct bonded copper (DBC) substrate. The DBC substrate utilizes a conductive ceramic substrate with high thermal conductivity to isolate the copper layers [74]. The three major ceramic substrates available are Alumina, Alumina doped with 9% ZrO₂, and Aluminum Nitride and their properties are shown in table 4.5

[80]. The ceramic substrate used in this project was alumina, it was chosen as the ceramic for this project because of its thin ceramic thickness, high mechanical stability, and low cost. The impact of the ceramic thickness on module electrical performance is critical and will be discussed in detail in this chapter.

	Thermal conductivity W/mK	Minimum ceramic thickness (mm)
Alumina	24	0.25
Alumina w/ 9% ZrO2	28	0.32
Aluminum Nitride	180	0.63

Table 4.5. Direct bond copper substrate material characteristics

Shown in figure 4.17b is the thermal image from the DBC design. For the DBC design, the heat is distributed throughout the board by the highly thermal conductive alumina substrate, resulting in a more uniform board temperature without hotspots. For the DBC design, the difference in temperature from the GaN to the coolest portion of the board is only 5°C. The hottest spot on the DBC board is the drive chip, which has a temperature difference of 14°C from the coldest area of the board and is limited by the poor thermal conductivity of its LLP package. The thermal tests were run at a frequency of 2MHz and under natural convection conditions.

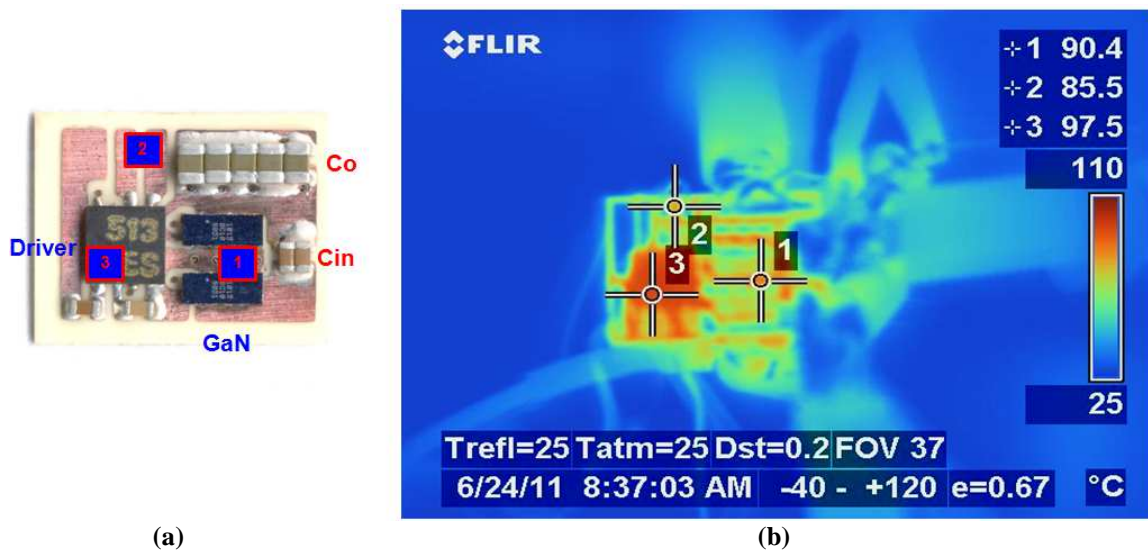


Figure 4.17: (a) Generation 3 DBC design with corresponding temperature measurement points (b) Thermal image of generation 3 @ Ta=25C Fs=2MHz Ploss=5.4W under natural convection

The improved thermal performance from the alumina substrate allows for the module to handle more power loss while maintaining a safe device operating temperature. Shown in figure 4.18 is the device peak temperature vs power loss for the PCB and DBC designs. The DBC design can handle around 2 additional watts of power loss than the original PCB module. This allows for a much higher power handling capability which is necessary to have a high power density module design.

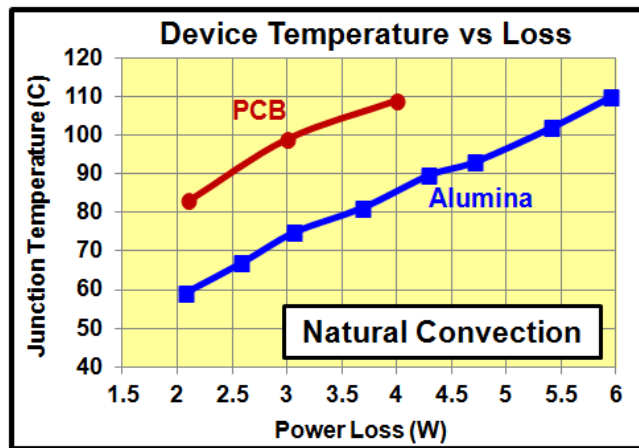


Figure 4.18: Device Temperature vs Power Loss for generation 3 PCB and DBC designs

4.4 High Density DBC Module Electrical Improvements

4.4.1 Generation 3 PCB and DBC Electrical Performance Comparison

The DBC substrate provided superior thermal performance when compared to the PCB design; while the footprint and part layout of the two designs were identical there were some differences in the designs: the number of inner copper layers and the distance between the inner layers. The fr4 epoxy used as an insulator in PCB design provides low thermal conductivity but can achieve very low insulator thicknesses, down to 5 mils. Traditional PCB technology also has the benefit of the ability to easily build multi layer designs. Most industry PCB designs use 4 to 6 inner layers to improve electrical

performance and the inner layers are connected with internal metalized vias. For the third generation PCB design the board contained 4 layers, each containing 2 ounce copper, and the insulating fr4 epoxy between each layer was 5mils. The cross section view of the board is shown in figure 4.19b.

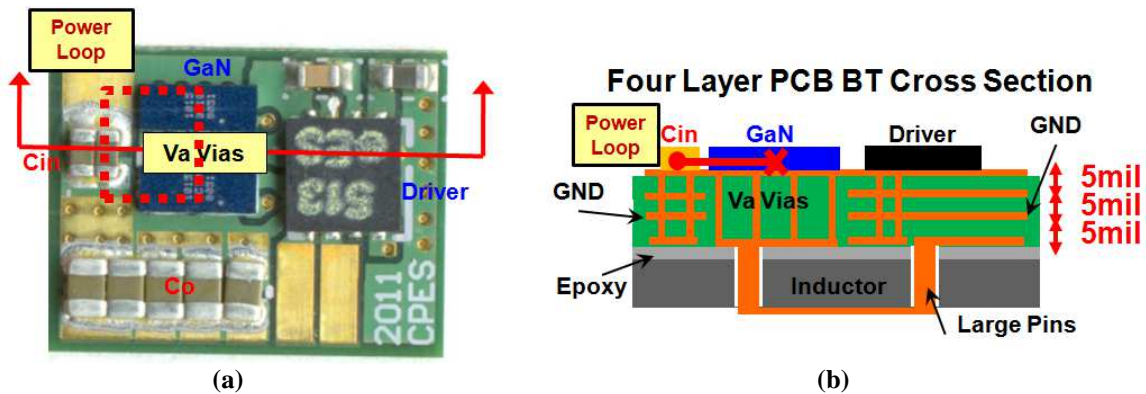


Figure 4.19: Generation 3 PCB design (a) top view with cross cut shown in solid red (b) cross section view of 4 layer structure

For the alumina based design, the minimum substrate thickness is limited to 10 mils to ensure mechanical stability and prevent ceramic cracking. For cost reduction and fabrication simplicity, the ceramic substrate is also limited to a 2 layer design. For the third generation DBC design the board contained 2 layers, each having 2 ounce copper, and the insulating alumina between the layers measuring 15 mils. The cross section view of the board is shown in figure 4.20b.

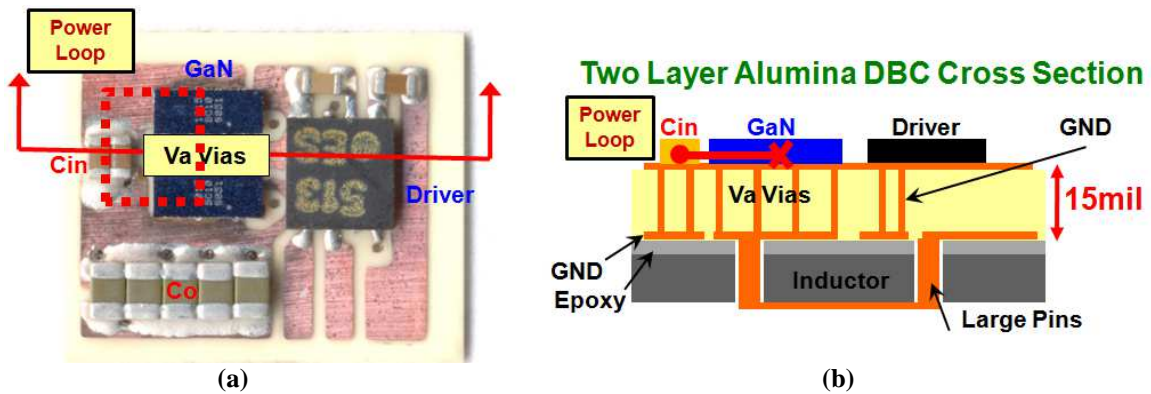


Figure 4.20: Generation 3 DBC design (a) top view with cross cut shown in solid red (b) cross section view of 2 layer structure

The efficiency of the PCB and DBC designs were compared in figure 4.21. By switching from the traditional PCB substrate to the alumina DBC substrate the power handling capability improved by 50%, but the electrical performance suffered. The efficiency of the DBC module experienced a 2% decrease in peak efficiency and a full load efficiency drop of 2.5%.

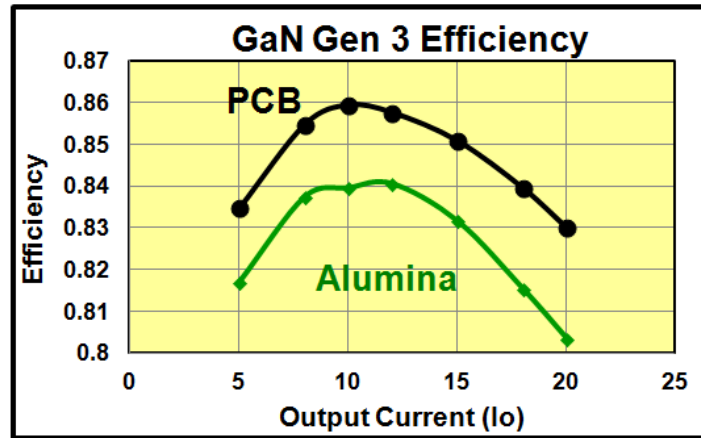


Figure 4.21: Generation 3 PCB and DBC efficiency comparison $V_{in}=12V$, $V_o=1.2V$, $F_s=2MHz$, $L=75nH$, T/SR:EPC1015

4.4.2 Shield Layer Impact on Performance

In the previous section, two designs with identical part layouts experienced drastically different performance based on the construction of the substrate and the number of inner copper layers. To improve the performance of the high density module, the large efficiency drop encountered by switching from PCB to DBC had to be explained. This section will quantify the impact of the substrate and inner layers on circuit parasitics and circuit performance.

The major difference between the PCB and DBC designs was the first inner layer, directly underneath the power loop. The first inner layer serves as a “shield layer”, originally described in [82] to shield the power loop from the inductor substrate. The shield layer is critical for all designs, independent of the inductor and will be discussed in

this section. The concept of shield layer is shown in figure 4.22, the power loop current flows on the top layer of the board parallel to the substrate. The power loop current will generate a magnetic field, as shown in figure 4.22c; this magnetic field will induce a current, opposite in direction to the power loop, inside the shield layer. The current in the shield layer will generate a magnetic field to counteract the original power loops magnetic field. The end result is a cancellation of magnetic fields, translating to a reduction in parasitic inductance, as depicted in figures 4.22d.

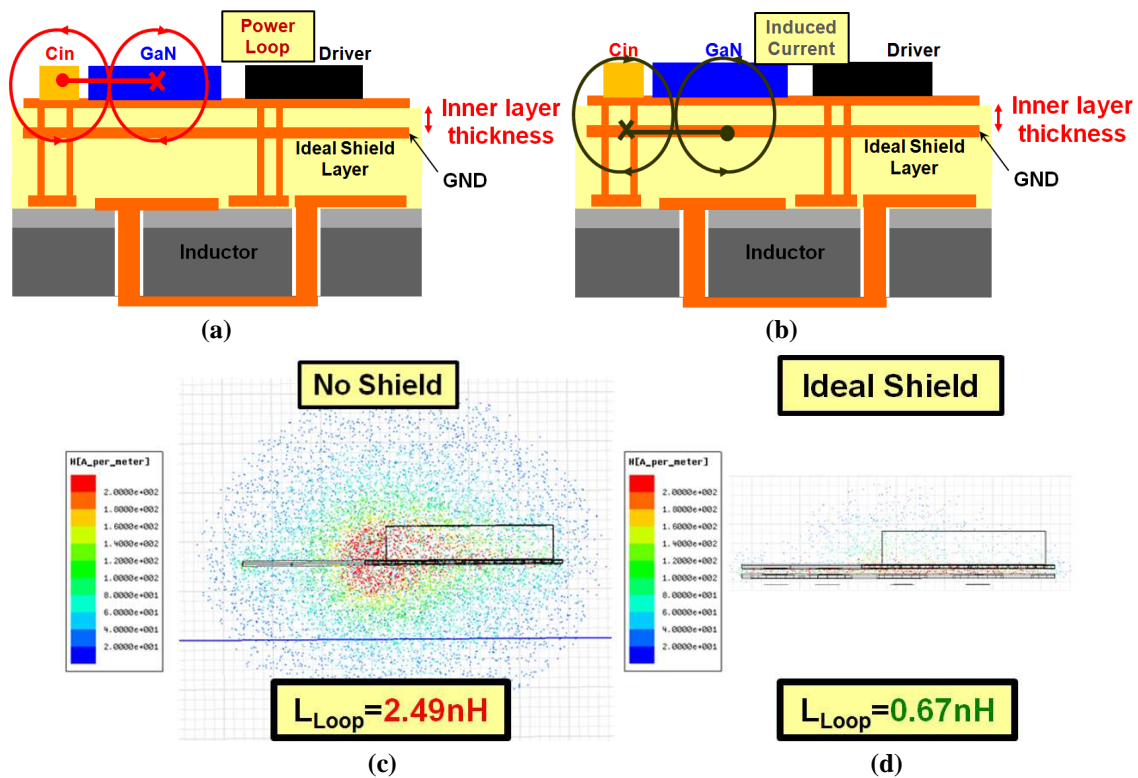


Figure 4.22: Cross sectional view of generation 3 design (a) Flux induced by power loop (b) Induced flux and current in shield layer (c) Magnetic field intensity plot without shield layer (d) Magnetic field intensity plot with ideal shield layer

To accurately model the inductance and study the shield effectiveness, Maxwell 3D FEA simulation software was used. The basic principle behind FEA analysis is to break up a larger simulation into many smaller, solvable tetrahedral elements. In each tetrahedral element, the simulator solves Maxwell's differential equations to evaluate the magnetic fields

in the system [83]. The FEA software package, using the eddy current solver method takes into account the eddy current effect, skin depth effect, cornering effect, and proximity effect encountered in high frequency low profile magnetics [84]. As described in [85], the eddy current solver uses an AC current input and computes the magnetic field in the system (and stores them in magnitude and phase vectors) by using the following equation:

$$\nabla \times \left(\frac{1}{\sigma + j\omega\epsilon} \nabla \times H \right) = j\omega\mu H \quad (4.12)$$

where σ represents conductivity, ω represents radian frequency, and H represents magnetic field intensity.

The energy stored in a magnetic field is given by [86]:

$$W_H = \frac{1}{2} \int_{Vol} B \bullet H dv = \frac{1}{2} L \cdot I^2 \quad (4.13)$$

This energy is equal to the energy stored in the leakage inductance produced by an external AC current source. Solving the energy equation yields the value of the leakage inductance:

$$L = \frac{1}{I^2} \int_{Vol} B \bullet H dv \quad (4.14)$$

For the shield layer to be effective it must be complete, and close to the power loop. The closer the placement of the shield layer to the power loop, the higher coupling that will exist between the layers, and the more effective the field cancellation. The completeness of the shield layer is also important, ensuring that the induced current can flow in the proper direction to effectively cancel fields. Shown in figure 4.23a is the top

layer containing the power loop; and in 4.23b, an ideal shield plane, consisting of a solid sheet of copper on the first inner layer.

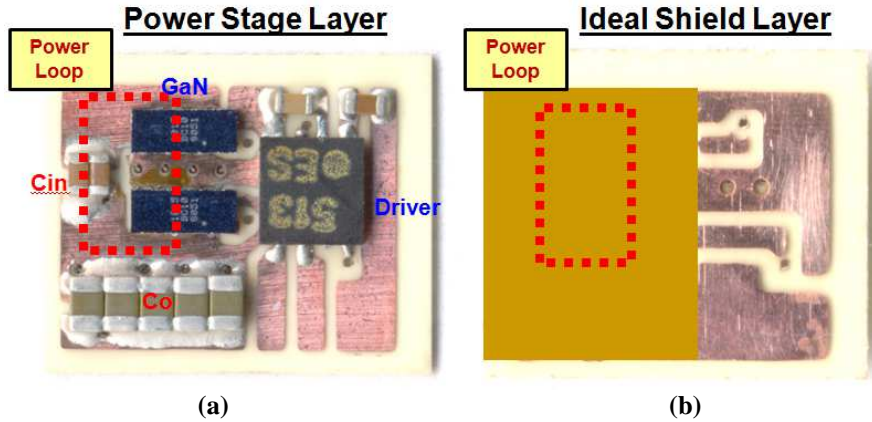


Figure 4.23: (a) Power stage plane with high frequency power loop (b) Ideal shield layer with high frequency power loop superimposed

The current density plots for the shield layer are shown in figure 4.24 with the distance between the shield layer and power loop layer varying from 5 to 15 mils. As the shield layer is moved closer to the power loop layer the coupling increases, causing the current to more closely resemble the top layer current. When the induced current in the shield layer increases and counteracts the power loop, greater amounts of field cancellation are achieved, minimizing inductance.

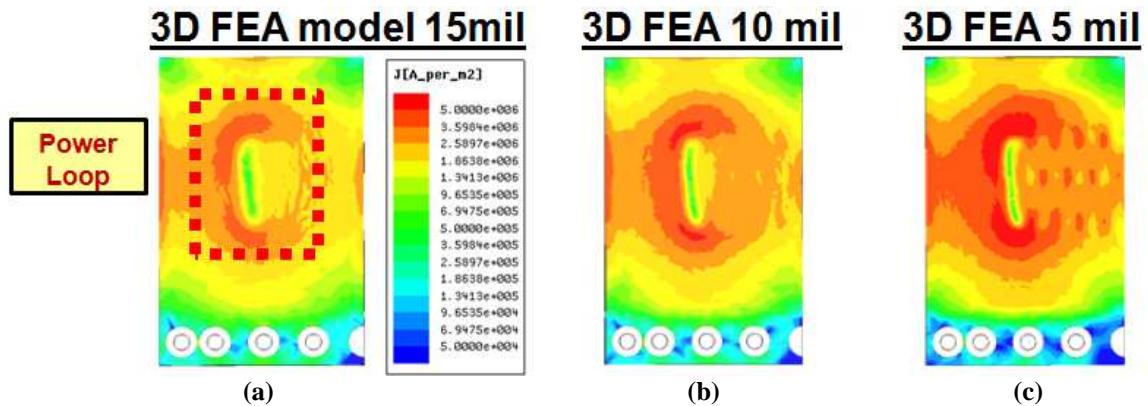


Figure 4.24: Shield plane current density for (a) 15mil distance from power plane to shield plane (b) 10mil distance from power plane to shield plane (c) 5mil distance from power plane to shield plane

Figure 4.25 shows the magnetic field intensity plots for ideal shield layer designs for the cases with the shield separation from the power loop of 5 and 15 mils. For the 15

mil separation distance, there is partial field cancellation and a large amount of energy stored in between the shield layer and the power loop and above the power loop; this is a result of the poor coupling between the shield layer and power loop. For the 5 mil case, there is high coupling between the power loop and the shield, improving field cancellation, producing a significant reduction in field and parasitic inductance in the design.

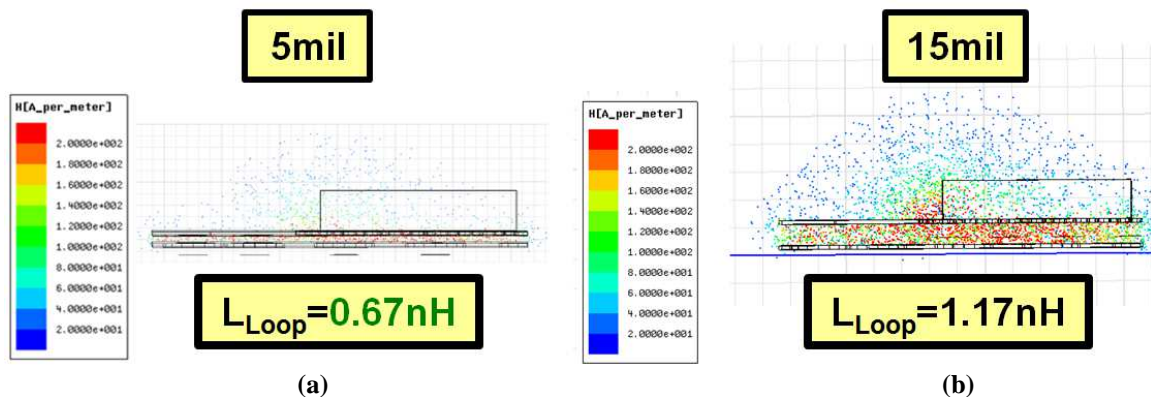


Figure 4.25: Generation 3 DBC with ideal shield magnetic field intensity for (a) 5 mil shield separation distance from power loop (b) 15 mil shield separation distance from power loop

Shown in figure 4.26 are the simulated values of the high frequency loop inductance vs separation distance between the shield and power layer. The inductance is broken down into two components, the inductance from the power loop and shield layer traces and the leakage, which consists of the energy stored in the substrate and air.

It can be seen that impact of separation distance between the shield layer and power loop dominates the inductance at larger distances. With the isolating layers ranging from 5-15mil in standard PCB and DBC designs, the inductance contributed by the trace accounts for less than 20% of the overall loop inductance. The winding inductance decreases slightly as the separation distance is increased due to reduced coupling while the leakage energy increases significantly. The impact of shield copper thickness on inductance is shown in figure 4.26b. The total loop inductance has little

dependence on the shield thickness, and for this work a shield distance of 2oz is selected to match the top power layer thickness, simplifying fabrication.

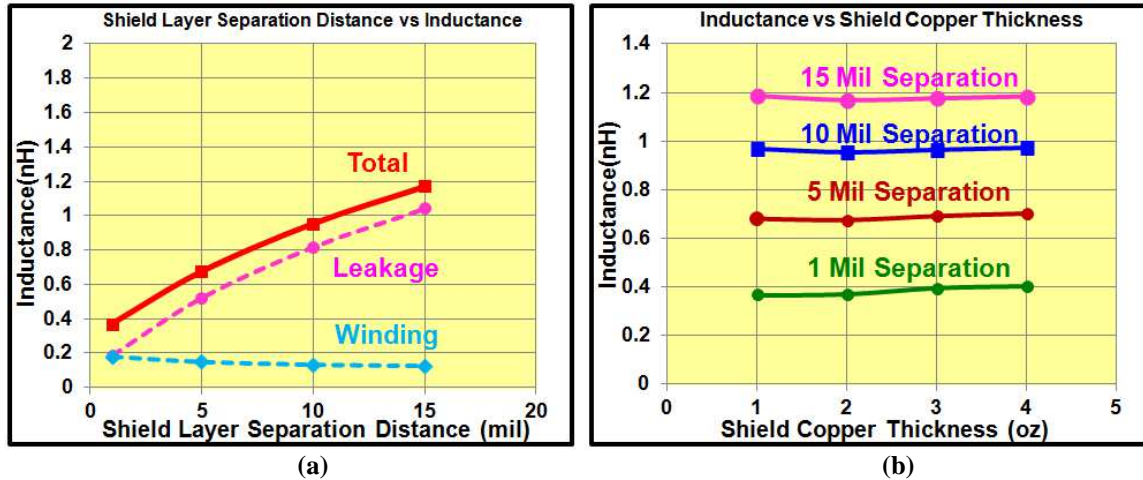


Figure 4.26: (a) Inductance breakdown for inductance vs distance between shield layer and power plane (b) Inductance vs shield thickness for 1-15mil shield separation distances

4.4.3 Generations 3 DBC and PCB Shield Layer Comparisons

Looking closely at the PCB and DBC designs, the impact of the shield on inductance can be compared to help explain the efficiency drop of the DBC module. The shield layer for the PCB design is shown in figure 4.27a, underneath the power loop is a solid sheet of copper except for the inductor via connections. The inductor vias were located in between the two GaN devices to minimize the trace and via resistance to the inductor and allow for the reduction in size of the power loop by placing the capacitors in close proximity to the GaN devices, as shown in figure 4.23a.

Figure 4.27b shows the current density in the shield layer for the generation 3 PCB design; the coupling is very good as a result of the 5 mil separation between the shield and power loop. The inductor vias have a major impact on the performance of the shield plane in this design; cutting the shield plane and forcing the shield current to crowd. The partial shield plane results in poor field cancellation, resulting in large inductance. The magnetic field intensity plots from the side and top views are shown in

figure 4.27 c&d, there is a large pocket of field in the area where the shield current crowds and does not effectively cancel out with the power loop. The resulting loop inductance for the third generation design was 1.19nH.

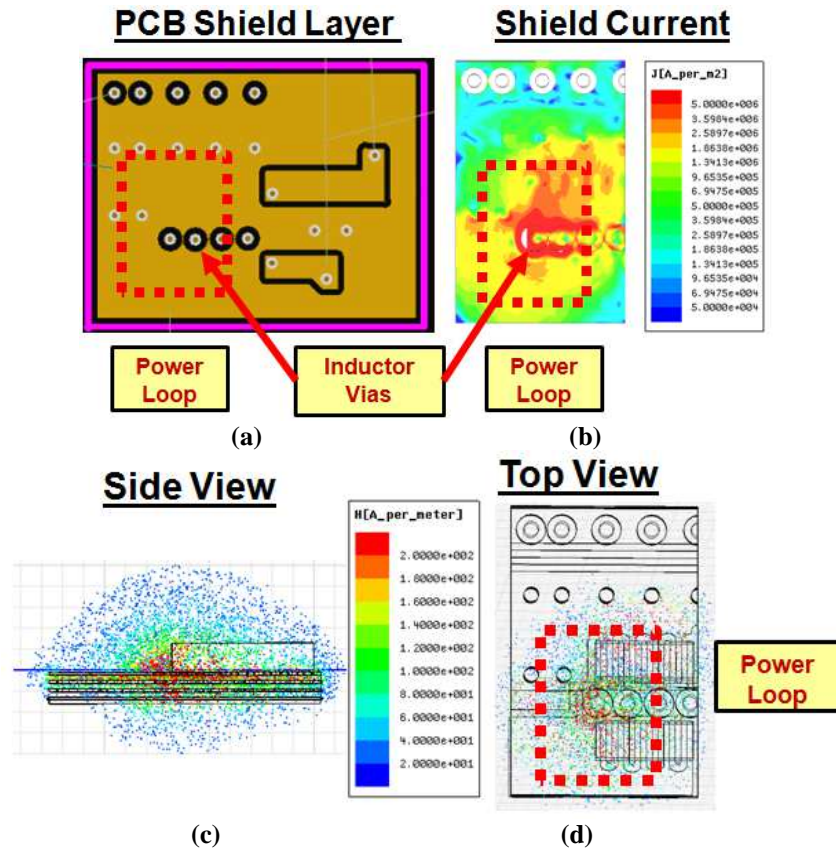


Figure 4.27: Generation 3 5 mil separation PCB design (a) shield layer (b) shield current density (c) side view of magnetic field (d) top view of magnetic field

Figure 4.28b shows the current density in the DBC design for generation 3, the coupling is poor as a result of the 15 mil separation distance between the shield and power loop. Due to the two layer design, the inductor connection pad and vias take up a large portion of the bottom layer, cutting the shield plane completely. The induced shield current crowds around the boundary of the shield layer and inductor pad; this causes poor field cancellation and large inductance. The magnetic field intensity plots from the side and top views are shown in figure 4.28 c&d, there again is a large pocket of field in the area where the shield current crowded and did not effectively cancel out with the power

loop. There is also a large amount of field in the large 15 mil separation between the power loop and shield layer. The resulting loop inductance for the third generation design was 1.73nH.

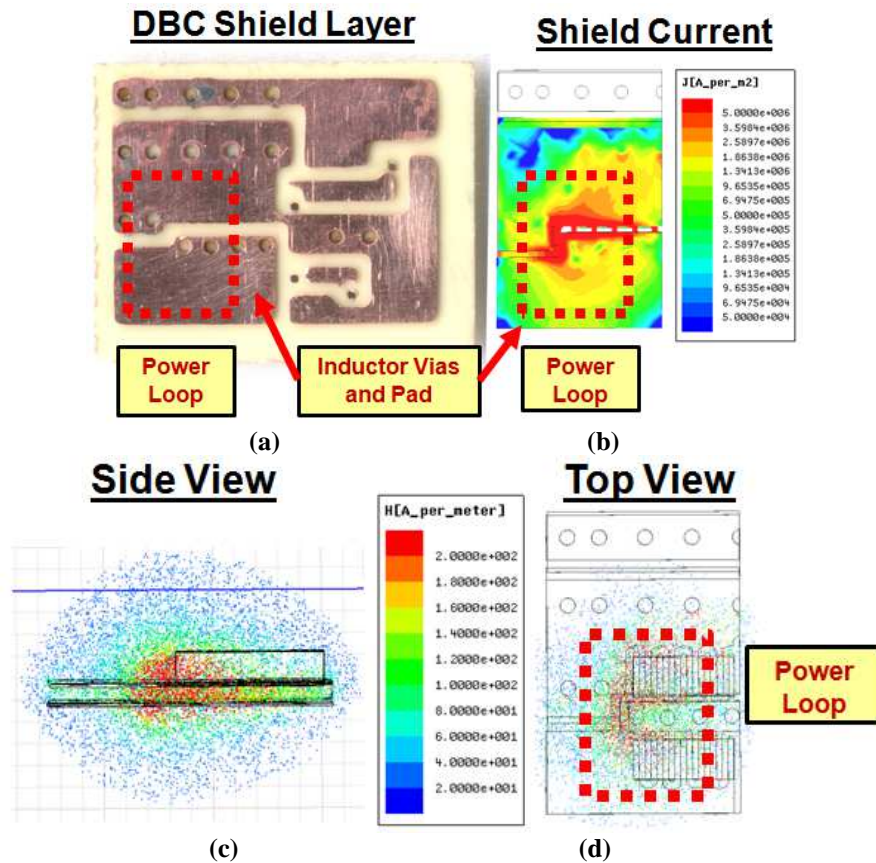


Figure 4.28: Generation 3 15 mil separation distance DBC design (a) shield layer (b) shield current density (c) side view of magnetic field (d) top view of magnetic field

The final comparison of the loop inductance for the PCB and DBC designs is shown in figure 4.29. Both of the third generation designs had poor shield layer designs, resulting in larger parasitic inductance. The cause of the incomplete shield layer was the location of the inductor vias; which were located in the center of the shield layer. While the location of the inductor vias minimized conduction loss, it increased the overall loop inductance increasing switching loss which dominates at higher frequencies. For the two layer DBC design, the location of the inductor connection pad also greatly decreases the

shield layers effectiveness. The PCB design, with a more complete shield plane, in closer proximity to the power loop, offered significantly lower inductance and higher efficiency.

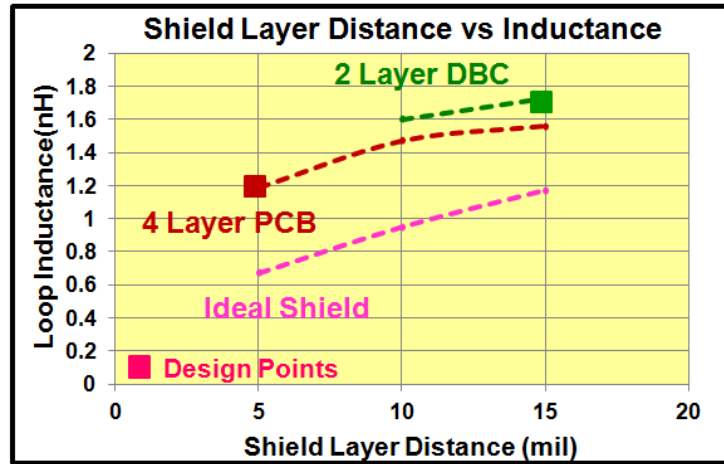


Figure 4.29: Inductance vs distance between shield layer and power plane for different designs

Both the PCB and DBC designs had inductances much larger than the case with an ideal shield. The DBC module, being a two layer design, allowed for the addition of an external shield layer underneath the incomplete shield layer to improve performance. The cross sectional and bottom views of the DBC module with and external shield are shown in figure 4.30. The shield layer thickness was 2 ounce copper and only a small opening was introduced to allow for the inductor pad connections.

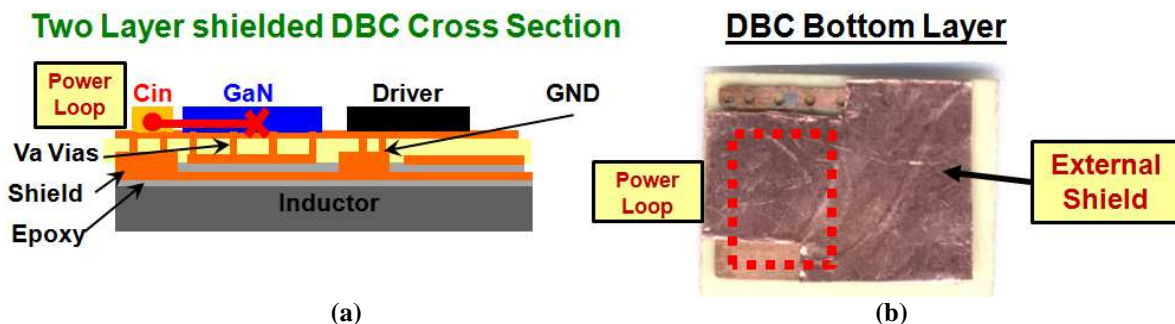


Figure 4.30: (a) Cross section view of generation 3 DBC with shield layer (b) Bottom view of DBC module with shield layer

The generation 3 DBC design with an additional external shield layer achieves better current distribution in the shield layer, as shown in figure 4.31b. The magnetic field intensity plots, in figures 4.31c&d show that better field cancellation is achieved,

resulting in lower inductance. The PCB and DBC designs had inductances much larger than the case with an ideal shield. The addition of the more complete external shield layer reduced the loop inductance 25% to 1.32nH.

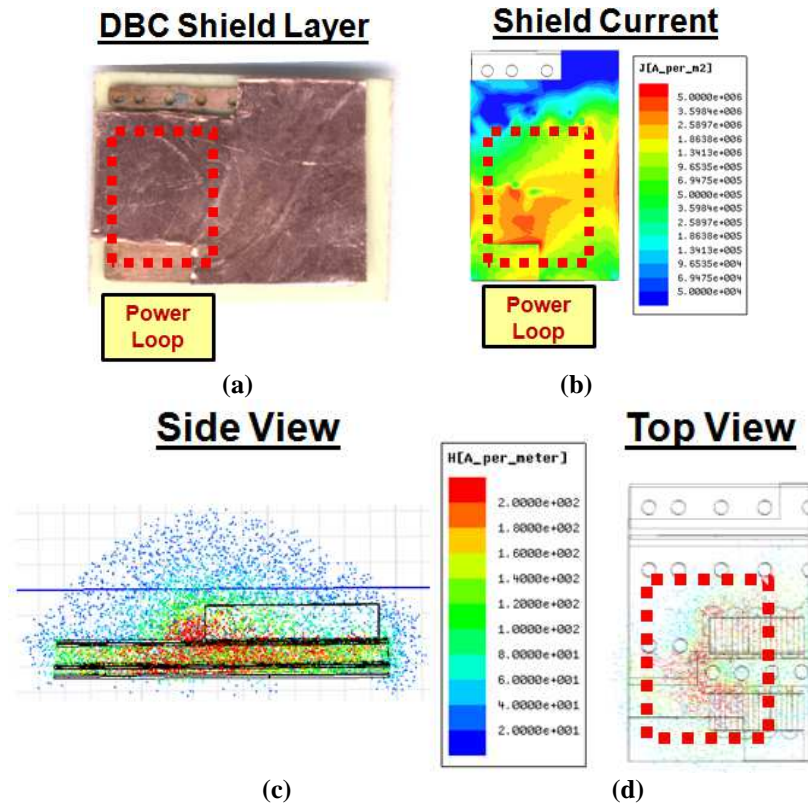


Figure 4.31: Generation 3 15 mil separation distance DBC design with shield (a) bottom view of shield layer (b) shield current density (c) side view of magnetic field (d) top view of magnetic field

The DBC designs, despite improvements in shield design, still had larger inductance than the PCB design; the increased distance between the shield and power loop of the DBC module led to the increase the parasitic inductance. Thinner 10 mil DBC alumina substrates have been introduced since the work in this section was completed [81], which can further improve DBC electrical performance. The lower inductance provided by the shielded DBC design reduced the switching losses; improving the efficiency over 1.5% and the efficiency curve for the generation 3 designs is shown in figure 4.32b. The DBC module with and external shield experienced a 1% drop in

efficiency compared to the PCB design. The small sacrifice in efficiency from the DBC module is justified by the significant gains in thermal performance, which is a major obstacle in high density modules.

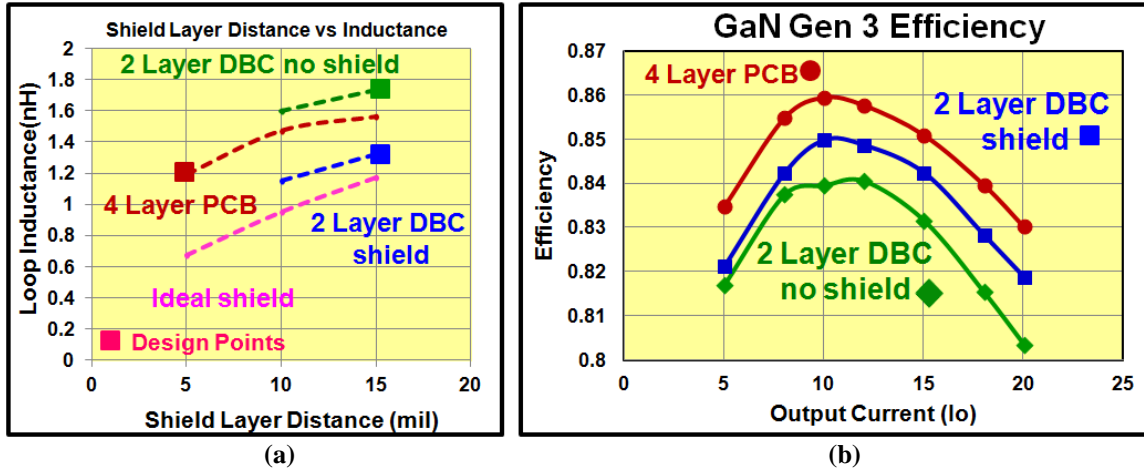


Figure 4.32: (a) Inductance vs distance between shield layer and power plane for different designs (b) Generation 3 PCB and DBC efficiency comparison

4.4.4 Generation 4 Shield Less DBC Module

The previous section discussed the importance of the shield design in a lateral power loop layout. The lateral power loop is defined as a power loop that is on a single layer with the current flowing parallel to the shield layer. The lateral power loop has benefits in that it can be placed on a single layer, minimize the total physical distance of the high frequency loop, and offer the shortest resistance connection between the power devices and the inductor. The main disadvantage of the lateral power loop is that it requires careful design of the shield layer to reduce parasitic inductance, as was demonstrated in the previous section. This section will propose the design of a module that can offer high efficiency while minimizing circuit parasitics without the use of a complicated shield layer.

With the lateral power loop requiring a shield layer to improve performance, the use of a second conductive layer is a requirement for all designs. With the option of

using a two layer design, more options can be explored to further improve performance. The concept presented in this section will be to use both layers for the power loop and have the power loop interleave on the two layers to offer self cancellation of fields. This will allow for the reduction of the inductance and eliminate the need for a shield plane.

The design of the fourth generation DBC module is shown in figure 4.33. The first change was replacing the LM5113 LLP packaged driver to a micro-SMD (usmd) bumped bare die to reduce footprint and improve driver thermal performance. The second change is the placement of the schottky diode; due to the vertical nature of the power loop, the ground of the input capacitor can be connected to the source of the SR through the bottom layer, allowing the schottky diode could be moved to the top side of the board in closer proximity to the SR than was possible with the third generation design, improving the effectiveness of the diode during dead time. The last change was the location of the inductor vias; which were moved above the devices as opposed to in the middle of the device pair. For the third generation design, moving the inductor vias above the devices would have increased the size of the power loop, increasing the parasitic inductance and footprint, decreasing the power density.

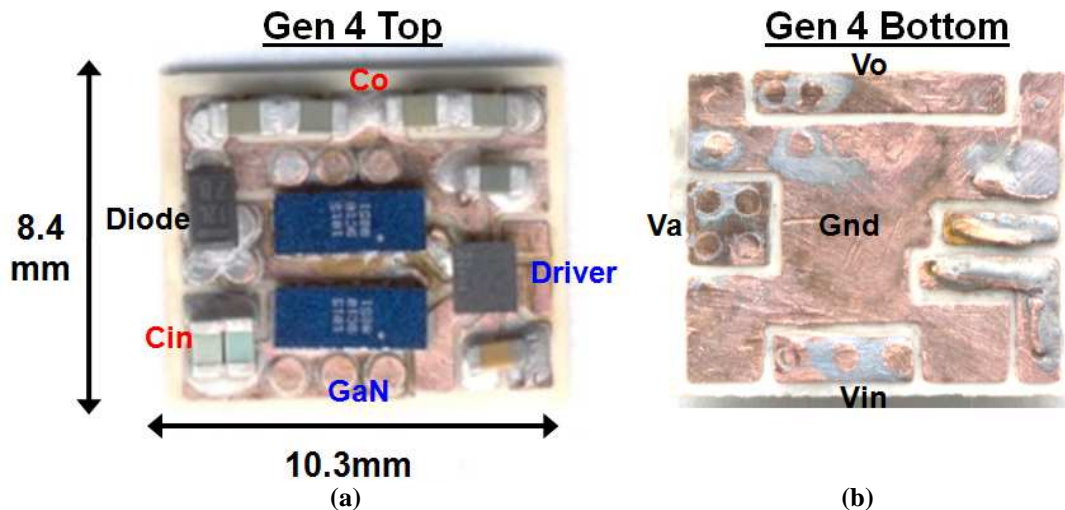


Figure 4.33: Generation 4 DBC hardware (a) Top layer view (b) Bottom layer view

The high frequency power loop for generation 4 is considered to be a vertical power loop as it is routed on both the top and bottom layers and is shown in figure 4.34. To allow for the inductor to be integrated to the bottom substrate, the bottom layer must remain flat and no components may be contained on the bottom layer. The power loop begins on the top layer at the ground terminal of the input capacitors; two 16V 0603 4.7uF capacitors are used in parallel to minimize parasitic inductance. The positive terminal of the input capacitors is placed in close proximity to the drain of the top side device to minimize loop distance. The top and SR device and placed side by side, and then the source of the SR are connected to ground vias. From the source of the SR the power loop flows vertically to the bottom layer containing the ground plane. The ground plane is routed directly underneath the top power loop to allow for self cancellation of the power loop. The high frequency loop is completed when the power loop returns to the top layer through vias underneath the negative terminal of the input capacitor.

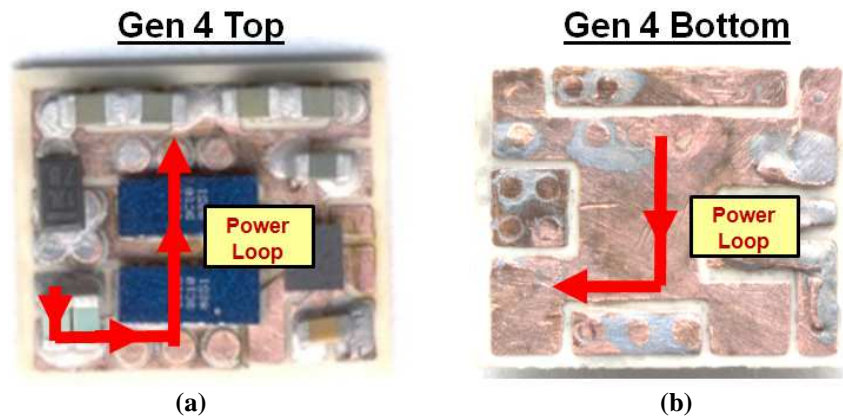


Figure 4.34: Generation 4 DBC Power Loop (a) Top layer view (b) Bottom layer

The performance of the vertical power loop in the fourth generation design can be seen in figure 4.35. The current distribution on the bottom layer, shown in figure 4.31b, displays good current distribution. Minor crowding occurs by the input capacitor ground vias, but overall, good field cancellation can be achieved. This is an improvement over

the lateral loop cases that had severe current crowding around the inductor via connections. The self cancelling power loop and better current distribution results in lower magnetic field intensity, as shown in figure 4.31 c&d, reducing parasitic inductance. From the field intensity plots it can be seen that there is still a large amount of energy stored in the substrate layer; this indicates that reduced substrate thickness can further improve the performance in the generation 4 design.

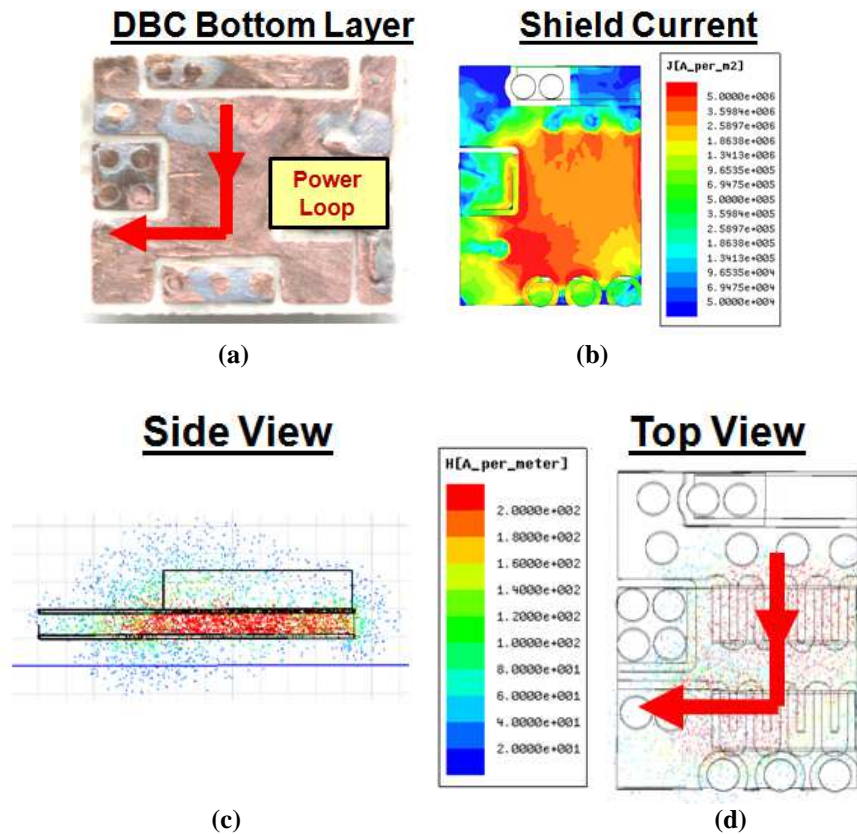


Figure 4.35: Generation 4 15 mil separation distance DBC design (a) bottom layer (b) bottom layer current density (c) side view of magnetic field (d) top view of magnetic field

The inductance breakdown for the fourth generation design is shown in figure 4.36. As was the case for generation 3, the majority of the total inductance was from the leakage and only for small substrate thicknesses was the trace inductance a major contributor to the total inductance. From the removal of the shield layer the winding

inductance was reduced almost a factor of two; and with the improved field cancellation, the leakage inductance is reduced by almost a factor of three.

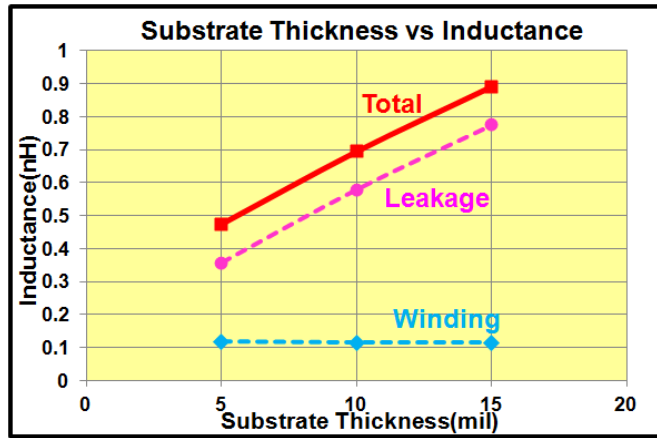


Figure 4.36: Inductance breakdown for generation 4 inductance vs substrate thickness

The inductance comparisons for the third and fourth generation designs are shown in figure 4.37, with the actual design points noted by a square symbol. The fourth generation design, through the use of a self cancelling power loop, was able to reduce the loop inductance over the best generation 3 DBC design by over 30%, reduce mechanical complexity, and reduce cost by eliminating the need for a shield layer.

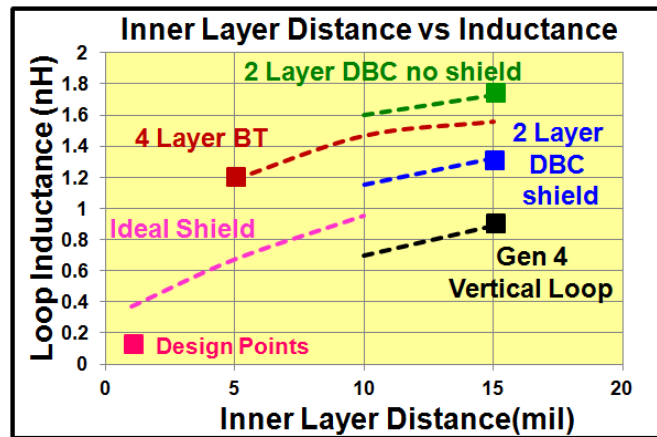


Figure 4.37: Loop inductance for generations 3 and 4 designs

The four generations of GaN converter designs are compared in table 4.6. For generations 1 through 3, a lateral power loop was utilized, and the power loop inductance was very dependent upon the size of the power loop as well as the shield design. The

drawback of these lateral power loops is that they required a complete shield layer underneath the power loop; this was not possible in actual layout do to physical space limitations, driver connections, and inductor connections. For the fourth generation, a self cancelling power loop design was proposed to minimize the parasitics while removing the need for an external shield layer. The fourth generation design slightly increased the physical distance of the power loop, but from improved cancellation, offered a significant reduction in loop parasitics.

	Generation 1	Generation 2	Generation 3	Generation 4
Board Footprint	840mm ²	570mm ²	154mm ²	86.5mm ²
Power Loop Size	46mm	31mm	18mm	20mm
Loop Inductance	6.30nH	2.90nH	1.19nH	0.89nH

Table 4.6: Parasitic loop inductances for generations 1, 2, 3, and 4 designs

The efficiency comparison of the DBC modules considered in this work is shown in figure 4.38. The generation 4 design offered a 0.8% peak efficiency gain over the shielded DBC generation 3 module; resulting from lower switching parasitics. The generation 4 converter and shielded generation 3 design matched efficiency at 15A. To summarize the performance of the fourth generation module: the power density was increased 80%, the shield layer was removed, and the peak efficiency increased 0.8%.

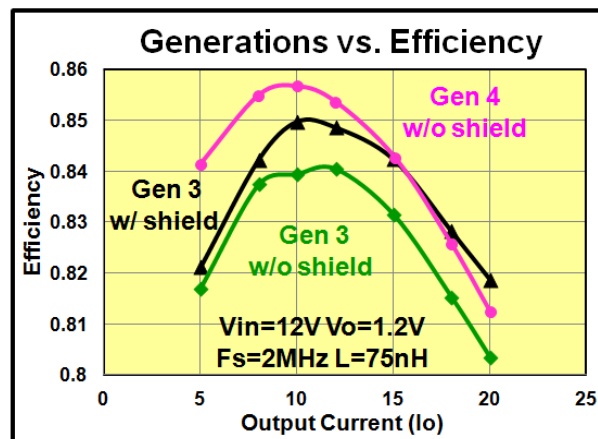


Figure 4.38: DBC module efficiency comparison (Top device:EPC1015 SR:EPC1015 Driver:LM5113)

Generation 4 experienced a drop in efficiency at heavy loads, in particular above 15A. This efficiency drop is related to the layout resistance, in particular the SR current loop shown in figure 4.32. The standard 12V POL modules generally operate at very small duty cycles, often around 10%. During the larger off state period, the current is conducted through the synchronous rectifier to the load. Minimizing the resistance of this high current trace is critical for higher current designs.

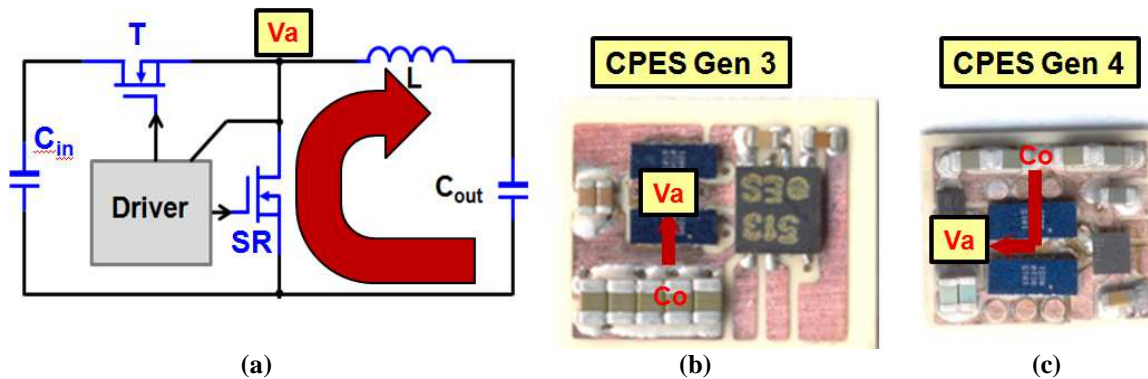


Figure 4.39: Synchronous rectifier conduction loop (a) Electrical diagram (b) Generation 3 (c) Generation 4

For the third generation design, the inductor vias were placed in between the devices, and the SR ground connection was kept very short to minimize the conduction loss during the freewheeling period. The location of the vias in the middle of the devices interrupted the shield plane, resulting in higher parasitic inductance and switching loss. For the generation 4 design, the inductor connection was moved to allow the power loop to be routed to achieve better field cancellation, reducing inductance and switching loss but increasing conduction loss.

The synchronous rectifier conduction loop was simulated using Maxwell 3D FEA to determine the trace resistance and observe the current distribution in the inductor connection vias. The FEA analysis of the AC resistance is derived from the power dissipation perspective.

$$I = \int_S \mathbf{J} \cdot d\mathbf{S} \quad (4.15)$$

$$V = \int_L \frac{\mathbf{J}}{\sigma} \cdot d\mathbf{L} \quad (4.16)$$

$$P = I_{RMS} \cdot V_{RMS} = I_{RMS}^2 R_{AC} = \frac{1}{2} \cdot I_{Peak}^2 \cdot R_{AC} \quad (4.17)$$

which yields the value for AC resistance:

$$R_{AC} = \frac{1}{I^2} \iiint_V \frac{\mathbf{J} \cdot \mathbf{J}^*}{\sigma} dV \quad (4.18)$$

The current density plots, performed at 2MHz, for the vias are shown in figure 4.40. For the third generation design, the current flows directly from the SR to the inductor vias and the current is evenly distributed between the four inductor vias. The skin effect of the vias limits the current to the inner portion of the via; reduction in via size could not be achieved in DBC because of fabrication limitations.

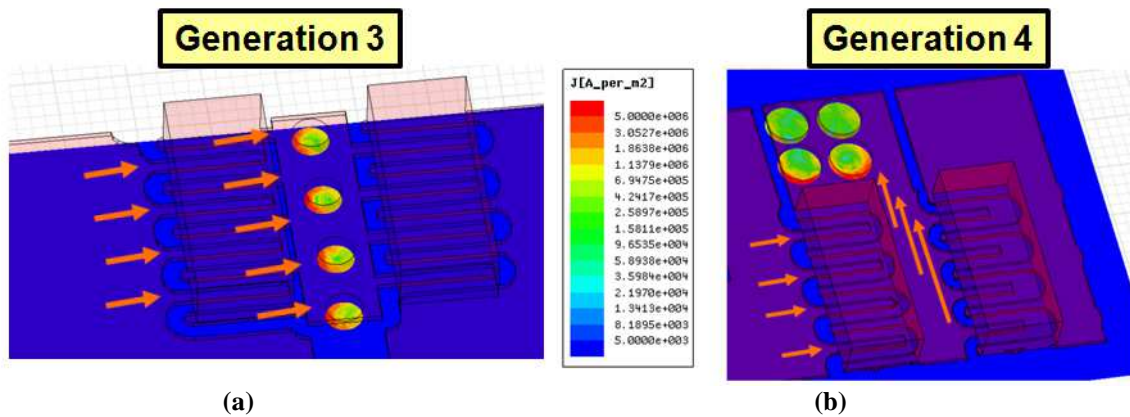


Figure 4.40: inductor connection via current distribution for (a) Generation 3 (b) Generation 4

For the fourth generation design the four vias were moved above the SR and the current flowed from the SR to a copper trace connecting to the inductor vias. This design resulted in higher resistance because of the current going through the small copper trace and the uneven current distribution inside the vias. The current crowds inside the edge of

the first two vias and the back set of vias sees much less current as is shown in figure 4.40b. The result is a small increase in trace resistance; this results in a drop in heavy load efficiency as was encountered in the fourth generation design.

	DC (mΩ)	1MHz (mΩ)	2MHz (mΩ)
Generation 3	0.57	1.04	1.23
Generation 4	0.63	1.39	1.68

Table 4.7: Synchronous rectifier conduction loop resistances

Lastly, the thermal performance of the fourth generation module was assessed. The fourth generation module had a 45% reduction in footprint from the third generation design, further challenging the thermal demands. The peak device temperature vs power loss measurements for the third and fourth generations are shown in figure 4.41. The temperature rise of the fourth generation increased more rapidly than generation 3, resulting in lower power handling capability, and limiting maximum load current to 15A. The measurements were for a standalone module, and thermal improvements will be achieved when mounted to a motherboard. With the GaN being the tallest component on the board, the GaN devices in the generation 4 module, when mounted active side down, could transfer heat directly to the motherboard. This would provide a double sided cooling effect, showing another potential benefit of the GaN package.

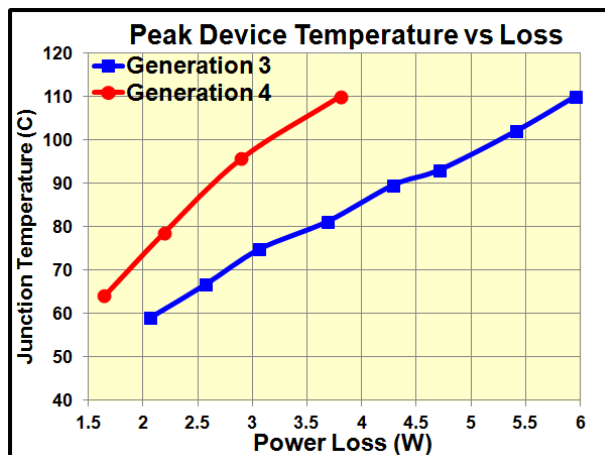


Figure 4.41: Device temperature vs power loss for generation 3 and 4 DBC designs at natural convection $V_{in}=12V$, $V_o=1.2V$, $F_s=2MHz$

4.5 Conclusions

This chapter explored the optimization of a high frequency, high current, high density 3D integrated GaN based point of load module. The impact of parasitics on switching loss was quantified; exploring the contributions of the common source and high frequency loop inductance on switching loss. With the improvements of the GaN device packaging reducing the package parasitics, in particular the common source inductance, layout of the module becomes the major barrier to higher efficiencies and frequencies. Reduction of the high frequency power loop size can offer significant inductance improvements and provide a smaller design footprint.

As power density is increased in the module, the thermal design becomes a critical aspect to consider and is often the bottleneck in maximum power. The use of highly thermal conductive alumina DBC substrates to improve thermal performance with better heat distribution was demonstrated, improving power handling capability by 50% over the traditional PCB which is prone to hot spots.

The impact of switching from a traditional multi-layer PCB to a two layer DBC has major implications on the module design to achieve good electrical performance. The impact of the shield plane on electrical performance was quantified, showing the effect of shield completeness and distance from power loop on parasitic inductance and circuit efficiency. The proper shield plane design was implemented in DBC to improve electrical performance. Lastly, an improved vertical power loop structure was proposed to eliminate the need for a shield layer and improve performance by providing a self cancelling power loop.

The final demonstration was a $900\text{W}/\text{in}^3$, $V_{\text{in}}=12\text{V}$, $V_{\text{o}}=1.2\text{V}$, $F_{\text{s}}=2\text{MHz}$, $I_{\text{o}}=15\text{A}$ Alumina DBC GaN converter which offers unmatched power density compared to state of the art industry products and research. Figure 4.41 shows the power density map of the current products and the DBC designs. The fourth generation design achieves a three times improvement in power density over similar products.

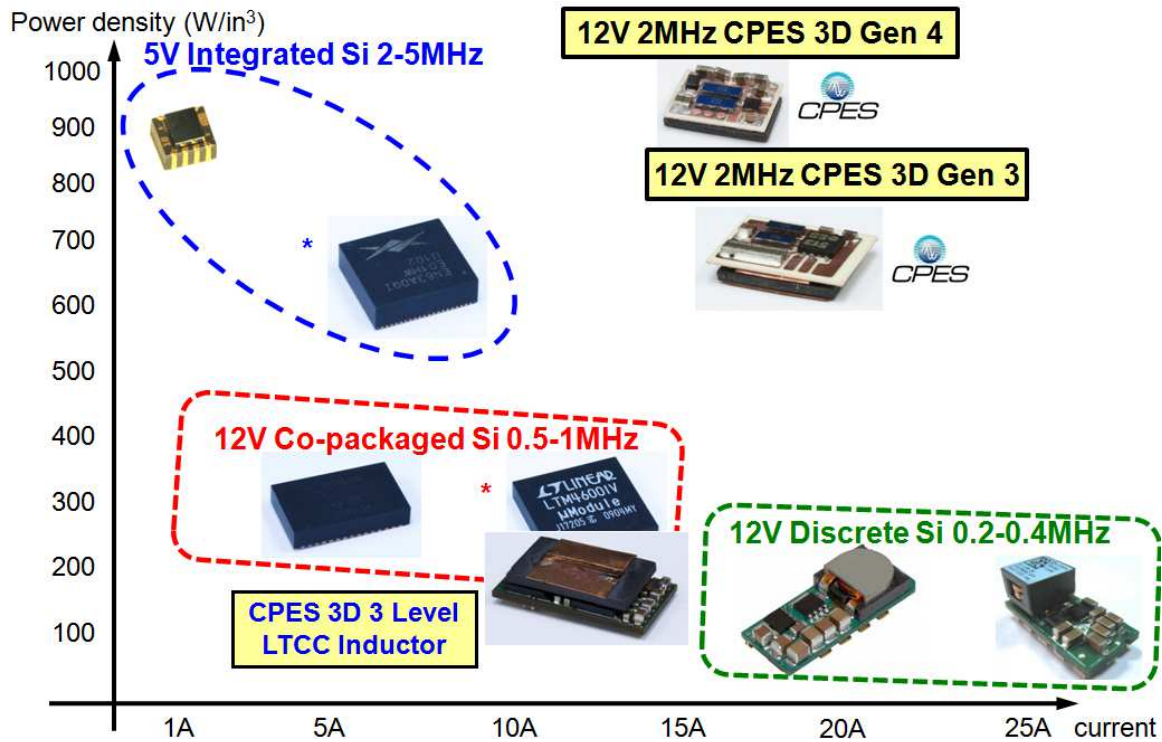


Figure 4.42: Power density comparison of state of the art power modules. *: Picture taken by author.

Chapter 5

High Density Isolated Bus Converter with Integrated Matrix Transformers

5.1 Introduction

Intermediate bus architecture (IBA) is gaining popularity in CPU and telecom applications [87][88][89] to replace the traditional distributed power architecture discussed in chapter 1 and shown in figure 5.1a. The IBA employs an isolated first stage to convert a nominal 48V input to the range of 8-12V. The second stage contains a series of small, high efficiency point of load converters like those discussed in chapters 2 and 4 to regulate the second stage voltage to the final output. The IBA approach can greatly reduce complexity and cost while improving performance.

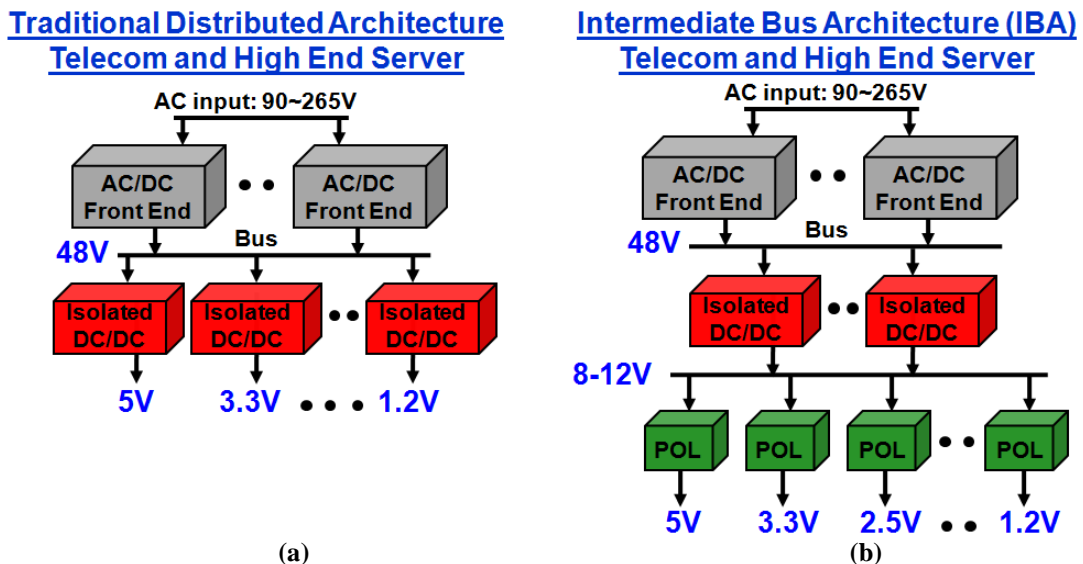


Figure 5.1: (a) Traditional Distributed Power Architecture (b) Intermediate Bus Distributed Power Architecture

The isolated first stage in IBA's generally employs an unregulated bus converter, also known as a DCX, or DC transformer, operated at 50% duty cycle to offer the highest

efficiency and power density. The majority of today's bus converters use traditional hard switching bridge topologies operating at lower frequencies to maximize efficiency [90][91]. The ZVS phase shift full bridge is commonly used for higher frequencies and higher power designs. It offers the ability to provide ZVS for the full bridge switches, utilizing the energy in the leakage inductance. The leakage inductance provides ZVS but also causes duty cycle loss and body diode loss. The leakage inductance also causes large transient spikes, as seen in figure 5.2a, that require the designer to use higher voltage synchronous rectifiers which further lead to higher losses [92].

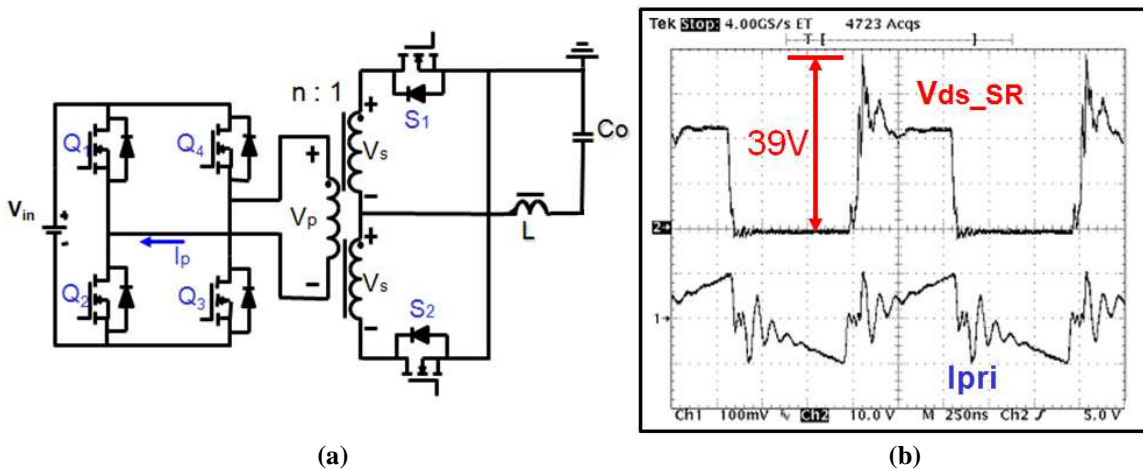


Figure 5.2: (a) Conventional full bridge converter with center tapped rectifier (b) Operational waveforms for synchronous rectifier voltage and primary current

At lower switching frequencies, the isolation transformer and output inductor are very bulky, occupying a large board area as can be seen in figure 5.3a. In an effort to improve power density, frequency can be increased to shrink the inductor and transformer size. As frequency is increased the body diode conduction, reverse recovery, and turn off losses of the converter increase significantly as can be seen in figure 5.3b. At 800 kHz, the reverse recovery and turn off loss contribute over 15W of loss, surpassing the total converter loss at 150 kHz [93]. To be able to pursue higher switching frequencies an improved topology must be utilized to reduce these losses.

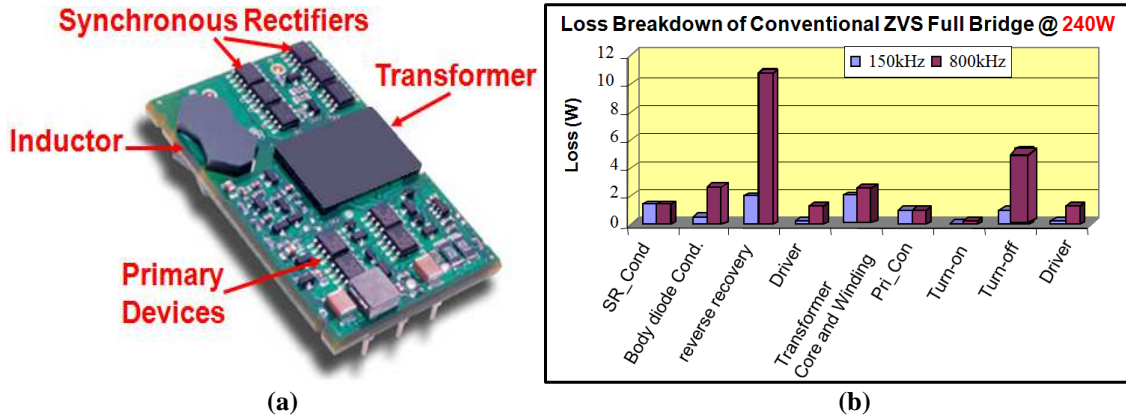


Figure 5.3: (a) Typical Low frequency unregulated bus converter module (b) Loss breakdown for ZVS full bridge at $V_{in}=48V$, $V_o=12V$, $I_o=20$ for frequencies 150 and 800kHz [93]

New topologies [92]-[94], like those shown in figure 5.4 a&b can reduce switching loss and ringing issues by using a resonant technique that utilizes the transformer's magnetizing inductance and resonance of the leakage inductance with a small capacitance to achieve ZVS, limit turn off current, and eliminate body diode conduction. These improved topologies allow for high efficiency at high switching frequency. Due to the resonant nature of the current in these designs another major benefit is introduced, the removal of the filter inductance.

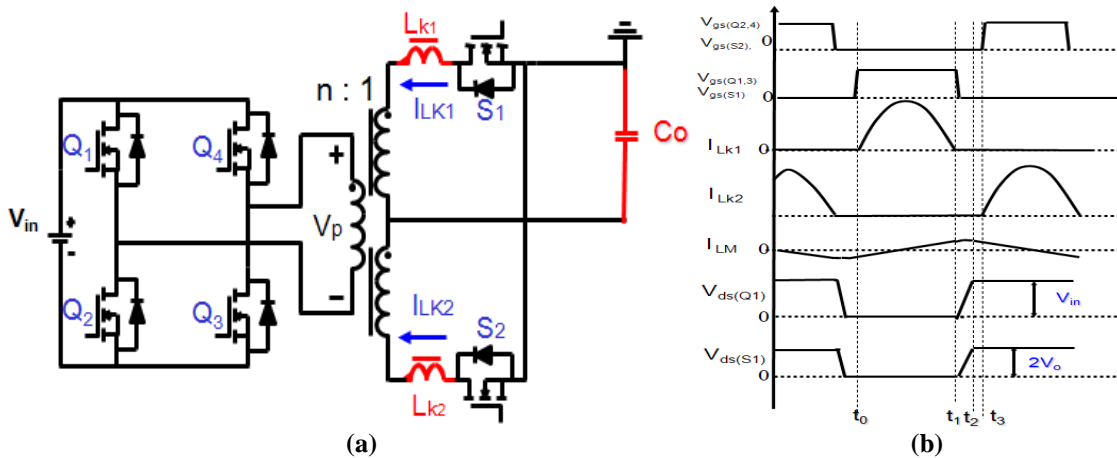


Figure 5.4: (a) Inductor Less Full Bridge Converter (b) Operating Waveforms

The improved resonant topologies can provide higher efficiency at higher switching frequencies by providing ZVS for all devices, ZCS for the secondary devices,

and almost ZCS for the primary devices. For the primary devices, they turn off with just the magnetizing current. With the soft switching bus converter, the losses become lower than a traditional topology operated at lower switching frequencies, as shown in figure 5.5, and the major loss barrier now becomes the transformer.

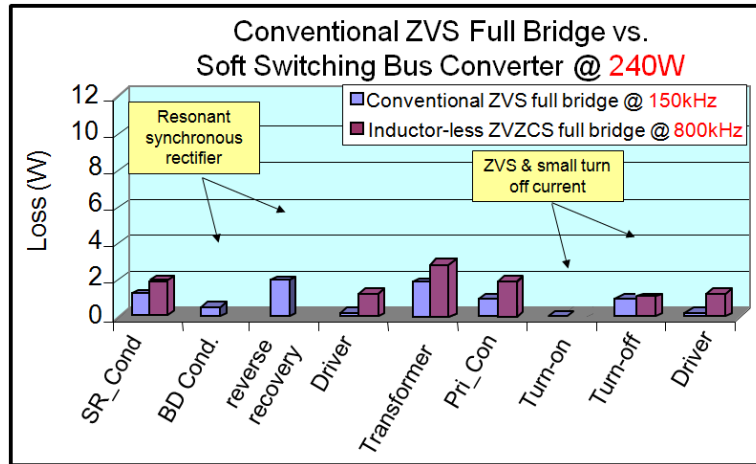


Figure 5.5: Loss breakdown of 150kHz ZVS full bridge and 800kHz soft switching bus converter [93]

The challenges of high frequency transformer design are minimizing winding loss, termination loss, and leakage inductance while reducing core volume and loss. This chapter will explore the transformer design in depth and explore the use of distributed matrix transformers to improve performance by reducing leakage inductance and winding resistance. This work will also propose an integrated matrix transformer structure that can reduce core loss while offering low leakage and winding resistance, providing a high efficiency, high density transformer structure.

5.2 High Frequency Transformer Design

5.2.1 Impact of High Frequency on Transformer Size

The goal of higher frequencies is to reduce passive size and improve power density. It is known that increased frequencies in non-isolated applications can decrease filter inductance and capacitance as was demonstrated in the earlier chapters. For the

high frequency isolated soft switching topology used in this work, the LC output filter is replaced by a small resonant network that utilizes the transformers leakage inductance for the inductor. This greatly reduces the size of the filter passives. For the high frequency design the bulkiest component is the transformer which occupies around 40% of the converter volume. The impact of increased frequency on the size of the transformer in high frequency isolated converters is considered in this section.

The traditional method to evaluate core loss uses the Steinmetz equation [95], given as:

$$P_{cv_stein} = k \cdot f_s^\alpha \cdot \hat{B}^\beta \quad (5.1)$$

Where P_{cv_stein} represents the core loss per unit volume, f_s is the switching frequency, B is the peak flux density, and k , α and β are determined by curve fitting measured loss data supplied by magnetic material manufacturers.

The Steinmetz parameters given by core manufacturers are for a sinusoidal excitation. Much research has been done to consider the impact of non-sinusoidal excitations [96]-[98]. For this work, the transformer is excited with a square pulse having a duty cycle close to 50%. The resulting flux inside the transformer is a triangular shaped wave with close to a 50% duty cycle. Based off of the results from [96] the k factors will be multiplied by a factor of 0.85 to represent the core loss in this design case.

From faradays law the change in flux density can be determined by:

$$\Delta B = \frac{D \cdot V_{in}}{2 \cdot N_p \cdot A_e \cdot f_s} \quad (5.2)$$

Where D is the duty cycle, V_{in} is the input voltage, N_p is the number of primary winding turns, A_e is the cross sectional area of the core, and F_s is the switching frequency.

Inserting equation (5.2) into equation (5.1) and multiplying by the core volume yields total core loss:

$$P_c = V_e \cdot k \cdot f_s^\alpha \cdot \left(\frac{D \cdot V_{in}}{2 \cdot N_p \cdot A_e \cdot f_s} \right)^\beta \quad (5.3)$$

This gives the core loss in terms of circuit parameters D and V_{in} , core material parameters k , α , and β , design dependant quantities f_s and N_p , and core dependant quantities A_e and V_e .

The loss coefficients for the manganese zinc (Mn-Zn) materials considered in this work were curve fit from manufacturer's data sheets at a temperature of 100°C and obtained from [99] and are shown in table 5.1. As the individual ferrite materials are pushed higher in frequency, the α component rises. When the α coefficient for a given material becomes larger than the beta coefficient the material can no longer reduce size with increased frequency.

Ferrite	Frequency Range (kHz)	k	α	β
3c96	200-500	4.60×10^{-9}	2.50	2.75
3f3	200-400	2.20×10^{-6}	2.00	2.60
3f3	400-700	6.50×10^{-9}	2.42	2.45
3f35	500-1000	9.00×10^{-12}	2.95	2.94
3f4	400-1000	5.80×10^{-5}	1.80	2.90
3f45	500-1000	2.00×10^{-2}	1.29	2.75
3f45	1000-2000	3.00×10^{-12}	2.9	2.6
3f5	1000-2000	4.10×10^{-7}	2	2.4

Table 5.1: Core loss Steinmetz constants

An assumption used in this method is that the core volume is related to the cross sectional area for a given transformer series. The relationship between A_e and V_e can be found by curve fitting common core shapes into the resulting equation:

$$V_e = y \cdot A_e^C \quad (5.4)$$

Where y and C are constants determined by the core geometry used. Shown in figure 5.6 are the plots for core volume vs cross sectional area for planer EQ, EE, and EIR cores. Table 5.2 contains the corresponding values for y and c . Note the core volume is given for two cores.

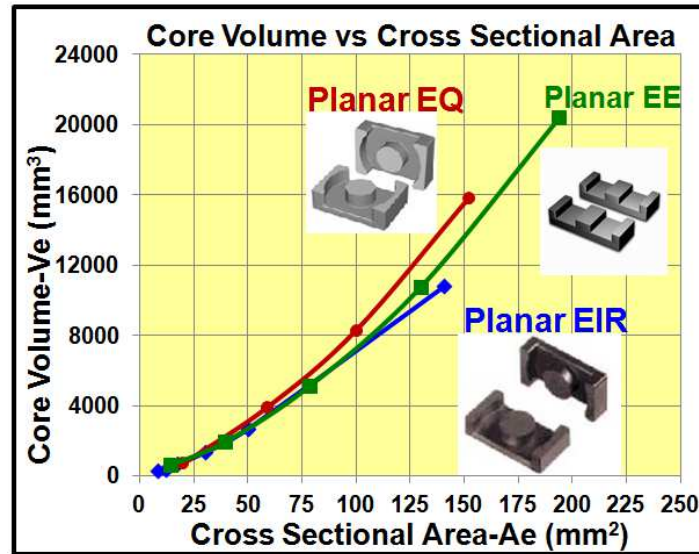


Figure 5.6: Core volume vs cross sectional area for EQ, EE, and EIR planar transformer cores

Core Series	y	C
Planar EQ	7.2326	1.5329
Planar EE	14.432	1.3600
Planar EIR	12.690	1.3651

Table 5.2: Core volume to cross-sectional area constants

Having determined the relationship of cross sectional area to core volume the impact of frequency on core volume can be determined by inserting equation (5.4) into equation (5.3) and solving for core volume. The end result is:

$$V_e = y \cdot \left[\left(\frac{P_{core}}{y \cdot k} \right)^{\frac{1}{C-\beta}} \cdot f_s^{\frac{\beta-\alpha}{C-\beta}} \cdot \left(\frac{D \cdot V_{in}}{2 \cdot N_p} \right)^{\frac{-\beta}{C-\beta}} \right]^C \quad (5.5)$$

With equation 5.5 the impact of frequency on core size can be solved for a given core loss, circuit parameters, core series, and core material. For this case, the core loss is selected to be 2W, the input voltage is 48V, the duty cycle is 0.5, the turns ratio of the

transformer is 4:1, and the core is a planar EIR core. Shown in figure 5.7 is the core volume vs frequency plot for the design case with different Mn-Zn materials.

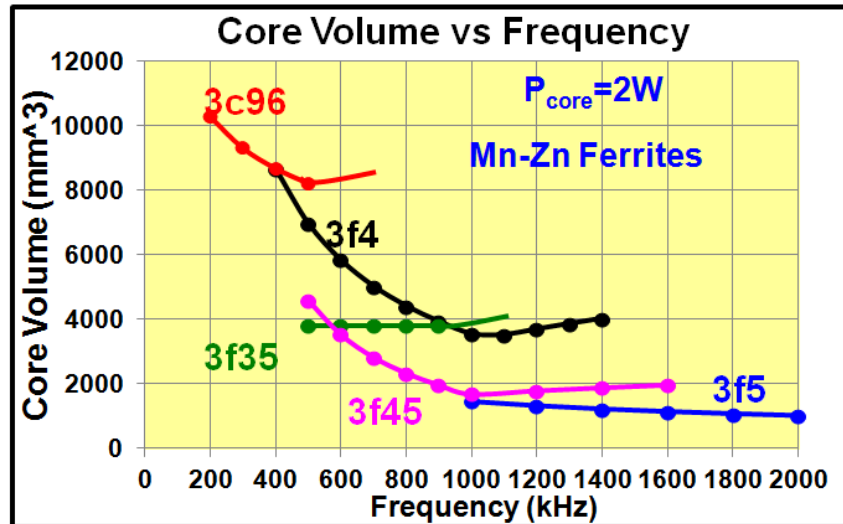


Figure 5.7: Core volume vs frequency for EIR planar transformer for $P_{core}=2W$, $V_{in}=48V$, $V_o=12V$, and $D=0.5$

As frequency is increased the size of the transformer core can be further decreased for this application. The new magnetic materials such as 3f35 and 3f45 can help decrease core loss at the higher frequencies. For this work, the target switching frequency is between 1-2MHz to offer a tradeoff of small magnetic size and high efficiency.

5.2.2 Limitations of Traditional Transformer at High Frequency

Increasing switching frequency can reduce transformer size but will introduce high frequency effects to the windings. The traditional transformer design used at higher frequencies will suffer from large winding resistance as a result of eddy current and proximity effects. As frequency increases, the current will crowd around the edges of the winding, making the use of a traditional transformer ineffective for high current designs. Also at higher frequencies, the termination of the transformer contributes significantly to

leakage inductance and resistance. In this section, these issues will be considered for a high frequency transformer.

To study the impact of frequency on transformer leakage inductance and winding resistance Maxwell 3D FEA simulations were used. The simulation method is discussed in detail in chapter 4. A commonly used core in DCX applications, a planar EIR 22, is considered. The transformer has a four turn primary winding and a single turn center tapped secondary winding, as shown in figure 5.8a. The PCB is a twelve layer, two ounce pcb with four layers for the primary, each containing a single turn and four parallel layers for each secondary. The FEA model and winding arrangement are shown in figures 5.8 b-e. The winding structure is interleaved to minimize leakage inductance and proximity effects.

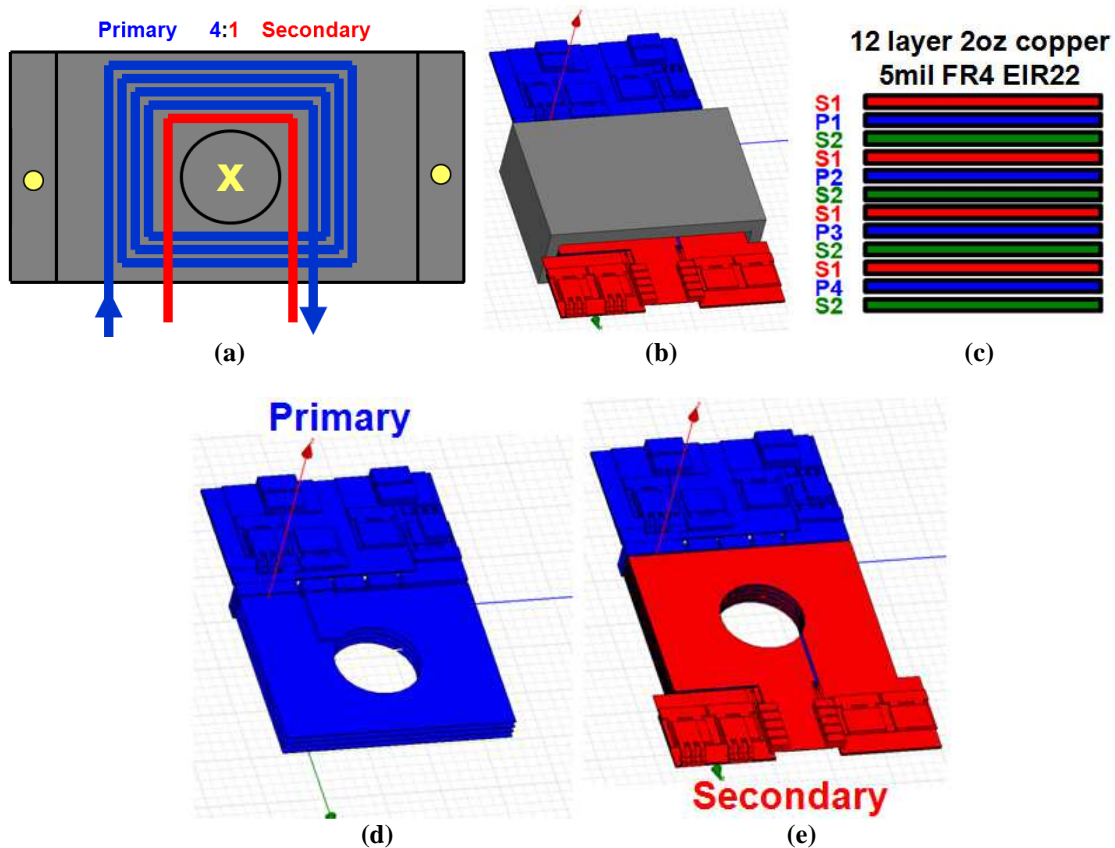


Figure 5.8: EIR22 transformer (a) Structure (b) FEA model (c) Winding Arrangement (d) Primary winding and termination loop (e) Secondary winding and termination loop

For the transformer design, the terminations can introduce large resistance and leakage inductance [100]. At higher frequencies and smaller transformer sizes, the design of the terminations is critical to an efficient design. To accurately model the transformer structure the termination must be modeled accurately as is shown in figure 5.8. For [93], the transformer loss was simplified using DC resistance values of the windings and neglected the termination effects. For the high frequency resonant converters, the current is sinusoidal in nature and AC effects can't be neglected.

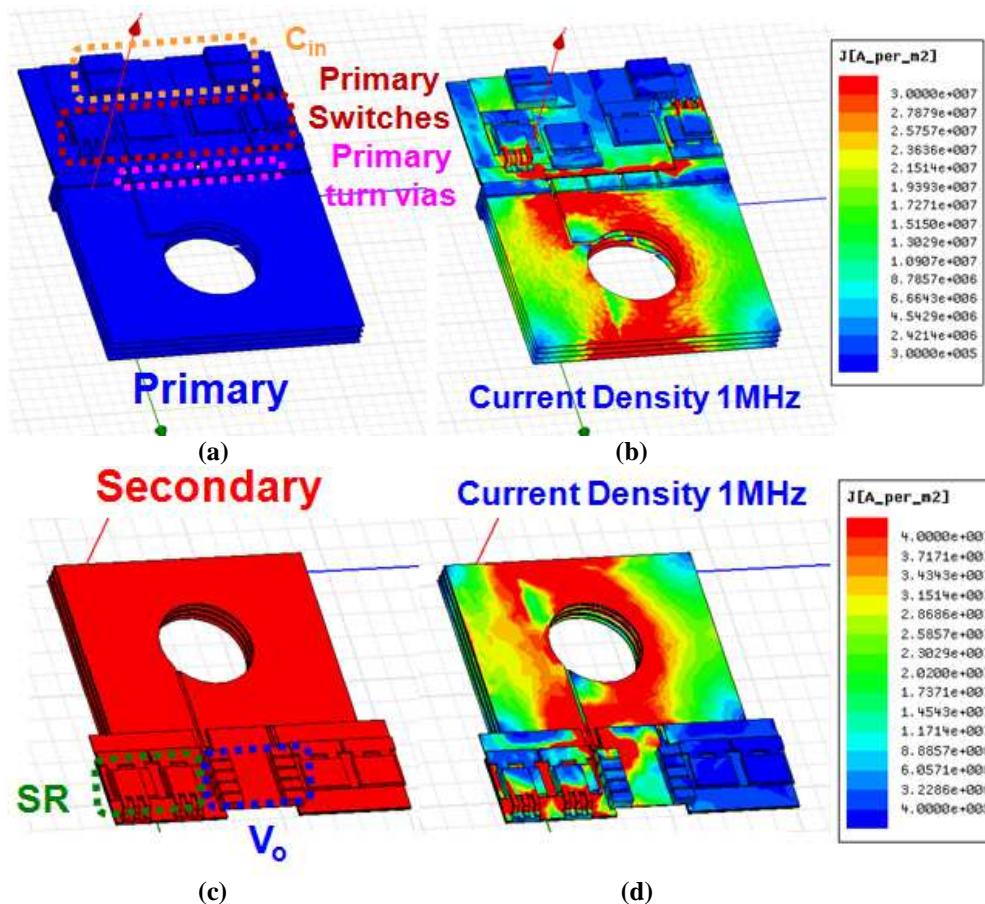


Figure 5.9: EIR22 transformer (a) Primary winding (b) Primary winding current density at 1MHz (c) Secondary winding (d) Secondary winding current density at 1MHz

At high frequencies, the transformer will experience current crowding in the windings and in the terminations, increasing resistance, and transformer loss. Figure 5.9 shows the primary and secondary windings of the traditional transformer design and their

current distributions at 1MHz. The traditional transformer suffers from severe current crowding in the inner portion of the transformer and the areas where good interleaving is not achieved; in particular the terminations and around the primary turns vias. To evaluate conduction loss, the RMS currents for the primary and secondary windings must be determined. The current for the secondary resonant network under ideal conditions is sinusoidal at the optimal frequency and given by:

$$i_{Lk}(t) = I_o - I_o \cos(\omega \cdot t) + \frac{V_{in} - V_{co}}{N_p Z_o} \cdot \sin(\omega \cdot t) \quad (5.6)$$

where I_o is the output current, V_{in} is the input voltage, $\omega = \frac{1}{\sqrt{L_k \cdot C_o}}$, N_p is the turns ratio of the transformer, $Z_o = \sqrt{\frac{L_k}{C_o}}$, and V_{co} is the initial output capacitor voltage.

The RMS current for the secondary winding is given by:

$$i_{Lk_RMS} = \sqrt{\frac{1}{T_s} \int_0^{D \cdot T_s} (i_{Lk}(t))^2 dt} \quad (5.7)$$

With the converter operating at the resonant frequency, having a gain close to one, and a duty cycle close to 0.5, equation (5.6)-(5.7) can be simplified to:

$$i_{Lk_RMS} = \sqrt{\frac{1}{T_s} \int_0^{D \cdot T_s} (I_o - I_o \cos(\omega \cdot t))^2 dt} = I_o \sqrt{\frac{3}{4}} \quad (5.8)$$

The loss of the secondary windings can be found by:

$$P_{Sec} = i_{Lk_RMS}^2 \cdot 2 \cdot R_{Sec} \quad (5.9)$$

For the primary current, the magnetizing current will be ignored initially as it is significantly lower than the peak load currents. The rms current can be described as:

$$i_{pr_RMS} = \sqrt{\frac{2}{T_S} \int_0^{D \cdot T_s} \left(\frac{I_o - I_o \cos(\omega \cdot t)}{N_p} \right)^2 dt} = \frac{I_o}{N_p} \sqrt{\frac{3}{2}} \quad (5.10)$$

For the experimental designs later in the chapter, the magnetizing current will be considered, increasing the primary winding loss slightly.

Using the FEA simulation of the EIR22 transformer the impact of frequency on winding loss and leakage inductance can be studied. The impact of frequency and load current on winding loss is shown in figure 5.10; the conduction loss of the transformer increases 43% from 200kHz to 2MHz. With this transformer structure, at 1MHz and 40A the transformer conduction loss approaches 8W of loss. Generally, at higher current levels, the copper thickness is increased to minimize resistance; this approach is not possible at higher frequencies due to the skin effect of the transformer windings. The skin depth, given by 5.11, is 0.075mm at 1MHz for copper, or roughly 2 ounce copper.

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \quad (5.11)$$

where ρ is resistivity, and μ is the permeability, both for copper.

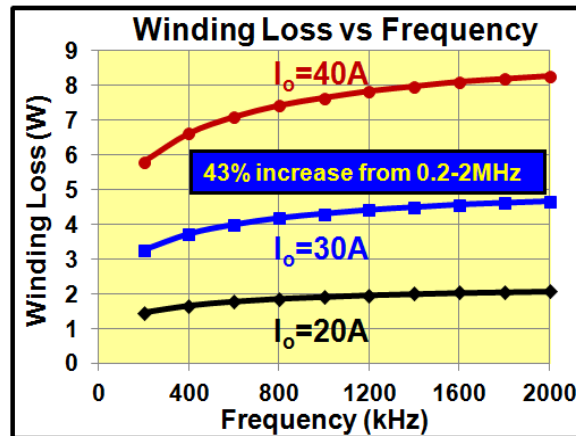


Figure 5.10: EIR22 transformer Winding loss from 200kHz to 2MHz for $I_o=20A, 30A, 40A$

The impact of frequency on leakage inductance is shown in figure 5.11; leakage inductance has much less dependence on frequency, with the inductance reducing 8%

from 200kHz to 2MHz and only 2% from 600kHz to 2MHz. At higher frequencies, minimizing leakage inductance maximizes power transfer and optimizes performance.

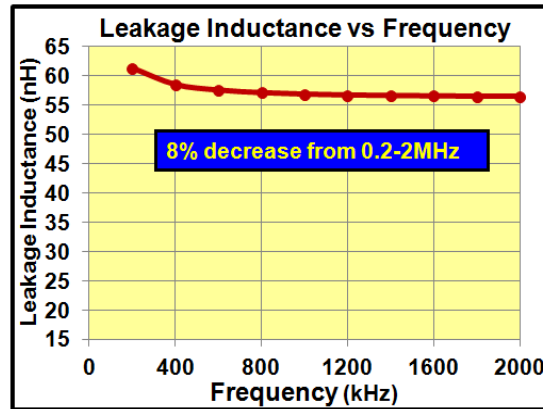


Figure 5.11: EIR22 transformer Leakage inductance from 200kHz to 2MHz

From the previous analysis, it becomes apparent that the transformer and its termination are major limitations to high efficiency at higher currents and higher frequencies. To study the impact of termination on performance, the transformer models were simulated without the termination loops. The leakage inductance plots in figure 5.12a&b show the field intensity plots for the transformer case with and without the terminations, respectively. The case with the complete design termination experiences major leakage in the termination areas: the primary winding connection vias, secondary SR's, and the secondary output connection.

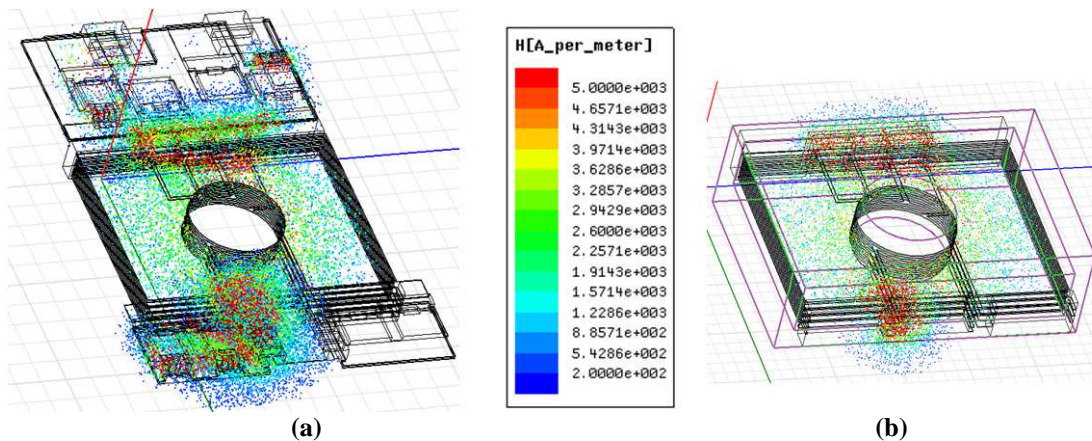


Figure 5.12: EIR22 transformer field intensity plot (a) with complete design termination (b) Simplified termination

From analyzing the current density and field intensity plots with the terminations, the termination of the transformer will contribute significant loss and leakage inductance to the design. Using FEA analysis, the loss in the primary and secondary windings was broken down to determine the loss in the transformer winding and the loss in the transformer terminations for the primary and secondary windings.

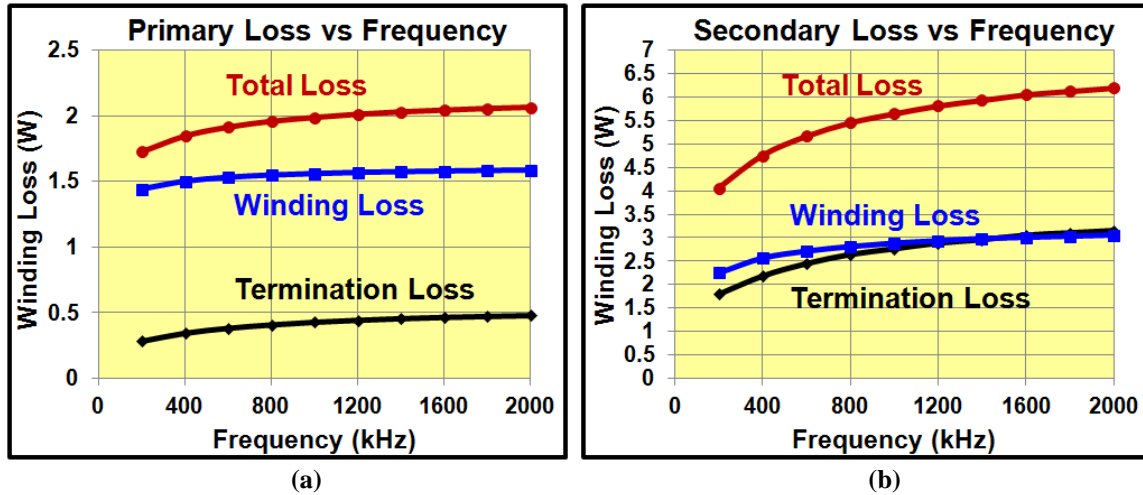


Figure 5.13: EIR22 transformer winding loss breakdown at $I_o=40A$ (a) Primary winding (b) Secondary winding

From the winding loss breakdown in figure 5.13a, the primary winding loss is due mostly to the winding; at 2MHz, the primary termination contributes 23% of the total loss. This is a result of a large resistance in the four layer primary winding connected in series. For the secondary winding, comprised of four parallel windings to reduce loss, the termination loss is significant, comprising 51% of the secondary loss at 2MHz. At higher frequencies, the termination becomes more critical due to its inability to achieve proper interleaving. The high termination loss in the secondary makes it the far lossier of the two windings and must be improved to improve performance.

The impact of termination on leakage inductance can be seen in figure 5.14. The termination contributes over 50% of the leakage inductance. For this design, the leakage

was minimized using techniques from [101]; even with an optimized design, the termination dominates the total inductance. Looking at field intensity plots in figure 5.12, it can be seen that the majority of the termination leakage results in the primary winding connection vias and the secondary connection point. For the primary and secondary device loops, the inductance was minimized using a shield plane as discussed in chapter 4. This helps minimize leakage inductance, and more importantly, the loop inductance, reducing switching loss if the converter.

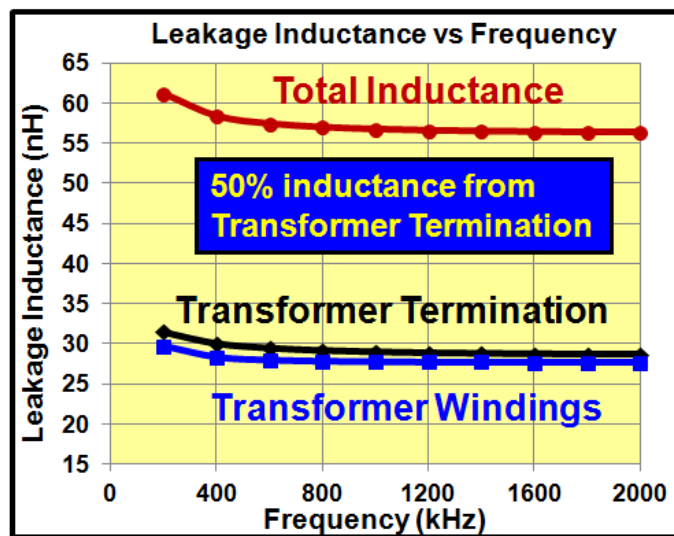


Figure 5.14: EIR22 transformer leakage inductance breakdown

To improve transformer performance at high frequencies, another approach to transformer design must be explored to reduce the frequency effects and minimize the termination effects which contribute significantly to winding loss and leakage inductance. Looking at the industry products today, [90][91][104], there is only one high frequency, high density module available, and it is limited to lower current. This section will explore methods to improve current handling capability of a high frequency transformer for a high density isolated 48V converter design. This chapter will also explore the use of GaN devices to further push frequency and improve converter power density.

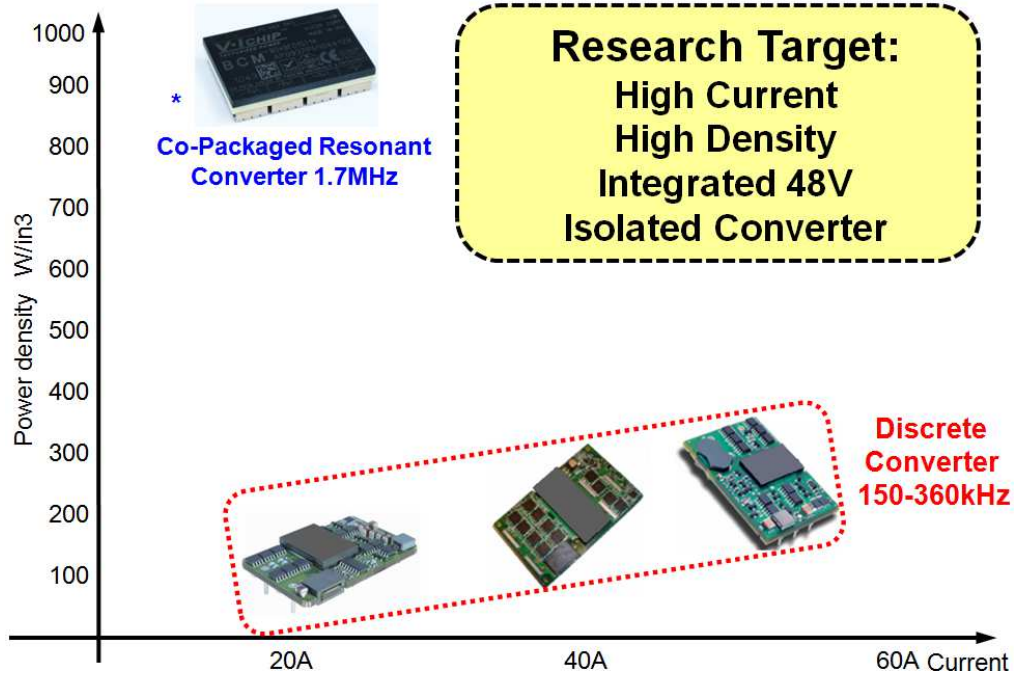


Figure 5.15: Power density comparison of $V_{in}=48V, V_o=12V$ discrete isolated bus converters. *: Picture by author

5.3 Matrix Transformers in High Frequency Designs

5.3.1 Basic Principles of Matrix Transformers

For high current applications, multiple devices are commonly used in parallel to limit the loss at high currents, as shown in figure 5.16. In the current DCX products, every design employs the paralleling of synchronous rectifiers in the high current output stage to reduce loss, with current designs ranging from two to four devices in parallel for each secondary. The conduction loss in the devices is given by:

$$P_{conduction} = \sum_{k=1}^N \left(\frac{I_{RMS}}{N} \right)^2 \cdot R_{ds_on} = \frac{I_{RMS}^2 \cdot R_{ds_on}}{N} \quad (5.12)$$

Where I_{RMS} is the total RMS current going through the switch network, N is the number of devices in parallel, and R_{ds_on} is the on state resistance of device. Increasing the

number of devices can reduce the loss by dividing up the high current; this also allows for the use of lower current devices and gives design scalability.

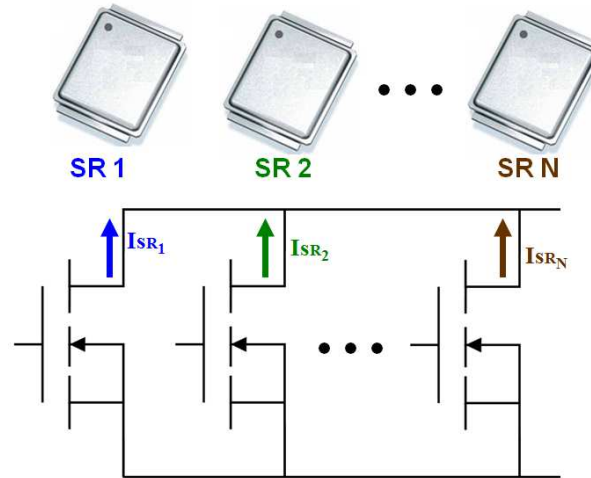


Figure 5.16: Multiple MOSFET devices in parallel configuration

The drawbacks of using multiple devices in parallel are that it adds footprint and increases driving losses. With the improvements of on resistance vs device area increasing rapidly and the push for high frequency, the driving loss becomes a major concern. The driving loss for the devices is given as:

$$P_{drive} = \sum_{k=1}^N Q_g \cdot V_{dr} \cdot f_s = N \cdot Q_g \cdot V_{dr} \cdot f_s \quad (5.13)$$

Where Q_g is the total gate charge of each device, N is the number of devices in parallel, V_{dr} is gate drive voltage, and f_s is the switching frequency. Increasing the number of devices increases the gate drive losses in the circuit. For high current designs, the conduction loss is much greater than the driving loss and the benefit of paralleling multiple devices is significant.

The matrix transformer employs a concept similar to the paralleling of devices to the transformer. This is done to reduce high frequency secondary winding loss; the basic concept is shown in figure 5.17. The matrix transformer is defined as an array of

elements interwired so that the whole functions as a single transformer [102][103]. An element being a single transformer that contains a set turns ratio, i.e. 1:1, 2:1 ...N:1; the secondary turns ratio is set to one for this work in an effort to reduce winding loss and push for high current.

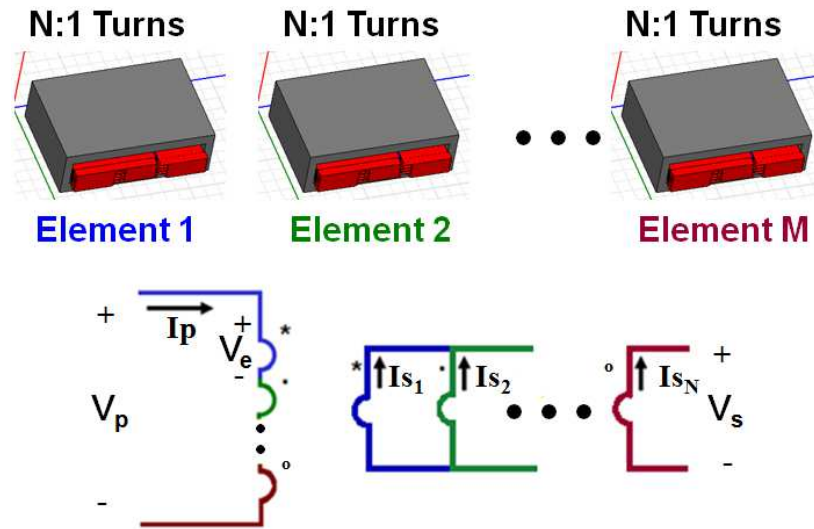


Figure 5.17: Matrix transformer element structure and electrical configuration

The desired turns ratio of the final transformer is obtained by connecting the primary windings of the elements in series and the secondary's in parallel.

$$N_p = \sum_{k=1}^M N_e = M \cdot N_e \quad (5.14)$$

Where N_p is the effective turns ratio of the final transformer structure, M is the number of transformer elements used, and N_e is the turns ratio for each element.

The voltage and current conversion of the matrix transformer follows the same principles as the traditional transformer design.

$$\frac{V_p}{V_s} = N_p \quad (5.15)$$

$$\frac{I_p}{I_{S_total}} = \frac{1}{N_p} \quad (5.16)$$

Where V_p is the total voltage across the primary elements, V_s is the voltage shared across the parallel secondary elements, I_p is the primary current, and I_{s_total} is the total current.

With the secondary elements connected in parallel, the primary windings share the voltage equally. With the primary windings connected in series, the secondary windings distribute current equally.

$$V_e = \frac{V_p}{M} \quad (5.17)$$

$$I_{s_e} = \frac{I_{s_total}}{M} \quad (5.18)$$

Where V_e is the primary voltage of each matrix element and I_{s_e} is the current in each secondary element.

For the secondary windings, the loss can be reduced due to the distribution of the high current in a similar manner as parallel devices and derived from equation (5.12).

$$P_{conduction_sec} = \sum_{k=1}^M \left(\frac{I_{RMS}}{M} \right)^2 \cdot 2 \cdot R_{sec} = \frac{I_{RMS}^2 \cdot 2 \cdot R_{sec}}{M} \quad (5.19)$$

From the previous analysis of the EIR 22 core with high secondary winding and termination loss, the matrix transformer structure could offer significant performance gains by reducing the total secondary conduction loss. While being able to reduce winding loss, the matrix transformer has similar frequency related loss drawbacks to the paralleling of active MOSFET devices; they are the increasing of core volume and core loss. The core loss of the matrix transformer can be found from:

$$P_{Matrix} = \sum_{k=1}^M P_{element} = M \cdot P_{element} \quad (5.20)$$

Where P_{matrix} is the total core loss of the matrix transformer structure and $P_{element}$ is the core loss in each element.

The flux excursion in each matrix element is the same as traditional transformer and can be found from:

$$\Delta B = \frac{D \cdot V_e}{2 \cdot N_e \cdot f_s \cdot A_e} = \frac{D \cdot V_{in}}{2 \cdot N_p \cdot f_s \cdot A_e} \quad (5.21)$$

Where D is the duty cycle, V_{in} is the input voltage, A_e is the cross sectional area of the core, and f_s is the switching frequency.

Increasing the number of transformer elements increases the core losses in the circuit. For low frequency, high current designs the size of the transformer is the largest component on the board and increasing the number of transformer elements to decrease conduction loss comes would introduce a large amount of core loss and significantly decrease power density with larger magnetic volume. At higher frequencies, the core size can be reduced significantly and the possibility of using matrix transformer can be considered. The benefits of the matrix transformer are that it can split current between secondary windings connected in parallel, reduce leakage inductance by lowering the N^2 value of the secondary loop inductance, and alleviate the termination effect by distributing the power loss throughout the elements.

5.3.2 Matrix Transformer Modeling

To be able to make a fair comparison between the different transformer designs, this section develops a method to model the matrix transformer so that the different transformer structures can be compared simply. For a 4:1 transformer design there are three possible matrix configurations to achieve the desired turns ratio and are shown in figures 5.18, a, b, and c. The different configurations can be simplified into an equivalent circuit, shown in figure 5.18d. By modeling the matrix transformers as a traditional single transformer with a single resistance and leakage inductance, the effective in circuit

values of the transformer can be easily determined. The equivalent resistance contains the DC and AC resistance information and the equivalent inductance contains the loop inductances of the primary, secondary, and the leakage generated in the transformer.

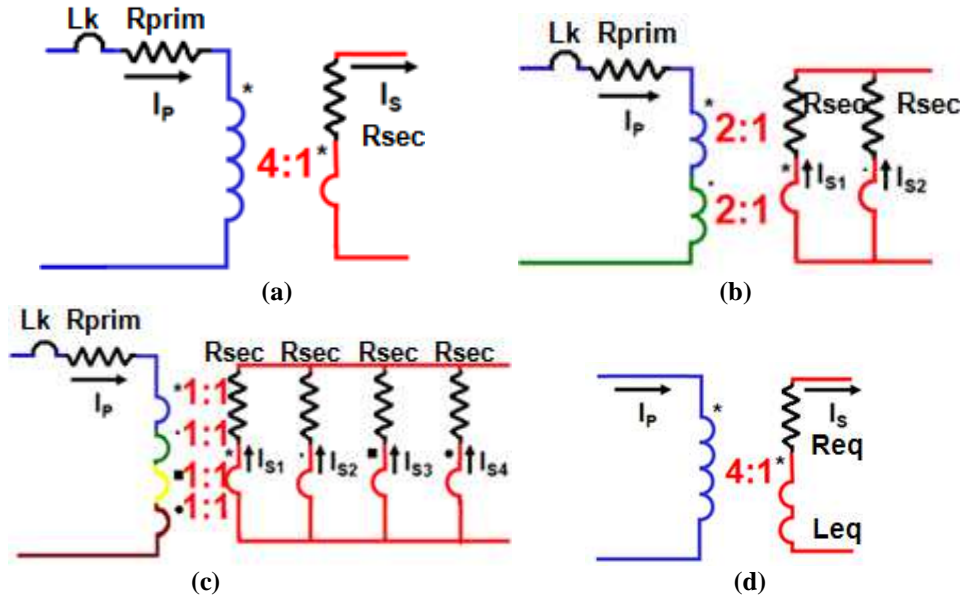


Figure 5.18: (a) Single 4:1 transformer (b) Two 2:1 matrix Transformer (c) Four 1:1 matrix transformer (d) Equivalent transformer model

The value for the equivalent resistance is based off winding conduction loss for the center tapped resonant structure. The equivalent leakage inductance is derived from the energy storage in the leakage inductance and both are derived below:

$$P_{\text{cond}} = I_{\text{PRMS}}^2 \left(R_{\text{prim}} + \frac{R_{\text{sec}} \cdot N_p^2}{M} \right) \rightarrow R_{\text{eq}} = \frac{1}{N^2} \left(R_{\text{prim}} + \frac{R_{\text{sec}} \cdot N_p^2}{M} \right) \quad (5.22)$$

$$W_L = \frac{1}{2} \cdot (L_k) \cdot I_p^2 \rightarrow L_{\text{eq}} = L_k \quad (5.23)$$

Where R_{prim} is the resistance of the primary winding, R_{sec} is the resistance of each secondary winding, M is the total number of transformers used, N_p is the turns ratio for the total transformer, and L_k is the lumped inductance seen on the primary side including transformer leakage, primary loop inductance, and secondary loop inductance.

5.3.3 Matrix Transformers in State of Art Designs

Previous research and products have employed the use of matrix transformers [92],[104] in high frequency bus converters but their designs have not been discussed in great detail. For the matrix transformer to be a viable option, the switching frequency of the converter must be high enough to allow for smaller transformer to be used. The designs employing matrix transformers have increased the operating frequency of the bus converter five to ten times the traditional design.

There is one high frequency product on the market today. The product is from Vicor and operates using a resonant topology similar to figure 5.4; it is discussed in detail in [94]. The product x-ray image, shown in figure 5.19, provides a high density co-packaged solution operating at 1.7MHz; utilizing a matrix transformer structure and low parasitic BGA bare die devices to improve high frequency performance.

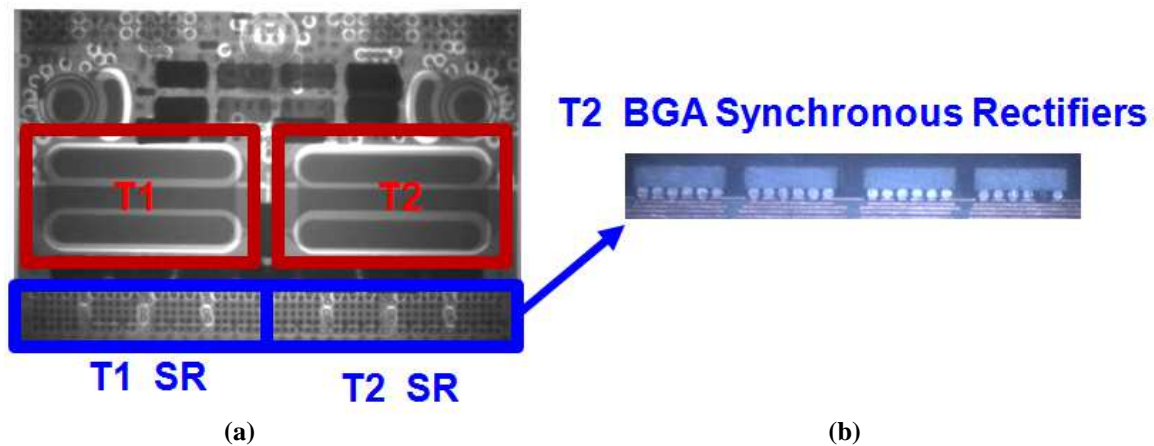


Figure 5.19: Co-packaged module $V_{in}=48V$, $V_o=12V$, $F_s=1.7MHz$, $I_o=25A$ internal view (a) top view (b) side view of BGA SR output for each transformer (Photos by author)

The approach taken in this high density module is to distribute the transformers using a two element matrix transformer, as shown in the circuit diagram of the converter in figure 5.20. The transformer structure uses a 12 layer PCB winding with custom embedded magnetic cores, made of material similar to Ferroxcube 3f45 [105], and a FEA

model was created to estimate the resistance and leakage inductance of the structure is shown in figure 5.20b. The structure interleaves the primary and secondary windings in the same fashion as figure 5.8c. The simulated value for the leakage inductance and winding resistance are given in table 5.3 at 1.7MHz. It should be noted that this simulation did not include termination effects.

	Leakage Inductance (nH)	Primary Winding Resistance (mΩ)	Secondary Winding Resistance (mΩ)	Total Core Loss (W)
1.7 MHz Matrix Structure	13.01	14.53	2.76	1.89

Table 5.3: Matrix transformer simulated leakage inductance and winding resistance

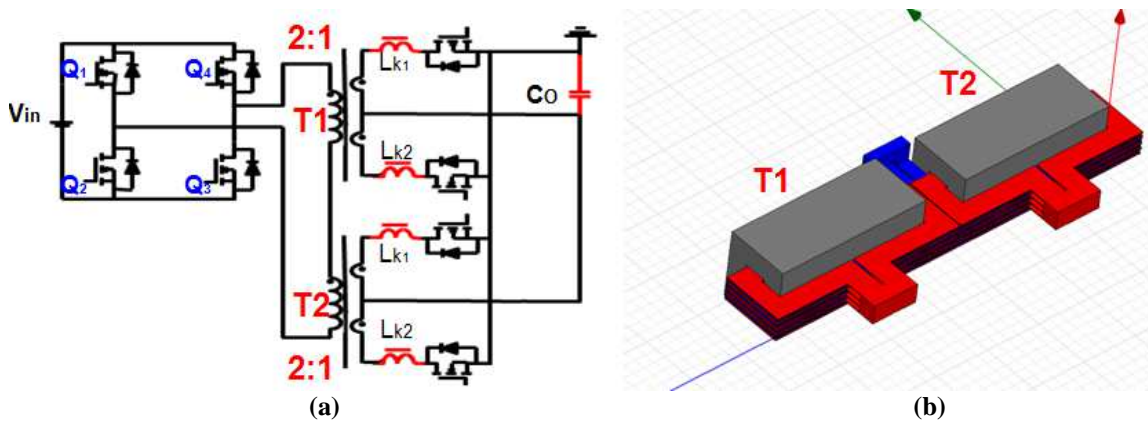


Figure 5.20: (a) Circuit diagram for DCX with matrix transformer (b) FEA model of co-packaged module $V_{in}=48V$, $V_o=12V$, $F_s=1.7MHz$, $I_o=25A$ matrix transformer structure

5.4 Matrix Transformer Design

The other high frequency DCX converter is from research performed in [92], the 800kHz experimental hardware is shown in figure 5.21a. The transformer design also utilizes a two core 2:1 matrix transformer that employs two EIR18 transformers with layers interleaved in the same manner as figure 5.8c. A FEA model was created to model the 12 layer, 2oz copper PCB matrix planar transformer structure. The transformer material was made out of PC44 material [106], which is targeted from 200-500 kHz, resulting in large core loss.

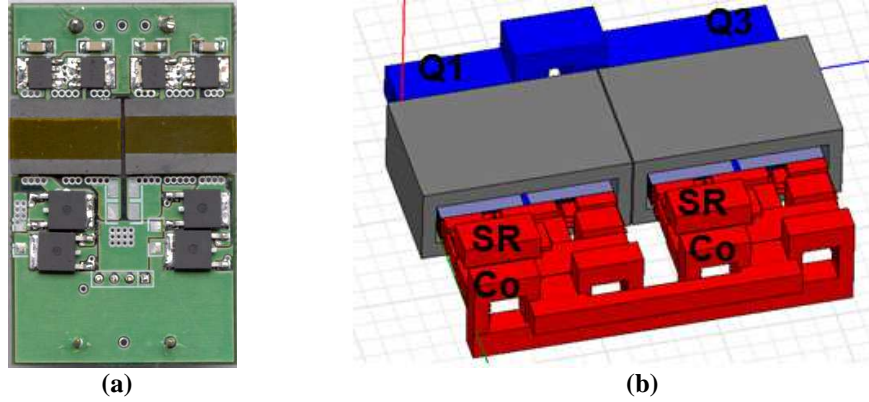


Figure 5.21: (a) Experimental hardware for 800kHz DCX with matrix transformer (b) FEA model of $V_{in}=48V$, $V_o=12V$, $F_s=800kHz$, $I_o=40A$ matrix transformer structure

The benefits of the matrix structure are the ability to split the high current between the two cores, minimizing winding loss, termination loss, and leakage inductance. Looking at the FEA analysis of the structure, it can be seen in figure 5.22a that leakage inductance is reduced in the termination area, the major source of flux in the single core design. The current density plot is shown in figure 5.21b; due to the splitting of the winding current the crowding effects are also minimized.

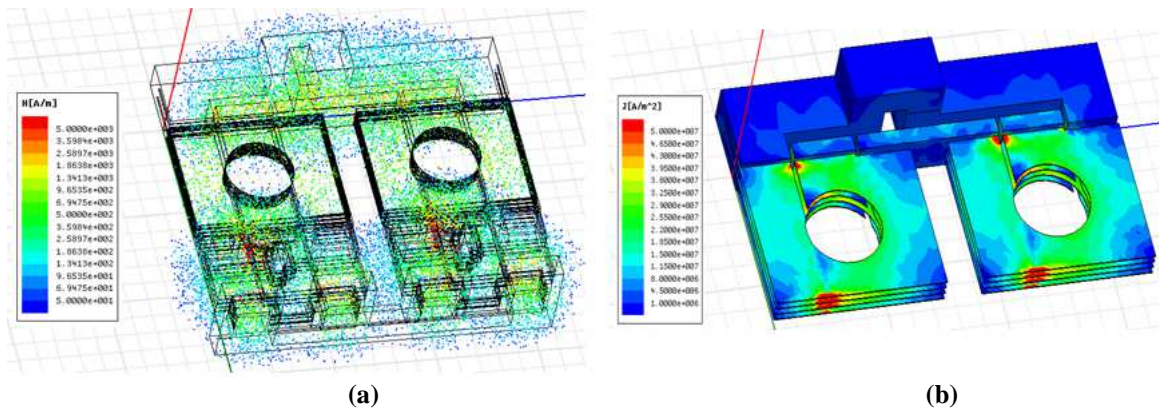


Figure 5.22: 800kHz DCX with matrix transformer (a) Field intensity plot (b) Current density plot

From FEA simulations, verified by measurement, the leakage and equivalent winding resistances are extracted at 800kHz. The original matrix transformer design reduced the effective winding resistance by over 45% and leakage inductance 30% compared to the traditional single transformer design, making it very attractive for high

current applications. The drawback of the matrix transformer structure was that the core loss was increased because of the use of two cores; this results in lower light load efficiency. The final values for the two designs are compared in table 5.4.

	Leakage Inductance (nH)	Equivalent Resistance (mΩ)	Total Core Loss (W)
Single 4:1 EIR 22 Core	57.02	49.36	3.20
Two 2:1 EIR 18 Core	39.08	25.82	5.28

Table 5.4: Leakage inductance and winding resistance for single and matrix transformer structures at 800kHz with PC44 core materials

The reduction in leakage inductance offered by the original matrix structure was not as large as expected. The original design had a large termination loop, shown in red in figure 5.23, resulting in large leakage inductance and termination resistance. In figure 5.23a, the current flow from the SR through the winding to the resonant capacitor is shown, it can be seen that the termination distance from the winding to the capacitor is very long, introducing a large termination effect. In figure 5.23b, the completion of the output loop is completed, further adding to the termination length.

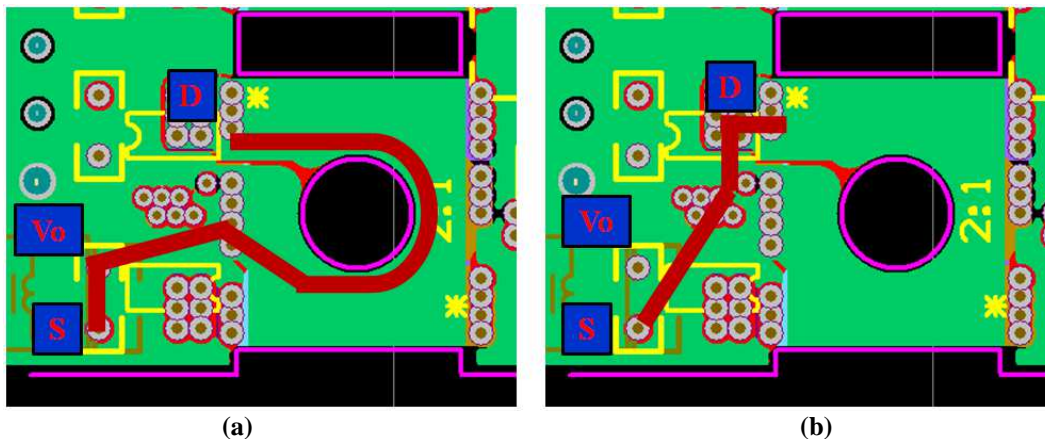


Figure 5.23: 800kHz DCX matrix transformer element (a) Secondary current path in red through winding into output capacitor (b) Return path from capacitor to device

The loop termination can be minimized by moving the output capacitor in close proximity the SR, allowing for further reduction in leakage inductance and winding

resistance. The resulting improvements achievable by improving the secondary loop are shown in table 5.5. The improved connection is utilized in the later designs in this chapter.

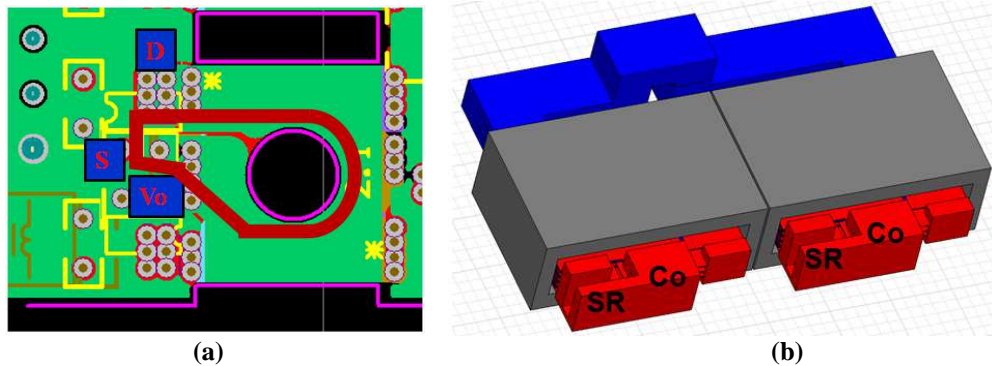


Figure 5.24: 800kHz DCX matrix transformer element (a) layout with improved secondary termination (b) FEA model

	Leakage Inductance (nH)	Equivalent Resistance (mΩ)
Original Termination	39.08	25.82
Improved Termination	27.60	19.49

Table 5.5: Leakage inductance and winding resistance for matrix transformer structure with improved termination at 800kHz

5.4.1 Integrated Matrix Transformer Structure with Flux Cancellation

The matrix transformer can significantly reduce leakage inductance and winding resistance, but this comes at the price of core volume and loss. The use of integrated magnetic structures allows for the integration of multiple magnetic components into a single core, reducing the number of cores and allowing for flux cancellation [107]. The matrix transformer configuration offers an ideal case for core flux cancellation; the cores are excited with identical voltages generating the same flux in each core. This allows for almost complete flux cancellation if designed properly. This can lead to decreased overall size and core loss. The section will discuss the integration of a matrix transformer

into a single core and the arrangement of the windings to provide flux cancellation, giving improved high frequency performance.

The traditional transformer design is shown in figure 5.25a, it contains four primary turns and the secondary configuration is a single turn center tapped winding. To reduce the winding resistance and leakage inductance the traditional structure is shifted to a matrix design with a two core structure with each structure containing two primary turns and a center tapped secondary configuration with single turn windings. The two transformers in the matrix design are completely decoupled as a result of the use of separate magnetic cores.

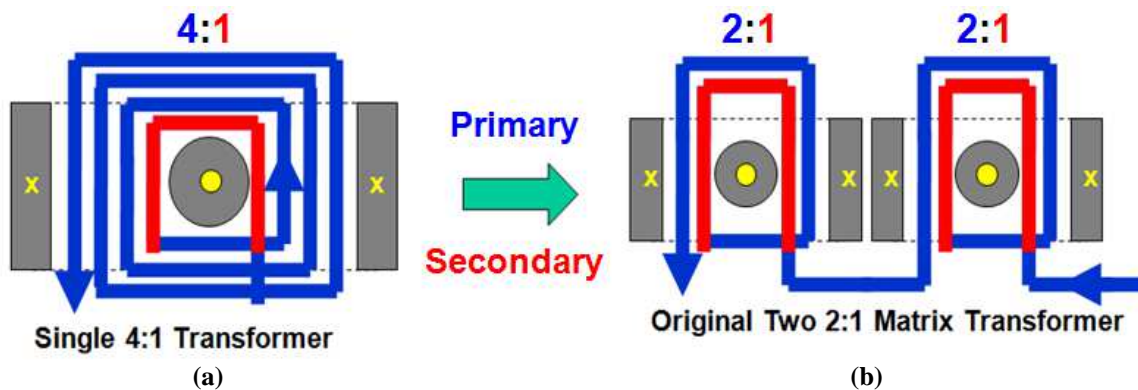


Figure 5.25: 48V bus converter transformer structure cross sectional top view (a) Traditional single core 4:1 design (b) Two core 2x2:1 matrix transformer design

To improve performance of the matrix transformer, the two magnetic cores are integrated into a single core to simplify the matrix transformer structure. The simplification of the design is done by combining the two discrete cores into a single EI core by removing the outer legs of the design in 5.25b, widening the center leg, and wrapping the primary and secondary windings around the outer legs of the EI structure. The result of this is a single core with the flux of the two transformers adding in the center leg as shown in figure 5.26a. The flux in the outer legs is given by:

$$\Delta\phi_{Outer_Leg} = \frac{V_o \cdot D}{2 \cdot N_s \cdot f_s} \quad (5.24)$$

Where V_o is the output voltage, D is the duty cycle, N_s is the number of secondary turns, and f_s is the switching frequency.

With the outer legs sharing the same voltage in phase with each other, the flux forms the outer legs add and the center leg flux is given by:

$$\Delta\phi_{Center_Leg} = \frac{V_o \cdot D}{N_s \cdot f_s} \quad (5.25)$$

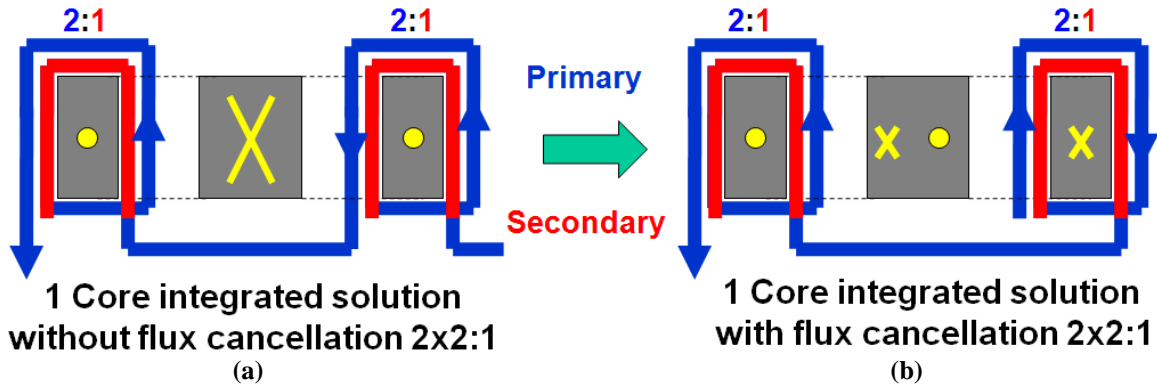


Figure 5.26: 48V bus converter transformer structure (a) Single core 2x2:1 design without flux cancellation (b) Single core 2x2:1 design with flux cancellation

In the proposed structure, to achieve flux cancellation in the center leg, the polarity of one of the outer leg windings of the transformers is rearranged to change the flux direction as shown in 5.26b. The result is an integrated matrix transformer design with the flux in the center leg being cancelled. Figure 5.27 shows the FEA results of the AC flux distribution in the core structures with and without core flux cancellation. In both structures, the flux distribution is the same in the outer legs. In the proposed structure, the flux in center leg is cancelled, reducing the core loss of the structure compared to the traditional matrix transformer structure. To ensure the flux cancels in the center leg, the magnetizing inductance, needed for ZVS is created by placing air gaps in the outer legs, making the center leg a low reluctance path.

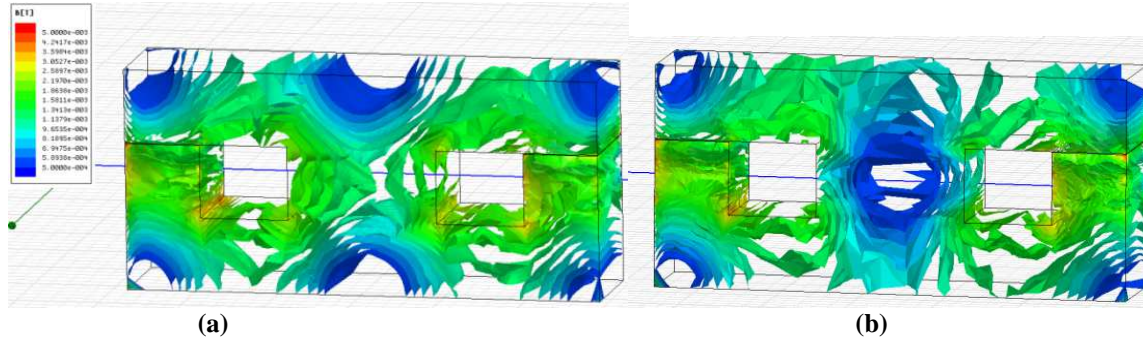


Figure 5.27: 48V bus converter transformer core flux simulation (a) Single core 2x2:1 design without flux cancellation (b) Single core 2x2:1 design with flux cancellation

The new integrated matrix transformer structure offers lower core loss while greatly decreased winding resistance and leakage inductance. Figure 5.28a shows the model of the modified matrix transformer design. The current distribution is shown in figure 5.28b and it can be seen that there is less current crowding leading to good thermal distribution in the core. The cases with and without flux cancellation are compared and the results are shown in table 5.6. Both structures had similar winding resistance and leakage inductance and the case with core flux cancellation reduced core loss 45%. To improve core loss, the core material is selected to be 3f35.

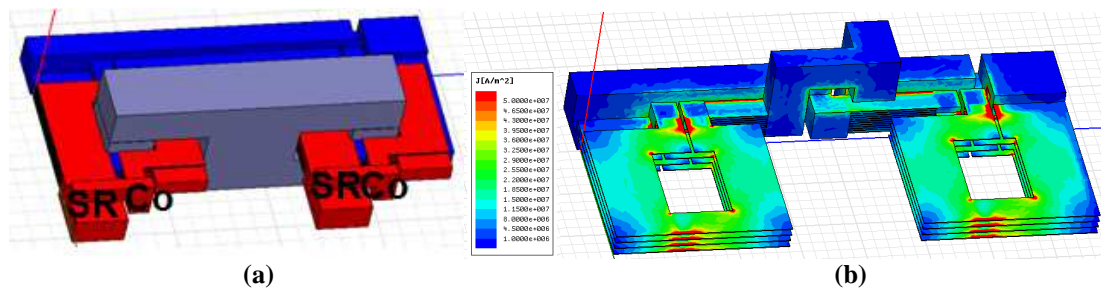


Figure 5.28: (a) AC flux cancellation matrix transformer design (b) FEA simulation of current distribution in primary windings

	Leakage Inductance (nH)	Equivalent Resistance (mΩ)	Total Core Loss (W)
Integrated structure without flux cancellation	23.88	21.58	3.52
Integrated structure with flux cancellation	25.60	21.71	1.94

Table 5.6: Transformer leakage inductance winding resistance, and core loss comparison for integrated transformer designs at 800kHz

The transformer loss comparison for the traditional single transformer design, the integrated matrix structure without flux cancellation, and the proposed integrated structure with flux cancellation are shown in figure 5.29. The traditional transformer structure provides low core loss, improving light load efficiency, but suffers from high conduction loss, especially in the secondary, lowering heavy load efficiency. The integrated matrix transformer structure without flux cancellation offers lower conduction loss but suffers from higher core loss. The proposed integrated matrix transformer with core flux cancellation can provide low core loss from the flux cancellation and low conduction loss and leakage inductance from the distributed winding structure.

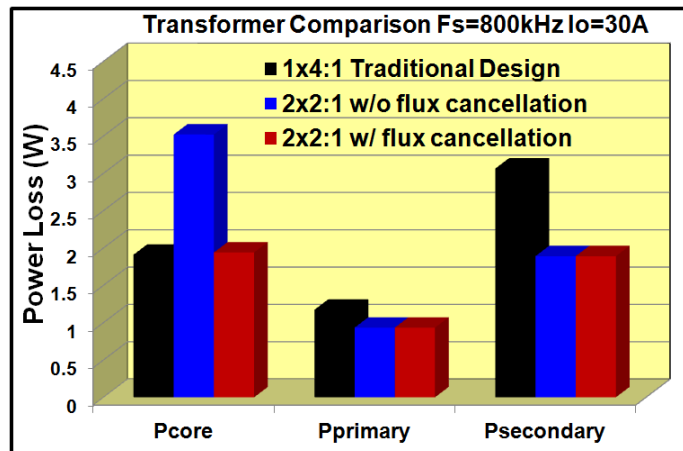


Figure 5.29: Transformer Loss Comparison, $F_s=800\text{kHz}$ $I_o=30\text{A}$

5.4.2 800kHz Silicon Experimental Verification

To verify the design improvements of the transformer structure, three designs were created to operate at 800KHz. The specifications for the integrated transformer structure converter, shown in figure 5.30, were $V_{in}=48\text{V}$, $V_o=12\text{V}$, $P_o=700\text{W}$, $f_s=800\text{kHz}$, $L_k=25\text{nH}$, $D=0.5$, and $C_o=6.58\mu\text{F}$. The primary devices were four Infineon BSB044N08NN3, the secondary devices were four BSB015N04NX3, both employed the

can package to minimize parasitics. The primary side driver is Intersil HIP2101. The cores were a custom designed 3f35 Mn-Zn ferrite from ferroxcube.

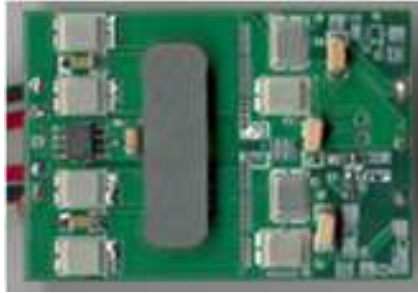


Figure 5.30: Experimental hardware Vin=48V Vo=12V Fs=800kHz

To achieve ZVS, the magnetizing inductance was chosen to be 4uH. To ensure that the flux does not circulate between the two outer legs the air gaps used to obtain the magnetizing inductance required for ZVS are placed in the outer legs while the center leg has no gap. Arranging the gaps in this manner ensures that the flux will flow through the low reluctance center leg and no coupling will occur between the matrix transformer elements. The turn off current is determined by the magnetizing current and given by:

$$\Delta I_{LM} = \frac{D \cdot V_{in}}{2 \cdot L_m \cdot f_s} = 3.7 A \quad (5.26)$$

Shown in figure 5.31A is the switching waveform of the converter showing ZVS is achieved. For the resonant design employed, ZVS can be achieved for the full load range because the magnetizing inductance is used for ZVS and it is not load dependant as in the case in the phase shift full bridge. Shown in figure 5.31b are the primary waveforms with the current waveform shown in pink; the turn off current is reduced by resonating the current waveform, minimizing the turn off loss. For higher frequencies, a smaller device with lower output capacitance could be employed, allowing for a lower magnetizing current to be used, further reducing turn off current.

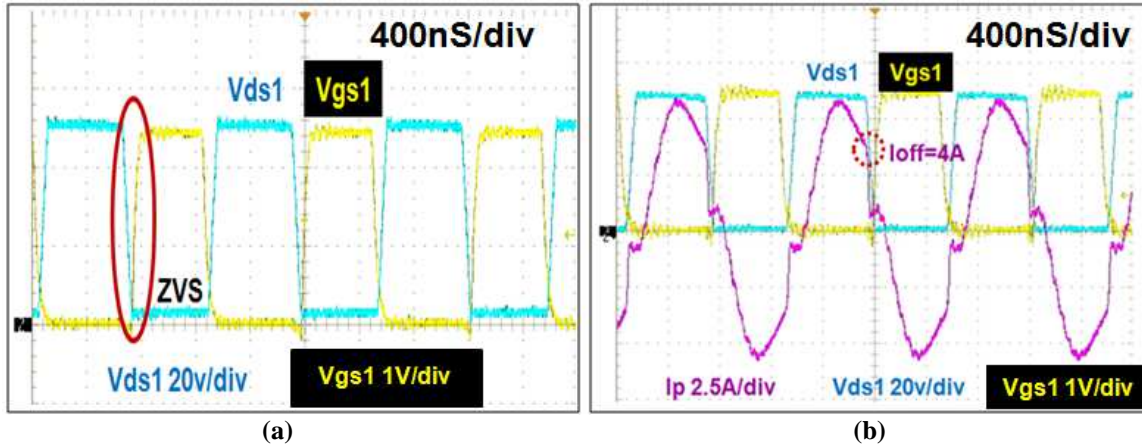


Figure 5.31: Experimental waveforms for $F_s=800\text{kHz}$, $V_{in}=48\text{V}$, $V_o=48\text{V}$ (a) Primary side device Vgs and Vds showing ZVS (b) Primary current waveform showing reduced turn off current

The efficiency curves for the designs are shown in figure 5.32, the proposed integrated transformer with flux cancellation design achieves a peak efficiency of 95.9% at 300W and maintains an efficiency over 95% until 530W of output power. The proposed transformer structure offers similar light load and improved heavy load efficiency when compared to the traditional transformer design and efficiency improvement in all load for the traditional matrix structure.

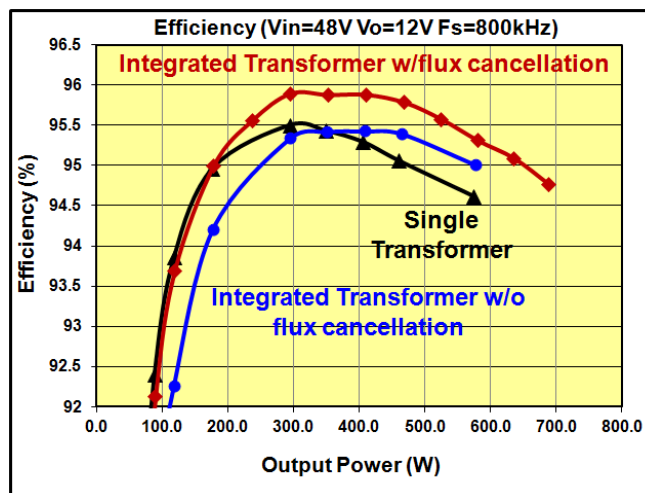


Figure 5.32 Efficiency at $V_{in}=48\text{V}$, $V_o=12\text{V}$, $F_s=800\text{kHz}$ integrated matrix transformer structures with and without flux cancellation

A loss breakdown is performed for the converter with the proposed integrated matrix transformer with flux cancellation and is shown in figure 5.33. From the loss

breakdown it can be seen that the turn off loss, transformer core loss, and driver losses are the largest barriers to higher efficiency. The improved topology reduces the turn off loss and the self driven method reduces SR driving loss, but at very high frequencies, switching related losses still dominate the overall power loss. To minimize transformer core loss the frequency can be increased, leading to a further increase in switching related losses. To further push for higher frequency and higher density, improved devices must be considered.

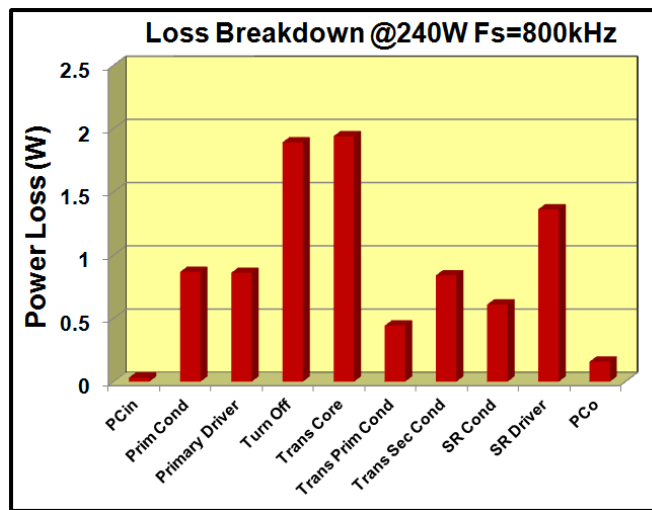


Figure 5.33 Loss breakdown of $V_{in}=48V$, $V_o=12V$, $F_s=800kHz$, $I_o=20A$ integrated matrix transformer structures with flux cancellation

5.4.3 Improved Integrated Transformer Structure

The proposed integrated transformer with flux cancellation in the center leg has a net flux of zero in the center leg, as shown in figure 5.34b. With the net flux of zero in the center leg in the previous structure, it can be removed and the area occupied by the core can be reduced, shrinking overall magnetic size while improving the magnetic performance. Figure 5.34d shows the improved structure and flux density plots from Maxwell 3D FEA simulation at 0.8MHz. The core loss remains the same while the

winding resistance and leakage inductance are reduced. Also, the footprint consumed by the transformer is reduced 25%. This improved structure will be applied in the following section for a higher frequency, higher density GaN based DCX converter.

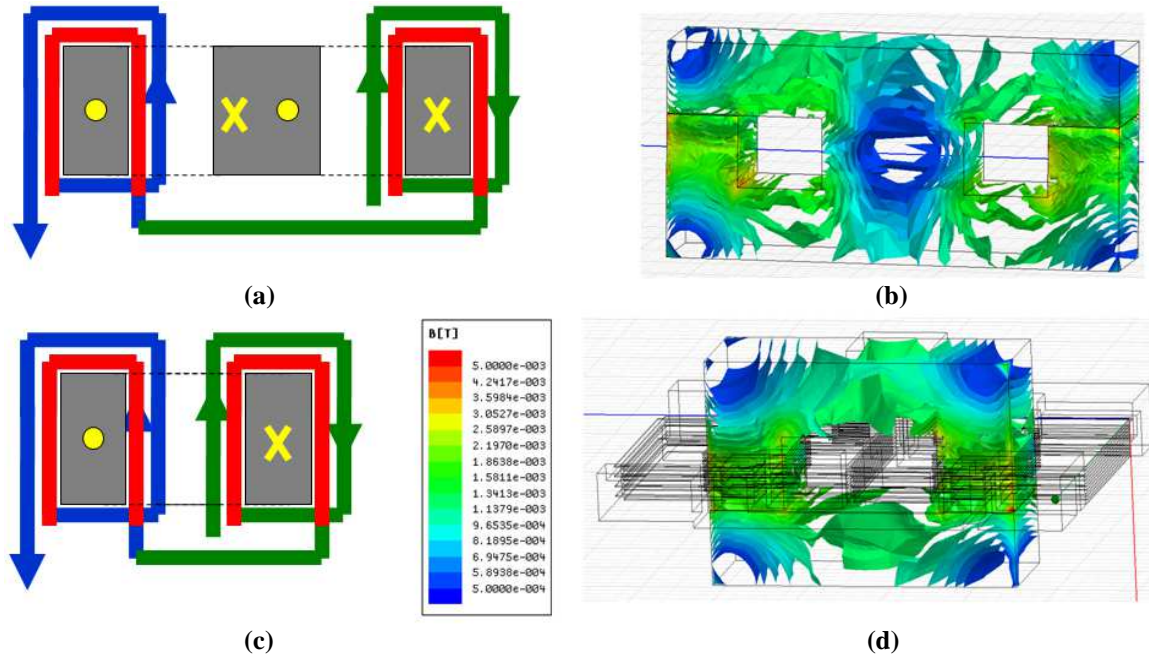


Figure 5.34: Integrated single core matrix structure with flux cancellation in center leg (a) Winding structure (b) Flux density distribution. Proposed integrated matrix structure without center leg (c) Winding structure (d) Flux density distribution

5.5 High Frequency GaN DCX Bus Converter

5.5.1 Benefits of GaN for High Frequency 48V Applications

To further push for higher frequency and power density, GaN devices are considered in this section. From chapters 3 and 4, the benefits of GaN technology were demonstrated for a hard switching 12V buck application. In this section the use of GaN devices will be explored in a 48V soft switching application. The figure of merit for GaN and Si devices from 25 to 100V are shown in figure 5.35, the GaN device shows significant improvements when compared to silicon devices, with the FOM decreasing by a factor of 4 and 2.5 for 100 and 40V devices respectively. The packaging of the GaN

device also provides improvements; employing the low parasitic LGA package compared to the can package used in the Si devices.

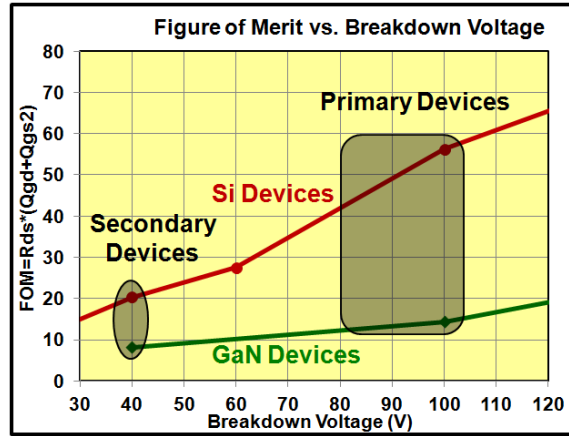


Figure 5.35 Figure of merit comparison for primary and secondary GaN devices for use in 48V GaN DCX bus converter

Direct comparisons of the key parameters for the GaN and Si devices are shown in tables 5.7 and 5.8. For the primary side EPC2001 GaN devices, all of the key parameters are decreased when switching to the GaN except the dead time conduction voltage, which can be handled in by a schottky diode and dead time tuning, as was shown in chapter 3. With the turn off loss for the previous Si design being a large loss contributor, minimizing Qgd is critical, and the GaN provides an 80% reduction in Qgd.

	Parameter	80V Si	100V GaN	GaN Difference
Primary Conduction	R_{dson}	6.5m Ω	5.6m Ω	14% decrease
Driver	Q_g	30nC	8nC	73% decrease
Turn Off	Q_{gd}	11nC	2.2nC	80% decrease
Turn On	C_{oss}	1000pF	450pF	55% decrease
Dead Time Conduction	V_{SD}	0.9V	1.75V	94% increase
Reverse Recovery	Q_{rr}	110nC	0nC	100% decrease

Table 5.7: Device comparison between GaN and Si for primary side devices

For the secondary side comparison, two GaN EPC 2015 devices in parallel are compared to a single Si device. The previous Si converter suffered from high gate driving losses; for the GaN, the gate drive losses can be decreased by a factor of 2

compared to Si devices. For the 40V secondary devices, the GaN devices have an increase in on resistance of 23%; with the push for higher frequencies, the number of SR devices employed remains at four, increasing total design on resistance and limiting the total output current capable for the GaN design considered in this section. The biggest disadvantage of the GaN device is the large dead time loss, which needs to be limited through the use of a schottky diode and reduced dead time.

	Parameter	40V Si	2x40V GaN	GaN Difference
Secondary Conduction	R_{dson}	1.3m Ω	1.6m Ω	23% increase
Driver	Q_g	107nC	21nC	80% decrease
Dead Time Conduction	V_{SD}	0.81V	1.75V	116% increase
Reverse Recovery	Q_{rr}	50nC	0nC	100% decrease

Table 5.8: Device comparison between GaN and Si for secondary side devices

5.5.2 Impact of Soft Switching on GaN Performance

For the high frequency GaN design, both hard switching and soft switching solutions were compared to see the impact of the soft switching topology on GaN performance. For the hard switching topology the standard hard switching full bridge converter operated at 50% duty cycle was considered, the electrical schematic is shown in figure 5.36a, and the driving signals with primary current is shown in figure 5.36b.

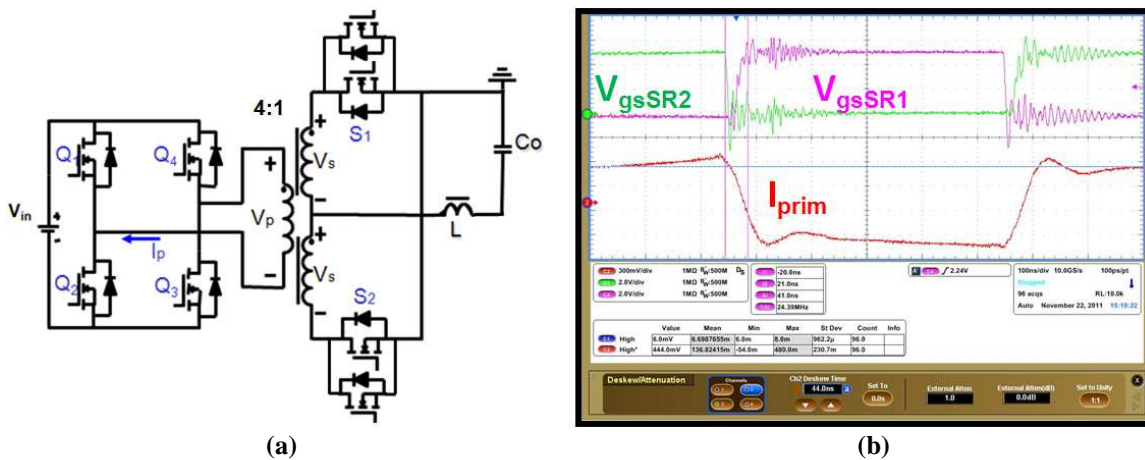


Figure 5.36: (a) GaN hard switching FB schematic $V_{in}=48V$, $V_o=12V$, Primary: 4xEPC2001, SR: 4xEPC2015, $L=150nH$, $C_o=88\mu F$ (b) Primary current waveform and secondary drive voltages

The difference in performance between the hard and soft switching topologies for the GaN converter is shown in figure 5.37a and the corresponding power loss is shown in figure 5.37b. Utilizing soft switching with GaN devices can offer superior efficiency at over twice the switching frequency. The major reasons for the improved performance are ZVS and low turn off current provided for the devices in the resonant topology, and reduced core loss due to higher frequency operation. The turn on loss for a switch without ZVS is given by:

$$P_{Turn_on} = 0.5 \cdot V_{in} \cdot Q_{oss} \cdot f_s \quad (5.27)$$

Where Q_{oss} is the output charge of the device at the turn on voltage.

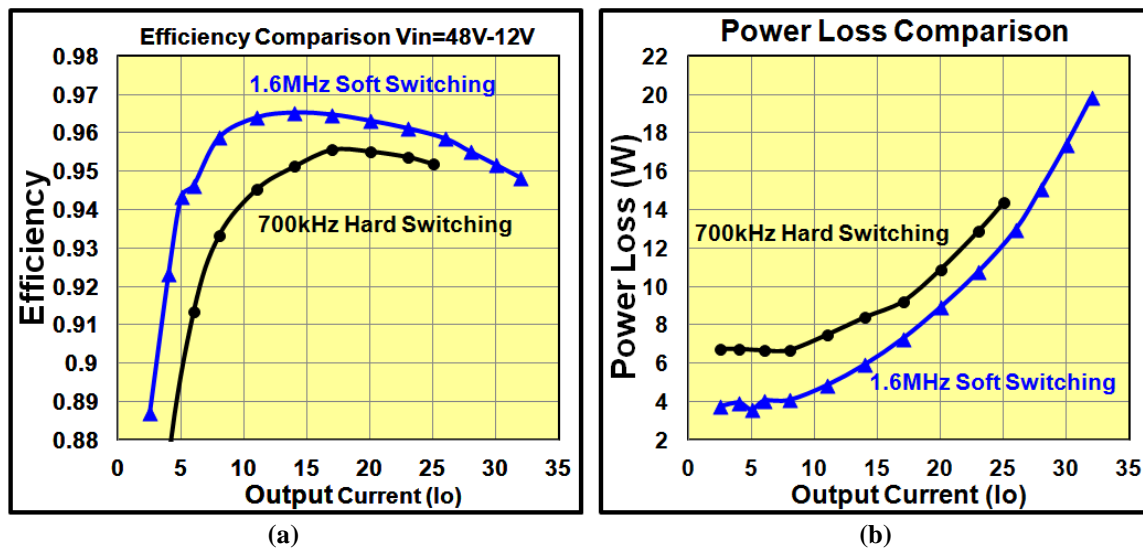


Figure 5.37: Experimental results for $V_{in}=48V$, $V_o=12V$, primary devices: EPC2001, secondary devices :EPC2015, driver:LM5113(a) Efficiency comparison between 700kHz hard switching and 1.6MHz soft switching (b) Power loss comparison

Another major benefit of soft switching is reduced voltage stress across the SR devices. For the hard switching converter, there is a large current during at the turn off of the SR devices. The energy stored in the leakage inductance at turn off rings with the output capacitance of the SR devices, as seen in figure 5.38a, causing a large voltage overshoot of around 20V, resulting in a peak voltage of 44V for the GaN SR's. For the

hard switching design, the use of 40V devices is not safe and 60V devices should be selected, increasing SR resistance. For the resonant topology, ZVS and ZCS is achieved for the secondary devices and no energy is stored in the leakage inductance at turn off, almost eliminating the voltage spike as shown in figure 5.38b. This allows for 40V devices to be used, improving performance, and device safety.

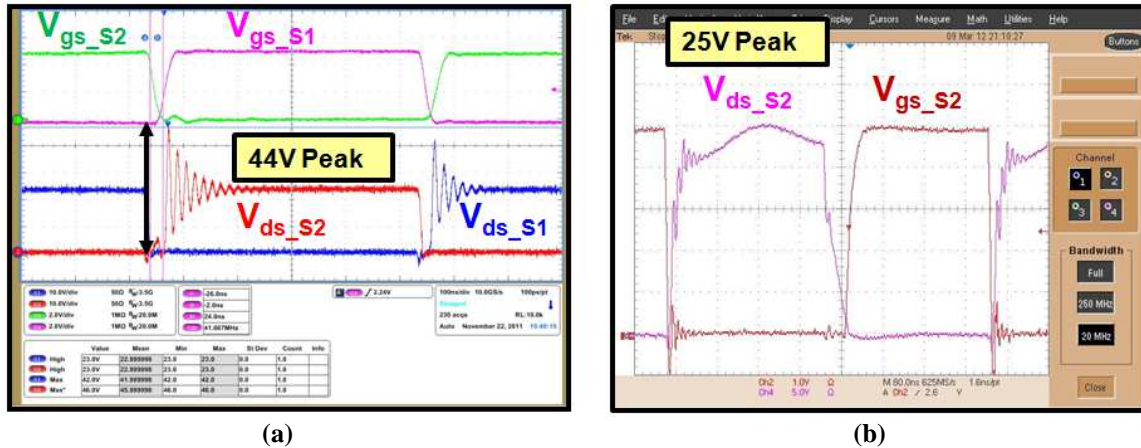


Figure 5.38: Experimental waveforms for $V_{in}=48V$, $V_o=12V$, primary devices: EPC2001, secondary devices :EPC2015, driver:LM5113 (a) GaN hard switching secondary voltage waveforms (b) GaN soft switching secondary voltage waveforms

5.5.3 1.6 MHz Transformer Structures

To explore the benefits of the proposed integrated transformer structure in figure 5.34 at higher frequencies, three transformer structures, each occupying the same footprint, were designed to compare the impact of different matrix structures on winding loss, termination loss, core loss, and leakage inductance. In the previous analysis of the integrated structure at 800kHz, the simulations required termination simplifications due to software and processor limitations, and were solved only for total equivalent winding resistances and leakage inductances.

For the designs considered in this section, allowed by improved simulation tools and processor capability, the detailed impact of the termination of transformer structures will be considered. The cores used in these designs were customized 3f45 planar cores,

and the total transformer structure width was fit to match the active power stage to maximize power density.

The first transformer considered is the traditional EE single core design for benchmarking purposes; having a four turn primary winding and a single turn center tapped secondary winding. The PCB is a twelve layer, two ounce pcb with four layers for the primary, each containing a single turn and four parallel layers for each secondary. The electrical diagram and transformer structure are shown in figures 5.39, two SR's are used in parallel to minimize conduction.

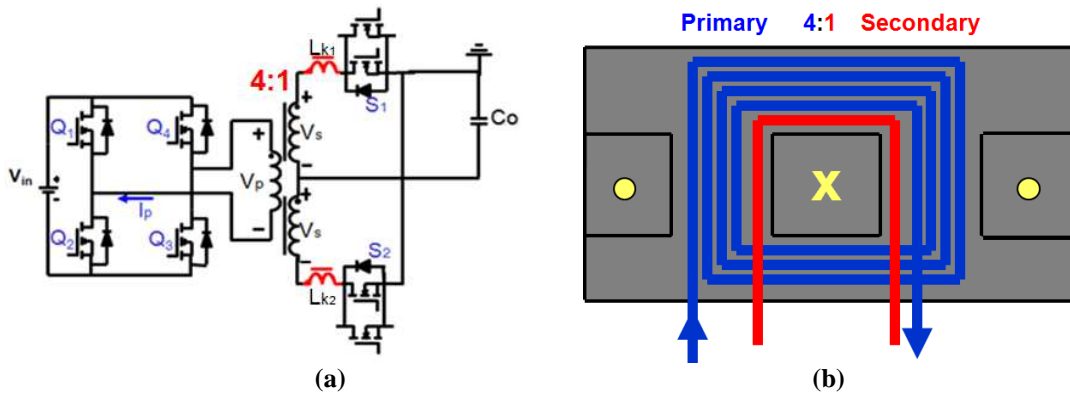


Figure 5.39: (a) Circuit diagram with secondary loop (b) Transformer structure of 4:1 EE transformer

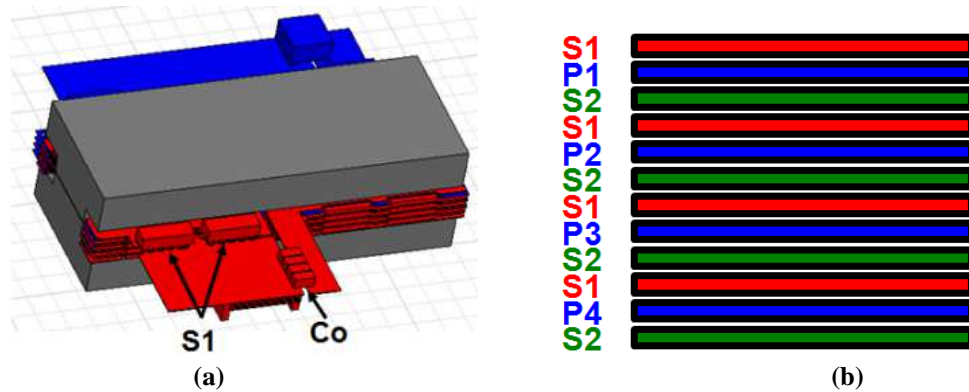


Figure 5.40: (a) FEA model of 4:1 EE transformer (b) winding interleaving arrangement of transformer

To identify the impact of the primary and secondary loops on transformer performance three separate simulations and experimental setups were considered to

identify the portion of leakage inductance and resistance that are generated by the primary loop, the transformer, and the secondary loop. The FEA model with detailed modeling of the termination is shown in figure 5.40a. The winding structure is interleaved to minimize leakage inductance and proximity effects and shown in figure 5.40b. The tests were run at 1,1.5, and 2MHz and the results for the leakage inductance, reflected to the primary side, are shown in table 5.9. For the traditional EE design, with minimized primary and secondary loops, almost a quarter of the leakage inductance is a result of the terminations. In cases with larger loops or high parasitic packages, this percentage would increase significantly.

	Shorted Transformer Leakage	Primary Loop Inductance	Secondary Loop Inductance	Total Leakage Inductance
1MHz	35.75nH	1.90nH	8.68nH	46.33nH
1.5MHz	35.54H	1.82nH	8.51nH	45.87nH
2MHz	35.48nH	1.79nH	8.40nH	45.67nH

Table 5.9: Leakage inductance breakdown for the traditional 1x4:1 EE transformer

Using Maxwell 3D FEA simulations, the sources of leakage were analyzed for the case with the primary and secondary loops and the case with shorted primary and secondary loops. The case with the shorted primary and secondary loop is shown in figure 5.41a, it has strong magnetic field intensity in the regions where there is no winding interleaving. The regions where there is no interleaving are located in close proximity to the transformers input and output connections and the transformers inner layer via connections. In these regions the current in the primary and secondary are not flowing in opposing directions and there is little flux cancellation.

Shown in figure 5.41b is the simulation with complete terminations; the field intensity increases in the termination regions. The high current secondary termination

contributes the largest amount of leakage inductance, matching the measurement results. The primary and secondary termination regions experience little field cancellation, increasing the leakage inductance in these areas. The leakage inductance for the transformer structure and termination shows little dependence on frequency with the leakage dropping 2% from 1 to 2MHz.

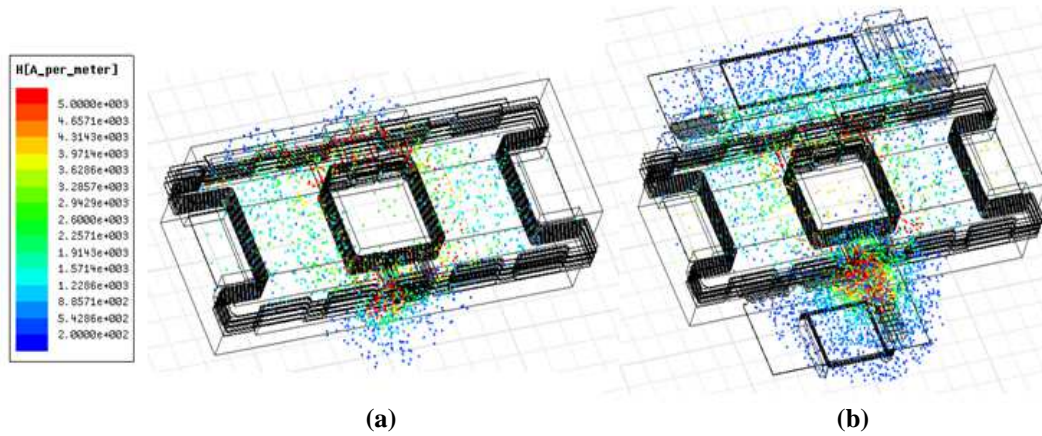


Figure 5.41: (a) Magnetic field intensity plot of shorted transformer at 2MHz (b) Magnetic field intensity plot of design case at 2MHz

The impact of termination on the winding resistances was also considered from 1 to 2MHz. Figures 5.42 a&b show the simulated current density in the primary and secondary windings in the traditional transformer design. For higher frequencies the winding experiences current crowding in the inner sections of the winding. The other major areas of current crowding occur in the areas with poor interleaving. These areas are the same as the high leakage areas.

With the severe current crowding existing in the high current secondary loop the resistance of the termination becomes a major loss component in the circuit. Shown in table 5.10 are the measured resistances of the transformer; the secondary loop resistance accounts for half of the winding loss in the secondary of the transformer. For the primary

winding, because of the high resistance inside the multi-winding transformer, the loop resistance represents only 9% of the winding resistance in the primary side.

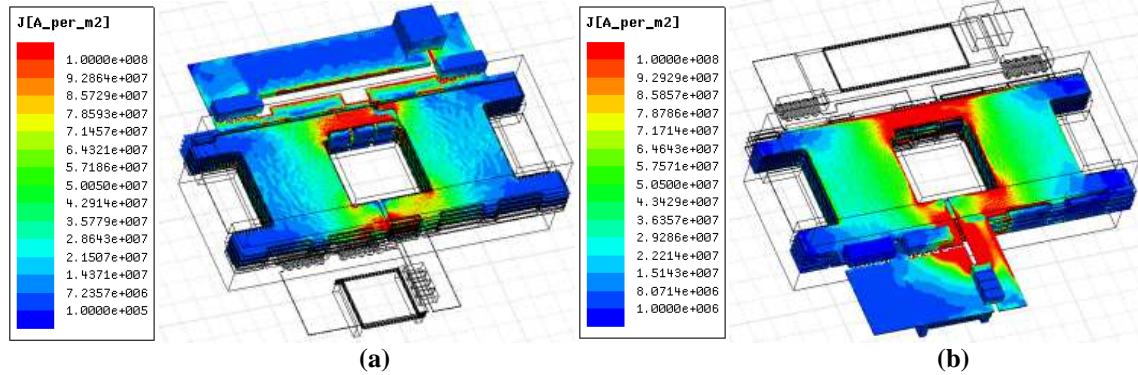


Figure 5.42: (a) Primary winding current density at 2MHz (b) Secondary winding current density at 2MHz

	Primary Winding Resistance	Primary Loop Resistance	Total Secondary Winding Resistance	Secondary Loop Resistance
1MHz	19.70mΩ	1.81mΩ	3.45mΩ	1.75mΩ
1.5MHz	21.53mΩ	2.02mΩ	3.82mΩ	1.88mΩ
2MHz	23.22mΩ	2.15mΩ	4.15mΩ	1.94mΩ

Table 5.10: Winding resistance breakdown for the traditional 1x4:1 EE transformer

The impact of transformer termination on leakage inductance and winding resistance is a major issue in high frequency transformer design. For improved high frequency transformer design, a better solution is needed.

The proposed integrated core structure’s electrical schematic and transformer structure are shown in figures 5.43a&b. The high current secondary loops are divided into two separate, parallel outputs to improve performance. The outputs are horizontally distributed on the PCB board. In higher voltage applications [108][109], the distribution of the secondary has been considered in a vertical manner by adding multiple secondaries. The lateral and vertical distribution approaches both reduce resistance and leakage inductance, but the vertical design adds mechanical complexity, results in thermal issues for the synchronous rectifiers in between output layers, and increases core

and board height. For higher frequencies and lower voltages the horizontal distribution can offer improved performance with a simplified design.

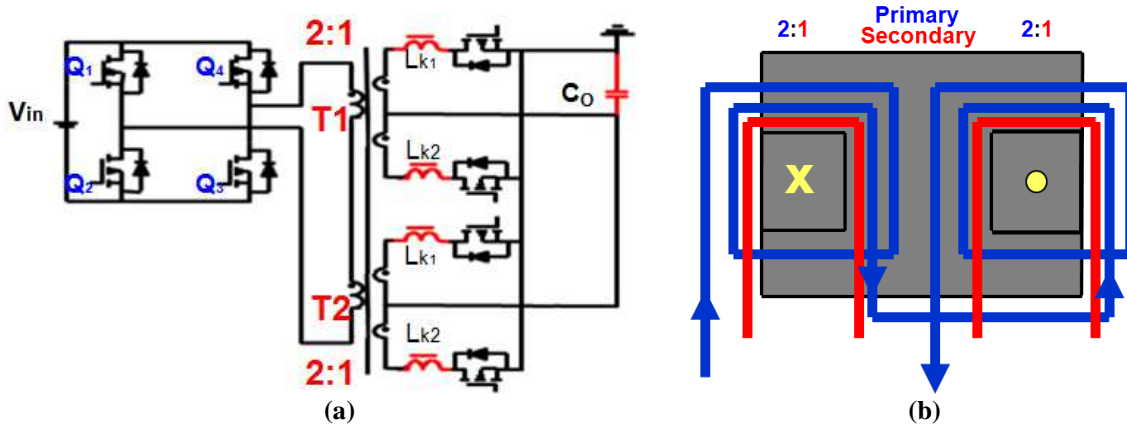


Figure 5.43: (a) Circuit diagram with 2x2:1 distributed secondary loop (b) Transformer structure of 2x2:1 proposed integrated design

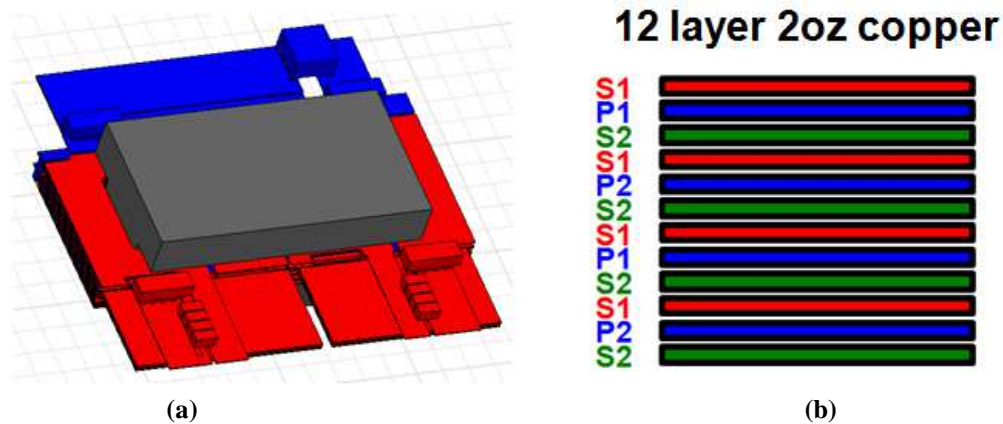


Figure 5.44: (a) FEA model of proposed 2x2:1 integrated transformer (b) winding interleaving arrangement of transformer

The simulated magnetic field intensity plots for the proposed structure are shown in figures 5.45 a&b for the case with the transformer windings shorted and the case with the complete primary and secondary terminations. In the new proposed integrated matrix structure, the magnetic field intensity in the termination areas is reduced, resulting in lower leakage inductance. Table 5.11 shows the effective leakage inductances of the new transformer structure; the new structure reduces the leakage inductance 35% compared to the traditional EE transformer design.

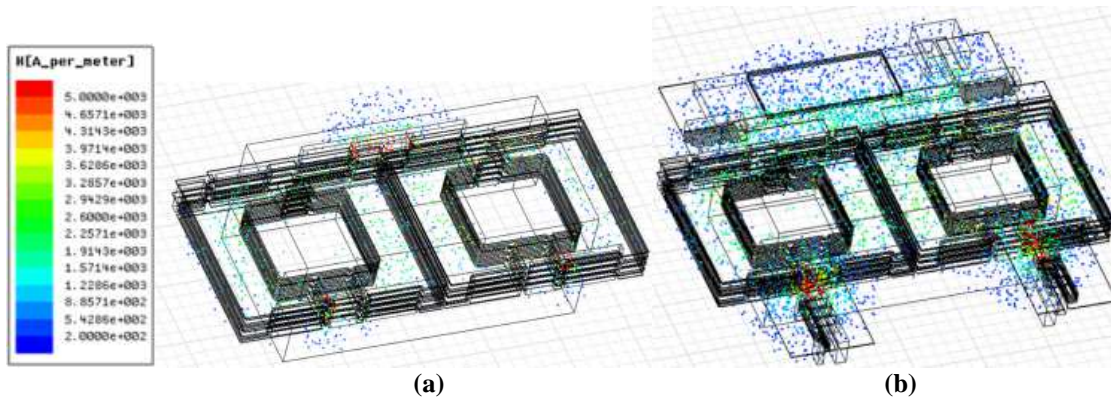


Figure 5.45: (a) Magnetic field intensity plot of shorted transformer at 2MHz (b) Magnetic field intensity plot of design case at 2MHz

	Shorted Transformer Leakage	Primary Loop Inductance	Secondary Loop Inductance	Total Leakage Inductance
1MHz	24.09nH	1.90nH	3.86nH	29.85nH
1.5MHz	23.75nH	1.82nH	3.82nH	29.39nH
2MHz	23.44nH	1.79nH	3.78nH	29.01nH

Table 5.11: Leakage inductance breakdown for proposed 2x2:1 transformer

The winding resistances were simulated and experimentally measured and the values are reported in table 5.12. Figures 5.46 a&b show the current distribution in the primary and secondary windings.

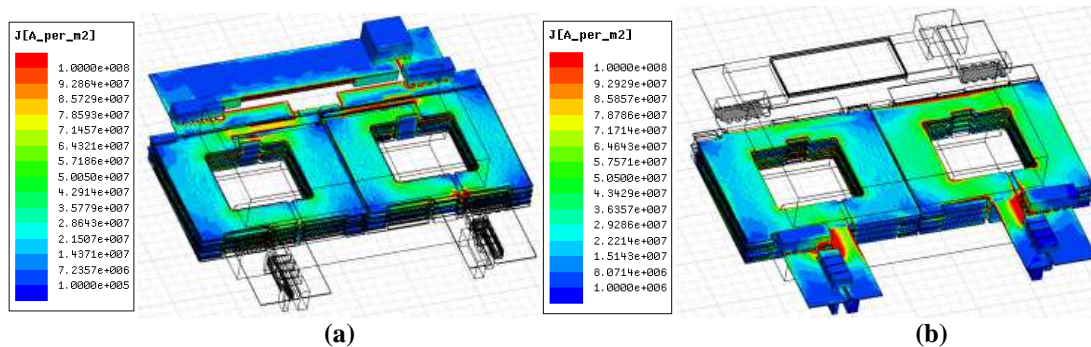


Figure 5.46: (a) Primary winding current density at 2MHz (b) Secondary winding current density at 2MHz

	Primary Winding Resistance	Primary Loop Resistance	Total Secondary Winding Resistance	Secondary Loop Resistance
1MHz	16.14mΩ	1.82mΩ	2.23mΩ	0.86mΩ
1.5MHz	17.54mΩ	2.00mΩ	2.46mΩ	0.98mΩ
2MHz	18.68mΩ	2.11mΩ	2.64mΩ	1.05mΩ

Table 5.12: Winding resistance breakdown for proposed 2x2:1 transformer

Compared to the traditional EE single transformer case the current is better distributed throughout the winding and the current crowding in the terminations is

reduced. The total effective winding resistance is reduced in the primary by 17% and by 40% in the secondary winding. The large reduction in the secondary winding resistance results from having two outputs in parallel to divide the output termination connections and reduce high frequency effects.

The final transformer to be tested was the four transformer structure, comprising of two of the proposed integrated structures with the primaries connected in series. The electrical diagram and transformer design are shown in figures 5.47a&b. For this design, the number of SR devices remained unchanged and the connections for the transformer secondary's were tied together at an SR device.

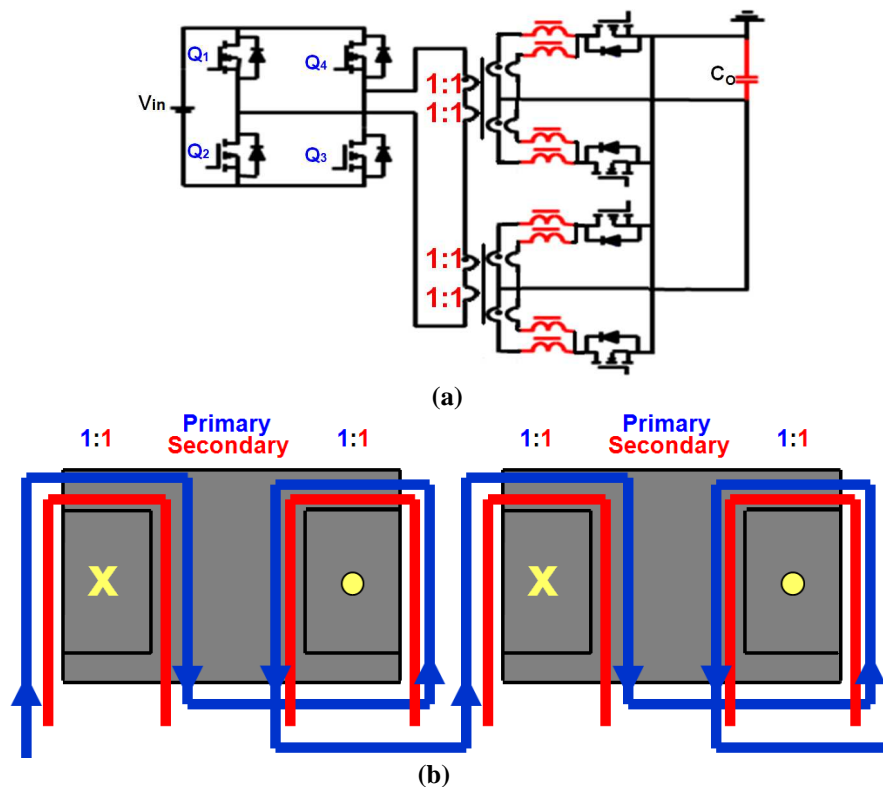


Figure 5.47: (a) Circuit diagram with 4x1:1 transformer (b) Transformer structure of 4x1:1 using two proposed integrated structures

The equivalent leakage inductance and winding resistance for this structure is shown in table 5.13. It can be seen that for the 4x1:1 design that the resistance and

leakage inductance are not improved significantly over the 2x2:1 structure; and the structure incurs higher core loss due to multiple magnetic cores. The cause of the higher resistance and leakage inductance of this structure comes from layout; the termination distance to connect the secondaries to the corresponding SR is increased, diminishing the benefits of extra parallel outputs. Figure 5.48 compares the loss breakdown for the three transformer structures, due to the higher losses and increased amount of magnetic material required for the 4x1:1 design, it was ruled out for possible structure in this application. For higher current applications with a higher number of SR devices and larger secondary footprint this design approach could prove beneficial.

	Total Leakage Inductance	Total Winding Resistance
1MHz	27.30nH	58.60 mΩ
1.5MHz	26.40nH	66.50 mΩ
2MHz	26.00nH	72.10 mΩ

Table 5.13: Leakage inductance and winding resistance for 4 x 1:1 transformer structures

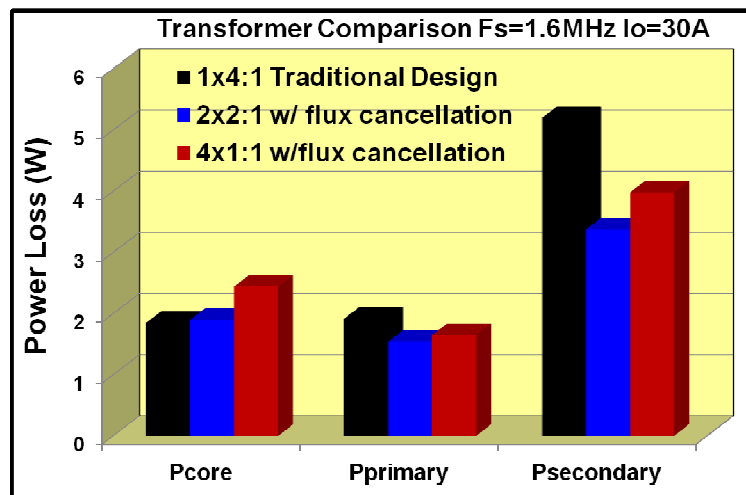


Figure 5.48: Transformer Loss Comparison at 1.6MHz, Io=30A

5.5.4 1.6MHz GaN Experimental Verification

To verify the transformer improvements for the high frequency GaN resonant converter experimental hardware was built using 4xEPC2001 100V primary devices for the primary, 4xEPC2015 devices for the SR's, and 4 National semiconductor LM5113

drivers with additional an additional turn on resistance of 3Ω and turn off resistance of 0.5Ω to protect the devices from overshoot and false turn on. The cores were custom designed 3f45 EE and UI cores described in the previous section, the core cross sectional area was around 40mm^2 . The volume was 1700mm^3 for the proposed integrated structure and 2100mm^3 for the traditional EI core design. The magnetizing inductance for each design was $5\mu\text{H}$. The resonant capacitances for the 1x4:1 and 2x2:1 designs were $0.89\mu\text{F}$ and $1.29\mu\text{F}$, respectively. The hardware and experimental waveforms are shown in figure 5.49 a-d. Both designs achieve ZVS for both the primary and secondary devices, and the turn off current for the primary devices is limited to 3.5A .

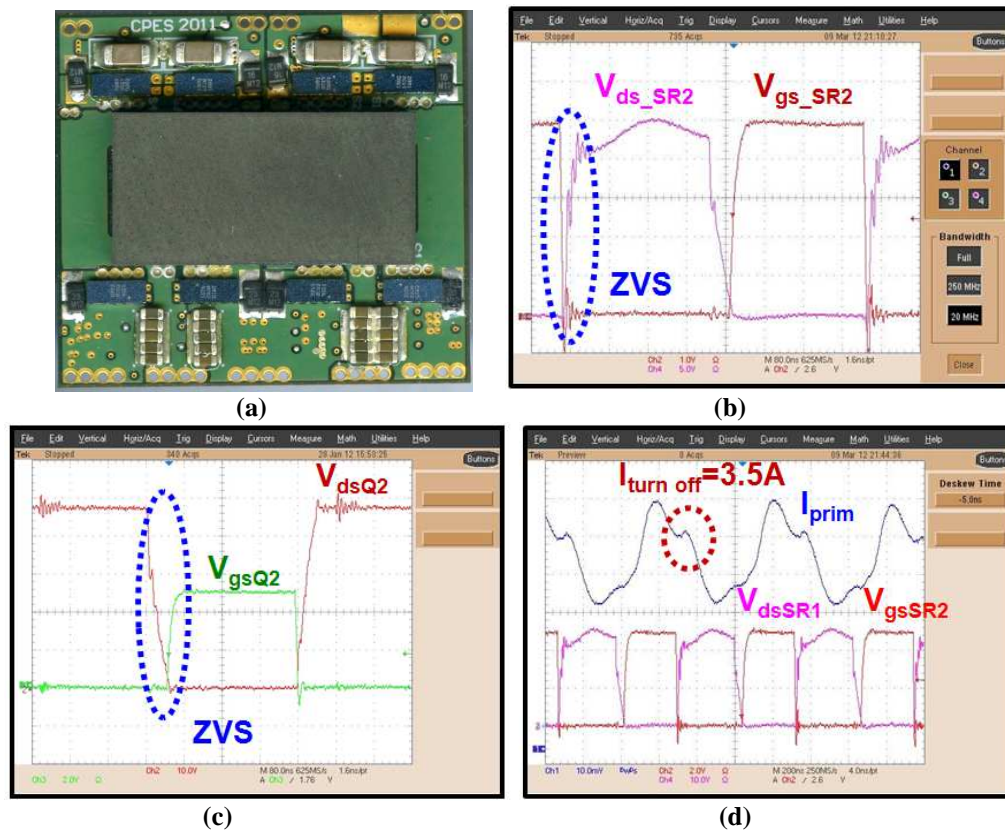


Figure 5.49: (a) Experimental hardware $V_{in}=48\text{V}$, $V_o=12\text{V}$, $F_s=1.6\text{MHz}$ (b) Synchronous rectifier gate and drain voltages achieving ZVS (c) Primary device gate and drain voltages achieving ZVS (d) Primary side current waveform

The efficiency and loss comparison between the two transformer GaN designs are shown in figures 5.50a&b. The results match the expectations from the transformer

simulations/measurements well, with the proposed 2x2:1 transformer structure providing similar light load efficiency from the improved core structures lower core loss and better efficiency at heavy load due to the reduced winding loss.

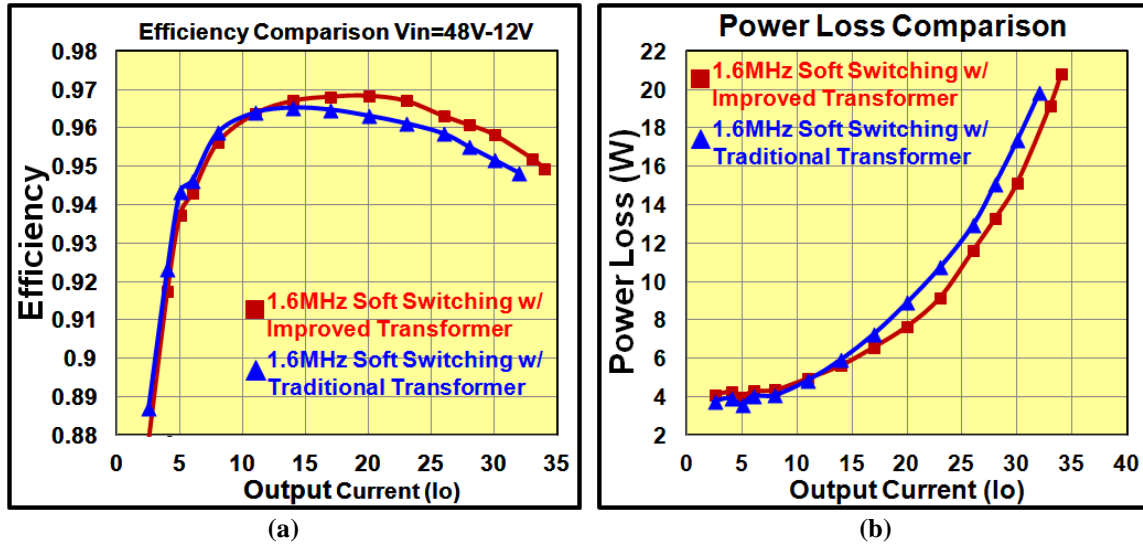


Figure 5.50: Experimental results for $V_{in}=48V$, $V_o=12V$, primary devices: EPC2001, secondary devices :EPC2015, driver:LM5113, $f_s=1.6MHz$ (a) Efficiency comparison between traditional and improved transformer structures (b) Power loss comparison

The efficiency using the GaN devices with the proposed transformer achieves peak efficiency of around 97% at 20A of output current. The comparison between the GaN and Si designs are shown in figures 5.51 a&b. The GaN converter can offer a percent gain in peak efficiency at double the switching frequency of the Si based converter. The improved FOM of the GaN device dramatically reduces the turn off loss and SR driver losses. The GaN suffers from higher SR conduction loss, which could be resolved with an increased number of SR devices being employed. Due to the higher switching frequency and smaller magnetic footprint, the conduction loss of the GaN transformer also is increased over the lower frequency Si design. The volume and footprint comparisons for the 800 kHz and 1.6 MHz transformer designs are given in

table 5.14, the high frequency GaN design provides a 55% smaller transformer footprint and a 62% smaller volume, allowing for improved power density.

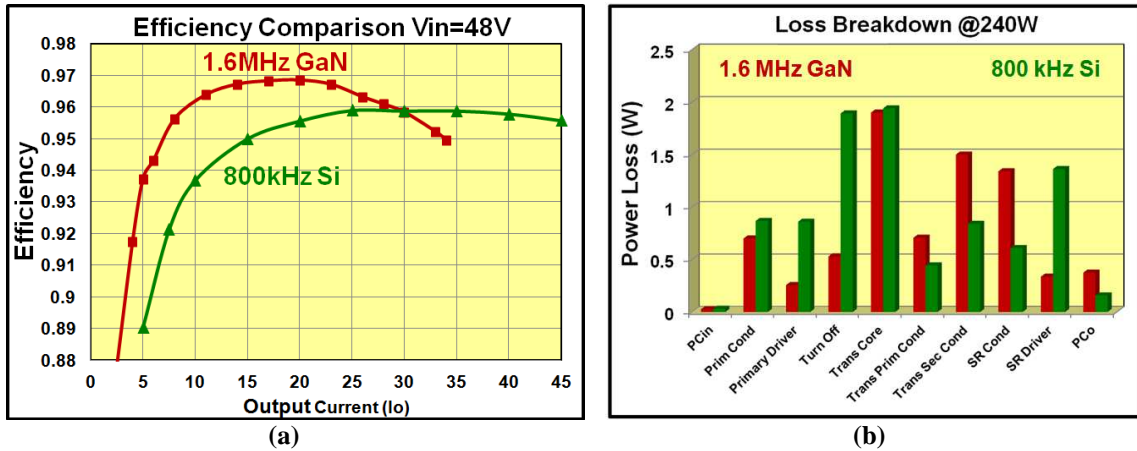


Figure 5.51: Bus converter comparison for 800kHz Si and 1.6MHz GaN with proposed integrated 2x2:1 transformers (a) Efficiency curves $V_{in}=48V$ $V_o=12V$ (b) Loss breakdowns @ 240W

	Transformer Footprint (mm ²)	Transformer Volume (mm ³)
800kHz Si Design	720	7920
1.6MHz GaN Design	320	2970

Table 5.14: Footprint and volume comparison between 800kHz and 1.6MHz designs

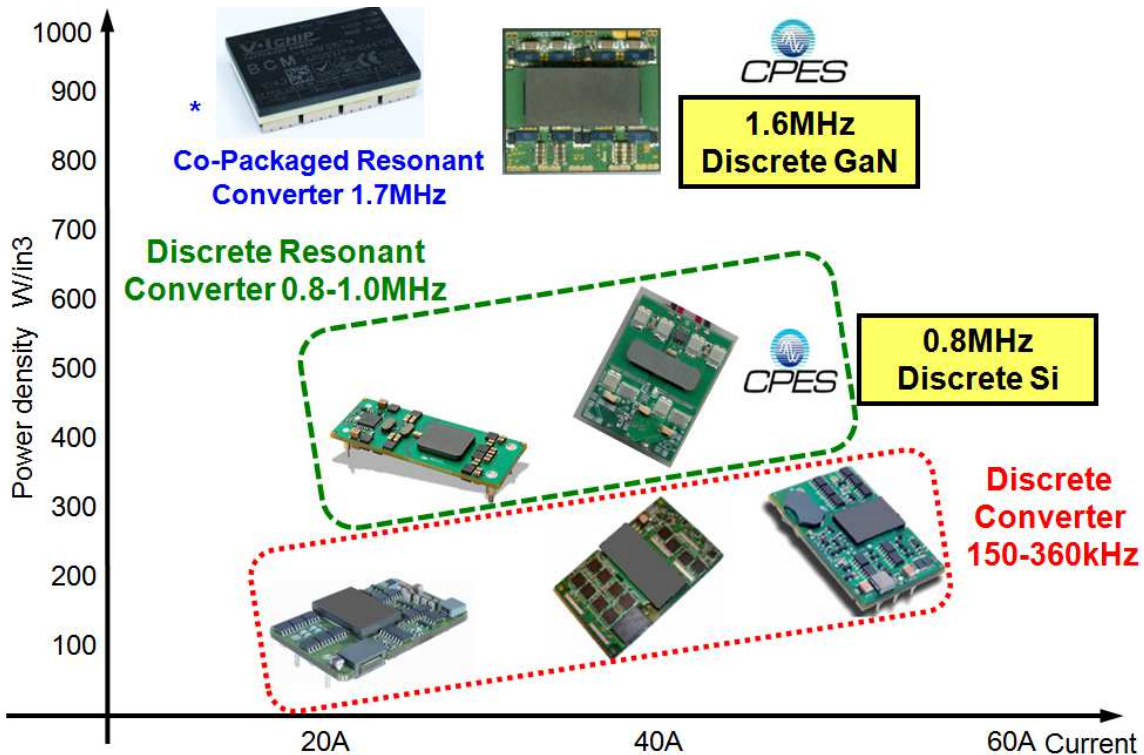


Figure 5.52: Power density comparison of bus converters. *: picture by author.

5.6 Conclusions

In this chapter, high frequency operation of the DCX bus converter for IBA's was considered. First, the impact of frequency on core size was explored, quantifying the transformer size reduction capabilities of higher frequencies. At higher switching frequencies, the transformer winding and termination loss increases and the transformer becomes the major loss component in the circuit. The impact of frequency on winding resistance and termination loss of traditional transformer structures were assessed, identifying potential high frequency improvements capable with matrix transformers.

At higher frequencies, the reduction in core volume facilitates the use of matrix transformers to improve performance. Matrix transformers can offer significantly reduced winding resistance, termination resistance, and leakage inductance, but suffer from increased magnetic volume and higher core loss. An improved transformer structure is proposed in this chapter that can reduce core loss and volume of the traditional matrix transformer design by integrating the matrix transformers into a single core with flux cancellation. The proposed improved structure can offer improved performance and higher power density than the traditional designs.

To further push frequency and power density a 1.6MHz GaN design is explored. This chapter assesses the different transformer structures up to 2MHz, the benefits of soft switching for high frequency GaN devices, and demonstrates the high frequency efficiency improvements possible using low FOM GaN devices. The final demonstration being a $V_{in}=48V$, $V_o=12V$, $I_o=30A$, 1.6MHz GaN converter with an improved integrated transformer offering a power density of $900W/in^3$, a 100% increase over the state of the art Si discrete designs available today.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The demand for future power supplies to achieve higher output currents, smaller size, and higher efficiency cannot be achieved with conventional technologies. There are limitations in the device loss, passive size, packaging parasitics, thermal management, and layout parasitics that must be addressed to push for higher frequencies and improved power density. The focus of this work was improving power density and performance in non-isolated and isolated point of load converters ranging from 10W to 600W. To achieve this objective, different topologies, semiconductors, and magnetic designs were proposed to improve performance and reduce magnetic size, improving power density, in non-isolated point of load and isolated bus converters.

In the second chapter, the use of the three level buck converter to reduce required passives and increase efficiency over the traditional buck converter in low current point of load applications was proposed. This improved performance was achieved by doubling the effective switching frequency, reducing the voltage across the inductor, and reducing the voltage stress across the semiconductors to $0.5V_{in}$, reducing switching loss and allowing for the use of superior low voltage devices. The gain in efficiency and magnetic reduction is verified experimentally.

In chapters three and four, the use of Gallium Nitride (GaN) transistors to push switching frequencies to multi-MHz while maintaining high efficiency for a $V_{in}=12V$, $I_o=20A$ point of load (POL) converter was discussed. These chapters discussed the new GaN device characteristics, compared the different technologies available today, and discussed the benefits and drawbacks of the GaN power devices when compared to Si devices. Module design techniques to minimize layout parasitics were explored to improve high frequency performance and ceramic based designs using Alumina substrates were considered to improve the thermal management in these small, high density modules. The final demonstration being a $V_{in}=12V$, $I_o=20A$ 2MHz converter with an integrated low profile LTCC inductor achieving a power density of $900W/in^3$, a 3x improvement over the state of the art Si based designs.

In the fifth chapter, high frequency operation of the DCX bus converter for IBA's was considered. First, the impact of frequency on core size was explored, quantifying the transformer size reduction capabilities of higher frequencies. At higher switching frequencies with the utilization of soft switching topologies, the transformer winding and termination loss increase significantly and the transformer becomes the major loss component in the circuit. An improved transformer structure is proposed in this chapter that can reduce the core loss and volume of the traditional matrix transformer designs, while offering reduced winding resistance and leakage inductance over the traditional single transformer designs. This is achieved by integrating the matrix transformers into a single core with flux cancellation. To further push frequency and power density a 1.6MHz GaN design is explored. The final demonstration being a $V_{in}=48V$, $V_o=12V$, $I_o=30A$, 1.6MHz GaN converter with an improved integrated transformer offering a

power density of $900\text{W}/\text{in}^3$, a 100% increase over the state of the art Si discrete designs available today.

6.2 Future Work

Future work recommended to build upon the findings in this dissertation is to push for higher levels of integration. The three level converter in chapter 2 demonstrated the benefits of the topology using discrete packaged devices; with the ability to monolithically integrate lateral devices, the benefit of this topology over the discrete or co-packaged trench solutions can show further gains for the three level topology. For the low voltage GaN work, the understanding of the benefits and weaknesses of the GaN devices along with the improvements in packaging and thermal management can be applied to higher voltage applications to improve the level of integration and power density in areas such as 400V offline applications. For 48V isolated converters, the opportunity of further magnetic size reduction utilizing new high frequency magnetic materials should be considered. For the isolated bus converter work, the concept of transformer integration can be applied and extended to higher voltage and higher current applications. To further improve transformer performance at high frequency, methods of interleaving terminations and connection vias to further reduce conduction loss should be explored.

Appendix 1

GaN Analytical Loss Model

To accurately evaluate the impact of the different parasitics on the performance of the GaN device an analytical loss model must be employed. An accurate model was proposed for Si devices in [37][38]. For this work, the model was applied to GaN devices with some modifications. The GaN loss model is detailed in this section.

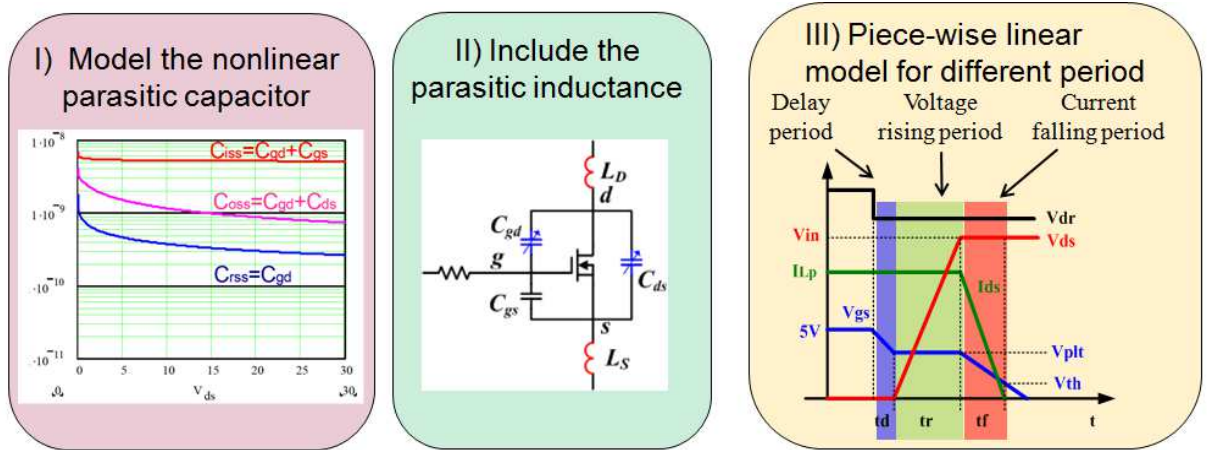


Figure A1.1: Accurate loss model process chart from [37][38]

To accurately model the increased non-linearity of the GaN capacitance, in particular the output capacitance, C_{ds} , more advanced curve fitting was used. C_{ds} is represented by a third order polynomial equation, the relationship for the EPC1015 GaN is:

$$C_{ds}(V_{ds}) = 5.244 \cdot 10^{-5} \cdot V_{ds}^3 - 2.220 \cdot 10^{-3} \cdot V_{ds}^2 + 1.244 \cdot 10^{-3} \cdot V_{ds} + 0.977 \quad (\text{A.1})$$

The GaN gate to source capacitor, C_{gs} , can still be accurately estimated by a constant value. The gate to drain capacitor, C_{gd} , is represented by a second order polynomial. The relationship for C_{gd} is:

$$C_{gd}(V_{ds}) = 2.881 \cdot 10^{-4} \cdot V_{ds}^2 - 0.014 \cdot V_{ds} + 0.220 \quad (\text{A.2})$$

Increasing the number of data points used to model the capacitances is necessary to model the greater non-linearity of the GaN capacitances. The capacitance equations are derived from an increased number of data points, ranging 0V to 30V in 5V steps. Figure 3.20 shows the nonlinear capacitors curves from the EPC1015 datasheet and the curves obtained from the model.

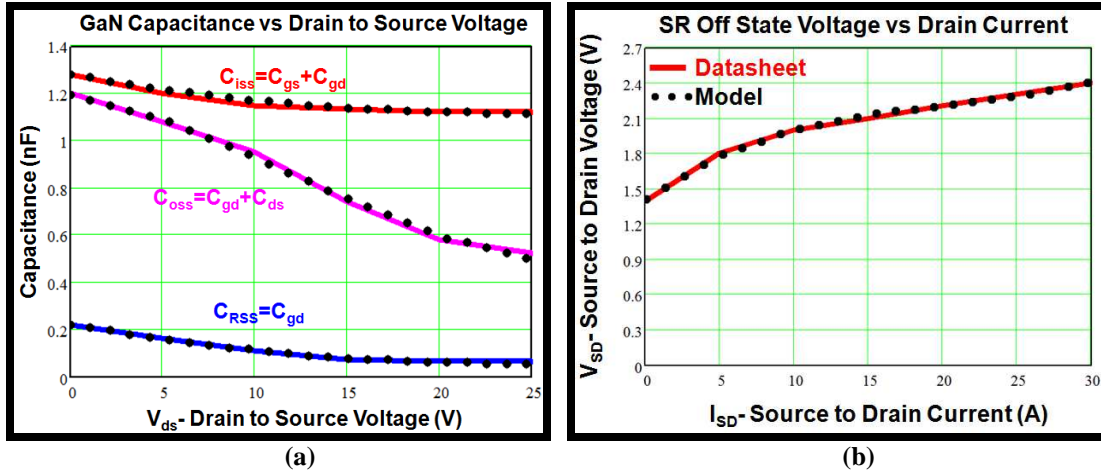


Figure A2.2: (a) Nonlinear capacitance comparison between the data from datasheet (solid lines) and data obtained from GaN model (dotted lines) (b) Reverse drain source characteristics from datasheet (solid lines) and data obtained from GaN model (dotted lines)

The dead time voltage of the GaN transistor was shown to have a large impact on loss earlier in the chapter. To accurately model the loss during the dead time; the source to drain off state voltage drop was modeled using a third order describing function given by equation 3.16, the dead time loss can be found by inserting 3.16 in equation 3.3:

$$V_f(I_o) = 2 \cdot (6.859 \cdot 10^{-5} \cdot I_o^3 - 4.060 \cdot 10^{-3} \cdot I_o^2 + 0.094 \cdot I_o + 1.401) \cdot t_{dead} \cdot f_s \cdot I_o \quad (\text{A.3})$$

The comparison of the loss model and data sheet values for off state source to drain voltage is shown in figure 3.20b. With improved modeling of the capacitances and dead time loss, the GaN loss model's accuracy can be improved.

To accurately model the loss in a high frequency, high density module, the modeling of the parasitics is critical to accuracy. With low loss GaN devices, a greater majority of the loss is a result of the trace inductances and resistances of the PCB design. The circuit layouts and devices were simulated using FEA analysis to accurately model the layout and device parasitics. Figure A2.2 shows the parasitics extracted for generations 1 through 3.

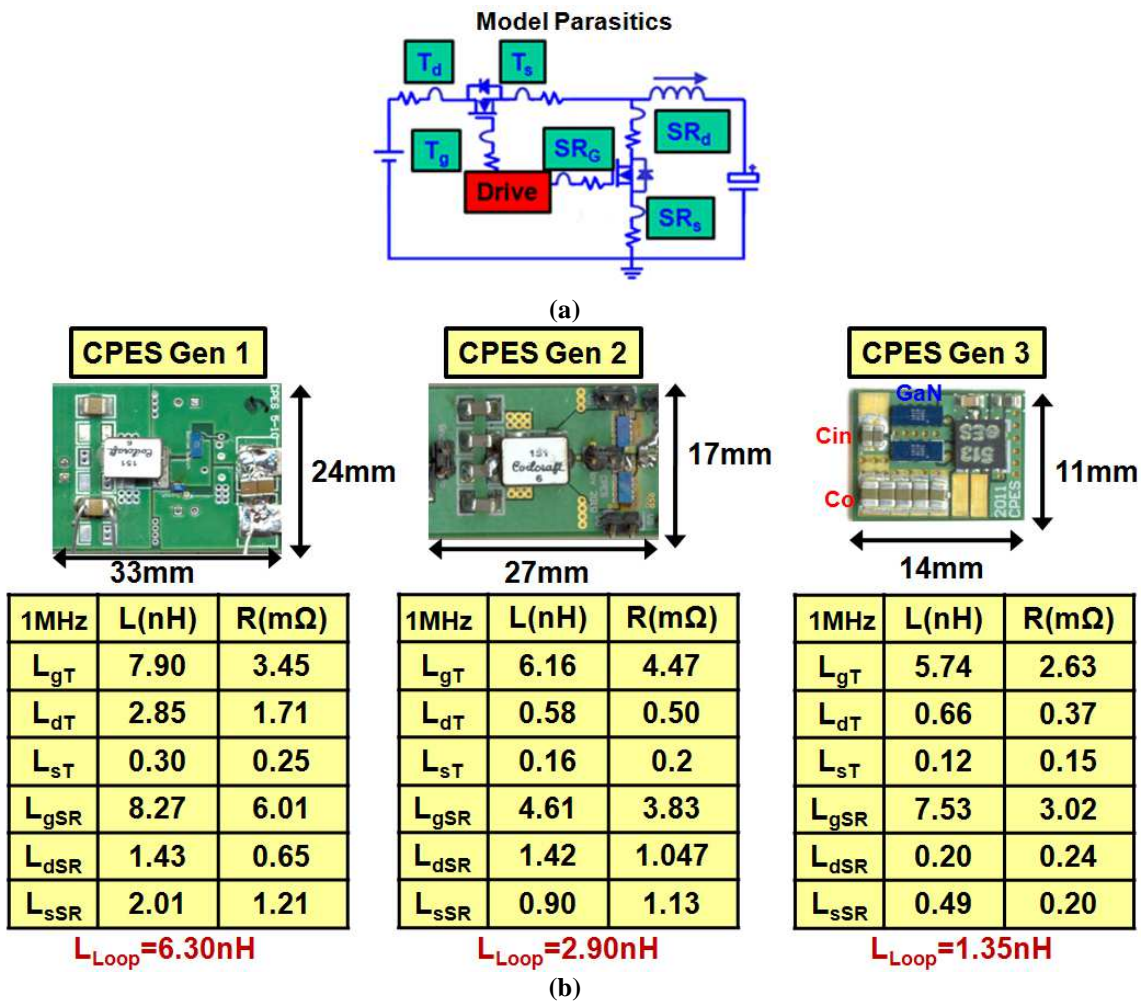


Figure A2.3: (a) Buck converter with parasitics (b) Parasitics extracted for generations 1 through 3

Having accurately modeled the non-linear capacitances, the third quadrant voltage drop of the GaN transistor, and accurately identified the parasitics the analytical loss

model can be applied to estimate switching losses. For the inductances, they can be simplified to:

$$L_S = L_{ST} \quad (\text{A.4})$$

$$L_{Loop} = L_D = L_{DT} + L_{DSR} + L_{SSR} \quad (\text{A.5})$$

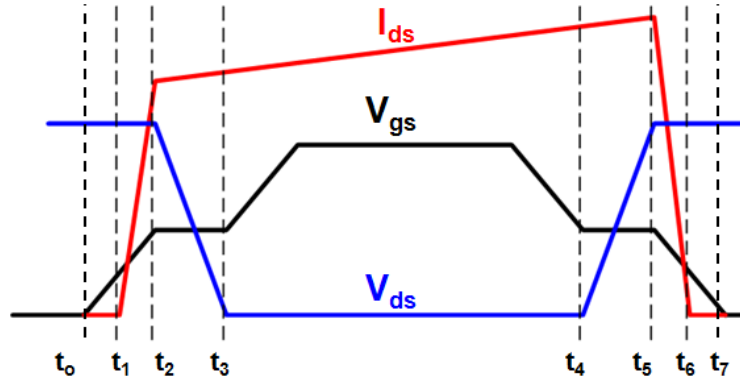


Figure A2.4: Timing diagram for ideal switching waveforms

Turn on Period:

(t_0-t_1) : Delay period: The transistor is operating in cutoff region as an open circuit. When the gate voltage is applied to the gate, the two gates capacitances, C_{gs} and C_{gd} , are in parallel and charged until the gate to source voltage reaches the threshold voltage. The parasitic inductances do not influence during this period because the power stage current is constant. The equations for this period are given as:

$$\tau_G = R_G (C_{gs} + C_{gd}) \quad (\text{A.6})$$

$$V_{gs_ondelay}(t) = V_{dr} \left(1 - e^{-\frac{t}{\tau_G}} \right) \quad (\text{A.7})$$

(t_1-t_2) : The main transition period: When the device reaches the threshold voltage, the drain current begins to flow, the transistor operates in the saturation region as a voltage controlled current source. With a changing drain to source current, the high frequency loop and common source inductances experience voltage that impact switching. The corresponding circuit voltages and currents are derived in [38]:

$$v_{gs}(s) = \frac{V_{dr}}{s^2 \tau_m \tau_{G'} + s \tau_{G''} + 1} \quad (\text{A.8})$$

Where $\tau_m = g_{fs} (L_D + L_S)$, $\tau_{G'} = C_{gd} R_G$, $\tau_{G''} = (C_{gd} + C_{gs}) R_G + g_{fs} L_S$

There are two possible solutions for A.8. If $\tau_{G''}^2 < 4\tau_{G'}\tau_m$, the solution is sinusoidal and given by:

$$v_{gs}(t) = V_{dr} - (V_{dr} - V_{th}) e^{-\frac{t}{\tau_a}} \left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a} \sin(\omega_a t) \right) \quad (\text{A.9})$$

Where $\tau_a = \frac{2\tau_m \tau_{G'}}{\tau_{G''}}$, $\omega_a = \sqrt{\frac{1}{\tau_m \tau_{G'}} - \left(\frac{\tau_{G''}}{2\tau_m \tau_{G'}} \right)^2}$

$$i_d(t) = g_{fs} (v_{gs}(t) - V_{th}) = g_{fs} (V_{dr} - V_{th}) \left(1 - e^{-\frac{t}{\tau_a}} \left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a} \sin(\omega_a t) \right) \right) \quad (\text{A.10})$$

$$v_{ds}(t) = V_{in} - (L_S + L_D) \frac{di_d(t)}{dt} = V_{in} - g_{fs} (V_{dr} - V_{th}) \omega_a (L_S + L_D) e^{-\frac{t}{\tau_a}} \left(1 + \left(\frac{1}{\omega_a \tau_a} \right)^2 \right) \sin(\omega_a t) \quad (\text{A.11})$$

If $\tau_{G''}^2 > 4\tau_{G'}\tau_m$, the solution is exponential and given by:

$$v_{gs}(t) = V_{dr} - (V_{dr} - V_{th}) \frac{e^{-\frac{t}{\tau_b}} \tau_b - e^{-\frac{t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \quad (\text{A.12})$$

Where $\tau_b = \frac{2(\tau_m \tau_{G'})}{\tau_{G''} - (\tau_{G''}^2 - 4\tau_m \tau_{G'})^{1/2}}$, $\tau_c = \frac{2(\tau_m \tau_{G'})}{\tau_{G''} + (\tau_{G''}^2 - 4\tau_m \tau_{G'})^{1/2}}$

$$i_d(t) = g_{fs} (V_{dr} - V_{th}) \left(1 - \frac{e^{-\frac{t}{\tau_b}} \tau_b - e^{-\frac{t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \right) \quad (\text{A.13})$$

$$i_d(t) = g_{fs} (V_{dr} - V_{th}) \left(1 - \frac{e^{-\frac{t}{\tau_b}} \tau_b - e^{-\frac{t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \right) \quad (\text{A.14})$$

The two different inductances have different impacts on the switching loss during this period. The high frequency loop inductance, L_{Loop} , reduces switching loss during turn on; in the main transition period, the induced high frequency loop inductance reduces the device drain to source voltage and limits the current rise time by diverting gate current to the miller capacitance. The theoretical waveforms for this case are shown in figure A2.5, represented by the dashed lines with the ideal waveforms depicted by

solid lines. The common source inductance, L_s , increases switching loss during turn on; the induced common source voltage reduces the available driving current, slowing the current rise time, delaying the voltage falling period.

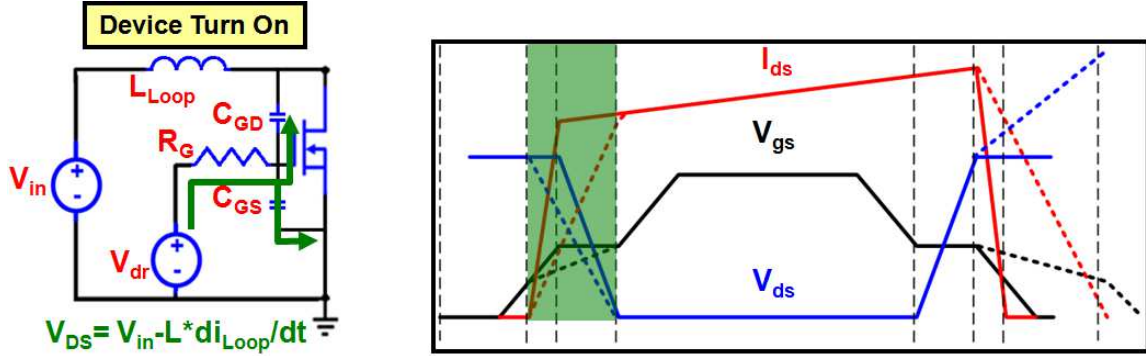


Figure A2.5: Impact of high frequency loop inductance, L_{Loop} , on turn on. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line

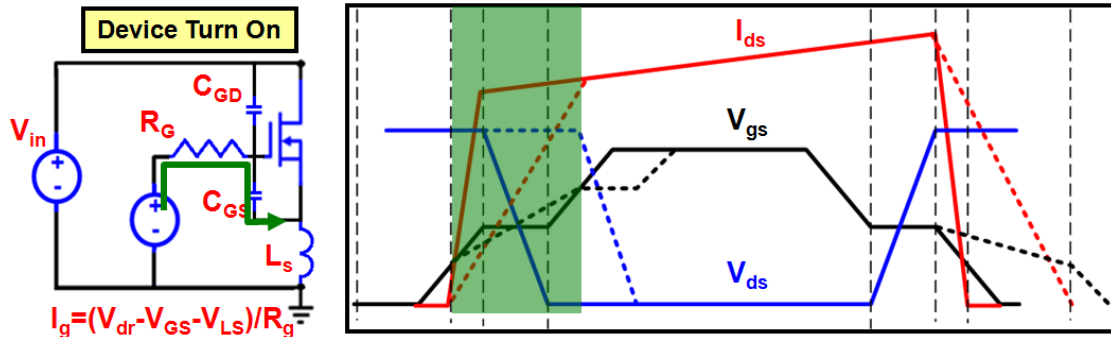


Figure A2.6: Impact of common source inductance, L_s , on turn on. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line

(t_2 - t_3): The main transition period ends when the current reaches the inductor current or the voltage reaches zero. If the drain to source voltage reaches zero before the current reaches the inductor current, the gate to source voltage and drain current can be given by:

$$v_{gs}(t) = \left(V_{dr} - V_{gs_main} - \frac{L_s}{L_D + L_s} V_{in} \right) \left(1 - e^{-\frac{t}{\tau_{G^m}}} \right) + V_{gs_main} \quad (A.15)$$

$$i_d(t) = I_{d_main} + \frac{V_{in}}{L_D + L_s} t \quad (A.16)$$

Where $\tau_{G^m} = R_G (C_{gs} + C_{gd})$, V_{gs_main} is the gate-source voltage at the end of the main transition period, and I_{d_main} is the drain current at the end of main transition period. This period ends when the current reaches the inductor current.

After the current reaches the inductor current, the current begins to ring. The ringing loss can be given by A.17, a detailed derivation is found in [38].

$$E_{ring_turnon} = V_{in} Q_{rr} + \frac{1}{2} Q_{oss_bot} V_{in} \quad (A.17)$$

Turn off Period:

The beginning of the turn off period begins with the falling of the gate to source voltage, which can be given by:

$$V_{gs}(t) = V_{dr} e^{\frac{-t}{\tau_{G^*}}} \quad (A.18)$$

The period ends when the plateau voltage is reached at A.19 and the turn off switching transition begins:

$$V_{gs}(t) = V_{th} + \frac{I_o}{g_{fs}} \quad (A.19)$$

(t₄-t₅): Drain to source voltage rising period. When the gate voltage reaches the plateau voltage, the drain voltage will rise. With no change in drain current during this period the parasitic inductances have no influence, this period ends when the drain to source voltage reaches the input voltage, V_{in}.

$$V_{ds}(t) = \left(\frac{g_{fs} V_{th} + I_o}{1 + g_{fs} R_G} \right) C_{gd} t \quad (A.20)$$

(t₅-t₆): Drain current falling period. When the drain to source voltage reaches the input voltage, the drain current will begin to fall, this period ends when the drain current reaches zero. The switch voltages and currents are given by:

The sinusoidal solutions occur when $\tau_G'^2 < 4\tau_G \tau_m$.

$$V_{gs}(t) = \left(\frac{I_o}{g_{fs}} + V_{th} \right) e^{\frac{-t}{\tau_a}} \left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a} \sin(\omega_a t) \right) \quad (A.21)$$

$$i_d(t) = (g_{fs} V_{th} + I_o) e^{-\frac{t}{\tau_a}} \left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a} \sin(\omega_a t) \right) - g_{fs} V_{th} \quad (\text{A.22})$$

$$v_{ds}(t) = V_{in} + (g_{fs} V_{th} + I_o) \omega_a (L_S + L_D) e^{-\frac{t}{\tau_a}} \left(1 + \left(\frac{1}{\omega_a \tau_a} \right)^2 \right) \sin(\omega_a t) \quad (\text{A.23})$$

The exponential solutions occur when $\tau_G'^2 > 4\tau_G \tau_m$.

$$v_{gs}(t) = \left(\frac{I_o}{g_{fs}} + V_{th} \right) \frac{e^{-\frac{t}{\tau_b}} \tau_b - e^{-\frac{t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \quad (\text{A.24})$$

$$i_d(t) = (g_{fs} V_{th} + I_o) \left(1 - \frac{e^{-\frac{t}{\tau_b}} \tau_b - e^{-\frac{t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \right) - g_{fs} V_{th} \quad (\text{A.25})$$

$$v_{ds}(t) = V_{in} + (g_{fs} V_{th} + I_o) (L_S + L_D) \frac{e^{-\frac{t}{\tau_b}} - e^{-\frac{t}{\tau_c}}}{\tau_b - \tau_c} \quad (\text{A.26})$$

The two different inductances negatively impact the switching loss during this period. The high frequency loop inductance, L_{Loop} , increases switching loss during turn on; in the current falling period, the induced high frequency loop inductance increases the device drain to source voltage and limits the current fall time by diverting gate current to the miller capacitance. The theoretical waveforms for this case are shown in figure A2.5, represented by the dashed lines with the ideal waveforms depicted by solid lines.

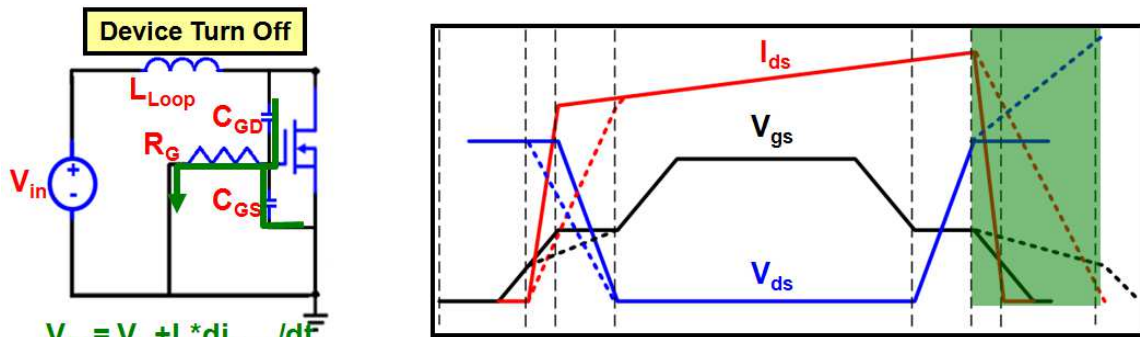


Figure A2.7: Impact of high frequency loop inductance, L_{Loop} , on turn off. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line

The common source inductance, L_s , increases switching loss during turn on; the induced common source voltage reduces the available driving current, slowing the current fall time, delaying the voltage falling period. The negative impact from both parasitic inductances during the turn off period results in a larger turn off loss for a synchronous buck converter.

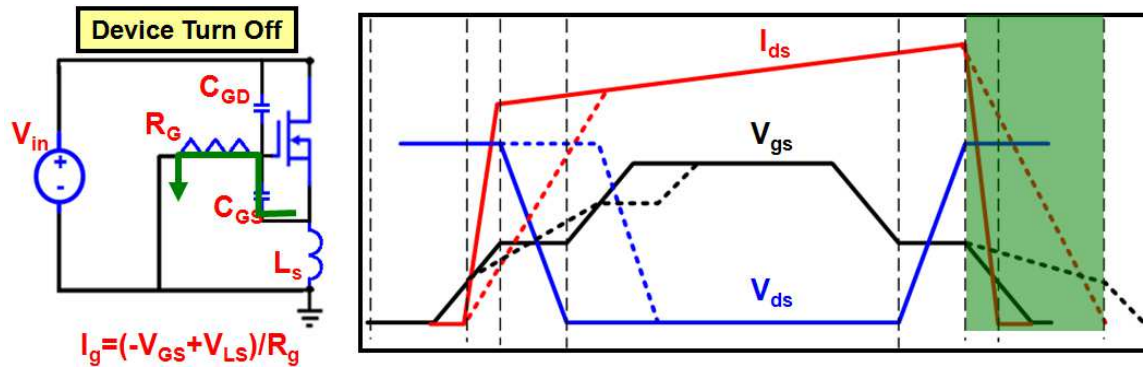


Figure A2.8: Impact of common source inductance, L_s , on turn off. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line

After the current reaches zero the voltage continues to ring, the loss during this period is given by:

$$E_{ring_turnoff} = \frac{1}{2} Q_{V_{peak}} (V_{peak} - 2 V_{in}) + \frac{1}{2} Q_{V_{in}} V_{in} \quad (A.27)$$

Where V_{peak} is reached at the end of the drain current falling period when the current reaches zero.

The verification of the loss model is confirmed in chapter 3 and this model is used to evaluate the loss for various parasitics and perform loss breakdowns on the various designs in this dissertation. For the high frequency designs, accurate parasitic extraction is critical and discussed in detail in chapter 4.

References

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