Current-Mode Control:
Modeling and its Digital Application

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(Abstract)

Due to unique characteristics, current-mode control architectures with different implementation approaches have been widely used in power converter design to achieve current sharing, AVP control, and light-load efficiency improvement. Therefore, an accurate model for current-mode control is indispensable to system design due to the existence of subharmonic oscillations. The fundamental difference between current-mode control and voltage-mode control is the PWM modulation. The inductor current, one of state variables, is used in the modulator in current-mode control while an external ramp is used in voltage-mode control. The dynamic nonlinearity of current-mode control results in the difficulty of obtaining the small-signal model for current-mode control in the frequency domain. There has been a long history of the current-mode control modeling. Many previous attempts have been made especially for constant-frequency peak current-mode control. However, few models are available for variable-frequency constant on-time control and V^2 current-mode control. It's hard to directly extend the model of peak current-mode control to those controls. Furthermore, there is no simple way of modeling the effects of the capacitor ripple which may result in subharmonic oscillations in V^2 current-mode control. In this dissertation, the primary objective to investigate a new and general modeling approach for current-mode control with different implementation methods.

First, the fundamental limitation of average models for current-mode control is identified. The sideband components are generated and coupled with the fundamental component through the PWM modulator in the current loop. Moreover, the switching frequency harmonics cannot be ignored in the current loop since the current ripple is used for the PWM modulation. Available average models failed to consider the sideband effects and high frequency harmonics. Due to the complexity of the current loop, it is difficult to

analyze current loop in the frequency domain. A new modeling approach for current-mode control is proposed based on the time-domain analysis. The inductor, the switches and the PWM modulator are treated as a single entity to model instead of breaking them into parts to do it. Describing function method is used. Proposed approach can be applied not only to constant-frequency modulation but also to variable-frequency modulation. The fundamental difference between different current-mode controls is elaborated based on the models obtained from the new modeling approach.

Then, an equivalent circuit representation of current-mode control is presented for the sake of easy understanding. The effect of the current loop is equivalent to controlling the inductor current as a current source with certain impedance. The circuit representation provides both the simplicity of the circuit model and the accuracy of the proposed model.

Next, the new modeling approach is extended to V^2 current-mode control based on similar concept. The model for V^2 current-mode control can accurately predict subharmonic oscillations due to the influence of the capacitor ripple. Two solutions are discussed to solve the instability issue.

After that, a digital application of current-mode control is introduced. High-resolution digital pulse-width modulator (DPWM) is considered to be indispensable for minimizing the possibility of unpredicted limit-cycle oscillations, but results in high cost, especially in the application of voltage regulators for microprocessors. In order to solve this issue, a fully digital current-mode control architecture which can effectively limit the oscillation amplitude is presented, thereby greatly reducing the design challenge for digital controllers by eliminating the need for the high-resolution DPWM. The new modeling strategy is also used to model the proposed digital current-mode control to help system design.

As a conclusion, a new modeling approach for current-mode control is fully investigated. Describing function method is utilized as a tool in this dissertation. Proposed approach is quite general and not limit by implementation methods. All the modeling results are verified through simulation and experiments.

TO MY FAMILY

My Parenets: Hongmao Li and Xiuhua Li

My Parents-in-law: Ligang Mi and Fulan Cao

My Wife: Na Mi

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Chapter 1. Introduction

1.1 Research Background: Current-Mode Control

Current-mode control has been widely used in the power converter design for several decades [1][2][3][4][5][6][7][8][9]. The fundamental difference between voltage-mode control and current-mode control is the PWM modulation. In voltage mode control, as shown in Figure 1.1, a fixed external ramp is used to compare with the control signal v_c to generate the duty cycle in the PWM modulator. Usually, there is only one loop in voltage-mode control. However, in current-mode control, as shown in Figure 1.2, the sensed inductor-current ramp, which is one of state variables, is used in the PWM modulator. Generally speaking, two-loop structure has to be used in current-mode control.
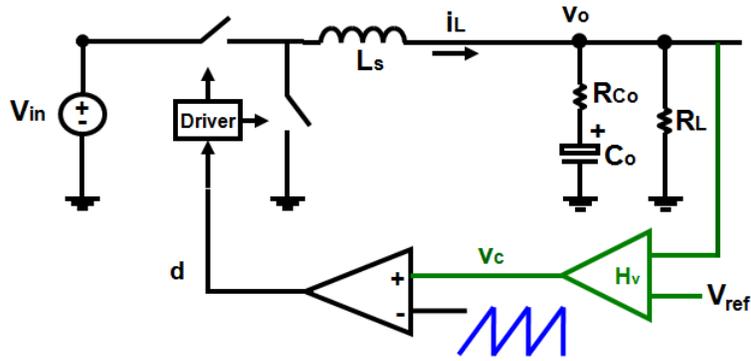
(a)
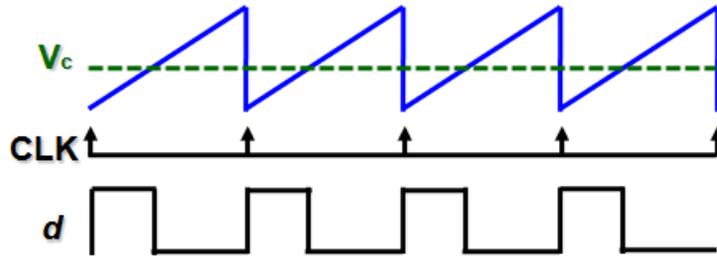
(b)

Figure 1.1. Voltage-mode control: (a) control structure, and (b) modulation principle

(a)

(b)
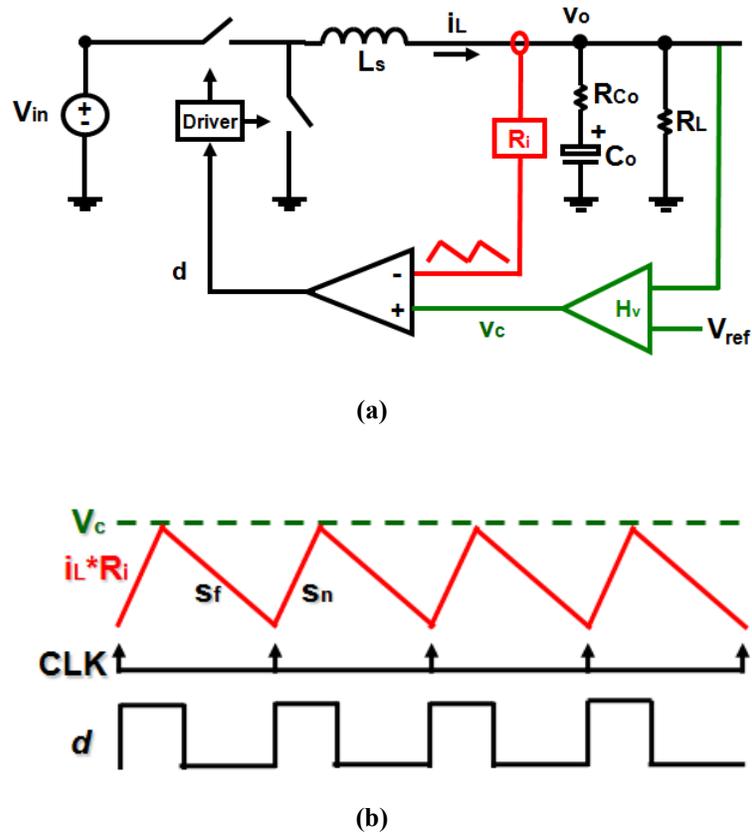
Figure 1.2. Current-mode control: (a) control structure, and (b) modulation principle

There are many different ways to implement current-mode control. One of the earliest implementations is known as the "standardized control module" (SCM) implementation [4]. The inductor-current ramp is obtained by integrating the voltage across the inductor. Essentially, only AC information of the inductor current is maintained in this implementation. Later, the "current injection control" (CIC) was proposed in [5]. The active switch current which is part of the inductor current is sensed usually with a current transformer or resistor in series with the active switch. During the on-time period, the active switch current is the same as the inductor current, so peak current protection can be achieved by the limited value of the control signal v_c. Except the DC operation, systems behave the same as the SCM implementation.

Different modulation schemes in current-mode control were summarize in [6], including peak current-mode control, valley current-mode control, constant on-time control, constant off-time control, and hysteretic control, as shown in Figure 1.3. The first two

schemes belong to the constant-frequency modulation, and the rest belong to the variable-frequency modulation.
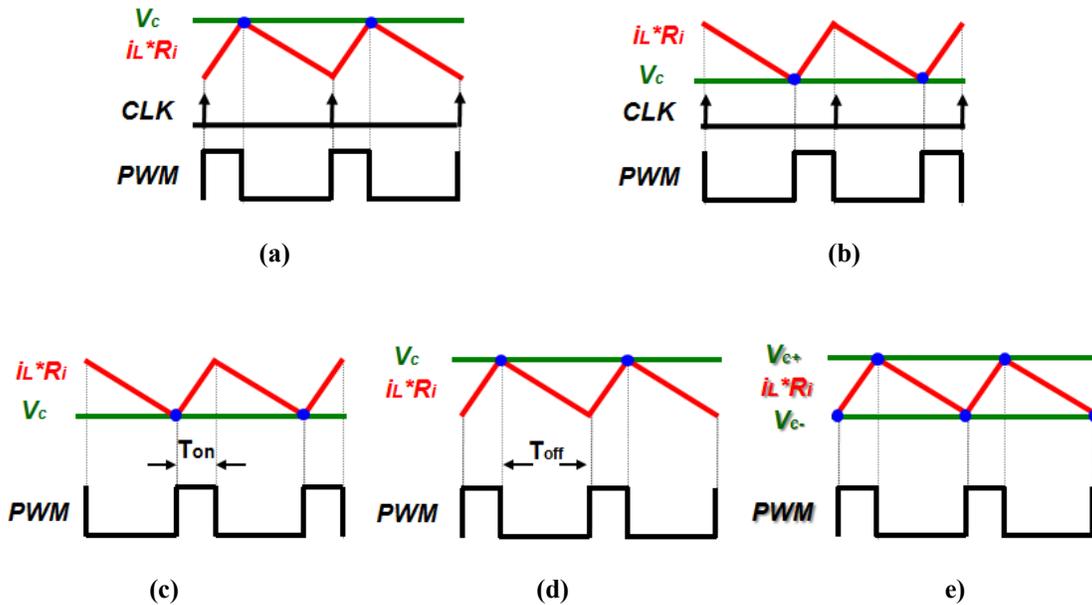
Figure 1.3. Different modulation schemes in current-mode control: (a) peak current-mode control, (b) valley current mode control, (c) constant on-time control, (d) constant off-time control, and (e) hysteretic control

Other than those current-mode controls mentioned above, the "average current-mode control" is somewhat different [7][8]. A low-pass filter is added into the feedback path of the inductor current in order to control the average inductor current and improve the noise immunity. Similar concept was also proposed as the "charge control" [9] to control the average input current.

1.2   Applications of Current-Mode Control

Due to its unique characteristics, current-mode control is indispensable to power converter design in almost every aspect. A few applications of current-mode control are introduced in the following paragraphs.

A. Current sharing

With the development of information technology, telecom, computer and network systems have become a large market for the power supply industry [10]. Power supplies for the telecom, computer and network applications are required to provide more power with less size and cost [11][12]. To meet these requirements, the distributed power system (DPS) is widely adopted. Instead of using a single bulky power supply to provide the final voltages required by the load, the distributed power system is characterized by distribution of the power processing functions among many power processing units [13]. One typical DPS structure based on the modular approach is the intermediate bus structure [14][15], as shown in Figure 1.4. Because of this modular approach, DPS system has many advantages comparing with conventional centralized power systems, such as less distribution loss, faster current slew rate to the loads, better standalization and ease of maintenance [16][17].
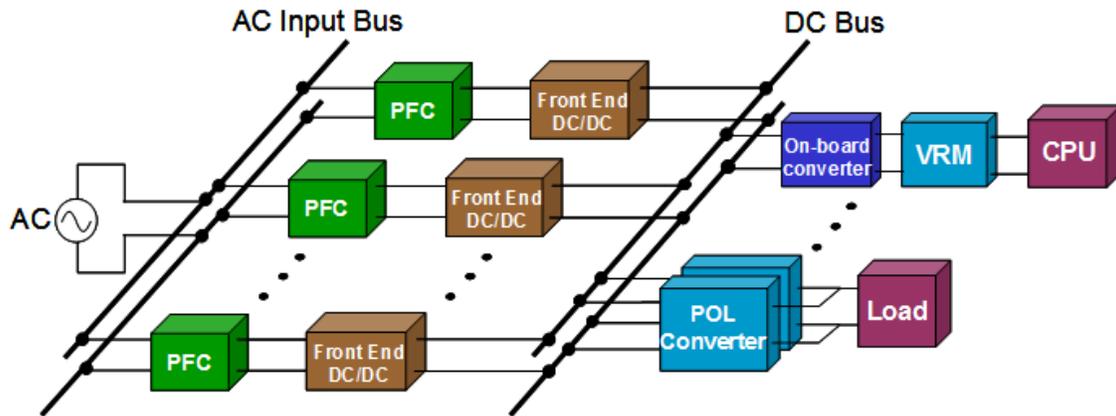
Figure 1.4. A typical distributed power system

Paralleling module approach for point-of-load (POL) converters has been successfully used in various power systems. The multi-phase buck converter topology can be treated as an example to demonstrate the benefits of this approach in terms of thermal management, reliability and power density. However, it is the nature of voltage sources that only one unit can establish the voltage level in a paralleling system. Even a small difference between paralleled modules will cause the current imbalanced. With unequal load sharing, the stress placed on the individual module will be different, resulting in some units operating with higher temperatures — a recognized contributor to reduced reliability.

Therefore, the challenge in paralleling modular supplies is to ensure predictable, uniform current sharing-regardless of load levels and the number of modules.

There are many methods to achieve current sharing among different modules (phases). One of the most popular methods is the active current sharing method with current-mode control [18]. As shown in Figure 1.5, a current sharing bus is easily built by the control signal in peak current-mode control. It usually provides a common current reference. Each phase then adjust its own control to follow this common reference thus the load current will finally evenly distributed among these phases.
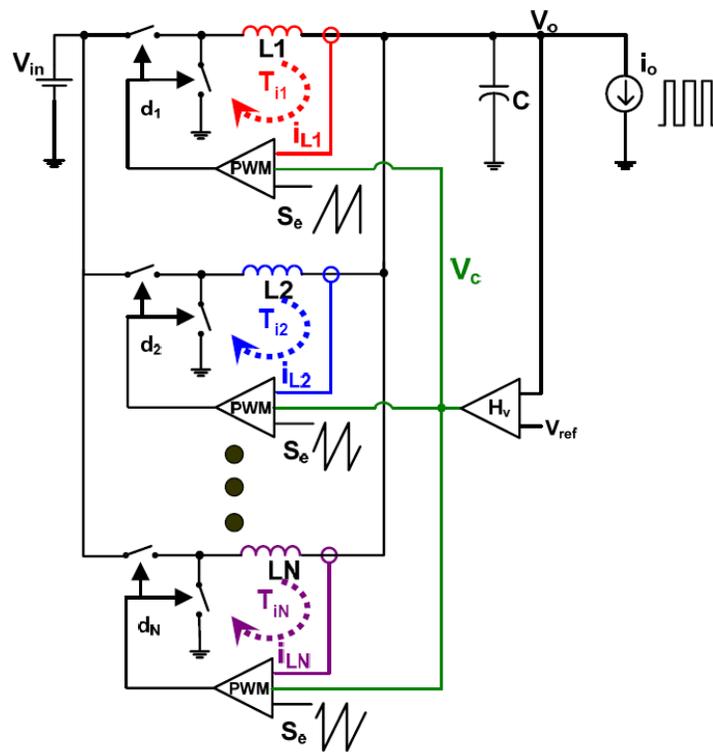
Figure 1.5. A multi-phase buck converter with peak current-mode control

B. Adaptive Voltage Positioning (AVP) Control

In order to provide power to the microprocessor with high current and low voltage demand, a dedicated power supply named voltage regulator (VR) is used. In low-end computer systems, since there is no isolation requirement, multi-phase buck converters are widely used in VRs because of their simple structure, low cost and low conduction loss. Current VR faces the stringent challenge of not only high current but also a strict transient

response requirement. In the Intel VRD 11.0 specification, the maximum current slew rate is 1.9A/ns at the CPU socket [19]. Figure 1.6 shows the VR output load line from the Intel VRD 11.0 specification. The vertical axis is the VR output voltage deviation from the voltage identification (or VID, which is a code supplied by the processor that determines the reference output voltage), and the horizontal axis is the CPU current (I_{CC}). The maximum, typical and minimum load lines are defined by:

$$V_{max} = VID - R_{LL} \cdot I_{cc} \tag{1.1}$$

$$V_{typ} = VID - R_{LL} \cdot I_{cc} - TOB \tag{1.2}$$

$$V_{min} = VID - R_{LL} \cdot I_{cc} - 2TOB \tag{1.3}$$

where R_{LL} is the load-line impedance and TOB is the tolerance band. The VR output voltage should be within this load line band for both static and transient operation.
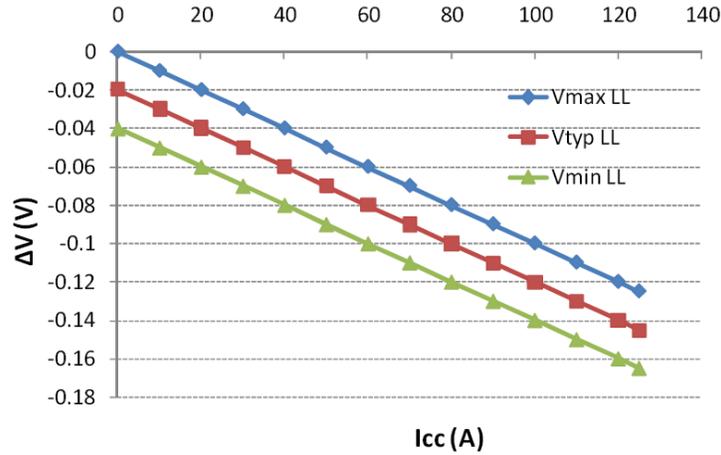
Figure 1.6. Load-line specification of Intel VRD 11.0

Figure 1.7 shows the relationship between the load-line specifications and the time domain waveforms [19]. When the CPU current ($I_o = I_{cc}$) is low, the VR output voltage should be high, and when the CPU current is high, the VR output voltage should be low. The VR output voltage must also follow the load line during the transient, with one exception. During the load step-down transient, the VR output voltage can be over V_{max} load line for 25µs. This overshoot should not exceed the overshoot relief, which is VID+50mV in the VRD 11.0 specification.
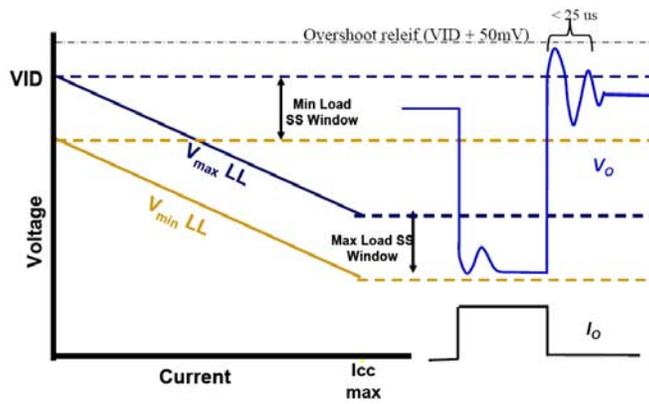
Figure 1.7. The relationship between the load-line specifications and time domain waveforms

Adaptive voltage positioning (AVP) control is widely used to achieve constant-output impedance design to meet the load-line requirement [19][20][21][22][23][24]. Current-mode control architecture shown in Figure 1.8 is endowed with the capabilities of controlling both the output voltage and the inductor current, which is one of key factors to achieve AVP control.
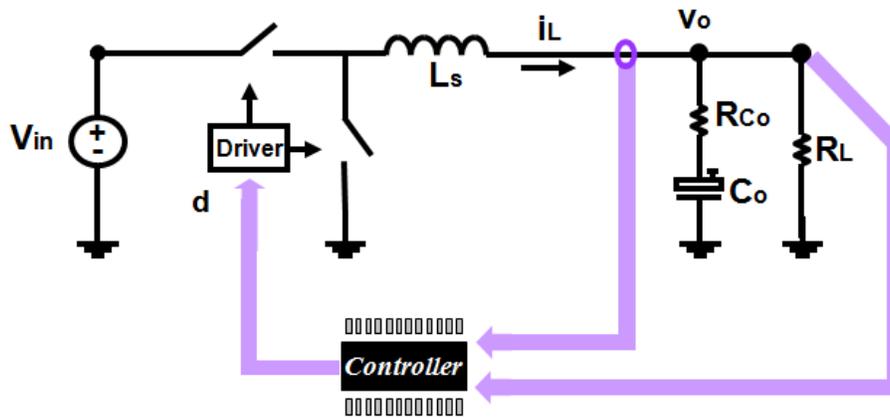
Figure 1.8. Current-mode control to achieve AVP

C. Light-load efficiency improvement

With the emergence of important climate saving legislation such as 80 PLUS, Climate Savers and EnergyStar' 5, it's time to reexamine DC-DC systems to improve efficiency across the entire load spectrum.

Focusing on a typical notebook personal computer, the CPU goes into sleep states very frequently, as shown in Figure 1.9. When the CPU goes into sleep mode, the clock frequency and the supply voltage are reduced, which means power consumption of the CPU is decreased to a very low level. Therefore, light-load efficiency of the VR is very important for battery life extension.
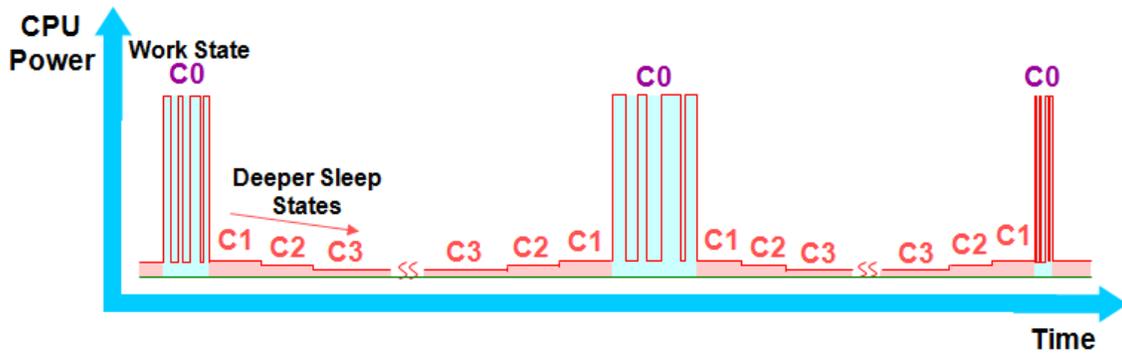
Figure 1.9. CPU power chart

Figure 1.10 shows an example of the light-load efficiency expectation from Intel.
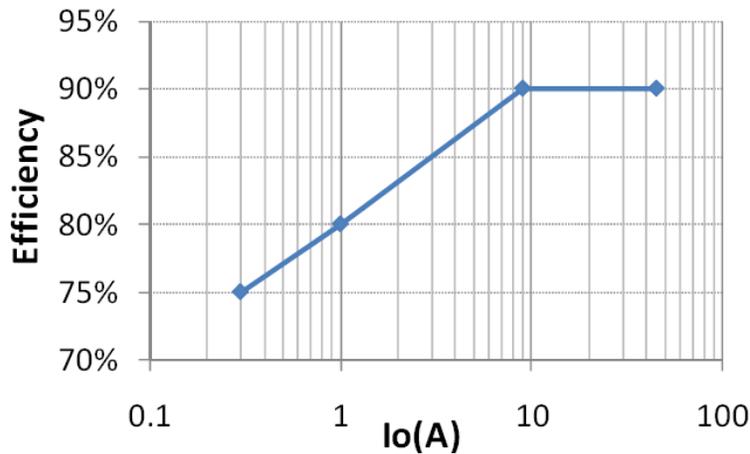
Figure 1.10. Light-load efficiency target for laptop voltage regulators

The expected efficiency is 90% for the active state (9A to 45A), 80% at 1A, and 75% at 300mA for the sleep states. Since the fixed power loss, which consists of gate driving losses, core losses, etc., becomes dominant at light load, it is very challenging to meet the efficiency requirement.

At the light load condition, switching-related loss dominates the total loss. Thus, constant on-time control is widely used to improve light-load efficiency, since the switching frequency can be lowered to reduce switching-related loss [25][26][27][28][29][30]. The general constant on time control structure is shown in Figure 1.11.
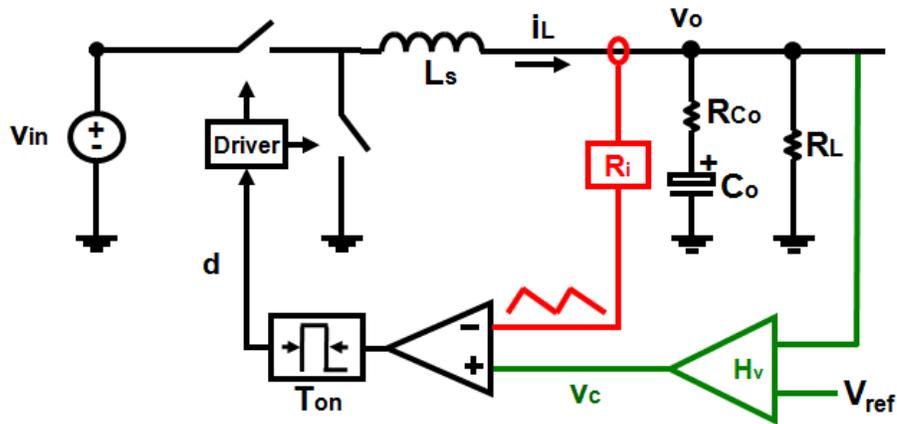
Figure 1.11. Constant on-time control

The V^2 type implementation of constant on-time control is used for practical design, as shown in Figure 1.12.
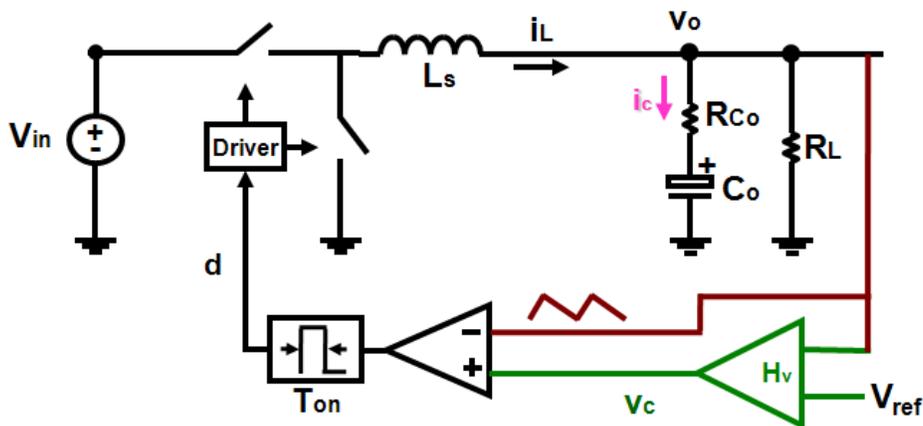
Figure 1.12. V^2 constant on-time control

Equivalent series resistor (ESR) of the output capacitor is used as a sensing resistor. It means that the output voltage ripple, which includes the inductor-current information,

can be directly used as the ramp for the PWM modulation. The benefits of the V^2 type implementation is its simplicity and capability of automatic switching frequency variation. The switching frequency is related to the load at the discontinuous conduction mode (DCM), as shown in Figure 1.13: the lighter the load is, the lower the switching frequency.
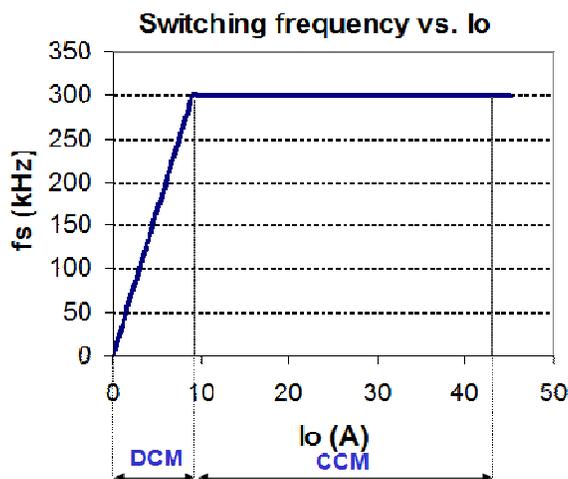
Figure 1.13. Switching frequency variation of V^2 constant on-time control

D. Digital implementation

Recently, digital power supplies have become more and more popular in the field of power electronics. Power supplies with a digital controller can overcome many drawbacks of those with an analog controller, and provide more functions that can improve the system performance, such as noise immunity, programmability and communication capability.

However, the design of a low-cost and high-performance digital controller is still a challenge. At present, voltage-mode control architecture is widely used in digital controller design. High-resolution digital pulse-width modulator (DPWM) is considered to be indispensable for minimizing the possibility of unpredicted limit-cycle oscillations, but results in high cost, especially in the application of the voltage regulator (VR) for microprocessors. Figure 1.14 shows the clock frequency requirement to achieve 3mV output-voltage resolution under different switching frequencies in the VR application (assuming $V_{in} = 12V$). As shown in the graph, even for a 300-KHz switching frequency VR, the system clock frequency has to be 1.2 GHz to meet the resolution requirement. Over GHz clock frequency is not feasible for practical implementation.
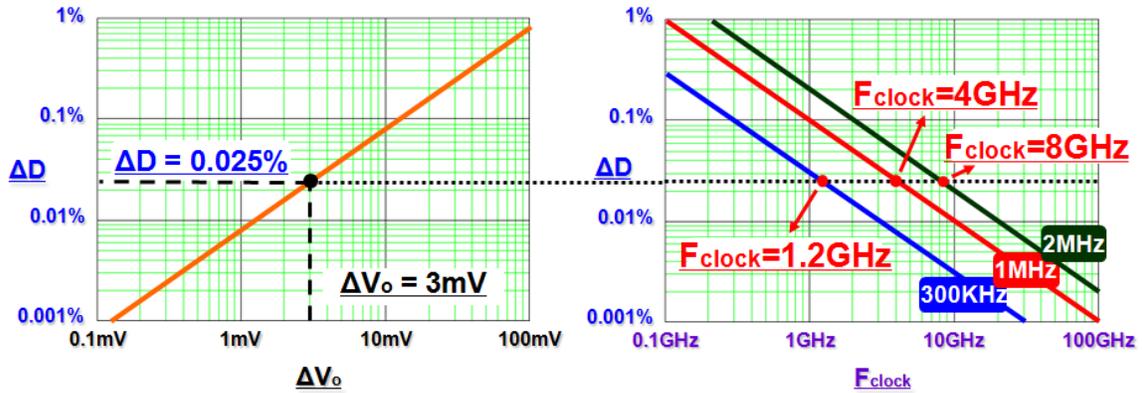
Figure 1.14. System clock frequency requirement for digital controllers with voltage-mode control

One of the keys to solving this issue is the selection of suitable digital control architecture. Current-mode control provides more opportunities for the digital implementation. In this dissertation, a digital current-mode control structure is proposed based on V^2 current-mode control to eliminate the need for high-resolution DPWM, as shown in Figure 1.15. The clock frequency requirement is reduced from over 1 GHz to tens of MHz. Details about the digital implementation will be introduced in Chapter 5.
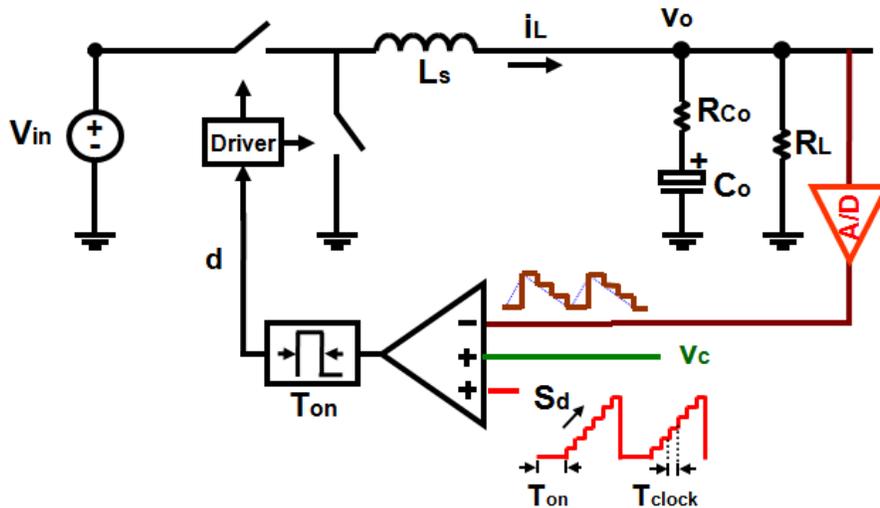
Figure 1.15. Proposed digital current-mode control architecture

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1.3   Review of Previous models for Current-Mode Control

Due to the popularity of current-mode control, an accurate model for current-mode control is indispensable to system design.

As mentioned before, the fundamental difference between voltage-mode control and current-mode control is the PWM modulation. A fixed external ramp is used in voltage-mode control, while the inductor current ramp, which is one of state variables, is used in current-mode control. This dissimilarity brings a unique characteristic of subharmonic oscillations in current-mode control. As shown in Figure 1.16, when the duty cycle d is greater than 0.5 in peak current-mode control, subharmonic oscillations occur. It means that there exists instability issue when the current loop is closed. Practically, an external ramp is added to help stabilize the system. Besides, the inductor current is influenced by the input voltage and the output voltage, which makes the PWM modulator highly nonlinear and hard to model. Due to the comlication mentioned above, exploration of a small-signal model for current-mode control in the frequency domain is a challenge to researchers.

(a)

(b)
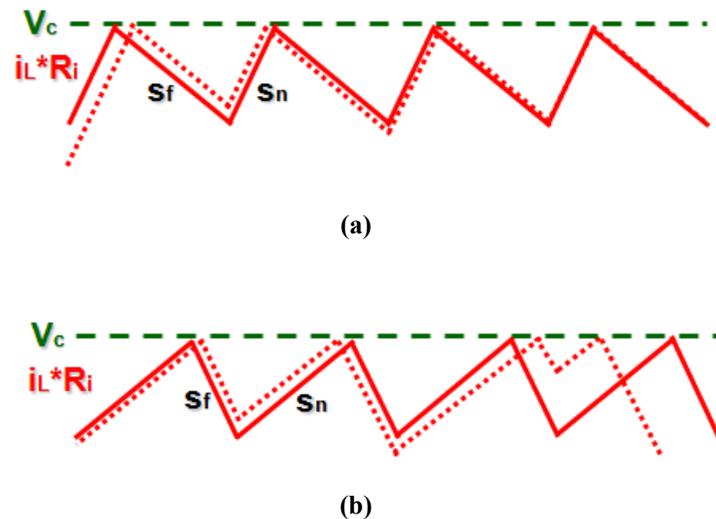
Figure 1.16. Subharmonic oscillations in peak current-mode control: (a) D < 0.5, and (b) D>0.5

Many previous attempts have been made to model current-mode control, particularly peak current-model control. The modeling methodologies can be categorized into several groups and listed as follows.

A. "Current source" model

The "current-source" concept is the simplest way to model current-mode control [40]. Based on this concept, the inductor current is treated as a well-controlled current source, as shown in Figure 1.17, which is a simple interpretation of current-loop effects. This model provides very good physical insight to power supply designers. However, this model is is too simple to predict subharmonic oscillations and the audio susceptibility.

(a)

(b)
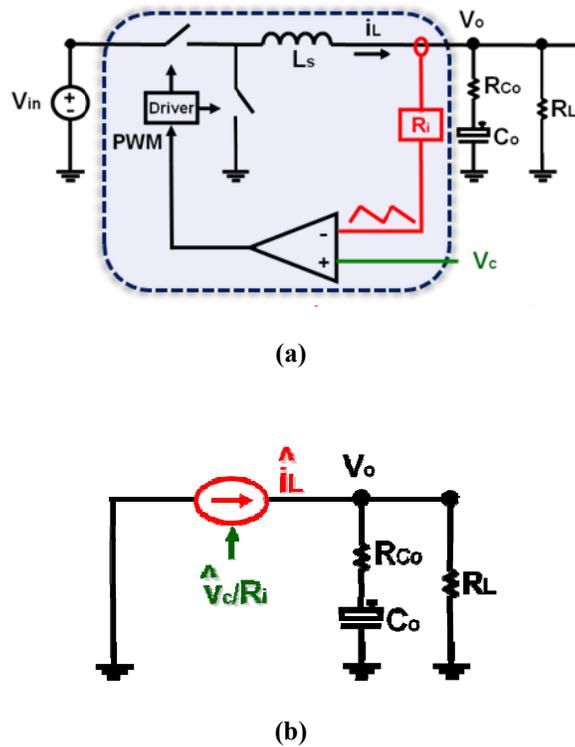
Figure 1.17. current-mode control: (a) control structure, (b) "current source" concept

B. Average model

Due to the presence of the low-pass filter in the power stage, the average concept is sucessfully used in the modeling of power converters [31][32][33][34][35][36][37][38]. The average models for peak current-mode control are built upon the average model for the power stage [39][40][41][42][43][44][45][46][47][48][49][50]. The sensed inductor-current information is fed back to the modulator directly, as shown in Figure 1.18. The relationship between the inductor current, the control voltage and the duty cycle, e.g. the

modulator gain F_m, is different due to different modeling processes by using geometrical calculations. The loop gain is used to represent the influence of the current loop.
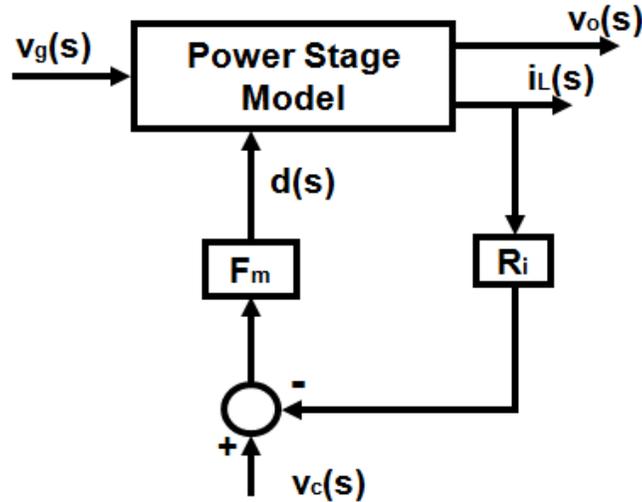
Figure 1.18. Average model for current-mode control

In order to model the effect of the variation of the inductor current ramp, two additional feed forward gain and feedback gain are added by R. D. Middlebrook [41].
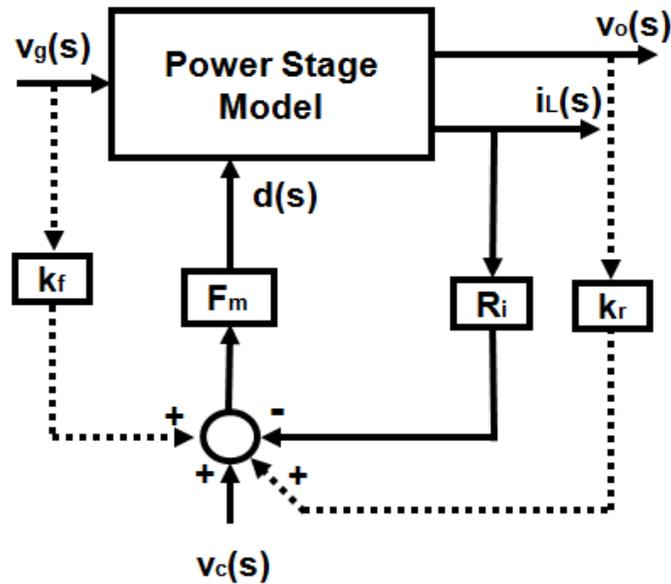
Figure 1.19. Average model for current-mode control with two additional feed forward gain and feedback gain

The low-frequency response can be well predicted by the average models. However, one common issue of the average models is that they failed to predict the high-gain effect at half of the switching frequency, which means that they can't predict subharmonic oscillations in peak current-mode control, as shown in Figure 1.20.
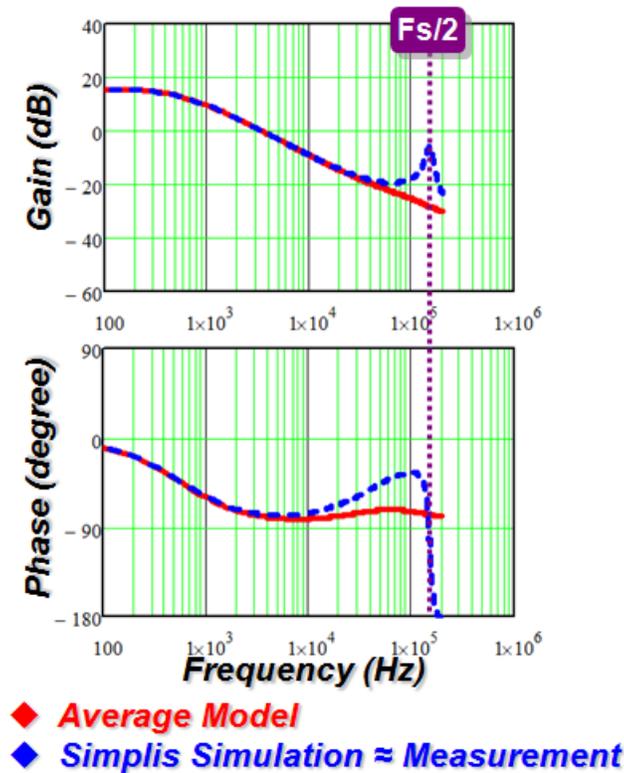
Figure 1.20. Control-to-output transfer function comparison (D=0.45)

C. Discrete-time model

Discrete-time analysis is applied to model current-mode control. In [51][52], F. C. Lee utilized numerical techniques to obtain the transfer fucntion, while it is too complicated to be used in practical design.

The analytical prediction of current loop instability in peak current-mode control was firstly achieved by the discrete-time model proposed by D. J. Packard [34] and A. R. Brown [53]. The analysis was performed based on the time-domain waveform of the inductor current, as shown in Figure 1.21.

(a)

(b)
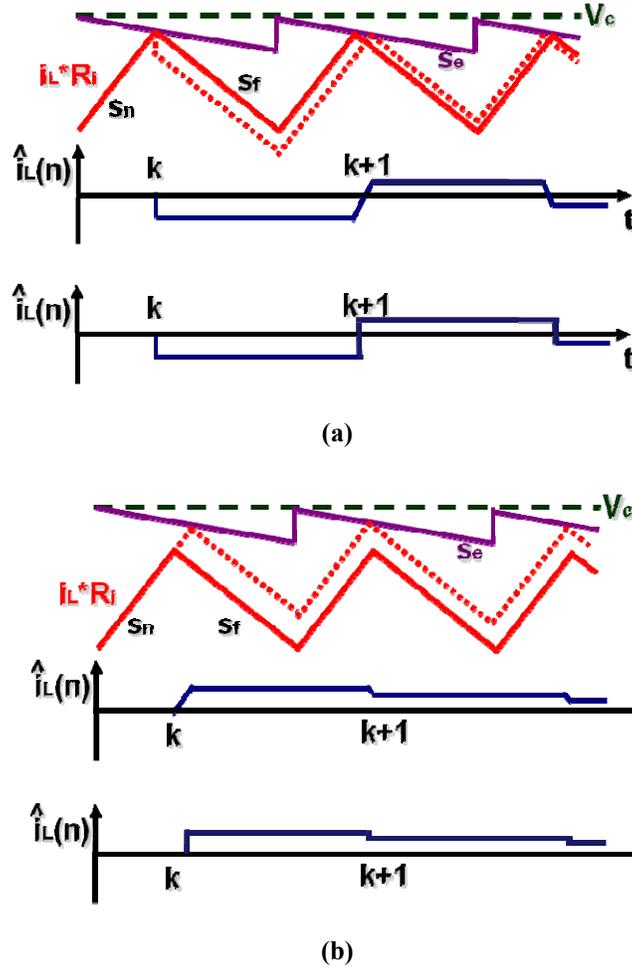
Figure 1.21. Discrete-time analysis: (a) natural response, and (b) forced response

The response of the inductor current is divided into two parts, including the natural response and the forced response. The discret-time expression can be found as:

Natural response:
$$\hat{i}_L(k+1) = -\alpha \cdot \hat{i}_L(k) \qquad (1.4)$$

Forced response:
$$\hat{i}_L(k+1) = (1+\alpha)/R_i \cdot \hat{v}_c(k+1) \qquad (1.5)$$

where $\alpha = (s_f - s_e)/(s_n + s_e)$, s_n is the magnitude of the inductor current slope during the on-time period, s_f is the magnitude of the inductor current slope during the off-time period, s_e is the magnitude of the external ramp, and R_i is the sensing gain of the inductor current.

Based on the combination of two parts, the control-to-inductor current transfer function in the discrete-time domain can be calculated as:

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$$H(z) = \frac{\hat{i}_L(z)}{\hat{v}_c(z)} = \frac{1+\alpha}{R_i} \frac{z}{z+\alpha} \tag{1.6}$$

The discrete-time transfer function shows that there is a pole loacated at α. The system stability is determined by the absolute value of α, which is a function of s_n, s_f, and s_e. The absolute value of α has to be less than 1 to guarantee system stability. For example, when $s_e=0$ and $s_n<s_f$ (D>0.5), the absolute value of α is larger than 1, which means the system is unstable. This model can accurately predict subharmonic oscillations and the influence of the external ramp in peak current-mode control and valley current-mode control. However, it is too complicated to be used in practical design.

D. Sampled-data model

In order to model peak-current mode control in the continuous-time domain instead of the discrete-time domain, sample-data analysis by A. R. Brown [53] is performed to explain the current-loop instability in the s-domain, as shown in Figure 1.23.
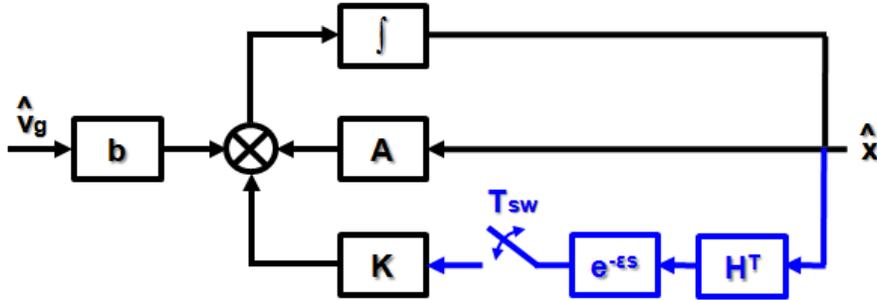
Figure 1.22. Sample-data model

With simplified power stage (no output capacitor), the current-loop gain can be calculated as:

$$T_s^* = H^T [e^{-\varepsilon s}(sI - A)^{-1}]^* K \tag{1.7}$$

Therefore, the system poles without the external ramp can be calculted as:

$$s_p = \frac{\omega_s}{2\pi} \ln(\frac{D}{D'}) + j(n+1/2)\omega_s \tag{1.8}$$

It's clearly shown that, when the duty cycle D is greater than 0.5, system poles are located at the right-half plane, which means the system is unstable.

Although the sampled-data model can precisely predict the high-freqeuncy response, it is hard to be used, just like the discrete-time model.

E. Modified average model

In order to extend the validation of the averaged models to the high-frequency range, several modified average models are proposed based on the results of discrete-time analysis and sample-data analysis [54][55][56][57][58][59] [60][61][62].

One of popular models is investigated by R. Ridley [56], which provided both the accuracy of the sample-data model and the simplicity of the three-terminal switch model. Essentially, R. Ridley's modeling strategy is based on the hypothesis method. In this method, first, the control-to-inductor current transfer function is obtained by transferring previous accurate disctrete-time transfer function (1.6) into its continuous-time form:

$$\frac{i_L(s)}{v_c(s)} = \frac{1}{R_i}\frac{1+\alpha}{sT_{sw}}\frac{e^{sT_{sw}}-1}{e^{sT_{sw}}+\alpha} \tag{1.9}$$

Then, "sample and hold" effects are equivalently represented by the $H_e(s)$ function which is inserted into the feedback path of the inductor current in the continuous avarge model, as shown in Figure 1.23. Another form of the control-to-inductor current transfer function can be calculated based on this assumed average model:

$$\frac{i_L(s)}{v_c(s)} = \frac{F_m F_i(s)}{1+F_m F_i(s)R_i H_e(s)} \tag{1.10}$$

Finally, based on (1.9) and (1.10), the $H_e(s)$ function is obtained as

$$H_e(s) = \frac{sT_{sw}}{e^{sT_{sw}}-1} \tag{1.11}$$

Following the same concept used in [41], the complete model is completed by adding two additional feed-forward gain and feedback gain. Due to its origination from the discrtete-time model, there is no doubt that this model can accurately predict subharmonic

oscillations in peak current-mode control and valley current-mode control. According to the control-to-output transfer function, as shown in Figure 1.24, the position of the double poles at high frequency is determined by the duty cycle value.
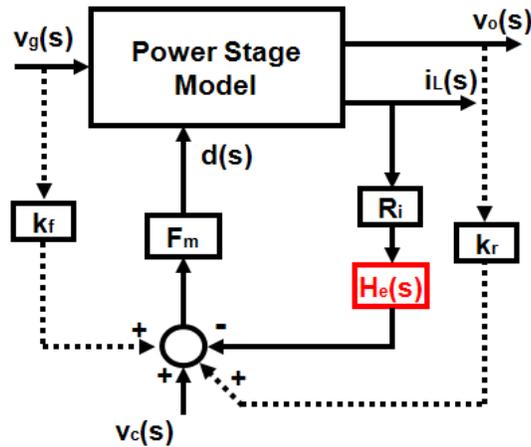
Figure 1.23. R. Ridley' model for peak current-mode control
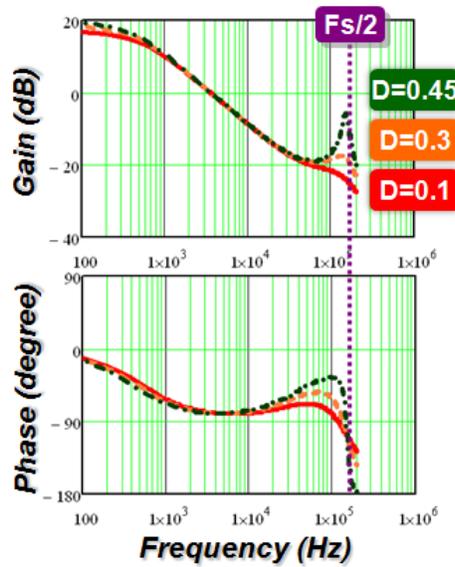
Figure 1.24. Control-to-output transfer function based on R. Ridley' model ($s_e = 0$)

Another of modified models is proposed by F. D. Tan and R. D. Middlebrook [58]. In order to consider the sampling effects in the current loop, one additional pole needs to be added to a current-loop gain derived from the low-frequency model, as shown in Figure 1.25.
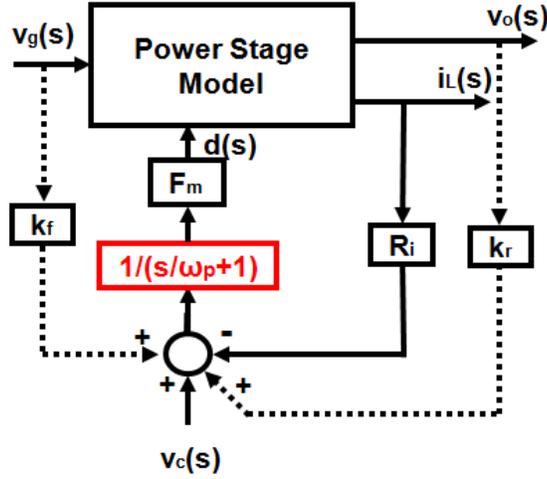
Figure 1.25. F. D. Tan and R. D. Middlebrook's model for peak current-mode control

Further analysis based on the modified models above is discussed for peak current-mode control [60][61][62]. The models for average current-mode control and charge control are obtained by extending the modified average model [63][64][65].

So far, R. Ridley's model is the most popular model for system design.

F. Other models

As mentioned before, the relationship between the inductor current, the control voltage and the duty cycle is majorly derived by using geometrical calculations in previous average models. However, in [66][67], Krylov-Bogoliubov-Mitropolsky (KBM) algorithm is applied to achieve the similar goal. KBM algorithm is used for recovering waveform details of state variables from their average values and the corresponding averaged model [68]. Therefore, the instantaneous inductor current can be recovered by ripple estimation. Based on KBM algorithm, the inductor-current ripple $\hat{i}_L(t)$ can be calculated as:

$$\hat{i}_L(t) = \Psi(t, \bar{i}_L, \bar{v}_c) \tag{1.12}$$

So, the instantaneous inductor current $i_L(t)$ can be expressed by:

$$i_L(t) = \bar{i}_L + \hat{i}_L(t) \tag{1.13}$$

Then, it can be used to define the duty cycle as follows based on the peak current-mode control princle:

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$$v_c - s_e dT_{sw} = \bar{i}_L + \Psi(t, \bar{i}_L, \bar{v}_c) \tag{1.14}$$

where v_c is the control voltage, s_e is the amplitude of the external ramp, and T_{sw} is the switching period. The accuracy of this approach is determined by the ripple estimation. The first-order extimation is used in [68] but not accuray enough. Higher-order estimation is more precise but too complicate. This method can be used especially for the average current-mode control and the charge control.

This disseration focuses on the modeling of current-mode control in the frequency domain. Other modeling approaches, such as the one based on bifurcation theory [69][70][71][72], are not introduced in this disseration.

1.4 Challenges to the Current-Mode Control Modeling

Previous models mainly focus on the prediction of subharmonic oscillations in peak current-mode control. However, subharmonic oscillations occur in other current-mode controls as well. As mentioned previously, constant on-time control is widely used to improve light-load efficiency. In the V^2 implementation, the nonlinear PWM modulator becomes much more complex, because not only is the inductor current information fed back to the modulator, but the capacitor voltage ripple information is also fed back to the modulator as well. Generally speaking, there is no subharmonic oscillation in constant on-time control. However, the delay due to the capacitor ripple results in subharmonic oscillations in V^2 constant on-time control, as shown in Figure 1.26.

In order to model this control, it'd better start from the basic structure of constant on-time control, as shown in Figure 1.11. It is found that the current-loop behavior in constant on-time control is fundamentally different from that in peak current-mode control, as shown in Figure 1.27. In peak current-mode control, the inductor current error stays the same for one switching cycle, until the next sampling event occurs. If the current loop is stable, the error will become zero after several swtiching cycles. This is called the "sample and hold" effects. However, in constant on-time control: the inductor current goes into steady state after one switching cycle, and an error will always exist for the following

switching cycles. This means that there are no similar "sample and hold" effects in constant on-time conrol.
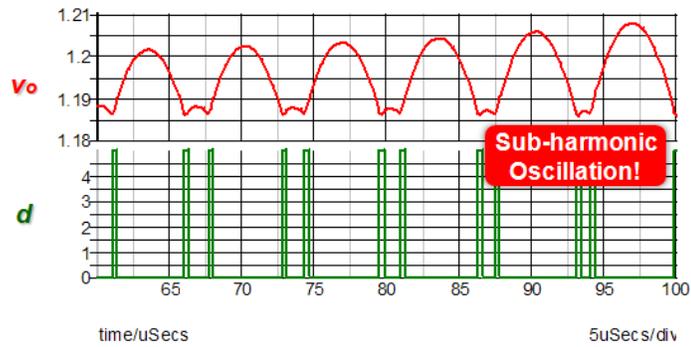
Figure 1.26. Subharmonic oscillations in V^2 constant on-time control

(a)

(b)
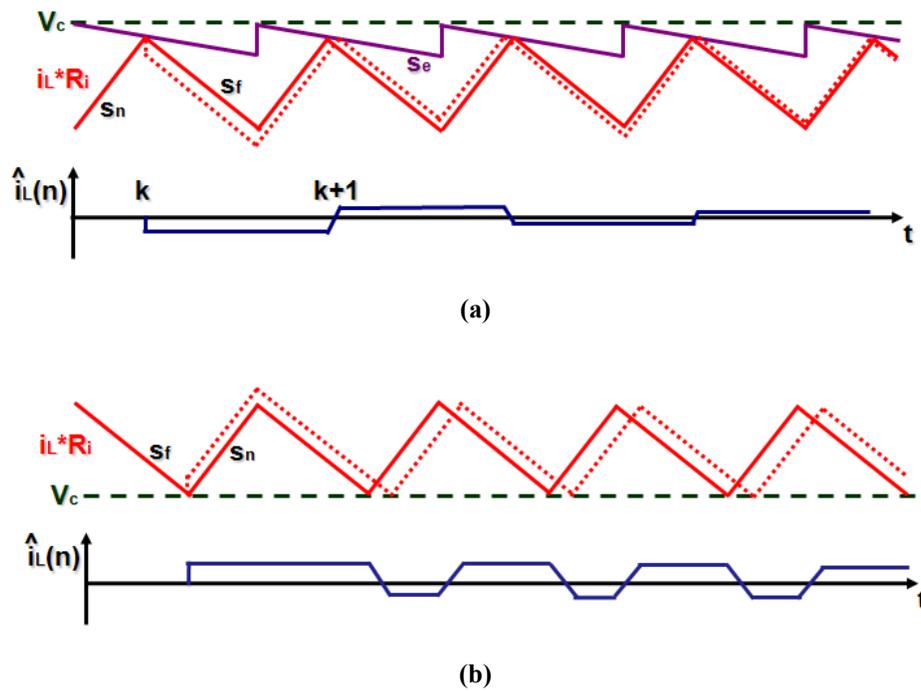
Figure 1.27. Perturbed inductor current waveform: (a) in peak current-mode control, and (b) in constant on-time control

It's easy to conclude that previous discrete-time analsys and sample-data analysis can't be applied to constant on-time control, because the effectiveness of those models are limited to constant-frequency modulation. Therefore, it is hard to justify that R. Ridley's model can be extended to constant on-time control [73], since the model should not include

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the same $H_e(s)$ function for "sample and hold" effects. As expected, there is a huge phase discrepancy in the extended model, as shown in Figure 1.28, which proves that previous discrete-time analysis which is the basis of the model for peak current-mode control, is no longer valid for constant on-time control.
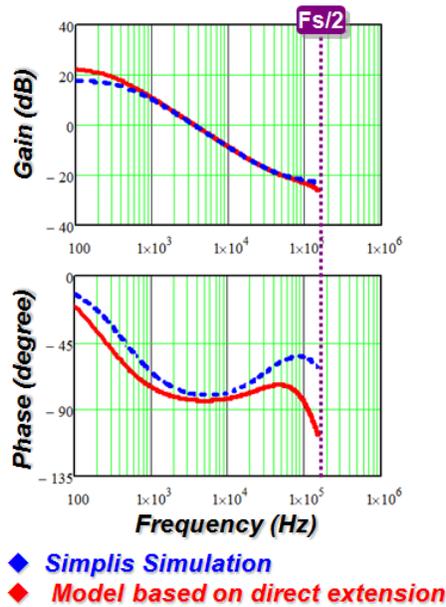
Figure 1.28. Discrepancy in the extended model
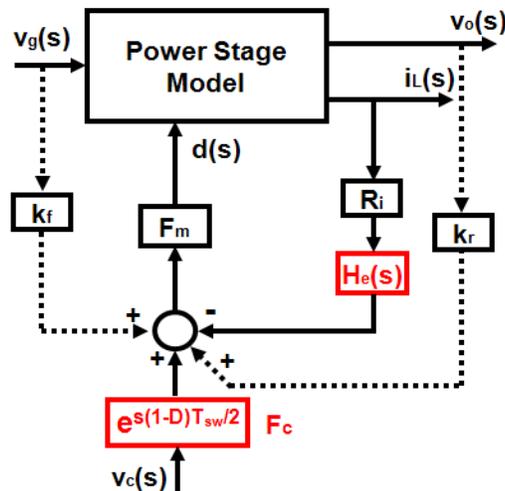
Figure 1.29. R. Ridley' model for constant on-time control
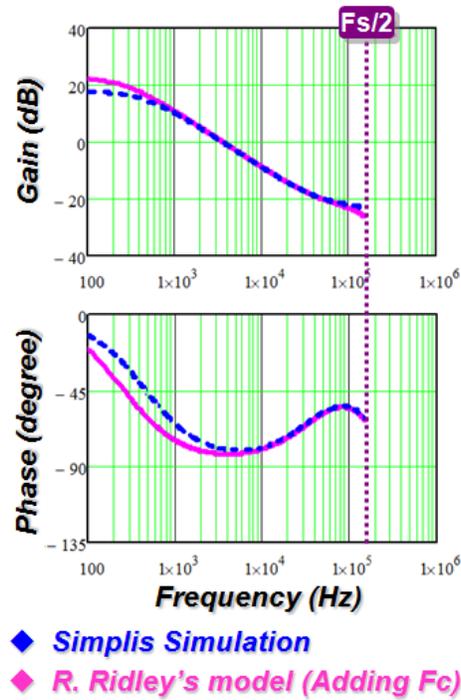
Figure 1.30. Control-to-output transfer function comparison in constant on-time control

In order to correct the error, an additonal term F_c, which has a phase-leading characteristic, must be added based on experiment data, which is lacking of theritical anlysis, as shown in Figure 1.29 and Figure 1.30.

Furthermore, the extended model in [74] is also not good enough for practical design.

In the V^2 type implementation, the situation becomes more stringent due to the influence of the capacitor ripple. The control-to-output transfer function with different capacitor parameters in V^2 constant on-time control is simulated based on the SIMPLIS tool, as shown in Figure 1.31. One important thing is that there is a double pole located at half of the switching frequency which is related to capacitor parameters. This phenomenon is very similar to that in peak current-mode control.

At present, there is no available small-signal model for V^2 constant on-time control. As shown in Figure 1.32, the extension of R. Ridley's model to V^2 constant on-time control is not a successful attempt due to the limitation of the fundamental basis of his model, which means that previous discrete-time analysis is not valid either in the case of the V^2 type implementation or in the case of constant on-time control.
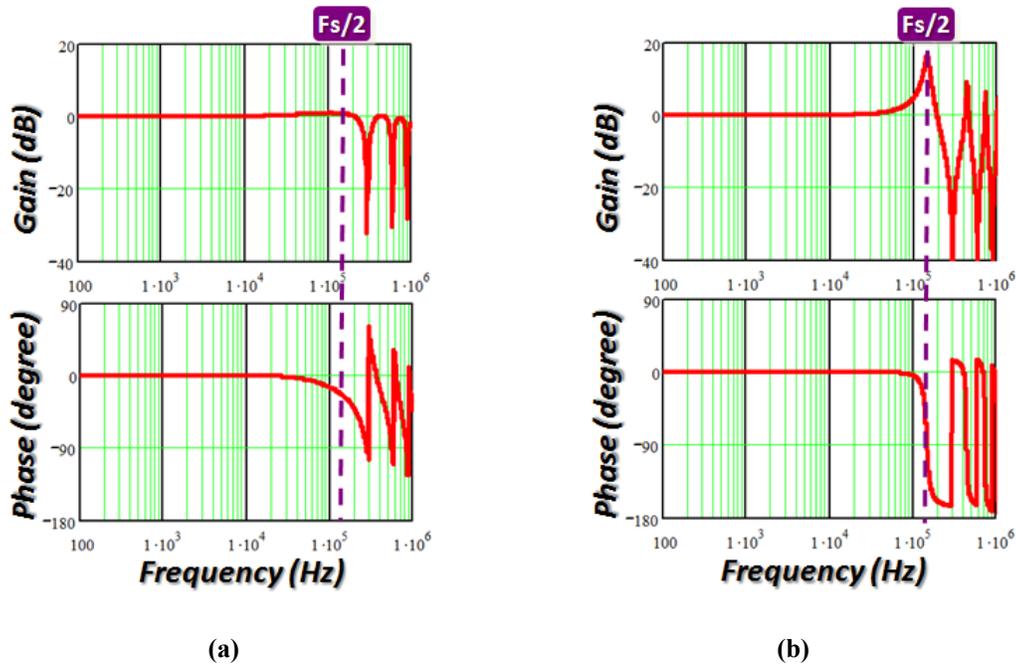
Figure 1.31. Control-to-output transfer function simulation: (a) capacitor: 560uF/6mΩ, and (b) capacitor: 560uF/0.6mΩ
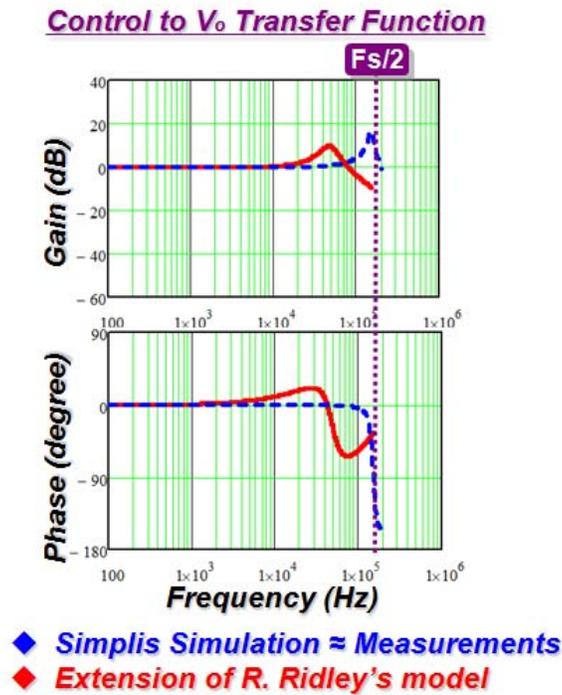
Figure 1.32. Extension of R. Ridley's model to V^2 constant on-time control

In addition, there are several other types of V^2 current mode controls including peak voltage control, valley voltage control, and V^2 constant off-time control [75][76][77]. Peak voltage control is also used in the industry products. But the models used in [78][79][80] can't accurately predict the influence from the capacitor ripple in peak voltage control, since all of them are extension of R. Ridley's model. In [81], the Krylov-Bogoliubov-Mitropolsky (KBM) algorithm is used to improve the accuracy of the model, but it is too complicated to be used in practical design.

So far, there is no simple and accurate small-signal model for V^2 current-mode control.

Furthermore, in the proposed digital current-mode control architecture, the control principle can be simplified without considering the quantization effects, as shown in Figure 1.33. It is very similar to V^2 control except for the sampling effect in the control loop. Again, there is no available model for system design in the proposed structure.

Figure 1.33. Simplified structure for the proposed digital current-mode control

In a word, there are still several challenges to the current-mode control modeling.

1.5 Dissertation Outline

Due to unique characteristics, current-mode control architectures with different implementation approaches have been widely used in power converter design. An accurate model for current-mode control is indispensable to system design due to the existence of subharmonic oscillations. However, available models can only solve partial issues related to current-mode control. The primary objective of this work is to present a new modeling approach to model current-mode control with different implementation methods. This dissertation consists of six chapters. They are organized as follows. First, the background of current-mode control and challenges to the current-mode control modeling has been introduced. Then, a new modeling approach for current-mode control is presented. Next, from the sake of easy understanding, an equivalent circuit representation of current-mode control is proposed based on the model obtained from the new approach. After that, this new approach is applied to V^2 current-mode control to model the influence of the capacitor ripple. At last, a digital application of the current-mode control is investigated to eliminate the need for high-resolution DPWM. Proposed digital structure is also modeled based on the proposed approach to help system design. In the end, conclusions are given.

The detailed outline is elaborated as follows.

Chapter 1 is the review of the background of current-mode control and challenges to the current-mode control modeling. Current-mode control architectures are widely used to guarantee the current sharing, achieve the AVP control, and improve the light load efficiency in power converter design. An accurate model for current-mode control is indispensable to system design. However, available models can only solve partial issues. The primary objective of this work is to present a new modeling approach to model the current-mode control with different implementation methods.

Chapter 2 presents a new modeling approach for current-mode control. Proposed modeling strategy is based on the time-domain analysis. Describing function method is used. The inductor, the switches and the PWM modulator are treated as a single entity to model instead of breaking them into parts to do it. The fundamental difference between different current-mode controls is elaborated based on the models obtained from the new modeling approach.

Chapter 3 introduces an equivalent circuit representation of current-mode control for the sake of easy understanding. The effect of the current loop is equivalent to controlling the inductor current as a current source with a certain impedance. This circuit representation provides both the simplicity of the circuit model and the accuracy of the proposed model.

Chapter 4 analyzes the extension of the new modeling approach to V^2 current-mode control. The power stage, the switches and the PWM modulator are treated as a single entity and modeled based the describing function method. The model for V^2 current-mode control achieved by the new approach can accurately predict subharmonic oscillations due to the influence of the capacitor ripple. Two solutions are discussed to solve the instability issue.

Chapter 5 investigates a digital application of current- mode control. High-resolution digital pulse-width modulator (DPWM) is considered to be indispensable for minimizing the possibility of unpredicted limit-cycle oscillations, but results in high cost, especially in the application of voltage regulators for microprocessors. This chapter firstly introduces several DPWM modulation methods to improve the DPWM resolution. And then, a fully digital current-mode control architecture which can effectively limit the oscillation amplitude is presented, thereby greatly reducing the design challenge for digital controllers by eliminating the need for the high-resolution DPWM. New modeling strategy is also used to model the proposed digital current-mode control in this chapter.

Chapter 6 is conclusions with the summary and the future work.

Chapter 2. New Modeling Approach for Current-Mode Control

This chapter introduces a new modeling approach for current-mode control. Proposed modeling strategy is based on the time-domain analysis. Describing function method is utilized as a tool. The inductor, the switches and the PWM modulator are treated as a single entity to model instead of breaking them into parts to do it. The fundamental difference between different current-mode controls is elaborated based on the models obtained from the new modeling approach. Simulation and experimental results are used to verify the proposed models.

2.1   The Scenario in Current-Mode Control

The nonlinearity of current-mode control belongs to dynamic nonlinearity due to the modulation based on the inductor-current ramp. The scenario of current-mode control in the frequency domain is shown in Figure 2.1.
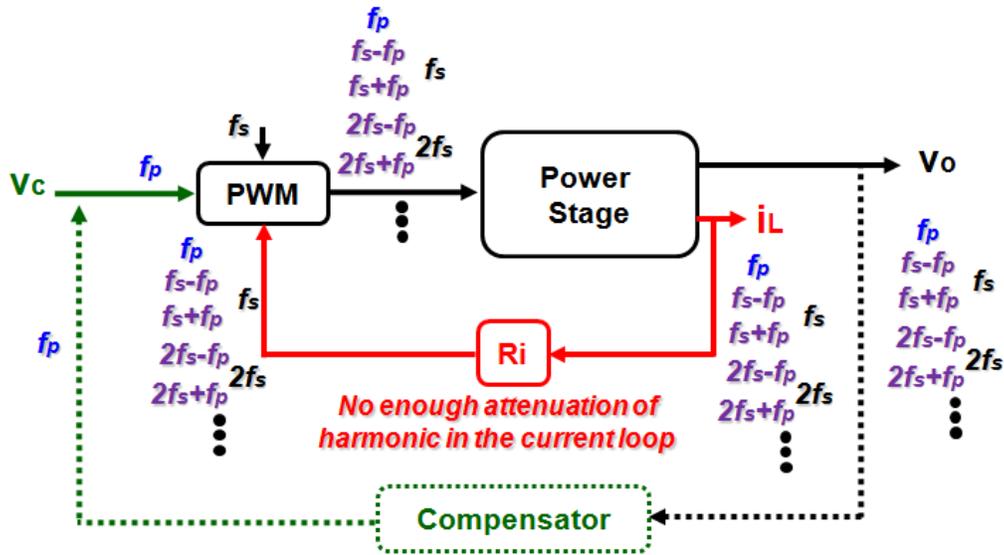
Figure 2.1. The scenario in current-mode control

In the inner current loop, when there is a perturbation at frequency f_p in the control signal, multiple frequency components are generated at the output of the PWM comparator, including the fundamental component (f_p), the switching frequency component (f_s) and its harmonic (nf_s), and the sideband components ($f_s \pm f_p$, $nf_s \pm f_p$). When the inductor current is fed back to the modulator, there is no enough attenuation on high frequency components. All components are coupled through the modulator. In [82][83], the primary components (f_p and f_s-f_p) are taken into consideration in voltage-mode control. However, the situation is much more complicated in current mode control, because neither the sideband components nor the switching frequency components can be ignored. This is why the frequency domain analysis is very difficult to perform in the current loop. Previous average models for current-mode control failed to consider high frequency components. That's why they can only predict the low-frequency response.

It is relatively easy for the outer voltage loop, since high frequency components can be attenuated due to the compensation (low pass filter).

In the following paragraphs, a new modeling approach is presented.

2.2   New Modeling Approach for Peak Current-Mode Control

Before presenting the new modeling approach, the basic concept of describing function (DF) method [84][85] is introduced first. The DF method is an approximate procedure for analyzing non-linear control problems. It is based on quasi-linearization that is the approximation of the non-linear system under investigation by a system that is linear except for a dependence on the amplitude of the input waveform. This quasi-linearization must be carried out for a specific family of input waveforms. One choice might be to describe the system response to the family of sine wave inputs; in this case the system would be characterized by an sine input describing function $H(A, j\omega)$ (SIDF) giving the system response to an input consisting of a sine wave of amplitude A and frequency ω. This SIDF is a generalization of the transfer function $H(j\omega)$ used to characterize linear systems. In a quasi-linear system when the input is a sine wave, the output will be a sine wave of the same frequency but with different amplitude and phase as given by $H(A, j\omega)$. Many systems are approximately quasi-linear in the sense that although the response to a

sine wave is not a pure sine wave, most of the energy in the output is indeed at the same frequency ω as the input. This is because such systems may possess intrinsic low-pass or band-pass characteristics such that harmonics are naturally attenuated, or because external filter are added for this purpose.

In the area of power electronics, power converters possess intrinsic low-pass or band-pass filter in power stages. This is why the DF method is suitable to the modeling of power converter systems. In voltage-mode control, the DF method has been successfully used to derive the equivalent gain of constant-frequency PWM modulator [86][87]. As shown in Figure 2.2, in order to model the PWM modulator, a small sinusoidal perturbation at the frequency f_m is injected through the control signal v_c; then perturbed duty cycle expression in the time domain can be found out based on the waveform; next, Fourier analysis is applied to calculate the perturbation frequency component of the duty cycle; at last, the describing function from the control signal to the duty cycle can be obtained. The approximation ignores all the components at harmonic frequencies due to the existence of a low pass filter in the system. Similar method is applied to variable-frequency modulator [88], as shown in Figure 2.3. In [82][83], author used similar concept to find sideband components in order to obtain the multi-frequency model.
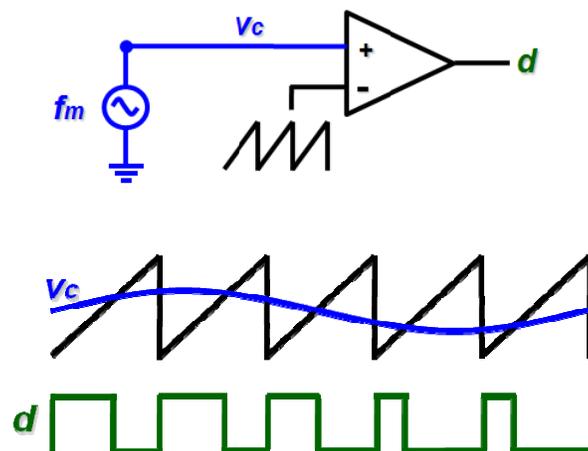
Figure 2.2. Constant-frequency trailing edge modulation
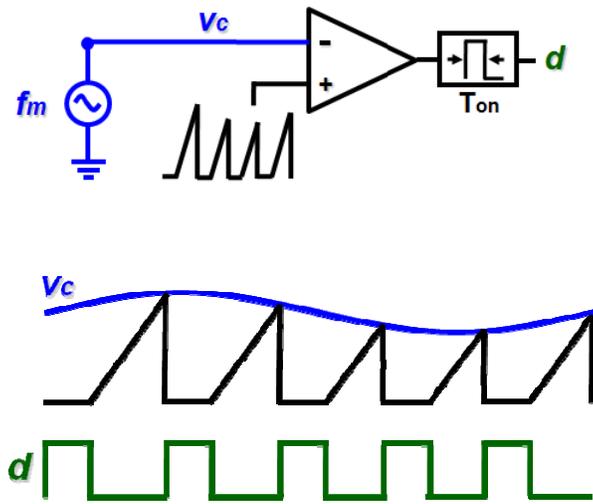
Figure 2.3. Variable-frequency constant on-time modulation

As mentioned previous, it is hard to model the current-loop sideband effects from the frequency domain. However, proposed new modeling approach can solve this issue from time-domain analysis based on the DF method.

Peak current-mode control is chosen to illustrate the proposed modeling process. As shown in Figure 2.4, the non-linear modulator consists of the switches, the inductor current, and the comparator.
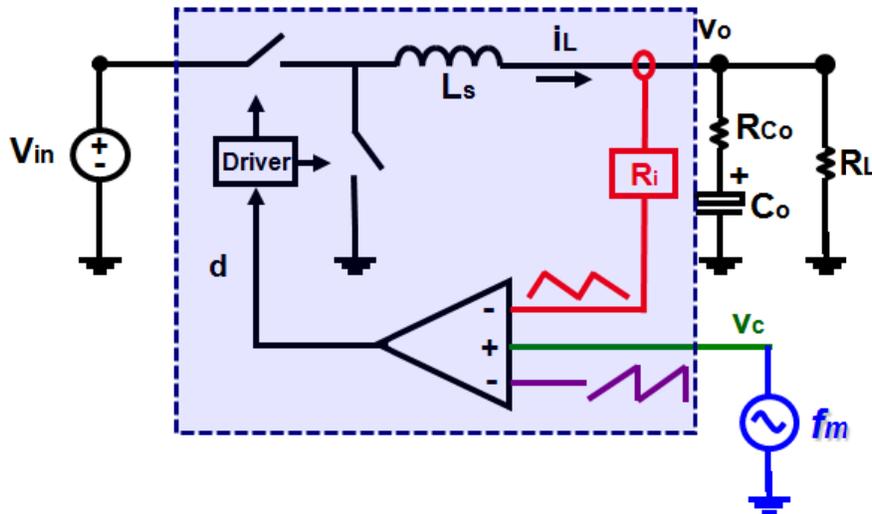
Figure 2.4. Proposed modeling methodology for peak current-mode control

It's reasonable to treat them as a single entity to model instead of breaking them into parts. In the proposed modeling appproach, the DF method is applied to the closed-loop time-domain waveform to model the non-linear current-mode modulator to obtain the transfer function from the control signal v_c to the output voltage v_o. To do so, the current-loop sideband effects can be identified thorough the time-domain waveform which includes all the effects due to the nonlinearity of the modulator. As shown in Figure 2.4, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the control signal v_c; then, based on the perturbed inductor current waveform, the describing function from the control signal v_c to the inductor current i_L can be found by mathematical derivation. Before applying the DF method, it is necessary to make several assumptions:

(i)   The magnitude of the inductor-current slopes during the on-period and the off-period stays constant;

(ii) The magnitude of the perturbation signal is very small;

(iii) The perturbation frequency f_m and the switching frequency f_s are commensurable, which means that $N \times f_s = M \times f_m$, where N and M are positive integers.

Following the modulation law of peak current-mode control, the duty cycle and the inductor current waveforms are shown in Figure 2.5.
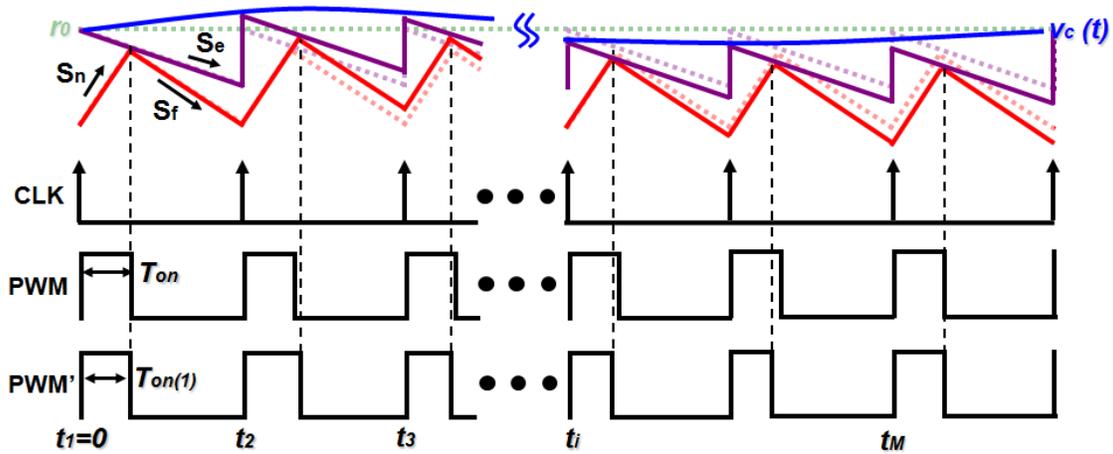
Figure 2.5. Perturbed inductor current waveform in peak current-mode control

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Because the switching cycle T_{sw} is fixed, the on-time and the off-time is modulated by the perturbation signal $v_c(t)$: $v_c(t) = r_0 + \hat{r}\sin(2\pi f_m \cdot t - \theta)$, where, r_0 is the steady state value of the control signal, $\hat{r}_0$ is the magnitude of the signal, and θ is the initial angle. Based on the modulation law, it is found that:

$$v_c(t_{i-1} + T_{on(i-1)}) - s_e T_{on(i-1)} - s_f(T_{sw} - T_{on(i-1)}) = v_c(t_i + T_{on(i)}) - (s_n + s_e)T_{on(i)} \quad (2.1)$$

where, $T_{on(i)}$ is the i_{th} cycle on-time, $s_n = R_i(V_{in} - V_o)/L_s$, $s_f = R_i V_o / L_s$, s_e is the amplitude of the external ramp, L_s is the inductance of the inductor, and R_i is the current sensing gain. Assuming $T_{on(i)} = T_{on} + \Delta T_{on(i)}$, where T_{on} is the steady-state on-time and $\Delta T_{on(i)}$ is the i_{th} cycle on-time perturbation, t_i can be calculated as: $t_i = (i-1)T_{sw}$.

Based on (2.1), it is found that:

$$(s_n + s_e)\Delta T_{on(i)} + (s_f - s_e)\Delta T_{on(i-1)} = v_c(t_i + T_{on(i)}) - v_c(t_{i-1} + T_{on(i-1)}) \quad (2.2)$$

Hence, $\Delta T_{on(i)}$ can be calculated as:

$$(s_n + s_e)\Delta T_{on(i)} + (s_f - s_e)\Delta T_{on(i-1)} = 2\hat{r}\sin \pi f_m T_{sw} \cos \pi f_m[(2i-3)T_{sw} + 2T_{on}] \quad (2.3)$$

The duty cycle $d(t)$ and the inductor current $i_L(t)$ can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M}[u(t - t_i) - u(t - t_i - T_{on(i)})] \quad (2.4)$$

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \int_0^t [\frac{V_{in}}{L_s} d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} - \frac{V_o}{L_s}]dt + i_{L0} \quad (2.5)$$

where u(t)=1, when t>0, and i_{L0} is the initial value of the inductor current.

Then, Fourier analysis can be performed on the inductor current:

$$
\begin{aligned}
c_m &= \frac{j2f_m}{N}\sum_{i=1}^{M}\int_{t_i}^{t_i + T_{on(i)}} i_L(t) \cdot e^{-j2\pi f_m t} dt \\
&= \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\sum_{i=1}^{M}(e^{-j2\pi f_m[(i-1)T_{sw}]}\Delta T_{on(i)})
\end{aligned}
\quad (2.6)
$$

where c_m is the Fourier coefficient at perturbation frequency f_m.

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By substituting (2.3) into (2.6), the coefficient can be calculated as:

$$c_m == \hat{r} \cdot \frac{f_s(1-e^{-j2\pi f_m T_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-j2\pi f_m T_{sw}}} \frac{V_{in}}{L_s \cdot j2\pi f_m} e^{-j\theta} \tag{2.7}$$

The Fourier coefficient at perturbation frequency f_m for the control signal $v_c(t)$ is $\hat{r} \cdot e^{-j\theta}$, so the describing function from control to inductor current can be calculated as:

$$\frac{i_{L(f_m)}}{v_{c(f_m)}} = \frac{c_m}{\hat{r} \cdot e^{-j\theta}} = \frac{f_s(1-e^{-j2\pi f_m T_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-j2\pi f_m T_{sw}}} \frac{V_{in}}{L_s \cdot j2\pi f_m} \tag{2.8}$$

For the detail derivation, refer to Appendix A.

Note that the results are not applicable to frequencies where $f_m = n \times f_s$, where n is a positive integer. In order to avoid getting too detailed, the results at those frequencies are not shown here. The transfer function in the s-domain can be expressed as:

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \frac{V_{in}}{L_s s} \tag{2.9}$$

It is found that this transfer function is identical to the one derived from previous discrete-time analysis, as shown in (1.9). It proves the validity of the new modeling approach.

The exponential term $e^{-sT_{sw}}$ can be simplified by using the Padé approximation:

$$e^{-sT_{sw}} = 1 - sT_{sw}/(1 + \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2}) \tag{2.10}$$

where $\omega_2 = \pi/T_{sw}$ and $Q_1 = 2/\pi$. This approximation is valid up to the frequency of $1/(2T_{sw})$. Finally, (2.9) can be simplified as (2.11) and defined as DF:

$$\frac{i_L(s)}{v_c(s)} \approx \frac{1}{R_i} \cdot \frac{1}{1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}} \doteq DF \tag{2.11}$$

where $Q_2 = 1/\{\pi[(s_n+s_e)/(s_n+s_f)-0.5]\}$.

Then, the control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{R_i} \cdot \frac{1}{1 + \dfrac{s}{Q_2 \omega_2} + \dfrac{s^2}{\omega_2^2}} \cdot \frac{R_L (R_{Co} C_o s + 1)}{(R_L + R_{Co}) C_o s + 1} \qquad (2.12)$$

where R_{Co} is the ESR of the output capacitors, C_o is the capacitance of the output capacitors, and R_L is the load resistor.

In order to consider the variation of the inductor-current slopes, similar methodology is used to derive two additional terms that represent the influence from the input voltage v_{in} and the output voltage v_o, as shown in Figure 2.6 and Figure 2.7.
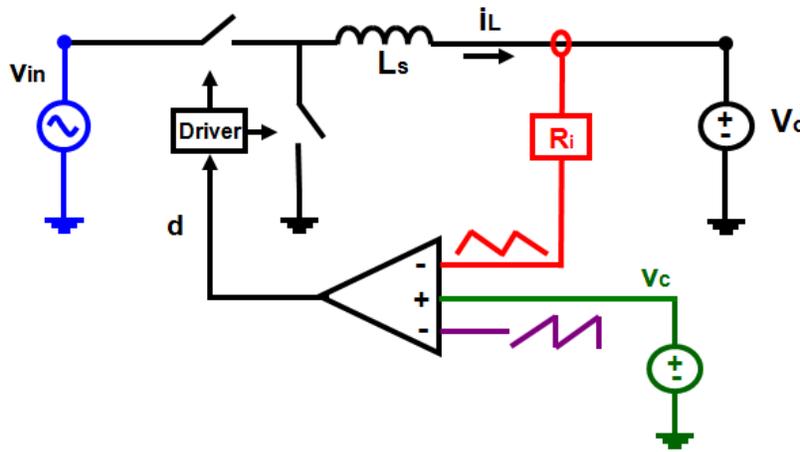
Figure 2.6. Modeling for the influence of the input voltage v_{in} in peak current-mode control
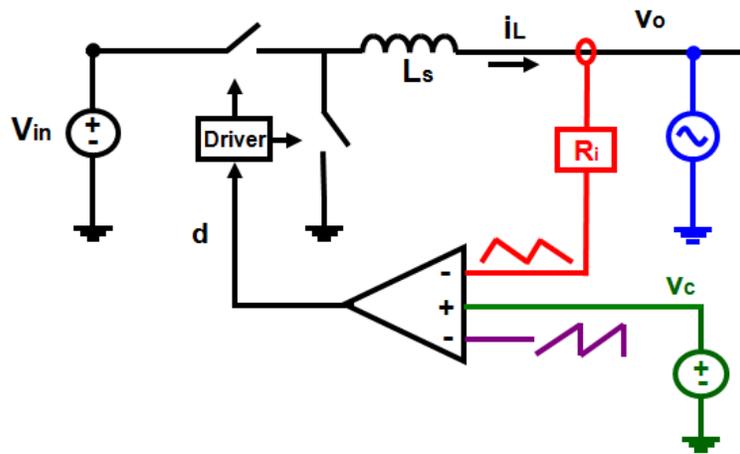
Figure 2.7. Modeling for the influence of the output voltage v_o in peak current-mode control

The transfer functions from the input voltage to the inductor current and from the output voltage to the inductor current are calculated as:

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s}{(s_n + s_e) + (s_f - s_e)e^{-sT_{sw}}} \frac{(1 - e^{-sT_{on}})}{s \cdot L_s / R_i} \cdot V_{in} + D]$$ (2.13)

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s} \cdot [\frac{f_s(1 - e^{-sT_{sw}})}{(s_n + s_e) + (s_f - s_e)e^{-sT_{sw}}} \frac{1}{s \cdot L_s / R_i} \cdot V_{in} - 1]$$ (2.14)

where D is the steady-state duty cycle. For the detail derivation, refer to Appendix A.

The complete model for peak current-mode control is shown in Figure 2.8.
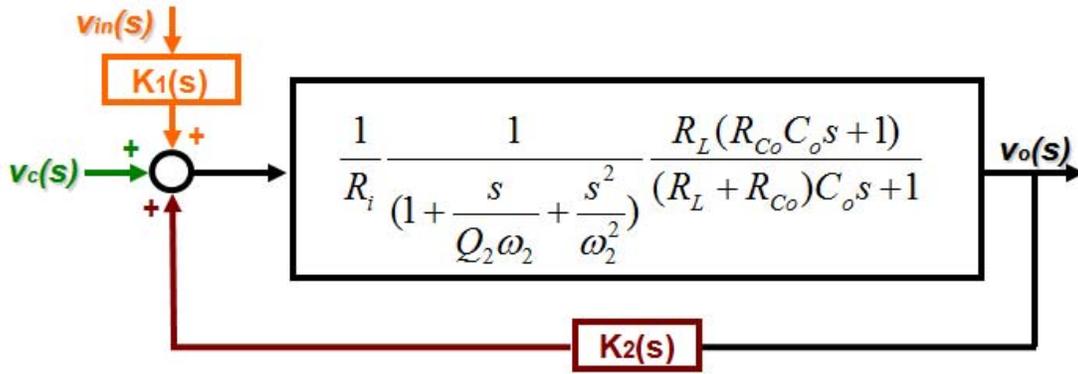
Figure 2.8. Complete model for peak current-mode control

where

$$k_1(s) = \frac{i_L(s)/v_{in}(s)}{i_L(s)/v_c(s)} \approx \frac{DR_i}{L_s}[\frac{1}{Q_2\omega_2} - \frac{T_{off}}{2}]$$ (2.15)

$$k_2(s) = \frac{i_L(s)/v_o(s)}{i_L(s)/v_c(s)} \approx -\frac{R_i}{L_s Q_2 \omega_2}$$ (2.16)

Finally, the control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{R_L}{R_i(1 - \frac{k_2}{R_i}R_L)} \cdot \frac{(R_{Co}C_o s + 1)}{\frac{(R_L + R_{Co})C_o - R_L R_{Co} C_o k_2 / R_i}{1 - R_L k_2 / R_i} s + 1} \cdot \frac{1}{1 + \frac{s}{Q_2 \omega_2} + \frac{s^2}{\omega_2^2}}$$ (2.17)

It is clearly shown that there is a double pole located at $\omega_2 = \pi / T_{sw}$, and it is possible that the double pole moves to the right-half plane resulting in subharmonic oscillations in the current loop. Moreover, the additional feedback gain k_2 is responsible for the movement of the low frequency pole, as shown in Figure 2.9 and Figure 2.10.
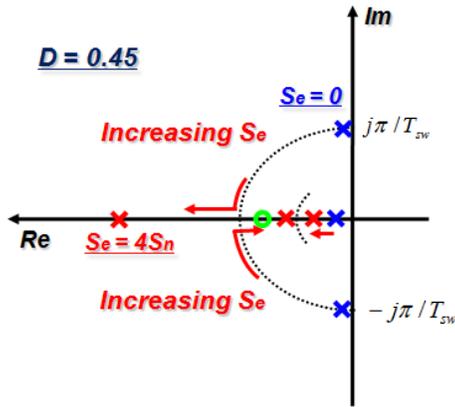
Figure 2.9. System poles in peak current-mode control
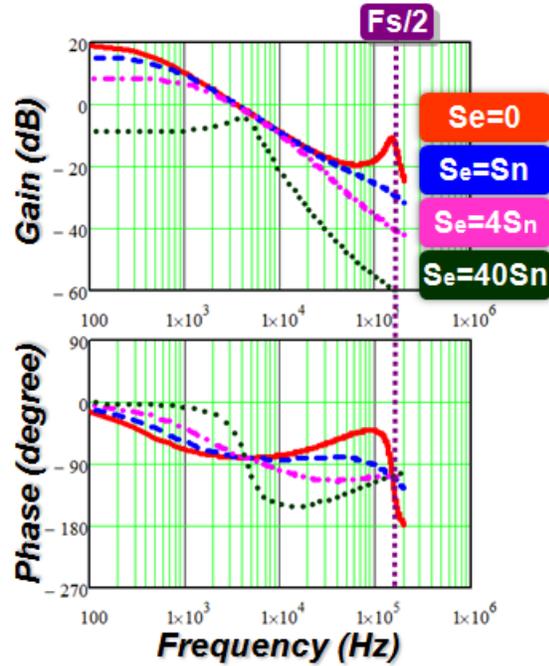
Figure 2.10. Control-to-output transfer function with different s_e in peak current-mode control

In fact, the effectiveness of the model obtained from the new modeling approach is not limited by the switching frequency. The SIMPLIS simulation tool is used to verify the proposed model for peak current-mode control. The parameters of the buck converter are as follows: V_{in} = 12V, V_o = 5V, f_s = 300KHz, C_o = 8×560µF, R_{Co} = 6/8mΩ, and L_s = 300nH. The control-to-output transfer function and the audio susceptibility comparisons are shown in Figure 2.11 and Figure 2.12. The complete model without approximation can accurately predict the system response even beyond the switching frequency. For the case with the outer voltage loop closed, the similar concept in [83] can be applied here to predict the voltage-loop sideband effects. For the practical purpose, the model is simplified and limited by the half of the switching frequency.

The detail comparisons between the new model and R. Ridley's model are shown in Figure 2.13 and Figure 2.14. The new model can achieved the same results as R. Ridley's model in terms of the control-to-out transfer function in peak current-mode control. Furthermore, the new model is more accurate than R. Ridley's model in terms of the audio susceptibility as shown in Figure 2.14. In a word, the model obtained from the new modeling approach can precisely predict the system response in peak current-mode control.
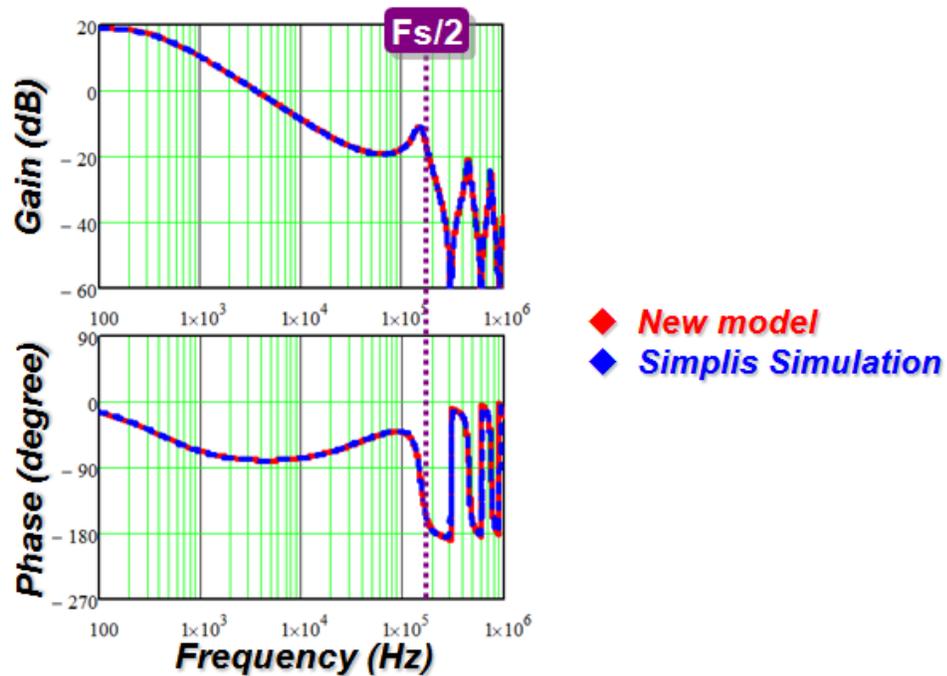
Figure 2.11. Control-to-output transfer function in peak current-mode control
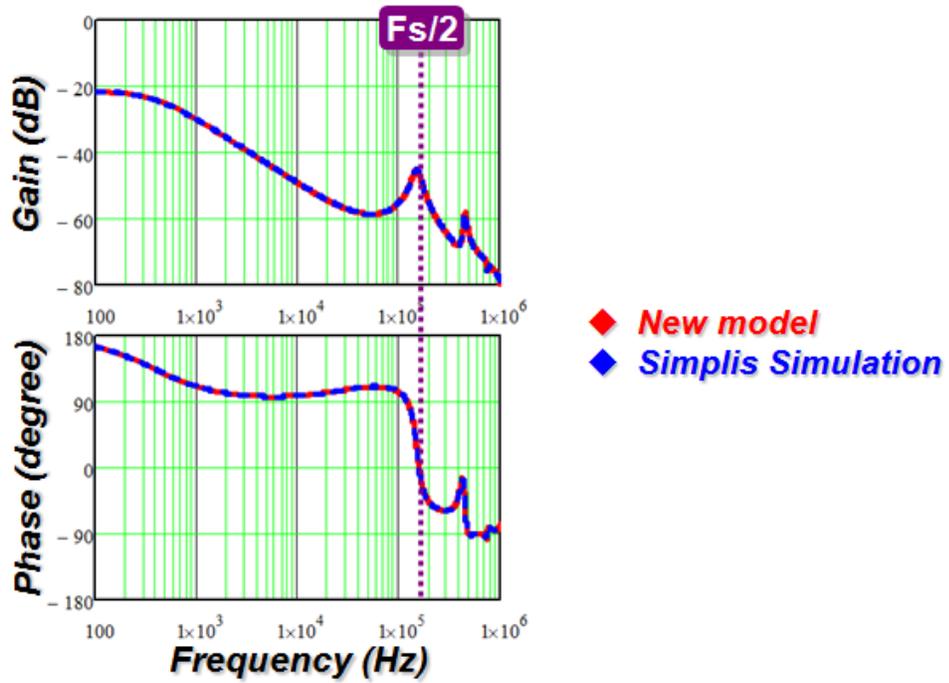
Figure 2.12. Audio susceptibility in peak current-mode control
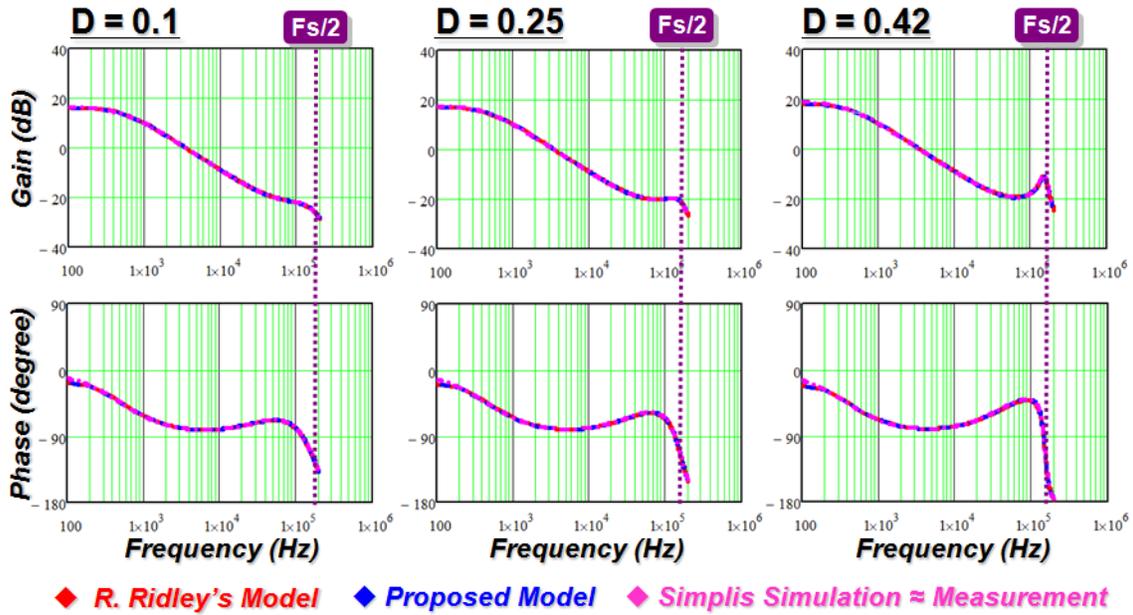
Figure 2.13. Control-to-output transfer function comparison in peak current-mode control
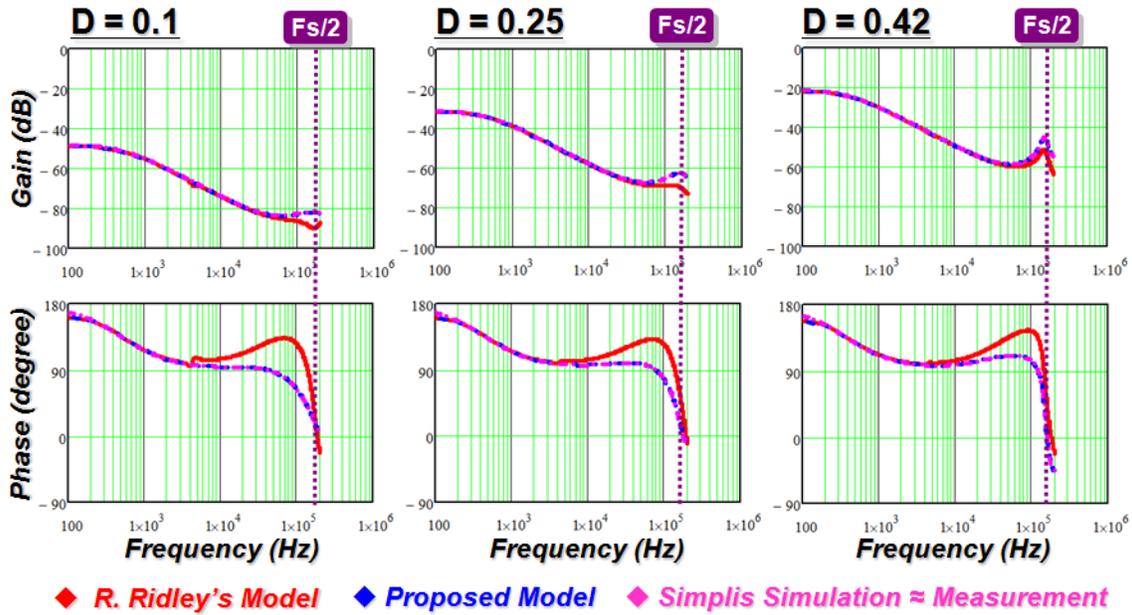
Figure 2.14. Audio susceptibility comparison in peak current-mode control

For the case of considering the DCR of the inductor, please refer to Appendix C

2.3   Model Extension to Constant On-time Control

As introduced in Chapter 1, there is a fundamental issue of extending R. Ridley's model for peak current-mode control to constant on-time control. However, it's very easy to apply the new model approach to constant on-time control.

In constant on-time control, as shown in Figure 2.15, the non-linear constant on-time modulator consists of the switches, the inductor current, the comparator and the on-time generator. Following the same methodology, all of them are treat as as a single entity to model instead of breaking them into parts. As shown in Figure 2.15, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the control signal v_c, then, based on the perturbed inductor current waveform, the describing function from the control signal v_c to the inductor current i_L can be found by mathematical derivation.
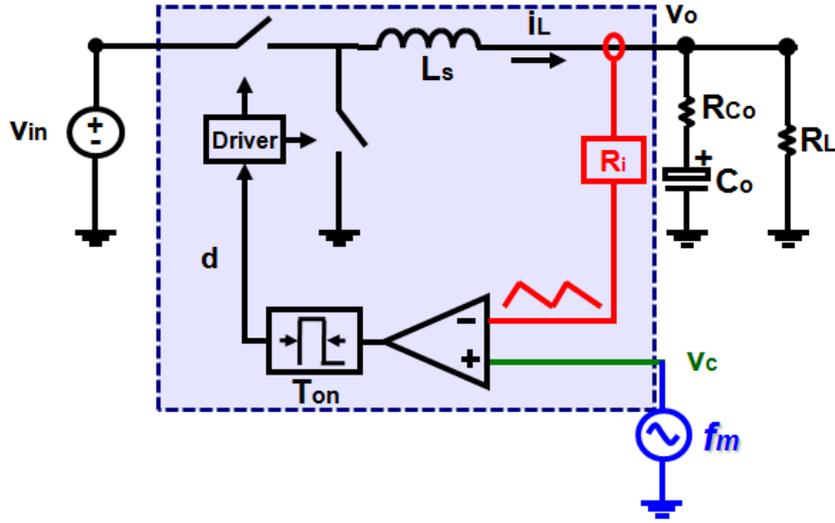
Figure 2.15. Proposed modeling methodology for constant on-time control

Following the modulation law of constant on-time control, the duty cycle and the inductor current waveforms are shown in Figure 2.16.
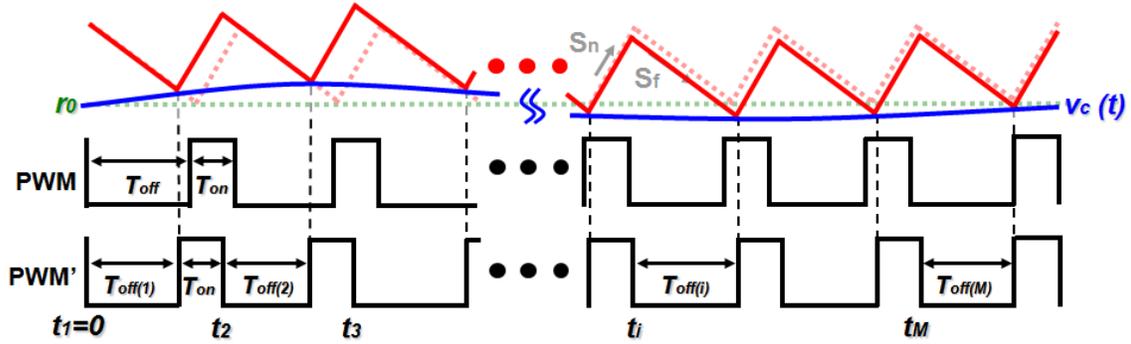
Figure 2.16. Perturbed inductor current waveform in constant on-time control

Because the on-time is fixed, the off-time is modulated by the perturbation signal $v_c(t)$: $v_c(t) = r_0 + \hat{r}\sin(2\pi f_m \cdot t - \theta)$. Based on the modulation law, it is found that:

$$v_c(t_{i-1} + T_{off(i-1)}) + s_n T_{on} = v_c(t_i + T_{off(i)}) + s_f T_{off(i)} \tag{2.18}$$

where, $T_{off(i)}$ is the i_{th} cycle off-time. Assuming $T_{off(i)} = T_{off} + \Delta T_{off(i)}$, where T_{off} is the steady-state off-time and $\Delta T_{off(i)}$ is the i_{th} cycle off-time perturbation, t_i can be calculated as: $t_i = (i-1)(T_{on} + T_{off}) + \sum_{k=1}^{i-1} \Delta T_{off(k)}$. Based on (2.18) , it is found that:

$$s_f \Delta T_{off(i)} = v_c(t_{i-1} + T_{off(i-1)}) - v_c(t_i + T_{off(i)})$$

(2.19)

Hence, $\Delta T_{off(i)}$ can be calculated as:

$$\Delta T_{off(i)} \approx -2 \frac{\hat{r}}{s_f} \sin[\pi f_m \cdot (T_{on} + T_{off})] \cdot \cos[2\pi f_m[(i-1)(T_{on} + T_{off}) - \frac{T_{on} - T_{off}}{2}]$$

(2.20)

The perturbed duty cycle d(t) and the perturbed inductor current $i_L(t)$ can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M}[u(t - t_i - T_{off(i)}) - u(t - t_i - T_{off(i)} - T_{on})]$$

(2.21)

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \int_0^t [\frac{V_{in}}{L_s} d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} - \frac{V_o}{L_s}]dt + i_{L0}$$

(2.22)

Then, the Fourier analysis can be performed on the inductor current:

$$c_m = j \frac{2f_m}{N} \int_0^{t_M + T_{off(M)} + T_{on}} i_L(t) \cdot e^{-j2\pi f_m t} dt$$

$$= \frac{1}{N\pi} \frac{V_{in}}{L_s} e^{-j2\pi f_m T_{off}} (e^{-j2\pi f_m T_{on}} - 1)[\sum_{i=1}^{M}(e^{-j2\pi f_m(i-1)T_{sw}} \sum_{k=1}^{i} \Delta T_{off(k)})]$$

(2.23)

where, c_m is the Fourier coefficient at perturbation frequency f_m.

By substituting (2.20) into (2.23), the coefficient can be calculated as:

$$c_m == \hat{r} \cdot \frac{f_s}{s_f}(1 - e^{-j2\pi f_m T_{on}}) \frac{V_{in}}{L_s \cdot j2\pi f_m} e^{-j\theta}$$

(2.24)

The Fourier coefficient at perturbation frequency f_m for the control signal $v_c(t)$ is $\hat{r} \cdot e^{-j\theta}$, so the describing function from control to inductor current can be calculated as:

$$\frac{i_{L(f_m)}}{v_{c(f_m)}} = \frac{c_m}{\hat{r} \cdot e^{-j\theta}} = \frac{f_s}{s_f}(1 - e^{-j2\pi f_m T_{on}}) \frac{V_{in}}{L_s \cdot j2\pi f_m}$$

(2.25)

For the detail derivation, refer to Appendix A.

Note that the results are not applicable to frequencies where $f_m = n \times f_s$, where n is a positive integer. In order to avoid getting too detailed, the results at those frequencies are not shown here. The transfer function in the s-domain can be expressed as:

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$$\frac{i_L(s)}{v_c(s)} = \frac{f_s}{s_f}(1 - e^{-sT_{on}})\frac{V_{in}}{L_s s} \tag{2.26}$$

The exponential term $e^{-sT_{on}}$ can be simplified by using the Padé approximation:

$$e^{-sT_{on}} = 1 - \frac{sT_{on}}{1 + \dfrac{s}{Q_1\omega_1} + \dfrac{s^2}{\omega_1^2}} \tag{2.27}$$

where $\omega_1 = \pi/T_{on}$ and $Q_1 = 2/\pi$. This approximation is valid up to the frequency of $1/(2T_{on})$. Finally, (2.26) can be simplified as (2.28) and defined as DF:

$$\frac{i_L(s)}{v_c(s)} \approx \frac{1}{R_i} \cdot \frac{1}{1 + \dfrac{s}{Q_1\omega_1} + \dfrac{s^2}{\omega_1^2}} \doteq DF \tag{2.28}$$

Then the control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{R_i} \cdot \frac{1}{1 + \dfrac{s}{Q_1\omega_1} + \dfrac{s^2}{\omega_1^2}} \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1} \tag{2.29}$$

In order to consider the variation of the inductor-current slopes, similar methodology is used to derive two additional terms that represent the influence from the input voltage v_{in} and the output voltage v_o, as shown in Figure 2.17 and Figure 2.18.

The transfer functions from the input voltage to the inductor and from the output voltage to the inductor current are calculated as:

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[\frac{1 - e^{-sT_{on}}}{1 - e^{sT_{sw}}} \frac{f_s}{s_f} \frac{-(1 - e^{sT_{on}})}{s \cdot L_s/R_i} \cdot V_{in} + D] \approx \frac{D}{L_s} \frac{0.5}{0.5s + 1} \tag{2.30}$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s} \cdot [\frac{f_s(1 - e^{-sT_{on}})}{s_f} \cdot \frac{1}{s \cdot L_s/R_i} \cdot V_{in} - 1] \approx -\frac{1}{L_s} \frac{0.5D}{(0.5 + D/2)s + 1} \tag{2.31}$$

For the detail derivation, refer to Appendix A.
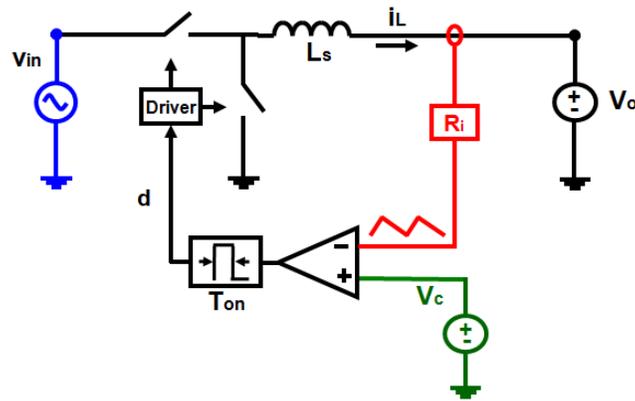
Figure 2.17. Modeling for the influence of the input voltage v_{in} in constant on-time control
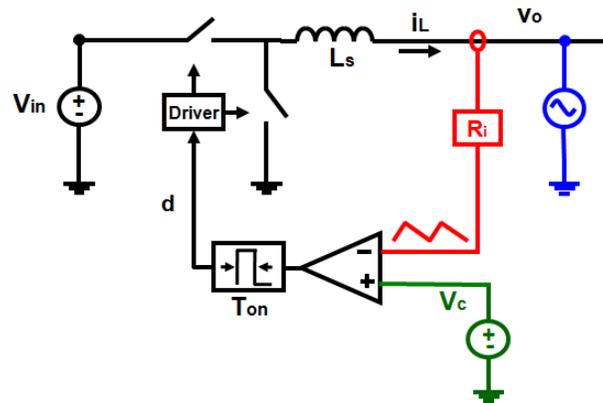
Figure 2.18. Modeling for the influence of the output voltage v_o in constant on-time control

The complete model for constant on-time control is shown in Figure 2.19.
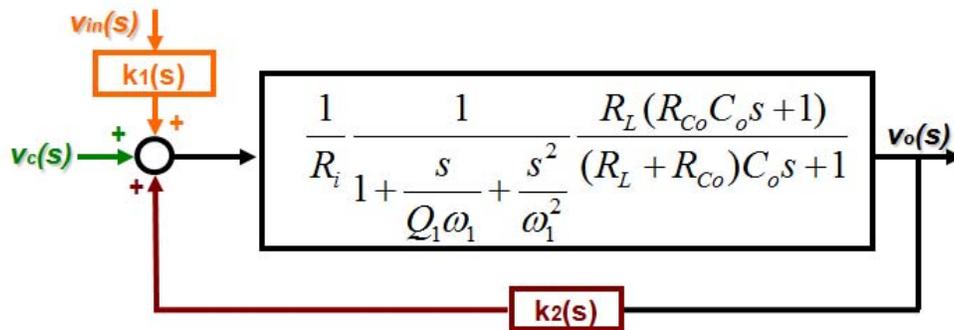
Figure 2.19. Complete model for constant on-time control

Where,
$$k_1(s) = \frac{i_L(s)/v_{in}(s)}{i_L(s)/v_c(s)} \approx \frac{1}{2}\frac{T_{on}R_i}{L_s} \qquad (2.32)$$

$$k_2(s) = \frac{i_L(s)/v_o(s)}{i_L(s)/v_c(s)} \approx -\frac{1}{2}\frac{T_{on}R_i}{L_s} \qquad (2.33)$$

Finally, the control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{R_L}{R_i(1 - \frac{k_2}{R_i}R_L)} \cdot \frac{(R_{Co}C_o s + 1)}{\frac{(R_L + R_{Co})C_o - R_L R_{Co}C_o k_2/R_i}{1 - R_L k_2/R_i}s + 1} \cdot \frac{1}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \qquad (2.34)$$

It is possible to find the fundamental difference between constant on-time control and peak current-mode control by comparing (2.17) and (2.34). The position of the double pole located at the high frequency is different for two cases. In constant on-time control, the double pole is located at $\omega_1 = \pi/T_{on}$, and the double pole will never move to the right half-plane. That's why there is no subharmonic oscillation in the current loop for constant on-time control, as shown in Figure 2.20.
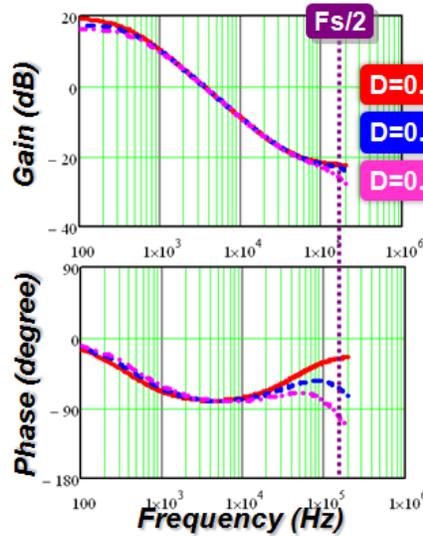
Figure 2.20. Control-to-output transfer function in constant on-time control

In the SIMPLIS simulation, the parameters of the buck converter are as follows: V_{in} = 12V, $f_s \approx 300\text{KHz}$, $C_o = 8 \times 560\mu\text{F}$, $R_{Co} = 6/8\text{m}\Omega$, and $L_s = 300\text{nH}$. The control-to-output transfer function and the audio susceptibility are plotted using simulation results, as shown

in Figure 2.21 and Figure 2.22. The proposed model can accurately predict the system response in comparison with R. Ridley's model.
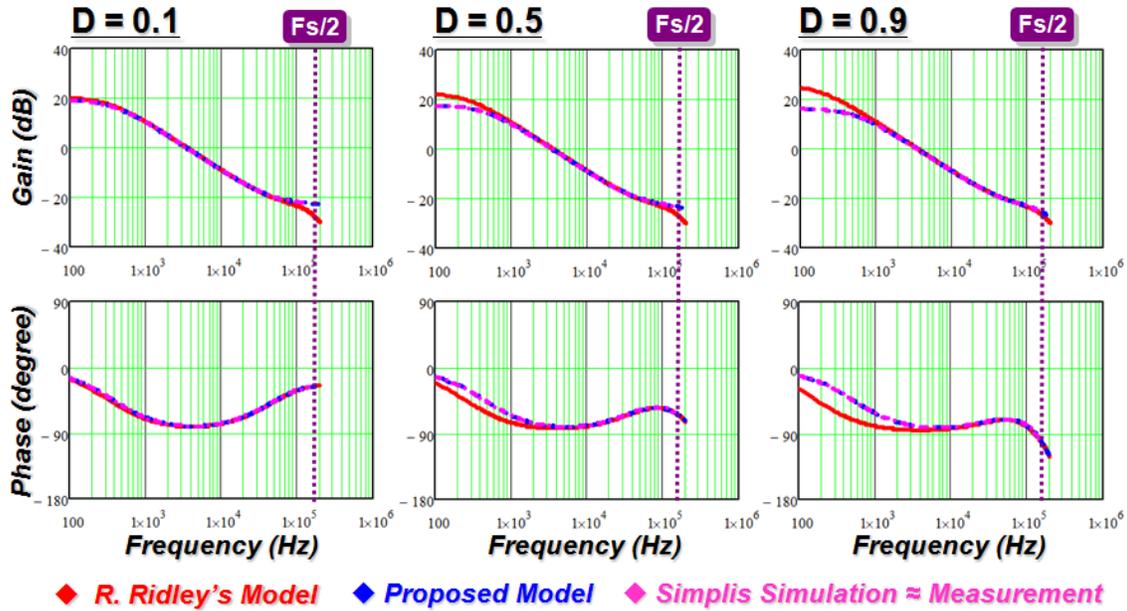
Figure 2.21. Control-to-output transfer function comparison in constant on-time control
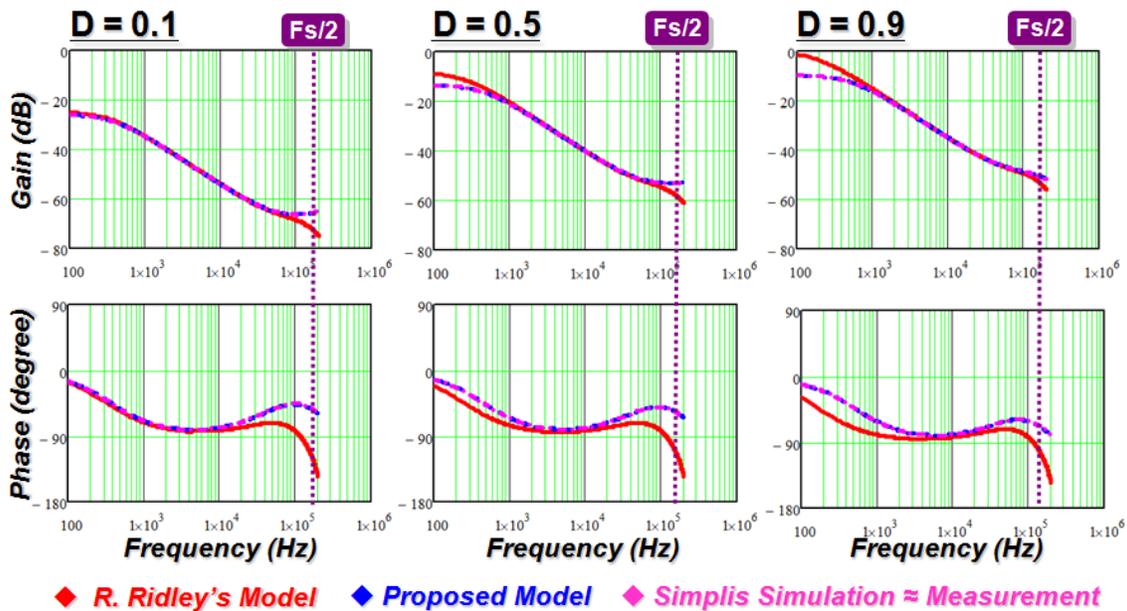
Figure 2.22. Audio susceptibility comparison in constant on-time control

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The experimental verification is done based on the LTC3812 evaluation board from Linear Technology. The parameters are: V_o = 3.3V, T_{on} = 0.26μs, L_s = 3.1μF, C_o = 2×150μF, and R_{Co} = 9/2mΩ. Experimental results with different duty cycle values are shown in Figure 2.23. The proposed model accurately predicts the system response.
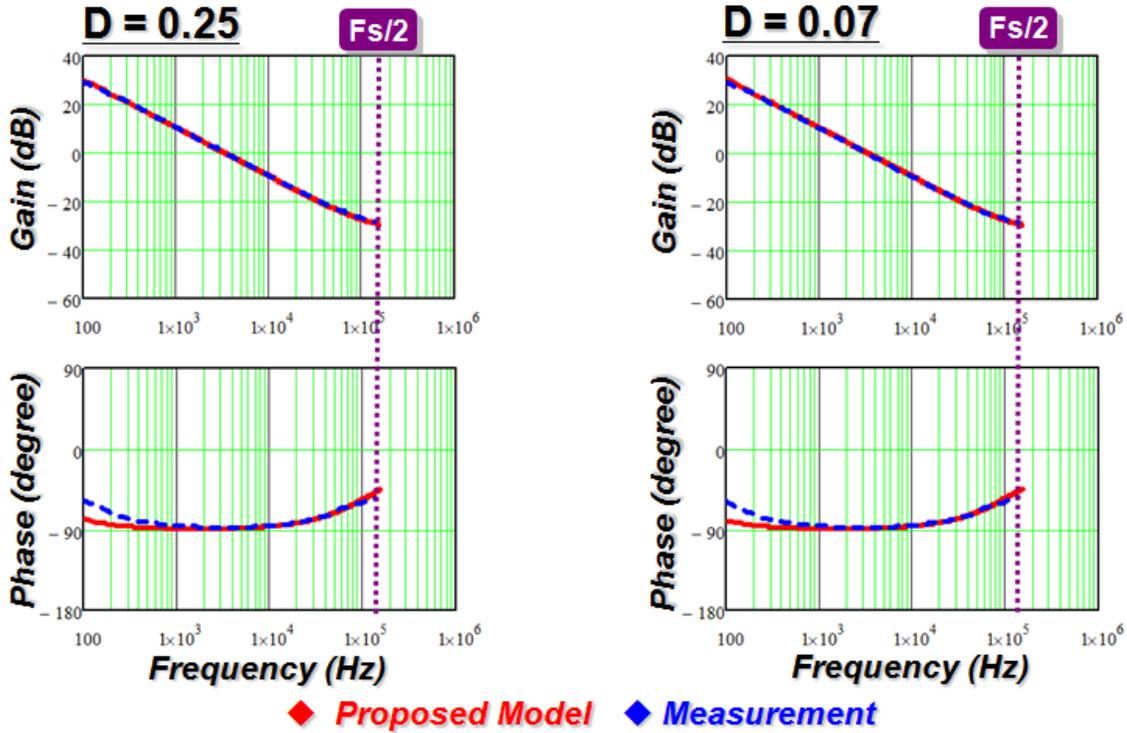
Figure 2.23. Control-to-output transfer function measurements

2.4   Complete model for Other Current-Mode Controls

The proposed modeling strategy can be used for other types of current-mode control structures. Based on the duality, the model for valley current-mode control can be otained based on the model for peak current-mode control, as shown in Table 2.1. Based on the same concept, the model for constant off-time control can be otained based on the model for constant on-time control, as shown in Table 2.2.

Table 2.1. Model for valley current-mode control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\frac{V_{in}}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\frac{e^{-sT_{off}}(1-e^{-sT_{on}})}{s\cdot L_s/R_i}\cdot V_{in}+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s}\cdot[\frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}\cdot V_{in}-1]$$

$DF = 1/[R_i(1+\frac{s}{Q_2'\omega_2}+\frac{s^2}{\omega_2^2})]$	$k_1 \approx \frac{DR_i}{L_s}[\frac{1}{Q_2'\omega_2}+\frac{T_{off}}{2}]$	$k_2 \approx -\frac{R_i}{L_s Q_2'\omega_2}$
		$Q_2' = 1/\{\pi[(s_f+s_e)/(s_n+s_f)-0.5]\}$

Table 2.2. Model for constant off-time control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\frac{V_{in}}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{off}})}{(1-e^{sT_{sw}})[(s_e+s_n)-s_e e^{-sT_{sw}}]}\frac{e^{sT_{off}}(1-e^{sT_{on}})}{s\cdot L_s/R_i}\cdot V_{in}+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s}\cdot[\frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}\cdot V_{in}-1]$$

$DF = 1/[R_i(1+\frac{s}{Q_1\omega_3}+\frac{s^2}{\omega_3^2})]$	$k_1 \approx 0$	$k_2 \approx -T_{off}R_i/(2L_s)$
		$\omega_3 = \pi/T_{off}$

Charge control is used to control average input current of converters with pulsating current, such as buck converters, in order to achieve good input current sharing, as shown in Figure 2.24. The new modeling approach can also be extended to this case. In the charge control structure, C_T is the capacitor which is used for the accumulation of the input current. The model results are shown in Table 2.3.
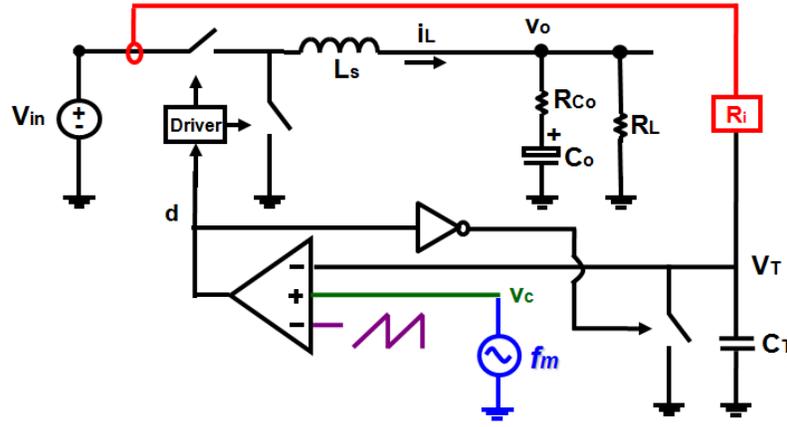
Figure 2.24. Charge control

Table 2.3. Model for charge control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(\dfrac{\dfrac{1}{2}s_nT_{on}+I_LR_i}{C_T}+s_e)+[\dfrac{(\dfrac{1}{2}s_n+s_f)T_{on}-I_LR_i}{C_T}-s_e]e^{-sT_{sw}}} \frac{V_{in}}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[\frac{f_s(1-e^{-sT_{sw}})(e^{-sT_{on}}-1)\dfrac{1}{s \cdot s \cdot L_s/R_i}-D(e^{-sT_{on}}-e^{-sT_{sw}})\dfrac{-V_{in}}{s \cdot L_s/R_i}}{(I_LR_i+\dfrac{s_nT_{on}}{2}+C_Ts_e)+[(s_n+s_f)T_{on}-I_LR_i-\dfrac{s_nT_{on}}{2}-C_Ts_e]e^{-sT_{sw}}}+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s} \cdot [\frac{f_s(1-e^{-sT_{sw}})(1-e^{-sT_{on}}) \cdot \dfrac{V_{in}}{s^2 \cdot L_s/R_i}}{(I_LR_i+\dfrac{s_nT_{on}}{2}+C_Ts_e)+[(s_n+s_f)T_{on}-I_LR_i-\dfrac{s_nT_{on}}{2}-C_Ts_e]e^{-sT_{sw}}}-1]$$

$DF = \dfrac{C_T}{R_iDT_{sw}}/(1+\dfrac{s}{Q_c\omega_2}+\dfrac{s^2}{\omega_2^2})$	$k_1 \approx \dfrac{DR_iT_{on}}{C_TL_s}(\dfrac{1}{Q_c\omega_2}+\dfrac{T_{on}}{2})$	$k_2 \approx -\dfrac{R_iT_{on}}{C_TL_s}(\dfrac{1}{Q_c\omega_2}+\dfrac{T_{on}}{2})$

$$Q_c = 1/[\pi(\frac{L_sf_s}{R_L}-\frac{D}{2}+\frac{L_sC_Tf_s}{V_oR_i}s_e)]$$

The models for boost and buck-boost converter with different current-mode controls are shown in Appendix B.

2.5   Multi-phase model for Current-Mode Control

As mentioned before, multi-phase topology is widely used to improve the transient response, and distribute power and heat for better thermal performance. The model for multi-phase converters with current-mode control can be obtained from the extension of the mode for the single-phase converter with current-mode control.

A. Multi-phase model for peak current-mode control

A multi-phase buck converter with peak current-mode control is shown in Figure 2.25. The parameters for each phase are the same as those for the previous single phase. The interleaving is achieved by the clock in each phase.
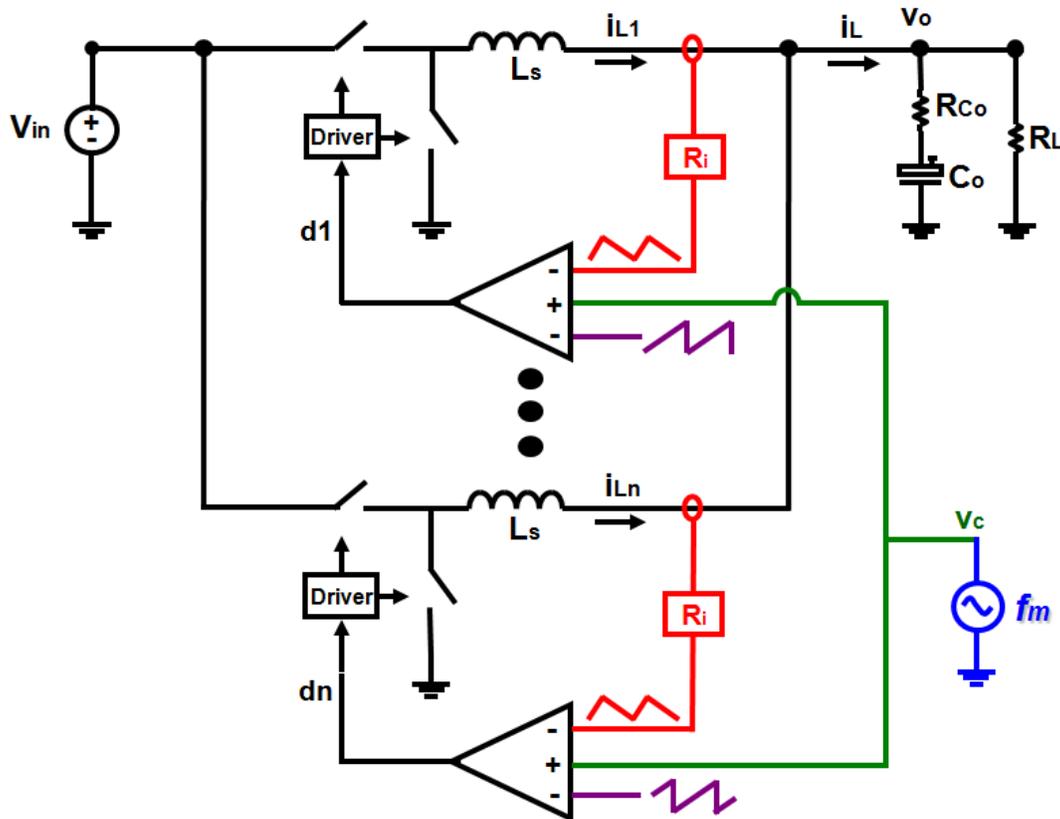
Figure 2.25. Multi-phase buck converter with peak current-mode control

Based on the implementation, each phase is identical and parallel together no matter whatever the phase-shift angle is. The model can be directly extended from paralleling single phase model, as shown in Figure 2.26.
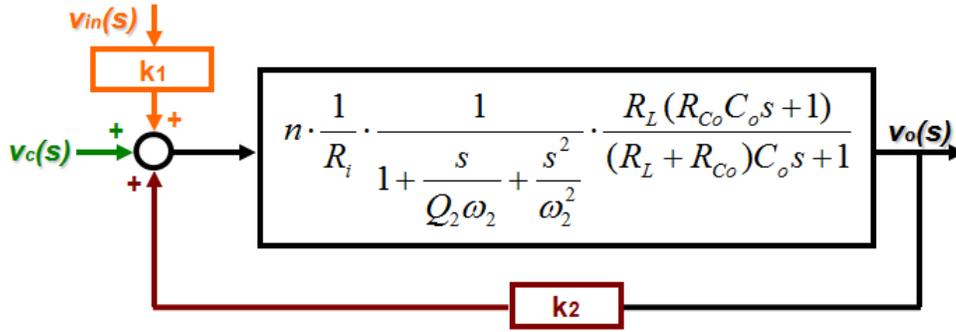
Figure 2.26. A multi-phase model for peak current-mode control

where, n is the phase number.

SIMPLIS simulation tool is used to simulate the system with 2 phase interleaving and $D = 0.42$. Simulation results are shown in Figure 2.27 and Figure 2.28. It is clearly shown that the model is independent on the phase-shift angle as expected.
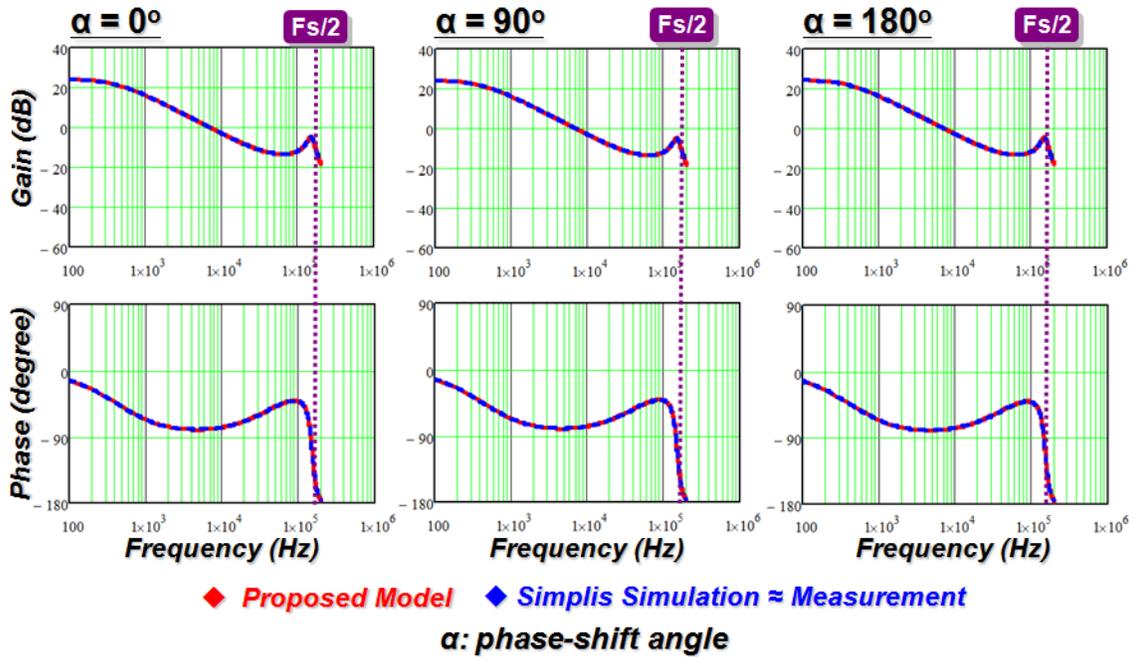
Figure 2.27. Control-to-output transfer function comparison for multi-phase buck converters with peak current-mode control
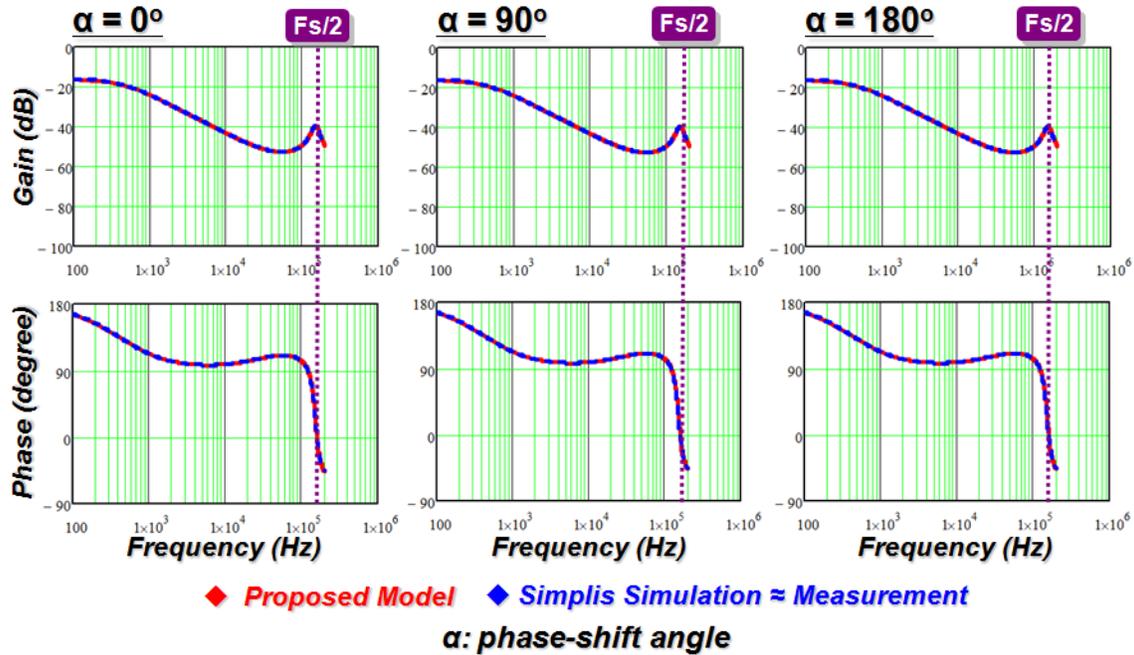
Figure 2.28. Audio susceptibility comparison for multi-phase buck converters with peak current-mode control

B. Multi-phase model for constant on-time control

There are two kinds of implementations for multi-phase buck converters with constant on-time control. One implementation is shown in Figure 2.29. The current information of each phase is fed back to its own modulator. The interleaving is achieved by an additional phase lock loop (PLL).
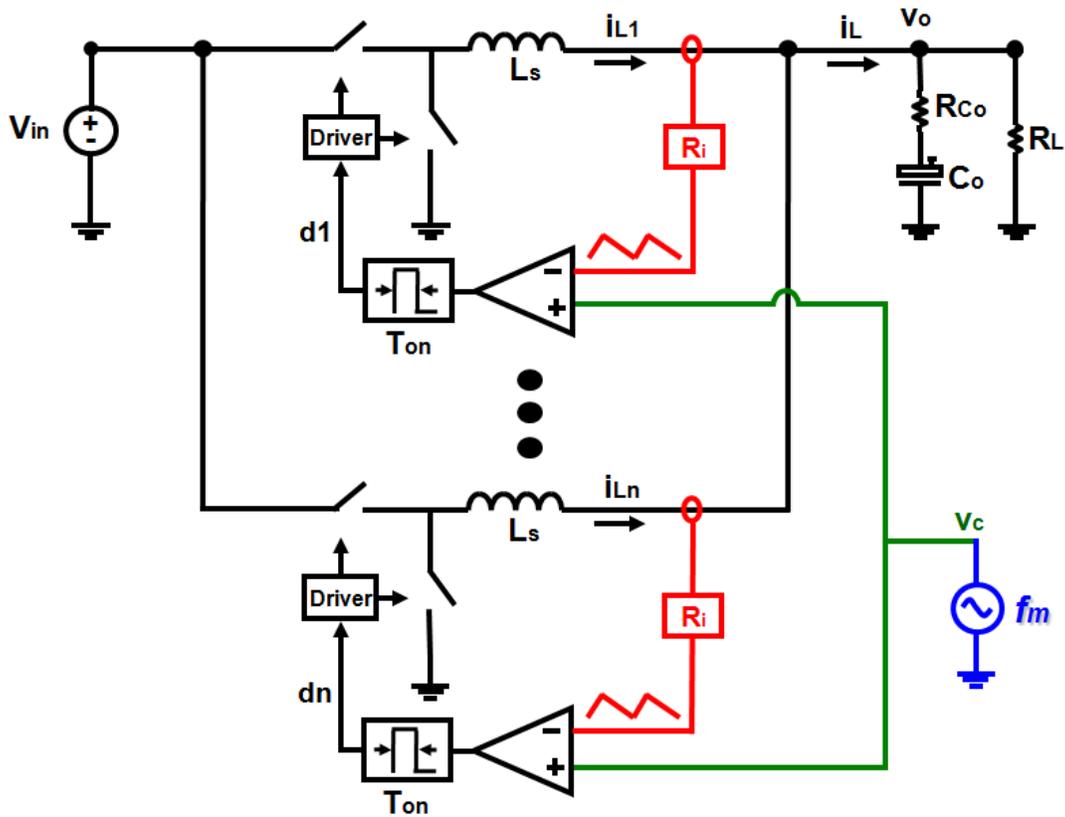
Figure 2.29. A multi-phase buck converter with constant on-time control (1)

This implementation is similar to previous case with peak current-mode control. So the model can be found as shown in Figure 2.30.
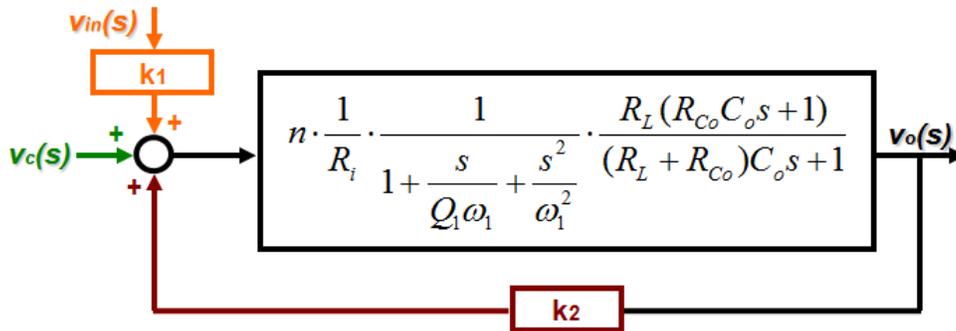
Figure 2.30. Multi-phase model for constant on-time control (1)

The other implementation is shown in Figure 2.31.
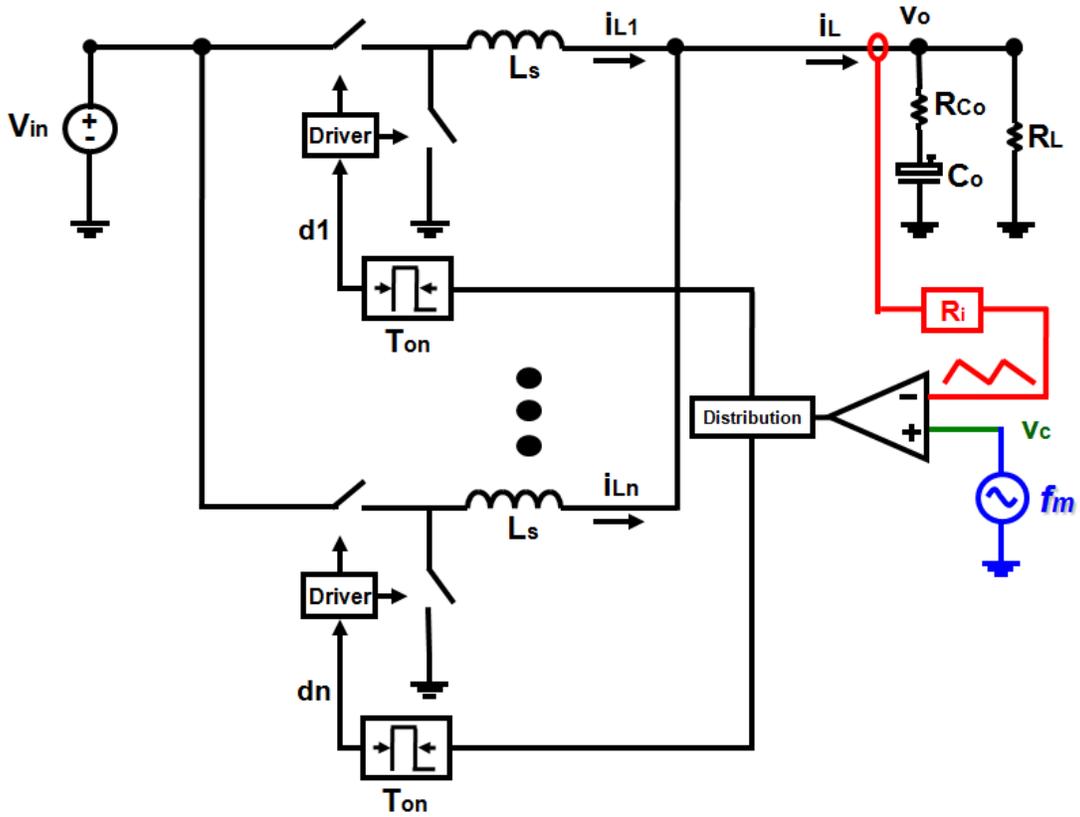
Figure 2.31. A multi-phase buck converter with constant on-time control (2)

The total current information is fed back to the modulator, and the on-time pulses are distributed to each phase. Interleaving can be achieved automatically. Generally speaking, this implementation can be used to the case of no duty cycle overlapping.

The slopes of the total inductor current ripple can be calculated as:

$$s_n = R_i \frac{V_{in} - nV_o}{L_s} \qquad (2.35)$$

$$s_f = R_i \frac{nV_o}{L_s} \qquad (2.36)$$

Therefore, the multi-phase buck converter is equivalent to a single-phase buck converter, as shown in Figure 2.32. The switching frequency is n times of original f_s. The output voltage is n times of original V_o.
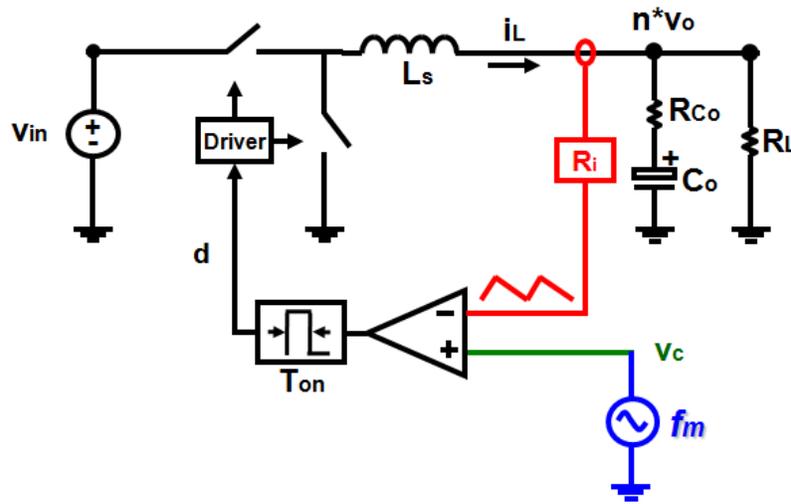
Figure 2.32. Equivalent single-phase buck converter

For this case, the model of the multi-phase buck converter with the constant on-time control is shown in Figure 2.33.
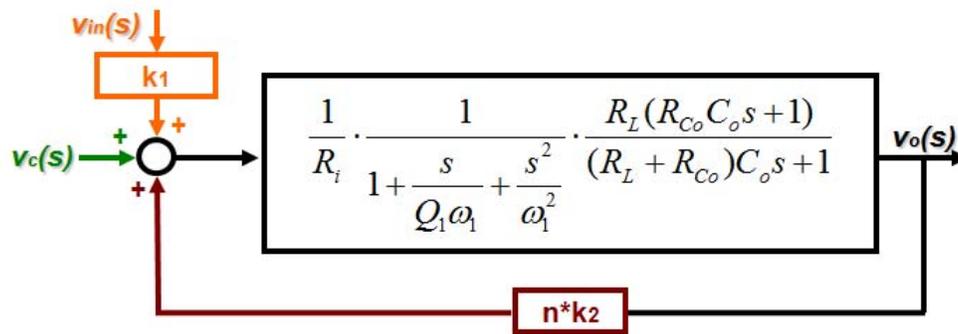
Figure 2.33. Multi-phase model for constant on-time control (2)

SIMPLIS simulation tool is used to simulate the system with 2 phase interleaving. Simulation results are shown in Figure 2.34 and Figure 2.35. It is clearly shown that the model results match with simulation results very well.
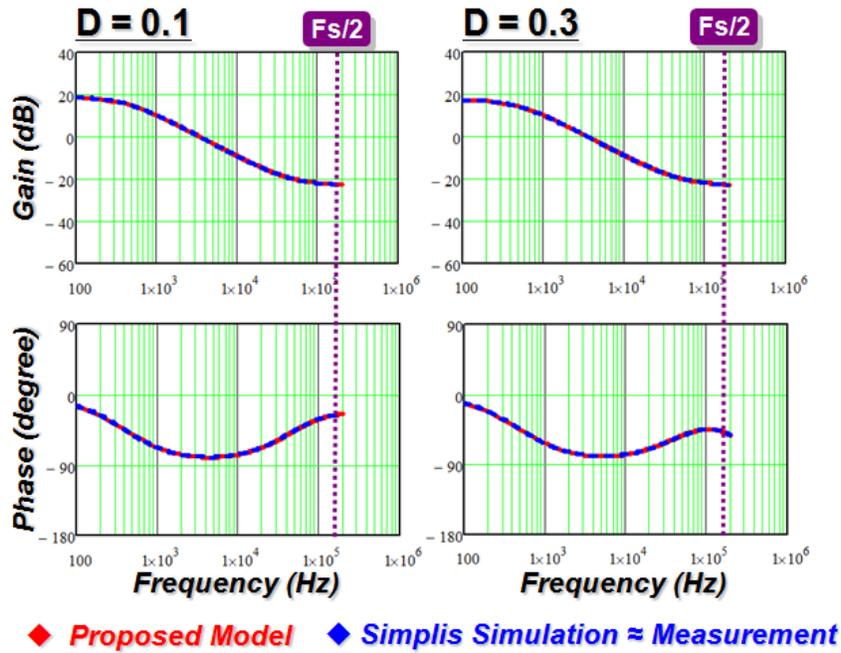
Figure 2.34. Control-to-output transfer function comparison for multi-phase buck converters with constant on-time control
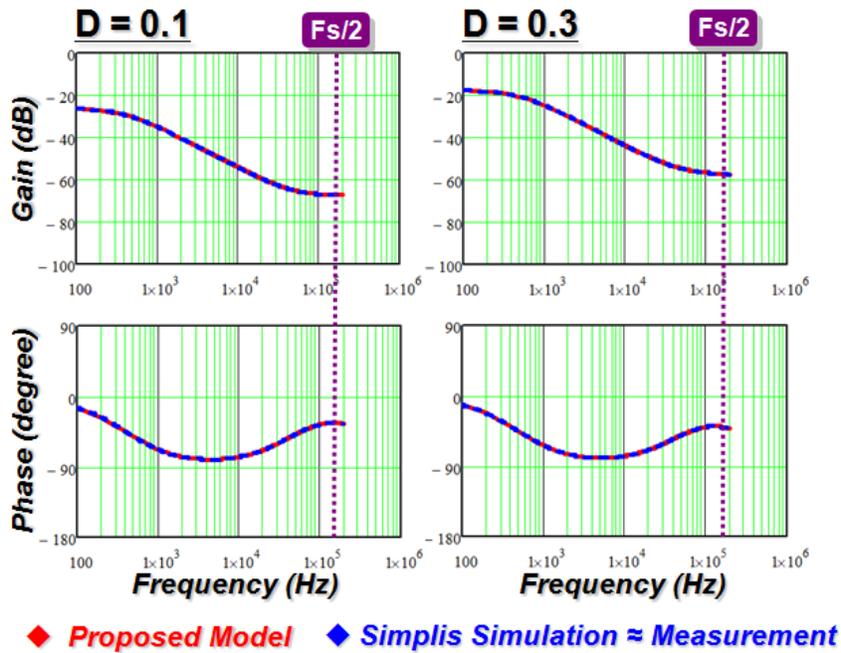
Figure 2.35. Audio susceptibility comparison for multi-phase buck converters with constant on-time control

2.6 Summary

In this chapter, a new modeling approach is presented for current-mode control. The inductor, the switches and the PWM modulator are treated as a single entity to model instead of breaking them into parts to do it. In the proposed modeling appproach, the DF method is applied on the closed-loop time-domain waveform to model the non-linear current-mode modulator to obtain the transfer function from the control signal v_c to the output voltage v_o. To do so, the current-loop sideband effects can be identified because the time-domain waveform includes all the effects due to the nonlinearity of the modulator.

In fact, the effectiveness of the model obtained from the new modeling approach is not limited by the switching frequency. The complete model without approximation can accurately predict the system response even beyond the switching frequency. For the practical purpose, the model is simplified and limited by the half of the switching frequency.

The fundamental difference between peak current-mode control and constant on-time control is elaborated based on the models obtained from the new modeling approach. The position of the double pole located at the high frequency is different for two cases. In peak current-mode control, there is a double pole located at $\omega_2 = \pi / T_{sw}$, and it is possible that the double pole moves to the right half-plane resulting in subharmonic oscillations in the current loop. However, in constant on-time control, there is a double pole located at $\omega_1 = \pi / T_{on}$, and the double pole will never move to the right half-plane. This is why there is no subharmonic oscillation in the current loop for constant on-time control.

The new modeling approach can be applied to other current-mode controls without any issue. The multi-phase extension is also shown in this chapter.

In sum, the model for current-mode control obtained from the new modeling approach is more accurate and effective than the previous models.

Chapter 3. Equivalent Circuit Representation of Current-Mode Control

Based on the precise model obtain in the previous chapter, this chapter introduces an equivalent circuit representation for current-mode control for the sake of easy understanding. The effect of the current loop is equivalent to controlling the inductor current as a current source with certain impedance. This circuit representation provides both the simplicity of the circuit model and the accuracy of the proposed model.

3.1 Equivalent Circuit Representation of Peak Current-Mode control

Based on the previous analysis, the complete model for the peak current-mode control is shown in Figure 3.1.
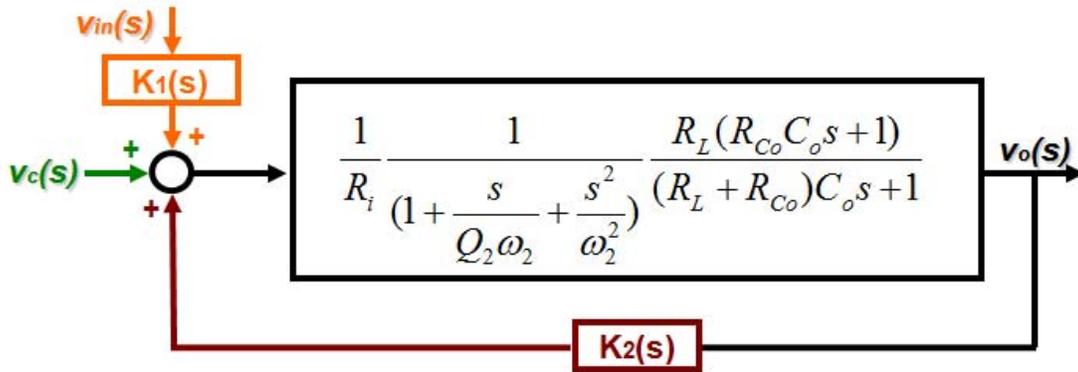
Figure 3.1. Complete model for peak current-mode control

where,

$$k_1(s) \approx k_1 \approx \frac{DR_i}{L_s}[\frac{1}{Q_2\omega_2} - \frac{T_{off}}{2}] \tag{3.1}$$

$$k_2(s) \approx k_2 \approx -\frac{R_i}{L_s Q_2 \omega_2} \tag{3.2}$$

As shown in Figure 3.1, the system model can be expressed by:

$$v_o(s) = \frac{v_c(s)}{R_i} \cdot \frac{Z_e(s) \cdot \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{Z_e(s) + L_s s + \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}} \tag{3.3}$$

$$v_o(s) = v_{in}(s) \cdot k_{vin} \cdot \frac{Z_e(s) \cdot \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{Z_e(s) + L_s s + \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}} \tag{3.4}$$

where, $Z_e(s) = L_s / [1/(Q_2\omega_2) + s/\omega_2^2]$ and $k_{vin} = k_1 / R_i = D / \{L_s[1/(Q_2\omega_2) - T_{off}/2]\}$. For the detail derivation and the case of considering the DCR of the inductor, please refer to Appendix C.

Therefore, based on (3.3) and (3.4), the equivalent circuit representation for peak current-mode control can be found as shown in Figure 3.2.
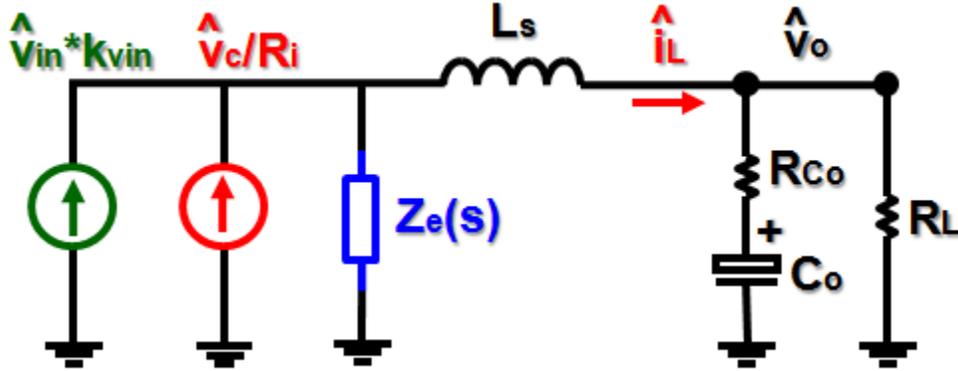
Figure 3.2. Equivalent circuit representation (w/ Z$_e$(s)) of peak current-mode control

The effect of the current loop is equivalent to controlling the inductor current as a current source with an impedance $Z_e(s)$. Comparing with the previous "current source" concept shown in Figure 1.17, the new model possesses an impedance $Z_e(s)$ and an additional current source representing the influence of the input voltage. The new model can greatly improve the accuracy without losing simplicity. Furthermore, the impedance $Z_e(s)$ can be expressed by a resistor R$_e$ and a capacitor C$_e$, as shown in Figure 3.3.
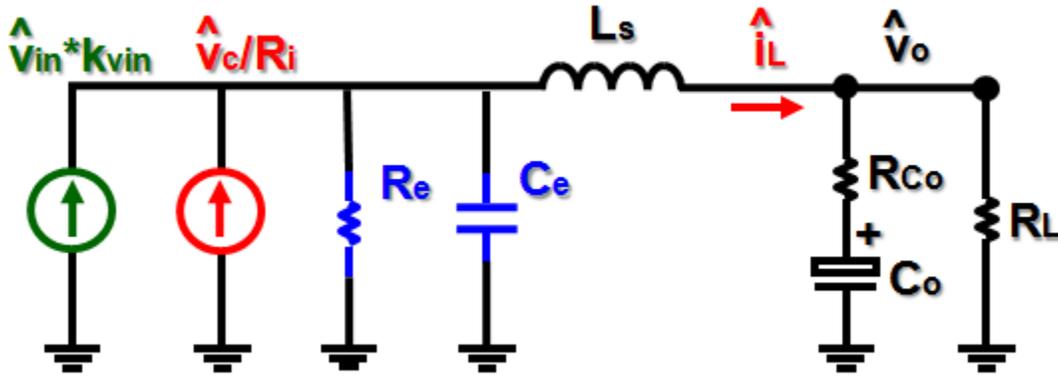
Figure 3.3. Equivalent circuit representation (w/ R_e and C_e) of peak current-mode control

where, $R_e = L_s Q_2 \omega_2$ and $C_e = 1/(L_s \omega_2^2)$.

Clear physical meaning can be found based on the new circuit model. The power stage inductor L_s is probably resonant with the output capacitor C_o or the equivalent capacitor C_e depending on the value of R_e. The R_e is relatively large when there is no external ramp, so the original double pole related to the power stage filter is split into two real poles. One pole moves to the low-frequency range. That' why the system behaves like a first order system in the low-frequency range.

Meanwhile, the other pole moving to the high-frequency range and a high-frequency pole result in another double pole at the frequency of ω_2 which is formed by the resonance between the inductor and the equivalent capacitor C_e. When the duty cycle is larger than 0.5, R_e becomes negative which makes the double pole move to the right half-plane and predicts subharmonic oscillations.

Adding the external ramp can effectively change the value of R_e. When the external ramp is too large, R_e becomes very small. The double pole at the frequency of ω_2 is split and the power stage double pole comes into being.

Under certain circumstance, the equivalent circuit model can be simplified to the "current-source" model as introduced in Chapter 1. In the low-frequency range, the capacitor C_e can be ignored as shown in Figure 3.4. Then, if R_e is large enough, the circuit can be further simplified to the "current-source" model, as shown in Figure 3.5.
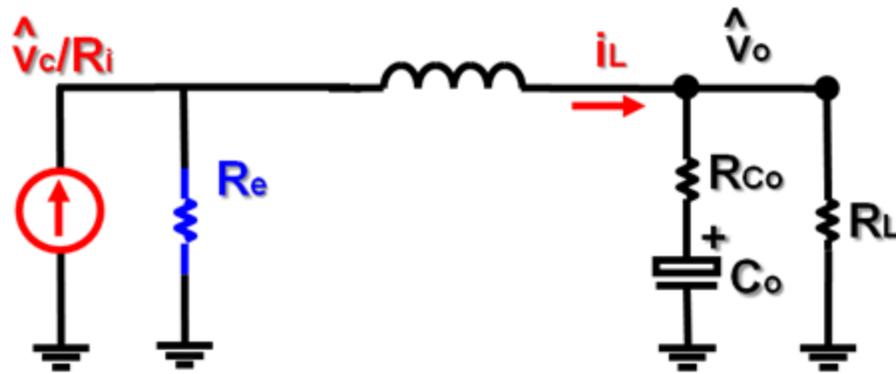
Figure 3.4. Simplified equivalent circuit (ignoring C_e)
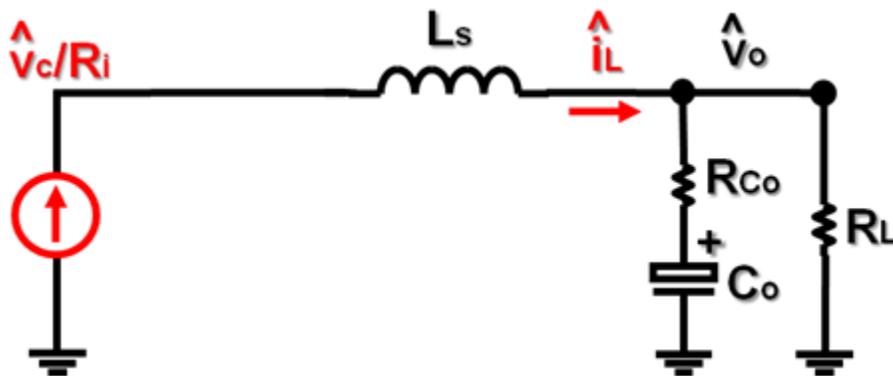
Figure 3.5. Simplified equivalent circuit (ignoring C_e and R_e)

The SIMPLIS simulation tool is used to verify the circuit model for peak current-mode control. The parameters of the buck converter are as follows: $V_{in} = 12V$, $V_o = 5.4V$, $D = 0.45$, $f_s = 300KHz$, $C_o = 8 \times 560\mu F$, $R_{Co} = 6/8m\Omega$, and $L_s = 300nH$. The control-to-output transfer function, the audio susceptibility and the output impedance comparisons are shown in Figure 3.6, Figure 3.7 and Figure 3.8. There is a little phase discrepancy in the audio susceptibility due to the approximation of $k_1(s)$.
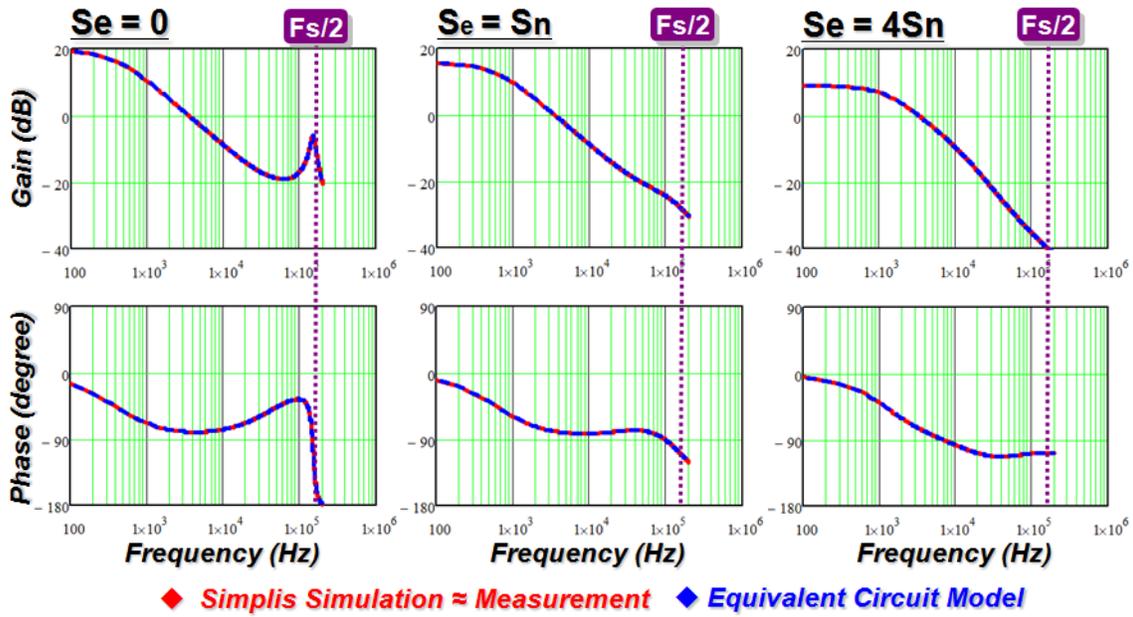
Figure 3.6. Control-to-output transfer function comparison in peak current-mode control
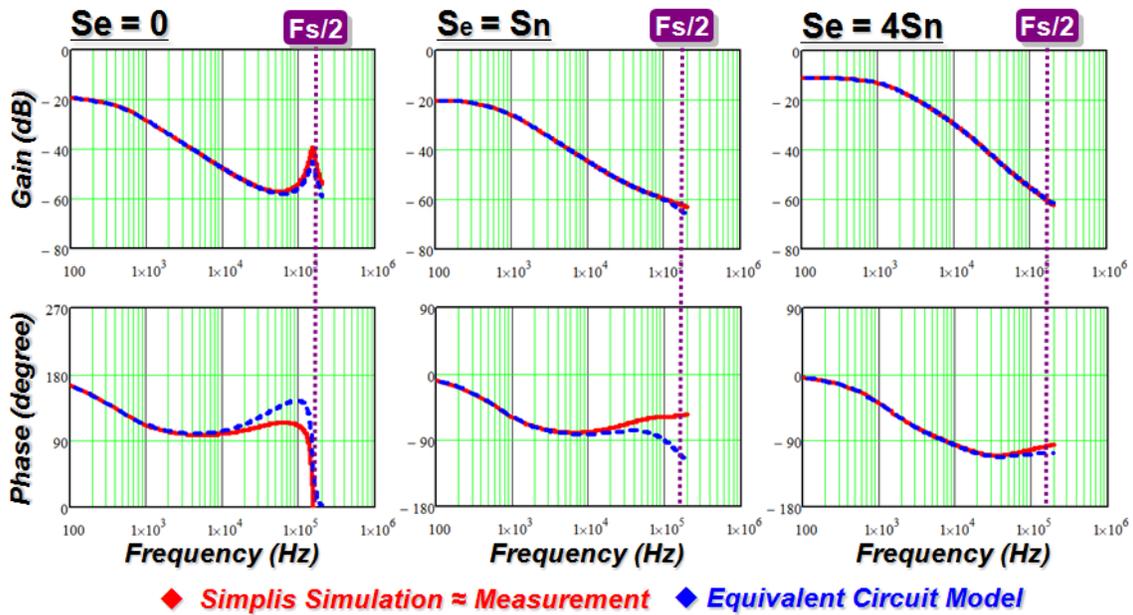
Figure 3.7. Audio susceptibility comparison in peak current-mode control
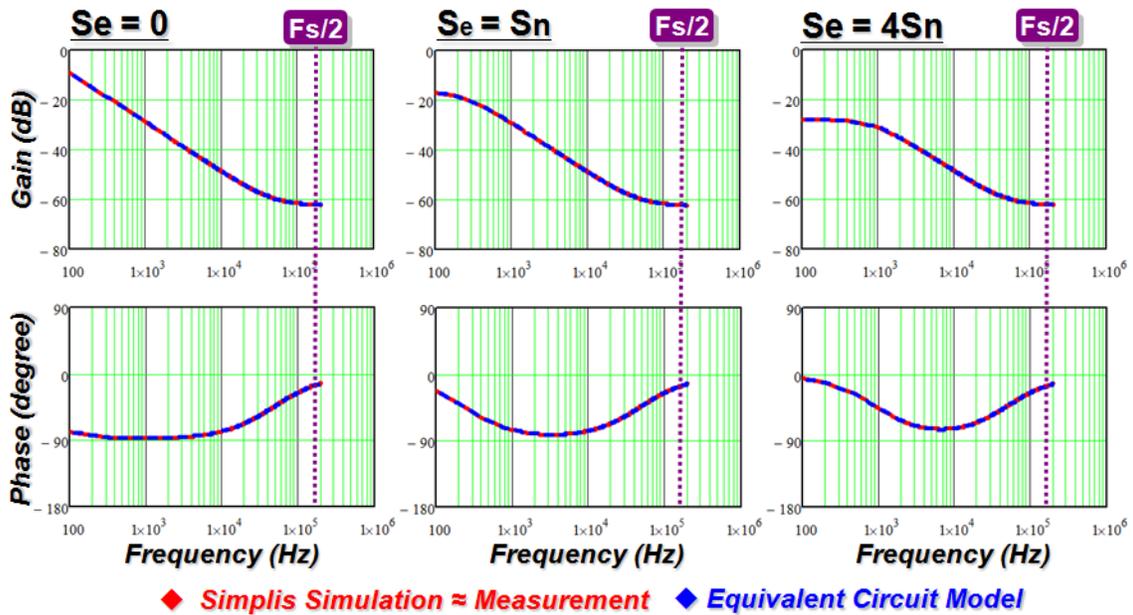
Figure 3.8. Output impedance comparison in peak current-mode control

Based on the multi-phase model of peak current-mode control in Chapter 2, the equivalent circuit model for multi-phase buck converters with peak current-mode control is shown in Figure 3.9,
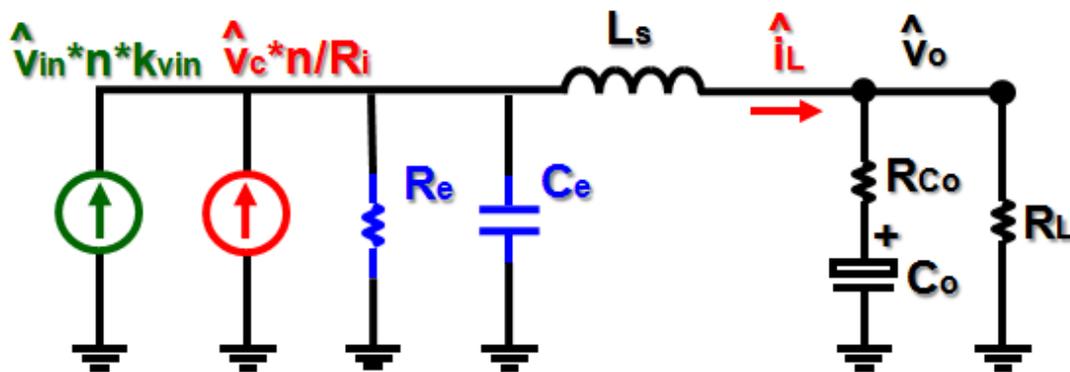
Figure 3.9. Equivalent circuit representation (w/ R_e and C_e) of multi-phase buck converters with peak current-mode control

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3.2   Equivalent Circuit Representation of Constant On-time Control

Based on the similar methodology, the equivalent circuit representation for constant on-time control is shown in Figure 3.10.
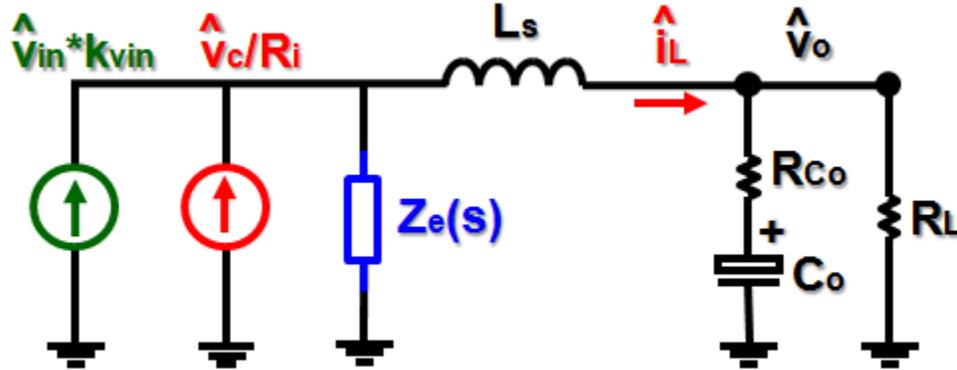
Figure 3.10. Equivalent circuit representation (w/ Z_e(s)) of constant on-time control

where, $Z_e(s) = L_s /[1/(Q_1\omega_1) + s/\omega_1^2]$ and $k_{vin} = k_1/R_i = T_{on}/(2L_s)$.

Furthermore, the impedance Z_e(s) can be expressed by a resistor R_e and a capacitor C_e, as shown in Figure 3.11.
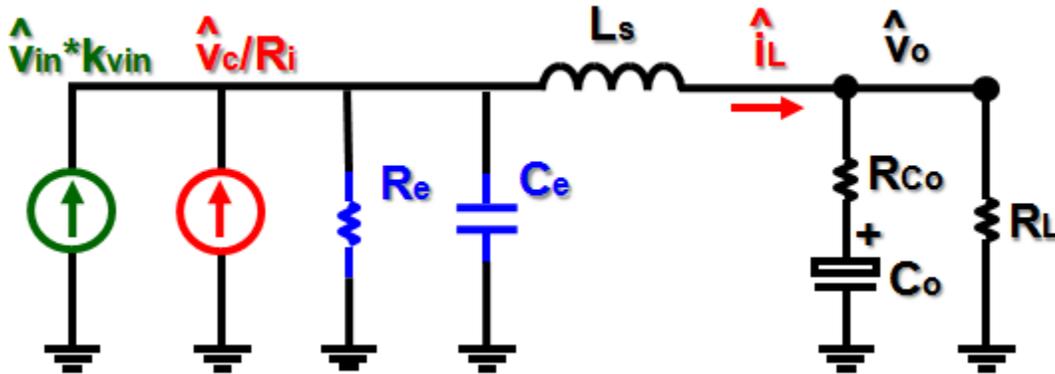
Figure 3.11. Equivalent circuit representation (w/ R_e and C_e) of constant on-time control

In constant on-time control, the situation is much simpler than peak current-mode control. The R_e is relatively large, so the original power stage double pole is split into two

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real poles. One pole moves to the low-frequency range. This is why the system behaves like a first order system in the low-frequency range.

Meanwhile, the other pole moving to the high-frequency range and another high-frequency pole result in another double pole at the frequency of ω_1 which is formed by the resonance between the inductor and the equivalent capacitor C_e. However, this double pole never move to the right half-plane, which predicts that there is no subharmonic oscillation in constant on-time control.

The SIMPLIS simulation tool is used to verify the circuit model for constant on-time control. The parameters of the buck converter are as follows: $V_{in} = 12V$, , $f_s \approx 300KHz$, $C_o = 8 \times 560\mu F$, $R_{Co} = 6/8m\Omega$, and $L_s = 300nH$. The control-to-output transfer function, the audio susceptibility and the output impedance comparisons are shown in Figure 3.12, Figure 3.13, and Figure 3.14. There is a little phase discrepancy in the audio susceptibility due to the approximation of $k_1(s)$.
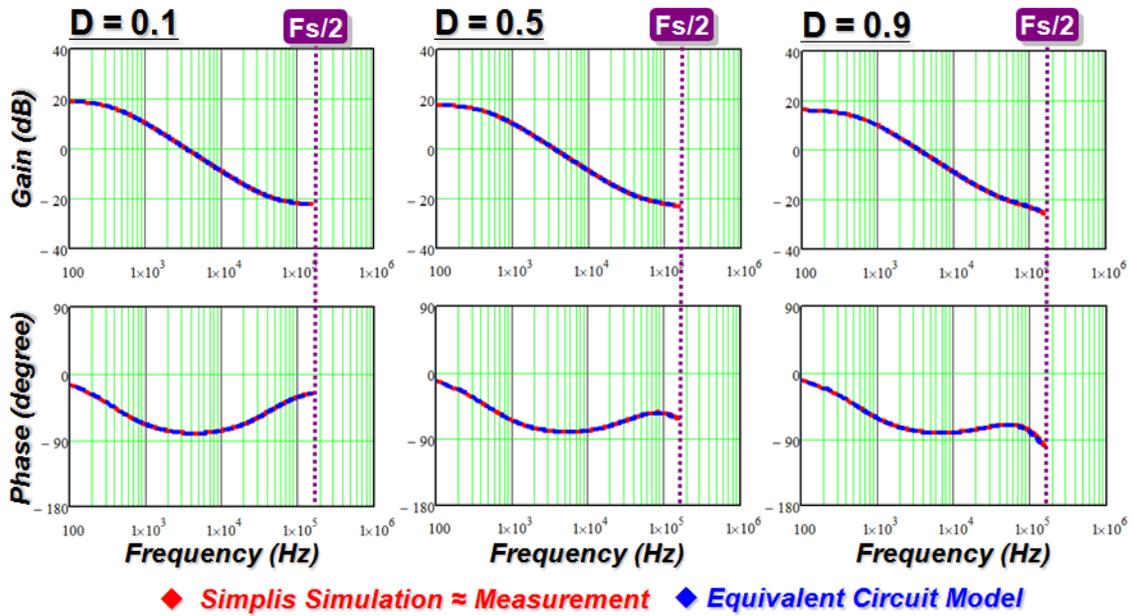
Figure 3.12. Control-to-output transfer function comparison in constant on-time control
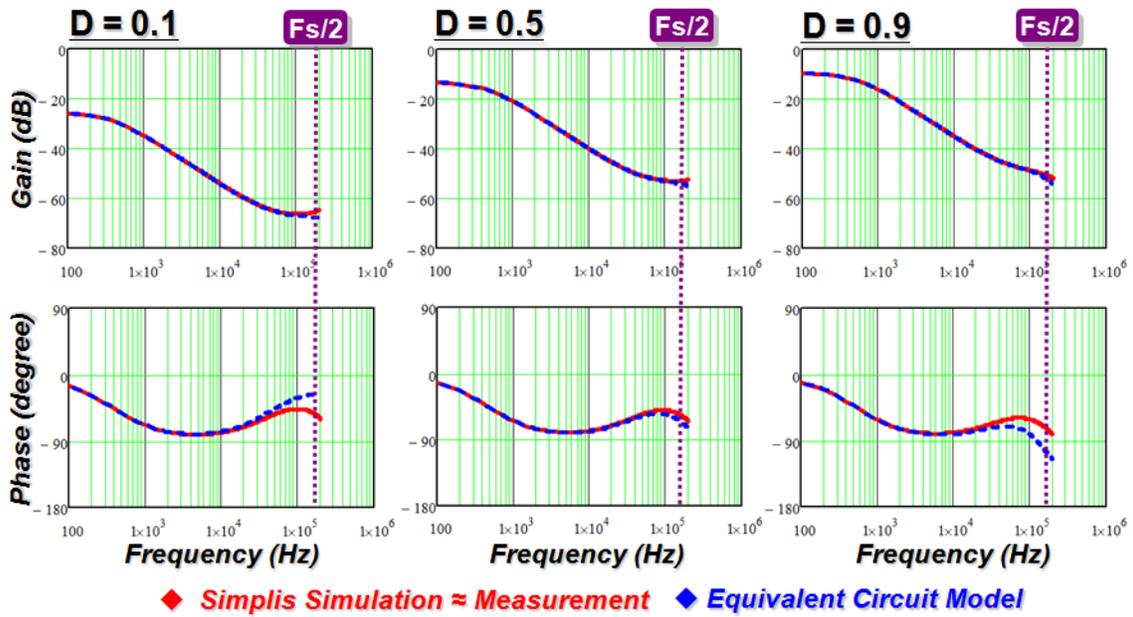
Figure 3.13. Audio susceptibility comparison in constant on-time control
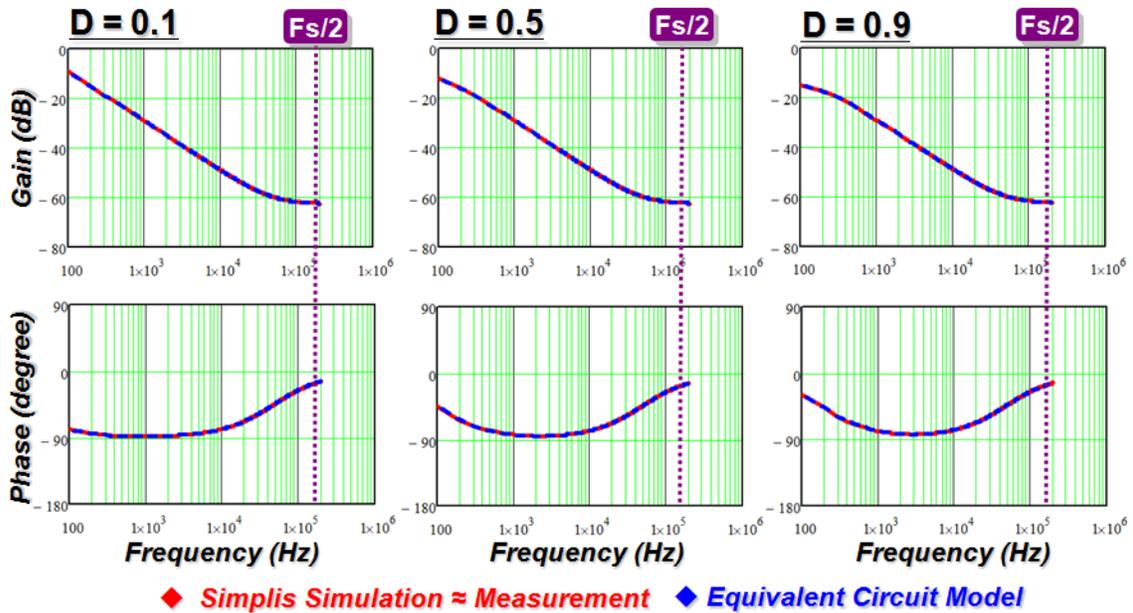
Figure 3.14. Output impedance comparison in constant on-time control

For the simplicity, the equivalent capacitor C_e can be ignored for practical design.

Based on the multi-phase model of constant on-time control in Chapter 2, the equivalent circuit models for the multi-phase buck converters with constant control are shown in Figure 3.15 and Figure 3.16.
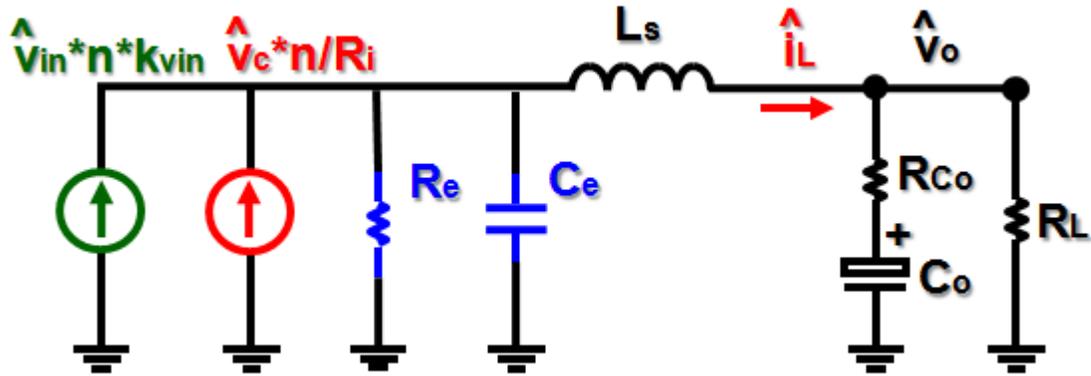
Figure 3.15. Equivalent circuit representation (w/ R_e and C_e) of multi-phase buck converters with constant on-time control based on the implementation (1)
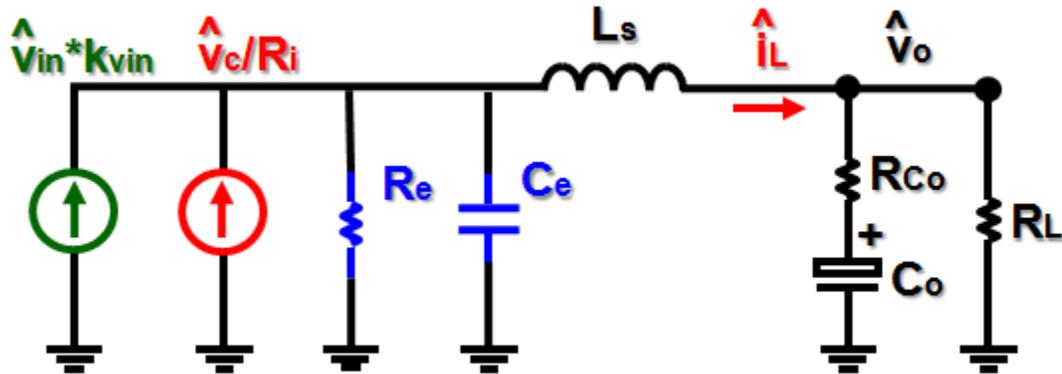
Figure 3.16. Equivalent circuit representation (w/ R_e and C_e) of multi-phase buck converters with constant on-time control based on the implementation (2)

3.3   Extension to Other Current-Mode Controls

The equivalent circuit representation can be extended to other current-mode controls. For valley current-mode control and constant off-time control, the circuit is the same as the one shown in Figure 3.11, and the parameters are shown in as shown in Table 3.1 and Table 3.2.

Table 3.1. Circuit parameters for valley current mode control

$R_e = L_s Q_2' \omega_2$	$C_e = \dfrac{1}{L_s \omega_2^2}$	$k_{vin} = \dfrac{k_1}{R_i} = \dfrac{D}{L_s}[\dfrac{1}{Q_2' \omega_2} + \dfrac{T_{off}}{2}]$

Table 3.2. Model extension for constant off-time control

$R_e = L_s Q_1 \omega_3$	$C_e = \dfrac{1}{L_s \omega_3^2}$	$k_{vin} = \dfrac{k_1}{R_i} \approx 0$

The circuit representation for charge control is shown in Figure 3.17, and the circuit parameters are shown in Table 3.3.
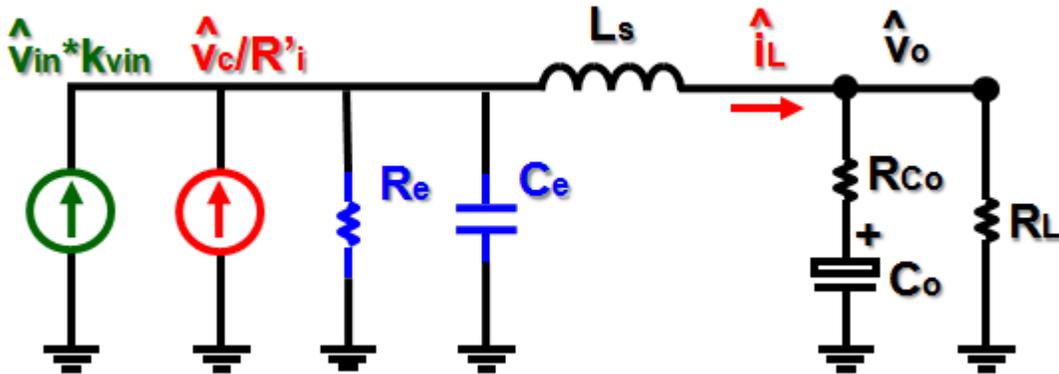
Figure 3.17. Equivalent circuit representation (w/ R$_e$ and C$_e$) in charge control

Table 3.3. Model extension for charge control

$R_i' = \dfrac{R_i T_{on}}{C_T}$	$R_e = L_s Q_c \omega_2$	$C_e = \dfrac{1}{L_s \omega_2^2}$	$k_{vin} = \dfrac{k_1}{R_i'} = \dfrac{D}{L_s}[\dfrac{1}{Q_c \omega_2} + \dfrac{T_{on}}{2}]$

3.4 Summary

This chapter presented an equivalent circuit representation for current-mode control for the sake of easy understanding. The effect of the current loop is equivalent to controlling the inductor current as a current source with certain impedance. This circuit representation can provide both the simplicity of the circuit model and the accuracy of the proposed model for practical design.

Chapter 4. Modeling for V^2 Current-Mode Control

V^2 type of constant on-time control has been widely used to improve light-load efficiency. However, the delay due to the capacitor ripple results in subharmonic oscillations in V^2 constant on-time control. This chapter presents a new modeling approach for V^2 constant on-time control. The power stage, the switches and the PWM modulator are treated as a single entity and modeled based the describing function method. The model for V^2 constant on-time control achieved by the new approach can accurately predict subharmonic oscillation. Two solutions are discussed to solve the instability issue. The extension of the model to other types of V^2 current-mode controls is also shown in this chapter. Simulation and experimental results are used to verify the proposed model.

4.1   Subharmonic Oscillations in V^2 Current-Mode Control

Based on different modulation schemes, V^2 control architectures consist of constant-frequency peak voltage control, constant-frequency valley voltage control, constant on-time control, constant off-time control and hysteretic control. Among all of these control structures, the constant on-time control is the most widely used to improve light-load efficiency, since the switching frequency can be lowered to reduce switching-related loss, as shown in Figure 4.1. In the V^2 implementation, the nonlinear PWM modulator becomes much more complicated, because not only is the inductor current information fed back to the modulator, but the capacitor voltage ripple information is fed back to the modulator as well. Generally speaking, there is no subharmonic oscillation in constant on-time control. However, the delay due to the capacitor ripple results in subharmonic oscillations in V^2 constant on-time control. The influence of the capacitor ripple is shown in Figure 4.2. For those four cases, the ESR ripple keeps the same while the capacitor ripple becomes larger and larger. When the capacitor ripple is larger than certain amplitude, subharmonic oscillations occur.
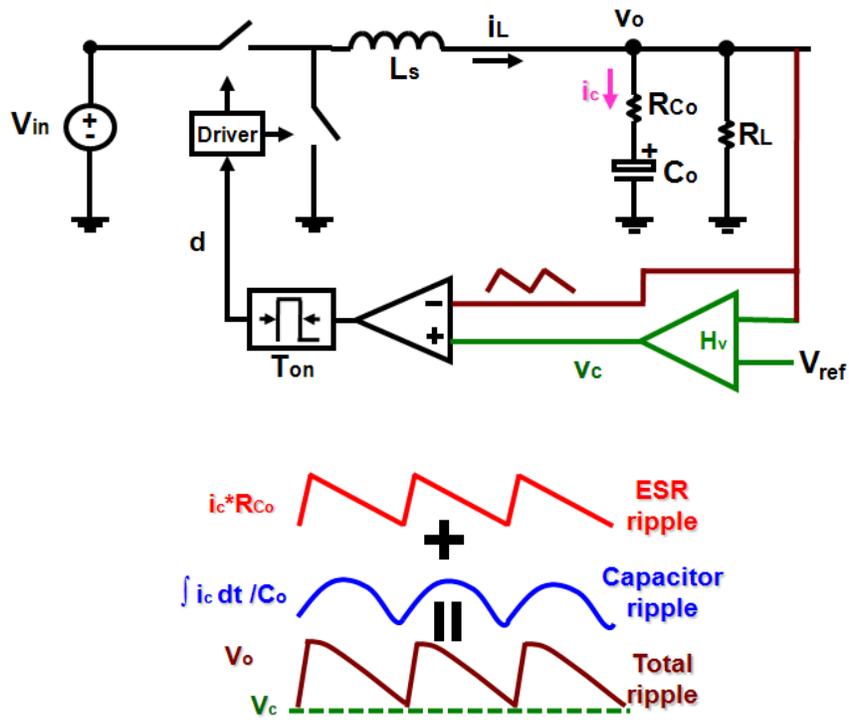
Figure 4.1. V^2 constant on-time control
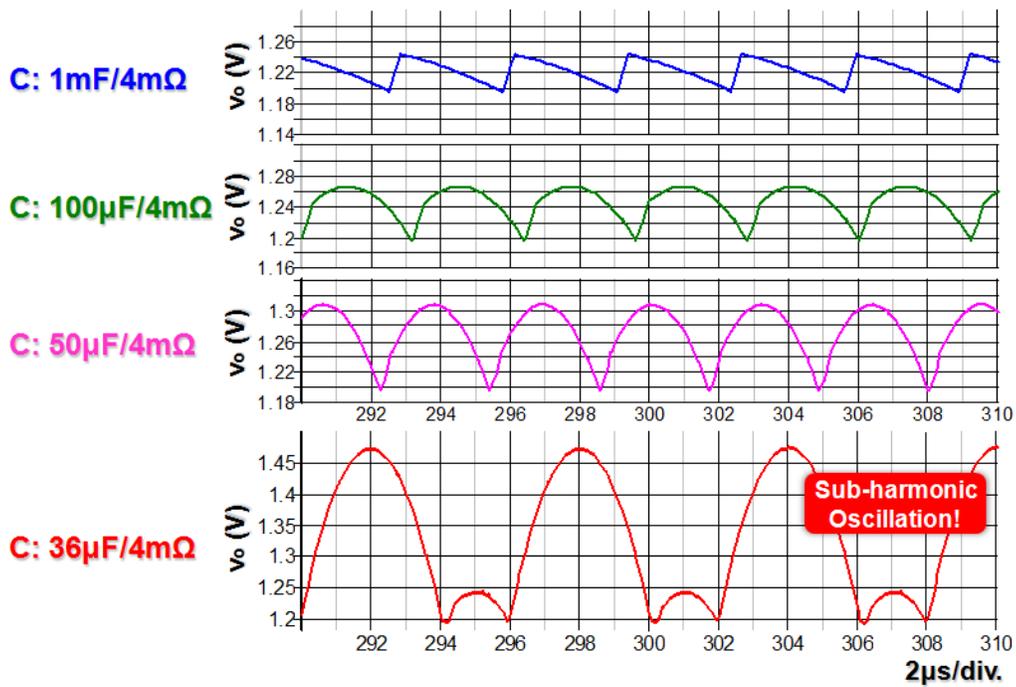
Figure 4.2. The influence of the capacitor ripple in V^2 constant on-time control

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An example with the parameters of the existing capacitors is shown in Figure 4.3. The system is stable when used with the OSCON capacitor, because the inductor current information dominates the total output voltage ripple; meanwhile subharmonic oscillations occur when the ceramic capacitor is used in constant on-time control, since the capacitor voltage ripple is too large. This phenomenon also occurs in peak voltage control.
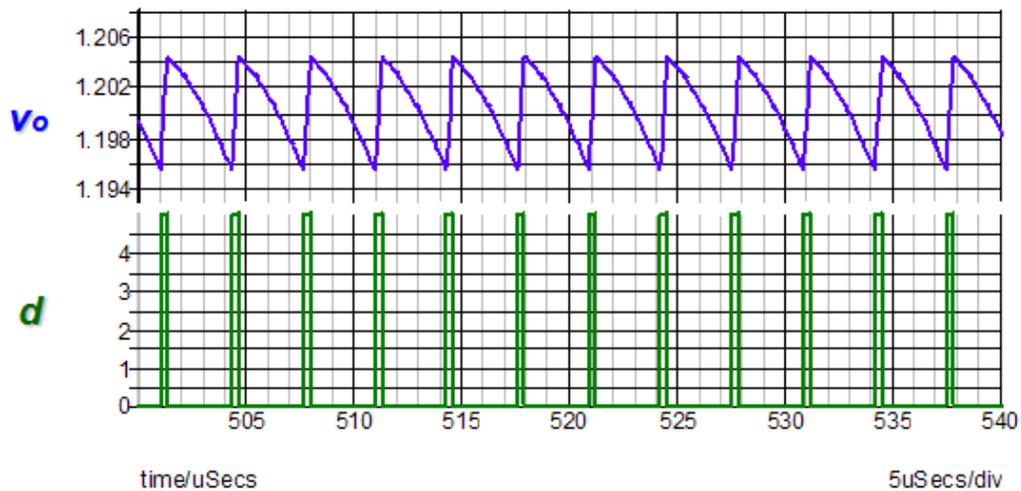
(a)
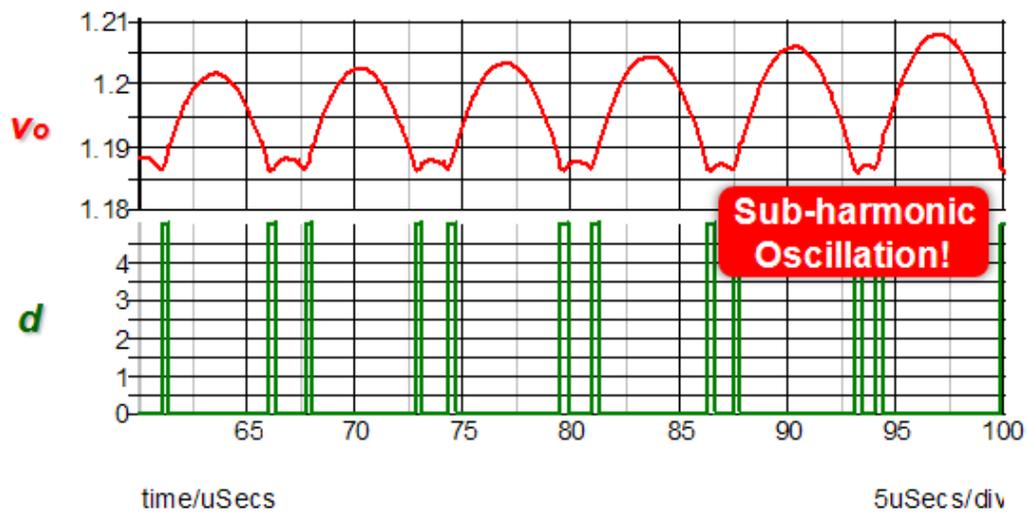
(b)

Figure 4.3. Subharmonic oscillation in V² constant on-time control: (a) OSCON capacitor (560μF/6mΩ), and (b) Ceramic capacitor (100μF/1.4mΩ)

4.2 Proposed Modeling Approach for V^2 Constant On-time Control

If the influence of the capacitor ripple is ignored, the model for V^2 constant on-time control can be obtained from the extension of previous results, as shown in Figure 4.4.
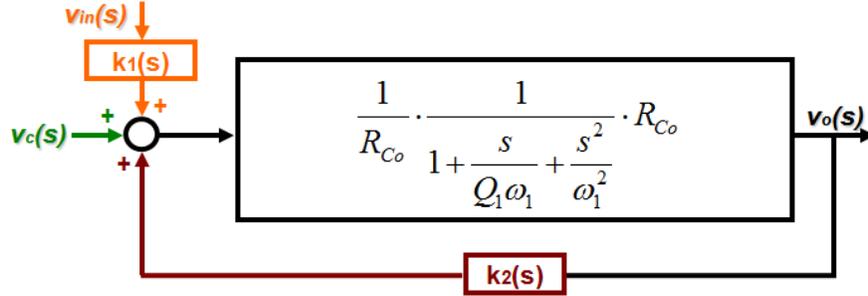
Figure 4.4. Simple model for V^2 constant on-time control

The control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{1 + \dfrac{s}{Q_1 \omega_1} + \dfrac{s^2}{\omega_1^2}} \tag{4.1}$$

This model shows that the control signal can control the output voltage very well in the low-frequency range. However, it is too simple to predict subharmonic oscillations.

In order to consider the effects of the capacitor ripple, the new modeling approach is extended to V^2 constant on-time control. As shown in Figure 4.5, the non-linear constant on-time modulator consists of switches, the output voltage, the comparator and the on-time generator. It's reasonable to treat these components as a single entity to model instead of breaking them into parts. In the proposed modeling approach, the describing function (DF) method is used to model the non-linear current-mode modulator to obtain the transfer function from the control signal v_c to the output voltage v_o.

As shown in Figure 4.5, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the control signal v_c; then based on the perturbed output voltage waveform, the describing function from the control signal v_c to the output voltage v_o can be found by mathematical derivation.
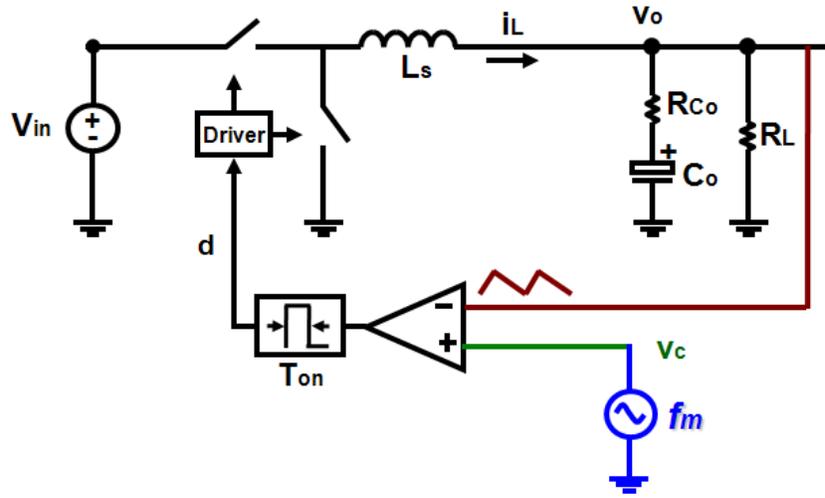
Figure 4.5. Modeling strategy for V² constant on-time control

Before applying the DF method, it is necessary to make several assumptions: (i) the magnitude of the inductor current slopes during the on-period and the off-period stays constant separately; (ii) the magnitude of the perturbation signal is very small; and (iii) the perturbation frequency f_m and the switching frequency f_s are commensurable, which means that $N \times f_s = M \times f_m$, where N and M are positive integers. Following the modulation law of constant on-time control, the duty cycle and the output voltage waveforms are shown in Figure 4.6.
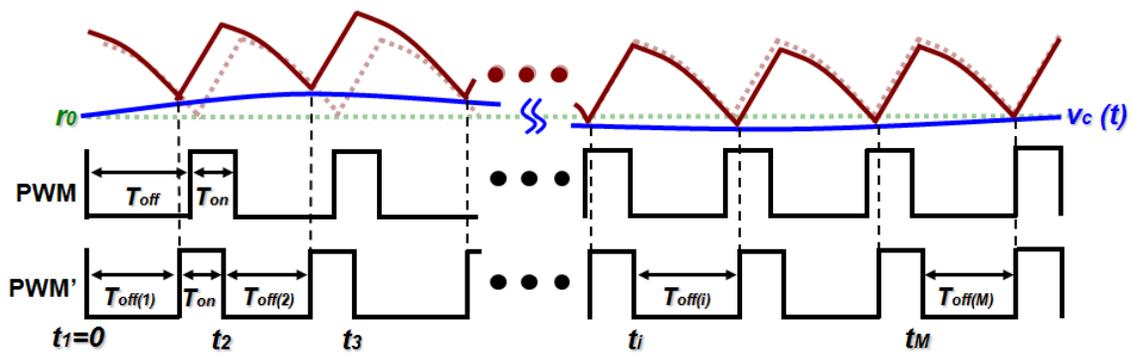
Figure 4.6 Perturbed output voltage waveform

Because the on-time T_{on} is fixed, the off-time T_{off} is modulated by the perturbation signal $v_c(t)$: $v_c(t) = r_0 + \hat{r}\sin(2\pi f_m \cdot t - \theta)$, where r_0 is the steady-state DC value of the

control signal, $\hat{r}_0$ is the magnitude of the perturbation, and θ is the initial angle. Based on the modulation law, it is found that:

$$v_c(t_{i-1} + T_{off(i-1)}) + s_n T_{on} - s_f T_{off(i)} - \frac{\int_{t_{i-1}+T_{off(i-1)}}^{t_i+T_{off(i)}} [i_L(t) - v_o(t)/R_L]dt}{C_o} = v_c(t_i + T_{off(i)}) \qquad (4.2)$$

where, $T_{off(i)}$ is the i_{th} cycle off-time, $s_n = R_{Co}(V_{in} - V_o)/L_s$, $s_f = R_{Co}V_o/L_s$, L_s is the inductance of the inductor, R_{Co} is the ESR of the output capacitors, C_o is the capacitance of the output capacitors, R_L is the load resistor, $i_L(t)$ is the inductor current, and $v_o(t)$ is the output voltage. Assuming $T_{off(i)} = T_{off} + \Delta T_{off(i)}$, where T_{off} is the steady state off-time, and $\Delta T_{off(i)}$ is the i_{th} cycle off-time perturbation, t_i can be calculated as: $t_i = (i-1)(T_{on} + T_{off}) + \sum_{k=1}^{i-1} \Delta T_{off(k)}$. Based on (4.2), it is found that:

$$
\begin{aligned}
& s_f[(1 + \frac{T_{off}}{2C_o R_{Co}})\Delta T_i - (1 - \frac{2T_{on} + T_{off}}{2C_o R_{Co}})\Delta T_{i-1}] \\
& = [v_c(t_{i-1} + T_{off(i-1)}) - v_c(t_i + T_{off(i)})] - [v_c(t_{i-2} + T_{off(i-2)}) - v_c(t_{i-1} + T_{off(i-1)})] \\
& - [v_c(t_{i-1} + T_{off(i-1)} + \frac{\pi}{2\pi f_m \cdot 2}) - v_c(t_i + T_{off(i)} + \frac{\pi}{2\pi f_m \cdot 2})]/(2\pi f_m \cdot R_L C_o) \\
& + [v_c(t_{i-2} + T_{off(i-2)} + \frac{\pi}{2\pi f_m \cdot 2}) - v_c(t_{i-1} + T_{off(i-1)} + \frac{\pi}{2\pi f_m \cdot 2})]/(2\pi f_m \cdot R_L C_o)
\end{aligned}
\qquad (4.3)
$$

The perturbed duty cycle $d(t)$ and the perturbed inductor current $i_L(t)$ can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M}[u(t - t_i - T_{off(i)}) - u(t - t_i - T_{off(i)} - T_{on})] \qquad (4.4)$$

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \int_0^t [\frac{V_{in}}{L_s} d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} - \frac{V_o}{L_s}]dt + i_{L0} \qquad (4.5)$$

where, u(t)=1 when t>0, and i_{L0} is the initial value of the inductor current.

Then, the Fourier analysis can be performed on the inductor current:

$$c_{m(iL)} = j2f_m/N \cdot \int_0^{t_M + T_{off(M)} + T_{on}} i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} \cdot e^{-j2\pi f_m t} dt \qquad (4.6)$$

where, $c_{m(iL)}$ is the Fourier coefficient at the perturbation frequency f_m for the inductor current. Based on the result in Chapter 2, the coefficient can be calculated as:

$$c_{m(iL)} = \frac{f_s}{s_f} \frac{(1-e^{-j2\pi f_m T_{on}})(1-e^{-j2\pi f_m T_{sw}})(1-\frac{e^{j\frac{\pi}{2}}}{2\pi f_m \cdot R_L C_o})}{(1+\frac{T_{off}}{2C_o R_{Co}})-(1-\frac{2T_{on}+T_{off}}{2C_o R_{Co}})e^{-j2\pi f_m T_{sw}}} \frac{V_{in}}{L_s \cdot j2\pi f_m} e^{-j\theta} \tag{4.7}$$

where, T_{sw} is the steady-state switching period.

Next, the Fourier coefficient $c_{m(vo)}$ of the output voltage v_o can be calculated based on:

$$c_{m(vo)} = c_{m(iL)} \cdot \frac{R_L(R_{Co}C_o \cdot j2\pi f_m +1)}{(R_L+R_{Co})C_o \cdot j2\pi f_m +1} \tag{4.8}$$

The Fourier coefficient at the perturbation frequency f_m for the control signal $v_c(t)$ is $\hat{r}\cdot e^{-j\theta}$, so the describing function from the control-to-output can be calculated as:

$$\frac{v_{o(f_m)}}{v_{c(f_m)}} = \frac{f_s}{s_f} \frac{(1-e^{-j2\pi f_m T_{on}})(1-e^{-j2\pi f_m T_{sw}})(1-\frac{e^{j\frac{\pi}{2}}}{2\pi f_m \cdot R_L C_o})}{(1+\frac{T_{off}}{2C_o R_{Co}})-(1-\frac{2T_{on}+T_{off}}{2C_o R_{Co}})e^{-j2\pi f_m T_{sw}}} \frac{V_{in}}{L_s \cdot j2\pi f_m} \frac{R_L(R_{Co}C_o \cdot j2\pi f_m +1)}{(R_L+R_{Co})C_o \cdot j2\pi f_m +1}$$

$$\tag{4.9}$$

Note that the results are not applicable to frequencies where $f_m = n \times f_s$, where n is a positive integer. In order to avoid getting too granular, the results at those frequencies are not shown here. The influence from the variation of the inductor current slope is ignored since it is much smaller than the influence of the capacitor voltage ripple. In the s-domain, the control-to-output transfer function can be expressed by:

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s}{s_f} \frac{(1-e^{-sT_{on}})(1-e^{-sT_{sw}})(1+\frac{1}{R_L C_o s})}{(1+\frac{T_{off}}{2C_o R_{Co}})-(1-\frac{2T_{on}+T_{off}}{2C_o R_{Co}})e^{-sT_{sw}}} \frac{V_{in}}{L_s s} \frac{R_L(R_{Co}C_o \cdot s+1)}{(R_L+R_{Co})C_o \cdot s+1} \tag{4.10}$$

This transfer function is effective at frequencies even beyond half of the switching frequency if there is no outer loop compensation. Padé approximation is used to simplify the transfer function as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\frac{s}{Q_3\omega_2}+\frac{s^2}{\omega_2^2})}$$ (4.11)

where, $\omega_1 = \pi/T_{on}$, $Q_1 = 2/\pi$, $\omega_2 = \pi/T_{sw}$, $Q_3 = T_{sw}/[(R_{Co}C_o - T_{on}/2)\pi]$, and $R_L \gg R_{Co}$. The simplification is valid for up to half of the switching frequency. Comparing (4.11) with (4.1), it is found that the low-frequency response is the same, while the high-frequency response is different. When the duty cycle is relatively small, the transfer function can be further simplified as:

$$\frac{v_o(s)}{v_c(s)} \approx (R_{Co}C_o \cdot s+1)/(1+\frac{s}{Q_3\omega_2}+\frac{s^2}{\omega_2^2})$$ (4.12)

From the transfer function, it is clear that the double pole at half of the switching frequency may move to the right half-plane according to different capacitors' parameters. The critical condition for stability is $R_{Co}C_o > T_{on}/2$, which clearly shows the influence of the capacitance ripple.

The control-to-output voltage transfer function comparison between peak current-mode control and V² constant-on time control is shown in Figure 4.7. In peak current-mode control, the Q factor of the double pole at half of the switching frequency is determined by the duty cycle and the external ramp: if there no external ramp, when the duty cycle is larger than 0.5, the double pole will move to the right half-plane and the system becomes unstable. In V² constant on-time control, the Q factor is not only related to the on-time T_{on}, but also related to capacitor parameters. The critical condition $R_{Co}C_o > T_{on}/2$ reflects the interaction between the ESR and the capacitance of the output capacitor, which means that those two parameters must be considered at the same time. Different types of capacitors result in different system performance. When f_s = 300 KHz and D ≈ 0.1, the parameters of the OSCON capacitors (560μF/6mΩ) meet the critical condition, so the system is stable. However, the parameters of the ceramic capacitors

(100μF/1.4mΩ) cannot meet the critical condition, so subharmonic oscillations occur, as shown in Figure 4.3.
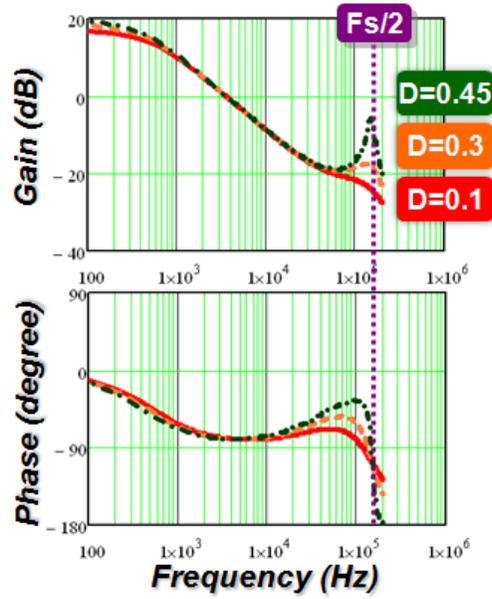
(a)
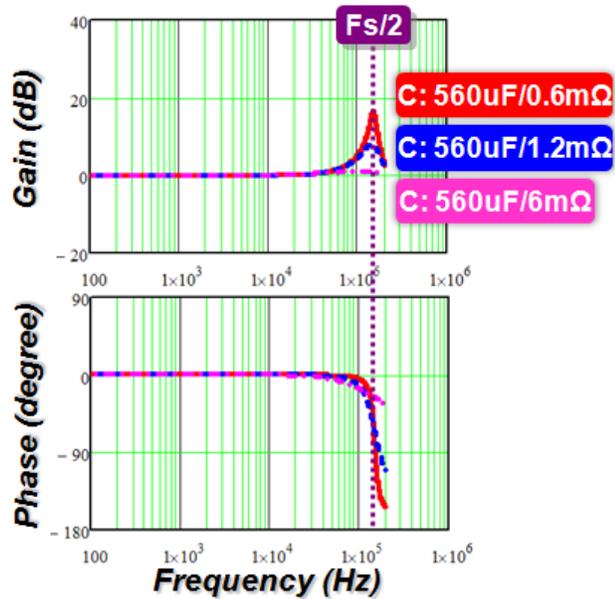
(b)

Figure 4.7. Control-to-output transfer function comparison: (a) in peak current-mode control, and (b) in V² constant on-time control

The output impedance can be also derived based on the similar methodology. As shown in Figure 4.8, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the output current i_o, then based on the perturbed output voltage waveform, the describing function from the output current i_o to the output voltage v_o can be found out by mathematical derivation.
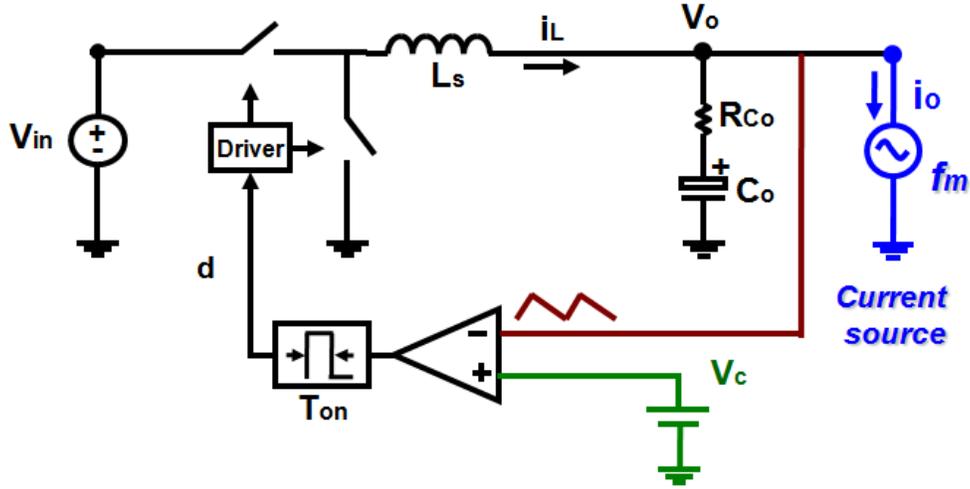
Figure 4.8. Model methodology for output impedance

In the s-domain, the output impedance is derived as:

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} = [\frac{f_s}{s_f} \frac{(1 - e^{-sT_{on}})(1 - e^{-sT_{sw}})(R_{Co} + \frac{1}{C_o s})}{(1 + \frac{T_{off}}{2C_o R_{Co}}) - (1 - \frac{2T_{on} + T_{off}}{2C_o R_{Co}})e^{-sT_{sw}}} \frac{V_{in}}{L_s s} - 1] \cdot (R_{Co} + \frac{1}{C_o s}) \qquad (4.13)$$

The simplified output impedance is expressed as:

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} \approx [\frac{1}{(1 + \frac{s}{Q_1 \omega_1} + \frac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s + 1)}{(1 + \frac{s}{Q_3 \omega_2} + \frac{s^2}{\omega_2^2})} - 1] \cdot (R_{Co} + \frac{1}{C_o s}) \qquad (4.14)$$

When the duty cycle D is small, the output impedance can be further simplified as:

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} \approx [\frac{T_{on}}{2}(\frac{T_{on}}{2C_o} - R_{Co}) - \frac{(1+D^2)}{\omega_2^2 C_o}] \frac{s \cdot (R_{Co} C_o s + 1)}{(1 + \frac{s}{Q_3 \omega_2} + \frac{s^2}{\omega_2^2})} \qquad (4.15)$$

The Bode plot of the output impedance is shown in Figure 4.9. It is found that the output impedance is very low throughout a wide frequency range. This is why this control can deal with the transient response even without the outer loop compensation.
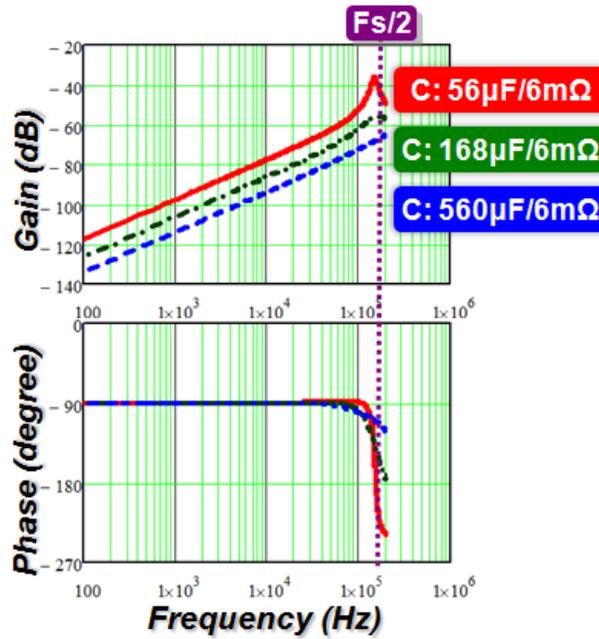
Figure 4.9. Output impedance

The SIMPLIS simulation tool is used to verify the proposed model for V^2 constant on-time control. The parameters of the buck converter are as follows: V_{in} = 12V, V_o = 1.2V, T_{on} = 0.33μs, $f_s \approx$ 300KHz, and L_s = 300nH. The control-to-output transfer function and the output impedance are plotted using the simulation results. As shown in Figure 4.10 and Figure 4.11, the proposed model can accurately predict the system response.

(a)   **(b)**
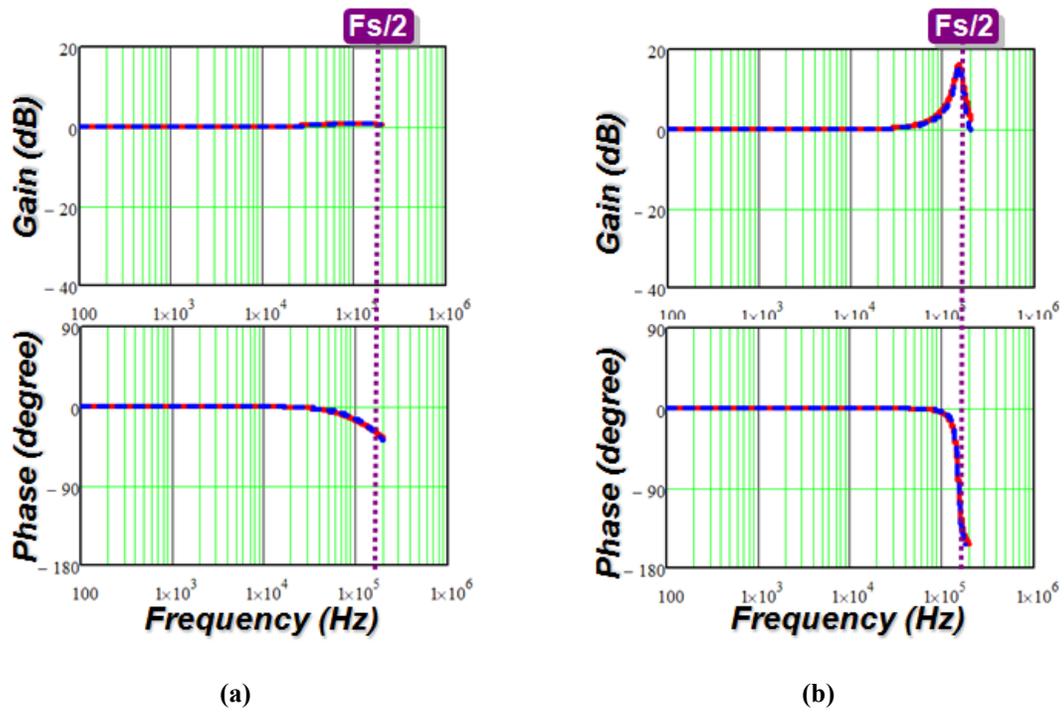
Red curve: proposed model; **Blue curve: Simplis simulation (≈ measurement)**

Figure 4.10. Control-to-output transfer function comparison: (a) output capacitor (560μF/6mΩ), and (b) output capacitor (56μF/6mΩ)

(a)   (b)
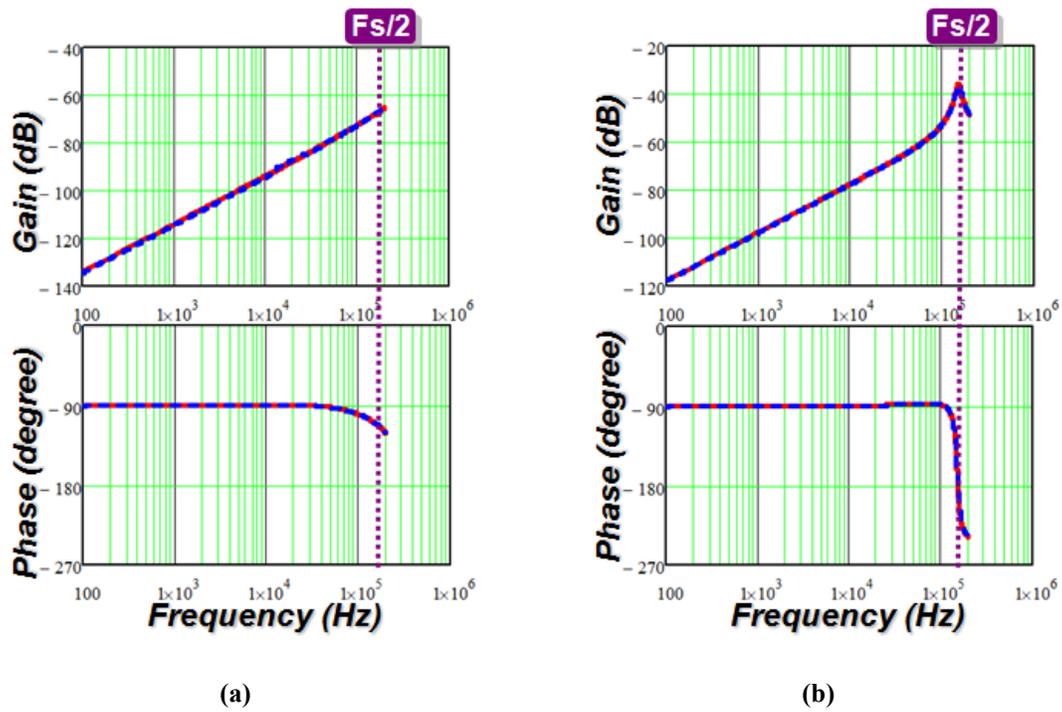
Red curve: proposed model; Blue curve: Simplis simulation (≈ measurement)
Figure 4.11. Output impedance comparison: (a) output capacitor (560µF/6mΩ), and (b) output capacitor (56µF/6mΩ)

4.3   Solutions to Eliminate Subharmonic Oscillations

In order to eliminate subharmonic oscillation due to the capacitor ripple in V^2 constant on-time control, two possible solutions are proposed: the first is adding the inductor current ramp; and the second solution is adding an external ramp.   Detailed analysis of these two approaches is presented below.

A. Solution I: Adding the inductor-current ramp

As discussed above, the capacitor voltage ripple is detrimental to the system stability, so an additional current loop can be introduced to enforce the current feedback information and reduce the influence of the capacitor voltage ripple, as shown in Figure 4.12.
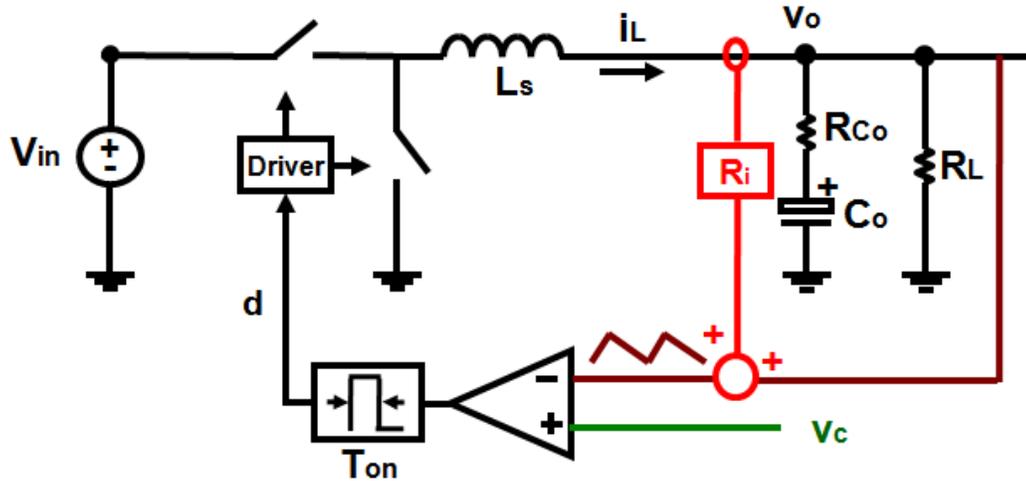
Figure 4.12. Solution I: adding the inductor-current ramp

Following the same modeling methodology, the control-to-output transfer function can be derived as (4.16) and simplified as (4.17):

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s}{s'_f} \frac{(1-e^{-sT_{on}})(1-e^{-sT_{sw}})(1+\dfrac{1}{R_LC_os})}{[1+\dfrac{T_{off}}{2C_o(R_{Co}+R_i)}]-[1-\dfrac{2T_{on}+T_{off}}{2C_o(R_{Co}+R_i)}]e^{-sT_{sw}}} \frac{V_{in}}{L_s s} \frac{R_L(R_{Co}C_o \cdot s+1)}{(R_L+R_{Co})C_o \cdot s+1} \quad (4.16)$$

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\dfrac{s}{Q_3'\omega_2}+\dfrac{s^2}{\omega_2^2})} \tag{4.17}$$

where, $s_f' = (R_{Co}+R_i) \cdot V_o / L_s$, $Q_3' = T_{sw}/\{[(R_{Co}+R_i)C_o - T_{on}/2]\pi\}$, and R_i is the sensing gain of the additional current loop. By comparing (4.11) and (4.17), we see that adding the inductor current ramp equivalently increases the ESR of the output capacitors. The sensing gain of the inductor current R_i can be used as a design parameter to eliminate subharmonic oscillation for various output capacitors.

The output impedance can also be derived as (4.18) and simplified as (4.19):

$$Z_o(s) = [\frac{f_s}{s_f'} \frac{(1-e^{-sT_{on}})(1-e^{-sT_{sw}})(R_{Co}+\dfrac{1}{C_o s})}{(1+\dfrac{T_{off}}{2C_o(R_{Co}+R_i)})-(1-\dfrac{2T_{on}+T_{off}}{2C_o(R_{Co}+R_i)})e^{-sT_{sw}}} \frac{V_{in}}{L_s s}-1] \cdot (R_{Co}+\frac{1}{C_o s}) \tag{4.18}$$

$$Z_o(s) \approx [\frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \frac{(R_{Co}C_o \cdot s+1)}{(1+\dfrac{s}{Q_3'\omega_2}+\dfrac{s^2}{\omega_2^2})}-1] \cdot (R_{Co}+\frac{1}{C_o s}) \tag{4.19}$$

Moreover, when the duty cycle is relatively small, (4.19) can be further simplified as:

$$Z_o(s) \approx R_i \cdot \frac{-\{[\dfrac{(1+D^2)}{\omega_2^2 R_i C_o}-\dfrac{T_{on}}{2R_i}(\dfrac{T_{on}}{2C_o}-R_i-R_{Co})]s+1\} \cdot (R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_3'\omega_2}+\dfrac{s^2}{\omega_2^2})} \tag{4.20}$$

An example using the ceramic capacitors is shown in Figure 4.13 and Figure 4.14. The parameters are: V_{in} = 12V, V_o = 1.2V, L_s = 300nH, T_{on} = 0.33μs, and the output capacitor consists of eight ceramic capacitors (100μF/1.4mΩ).
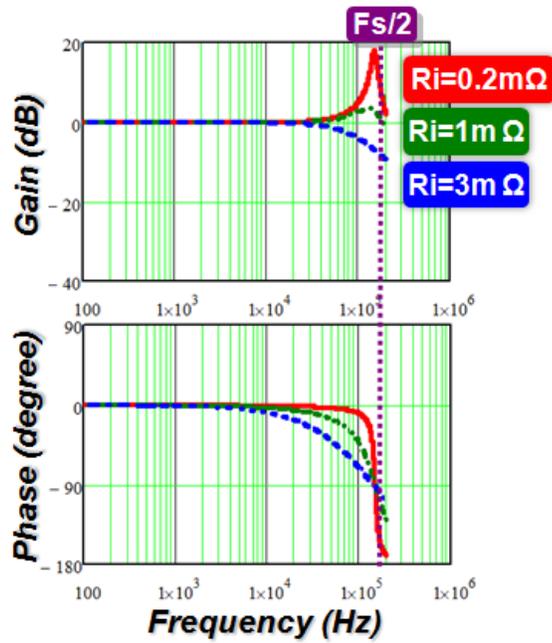
Figure 4.13. Control-to-output transfer function with different R$_i$
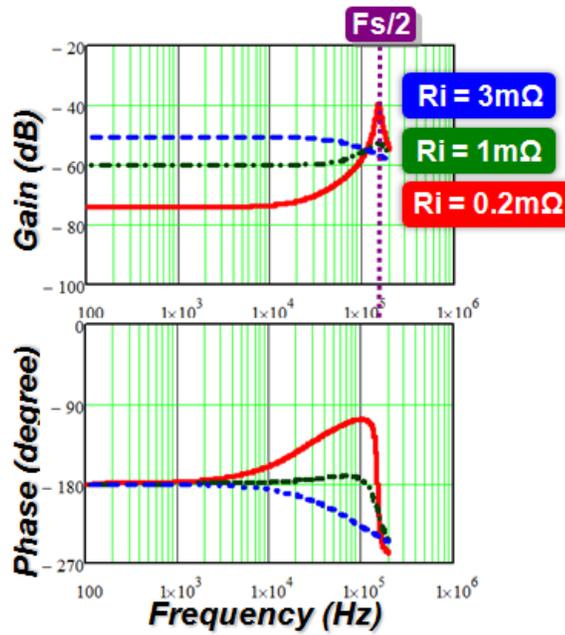
Figure 4.14. Output impedance with different R$_i$

The control-to-output transfer function and the output impedance are plotted to show the influence of the inductor-current ramp. Comparing Figure 4.9 with Figure 4.14, it is found that the output impedance stays a constant value R_i at low frequency when there is an additional current loop. In some applications, such as voltage regulators for microprocessors where constant output impedance is required, this control structure can be used to meet the design target. For other applications without such a requirement, the outer loop compensation can be used to lower the output impedance in the frequency range within the control bandwidth.

Adding the current-ramp approach to eliminate the subharmonic oscillation in V^2 constant on-time control is verified through the SIMPLIS simulation based on the similar parameters. The control-to-output transfer function and the output impedance are shown in Figure 4.15 and Figure 4.16.

(a)   (b)
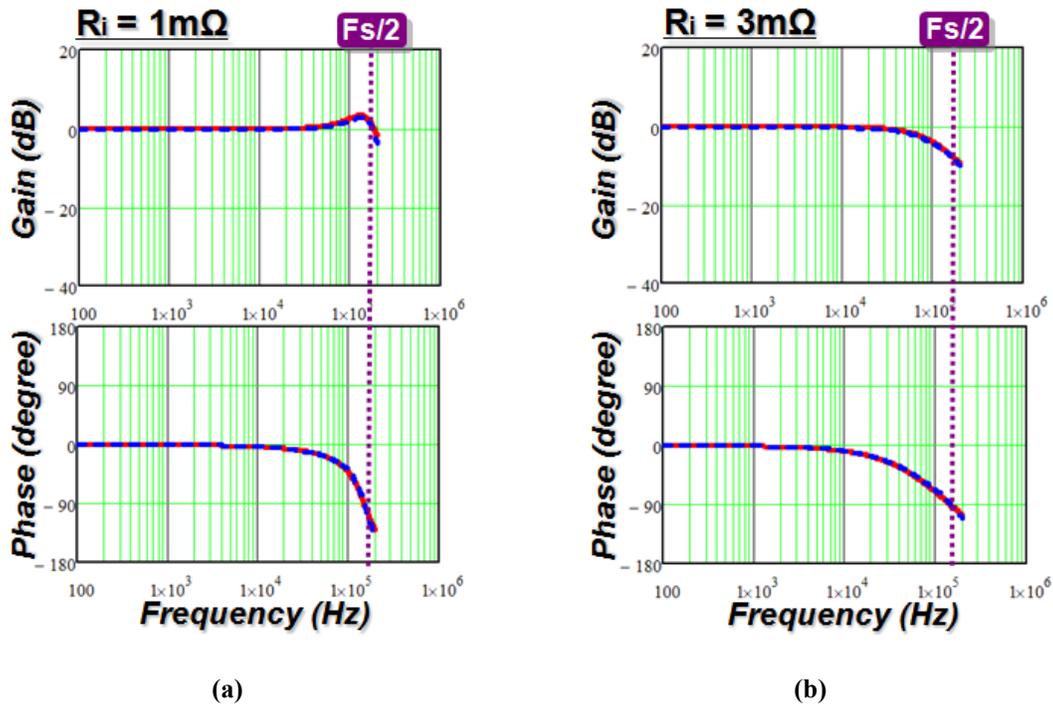
Red curve: proposed model; Blue curve: Simplis simulation (≈ measurement)
Figure 4.15. Control-to-output transfer function for Solution I (8 output capacitors:
100μF/1.4mΩ): (a) $R_i = 1mΩ$, and (b) $R_i = 3mΩ$

(a)   (b)
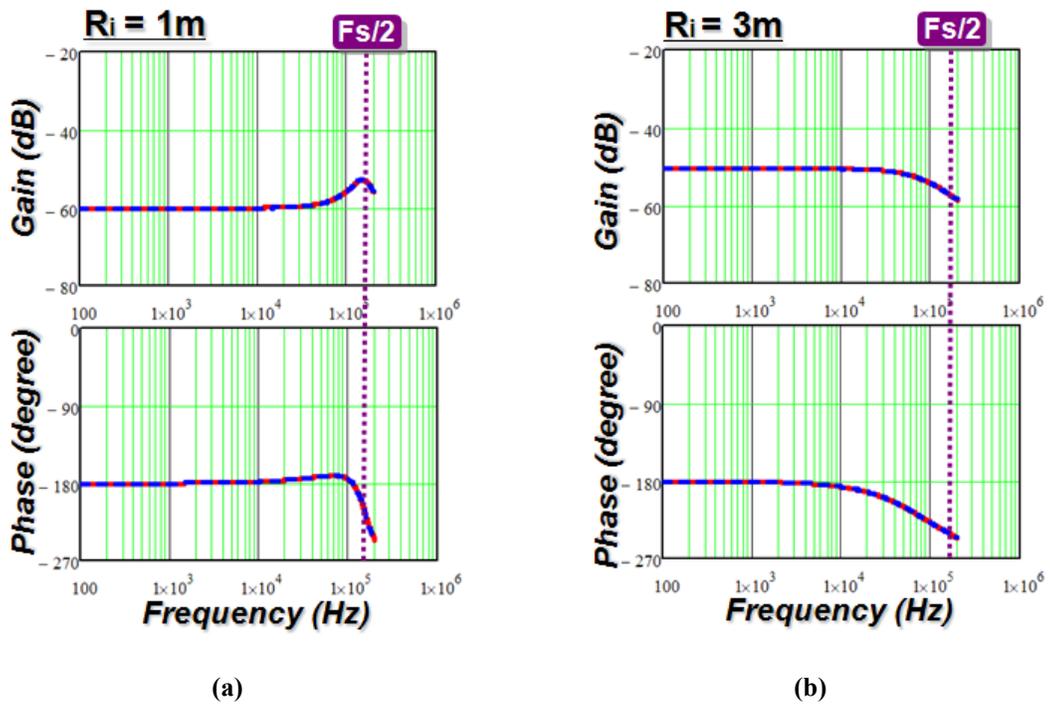
Red curve: proposed model; Blue curve: Simplis simulation (≈ measurement)
Figure 4.16. Output Impedance for Solution I (8 output capacitors: 100μF/1.4mΩ): (a) $R_i = 1m\Omega$,
and (b) $R_i = 3m\Omega$

B. Solution II: Adding the external ramp

As we know, the external ramp is used to eliminate subharmonic oscillation in peak current-mode control. A similar concept can be used in V^2 constant on-time control, as shown in Figure 4.17. The external digital ramp starts to build up at the end of the on-time period and resets at the beginning of the on-time period in every switching cycle.
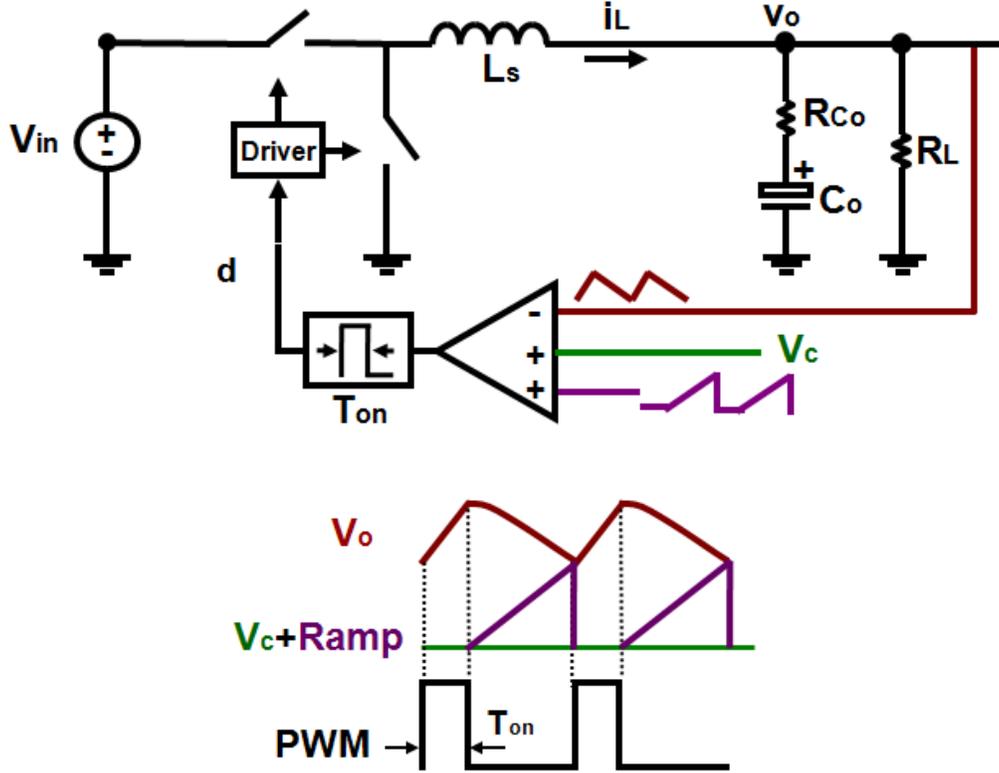
Figure 4.17. Solution II: adding the external ramp

The control-to-output transfer function can be derived as (4.21) and simplified as (4.22):

$$\frac{v_o(s)}{v_c(s)} = \frac{\dfrac{f_s}{s_e + s_f}(1 - e^{-sT_{on}})(1 - e^{-sT_{sw}})(1 + \dfrac{1}{R_L C_o s})\dfrac{V_{in}}{L_s s}\dfrac{R_L(R_{Co}C_o \cdot s + 1)}{(R_L + R_{Co})C_o \cdot s + 1}}{(1 + \dfrac{s_f}{s_e + s_f}\dfrac{T_{off}}{2C_o R_{Co}}) - (\dfrac{s_e}{s_e + s_f} + 1 - \dfrac{s_f}{s_e + s_f}\dfrac{2T_{on} + T_{off}}{2C_o R_{Co}})e^{-sT_{sw}} + \dfrac{s_e e^{-s2T_{sw}}}{s_e + s_f}} \qquad (4.21)$$

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$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_3\omega_2}+\dfrac{s^2}{\omega_2^2})(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})+\dfrac{s_e}{s_f}R_{Co}C_o T_{sw}\cdot s^2} \tag{4.22}$$

where, s_e the magnitude of the external ramp.

When the duty cycle and the external ramp are small, (4.22) can be simplified as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_4\omega_2}+\dfrac{s^2}{\omega_2^2})} \tag{4.23}$$

where, $Q_4 = T_{sw}/\{[(2s_e/s_f+1)R_{Co}C_o - T_{on}/2]\pi\}$. The Q factor is damped due to the external ramp.

The output impedance can be derived as (4.24) and simplified as (4.25) and (4.26):

$$Z_o(s) = [\frac{\dfrac{f_s}{s_e+s_f}(1-e^{-sT_{on}})(1-e^{-sT_{sw}})(R_{Co}+\dfrac{1}{C_o s})\dfrac{V_{in}}{L_s s}}{(1+\dfrac{s_f}{s_e+s_f}\dfrac{T_{off}}{2C_o R_{Co}})-(\dfrac{s_e}{s_e+s_f}+1-\dfrac{s_f}{s_e+s_f}\dfrac{2T_{on}+T_{off}}{2C_o R_{Co}})e^{-sT_{sw}}+\dfrac{s_e}{s_e+s_f}e^{-s2T_{sw}}}-1]\cdot(R_{Co}+\dfrac{1}{C_o s})$$

$$\tag{4.24}$$

$$Z_o(s) \approx [\frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_3\omega_2}+\dfrac{s^2}{\omega_2^2})(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})+\dfrac{s_e}{s_f}R_{Co}C_o T_{sw}\cdot s^2}-1]\cdot(R_{Co}+\dfrac{1}{C_o s})$$

$$\tag{4.25}$$

$$Z_o(s) \approx \frac{-[\dfrac{(1+D^2)}{\omega_2^2 C_o}+\dfrac{T_{on}}{2C_o}(R_{Co}C_o-\dfrac{T_{on}}{2})+\dfrac{s_e}{s_f}R_{Co}T_{sw}]s\cdot(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_4\omega_2}+\dfrac{s^2}{\omega_2^2})} \tag{4.26}$$

Based on the parameters used in the previous section, the control-to-output transfer function and the output impedance are plotted in Figure 4.18 and Figure 4.19 and to show the influence of the external ramp.
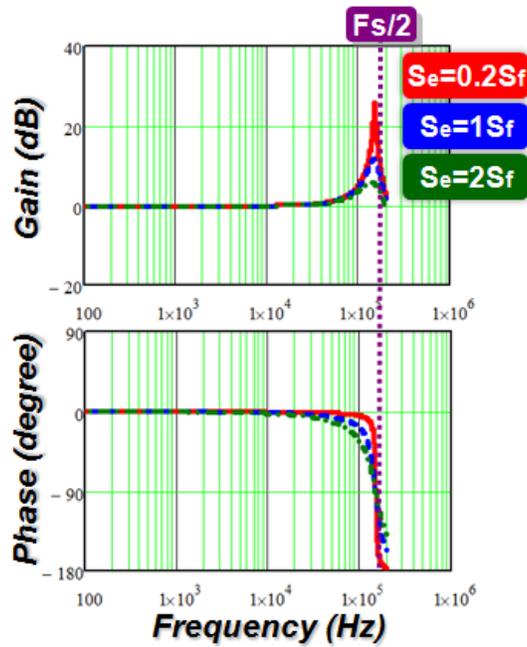
Figure 4.18. Control-to-output transfer function with different external ramps
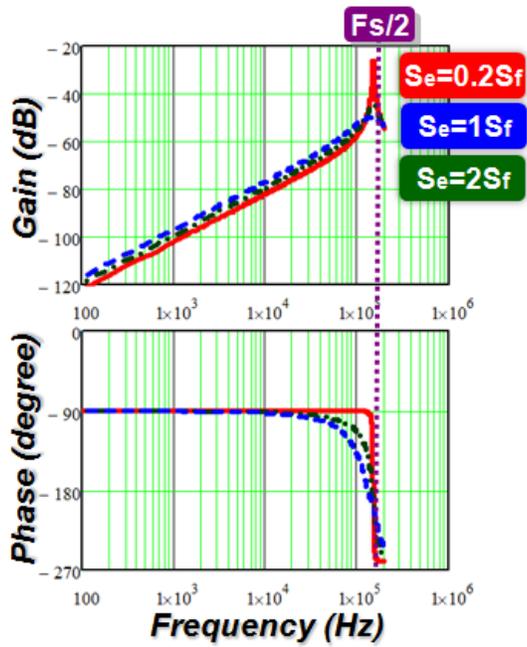
Figure 4.19. Output impedance with different external ramps

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Adding the external ramp approach to eliminate subharmonic oscillations in V^2 constant on-time control is verified through the SIMPLIS simulation based on the similar parameters. The control-to-output transfer function and the output impedance are shown in Figure 4.20 and Figure 4.21.

(a)   **(b)**
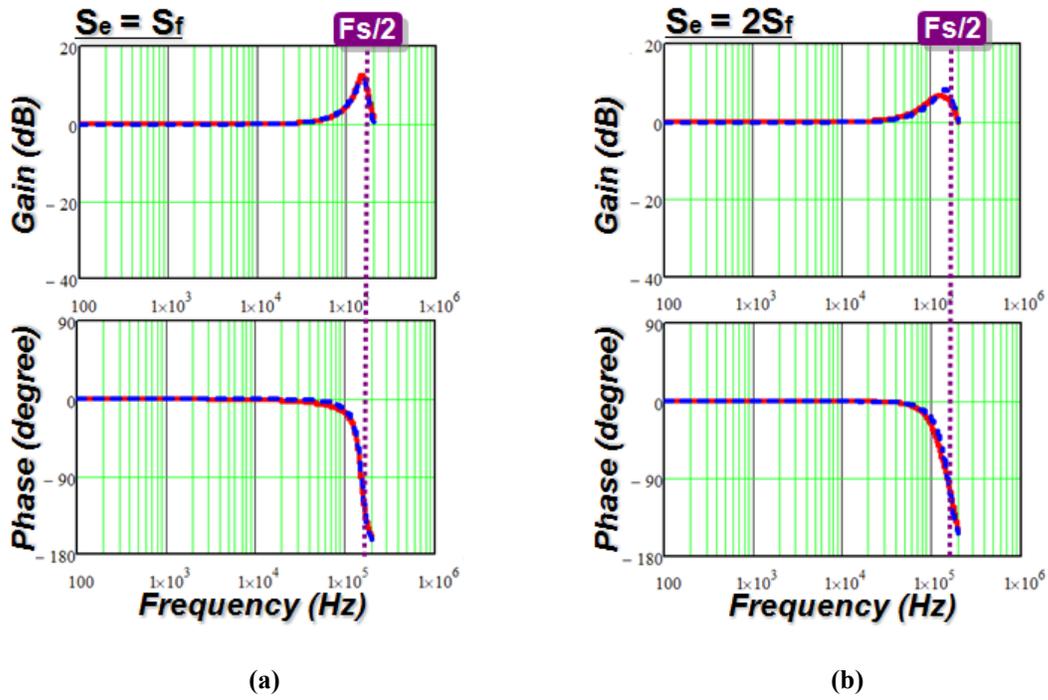
Red curve: proposed model; **Blue curve: Simplis simulation (≈ measurement)**
Figure 4.20. Control-to-output transfer function for Solution II (8 output capacitors: 100μF/1.4mΩ): (a) $s_e = s_f$, and (b) $s_e = 2s_f$

(a)   (b)
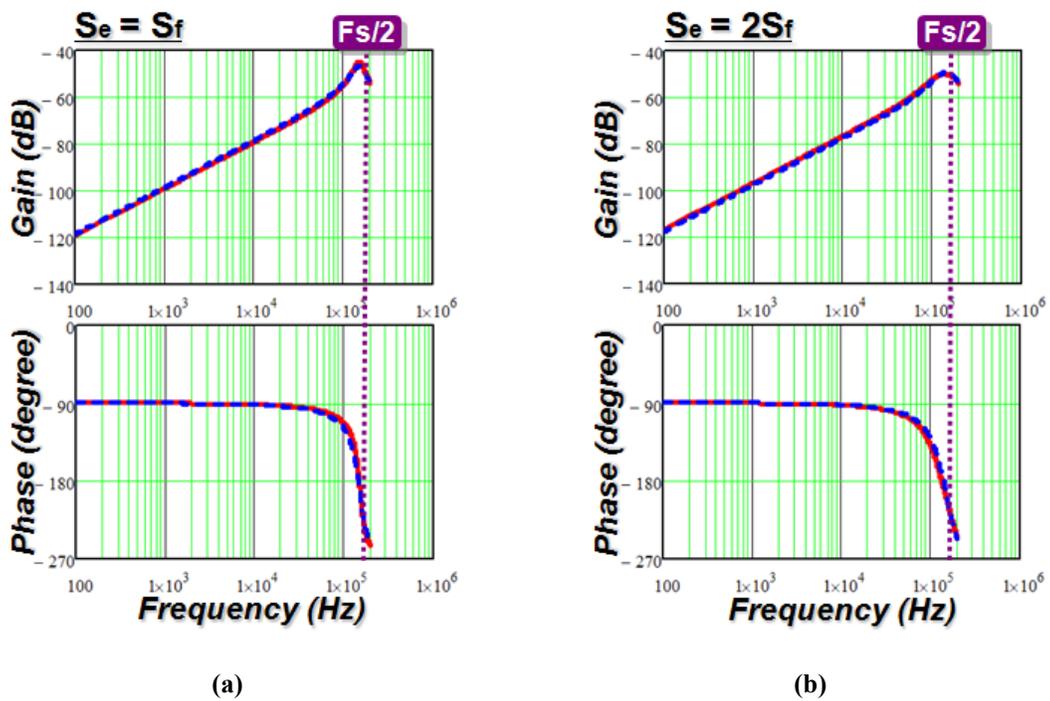
Red curve: proposed model; Blue curve: Simplis simulation (≈ measurement)
Figure 4.21. Output Impedance for Solution II (8 output capacitors: 100μF/1.4mΩ): (a) $s_e = s_f$, and
(b) $s_e = 2s_f$

To summarize, both of the approaches analyzed above can effectively eliminate subharmonic oscillations due to the capacitor ripple.

4.4   Extension to Other V^2 Current-Mode Controls

The proposed model strategy can be extend to other types of V^2 current-mode control structures, including constant off-time, constant-frequency peak voltage control, and constant-frequency valley voltage control structures.   When using constant frequency modulation, an external ramp is added to help stabilize the system.   The model results for V^2 constant off-time control are shown in Table 4.1.

Table 4.1. Extended model for V^2 constant off-time control

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s}{s_n} \frac{(1-e^{-sT_{off}})(1-e^{-sT_{sw}})(1+\frac{1}{R_L C_o s})}{(1+\frac{T_{on}}{2C_o R_{Co}}) - (1-\frac{2T_{off}+T_{on}}{2C_o R_{Co}})e^{-sT_{sw}}} \frac{V_{in}}{L_s s} \frac{R_L(R_{Co}C_o \cdot s+1)}{(R_L + R_{Co})C_o \cdot s+1}$$

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\frac{s}{Q_1 \omega_3}+\frac{s^2}{\omega_3^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\frac{s}{Q_5 \omega_2}+\frac{s^2}{\omega_2^2})}$$

$$Z_o(s) = [\frac{\frac{f_s}{s_n}(1-e^{-sT_{off}})(1-e^{-sT_{sw}})(R_{Co}+\frac{1}{C_o s})}{(1+\frac{T_{on}}{2C_o R_{Co}}) - (1-\frac{2T_{off}+T_{on}}{2C_o R_{Co}})e^{-sT_{sw}}} \frac{V_{in}}{L_s s} - 1] \cdot (R_{Co}+\frac{1}{C_o s})$$

$$Z_o(s) \approx [\frac{1}{(1+\frac{s}{Q_1 \omega_3}+\frac{s^2}{\omega_3^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\frac{s}{Q_5 \omega_2}+\frac{s^2}{\omega_2^2})} - 1] \cdot (R_{Co}+\frac{1}{C_o s})$$

$$\omega_3 = \pi/T_{off} \qquad Q_5 = T_{sw}/[(R_{Co}C_o - \frac{1}{2}T_{off})\pi]$$

The model results for peak voltage control are shown in Table 4.2.

Table 4.2. Extended model for peak voltage control

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})(1-e^{-sT_{sw}})(1+\frac{1}{s \cdot R_L C_o})\frac{V_{in}}{L_s s}\frac{R_L(R_{Co}C_o \cdot s + 1)}{(R_L + R_{Co})C_o \cdot s + 1}}{(s_n + s_e + \frac{s_n T_{on}}{2R_{Co}C_o}) + (-s_n + s_f - 2s_e + \frac{s_n T_{sw} + s_f T_{on}}{R_{Co}C_o})e^{-sT_{sw}} + (-s_f + s_e + \frac{s_f T_{off}}{2R_{Co}C_o})e^{-2sT_{sw}}}$$

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s + 1)}{(1+\frac{s}{Q_6 \omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_1 \omega_2}+\frac{s^2}{\omega_2^2}) - \frac{(s_f - s_e)R_{Co}C_o - s_f T_{off}/2}{s_n + s_f}T_{sw} \cdot s^2}$$

$$Z_o(s) = [\frac{f_s(1-e^{-sT_{sw}})(1-e^{-sT_{sw}})(R_{Co}+\frac{1}{C_o s})\frac{V_{in}}{L_s s}}{(s_n + s_e + \frac{s_n T_{on}}{2R_{Co}C_o}) + (-s_n + s_f - 2s_e + \frac{s_n T_{sw} + s_f T_{on}}{R_{Co}C_o})e^{-sT_{sw}} + (-s_f + s_e + \frac{s_f T_{off}}{2R_{Co}C_o})e^{-2sT_{sw}}} - 1]$$

$$\cdot (R_{Co}+\frac{1}{C_o s})$$

$$Z_o(s) \approx [\frac{(R_{Co}C_o s + 1)}{(1+\frac{s}{Q_6 \omega_2}+\frac{s^2}{\omega_2^2})(1+\frac{s}{Q_1 \omega_2}+\frac{s^2}{\omega_2^2}) - \frac{(s_f - s_e)R_{Co}C_o - s_f T_{off}/2}{s_n + s_f}T_{sw} \cdot s^2} - 1] \cdot (R_{Co}+\frac{1}{C_o s})$$

$$Q_6 = 1/[(\frac{1}{2}+\frac{R_{Co}C_o - T_{sw}}{T_{sw}s_n/(s_n + s_f)+T_{on}})\pi]$$

The model results for valley voltage control are shown in Table 4.3.

Table 4.3. Extended model for valley voltage control

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})(1-e^{-sT_{sw}})(1+\dfrac{1}{s \cdot R_L C_o})\dfrac{V_{in}}{L_s s}\dfrac{R_L(R_{Co}C_o \cdot s+1)}{(R_L+R_{Co})C_o \cdot s+1}}{(s_f+s_e+\dfrac{s_f T_{off}}{2R_{Co}C_o})+(-s_f+s_n-2s_e+\dfrac{s_f T_{sw}+s_n T_{off}}{R_{Co}C_o})e^{-sT_{sw}}+(-s_n+s_e+\dfrac{s_n T_{on}}{2R_{Co}C_o})e^{-2sT_{sw}}}$$

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_7\omega_2}+\dfrac{s^2}{\omega_2^2})(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})-\dfrac{(s_n-s_e)R_{Co}C_o-s_n T_{on}/2}{s_n+s_f}T_{sw}\cdot s^2}$$

$$Z_o(s) = [\frac{f_s(1-e^{-sT_{sw}})(1-e^{-sT_{sw}})(R_{Co}+\dfrac{1}{C_o s})\dfrac{V_{in}}{L_s s}}{(s_f+s_e+\dfrac{s_f T_{off}}{2R_{Co}C_o})+(-s_f+s_n-2s_e+\dfrac{s_f T_{sw}+s_n T_{off}}{R_{Co}C_o})e^{-sT_{sw}}+(-s_n+s_e+\dfrac{s_n T_{on}}{2R_{Co}C_o})e^{-2sT_{sw}}}-1]$$

$$\cdot (R_{Co}+\frac{1}{C_o s})$$

$$Z_o(s) \approx [\frac{(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_7\omega_2}+\dfrac{s^2}{\omega_2^2})(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})-\dfrac{(s_n-s_e)R_{Co}C_o-s_n T_{on}/2}{s_n+s_f}T_{sw}\cdot s^2}-1]\cdot(R_{Co}+\frac{1}{C_o s})$$

$$Q_7 = 1/[(\frac{1}{2}+\frac{R_{Co}C_o-T_{sw}}{T_{sw}s_f/(s_n+s_f)+T_{off}})\pi]$$

Peak voltage control is used as example for further illustration. The parameters are: input voltage V_{in} = 12V, switching frequency f_s = 300KHz, and external ramp s_e = 0. The control-to-output transfer function is plotted based on different duty cycles and different capacitor parameters, as shown in Figure 4.22 and Figure 4.23. One common characteristic of peak voltage control and peak current-mode control is that subharmonic oscillations occur when the duty cycle is larger than a critical value. The difference between these two control structures is that this critical duty cycle value is 0.5 for peak current-mode control, while this value for peak voltage control is less than 0.5 which is related to the capacitor parameters. As shown in Figure 4.23, different capacitor parameters may result in subharmonic oscillation in the peak voltage control even when D = 0.1. It is clear that subharmonic oscillations are more likely occurs when using peak voltage control due to the influence of the capacitor ripple.

Based on the duality principle, the properties of constant off-time control and valley voltage control can be easily found based on the previous analysis on constant on-time control and peak voltage control.
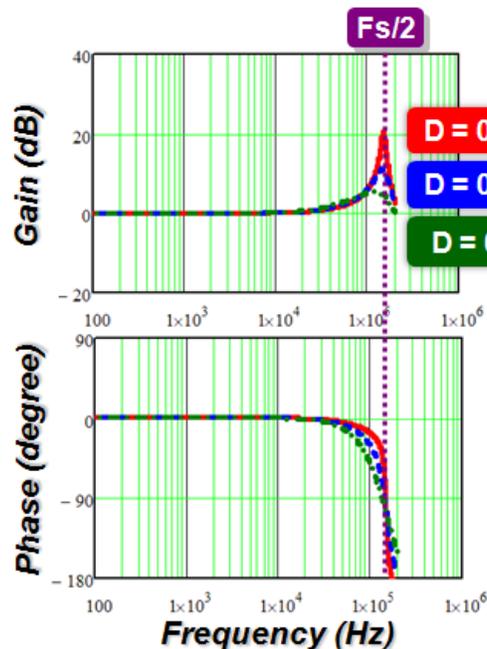
Figure 4.22. Control-to-output transfer function with different duty cycles: capacitor (560μF/6mΩ)

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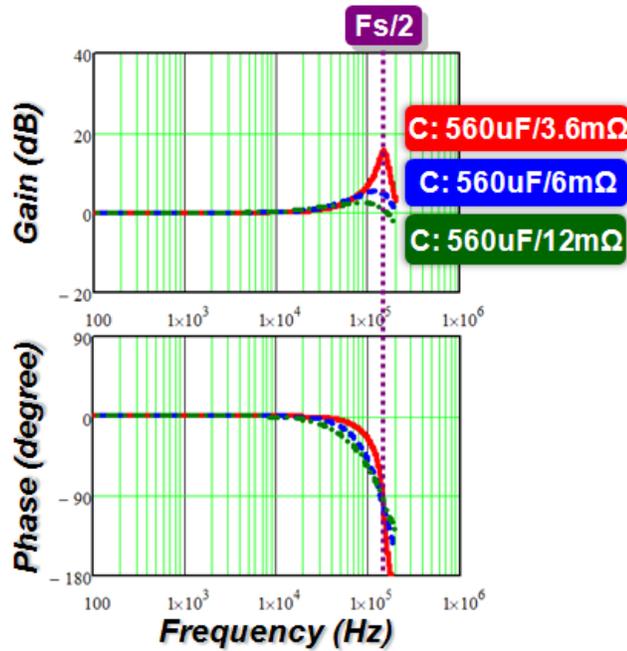
Figure 4.23. Control-to-output transfer function with different capacitor parameters: D = 0.1

4.5 Multi-phase Model for V^2 Current-Mode Control

As mentioned before, multi-phase topology is widely used to improve the transient response, and distribute power and heat for better thermal performance. The model for the multi-phase converters can be obtained from the extension of the single-phase converter model. V^2 constant on-time control is used as an example to illustrate how to derive the multi-phase model.

A multi-phase buck converter with the V^2 constant on-time control is shown in Figure 4.24. The total output voltage ripple information is fed back to the modulator, and the on-time pulse is distributed to each phase. Interleaving can be achieved automatically. Generally speaking, this implementation can be used to the case of no duty cycle overlapping. Based on the previous analysis in Chapter 2, the multi-phase buck converter is equivalent to a single-phase buck converter, as shown in Figure 4.25. The switching frequency is n times of original f_s. The output voltage is n times of original V_o.
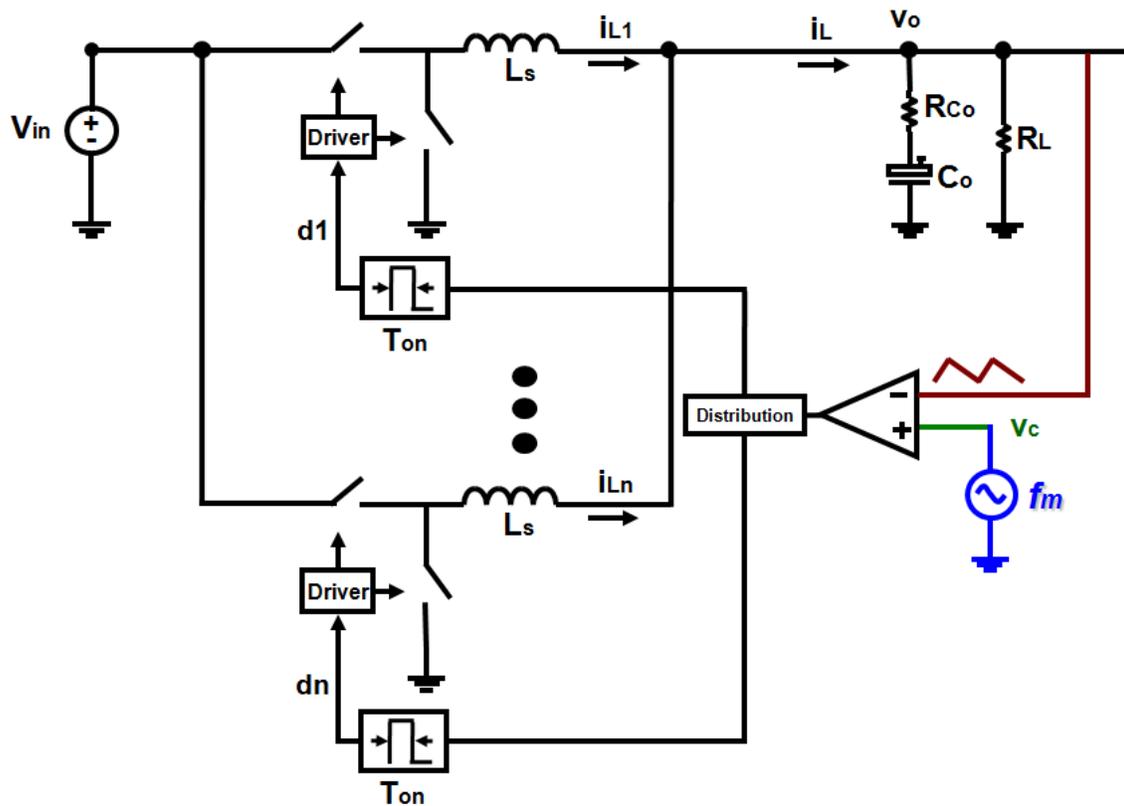
Figure 4.24. A multi-phase buck converter with V² constant on-time control
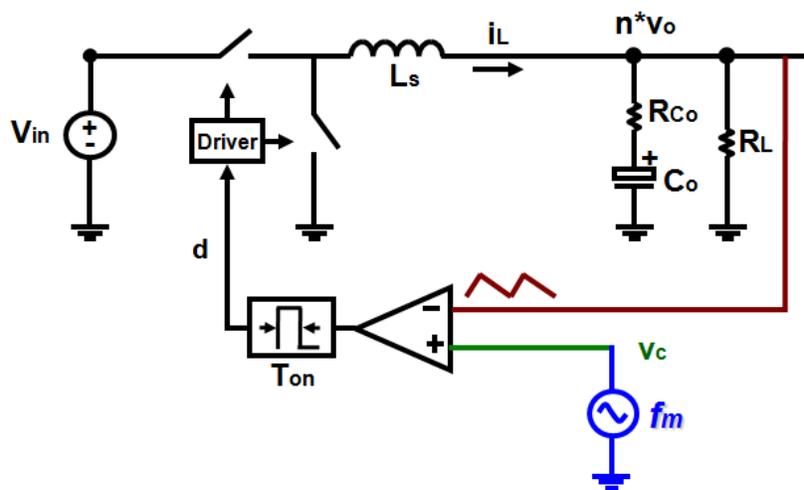
Figure 4.25. Equivalent single-phase buck converter

Therefore, the control-to-output transfer function and the output impedance can be derived as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\dfrac{s}{(\dfrac{Q_3}{n})(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})} \qquad (4.27)$$

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} \approx [\frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\dfrac{s}{(\dfrac{Q_3}{n})(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})} - 1] \cdot (R_{Co}+\frac{1}{C_o s}) \qquad (4.28)$$

Based on the control-to-output transfer function, it is found that the position of the high frequency double poles is located as half of the equivalent switching frequency. And the critical condition for stability keeps the same. Following the same methodology, the multi-phase models for the cases with different ramps can be easily obtained. Figure 4.26 shows the validity of the extended model.
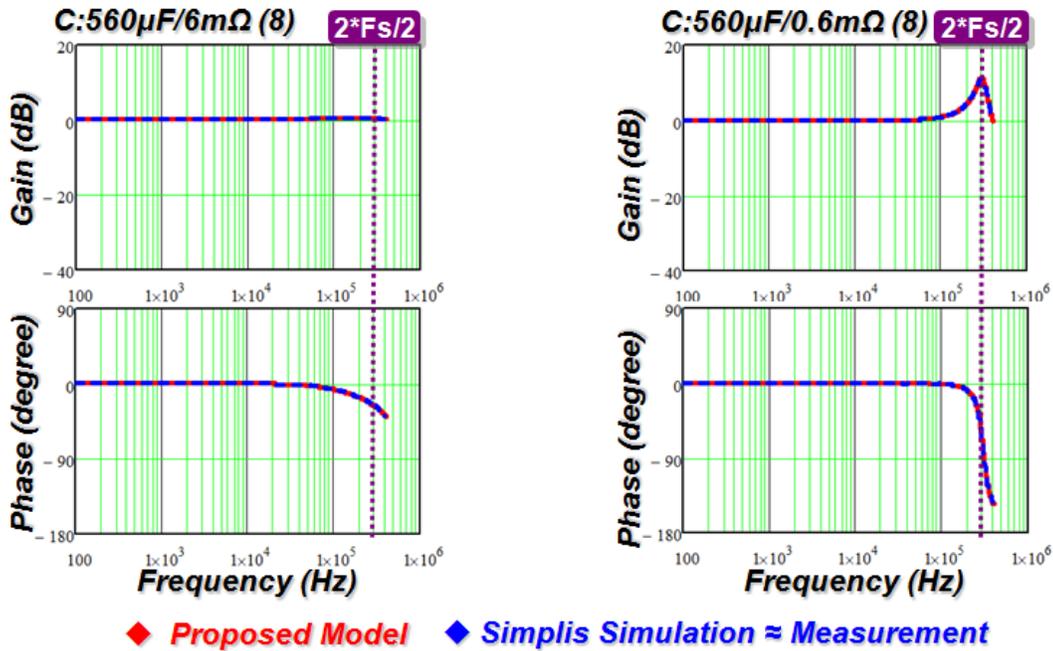
Figure 4.26. Control-to-output transfer function comparison for multi-phase buck converters with V² constant on-time control

Following the same methodology, the control-to-output transfer function and the output impedance in the case of with the inductor-current ramp can be derived as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\dfrac{s}{(\dfrac{Q_3'}{n})(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})} \tag{4.29}$$

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} \approx \left[\frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(R_{Co}C_o \cdot s+1)}{(1+\dfrac{s}{(\dfrac{Q_3'}{n})(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})} -1\right] \cdot (R_{Co}+\frac{1}{C_o s}) \tag{4.30}$$

The control-to-output transfer function and the output impedance in the case of with the external ramp can be derived as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(1+\dfrac{s}{\dfrac{Q_1}{n}(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})(R_{Co}C_o s+1)}{(1+\dfrac{s}{\dfrac{Q_3}{n}(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})(1+\dfrac{s}{\dfrac{Q_1}{n}(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})+\dfrac{s_e}{s_f}R_{Co}C_o\dfrac{T_{sw}}{n}\cdot s^2}$$

$$\tag{4.31}$$

$$Z_o(s) \approx \left[\frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(1+\dfrac{s}{\dfrac{Q_1}{n}(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})(R_{Co}C_o s+1)}{(1+\dfrac{s}{\dfrac{Q_3}{n}(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})(1+\dfrac{s}{\dfrac{Q_1}{n}(n\omega_2)}+\dfrac{s^2}{(n\omega_2)^2})+\dfrac{s_e}{s_f}R_{Co}C_o\dfrac{T_{sw}}{n}\cdot s^2} -1\right] \cdot (R_{Co}+\frac{1}{C_o s})$$

$$\tag{4.32}$$

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4.6   Experimental Verification

The experimental verification is done based on the LM34919 evaluation board from National Semiconductor.   The experiment setup is shown in Figure 4.27, and the parameters are: $V_{in} = 12V$, $V_o = 5V$, $F_s = 800kHz$, $L_s = 15\mu H$, $R_x = R_y = 2.49K\Omega$, and $R_L = 10\Omega$. Experiment verification for adding the inductor-current ramp is done based on the same evaluation board with some modifications as shown in Figure 4.28. The inductor information is sensed using sensing resistor R_i, and the feedback information is the sum of the inductor current and the output voltage.
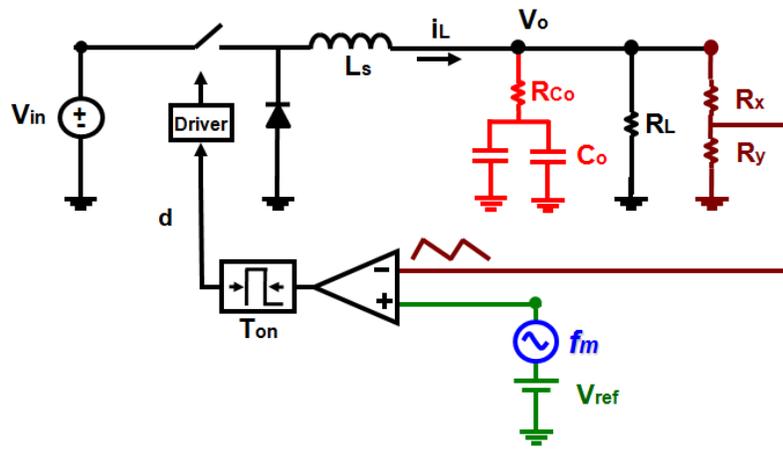
Figure 4.27. Experiment setup (1)
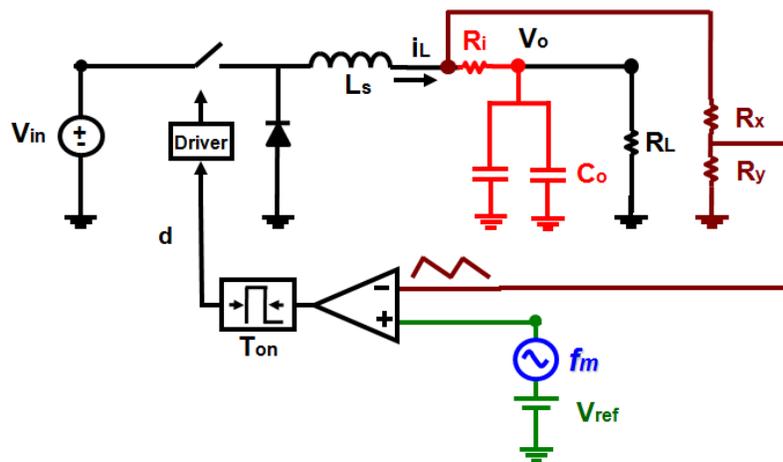
Figure 4.28. Experiment setup (2)

Experimental results with different values for C_o are shown in Figure 4.29. The proposed model can accurately predict the double pole at half of the switching frequency.

(a)

(b)
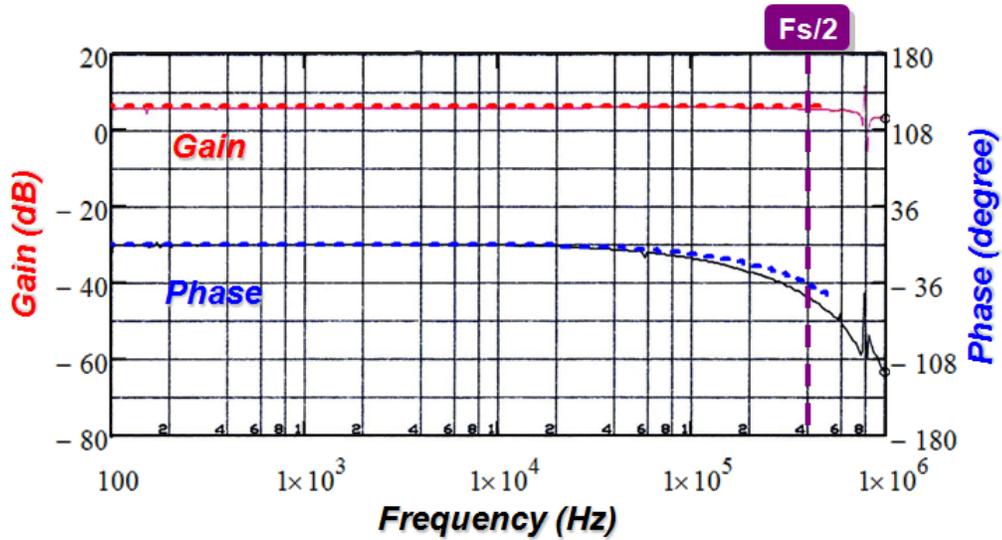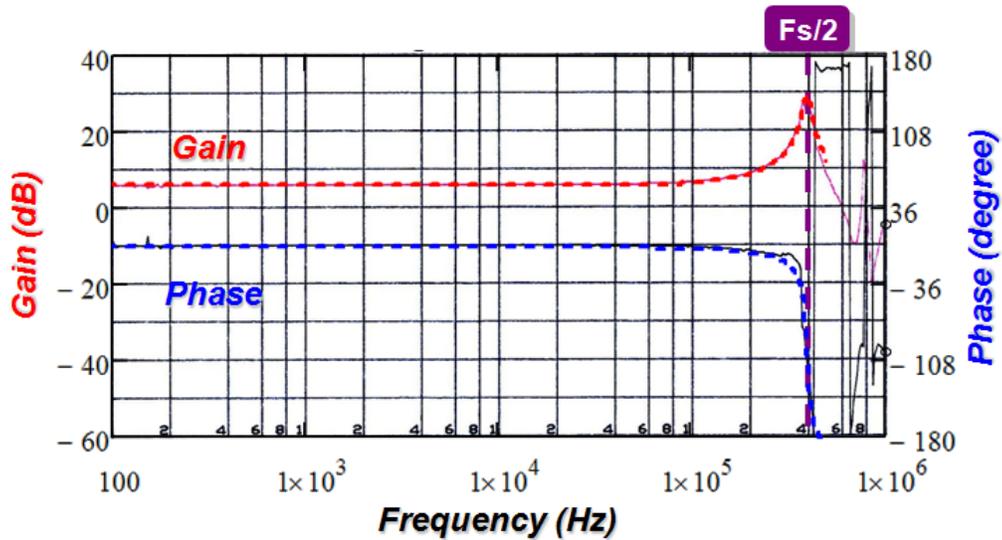
Dashed line: proposed model; Solid line: measurement
Figure 4.29. Control-to-output transfer function comparison: (a) $R_{C_o} = 0.39\Omega$, $C_o = 2\times10\mu F$, and (b) $R_{C_o} = 0.39\Omega$, $C_o = 2\times0.47\mu F$

Experiment results with different values for R_i are shown in Figure 4.30. The experiment results agree with the model results very well.

(a)

(b)
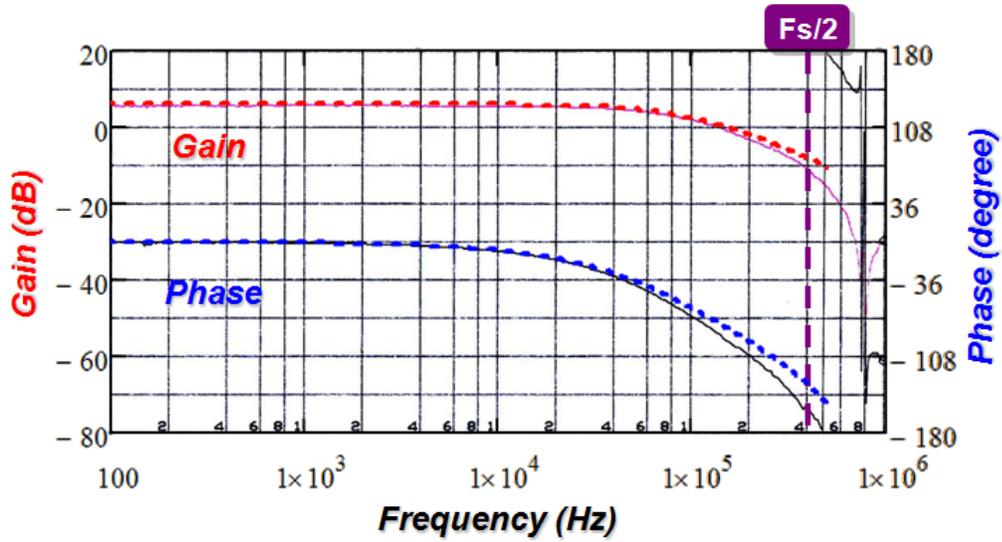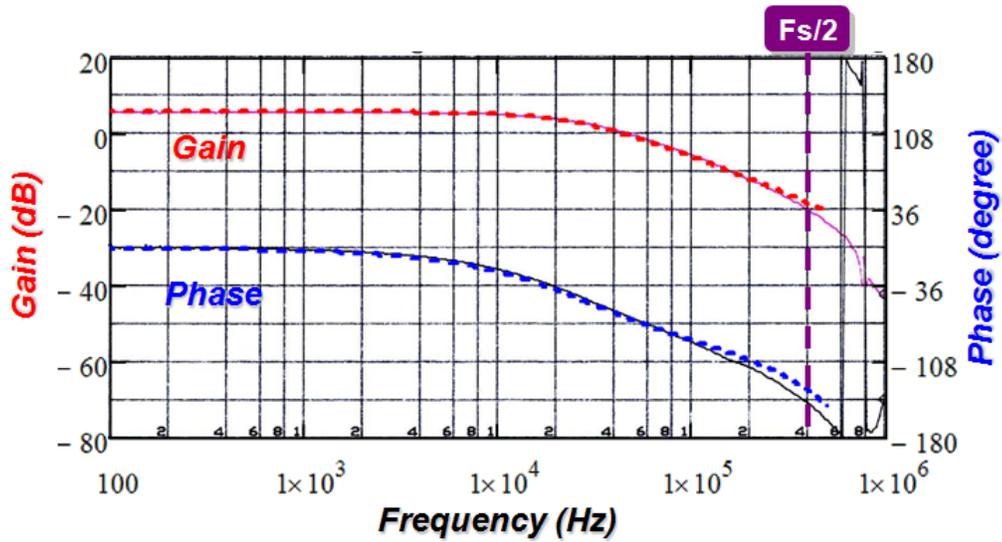
Dashed line: proposed model; Solid line: measurement
Figure 4.30. Control-to-output transfer function comparison: (a) $R_i = 0.15\Omega$, $C_o = 2 \times 10\mu F$, and (b)
$R_i = 0.39\Omega$, $C_o = 2 \times 10\mu F$

4.7 Summary

This chapter presented a new modeling approach for V^2 current-mode control. The power stage, the switches and the PWM modulator were treated as a single entity and modeled based the describing function method. The model for V^2 current-mode control achieved by the new approach can accurately predict subharmonic oscillations due to the capacitor ripple. Two solutions were discussed to solve the instability issue. Simulation and experimental results verify the proposed model.

Chapter 5. Digital Application of Current-Mode Control

High-resolution digital pulse-width modulator (DPWM) is considered to be indispensable for minimizing the possibility of unpredicted limit-cycle oscillations, but results in high cost, especially in the application of the voltage regulator (VR) for microprocessors. This chapter firstly introduces several DPWM modulation methods to improve the DPWM resolution. And then, a fully digital current-mode control architecture which can effectively limit the oscillation amplitude is presented, thereby greatly reducing the design challenge for digital controllers by eliminating the need for the high-resolution DPWM. New modeling strategy is also used to model the proposed digital current-mode control in this chapter. Simulation and experimental results are used to verify the proposed concepts.

5.1   Challenges to Digitally-Controlled DC-DC Converters

Recently, digital power supplies have become more and more popular in the field of power electronics [89]. Power supplies with a digital controller can overcome many drawbacks of those with an analog controller, and provide more functions that can improve the system performance, such as noise immunity, programmability and communication capability.

However, the design of a low-cost and high-performance digital controller is still a challenge. One of the keys to solving this issue is the selection of suitable digital control architecture. At present, the voltage-mode control architecture is widely used in the design of the digital controller [90][91] as shown in Figure 5.1. The digital voltage-mode control architecture evolved directly from its analog form. The difference between the analog structure and the digital structure is that two major quantizers, the analog-to-digital converter (ADC) and the digital pulse-width modulator (DPWM), are added into the system. Unfortunately, unpredicted limit-cycle oscillation may occur due to the quantization effects of those two quantizers [92]. Hao Peng et al. introduced a modeling method mainly for sinusoidal limit-cycle oscillation in the digital voltage-mode control

structure [93]. Based on [92] and [93], we found the high-resolution DPWM is indispensable for minimizing the possibility of the limit-cycle oscillation. However, the DPWM with high resolution is expensive and introduces more challenges to the digital controller design, especially in the application of the voltage regulator (VR) for the microprocessor.
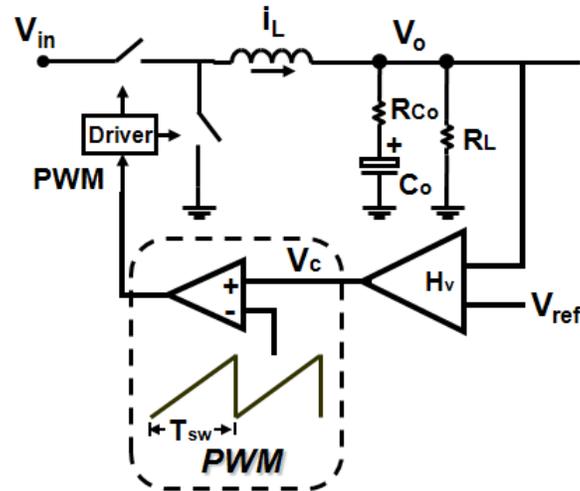
(a)
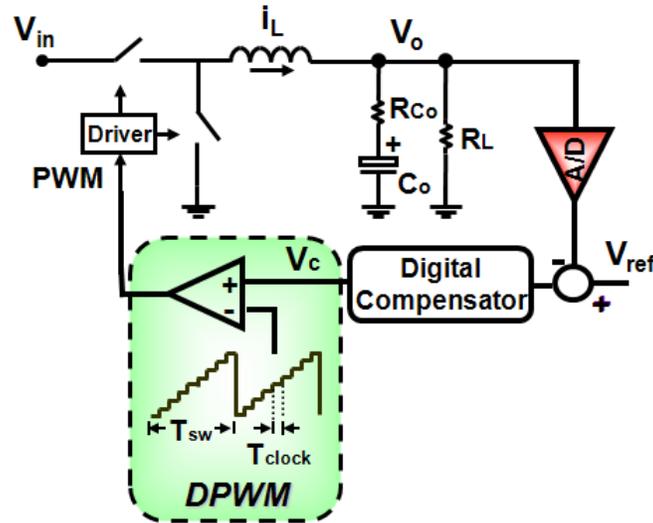
(b)

Figure 5.1. Voltage-mode control architecture: (a) the analog form, and (b) the digital form

Different DPWM implementation methods have been proposed to solve this issue [94][95][96][97][98][99][100][101][102]. The counter-based DPWM [94] is one of most common practices. In the counter-based DPWM, a counter is used to count the system clock cycle to determine the on-time and switching cycle. In this modulator, the duty cycle resolution is determined by:

$$\Delta D = f_s / f_{clock} \qquad (5.1)$$

where, f_s is the switching frequency of the power stage and f_{clock} is the system clock frequency of the controller. Taking the Buck converter as an example, the output voltage resolution ΔV_o in the continuous conduction mode (CCM) is determined by:

$$\Delta V_o = V_{in} \cdot \Delta D \qquad (5.2)$$

where, V_{in} is the input voltage.

Figure 5.2 shows the clock frequency requirement to achieve 3mV output voltage resolution under different switching frequencies in the VR application (assuming V_{in} = 12V). As shown in the graph, even for a 300-KHz switching frequency VR, the system clock frequency has to be 1.2 GHz to meet the resolution requirement. Over GHz clock frequency is not feasible for practical implementation due to the large power consumption. When the switching frequency goes higher, the situation becomes worse.
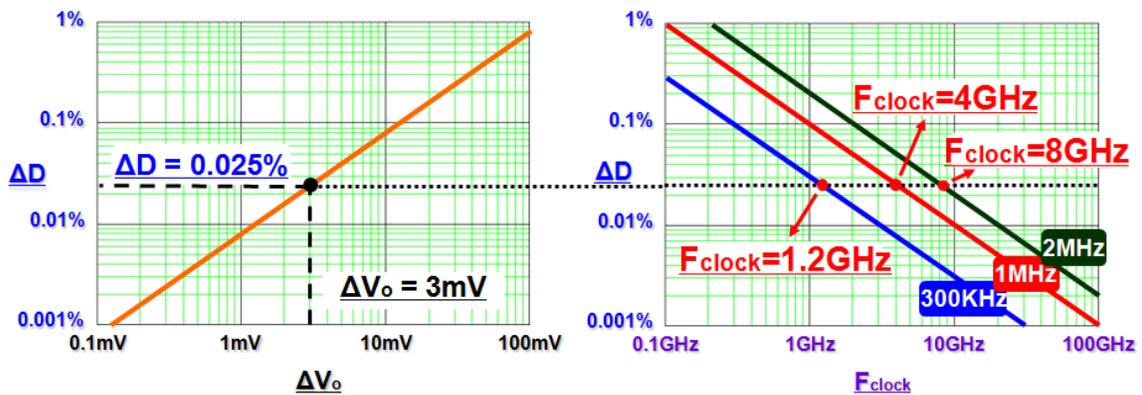
Figure 5.2. System clock frequency requirement for digital controllers with voltage-mode control

To deal with this problem, the hybrid DPWM [94]~[98] is proposed to lower the system clock frequency by adding the delay-line structure, which consists of a series of

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delay cells. A delayed clock is generated after each delay cell. This time delay t_{delay} is much shorter than the system clock cycle T_{clock}. Considering the multi-output of the delay-line, the clock frequency has been equivalently increased by n_d times with about n_d delay cells. The resolution of the hybrid DPWM, ΔD_{hybrid}, is determined by:

$$\Delta D_{hybrid} = f_s / (f_{clock} \cdot n_d) \tag{5.3}$$

Generally speaking, the hybrid DPWM is usually used in the digital controller design since the required equivalent clock frequency is too high to be achieved by the oscillator along. However, extra silicon area is required by the delay-line, which results higher cost than the counter-based DPWM. Other than those two structures, dithering technique is introduced to increase the effective resolution of the DPWM [92][99][100], but the additional voltage ripple caused by the dithered duty cycle limits the benefits of this technique. Therefore, it is worth paying more efforts on the resolution improvement of DPWM for digital controlled power converters.

5.2 Proposed High Resolution Digital Duty Cycle Modulation Schemes

A. Conventional DPWM schemes

Similar to the analog PWM modulation scheme, digital PWM has several schemes, such as trailing-edge modulation, leading-edge modulation and double-edge modulation, as shown in Figure 5.3, where v_c is the control signal.
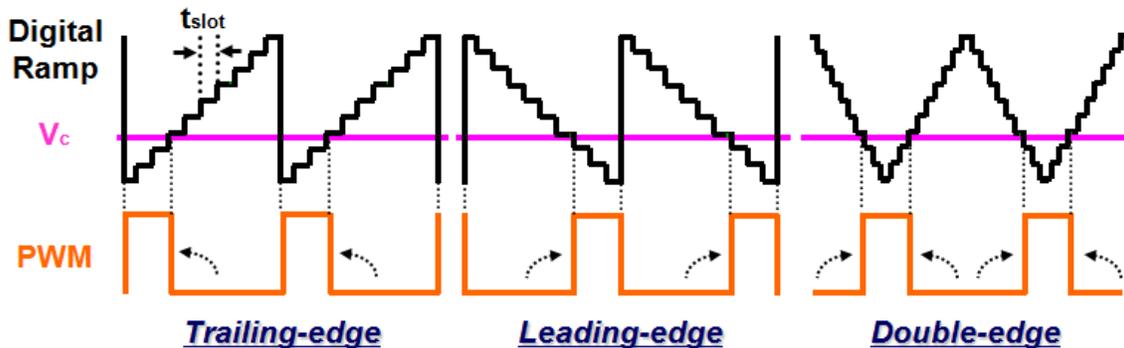
Figure 5.3. DPWM modulation schemes

The difference is that digital ramp is used in the digital PWM while the analog ramp is used in analog PWM. The digital ramp is updated every time slot (t_{slot}), which is equal to T_{clock} (in the counter-based DPWM) or t_{delay} (in the hybrid DPWM).

All of those DPWM schemes are based on constant frequency modulation. In the following analysis, the counter-based DPWM with trailing-edge modulation is used as an example. The digital duty cycle can be express as:

$$D = (m \cdot T_{clock})/(n \cdot T_{clock}) = m/n \qquad (5.4)$$

where m and n are positive numbers. Because of constant frequency modulation, n is fixed for a given switching frequency, while m is variable for different duty cycle values. The resolution can be easily calculated by:

$$\Delta D = m/n - (m-1)/n = 1/n \qquad (5.5)$$

The higher the clock frequency is, the higher the n value, which means the higher the duty cycle resolution.

B. Proposed high resolution DPWM schemes

Different modulation schemes may give different duty cycle resolution. In the following paragraphs, three different modulation schemes are investigated.

(a) Proposed method #1 (Constant on-time modulation)

Method #1 is the constant on-time modulation, as shown in Fig. 6. In the method #1, m is constant and n is variable, and the duty cycle is expressed by (5.4).
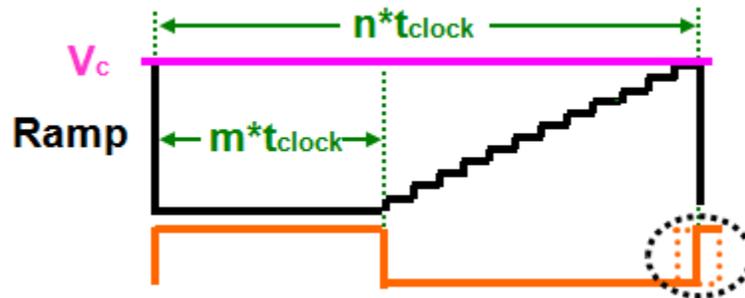
Figure 5.4. Method #1: constant on-time modulation

The duty cycle resolution is obtained as:

$$\Delta D_{\#1} = \frac{m}{n} - \frac{m}{n+1} = \frac{m}{n(n+1)} \approx D \cdot \frac{1}{n} \tag{5.6}$$

Comparing with the constant frequency modulation, the smaller the duty cycle is, the higher the resolution of the constant on-time modulation. For the VR application, the steady state duty cycle is around 0.1, which means that about 10 times improvement can be achieved by changing the modulation scheme with the same system clock frequency.

(b) Proposed method #2 (Constant off-time modulation)

When the duty cycle is small, much higher resolution can be achieved in the method #1. However, when the duty cycle is close to 1, this advantage is not so promising. In order to overcome this problem, the method #2 is proposed. Method #2 is constant off-time modulation, as shown in Figure 5.5.
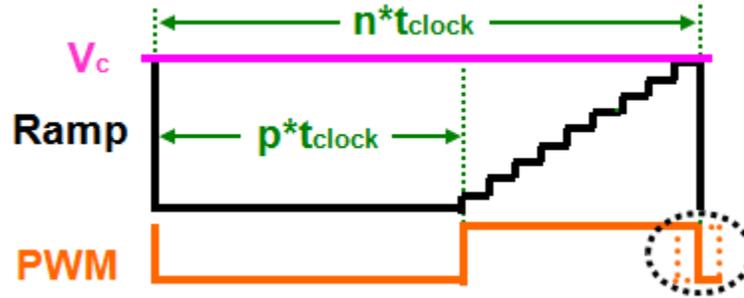
Figure 5.5. Method #2: constant off-time modulation

In the method #2, p is constant and n is variable, and the duty cycle is expressed as:

$$D = (n - p)/n \tag{5.7}$$

The duty cycle resolution is obtained by:

$$\Delta D_{\#2} = \frac{(n+1) - p}{(n+1)} - \frac{n-p}{n} = \frac{p}{n(n+1)} \approx (1-D)\frac{1}{n} \tag{5.8}$$

Assuming f_{clock}= 150 MHz, f_s = 300 KHz, duty cycle resolution comparison is shown in Figure 5.6. Comparing with the constant on-time modulation, constant off-time

modulation can achieve higher resolution when the duty cycle is close to 1. Method #1 and #2 are complementary with each other.
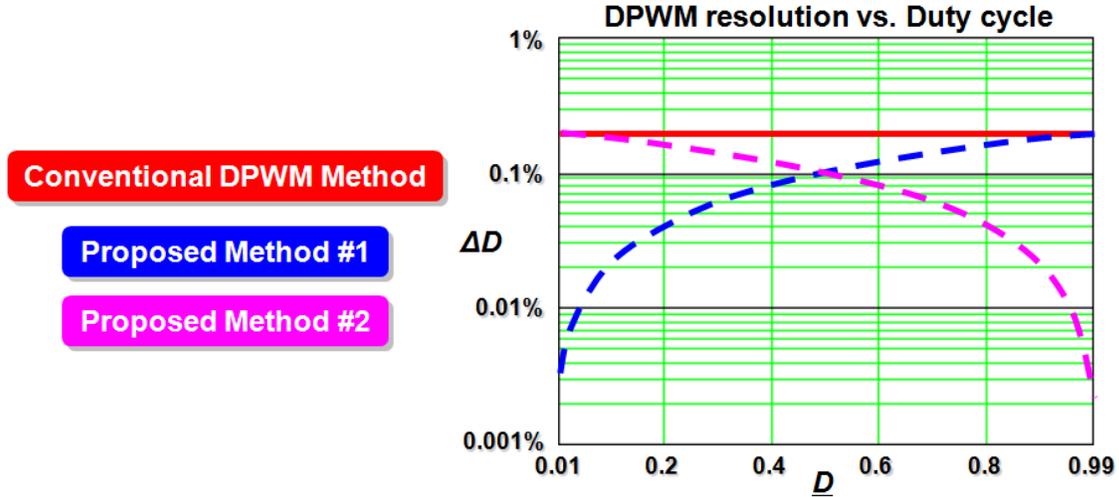
Figure 5.6. Duty cycle resolution comparison

(c) Proposed method #3 (Nearly constant frequency modulation)

One concern about constant on-time and constant off-time modulation is the switching frequency variation. For different duty cycle value, the switching frequency is different. This situation is severer in the laptop VR application, where the input voltage varies from 9V to 19V. In order to overcome the drawback of variable switching frequency, Method #3 is proposed. Assuming the duty cycle is small, comparing (5.5) with (5.6), it is found that changing m results in larger variation of duty cycle, while changing n results in achieve smaller variation. Therefore, the method #3 is proposed based on the combination of constant frequency modulation and constant on-time modulation. In this method, the duty cycle is expressed by (5.4), and m & n are both variable: changing m for coarse regulation; changing n for fine regulation. Because there is only a small variation on variable n, the switching frequency is almost constant for different duty cycle value. An example with $D = 0.2$ is shown in Figure 5.7.

V_o

$V_{in}*D_q$

$V_{in}*D_{q-1}$

D_k

D_q D_{q-1}

Coarse regulation (m is variable)					$\dfrac{m}{n}$				$\dfrac{m+1}{n}$	
Fine regulation (n is variable)	$\dfrac{m}{n+2}$	$\dfrac{m}{n+1}$		$\dfrac{m}{n-1}$	$\dfrac{m}{n-2}$	$\dfrac{m+1}{n+2}$	$\dfrac{m+1}{n+1}$		$\dfrac{m+1}{n-1}$	$\dfrac{m+1}{n-2}$
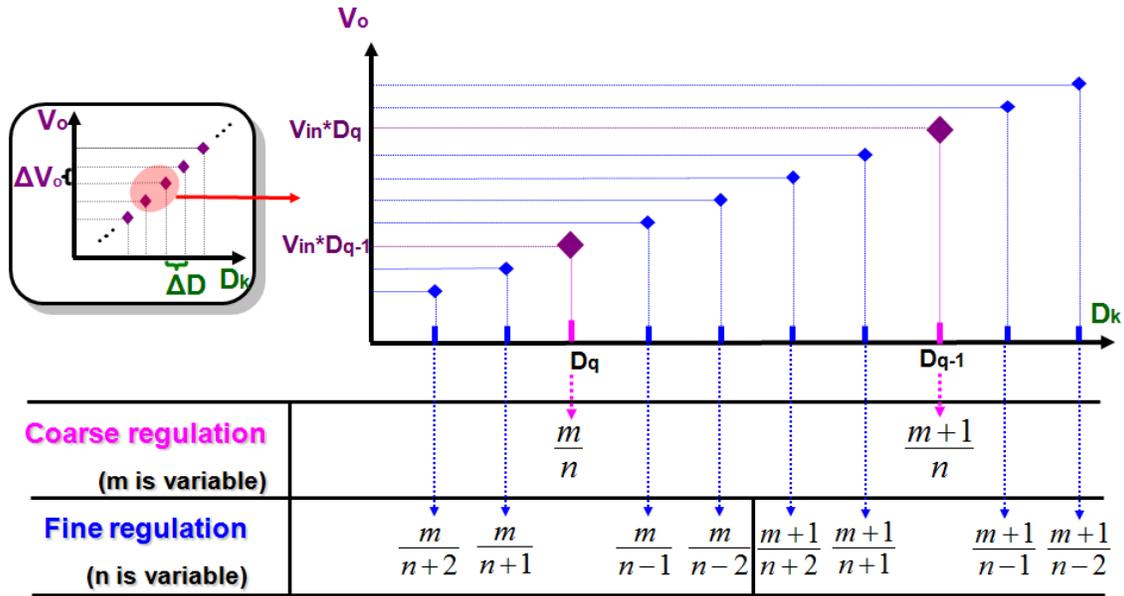
Figure 5.7. Method #3 (D = 0.2)

Figure 5.7 shows the relationship between the output voltage V_o and the duty cycle. D_q and D_{q+1} are two adjacent values achieved by coarse regulation, where m is variable. Therefore $D_q = m/n$, $D_{q+1} = (m+1)/n$. According to (5.6), the resolution can be increased about 5 times by changing n, since the duty cycle is about 0.2. Therefore, fine regulation is achieved as shown in Figure 5.7. The variation of n is only 5, which guarantees the smallest switching frequency variation. For different duty cycle values, the variation of n is different. Similarly, when duty cycle is close to 1, the method #3 is based on the combination of constant frequency modulation and constant off-time modulation.

C. The benefits of proposed schemes

Proposed modulation methods can greatly reduce the design challenge of the DPWM, especially for the VR application. Assuming D is about 0.1, for the counter-based DPWM, the duty cycle resolution can be increased about 10 times based on the same system clock frequency; for the hybrid DPWM, due to 10 times higher resolution, delay cells can be reduced from the cost point view: with the same resolution, about 90% delay cell reduction can be achieved, which means significant cost reduction.

D. Additional benefits in DCM operation

Continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are two basic operation modes for power supplies. This section investigates additional benefits of the proposed method #3 in DCM operation. For the Buck converter, V_o can be expressed by:

$$V_o = \begin{cases} V_{in} \cdot D & CCM \\ 2V_{in} \cdot (1 + \sqrt{1 + \dfrac{8L_s I_o}{V_o} \cdot \dfrac{f_s}{D^2}})^{-1} & DCM \end{cases} \tag{5.9}$$

where I_o is the load current, L_s is the power stage inductor. And the duty cycle can be expressed by:

$$D = \begin{cases} \dfrac{V_o}{V_{in}}, & CCM \\ \sqrt{\dfrac{2L_s f_s I_o}{V_{in} V_o}} \cdot \dfrac{V_o}{\sqrt{V_{in} - V_o}}, & DCM \end{cases} \tag{5.10}$$

The duty cycle becomes smaller when load decreases at DCM operation. Assuming f_s = 300KHz, V_{in} = 12V, V_o=1.2V, f_{clcok} = 150MHz, L_s = 600nH, Figure 5.8 shows the duty cycle resolution comparison between the constant frequency modulation and proposed modulation method #3.

The relationship between output voltage resolution (ΔV_o) and duty cycle resolution (ΔD) is expressed by:

$$\Delta V_o = \Delta D \cdot \partial V_o / \partial D_{D=D_{ss}} \tag{5.11}$$

where D_{ss} is the steady state duty cycle. Based on (5.9), it can be obtained as:

$$\frac{\partial V_o}{\partial D} = \begin{cases} V_{in} & CCM \\ \sqrt{\dfrac{2V_o}{L_s I_o F_{sw}}} \cdot \dfrac{(1 - V_o / V_{in})^{3/2}}{V_o / V_{in} \cdot (2 - V_o / V_{in})} V_o & DCM \end{cases} \tag{5.12}$$

According to (5.9)~(5.12), ΔV_o can be calculated and shown in Figure 5.9. Proposed method #3 can achieve identical and much finer ΔV_o in both CCM and DCM, which is very promising for digital control system design.
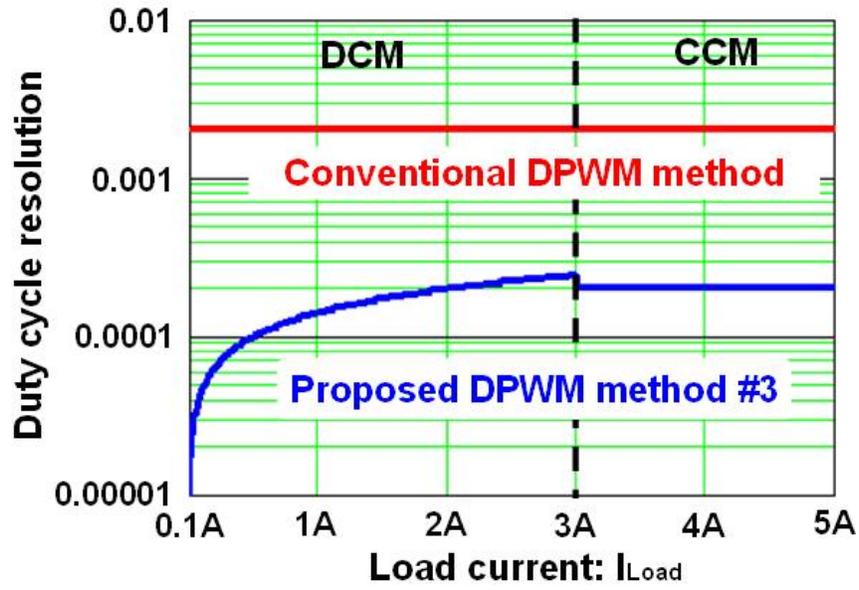
Figure 5.8. Duty cycle resolution comparison at CCM and DCM
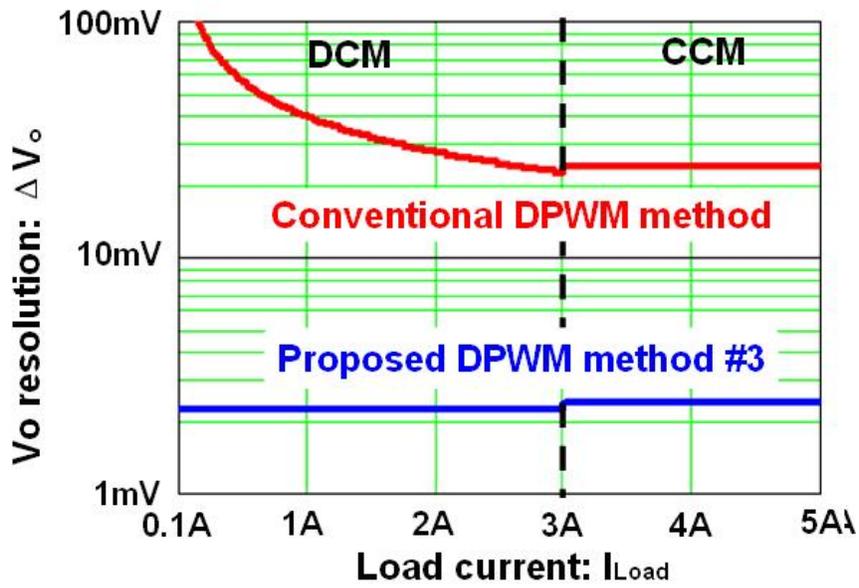
Figure 5.9. Output voltage resolution comparison at CCM and DCM

5.3 Proposed Digital Current-Mode Control Architecture Eliminating the Need for High Resolution DPWM

The high-resolution DPWM does not change the nonlinearity of the quantizers, and so it cannot completely eliminate the unpredicted limit-cycle oscillation. Once the limit-cycle oscillation occurs, which is not necessarily the sinusoidal type as shown in Figure 5.10, it is very hard to predict the oscillation amplitude and frequency in the digital voltage-mode control architecture.
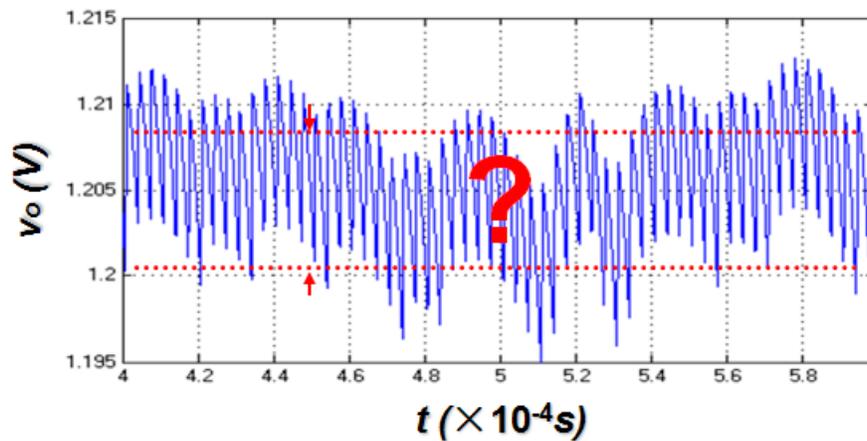
Figure 5.10. Unpredicted limit-cycle oscillation

Current-mode control provides more opportunities for the digital implementation [103][104][105][106]. In current-mode control, the equivalent series resistor (ESR) of the output capacitor can be used as the sensing resistor, so that the output voltage ripple, which includes the current information, can be directly used as the ramp for the duty cycle modulation. Later, the control structure can be implemented with an additional compensation loop, which is called V^2 current-mode control, as introduced in the previous chapters.

Based on the different modulation schemes, these two architectures consist of constant-frequency peak voltage control, constant-frequency valley voltage control, V^2 constant on-time control, V^2 constant off-time control and hysteretic control. The common characteristic of these control structures is that the instantaneous output voltage is limited by the control signal v_c, which provides an opportunity for limiting the limit-cycle

oscillations in their digital forms. Among all those control structures, constant on-time control is the most widely used to improve the light-load efficiency, since the switching frequency can be lowered to reduce switching-related loss. Therefore, constant on-time control is used for further illustration.

Direct digitization is taken by using the ADC to sample the output voltage v_o, including the ripple information, as shown in Figure 5.11.
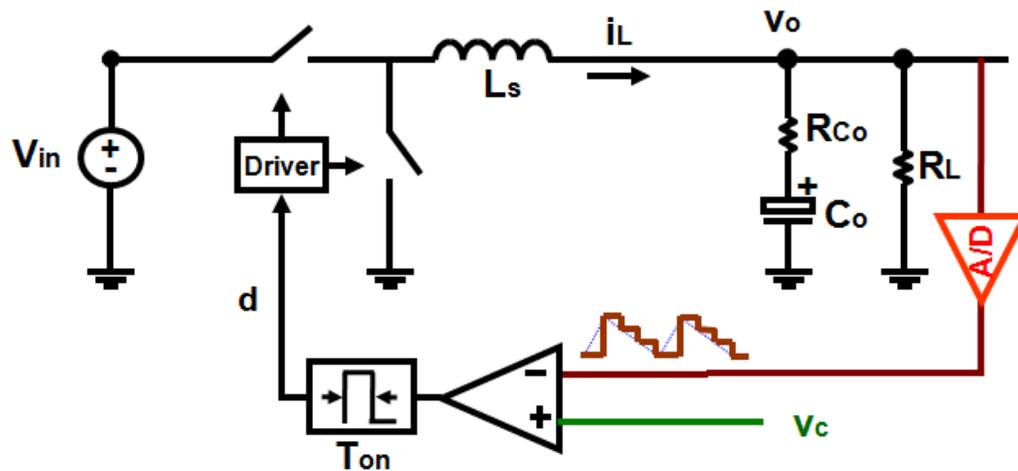
Figure 5.11. Digital constant on-time control

As shown in Figure 5.12, limit-cycle oscillation occurs due to the sampling of the ideal ADC without quantization effects. However, the pattern of the oscillation is quite different from that shown in Figure 5.10, which occurs in the digital voltage-mode control structure. As had been expected, the control signal v_c limits the oscillation amplitude cycle by cycle through the voltage ripple feedback in the PWM modulator.
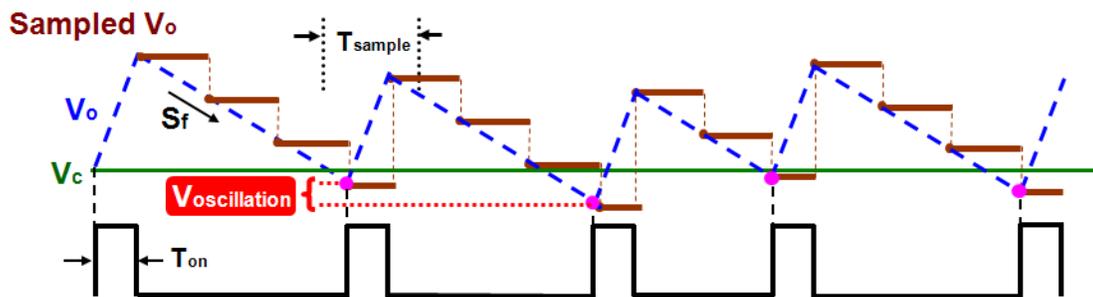
Figure 5.12. Voltage waveforms in the digital constant on-time control

In addition, by assuming that the output voltage ripple is dominated by the ESR ripple, even the maximum oscillation amplitude $V_{oscillation.max}$ can be easily calculated as:

$$V_{oscillation.max} = T_{sample} \cdot s_f \qquad\qquad (5.13)$$

where T_{sample} is the sampling period and s_f is the magnitude of down-slope of the voltage ripple. It is found that (1) is also true for a non-ideal ADC with quantization effects and a certain conversion time.

In this group of digital current-mode control structures, the oscillation amplitude is easily controllable, and the resolution of the DPWM is no longer critical. Therefore, it is not necessary to follow the usual rules [92][93] in the digital voltage-mode control architecture. A straightforward way to reduce the oscillation amplitude is to increase the sampling rate of the ADC. However, this will increase the design challenge for the ADC. Referring to the solution of eliminating the subharmonic oscillation in the analog peak current-mode control, the external ramp is used as the compensation ramp. Although the oscillation in the digital current-mode control is quite different from the subharmonic oscillation, the concept can be applied here too. The external digital ramp starts to count at the end of the on-time period and resets at the beginning of the on-time period in every switching cycle, as shown in Figure 5.13.
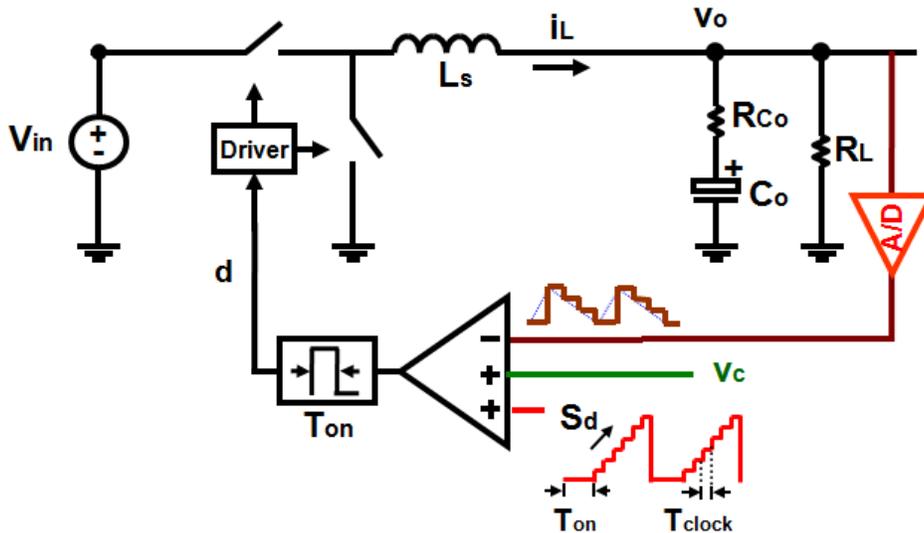
Figure 5.13. Proposed digital current-mode control architecture

In the proposed current-mode control architecture, the oscillation amplitude calculation is quite different from the previous analysis. For the case of using the ideal ADC, as shown in Figure 5.14, the maximum oscillation amplitude is calculated by:

$$V_{oscillation.\max} = T_{clock} \cdot s_f \tag{5.14}$$

where, T_{clock} is the system clock period. Comparing this with (5.13), it is apparent that T_{clock} is much smaller than T_{sample} in the digital controller, which means that the oscillation amplitude becomes very small due to the effects of the digital external ramp.
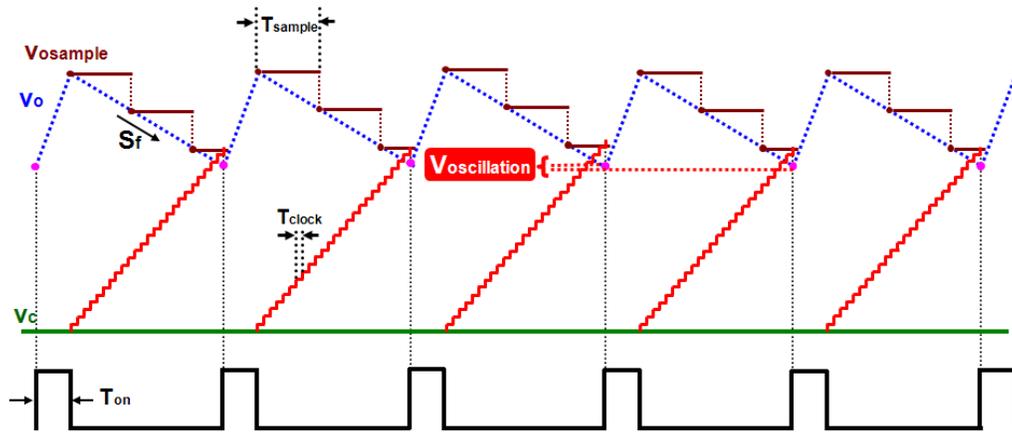
(a)
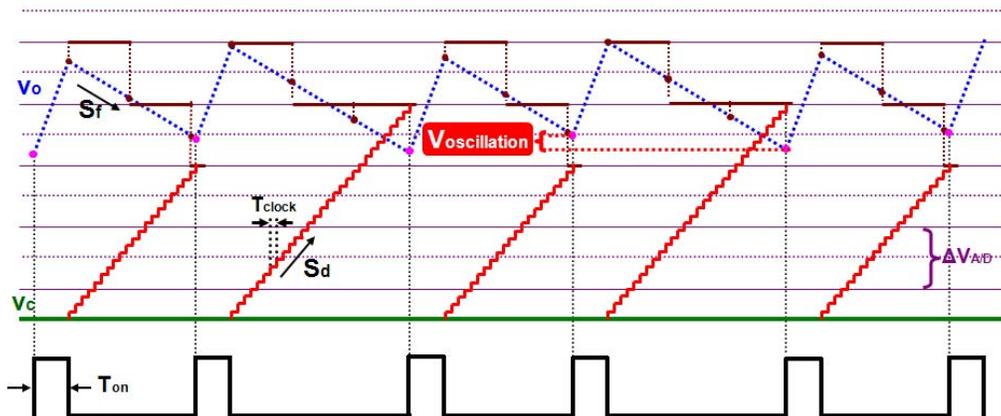
(b)

Figure 5.14. Voltage waveform in the proposed digital current-mode control architecture: (a) the

ideal ADC case, and (b) the non-ideal ADC case

When using the non-ideal ADC, as shown in Figure 5.14, the maximum oscillation amplitude is calculated by:

$$V_{oscillation.max} = [\Delta V_{ADC} / s_d]_{T_{clock}} \cdot s_f \qquad\qquad (5.15)$$

where, ΔV_{ADC} is the resolution of the ADC, and s_d is the magnitude of slope of the external ramp. In (5.15), s_d is designed according to a given ΔV_{ADC}, so that ($\Delta V_{ADC}/s_d$) is less than T_{sample}. The expression $[\Delta V_{ADC}/s_d]_{Tclock}$ means the value of ($\Delta V_{ADC}/s_d$) is quantized by T_{clock}. This result is also true when there is a certain time delay due to the conversion time of the ADC.

Based on (5.13)~(5.15), it is found that, with a given ΔV_{ADC}, the reduction of oscillation amplitude can be achieved only when s_d is larger than a certain value, which makes $\Delta V_{ADC}/s_d < T_{sample}$. The oscillation amplitude can be further reduced by increasing the s_d until it reaches the extreme case in which the value $[\Delta V_{ADC}/s_d]_{Tclock}$ is equal to T_{clock}.

In the proposed digital current-mode control architecture, oscillation always happens intentionally in order to achieve equivalent high resolution output based on the average effects from the power stage low-pass filter. At the same time, the instantaneous output voltage is also limited through the current information feedback in the proposed structure. It is different to achieve these two characteristics at the same time through the dithering techniques in the voltage-mode control architecture [92][99][100].

The MATLAB simulation tool is used to do preliminary simulation. The simulation parameters are: inductor L_s = 300nH, capacitor: 8 OSCON capacitor (560uF/6mΩ), input voltage V_{in} = 12V, load resistor R_L = 0.1Ω, on time T_{on} = 0.33us, sampling frequency F_{sampe} = 1.2MHz (about 4 times the switching frequency), ΔV_{ADC} = 3.125mV, and system clock F_{clcok} = 12MHz. Simulation results are shown in Figure 5.15. From the simulation results, the improvement is obvious: the oscillation amplitude of the output voltage is greatly reduced due to the effects of the external ramp.
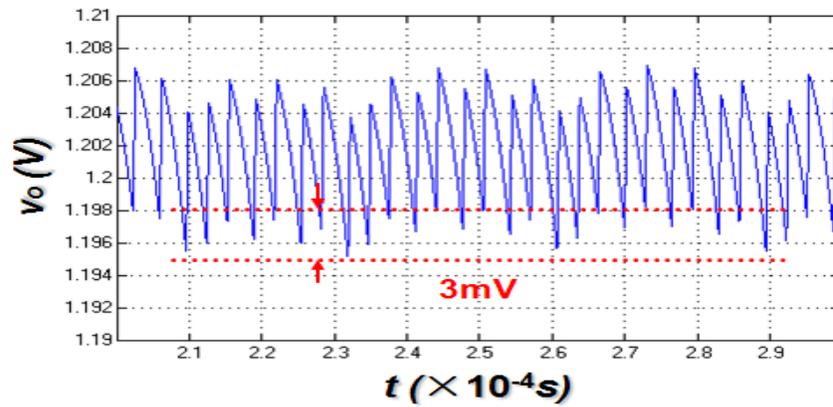
(a)
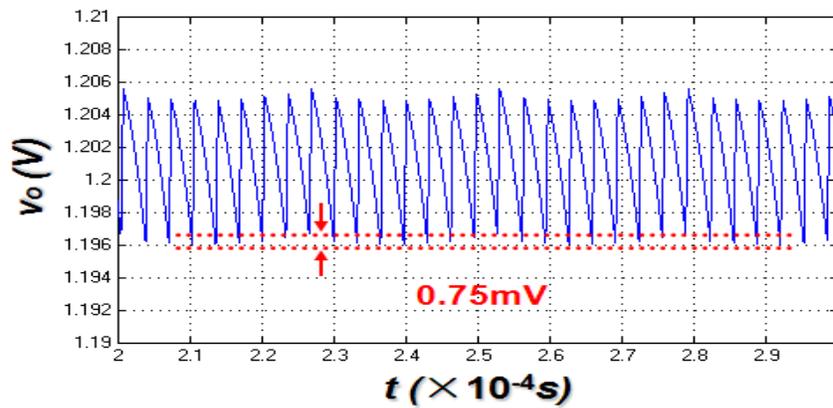
(b)

Figure 5.15. Steady-state simulation results: (a) no external ramp, and (b) with the external ramp

($s_d = 4s_f$)

5.4   Modeling of Proposed Digital Current-Mode Control Architecture

In the previous chapter a new modeling approach has been proposed to model the current-mode control and the V^2 type current-mode control. The power stage, the switches and the PWM modulator are treated as an entity to model. The describing function (DF) method is used to derive the transfer function from the control signal v_c to the output voltage v_o directly. A similar modeling concept can also be applied in the proposed digital current-mode control architecture. As shown in Figure 5.16, a small magnitude sinusoidal

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perturbation at the frequency f_m is injected through control signal v_c, then based on the perturbed output voltage waveform, the describing function from the control signal v_c to the output voltage v_o can be determined by mathematical derivation. The quantization effects of the ADC and the digital ramp are ignored during the derivation, and the ramp is assumed to intersect with the sampled output voltage $v_{osample}$ at the k_{th} sampling period in each switching cycle. For the detailed derivation process please refer to previous chapters.
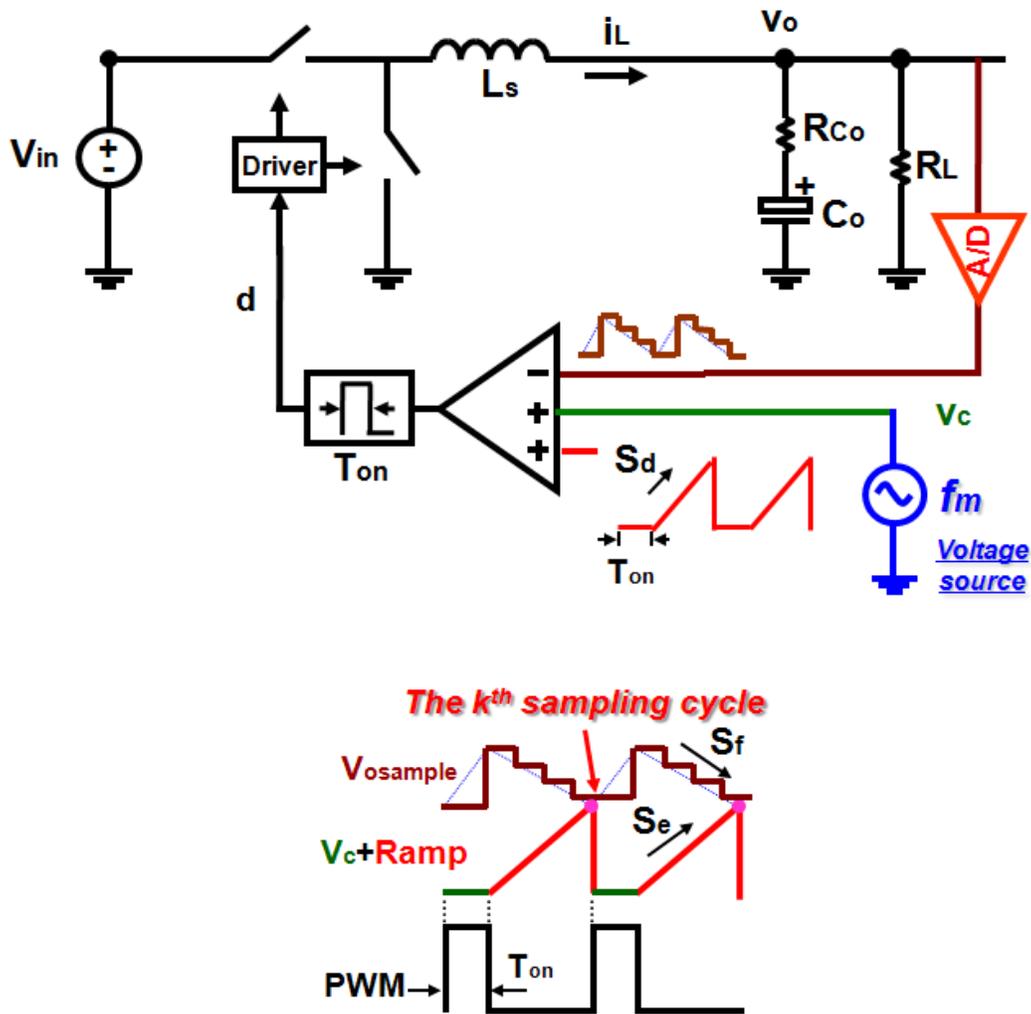
Figure 5.16. Modeling methodology for the control-to-output transfer function

The small-signal transfer function is derived as:

$$\frac{v_o(s)}{v_c(s)} = \frac{\dfrac{f_s}{s_d}(1-e^{-sT_{on}})(1-e^{-sT_{sw}})(1+\dfrac{1}{R_L C_o s})\dfrac{V_{in}}{L_s s}\dfrac{R_L(R_{Co}C_o \cdot s+1)}{(R_L+R_{Co})C_o \cdot s+1}}{1-(2-\dfrac{s_f}{s_d}-\dfrac{s_f}{s_d}\dfrac{(k-1)T_{sample}+\dfrac{T_{on}+T_{sw}}{2}}{C_o R_{Co}})e^{-sT_{sw}}-(\dfrac{s_f}{s_d}-1+\dfrac{s_f}{s_d}\dfrac{(k-1)T_{sample}-\dfrac{T_{sw}-T_{on}}{2}}{C_o R_{Co}})e^{-s2T_{sw}}}$$

(5.16)

where, T_{sw} is the switching period, f_s is the switching frequency, L_s is the inductance of inductor, R_{Co} is the ESR of the output capacitors, C_o is the capacitance of the output capacitors, V_{in} is the input voltage, R_L is the load resistor, and $s_f = R_{Co} \cdot V_o / L_s$. The result is not applicable to the frequencies when $f_m = n*f_s$ where n is positive integer. Without losing generality, the results at those frequencies will not be shown in this paper. This can be further simplified as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{1}{(1+\dfrac{s}{Q_1\omega_1}+\dfrac{s^2}{\omega_1^2})} \cdot \frac{(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_d\omega_2}+\dfrac{s^2}{\omega_2^2})(1-\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})+\dfrac{s_d}{s_f}R_{Co}C_o T_{sw} \cdot s^2}$$

(5.17)

where, $\omega_1 = \pi/T_{on}$, $Q_1 = 2/\pi$, $\omega_2 = \pi/T_{sw}$, and $Q_d = T_{sw}/[R_{Co}C_o + T_{on}/2 + (k-1)T_{sample}]\pi$. This approximation is valid up to half of the switching frequency.

When the duty cycle is small, the transfer function can be further simplified as:

$$\frac{v_o(s)}{v_c(s)} \approx \frac{(1+\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})(R_{Co}C_o s+1)}{(1+\dfrac{s}{Q_d\omega_2}+\dfrac{s^2}{\omega_2^2})(1-\dfrac{s}{Q_1\omega_2}+\dfrac{s^2}{\omega_2^2})+\dfrac{s_d}{s_f}R_{Co}C_o T_{sw} \cdot s^2}$$

(5.18)

The Simplis simulation tool is used to verify the model. The quantization effects of the ADC and the digital ramp are ignored. The model can predict the system response very well as shown in Figure 5.17.

(a)

(b)
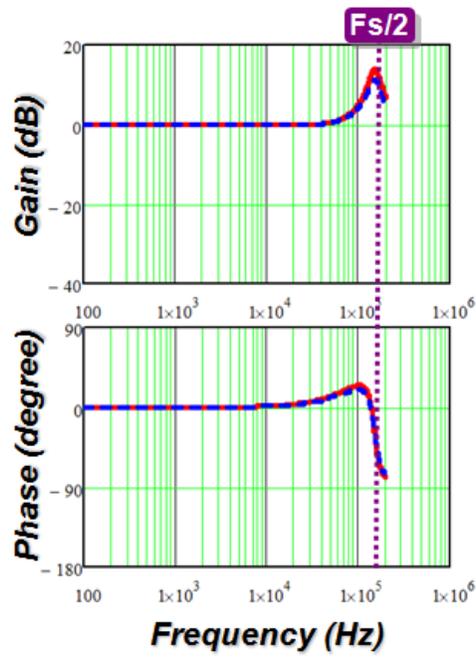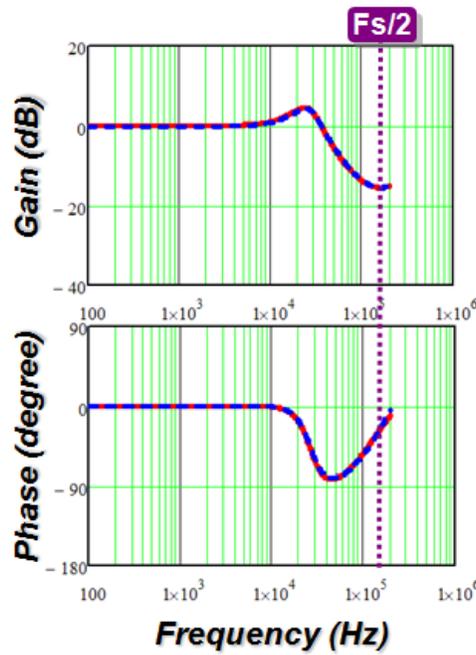
Red curve: proposed model; Blue curve: Simplis simulation (≈ measurement)
Figure 5.17. Control-to-output transfer function comparison: (a) $s_d = s_f$, and (b) $s_d = 4s_f$

The stability of the system can be determined by the location of the system poles based on (5.18). The location of the system poles and zeros is shown in Figure 5.18.

(a)   **(b)**
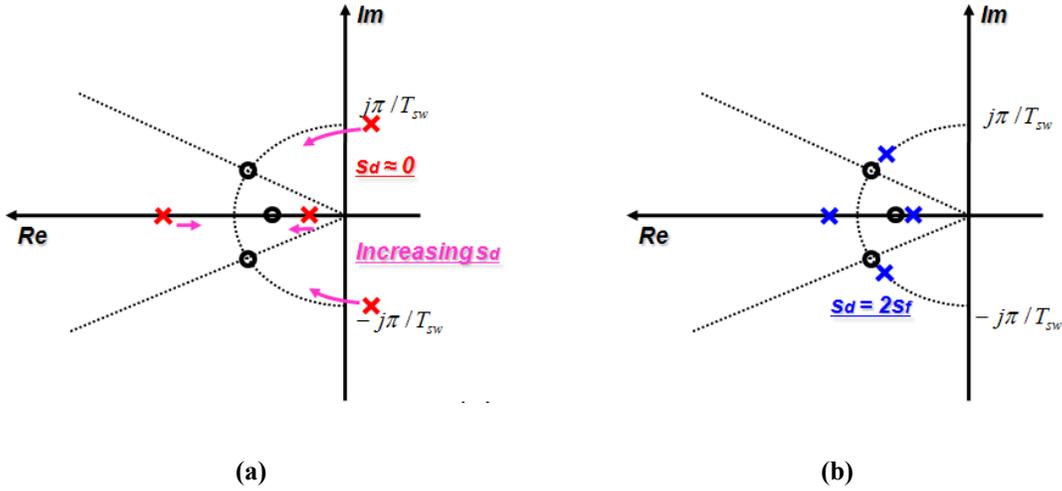
Figure 5.18. Location of the system poles (x) and zeros (o): (a) $s_d \approx 0$, and (b) $s_d = 2s_f$

It is found that when s_d is very small, there are two poles at the right-half plane which means the system is unstable. When s_d is increased, the two poles will move to the left-half plane. In a word, the selection of the external ramp is not only related to the amplitude of the limit-cycle oscillation, but also very important to the stability of the system.

The output impedance can be modeled as shown in Figure 5.19. Following the same methodology, a small magnitude sinusoidal perturbation at the frequency f_m is injected through the output current i_o, then based on the perturbed output voltage waveform, the describing function from the output current i_o to the output voltage v_o can be found out by mathematical derivation.

The output impedance can also be derived as (5.19) and simplified as (5.20):

$$Z_o(s) = \{ \frac{\frac{f_s}{s_d}(1-e^{-sT_{on}})(1-e^{-sT_{sw}})e^{-[T_{sw}-T_{on}-(k-1)T_{sample}]s}(R_{Co}+\frac{1}{C_o s})\frac{V_{in}}{L_s s}}{1-(2-\frac{s_f}{s_d}-\frac{s_f}{s_d}\frac{(k-1)T_{sample}+\frac{T_{on}+T_{sw}}{2}}{C_o R_{Co}})e^{-sT_{sw}}-(\frac{s_f}{s_d}-1+\frac{s_f}{s_d}\frac{(k-1)T_{sample}-\frac{T_{sw}-T_{on}}{2}}{C_o R_{Co}})e^{-s2T_{sw}}} -1\}$$

$$\cdot (R_{Co}+\frac{1}{C_o s})$$

<div align="right">(5.19)</div>

$$Z_o(s) \approx \{ \frac{1}{(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2})} \cdot \frac{(1 - \frac{s}{Q_1\omega_3} + \frac{s^2}{\omega_3^2})}{(1 + \frac{s}{Q_1\omega_4} + \frac{s^2}{\omega_4^2})} \cdot \frac{(1 + \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2})(R_{Co}C_o s + 1)}{(1 + \frac{s}{Q_d\omega_2} + \frac{s^2}{\omega_2^2})(1 - \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2}) + \frac{S_d}{s_f}R_{Co}C_o T_{sw} \cdot s^2} - 1\}$$

$$\cdot (R_{Co} + \frac{1}{C_o s})$$

(5.20)

where, $\omega_4 = \pi/[T_{sw} - T_{on} - (k-1)T_{sample}]$
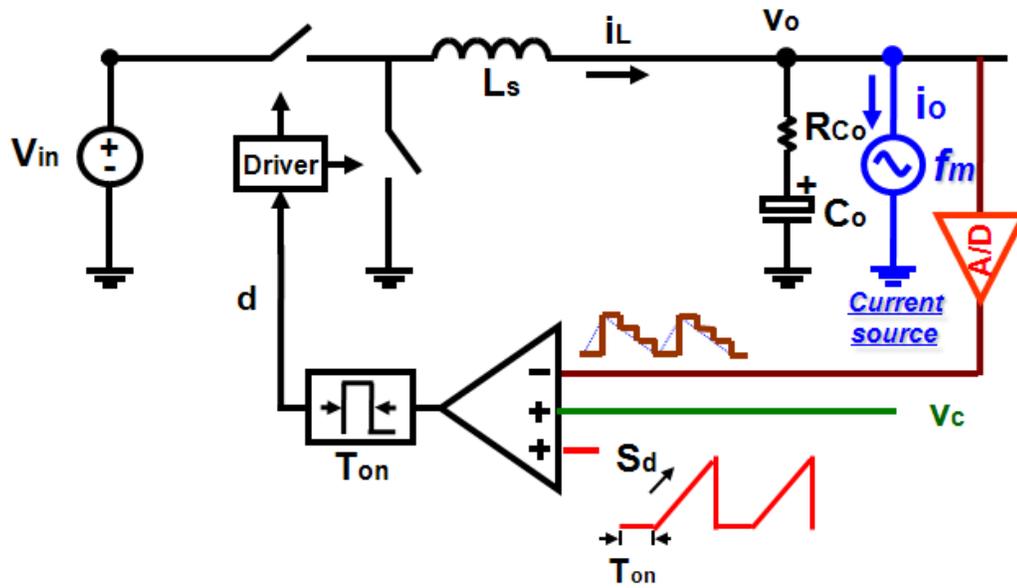
Figure 5.19. Modeling methodology for the output impedance

The model can accurately predict the output impedance of the system as shown in Figure 5.20.

The control-to-output transfer function and the output impedance are plotted for different external ramp cases, as shown in Figure 5.21 and Figure 5.22. It is clear that the control-to-output transfer function can be approximated as a second-order transfer function. Furthermore, when the amplitude of the ramp is increased, the output impedance becomes larger which means the transient response becomes worse.

(a)

(b)
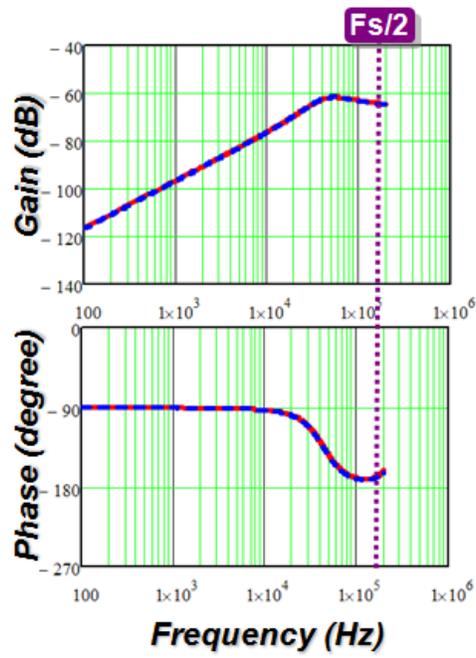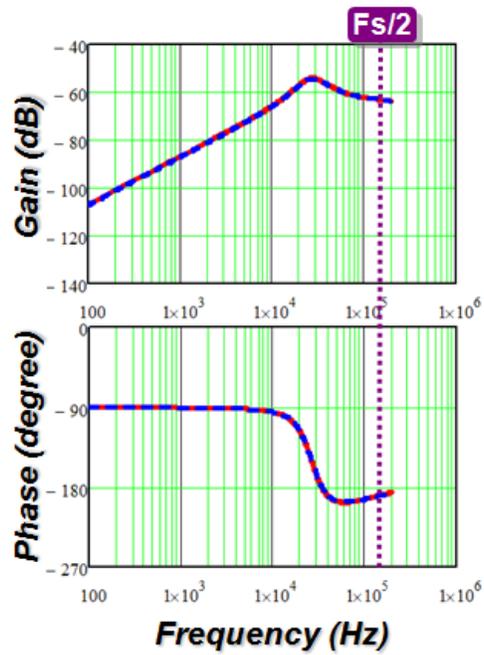
Red curve: proposed model; Blue curve: Simplis simulation (≈ measurement)
Figure 5.20. Output impedance comparison: (a) $s_d = 2s_f$, and (b) $s_d = 4s_f$
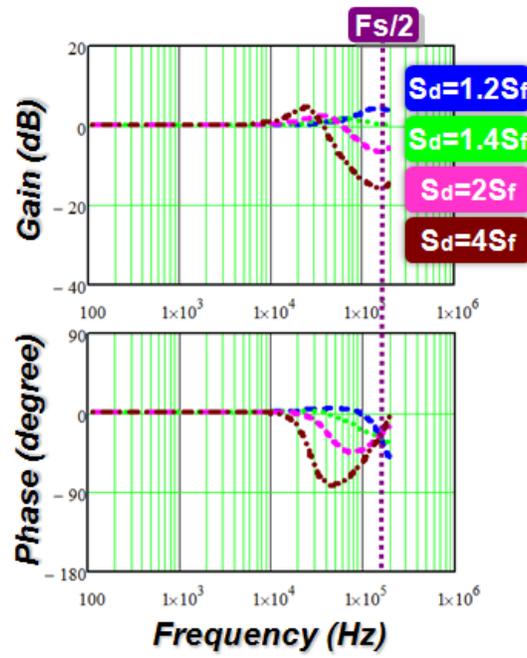
Figure 5.21. Control-to-output transfer function
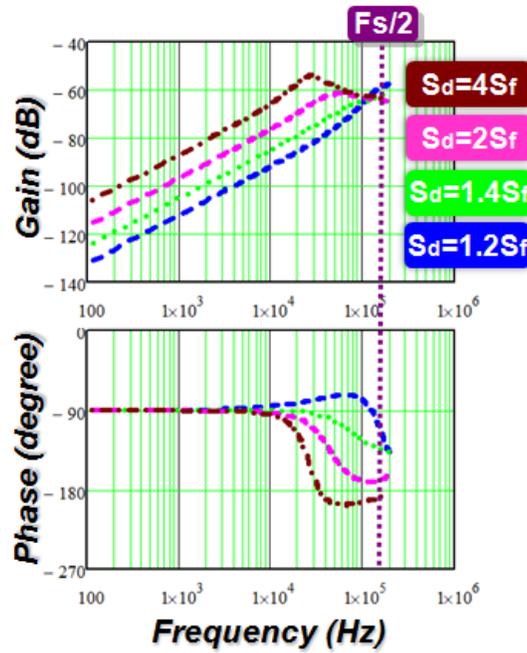
Figure 5.22. Output impedance

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Again, the MATLAB simulation tool is used to simulate the transient response, as shown in Fig. 18. As has been predicted, the voltage spike during the load step-up and step-down becomes larger with the larger external ramp.
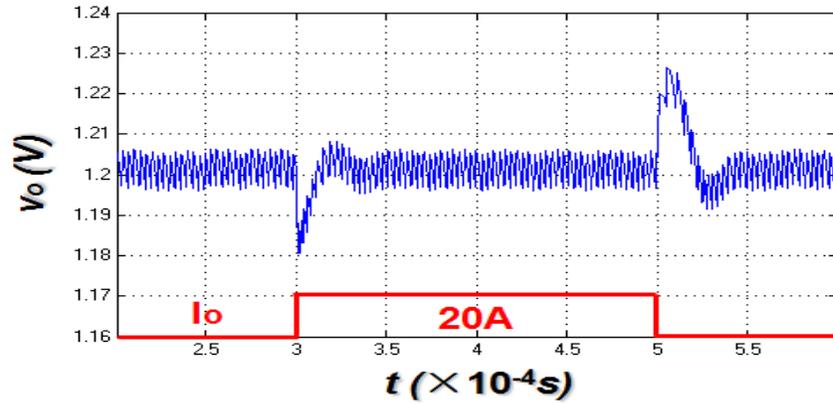
(a)
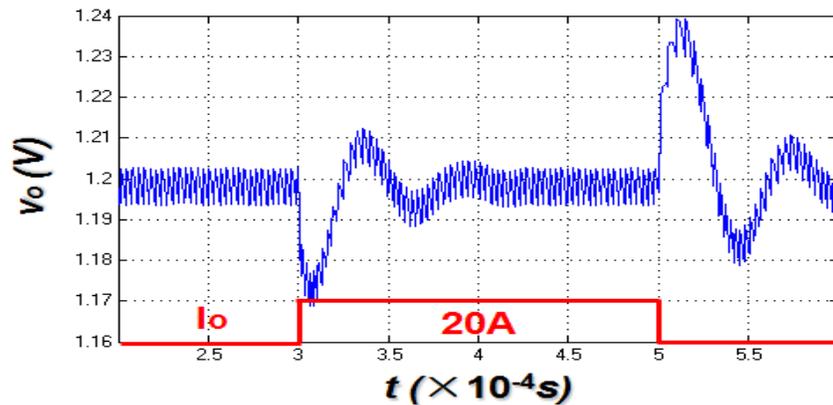
(b)

Figure 5.23. Transient simulation results: (a) $s_d = 2s_f$, and (b) $s_d = 6s_f$

Based on previous analysis, we prefer the external ramp with relatively large amplitude in terms of the reduction of the limit-cycle oscillation, but the transient response suffers with this condition. In other words, the single inner loop is unable to compensate the steady-state (limit-cycle oscillation) and transient response at the same time. One way to solve this issue is: to design the inner loop to reduce the amplitude of the limit-cycle oscillation and to design the outer loop based on (5.17) to improve the transient response.

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One thing to be aware of is that we need to make sure that outer loop compensator is not influenced by the limit-cycle oscillation. An example is shown in Fig. 19.
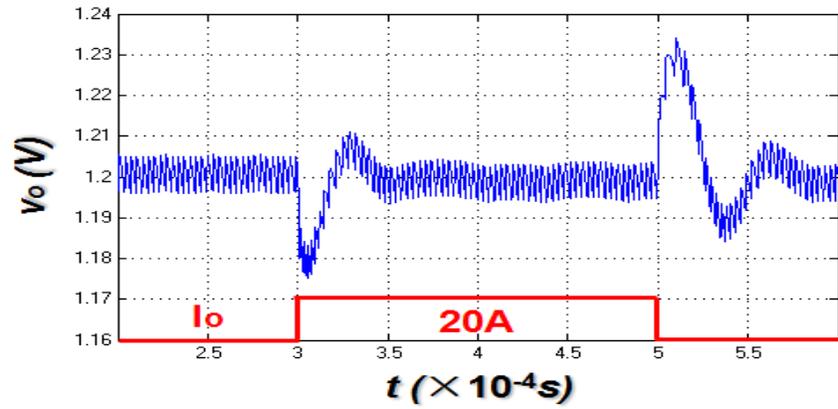
(a)
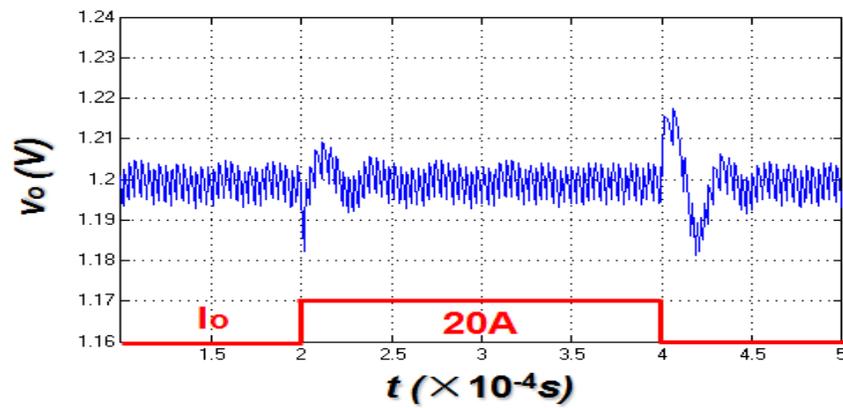
(b)

Figure 5.24. Transient simulation results ($s_d=4s_f$): (a) no compensation, and (b) with outer loop compensation

5.5   Adaptive Ramp Design and the Extension of Proposed Structure

A. Adaptive ramp design

The previous section presents the inner loop and the outer loop designs to deal with different aspects separately. However, with the help of the flexibility of digital control, an adaptive ramp design is proposed so that the single inner loop can handle not only the steady-state but also the transient response. As shown in Figure 5.25, in the original design of the external ramp, the ramp starts to count at the end of the on-time period, which means that the ramp exists for the entire off-time range; in the adaptive design, the slope of the external ramp stays the same but the ramp only exists in a very small range of time around the steady state off-time ending point (for example, $T_{ramp} = 10\sim20\%T_{sw}$).

<div align="center">(a)   (b)</div>
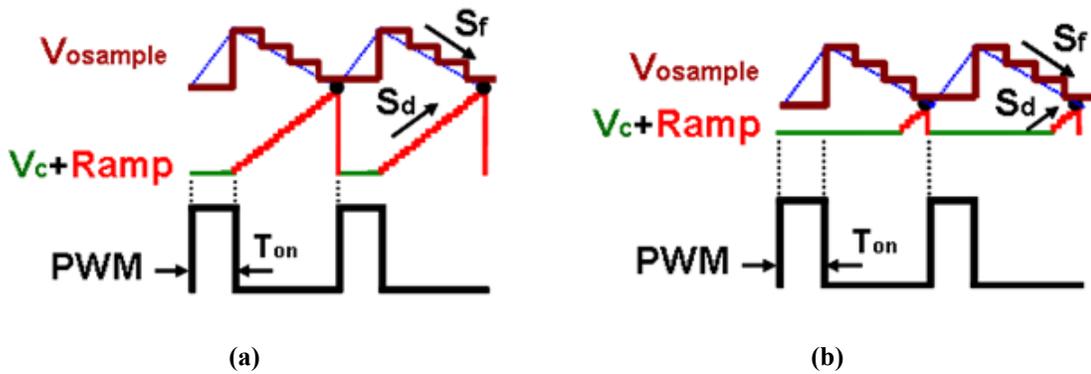
Figure 5.25. External ramp design: (a) original design, and (b) adaptive design

The benefit of the new design is that the inner loop can reduce the steady-state limit-cycle oscillation and the voltage spike when the transient occurs at the same time: at the steady state when the limit-cycle oscillation is relatively small, the sampled output voltage will intersect with the external ramp which is good for the reduction of the limit-cycle oscillation; when the transient occurs, the sampled output voltage will directly intersect with the control signal instead of the external ramp, which can boost the transient response. As shown in Figure 5.26, the steady-state limit-cycle oscillation is similar for both cases, but the adaptive ramp design can greatly reduce the voltage spike when the transient occurs.

<div align="center">131</div>
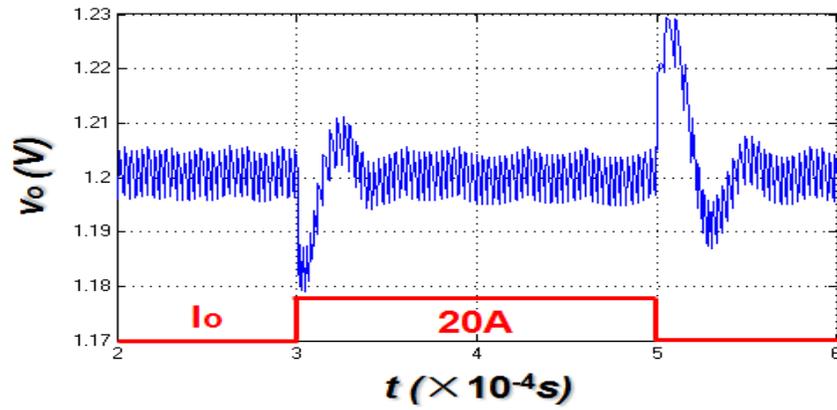
(a)
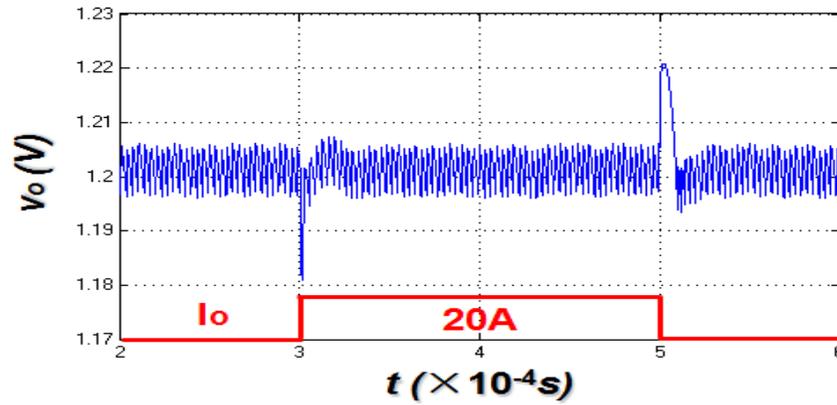
(b)

Figure 5.26. Transient simulation results ($s_d = 4s_f$): (a) original ramp design, and (b) adaptive ramp design

In order to implement the adaptive ramp design, we must know the approximate duty cycle value at the steady state. Therefore, in an application with a large steady-state duty cycle range, the additional feed-forward loop is necessary for the digital controller to calculate the duty cycle value for a certain input voltage and output voltage.

B. Extension of proposed structure

All of the previous analysis in this study is based on the assumption that the output voltage ripple is dominated by the ESR ripple. This assumption is true for the OSCON capacitor and the SP capacitor with a low ESR zero. For some types of capacitors, e.g. the ceramic capacitors, the ESR zero is very high, and the current feedback information is

diminished by the capacitor ripple. In order to implement the proposed digital control structure, the current information can be obtained from a sensing network other than the ESR. The DCR sensing network is shown as an example in Figure 5.27.
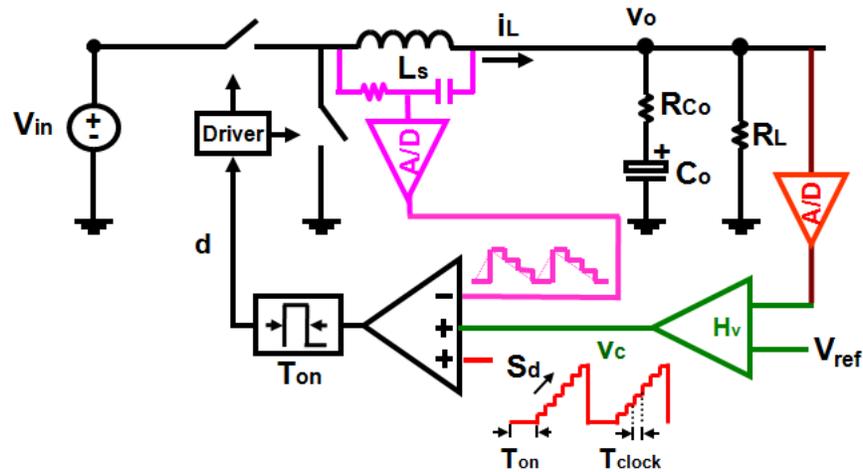
Figure 5.27. Extension of the proposed digital current-mode control architecture

Multi-phase implementation can be achieved as shown in Figure 5.28. The additional current information is used to guarantee current sharing among different phases by adjusting the on-time.
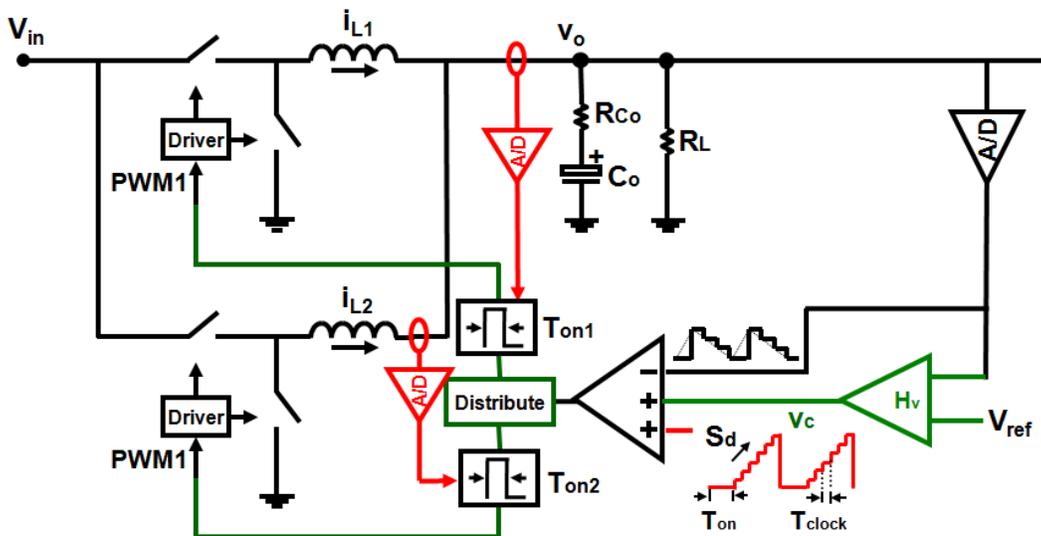
Figure 5.28. Multi-phase implementation

5.6   Experimental Verification

Experimental verification has been done through the buck converter power stage and Xilinx Spartan II FPGA board with an additional ADC, as shown in Figure 5.29. In the power stage, inductor L = 300nH, and the capacitor is the 10 SP capacitor (390uF/10mΩ). The input voltage is 12V, and the output voltage is 1.2V. The switching frequency is about 300 KHz.
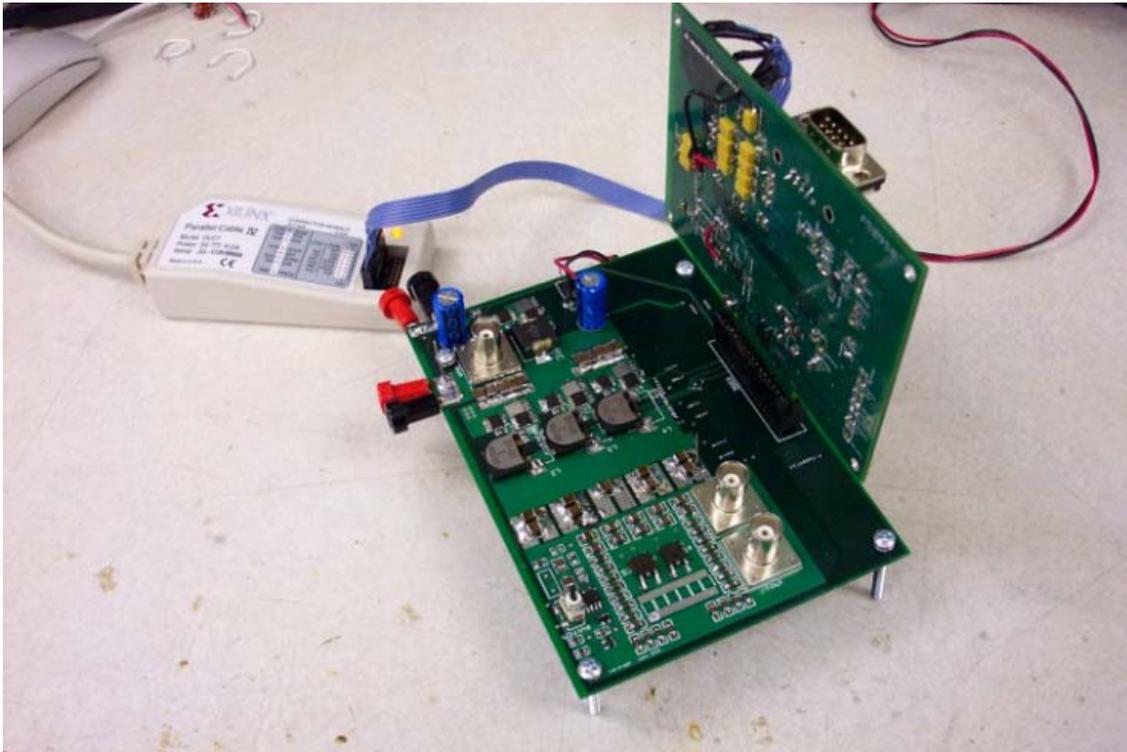
Figure 5.29. FPGA-based digital control platform

In order to verify the proposed high resolution DPWM modulation method, The ADC resolution ΔV_{ADC} is set to be 8 mV and the system clock frequency is 150 MHz. For the conventional counter-based DPWM: $\Delta V_o = V_{in}*\Delta D = 24$mV, which is larger than ΔV_{ADC} (8mV); Severe limit cycle oscillations occur in this case, as shown in Figure 5.30. However, for the proposed DPWM method #1 and #3: $\Delta V_o = 2.4$mV, which is less than ΔV_{ADC} (8mV); Limit cycle oscillations can be greatly reduced.
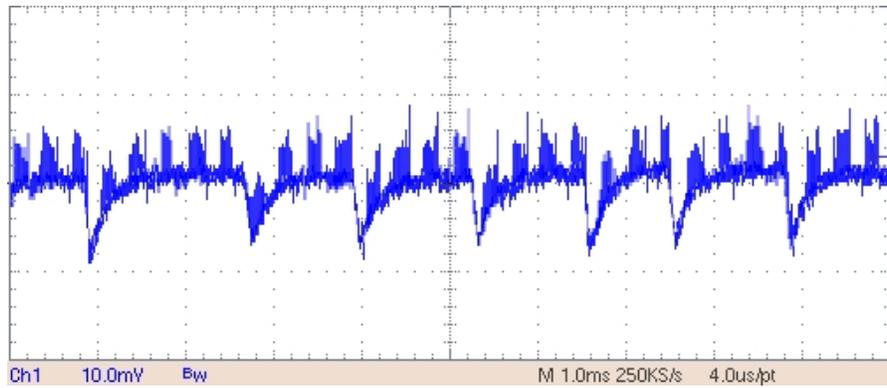
(a)
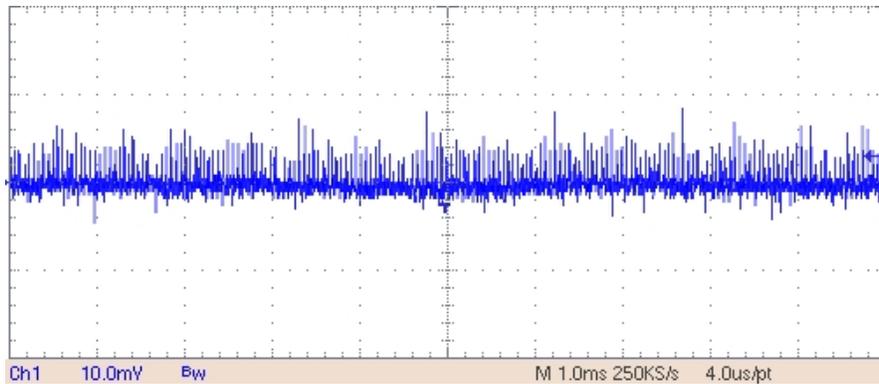
(b)
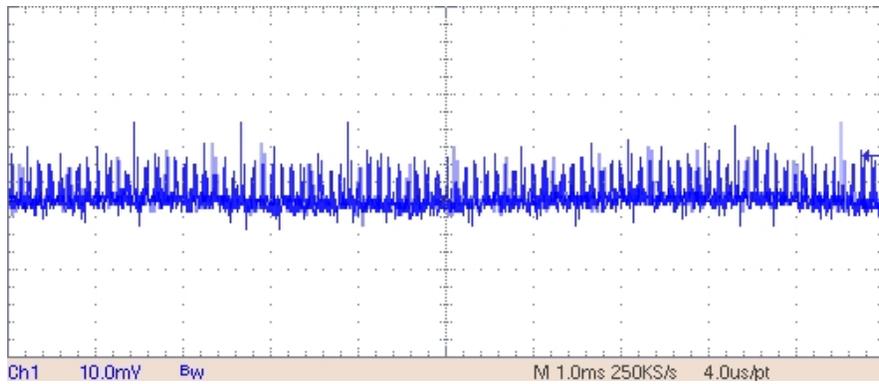
(c)

Figure 5.30. Output voltage waveform: (a) conventional DPWM, (b) proposed method #1, and (c) proposed method #3

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The switching frequency variation for different methods is shown in Figure 5.31. Proposed method #3 can achieve nearly constant switching frequency operation.

$V_{in} = 8.7V$ $V_{in} = 19V$

(a)

$V_{in} = 8.7V$ $V_{in} = 19V$

(b)
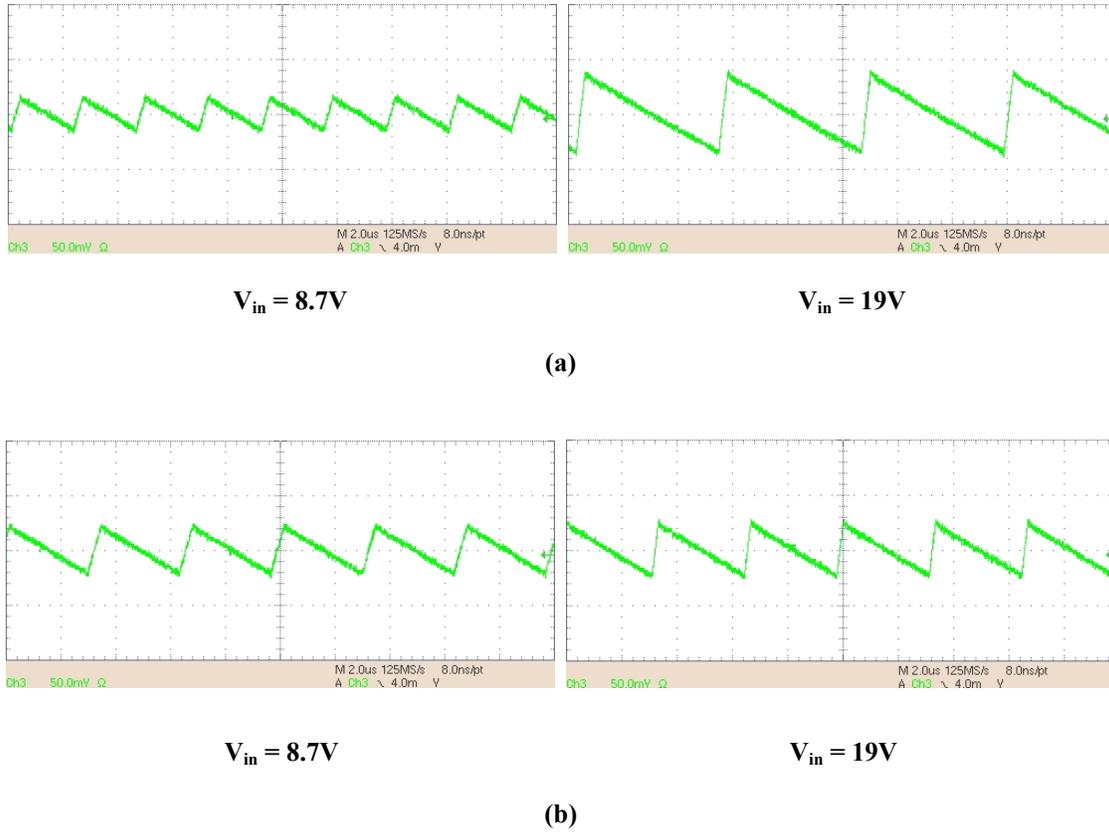
Figure 5.31. Inductor current waveform: (a) proposed mothed #1, and (b) proposed method #3

In order to verify the proposed digital control structure, the ADC resolution ΔV_{ADC} is 3.2 mV, and the sampling rate is about 4 times the switching frequency. The clock frequency is 18MHz. The steady-state experiment results are shown in Figure 5.32. The oscillation amplitude is reduced due to the effects of the external ramp. Moreover, the steady state is very similar for two different ramp designs with the same s_d.

The transient response is shown in Figure 5.33. Comparing the two ramp designs, it is apparent that the adaptive ramp design can greatly improve the transient response.
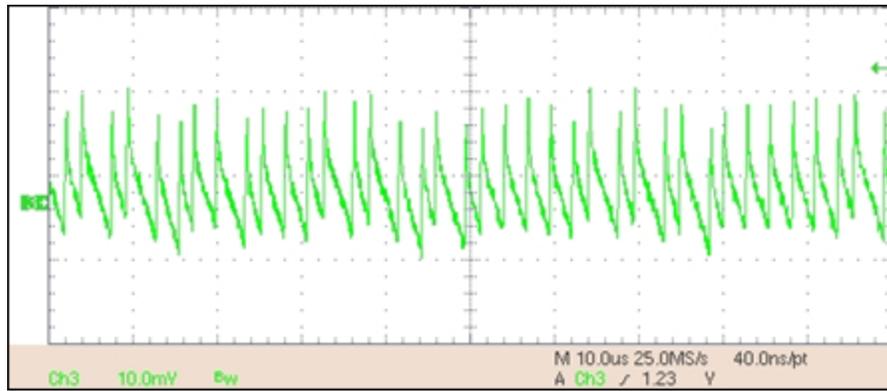
(a)
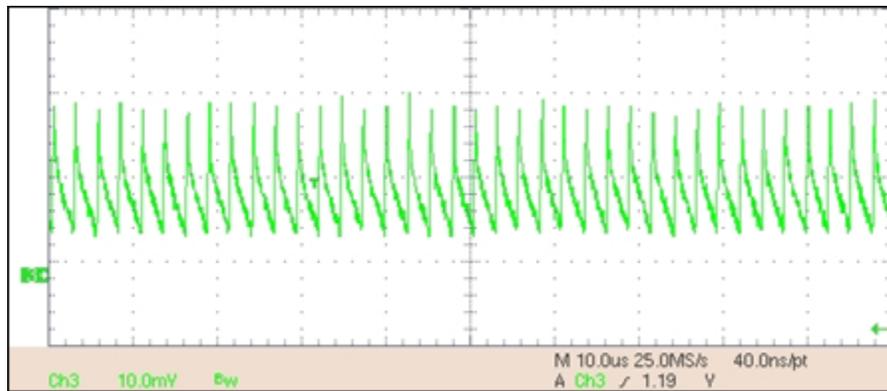
(b)
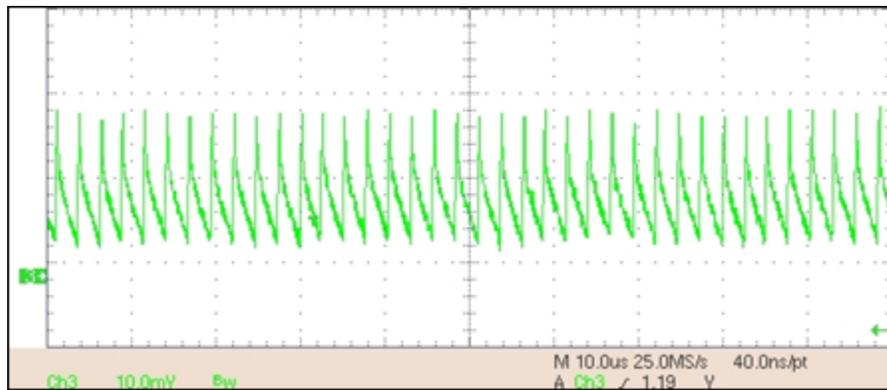
(c)

Figure 5.32. Output voltage steady state experiment results: (a) no external ramp, (b) original ramp design ($s_d = 8s_f$), and (c) adaptive ramp design ($s_d = 8s_f$)

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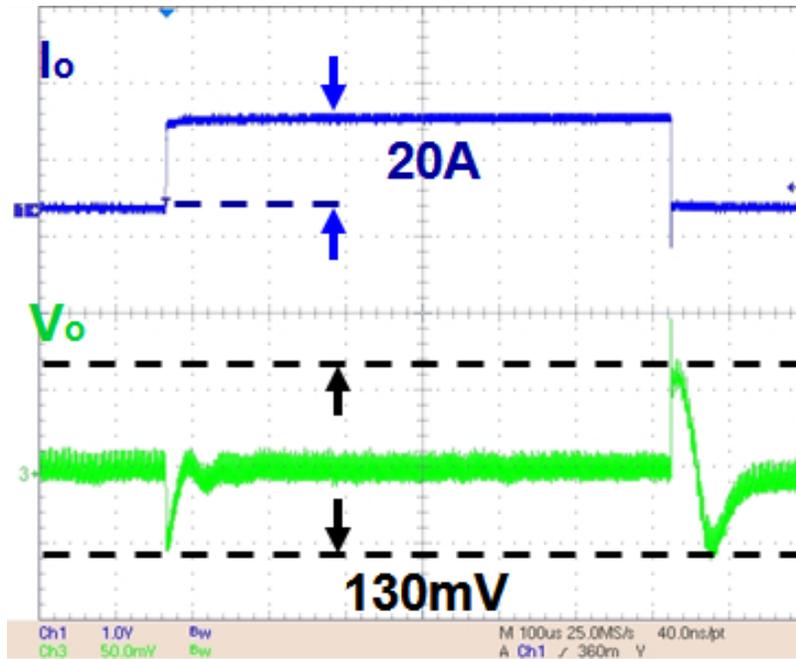
(a)
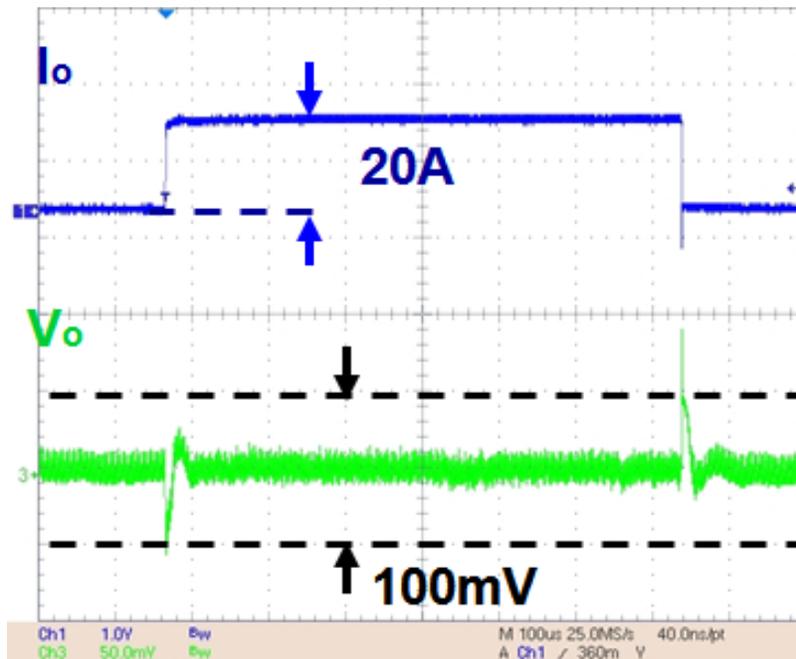
(b)

Figure 5.33. Output voltage transient response experiment results($s_d = 8s_f$): (a) original ramp design, and (b) adaptive ramp design

5.7   Summary

High-resolution digital pulse-width modulator (DPWM) is considered to be indispensable for minimizing the possibility of the unpredicted limit-cycle oscillation, but results in high cost, especially in the application of the voltage regulator (VR) for the microprocessor. In order to solve this issue, several DPWM modulation methods are proposed to improve the DPWM resolution. Furthermore, a fully digital current-mode control architecture which can effectively limit the oscillation amplitude is presented, thereby greatly reducing the design challenge for the digital controller by eliminating the need for the high-resolution DPWM. New modeling strategy is also used to model the proposed digital current-mode control in this chapter. Simulation and experimental results are used to verify the proposed concepts.

Chapter 6. Conclusion

6.1 Summary

Due to unique characteristics, current-mode control architectures with different implementation approaches has been widely used in power converter design to achieve current sharing, AVP control, and light-load efficiency improvement. Therefore, an accurate model for current-mode control is indispensable to system design due to the existence of subharmonic oscillations. The fundamental difference between current-mode control and voltage-mode control is the PWM modulation. The inductor current ramp, one of state variables influenced by the input voltage and the output voltage, is used in the modulator in current-mode control while an external ramp is used in voltage-mode control. The peculiarity of current-mode control results in the difficulty of obtaining the small-signal model for current-mode control in the frequency domain. There has been a long history of the current-mode control modeling. Many previous attempts have been made especially for constant-frequency peak current-mode control.   However, few models are available for variable-frequency constant on-time control and V^2 current-mode control. It's hard to directly extend the model for peak current-mode control to those controls. Furthermore, there is no simple way of modeling the effects of the capacitor ripple which may result in subharmonic oscillations in V^2 current-mode control. In this dissertation, the primary objective to investigate a new, general modeling approach for current-mode control with different implementation methods.

First, the fundamental limitation of average models for current-mode control is identified. The sideband components are generated and coupled with the fundamental component through the PWM modulator in the current loop. Moreover, the switching frequency harmonics cannot be ignored in the current loop since the current ripple is used for the PWM modulation. Available average models failed to consider the sideband effects and high frequency harmonics. Due to the complexity of the current loop, it is difficult to analyze current loop in the frequency domain. A new modeling approach for current-mode control is proposed based on the time-domain analysis. The inductor, the switches and the

PWM modulator are treated as a single entity to model instead of breaking them into parts to do it. Describing function method is used. Proposed approach can be applied not only to constant-frequency modulation but also to variable-frequency modulation. The fundamental difference between different current-mode controls is elaborated based on the models obtained from the new modeling approach.

Then, an equivalent circuit representation of current-mode control is presented for the sake of easy understanding. The effect of the current loop is equivalent to controlling the inductor current as a current source with certain impedance. This circuit representation provides both the simplicity of the circuit model and the accuracy of the proposed model.

Next, the new modeling approach is extended to V^2 current-mode control based on similar concept. The model for V^2 current-mode control can accurately predict subharmonic oscillations due to the influence of the capacitor ripple. Two solutions are discussed to solve the instability issue.

After that, a digital application of current-mode control is introduced. High-resolution digital pulse-width modulator (DPWM) is considered to be indispensable for minimizing the possibility of unpredicted limit-cycle oscillations, but results in high cost, especially in the application of voltage regulators for microprocessors. In order to solve this issue, a fully digital current-mode control architecture which can effectively limit the oscillation amplitude is presented, thereby greatly reducing the design challenge for digital controllers by eliminating the need for the high-resolution DPWM. The new modeling strategy is also used to model the proposed digital current-mode control to help system design.

As a conclusion, a new modeling approach for current-mode control is fully investigated. The describing function is utilized as a tool in this dissertation. Proposed approach is quite general and not limit by implementation methods. All the modeling results are verified through simulation and experiments.

6.2   Future Works

In the dissertation, the new modeling approach is applied to current-mode control and V^2 current-mode control separately. The models results are quite different for different implementations. It could be interesting to summarize them and form a unified model for all current-mode controls. Furthermore, the equivalent circuit model could be extended to boost converters and buck-boost converters with current-mode control. Average current-mode control could be another application of the new modeling approach.

Appendix A. Describing Function Derivation

The appendix provides the detail derivations for the describing function used in peak current-mode control and constant on-time control.

A.1 Derivation for Peak-Current-Mode Control

(a) Control-to-inductor current transfer function

As shown in Figure A.1, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the control signal v_c; then, based on the perturbed inductor current waveform, the describing function from the control signal v_c to the inductor current i_L can be found by mathematical derivation.
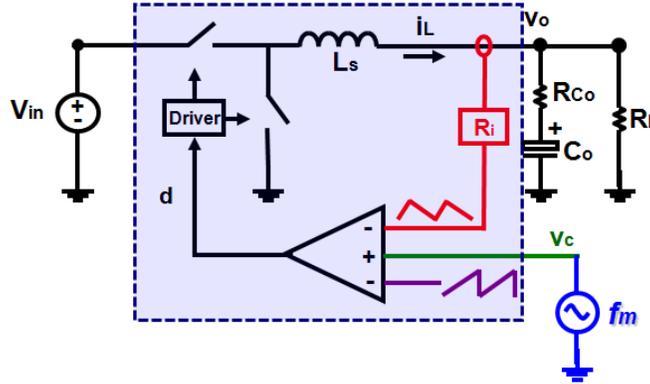
Figure A.1. Modeling for the influence of the control signal v_c in peak current-mode control

Because the switching cycle T_{sw} is fixed, the on-time and the off-time is modulated by the perturbation signal $v_c(t)$: $v_c(t) = r_0 + \hat{r}\sin(2\pi f_m \cdot t - \theta)$, where, r_0 is the steady state value of the control signal, $\hat{r}_0$ is the magnitude of the signal, and θ is the initial angle. Based on the modulation law, it is found that:

$$v_c(t_{i-1} + T_{on(i-1)}) - s_e T_{on(i-1)} - s_f(T_{sw} - T_{on(i-1)}) = v_c(t_i + T_{on(i)}) - (s_n + s_e)T_{on(i)} \quad (A.1)$$

where, $T_{on(i)}$ is the i_{th} cycle on-time, $s_n = R_i(V_{in} - V_o)/L_s$, $s_f = R_i V_o / L_s$, s_e is the amplitude of the external ramp, L_s is the inductance of the inductor, and R_i is the current sensing gain.

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Assuming $T_{on(i)} = T_{on} + \Delta T_{on(i)}$, where T_{on} is the steady-state on-time and $\Delta T_{on(i)}$ is the i_{th} cycle on-time perturbation, t_i can be calculated as: $t_i = (i-1)T_{sw}$.

Based on (A.1) , it is found that:

$$(s_n + s_e)\Delta T_{on(i)} + (s_f - s_e)\Delta T_{on(i-1)} = v_c(t_i + T_{on(i)}) - v_c(t_{i-1} + T_{on(i-1)}) \tag{A.2}$$

Hence, $\Delta T_{on(i)}$ can be calculated as:

$$\begin{aligned}
(s_n + s_e)\Delta T_{on(i)} &+ (s_f - s_e)\Delta T_{on(i-1)} = v_c(t_i + T_{on(i)}) - v_c(t_{i-1} + T_{on(i-1)}) \\
&= \hat{r}\sin[2\pi f_m \cdot (t_i + T_{on(i)}) - \theta] - \hat{r}\sin[2\pi f_m \cdot (t_{i-1} + T_{on(i-1)}) - \theta] \\
&= \hat{r}2\cos[\pi f_m(t_i + T_{on(i)} + t_{i-1} + T_{on(i-1)}) - \theta]\sin\pi f_m(t_i + T_{on(i)} - t_{i-1} - T_{on(i-1)}) \\
&\approx \hat{r}2\cos[\pi f_m[(2i - 3)T_{sw} + 2T_{on}] - \theta]\sin\pi f_m T_{sw}
\end{aligned} \tag{A.3}$$

The duty cycle d(t) can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M}[u(t_i) - u(t_i - T_{on(i)})] \tag{A.4}$$

where u(t)=1, when t>0, and i_{L0} is the initial value of the inductor current.

Then, Fourier analysis can be performed on the duty cycle:

$$\begin{aligned}
c_{m(d)} &= \frac{j2f_m}{N}\sum_{i=1}^{M}\int_{t_i}^{t_i+T_{on(i)}} d(t) \cdot e^{-j2\pi f_m t}\,dt = \frac{j2\pi f_m}{N\pi}\sum_{i=1}^{M}\int_{t_i}^{t_i+T_{on(i)}} e^{-j2\pi f_m t}\,dt \\
&= \frac{1}{N\pi}\sum_{i=1}^{M}(e^{-j2\pi f_m(t_i)} - e^{-j2\pi f_m(t_i+T_{on(i)})}) \\
&= \frac{1}{N\pi}\sum_{i=1}^{M}(e^{-j2\pi f_m(i-1)T_{sw}} - e^{-j2\pi f_m[(i-1)T_{sw}+T_{on}+\Delta T_{on(i)}]}) \\
&= \frac{1}{N\pi}\sum_{i=1}^{M}[e^{-j2\pi f_m[(i-1)T_{sw}]}(1 - e^{-j2\pi f_m(T_{on}+\Delta T_{on(i)})})] \\
&= \frac{1}{N\pi}\sum_{i=1}^{M}[e^{-j2\pi f_m[(i-1)T_{sw}]}(1 - e^{-j2\pi f_m T_{on}}(1 - j2\pi f_m \Delta T_{on(i)}))] \\
&= \frac{j2\pi f_m}{N\pi}e^{-j2\pi f_m T_{on}}\sum_{i=1}^{M}(e^{-j2\pi f_m[(i-1)T_{sw}]}\Delta T_{on(i)})
\end{aligned} \tag{A.5}$$

where $c_{m(d)}$ is the Fourier coefficient of the duty cycle at perturbation frequency f_m.

The inductor current $i_L(t)$ can be expressed by:

$$i_L(t)\big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \int_0^t [\frac{V_{in}}{L_s}d(t)\big|_{0\le t\le t_M+T_{off(M)}+T_{on}} - \frac{V_o}{L_s}]dt + i_{L0} \tag{A.6}$$

Then, Fourier analysis can be performed on the inductor current:

$$c_m = \frac{j2f_m}{N}\sum_{i=1}^{M}\int_{t_i}^{t_i+T_{on(i)}} i_L(t)\cdot e^{-j2\pi f_m t}dt = \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\sum_{i=1}^{M}(e^{-j2\pi f_m[(i-1)T_{sw}]}\Delta T_{on(i)}) \tag{A.7}$$

where c_m is the Fourier coefficient of the inductor current at perturbation frequency f_m.

Based on (A.3) and (A.7), it is found that:

$$(s_n+s_e)c_m + (s_f-s_e)c_m e^{-j2\pi f_m T_{sw}}$$

$$= \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\sum_{i=1}^{M}(e^{-j2\pi f_m[(i-1)T_{sw}]}\cdot(\hat{r}2\cos[\pi f_m[(2i-3)T_{sw}+2T_{on}]-\theta]\sin\pi f_m T_{sw})$$

$$= \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\hat{r}\sin\pi f_m T_{sw}\sum_{i=1}^{M}(e^{-j2\pi f_m[(i-1)T_{sw}]}(e^{j2\pi f_m[(i-\frac{3}{2})T_{sw}+T_{on}]}e^{-j\theta}+e^{-j2\pi f_m[(i-\frac{3}{2})T_{sw}+T_{on}]}e^{j\theta}))$$

$$= \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\hat{r}\sin\pi f_m T_{sw}\sum_{i=1}^{M}(e^{j2\pi f_m(-\frac{1}{2}T_{sw}+T_{on})}e^{-j\theta}+e^{-j2\pi f_m[(2i-\frac{5}{2})T_{sw}+T_{on}]}e^{j\theta})$$

$$= \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\hat{r}\sin\pi f_m T_{sw}(M\cdot e^{j2\pi f_m(-\frac{1}{2}T_{sw}+T_{on})}e^{-j\theta}+e^{-j2\pi f_m(-\frac{5}{2}T_{sw}+T_{on})}\sum_{i=1}^{M}e^{-j4i\pi f_m T_{sw}}e^{j\theta}) \tag{A.8}$$

$$= \frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{on}}\hat{r}\sin\pi f_m T_{sw}(M\cdot e^{j2\pi f_m(-\frac{1}{2}T_{sw}+T_{on})}e^{-j\theta}+0)$$

$$= \hat{r}\frac{V_{in}}{L_s\cdot j2\pi f_m}j2f_s\sin\pi f_m T_{sw}\cdot e^{j2\pi f_m(-\frac{1}{2}T_{sw})}e^{-j\theta}$$

$$= \hat{r}\frac{V_{in}}{L_s\cdot j2\pi f_m}f_s(e^{j\pi f_m T_{sw}}-e^{-j\pi f_m T_{sw}})\cdot e^{-j\pi f_m T_{sw}}e^{-j\theta} = \hat{r}\frac{V_{in}}{L_s\cdot j2\pi f_m}f_s(1-e^{-j2\pi f_m T_{sw}})e^{-j\theta}$$

So, c_m can be found out as:

$$c_m = \hat{r}\cdot e^{-j\theta}\cdot\frac{f_s(1-e^{-j2\pi f_m T_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-j2\pi f_m T_{sw}}}\frac{V_{in}}{L_s\cdot j2\pi f_m} \tag{A.9}$$

The Fourier coefficient at perturbation frequency f_m for the control signal $v_c(t)$ is $\hat{r}\cdot e^{-j\theta}$, so the describing function from control-to-inductor current can be calculated as:

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}}\frac{V_{in}}{L_s s} \tag{A.10}$$

(b) Input voltage to inductor current transfer function

In order to consider the variation of the inductor current slopes, similar methodology is used to derive the feed forward gain that represents the influence from the input voltage v_{in}, as shown in Figure A.2.
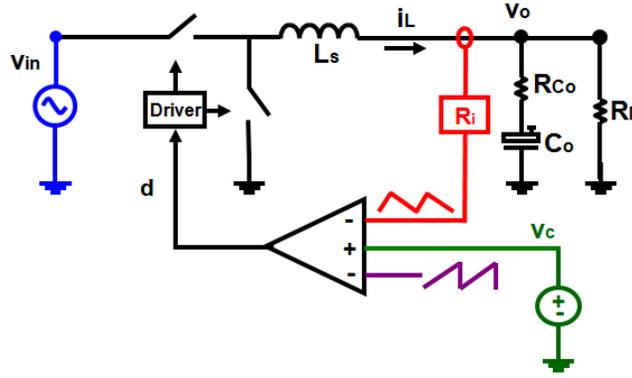
Figure A.2. Modeling for the influence of the input voltage v_{in} in peak current-mode control

Because the switching cycle T_{sw} is fixed, the on-time T_{on} and the off-time T_{off} is modulated by the perturbation signal $v_{in}(t)$: $v_{in}(t) = V_{in} + \hat{r}\sin(2\pi f_m \cdot t - \theta)$, where, V_{in} is the steady state value of the input voltage, $\hat{r}_0$ is the magnitude of the signal, and θ is the initial angle. Based on the modulation law, it is found that:

$$s_e T_{on(i-1)} + \int_{t_{i-1}+T_{on(i-1)}}^{t_i} \frac{V_o}{L_s} R_i \cdot dt = \int_{t_i}^{t_i+T_{on(i)}} \frac{v_{in}(t)-V_o}{L_s} R_i \cdot dt + s_e T_{on(i)} \qquad (A.11)$$

Then, $\Delta T_{on(i)}$ can be calculated as:

$$(s_n + s_e)\Delta T_{on(i)} + (s_f - s_e)\Delta T_{on(i-1)} - [(s_n + s_e)\Delta T_{on(i-1)} + (s_f - s_e)\Delta T_{on(i-2)}]$$

$$= \frac{v_{in}(t_i + T_{on(i)} + \frac{\pi}{2\pi f_m \cdot 2}) - v_{in}(t_{i-1} + T_{on(i-1)} + \frac{\pi}{2\pi f_m \cdot 2})}{2\pi f_m \cdot L_s / R_i} - \qquad (A.12)$$

$$\frac{[v_{in}(t_i + \frac{\pi}{2\pi f_m \cdot 2}) - v_{in}(t_{i-1} + \frac{\pi}{2\pi f_m \cdot 2})]}{2\pi f_m \cdot L_s / R_i}$$

The perturbed duty cycle $d(t)$ and the perturbed inductor current $i_L(t)$ can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M} [u(t_i) - u(t_i - T_{on(i)})] \tag{A.13}$$

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \int_0^t \left\{ \frac{V_{in}}{L_s} d(t) + \frac{\hat{r}\sin(2\pi f_m \cdot t - \theta)}{L_s} d(t) - \frac{V_o}{L_s} \right\} \cdot dt + i_{L0} \tag{A.14}$$

Then, Fourier analysis can be performed on the inductor current:

$$
\begin{aligned}
c_m &= \frac{j2f_m}{N} \sum_{i=1}^{M} \int_{t_i}^{t_i + T_{on(i)}} i_L(t) \cdot e^{-j2\pi f_m t} dt \\
&= \frac{1}{L_s \cdot j2\pi f_m} [V_{in} \frac{j2\pi f_m}{N\pi} e^{-j2\pi f_m T_{on}} \sum_{i=1}^{M} (e^{-j2\pi f_m [(i-1)T_{sw}]} \Delta T_{on(i)}) + D]
\end{aligned}
\tag{A.15}
$$

Finally, the transfer function in the s-domain can be expressed as:

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s}{(s_n + s_e) + (s_f - s_e)e^{-sT_{sw}}} \frac{(1 - e^{-sT_{on}})}{s \cdot L_s / R_i} \cdot V_{in} + D] \tag{A.16}$$

(c) Output voltage to inductor current transfer function

Similar methodology is used to derive the feedback gain that represents the influence from the output voltage v$_o$, as shown in Figure A.3.
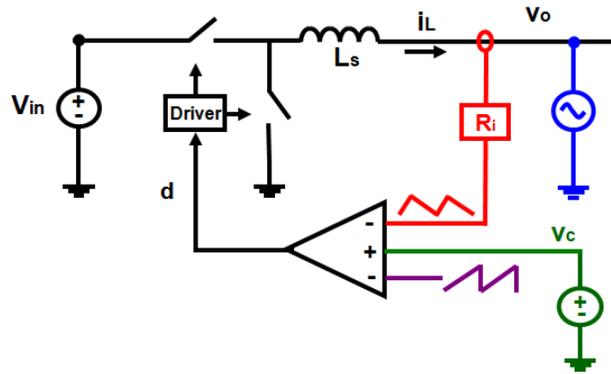
Figure A.3. Modeling for the influence of the output voltage v$_o$ in peak current-mode control

Because the switching cycle T$_{sw}$ is fixed, the on-time T$_{on}$ and the off-time T$_{off}$ is modulated by the perturbation signal v$_o$(t): $v_o(t) = V_o + \hat{r}\sin(2\pi f_m \cdot t - \theta)$, where, V$_o$ is the

steady state value of the input voltage, $\hat{r}_0$ is the magnitude of the signal, and θ is the initial angle. Based on the modulation law, it is found that:

$$s_e T_{on(i-1)} + \int_{t_{i-1}+T_{on(i-1)}}^{t_i} \frac{v_o(t)}{L_s} R_i \cdot dt = \int_{t_i}^{t_i+T_{on(i)}} \frac{V_{in}-v_o(t)}{L_s} R_i \cdot dt + s_e T_{on(i)} \qquad (A.17)$$

Then, $\Delta T_{on(i)}$ can be calculated as:

$$(s_n + s_e)\Delta T_{on(i)} + (s_f - s_e)\Delta T_{on(i-1)} =$$
$$-\frac{v_o(t_i + T_{on(i)} + \frac{\pi}{2\pi f_m \cdot 2}) - v_o(t_{i-1} + T_{on(i-1)} + \frac{\pi}{2\pi f_m \cdot 2})}{2\pi f_m \cdot L_s / R_i} \qquad (A.18)$$

The perturbed duty cycle d(t) and the perturbed inductor current i_L(t) can be expressed by:

$$d(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \sum_{i=1}^{M}[u(t_i)-u(t_i-T_{on(i)})] \qquad (A.19)$$

$$i_L(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \int_0^t \left\{\frac{V_{in}}{L_s}d(t) - \frac{V_o}{L_s} - \frac{\hat{r}\sin(2\pi f_m \cdot t - \theta)}{L_s}\right\} \cdot dt + i_{L0} \qquad (A.20)$$

Then, the Fourier analysis can be performed on the inductor current:

$$c_m = \frac{j2f_m}{N}\sum_{i=1}^{M}\int_{t_i}^{t_i+T_{on(i)}} i_L(t)\cdot e^{-j2\pi f_m t}dt$$
$$= \frac{1}{L_s \cdot j2\pi f_m}[V_{in}\frac{j2\pi f_m}{N\pi}e^{-j2\pi f_m T_{on}}\sum_{i=1}^{M}(e^{-j2\pi f_m[(i-1)T_{sw}]}\Delta T_{on(i)}) - 1] \qquad (A.21)$$

Finally, the transfer function in the s-domain can be expressed as:

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s}\cdot[\frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}\cdot V_{in} - 1] \qquad (A.22)$$

A.2 Derivation for Constant On-time Control

(a) Control-to-inductor current transfer function

As shown in Figure A.4, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the control signal v_c; then, based on the perturbed inductor current waveform, the describing function from the control signal v_c to the inductor current i_L can be found by mathematical derivation.
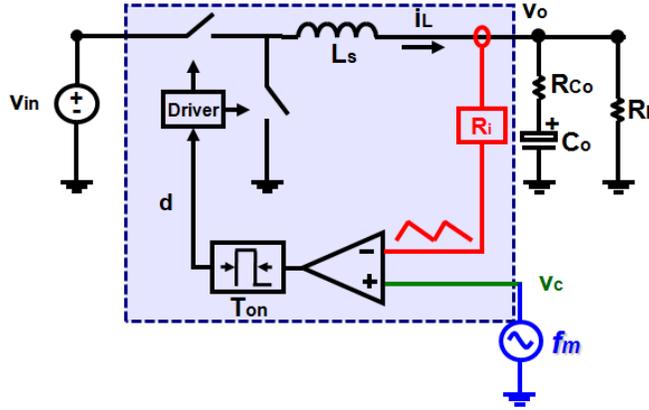
Figure A.4. Modeling for the influence of the control signal v_c in constant on-time control

Because the on-time is fixed, the off-time is modulated by the perturbation signal v_c(t): $v_c(t) = r_0 + \hat{r}\sin(2\pi f_m \cdot t - \theta)$. Based on the modulation law, it is found that:

$$v_c(t_{i-1} + T_{off(i-1)}) + s_n T_{on} = v_c(t_i + T_{off(i)}) + s_f T_{off(i)} \tag{A.23}$$

where, $T_{off(i)}$ is the i_{th} cycle off-time. Assuming $T_{off(i)} = T_{off} + \Delta T_{off(i)}$, where T_{off} is the steady-state off-time and $\Delta T_{off(i)}$ is the i_{th} cycle off-time perturbation, t_i can be calculated as: $t_i = (i-1)(T_{on} + T_{off}) + \sum_{k=1}^{i-1} \Delta T_{off(k)}$. Based on (A.23), it is found that:

$$s_f \Delta T_{off(i)} = v_c(t_{i-1} + T_{off(i-1)}) - v_c(t_i + T_{off(i)}) \tag{A.24}$$

Hence, $\Delta T_{off(i)}$ can be calculated as:

$$\Delta T_{off(i)} = \frac{1}{s_f} \hat{r} \{\sin[2\pi f_m \cdot (t_{i-1} + T_{off(i-1)}) - \theta] - \sin[2\pi f_m \cdot (t_i + T_{off(i)}) - \theta]\}$$

$$\approx -\frac{1}{s_f} \hat{r} \cdot 2\cos[\pi f_m \cdot (t_{i-1} + t_i + 2T_{off}) - \theta] \cdot \sin(\pi f_m \cdot T_{sw}) \qquad (A.25)$$

$$\approx -2\frac{\hat{r}}{s_f} \sin[\pi f_m \cdot (T_{on} + T_{off})] \cdot \cos[2\pi f_m [(i-1)(T_{on} + T_{off}) - \frac{T_{on} - T_{off}}{2}]$$

The perturbed duty cycle d(t) can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M} [u(t - t_i - T_{off(i)}) - u(t - t_i - T_{off(i)} - T_{on})] \qquad (A.26)$$

Then, Fourier analysis can be performed on the duty cycle:

$$c_{m(d)} = \frac{j2\pi f_m}{N\pi} \sum_{i=1}^{M} \int_{t_i + T_{off(i)}}^{t_i + T_{off(i)} + T_{on}} e^{-j2\pi f_m t} dt$$

$$= \frac{1}{N\pi} \sum_{i=1}^{M} (e^{-j2\pi f_m(t_i + T_{off(i)})} - e^{-j2\pi f_m(t_i + T_{off(i)} + T_{on})})$$

$$= \frac{1}{N\pi} \sum_{i=1}^{M} e^{-j2\pi f_m(t_i + T_{off(i)})} (1 - e^{-j2\pi f_m T_{on}})$$

$$= \frac{1}{N\pi} (1 - e^{-j2\pi f_m T_{on}}) \sum_{i=1}^{M} (e^{-j2\pi f_m[(i-1)T_{sw} + T_{off}]} \cdot e^{-j2\pi f_m \sum_{k=1}^{i} \Delta T_{off(k)}}) \qquad (A.27)$$

$$\approx \frac{1}{N\pi} e^{-j2\pi f_m T_{off}} (1 - e^{-j2\pi f_m T_{on}}) \sum_{i=1}^{M} [e^{-j2\pi f_m[(i-1)T_{sw}]} (1 - j2\pi f_m \sum_{k=1}^{i} \Delta T_{off(k)})]$$

$$= -\frac{j2\pi f_m}{N\pi} e^{-j2\pi f_m T_{off}} (1 - e^{-j2\pi f_m T_{on}}) \sum_{i=1}^{M} [e^{-j2\pi f_m[(i-1)T_{sw}]} \cdot \sum_{k=1}^{i} \Delta T_{off(k)})]$$

The inductor current $i_L(t)$ can be expressed by:

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \int_0^t [\frac{V_{in}}{L_s} d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} - \frac{V_o}{L_s}] dt + i_{L0} \qquad (A.28)$$

Then, Fourier analysis can be performed on the inductor current:

$$c_m = j\frac{2f_m}{N} \int_0^{t_M + T_{off(M)} + T_{on}} i_L(t) \cdot e^{-j2\pi f_m t} dt$$

$$= -\frac{1}{N\pi} \frac{V_{in}}{L_s} e^{-j2\pi f_m T_{off}} (1 - e^{-j2\pi f_m T_{on}}) [\sum_{i=1}^{M} (e^{-j2\pi f_m(i-1)T_{sw}} \sum_{k=1}^{i} \Delta T_{off(k)})] \qquad (A.29)$$

where c_m is the Fourier coefficient of the inductor current at perturbation frequency f_m.

Based on (A.25) and (A.29), it is found that:

$$c_m = -\frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{off}}(1-e^{-j2\pi f_m T_{on}})\cdot\{-2\frac{\hat{r}}{s_f}\sin[\pi f_m \cdot T_{sw}]\}\cdot$$

$$\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot\sum_{k=1}^{i}\cos[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]\}$$

$$=-\frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{off}}(1-e^{-j2\pi f_m T_{on}})\cdot\{-2\frac{\hat{r}}{s_f}\sin[\pi f_m \cdot T_{sw}]\}\cdot$$

$$\frac{1}{2}\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot\sum_{k=1}^{i}\{e^{j[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]}+e^{-j[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]}\}\} \qquad (A.30)$$

$$=\frac{1}{N\pi}\frac{V_{in}}{L_s}e^{-j2\pi f_m T_{off}}(1-e^{-j2\pi f_m T_{on}})\cdot\{2\frac{\hat{r}}{s_f}\sin[\pi f_m \cdot T_{sw}]\}\cdot$$

$$\frac{1}{2}\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot\{\sum_{k=1}^{i}e^{j[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]}+\sum_{k=1}^{i}e^{-j[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]}\}\}$$

$$\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot\{\sum_{k=1}^{i}e^{j[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]}\}\}$$

$$=e^{-j\theta}\cdot e^{-j2\pi f_m\frac{T_{on}-T_{off}}{2}}\cdot\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot[\sum_{k=1}^{i}e^{j2\pi f_m(k-1)T_{sw}}]\}$$

$$=e^{-j\theta}\cdot e^{-j2\pi f_m\frac{T_{on}-T_{off}}{2}}\cdot\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot\frac{1-e^{j2\pi f_m iT_{sw}}}{1-e^{j2\pi f_m T_{sw}}}\} \qquad (A.31)$$

$$=e^{-j\theta}\cdot\frac{e^{-j2\pi f_m\frac{T_{on}-T_{off}}{2}}}{1-e^{j2\pi f_m T_{sw}}}\cdot\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}-e^{j2\pi f_m T_{sw}}\}=e^{-j\theta}\cdot\frac{e^{-j2\pi f_m\frac{T_{on}-T_{off}}{2}}}{1-e^{-j2\pi f_m T_{sw}}}\cdot M$$

$$\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot\{\sum_{k=1}^{i}e^{-j[2\pi f_m[(k-1)T_{sw}-\frac{T_{on}-T_{off}}{2}]-\theta]}\}\}$$

$$=e^{j\theta}\cdot e^{j2\pi f_m\frac{T_{on}-T_{off}}{2}}\cdot\sum_{i=1}^{M}\{e^{-j2\pi f_m(i-1)T_{sw}}\cdot[\sum_{k=1}^{i}e^{-j2\pi f_m(k-1)T_{sw}}]\}$$

$$=e^{j\theta}\cdot e^{j2\pi f_m\frac{T_{on}-T_{off}}{2}}\sum_{i=1}^{M}[e^{-j2\pi f_m(i-1)T_{sw}}\cdot\frac{1-e^{-j2\pi f_m iT_{sw}}}{1-e^{-j2\pi f_m T_{sw}}}] \qquad (A.32)$$

$$=e^{j\theta}\cdot\frac{e^{j2\pi f_m\frac{T_{on}-T_{off}}{2}\cdot}}{1-e^{-j2\pi f_m T_{sw}}}\sum_{i=1}^{M}[e^{-j2\pi f_m(i-1)T_{sw}}\cdot(1-e^{-j2\pi f_m iT_{sw}})]$$

$$=e^{j\theta}\cdot\frac{e^{j2\pi f_m\frac{T_{on}-T_{off}}{2}\cdot}}{1-e^{-j2\pi f_m T_{sw}}}\sum_{i=1}^{M}(e^{-j2\pi f_m(i-1)T_{sw}}-e^{-j2\pi f_m(2i-1)T_{sw}})=0$$

Finally, it can be found that:

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$$c_m = \frac{1}{2} \frac{1}{N\pi} \frac{V_{in}}{L_s} e^{-j2\pi f_m T_{off}} (1 - e^{-j2\pi f_m T_{on}}) \cdot \{2\frac{\hat{r}}{s_f} \sin(\pi f_m \cdot T_{sw})\} \cdot e^{-j\theta} \cdot \frac{e^{-j2\pi f_m \frac{T_{on}-T_{off}}{2}}}{1 - e^{-j2\pi f_m T_{sw}}} \cdot M$$

$$= \frac{V_{in}}{L_s \cdot j2\pi f_m} \frac{j2\pi f_m M}{N\pi} \frac{\hat{r}}{s_f} \sin(\pi f_m \cdot T_{sw}) \cdot e^{-j\theta} \cdot \frac{e^{-j2\pi f_m \frac{T_{sw}}{2}}(1 - e^{-j2\pi f_m T_{on}})}{1 - e^{-j2\pi f_m T_{sw}}}$$

$$= \frac{V_{in}}{L_s \cdot j2\pi f_m} j2f_s \frac{\hat{r}}{s_f} \sin(\pi f_m \cdot T_{sw}) \cdot e^{-j\theta} \cdot \frac{(1 - e^{-j2\pi f_m T_{on}})}{e^{j\pi f_m T_{sw}} - e^{-j\pi f_m T_{sw}}} \qquad \text{(A.33)}$$

$$= \frac{V_{in}}{L_s \cdot j2\pi f_m} j2f_s \frac{\hat{r}}{s_f} \sin(\pi f_m \cdot T_{sw}) \cdot e^{-j\theta} \cdot \frac{(e^{-j2\pi f_m T_{on}} - 1)}{2j \sin(\pi f_m T_{sw})}$$

$$= \frac{V_{in}}{L_s \cdot j2\pi f_m} \hat{r} \frac{f_s}{s_f} (1 - e^{-j2\pi f_m T_{on}}) e^{-j\theta}$$

The Fourier coefficient at perturbation frequency f_m for the control signal $v_c(t)$ is $\hat{r} \cdot e^{-j\theta}$, so the transfer function from control to inductor current can be calculated as:

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s}{s_f}(1 - e^{-sT_{on}})\frac{V_{in}}{L_s s} \qquad \text{(A.34)}$$

(b) Input voltage to inductor current transfer function

Similar methodology is used in the constant on-time control, as shown in Figure A.5.
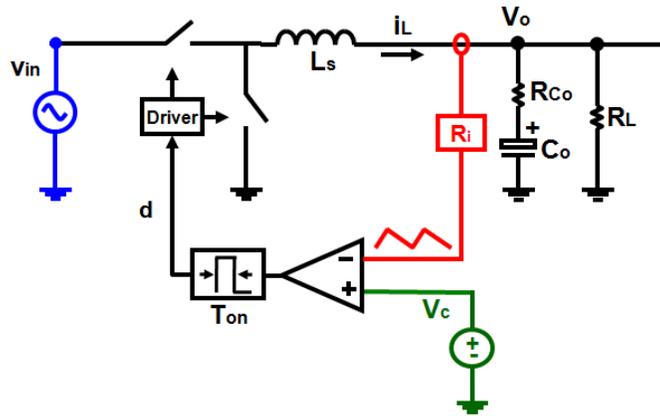
Figure A.5. Modeling for the influence of the input voltage v_{in} in constant on-time control

Because the on-time T_{on} is fixed, the off-time T_{off} is modulated by the perturbation signal $v_{in}(t)$: $v_{in}(t) = V_{in} + \hat{r}\sin(2\pi f_m \cdot t - \theta)$. Based on the modulation law, it is found that:

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$$\int_{t_{i-1}+T_{off(i-1)}}^{t_i} \frac{v_{in}(t)-V_o}{L_s} R_i \cdot dt = \int_{t_i}^{t_i+T_{off(i)}} \frac{V_o}{L_s} R_i \cdot dt \tag{A.35}$$

Then, $\Delta T_{on(i)}$ can be calculated as:

$$
\begin{aligned}
&s_f \Delta T_{off(i)} - s_f \Delta T_{off(i+1)} \\
&= \frac{v_{in}(t_{i-1}+T_{off(i-1)}+\frac{\pi}{2\pi f_m \cdot 2})-v_{in}(t_i+T_{off(i)}+\frac{\pi}{2\pi f_m \cdot 2})}{2\pi f_m \cdot L_s / R_i} - \\
&\quad \frac{[v_{in}(t_i+\frac{\pi}{2\pi f_m \cdot 2})-v_{in}(t_{i+1}+\frac{\pi}{2\pi f_m \cdot 2})]}{2\pi f_m \cdot L_s / R_i}
\end{aligned}
\tag{A.36}
$$

The perturbed duty cycle $d(t)$ and the perturbed inductor current $i_L(t)$ can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)}+T_{on}} = \sum_{i=1}^{M} [u(t_i)-u(t_i-T_{on(i)})] \tag{A.37}$$

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)}+T_{on}} = \int_0^t \left\{ \frac{V_{in}}{L_s}d(t) + \frac{\hat{r}\sin(2\pi f_m \cdot t - \theta)}{L_s}d(t) - \frac{V_o}{L_s} \right\} \cdot dt + i_{L0} \tag{A.38}$$

Then, the Fourier analysis can be performed on the inductor current:

$$
\begin{aligned}
c_m &= \frac{j2f_m}{N} \sum_{i=1}^{M} \int_{t_i}^{t_i+T_{on(i)}} i_L(t) \cdot e^{-j2\pi f_m t} dt \\
&= \frac{1}{L_s \cdot j2\pi f_m}[V_{in}[-\frac{j2\pi f_m}{N\pi}e^{-j2\pi f_m T_{off}}(1-e^{-j2\pi f_m T_{on}})\sum_{i=1}^{M}[e^{-j2\pi f_m[(i-1)T_{sw}]} \cdot \sum_{k=1}^{i}\Delta T_{off(k)})]]+D]
\end{aligned}
\tag{A.39}
$$

Finally, the transfer function in the s-domain can be expressed as:

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[\frac{1-e^{-sT_{on}}}{1-e^{sT_{sw}}} \frac{f_s}{s_f} \frac{-(1-e^{sT_{on}})}{s \cdot L_s / R_i} \cdot V_{in}+D] \tag{A.40}$$

(c) Output voltage to inductor current transfer function

Similar methodology is used to derive the feedback gain that represents the influence from the output voltage v_o, as shown in Figure A.6.

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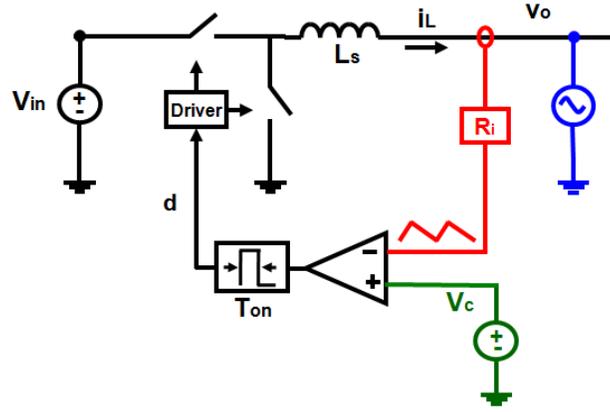
Figure A.6. Modeling for the influence of the output voltage v$_o$ in constant on-time control

Because the switching cycle T$_{sw}$ is fixed, the on-time T$_{on}$ and the off-time T$_{off}$ is modulated by the perturbation signal v$_o$(t): $v_o(t) = V_o + \hat{r}\sin(2\pi f_m \cdot t - \theta)$, where, V$_o$ is the steady state value of the input voltage, $\hat{r}_0$ is the magnitude of the signal, and θ is the initial angle. Based on the modulation law, it is found that:

$$s_e T_{off(i-1)} + \int_{t_{i-1}+T_{off(i-1)}}^{t_i} \frac{V_{in} - v_o(t)}{L_s} R_i \cdot dt = \int_{t_i}^{t_i+T_{off(i)}} \frac{v_o(t)}{L_s} R_i \cdot dt + s_e T_{off(i)} \qquad (A.41)$$

Then, $\Delta T_{on(i)}$ can be calculated as:

$$s_f \Delta T_{off(i)} = -\frac{v_o(t_{i-1} + T_{off(i-1)} + \frac{\pi}{2\pi f_m \cdot 2}) - v_o(t_i + T_{off(i)} + \frac{\pi}{2\pi f_m \cdot 2})}{2\pi f_m \cdot L_s / R_i} \qquad (A.42)$$

The perturbed duty cycle d(t) and the perturbed inductor current i$_L$(t) can be expressed by:

$$d(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^{M} [u(t_i) - u(t_i - T_{on(i)})] \qquad (A.43)$$

$$i_L(t)\Big|_{0 \le t \le t_M + T_{off(M)} + T_{on}} = \int_0^t \left\{ \frac{V_{in}}{L_s} d(t) - \frac{V_o}{L_s} - \frac{\hat{r}\sin(2\pi f_m \cdot t - \theta)}{L_s} \right\} \cdot dt + i_{L0} \qquad (A.44)$$

Then, the Fourier analysis can be performed on the inductor current:

$$c_m = \frac{j2f_m}{N} \sum_{i=1}^{M} \int_{t_i}^{t_i + T_{on(i)}} i_L(t) \cdot e^{-j2\pi f_m t} dt$$

$$= \frac{1}{L_s \cdot j2\pi f_m} [V_{in}[-\frac{j2\pi f_m}{N\pi} e^{-j2\pi f_m T_{off}} (1 - e^{-j2\pi f_m T_{on}}) \sum_{i=1}^{M} [e^{-j2\pi f_m[(i-1)T_{sw}]} \cdot \sum_{k=1}^{i} \Delta T_{off(k)})] - 1]$$

(A.45)

Finally, the transfer function in the s-domain can be expressed as:

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{L_s s} \cdot [\frac{f_s(1 - e^{-sT_{on}})}{s_f} \cdot \frac{1}{s \cdot L_s / R_i} \cdot V_{in} - 1]$$

(A.46)

Appendix B. Model for Boost and Buck-Boost converters with Current-Mode Control

The general model for boost and buck-boost converters with current-mode control is shown in Figure B.1, where $DF = i_p(s)/v_c(s)$, $k_1(s) = [i_p(s)/v_{in}(s)]/[i_p(s)/v_c(s)]$, $k_2(s) = [i_p(s)/v_o(s)]/[i_p(s)/v_c(s)]$, and i_p is the diode current.
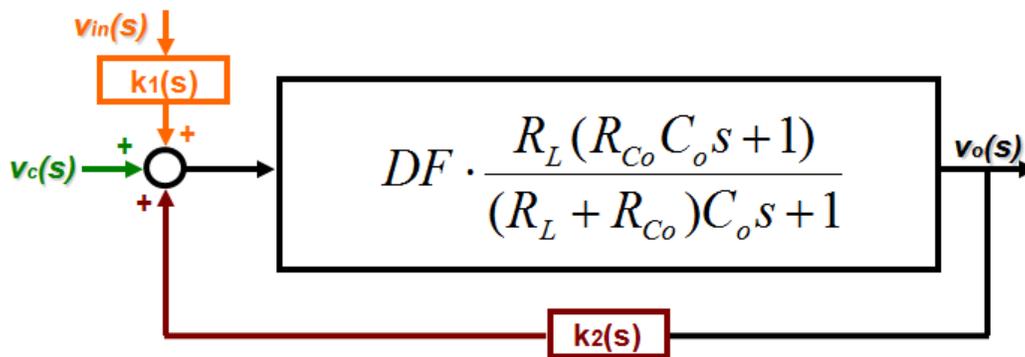
Figure B.1. General model for boost and buck-boost converters with current-mode control

A boost converter with current-mode control is shown in Figure B.3.
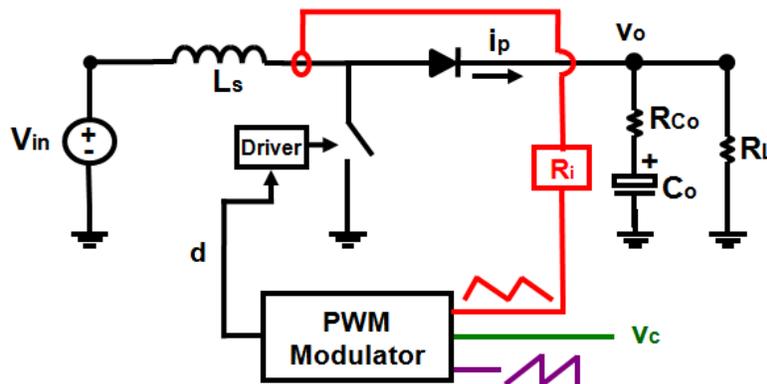
Figure B.2. A boost converter with current-mode control

The model results are as follows.

Table B.1. Model for boost converters with constant on-time control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\frac{V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}V_o+1]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\cdot\frac{(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{V_o}{L_s s}-\frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\cdot\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]+\frac{(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_e e^{-sT_{sw}}}\cdot\frac{(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i}\cdot\frac{1}{(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2})}(1-D)\cdot[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{on}R_i}{2L_s}+\frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -\frac{V_o R_i}{V_{in}R_L}$$

where $\omega_1 = \frac{\pi}{T_{on}}$, $Q_1 = \frac{2}{\pi}$, $D = \frac{V_o-V_{in}}{V_o}$, $s_n = R_i\frac{V_{in}}{L_s}$ and $s_f = R_i\frac{V_o-V_{in}}{L_s}$.

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Table B.2. Model for boost converters with constant off-time control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\frac{V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}V_o+1]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{e^{-sT_{on}}(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{V_o}{L_s s}-\frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]+\frac{(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{-1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{e^{-sT_{on}}(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i}\cdot\frac{1}{(1+\dfrac{s}{Q_1\omega_3}+\dfrac{s^2}{\omega_3^2})}(1-D)\cdot[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{off}R_i}{2L_s}+\frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -(\frac{T_{off}R_i}{2L_s}+\frac{V_o R_i}{V_{in} R_L})$$

where $\omega_3 = \dfrac{\pi}{T_{off}}$, $Q_1 = \dfrac{2}{\pi}$, $D = \dfrac{V_o-V_{in}}{V_o}$, $s_n = R_i\dfrac{V_{in}}{L_s}$ and $s_f = R_i\dfrac{V_o-V_{in}}{L_s}$.

Table B.3. Model for boost converters with peak current-mode control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \frac{V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{1}{s\cdot L_s/R_i} V_o + 1]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})} \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{(1-e^{sT_{off}})}{s\cdot L_s/R_i} \frac{V_o}{L_s s} - \frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \frac{V_o}{L_s s} \cdot \frac{(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{1}{s\cdot L_s/R_i} \frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]+\frac{(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})} \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{(1-e^{sT_{off}})}{s\cdot L_s/R_i} \frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i} \cdot \frac{1}{(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2})}(1-D)\cdot[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{sw}R_i(2V_{in}-V_o)}{2L_s V_o}+\frac{T_{sw}s_e}{V_o}+\frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -(\frac{T_{sw}V_{in}s_e}{V_o^2}+\frac{T_{sw}V_{in}^2 R_i}{2L_s V_o^2}+\frac{V_o R_i}{V_{in}R_L})$$

where $\omega_2 = \frac{\pi}{T_{sw}}$, $Q_2 = \frac{1}{\pi(\frac{s_n+s_e}{s_n+s_f}-0.5)}$, $D = \frac{V_o-V_{in}}{V_o}$, $s_n = R_i \frac{V_{in}}{L_s}$ and $s_f = R_i \frac{V_o-V_{in}}{L_s}$.

Table B.4. Model for boost converters with valley current-mode control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\frac{V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}V_o+1]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})}\frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{e^{sT_{on}}(1-e^{sT_{off}})}{s\cdot L_s/R_i}\frac{V_o}{L_s s}-\frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\frac{V_o}{L_s s}\cdot\frac{(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{1}{s\cdot L_s/R_i}\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]+\frac{(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})}\frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{e^{sT_{on}}(1-e^{sT_{off}})}{s\cdot L_s/R_i}\frac{V_o(1-D)}{L_s s}[1-\frac{L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i}\cdot\frac{1}{(1+\frac{s}{Q_2'\omega_2}+\frac{s^2}{\omega_2^2})}(1-D)\cdot[1-\frac{L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{sw}(V_o-2V_{in})R_i}{2L_sV_o}+\frac{T_{sw}s_e}{V_o}+\frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -(\frac{T_{sw}V_{in}s_e}{V_o^2}-\frac{T_{sw}V_{in}^2 R_i}{2L_sV_o^2}+\frac{V_o R_i}{V_{in}R_L})$$

where $\omega_2 = \frac{\pi}{T_{sw}}$, $Q_2' = \frac{1}{\pi(\frac{s_f+s_e}{s_n+s_f}-0.5)}$, $D = \frac{V_o-V_{in}}{V_o}$, $s_n = R_i\frac{V_{in}}{L_s}$ and $s_f = R_i\frac{V_o-V_{in}}{L_s}$.

A boost converter with current-mode control is shown in Figure B.3.
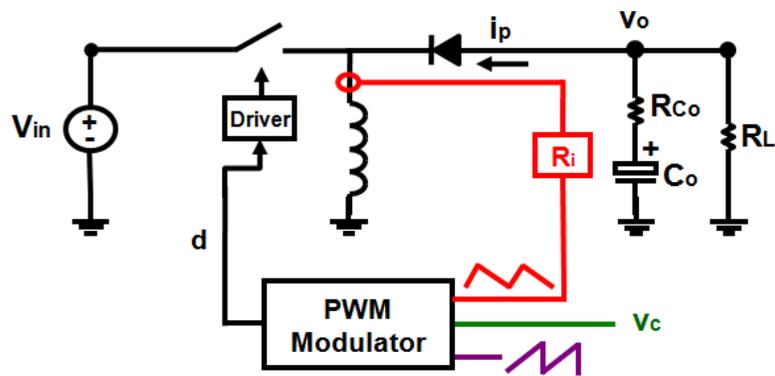
Figure B.3. A buck-boost converter with current-mode control

The model results are as follows.

Table B.5. Model for buck-boost converters with constant on-time control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_ee^{-sT_{sw}}}\frac{V_{in}+V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{on}})}{(1-e^{sT_{sw}})[(s_f+s_e)-s_ee^{-sT_{sw}}]}\frac{(1-e^{sT_{on}})}{s\cdot L_s/R_i}\cdot(V_{in}+V_o)+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_ee^{-sT_{sw}}}\cdot\frac{(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{V_{in}+V_o}{L_s s}-\frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_ee^{-sT_{sw}}}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s(1-e^{-sT_{on}})}{(1-e^{sT_{sw}})[(s_f+s_e)-s_ee^{-sT_{sw}}]}\frac{(1-e^{sT_{on}})}{s\cdot L_s/R_i}\cdot\frac{(V_{in}+V_o)(1-D)}{L_s s}\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]+\frac{D(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_f)-s_ee^{-sT_{sw}}}\cdot\frac{(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i}\cdot\frac{1}{(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2})}(1-D)\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{on}R_i}{2L_s}+\frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -\frac{V_o R_i}{V_{in} R_L}$$

where $\omega_1 = \frac{\pi}{T_{on}}$, $Q_1 = \frac{2}{\pi}$, $D = \frac{V_o}{V_{in}+V_o}$, $s_n = R_i\frac{V_{in}}{L_s}$ and $s_f = R_i\frac{V_o}{L_s}$.

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Table B.6. Model for buck-boost converters with constant off-time control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\frac{V_{in}+V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s(1-e^{-sT_{off}})}{(1-e^{sT_{sw}})[(s_n+s_e)-s_e e^{-sT_{sw}}]}\frac{e^{sT_{off}}(1-e^{sT_{on}})}{s\cdot L_s/R_i}\cdot(V_{in}+V_o)+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{on}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{e^{-sT_{on}}(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{V_{in}+V_o}{L_s s}-\frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s(1-e^{-sT_{off}})}{(1-e^{sT_{sw}})[(s_n+s_e)-s_e e^{-sT_{sw}}]}\frac{e^{sT_{off}}(1-e^{sT_{on}})}{s\cdot L_s/R_i}\cdot\frac{(V_{in}+V_o)(1-D)}{L_s s}\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]+\frac{D(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{-sT_{sw}})}\frac{f_s(1-e^{-sT_{off}})}{(s_e+s_n)-s_e e^{-sT_{sw}}}\cdot\frac{e^{-sT_{on}}(1-e^{-sT_{off}})}{s\cdot L_s/R_i}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i}\cdot\frac{1}{(1+\frac{s}{Q_1\omega_3}+\frac{s^2}{\omega_3^2})}(1-D)\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -(\frac{T_{off}R_i}{2L_s}+\frac{V_o R_i}{V_{in}R_L})$$

where $\omega_3 = \frac{\pi}{T_{off}}$, $Q_1 = \frac{2}{\pi}$, $D = \frac{V_o}{V_{in}+V_o}$, $s_n = R_i\frac{V_{in}}{L_s}$ and $s_f = R_i\frac{V_o}{L_s}$.

Table B.7. Model for buck-boost converters with peak current-mode control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \frac{V_{in}+V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{(1-e^{-sT_{on}})}{s \cdot L_s / R_i}(V_{in}+V_o)+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})} \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{(1-e^{sT_{off}})}{s \cdot L_s / R_i} \frac{V_{in}+V_o}{L_s s} - \frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D \cdot L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{(1-e^{-sT_{on}})}{s \cdot L_s / R_i} \cdot \frac{(V_{in}+V_o)(1-D)}{L_s s} \cdot [1-\frac{D \cdot L_s s}{R_L(1-D)^2}]+\frac{D(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})} \frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}} \cdot \frac{(1-e^{sT_{off}})}{s \cdot L_s / R_i} \frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D \cdot L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i} \cdot \frac{1}{(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2})}(1-D) \cdot [1-\frac{D \cdot L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{sw}V_o s_e}{(V_o+V_{in})^2} - \frac{T_{sw}R_i V_o^2}{2L_s(V_o+V_{in})^2} + \frac{V_o^2 R_i}{V_{in}^2 R_L}$$

$$k_2 \approx -(\frac{T_{sw}V_{in}s_e}{(V_o+V_{in})^2} + \frac{T_{sw}V_{in}^2 R_i}{2L_s(V_o+V_{in})^2} + \frac{V_o R_i}{V_{in} R_L})$$

where $\omega_2 = \frac{\pi}{T_{sw}}$, $Q_2 = \frac{1}{\pi(\frac{s_n+s_e}{s_n+s_f}-0.5)}$, $D = \frac{V_o}{V_{in}+V_o}$, $s_n = R_i \frac{V_{in}}{L_s}$ and $s_f = R_i \frac{V_o}{L_s}$.

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Table B.8. Model for buck-boost converters with valley current-mode control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\frac{V_{in}+V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[-\frac{f_s}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{(1-e^{-sT_{on}})}{s\cdot L_s/R_i}(V_{in}+V_o)+D]$$

$$\frac{i_L(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})}\frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{(1-e^{sT_{off}})}{s\cdot L_s/R_i}\frac{V_{in}+V_o}{L_s s}-\frac{1-D}{L_s s}$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = -\frac{f_s}{(s_f+s_e)+(s_n-s_e)e^{-sT_{sw}}}\cdot\frac{e^{-sT_{off}}(1-e^{-sT_{on}})}{s\cdot L_s/R_i}\cdot\frac{(V_{in}+V_o)(1-D)}{L_s s}\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]+\frac{D(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{1}{(1-e^{sT_{sw}})}\frac{f_s(1-e^{-sT_{sw}})}{(s_n+s_e)+(s_f-s_e)e^{-sT_{sw}}}\cdot\frac{e^{sT_{on}}(1-e^{sT_{off}})}{s\cdot L_s/R_i}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

$$DF = \frac{1}{R_i}\cdot\frac{1}{(1+\frac{s}{Q_2'\omega_2}+\frac{s^2}{\omega_2^2})}(1-D)\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$k_1 \approx \frac{T_{sw}V_o^2R_i}{2L_s(V_o+V_{in})^2}+\frac{T_{sw}V_os_e}{(V_o+V_{in})^2}+\frac{V_o^2R_i}{V_{in}^2R_L}$$

$$k_2 \approx -(\frac{T_{sw}V_{in}s_e}{(V_o+V_{in})^2}-\frac{T_{sw}V_{in}^2R_i}{2L_s(V_o+V_{in})^2}+\frac{V_oR_i}{V_{in}R_L})$$

where $\omega_2 = \frac{\pi}{T_{sw}}$, $Q_2' = \frac{1}{\pi(\frac{s_f+s_e}{s_n+s_f}-0.5)}$, $D = \frac{V_o}{V_{in}+V_o}$, $s_n = R_i\frac{V_{in}}{L_s}$ and $s_f = R_i\frac{V_o}{L_s}$.

Table B.9. Model for buck-boost converters with charge control

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(\dfrac{\dfrac{1}{2}s_nT_{on}+I_LR_i}{C_T}+s_e)+[\dfrac{(\dfrac{1}{2}s_n+s_f)T_{on}-I_LR_i}{C_T}-s_e]e^{-sT_{sw}}}\frac{V_{in}+V_o}{L_s s}$$

$$\frac{i_L(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(\dfrac{\dfrac{1}{2}s_nT_{on}+I_LR_i}{C_T}+s_e)+[\dfrac{(\dfrac{1}{2}s_n+s_f)T_{on}-I_LR_i}{C_T}-s_e]e^{-sT_{sw}}}\frac{V_{in}+V_o}{L_s s}$$

$$\frac{i_L(s)}{v_{in}(s)} = \frac{1}{L_s s}[\frac{f_s(1-e^{-sT_{sw}})(e^{-sT_{on}}-1)\dfrac{1}{s\cdot s\cdot L_s/R_i}-D(e^{-sT_{on}}-e^{-sT_{sw}})\dfrac{-1}{s\cdot L_s/R_i}}{(I_LR_i+\dfrac{s_nT_{on}}{2}+C_Ts_e)+[(s_n+s_f)T_{on}-I_LR_i-\dfrac{s_nT_{on}}{2}-C_Ts_e]e^{-sT_{sw}}}(V_{in}+V_o)+D]$$

$$\frac{i_p(s)}{v_c(s)} = \frac{f_s(1-e^{-sT_{sw}})}{(\dfrac{\dfrac{1}{2}s_nT_{on}+I_LR_i}{C_T}+s_e)+[\dfrac{(\dfrac{1}{2}s_n+s_f)T_{on}-I_LR_i}{C_T}-s_e]e^{-sT_{sw}}}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]$$

$$\frac{i_p(s)}{v_{in}(s)} = \frac{f_s(1-e^{-sT_{sw}})(e^{-sT_{on}}-1)\dfrac{1}{s\cdot s\cdot L_s/R_i}-D(e^{-sT_{on}}-e^{-sT_{sw}})\dfrac{-1}{s\cdot L_s/R_i}}{(I_LR_i+\dfrac{s_nT_{on}}{2}+C_Ts_e)+[(s_n+s_f)T_{on}-I_LR_i-\dfrac{s_nT_{on}}{2}-C_Ts_e]e^{-sT_{sw}}}\cdot\frac{(V_{in}+V_o)(1-D)}{L_s s}\cdot[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]+\frac{D(1-D)}{L_s s}$$

$$\frac{i_p(s)}{v_o(s)} = \frac{D(e^{-sT_{on}}-e^{-sT_{sw}})\dfrac{1}{s\cdot L_s/R_i}}{(I_LR_i+\dfrac{s_nT_{on}}{2}+C_Ts_e)+[(s_n+s_f)T_{on}-I_LR_i-\dfrac{s_nT_{on}}{2}-C_Ts_e]e^{-sT_{sw}}}\frac{(V_{in}+V_o)(1-D)}{L_s s}[1-\frac{D\cdot L_s s}{R_L(1-D)^2}]-\frac{(1-D)^2}{L_s s}$$

Appendix C. Derivation of the Equivalent Circuit Model

This appendix presents the process of obtaining the equivalent circuit model for current-mode control.

The complete model for peak current-mode control is shown in Figure B.2.
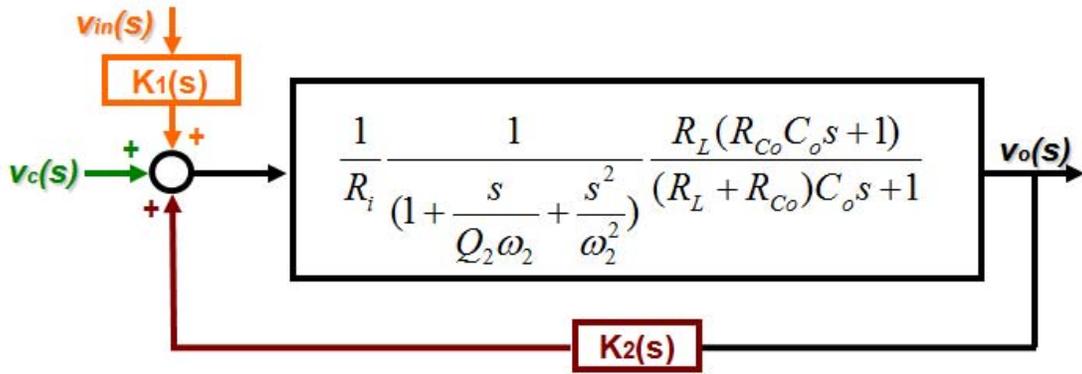
Figure C.1. Complete model for peak current-mode control

where,

$$k_1(s) \approx k_1 \approx \frac{DR_i}{L_s}[\frac{1}{Q_2\omega_2} - \frac{T_{off}}{2}] \tag{C.1}$$

$$k_2(s) \approx k_2 \approx -\frac{R_i}{L_s Q_2 \omega_2} \tag{C.2}$$

The control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} = \frac{\dfrac{1}{R_i}\dfrac{1}{1+\dfrac{s}{Q_2\omega_2}+\dfrac{s^2}{\omega_2^2}}\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{1-k_2\dfrac{1}{R_i}\dfrac{1}{1+\dfrac{s}{Q_2\omega_2}+\dfrac{s^2}{\omega_2^2}}\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.3}$$

Then, based on the equivalent transform, it is found that:

$$\frac{v_o(s)}{v_c(s)} = \frac{1}{R_i} \frac{\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{1+\dfrac{s}{Q_2\omega_2}+\dfrac{s^2}{\omega_2^2}+\dfrac{-k_2}{R_i}\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.4}$$

$$\frac{v_o(s)}{v_c(s)} = \frac{1}{R_i} \frac{\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{1+\dfrac{L_s s}{\dfrac{L_s}{\dfrac{1}{Q_2\omega_2}+\dfrac{s}{\omega_2^2}}}+\dfrac{-k_2}{R_i}\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.5}$$

Let $Z_e(s) = L_s /[1/(Q_2\omega_2)+s/\omega_2^2]$, then:

$$\frac{v_o(s)}{v_c(s)} = \frac{1}{R_i} \frac{\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{1+\dfrac{L_s s}{Z_e(s)}+\dfrac{-k_2}{R_i}\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.6}$$

$$v_o(s) = \frac{v_c(s)}{R_i} \frac{Z_e(s)\cdot\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{Z_e(s)+L_s s+\dfrac{Z_e(s)}{R_i/(-k_2)}\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.7}$$

$$v_o(s) = \frac{v_c(s)}{R_i} \frac{Z_e(s)\cdot\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{Z_e(s)+(\dfrac{Z_e(s)}{R_i/(-k_2)}-1)\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}+L_s s+\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.8}$$

Let $Z_x(s) = (\dfrac{Z_e(s)}{R_i/(-k_2)}-1)\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}$, then

$$v_o(s) = \frac{v_c(s)}{R_i} \frac{Z_e(s)\cdot\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}}{Z_e(s)+Z_x(s)+L_s s+\dfrac{R_L(R_{Co}C_o s+1)}{(R_L+R_{Co})C_o s+1}} \tag{C.9}$$

Comparison between $Z_e(s)$ and $Z_x(s)$ is shown in Figure C.2. Since the magnitude of $Z_x(s)$ is much smaller than $Z_e(s)$, so $Z_x(s)$ can be ignored.
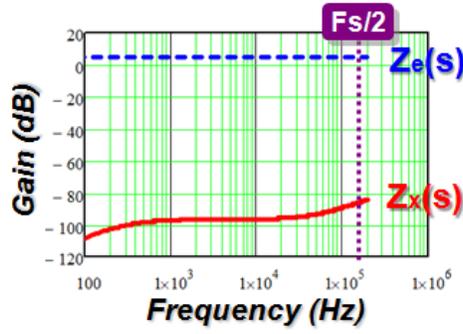
Figure C.2. Comparison between $Z_e(s)$ and $Z_x(s)$

Finally, the output voltage can be calculated as

$$v_o(s) = \frac{v_c(s)}{R_i} \frac{Z_e(s) \cdot \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{Z_e(s) + L_s s + \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}} \tag{C.10}$$

Based on the same concept, it also can be calculated as:

$$v_o(s) = v_{in}(s) \cdot k_{vin} \cdot \frac{Z_e(s) \cdot \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{Z_e(s) + L_s s + \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}} \tag{C.11}$$

where, $k_{vin} = k_1 / R_i = D / \{L_s[1/(Q_2\omega_2) - T_{off}/2]\}$. The equivalent circuit is shown as in Figure C.3.
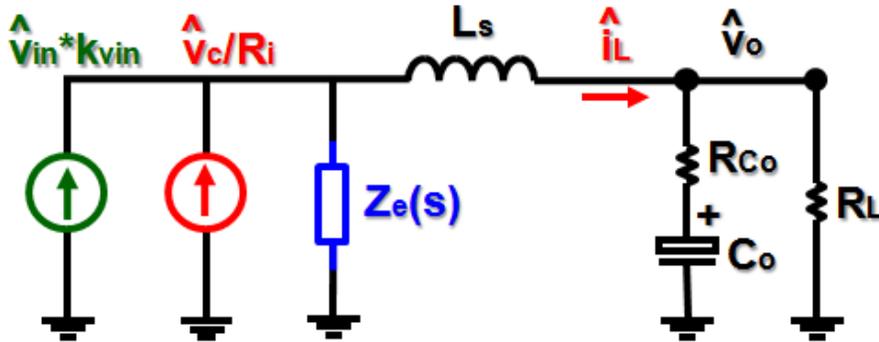
Figure C.3. Equivalent circuit representation of peak current-mode control

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For the case of considering the DCR of the inductor, the control-to-out transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} = \frac{\dfrac{1}{R_i} \dfrac{1}{1 + \dfrac{s}{Q_2 \omega_2} + \dfrac{s^2}{\omega_2^2}} \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{1 - k_2 \dfrac{1}{R_i} \dfrac{1}{1 + \dfrac{s}{Q_2 \omega_2} + \dfrac{s^2}{\omega_2^2}} \left[DCR + \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1} \right]} \tag{C.12}$$

Following the similar derivation, it can be found that:

$$v_o(s) = \frac{v_c(s)}{R_i} \frac{Z_e(s) \cdot \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{Z_e(s) + L_s s + DCR + \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}} \tag{C.13}$$

$$v_o(s) = v_{in}(s) \cdot k_{vin} \cdot \frac{Z_e(s) \cdot \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}}{Z_e(s) + L_s s + DCR + \dfrac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1}} \tag{C.14}$$

The equivalent circuit with the DCR is shown in Figure C.4.
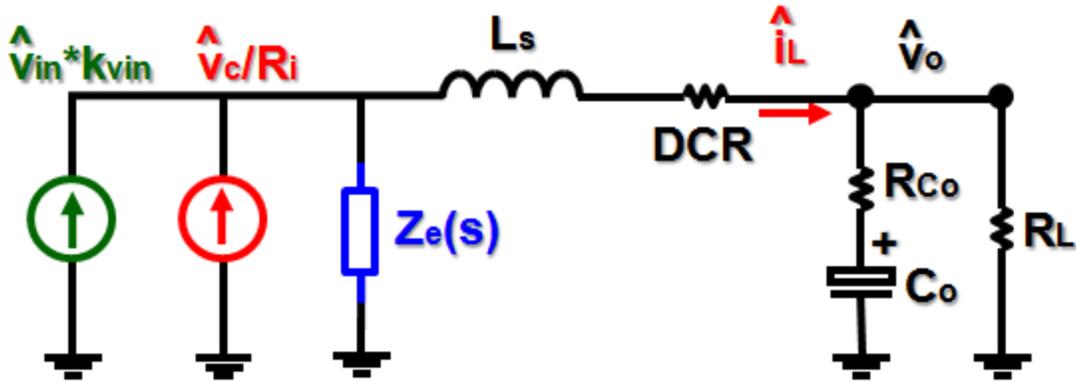
Figure C.4. Equivalent circuit representation (w/ DCR) of peak current-mode control

References

[1]   L. E. Galllaher, "Current Regulator with AC and DC Feedback," U.S. Patent 3,350,628, 1967.

[2]   F. C. Schwarz, "Analog Signal to Discrete Time Interval Converter (ASDTIC)," U. S. Patent 3,659,184, 1972.

[3]   A. Capel, G. Ferrante, D. O'Sullivan, and A. Weinberg, "Application of the Injected Current Model for the Dynamic Analysis of Switching Regulators with the New Concept of LC3 Modulator," in *proc. IEEE PESC'78*, pp. 135-147.

[4]   A. D. Schoenfeld, Y. Yu, "ASDTIC Control and Standardized Interface Circuits Applied to Buck, Parallel and Buck-Boost DC-to-DC Power Converters," NASA Report NASA CR-121106, February, 1973.

[5]   C. W. Deisch, "Switching Control Method Changes Power Converter into a Current Source," in *proc. IEEE PESC'78*, pp. 300-306.

[6]   R. Redl and N. O. Sokal, "Current-mode control, five different types, used with the three basic classes of power converters: small-signal ac and large-signal dc characterization, stability requirements, and implementation of practical circuits," in *Proc. IEEE PESC'85*, pp. 771-785.

[7]   P. L. Hunter, "Converter Circuit and Method Having Fast Responding Current Balance and Limiting," U.S. Patent 4,002,963, 1977.

[8]   L.H. Dixon, "Average Current-Mode Control of Switching Power Supplies," Unitrode Power Supply Design Seminar handbook, 1990, pp. 5.1-5.14

[9]   I. Cohen, "Adaptive control method for power converters," U. S. Patent 5,438,505, 1995.

[10]   J. P. Bryant, "AC-DC power supply growth variation in China and North America," in p*roc. IEEE APEC'05*, pp.159-162.

[11] S. Varma, "Future power solutions," _Special Session Presentation of IEEE APEC_, 2005.

[12] E. Stanford, "Power delivery challenges in computer platforms," _Special Session Presentation of IEEE APEC_, 2006.

[13] B. Mammano, "Distributed power system," _Unitrode Seminar_, SEM-900, 1993.

[14] F. C. Lee, P. Barbosa, P. Xu, J. Zhang, B. Yang, and F. Canales, "Topologies and design considerations for distributed power system applications," in _proc. IEEE_, vol. 89, no. 6, Jun. 2001, pp. 939–950.

[15] P. Xu, W. Chen, J. Shao, P.-L. Wong, B. Yang, and F. C. Lee, "Development of 1 kW front-end module for DPS testbed," in _proc.CPES Annual Seminar_, 2000, pp. 116-119.

[16] B. Yang, "Topology Investigation for Front End DC/DC Power Conversion for Distributed Power System", Ph. D Dissertation, Virginia Tech, Blacksburg, 2003.

[17] B. Lu, "Investigation of High-density Integrated Solution for AC/DC Conversion of a Distributed Power System", Ph. D Dissertation, Virginia Tech, Blacksburg, 2006.

[18] J. Sun, "Dynamic Performance Analyses of Current Sharing Control for DC/DC Converters," Ph. D. dissertation, Virginia Tech., 2007

[19] Intel document, "Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines for Desktop LGA775 Socket," November, 2006, Available at http://www.intel.com.

[20] R. Redl, B. P. Erisman and Z. Zansky, "Optimizing the Load Transient Response of the Buck Converter,"in _proc. IEEE APEC'98_, pp. 170-176.

[21] K. Yao, Y. Meng, P. Xu and F. C. Lee, "Design Considerations for VRM Transient Response Based on the Output Impedance," in _proc. IEEE APEC'02_, pp. 14-20.

[22] K. Yao, M. Xu, Y. Meng, and F. C. Lee, "Design considerations for VRM transient response based on theoutput impedance," _IEEE Trans. Power Electron._, Vol. 19, Issue 6, Nov. 2004, pp. 1454-1461.

[23] K. Yao, K. Lee, M. Xu, and F. C. Lee, "Optimal design of the active droop control

method for the transient response," in *proc. IEEE APEC'03*, pp. 718-723.

[24]   K. Yao, Y. Ren, J. Sun, K. Lee, M. Xu, J.i Zhou and F. C. Lee, "Adaptive Voltage Position Design for Voltage Regulators," in *proc. IEEE APEC'04*, pp. 272-278.

[25]   Maxim, MAX1545 datasheet, http://datasheets.maxim-ic.com/en/ds/MAX1519-MAX1545.pdf.

[26]   National Semiconductor, LM34919 datasheet, http://www.national.com/ds/LM/LM34919.pdf.

[27]   Texas Instruments, TPS51116 datasheet, http://focus.ti.com/lit/ds/symlink/tps51116.pdf.

[28]   Analog Devices, ADP2102 datasheet, http://www.analog.com/static/imported-files/data_sheets/ADP2102.pdf.

[29]   Linear Technology, LTC2812 datasheet, http://www.linear.com/pc/download Document.do?navId=H0,C1,C1003,C1042,C1032,C1082,P37683,D25009.

[30]   STMicroelectronics, PM6685 data sheet, http://www.st.com/stonline/products/literature/ds/11674/pm6685.pdf.

[31]   G. W. Wester and R. D. Middlebrook, "Low Frequency characterization of switched dc-to-dc converters," in *proc. IEEE PESC'72*, pp. 9-20.

[32]   R.D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages" in *proc. IEEE PESC'76*, pp. 18-34.

[33]   R. Dirkman, "Generalized State Space Averaging", in *proc. IEEE PESC'83*, pp. 283-294.

[34]   D. J. Packard, "Discrete Modeling and Analysis of Switching Regulators," Ph.D. dissertation, Cal. Tech., CA, May 1976

[35]   F.C. Lee and D.J. Shortt, "An Improved Switching Converter Power Model Using Discrete and Average Techniques," in *proc. IEEE PESC'82*, pp.199-212.

[36] S. Cuk and R. D. Middlebrook, "A General Unified Approach to Modeling Switching Dc-to-Dc Converters in Discontinuous Conduction Mode," in *proc. IEEE PESC'77*, pp. 36-57.

[37] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode," *IEEE Trans. Aerosp.*, Vol. 26, pp. 490 –496, May 1990.

[38] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode," *IEEE Trans. Aerosp.*, Vol. 26, pp. 497 -505, May 1990.

[39] F.C. Lee, Y. Yu, and M.F. Mahmoud, "A Unified Analysis and Design Procedure for a Standardized Control Module for DC-DC Switching Regulators, " in *proc. IEEE PESC'80*, pp.284-301.

[40] S. P. Hsu, A. Brown, L. Rensink, and R. D. Middlebrook, "Modeling and analysis of switching dc-to-dc converters in constant-frequency current-programmed mode," in *proc. IEEE PESC'79*, pp. 284-301.

[41] R. D. Middlebrook, "Topics in Multiple-Loop Regulators and Current Mode Programming," in *proc. IEEE PESC'85*, pp. 716-732.

[42] R.D. Middlebrook, "Modeling Current-Programmed Buck and Boost Regulators," *IEEE Trans. Power Electron.*, Vol. 4, pp. 36-52, January 1989.

[43] R. Martinelli, "The Benefits of Multi-Loop Feedback," in *proc. PCI'87*, pp. 227-245.

[44] G.K. Schoneman and D. M. Mitchell, "Output Impedance Considerations for Switching Regulators with Current-Injected Control," *IEEE Trans. Power Electron.*, vol. 4, pp. 25-35, January 1989.

[45] V. G. Bello, "Using the SPICE2 CAD Package to Simulate an Design the Current-Mode Converter," in *proc. POWERCON'84*, paper H-2.

[46] B. Holland, "Modelling , Analysis and Compensation of the Current-Mode Converter," in *proc. POWERCON'84*, paper H-2.

[47] A. S. Kislovski, "Controlled-Quantity Concept in Small-Signal Analysis of Switching Power Cells," *IEEE Trans. Aerosp.*, Vol. AES-19, No. 3, pp. 438-446,1983.

[48] L. H. Dixon, "Closing the Feedback Loop", Appendix C, Unitrode Power Design Seminar, pp. 2C1-2C18, 1983.

[49] A. S. Kislovski, "Current-Mode Control: a Unified Model for Open-loop Stability," in *proc. IEEE APEC'91*, pp. 459-465.

[50] V. Voqkrian, "Analysis of current-mode controlled PWM converters using the model of the current-controlled PWM switch," in *proc. PCIM Con'90.*

[51] F. C. Lee and Y. Yu "Computer-Aided Analysis and Simulation of Switched DC-DC Converters," *IEEE Trans. Ind. Applic.*, Vol. IA-15, pp. 511-520, Sept/Oct 1979.

[52] F. C. Lee, R. P. Iwens, Y. Yu and J. E. Triner, "Generalized Computer-Aided Discrete Time Domain Modeling and Analysis of DC-DC Converters," in *proc. PESC'77*, pp. 58-69.

[53] A. R. Brown and R. D. Middlebrook, "Sample-Data Modeling of Switched Regulators," in *proc. IEEE PESC'81*, pp. 349-369.

[54] G. C. Verghese, C. A. Bruzos, and K. N. Mahabir, "Averaged and sample-data models for current mode control: A reexamination," in *Proc. IEEE PESC'89*, pp. 484-491.

[55] R. Redl, "High-frequency extension of the small-signal model of the constant-frequency current-mode-controlled converter," in *proc. IEEE APEC '91*, pp. 466 – 472.

[56] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271-280, April 1991.

[57] R. Tymerski and D. Li, "State-space models for current-programmed pulsewidth-modulated converters," *IEEE Trans. Power Electron.*, vol.8, no. 3, pp. 271-278, July 1993.

[58] F. D. Tan and R. D. Middlebrook, "A unfied model for current-programmed converters," *IEEE Trans. Power Electron.*, vol. 10, no. 4, pp.397–408, Jul. 1995.

[59] D. J. Perreault and G. C. Verghese, "Time-varying effects for current-mode control," in *proc. IEEE PESC'95*, pp. 621-628.

[60] M. K. Kazimierczuk, "Transfer function of current modulator in pwm converters with current-mode control," *IEEE Trans. Circuits and Systems I*, vol. 47, no. 9, pp. 1407-1412, Sep. 2000.

[61] E. A. Mayer and A. J. King, "An improved sampled-data current-mode control which explains the effects of the control delay," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 369-374, May. 2001.

[62] B. Bryant and M. K. Kazimierczuk, "Modeling the closed-current loop of pwm dc-dc converters operating in ccm with peak current-mode control," *IEEE Trans. Circuits and Systems*, vol. 52, no. 11, pp. 2404-2412, Nov. 2005.

[63] W. Tang, F. C. Lee, and R. B. Ridley, "Small-signal modeling of average current-mode control," *IEEE Trans. Power Electron.*, vol. 8, pp. 112-119, April 1993.

[64] W. Tang, F. C. Lee, R. B. Ridley, and I. Cohen, "Charge control: modeling, analysis, and design," *IEEE Trans. Power Electron.*, vol. 8, pp. 396-403, Oct. 1993.

[65] Y.-W. Lo and R. J. King, "Sampled-data modeling of the average-input current-mode-controlled buck converter", *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 918-927, Sept. 1999.

[66] J. Sun and R. M. Bass, "A new approach to averaged modeling of PWM converters with current-mode control," in *proc. IEEE IECON'97*, pp. 599-604.

[67] J. Sun and B. Choi, "Averaged Modeling and Switching Instability Prediction for Peak Current Control," in *proc. IEEE PESC'05*, pp. 2764-2770.

[68] N. N. Bogoliubov and Y. A. Mitropolslq, *Asymptotic Methods in the Theory of Nonlinear Oscillations*, Hindustan PublishingCorpn. (India), 1961.

[69] J. H. B. Deane and D. C. Hamill, "Instability, subharmonics, and chaos in power electronics circuits," *IEEE Trans. Power Electron.*, vol. 5, pp. 260-268, July 1990.

[70] J. H. B. Deane, "Chaos in a current-mode controlled boost dc-dc converter," IEEE Transactions on Circuits and Systems-I, vol. 39, pp. 680-683, August 1992.

[71] J. L. R. Marrero, J. M. Font, and G. C. Verghese, "Analysis of the chaotic regime for dc-dc converters under current mode control," in *proc. IEEE PESC'96*, pp. 1477-1483.

[72] W. C. Y. Chan and C. K. Tse, "Study of bifurcations in current programmed dc/dc boost converters: from quasiperiodicity to period doubling," *IEEE Transactions on Circuits and Systems-I*, vol. 44, no. 12, pp. 1129-1142, 1997.

[73] R. B. Ridley, "A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM," in *proc. IEEE PESC'90*, pp. 382- 389.

[74] R. Redl, "Small-signal high-frequency analysis of the free-running current-mode-controlled converter," in *proc. IEEE PESC '91*, pp. 897 – 906.

[75] B. P. Schweitzer and A. B. Rosenstein, "Free running switching mode power regulator: analysis and design," *IEEE Trans. Aerosp.*, vol. AS-2, pp. 1171-1180, Oct. 1964.

[76] D. Goder and W. R. Pelletier, "V^2 architecture provides ultra-fast transient response in switch mode power supplies," in p*roc. HFPC'96*, pp. 19-23.

[77] D. Goder, "Switching regulators," U.S. Patent, 5,770,940, 1998.

[78] W. Huang and J. Clarkin, "Analysis and design of multiphase synchronous buck converter with enhanced V^2 control," in *Proc. HFPC'00*, 2000, pp. 74–81.

[79] W. Huang, "A new control for multi-phase buck converter with fast transient response," in *Proc. IEEE APEC'01*, Anaheim, California, pp. 273–279.

[80] S. Qu, "Modeling and design considerations of V^2 controlled buck regulator," in *Proc. IEEE APEC'01*, Anaheim, California, pp. 507–513.

[81] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol.21, pp. 346 – 353, March 2006.

[82] Y. Qiu, M. Xu, K. Yao, J. Sun, and F. C. Lee, "Multifrequency Small-Signal Model for Buck and Multiphase Buck Converters**,**" *IEEE Trans. Power Electron.*, vol. 21, pp. 1185-1192, September, 2006.

[83] Y. Qiu, "High-Frequency Modeling and Analyses for Buck and Multiphase Buck Converters," Ph. D. Dissertation, Virginia Tech, 2005.

[84] N. Krylov, and N. Bogolyubov: Introduction to Nonlinear Mechanics, Princeton University Press, 1947

[85] A. Gelb, and W. E. Vander Velde: Multiple-Input Describing Functions and Nonlinear System Design, McGraw Hill, 1968.

[86] D. M. Mitchell, "Pulse width modulator phase shift." *IEEE Trans. Power Electron.*, vol. AES-16, pp. 272-278, May 1980.

[87] R. D. Middlebrook, "Predicting modulator phase lag in PWM converter feedback loops," In *proc. POWERCON' 81*, paper H-4.

[88] J. Sun, "Small-signal modeling of variable-frequency pulsewidth modulators," *IEEE Trans. Aerosp.*, vol 38, pp. 1104-108, July 2002.

[89] D. Maksimovic, R. Zane, and R. Erickson, "Impact of Digital Control in Power Electronics," IEEE Int. Symp. on Power Semiconductor Devices & ICs, Kitakyushu, Japan, May 2004, pp. 13-22.

[90] A. M. Wu, J. Xiao, D. Markovic, and S. R. Sanders, "Digital PWM control: Application in voltage regulation modules," in *Proc. IEEE PESC'99*, Charlestion, South Carolina, pp. 77-83.

[91] A. Prodic, D. Maksimovic, and R. Erickson, "Design and Implementation of a Digital PWM Controller for a High- Frequency Switching DC-to-DC Power Converter," in *Proc. IEEE Industrial Electronics Society Annu. Conf.*, Nov. 2001, pp. 893-898.

[92] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters", *IEEE Trans. Power Electron.*, vol. 18, pp. 301-308, Jan. 2003.

[93] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of quantization effects in digitally controlled dc-dc converters," in *Proc. IEEE PESC'04*, Aachen, Germany, pp. 4312-4318.

[94] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. on Power Electron.*, vol. 18, pp. 438-446, January 2003.

[95] R. F. Foley, R. C. Kavanagh, W. P. Marnane, and M.G. Egan, "An area-efficient digital pulsewidth modulation architecture suitable for FPGA implementation," in *Proc. APEC'05*, Austin, Texas, pp. 1412-1418.

[96] A. Syed, E. Ahmen, E. Alarcon, and D. Maksimovic, "Digital pulse-width modulator architectures," in *Proc. IEEE PESC'4*, Aachen, Germany, vol. 6, pp. 4689-4695.

[97] A. M. Wu, J. Xiao, D. Markovic, and S. R. Sanders, "Digital PWM control: Application in voltage regulation modules," in *Proc. IEEE PESC'99*, Charlestion, South Carolina, pp. 77-83, 1999.

[98] A. Syed, E. Ahmed, D. Maksimovic, "Digital PWM Controller with Feed-Forward Compensation," in *Proc. APEC'04*, pp. 60-66.

[99] A. Kelly, K. Rinne, "High Resolution DPWM in a DC-DC Converter Application Using Digital Sigma-Delta Techniques," in *Proc. PESC'05*, pp. 1458 - 1463.

[100] Z. Lukic, K. Wang, and A. Prodic, "High-frequency digital controller for dc-dc converters based on multi-bit /spl Sigma-Delta-pulse-width modulation," in *Proc. APEC'05*, Austin, Texas, pp.35-40.

[101] Y. Qiu, J. Li, F. C. Lee et al., "Proposed DPWM Scheme with Improved Resolution for Switching Power Converters," in *Proc. APEC'07*, Anaheim, California, pp. 1588-1593.

[102] S. Bibian and H. Jin, "High performance predictive dead-beat digital controller for DC power supplies," in *Proc. APEC'01*, Anaheim, California, pp. 67-73.

[103] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, vol. 18, pp. 411-419, Jan. 2003.

[104] P. Athalye, D. Maksimovic, and R. Erickson, "Variable-frequency predictive digital current mode control," *IEEE Power Electron. Lett.*, vol. 2, Issue 4, pp. 113-116, Dec. 2004.

[105] S. Chattopadhyay and S. Das, "A digital current mode control technique for DC-DC converters," in *Proc. APEC'05*, Austin, Texas, pp. 885-891.

[106] G. Garcea, P. Mattavelli, K. Lee, and F. C. Lee, "A Mixed-Signal Control for VRM applications," in *Proc. 11th European conf. on power electronics and applications,* pp. 10-15, September 2005.