High Frequency, High Efficiency Two-Stage Approach for Future Microprocessors

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(Abstract)

It is perceived that Moore's Law will prevail at least for the next decade, with continuous advancements of processing technologies for very-large-scale integrated (VLSI) circuits. Nano technology is driving VLSI circuits in a path of greater transistor integration, faster clock frequency, and lower operation voltage. This has imposed a new challenge for delivering high-quality power to modern processors. Power management technology is critical for transferring the required high current in a highly efficient way, and accurately regulating the sub-1V voltage in very fast dynamic transient response conditions. Furthermore, the VRs are limited in a given area and the power density is important to save the precious real estate of the motherboard.

Based on the power delivery path model, the analysis results show that as long as the bandwidth can reach around 350 kHz, the bulk capacitor of the VR can be completely eliminated, which means significant savings in cost and real estate. Analysis also indicates that 650kHz bandwidth can reduce the number of the decoupling capacitor from 230 to 50 for future microprocessor case. Beyond 650kHz, the reduction is not obvious any more due to the parasitic components along the power delivery path.

Following the vision of high bandwidth, the VRs need to operate at much higher frequency than today's practice. Unfortunately, the multiphase buck converter cannot benefit from it due to the low efficiency at high switching frequency. The extreme duty is the bottleneck. The extreme duty cycle increases VR switching loss, reverse recovery loss, and conduction loss; therefore makes the 12V-input VR efficiency drop a good deal when compared with 5V-input VR efficiency.

Two-stage approach is proposed in this dissertation to solve this issue. The analysis shows that the two-stage conversion has much better high frequency capability than the conventional single stage VRs. Based on today's commercial devices, 2-MHz is realized by the hardware and

350kHz bandwidth is achieved to eliminate the output bulk capacitors. Further improvement based on future devices and several proposed methods of reducing switching loss and body diode loss can push the switching frequency up to 4MHz while maintaining good efficiency. Such a high frequency makes the high bandwidth design (650kHz) feasible. Hence, the output capacitance can be significantly reduced to save cost and real estate.

The two-stage concept is also effective in laptop computer and 48V DPS applications. It has been experimentally proved that two-stage VR is able to achieve higher switching frequency than single stage not only at full load condition but also at light load condition by the proposed ABVP and AFP concept based on two-stage configuration. These unique control strategies make the two-stage approach even more attractive.

As the two-stage approach is applied to 48V DPS applications, such as telecommunication system and server systems, more efficient and higher power density power supply can be achieved while greatly cut down the cost. Therefore, after the two-stage approach is proposed, it has been widely adopted by the industry.

In order to further reduce the output capacitance, the power architecture of computer needs to be modified. Based on two-stage approach, one possible solution is to move the second stage VR up to the OLGA board. Based on this structure, the parasitics can be dramatically reduced and the number of the cavity capacitor is reduced from 50 to 14. By reducing ESL of the capacitor, the output capacitance could be further reduced. After that and based on two-stage approach again, VR+LR structure is discussed, which provides the opportunity to reduce the output capacitance and integrate the power supply with CPU. The feasibility is studied in this dissertation from both power loss reduction and output capacitance reduction perspectives. Experimental results prove that LR can significantly reduce the voltage spike while minimizing the output capacitance.

As a conclusion, the two-stage approach is a promising solution for powering future processors. It is widely effective in computer and communication systems. Far beyond that, it provides a feasible platform for new architectures to power the future microprocessors.

To my parents

Xiaoniu Ren

Juying Wang

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TABLE OF CONTENTS

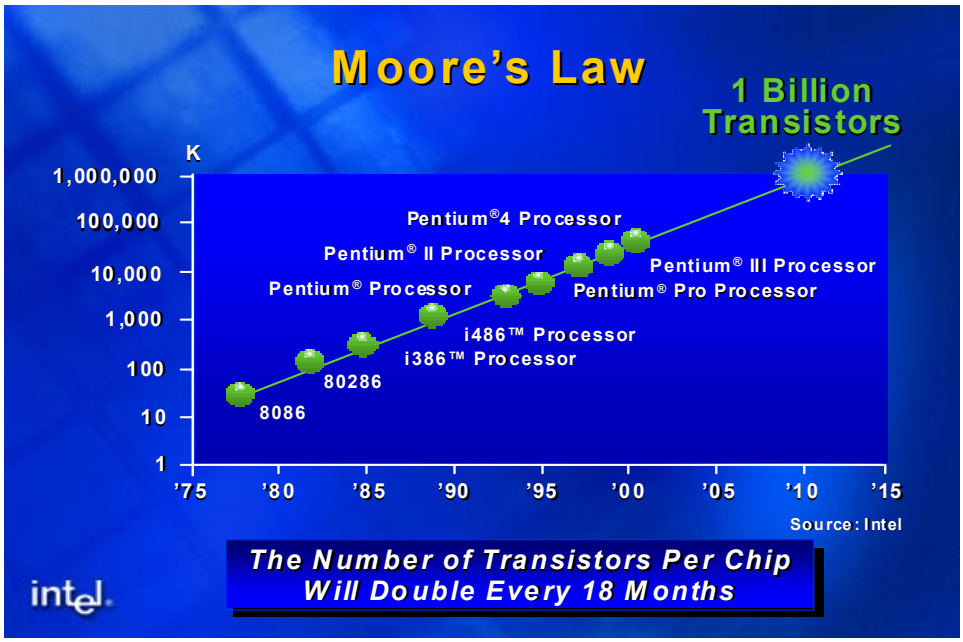
LIST OF TABLES

LIST OF FIGURES

Chapter 1. Introduction

1.1. Background: Evolution of Microprocessors

Advances in microprocessor technology challenge the power supplies of these devices. Complying with Moore's Law, which states that "transistor density … doubles every eighteen months," the transistors per die in the microprocessors have been steadily increasing in the past decade, as shown Figure 1-1.



(From *Intel Material Technology Operation 2003*, by Ed Stanford, Intel)

Figure 1-1. Number of transistors in the microprocessors increases exponentially.

The increasing number of transistors in the microprocessors results in continuous increase of the microprocessor current demands. In order to reduce the power consumption of the microprocessors, the supply voltages have been decreased, as shown in Figure 1-2. Moreover, due to the high frequencies, the microprocessors' load transition speeds also increase. The trends for microprocessor current slew rates are shown in Figure 1-3. In the mean time, the voltage

deviation window during the transient is becoming smaller and smaller since the output voltage keeps decreasing. In terms of output impedance, the R_{droop} keeps decreasing too.

The low voltage, high current and fast load transition speeds are the challenges imposed on microprocessors' power supplies.

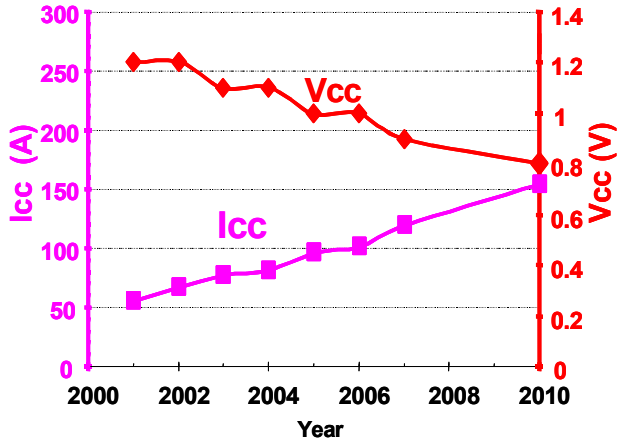


Figure 1-2. The microprocessor voltage and current roadmap.

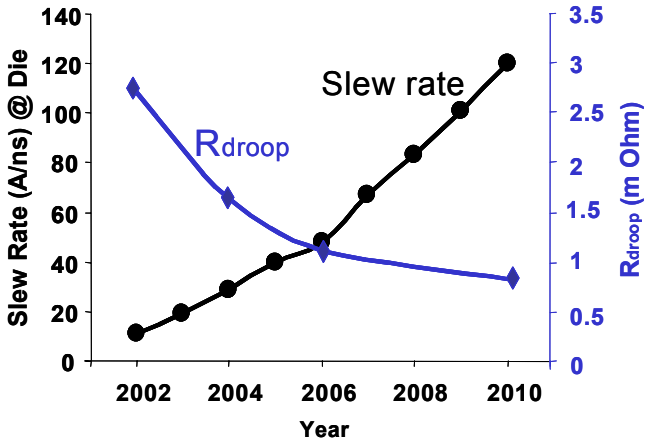


Figure 1-3. The microprocessor current slew rate and R_{droop} roadmap.

1.2. Evolution of Voltage Regulators (VR)

1.2.1. VR Architecture

Starting with the Intel Pentium ™ microprocessor, microprocessors began to use a non-standard power supply of less than 5V. Opposite to the voltage decrease, the current

requirements of the microprocessors greatly increased. Because of the microprocessors' low voltage and high current demands, the parasitic resistors and inductors of the connections between the centralized silver boxes and the microprocessors have a severe, negative impact on power quality. It is no longer practical for the bulky silver box to provide energy directly to the microprocessor. It is now necessary to power the microprocessors of computer systems with dedicated converters, voltage regulator (VRs).

The point-of-load regulation system is used to deliver a highly accurate supply voltage to the microprocessor, where a dedicated dc/dc converter, the VR, is placed in close proximity to the microprocessor in order to minimize the parasitic impedance between the VRM and the microprocessor. Figure 1-4 shows the conceptual power delivery architecture for low-end computer systems. In the beginning, a 5-V is used as the input of the VRM. As the power consumption of the microprocessor increases, the distribution loss of the 5-V bus dramatically increases. Therefore, the input voltage from the silver box turns to 12-V.

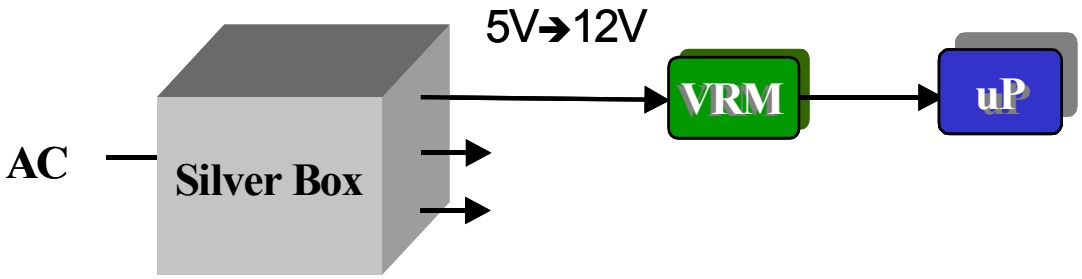


Figure 1-4. Power delivery architecture for low-end computer systems.

In order to minimize the impact of the parasitic impedance on the VR transient response, VRs need to be located very close to the microprocessors. There are basically two types of VRs: plug-in VR or so-called VR modules (VRM), which is a power module that can be plugged into a standard socket on the motherboard, and the on-board VR or so-called VR-down, which is built directly onto the motherboard, as shown in Figure 1-5 and Figure 1-6, respectively.

The benefit of VRMs is its exchangeability. The benefit of VR-Down is that they can eliminate the problematic and costly connector that comes with VRMs. Most of today's low-end computer systems use VR-Down.

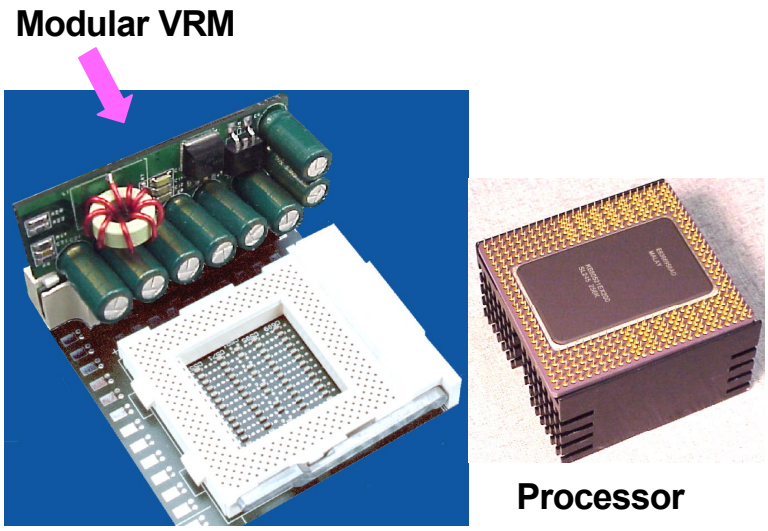


Figure 1-5. Plug-in VR module (VRM).

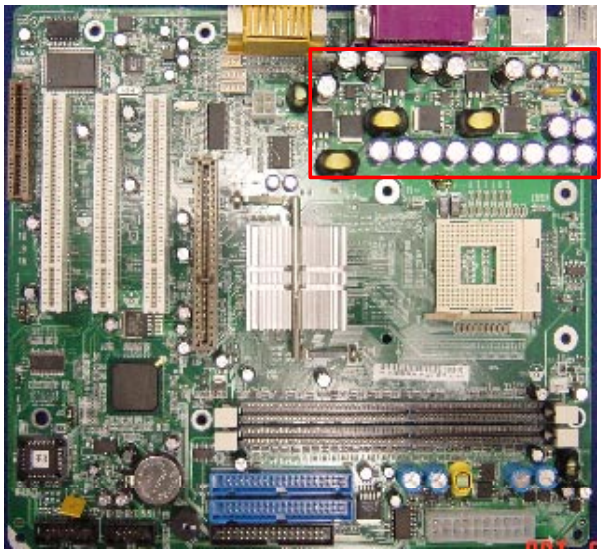


Figure 1-6. On board VR (VR-Down) on a motherboard for Pentium IV.

For high-end computer systems with multi-processors, such as high-end servers, the distribution power architecture is often used, as shown in Figure 1-7. The paralleled front-end converters provide a single DC distribution bus around the system, which is often +48 V and feeds VRMs and other DC/DC converters. Each processor has its own VRM in close proximity. Figure 1-8 shows a four-processor server system from Intel [17]. The VRM, also called the Power Pod, is directly connected to the interposer of the processor through power tabs.

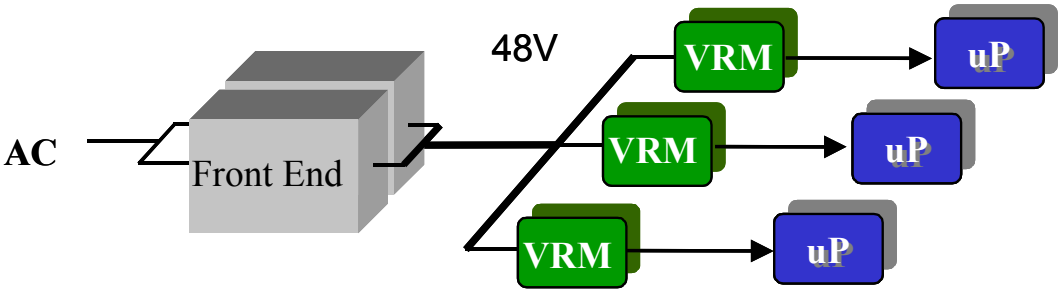


Figure 1-7. Power delivery architecture for high-end server computer systems.

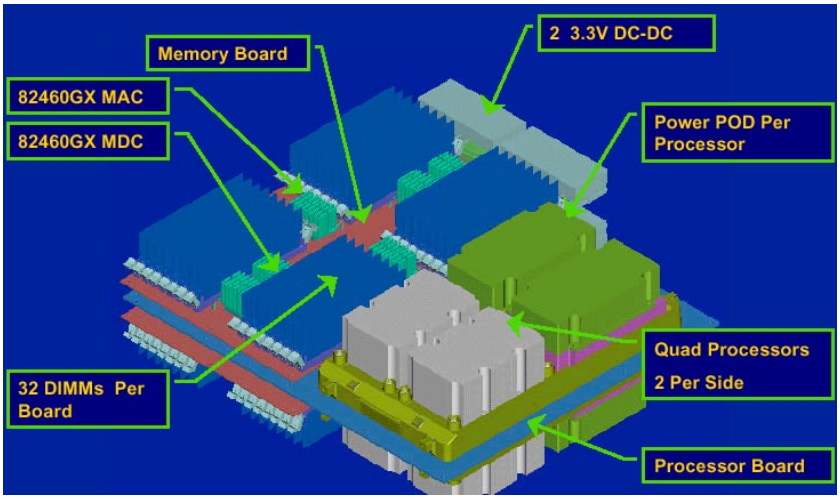


Figure 1-8. Power Pod in Intel high-end servers [17].

Although VRs take a variety of form factors for different computer systems, the fundamental requirements for VRs are generally the same. The fast dynamic transients happen when the microprocessor chip operates from sleep mode to active mode and vice-versa. The small transient voltage deviation under high currents and high slew rates is the most stringent requirement. As the operating voltage is reduced to sub-1V, the transient voltage tolerance is also expected to decrease and become much tighter. Because of the high cost of space in the motherboard, power density and efficiency are also very important for VRs. These performance requirements pose serious challenges for the VR design.

1.2.2. Technologies for VR design

The purpose of the VR is to maintain voltage to the microprocessor during its transient response periods. When the microprocessor switches between “sleep mode” and “active mode,” and vice versa, the current demand of the microprocessor transits between no load and full load

with very high current slew rates. During operation, the microprocessors also have fast transitions between different load levels due to the number of transistors involved in the computations. Because of the tremendous clock speed of the microprocessor, the transitions need to be completed quickly, which imposes very high current slew rates on the VR. The transition corresponding to microprocessor load current increase is called the step-up transient. The load current decrease transition is called the step-down transient.

For the next generation of microprocessors, high load currents, high current slew rates and tight voltage regulation are the most stringent requirements of the VRs. Moreover, because of the high cost of the board area in computers, power density and efficiency are also very important. These performance requirements pose serious challenges for the VR design.

1.2.2.1. Interleaving Technology

Earlier VRs for the low-end computer use a single conventional buck or synchronous buck topology for power conversion [1][2][3]. They operate at a lower switching frequency with a higher filter inductance that limits the transient response [4][5][6].

Figure 1-9 shows a single-phase VR. The large output-filter inductance limits the energy transfer speed. In order to meet the microprocessor requirements, huge output-filter capacitors and decoupling capacitors are needed to reduce the voltage spike during the transient.

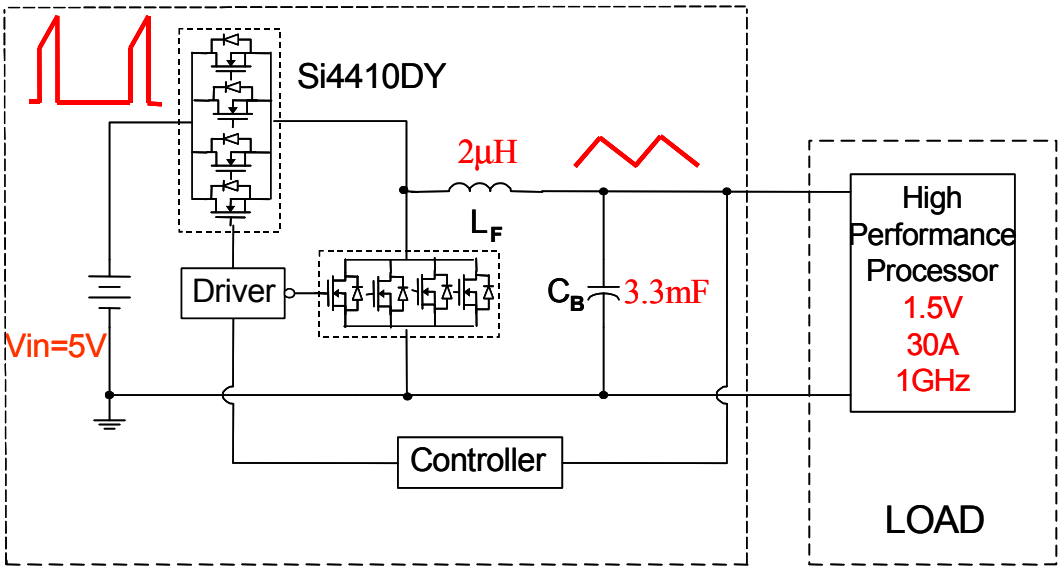


Figure 1-9. Conventional single-phase synchronous Buck converter for VRs.

In order to reduce the VR output capacitance to increase the power density and to save the real estate of the motherboard, a large inductor current slew rate is preferred. Smaller inductances give larger inductor current slew rates; therefore, a smaller output capacitance can be used to meet the transient requirements. In order to greatly increase the transient inductor current slew rate, the inductances need to be reduced significantly, as compared with those in conventional designs (as shown in Figure 1-9).

However, small inductances result in large current ripples in the circuit's steady-state operation. The large current ripple usually causes a large turn off loss. In addition, it generates large steady-state voltage ripples at the VRM output capacitors. The steady-state output voltage ripples can be so large that they are comparable to transient voltage spikes. It is impractical for the converter to work this way.

In 1997, VPEC (CPES) proposed using interleaving technology to solve the large current ripples in VRs [7][8][9][10]. The topology of an interleaving buck converter is shown in Figure 1-10. It consists of n identical converters with interconnected inputs and outputs. The duty cycles of adjacent channels have a phase shift of $\frac{360^o}{Nc}$, where N_c is the total channel number.

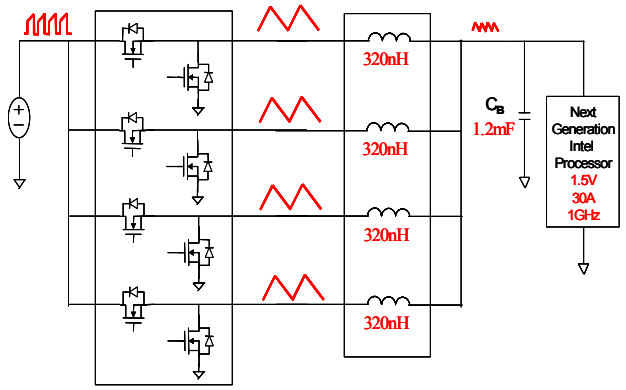


Figure 1-10. CPES proposed interleaving synchronous Buck converter for VRs.

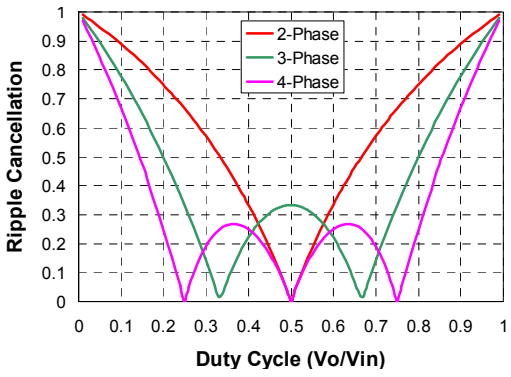


Figure 1-11. Current ripple cancellation in multiphase VRs.

Interleaving greatly reduces the current ripples to the output capacitors (refer to Figure 1-11), which in turn greatly reduces the steady-state output voltage ripples, making it possible to use very small inductances in VRs to improve transient responses. Interleaving VRs with small inductances reduces both the steady-state voltage ripples and the transient voltage spikes, so that a much smaller output capacitance can be used to meet the steady-state and transient voltage

requirements. Thus, power density can be significantly improved. Moreover, interleaving makes the thermal dissipation more evenly distributed. Studies show that in high-current applications, the overall cost of the converter can be reduced using this technology. The concept of applying interleaving to VRs is so successful that it has become standard practice in VRM industry. Correspondingly, many semiconductor companies, such as Intersil, Semitech, National Semiconductor, On Semiconductor, Analog Devices, and Volterra, have produced dedicated control ICs for multiphase VRs.

For the high-end computer, isolated topologies are used, and the current-doubler rectifier is usually adopted at the secondary side. Basically, it can be treated as a two-phase interleaving.

1.2.2.2. Non-Isolated Transformer and Autotransformer Version Buck Converter for 12V VRs

In recent years, the output current has increased while output voltage is reduced. More and more real estate of the motherboard will be taken over by VRs, especially the output capacitors. High frequency is becoming the only solution to increase the power density and save real estate. However, the conventional interleaving buck converter's performance suffers a lot as switching frequency increases. The major reason is the small duty cycle, which results in low efficiency and poor ripple cancellation.

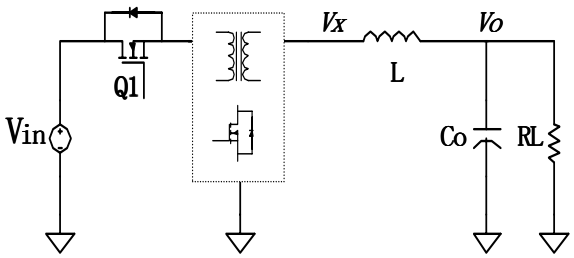


Figure 1-12. A conceptual drawing of autotransformer version buck converter.

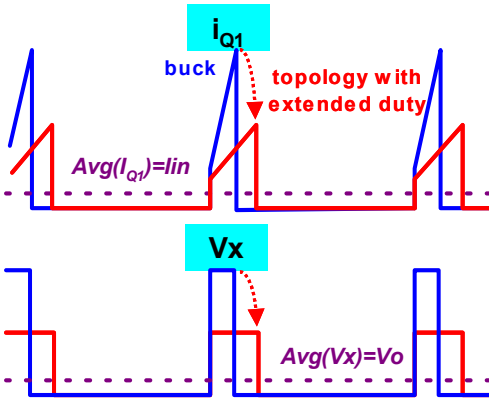


Figure 1-13. By employing the autotransformer, the turn off current and reverse voltage across the body diode are reduced.

CPES has proposed a family of autotransformer version buck converters [11]~[16] to increase the switching frequency while achieving high efficiency. The concept is shown in

Figure 1-12. By employing an autotransformer in the circuit, the duty cycle can be extended and the turn off current of the top switch, as well as the turn off loss (as shown in Figure 1-13), can be significantly reduced. In the mean time, the reverse voltage across the body diode of the bottom switch is also reduced by the turns-ratio. Therefore, the body diode reverse recovery loss is reduced.

As a conclusion, the autotransformer version buck converter is capable of achieving higher efficiency at high frequency applications compared with the synchronous Buck converters.

By adopting the transformer or autotransformer, the duty cycle is extended, which not only reduces the current ripple and the phase voltage, but the switching loss and body diode losses are correspondingly reduced. However, the transformer introduces a leakage inductor into the circuit, which causes a common issue: duty cycle loss. The larger leakage inductance, the more duty cycle is lost.

In order to reduce the leakage inductance, the transformer/autotransformer should be well designed, for example, the use of PCB winding increases the coupling effect. This kind of structure usually results in higher cost. If the traditional transformer structure is still used, the turns-ratio has to be reduced in order to reduce the impact of large leakage inductance. However, smaller turns-ratio significantly increases the turn-off loss and conduction loss at the primary side.

As a result, the inherent leakage inductor fundamentally limits the high frequency capability of the topologies employing transformer/autotransformer. In order to achieve high efficiency at high frequency, an alternative way should be explored.

1.2.2.3. 48V Input VRM

High efficiency and high power density are the general requirements for 48V input VRM. More and more output capacitors would be needed by the future microprocessors if the switching frequency and bandwidth cannot be pushed. Because of similar input and output specification, substantial research efforts made for low-voltage DC/DC converters can be extended to 48V VRM. As mentioned in [16], the non-isolated topologies can be derived from the isolated topologies.

Synchronous rectification with specifically designed low-voltage MOSFETs is widely used to dramatically improve the efficiency of low-voltage DC/DC converters [18]~[23]. For 48V VRM, synchronous rectification is the must technology.

The active clamped forward converter has become the prevailing topology in low-voltage DC/DC converter applications because it recovers the magnetizing energy of the transformer and minimizes the voltage and current stresses of the primary switches as well as those of the synchronous rectifiers (SRs). However, this topology is a fourth-order system. For 48V VRM, it is difficult to achieve a higher bandwidth design to improve transient responses [24].

Research has proven that the symmetrical half-bridge topology with the synchronous rectifier is a suitable approach for this application [25]. Major power supply vendors such as Delta and Celestica have already used this technology in their 48V VRM designs.

In 1998, VPEC (CPES) proposed a novel push-pull forward topology for 48V VRM. It has an improved transient response, improved efficiency, and increased package density. This topology is essentially a modified push-pull converter topology with a clamp capacitor. One can clamp the voltage overshoot and recover the leakage energy. This topology also provides a reduced input current ripple and requires a smaller input filter. Experimental results show that the push-pull forward topology can demonstrate 3% better efficiency compared to either a symmetrical or an asymmetrical half-bridge converters [24].

The topologies discussed above belong to the PWM hard-switching domain. In order to push the switching frequency and maintain good efficiency, PWM soft-switching technique was applied in 48V VRM from 2000. Power supply vendors, such as Celestica, were using phase-shifted full bridge converter in their 48V VRM product.

In 2002, CPES proposed a self-driven soft-switching full bridge converter [26]. It can achieve not only ZVS for the primary switches, but also the self-driven for the synchronous rectifiers. Further research indicated that this self-driven scheme can save the drive loss and body diode conduction loss of SRs. The hardware demonstrated over 84% efficiency at 1MHz.

However, the isolated topologies can hardly meet the transient requirements posed by the future microprocessors because the isolated feedback dramatically limits the high bandwidth

design. Although the evolution of the topologies for 48V VRM are making better and better steady state performance, it lacks of the capability to handle high di/dt load.

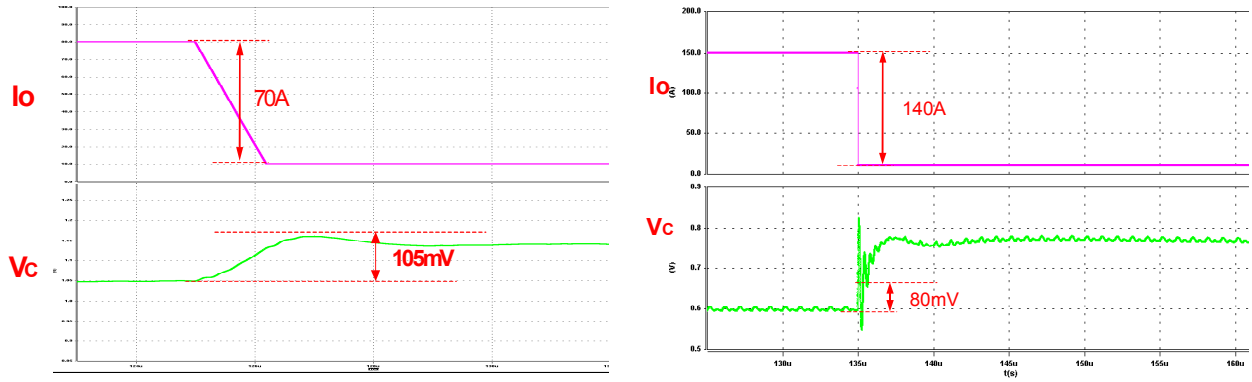
It is time to re-investigate the power delivery systems for servers, as the microprocessors are fast moving forward.

1.3. Challenges for VR Design

As discussed in section 1.1, power management related issues become much more critical for future microprocessors and much more difficult to deal with. Table 1-1 lists the specification comparison. Figure 1-14 shows the output voltage spike V_c (refer to Figure 1-15) comparison between today's microprocessor and the future's microprocessor, if today's low frequency multi-phase VR design is followed. It is obvious that the future's microprocessor poses a serious challenge for the VR transient design.

Table 1-1. Specification comparison between 2005 and 2010 microprocessors

	Output	Slew rate @ CPU die	ΔV_C (mV) @ the sensing point
Present (2005)	1.2V/90A	20A/ns	150
Future (2010)	0.8V/150A	120A/ns	80



(a) (b)

Figure 1-14. Output voltage spike comparison between 2005 and 2010 microprocessors: (a) 2005, (b) 2010.

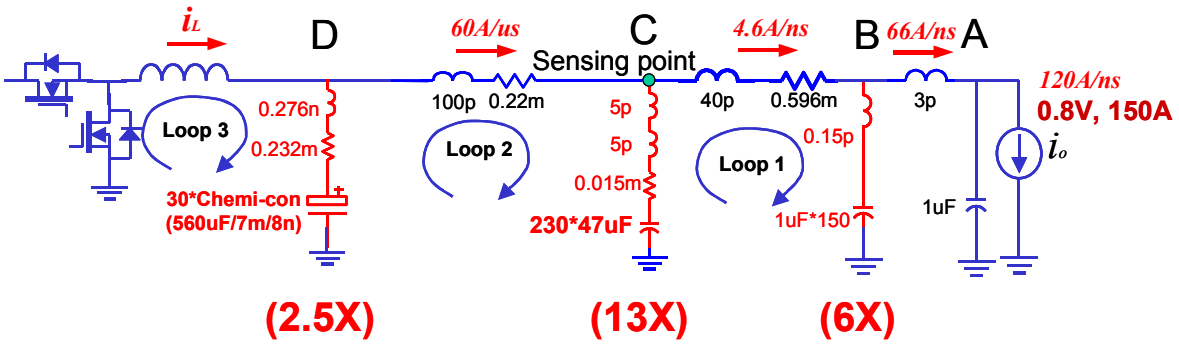


Figure 1-15. Future microprocessor demands much more capacitors if today's solution is still followed.

In order to meet the future transient requirement, more and more capacitors have to be paralleled if low frequency solution is still employed. As shown in Figure 1-15, the bulk capacitor number will increase by 2.5 times. The decoupling capacitor number will increase by 13 times and the packaging capacitor number will increase 6 times. The analysis will be elaborated in Chapter 2. Basically, so many capacitors mean a huge cost and big size. To reduce the output capacitance, high bandwidth or high frequency design is mandatory.

To achieve the high bandwidth target, the following technology challenges should be addressed:

1. Advanced VR topologies: High efficiency, high power-density and fast transient response for low voltage high-current application.
2. Advanced power architecture: As the power requirement of the microprocessors is fast moving forward, it is important to re-investigate the power architecture. More efficient and cost-effective architecture should be explored.
3. High bandwidth design: As the bandwidth increases, the propagation delay, controller op-amp design and other issues show up. How to overcome these barriers is still not clear to us. On the other hand, today's practice is to design the bandwidth at around 1/10~1/6 of the switching frequency. Due to the aliasing effect and sample-hold effect, it is difficult to push the bandwidth beyond 1/3 of the switching frequency. If the bandwidth can be pushed without increasing the switching frequency, the circuit performance could be significantly improved.

4. Efficient synchronous rectification: New driving means or topologies means to eliminate the body diode loss for high frequency operation.
5. Advanced power devices: High frequency VRs need the support of devices. Basically, the device performance needs to be improved.
6. Advanced packaging technology: Minimizing parasitics to improve the device performance for high frequency operation.

The first, second, forth, fifth and sixth preceding challenges have been addressed in this dissertation. The primary objectives of this dissertation are to develop advanced architecture and advanced topologies for high efficiency, high power-density, and fast-transient VRs.

1.4. Dissertation Outlines

This dissertation consists of six chapters. They are organized as follows. First, the background information is introduced, and the challenges for VR design are discussed. Then, the whole power architecture is investigated and the roadmap of VR is drawn. Following this roadmap, two-stage architecture is proposed to satisfy the future specifications of the microprocessors. After that, the switching regulator might hit its limitation. Therefore, new power delivery structures are proposed. The hybrid filter concept is one of the most promising methods to reduce the output capacitance. The detailed outline is elaborated as follows.

Chapter 1 is the background review of existing VR technologies and the technical challenges for VRM designs. In order to improve the transient response, small inductances must be used. The ripple cancellation in multiphase converter makes it possible to use very small inductances in VRs. Multiphase converters have become the standard practice for 12V VRs in the industry. Today's multiphase VRs are almost universally based on the synchronous buck topology. A great amount of work has been done analyzing and designing the synchronous buck VR. As the microprocessors quickly develop, the conventional multiphase synchronous buck converter is not suitable any more. A family of topologies employing transformer/autotransformer proposed by CPES is introduced in this chapter. They are able to greatly improve the efficiency and are able to increase the power density. However, the inherent leakage inductor of the transformer, which causes duty cycle loss, fundamentally limits their high frequency capability.

The technical challenges of VRM designs can be summarized as advanced VR architecture and topologies, efficiency synchronous rectification, innovative integrated magnetic, advanced power devices, advanced packaging technology and advanced control technology. The primary objectives of this dissertation are to develop advanced architecture and topologies for high efficiency, high power-density, and fast-transient VRs.

Chapter 2 analyzes the whole power delivery path from VR to the microprocessor. In order to meet the specification of future microprocessors, more and more capacitors have to be paralleled if today's low frequency solution is followed. However, it is not feasible because the cost of VR will dramatically increase and the VR will occupy too much real estate of the motherboard. To overcome the aforementioned challenges, the bandwidth of the VR should be pushed to reduce the output capacitors. The detailed relationship between the bandwidth of the VR and the output capacitance of the desktop computer is illustrated first in this chapter. At 200-KHz bandwidth, the output bulk capacitor should be switched from OS-CON capacitor to ceramic capacitor to reduce the footprint while keeping the same cost. At 350-KHz bandwidth, the output bulk capacitors are eliminated. At 650-KHz bandwidth, the decoupling capacitors on the motherboard are reduced from 230 pieces to 50 pieces. However, beyond 650-KHz bandwidth, the parasitic inductance and ESL of the capacitors hinder the capacitance reduction.

Basically, this analysis draws a big picture for the development of the power architecture and the high switching frequency VRs.

Chapter 3 proposes a two-stage approach in order to achieve high bandwidth VR design. The first stage is designed at relatively low switching frequency to step down the input voltage from 12V or 48V to around 5V. Such a low intermediate bus voltage can dramatically reduce the switching loss and the body diode loss of the second stage. Furthermore, the low-voltage-rating (12~20V) device, which shows better performance than today's 30V device, can be used in the second stage to further improve the efficiency. As a result, the second stage's switching frequency can be pushed to 2MHz to achieve 350kHz bandwidth and eliminate the bulk capacitors. More thorough device study based on physics-based simulation tool shows that the second stage is able to reach 4MHz by integration packaging technology (DrMOS) and low-voltage-rating devices while still maintaining 20W total device loss constrain specified by Intel. At such a high frequency, the decoupling capacitors can also be greatly reduced over 80%.

Compared with single stage, two-stage approach shows a much better high frequency capability, is more cost-effective and can also be applied to a laptop computer application.

Chapter 4 discusses the application of two-stage structure to 48V telecommunication and server power system. The second stage is exactly same as that in 12V two-stage VRs. The only difference is the first stage. In this chapter, a family of high power density bus converters is proposed for 48V two-stage structure. A full-bridge converter is used as an example to explain the operation principle for the isolated bus converter and a proposed resonant Buck converter is used as an example for the non-isolated bus converters. Based on the concept of energy transferring by the leakage inductor, the bulky output inductor can be eliminated. Through careful selection of the output capacitor, ZCS turn-off can be achieved, and the body diode loss can be eliminated. Meanwhile, the magnetizing current is used to achieve ZVS turn-on for all switches, and a self-driven structure is proposed to this family of bus converters in order to further simplify the circuit and to save drive loss.

As a result, the proposed inductor-less bus converter is able to run at high frequencies with higher power density. The experimental results of the inductor-less full bridge bus converter show that it can achieve over 95% efficiency at 500W output in a quarter-brick size. Its power density is around 3 times higher than today's industry practices.

The experimental results of the whole system are also provided to prove that the two-stage approach is also effective in the telecommunication and server power systems.

Chapter 5 proposes some new power delivery architectures for future microprocessors. A hybrid filter concept, which combines switching regulator and linear regulator, is articulated in this chapter. Basically, it is a new power delivery structure to dramatically reduce the requirement of ESL of the packaging capacitors. A LR is used to supply fast transient response during the rising edge and falling edge of the output current demand. The major energy is still provided by output capacitors. The advantage of the proposed structure is to greatly reduce the power dissipation of the LR while minimizing the number of output capacitors. The design procedure is elaborated in this chapter and verified by the simulation. Compared with the conventional capacitor solution, it can reduce the amount of capacitors by over 90%. Compared with the conventional linear regulator solution, the proposed topology can also reduce the power

loss over 95%. Moreover, this structure can be applied to other high di/dt applications to reduce the output capacitors and improve the power density.

Meanwhile, other technical barriers and possible solutions are discussed as well.

Chapter 6 is the summary of this dissertation.

Chapter 2. Analysis of the Power Delivery Architecture from the VR to the Microprocessors

2.1. Introduction

Microprocessors are becoming more and more powerful, and their power consumption is correspondingly increasing. As a result, voltage regulator (VR) design has become a serious challenge. The output voltage of the microprocessor for desktop will be less than 1 V while the output current will increase up to 150 A (shown in Figure 1-2). Additionally, the current slew rate of the microprocessor will reach 120 A/ns as compared with the 10 A/ns of today (shown in Figure 1-3). Another aspect of the transient performance is the voltage deviation window (ΔV). Since the output voltage of a future microprocessor is sub-1V, ΔV is limited to less than 100 mV, although the output current is higher. Therefore, the transient requirement is more stringent.

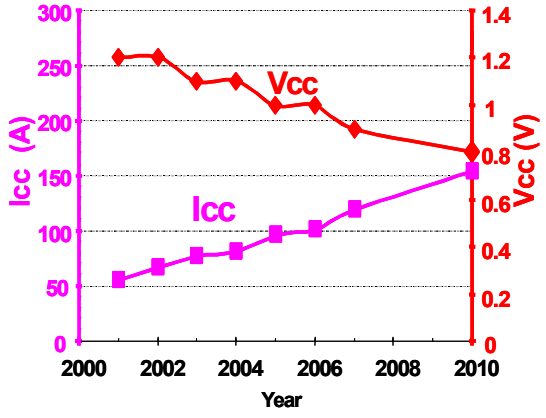


Figure 2-1. The microprocessor voltage and current roadmap.

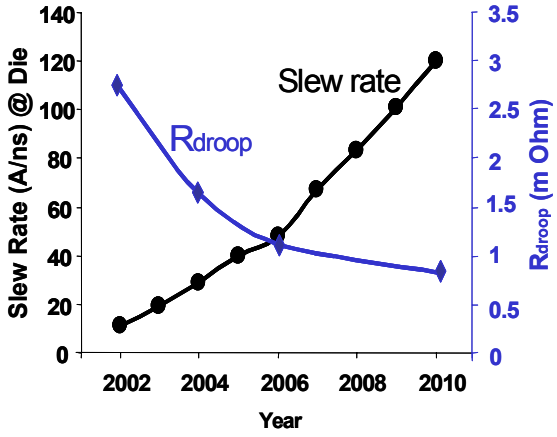


Figure 2-2. The microprocessor current slew rate and Rdroop roadmap.

If today's solution is still followed, more and more capacitors have to be paralleled, as shown in Figure 2-3, which will be derived in this chapter based on the power delivery architecture model. Meanwhile, the real estate on the motherboard (MB) for the VR is almost

fixed, which means the future VR should have much higher current density as compared with today's version.

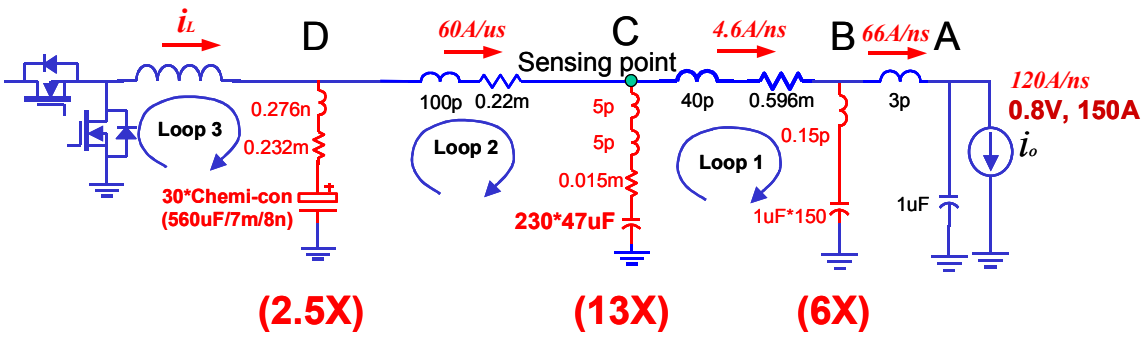


Figure 2-3. Future microprocessor demands much more capacitors if today's solution is still followed.

The only solution is to shrink the passive components, thus leaving more room for the active components. For this purpose, some non-linear methods have been proposed to reduce the output capacitors [27][28]. However, the non-linear control method is not practical for VR applications yet. From the standpoint of industry product, the linear control method [29][30] is preferred.

Under the linear control, the output capacitance generally becomes smaller as the bandwidth of the VR is pushed higher. However, an accurate description of the relationship between the bandwidth of the VR and the capacitance (especially the decoupling capacitance) in the power delivery path is still unclear. The three-loop concept has been proposed to analyze the transient [31], but only simulation was used in this approach; no expression was derived to explain the relationship between the voltage spike and the current slew rate of each loop. Other work derived a critical bandwidth concept and determined the relationship between the bandwidth of the VR and the output bulk capacitance [32]. However, this work assumes that the slew rate of the current demand is infinite, and the equivalent series inductance (ESL) is ignored. Actually, as the current slew rate of the future microprocessor increases, the ESL effect proves to be significant and should therefore be considered in the design. In addition, this paper drew a conclusion that the higher bandwidth doesn't help to reduce the output capacitance once the critical bandwidth is reached. It will be proved in this chapter that this statement is not true. Other researchers derived an extended adaptive voltage positioning (EAVP) concept in the frequency domain [34]. It helps us to understand why AVP is desired by the microprocessor. But

they omitted the expression in the time domain, which would have been easier to understand. Furthermore, EAVP concept is difficult to be realized because additional resistors have to be in series with the output capacitors, which is not desired.

This chapter addresses these issues relating to the power delivery path analysis. First, the current slew rate of each loop is derived. Then, the relationship between the bandwidth of the VR and the inductor current slew rate is determined. After that, the voltage spike across the capacitors of each loop can be easily derived. Finally, the relationship between the bandwidth of the VR and the capacitance is plotted. Experimental results are provided to verify the analysis. For illustration purposes, an example of today's desktop power delivery path is used; however, the methodology is generic to any power network design.

Based on the analysis methodology, the power delivery architecture of the desktop computer is discussed in this chapter. As a conclusion, today's power delivery architecture is facing a big challenge posed by the microprocessors. The limitations of today's solutions are pointed out and discussed as well.

2.2. Power Delivery Architecture Model

A model of the power delivery path is required before a way can be found to reduce the number of passive components, especially capacitors. Based on this model, the current slew rate of each loop and the inductor current slew rate of the VR are derived and used to calculate the unbalanced charge that results in the voltage spike across the capacitors. Finally, the relationship between the bandwidth of the VR and the capacitance can be determined.

Figure 2-4 shows one of today's desktop computer MBs as an example; its typical conceptual drawing and the definition of capacitors in different locations are illustrated in Figure 2-5. Normally, electrolytic capacitors, such as Oscon, Chemi-Con and etc., are used as the bulk capacitor of the VR. Those capacitors have large capacitance, equivalent series resistance (ESR) and equivalent series inductance (ESL). In order to deal with the high slew rate current, decoupling capacitors are needed. A part of them is located in the cavity of the socket and therefore is called cavity capacitor. For each piece, the capacitance is around 10~22uF; ESR is negligible and the ESL is around 1~2nH. Another part of decoupling capacitors is placed right on the backside of the microprocessor, which is so called packaging capacitors. Because it faces

much higher current slew rate, ESL should be extremely small. Special attention is paid to the design of the packaging capacitors, such as reverse geometry structure. Normally, the value of this kind of capacitor is 1uF and ESL is around 30pH for each piece. Besides these discrete capacitors, there are distributed capacitors integrated with in the microprocessor, which are called on-die capacitors.

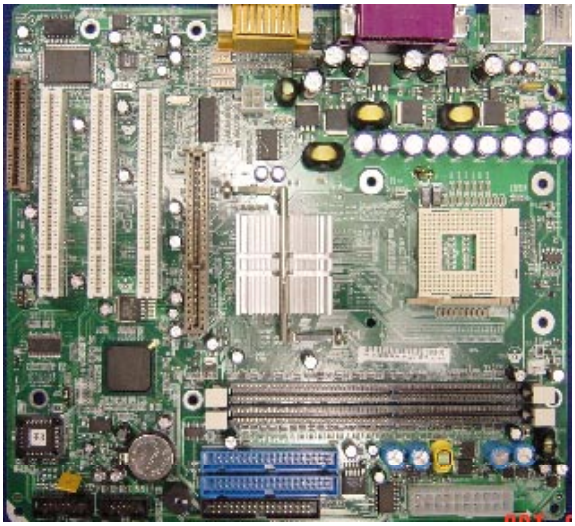


Figure 2-4. A picture of today's motherboard based on Pentium IV microprocessor.

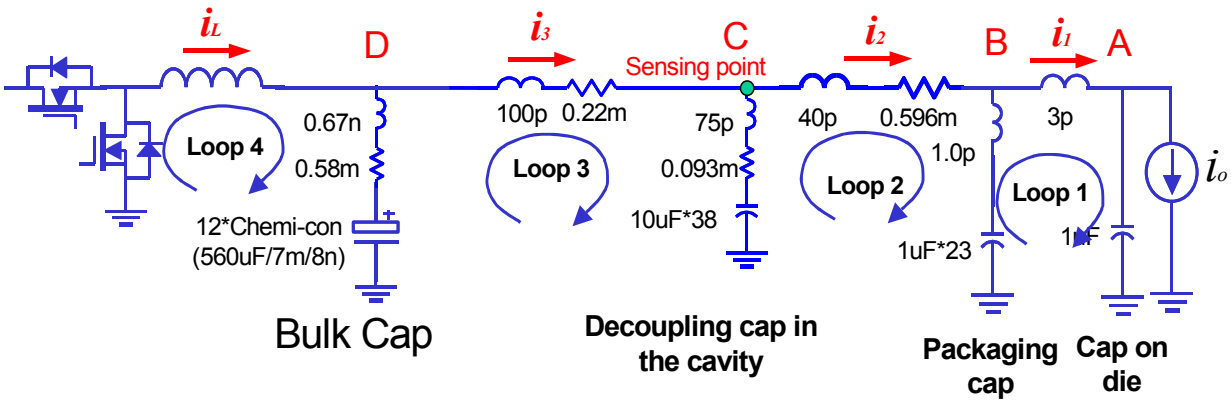


Figure 2-5. The lump model of today's power delivery path. (Supplied by Intel [43])

Its power delivery path model [35] is drawn in Figure 2-5. Compared to the three loops described by Wong, et al. [31], today's power delivery path is somewhat different.

2.2.1. The Current Slew Rate of Each Loop

Figure 2-5 shows that the power delivery path could be separated into four loops. The resonant frequencies of the loops usually have the basic relationship given by $f_1>>f_2>>f_3>>f_4$. As long as there is at least a five-time difference between the loops' resonant frequencies, e. g, $f_1>5f_2$, these loops can be approximately decoupled in the transient analysis. Fortunately, today's power delivery path satisfies the criterion. Therefore, in the current slew rate analysis, each loop can be approximately considered as a second-order system (as shown in Figure 2-6).

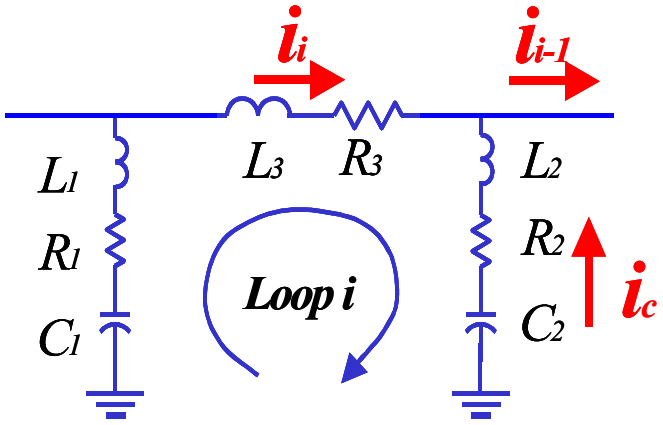


Figure 2-6. Basic cell of each loop.

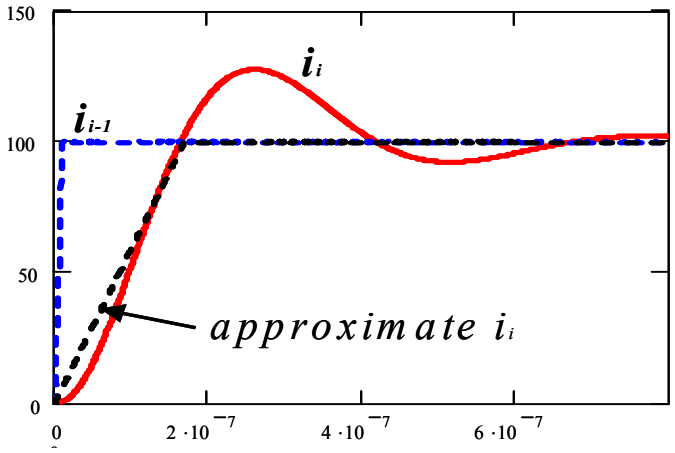


Figure 2-7. The ramp excitation i_{i_1} and response i_i of a system shown in Figure 2-6.

First, it is important to clarify some definitions:

$$L_{eq}=L_1+L_2+L_3;\quad R_{eq}=R_1+R_2+R_3;\quad C_{eq}=\frac{C_1C_2}{C_1+C_2}. \tag{2-1}$$

The expression of the excitation i_{i-1} (shown in Figure 2-7) is:

$$i_{i-1} = SR_{i-1}t - SR_{i-1}(t - t_{r\_i-1})\cdot\Phi(t - t_{r\_i-1}) \tag{2-2}$$

$$i_{i\_ramp}(t) = SR_{i-1}\left(K_1\cdot t + K_2 + 2e^{-\xi\omega t}\left(A\cos\left(\omega\sqrt{1-\xi^2}\cdot t\right) + B\sin\left(\omega\sqrt{1-\xi^2}\cdot t\right)\right)\right), \text{ where} \tag{2-3}$$

$$K_1 = \frac{C_{eq}}{C_2} \quad K_2 = \frac{\frac{-R_{eq}}{C_2} + \frac{R_2}{C_{eq}}}{\left(\frac{1}{C_{eq}}\right)^2},$$

$$A = \frac{2\xi\,\frac{\frac{1}{C_2} - \frac{1}{C_{eq}}\frac{L_2}{L_{eq}}}{L_{eq}} - \omega\,\frac{R_2L_{eq} - R_{eq}L_2}{L_{eq}^2}}{2\,\omega^3},$$

$$B = \frac{\left(4\,\xi^2\omega^3 - 2\,\omega^3\right)\frac{\frac{1}{C_2} - \frac{1}{C_{eq}}\frac{L_2}{L_{eq}}}{L_{eq}} - 2\,\xi\,\omega^4\frac{R_2L_{eq} - R_{eq}L_2}{L_{eq}^2}}{4\,\omega^6\sqrt{1-\xi^2}},$$

$$\xi = \frac{\frac{R_{eq}}{L_{eq}}}{2\sqrt{\frac{1}{L_{eq}C_{eq}}}} \quad \omega = \sqrt{\frac{1}{L_{eq}C_{eq}}}.$$

$$i_i(t) = i_{i\_ramp}(t) - i_{i\_ramp}(t - t_{r\_i-1})\cdot\Phi(t - t_{r\_i-1}) \tag{2-4}$$

where SR_{i-1} is the slew rate of i_{i-1}, t_{r_i-1} is the rise time of i_{i-1}, and Φ is the unit step function. In order to solve the response of i_i to i_{i-1}, the first step is to determine the response of i_i to a ramp change, which is expressed in (2-3). Then, we can easily derive the response of i_i to the excitation (2-2) in terms of i_{i_ramp}, which is expressed in (2-4). Obviously, this process is too complicated. A simplified expression should be explored.

Actually, the rise time of i_i can be simply divided into two parts: One is t_{r_i-1}, the rise time of the excitation i_{i-1}; the other is $\frac{\pi - \arctan\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)}{\sqrt{1-\xi^2}\,\omega}$, the rise time of the second-order system for a step change. If the rise time of the excitation is very small, the slew rate of the response is determined only by the system itself. The step change of the excitation is the extreme case.

The approximation expressions (2-5) and (2-6) are used to simulate the response. In Figure 2-7, the accurate response and the approximate response are compared. The approximate curve is good enough to be used in the following analysis.

$$i_i(t) = SR_i t - SR_i (t - t_{r\_i}) \cdot \Phi (t - t_{r\_i}), \tag{2-5}$$

where

$$t_{r\_i} = \frac{I_o}{SR_i} \quad SR_i = \frac{I_o}{\frac{\pi - \arctan\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)}{\sqrt{1-\xi^2}\,\omega} + t_{r\_i-1}}. \tag{2-6}$$

Based on the expressions shown above, the slew rate of the first three loops can be determined. It is clear that the slew rate is related to the excitation (which includes both slew rate and the amplitude) and the parasitic components of the power delivery path. For different generation microprocessors or different power delivery structures, the slew rate of each loop might change a lot. For example, based on today's power delivery path and microprocessor specification, the following results are derived: for a 10 A/ns at the die side, the results are 10 A/ns for i_1, 450 A/us for i_2, and 50 A/us for i_3. However, if today's power delivery path will still be used for the future microprocessor (2010), the slew rate will change to 120 A/ns at the die side, 66 A/ns for i_1, 4600 A/us for i_2, and 60 A/us for i_3.

2.2.2. The Slew Rate of the VR Inductor Current

In the previous section, the current slew rates for the first three loops have been expressed. In this section, the slew rate of the inductor current in loop 4 is derived. Because the control circuit greatly influences the slew rate of inductor current of the VR, the derivation is different.

2.2.2.1. Critical Inductance Concept [42]

In addressing the inductance design, references [42] propose the concept of critical inductance as a tool to analyze transient response. To achieve fast transient response, VRs tend to use small inductance to accelerate the energy delivery. However, it is not always the case that smaller inductance provides faster transient response. Figure 2-8 shows a simulated result of

voltage spike as a function of inductance, with given control bandwidth f_c. The vertical axis is the voltage spike during transient response and the horizontal axis is the inductance. It can be seen that there is a critical inductance L_{ct} that is the largest inductance that yields the best transient response. When L value is smaller than L_{ct}, the voltage spike is the same regardless of the L value; when L value is larger than L_{ct}, the voltage spike increases as L value increases.

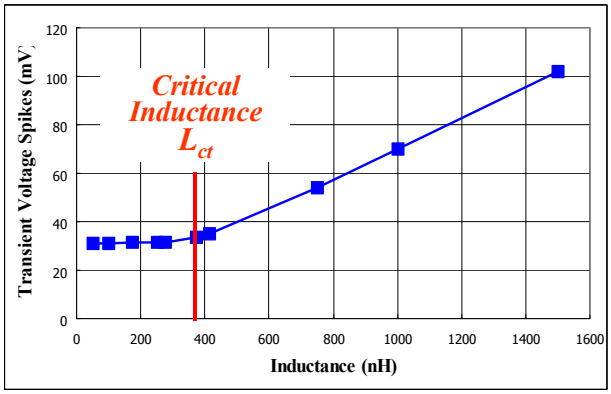


Figure 2-8. Inductances smaller than Lct give the same transient responses; transient voltage spikes increase linearly for inductances larger than Lct (Constant f_c).

The critical inductance is given by

$$L_{ct} = \frac{V_{in}}{4 \cdot \Delta I_o \cdot f_c} \cdot \Delta D_{max} \qquad (2\text{-}7)$$

where V_{in} is the input voltage, ΔI_o is the maximum current change, f_c is the control bandwidth, and ΔD_{max} is the maximum allowed duty cycle change.

Formula (2-7) reveals that the critical inductance is proportional to the maximum allowed duty cycle change during transient response. The duty cycle responds to the load change in two ways: it increases when the load steps up and decreases when the load steps down. For the step up case, the maximum duty cycle change is 1-D. For step down case, the maximum one is D. It is apparent that there are two candidates for the critical inductance as shown in Figure 2-9. Since the critical inductance is the largest inductance that yields the best transient response, it should be the smaller one of the candidates, which results in symmetric transient voltage spike.

If the inductance is designed larger than L_{ct2}, the step-down voltage spike is larger than that of the step-up case. To maintain the same voltage spike magnitude, more capacitance is needed, which results in the output capacitor size and cost increase. This is the penalty for using the large

inductance. In order to avoid the asymmetrical transient waveform, the inductance design in this analysis follows the critical value. At this condition, the duty cycle doesn't go to saturation during transient. Therefore, the inductor current slew rate is fully determined by the control bandwidth.

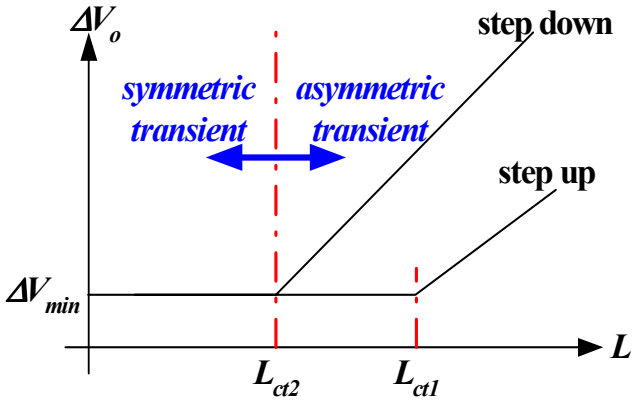


Figure 2-9. Inductances smaller than L_{ct2} give symmetric step-up and step-down transient responses.

2.2.2.2. The Derivation of Inductor Current Slew Rate During Transient

For different control methods, the slew rate of the inductor current changes accordingly. Basically, the control methods are classified into two categories: either voltage-mode control or current-mode control.

Today's VR definitely requires current sharing between each phase and adaptive voltage positioning (AVP), which can be easily realized by current-mode control. Therefore, only current-mode control is studied in the dissertation.

To obtain the relationship between the bandwidth and the inductor current slew rate, the transfer function for the output current to the inductor current ($G_{ii}(s)=i_L/i_o$) should be investigated. Figure 2-10 shows the small-signal block of the VR under AVP control. $G_{ii}(s)$ at the open loop is shown in Figure 2-11. Based on Figure 2-10, the $G_{ii}(s)$ at the closed loop can be derived, as plotted in Figure 2-11. At the open-loop condition, the roll-off slope of $G_{ii}(s)$ is 40 dB/dec. At the closed-loop condition, the roll-off slope changes to 20 dB/dec in a certain range (10kHz~300kHz in Figure 2-11). Therefore, the current transfer function at close loop can be approximated as a first-order system (expressed in (2-8)) at a relatively low-frequency range.

$$G_{ii\_cl}(s) = \frac{1}{1 + \frac{s}{\omega_c}} \tag{2-8}$$

where ω_c is the crossover frequency, which is equal to $2\pi f_c$.

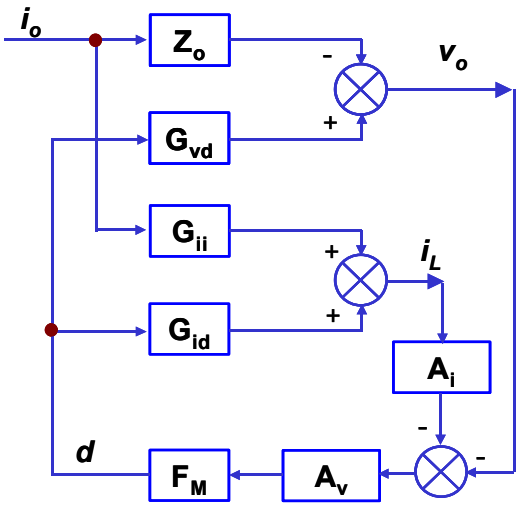


Figure 2-10. The small signal control block of a VR with AVP control realized by current injection method.

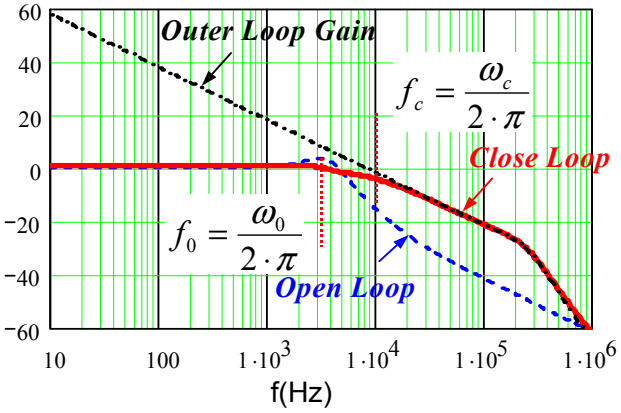


Figure 2-11. The current-transfer function (i_L to i_o) of a VR at open loop and under current-mode control, respectively (refer to Figure 2-10).

The product of $G_{ii}(s)$ and $i_3(s)$ is the inductor current expression in the S domain as follows:

$$i_L(s) = G_{ii}(s) \cdot i_3(s) = G_{ii}(s) \cdot \frac{SR_3}{s^2}\left(1 - e^{-\frac{\Delta I_o}{SR_3}s}\right) \tag{2-9}$$

where SR_3 is the slew rate of i_3.

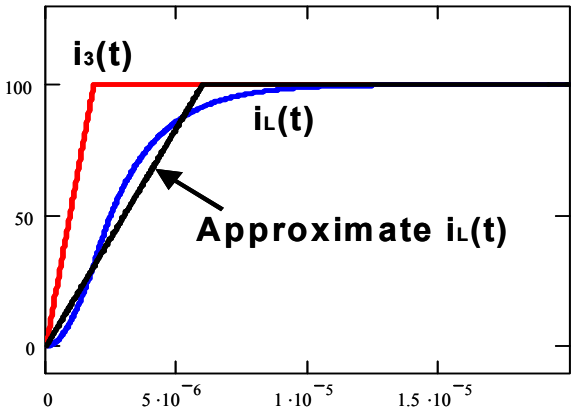


Figure 2-12. The inductor current $i_L(t)$ response to a ramp excitation $i_3(t)$ under current-mode control.

By using an inverse Laplace transformation, the inductor current expression in the time domain (2-10) is determined. Figure 2-12 shows the response of the inductor current to the excitation i_3 with peak current-mode control.

$$i_L(t) = \frac{SR_3}{\omega_c}\left(e^{-\omega_c t} - 1\right) + \frac{SR_3}{\omega_c}\Phi\left(t - \frac{\Delta I_o}{SR_3}\right)\left(1 - e^{-\omega_c\left(t - \frac{\Delta I_o}{SR_3}\right)}\right) + SR_3 t\left(1 - \Phi\left(t - \frac{\Delta I_o}{SR_3}\right)\right) + \Delta I_o \Phi\left(t - \frac{\Delta I_o}{SR_3}\right), \quad (2\text{-}10)$$

Again, this expression is too complicated to be used in the analysis. To simplify the expression, an approximate slew rate expression is derived. The rise time of the excitation, $\Delta I_o/SR_3$, is substituted into (2-10) to calculate the inductor current at that moment. Connecting this point with the origin, an approximate inductor current can be plotted (as shown in Figure 2-12). Compared with the accurate inductor current curve, the approximate expression is good enough to be used in the following analysis.

$$SR_{i_L} = \frac{\frac{SR_3}{\omega_c}\left(e^{-\omega_c \frac{\Delta I_o}{SR_3}} - 1\right) + \Delta I_o}{\Delta I_o} SR_3 \quad (2\text{-}11)$$

By using (2-11), the inductor current is expressed as:

$$i_L(t) = SR_{i_L} t - SR_{i_L}\left(t - \frac{\Delta I_o}{SR_{i_L}}\right)\cdot\Phi\left(t - \frac{\Delta I_o}{SR_{i_L}}\right). \quad (2\text{-}12)$$

2.2.3. The General Expression of the Voltage Spike across the Capacitor

Referring to Figure 2-6, since the slew rate has been derived for each loop, the current through the capacitor (see Figure 2-13) can be easily determined.

There are two intervals for i_c. The first interval starts at t_0 and ends at t_1, and has a positive current slew rate SR_{i-1}-SR_i. The second interval is from t_1 to t_2, and has a negative current slew rate -SR_i. The voltage across the capacitors is given by

$$v_c(t) = i_c(t)\cdot ESR + ESL\cdot\frac{di_c(t)}{dt} + \frac{1}{C}\int_{t_0}^{t} i_c(t)\cdot dt \quad (2\text{-}13)$$

where ESR is the equivalent series resistance (ESR) of the capacitor, ESL is the equivalent series inductance (ESL) of the capacitor, and C is its capacitance. Please note that these values are not for each piece, but the results based on the capacitor paralleling.

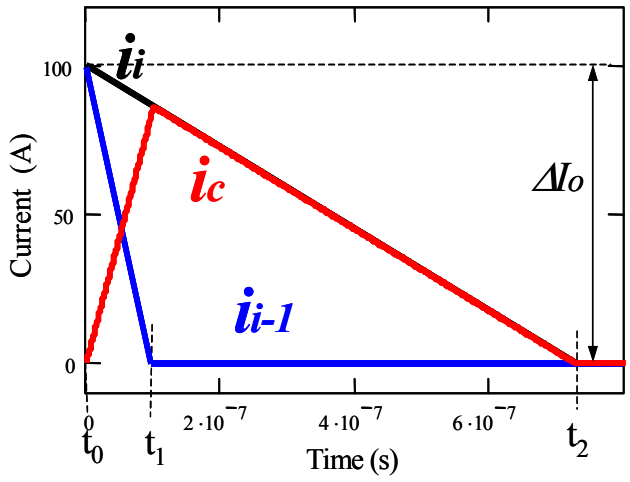


Figure 2-13. The currents' waveforms of loop i: i_{i_1} is the excitation, i_i is the response, and i_c is the current through the capacitors.

The maximum voltage spike could appear not only during t_0 to t_1 but also from t_1 to t_2. Actually, the maximum voltage spike could only appear at the moment t_1 or later than t_1. Based on Figure 2-13 and (2-13), the voltage spike at t_1 can be easily determined as the maximum value during t_0 to t_1. On the other hand, the voltage spike expression and the maximum value during t_1 to t_2 can also be derived based on Figure 2-13 and (2-13). By letting these two maximum voltage spikes be equal, a criterion time (2-14) for loop i can be derived, which is used to judge when the absolute maximum voltage spike appears in the range.

$$t_{criteria} = \frac{\Delta I_o}{SR_{i-1}} + ESR \cdot C + \sqrt{2\frac{SR_{i-1}}{SR_i} ESL \cdot C}, \qquad (2\text{-}14)$$

When the rise time of current i_i is less than or equal to $t_{criteria}$, the maximum voltage deviation always appears at the moment t_1 (see Figure 2-14(a)), such that:

$$v_{o\_max} = \frac{\left(\frac{\Delta I_o}{SR_{i-1}}\right)^2}{2C}(SR_{i-1} - SR_i) + (SR_{i-1} - SR_i)\frac{\Delta I_o}{SR_{i-1}} \cdot ESR + ESL \cdot (SR_{i-1} - SR_i). \qquad (2\text{-}15)$$

That means ESR and ESL of the capacitor determine the voltage spike.

When the rise time of current i_i is greater than $t_{criteria}$ (see Figure 2-14(b)), the maximum voltage deviation appears at a certain moment after t_1, such that:

$$v_{o\_max} = \frac{\left(\frac{\Delta I_o}{SR_{i-1}}\right)^2}{2C} SR_{i-1} + \frac{SR_i \cdot ESR^2 \cdot C}{2} + \frac{\Delta I_o^2}{2C\ SR_i} - \frac{\Delta I_o^2}{C\ SR_{i-1}} - ESL \cdot SR_i \cdot \qquad (2\text{-}16)$$

That means the energy storage dictates the voltage spike.

Figure 2-14 clearly shows that the voltage spike across the capacitor includes three parts: the voltage deviation caused by the ESR, the voltage deviation caused by the ESL, and the voltage deviation caused by the energy storage. The higher the slew rate of i_i, the smaller the voltage deviation caused by energy storage.

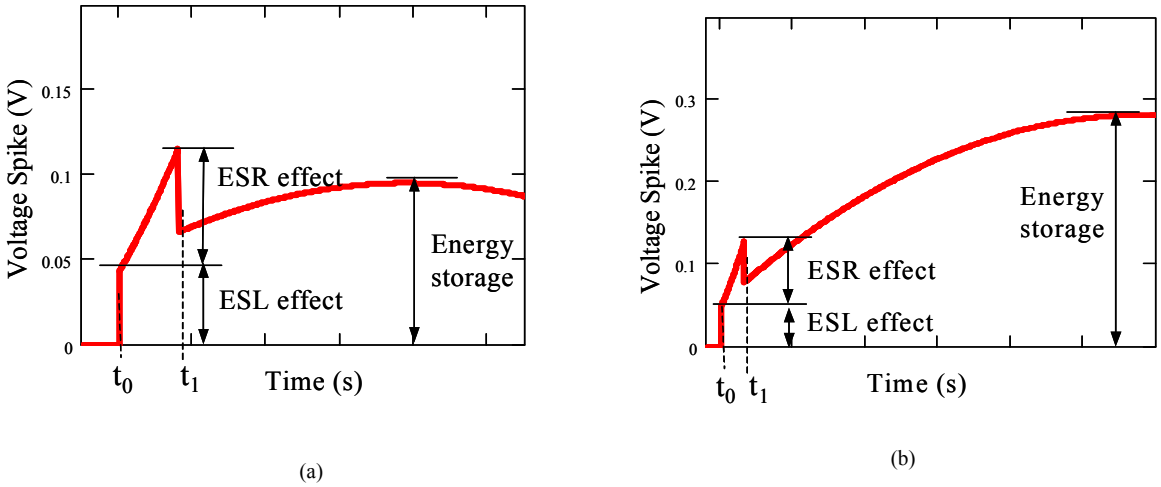


Figure 2-14. The voltage waveform across the capacitor: (a) the maximum voltage deviation appears at t_1 when i_c reaches its peak value, and (b) the maximum voltage deviation appears at a certain moment after t_1.

Based on (2-15) and (2-16), the capacitor number can be easily derived according to the voltage deviation requirement and the specification of the capacitor. It is important to note that the change of the capacitor number also changes the slew rate of the corresponding loops. Therefore, this calculation is iterative.

2.2.4. Critical Bandwidth

In [32], a critical bandwidth concept is proposed to judge when the voltage spike appears and what dictates the spike amplitude. It is valid for low frequency VR design. However, too many assumptions are behind the conclusion. Actually, it is not suitable for the power delivery path analysis at all because ESL effect is ignored and the excitation is treated as a step function only, which is not true.

In the previous section, since the general expression for the voltage spike across the capacitors is derived and the relationship between the bandwidth of the VR and the inductor current slew rate is also established in (2-11), an accurate critical bandwidth can be derived. Combining these expressions also yields the relationship between the bandwidth of VR and the voltage spike across the capacitors.

The judgment as below is used to determine when the voltage spike appears.

$$t_{criteria} = \frac{\Delta I_o}{SR_{i_L}} \tag{2-17}$$

By substituting(2-14) and (2-11) into (2-17), a critical bandwidth of current-mode control is derived as follows:

$$f_{critical} = \frac{\left(ESR \cdot C + \frac{\Delta I_o}{SR_{i-1}} + \frac{ESL \cdot C \cdot SR_{i-1}}{\Delta I_o}\right)}{\pi \left(ESR \cdot C + \frac{\Delta I_o}{SR_{i-1}}\right)^2} - \frac{\sqrt{\left(ESR \cdot C + \frac{\Delta I_o}{SR_{i-1}} + \frac{ESL \cdot C \cdot SR_{i-1}}{\Delta I_o}\right)^2 - \left(ESR \cdot C + \frac{\Delta I_o}{SR_{i-1}}\right)^2}}{\pi \left(ESR \cdot C + \frac{\Delta I_o}{SR_{i-1}}\right)^2}. \tag{2-18}$$

The critical bandwidth is defined: when the bandwidth of the VR is smaller than the critical value, the voltage spike across the capacitor is determined by the energy storage factor. The expression is shown in (2-16). Therefore, it is necessary to parallel more capacitors in order to increase the capacitance so that the voltage specification can be satisfied. When the bandwidth of the VR is greater than the critical value, the ESR and ESL effects determine the voltage spike.

This expression is shown in (2-15). The purpose of paralleling more capacitors is not to achieve a larger capacitance, but to reduce the ESR and ESL.

2.3. Power Delivery Architecture Analysis for Desktop Computer Systems

It is widely known that the performance of microprocessors is becoming more and more powerful. The power consumption requirement could be very different from today's specifications. Therefore, the relationship between the bandwidth of VR and the capacitance will be illustrated according to different microprocessors in this section.

Besides differing microprocessor specifications, the power delivery structure also strongly impacts the relationship between the bandwidth of the VR and the capacitance, by influencing the current slew rate of each loop. This factor will also be taken into account.

2.3.1. Today's Microprocessor with Today's Power Delivery Path

In this section, we are going to use the formula derived as above to investigate the relationship between the bandwidth and the output capacitors. The bulk capacitor is studied first.

2.3.1.1. The Bulk Capacitor of the VR

To get a clear picture and the fundamental results, an assumption is made that the ESL effect of the bulk capacitor is negligible because some ceramic capacitors with small levels of ESL are normally paralleled with bulk capacitors, meanwhile the slew rates of i_3 and i_L are small compared with the slew rates of the die side and socket sensing point. For example, the slew rate of i_3 is 50 A/us and the total ESL (including the ceramic capacitors paralleling with the bulk capacitors) is 200-pH; the voltage deviation due to the ESL is only 10 mV. Compared with the 120 mV voltage window of today's specification, this value is negligible. By assuming the ESL=0, the critical bandwidth can be simplified as follows:

$$f_{criteria\_ESR} = \frac{1}{\pi \left(\frac{\Delta I_o}{SR_3} + ESR \cdot C \right)}. \qquad (2\text{-}19)$$

When the bandwidth of the VR is higher than or equal to the critical value, the maximum voltage deviation appears at the moment when the load current reaches its maximum value (see

Figure 2-15(a) and (b)). In this case, the ESR of the capacitors determines the maximum voltage deviation. By simply substituting ESL=0 into (2-15), the maximum voltage spike is expressed as

$$v_{o\_\max} = \frac{\left(\frac{\Delta I_o}{SR_3}\right)^2}{2C}\left(SR_3 - SR_{i_L}\right) + \left(SR_3 - SR_{i_L}\right)\frac{\Delta I_o}{SR_3}\cdot ESR \quad . \tag{2-20}$$

And the capacitor number at this condition is easily derive according to (2-20) as:

$$N = \frac{\left(\frac{\Delta I_o}{SR_3}\right)^2}{2C_{piece}\Delta V_o}\left(SR_3 - SR_{i_L}\right) + \left(SR_3 - SR_{i_L}\right)\frac{\Delta I_o ESR_{piece}}{SR_3 \Delta V_o} \tag{2-21}$$

where C_{piece} and ESR_{piece} are the capacitance and ESR for each piece, respectively. ΔV_o is the maximum voltage deviation given by the specification.

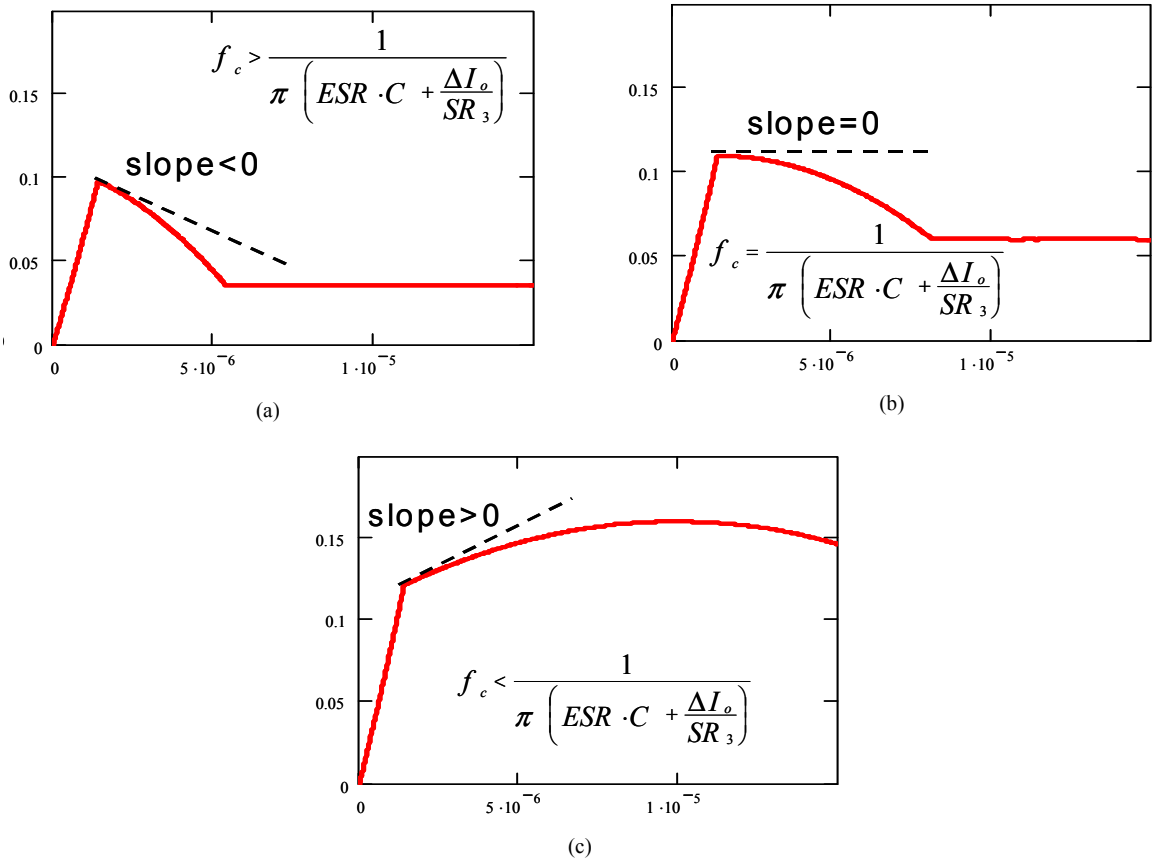


Figure 2-15. The voltage deviation at different bandwidth design: (a)$f_c > f_{criteria\_ESR}$, (b) $f_c = f_{criteria\_ESR}$, and (c) $f_c < f_{criteria\_ESR}$.

When the bandwidth of the VR is lower than the critical value, the maximum voltage deviation appears at a certain moment after the load current reaches its maximum value (see Figure 2-15(c)). In this case, the energy storage is dominant. In other words, the capacitance should be increased in order to reduce the voltage deviation. By substituting ESL=0 into (2-16), the maximum voltage spike is expressed as

$$v_{o\_\max} = \frac{\left(\frac{\Delta I_o}{SR_3}\right)^2}{2C} SR_3 + \frac{SR_{i_L} \cdot ESR^2 \cdot C}{2} + \frac{\Delta I_o^2}{2C\ SR_{i_L}} - \frac{\Delta I_o^2}{C\ SR_3}. \qquad (2\text{-}22)$$

At this condition, the capacitor number is given by

$$N = \frac{\left(\frac{\Delta I_o}{SR_3}\right)^2}{2C_{piece}\Delta V_o} SR_3 + \frac{SR_{i_L} ESR_{piece}^2 C_{piece}}{2\ \Delta V_o} + \frac{\Delta I_o^2}{2C_{piece} SR_{i_L} \Delta V_o} - \frac{\Delta I_o^2}{C_{piece} SR_3 \Delta V_o}. \qquad (2\text{-}23)$$

Based on the capacitor number expressions (2-21) and (2-23), the inductor current slew rate expression (2-11), and the current slew rate of i_3, the relationship between the number of bulk capacitor and the bandwidth can be plotted. Figure 2-16 shows the bandwidth vs. the output bulk capacitor number at the condition of Io=100A and with today's power delivery structure. As the bandwidth increases, the capacitor number is continually reduced. This is a big motivation for high-frequency VRs.

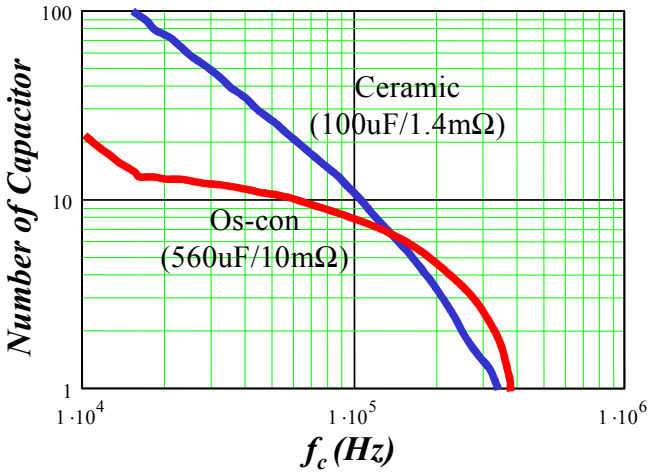


Figure 2-16. The bandwidth vs. the bulk capacitor number based on today's power delivery path.

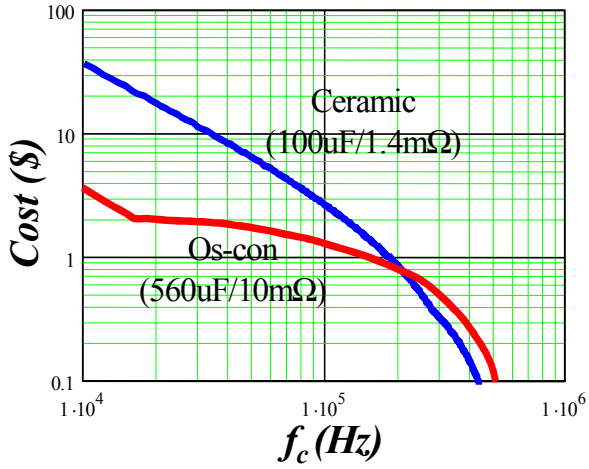


Figure 2-17. The bandwidth vs. the cost of bulk capacitors based on today's power delivery path.

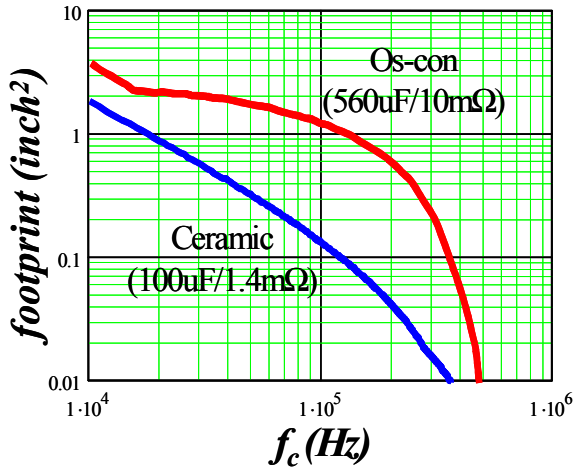


Figure 2-18. The bandwidth vs. the footprint of bulk capacitors based on today's power delivery path.

As long as the amount of capacitor is derived, the cost and footprint between different bulk capacitors can be compared to determine which one is more cost-effective and which one occupies less real estate of the motherboard. For example, Figure 2-17 illustrates the cost comparison between the TDK 100uF/1.4mΩ ceramic capacitor and the Electrolytic capacitor Os-con (560uF/10mΩ). The ceramic capacitor is around 0.25 cents for each piece and Os-con capacitor is 0.15 cents for each piece at the middle of year 2004. Below 200kHz bandwidth, the Os-con capacitor is cheaper while the ceramic capacitor is more cost-effective beyond 200kHz bandwidth. Because the cost is always changing, this bandwidth is also moving correspondingly.

From the footprint wise (as shown in Figure 2-18), the ceramic capacitor (1210 form factor) is always smaller. Therefore, the bulk capacitor should switch from Os-con capacitor to the ceramic capacitor when the bandwidth is beyond 200kHz.

Another very interesting phenomenon can also be observed in Figure 2-16: When the bandwidth is pushed to a certain value, the output bulk capacitor can be eliminated no matter whether Os-con capacitors or ceramic capacitors are used. Actually, a 300kHz~400kHz bandwidth is already high enough to get rid of the bulk capacitors, because the slew rate of the inductor current is already very close to that of the current demand i_3.

2.3.1.2. The Cavity Capacitors

In contrast to the bulk capacitor, the decoupling capacitor in the cavity of the socket faces a much higher current slew rate demand. For example, the slew rate at the sensing point of the socket is around 450 A/us, and this value will be even higher for future specifications (4~5 A/ns). Referring to Figure 2-5, the total ESL and parasitic inductance of the cavity capacitors is around 75pH, which results in 33.5mV voltage spike for 450A/us current slew rate. Therefore, the ESL of the decoupling capacitor plays an important role in the design and cannot be ignored any more.

Following the expressions (2-15) and (2-16) used for the general voltage spike analysis, the amount of the decoupling capacitors are given by

At $f_c \geq f_{critical}$,

$$N = \frac{\left(\frac{\Delta I_o}{SR_2}\right)^2}{2C_{piece}\Delta V_o}\left(SR_2 - SR_{i_L}\right) + \left(SR_2 - SR_{i_L}\right)\frac{\Delta I_o ESR_{piece}}{SR_2 \Delta V_o} + \frac{ESL_{piece}\left(SR_2 - SR_{i_L}\right)}{\Delta V_o} \tag{2-24}$$

And at $f_c < f_{critical}$,

$$N = \frac{\left(\frac{\Delta I_o}{SR_2}\right)^2}{2C_{piece}\Delta V_o} SR_2 + \frac{SR_{i_L} ESR_{piece}^2 C_{piece}}{2\,\Delta V_o} + \frac{\Delta I_o^2}{2C_{piece} SR_{i_L} \Delta V_o} - \frac{\Delta I_o^2}{C_{piece} SR_2 \Delta V_o} - ESL_{piece} SR_{i_L} \tag{2-25}$$

where ESL_{piece} is the ESL for each piece. Please be aware that these expressions are valid after the bulk capacitors are eliminated.

Based on (2-24) and (2-25), the relationship between the quantity of the decoupling capacitors (10uF/3.5mΩ/1.5nH) and the bandwidth are plotted as Figure 2-19. Below 350-kHz bandwidth, there is no change of the decoupling capacitance, because the bulk capacitors haven't been eliminated. Beyond 350kHz bandwidth, a higher bandwidth means a smaller decoupling capacitance. As the bandwidth increases, the decoupling capacitance is reduced. There is a little

notch around 1MHz bandwidth, which is caused by ESL of the capacitors. Beyond this point, the voltage spike caused by ESL overwhelms that of the energy storage.

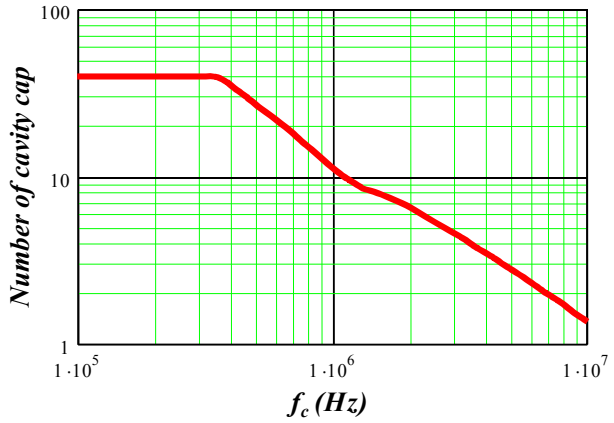


Figure 2-19. The bandwidth vs. the number of decoupling capacitors in the cavity of socket.

It is very difficult to eliminate the decoupling capacitors. Figure 2-19 shows that the decoupling capacitance cannot be eliminated until 10MHz bandwidth. Regardless, it is still worthwhile to push bandwidth in order to reduce the decoupling capacitors.

2.3.1.3. Cost Breakdown of Today' VR

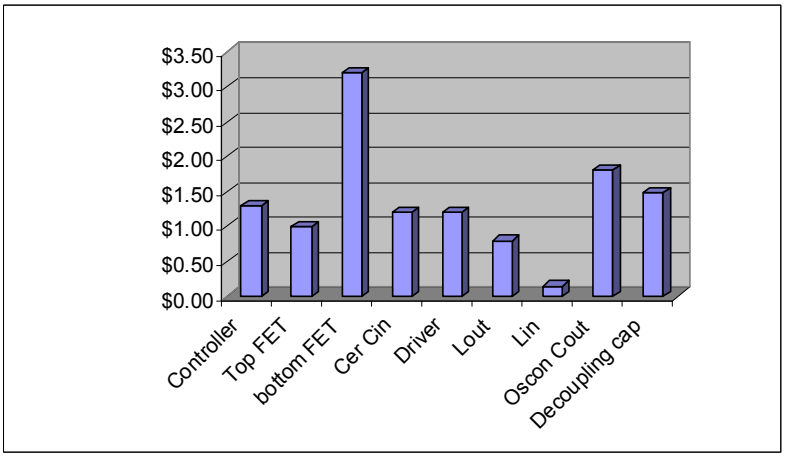


Figure 2-20. A typical cost breakdown of today's VR (1.3V/100A) based on cost information in 2004.

Today's VR is operating at 300-kHz and the bandwidth is designed at around 40~50-kHz. From Figure 2-16 and Figure 2-17, it can be seen that the Os-con capacitor is cheaper and the amount is around $12. There are 40 pieces of decoupling capacitors surrounding the socket and in the cavity of socket. Figure 2-20 shows the cost breakdown of today's 4- phase VR

(1.3V/100A). It is clear that output capacitors (both Os-con capacitors and the decoupling capacitors) are one of the most expensive parts. As predicted, if the bandwidth can be pushed up to 350-kHz to eliminate the bulk capacitors, the cost is reduced by 15%. Therefore, even for today's VR, there is a motivation for high frequency.

2.3.2. Future Microprocessor based on Today's Power Delivery Path

Future generation microprocessors are expected to operate at much lower voltages (0.7-1V) and to draw much higher currents (shown in Figure 1-2) with high di/dt dynamic characteristics (shown in Figure 1-3). Accordingly, VR will have to meet increasing challenges such as higher conversion efficiency, tighter voltage tolerances, and faster transient responses. 0.8V/150A is defined as the output specification of the future microprocessor. And its current slew rate is 120A/ns. The analysis methodology is exactly same as that in section 2.3.1.

First, the current slew rate of each loop is derived as shown in Figure 2-21. It can be seen that excited by such a high slew rate load, the di/dt for loop 1 is 66A/ns, the di/dt for loop 2 is 4.6A/ns and the di/dt for loop 3 is 60A/us. Generally speaking, the current slew rate will be much higher than that of today's specification. However, the di/dt for loop 3 doesn't increase much because the decoupling capacitors in loop 1 and loop 2 supply the majority of the high frequency energy and significantly reduce the burden for the electrolytic capacitors.

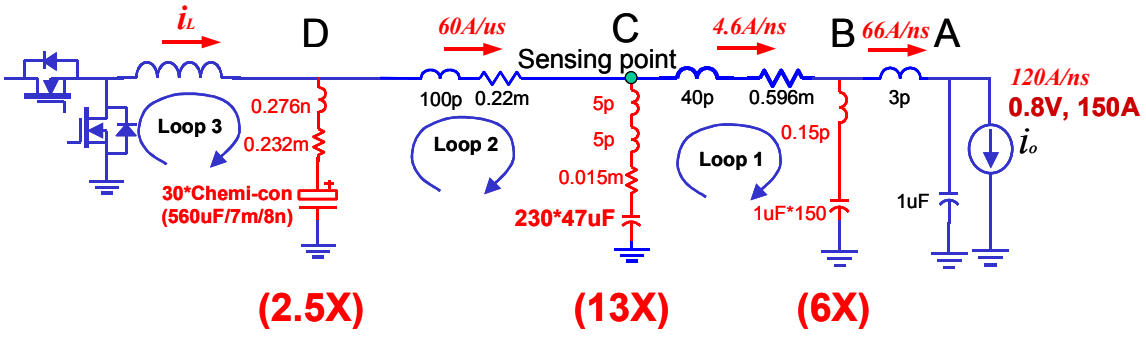


Figure 2-21. Future microprocessor demands much more capacitors if today's solution is followed.

Without fundamental change of the current power delivery architecture and following today's low frequency (300kHz~500kHz) and low bandwidth (40~50kHz) VR solution, it is expected that the amount of output capacitors will increase 2.5 times for bulk capacitors, 13 times for decoupling capacitor surrounding the socket and in the cavity of socket, and 6 times for

packaging capacitors on the backside of the CPU. This alone will result in 6.4 times increase in terms of capacitor cost (refer to Figure 2-22). Because the packaging capacitor is a part of microprocessor, its cost is not included. Meanwhile, the bulky VR will occupy over 30% of the real estate (shown in Figure 2-23) of the motherboard compared to 12% with today's VR design.

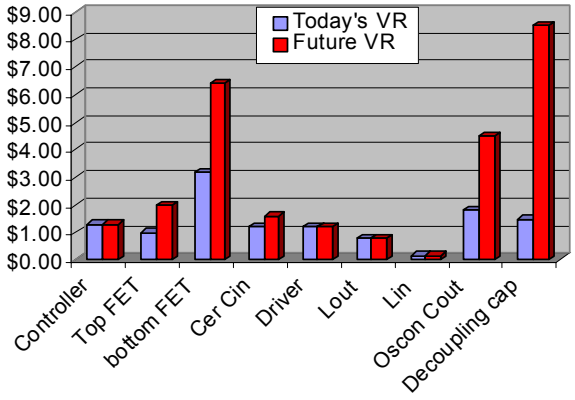


Figure 2-22. Cost estimation of future VRs with a huge capacitor increase.

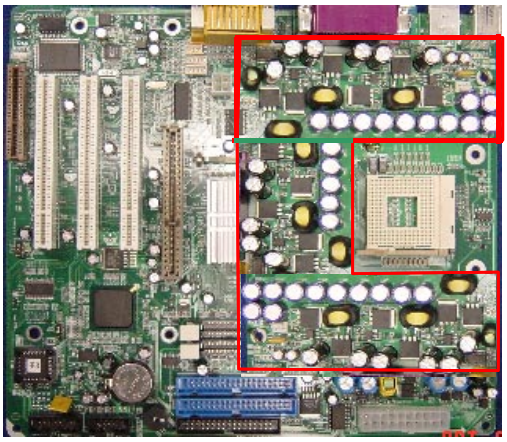


Figure 2-23. Conceptual drawing of future motherboard with a huge VR.

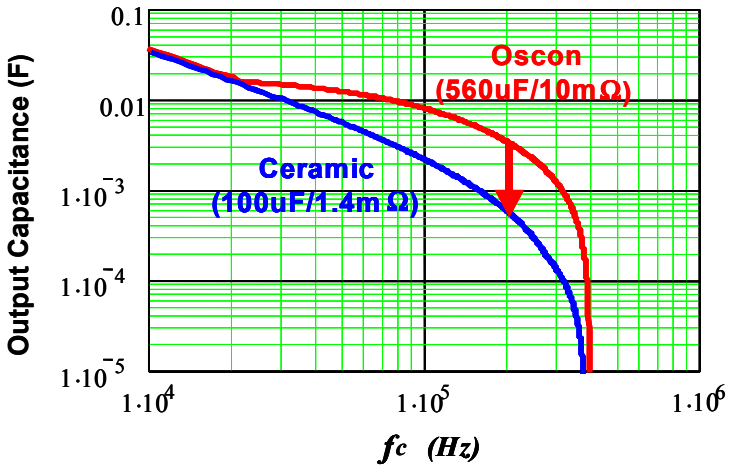


Figure 2-24. The relationship between the bandwidth of VR and the output bulk capacitance for the future microprocessors based on today's power delivery path.

Following the analysis in section 2.3.1, the relationship between the bandwidth of VR and the bulk capacitance is shown in Figure 2-24. It is apparent that to overcome the aforementioned challenges, the bandwidth of the VR should be pushed to reduce the output capacitance. There are several targets described as follows.

As the bandwidth increases, both the ceramic capacitor and the electrolytic capacitor decrease, although the trajectory is different. The cost and footprint are compared again. Figure 2-25 shows the bandwidth vs. the cost of different capacitors. Two curves cross over at 200-kHz bandwidth, which means the ceramic capacitor is more cost-effective beyond the 200-kHz bandwidth. Meanwhile, the footprint comparison in Figure 2-26 illustrates that the ceramic capacitor is always smaller. Therefore, it is desired to switch the bulk capacitor from an electrolytic Os-con capacitor to a ceramic one. Assuming $f_c=1/6*f_s$, the switching frequency of VR needs to reach 1.2MHz. This is a challenge for today's synchronous multi-phase buck converter design.

350-kHz bandwidth is the second target. At this bandwidth, the bulk capacitors can be completely eliminated, which means a lot of saving in the cost and real estate of the motherboard. As predicted, the cost can be saved by 17%. To realize this objective, the VR needs to operate at 2-MHz. This is even more challenging for VR design.

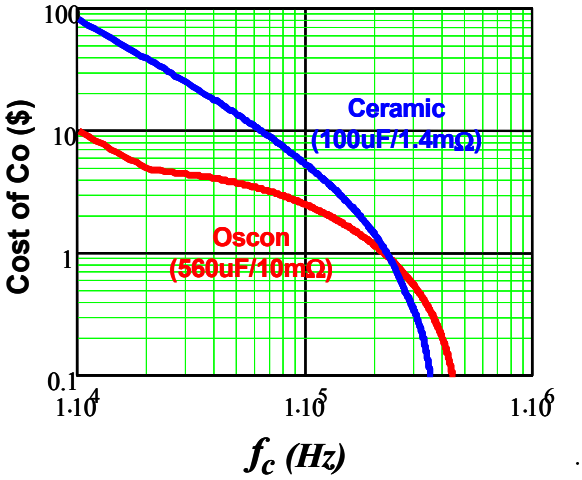


Figure 2-25. The bandwidth vs. the cost of bulk capacitors for the future microprocessors based on today's power delivery path.

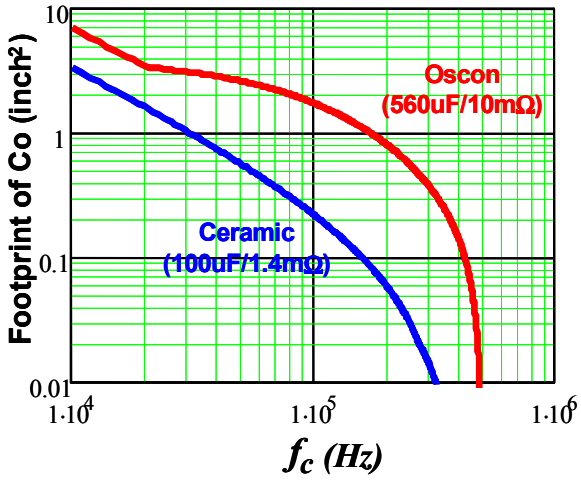


Figure 2-26. The bandwidth vs. the footprint of bulk capacitors for the future microprocessors based on today's power delivery path.

After the bulk capacitor is eliminated, the decoupling capacitors in the cavity and surrounding the socket are directly used as the output capacitors of VRs. Figure 2-27 shows the relationship between the bandwidth of VR and the output decoupling capacitance. It illustrates that 650kHz bandwidth (4MHz-switching frequency) is the third target. At this point, the amount of decoupling capacitors in the cavity can be reduced from 230 to 50. In other words, the cost

can be further reduced by 25%. This saving is even larger than that of the bulk capacitor elimination. Beyond this frequency, because the ESL and the interconnection parasitics dramatically hinder the capacitance reduction as the bandwidth increases, it is not necessary to push the bandwidth even higher as long as today's power delivery structure is still in use. However, 50 pieces of decoupling capacitors are still too many to fit into the cavity of the socket. We have to further reduce the capacitance, which will be discussed in Chapter 5.

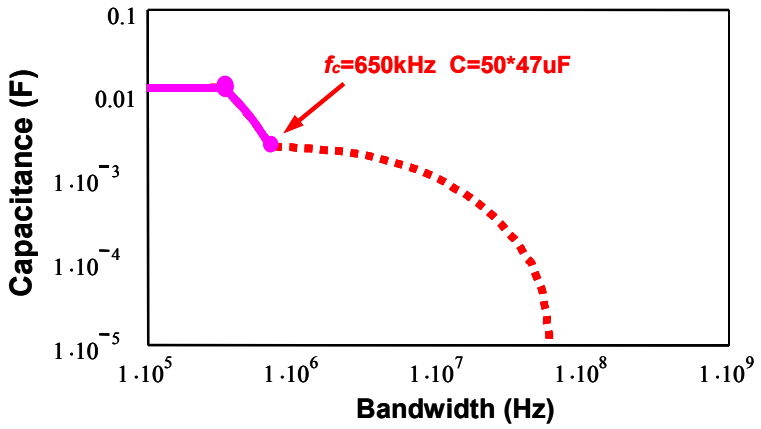


Figure 2-27. The relationship between the bandwidth of VR and the output decoupling capacitance in the cavity and surrounding the socket.

Basically, Figure 2-24 and Figure 2-27 draws a big picture of the high switching frequency VR roadmap. They clearly show the benefits of high frequency and high bandwidth design.

2.3.3. Experimental Verification

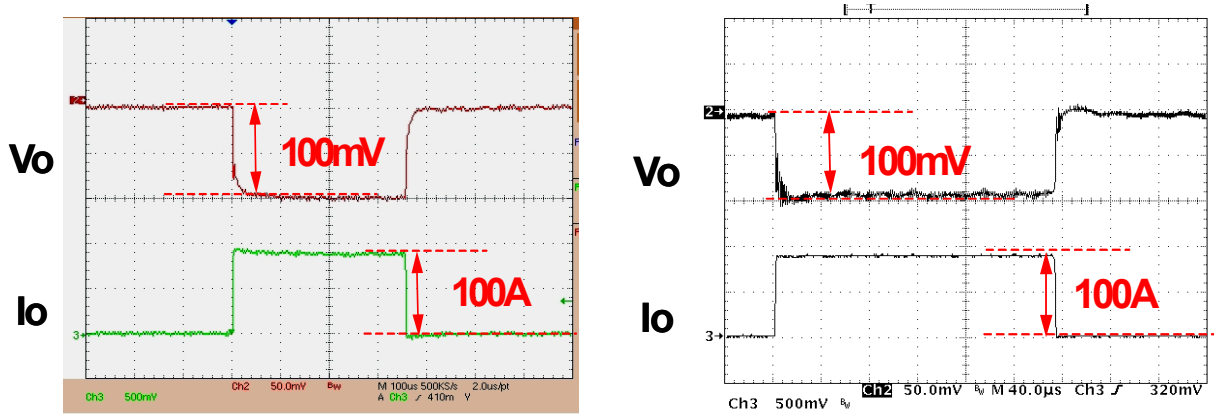
The relationship between the bandwidth of VR and capacitance has been illustrated in Section 1.2 and 1.3. To verify the analysis results based on today's microprocessor and power delivery path, hardware is built and tested.

As shown in Figure 2-16, to significantly reduce the bulk capacitance, the bandwidth should be pushed to beyond 350 kHz, which means the switching frequency is around 2-MHz if the assumption $f_c=1/6*f_s$ is made. Fortunately, a two-stage approach [36] (will be discussed in Chapter 3) developed in CPES (Figure 2-28) has reached such a high frequency, thus affording the opportunity to get rid of the bulk capacitors. The first stage runs at 300 kHz and only steps down the input voltage from 12-V to 5-V. The second stage operates at 2-MHz so that the

stringent transient requirements can be met. The output specification is 1.2-V/100-A. The current slew rate is 450-A/us. The top switch is HAT2168; the bottom switch is Si4864; the driver is LM2726; the output inductor is 50 nH for each phase; and the controller is Intersil ISL6561, which is so far the only controller that can reaches the 350-kHz bandwidth for VR. The bulk capacitance is determined by the bandwidth design. The decoupling capacitance is 40*10uF.

Figure 2-28. The picture of a two-stage prototype.

First, the 560uF/10mΩ Os-con capacitor is chosen as the bulk capacitors of the VR. The transient response results for the 25kHz bandwidth and 200kHz bandwidth cases are shown in Figure 2-29.

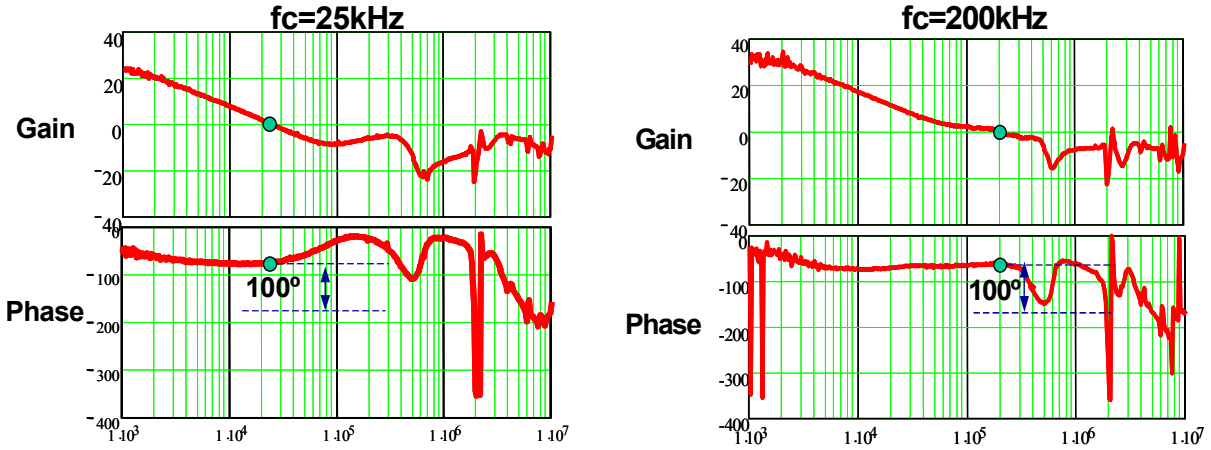


(a) (b)

Figure 2-29. The transient responses with 560uF/10mΩ Os-con capacitor design: (a) f_c=25kHz with ten Os-con; (b) f_c=200kHz with six Os-con.

In the 25kHz bandwidth case, ten Os-con capacitors are used. Six Os-con capacitors are used in the 200kHz bandwidth case. The voltage spikes in both cases meet the 100mV voltage

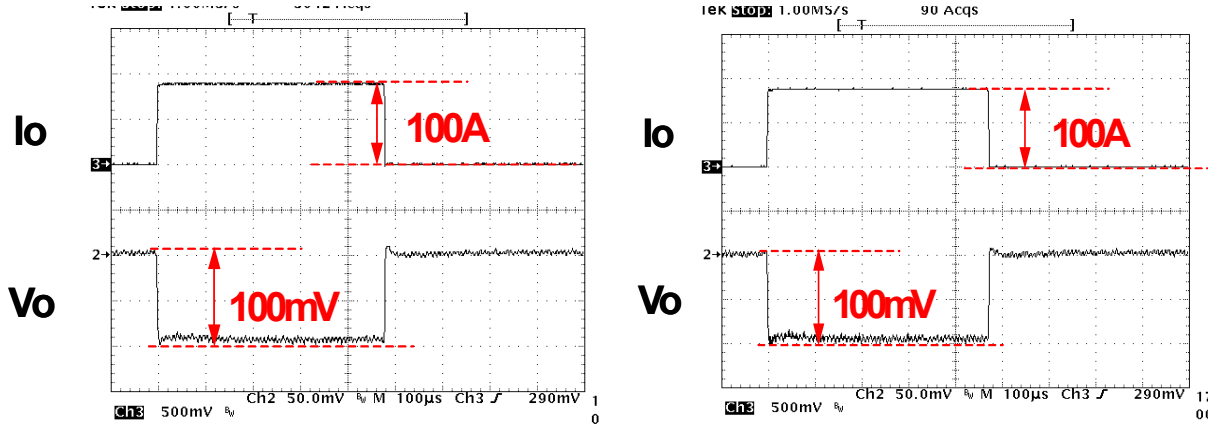
deviation requirement, which shows that the reduction is not that significant by pushing the bandwidth from 25kHz to 200kHz. The reason, as analyzed before, is the large ESR of Os-con capacitor. The measured loop gains of the system are shown in Figure 2-30. Both of them have sufficient phase margin to guarantee the system stable.



(a) (b)

Figure 2-30. The measured loop gain: (a) f_c=25kHz with ten Os-con capacitors; (b) f_c=200kHz with six Os-con capacitors.

The 100uF/1.4mΩ TDK ceramic capacitor is also tested in order to verify the analysis. The transient response results of the 200kHz bandwidth and 330kHz bandwidth cases are shown in Figure 2-31.



(a) (b)

Figure 2-31. The transient responses with 100uF/1.4mΩ ceramic capacitor design: (a) f_c=200kHz with four ceramic capacitors; (b) f_c=330kHz with no ceramic capacitor.

In the 200kHz bandwidth case, four ceramic capacitors are used. In the 330kHz bandwidth case, the bulk capacitor is eliminated. The voltage spikes in both cases can meet the 100mV voltage deviation requirement. The loop gains of the system are shown in Figure 2-32.

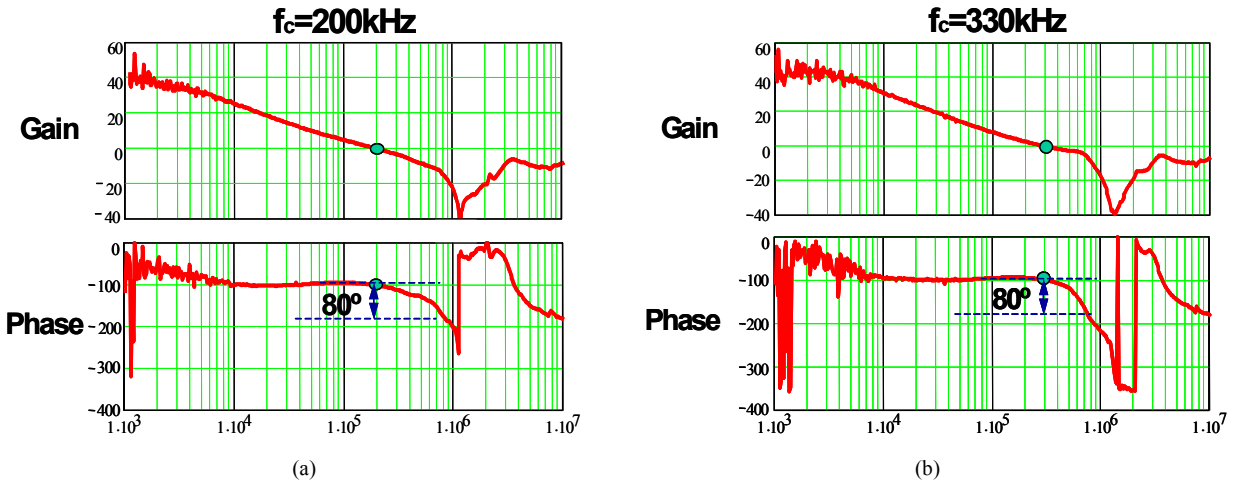


Figure 2-32. The measured loop gain: (a) f_c=200kHz with four 100uF ceramic capacitors; (b) f_c=330kHz with no 100uF ceramic capacitor.

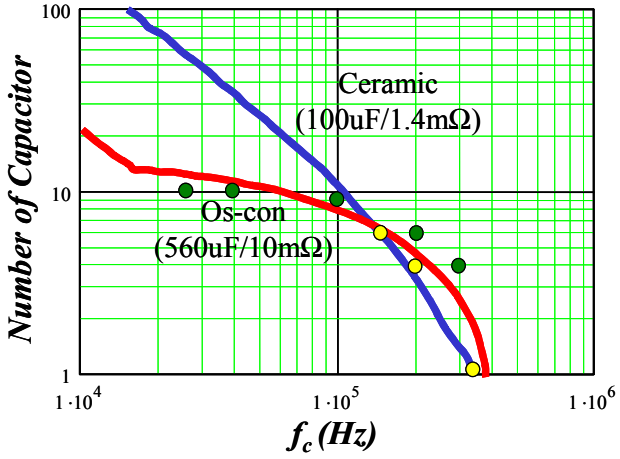


Figure 2-33. The verification of the relationship between the bandwidth and the bulk capacitor number.

Figure 2-33 shows the relationship between the bandwidth and the capacitor number. The curves are the analysis results, which are the same as those in Figure 2-16, and the dots are the experimental results. They match very closely. As expected, the reduction of Os-con capacitors is hindered in a certain range because of its large ESR. After this range, the reduction resumes and is even faster than does the ceramic capacitor. At around 350-kHz bandwidth, both of them can be eliminated. Only 400-uF decoupling capacitors are sufficient to deal with the transient.

As a conclusion, the bandwidth of VR is the key to reduce the output capacitance. Is today's VR able to reach such a high switching frequency?

2.4. The Limitations of Current Approach

The previous sections have pointed out that high switching frequency helps to reduce output capacitance, but the feasibility of high frequency solutions is limited by VR efficiency. Presently working with 12V input, the multiphase buck VR has historically worked with different input voltages. When CPUs are demanding 2V or so core voltage and 10, 20A core current, VRs work with 5V input. Later on when CPUs are demanding sub 1V core voltage and much higher core current, VRs work with 12V input to reduce the distribution loss. While a typical 5V input VR has efficiency in the range of 90%, a typical 12V input VR has efficiency in the range of 80%. This downgrading in efficiency is in the opposite direction of the VR efficiency requirement for the future. Can 2 MHz be reached based on today's single-stage multi-phase buck converter while maintaining the same efficiency as the low frequency case to eliminate the bulk capacitors?

A multiphase synchronous buck converter running at 300kHz and 1-MHz is used as an example to estimate the loss. It is a four-phase buck converter with one HAT2168 as the top switch and two HAT2165 as the bottom switch for each phase. Vin=12V, Vo=0.8-V and Io=70-A. The efficiency degrades around 5% from 300kHz to 1MHz as shown in Figure 2-34. It will be even worse when the switching frequency reaches 2-MHz. What is the reason?

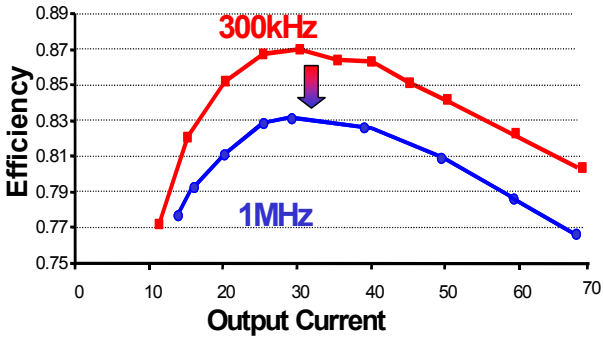


Figure 2-34. Conventional VRs' efficiency suffers a lot as the switching frequency increases.

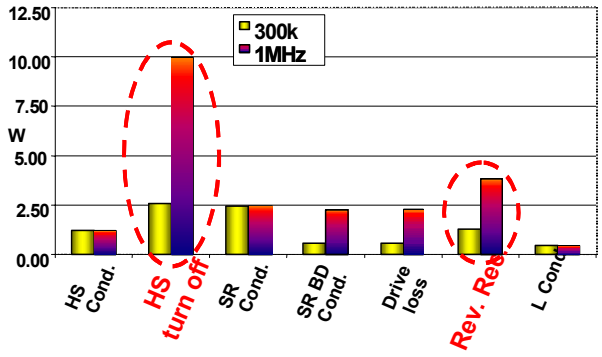


Figure 2-35. Loss breakdown of a conventional VR with Vin=12V, Vo=0.8V and Io=70A.

Based on the loss analysis shown in Figure 2-35, it is clear that high switching loss, especially the turn off loss, and high body diode loss are the dominant factors. In addition, driver loss and body diode conduction loss are becoming more and more significant as the switching frequency increases. Then, what contributes the high switching loss and body diode loss?

As we know, the duty cycle of a buck converter is given by

$$D = \frac{V_o}{V_{in}} \tag{2-26}$$

where V_o is the output voltage and V_{in} is the input voltage. For example: for Vo=1.5V, the duty cycle is 1.5/12=0.125 for a 12V-input buck VR (as shown in Figure 2-36), as opposed to 0.3 for a 5V-input buck VR. It can be seen that after the VR input voltage switches from 5V to 12V, the buck VR needs to work with a much smaller duty cycle due to the large step-down ratio. This extreme duty cycle makes it difficult to design an efficient buck converter.

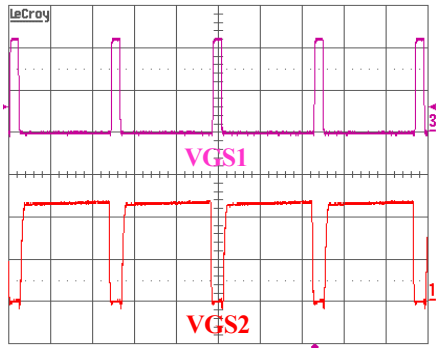


Figure 2-36. Gate signal of the top switch (top waveform) and the bottom switch (bottom waveform).

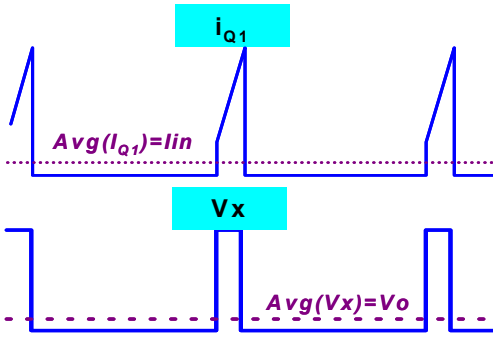


Figure 2-37. The waveforms of the current through the top switch and the voltage across the bottom switch.

Figure 2-37 draws the current through the top switch and the voltage across the bottom switch. The peak current value of switch Q_1 is expressed as

$$I_{Q1\_pk} = I_o + \frac{V_o \cdot (1 - D)}{2 f_s L} \tag{2-27}$$

where I_o is the output average current, T_s is the switching period, L is the output inductance, and V_o is the output voltage. It can be seen that as the duty cycle reduces, the turn-off current of the top switch is larger. And therefore the turn-off loss is larger. The turn-off loss of the top switch is roughly given by

$$P_{turn-off} = I_{Q1\_pk} V_{off\_stress} \tau_{off} f_s \quad (2\text{-}28)$$

where τ_{off} is the commutation time between the voltage across the switch and the switching current when the device turns off, V_{off_stress} is the turn-off voltage stress of Q_1, and f_s is the switching frequency. It is understandable that the higher input voltage and larger turn-off current; more commutation time is needed. More accurate loss expressions are discussed in the appendix. From these equations, it is clear that the turn off loss is strongly influenced by the input voltage not only in terms of V_{off_stress}, but also the turn off peak current as expressed in (2-27) and the commutation time.

In addition, the top switch turn on loss is directly relevant to the input voltage.

$$P_{turn-on} = I_{Q1\_valley} V_{in} \tau_{on} f_s \quad (2\text{-}29)$$

where τ_{on} is the commutation time between the voltage across the switch and the switching current when the device turns on, I_{Q1_valley} is the valley value of inductor current. Again, the input voltage dramatically impacts the turn-on loss of top switch in terms of V_{in} and commutation time.

Besides the switching loss of the top switch, the body diode reverse-recovery loss of the bottom switch is also related to the input voltage, as expressed in (2-30):

$$P_{bd\_rr} = V_{in} Q_{rr} f_s \quad (2\text{-}30)$$

where Q_{rr} is the reverse-recovery charge of the body diode. For a given circuit layout, the loop parasitic inductance is fixed. Hence, higher input voltage means high current slew rate during the commutation between top switch and bottom switch, which usually results in larger Q_{rr}. So, lowering down the input voltage yields smaller body diode reverse recovery loss.

Compared with today's 12-V input, lower input voltage is more desirable in the high-frequency application. In the following chapters, how to realize a high frequency high efficiency VR will be discussed in detail.

2.5. Summary

Fast-developing microprocessor places big challenges for VR design. To meet future VR specifications, more and more output capacitors have to be paralleled if today's low-frequency

solution is followed. In order to reduce the output capacitance, the bandwidth of the VR should be pushed. This chapter addresses the relationship between the bandwidth and the output capacitance.

Based on the power delivery path model, the current slew rate of each loop is derived. Therefore, the unbalanced charge going through the capacitors of each loop and the voltage spike across the capacitors can be easily obtained. Then, the relationship between the inductor current slew rate and the control bandwidth is derived. Based on these results, curves illustrating the relationship between the voltage spike across each loop's capacitors and the control bandwidth are plotted. The analysis results show that as long as the bandwidth can reach around 350 kHz, the bulk capacitor of the VR can be completely eliminated, which means significant savings in cost and real estate. A prototype based on the two-stage approach verifies the analysis results.

Continuously pushing the bandwidth of VR is able to reduce the decoupling capacitance in the cavity. Analysis results indicate that 650kHz bandwidth can reduce the number of the decoupling capacitor from 230 to 50 for future microprocessor case. Beyond 650kHz, the reduction is not significant any more due to the parasitic components along the power delivery path.

Basically, a big picture of the future power management for the microprocessor in the desktop application has been drawn. However, today's solution lacks high frequency capability because of its high switching loss and high body diode losses. The following chapters will discuss how to accomplish these goals proposed in this chapter through alternatives.

As a summary of this chapter, future microprocessor development puts a lot of challenges in VR design. Today's approaches are not suitable any more. New solutions need to be explored.

Chapter 3. Two-Stage Approach for Future Microprocessors

3.1. Introduction

Today's microprocessors for the desktop computer are becoming more and more powerful, and their power consumptions are dramatically increasing. As a result, VR design has become a serious challenge as the microprocessor is developing so quickly. In the near future, the output voltage will be less than 1 V while the output current will increase up to 150 A. Additionally, the current slew rate at the sensing point of the socket will reach 4~5 A/ns as compared with the 450 A/us of today. Meanwhile, the voltage deviation window will be less than 100 mV for such a high di/dt load change.

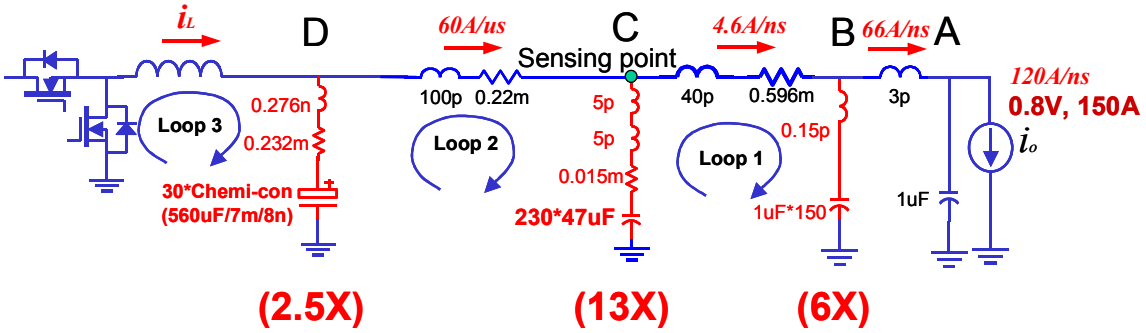


Figure 3-1. Future microprocessor demands much more capacitors if today's solution is followed.

Today's desktop VR normally runs at 300~500 kHz. To meet 100mV voltage droop @ 1.3V/100A and 450A/us output requirement, 10 Os-con capacitors are paralleled as bulk capacitors and 40*10uF 1206 case ceramic capacitors are used as decoupling capacitors. If such a low-frequency solution is followed, more and more capacitors have to be paralleled to satisfy the stringent requirements of the future microprocessors. Based on the analysis in the previous chapter (as shown in Figure 2-21), the number of the bulk capacitors will increase up to 30, and the number of the decoupling capacitors on the MB will increase up to 230 for the future 0.8V/150A and 4.6A/ns output requirement. Such a huge number of capacitors are not acceptable from both cost and real estate perspectives.

It is proven that the higher the bandwidth of the VR, the smaller the inductance and capacitance. Based on the analysis in the previous chapter, the relationship between the output bulk capacitance and the bandwidth of the VR with today's power delivery path and microprocessor specifications can be plotted. It is very interesting that if the bandwidth is pushed beyond 350 kHz, the bulk capacitors can be completely eliminated, which means a big cost saving. Assuming that the bandwidth is 1/6 of the switching frequency, 2-MHz switching frequency is necessary. At 650kHz bandwidth, the amount of decoupling capacitors on the MB can be reduced from 230 to 50.

Basically, Chapter 2 illustrates the benefits of high frequency. First of all, the high frequency helps us to eliminate the bulk capacitors, which means a great cost reduction. Second, it saves a lot of real estate on the MB, which allows the placement of more silicon devices to handle the increasing current demand of the microprocessor.

Most of today's VR topologies for desktop computers are the multiphase buck [45][46][47]. As pointed out in the Chapter 2, due to its very low output voltage and relatively high input voltage, the buck converter has an extremely small duty cycle, which dramatically impacts the VR's performance. Both the transient response and the efficiency suffer a lot. As a result, today's solution is no longer suitable for high-frequency applications. An alternative should be found.

To deal with the problems caused by the small duty cycle, various autotransformer versions of buck converters have been proposed [48][49][50]. These improve the efficiency significantly, and could be more cost effective. However, the leakage inductor of the transformer fundamentally limits its switching frequency because of the duty cycle loss. Usually, these versions cannot push the switching frequency beyond 1.5 MHz.

Basically, two simple messages are delivered here: 1. Future microprocessor seriously challenges VR design. High bandwidth is the only solution, which usually require high switching frequency design; 2. Today's topology and power architecture are not effective for high frequency applications. We need find alternatives.

In this chapter, the two-stage approach [55][56] is proposed first based on some preliminary experimental results and loss analysis. By simply decreasing the input voltage and using low-voltage-rating devices, the multi phase buck could be very efficient for high-frequency

applications. Another simple and highly efficient step-down converter is used as the first stage. At first glance, the two-stage approach is more complicated as compared with the single-stage approach, however, the detailed analysis in this chapter shows that the two-stage concept is very promising for future VRs from the standpoints of both performance and cost. Several very simple methods are also proposed based on two-stage structure to make the 4MHz VR design feasible.

Other design considerations of the two-stage approach, such as the optimal intermediate bus voltage design, the intermediate bus capacitance design and etc., are also discussed in Section 3.2. Then, the two-stage approach is applied to desktop computer and laptop computer, respectively. The experimental results are provided to verify the analysis. It is proven that the two-stage approach is promising for future microprocessors.

3.2. Analysis of Two-stage Approach

It has been pointed out in Chapter 2 that the characteristics of future microprocessors for the desktop computer are a fast transient response and a high current with low voltage. Actually, they are also true for other microprocessors, such as a laptop computer and a server.

The first challenge, fast transient response, needs VR with high bandwidth design, which could supply high di/dt current through the output inductor. Otherwise, more capacitors have to be paralleled to store the sufficient energy for transient. However, high bandwidth is usually achieved by high frequency design, which in turn suffers the system efficiency.

The second one, high current with low voltage, places a big challenge on the VR design for good steady state performance. Obviously, high current causes high conduction loss and switching loss. In addition, the relatively high input voltage makes the duty cycle of the Buck type PWM converter very small and inductor ripple current larger, which generally results in lower efficiency. To reduce the conduction loss, the common way is to parallel more devices. Circuit design can hardly reduce it. Thus, we leave it out of our discussion. For the switching loss, the common solutions are to reduce the drain-source voltage, the turn-off current and/or the overlapping time if PWM converter is still followed. Obviously, lower input voltage is desirable. In other words, larger duty cycle is preferred.

As a summary, the challenges are coming from two aspects. One is from the load side, which is stringent transient, and the other is from the input side, which is relatively high input voltage. The conventional single-stage can satisfy the transient requirement with a small duty cycle design for today's microprocessor while keeping a reasonable efficiency. However, when high frequency VR becomes mandatory for the future microprocessor (otherwise more capacitors are needed), the conventional solution cannot deal with the challenges from both sides by a single stage structure.

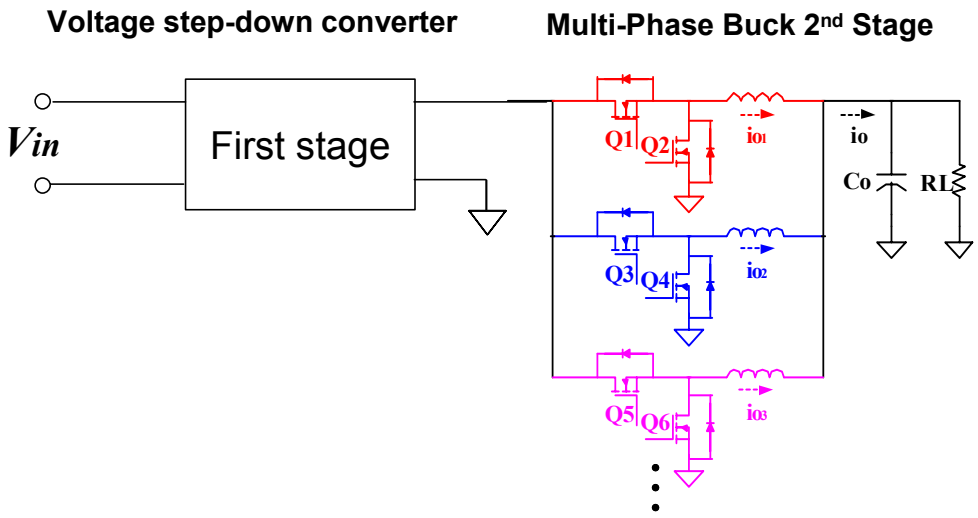


Figure 3-2. A typical two-stage structure for powering microprocessors.

In order to satisfy the specifications of future microprocessors, a two-stage structure is proposed as illustrated in Figure 3-2. Basically, there are three parts: the first stage, the second stage and the intermediate bus. The missions for these parts are very different. The core of two-stage structure is the high frequency, high efficiency second stage, which is still composed of multi-phase buck converters and used to handle the transient response. The task of the first stage is to step down the input voltage to a certain intermediate bus voltage efficiently and simply. The high frequency is optional for the first stage. It is obvious that each stage deals with only one challenge. For example, the first stage only handles the challenge from the input side, and the second stage only deals with the challenge from the output side.

At the first glance, the two-stage doesn't seem better than the single stage structure. However, in the following sections, the detailed analysis and experimental results will be provided to prove that two-stage approach is promising for the future microprocessor.

Basically, there are three challenges for two-stage VR design:

1. High frequency, and high bandwidth second stage design with high efficiency;
2. Simple and high efficiency first stage design;
3. Optimal intermediate bus voltage design.

The most straightforward two-stage design usually employs multi-phase buck converter for both the first stage and the second stage. It might not be optimally designed. The following section will address these challenges.

3.2.1. The Ultra-High-Frequency, Low-Input-Voltage Second Stage

The core of the two-stage approach is to realize ultra-high frequency and high bandwidth for the second stage, which is handling the stringent transient load. The device plays a very important role in achieving this goal. Therefore, the state-of-the-art device and the future device development are investigated, respectively.

3.2.1.1. The State-of-the-Art Discrete Device for 1~2 MHz VR

It is well known that the input voltage of today's VR in desktop application is 12 V. Therefore, the 30 V rating trench MOSFET is widely used. And its efficiency reaches around 85% at full load at 500kHz frequency. What about its high-frequency performance? To answer this question, a simple experiment is set up using the following: two-phase buck with Vin=12 V; the top switch is HAT2168; the bottom switch is HAT2165; and the driver is LM2726. To keep the inductor current ripple constant, the output inductance for each phase varies as the switching frequency changes: 400 nH @ 500 kHz, 200 nH @ 1 MHz, 140 nH @ 1.5 MHz and 100 nH @ 2 MHz. The output specification is 1.2 V/25 A. The bottom curve in Figure 3-3 is the efficiency at different switching frequencies and 12V input voltage. This curve indicates that its high-frequency performance is poor.

The next step is to simply change the input from 12 V to 5 V while keeping everything else the same. The efficiency (the second curve from bottom) is also shown in Figure 3-3. There is an efficiency improvement of around 5% at 2 MHz.

Furthermore, since the input voltage (5 V) is much lower than 12 V, low-voltage rating device can be used safely. Limited by the commercially available low-voltage-rating devices, only the bottom switch is changed from a 30 V MOS (HAT2165) to a 20 V MOS (Si4864) to reduce the conduction loss. Si4864 has smaller $R_{ds(on)}$ (2.4mΩ) than HAT2165 (3.4mΩ). Normally, a lower-voltage rating device can give a better performance. The experimental efficiency is shown as the top curve in Figure 3-3. There is an additional efficiency improvement of 2% at 2 MHz and it reaches 78% efficiency at 3 MHz.

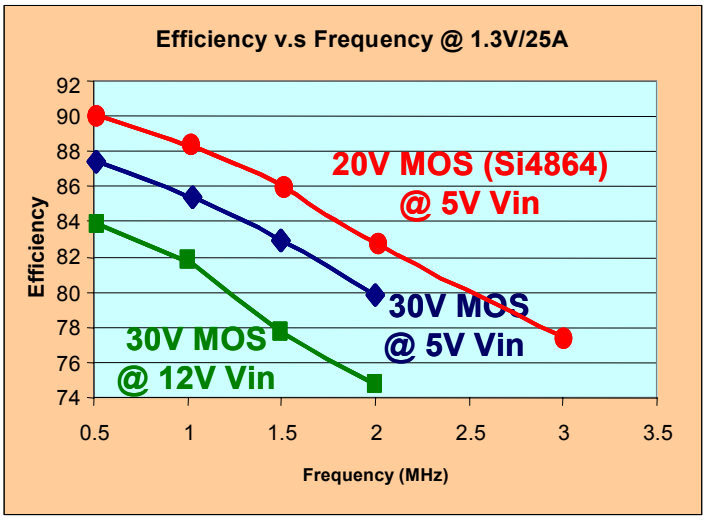


Figure 3-3. Efficiency improvements by lowering down V_{in} and using low voltage rating devices.

Quickly developing device techniques offer great opportunities to improve the multiphase buck performance. Based on these tests, it is apparent that the state-of-the-art discrete devices have already been available for us to develop 1~2MHz VR based on two-stage approach.

3.2.1.2. Technologies for 4 MHz VR Development

A. Proposed Method to Reduce the Switching Loss

In the previous section, it is proven that the two-stage approach with today's discrete devices is better than the single stage VR at high frequency application. The second stage can reach 2MHz switching frequency while maintaining around 84% efficiency. As mentioned in chapter 2, in order to reduce the decoupling capacitors in the cavity of the socket, the switching frequency needs to be further pushed up to 4 MHz.

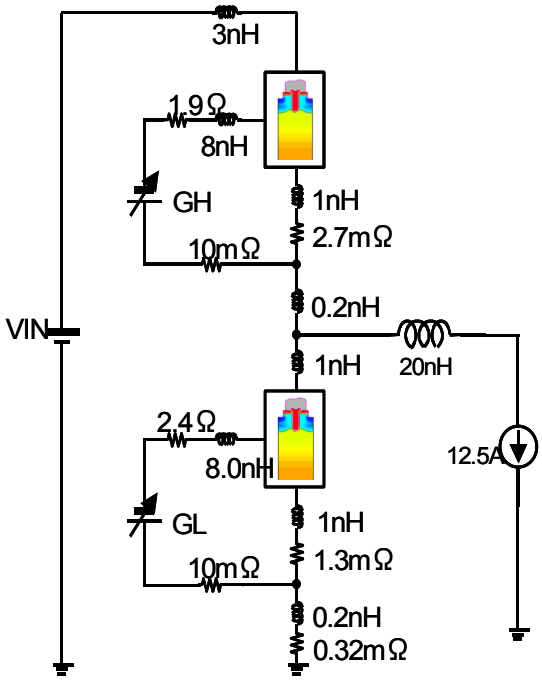


Figure 3-4. The simulation setup for discrete devices: Top switch HAT2168, bottom switch HAT2165.

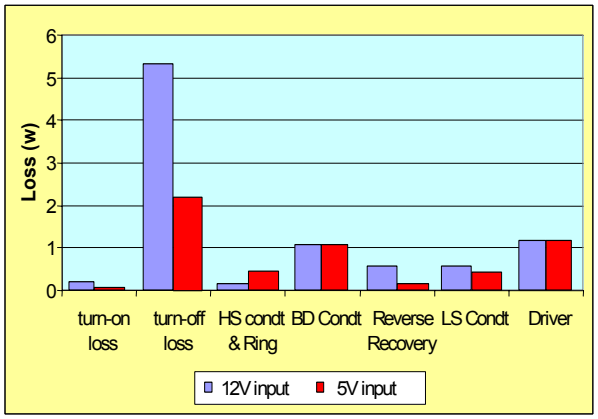


Figure 3-5. Loss breakdown of a 4MHz VR operating at 5V input and 12V input respectively.

To achieve high efficiency of the second stage at such a high frequency, the loss breakdown is analyzed first before doing any hardware test. Based on physics-based simulation tools, such as Medici and ISE, an accurate loss breakdown of VR can be obtained. The simulation setup (shown as Figure 3-4) is as follows: V_o=0.8V, I_o=12.5A, f_s=4MHz, top switch is HAT2168, bottom switch is HAT2165 and the output inductance is 20nH. It is clear that lowering down the input voltage dramatically reduces the switching loss and body diode reverse recovery loss (shown in Figure 3-5). Although the conduction loss increases somewhat, the gain is still significant.

However, the switching loss is still dominant. References [59][60] and the appendix of this dissertation analyze the switching loss and give the expressions based on the equivalent circuits of device behaviors. The analysis results reveal that the parasitic common source inductor, which is shared by the power stage and driver loop, is critical to the switching loss.

The recent integration of the driver and MOSFET (DrMOS) [51] gives a great opportunity to minimize the parasitic components and improve the switching performance. It is an integrated device including top switch, bottom switch and driver. The parasitic inductance can be

dramatically reduced, which results in much smaller switching loss. Furthermore, since the parasitic components are reduced, the voltage spikes across the devices are much smaller. Therefore, low-voltage-rating devices can be used in the DrMOS. As mentioned before, the voltage rating can be even smaller for the two-stage application since the input voltage of the second stage is as low as 5 V. As the voltage rating decreases, the FOM can be reduced, which means the performance is better.

Figure 3-6 shows the simulation setup for DrMOS structure. Everything is the same except that the device package changing from discrete component to integration structure. Compared to the discrete device, the common source inductance is reduced from 1nH to 0.1nH. The driver loop inductance is also reduced from 8nH to 1nH. Both of them contribute to the switching loss reduction. On the other hand, the whole loop inductance of power stage is reduced from 6.4nH to 2.3nH, which is also helpful in reducing the switching loss.

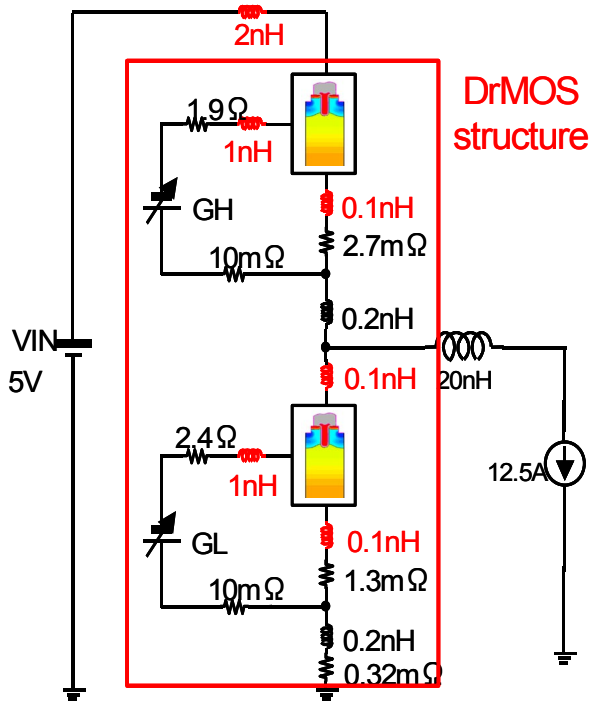


Figure 3-6. Simulation setup with DrMOS structure at 5V input.

Figure 3-7 shows the loss comparison between the discrete components and DrMOS at the same setup. The turn-off loss can be reduced by around 25%. However, the reduction is not significant.

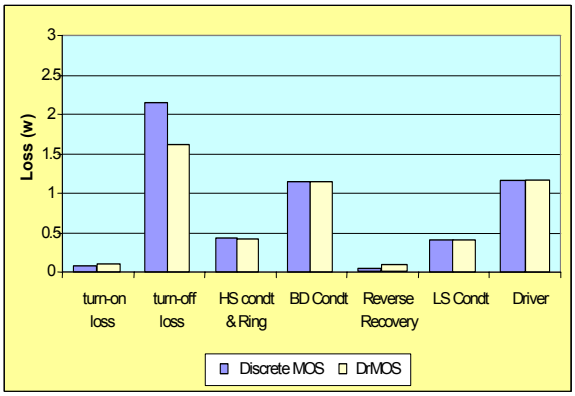


Figure 3-7. Loss comparison between the discrete device and DrMOS at 5V input.

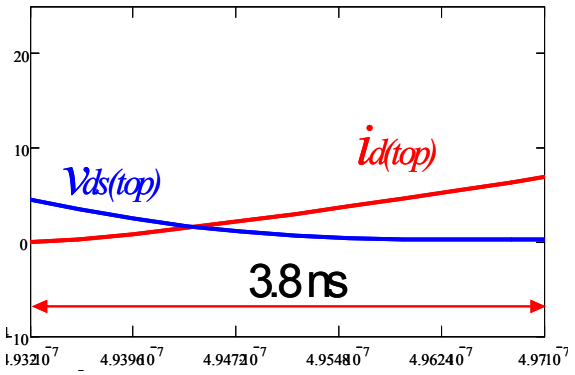


Figure 3-8. The waveforms of top switch during turn-on at 5V input indicate nearly ZVS operation.

Further improvement is stimulated by an observation. The waveforms of the top switch during the turn-on period are shown in Figure 3-8. It looks like zero-voltage-switching (ZVS) turn-on, which means a snubber capacitor can be paralleled with the top switch to reduce the turn-off loss. In the simulation circuit, a 4nF capacitor with 100pH ESL and 3mΩ ESR is paralleled with the top switch as shown in Figure 3-9. The capacitor parameters are based on Maxwell simulation for a 1206 form factor ceramic capacitor integrated with top switch.

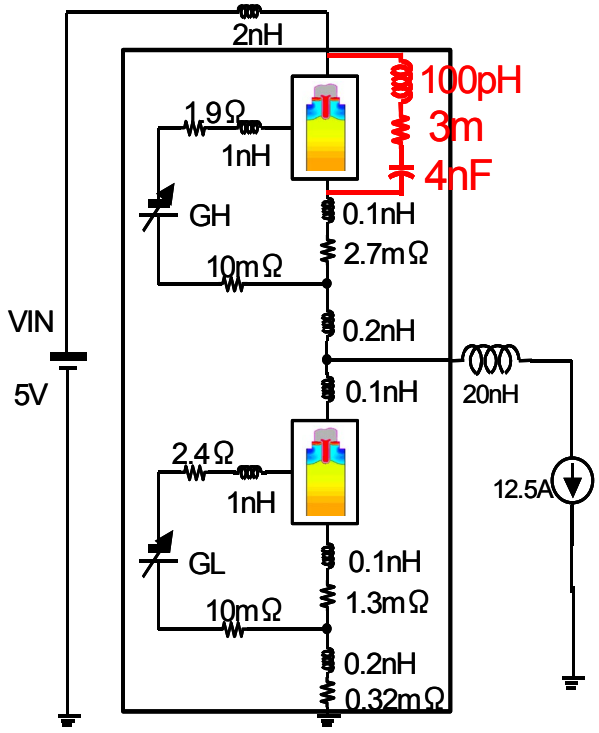
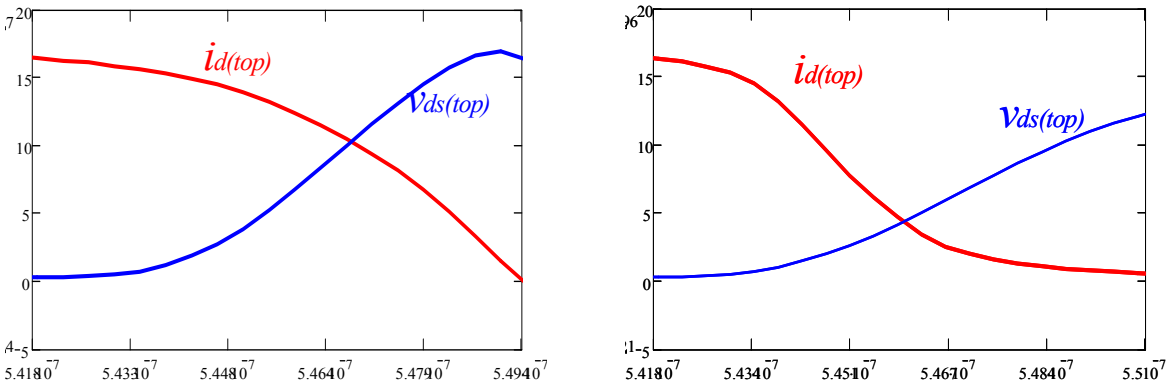


Figure 3-9. Simulation setup with DrMOS structure at 5V input with integrated snubber capacitor.

The top switch turn-off waveforms are shown in Figure 3-10. Compared with the no snubber capacitor case, the drain-source voltage rising speed is greatly reduced and therefore the overlapping area is much smaller. The loss comparison is shown in Figure 3-11. It is clear that the turn-off loss is significantly reduced, although the turn-on loss increases. The total switching loss reduction is still significant (around 70%).

Recently, CPES is implementing this idea in the VR embedded module, which can easily integrate the snubber capacitor with the devices.



(a) (b)

Figure 3-10. The waveforms of top switch during turn-off period: (a) without snubber capacitor and (b) with snubber capacitor.

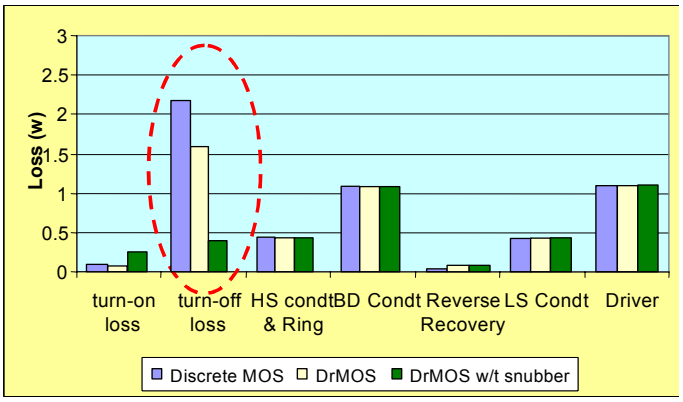


Figure 3-11. Loss comparison shows a significant turn-off loss reduction by paralleling snubber capacitor across the top switch.

As we know, the snubber capacitor results in smaller turn-off loss and larger turn-on loss. There must be an optimal value. Based on the Medici simulation tool, the optimal snubber capacitance and the impact of ESL are illustrated. The relationship between the switching loss

and capacitance is shown in Figure 3-12. The optimal capacitance range is 3nF~5nF. The relationship between the switching loss and the ESL is given in Figure 3-13. It is clear that the impact of ESL is very significant. In order to achieve better result, the ESL should be minimized. Therefore, integrating snubber capacitor with the device is desired.

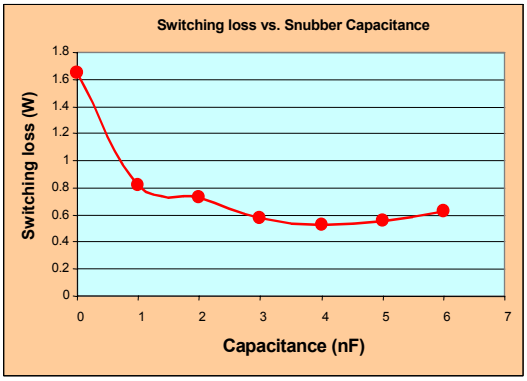


Figure 3-12. The relationship between the switching loss and the snubber capacitance shows an optimal capacitance range.

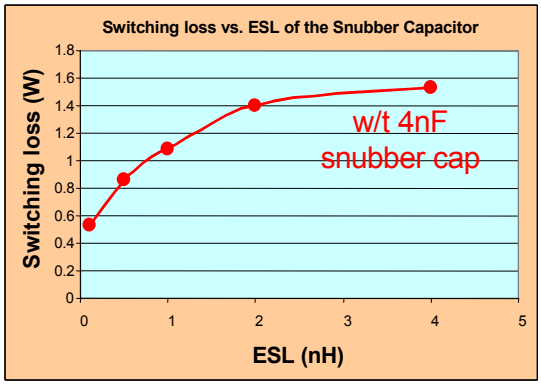


Figure 3-13. The relationship between the switching loss and the ESL of snubber capacitor.

To verify this idea, a two-phase Buck converter is built. The set-up is as follows: V_{in}=5-V, V_o=1.2-V, I_o=25-A, L=50-nH for each phase, fs=2-MHz; for each phase, one HAT2168 are used as the top switch and one Si4864 are used as the bottom switch, the driver is LM2726 from National Semiconductor. The PCB is 4-layer 2-oz copper. The experimental efficiency (labeled as "w/o snubber") in Figure 3-14 shows the efficiency with drive loss. At full load, it still can achieve 83% efficiency.

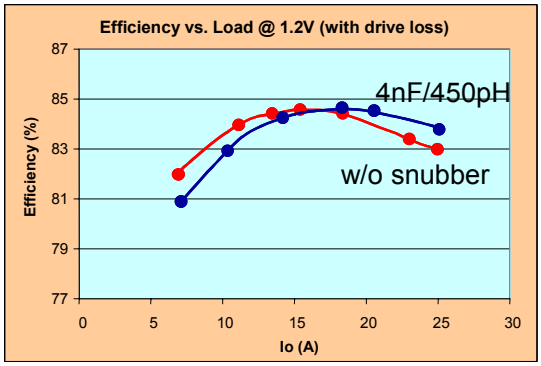


Figure 3-14. The second stage experimental efficiency comparison between with snubber capacitor and without snubber capacitor at 2MHz.

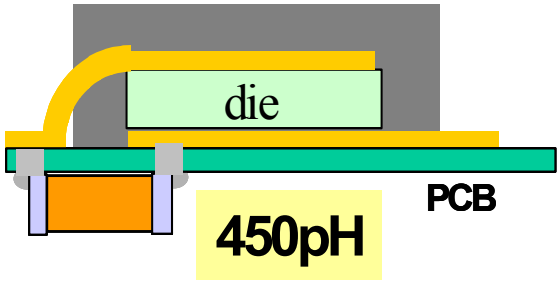


Figure 3-15. The ESL simulation of the snubber capacitor by Maxwell Q3D.

To verify the method of saving the switching loss by the snubber capacitor, the snubber capacitors are mounted on the backside of the PCB. The snubber capacitance is 4nF for each phase. Maxwell Q3D is used to estimate the ESL and ESR value. The simulated structure is illustrated in Figure 3-15. The ESL is 450pH and ESR is 5mΩ. Figure 3-14 shows the measured efficiency curves. It can be seen that the efficiency at full load is improved by around 1%. At light load, the efficiency is lower than the benchmark because the additional turn-on loss is larger than the turn-off loss saving. If the snubber capacitor is integrated with the device, the ESL can be reduced down to 100pH and the efficiency improvement is over 2% at 2-MHz. It is expected that the improvement is more significant at higher frequency, such as 4-MHz.

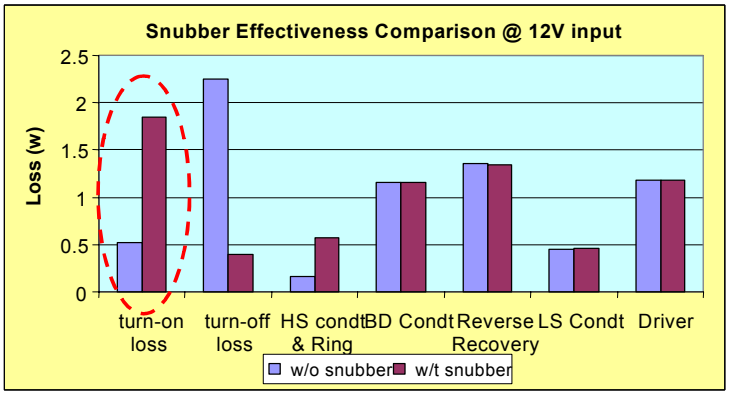


Figure 3-16. The loss comparison between w/t snubber capacitor and w/o snubber capacitor at 12V input.

However, this method is not effective for 12V input VR because the increased turn-on loss counteracts the turn-off loss reduction. Figure 3-16 shows the loss breakdown comparison between with snubber capacitor and without snubber capacitor at 12V input case. The simulation conditions are: V_{in}=12V, V_o=0.8V, I_o=12.5A, f_s=4MHz, L=20nH, HAT2168 and HAT2165 with DrMOS configuration. It is apparent that the turn on loss significantly increases although the turn off loss decreases in the case of with snubber capacitor. The gain is counteracted by the payment. Therefore, this method cannot be applied to 12V input VR. In other words, it is unique for two-stage approach.

B. Proposed Gate Driver to Reduce the Body Diode Conduction Loss and Gate Drive Loss ([61][62][63])

After solving the switching loss, the loss breakdown is redrawn in Figure 3-17. The simulation conditions are: V_{in}=5V, V_o=0.8V, I_o=12.5A, f_s=4MHz, L=20nH, 4nF snubber

capacitor parallels with top switch, and DrMOS structure with HAT2168 and HAT2165 integrated. Now, the body diode conduction loss and gate drive loss are the major barriers for the high frequency VR.

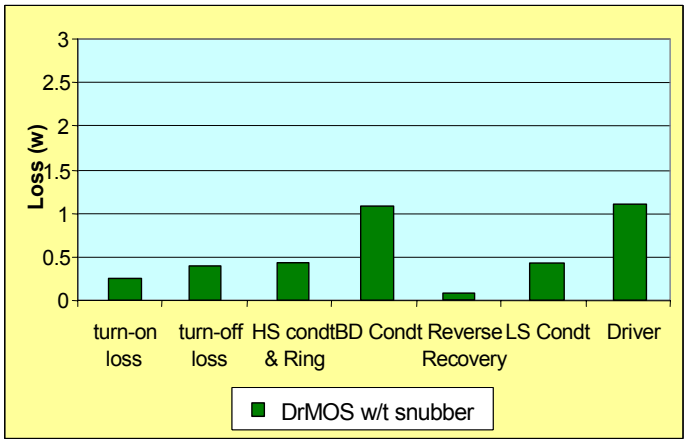


Figure 3-17. The loss breakdown at the condition of 5-V input, DrMOS structure and snubber capacitor shows the body diode conduction loss and drive loss are significant.

The reason for the body diode conduction loss is dead time. In order to avoid the shoot-through, dead time has to be inserted between the gate driver signals (as shown in Figure 3-18). The desired gate driver signals are shown in Figure 3-19. As long as the crossover level of the gate driver signals is equal to or less than the threshold voltage of the devices, the dead time can be eliminated and the shoot-through can also be avoided.

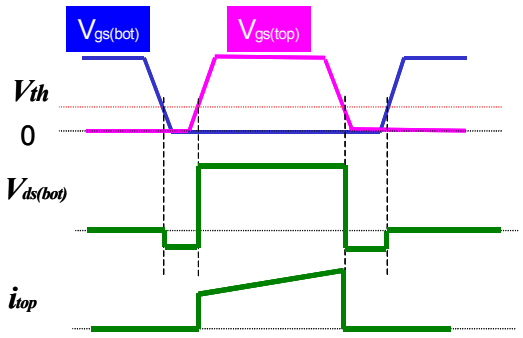


Figure 3-18. The body diode conduction caused by the conventional gate signals.

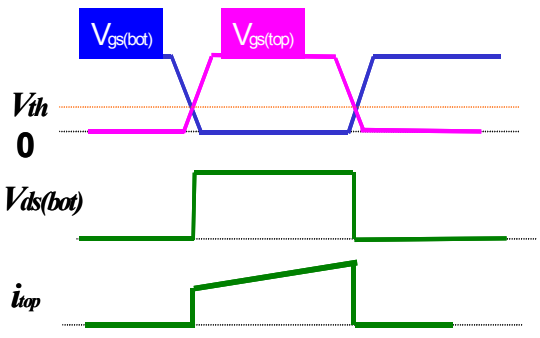


Figure 3-19. The desired gate signals.

In order to realize the desired waveforms, a transformer should be used to couple the gate capacitors of top switch and bottom switch together. The conceptual schematic and its equivalent

circuit are shown in Figure 3-20. It is easy to understand that except the polarity the gate-voltage slew-rates during the commutation time are exactly same.

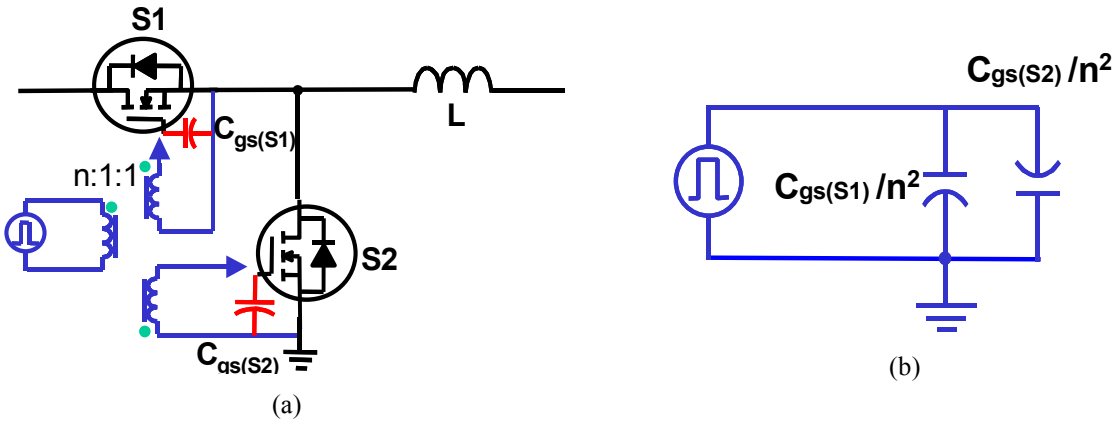


Figure 3-20. The transformer couples the gate capacitors of the top switch and bottom switch coupled together: (a) Conceptual drawing and (b) the equivalent circuit at the primary side.

Because the crossover level of the gate signals is always at half of V_{cc}, which is normally larger than the threshold voltage, the shoot through problem can be incurred (as shown in Figure 3-21). A level shifter circuit should be inserted into the driver loop of either the top switch or the bottom switch. Figure 3-22 shows the complete conceptual drawing of the proposed driver.

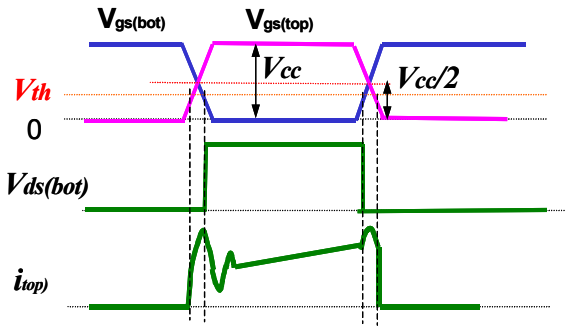


Figure 3-21. The shoot-through problem based on the driver scheme of Figure 3-20.

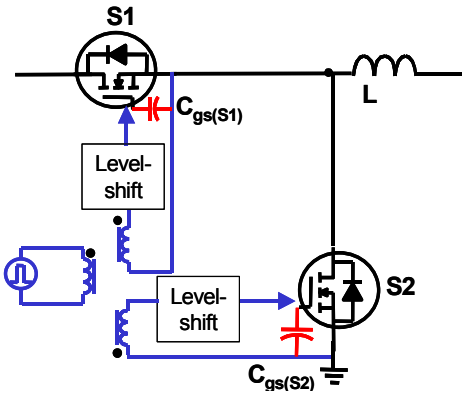


Figure 3-22. Level-shift circuit inserted into the driver loop to avoid the shoot-through problem.

Based on the level-shift circuit, the crossover point can be adjusted to avoid the shoot-through problem. Theoretically, the level shift could be a voltage source. However, it is a little bit complicated. Another simple implementation is composed of a Zener diode, a capacitor and a resistor as shown in Figure 3-23. The waveforms in Figure 3-24 illustrate that the drive signal for

the bottom switch is shifted. As long as V_z is greater than $V_{cc}/2-V_{th}$, the shoot-through can be avoided.

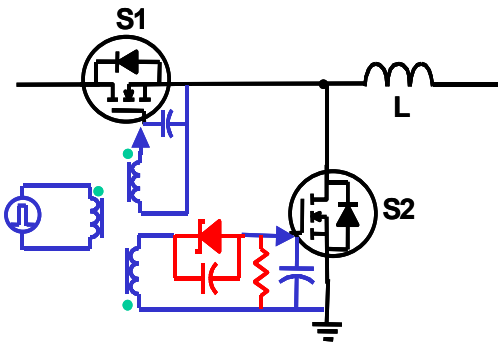


Figure 3-23. A simple implementation of the level-shift circuit.

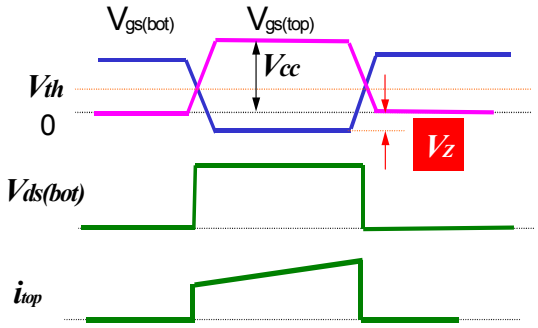


Figure 3-24. The shoot-through problem is avoided by the level-shift circuit.

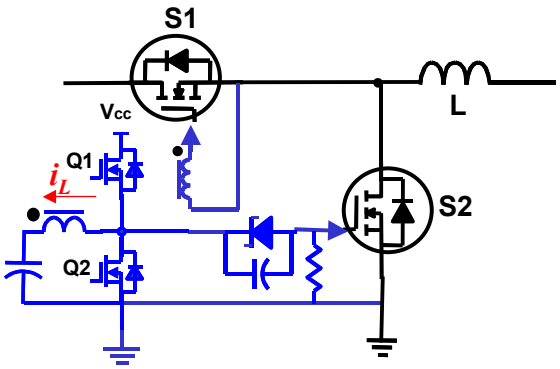


Figure 3-25. One of the implementations of the proposed concept.

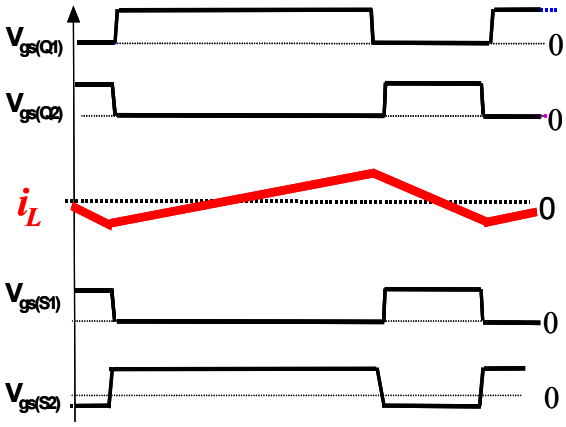


Figure 3-26. The gate signals based on the proposed driver's implementation in Figure 3-25.

Actually, for the Buck converter, it is not necessary to use two secondary windings. Figure 3-25 shows one of the implementations of the concept in the Buck converter. Q_1 and Q_2 could be either the discrete components or the output stage of the conventional driver chip. The gate signals and inductor current i_L are drawn in Figure 3-26. Different from the resonant drivers, the proposed driver is very easy to control. The signals can be gotten directly from the commercial VR controller and no additional timing or logical circuits are needed. Based on this driver scheme, simulation results indicate that around 80%~90% body diode conduction loss can be saved. The experimental results are provided in the following section.

After the body diode conduction loss is dramatically reduced or even eliminated, the drive loss turns to the most significant part. Can we save the drive loss based on the same driver scheme? The answer is yes.

As mentioned before, the gate capacitors have been coupled together at the primary side. Further investigation found that those capacitors also serve as the snubber capacitors for the bridge composed of Q_1 and Q_2. As long as ZVS of Q_1 and Q_2 can be achieved, the energy stored in the snubber capacitors can be recovered, which means the drive loss can also be saved.

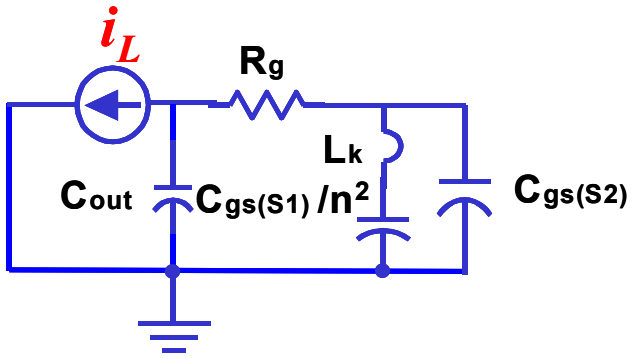
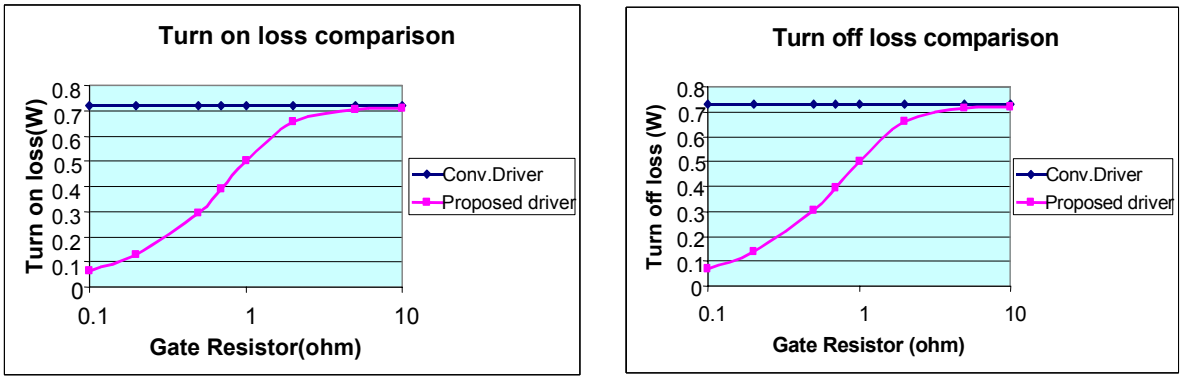


Figure 3-27. The equivalent circuit of the driver in Figure 3-25 during the commutation period.

In contrast to the external driver, which is a voltage-source driver, the proposed driver structure operates like a current-source driver. Figure 3-27 shows the equivalent circuit of the driver during the commutation period. The C_{out} is the output capacitor of Q_1 and Q_2. The $C_{gs(S1)}$ and $C_{gs(S2)}$ are the gate capacitor of S_1 and S_2, respectively. n is the turns ratio of the driver transformer. During the commutation period, inductor current i_L is used to charge/discharge the gate capacitors and the output capacitors of the gate driver.

It is well known that in a voltage-source driver, the driver loss is independent from the gate resistance. However, in this proposed driver, as R_g decreases, the loss reduction increases. The purpose of the gate resistor R_g is only to dampen the oscillation between the leakage inductor of the transformer and the gate capacitor C_{gs}. In an ideal case, if the leakage inductance L_k is zero, the gate resistor is not needed, and the driver loss can be entirely saved. Figure 3-28 shows the driver loss comparison between the conventional voltage-source driver and the proposed one at the condition of 4MHz, L_k=4nH, V_{cc}=5V and 1 HAT2165 parallel. For a practical design with R_g=0.5 Ohm, the drive loss savings could be around 60%.



(a) (b)

Figure 3-28. The drive loss comparison between the conventional voltage-source driver and the proposed driver: (a) drive loss during device turn-on and (b) drive loss during device turn-off.

In order to realize ZVS, it is very straightforward to decrease the magnetizing inductance of the transformer and use the magnetizing current. The theoretical waveforms are also shown in Figure 3-26. The simulation results indicate that around 50%~60% drive loss can be saved. The experimental results are also provided to verify the analysis.

The proposed driver can achieve two goals: body diode conduction loss saving and gate drive loss saving. Most importantly, it is very easy to be realized. No additional logical and timing circuits are needed.

As a summary, the loss breakdown comparison is shown in Figure 3-29. The simulation conditions are: V_{in}=5V, V_o=0.8V, I_o=12.5A, f_s=4MHz, L=20nH, DrMOS configuration, 4nF snubber capacitor parallels with top switch and the proposed driver is used. It can be seen that the proposed driver significantly reduces the body diode conduction loss and driver loss.

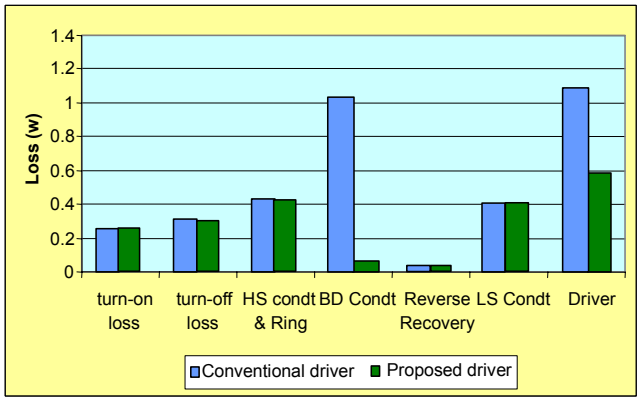


Figure 3-29. The VR loss breakdown comparison between the conventional driver and the proposed driver.

The experiment is carried out to verify the performance of the proposed driver. The set-up is as follows: V_{in}=5-V, V_o=1.2-V, I_o=25-A, L=50-nH for each phase, f_s=2-MHz; for each phase, one HAT2168 is used as the top switch and one Si4864 is used as the bottom switch. LM2726 from National Semiconductor is used as the benchmark. Q_1 and Q_2 of the proposed driver are Si3900DV from Siliconix. The PCB is 4-layer 2-oz copper. The snubber capacitors are paralleled with the top switch to reduce the switching loss. In order to show the improvement step by step, two versions of the proposed driver are built. One is called transformer version, which has larger magnetizing inductance and only body diode conduction loss is saved. Another one is called coupled-inductor version, which has smaller magnetizing inductance and gate drive loss is reduced as well as the body diode conduction loss.

Figure 3-30 shows the gate signal and drain-source voltage of the bottom switch with the transformer version driver design. It can be seen that the body diode conduction time is almost zero. The efficiency improvement is around 4%, as shown in Figure 3-32.

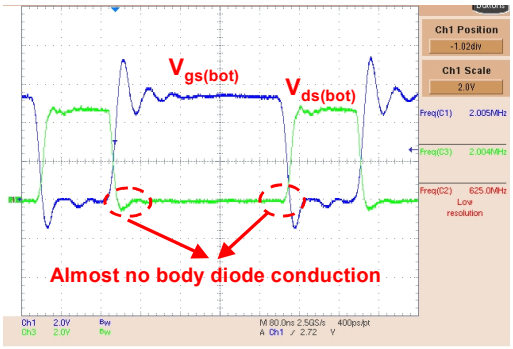


Figure 3-30. The gate signal and drain-source voltage of the bottom switch S_2 in power stage.

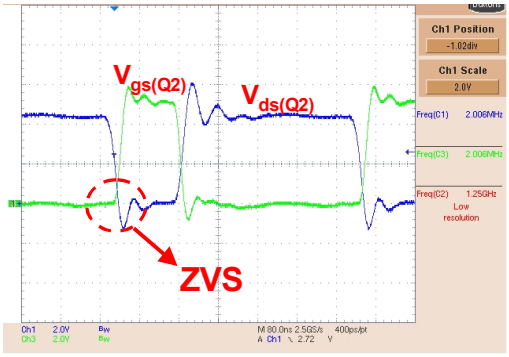


Figure 3-31. The gate signal and drain-source voltage of Q_2 in driver circuit.

The magnetizing inductance is reduced at the coupled-inductor version to realize ZVS of Q_1 and Q_2. Figure 3-31 shows the gate signal and drain-source voltage of Q_2. It is seen that ZVS is achieved. Consequently, the driver loss can be reduced as discussed in the previous section.

In Figure 3-32, the efficiency curves show that the coupled-inductor version has additional 1.5% efficiency improvement. Compared with the benchmark, the proposed driver is able to improve the efficiency by around 5.5% at 2MHz switching frequency. And the efficiency reaches 89% at 2MHz and full load. The improvement would be more significant at higher switching frequency applications.

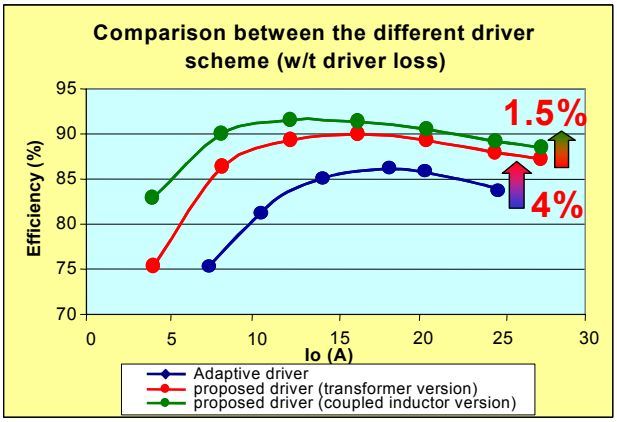


Figure 3-32. The second stage efficiency improvement by the proposed driver at 2MHz.

C. Future Devices

The loss breakdown in Figure 3-29 shows that the conduction loss is becoming significant after the body diode conduction loss and drive loss are reduced. In order to reduce it, better devices should be used. In other words, device FOM should be reduced.

Basically there are two ways to improve the device performance. First of all, more precise processing technology should be utilized. For example, Renesas Semiconductor developed D8 devices based on 0.35um process instead of the conventional 0.5um technology. The FOM of D8 devices can be reduced by 45% compared with D7 devices.

Another way is to develop low-voltage-rating devices as mentioned in the previous analysis. Figure 3-33 illustrates the FOM vs. voltage rating of trench device and lateral device, respectively. The top curve is the trench MOSFET based on 0.5um process and the middle curve is the trench MOSFET based on 0.35um process. The bottom one is the lateral MOSFET. It is obvious that no matter what kind of device, the common trend is that lower voltage rating, the smaller FOM.

Continuing the tests in 3.2.1.1, an experiment is carried out based on 20V trench MOS and DrMOS structure. The results are shown in Figure 3-34. Please note that the snubber capacitors and the proposed driver are not used in the test in order to highlight the device improvement. Compared with 30V trench MOS, the efficiency is improved over 5% at 2MHz frequency. Even at 3MHz, it can still achieve 82% efficiency.

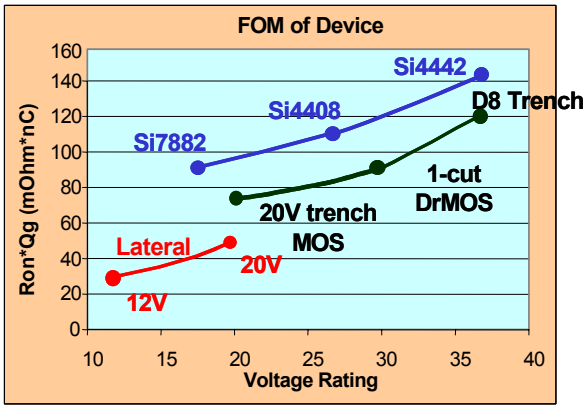


Figure 3-33. The FOM of devices vs. voltage rating.

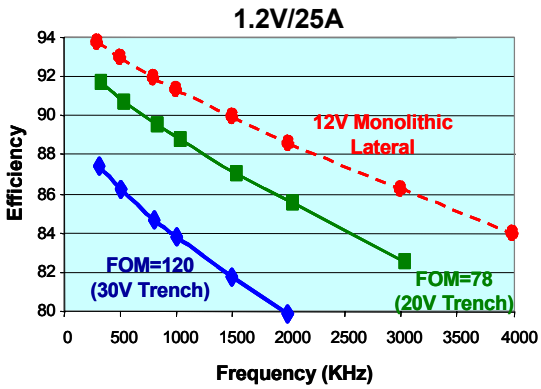


Figure 3-34. The efficiency vs. switching frequency based on different voltage-rating devices @ 1.2V/25A.

Another good candidate for high frequency application is lateral MOSFET. The most valuable characteristic of this lateral device is that it is easy to integrate with the driver and control circuits because the same process is used for all the parts. There is a lot of monolithic power ICs developed by industry for point-of-load (POL) application. The same structure can be applied to VRs application. CPES has designed a monolithic power IC [52] for 4MHz VR. Its voltage rating is 12V and the FOM is as small as 30. Its efficiency is projected in Figure 3-34 as the top dash line. 84% efficiency is expected at 4MHz.

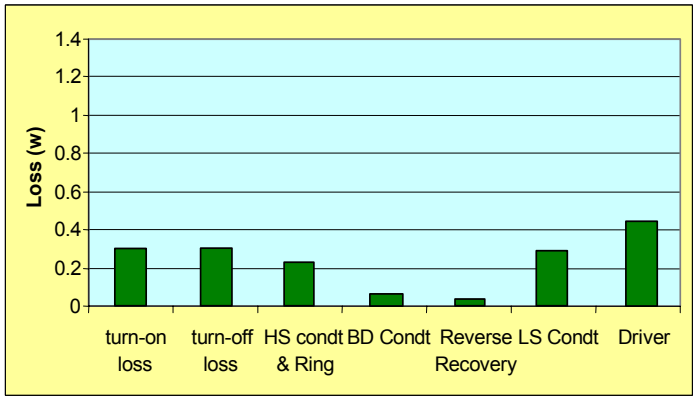


Figure 3-35. The loss breakdown of 12V lateral MOSFET at the condition of V_{in}=5V, V_o=0.8V, I_o=12.5A, f_s=4MHz, 4nF snubber capacitor paralleling with top switch and using the proposed driver.

As a summary, the loss breakdown based on 12V monolithic lateral MOSFET is shown in Figure 3-35. The simulation conditions are: V_{in}=5V, V_o=0.8V, I_o=12.5A, f_s=4MHz, L=20nH, DrMOS configuration, 4nF snubber capacitor parallels with top switch and using the proposed

driver. Compared with the loss breakdown of 30V trench MOS in Figure 3-29, the conduction loss and drive loss are reduced.

It is strongly believed that the two-stage approach is much more capable of being used in high frequency application compared with today's single stage because of the following advantages from the loss reduction perspective.

(1) By lowering down the input voltage, the switching loss can be significantly reduced.

(2) By paralleling snubber capacitors with the top switch, the switching loss can be further reduced.

(3) By the proposed driver scheme, the body diode loss and driver loss can be greatly reduced.

(4) By the fast developing device technology and low-voltage-rating devices (including both trench MOS and lateral MOS), the two-stage approach's performance can be further boosted.

3.2.2. The Simple and Highly Efficient First Stage

The requirement for the first stage is to achieve simplicity and high efficiency. Starting from this point, many candidates are available, such as the autotransformer version buck, the multi phase buck, etc. After careful comparison, a simple multi phase buck is chosen as the first stage. As the output voltage of the first stage increases from around 1V up to around 5 V, the duty cycle is enlarged. Therefore the current ripple of the output inductor could be smaller than that in single-stage case. Another important thing is that the switching frequency is not necessary higher because the stringent transient requirement is handled by the second stage. The theoretical estimation based on the loss model in the Appendix 1 shows that a two-phase buck with 12V input, 5V/25A output and 300kHz frequency could achieve around 97% efficiency.

A two-phase interleaving Buck converter (Figure 3-36) running at 300kHz is built as the first stage. The experimental efficiency is very good. Figure 3-37 shows the efficiency vs. the intermediate bus voltage at 120W output power. For example, it can achieve around 97% efficiency at 5V bus voltage and 120W full load output.

As the output power of future microprocessors increases, more current should be pushed from the first stage and the second stage, which means more devices are going to be paralleled to deal with the high current. However, the power density of the current first stage is very low due to its bulky passive components, especially the output inductors. As a result, high frequency is desired for the first stage design in order to increase the power density.

However, the performance of the first stage suffers a lot as the switching frequency increases. Figure 3-37 indicates that the efficiency of 1MHz PWM Buck converter degrades over 3% compared with 300 KHz one. The major reasons are illustrated in Figure 3-38. It is clear that the turn off loss and the body diode reverse recovery loss are the dominant parts.

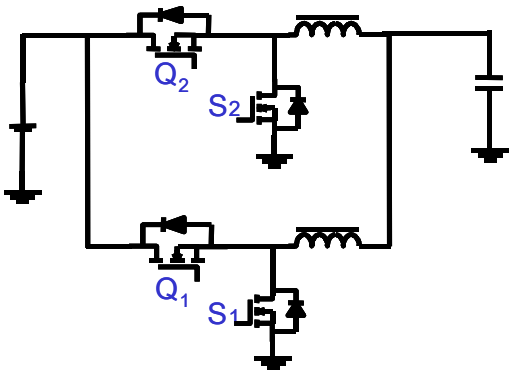


Figure 3-36. Two-phase interleaving Buck converter as the first stage.

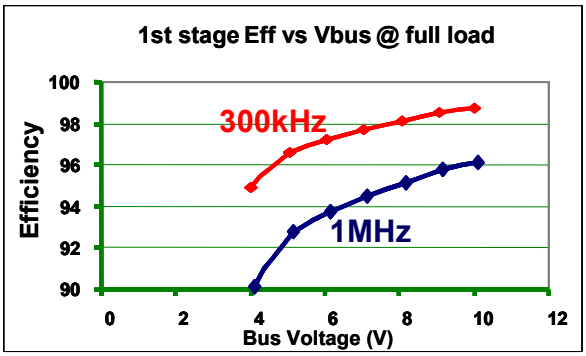


Figure 3-37. The efficiency of the PWM Buck vs. intermediate bus voltage. Top curve: 300 kHz and bottom curve: 1 MHz.

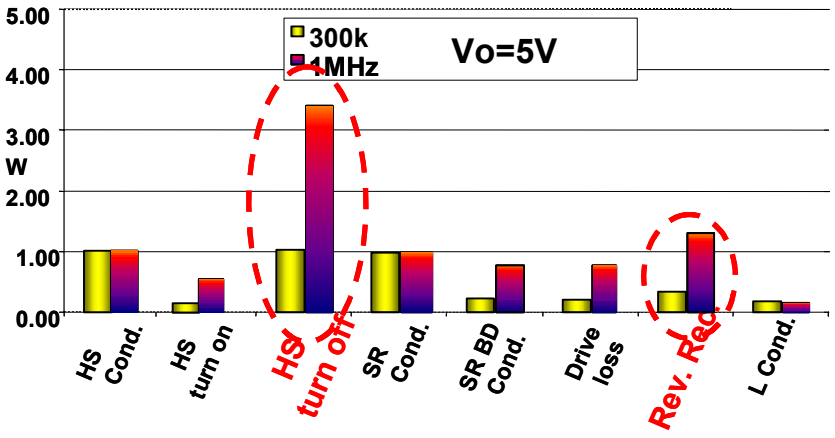


Figure 3-38. The loss breakdown of a two-phase interleaving Buck converter at the condition of 12 V input, 5 V output voltage and 120 W output power.

In order to reduce the aforementioned losses, a resonant Buck converter is proposed as shown in Figure 3-39, which can minimize the turn-off loss and body diode losses. The converter is operating at 50% duty cycle and open loop control. To simplify the circuit, self-driven scheme (shown in Figure 3-40) is also applied to the SRs. The voltage waveform at the corresponding phase node can be directly used as the driver signal. Compared with the conventional self-driven scheme, this self-driven scheme is much simpler.

The key operation waveforms are drawn in Figure 3-41. The detailed analysis is described in Appendix 2. ZVS and nearly ZCS conditions can be achieved. Meanwhile, the body diode conduction loss and the reverse recovery loss can be eliminated.

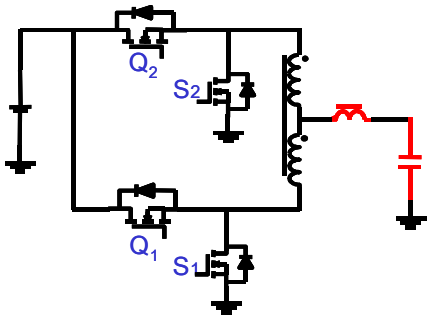


Figure 3-39. Proposed resonant Buck converter.

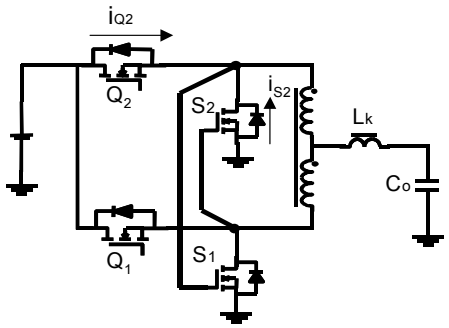


Figure 3-40. Proposed resonant Buck converter with self-driven scheme.

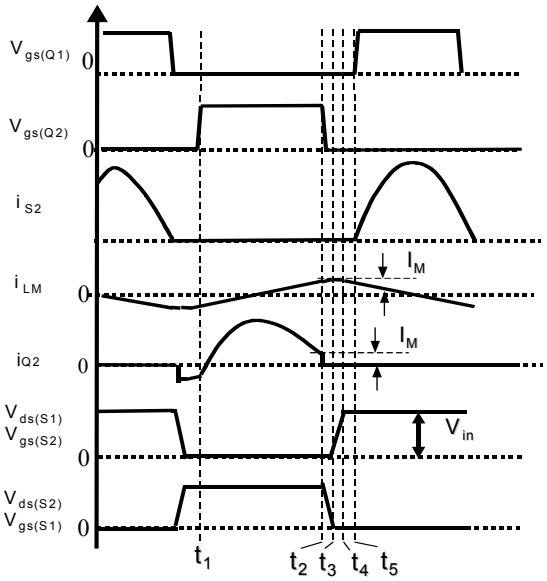


Figure 3-41. Key operation waveforms of the proposed resonant Buck converter.

Hardware is built to verify the analysis. The circuit is running at 1MHz. The specification is: V_{in}=12-V, V_o=6-V, P_o=120-W, f_s=1-MHz, L_k=1-nH, and C_o=8-uF. The devices are four HAT2165. The driver for the top switches is National LM2726. The core is TDK EIR18. Figure 3-42 shows the dimension comparison between the proposed resonant Buck and conventional PWM Buck. The footprint can be reduced by 33%, and the power density can be increased 2.5 times.

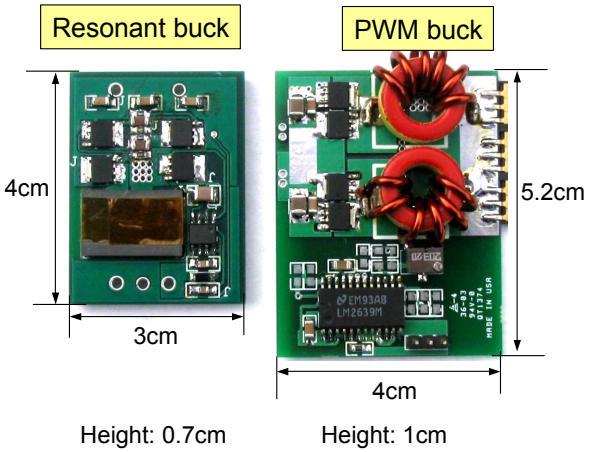
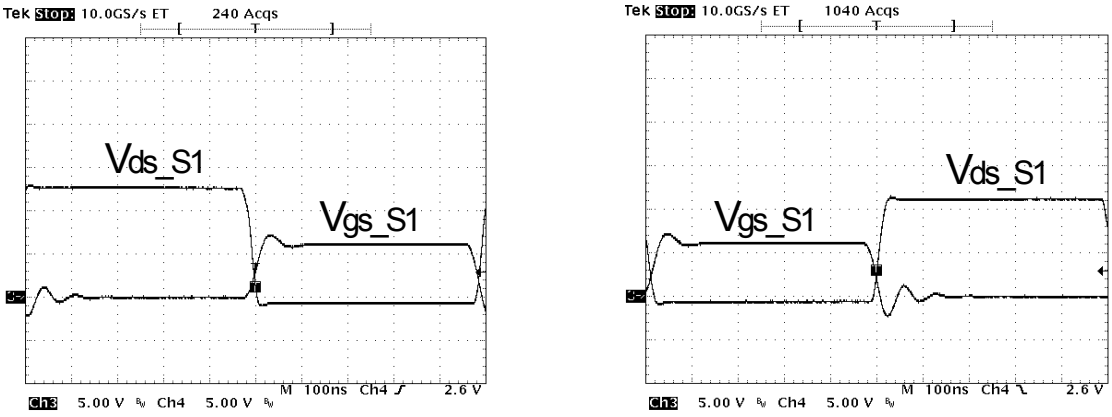


Figure 3-42. The dimension comparison between the proposed resonant Buck and conventional PWM Buck.

The waveforms in Figure 3-43 indicate no body diode conduction and ZVS condition. In Figure 3-44, the output inductor current waveform looks very nice. When the corresponding devices turn off, the current almost resonates back to zero. Therefore, the turn-off loss can be dramatically reduced.



(a) (b)

Figure 3-43. The drain-source waveform and gate signal of synchronous rectifier S_1.

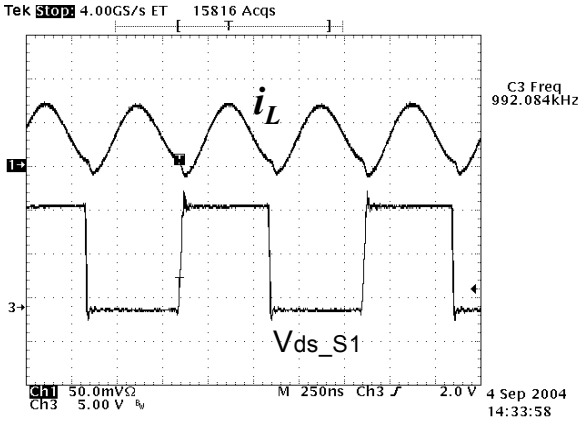


Figure 3-44. The output inductor current waveform and drain-source waveform of S_1.

As a summary, the efficiency of the proposed resonant Buck is compared with the conventional PWM Buck. At full load condition, the resonant Buck has 2% higher efficiency. At light load condition, the proposed one has lower efficiency because there is circulating energy in the magnetizing inductor. The self-driven scheme helps the light load efficiency somewhat because the drive loss can be partially recovered by the ZVS mechanism as analyzed in the proposed driver circuit for the second stage.

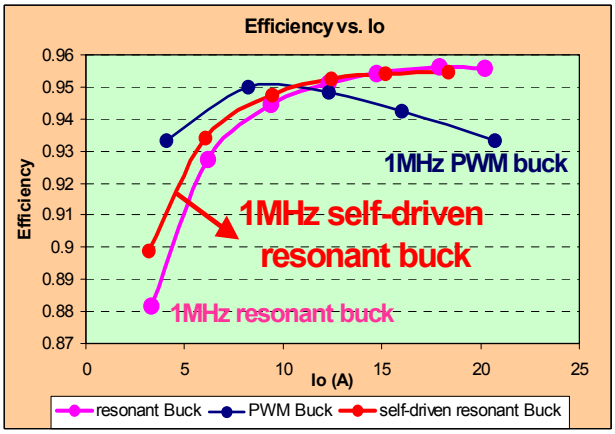


Figure 3-45. The efficiency comparison.

3.2.3. The Intermediate Bus Design

3.2.3.1. The Optimal Bus Voltage

It is known that when the bus voltage increases, the first-stage efficiency increases while the second-stage efficiency decreases. Therefore, an optimal bus voltage must exist from the

systems overall efficiency point of view. The criteria is very simple: at the optimal bus voltage, the whole system can achieve the highest efficiency.

Actually, the optimal bus voltage is related to many factors. In this chapter, the relationships between the optimal bus voltage and the switching frequency of the second stage, the device and the output specifications are investigated. Because the study needs to process a lot of data, the physics-based model and behavior model are no longer suitable due to their extremely low speed. An accurate device mathematic/analytical model is proposed in Appendix 1, which is used to investigate the bus voltage study.

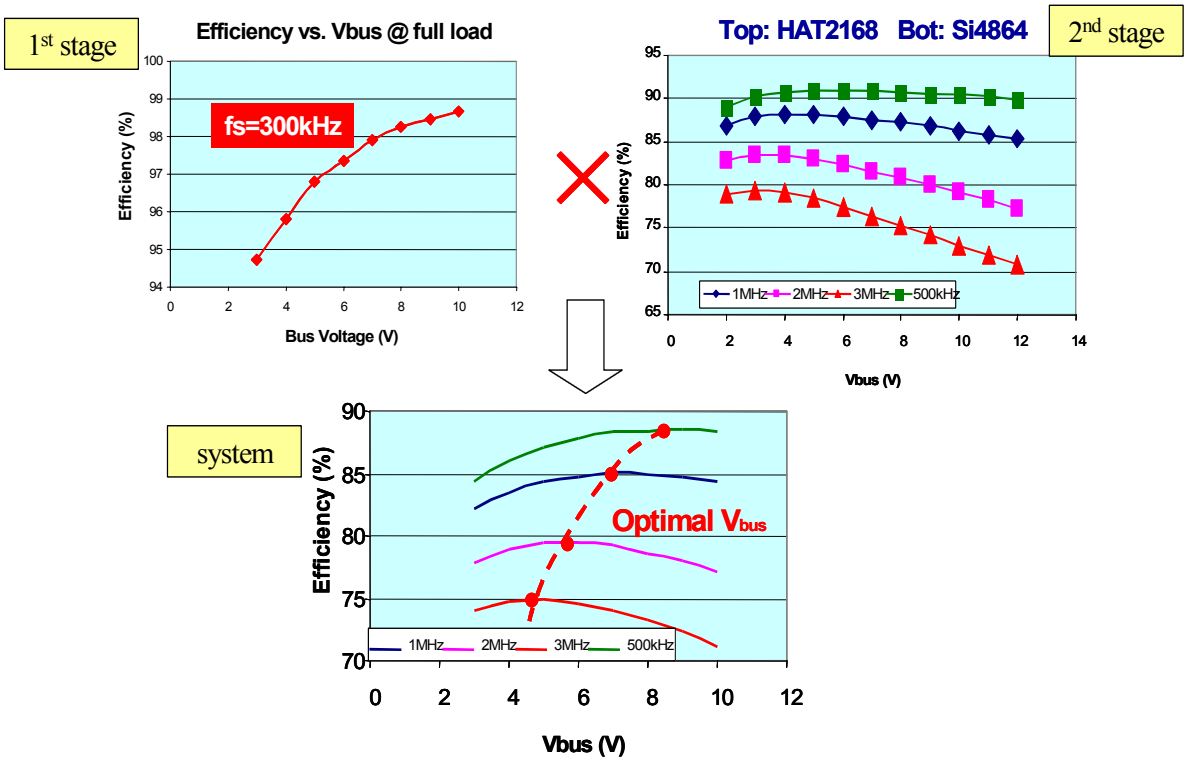


Figure 3-46. An example showing the process flow of determining the optimal bus voltage.

The methodology is as follows: at a specific switching frequency of the second stage and at a specific output specification, the efficiency vs. the intermediate bus voltage is plotted for the first and second stages, respectively. Then, these two sets of data are multiplied together and the system efficiency vs. the intermediate bus voltage is plotted. The optimal bus voltage at a specific condition can be easily determined. The process flow is repeated for different conditions, and these optimal bus voltages can be plotted. Figure 3-46 illustrates the process flow

by an example. Both the first stage and the second stage are using multi-phase buck converter. The first stage efficiency vs. bus voltage is shown as the top left figure. The second stage efficiency vs. bus voltage at the different switching frequency is plotted as the top right figure with HAT2168 and Si4864 device combination. Based on these data, the overall efficiency vs. bus voltage at different switching frequency can be achieved. Connecting the peak value of each curve, the dash line in the bottom diagram is redrawn in Figure 3-47 to illustrate the relationship between the optimal bus voltage and the switching frequency at the condition of HAT2168 and Si4864 combination.

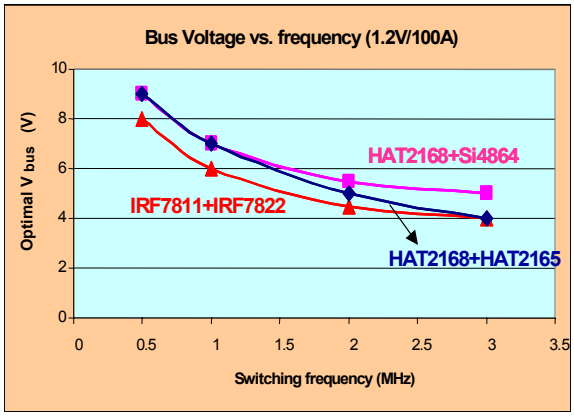


Figure 3-47. The optimal bus voltage vs. the frequency of the second stage with different device combination.

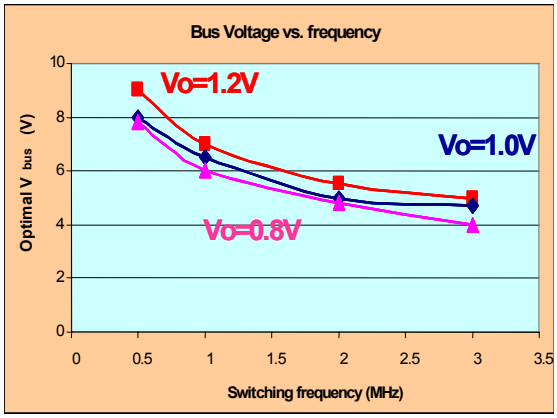


Figure 3-48. The optimal bus voltage vs. the frequency of the second stage at different output voltage.

For a different device combination, the optimal bus voltage could be very different. Figure 3-47 illustrates the relationship between the optimal bus voltage and the devices of the second stage. Normally, the better the devices (or smaller the FOM), the higher is the optimal bus voltage. As the switching frequency increases, the optimal bus voltage decreases. However, this trend becomes not so obvious when the frequency is above 2 MHz.

Figure 3-48 illustrates the relationship between the optimal bus voltage and the output voltage with the HAT2168 and Si4864 device combination. It is clear that the lower the output voltage, the lower the optimal bus voltage. However, this trend also disappears as the frequency is beyond 2 MHz.

After plotting these curves, it is found that for high-frequency applications (beyond 1-MHz switching frequency), 5-V could be the optimal intermediate bus voltage because it covers a

wide range of different devices and different output voltages. In addition, 5V has already been an industry standard and it can be easily picked up for VR application by industry.

3.2.3.2. The Intermediate Bus Capacitance

After choosing the two-stage approach for future VRs, the intermediate bus capacitance becomes a design concern. How large is it? To answer this question, the functions of the bus capacitors are listed as follows: to handle the ripple RMS current; to keep the system unconditionally stable and to meet the transient response requirement.

For the first requirement, Figure 3-49 shows the normalized RMS value of the ripple current vs. the duty cycle and the channel number. For an instance, a 5-V input, 1.2-V/100-A output four-phase buck, the input ripple RMS current is around 4 A. Normally 22uF ceramic capacitor can handle 2A RMS current. Therefore, two pieces of 22uF ceramic capacitors are adequate.

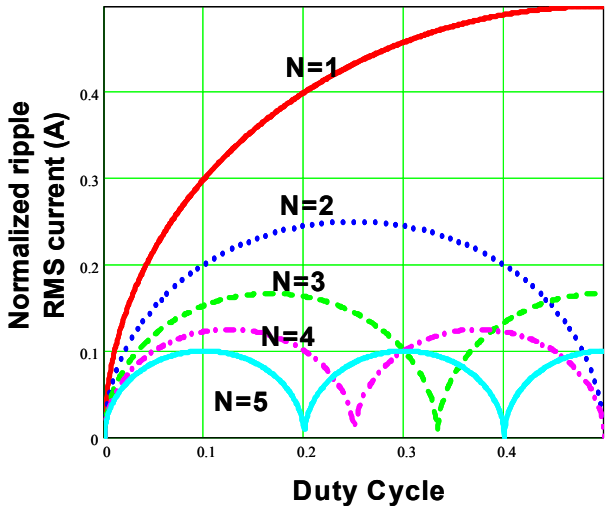


Figure 3-49. Normalized input ripple RMS current vs. duty cycle and channel number.

For the second requirement, the criteria of judging the stability of a cascaded system structure [70] are as follow: As long as there is no interaction between the output impedance of the first stage and the input impedance of the second stage, the system is stable. Figure 3-50 shows the output impedance of the first stage (two-phase buck converter) and the input impedance of the second stage at different conditions.

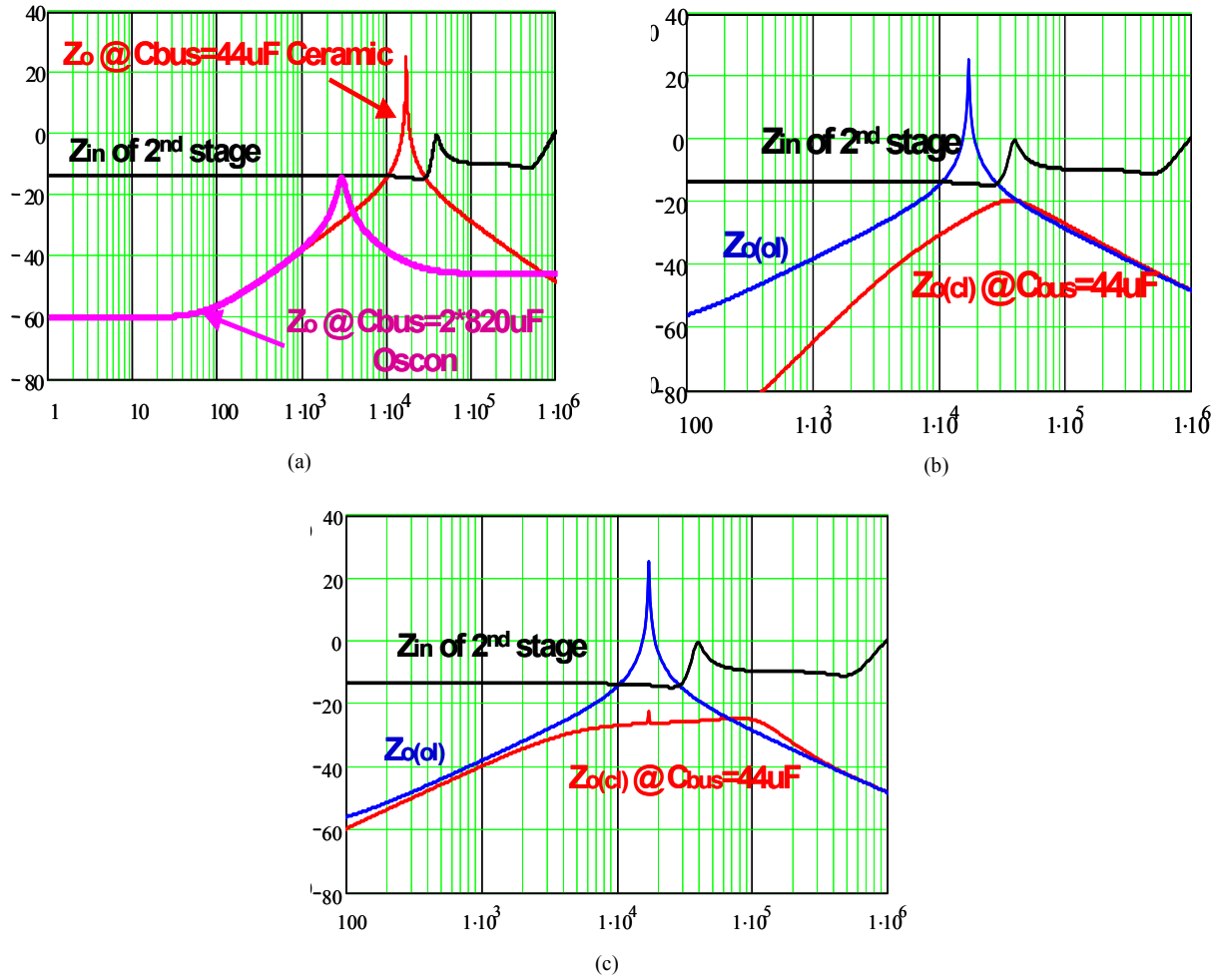


Figure 3-50. Input impedance of the second stage and output impedance of the first stage: (a) first-stage open loop; (b) first-stage under voltage-mode control with f_c=50kHz; and (c) first-stage under peak current-mode control with f_c=50kHz.

The close-loop input impedance of the second stage is expressed as follow:

$$Z_{in\_cl}(s) = \frac{\dfrac{1 + G_{v\_cl\_2nd}(s)}{G_{vg\_2nd}(s)}}{D \cdot \left(\dfrac{1}{R_c + \dfrac{1}{s \cdot C}} + \dfrac{1}{R} \right) - \dfrac{I_o \cdot G_{v\_cl\_2nd}(s)}{G_{vd\_2nd}(s)}} \qquad (3\text{-}1)$$

where: $G_{v\_cl\_2nd}(s)$ is the control to output voltage transfer function of the second stage in case of the current loop close and voltage loop open. $G_{vd\_2nd}(s)$ is the control to output voltage transfer function at open loop. $G_{vg\_2nd}(s)$ is the input voltage to output voltage transfer function. D is the

duty cycle. R_c is the equivalent series resistor (ESR) of the output capacitors. C is the output capacitance. I_o is the full load output current and R is the load.

The open-loop output impedance of the first stage is expressed in (3-2).

$$Z_o(s) = \frac{R_L\left[1 + \frac{s}{\omega_1 Q_1} + \left(\frac{s}{\omega_1}\right)^2\right]}{1 + \frac{s}{\omega_o Q} + \left(\frac{s}{\omega_o}\right)^2} \qquad (3\text{-}2)$$

where $\omega_o = \frac{1}{\sqrt{L \cdot C_o}}$ $\quad Q = \frac{1}{\omega_o C_o (R_c + R_L)}$

$\omega_1 = \frac{1}{\sqrt{L \cdot C_o}}\sqrt{\frac{R_L}{R_c}}$ $\quad Q_1 = \frac{1}{\omega_1\left(\frac{L}{R_L} + R_c C_o\right)}$

And L, C_o is the output inductance and capacitance of the first stage, respectively. R_c is the ESR of bus capacitors. R_L is the parasitic resistance of the output inductors of the first stage.

It is very difficult for a small bus capacitance to keep the system stable when the first stage is open loop (Figure 3-50 (a)). A large bus capacitance (two 820uF Os-con capacitors) has to be added to guarantee the system stability. However, when the first stage is close loop controlled (with either voltage-mode control or current-mode control), the output impedance will be changed to (3-3) (voltage-model control) or (3-4) (current-mode control), respectively.

$$Z_{o\_clv}(s) = \frac{Z_o(s)}{1 + T(s)} \qquad (3\text{-}3)$$

where T(s) is the loop gain of the first stage in voltage mode control.

$$Z_{o\_cli}(s) = \frac{Z_o(s)\cdot\left(1 + T_{i\_1st}(s)\right) + T_{i\_1st}(s)\cdot\frac{G_{vd\_1st}(s)\cdot G_{ii\_1st}(s)}{G_{id\_1st}(s)}}{1 + T_{i\_1st}(s) + T_{v\_1st}(s)} \qquad (3\text{-}4)$$

where $T_{i\_1st}(s)$ and $T_{v\_1st}(s)$ is the current loop gain and the voltage loop gain of the first stage, respectively. $G_{vd\_1st}(s)$ is the control to intermediate bus voltage transfer function. $G_{ii\_1st}(s)$ is the output current to the inductor current transfer function. $G_{id\_1st}(s)$ is the control to the inductor current transfer function.

Based on the close loop design, it is easy to attenuate the output impedance of the first stage and keep the system stable. Figure 3-50 (b) and (c) show the output impedance of the first stage with voltage mode control and current mode control, respectively. Both cases design the bandwidth at 50kHz. There is no interaction between the output impedance of first stage and the input impedance of the second stage. Therefore, closed-loop control for the first stage is preferred.

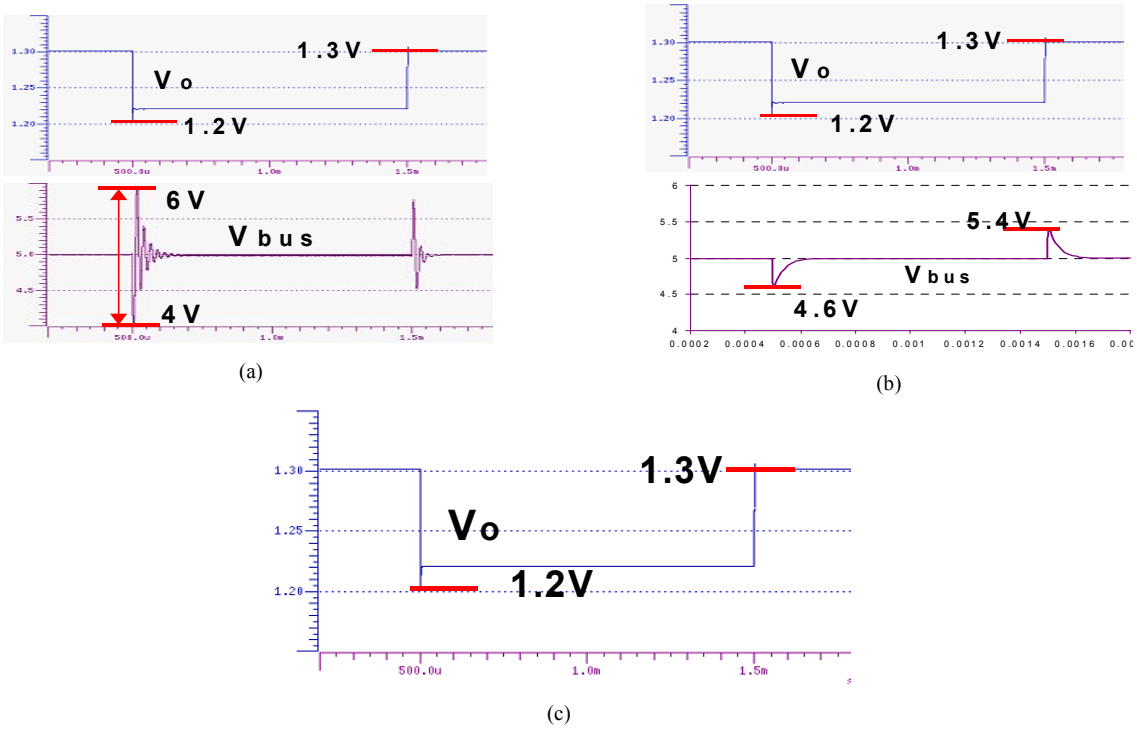


Figure 3-51. The transient simulation: (a) two-stage approach: first stage under voltage-mode control with fc=50kHz; (b) two-stage approach: first stage under current-mode control with fc=50kHz; and (c) single-stage approach.

For the third requirement, simulation method is used to investigate the influence of a small bus capacitance on the output (Figure 3-51). In the simulation, the output current jumps from 10-A to 100-A. Although there is a significant voltage variation on the intermediate bus, the output voltage of the two-stage approach is almost identical to that of the single-stage approach (Figure 3-51(c)). The major reason for this similarity is the high bandwidth design and strong audio-susceptibility of the second stage. With a high-bandwidth design, the second stage can attenuate a large bus voltage oscillation. Therefore, a small bus capacitance doesn't adversely impact the output as long as closed-loop control is used for the second stage.

From the preceding analysis, it is concluded that the intermediate bus capacitance is determined by the ripple requirement. By using closed-loop control, the small bus capacitance is sufficient to keep the system stable while not adversely impacting on the output voltage during the transient.

As a summary, the decoupling capacitors of the single-stage and the two-stage approaches are compared. 1.2V/100A output specification is chosen as an example. Based on the Figure 3-49, it can be easily calculated that a four-phase buck of the single-stage approach needs seven 22 uF ceramic capacitors to attenuate the ripple current. For the two-stage approach, which includes a two-phase buck for the first stage and a four-phase buck for the second stage with 5 V intermediate bus voltage. Based on Figure 3-49 again, it can be calculated that the total number of the input decoupling capacitors and the intermediate bus capacitors is four. So, the two-stage approach doesn't necessitate more input decoupling capacitors; on the contrary, it can save input decoupling capacitors.

3.3. Application of Two-Stage Concept

3.3.1. Applying Two-Stage Concept to Desktop Computer

3.3.1.1. Two-Stage Structure for Desktop Computer

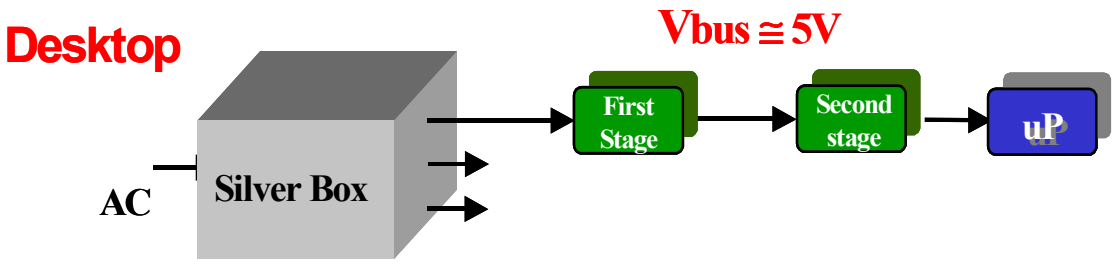


Figure 3-52. The conceptual drawing of two-stage structure for the desktop computer.

The conceptual drawing of two-stage structure for the desktop computer is illustrated in Figure 3-52. One of its implementations is drawn in Figure 3-53. The first stage is still simple buck converter with 12V input. As analyzed in the previous section, the optimal bus voltage is chosen as 5V allowing the second stage to realize high frequency and high efficiency.

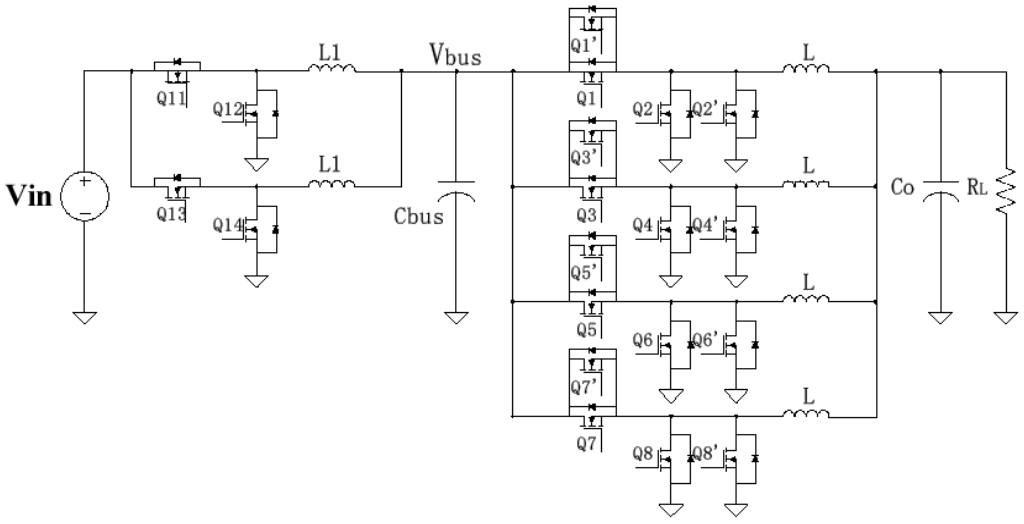


Figure 3-53. Two-stage structure for the desktop computer.

3.3.1.2. Experimental Verification

The setup of the first stage (Figure 3-54) is as follows: a two-phase buck has V_{in}=12-V, V_o=5-V, I_o=25-A, and f_s=300-kHz; LM2639 is the controller; HAT2168 is the top switch; HAT2165 is the bottom switch; L=1.6 uH for each phase; and two 22-uF ceramic capacitors are the bus capacitors. The efficiency curve in Figure 3-56 shows that it can reach 97% efficiency at full load.

The set-up of the second stage (Figure 3-55) is as follows: a four-phase buck has V_{in}=5-V, V_o=1.2-V, I_o=100-A, R_{droop}=1mΩ; for each phase, two HAT2168 are used as the top switch and two Si4864 are used as the bottom switch, the controller is ISL6561 from Intersil, the driver is LM2726 from National Semiconductor. The PCB is 4-layer 2-oz copper.

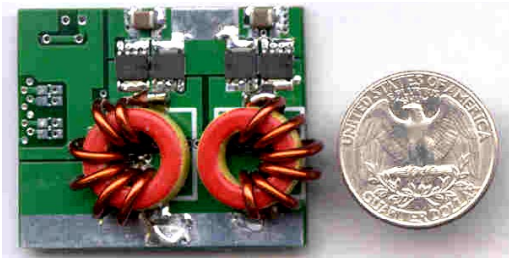


Figure 3-54. The prototype of the first stage.

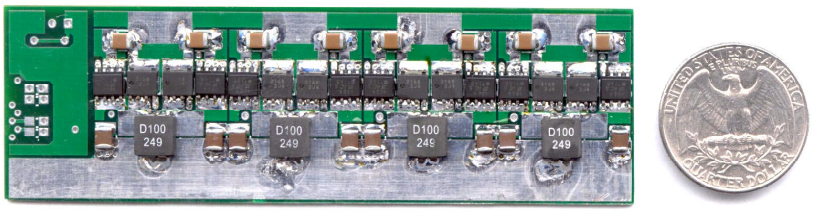


Figure 3-55. The prototype of the second stage.

In the test, the second stage operates at 1MHz and with 200kHz bandwidth design. L=100nH per phase. There are 4 pieces of 100uF ceramic capacitors as bulk capacitors and 440uF decoupling capacitance. The experimental efficiency including the driver loss is shown in Figure 3-57. Combining it with the first stage efficiency, the entire system efficiency is shown in Figure 3-58.

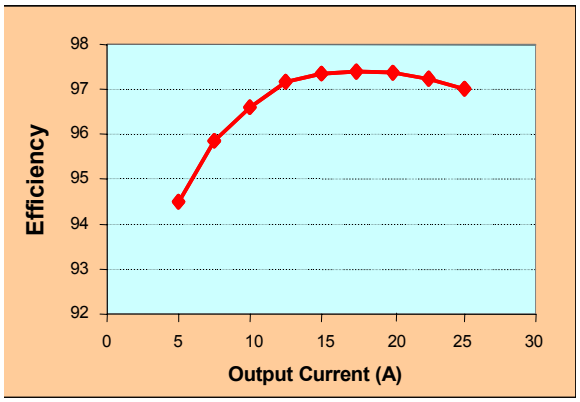


Figure 3-56. The experimental efficiency of the first stage.

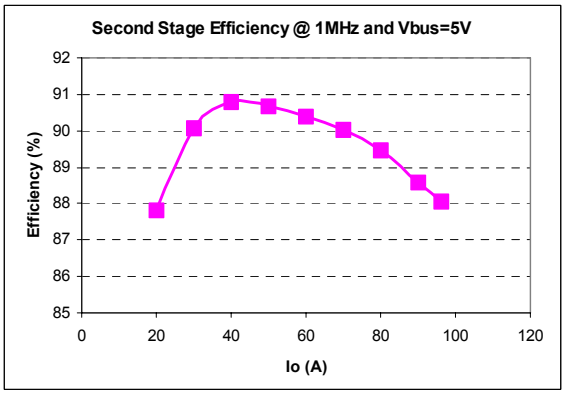


Figure 3-57. The experimental efficiency of the second stage @ 1MHz and Vbus=5V.

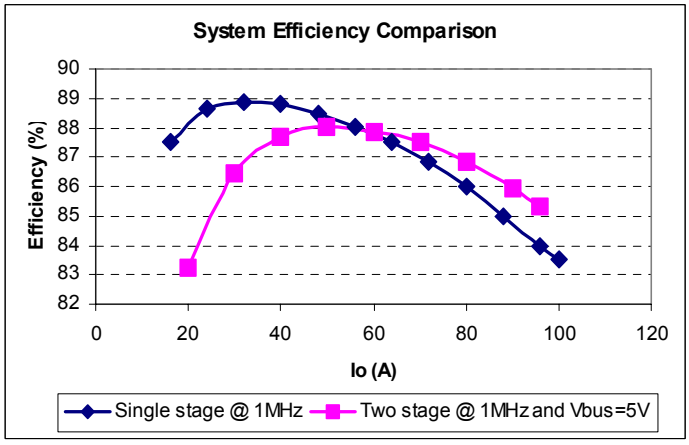


Figure 3-58. Overall efficiency comparison.

In order to get an idea of how good the two-stage approach is, a benchmark is also built. The specification is: a four-phase buck has V_{in}=12-V, V_o=1.2-V, I_o=100-A; for each phase, two HAT2168 are used as the top switch and two HAT2165 are used as the bottom switch, the controller is ISL6561 from Intersil, the driver is LM2726 from National Semiconductor; f_s=1-MHz for each phase, and L=200-nH. The PCB is 4-layer 2-oz copper. Please note that the bottom switch is changed from Si4864 to HAT2165 because Si4864 is a 20-V rating device and cannot sustain 12V input with voltage oscillation, whose peak value is usually higher than 25V. Its efficiency is also shown in Figure 3-58. It can be seen that the two-stage VR is able to achieve higher efficiency than the single stage VR.

The transient waveforms are measured as well as the loop gain. It can be seen that the voltage deviation is within 100mV window with 100A current step, which satisfies 1mΩ R_{droop} design specifications. As discussed in Chapter 2, at 200kHz bandwidth, the output bulk capacitors should switch from Os-Con to ceramic to save the footprint while maintaining the same cost. Verified by the hardware, the capacitor footprint reduction is 85%.

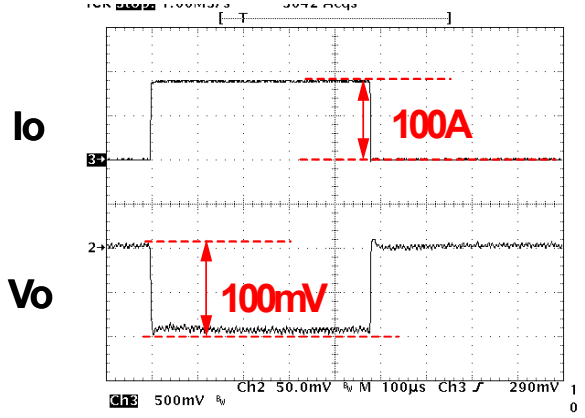


Figure 3-59. Transient response @ ΔI=100A with 450A/us slew rate at 200kHz bandwidth design.

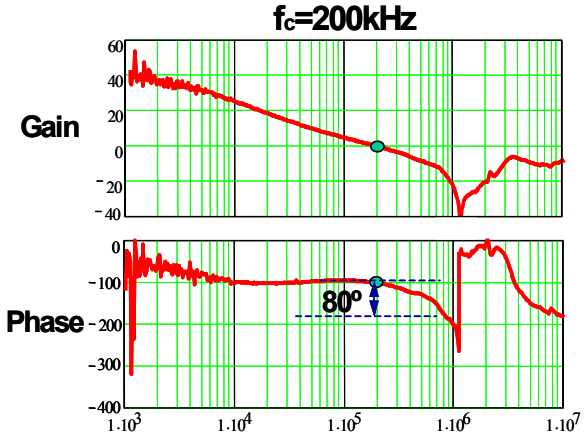


Figure 3-60. The measured loop gain: f_c=200kHz with four 100uF ceramic capacitors.

The next step is to push the switching frequency to 2-MHz in order to realize the 350kHz bandwidth design. L=50-nH for each phase. Only decoupling capacitors serve as the output capacitors and C=440uF. In order to achieve high efficiency, the snubber capacitors are paralleled with the top switches to reduce the switching loss. In addition, the proposed driver is also used to reduce the body diode loss and drive loss. The second stage efficiency is plotted in Figure 3-61.

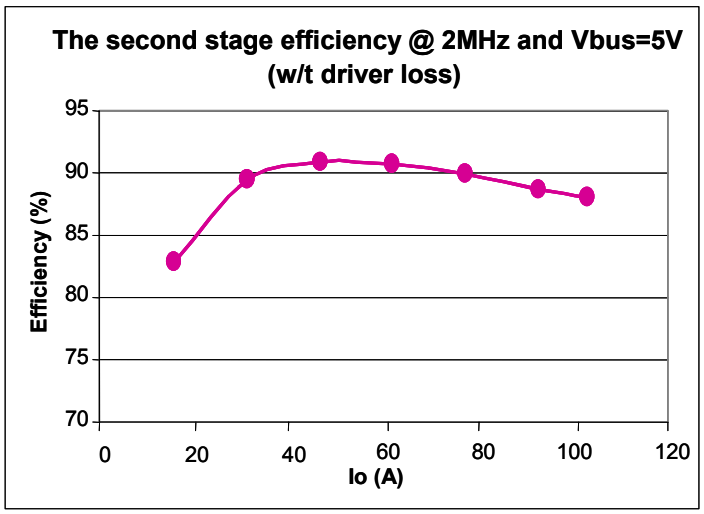


Figure 3-61. The experimental efficiency of the second stage @ 2MHz and Vbus=5V.

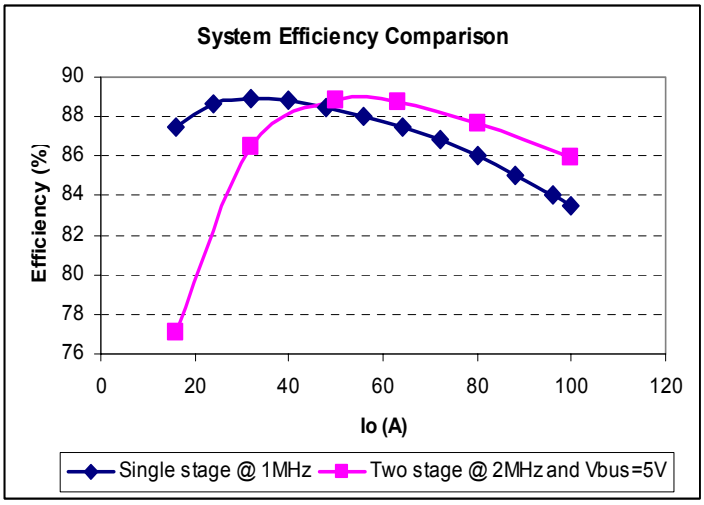


Figure 3-62. Overall efficiency comparison.

Compared with the conventional single stage VR with 1-MHz design, the overall system efficiency of the two-stage approach is even higher at much higher switching frequencies (2-MHz) (Figure 3-62). As the load decreases, the two-stage VRs' efficiency drops quickly due to its two-step conversion. This is a drawback of two-stage approach. Actually, the light load efficiency of the two-stage structure could be improved by the proposed adaptive bus voltage positioning (ABVP) and adaptive frequency positioning (AFP) concepts, which will be elaborated upon in the laptop application.

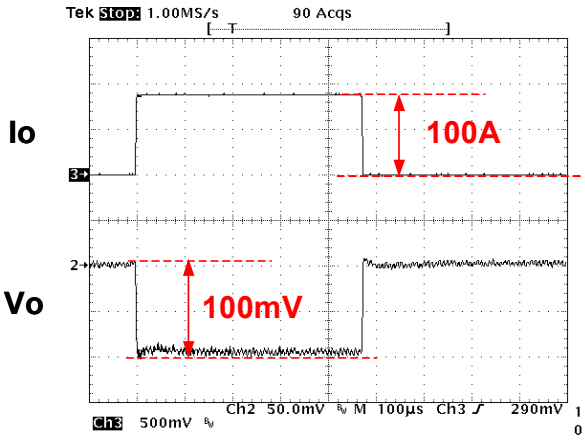


Figure 3-63. Transient response @ ΔI=100A with 450A/us slew rate at 320kHz bandwidth design.

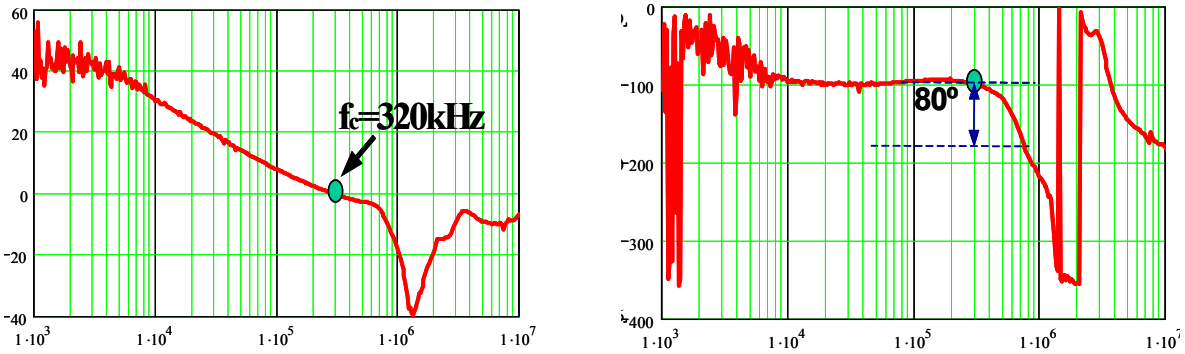


Figure 3-64. The measured loop gain: (a) gain; (b) phase.

At 2MHz switching frequency, high bandwidth design is feasible. The transient response waveforms are shown in Figure 3-63. The controller is Intersil ISL6561. The current injection method is used to realize AVP. The measured loop gain in Figure 3-64 indicates that the bandwidth of the VR is pushed to 320-kHz with sufficient phase margin. The voltage deviation is within the 100-mV window as the current step jumps from no load to 100-A with 450-A/us current slew rate. Please note that the output capacitance is only 440-uF decoupling capacitors and no bulk capacitor is needed at such a high bandwidth design.

Compared with the conventional single-stage buck, the two-stage VR is able to handle the stringent dynamic load step with much smaller output capacitance while achieving higher efficiency at higher frequency design. Based on the cost information of 2004 supplied by the industry, the cost breakdown is plotted in Figure 3-66 for today's microprocessor. It is shown that the two-stage approach can significantly save capacitors' cost although it pays the additional

cost for the first stage. In total, we can still gain a 5% cost reduction, size shrinkage and higher efficiency.

As discussed in the previous section, the future microprocessor will need a lot more capacitors, which will result in a huge cost increase. What can two-stage do? It has been analyzed that the two-stage is able to operate at 4-MHz with future devices, such as low-voltage rating lateral MOSFET. At such a high frequency and 650kHz bandwidth design, not only are the bulk capacitors eliminated, but also the amount of decoupling capacitors can be reduced from 230 to 50 (shown in Figure 3-65). Correspondingly, the cost is greatly reduced as shown in Figure 3-67. The total cost reduction is as high as 40%.

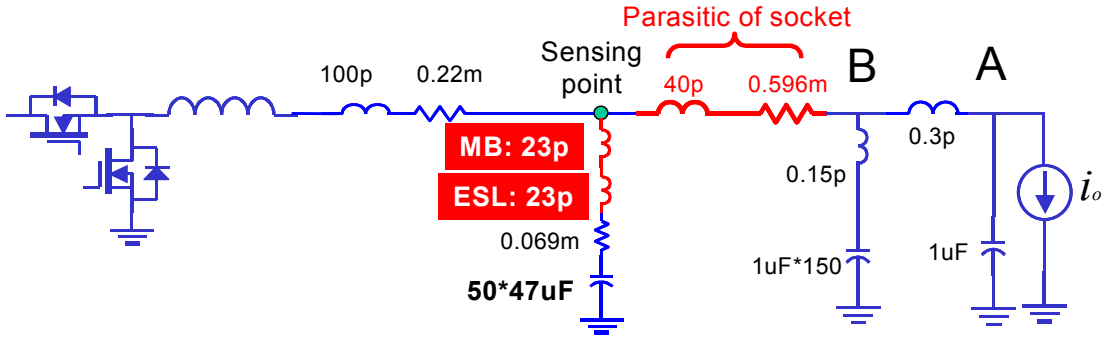


Figure 3-65. The power delivery architecture for future microprocessor with 650kHz bandwidth VR on the motherboard (MB).

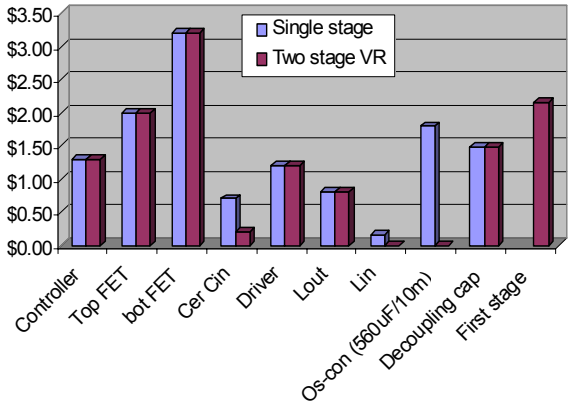


Figure 3-66. Cost comparison between single stage and two-stage VRs for today's CPU (1.3V/100A).

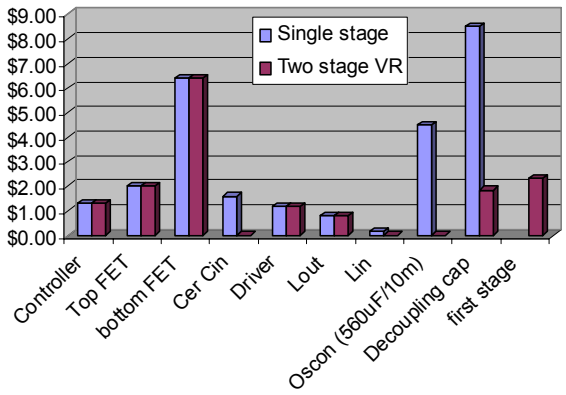


Figure 3-67. Cost comparison between single stage and two-stage VRs for future CPU (0.8V/150A).

As a conclusion, two-stage approach is a more cost-effective solution and a promising candidate for powering the future microprocessors in desktop computer.

3.3.2. Applying Two-Stage Concept to Laptop Computer

Just as the microprocessor for desktop computer, the microprocessors for laptop computers are fast moving as well. It will be proved that the two-stage approach is also effective for laptop computer applications from, not only heavy load efficiency and transient performance points of view, but also the light load efficiency and its good performance at wide input voltage range perspectives. Two-stage approach makes even better sense for laptop VRs.

3.3.2.1. Introduction of Laptop Computer's Power System

As we know, desktop is just one of the two main market segments of personal computers (PCs); the other is the laptop. Recent market news indicates that laptop PCs are expected to oversell desktop PCs in the near future. With laptop gaining more market share, the research on improving laptop VRs is getting more attention.

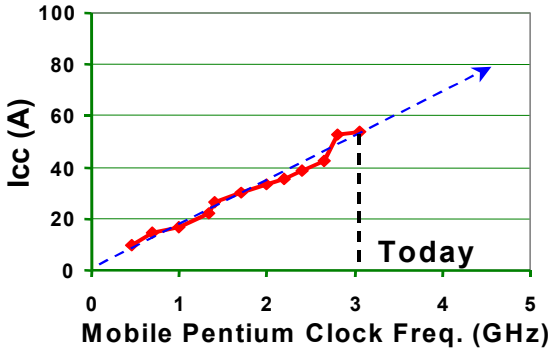


Figure 3-68. The development of fast CPU demanding higher and higher current.

Just as the CPUs for desktop applications are becoming more powerful, so are the CPUs for laptop computer. More current is demanded while the output voltage keeps decreasing as shown in Figure 3-68. Like the desktop VR, a laptop VR needs high efficiency at heavy load to be thermally alive, and needs to have good transient response. In addition, the laptop computer's power system has its unique characteristics, which are very different from that of the desktop computer.

A. Wide Input Voltage Range

Figure 3-69 shows a typical power delivery path of today's laptop computer. The CPU VR, other DC-DC converters and the system loads are connected after the power selector, which

basically selects between two input energy sources: the battery packs and the adaptor. Today, lithium battery packs are most widely used, because lithium is the lightest of all metals, has the greatest electrochemical potential, and provides the largest energy content. Rechargeable batteries using lithium as an electrode are capable of providing both high voltage and excellent capacity, resulting in an extraordinary energy density. The voltage range of a lithium battery cell is 4.2~2.9 V during the course of discharging. The most widely used battery packs have either three or four cells in series. This means a voltage range of 16.8~8.7 V. To charge the battery packs, the adapter has to generate a voltage higher than 16.8 V. 19 V output voltage is widely adopted as a standard. Therefore, it is clear that the input voltage of CPU VR has a wide range: 8.7V~19V. This wide input voltage range is very different from the desktop VR input voltage range of 12V±10%.

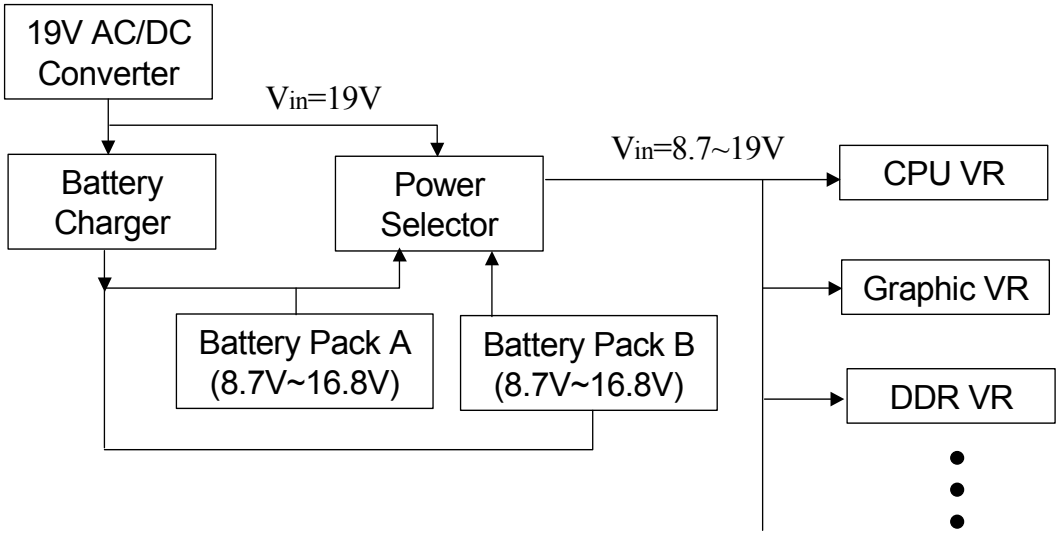


Figure 3-69. The power delivery path of the laptop computer.

B. High Efficiency Requirement in a Wide Load Range

Laptops are constrained by battery life. Laptop users often work on the road, which means the battery is the only energy source available. It is very important to reduce the power consumption of the entire laptop platform to prolong battery life. Figure 3-70 shows a laptop base power consumption analysis [71]. To reduce the CPUs loss, mobile CPUs adopt very complicated power management. It goes into sleep mode frequently. It can be seen that the third biggest part is the power supply loss, which accounts for 10% of the power.

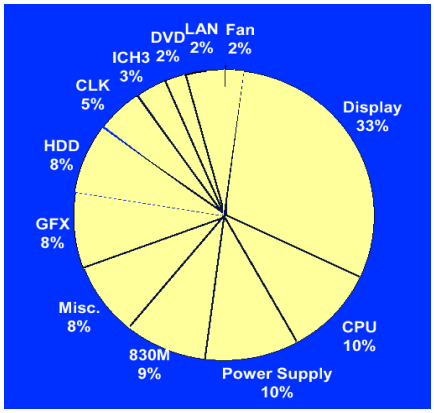


Figure 3-70. A typical laptop computer power consumption analysis. [71]

Just as the desktop VR, the laptop VR needs to have high efficiency at heavy load condition. Moreover, the laptop computer has an additional efficiency requirement for the light load condition. The reason is that the laptop CPUs frequently go into sleep mode even between keystrokes to save energy. The power vs. time shown in Figure 3-71 clearly indicates that the laptop CPUs work mostly at light load and the percentage could be as high as 90% of the time, which makes the power loss during the light load condition comparable with that in the heavy load condition. Therefore, high efficiency at the light load condition is also mandatory to extend the battery life.

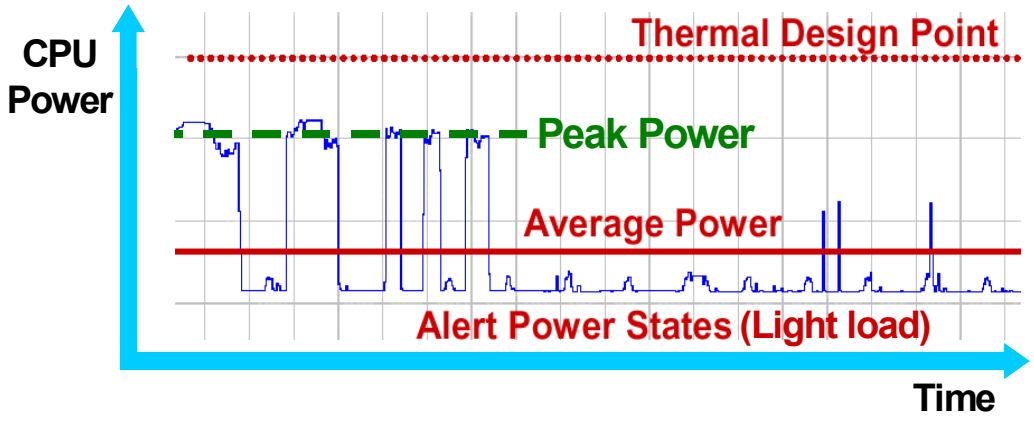


Figure 3-71. The power consumption of a typical mobile CPU.

C. Wide Output Voltage Range

As we know, the mobile CPUs frequently go into sleep mode even between keystrokes to save energy. When the CPU is in sleep mode, the output voltage is normally much lower than in

working mode. For example, today's mobile CPU demands 1.5 V output voltage at working mode while lowering down the output voltage to 0.6~0.8V in the sleep mode. Considering an extreme case, the duty cycle is only 0.03 when the input voltage is 19 V and the output voltage is 0.6 V. Such a small duty cycle makes the circuit design very challenging.

As a summary, the laptop computer basically has three unique "wide" features: wide input voltage range, wide output voltage range and wide efficiency requirement. In the mean time, the stringent transient requirement again puts a big challenge for the VR design.

3.3.2.2. The Limitation of Today's Laptop VR

Future CPUs will be more powerful and will consume more current. If the future VR still follows the current approach, it can be envisioned that the number of output capacitors would need to triple to reach around 6-mF, which means high cost. Meanwhile, the VR would occupy too much precious real estate on the motherboard and make the laptop bulky. High switching frequency can deliver high control bandwidth, and can therefore reduce the number of output capacitors needed to handle the transient response. If the VR can switch at 1 MHz, the achieved control bandwidth will be four times higher than that of a 250KHz VR, and the output capacitors will be dramatically reduced. However, the efficiency is penalized by the high switching frequency.

Since the VR needs to convert the 9 V~19 V input voltage to 1 V or even lower, the duty cycle of the buck topology is extremely small, possibly as small as 0.03. This extreme duty cycle is the main reason why it is so difficult to design an efficient VR at high switching frequencies, which has been discussed in the previous section.

Actually, these challenges for the laptop VR make the exploration of new solutions necessary.

3.3.2.3. Two-Stage Approach in Laptop Application

As analyzed in the previous section, the low input VR has a great potential for high frequency operation. To achieve a relatively low bus voltage, another step-down DC/DC converter is needed as the first stage. The two-stage architecture in laptop computer application is illustrated in Figure 3-72. Compared with the two-stage approach in desktop application, the

only difference is the wide input voltage range. Since the laptop computer has a much wider input range, it is more desirable to regulate the bus voltage, which makes the second stage more comfortable and efficient.

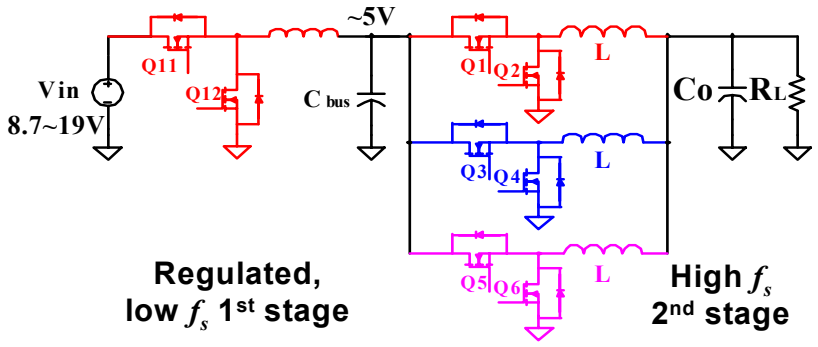


Figure 3-72. The two-stage architecture in laptop computer application with wide input range.

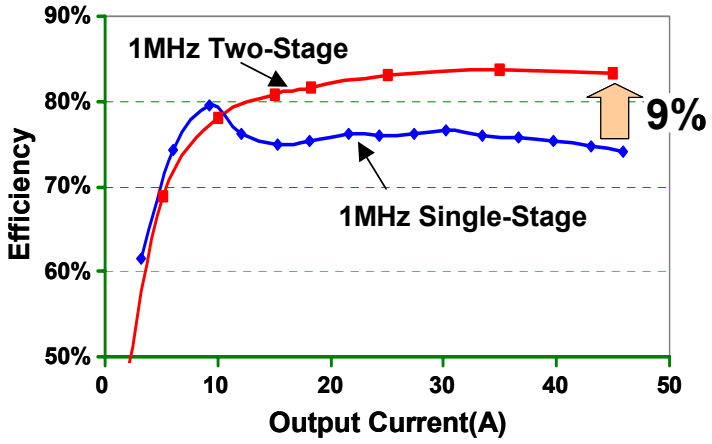


Figure 3-73. The efficiency comparison between the two-stage approach and single stage approach @ 16V input.

Experimental tests are done to evaluate the two-stage architecture as compared to the single-stage architecture [72]. The input voltage is 16 V, and the output voltage is 1.3-V. The single-stage solution is a three-phase buck converter, the switching frequency is 1-MHz, the inductance is 150-nH, and MOSFETs are HAT2168 (top) and HAT2164 (bottom). The two-stage configuration is shown in Figure 3-72. The first-stage switching frequency is 370 KHz, and the inductance is 2.2-uH; the second-stage switching frequency is 1-MHz, and the inductance is 150-nH, and the MOSFETs are HAT2168 (top) and Si4864 (bottom); the bus voltage is 6 V. Figure 3-73 shows the efficiency comparison. It can be seen that the two-stage architecture has a 9%

higher efficiency than the single-stage architecture at heavy load condition. Correspondingly, the output capacitance can be greatly reduced since the bandwidth of the two-stage approach could be 3 times higher than that of the single stage. Hence, from cost point of view, two-stage is cheaper although an additional buck converter is needed as the first stage.

Again, it is proven that the two-stage approach has a much better high frequency performance than does the conventional single-stage at the heavy load condition. Then, what about its performance at the light load condition? As shown in Figure 3-73, the light load efficiency is not as good as that of the single stage VR.

Light Load Efficiency Improvement Based on Two-Stage Approach [64As mentioned in previous chapter, laptop computers have a stringent light load requirement in order to extend the battery life. A lot of control strategies, such as pulse-frequency-modulation (PFM) [65][66][67], burst mode [68], phase-shedding method [68] and etc., have been proposed and widely used in the commercial IC controllers. Basically, all of those control methods are using discontinuous current mode (DCM) when the load is sufficiently low. Then, according to gain expression

$$M = \frac{V_o}{V_{in}} = \frac{2}{1 + \sqrt{1 + \frac{8L}{R T_{on}^2 f_s}}} \qquad (3\text{-}5)$$

where L is the output inductance, R is the load, T_{on} is the turn-on time of the top switch and f_s is the switching frequency.

It is found that the switching frequency is proportionally decreasing as the load is reduced. Is there any other control solution to further improve the light load efficiency?

A. Adaptive-Bus-Voltage-Positioning (ABVP) Concept

The reference [64] proposed an ABVP concept to improve the two-stage efficiency at light load condition. The basic idea is to lower down the bus voltage at the light load condition to reduce the switching related losses of the second stage. The analysis shows a trend that when the load is lighter, the optimal bus voltage is lower. At heavy load, the optimal bus voltage is around 5~6V as discussed previously; at light load, the optimal bus voltage gradually decreases. Base on that, the control strategy is illustrated in Figure 3-74.

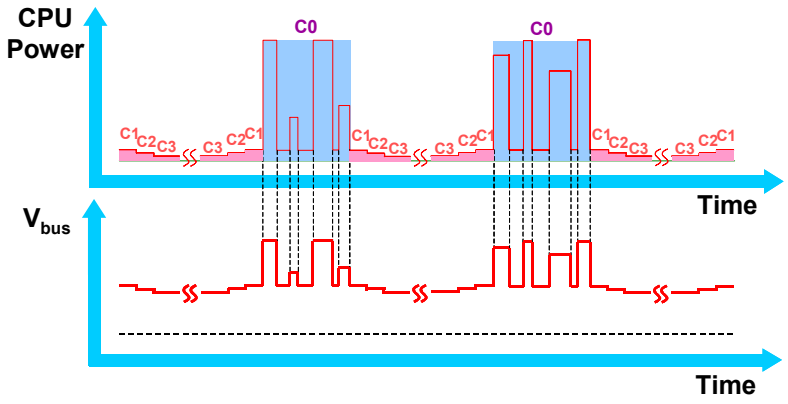


Figure 3-74. The CPU power consumption and the bus voltage following ABVP control strategy.

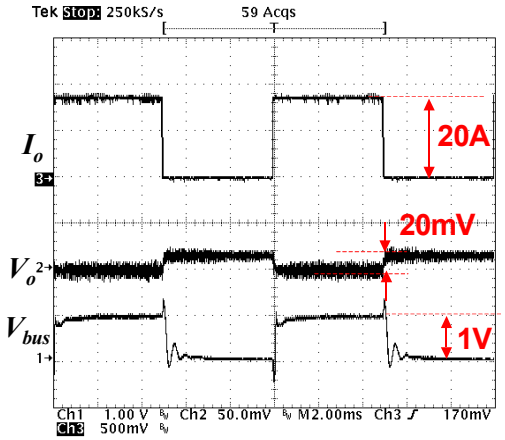


Figure 3-75. The transient waveforms of output current, output voltage and bus voltage.

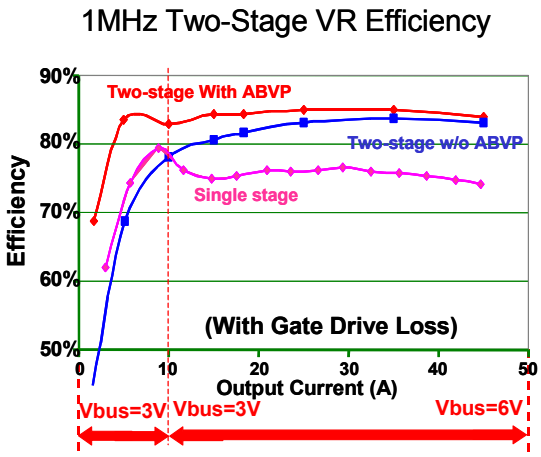


Figure 3-76. The efficiency improvement by ABVP control strategy.

A prototype is built to verify the feasibility of this concept. The input voltage is 12-V. The output voltage is transits from 1.28 to 1.3-V as load jumps from 0 to 20-A. The bus voltage varies from 4.2 to 5.3-V as load changes from 20-A to 0-A. The inductance of the first stage is 10-uH. The inductance of the second stage is 300-nH for each phase. The first stage switching frequency is 200-kHz and that of the second stage is 1-MHz. The bus capacitance is 1-mF and output capacitance is 1-mF. Figure 3-75 shows the experimental waveforms. It can be seen that the bus voltage jumps from 4-V to 5-V as the output current transits from 0-A to 20-A. Both ABVP and AVP functions are realized. The experimental efficiency in Figure 3-76 indicates that the ABVP concept is able to improve the efficiency in the whole load range. The improvement is more significant at the lighter load.

In the conventional single-stage configuration, the input voltage is regulated with only ±10% tolerance. In addition, the bus is also tied to other VRs, such as graphic VR, memory VR and so on. It is impossible to change the input voltage according to the load condition of CPUs only. Fortunately, in the two-stage solution, an intermediate bus voltage is generated, which is dedicated to the VR of CPUs. Therefore, to change the bus voltage according to the load condition is feasible. This is another big advantage of the two-stage approach.

B. Adaptive-Frequency-Positioning (AFP) Concept

Based on ABVP concept, it can be seen that the bus voltage is adjusted by a factor of two. The output inductor current ripple is changed accordingly. This relationship is given by

$$\Delta i_L = \frac{V_{out}}{Lf_s} \cdot (1 - D) \qquad (3\text{-}6)$$

where Δi_L is the peak-to-peak inductor current ripple; V_{out} is the output voltage; L is the inductance of each channel inductor; f_s is the switching frequency per channel; D is the duty cycle. When input voltage changes, D changes. Figure 3-77 illustrates the relationship between the normalized inductor ripple current, Δi_L, and the input voltage change, here equivalently the bus voltage.

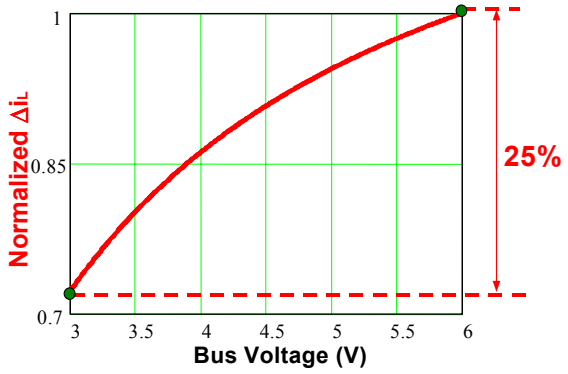


Figure 3-77. Normalized 2nd stage inductor current ripple when bus voltage changes.

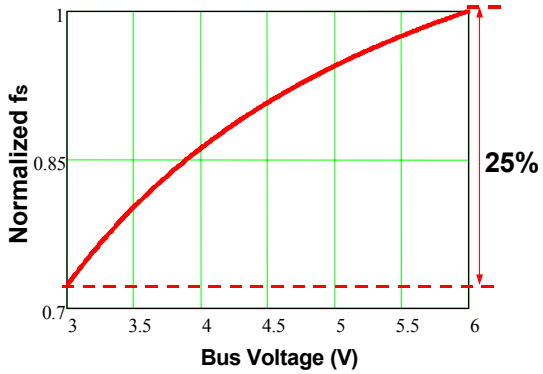


Figure 3-78. Normalized 2nd stage switching frequency when bus voltage changes.

If we look from a different angle, why can't we keep the same ripple current over the V_{bus} range? The whole power stage is designed to handle the ripple current at the maximum V_{bus}, 6V for instance. Why can't we take this advantage to reduce the switching frequency proportionally

so that the system efficiency can be improved when the bus voltage decreases, or, the load current decreases. This is shown in Figure 3-78, as the switching frequency becomes the vertical axis.

Figure 3-79 shows the measured efficiency improvement when this AFP concept applies. About 2~3% improvement is achieved at light load over ABVP only two-stage VRs.

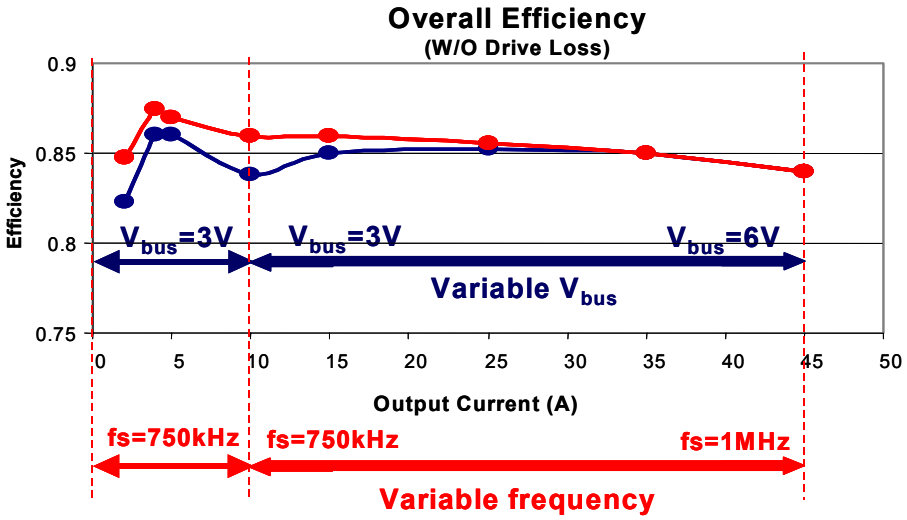


Figure 3-79. The measured efficiency improvement when this AFP concept applies.

As a conclusion, the two-stage approach achieves higher efficiency than the single-stage solution over a wide load range under the entire input voltage range. It is also a promising solution for future laptop VRs.

3.4. Summary

In this chapter, the challenge for the future VR design is addressed. To meet the future 12V VR specification, the two-stage approach is proposed. The design considerations are thoroughly discussed. The analysis shows that the first stage could be very efficient because its switching frequency is not necessarily high. Normally, 300~500kHz is sufficient. The second stage with low input voltage can run at very high switching frequencies while maintaining high efficiency because the low input voltage greatly reduces the switching loss and body diode reverse recovery loss and the low-voltage-rating device can be safely used to further improve the VRs' performance. Based on today's commercial devices, 2-MHz VR is realizable.

In this chapter, several methods are also proposed to further improve VR's efficiency based on two-stage approach. It is well known that DrMOS can improve the efficiency because of the parasitic components' reduction. However, it is not enough for a low input voltage case, such as the two-stage approach. Based on the observation, snubber capacitor can be paralleled with the top switch to significantly reduce the turn-off loss. Simulation results show 70% switching loss reduction at 4MHz frequency. A new gate driver is also proposed in this chapter. A transformer or coupled-inductor is utilized to couple the gate-source capacitors of top switch and bottom switch of VR and the dead time could be automatically eliminated. Hence, the body diode loss is greatly reduced. In addition, the magnetizing current is used to realize ZVS of driver, which means a gate drive loss saving. All the efforts make 4-MHz VR feasible.

To optimize the system performance, the intermediate bus is also investigated. The analysis indicates that 5-V is the optimal bus voltage for the high frequency application (beyond 1MHz). And the intermediate bus capacitance is smaller than that in the single-stage approach, as long as the first stage is close-loop controlled.

The experiment results verified the analysis. The second stage is running at 2MHz per phase, and its efficiency is as high as 89% at full load. The whole system efficiency is as high as 86%. The bandwidth of the second stage can be pushed up to 320 kHz to eliminate the bulk capacitors, which results in a big cost saving. Compared with today's single-stage approach, the two-stage approach is very promising from both performance and cost-effectiveness perspectives.

In addition, the two-stage approach is successfully applied to the laptop computer application to improve the whole system performance while lowering the cost. In the laptop computer, two-stage approach can not only improve the full load efficiency, but also improve the light load efficiency based on the proposed ABVP and AFP control strategy. The experimental results prove that two-stage approach is effective over a wide load range and wide input range. It can be seen that two-stage approach makes even better sense for laptop computer application.

As a conclusion, two-stage approach is a promising solution for future computer, where fast transient, tight regulation, and large output current and low output voltage are required.

Chapter 4. Extension of Two-Stage Concept for 48V Distributed Power Systems (DPS)

4.1. Introduction of DPS

The DPS is originally from the telephone industry. Alternating current (AC) power from the mains is rectified, filtered, passed over a battery and distributed to the equipment in the central office, whose power is distributed at around –48-V direct current (DC). The distribution buses are routed to each equipment frame and through each frame to its sub-racks or card cages.

In the 1970s, the telephone equipment typically used the –48-V directly. When electronic switching was introduced, centralized power in each sub-rack was typical. Each sub-rack would have one or more DC-DC converters. These converters converted the –48-V from the central office distribution to the voltages required by the equipment in that rack. The output of the DC-DC converters was bused across the back plane to the cards, or in the telephone jargon, "circuit packs" in that sub-rack.

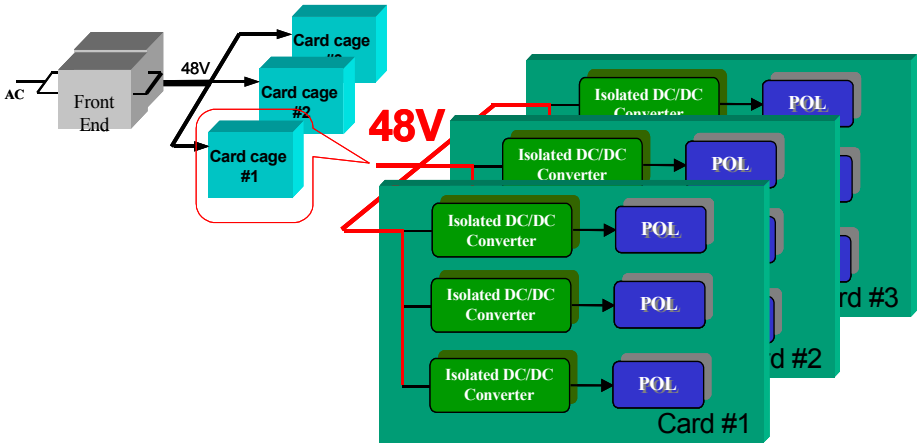


Figure 4-1. Conventional distribute power architecture.

In the early to middle 1980s, the compact, board mount DC-DC converter was introduced. The –48-V was routed directly to each circuit card. The DC-DC converters on each card created the supply voltages needed by that card (shown in Figure 4-1).

The computer industry soon followed the use of on-board DC-DC converters. Instead of the –48-V, the computer industry adopted +48-V for high-end computer systems, such as server and workstation computers. By the middle 1990s, the use of distributed power with on-board conversion was growing in popularity. The higher cost was offset by the ease of implementing highly available and highly scalable systems. These advantages made DPS most attractive in networking and high end computing applications.

4.2. Challenges for Traditional DPS

However, DPS is facing more and more challenges in the recent years.

As the integrated circuit (IC) quickly develops, the feature size of silicon devices has decreased at a steady rate. Each step in feature size requires a reduction in operating voltage and higher current. In order to maximize the performance, a wide variety of integrated circuits are used. The result is a system that requires many different supply voltages for various devices in the systems. For example, having over 10 power supplies in one motherboard is not unusual today. In addition, as more circuits are integrated into a single die, the power and the current slew-rate are becoming higher. These challenges make the design of the isolated DC-DC converter difficult.

Server application is used as an example to elaborate the challenges and limitations of today's 48V DPS. Figure 4-2 shows the power structure of server applications with Intel Itanium microprocessor. For each processor, there is a dedicated power converter.

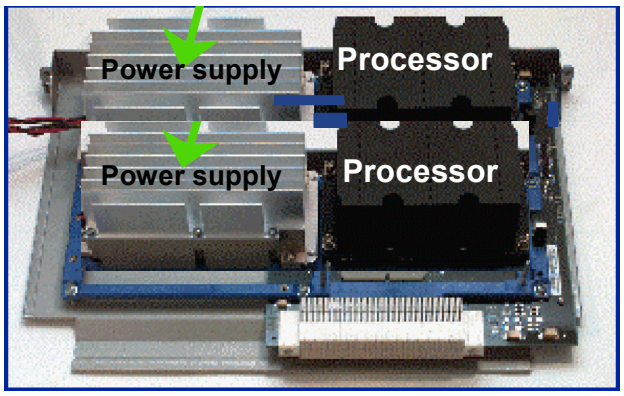


Figure 4-2. The power structure of Intel Itanium microprocessor for server application.

As the microprocessor is fast moving forward, the output voltage keeps decreasing while the current is increasing. It is expected Vo will reduce from 1.3V to 0.8V and Io increases from 100A to over 250A (shown in Figure 4-3) [73].

On the other hand, the power density requirement is more and more stringent. Figure 4-4 shows the trend of the power density for server power supply [74]. It can be expected that the power supply design will be more and more challenging.

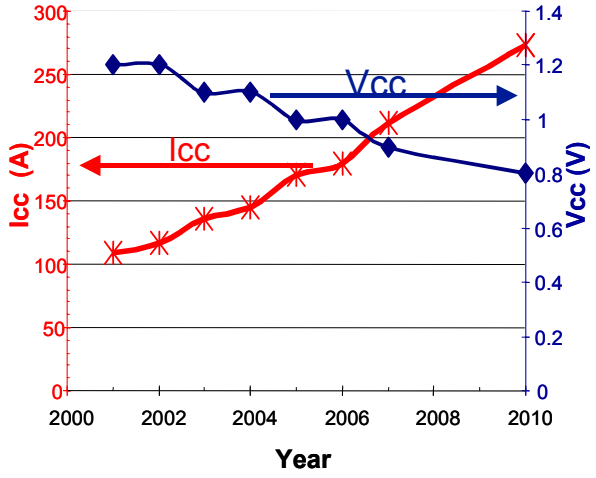


Figure 4-3. The roadmap of high end server microprocessor.

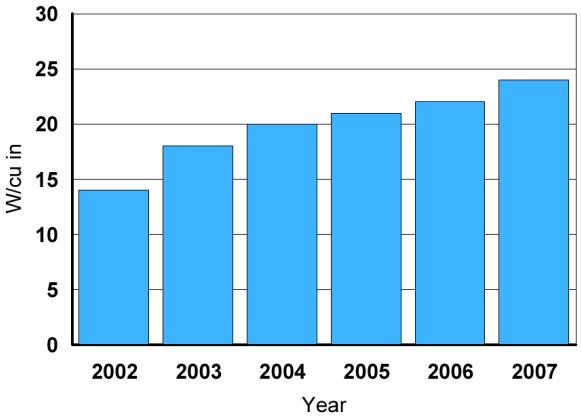


Figure 4-4. The trend of power density requirement for server power system.

If today's low frequency solution is still used, more and more capacitors have to be paralleled, which will result in a bulky and costly system. In order to shrink the passive components, especially the output capacitance, the switching frequency and bandwidth need to be pushed higher.

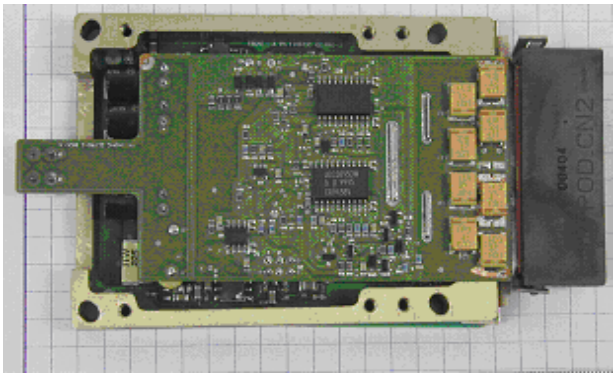


Figure 4-5. The power supply for Intel Itanium server.

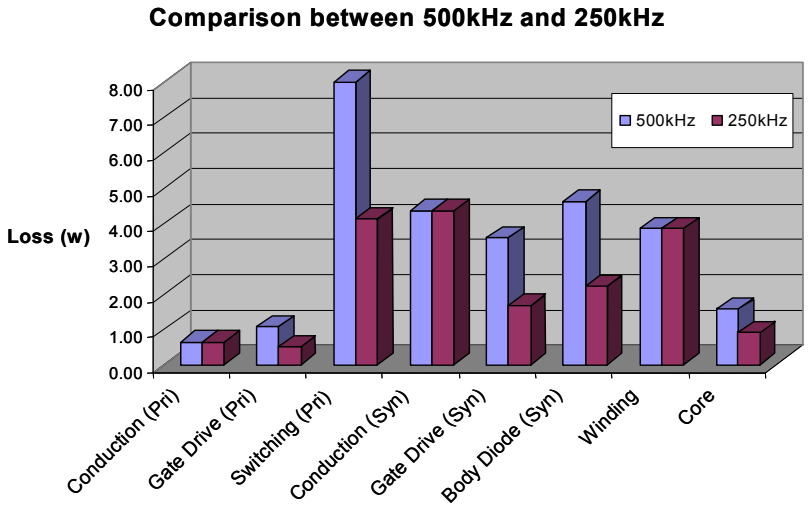


Figure 4-6. The loss breakdown of the power converter in Figure 4-5.

Figure 4-5 shows a typical power converter used in traditional DPS for server application. It is a full-bridge converter with phase-shifted control. Its input voltage is 48V, and output specification is Vo=1.2V, Io=100A and ΔVo=150mV at half load transient. Its switching frequency is 250kHz. The output inductors are made of EI22 core. The transformer uses EI32 core. It can be seen that for today's server processor, there have already been 16 tantalum capacitors used (eight on top and another eight on the backside). For future specifications, if the switching frequency is kept the same, the output capacitance needs to be doubled or even tripled, and the whole circuit will be very bulky and costly.

Unfortunately, today's isolated PWM converter lacks of high frequency capability. Figure 4-6 shows the loss breakdown of the power converter in Figure 4-5 running at 250kHz and 500kHz respectively. The increasing switching loss and body diode loss dramatically suffer the performance.

In addition, because of the existence of the transformer and the isolation of feedback loop, it is difficult to design a high bandwidth for a traditional DPS to satisfy the future requirement of the load even with high switching frequency. Therefore bulky output capacitance is required.

From the cost point of view, traditional DPS has higher cost than the centralized power systems. The major contributor is the large number of DC-DC converters for each load. Because of the requirement of isolation, every DC-DC converter has its own transformer. Moreover, the feedback loop needs isolation too. Therefore, the cost of DPS is usually higher than the

centralized power systems. In the near future, the number of power supplies will be even larger, which means even higher cost.

It can be envisioned that some new system architectures need to be investigated for the future communication and computer applications.

4.3. Two-Stage Approach: Intermediate Bus Architecture (IBA)

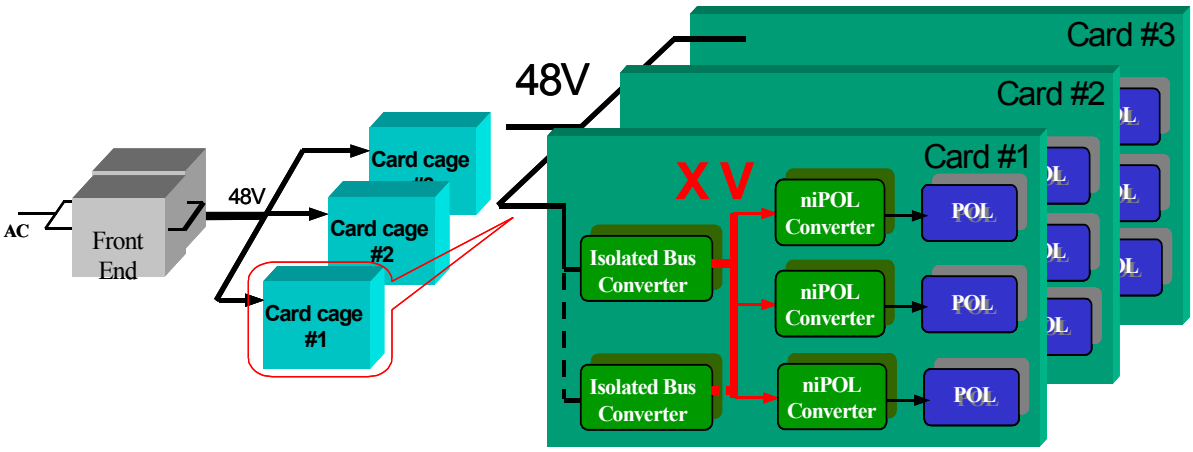


Figure 4-7. Intermediate bus architecture.

Actually, in most cases, only one isolated DC-DC converter is needed in one circuit card, which means the design complexity could be reduced. The output of this isolated converter could serve as the input of non-isolated DC-DC converters, which convert the voltages needed by load. Basically, this is a two-stage structure. This structure is also called intermediate bus architecture (IBA) as illustrated in Figure 4-7.

Another big driving force for this architecture is the standardization of non-isolated DC-DC converters, which make the cost drop quickly. From the technique perspective, the non-isolated DC-DC converter is pretty much mature. The non-isolated DC-DC converter usually can operate at much higher switching frequency (MHz range) than an isolated one while maintaining good efficiency. As shown in the previous section, the second stage could achieve around 85% efficiency at 2MHz switching frequency. Furthermore, its feedback loop doesn't need isolation, which benefits the high bandwidth design. Hence, it is good at handling the high slew-rate current, which means an effective reduction of output capacitance. Also, the passive components' shrinkage saves precious real estate.

On the other hand, the first stage, also called bus converter or DC/DC transformer, could be designed much more efficient because the regulation is optional and the duty cycle could be set as large as possible. Compared with the conventional isolated DC-DC converter, the bus converter has much higher power density and efficiency, which in turn further saves the real estate. Meanwhile, it is easy to be standardized.

Based on the reasons as above, IBA is quickly picked up by the communication and computer industry [75][76][77][78]. In the recent years, the bus converter has become one of the hottest products. Many bus converters have been released recently. Because the second stage has been discussed in detail in the previous chapter, only bus converter is analyzed here.

Basically, the bus converter can be divided into two categories [78], one is regulated, and the other is unregulated. In the telecommunication application, the input voltage is usually as wide as 36~75 V. The bus voltage regulation is usually required. For systems that need a tightly regulated voltage on the bus voltage, about the only choice is a traditional DC-DC converter. For server and other computer applications, the input voltage range is narrow. The tolerance is usually ±10% (42~53 V). The bus voltage regulation is optional. Therefore, the majority of today's bus converters for server applications are unregulated, which is discussed in this chapter.

Another unclear item is the optimal bus voltage. At very beginning, the intermediate bus voltage is chosen as 12-V because the following second stage could use the mature infrastructures. Recently, as the second stage frequency increases, 12-V might not be suitable because it results in larger losses at the second stage. Some server manufacturers, such as hp and Sun, change the intermediate bus voltage from 12-V to 8~9-V. However, the relationship between the bus voltage and the system performance is still not clear, which will be addressed in this chapter.

4.3.1. Un-regulated Bus Converter

4.3.1.1. Limitation of Today's Topology for Un-Regulated Bus Converter

The most of current unregulated bus converters, as shown in Figure 4-8 are open loop designed, convert 48-V input to 12-V output and deliver 20-A current in a quarter-brick size. The

power density is around 100 ~150-W/in^3 (refer to Table 4-1). The duty cycle is fixed at 50% to maximize the efficiency.

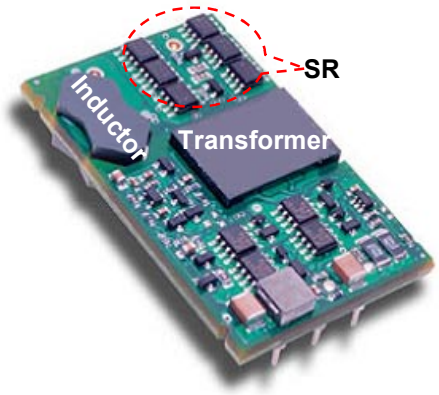


Figure 4-8. A typical bus converter product of industry.

Table 4-1. Industry Practices of the Bus Converter

Company	Output Power (W)	Volumn (in^3)	Efficiency at full load (%)	Power density (W/in^3)
IR	150	½ of a quarter brick 0.85×1.95×1.01	96	89
Synqor	240	Quarter brick 1.45 ×2.3 × 0.43	96	167
Artesyn	240	Quarter brick 1.45 ×2.3 × 0.43	96	167
Power-one	300	Quarter brick 1.45 ×2.3 × 0.4	96.2	225
Vicor/Celestica	200	1.26× 0.85 × 0.24	96	800

Generally, the unregulated bus converter has higher efficiency because the primary switches run at a duty cycle of around 50%, which facilitates ZVS. Today's bus converters still use the conventional topology, e.g., the full-bridge converter with center-tapped rectifier, as shown in Figure 4-9. To increase the output power, the output current must be pushed as high as possible. In order to reduce the conduction loss, more and more devices should be paralleled. However, the real estate is limited and there is no room for more devices. It is obvious that the

transformer and inductor are the bulkiest components on the board (refer to Figure 4-8). High frequency is an effective way to shrink these passive components. Unfortunately, the performance of the conventional topology is severely degraded as the switching frequency increases.

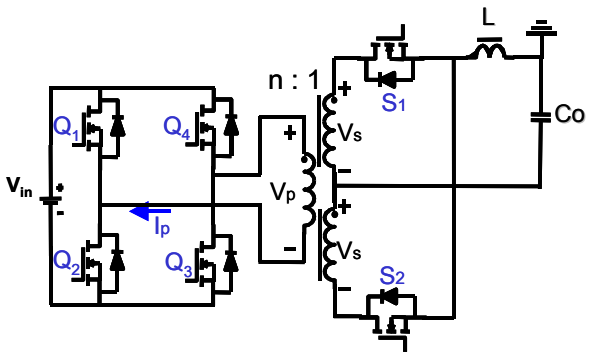


Figure 4-9. Conventional full-bridge converter with center-tapped rectifier.

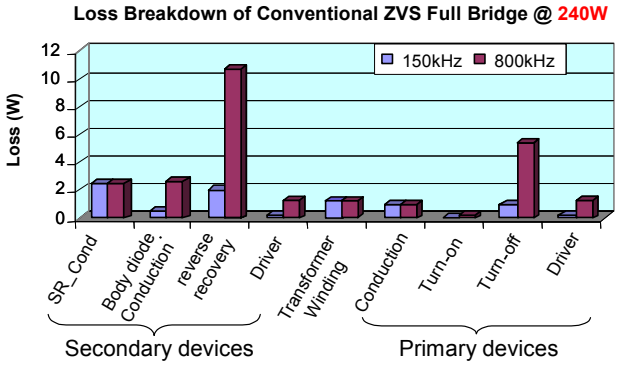


Figure 4-10. The loss breakdown of the conventional full-bridge converter at 150kHz and 800kHz.

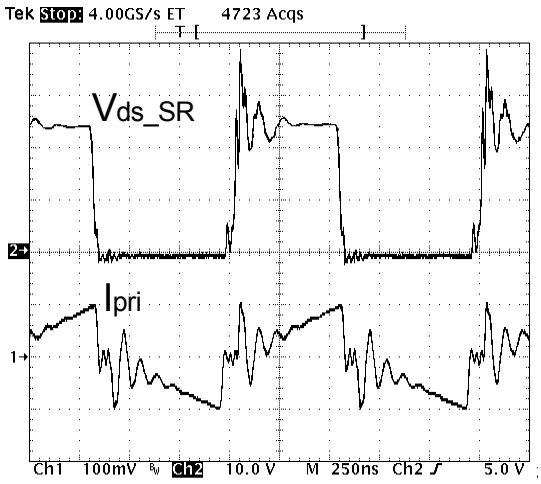


Figure 4-11. The drain-to-source voltage across the synchronous rectifier and the primary current.

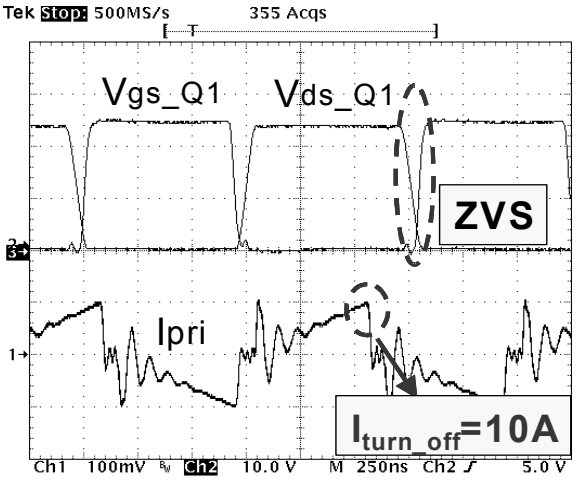


Figure 4-12. The gate signal, drain-to-source voltage of the primary switch and the primary current.

Figure 4-10 shows the loss breakdowns of a conventional full-bridge converter running at 150 kHz and 800 kHz, respectively. It is clear that the body diode loss [79][80][81] and the switching loss of the primary switches dramatically increase as the frequency increases. Figure 4-11 shows the severe ringing across the SRs, which is caused by the reverse-recovery charge of the body diode. For the 12V-output-voltage application, the voltage spike is usually higher than

30-V. Therefore; a 60-V device instead of 30-V one has to be used. Generally, the $R_{ds(on)}$ of a 60-V device is higher than that of a 30-V device. The waveforms in Figure 4-12 indicate that although ZVS can be achieved at certain load condition, the turn-off current of the primary switches is very high, which causes high turn-off loss. In order to achieve high power density, the body diode loss and switching loss should be reduced.

4.3.1.2. Proposed Inductor-less Full-Bridge Converter

Taking a hard look at the conventional full-bridge converter, it is found that the leakage inductor could be used as the "bridge" linking the input source and the output capacitors [82]. Therefore, the output inductor might not be necessary. After the output inductor is eliminated, other benefits appear. First of all, the magnetizing current of the transformer can be used to achieve ZVS. Furthermore, if the output capacitance is properly designed, the leakage inductor will resonate with the output capacitors and ZCS can also be achieved. Most importantly, the body diode loss can be easily eliminated by the use of simple timing synchronization. This concept can be applied to many topologies, e.g., full bridge, half-bridge, active-clamped forward, resonant-reset forward, push-pull, push-pull forward and so on. Figure 4-13 shows the full bridge converter employing the concepts described as above. The resonant inductors are the leakage inductors L_{k1} and L_{k2}. The resonant capacitor is the output cap C_o.

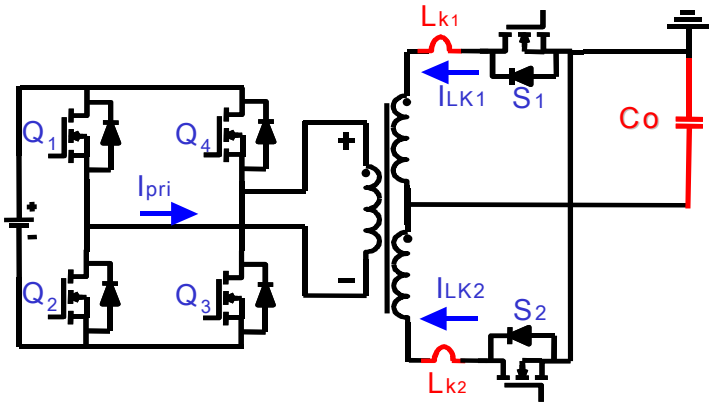


Figure 4-13. Proposed inductor-less full-bridge converter.

Compared with the conventional resonant converter, the output capacitor serves as the resonant capacitor to further simplify the circuit. The output voltage is composed of a DC component, which is the V_{in}/n, and a large ripple, e.g. for 12V/30A output case, the peak-to-peak

voltage is around 1 V. However, it is not difficult for the second stage to get rid of the voltage ripple by its input filter because the ripple frequency is very high. Therefore, large ripple is allowed in the unregulated bus converter.

Basically, it can be classified into two cases. One is a desired operation without any body diode conduction and turn-off loss at secondary side, which is illustrated in Figure 4-14. The other is non-ideal case with small body diode conduction time or turn-off loss. The analysis results indicate that small body diode conduction is acceptable while turn-off loss at the secondary side should be avoided. The ideal operation is briefly described in this chapter. The detailed operation principle and design guideline are elaborated in Appendix 2.

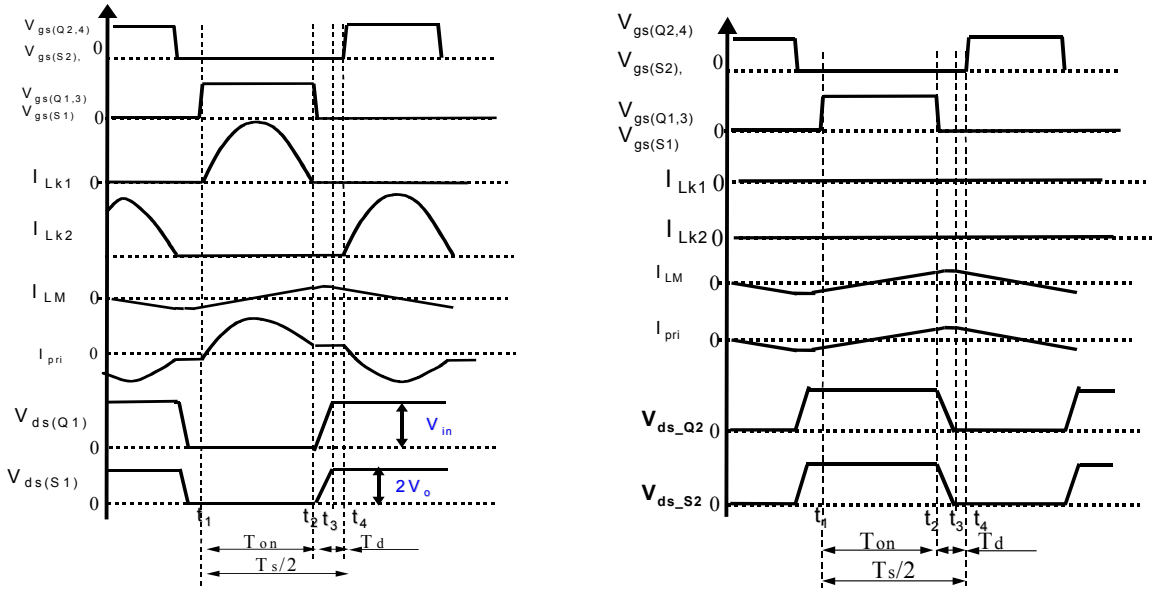


Figure 4-14. The operation waveforms of the inductor-less full-bridge converter.

During t_1 and t_2, the primary switches Q_1 and Q_3 and the secondary switch S_1 are on, the energy is transferred from the primary side to the secondary side through the leakage inductor L_{k1} of the transformer.

At t_2, switches Q_1, Q_3 and S_1 turn off. The resonant tank stops working. The output current is only supplied by the output capacitor C_o. Meanwhile, The magnetizing current starts to charge and discharge the output capacitors of the primary switches. Therefore, ZVS can be achieved for the primary switches. In the mean time, the output capacitors of the SRs, C_{os1} and C_{os2}, also serve as snubber capacitors. So ZVS for the SRs can also be achieved.

After t_3, the body diode of Q_2 and Q_4 are on, the magnetizing current is recovered by the input source.

Starting from t_4, another half-cycle begins and the resonant tank restarts to work. The operation is exactly same as that described above except that the polarity is changed.

The loss breakdown comparison is shown in Figure 4-15.

By the resonant technique, the body diode conduction loss and reverse recovery loss are eliminated. ZVS is realized for all devices and nearly ZCS is accomplished for the primary switches. Therefore, 65% power loss reduction is achieved when the converter is operating at 800 kHz. Compared with 150kHz conventional ZVS full bridge converter, the proposed topology is able to achieve even smaller power loss with much higher switching frequency.

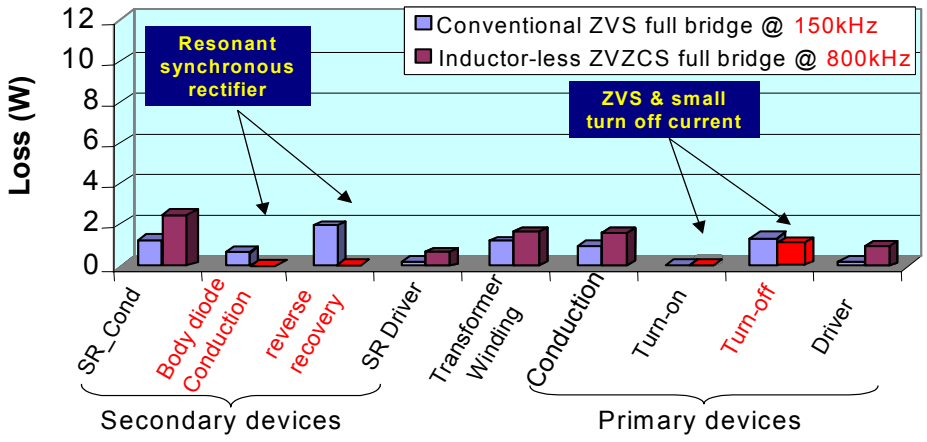


Figure 4-15. Loss breakdown comparison between conventional full bridge at 150kHz and proposed topology at 800kHz.

4.3.1.3. Experimental Verification for Bus Converter

A prototype with the quarter-brick-sized design is built to verify the described benefits. The specification is: V_{in}=48V, V_o=12V, P_o=500w, f_s=800kHz, L_k=10nH, and C_o=20uF. The primary devices are four Fairchild FD10AN06s. The primary side driver is Intersil HIP2101. The secondary switches are four HAT2165s. Instead of single transformer, two transformers are used in order to distribute the loss and to achieve better thermal performance. The transformers use TDK PC44 EIR18 cores with turns-ratios of 2:1. Figure 4-16 shows a picture of the prototype.

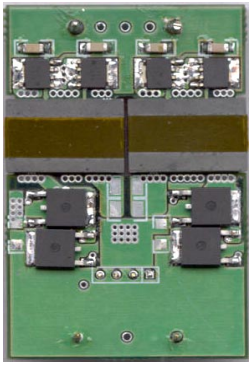


Figure 4-16. A picture of the inductor-less full-bridge converter prototype.

Figure 4-17 indicates that ZVS for the primary switches can be achieved. And most importantly, the turn-off current of the primary switches is only 2-A. Compared with 10-A turn-off current shown in Figure 4-12, the turn-off loss can be dramatically reduced. Figure 4-18 shows that the gate drive signal for the SR is very clean even without using an external gate resistor for damping. This is because of the ZVS operation. Figure 4-19 shows the clean drain-to-source voltage across the SRs. Because there is no voltage spike across the SRs, a 30V device (HAT2165) can be safely used. Figure 4-20 zooms in the parts 1 and 2 that are circled in Figure 4-19. The voltage scale of V_{ds_S1} is 2-V/scale. If the body diode conducts current, the drain-to-source voltage of the SRs is around –0.7-V. Figure 4-20 clearly shows that there is no body diode conduction.

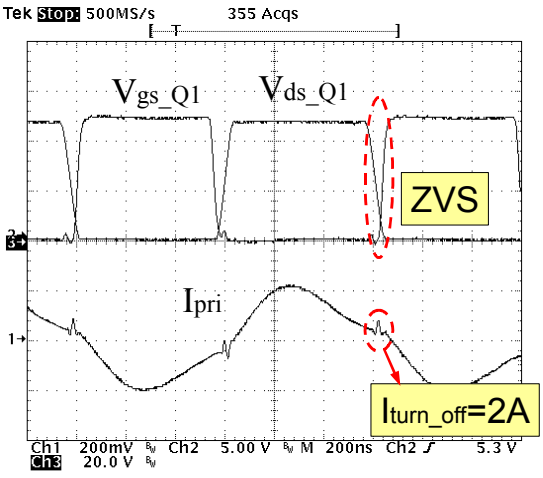


Figure 4-17. The gate signal, drain-to-source voltage of the primary switch and the primary transformer current.

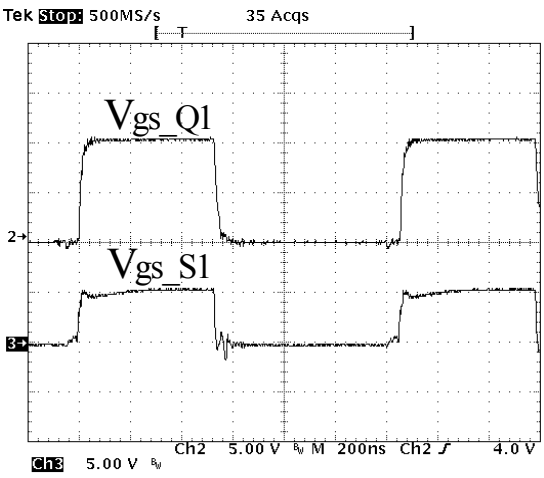


Figure 4-18. Top: gate signal for the primary switch; Bottom: gate signal for the SR.

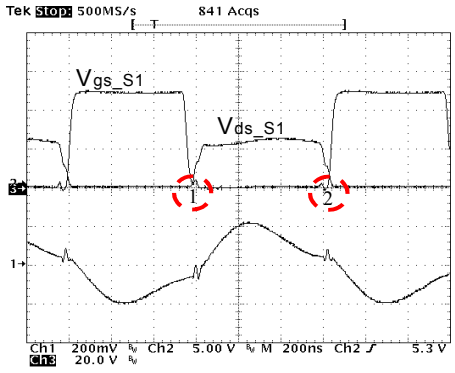


Figure 4-19. The gate signal of the primary switch, the drain-to-source voltage across the SR and the primary current.

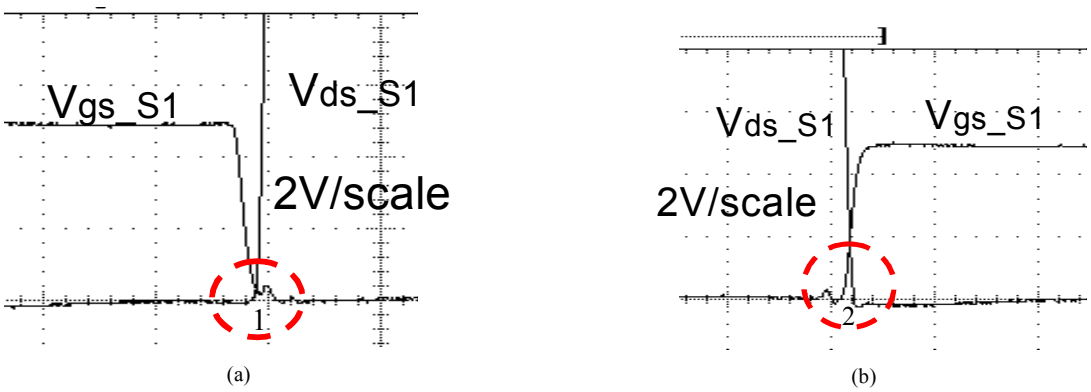


Figure 4-20. Close-up of Figure 4-19: (a) bottom switch turn-off edge and (b) bottom switch turn-on edge.

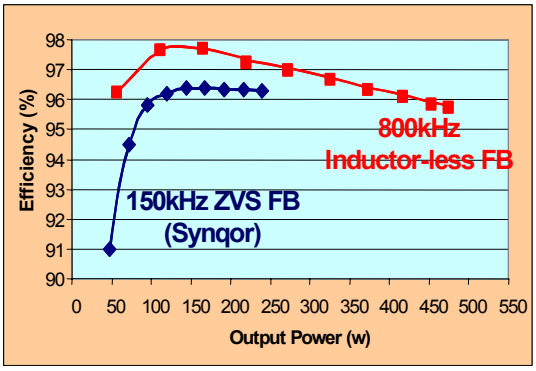


Figure 4-21. The efficiency comparison between the inductor-less FB and conventional ZVS FB.

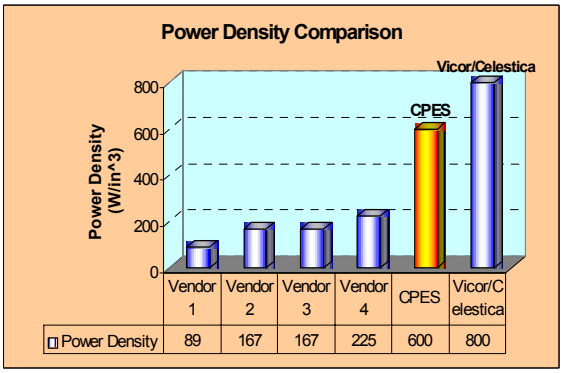


Figure 4-22. The power density comparison with industry products.

The efficiency and the power density comparisons are shown in Figure 4-21 and Figure 4-22. The proposed bus converter can reach 96% efficiency at 500 W. Normally, the quarter-brick can sustain losses of around 13 W without necessitating a heat-sink or airflow. At this

condition, the output power of the proposed bus converter is around 350 W, and the power density is around 600 W/in^3, which is much higher than most today's industry products. Although it is still lower than Vicor's product, it has the potential to be improved. Please note that only 2/3 of the quarter-brick is used (refer to Figure 4-16). More SRs can fit into the board to reduce the conduction loss and improve the power density. Meanwhile, integration can also improve the power density, which is adopted by Vicor.

4.3.2. Intermediate Bus Voltage

As we know, for the first stage, the efficiency increases as the intermediate bus voltage increases, but the efficiency of the second stage decreases. So, there must be an optimal bus voltage, at which the system efficiency reaches its highest point.

Actually, the optimal bus voltage is very sensitive to the second stage devices and switching frequency. For different devices and switching frequency, the optimal bus voltage is different. The design procedure is described as below.

The given specifications are output voltage V_o, maximum output current I_{omax}, channel number N_{ch}, minimum system efficiency requirement η_{sys_min}, efficiency of the first stage η_{first}, given devices and output capacitors. The constraint is that the system efficiency should be greater than the minimum system efficiency requirement. The design variables are the intermediate bus voltage, the switching frequency, the output inductance and the crossover frequency.

The first step is to plot the first-stage efficiency. Based on the first-stage topology proposed in the previous section, the efficiency vs. bus voltage curve can be easily obtained from both experiments and the mathematical model.

The second step is to plot several curves of the second-stage efficiency vs. the bus voltage at the condition of different switching frequencies. These curves are based on the loss estimation in Appendix 1, or obtained from experimental results.

The final step is to combine the first stage and the second stage together to plot a curve showing the system efficiency vs. the bus voltage. From this curve, we can choose the best

intermediate bus voltage to achieve the highest switching frequency while maintaining the minimum efficiency requirement.

Similar to the analysis results of the 12-V two-stage VR, as the switching frequency of the second stage increases, the optimal bus voltage drops. It will be proved in the following section.

4.4. Experimental Verification for IBA System Performance

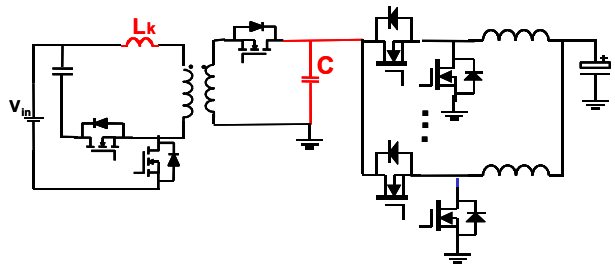
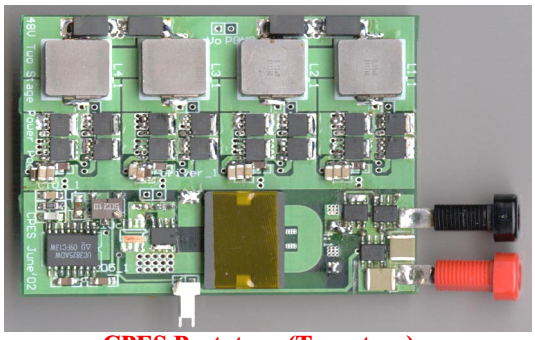


Figure 4-23. The schematics of a two-stage DC-DC converter.



CPES Prototype (Two-stage)

Figure 4-24. The prototype adopting two-stage structure.

As an example, a 48-V two-stage DC-DC converter is built to verify the advantages of IBA for server application. The schematic of a two-stage system is shown in Figure 4-23. The first stage adopts an inductor-less active-clamped forward, which employs the same concepts and is analyzed in Appendix 2. The second stage is a four-phase interleaving buck. Figure 4-24 shows a picture of the two-stage prototype. The experiment set-up is as follows: The first stage: V_{in}=48V, f_s=300kHz. Primary switch: Vishay 4488 ($R_{ds(on)}$=50 mΩ, Q_{gd}=8.5nC). Secondary switch: Hitachi HAT2099 ($R_{ds(on)}$=2.9mΩ @ V_{gs}=10V). Transformer is EI22 core from Philips. The second stage: V_o=1.2V, I_o=100A, f_s=1MHz. Top switch: HAT2168*2/phase (Q_{gd}=2.4nC, $R_{ds(on)}$=8.8mΩ @ V_{gs}=4.5V). Bottom switch: HAT2165*2/phase ($R_{ds(on)}$=3.4mΩ @ V_{gs}=4.5V). Output inductor: Vishay IHLP-5050FD 150nH/phase, Output capacitor: 4*270uF ESRE. The PCB uses nine-layer, 2oz copper.

Figure 4-25 shows the experimental waveforms of the first stage at V_{bus}=12 V. All devices work in ZVZCS conditions. Figure 4-26 shows its efficiency vs. output power. It can be seen that it reaches 96.5% efficiency at full load. Simply changing the turns-ratio of the transformer, different intermediate bus voltages can be achieved.

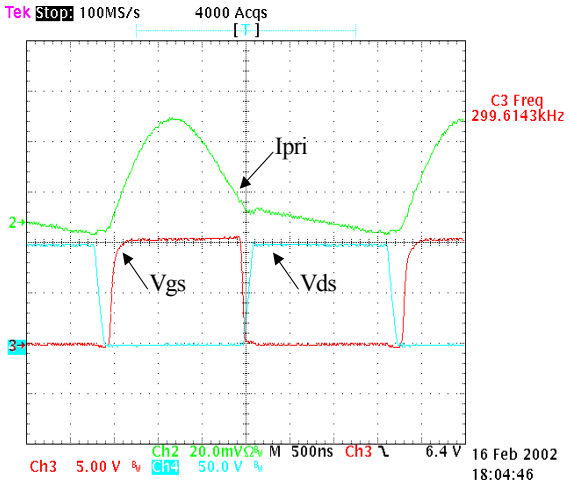


Figure 4-25. The experimental waveforms of the proposed inductor-less active-clamped forward.

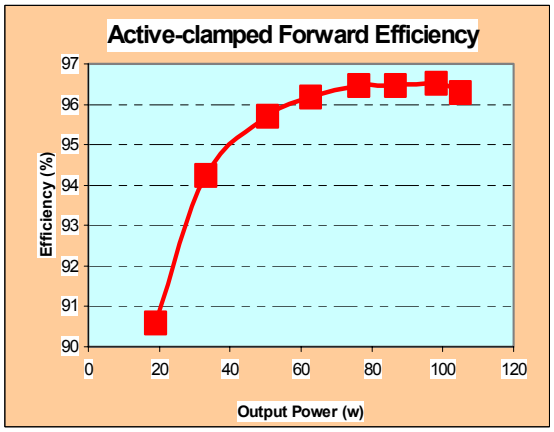


Figure 4-26. Active-clamped forward efficiency vs. output power.

Following the optimal bus voltage design guideline, the optimal bus voltage is illustrated as follows. Figure 4-27 shows the experimental results of the first-stage efficiency vs. bus voltage. At 5 V of output voltage and 20 A of output current, the first-stage can still achieve around 94% efficiency. Figure 4-28 shows the second-stage efficiency vs. the intermediate bus voltage at different switching frequencies with the critical inductance design. Figure 4-29 shows the system efficiency vs. the intermediate bus voltage at different switching frequencies. It is shown that the optimal intermediate bus voltage decreases as the second-stage switching frequency increases. At 1 MHz, the optimal bus voltage is around 6 V. So, in the prototype, we choose 6 V of bus voltage. The system efficiency is expected to reach 84% at full load.

Based on Figure 4-29, it can be seen that 8~9 V bus voltage is suitable for 600~800kHz switching frequency. That is the reason the industry recently showed a trend to lower down the bus voltage from 12V to 8~9V. As the switching frequency further increases, the optimal bus voltage moves toward even lower value.

Figure 4-30 shows the experimental system efficiency in which the second-stage frequency f_s=1 MHz and intermediate bus voltage V_{bus}=6 V. It can be seen that at full load, it can reach 83% efficiency. Potentially, since the 6V bus voltage is used, the low-voltage-rating devices can be used, which could further improve the two-stage performance.

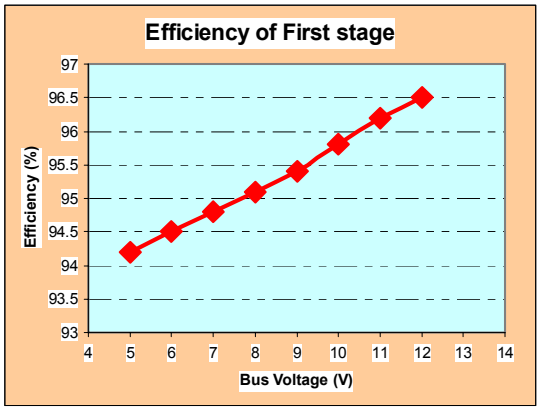


Figure 4-27. The 1st stage efficiency vs. bus voltage.

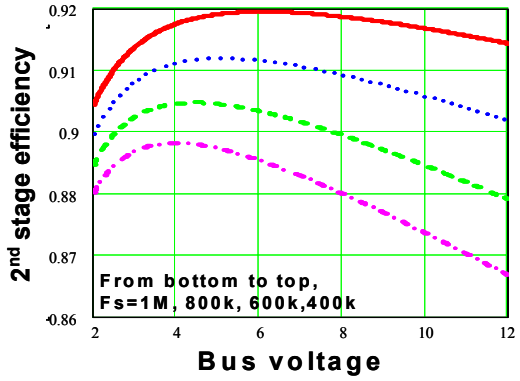


Figure 4-28. The 2nd stage efficiency vs. bus voltage.

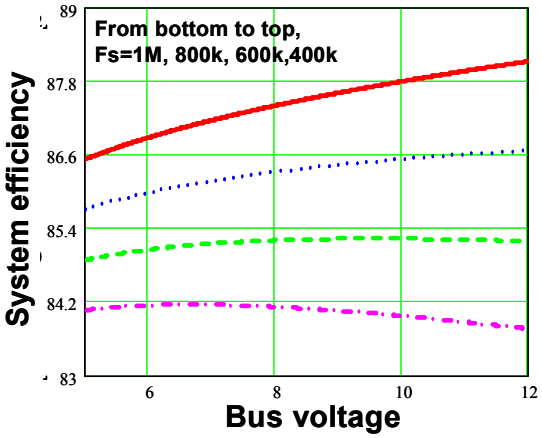


Figure 4-29. System efficiency vs. bus voltage

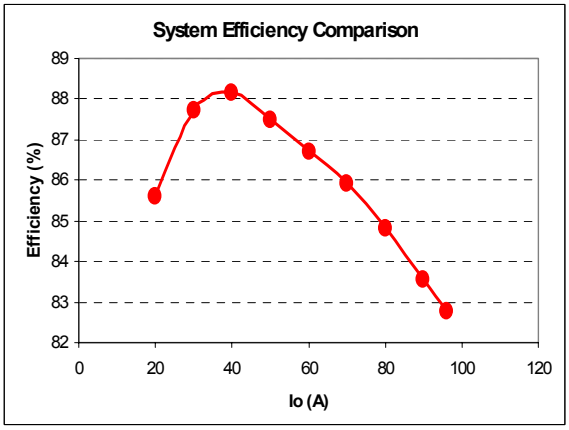


Figure 4-30. Experimental efficiency of 48V two-stage DC-DC converter.

Table 4-2. **The Comparison between Single-stage and Two-stage**

	Switching frequency	Transformer	Inductor	Capacitor
Industry Practice	250kHz	Philips EI32	2 Philips EI22 (customized)	15*1mF Tantalum
CPES Prototype	1st stage: 300kHz, 2nd stage: 1MHz	Philips EI22	4 Vishay IHLP-5050FD 150nH	4*270uF ESRE
Volume Reduction		54%	90%	75%

Thanks to the high-frequency second-stage, the passive components are dramatically reduced. Table 4-2 lists the comparison between the CPES prototype and one industry practice, which is the single-stage approach. Because of the reduction of passive components, the power density can be increased by around 150%. It is also apparent that since the expensive output capacitors are significantly reduced, the two-stage approach is less costly than the single-stage approach.

Again, the two-stage approach shows its advantages in the communication and computer power applications. After CPES proposed two-stage structure for server application in 2001, Intel adopted this solution and successfully applied it in its Itanium server.

It can be expected that the two-stage approach or IBA will overwhelm the traditional single stage DPS as the IC product further develops at the server applications.

4.5. Conclusion

In this chapter, IBA is successfully applied to 48V DPS. To increase the power density of the first stage, a family of inductor-less bus converters is proposed. A full-bridge converter is used as an example to explain the operation principle for the isolated bus converter and a proposed resonant Buck converter is used as an example for the non-isolated bus converters. Based on the concept of energy transfer by the leakage inductor, the bulky output inductor can be eliminated. Through careful selection of the output capacitor, ZCS turn-off can be achieved for the SRs, and the body diode loss can be eliminated. Meanwhile, the magnetizing current is used to achieve ZVS turn-on for all switches. And a self-driven structure is proposed to this family of bus converters in order to further simplify the circuit and to save drive loss.

As a result, the proposed inductor-less bus converter is able to run at high frequencies with higher power density. The experimental results of the inductor-less full bridge bus converter show that it can achieve over 95% efficiency at 500W output in a quarter-brick size. Its power density is around 3 times higher than today's industry practices.

Hardware is also built to demonstrate the resonant Buck converter. Compared with the conventional PWM Buck converter as the first stage in the previous chapter, its footprint is reduced over 33% and power density increases 2.5 times. Besides those benefits, the proposed

resonant Buck converter can achieve very low output impedance with open loop condition, which means the control circuit can be significantly simplified.

The system performance of IBA is verified by the experimental results as well. The whole system is able to achieve much higher power density by a form factor 150% compared with conventional single stage solution. Therefore, two-stage concept is also promising for 48V DPS.

Chapter 5. Investigation of New Power Delivery Architectures for Future Microprocessors

5.1. Introduction

The two-stage voltage regulator module (VRM) concept is proposed for future microprocessors of the desktop computers, with the VRM operating at switching frequencies of 4-MHz and a bandwidth of 650-KHz. Such a high bandwidth allows a dramatic reduction in the output capacitance by a factor of 80%. The capacitor number is reduced from 230 to 50 as shown in Figure 3-65.

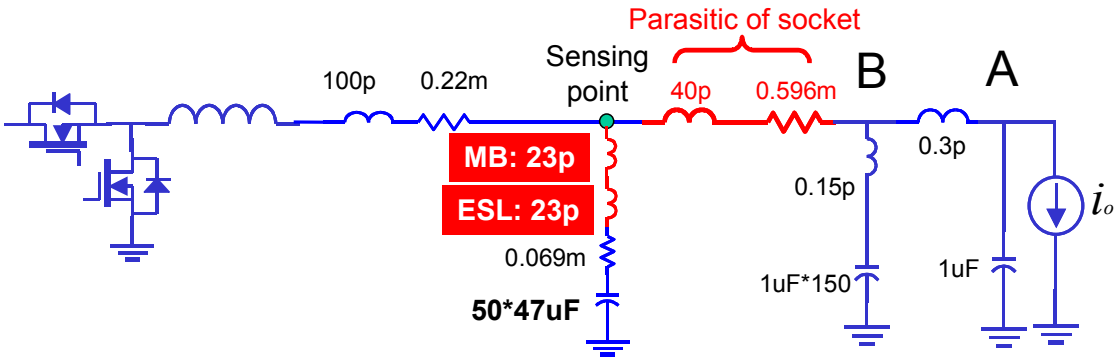


Figure 5-1. The power delivery architecture for future microprocessor with 650kHz bandwidth VR on the motherboard (MB).

Despite these benefits, the output capacitance at 4 MHz is still too large, with the required number consuming an area larger than the microprocessor itself. In the proposed operating region, the large number of parallel capacitors is not driven by the need for increased storage capability, but to reduce the ESL and parasitic inductance due to the microprocessor's high slew-rate requirements. As illustrated in Figure 3-65, the parasitics on MB and socket is still the dominant effect to limit the energy transfer. So, some new architecture is investigated in order to minimize the parasitics.

However, the output capacitance with new architecture design is still way too much. Many methods have been proposed in order to reduce the number of output capacitors, such as the

single-shot transient suppressor (SSTS) [91], interleaved QSW [92], linear regulator, transient current compensator [93], and so on. In addition, different capacitor designs have been proposed, such as the low-impedance line component (LILC) [94]. While the SSTS can improve the transient response at certain load conditions, it cannot deal with a wide range of load conditions. The linear regulator attracts a great deal of attention, however, the high power loss and associated thermal management are the biggest barriers to its implementation. The transient current compensator's switching topology also leads to similar power losses and thermal management issues. Even more problematic to both these topologies, the power loss is expected to be even larger as transient frequencies increase. While the LILC's experimental results show a 15% reduction in ESL compared to OS-CON capacitors, it still much larger than needed.

In order to further reduce the output capacitance while not placing additional burden on future microprocessors, the architecture of "VR + linear regulator (LR)" is discussed in detail. Basically, a LR is paralleled with a certain amount of packaging capacitors to deal with the high slew-rate output current. Different from the conventional linear regulator method and the transient current compensator, the proposed linear regulator deals with the rising edge and falling edge of the output current during the transient period by taking advantage of its fast transient response. As a result, the packaging capacitors don't need to deal with the high slew-rate current, and large ESL capacitors can be used. In other words, the number of output capacitors can be greatly reduced. From the energy perspective, the major part is still handled by the output capacitors, therefore, the energy processed by the LR is very small. By designing the compensator network of the control loop well, the power loss can be less than 10-W at 100-MHz transient frequency.

In this chapter, the design procedure is studied and the simulation results are also provided to verify the feasibility of the concept. In addition, this concept can also be applied to telecommunication power systems and other high di/dt applications.

After that, other technical barriers and possible solutions, which are investigated by integrated power supply (IPS) group, are described in this chapter as well.

5.2. Candidates of New Power Delivery Architectures

5.2.1. Future Microprocessor with VR on the OLGA Board

It is obvious that the current power delivery path can no longer satisfy the future requirements as pointed out in Chapter 2. The excessive interconnect parasitics between the VR and the CPU limits the transient performances. As a result, the limited control bandwidth of the VR is compromised with increasing numbers of output capacitors for energy storage.

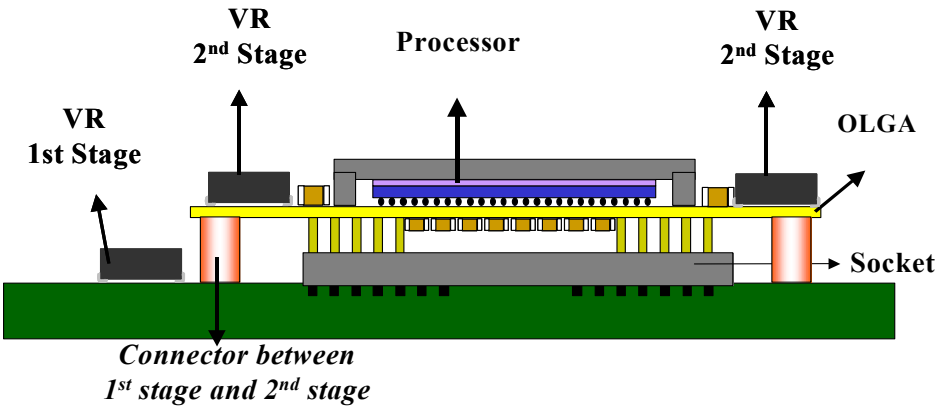


Figure 5-2. VR on the OLGA board of microprocessors.

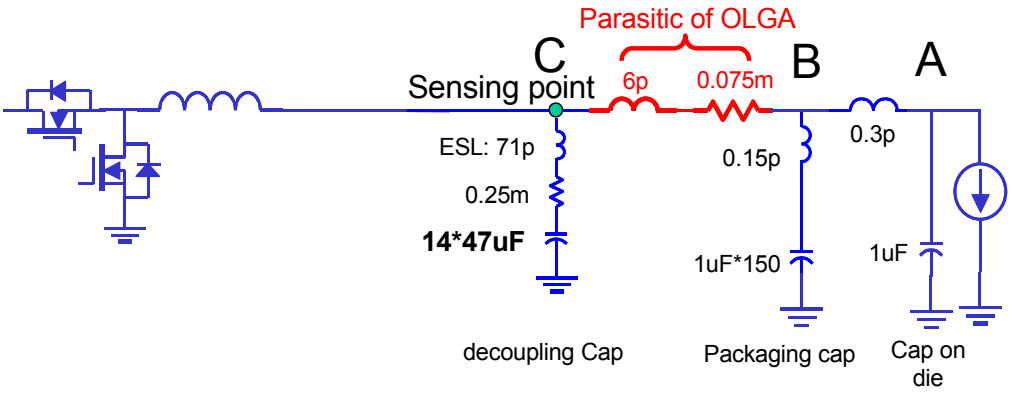


Figure 5-3. The simulation schematics of VR on the OLGA board [96].

In order to reduce the parasitic inductance on the motherboard, based on the two-stage concept, the high frequency and high power density second stage VR can be moved from MB up to the organic land grid array (OLGA) board (shown in Figure 5-2), which is a layer of the microprocessor. The corresponding simulation schematic is shown in Figure 5-3. Compared to

the power delivery path in Figure 3-65, there are two main improvements. First of all, the parasitic inductance between the output of VR (point C) and the packaging capacitor (point B) is reduced from 40pH to 6pH because the socket is eliminated. Another improvement is the reduction of the parasitic inductance in the branch of the decoupling capacitors because the capacitors can be placed much closer to the microprocessor and the current doesn't go through MB any more.

Based on this structure, the decoupling capacitance is reduced to 14*47uF at 650kHz bandwidth by the reduction of interconnection parastics. The relationship between the bandwidth of VR and the decoupling capacitance is shown as the middle curve in Figure 5-4. The top curve shows the benchmark in Figure 3-65, which is the future microprocessor based on today's power delivery architecture with 650kHz bandwidth VR design.

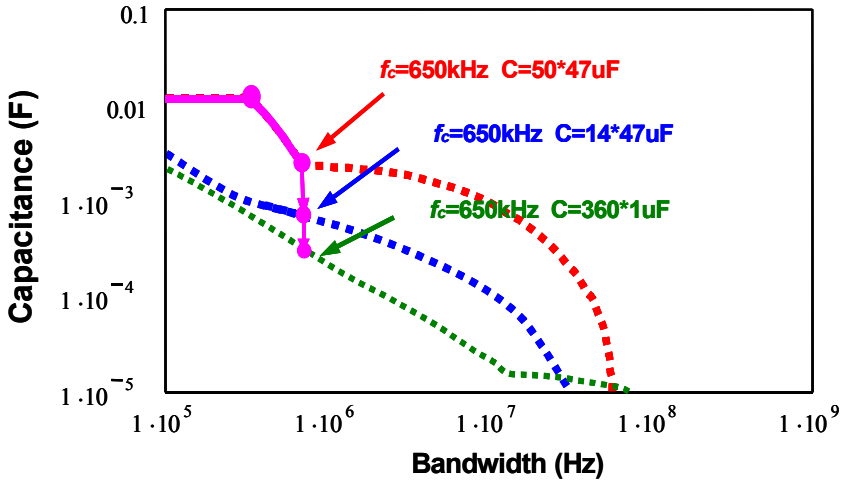


Figure 5-4. The relationship between the bandwidth of VR and the output decoupling capacitance. Top curve: future microprocessor based on today's power delivery path; Middle curve: future microprocessor with VR moved up to the OLGA board; Bottom curve: future microprocessor with VR on the OLGA board and low ESL capacitor as output capacitor.

After the VR is moved up to the OLGA board, the ESL of the capacitor becomes the dominant part that hinders the capacitance reduction. It is beneficial to choose smaller ESL capacitors. For example, the packaging capacitor has a much smaller ESL (23pH for each piece) than does a cavity capacitor (around 1nH for each piece) because the form factor is much smaller. Therefore, 1uF/23pH packaging capacitor is used as the output capacitor instead of 47uF/1nH ceramic capacitors. Assuming that all the capacitors are able to fit into the backside

area of the microprocessor, the simulation schematic is shown in Figure 5-5. The bottom curve in Figure 5-4 indicates that the capacitance will be 360*1uF if the packaging capacitors are directly used as the output capacitors. The reduction of the capacitance is because of the much smaller ESL.

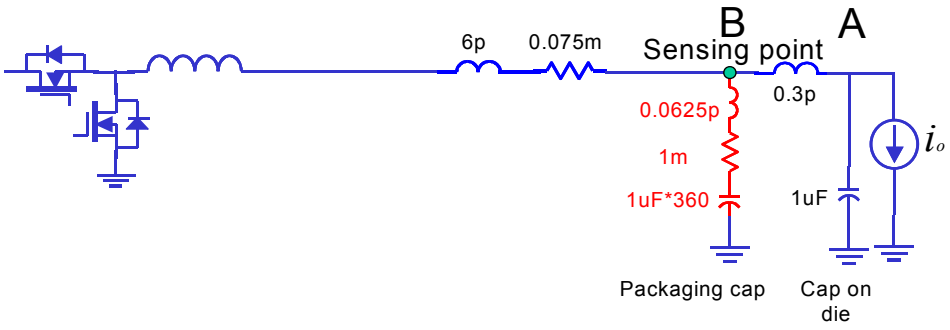


Figure 5-5. The simulation schematic of using packaging capacitor as the output capacitor [96].

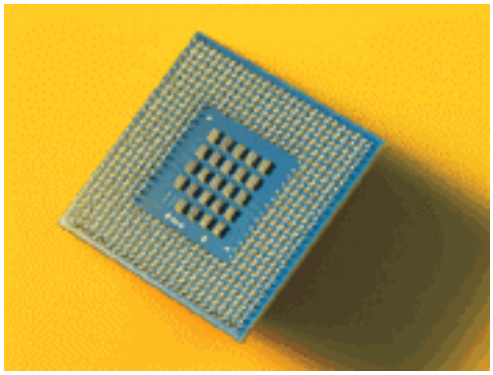


Figure 5-6. The backside of a Pentium IV microprocessor indicate that only 24 decoupling capacitors can be accommodated in such a small area.

However, the quantity is so huge that it is impossible to mount all the capacitors at the backside of the microprocessor. Usually, the packaging capacitors are located at the backside of the microprocessor, where only 24 capacitors can be accommodated (shown in Figure 5-6). It is impossible to fit 360 capacitors into such a small area.

5.2.2. Future Microprocessor with VR + LR Integration Structure

In order to further reduce the number of packaging capacitors, an alternative should be found instead of passive components and switching regulator solution.

Primarion has disclosed overlapping layers of integrated VRM modules and linear regulator (LR) to be directly mounted on the backside of the CPU [103] (shown in Figure 5-7). The advantages of this approach are that it provides local power to different areas of the processor and minimizes the impact of interconnection parasitic components. In addition, the high bandwidth LR is able to deal with high slew rate current demanded by CPU. Basically, the LR is an active filter and helps to reduce the output capacitance. The VR is only used to provide the average current.

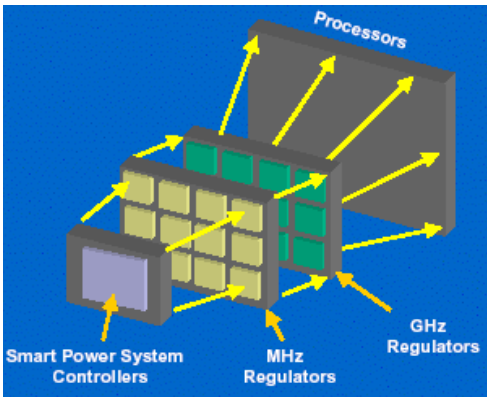


Figure 5-7. Integrating VR, LR and CPU together [97].

In 2003, CPES also proposed a fully integrated solution for powering future microprocessors. The conceptual drawing is depicted in Figure 5-8. Compared with Primarion's solution, the CPES' one integrates the ceramic capacitors and inductors. Starting in 2003, CPES organized a new team to study the fully integrated solution for the future microprocessor. The team covers a lot of research aspects, such as system and control, thermal, topology, packaging, device and materials.

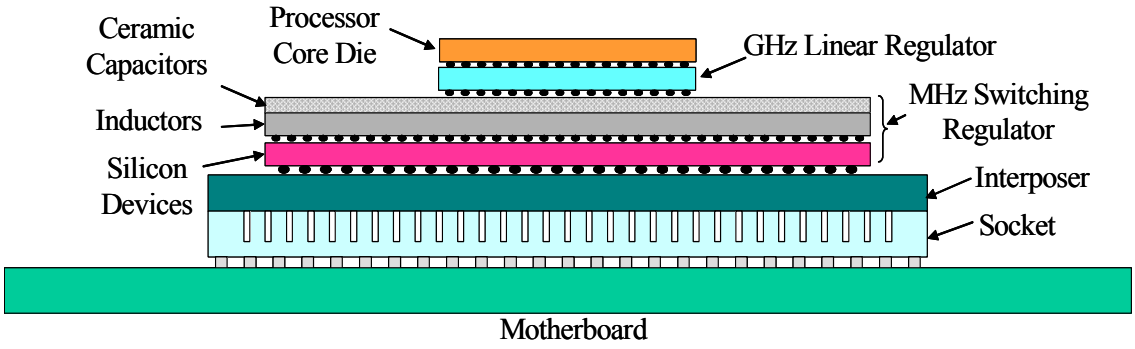


Figure 5-8. The proposed system architecture: a fully integration structure.

Basically, these two concepts are trying to use a hybrid filter, which is the combination of switching regulator (SR) and LR, instead of pure SR. However, the major issue is the large power dissipation in LR. For an instance, the future microprocessor will have the transient frequency as high as 100-MHz. As a result, the power dissipation of LR will be as high as over 100-W, which is definitely unacceptable. How to minimize the power loss while taking the advantages of LR is a big challenge. Another unsolved issue is how to match the output impedance of SR and LR. These issues are addressed in the following sections.

5.3. Proposed Hybrid Filter Concept

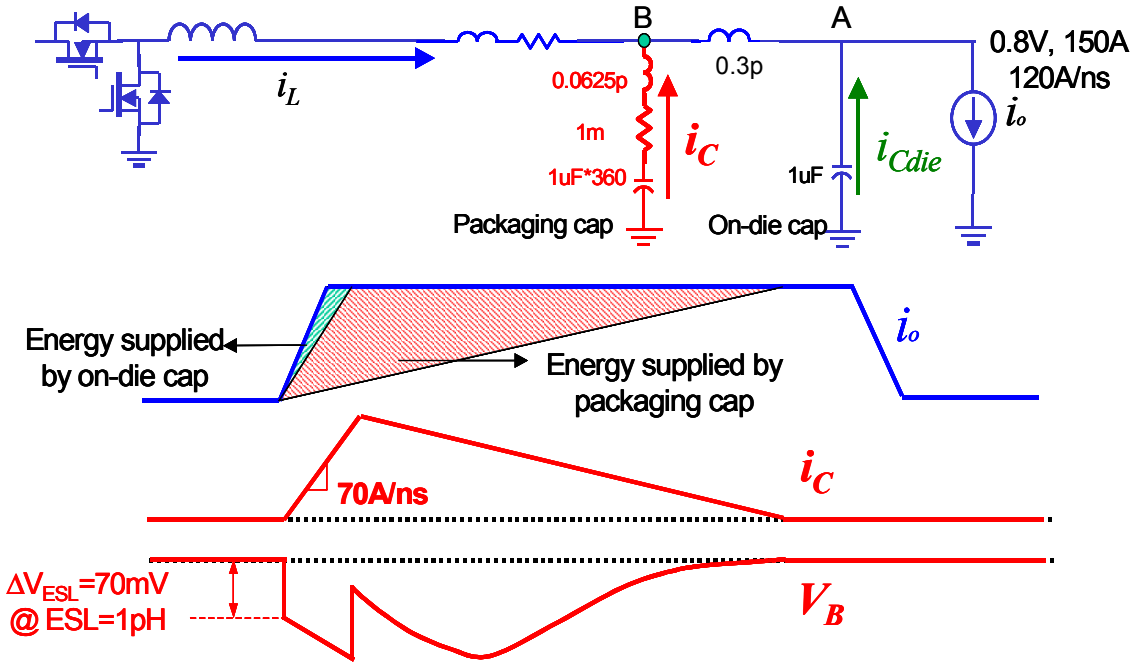


Figure 5-9. The simulation schematics of the power delivery structure in Figure 5-2.

For the 650-KHz bandwidth VRM with the new power delivery structure shown in Figure 5-2, 360*1uF packaging capacitors are needed. The reason for such a huge number of capacitors is the high di/dt requirement. As shown in Figure 5-9, the current slew-rate is 70A/ns, which causes 70-mV voltage spike even with capacitors having 1-pH ESL. In order to make the ESL effect invisible (less than 1/20 of ΔV_o), more capacitors have to be paralleled. For example, future microprocessor specifies 100-mV voltage window during transient. The packaging capacitor's specification is 1uF/23pH for each piece. In order to minimize the voltage spike

caused by ESL down to 5-mV, the total ESL should be less than 0.071-pH. Leaving a 10% margin in the design, the number of packaging capacitor is 360.

From the energy storage perspective, the capacitance is more than enough to guarantee that the voltage spike meets the 100mV requirement. We emphasize that the ESL requirement, not capacitance, determines the number of capacitors needed. Obviously, this is too many to be accommodated on the backside of a microprocessor.

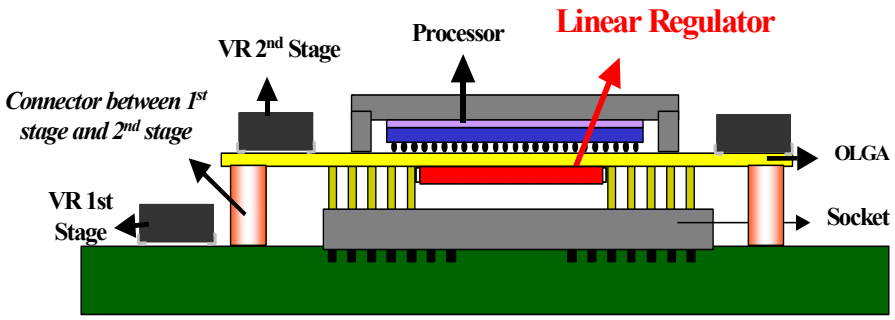


Figure 5-10. The power delivery structure with VR on the OLGA board and the linear regulator on the backside of microprocessors.

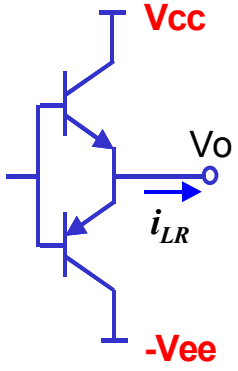


Figure 5-11. A simple linear regulator.

It is well known that a linear regulator has fast transient response capability. Using a linear regulator to replace the output capacitors is proposed before, as shown in Figure 5-10. The schematic of this power delivery structure is shown in Figure 5-12. However, the power dissipation of the linear regulator is so much that the method might not be practical. Referring to Figure 5-11 and Figure 5-12, the power loss of the linear regulator during the step-up transient can be expressed as:

$$P_{LR} = (V_{cc} - V_o) \cdot Q \cdot f_{tr} \qquad (5\text{-}1)$$

V_{cc} is the positive power supply of the linear regulator, V_o is the output voltage of 2nd stage VRM, Q is the charge supplied by the linear regulator (shown in Figure 5-12 as the shaded area), and f_{tr} is the transient frequency. For the step-down transient, the similar expression can be derived.

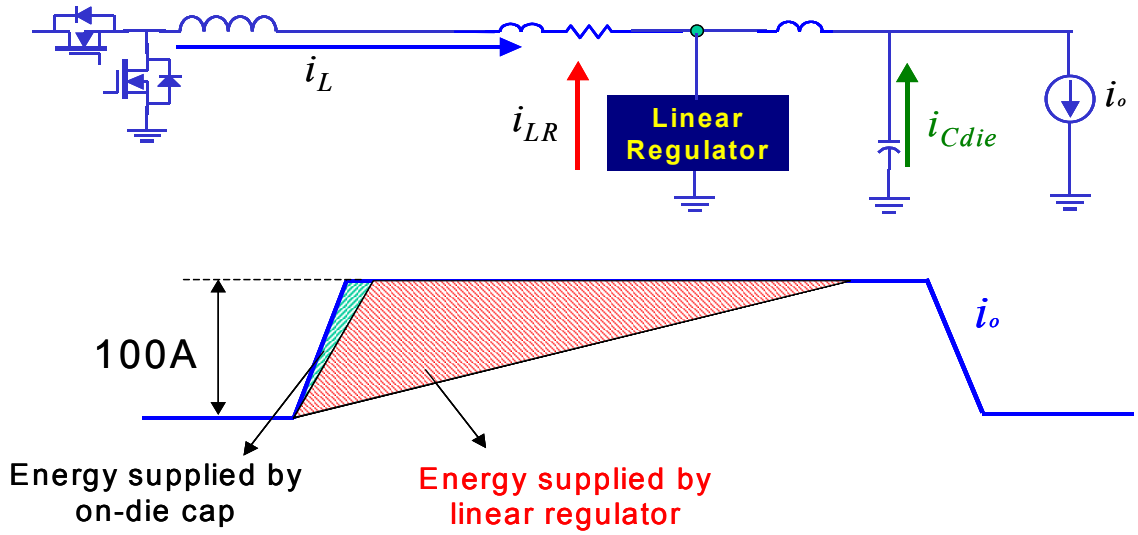


Figure 5-12. The simulation schematics of the power delivery structure in Figure 5-10.

Based on (5-1), it is clear that the power loss of linear regulator is proportional to the charge supplied by it and the difference between V_{cc} and V_o. The charge supplied by the linear regulator is related to the slew-rate of the inductor current, which is determined by the bandwidth of VR [95]. As an example, at 650-KHz bandwidth, 100-A current step, V_{cc}=4V, V_o=0.8V and f_{tr}=10MHz, the power loss is around 45-W. It is definitely unacceptable. If the transient frequency is even higher, this method cannot be used at all.

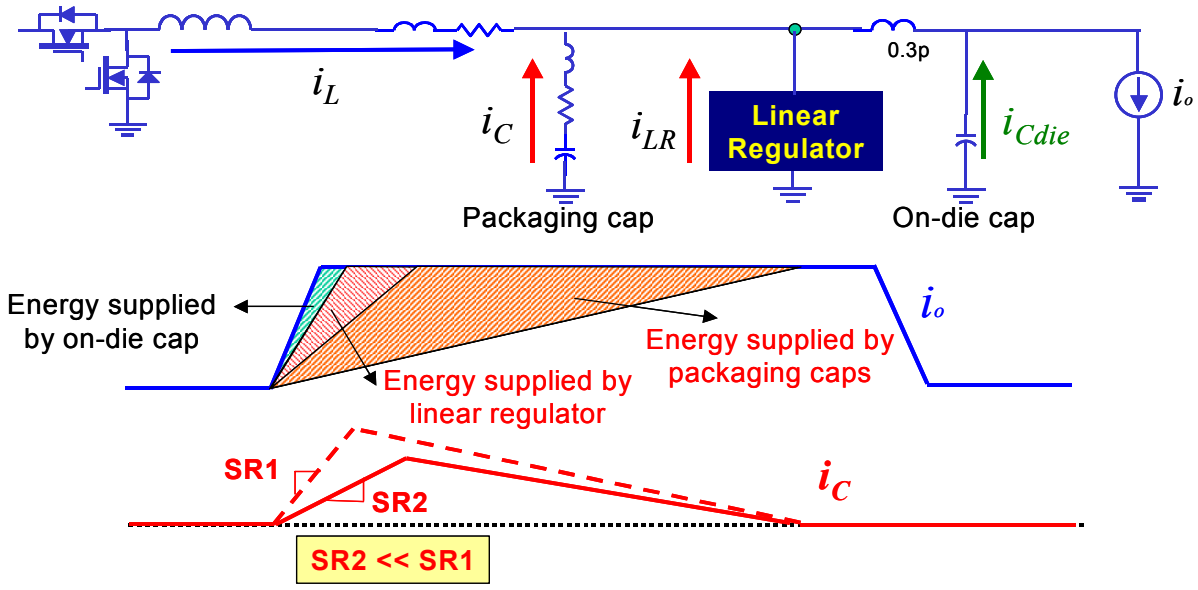


Figure 5-13. The schematic of proposed hybrid filter.

The proposed hybrid filter concept is to combine the advantages of capacitors and linear regulators (shown in Figure 5-13). The advantage of capacitor is low losses and the advantage of linear regulators is fast transient capability.

Basically, at the edge of transient, the linear regulator responds to supply the energy. Soon thereafter, output capacitors begin to take over the job of supplying the energy to the microprocessors. The capacitor current slew-rate of hybrid filter, shown as SR_2 in Figure 5-13, could be much smaller than that of the conventional capacitor solution, shown as the dashed line SR_1 in Figure 5-13. Therefore, the ESL requirement is not as stringent as in the conventional case.

On the other hand, the energy supplied by the linear regulator is not as large as the conventional linear regulator method because the majority of energy is still provided by the output capacitors. Therefore, a much smaller power loss is expected. Theoretically, the energy supplied by the linear regulator and the current waveform can be controlled by the compensator design. It will be explained in the following sections.

5.4. Design Procedure of Hybrid Filter

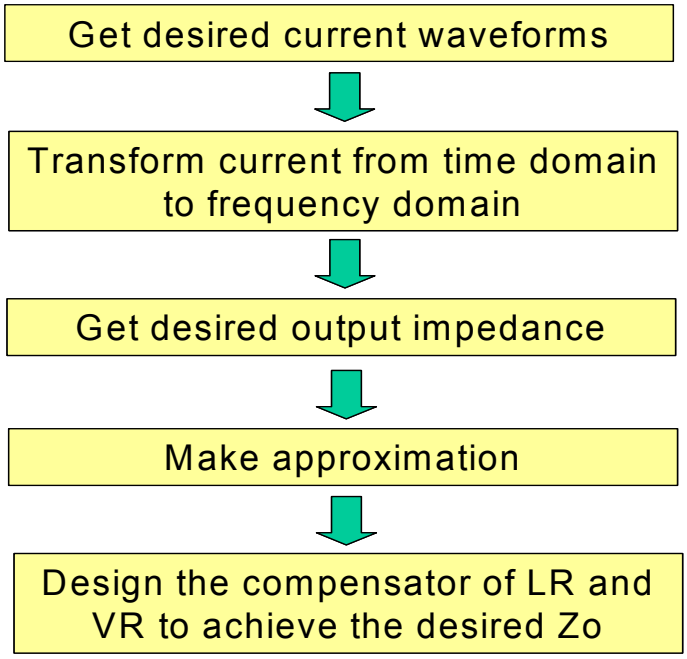


Figure 5-14. The design procedure of hybrid filter.

The design procedure is illustrated in Figure 5-14. First of all, the power loss constraint is taken into consideration, and from there, the desired current waveform can be determined. After that, we transform the current expression from time domain to frequency domain. Then, according to the output impedance specification, the output impedance of the linear regulator and switching regulator (VRM + output capacitor) can be derived. As expected, the accurate output impedance expressions are too complicated to compensate. However, we can make reasonable approximations to allow the compensators for both the linear regulator (LR) and switching regulator (SR) to be designed.

To make the procedure clear, an example is used to elaborate the design.

The generic description of the CPU current during transient is as follows: 60% step in 10 clock cycles and the remaining 40% in 40 clock cycles, for a total di/dt over 50 clock cycles. Assume the future microprocessor in 2010 operates at 10-GHz, the full load current is 150-A, and the leakage current is 20% of the full load.

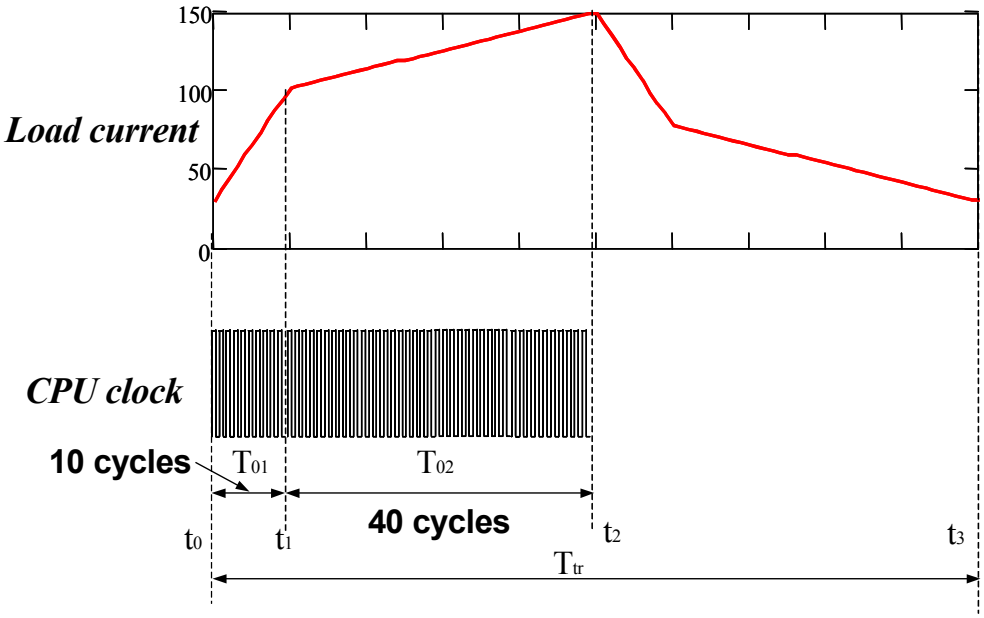


Figure 5-15. The worst case of CPU current during transient.

An extreme case is shown in Figure 5-15. The highest transient frequency is 1/100 of the clock frequency (50 clock cycles from peak-to-peak rising, 50 clock cycles from peak-to-peak falling), or 100-MHz. The waveform in one period is expressed as:

$$i_{cc}(t)=\begin{cases}(I_{step1}-I_{lk})\cdot\dfrac{t}{T_{01}}+I_{lk} & 0\le t\le T_{01}\\ I_{step1}+(I_{max}-I_{step1})\cdot\dfrac{t-T_{01}}{T_{02}} & T_{01}\le t\le(T_{01}+T_{02})\\ I_{max}-(I_{step1}-I_{lk})\cdot\dfrac{t-(T_{01}+T_{02})}{T_{01}} & (T_{01}+T_{02})\le t\le(2\cdot T_{01}+T_{02})\\ I_{max}-I_{step1}+I_{lk}-(I_{max}-I_{step1})\cdot\dfrac{t-(2\cdot T_{01}+T_{02})}{T_{02}} & (2\cdot T_{01}+T_{02})\le t\le T_{tr}\end{cases} \quad (5\text{-}2)$$

I_{lk} is the leakage current, I_{step1} is the magnitude of the first current, I_{max} is the full load current, T_{01} is the duration of the first 10 cycles, T_{02} is the duration of 40 cycles, and T_{tr} is the transient period.

Continuing with the design procedure, the desired current waveforms for the LR and VR should be determined first. The power loss of LR at 100-MHz transient frequency is specified as 10-W, which is only 2% of that of the conventional LR method. To achieve the symmetrical transient response, the positive voltage source (V_{cc}) and negative voltage source ($-V_{ee}$) of the LR follow the relationship:

$$V_{cc}-V_o=V_{ee}+V_o \quad (5\text{-}3)$$

Based on the output current waveform i_o, it is clear that the slew rate during $[t_1, t_2]$ is much smaller than during $[t_0, t_1]$. By compensator design, it is possible to make LR respond to the excitation as a symmetrical current waveform, which means LR's current has same slew rate during $[t_0, t_1]$ and $[t_1, t_1']$ except the sign, as shown in Figure 5-16.

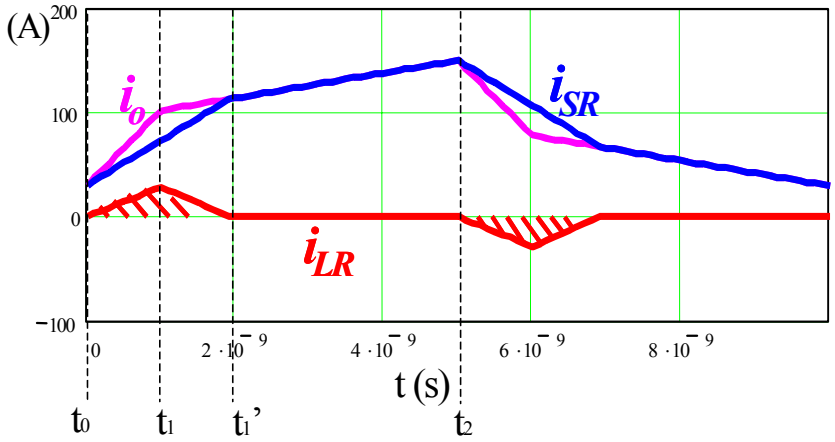


Figure 5-16. The output current i_o, and the desired current waveforms of LR and SR.

The power loss expression of LR can then be expressed as:

$$P_{LR} = 4 \cdot \left(\frac{1}{2} \cdot T_{01} \cdot I_{\max\_LR} \right) \cdot (V_{cc} - V_o) \cdot f_{tr} \tag{5-4}$$

where I_{max_LR} is the peak current value of LR. Therefore the LR's peak current value of LR can be shown as:

$$I_{\max\_LR} = \frac{P_{LR}}{2 \cdot T_{01} \cdot (V_{cc} - V_o) \cdot f_{tr}} \tag{5-5}$$

The current through LR can therefore be derived as follows:

$$i_{LR}(t) = \begin{cases} I_{\max\_LR} \cdot \dfrac{t}{T_{01}} & 0 \le t \le T_{01} \\ I_{\max\_LR} - I_{\max\_LR} \cdot \dfrac{t - T_{01}}{T_{01}} & T_{01} \le t \le 2T_{01} \\ -I_{\max\_LR} \cdot \dfrac{t - T_{tr}/2}{T_{01}} & \dfrac{T_{tr}}{2} \le t \le \left(\dfrac{T_{tr}}{2} + T_{01} \right) \\ -I_{\max\_LR} + I_{\max\_LR} \cdot \dfrac{t - \left(\frac{T_{tr}}{2} + T_{01} \right)}{T_{01}} & \left(\dfrac{T_{tr}}{2} + T_{01} \right) \le t \le \left(\dfrac{T_{tr}}{2} + 2T_{01} \right) \end{cases} \tag{5-6}$$

The current through the SR can be easily expressed as:

$$i_{SR}(t) = i_{cc}(t) - i_{LR}(t) \tag{5-7}$$

We can now show the desired current waveforms for the LR and SR in Figure 5-16. Next, we transform them from time domain to frequency domain. The purpose is to derive the desired output impedance and, finally, to design the compensators for the LR and SR.

The most common tool of the transformation is the FFT function. The components at different frequencies can be derived based on the following expressions, with $i_{LR}(t)$ as an example. First, the current in time domain is sampled according to the following rule:

$$i_{LR}(n) = i_{LR}(t) \Big|_{t = n T_s}, \tag{5-8}$$

where $T_s = \dfrac{T_{tr}}{N}$ $N = 2^m$. Therefore, the current waveform in one transient period is evenly sampled N times and the discrete data derived.

$$i_{LR\_FFT}(k) = \sum_{n=0}^{N-1} i_{LR}(n)\, e^{-j\frac{2\pi}{N}nk}, \tag{5-9}$$

where $i_{LR\_FFT}(k)$ is the k^{th} element in the spectrum of $i_{LR}(t)$ and is shown in Figure 5-17.

Following the same method, the current $i_{SR}(t)$ can also be transformed from time domain to frequency domain.

$$i_{SR}(n) = i_{SR}(t)\Big|_{t = n\,T_s}, \tag{5-10}$$

where $T_s = \frac{T_{tr}}{N}$ $N = 2^m$.

$$i_{SR\_FFT}(k) = \sum_{n=0}^{N-1} i_{SR}(n)\, e^{-j\frac{2\pi}{N}nk}, \tag{5-11}$$

where $i_{SR\_FFT}(k)$ is the k^{th} element in the spectrum of $i_{SR}(t)$ and is shown in Figure 5-18.

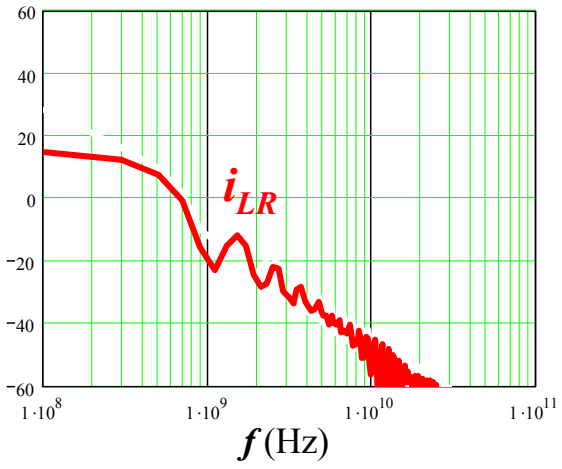


Figure 5-17. The current through LR in frequency domain.

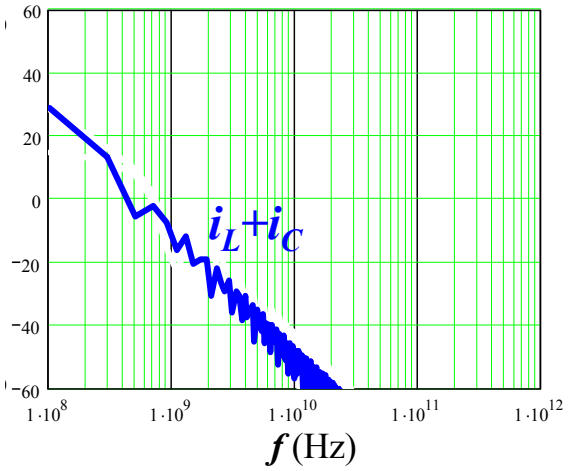


Figure 5-18. The current through SR in frequency domain.

In the next step, the output impedances of LR and SR are derived. Conceptually, the hybrid filter can be drawn as Figure 5-19. The LR and SR are paralleled together to supply the output current. The current and output impedance always satisfy the relationship (5-12) in both time domain and frequency domain. The ratio between the output impedance of the LR and SR is equal to the ration between i_{SR_FFT} and i_{LR_FFT}. Meanwhile, the paralleled output impedance

should satisfy the requirement of the microprocessor. In order to achieve AVP, the output impedance of the whole power delivery path should be designed as a pure resistor, R_{droop}, in a wide frequency range.

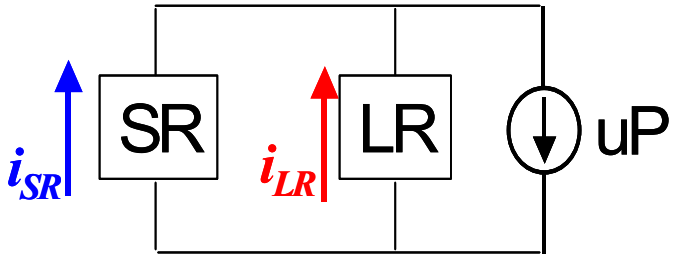


Figure 5-19. The conceptual drawing of "LR+SR" for powering the microprocessor.

$$\begin{cases} \dfrac{Z_{o\_LR}}{Z_{o\_SR}} = \dfrac{i_{SR\_FFT}}{i_{LR\_FFT}} \\ \dfrac{Z_{o\_LR} \cdot Z_{o\_SR}}{Z_{o\_SR} + Z_{o\_LR}} = R_{droop} \end{cases} \tag{5-12}$$

where Z_{o_LR} is the output impedance of the LR, Z_{o_SR} is the output impedance of the SR, and R_{droop} is specified by the microprocessor. Today's microprocessor specifies the R_{droop}=1.6mΩ. According to the CPU roadmap of Intel, R_{droop} will decrease to around 1-mΩ.

Based on (5-9), (5-11) and (5-12), the output impedance of the LR and SR are expressed as:

$$Z_{o\_LR} = \left(\frac{i_{SR\_FFT}}{i_{LR\_FFT}} + 1 \right) \cdot R_{droop} \tag{5-13}$$

$$Z_{o\_SR} = \frac{\dfrac{i_{SR\_FFT}}{i_{LR\_FFT}} + 1}{\dfrac{i_{SR\_FFT}}{i_{LR\_FFT}}} \cdot R_{droop} \tag{5-14}$$

Figure 5-20 and Figure 5-21 show the output impedance of the LR and SR, respectively. At low frequencies, Z_{o_LR} is much larger than Z_{o_SR}. Therefore, the major part of current is delivered by the SR. It can also be seen that the low frequency part of Z_{o_SR} (up to 300-MHz) is resistive. Beyond 300-MHz, the LR begins to take over the role of SR to keep the total output

impedance still resistive up to several GHz. Beyond 3-GHz, Z_{o_LR} shows its inductive behavior. It can be seen that this output impedance design require very high bandwidth op-amp.

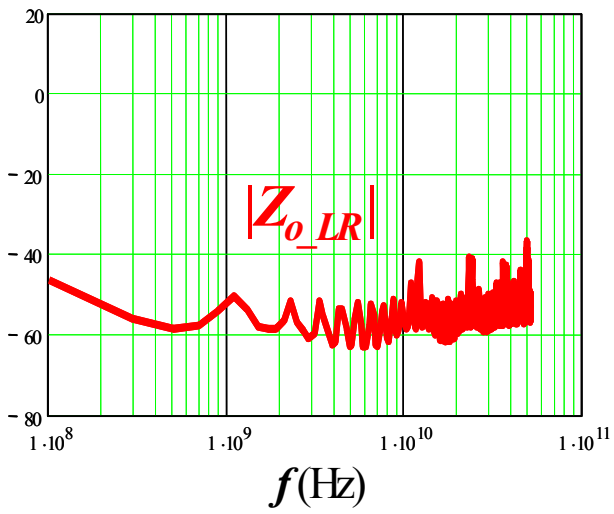


Figure 5-20. The output impedance of LR.

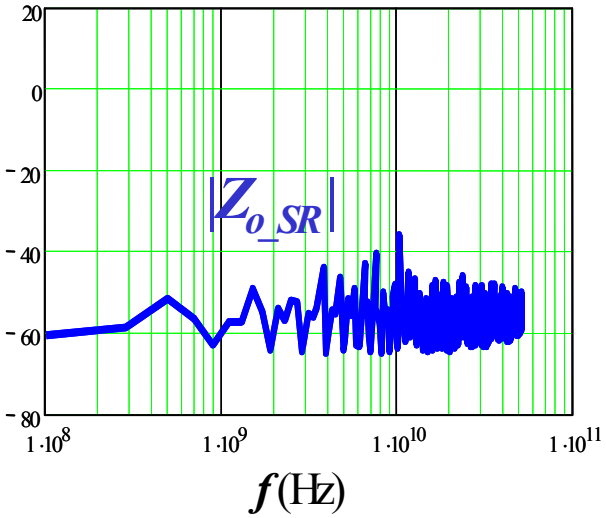


Figure 5-21. The output impedance of SR.

Obviously, it is very difficult to design a compensator to achieve the accurate output impedance value. Approximation might be necessary. Figure 5-22 and Figure 5-23 shows the approximate output impedance as the dashed lines.

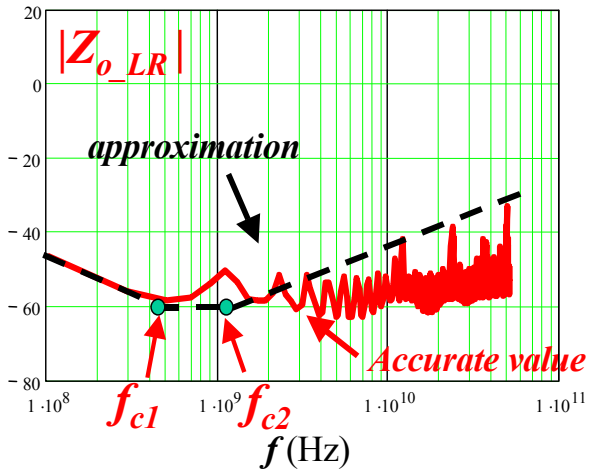


Figure 5-22. The approximated output impedance of LR.

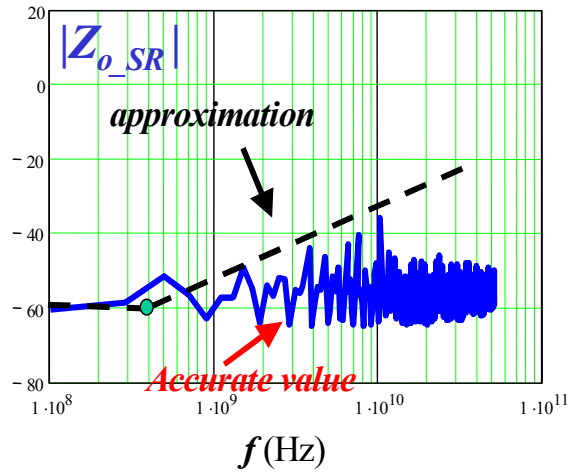


Figure 5-23. The approximated output impedance of SR.

It can be seen that there are two obvious corner-frequency points, shown as f_{c1} and f_{c2} in Figure 5-22. In the following LR's compensator design, f_{c1} and f_{c2} will determine the poles'

positions. Z_{o_SR} can also be expressed as the series combination of R_{droop} and capacitor. As the SR compensator design methodology is already well documented, we will focus on the LR's compensator design next.

Figure 5-24 shows a typical compensator and power amplifier design for a LR. The output impedance of the LR can be expressed as:

$$Z_{o\_LR} = \frac{R_b}{\beta \cdot \frac{\tilde{v}_c}{\tilde{v}_o}} \tag{5-15}$$

where β is the gain of the bipolar transistor (BJT), R_b is the base resistor and the transfer function of the compensator v_c/v_o is given by

$$\frac{\tilde{v}_c}{\tilde{v}_o} = \frac{\left(1+\frac{s}{\omega_{z1}}\right)\cdot\left(1+\frac{s}{\omega_{z2}}\right)\cdot s}{\left(1+\frac{s}{\omega_{p1}}\right)\cdot\left(1+\frac{s}{\omega_{p2}}\right)\cdot\left(1+\frac{s}{\omega_{p3}}\right)\cdot w_1} \tag{5-16}$$

where w_{p3} represents the inherent pole of the amplifier, which should be designed at least 10 times higher than $2\pi f_{c2}$.

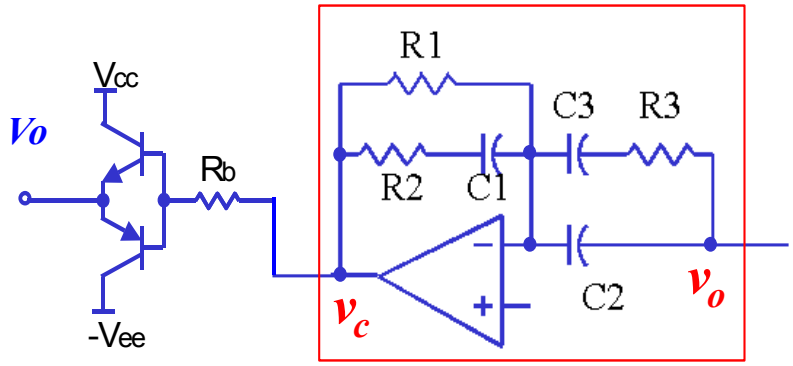


Figure 5-24. A typical design of the compensator and power amplifier of LR.

In order to achieve the desired output impedance, the zeroes and poles should be well designed. Based on Figure 5-22, (5-16) and (5-15), two poles should satisfy the following rules:

$$\omega_{p1} = 2\pi f_{c1} \qquad \omega_{p2} = 2\pi f_{c2} \tag{5-17}$$

We put ω_{z1} and ω_{z2} at least 10 times higher than $2\pi f_{c2}$. The gain w_1 can be easily derived by setting Z_{o_LR} equal to R_{droop} at f_{c1}. Based on the previous study, the open-loop bandwidth of the op-amp should be higher than 10GHz.

The relationship between the poles, zeroes, and the network parameters are expressed as:

$$\omega_{z1} = \frac{1}{R_2 C_1} \qquad \omega_{z2} = \frac{C_2 + C_3}{R_3 C_2 C_3}$$

$$\omega_{p1} = \frac{1}{R_3 C_3} \qquad \omega_{p2} = \frac{1}{C_1 (R_1 + R_2)} \tag{5-18}$$

$$\omega_1 = \frac{1}{R_1 (C_2 + C_3)}$$

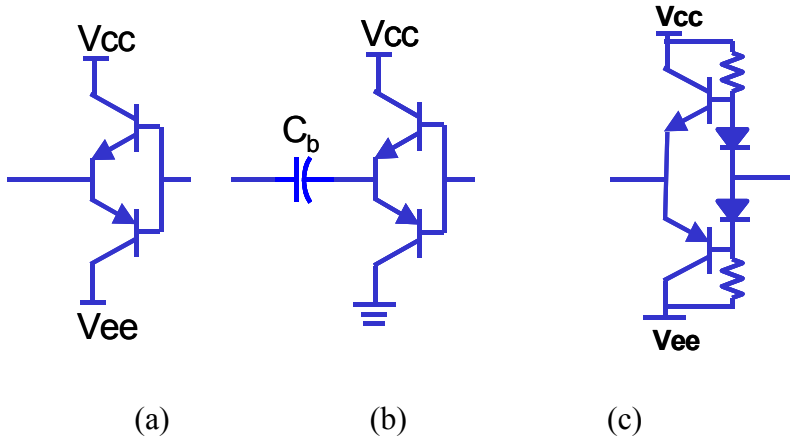


Figure 5-25. Different structures of power amplifier: (a) Output capacitor-less (OCL) structure, (b) single power supply structure, and (c) OCL with offset across base to minimize the crossover distortion.

Another important part of the LR is the power amplifier. In fact, there are many implementations for this part, and Figure 5-25 shows some of them. (b) shows the single power supply structure. With a DC block capacitor, the negative voltage V_{ee} can be eliminated to simplify the design. (c) shows a more practical design, where the diodes are connected between the base of NPN and PNP to generate an 0.7-V offset. This offset is able to minimize the distortion when the signal crossover reaches zero.

5.5. Simulation Verification

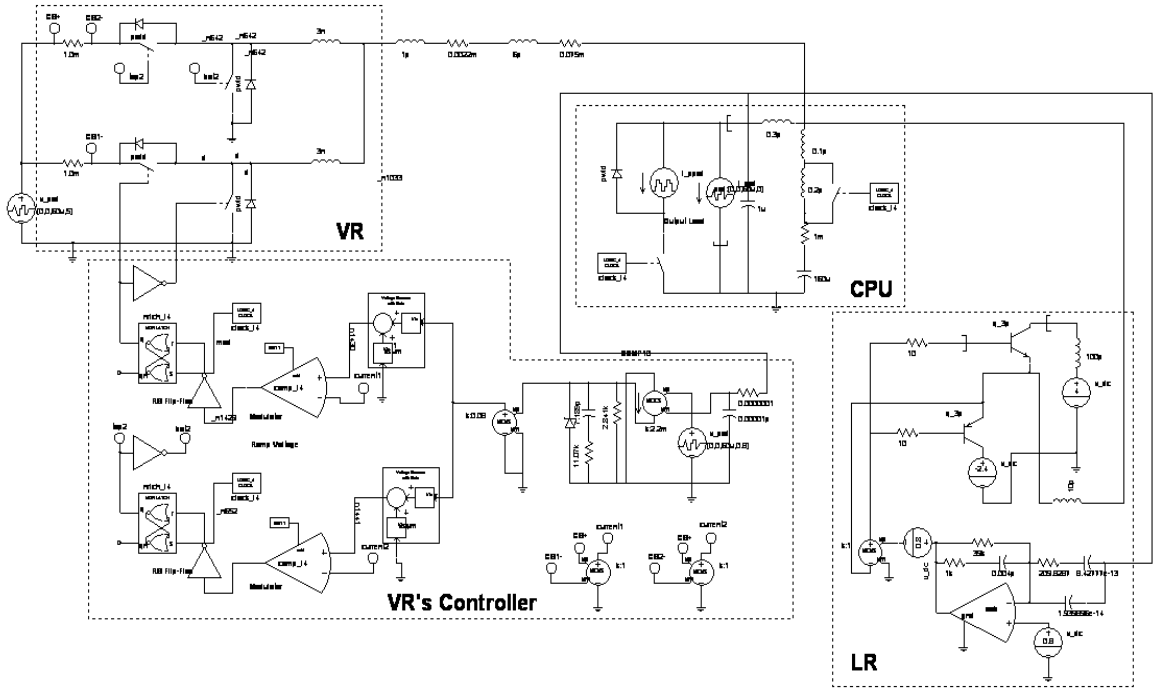


Figure 5-26. Simulation schematic of hybrid filter.

Simulations are carried out to verify the hybrid filter concept. The schematic is shown in Figure 5-26, and the specifications are as follows: Vin=5V, Vo=0.8V @ no load; the output current demanded by microprocessors is shown in Figure 5-15 (100-MHz transient period for clock frequency of 10GHz); the power loss of LR is designed for 10-W; the power supply for the LR has V_{cc}=4V and V_{ee}=2.5V; the crossover frequency of the LR is f_{c1}=900MHz, f_{c2}=2GHz; the parasitic inductance in the branch of LR is 3-pH (considering the position of LR, it is a reasonable assumption); the VR's bandwidth is designed at 650-KHz with 4-MHz switching frequency per phase; there are 32 output capacitors in parallel, for each piece, 4.7uF/23pH. Therefore, the total ESL is around 0.7-pH.

The simulation results are shown in Figure 5-27. In the middle graph, current through the SR and LR are illustrated. The comparison between the desired i_{LR} and the simulation results of i_{LR}, which is based on an approximation design, are shown in Figure 5-28. It is clear that the difference is very small. The major difference is that the approximate output impedance of the LR cannot keep the current as zero during $[t_1', t_2]$, which is defined in Figure 5-16. Actually, the

approximated design only causes around 1.2-W additional loss. Therefore, the total power loss of the LR is less than 12-W. Compared with a conventional LR solution (around 450-W at 100-MHz transient frequency), it reduces the power loss over 95%.

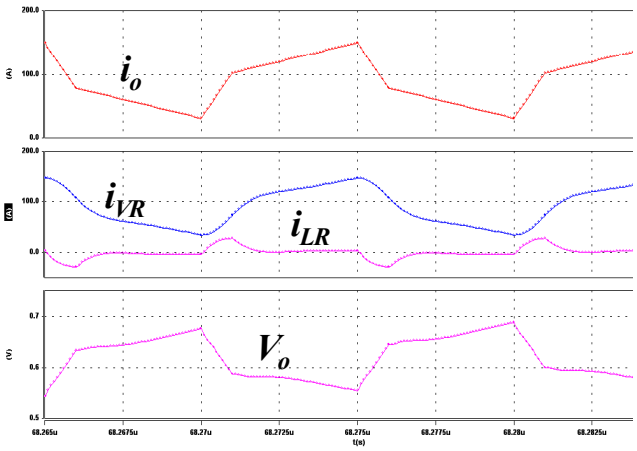


Figure 5-27. Simulation results of hybrid filter.

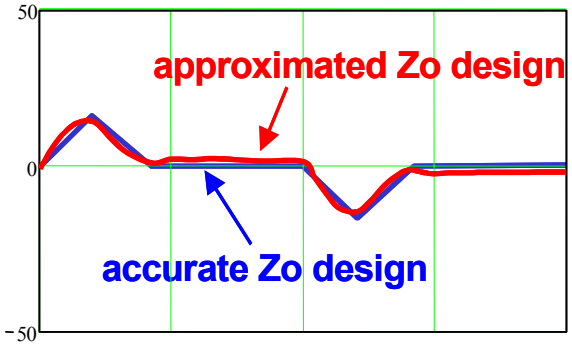


Figure 5-28. Comparison between the desired current waveform and the simulated result i_{LR}.

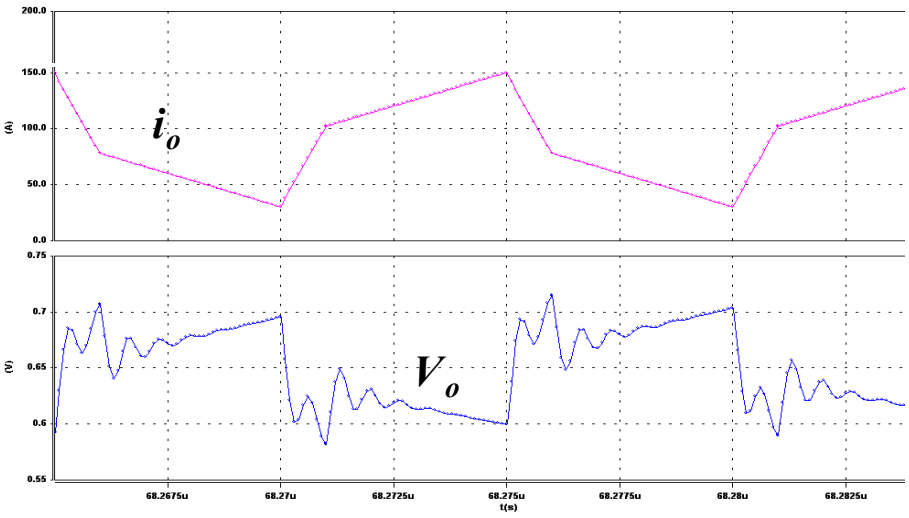


Figure 5-29. Simulation results of conventional capacitor method with 32 pieces of 4.7uF/23pH packaging capacitors.

The simulation results indicate that only 32 pieces of 4.7uF/23pH packaging capacitors are required to deal with the stringent transient requirement. Compared with the conventional capacitor solution, which needs 360 pieces 1uF or 4.7uF/23pH packaging capacitors, the proposed method is able to reduce the number of capacitors over 90%. The simulation results of

the conventional capacitor method with 32 pieces of 4.7uF/23pH packaging capacitors are shown in Figure 5-29. It is obvious that the severe ringing cannot meet the output voltage specification. In order to attenuate the voltage ringing, more capacitors have to be paralleled to reduce the ESL.

Another simulation case is to show the performance of the hybrid filter with large parasitic inductance in the branch of the LR. In the previous one, the parasitic L is 3-pH. What if the inductance increases to 20-pH? The only change is the voltage amplitude of the LR: V_{cc}=5V, V_{ee}=3.5V. Compared with the previous case, the power loss increases to around 3-W. The simulation results are shown in Figure 5-30. The waveforms are almost identical to that in Figure 5-27. The reason is that the LR operates like a current source. Its current is not as sensitive to the parasitic inductance in the power delivery path as in the conventional capacitor solution.

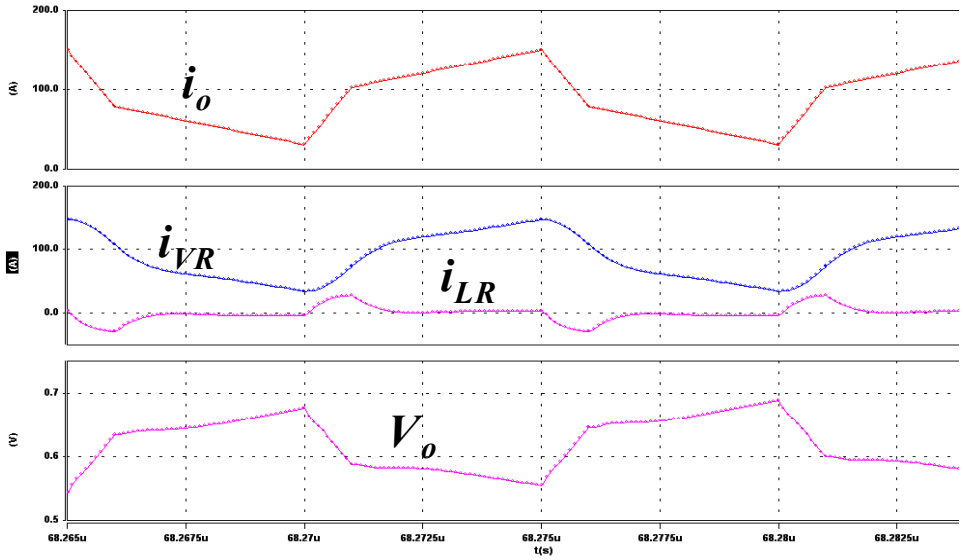


Figure 5-30. Simulation results of hybrid filter with 20-pH parasitic inductance in the branch of LR.

This characteristic of the hybrid filter highlights an intriguing benefit to the LR: it is not necessary to place LR very close to the microprocessor. This means more real estate on the backside of the microprocessor can be saved for the packaging capacitors.

Moreover, this hybrid filter can be applied to other high di/dt applications. Figure 5-31 illustrates another application where the bulk output capacitors can be replaced by the LR to improve the power density.

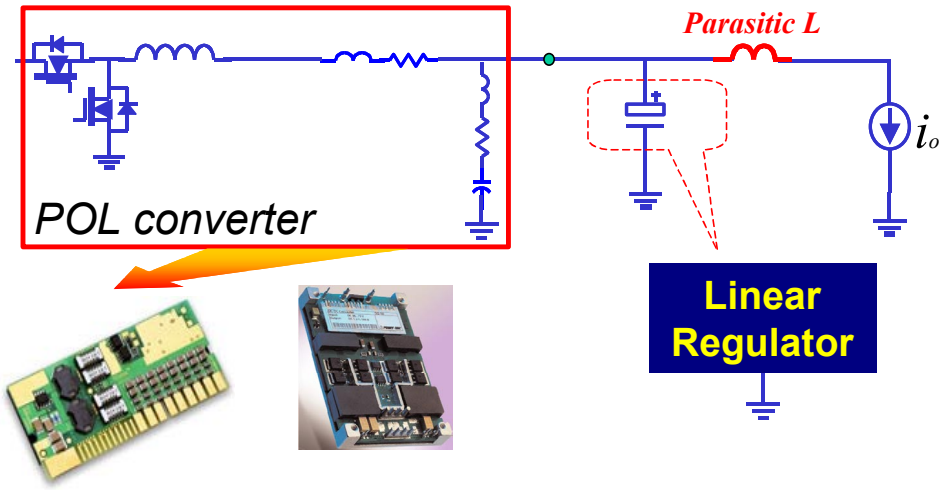


Figure 5-31. Apply hybrid filter structure to other high di/dt applications.

5.6. Experimental Verification

In order to verify the LR+VR idea, the hardware is built. Limited by the current practical components, the specification is scaled down, e.g. the current slew-rate. The switching regulator, that is VR, setup is as follows: two-phase buck converter, Vin=5V, Vo=1.2V/25A, the current slew-rate is 200A/us, fs=150kHz, L=1uH for each phase, 4 1mF/15mΩ Kemet Tantalum capacitors, ADP3167 controller, ADP3412 gate driver. The bandwidth is designed at 15kHz. The linear regulator setup is as follows: the op-amp is TI OPA2674; the power amplifier is from ZETEX 849X/951X for NPN and PNP pair; the power supply Vcc for the linear regulator is only 2.4V. Such a low voltage helps to reduce the power loss in the linear regulator.

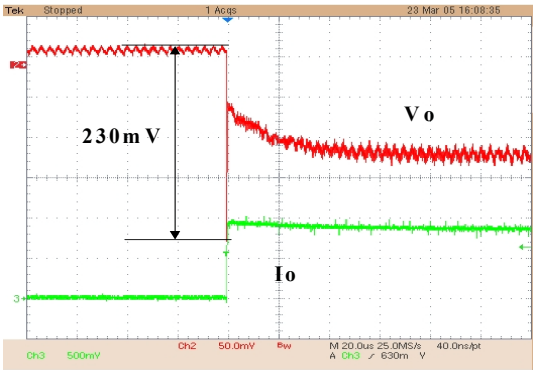


Figure 5-32. The experimental waveforms without linear regulator.

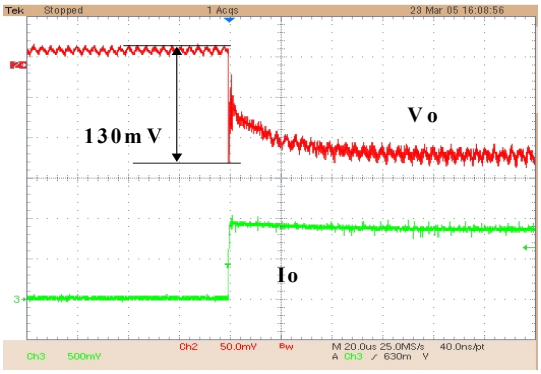


Figure 5-33. The experimental waveforms with linear regulator.

Figure 5-32 shows the output voltage waveform without the linear regulator. It is obvious that the ESL causes a significant voltage spike. Figure 5-33 shows the result with linear regulator. The voltage spike could be reduced by 100mV.

It can be seen that the linear regulator does supply energy during the transient, which in turn reduces the current through the output capacitors. Therefore, the voltage spike caused by the ESL can be reduced. It would be expected that for the future high current slew-rate microprocessors the linear regulator could show much more significant improvement in term of reducing the voltage spike caused by ESL.

5.7. Other Technical Barriers and Approaches

Other than linear regulator, more detailed discussions of the technical barriers and proposed approaches in each area are presented below.

5.7.1. System and Control

The essence of high frequency VRs is to achieve high bandwidth. For now, the bandwidth is limited by the switching frequency, e.g. fc<1/6fs. This relationship is not always true. If the bandwidth can be pushed up to 1/3 or even higher of the switching frequency, the switching frequency doesn't need to be pushed so high. This is a very interesting research direction.

In addition, in the conventional modeling work, it is assumed that the operation amplifier has an infinite gain and that there is no phase delay. Also, the control signal propagation delay and the gate drive delay are not considered. But in the practical design, the operation amplifier has its bandwidth limitation, and all the delays can account for tens of nanoseconds. When the system control bandwidth is far below the operation amplifier bandwidth and the delay is much smaller than a switching period, the theoretical analysis in an ideal situation is good enough to guide the practical design. However, for applications with very high bandwidth design, which is the trend of the VR design, the entire system can no longer be simplified as an ideal one. It is critical to accurately model the entire VR system so that we can predict the transient performance for a VR operating at multi-MHz switching frequencies. New issues and challenges will emerge.

It is also envisioned that the number of phases employed in the VR would increase considerably beyond 3-4 phases in supporting future generations of microprocessors. Therefore, the control of a large numbers of phases would be a challenge. Digital control appears to be an attractive alternative to the presently used analog control. Some start-up companies, such as Primarion and Volterra, are developing the digital controllers for these applications.

However, the sample and hold delay in the control signal loop and the limited resolution of digital control degrade the transient response of VRM. To overcome this difficulty, a mixed-signal control approach appears attractive. While the analog control is implemented where fast dynamics are required, the digital parts are used at the system level control for accurate scaling of the phase shift, current sharing, and more commutations between the VR and the microprocessor.

5.7.2. Power Semiconductor Devices and Power IC

Commercially available power semiconductor devices are not designed to operate at multi-MHz switching frequencies because of high switching losses [99][100]. This project calls for advances in the power device technology. The team should be working closely with our industry champions to investigate low-voltage-rating devices and other novel design structures such as lateral or lateral trench. First, we must develop a physics-based FEA model to analyze the loss breakdown of various device structures [101] to compare their relative advantages and disadvantages. Then, we will investigate the impact of the packaging parasitics [102][103] and explore the improvement of different gate drive schemes.

5.7.3. Magnetics design

Currently, powder iron and MgZn ferrite materials are used for the inductor design operating in the 200kHz to 1MHz range. These materials are not suitable for multi-MHz operation due to a high core loss. We are exploring different magnetic materials and winding structures such that both the core losses and winding losses can be minimized. Specially, we will look at certain matrix inductor structures with coupled inductor windings to improve both the efficiency and the dynamic response [104]~[110].

5.7.4. Packaging

The state-of-the-art technology in packaging active components includes wire-bonding, LFPAK, DirectFET, etc. [103]. The passive inductors and capacitors are used as discrete components. The current system design is based on a PCB layout with the socket connected to the microprocessor. Such packaging technology cannot meet the power delivery requirements for the future microprocessors because of the large parasitics associated with interconnection and layout [95].

CPES's developed embedded power technology has been successfully demonstrated in an IPEM form [111]. This integrated packaging concept will be extended to this application. Similar issues exist in the layout of a large array of capacitors, including the bulk capacitors, decoupling capacitors and packaging capacitors. We use Ansoft's Maxwell simulation tools to explore the capacitor construction and layout to improve the capacitance density and to reduce the ESL component.

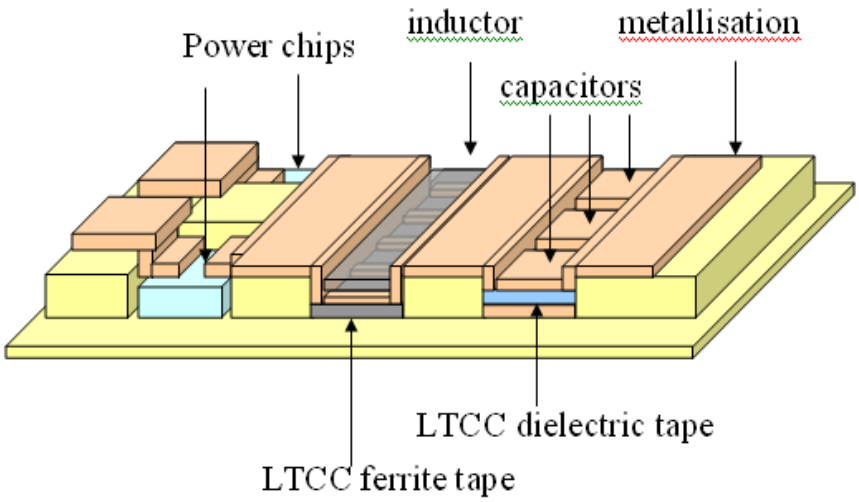


Figure 5-34. Embedded devices and components layout.

The goal of the project is to integrate active devices and passive components in the switching power supply. In the packaging part of the project, our short-term goal is to design and fabricate a low profile, high power and high frequency inductor to be integrated with the switching power supply. This inductor will be used in part of the embedded switching power supply module. Figure 5-34 shows an example of the System-In-Package layout. All these devices and components will be integrated into the substrate.

The LTCC technology is the selected technology as its gives us the prospect of making low profile passive components, which can eventually be integrated into the substrate, conserving the precious surface real estate. Besides, the magnetic properties can be controlled by the processing condition. In essence, the technology allows a greater degree of freedom in designing and processing.

5.8. Summary

Previously, the two-stage approach has been proposed to achieve high bandwidth and significantly reduce the output capacitors. However, the parasitic inductors and ESL of the packaging capacitors dramatically hinder the further capacitance reduction. In order to further reduce the capacitance, some new power delivery structures have been proposed. They are able to reduce the parasitic inductance. However, 360 pieces of packaging capacitor are still needed. It is impossible to fit so many capacitors on the backside of the microprocessors.

The hybrid filter structure is proposed in this chapter to overcome these barriers. Basically, a LR is used to supply fast transient response during the rising edge and falling edge of the output current demand. The major energy is still provided by output capacitors. The advantage of the proposed structure is to greatly reduce the power dissipation of the LR while minimizing the number of output capacitors. The design procedure is elaborated in this chapter and verified by the simulation. Compared with the conventional capacitor solution, it can reduce the amount of capacitors by over 90%. Compared with the conventional linear regulator solution, the proposed topology can also reduce the power loss over 95%. Moreover, this structure can be applied to other high di/dt applications to reduce the output capacitors and improve the power density.

Furthermore, other technical barriers and approaches are roughly discussed in this chapter too. Basically, these works are carried out by IPS group.

Chapter 6. Conclusion

It is perceived that Moore's Law will prevail at least for the next decade, with continuous advancements of processing technologies for very-large-scale integrated (VLSI) circuits. Nano technology is driving VLSI circuits in a path of greater transistor integration, faster clock frequency, and lower operation voltage. This has imposed a new challenge for delivering high-quality power to modern processors. Power management technology is critical for transferring the required high current in a highly efficient way, and accurately regulating the sub-1V voltage in very fast dynamic transient response conditions. Furthermore, the VRs are limited in a given area and the power density is important to save the precious real estate of the motherboard.

It is the purpose of this work to develop high-frequency, high-efficiency, high-power-density, fast-transient VRs to power present and future generations of processors. This dissertation has addressed the following issues.

- The power delivery architectures of the microprocessor of today and of future,
- The relationship between the bandwidth of VR and the output capacitors along the power delivery architecture,
- New VR structures for powering today and future's microprocessors those are used in desktop, laptop and server.

In order to fully understand the challenges caused by the future microprocessor, the power delivery architecture is studied first. The analysis prevails the relationship between the bandwidth of VR and the output capacitors along the power delivery architecture.

Based on the power delivery path model, the analysis results show that as long as the bandwidth can reach around 350 kHz, the bulk capacitor of the VR can be completely eliminated, which means significant savings in cost and real estate. A prototype based on the two-stage approach verifies the analysis results.

Continuously pushing the bandwidth of VR is able to reduce the decoupling capacitance in the cavity. Analysis results indicate that 650kHz bandwidth can reduce the number of the

decoupling capacitor from 230 to 50 for future microprocessor cases. Beyond 650kHz, the reduction is not obvious any more due to the parasitic components along the power delivery path.

Basically, a big picture of the future power management for the microprocessor has been drawn.

Following the vision of high bandwidth, the VRs need to operate at much higher frequency than today's practice. Unfortunately, the multiphase buck converter cannot benefit from it due to the low efficiency at high switching frequency. The extreme duty is the bottleneck. The extreme duty cycle increases VR switching loss, reverse recovery loss, and conduction loss; therefore making the 12V-input VR efficiency drop a good deal when compared with 5V-input VR efficiency.

Two-stage approach is proposed in this dissertation to solve this issue. The analysis shows that the two-stage conversion has a much better high frequency capability than the conventional single stage VRs. Based on today's commercial device, 2MHz is realized by the hardware and 350kHz bandwidth is achieved to eliminated the output bulk capacitors. Further improvement based on future devices and several proposed methods of reducing switching loss and body diode loss can push the switching frequency up to 4MHz while maintaining good efficiency. Such a high frequency makes the high bandwidth design feasible. Hence, the output capacitance can be significantly reduced to save cost and real estate.

The two-stage concept is also effective in laptop computer and 48V DPS applications. It has been experimentally proven that two-stage VR is able to achieve higher switching frequency than single stage, not only at full load condition but also at light load condition by the proposed ABVP and AFP concept based on two-stage configuration. These unique control strategies make the two-stage approach even more attractive.

As the two-stage approach is applied to 48V DPS applications, such as telecommunication system and server systems, more efficient and higher power density power supply can be achieved while greatly cutting down the cost. Therefore, after the two-stage approach is proposed, it has been widely adopted by the industry.

As a result, bus converter, which is the first stage of two-stage structure, has recently become one of the hottest products. This dissertation also proposes a family of high power

density bus converters. The basic concept is to utilize inductor-less structure and the resonant technique. Therefore, the circuit is significantly simplified. Meanwhile, ZVS, nearly ZCS and no body diode loss are achieved to greatly improve the efficiency. Compared with the industry products, its power density is around 3 times higher.

In order to further reduce the output capacitance, the power architecture needs to be modified. Based on two-stage approach, one possible solution is to move the second stage VR up to the OLGA board. Based on this structure, the parasitics can be dramatically reduced and the number of the cavity capacitor is reduced from 50 to 14. By reducing ESL of the capacitor, the output capacitance could be further reduced. After that and based on two-stage approach again, VR+LR structure is discussed, which provides the opportunity to reduce the output capacitance and integrate the power supply with CPU. The feasibility is studied in this dissertation from both power loss reduction and output capacitance reduction perspectives. Other technical barriers and possible solutions are described as well. Basically, it is long-term research, where a number of important technology fronts must be addressed, including advanced power semiconductor devices, advanced circuits and control, and advanced materials and packaging technologies. CPES has setup an Integrated Power Supply (IPS) group to tackle these challenges. Any progress would greatly impact the power electronics in the future.

As a conclusion, the two-stage approach is a promising solution for powering future processors. It is widely effective in computer and communication systems. Far beyond that, it provides a feasible platform for new architectures to power the future microprocessors.

Appendix 1. Device Analytical Loss Model

In order to investigate the performance of a circuit, an accurate loss model is usually needed before hardware is built. A lot of loss models have been proposed in the past years. Basically, the loss model can be classified into three types. One is the physics-based model. The physical parameters of the device, such as geometry, doping density and etc., are input into the device simulation software, e.g. Medici and ISE, to do the finite element analysis (FEA). The simulation results match the experimental results very well. However, it normally takes 1 to 2 days to calculate only two switching cycle of a simple Buck converter. Therefore, this method is not suitable for massive data processing.

The second level is the behavior model. This method is widely used in the loss analysis because it has good trade-off between the accuracy and the simulation time. Almost every device a vendor supplies is the device behavior model, which has some key parameters to describe the device. However, it is still not suitable for massive data processing although its simulation speed is much faster than that of the physics-based model.

The last method is the analytical model (also called mathematical model). Based on some equivalent circuits, the loss expressions are derived. Compared to the aforementioned two methods, this method is fastest and suitable for data processing. The major challenge for this model is how to improve its accuracy.

The most simple analytical loss model [A1-1] treats the switch turn-on and turn-off waveforms as piecewise linear (Figure A1-1). It doesn't consider the source inductance and the non-linear characteristics of the capacitors of the device. Therefore, the results normally don't match the experimental results very well, especially for high frequency application. Figure A1-2 shows the comparison between the analytical model and the experiment. The test condition is as follows: Vin=12 V, Vo=1.2 V, Io=12.5 A. The high side switch is HAT2168. The low side switch is HAT2165. The driver is LM2726. The difference is significantly increasing as the switching frequency increases.

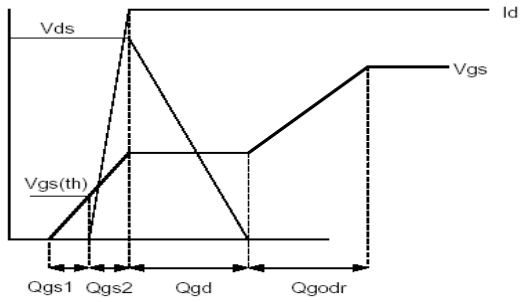


Figure A1-1. The piecewise linear approximation of the conventional analytical loss model (turn-on period).

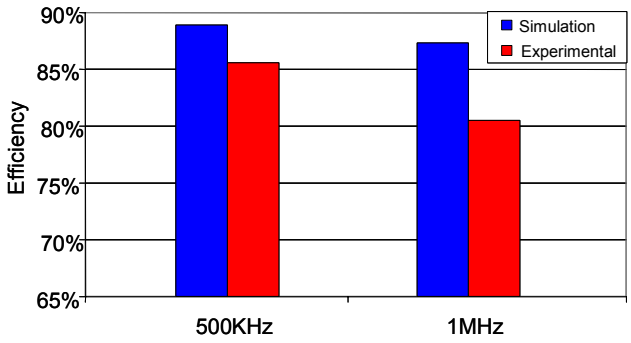


Figure A1-2. The loss comparison between the analytical model results and the experimental results.

In order to improve the accuracy of the analytical model, two important parameters should be taken into consideration: the parasitic inductors in the circuit and non-linear capacitors of the device.

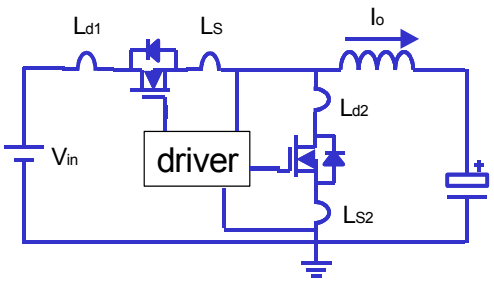


Figure A1-3. The buck converter with parasitic inductors.

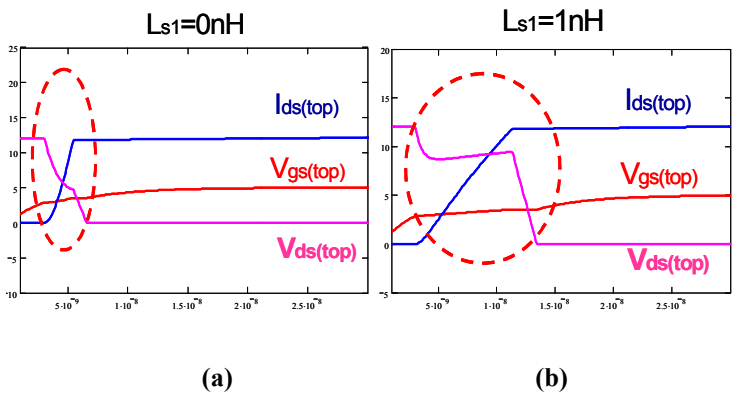


Figure A1-4. The comparison between with the source inductor (a) and without the source inductor (b).

Another important parameter is the common source inductor of the top switch, which is defined as the inductor shared by power stage and the driver loop. L_s in Figure A1-3 is an example. Reference [A1-2] partially addresses this issue. Based on this model, Figure A1-4 illustrates that after the common source inductor is considered; the commutation time dramatically increases, which significantly impacts on the switching loss. Further studies indicate that the common source inductor of the top switch has much more significant impact on

the switching loss than do other parasitic components. Therefore, it must be included in the analytical model.

However, the model in [A1-2] doesn't consider any ringing on the current through the device when the device turns on (refer to Figure A1-4), which is always observed in the PWM converters. Besides that, the non-linearity of the capacitors is not considered either.

The appendix would address these issues. The non-linear capacitors and the parasitic components in the circuit are considered. In addition, the ringing loss is discussed and a simple method is proposed to calculate it. Experimental results are provided to verify the accuracy of the proposed analytical model.

A1-1. The Model of Non-Linear Capacitance of Devices

The input parameters are C_{iss}, C_{oss} and C_{rss} @ 16-V drain-source voltage and C_{oss}, C_{rss} @ 1-V drain-source voltage. All of them can be obtained from the datasheet. Then, the gate-source capacitance at 16-V drain-source voltage is

$$C_{gs} = C_{iss\_16V} - C_{rss\_16V}. \quad \text{(A1-1)}$$

The drain-source capacitances at 16-V and 1-V are

$$C_{ds\_16V} = C_{oss\_16V} - C_{rss\_16V}, \text{ and} \quad \text{(A1-2)}$$

$$C_{ds\_1V} = C_{oss\_1V} - C_{rss\_1V}. \quad \text{(A1-3)}$$

The general drain-source capacitance can be expressed as below.

$$C_{ds} = \frac{C_{j1}}{\sqrt{1 + \frac{V_{ds}}{\Phi_1}}} \quad \text{(A1-4)}$$

Substituting (A1-2), (A1-3) into (A1-4) respectively, two equations are obtained. Based on these equations, the coefficient C_{j1} and Φ_1 can be solved.

The same method can be applied to the miller capacitor, which is gate-drain capacitor. The general gate-drain capacitance is expressed as following:

$$C_{gd} = \frac{1}{\frac{1}{C_{gd\_0V}} + \frac{V_{ds}^{x}}{C_{j2}}} \tag{A1-5}$$

where, $C_{gd\_0V} = \frac{Q_{gs(total)\_5V}}{5} - C_{gs}$

And the coefficient x and C_{j2} can be calculated based on (A1-6) and (A1-7).

$$C_{rss\_16V} = \frac{1}{\frac{1}{C_{gd\_0V}} + \frac{16^{x}}{C_{j2}}} \tag{A1-6}$$

$$C_{rss\_1V} = \frac{1}{\frac{1}{C_{gd\_0V}} + \frac{1^{x}}{C_{j2}}} \tag{A1-7}$$

Figure A1-5(a) is the non-linear capacitors' curves captured from HAT2165 datasheet and Figure A1-5(b) shows the curves gotten from the model. They match very well. Based on the capacitor model, more accurate losses and circuit behaviors can be obtained.

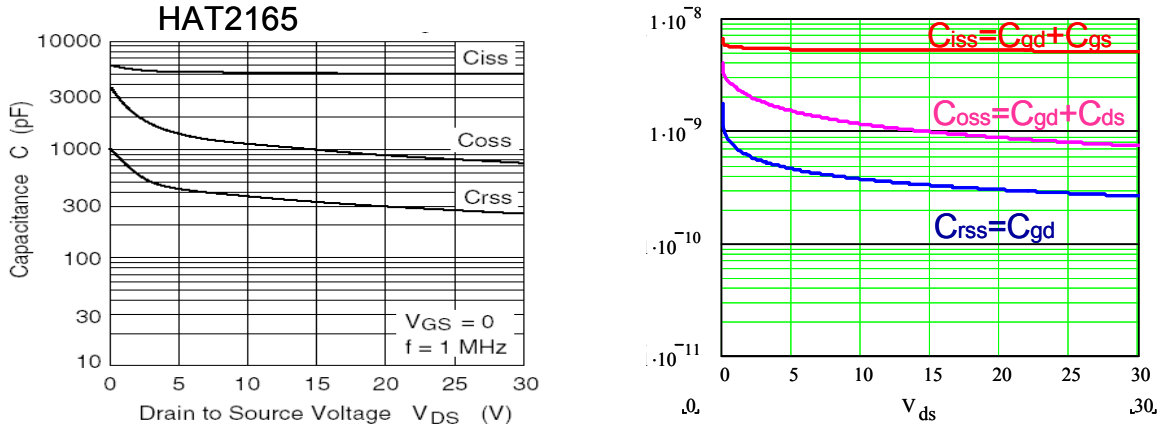


Figure A1-5. The non-linear capacitance comparison between the data from datasheet (a) and that from the proposed model (b).

A1-2. The Model of Devices' Behaviors in Circuit

After the non-linear capacitors of the devices are modeled, the next step is to analyze the impact of the parasitic inductance in the circuit, especially the common source inductance. The most difficult part of the device loss analysis is the switching loss and ringing loss compared to

the conduction loss and gate drive loss. Therefore, the purpose of majority of the appendix is to analyze the switching loss and ringing loss.

A simple synchronous Buck converter is taken as an example. In order to avoid the shoot through problem, the gate signals between the top switch and bottom switch normally have a certain dead time, during which the body diode conducts current. Therefore, it is reasonable to use a freewheeling diode instead of a MOSFET as the bottom switch for the switching loss analysis. The diode forward drop voltage is assumed 0-V for the convenience. And the inductor current is assumed as a current source I_o without ripple because the commutation time is sufficiently small that the inductor current doesn't apparently change during this period.

Based on the assumptions, the buck converter is redrawn in Figure A1-6. This equivalent circuit is valid as long as the freewheeling diode conducts current. Actually, the simplified circuit in Figure A1-6 is also suitable for other topologies, such as boost, buck-boost and etc., to analyze the device behaviors during the commutation period.

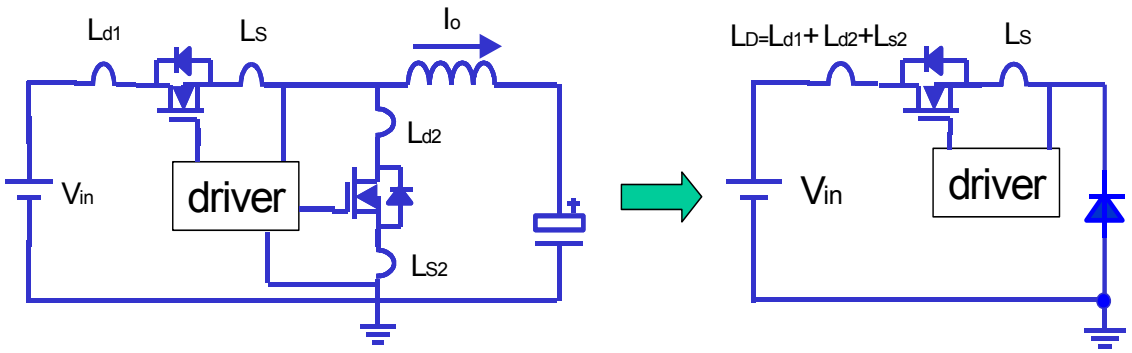


Figure A1-6. Simplified equivalent circuit for buck converter during the commutation period.

A1-2-1. The Turn-On Period

The MOSFET turn-on transition follows at least four distinct phases.

A1-2-1-1. The Delay Period

Following the assumed sharp rise in V_{gs}, the resultant gate current charges the two gate capacitances, C_{gs} and C_{gd}, which appear in parallel. The effects of L_d and L_s are neglected because the status in main power stage doesn't change in this phase. The gate voltage charges up exponentially toward drive voltage amplitude V_{dr} with a time constant τ_G given by

$$\tau_G = R_G\left(C_{gs} + C_{gd}\right) \tag{A1-8}$$

$$v_{gs\_ondelay}(t) = V_{dr}\left(1 - e^{\frac{-t}{\tau_G}}\right) \tag{A1-9}$$

This period ends when the gate-source voltage reaches the threshold voltage.

A1-2-1-2. The Main Transition Period

During the main transition period, both the drain current and the drain-source voltage vary. However, in most circuits the variation of one dominates that of the other. The simplified circuit in Figure A1-6 is redrawn in Figure A1-7 with the inherent components of the MOSFET.

Based on this equivalent circuit, the circuit equations are expressed by (A1-10), (A1-11), (A1-12) and (A1-13) by using Laplace form.

$$v_{gd}(s) = \frac{\left(V_{dr} - v_{gs}(s) - sL_s\left(i_G(s) + i_D(s)\right)\right)/R_G - sC_{gs}v_{gs}(s)}{sC_{gd}} \tag{A1-10}$$

$$v_{ds}(s) = V_{in} - sL_D i_D(s) - sL_s\left(i_D(s) + i_G(s)\right) \tag{A1-11}$$

$$i_G(s) = sC_{gd}v_{gd}(s) + sC_{gs}v_{gs}(s) \tag{A1-12}$$

$$v_{gs}(s) = v_{gd}(s) + v_{ds}(s) \tag{A1-13}$$

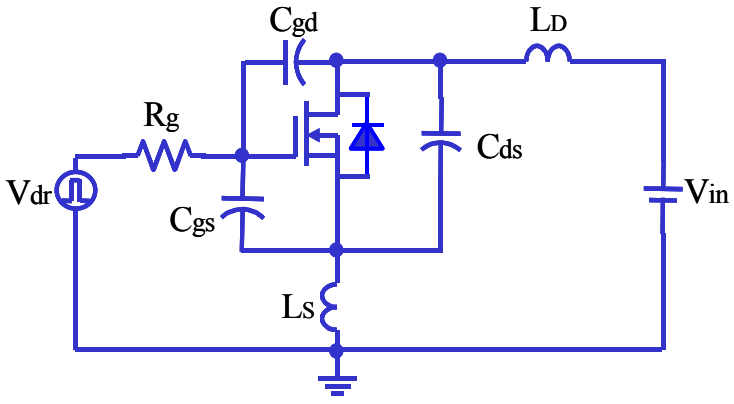


Figure A1-7. Simplified equivalent circuit for the main transition period.

Based on equations (A1-10), (A1-11), (A1-12) and (A1-13), the gate-source voltage is derived as follows:

$$v_{gs}(s) = \frac{V_{dr}}{s^2 \tau_m \tau_{G'} + s\tau_{G''} + 1}, \tag{A1-14}$$

where $\tau_m = g_{fs}(L_D + L_s)$, $\tau_{G'} = C_{gd} R_G$, $\tau_{G''} = (C_{gd} + C_{gs}) R_G + g_{fs} L_S$

Equation (A1-14) solves to give either sinusoidal or exponential solutions, depending on the relative magnitudes of $\tau_{G''}$ and $\tau_{G'}\tau_m$. The sinusoidal solutions occur when $\tau_{G''}^2 < 4\tau_{G'}\tau_m$.

$$v_{gs}(t) = V_{dr} - (V_{dr} - V_{th}) e^{\frac{-t}{\tau_a}} \left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a} \sin(\omega_a t) \right), \tag{A1-15}$$

where $\tau_a = \frac{2\tau_m \tau_{G'}}{\tau_{G''}}$, $\omega_a = \sqrt{\frac{1}{\tau_m \tau_{G'}} - \left(\frac{\tau_{G''}}{2\tau_m \tau_{G'}} \right)^2}$

The drain current and drain-source voltage are

$$\begin{aligned} i_d(t) &= g_{fs}(v_{gs}(t) - V_{th}) \\ &= g_{fs}(V_{dr} - V_{th}) \left(1 - e^{\frac{-t}{\tau_a}} \left(\cos(\omega_a t) + \frac{1}{\omega_a \tau_a} \sin(\omega_a t) \right) \right) \end{aligned} \quad \text{and} \tag{A1-16}$$

$$\begin{aligned} v_{ds}(t) &= V_{in} - (L_S + L_D) \frac{di_d(t)}{dt} \\ &= V_{in} - g_{fs}(V_{dr} - V_{th}) \omega_a (L_S + L_D) e^{\frac{-t}{\tau_a}} \left(1 + \left(\frac{1}{\omega_a \tau_a} \right)^2 \right) \sin(\omega_a t) \end{aligned} \quad . \tag{A1-17}$$

The exponential solutions occur when $\tau_{G''}^2 > 4\tau_{G'}\tau_m$.

$$v_{gs}(t) = V_{dr} - (V_{dr} - V_{th}) \frac{e^{\frac{-t}{\tau_b}} \tau_b - e^{\frac{-t}{\tau_c}} \tau_c}{\tau_b - \tau_c}, \tag{A1-18}$$

where $\tau_b = \frac{2(\tau_m \tau_{G'})^2}{\tau_{G''} - (\tau_{G''}^2 - 4\tau_m \tau_{G'})^{1/2}}$, $\tau_c = \frac{2(\tau_m \tau_{G'})^2}{\tau_{G''} + (\tau_{G''}^2 - 4\tau_m \tau_{G'})^{1/2}}$

The drain current is

$$i_d(t) = g_{fs}(V_{dr} - V_{th}) \left(1 - \frac{e^{\frac{-t}{\tau_b}} \tau_b - e^{\frac{-t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \right). \tag{A1-19}$$

The drain-source voltage is

$$v_{ds}(t) = V_{in} - g_{fs}(V_{dr} - V_{th})(L_S + L_D)\frac{e^{\frac{-t}{\tau_b}} - e^{\frac{-t}{\tau_c}}}{\tau_b - \tau_c}. \quad \text{(A1-20)}$$

Please note that the non-linearity of the device capacitances become quite important as the drain-source voltage falls below the gate voltage. Therefore taking the model of section A1-1 into the equations as above is necessary.

A1-2-1-3. The Remaining Transition Period

At the end of the main transition period, one of two situations obtains: Either the drain-source voltage reaches zero or the drain current reaches the load current. If the current reaches the load current I_o before the drain-source voltage goes to zero, this period can be ignored and the analysis directly jumps into the next phase: the current ringing period.

In the case where the current is slower than the voltage, the equivalent circuit is shown in Figure A1-8. Because the drain-source voltage has reached zero, the Miller effect no longer operates. The gate current supplies C_{gs} and C_{gd} in parallel, and the gate-source voltage resumes its exponential approach towards V_{dr}. The drain current rising time is determined by the loop inductance L_D and L_S, and the equations are listed as follows.

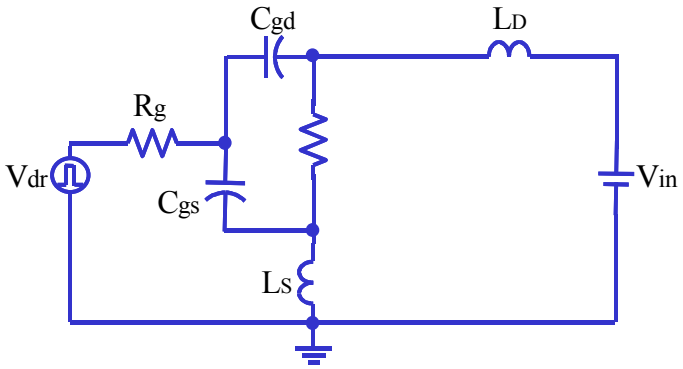


Figure A1-8. Simplified equivalent circuit for the remaining transition period.

$$v_{gs}(t) = \left(V_{dr} - V_{gs\_main} - \frac{L_S}{L_D + L_S}V_{in}\right)\left(1 - e^{\frac{-t}{\tau_{G'''}}}\right) + V_{gs\_main}, \quad \text{(A1-21)}$$

where $\tau_{G'''} = R_G(C_{gs} + C_{gd})$, and V_{gs_main} is the gate-source voltage at the end of the main transition period. Please note that at this stage, the gate-drain capacitance is much larger than that in the delay period A1-2-1.

The drain current is

$$i_d(t) = I_{d\_main} + \frac{V_{in}}{L_D + L_S} t \quad , \tag{A1-22}$$

where I_{d_main} is the drain current at the end of main transition period.

The period ends when the drain current reaches the load current I_o.

A1-2-1-4. The Current Ringing Period

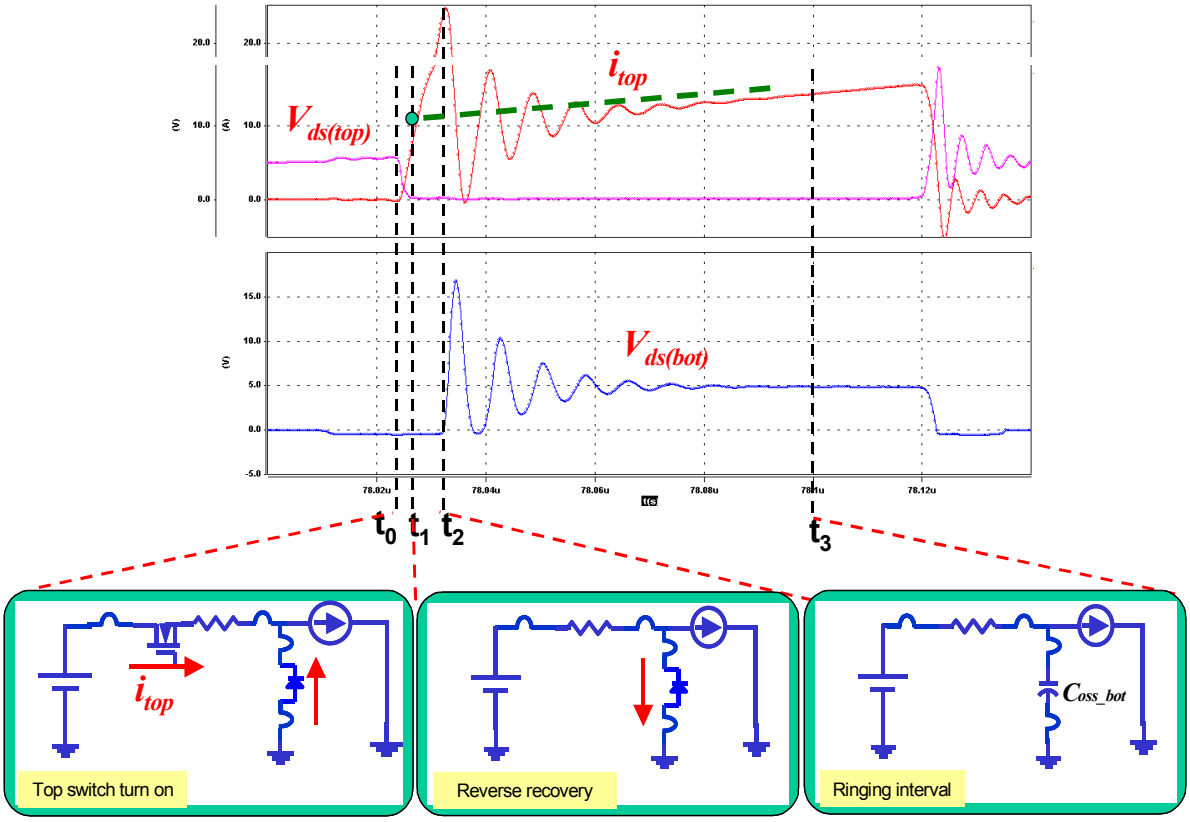


Figure A1-9. Typical waveforms of a buck converter and its simplified equivalent circuits for the different periods during turn-on.

After the drain current reaches the load current I_o, the current ringing begins. A typical top switch current and voltage waveforms are shown in Figure A1-9, which could be divided into three time frames. The first time frame [t_0, t_1] has been analyzed in A1-2-1-1, A1-2-1-2 and A1-2-1-3. The equivalent circuit is shown in Figure A1-6. Beyond t_1, the diode begins to recover but still cannot block voltage. At t_2, the drain current reaches its peak value and the diode begins to block voltage. The ringing isn't completely damped until t_3. The power loss derivation based on

the equivalent circuits during [t_1, t_2] and [t_2, t_3] could be very complicated. In this appendix, a simple method is introduced with very clear physical meaning.

To analyze the ringing loss, we assume the ringing can be well damped in one switching cycle, which is normally true for a converter with well-designed layout and switching frequency less than 3-MHz. With the development of the device integration, the parasitics are further reduced and the ringing could be completely damped in one switching cycle with even higher switching frequency.

The equivalent circuits for [t_1, t_2] and [t_2, t_3] can be unified as Figure A1-10. Please note that the current contributing the ringing is only the difference between drain current of the top switch i_{top} and I_o. The current source I_o doesn't influence the oscillation at all.

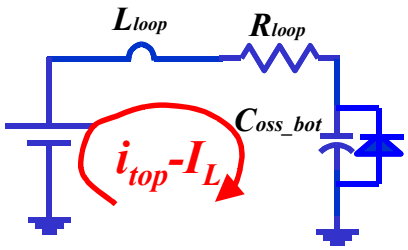


Figure A1-10. Unified equivalent circuit during [t_1, t_2] and [t_2, t_3] shown in Figure A1-9.

The L_{loop} is the sum of the parasitic inductance of the loop. The R_{loop} represents the AC and DC resistance. The AC resistance increases as the oscillation frequency increases. Usually, the oscillation of a buck converter in VR application has very high frequency, e.g. 20~40-MHz. Hence, the AC resistance could be much larger than the DCR [A1-3] and cannot be ignored in the ringing analysis. The analysis and measurement of AC resistance is beyond this discussion, which deserves more fundamental research. C_{oss_bot} represents the output capacitance of the bottom switch if the synchronous rectifier is used.

During the ringing, the energy pumped from the source is simply expressed as:

$$\begin{aligned} E_{source} &= \int_{t_1}^{t_2} V_{in}\left(i_{top}(t) - I_o\right)dt \\ &= V_{in} \cdot \int_{t_1}^{t_2} \left(i_{top}(t) - I_o\right)dt \\ &= V_{in} \cdot \left(Q_{rr} + Q_{oss\_bot}\right) \end{aligned} \tag{A1-23}$$

where Q_{rr} is the reverse recovery charge of the diode. The derivation of (A1-23) is similar to the analysis of a gate drive circuit at charging period.

At t_3, when the ringing is fully damped, the whole circuit reaches another steady state. The only energy saved is that stored in the output capacitor of the bottom switch. Therefore, the energy dissipation during the ringing period is

$$\begin{aligned} E_{ring\_turnon} &= E_{source} - \frac{1}{2} Q_{oss\_bot} V_{in} \\ &= V_{in} Q_{rr} \cdot + \frac{1}{2} Q_{oss\_bot} V_{in} \end{aligned} \tag{A1-24}$$

It is very interesting to find that the total ringing loss is not dependent on the loop resistance, but only V_{in}, Q_{rr} and Q_{oss_bot}. Therefore; the ringing loss can be easily derived without knowing the detailed waveforms of the voltage and current.

Another important thing should be pointed out is that the reverse recovery loss of the diode has been included in the ringing loss. Simply multiplying the voltage and current of the diode cannot achieve the reverse recovery loss. The majority of the reverse recovery loss is dissipated in the whole loop. A part of them causes additional turn-on loss of the top switch. A part of them dissipates in the loop resistance.

In order to get the ringing loss, Q_{oss_bot} and Q_{rr} should be known. Based on the non-linear capacitor model in A1-1, the Q_{oss_bot} can be easily achieved.

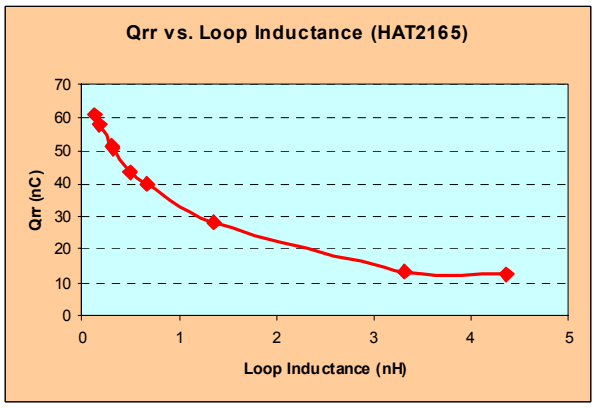


Figure A1-11. The relationship between the reverse recovery charge of the diode and the loop inductance.

For Q_{rr}, it is relatively difficult because it is related to the load current I_o and the loop inductance L_{loop}, which determines the current slew rate during the diode's reverse recovery

period. The data provided by the device vendor is normally obtained by a specific test condition. In order to achieve relatively accurate loss estimation, it is better to use a physics-based device model to simulate Q_{rr} under different conditions. For example, Figure A1-11 shows the relationship between Q_{rr} and L_{loop} of HAT2165 at I_o=12.5-A based on ISE simulation tool. As L_{loop} is less than 2-nH, Q_{rr} is very sensitive to di/dt. As L_{loop} is greater than 3-nH, Q_{rr} is pretty much constant. For today's practical layout, the loop inductance is usually larger than 3-nH. Therefore, it is a reasonable assumption that Q_{rr} is constant in the range of our interests.

Based on the ringing loss expression (A1-24) and the equations in the previous three periods of turn-on, it is possible to achieve the turn-on loss and ringing loss. Please keep in mind that the reverse recovery loss of the diode has been included in the ringing loss.

In this final phase, the gate-source voltage exponentially increases while the drain current is oscillating and drain-source voltage is sitting at the steady state. At this stage, only the $R_{ds(on)}$ is influenced by the gate-source voltage.

$$v_{gs}(t) = \left(V_{dr} - V_{gs\_remain}\right)\left(1 - e^{\frac{-t}{\tau_{G''''}}}\right) + V_{gs\_remain}, \tag{A1-25}$$

where $\tau_{G''''}$ has the same expression as $\tau_{G'''}$, but the value changes a lot due to the non-linear capacitance.

When the gate voltage reaches V_{dr}, the device is in the on-status. The current goes through the device and causes conduction loss.

A1-2-1-5. The Conduction Loss of the Top Switch

The calculation of the conduction loss is relatively simple. The expression is shown as

$$P_{cond\_top} = \left(I_o^2 + \frac{\Delta I_o^2}{12}\right) \cdot D \; R_{ds(on)\_top}, \tag{A1-26}$$

where ΔI_o is the ripple of the load current I_o, D is the duty cycle and $R_{ds(on)\_top}$ is the on resistance of the top switch. Because the $R_{ds(on)}$ is dependent on the temperature, it is better to consider the temperature effect in the loss calculation, which expressed in

$$R_{ds(on)} = R_{ds(on)\_25} + k\left(T_j - 25\right), \tag{A1-27}$$

where $R_{ds(on)\_25}$ is the on resistance at 25 degree C; k is the temperature coefficient, which can be obtained from the datasheet; and T_j is the junction temperature.

A1-2-2. The Turn-Off Period

Similar to the turn-on period, the MOSFET turn-off transition can also be divided into four distinct phases.

A1-2-2-1. The Delay Period

During the first phase of turn-off, the equivalent circuit is shown in Figure A1-12. The gate-source voltage starts to fall, and discharge the device capacitances C_{gs} and C_{gd}. The drain current and drain-source voltage don't change at this stage. The gate-source voltage is expressed as

$$v_{gs}(t) = V_{dr} e^{\frac{-t}{\tau_{G\cdots}}}. \quad \text{(A1-28)}$$

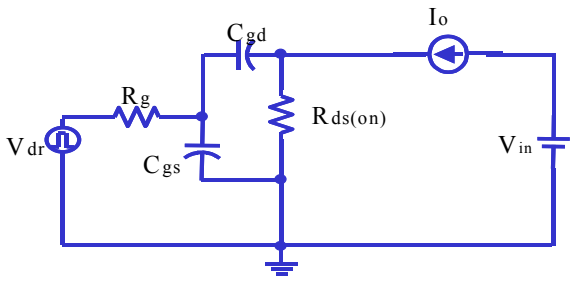


Figure A1-12. Simplified equivalent circuit for the delay period of turn-off.

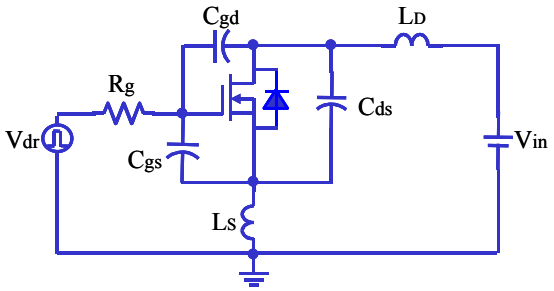


Figure A1-13. Simplified equivalent circuit for the drain-source voltage rising period.

This stage ends when the gate source voltage satisfies that following relationship

$$v_{gs}(t) = V_{th} + \frac{I_o}{g_{fs}}. \quad \text{(A1-29)}$$

A1-2-2-2. The Drain-Source Voltage Rising Period

During this stage, the equivalent circuit is shown in Figure A1-13. The gate voltage is held and a plateau is normally observed. The analysis indicates that the drain-source voltage linearly rises:

$$v_{ds}(t) = \frac{g_{fs}V_{th} + I_o}{(1 + g_{fs}R_G)C_{gd}}t \quad . \tag{A1-30}$$

When the drain-source voltage is equal to the input voltage V_{in}, this stage ends.

Please note that the gate-drain capacitance decreases as the voltage increases. Therefore, the non-linear capacitance model of the devices should be used.

A1-2-2-3. The Drain Current Falling Period

After the drain-source voltage reaches input voltage, the drain current begins to fall. Assuming the drain-source voltage is not clamped, which is a reasonable assumption because in a buck converter the voltage usually cannot be clamped due to the existence of parasitic components in the loop. The clamped-voltage case is not discussed in this appendix. The equivalent circuit is the same as Figure A1-13. The analysis is similar to that in section A1-2-1-2. The time constants are also defined as before.

The sinusoidal solutions occur when $\tau_G{}'^2 < 4\tau_G\tau_m$.

$$v_{gs}(t) = \left(\frac{I_o}{g_{fs}} + V_{th}\right)e^{\frac{-t}{\tau_a}}\left(\cos(\omega_a t) + \frac{1}{\omega_a\tau_a}\sin(\omega_a t)\right) \tag{A1-31}$$

The drain current is

$$i_d(t) = (g_{fs}V_{th} + I_o)e^{\frac{-t}{\tau_a}}\left(\cos(\omega_a t) + \frac{1}{\omega_a\tau_a}\sin(\omega_a t)\right) - g_{fs}V_{th} \quad . \tag{A1-32}$$

The drain-source voltage is

$$v_{ds}(t) = V_{in} + (g_{fs}V_{th} + I_o)\omega_a(L_S + L_D)e^{\frac{-t}{\tau_a}}\left(1 + \left(\frac{1}{\omega_a\tau_a}\right)^2\right)\sin(\omega_a t) \quad . \tag{A1-33}$$

The exponential solutions occur when $\tau_G{}'^2 > 4\tau_G\tau_m$.

$$v_{gs}(t) = \left(\frac{I_o}{g_{fs}} + V_{th}\right)\frac{e^{\frac{-t}{\tau_b}}\tau_b - e^{\frac{-t}{\tau_c}}\tau_c}{\tau_b - \tau_c} \quad . \tag{A1-34}$$

The drain current is

$$i_d(t) = \left(g_{fs}V_{th} + I_o\right)\left(1 - \frac{e^{\frac{-t}{\tau_b}}\tau_b - e^{\frac{-t}{\tau_c}}\tau_c}{\tau_b - \tau_c}\right) - g_{fs}V_{th}. \quad \text{(A1-35)}$$

The drain-source voltage is

$$v_{ds}(t) = V_{in} + \left(g_{fs}V_{th} + I_o\right)(L_S + L_D)\frac{e^{\frac{-t}{\tau_b}} - e^{\frac{-t}{\tau_c}}}{\tau_b - \tau_c}. \quad \text{(A1-36)}$$

This stage ends when the drain current reaches zero.

A1-2-2-4. The Ringing Period

A typical turn-off waveform is shown in Figure A1-14. A severe voltage ringing is observed after the current reaches zero.

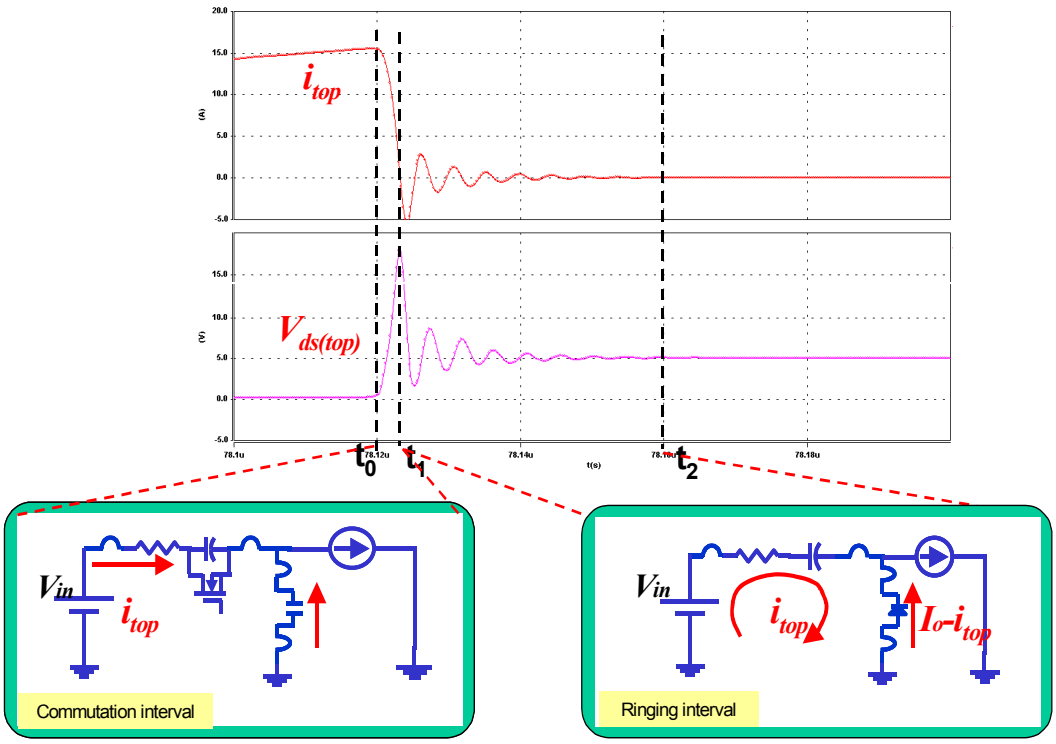


Figure A1-14. Typical waveforms of a buck converter and its simplified equivalent circuits for the different periods during turn-off period.

The $[t_0, t_1]$ period has been analyzed in A1-2-2-1, A1-2-2-2 and A1-2-2-3. At t_1, the drain-source voltage reaches its peak while drain current reaches zero. After t_1, the defined ringing period begins until it is well damped.

As usual, the loss can be calculated based on the current and voltage expressions. The ringing voltage is derived as

$$v_{ds}(t) = V_{in} + (V_{ds\_ifall} - V_{in}) e^{\frac{-t}{\tau_d}} \cos(\omega_d t), \quad \text{(A1-37)}$$

where $\tau_d = \frac{2L_{loop}}{R_{loop}}$, $\omega_d = \left[\frac{1}{L_{loop} C_D} - \left(\frac{R_{loop}}{2L_{loop}}\right)^2\right]^{1/2}$, V_{ds_ifall} is the drain-source voltage at the end of the drain-current falling period, and $C_D=C_{ds}+C_{gd}$. It is pointed out again that the resistance R_{loop} is not only the DC value any more. Due to the high frequency ringing, the AC resistance is very significant.

Obviously, it is complicated and difficult to get a physical meaning. Following the same method used in the ringing loss calculation of the turn-on period, the ringing loss during the turn-off period can be derived as follows. First, the equivalent circuit is shown in Figure A1-15. Again, the load current doesn't contribute to the ringing and therefore is ignored.

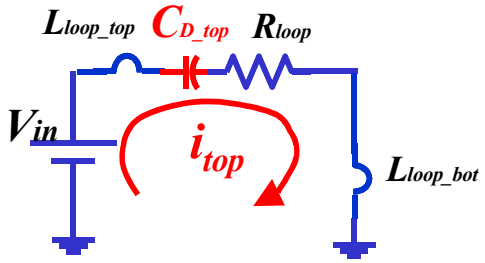


Figure A1-15. Simplified equivalent circuit for the ringing period during the turn-off period.

The energy stored in the loop at t_1 is

$$E_{t1} = \frac{1}{2} Q_{Vpeak} V_{peak} + \frac{1}{2} L_{loop\_bot} I_o^2, \quad \text{(A1-38)}$$

where Q_{Vpeak} is the charge stored in the output capacitor of the top switch when the voltage reaches its peak value V_{peak}, L_{loop_bot} is the parasitic inductance in series with the bottom switch.

At t_2, the oscillation is damped. The circuit reaches another steady state, and the energy stored in the output capacitor is

$$E_{t2} = \frac{1}{2} Q_{Vin} V_{in} + \frac{1}{2} L_{loop\_bot} I_o^2, \quad \text{(A1-39)}$$

where Q_{Vin} is the charge stored in the output capacitor of the top switch when the voltage reaches its steady state V_{in}.

The energy recovered by the input source V_{in} during $[t_1, t_2]$ is

$$\begin{aligned} E_{source} &= \int_{t1}^{t2} V_{in} i_{top}(t)\,dt = V_{in}\int_{t1}^{t2} i_{top}(t)\,dt \\ &= V_{in}\left(Q_{Vpeak} - Q_{Vin}\right) \end{aligned} \quad \text{(A1-40)}$$

Therefore, the energy dissipated in the loop is

$$\begin{aligned} E_{ring\_turnoff} &= E_{t1} - E_{t2} - E_{source} \\ &= \frac{1}{2} Q_{Vpeak}\left(V_{peak} - 2V_{in}\right) + \frac{1}{2} Q_{Vin} V_{in} \end{aligned} \quad \text{(A1-41)}$$

It is found that the ringing loss is relevant to the peak voltage value and independent on the loop resistance.

In order to derive the ringing loss, the peak voltage value is derived based on (A1-32) and (A1-33) or (A1-35) and (A1-36). The peak voltage is achieved at the moment when the drain current falls to zero.

A1-2-2-5. The Conduction Loss of the Bottom Switch

The calculation of the conduction loss is

$$P_{cond\_bot} = \left(I_o^2 + \frac{\Delta I_o^2}{12}\right)\cdot(1-D)R_{ds(on)\_bot}, \quad \text{(A1-42)}$$

where ΔI_o is the ripple of the load current I_o, D is the duty cycle and $R_{ds(on)\_bot}$ is the on resistance of the bottom switch. Following (A1-27), more accurate $R_{ds(on)}$ can be achieved.

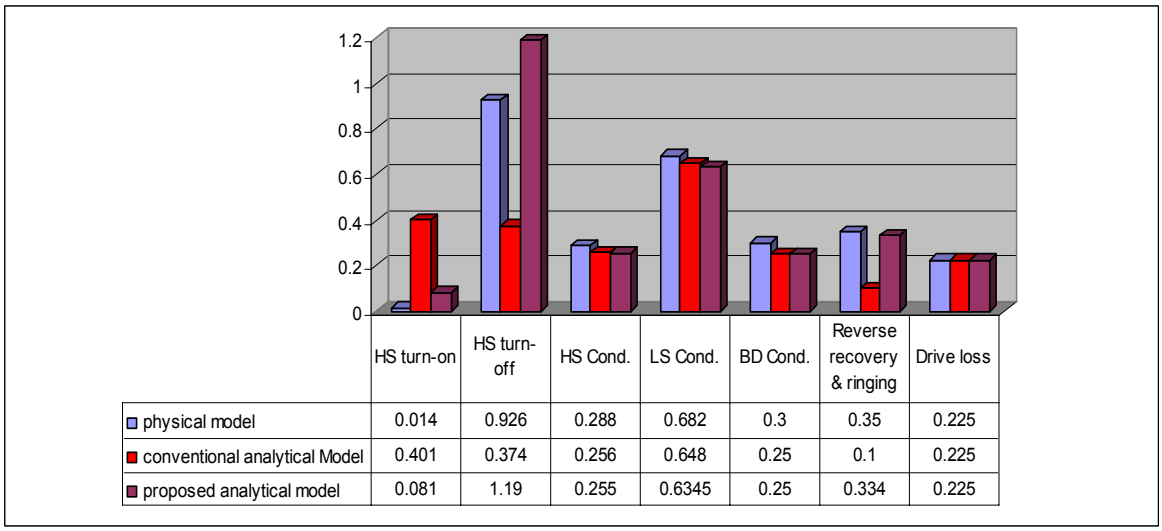
Due to the dead time of the gate signal, the body diode conducts current and causes body diode conduction loss. It is expressed as

$$P_{cond\_bot} = V_{DF}\Delta I_{o\_V} T_{d1} f_s + V_{DF}\Delta I_{o\_p} T_{d2} f_s, \quad \text{(A1-43)}$$

where V_{DF} is the forward voltage drop, ΔI_{o_V} is the valley value of the load current I_o, ΔI_{o_p} is the peak value of the load current I_o, T_{d1} and T_{d2} are the dead time and f_s is the switching frequency.

A1-3. Model Comparison and Discussion

In order to verify this analytical model, a comparison of loss breakdown from other model is provided. The circuit set up is as follow. The device combination is HAT2168 (for top switch) and HAT2165 (for bottom switch). The input voltage is 12V. The output voltage is 1.3-V. The output inductance is 200-nH. The output current is 12.5-A. The switching frequency is 1-MHz. The parasitic inductance are L_{d1}=3-nH, L_{s1}=1-nH, L_{d2}=3-nH and L_{s2}=1-nH. The AC resistance is 150-mOhm. The dead time for body diode conduction is 40-ns.



	HS turn-on	HS turn-off	HS Cond.	LS Cond.	BD Cond.	Reverse recovery & ringing	Drive loss
physical model	0.014	0.926	0.288	0.682	0.3	0.35	0.225
conventional analytical Model	0.401	0.374	0.256	0.648	0.25	0.1	0.225
proposed analytical model	0.081	1.19	0.255	0.6345	0.25	0.334	0.225

Figure A1-16. The comparison of loss breakdown based on different models.

The loss breakdown is shown in Figure A1-16. The left-hand-side bars are the simulation results based on device physical model and the simulation tool is Medici. The middle bars are the simulation results based on the conventional analytical model [A1-2]. And the right-hand-side bars are the simulation results based on the proposed analytical model.

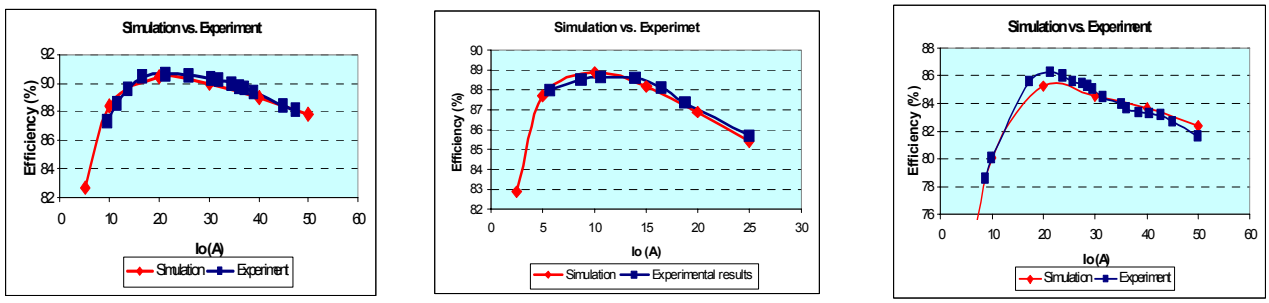
The device's physical model is used as a benchmark for this comparison because it is the most accurate model we have so far. The time frame of the turn-on loss is defined as [t_0, t_1] in Figure A1-9. The ringing loss during the top switch turn-on is calculated by the following way: when the drain current reaches I_o, start to integral the energy pumped from the input source until the oscillation is completely damped. Then, the energy sent to the output and the conduction loss of the top switch is deducted, and the ringing loss during the top switch turn-off is calculated from the moment when the drain current falls back to zero until the oscillation is damped.

Compared to the benchmark, the conventional analytical model has a huge error for the switching loss of the top switch. And the ringing loss is much smaller. The reason is that the non-linear capacitor and parasitic inductance dramatically impact the switching loss, and because the reverse recovery loss is treated as a part of turn-on loss by the conventional model, the turn-on loss is much larger than the real case.

The proposed analytical model shows better accuracy. The switching loss and ringing loss are close to the results of the benchmark. It is further verified by the experimental results in the next section.

A1-4. The Experiment Verification

Based on the proposed model, which considers the non-linear capacitors and the parasitic components in the power stage, the efficiency curves are compared between the experimental results and the simulation results.



(a) (b) (c)

Figure A1-17. The loss model verification with experimental results: (a) top switch HAT2168, bottom switch Si4864, L=200nH, driver LM2726, f_s=1MHz, V_{in}=5 V, V_o=1.2 V; (b) top switch HAT2168, bottom switch HAT2165, L=100nH, driver LM2726, f_s=1MHz, V_{in}=12 V, V_o=1.5 V and (c) top switch HAT2168, bottom switch Si4864, L=100nH, driver LM2726, f_s=2MHz, V_{in}=5 V, V_o=1.2 V.

Figure A1-17 shows three examples. The set up of (a) is as follows: top switch HAT2168, bottom switch Si4864, L=200-nH, driver LM2726, f_s=1-MHz, V_{in}=5-V, V_o=1.2-V. The setup of (b) is: top switch HAT2168, bottom switch HAT2165, L=100-nH, driver LM2726, f_s=1-MHz, V_{in}=12-V, V_o=1.5-V. And the setup of (c) is: top switch HAT2168, bottom switch Si4864, L=100-nH, driver LM2726, f_s=2-MHz, V_{in}=5-V, V_o=1.2-V. The parasitic inductances and AC resistances are simulated through the Maxwell Q3D.

The simulation results match the experimental results very well. It works well even at 2-MHz switching frequency.

This analytical model has been successfully used in the optimal bus voltage study for two-stage approach. It could also be used in other fields needing mass-data process while avoiding long simulation time.

Appendix 2. Analysis of Inductor-Less Un-regulated Bus Converter

The detailed operation principle of the inductor-less bus converter in Chapter 4 is described in this appendix.

A2-1. Operation Principle

A2-1-1. Ideal Operation without Body Diode Conduction

Figure A2-1 shows an inductor-less full-bridge converter with a center-tapped rectifier. The resonant inductors are the leakage inductors L_{k1} and L_{k2}. The resonant capacitor is the output cap C_o. Figure 4-14 shows its key operation waveforms at full load condition and no load condition, respectively. And Figure A2-3 maps its operation waveforms from time domain into the state plane. The converter operates at around 50% duty cycle with open loop control. The full load condition is used to elaborate the operation principle of this converter.

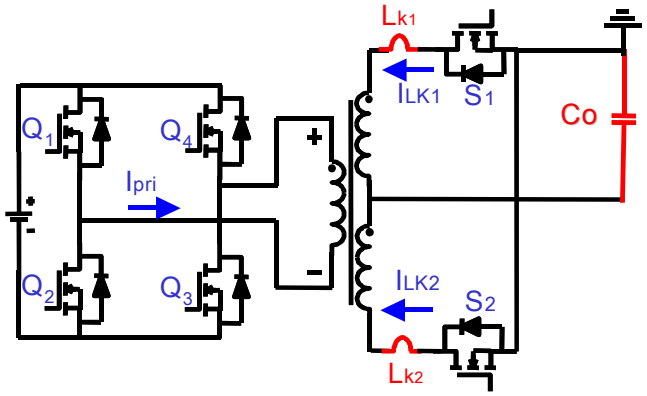
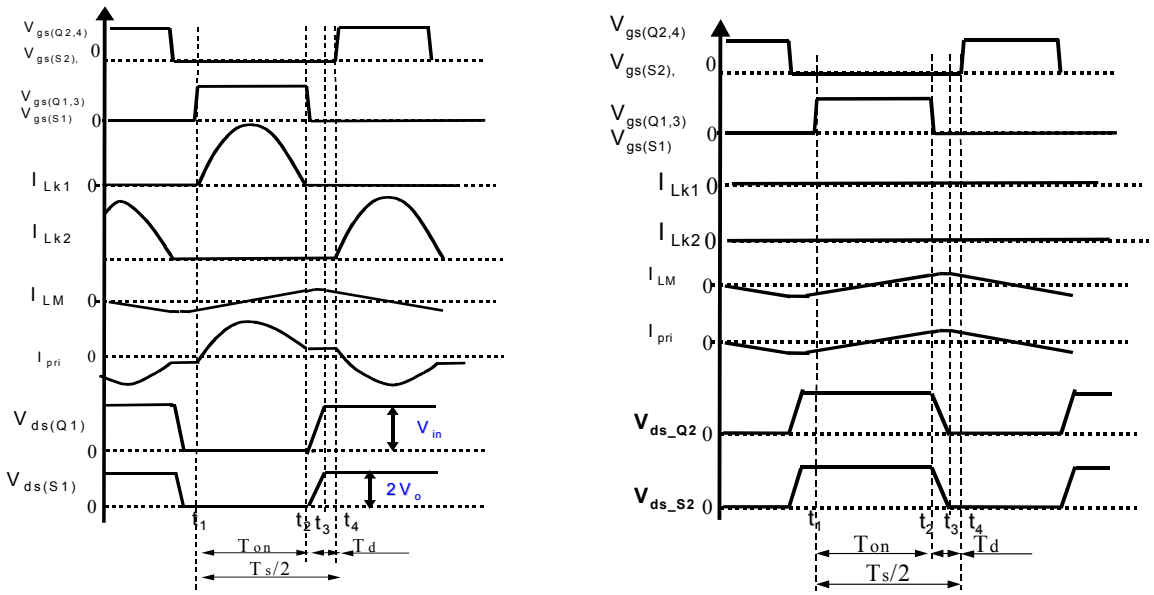


Figure A2-1. Proposed inductor-less full-bridge converter.



(a) full load condition (b) no load condition

Figure A2-2. The operation waveforms of the inductor-less full-bridge converter.

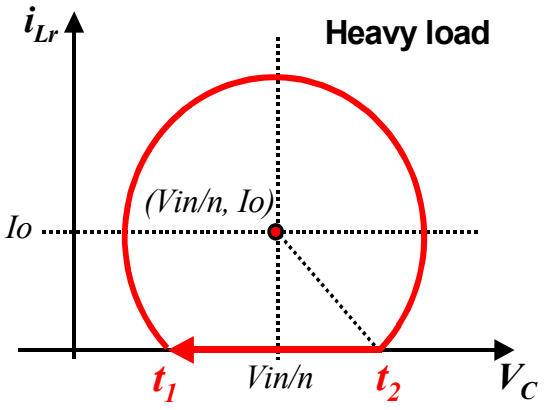


Figure A2-3. The state plane of the proposed inductor-less full-bridge converter with proper timing design at heavy load condition.

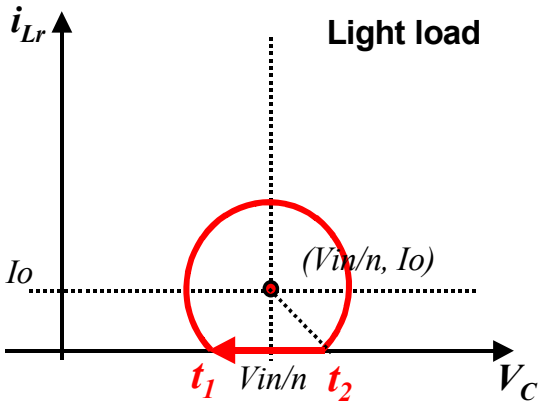


Figure A2-4. The state plane of the proposed inductor-less full-bridge converter with proper timing design at light load condition.

During t_1 and t_2, the primary switches Q_1 and Q_3 and the secondary switch S_1 are on, the energy is transferred from the primary side to the secondary side through the leakage inductor L_{k1} of the transformer. Its equivalent circuit is shown in Figure A2-5(a).

Considering the switching period and carefully designing the resonant components value, the current resonates back to zero and ZCS can be achieved for S_1. Meanwhile, the turn-off

current of the primary switches is only the magnetizing current. As long as the secondary switch is turned off when the secondary current reverts to zero, there is no body diode conduction and therefore no body diode reverse-recovery loss. This is very important for SRs, because the voltage spike is eliminated and a low-voltage-rating device can be safely used, which results in smaller conduction loss.

In order to achieve proper timing design, the values of resonant components need to be well designed. In the bus converter application, planar transformer with PCB winding is widely used, which makes the leakage inductance control easy. So only the capacitance tolerance is taken into consideration, which is discussed in the following section.

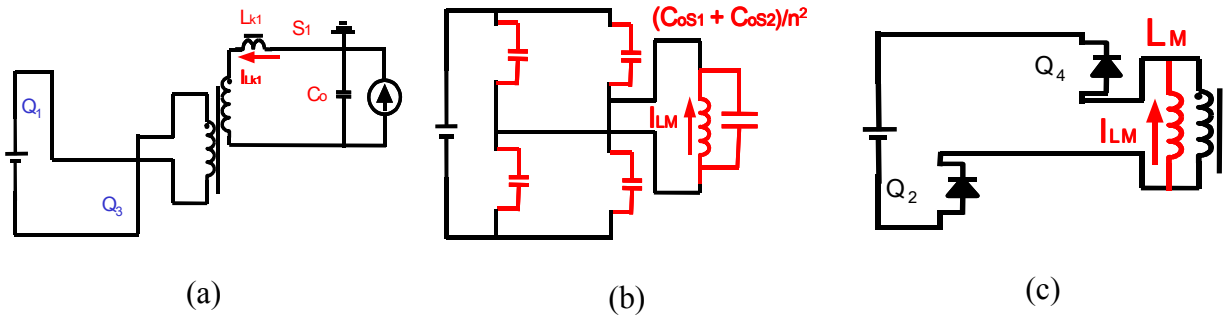


Figure A2-5. The equivalent circuits: (a) during [t_1, t_2], (b) during [t_2, t_3], and (c) during [t_3, t_4].

At t_2, switches Q_1, Q_3 and S_1 turn off and the resonant tank stops working. The output current is only supplied by the output capacitor C_o. Meanwhile, The magnetizing current starts to charge and discharge the output capacitors of the primary switches (as shown in Figure A2-5(b)). Therefore, ZVS can be achieved for the primary switches. In the mean time, the output capacitors of the SRs, C_{os1} and C_{os2}, also serve as snubber capacitors. So ZVS for the SRs can also be achieved.

After t_3, the body diode of Q_2 and Q_4 are on as shown in Figure A2-5(c), the magnetizing current is recovered by the input source.

Starting from t_4, another half-cycle begins and the resonant tank restarts to work. The operation is exactly same as that described above except that the polarity is changed.

It can be seen that the circulating energy of the proposed circuit is very small. If only the resonant tank L_k and C_o is considered, the circulating energy is zero. As the load is getting lighter, the resonant trajectory automatically reduces as shown in Figure A2-4. In the

conventional resonant converter, more and more energy is circulated back to the input source as the load decreases. Therefore, the circuit has very high energy transfer efficiency. As an extreme case, the resonant tank totally stops working at no load condition as illustrated in Figure 4-14 (b). The magnetizing current is still used to achieve ZVS for all devices. Therefore, the proposed converter is able to realize ZVS over the whole load range, which is different from the conventional PWM full-bridge converter.

Based on the state plane shown in Figure A2-3, it can be figure out that the output voltage conversion, nVo/Vin, is always equal to 1 and cannot be regulated as long as the symmetrical trajectory is achieved. However, if a certain status is inserted between t_1 and t_2, the output voltage can be regulated with the pay of turn-off loss at the primary side.

A2-1-2. Non-Ideal Operations

A2-1-2-1. Operation with Small Body Diode Conduction

If the timing is not perfect and the inductor current is not zero when the switches Q_1, Q_3 and S_1 turn off, the body diode conducts current for a while. The operation waveforms are illustrated in Figure A2-6 and its state plane is shown in Figure A2-7.

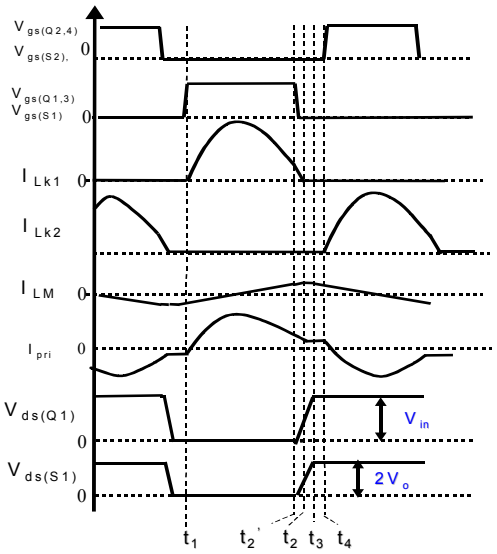


Figure A2-6. The operation waveforms of the inductor-less full-bridge converter with small body diode conduction during [t_2', t_2].

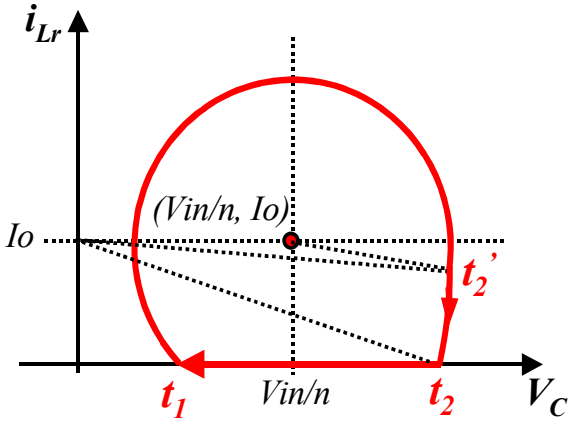


Figure A2-7. The state plane of the proposed inductor-less full-bridge converter with small body diode conduction during [t_2', t_2].

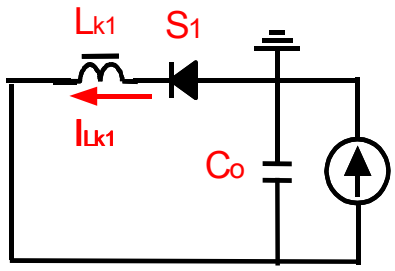


Figure A2-8. The equivalent circuit of phase [t_2', t_2].

It is seen that an additional status is inserted as shown between t_2' and t_2. At this phase, the equivalent circuit is shown in Figure A2-8. However, the excitation changes while the resonant tank keeps same. Compared with the phase [t_1, t_2'], the inductor current falls back to zero much faster. As an example, the inductor current at t_2' is 10-A, the capacitor voltage is 12-V and the leakage inductance is 3-nH. The body diode conduction time is as small as 2.5-ns. During such a small period, the capacitor voltage changes a little. It is a reasonable assumption that the output voltage is constant during this period. Therefore, the change of inductor current could be treated as a linear drop. Beyond t_2, the operation principle is same as the ideal case.

In the conventional PWM converter, the body diode conduction time is fully determined by the preset dead time. During the dead time, the inductor current is almost constant because the output inductance is so large that it can be treated as a current source. Consequently, the current through the body diode is constant, too.

However, in the proposed circuit, there is not an output inductor and the leakage inductance is so small that its energy can be totally, quickly reset before the next cycle begins (refer to the previous example). Consequently, the current through the body diode is a small triangle waveform instead of a constant value. Therefore, even there is body diode conduction; the proposed circuit has much smaller body diode conduction loss than the conventional PWM converter.

A2-1-2-2. Operation with Turn-Off Loss at the SRs

In case of that the resonant frequency is relatively higher and the inductor current changes its direction before the synchronous rectifier S_1 turns off, the waveforms and state plane are depicted in Figure A2-9 and Figure A2-10, respectively.

At this condition, a larger turn-off loss is generated because the SRs have to turn off the current. As we know, the SRs usually have large gate capacitance. Therefore, the switching performance is not good. In addition, a voltage spike occurs across the SRs, which is not desired, either. Compared with the operation with small body diode conduction, the turn-off loss is more severe. This will be proved by the experimental results. Hence, this case should be avoided in the control timing design.

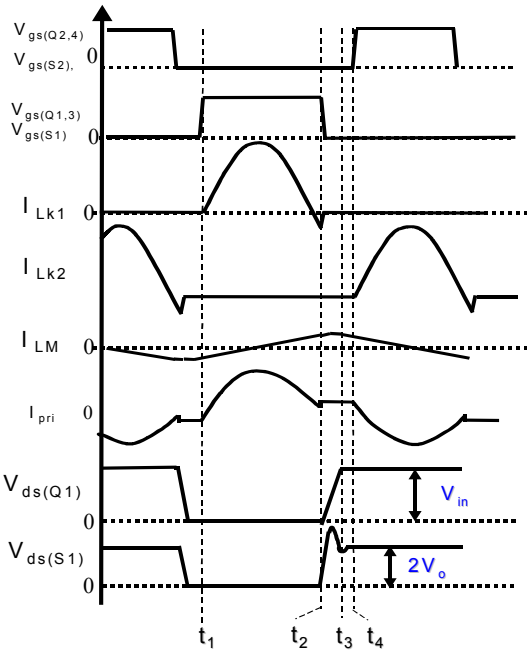


Figure A2-9. The operation waveforms of the inductor-less full-bridge converter with turn-off loss at the SRs.

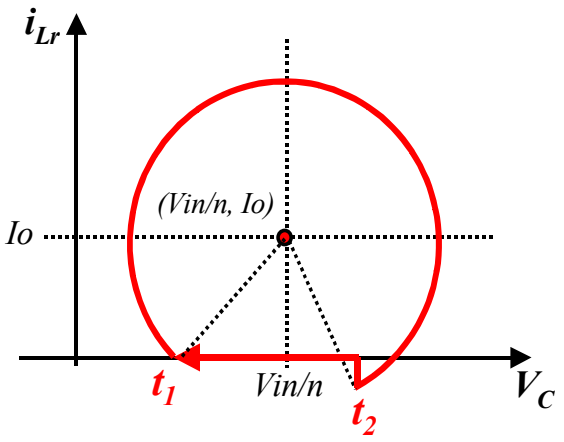


Figure A2-10. The state plane of the proposed inductor-less full-bridge converter with turn-off loss at the SRs.

A2-2. Design Guideline

First of all, the ideal operation case is discussed. During t_1 and t_2, the output voltage and leakage inductor current are expressed as follows:

$$v_c(t) = \frac{V_{in}}{n} - (I_o - I_{r0})\sqrt{\frac{L_k}{C_o}}\sin(\omega t) + (V_{c0} - \frac{V_{in}}{n})\cos(\omega t) \quad \text{(A2-1)}$$

$$i_{Lk}(t) = I_o - (I_o - I_{r0})\cos(\omega t) + \frac{\frac{V_{in}}{n} - V_{c0}}{\omega L_k}\sin(\omega t) \quad \text{(A2-2)}$$

where $\omega = \frac{1}{\sqrt{L_k C_o}}$, n is the transformer turns ratio, L_k is the leakage inductance at the secondary side with the relationship $L_k=L_{k1}=L_{k2}$, V_{in} is the input voltage, I_o is the output current, I_{r0} is the initial current of the leakage inductor and V_{c0} is the initial voltage across the output capacitor C_o.

In order to properly design the circuit, the following equations should be satisfied. As we know, with a proper timing design, the inductor initial current $I_{r0}=0$. After T_{on}, the leakage inductor current goes back to zero. Therefore,

$$i_{Lk}(T_{on}) = 0 . \tag{A2-3}$$

And, the average inductor current in half switching cycle is dictated by

$$\frac{2}{T_s}\cdot\int_0^{Ton} i_{Lk}(t)dt = I_o , \tag{A2-4}$$

where T_s is the switching period and T_{on} is the turn on time of Q_1, Q_3 and S_1 as depicted in Figure 4-14 (a). Meanwhile, the capacitor initial voltage is given by

$$v_c(T_{on}) - \frac{T_d I_o}{C_o} = V_{c0} , \tag{A2-5}$$

where T_d is the dead time equal to $T_s/2-T_{on}$. Based on the state plane, we are able to figure out that the average capacitor voltage in half switching cycle is equal to V_{in}/n, that is

$$\frac{2}{T_s}\int_0^{T_d}\left(v_c(T_{on}) - \frac{I_o t}{C_o}\right)dt + \frac{2}{T_s}\int_0^{T_{on}} v_c(t)\,dt = \frac{V_{in}}{n}\cdot \tag{A2-6}$$

Given a switching period and the load condition, based on (A2-3), (A2-4), (A2-5), and (A2-6), the leakage inductance, the output capacitance, the initial voltage across the output capacitor and the turn on time T_{on} can be derived.

As discussed in A2-1-2, if the inductor current is not zero when the switches turn off, the body diode conducts current. During this period, the inductor current quickly drops to zero. It is a reasonable assumption that the capacitor voltage doesn't change. Therefore, the inductor current at this period $i_{Lk\_additional}(t)$ is expressed by

$$i_{Lk\_additional}(t) = i_{Lk}(t_2') - \frac{v_c(t_2')}{L_k}t \cdot \tag{A2-7}$$

Based on the equations as above, the design parameters for the non-ideal case with small body diode conduction can also be derived.

A2-3. Self-Driven Scheme

To further simplify the circuit, self-driven is applied in this application. Figure A2-11 shows the self-driven scheme. Compared with Figure A2-1, there are two additional windings in the power transformer, which are used to turn on SRs. Besides that, two auxiliary transformers and corresponding circuits are used to turn off SRs. Its control timing is shown in Figure A2-12.

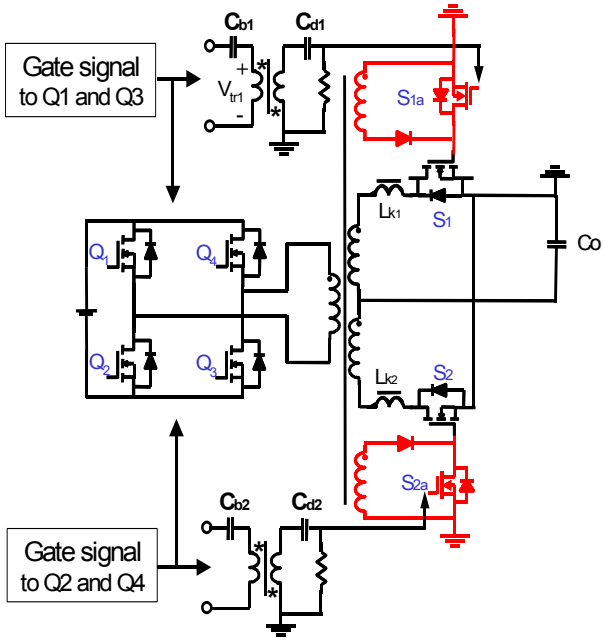


Figure A2-11. The self-driven structure for the inductor-less full-bridge converter.

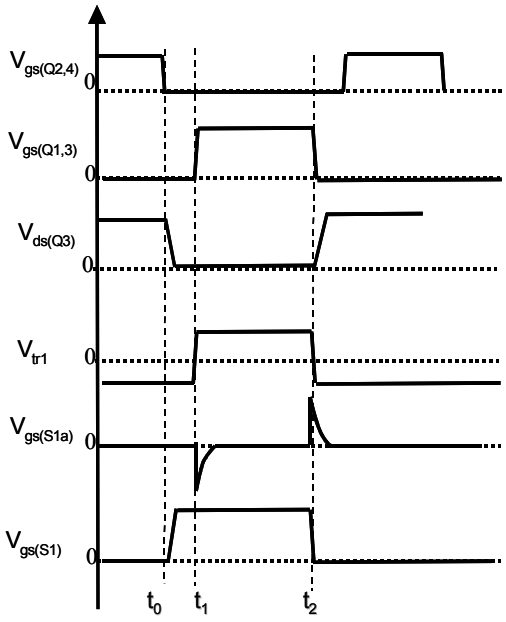


Figure A2-12. The control signal for the SRs with proposed self-driven scheme.

At t_0, when Q_2 and Q_4 turn off, the magnetizing current discharges the output capacitors of Q_1 and Q_3 to achieve ZVS. Meanwhile, the gate capacitor of S_1 is charged. At t_1, Q_1 and Q_3 turn on with ZVS condition. Although the rising edge of V_{gs} for Q_1 and Q_3 goes through a differential circuit, which is composed of a capacitor and resistor (shown in Figure A2-11), and a negative pulse is generated, this pulse doesn't affect the operation.

At t_2, Q_1 and Q_3 turn off. The signal goes through the DC block capacitor C_{b1}. Therefore the voltage across the transformer is only AC components shown as V_{tr1}. The falling edge signal passes through the differential circuit and generates a narrow positive pulse. This pulse is used to

trigger the auxiliary MOSFET S_{1a}. When S_{1a} turns on, the gate source of S_1 is directly shorted and S_1 turns off. Because the auxiliary transformer only transfers a narrow pulse, a small toroidal core is good enough.

Based on this self-driven structure, the gate capacitors of the SRs also serve as the snubber capacitors of the primary switches and are charged by the magnetizing current. As long as ZVS is achieved, a part of the turn-on drive loss can be saved. Basically, the proposed self-driven scheme utilizes a current source, which is magnetizing current, to charge the gate capacitor instead of a voltage source. The smaller the gate resistance, the more drive loss can be saved. However, it is very difficult to give an expression to quantify the relationship between the gate resistances and drive loss because the expression will be more than 4^{th} order. Therefore simulation method is carried out instead. The device model is downloaded from the website of the device vendor.

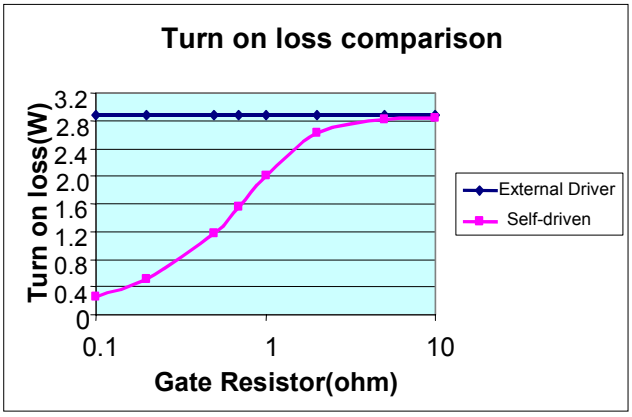


Figure A2-13. The turn-on drive loss comparison between the self-driven structure and the conventional external driver.

For the conventional drive scheme, which uses a voltage source to charge the gate capacitor, the turn-on drive loss can always be calculated by

$$P_{dr\_conv} = \frac{1}{2} C_{gs} \cdot V_{gs}^{2} \cdot f_s \qquad \text{(A2-8)}$$

where C_{gs} is the gate-source capacitance of the device, V_{gs} is the drive voltage and f_s is the switching frequency. It is clear that the drive loss is independent with the gate resistances. Eight HAT2165s running at 1 MHz is used as an example. The drive voltage is 10 V. The turn on drive

loss is always 2.9 W no matter how large the gate resistance is. Figure A2-13 shows the turn-on drive loss comparison between the conventional external driver and the self-driven structure. For a practical design, the gate resistance is around 0.2Ω. At this point, around 80% turn-on drive loss can be saved.

On the other hand, because the auxiliary MOSFET is triggered on by the primary signal to turn off SRs, the turn-off drive loss is completely dissipated.

A2-4. Experimental Verification for Bus Converter

Based on the same prototype of inductor-less full bridge bus converter in Chapter 4, more experimental results are provided to verify the analysis.

As mentioned in the previous section, one design concern is the impact of the tolerance of the output capacitors, which resonate with the leakage inductor of the transformer. If the timing is not perfectly matched, the turn-off current of the primary switches could be relatively larger as shown in Figure A2-14, which would result in a larger turn-off loss. Figure A2-15 illustrates the impact of the output capacitance tolerance on the efficiency at different levels of output power. The tolerance in the test is ±25%, which causes an efficiency variation of only 1.2%. Therefore, the efficiency is not very sensitive to the resonant capacitance tolerance. Actually, more careful observation finds that the efficiency at Co=1.25 case is 0.5% higher than Co=0.75 case. The reason is that the increased SRs' turn-off loss at Co=0.75 is more significant than the increased body diode conduction loss at Co=1.25. Hence, as discussed in previous section, the smaller resonant period is not desired and should be avoided.

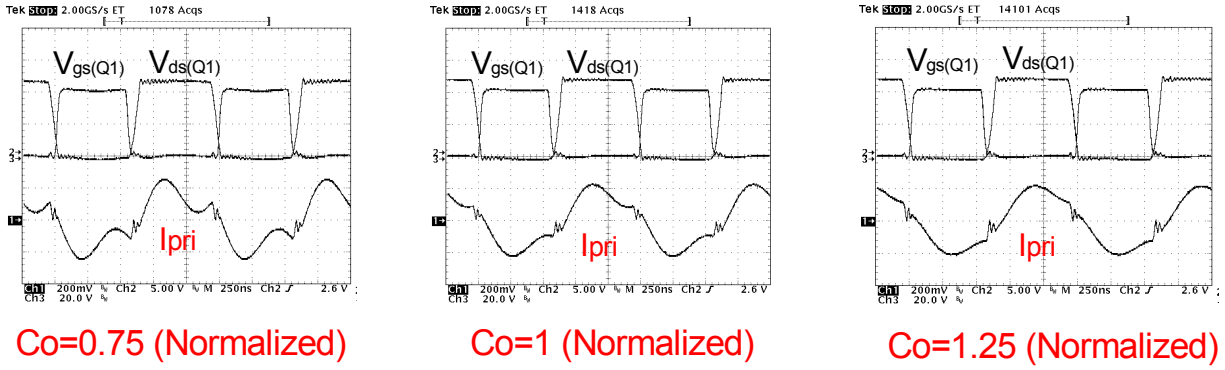


Figure A2-14. The current waveforms with different resonant capacitor values.

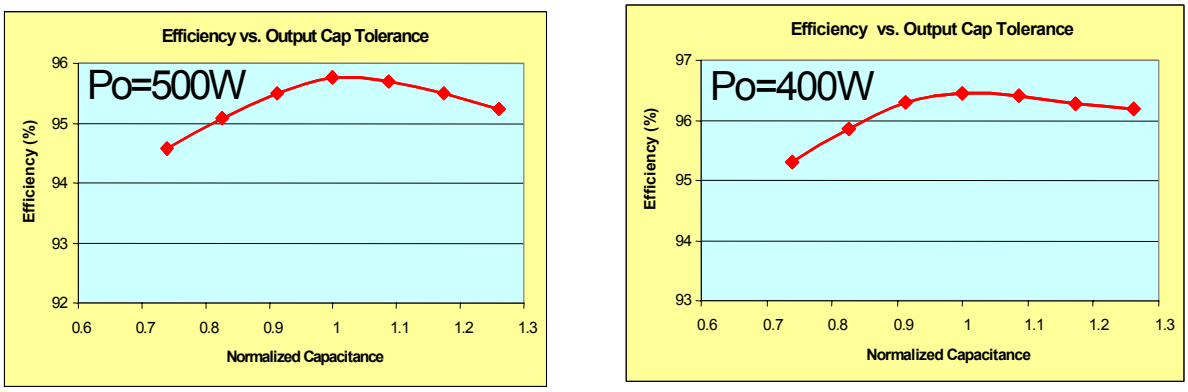


Figure A2-15. The impact of Co tolerance on the efficiency: (a) P_o=500W and (b) P_o=400W.

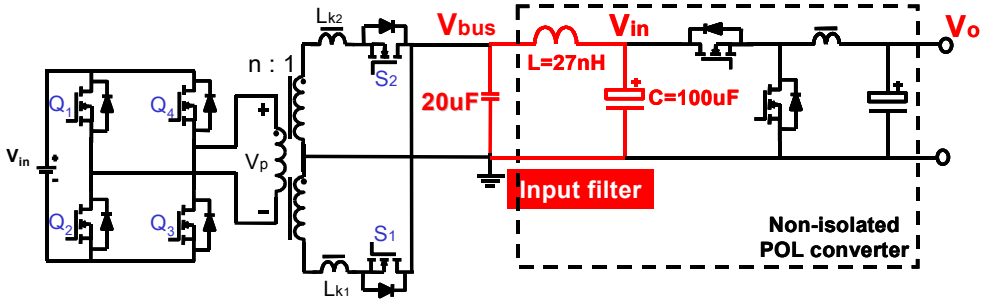


Figure A2-16. The whole system schematic and the input filter of the second stage is design as: L=27nH and C_{in}=100uF.

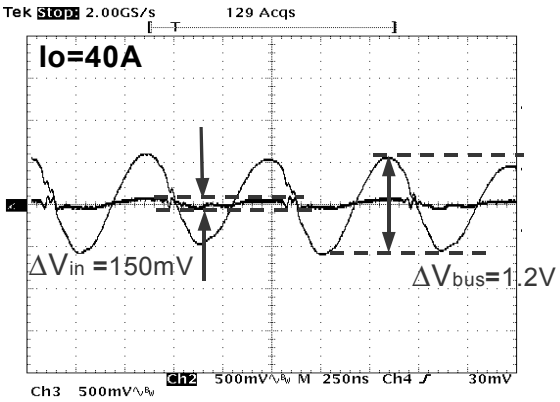


Figure A2-17. The intermediate bus voltage waveforms.

Another design concern is the large output voltage ripple. Figure A2-17 shows the voltage V_{bus}, which is across the resonant capacitor C_o. At 12V/40A output condition, the peak-to-peak voltage ripple is around 1.2 V. Fortunately, the ripple frequency is around 1.6 MHz, which can be easily attenuated by the input filter of the second stage (as shown in Figure A2-16). As an

example, the input inductance is designed only 27 nH and the input capacitance is 100 uF. The experimental results indicate that the voltage ripple after the input filter can be attenuated down to 150 mV (shown in Figure A2-17), which doesn't adversely impact the second stage's performance at all.

A2-5. Concept Extension

The concepts used in the full-bridge bus converter are resonance between the leakage inductor of the transformer and the output capacitors, ZVS realization by magnetizing inductor and no output inductor. Actually, they can be applied to many other topologies.

A2-5-1. Isolated Bus Converter

These concepts can be applied to many isolated topologies [11], e.g., half-bridge (Figure A2-18), active-clamped forward (Figure A2-19), resonant-reset forward (Figure A2-20), push-pull (Figure A2-21), push-pull forward (Figure A2-22), and so on. The resonant-reset forward converter is the simplest topology, employing only two devices and one transformer.

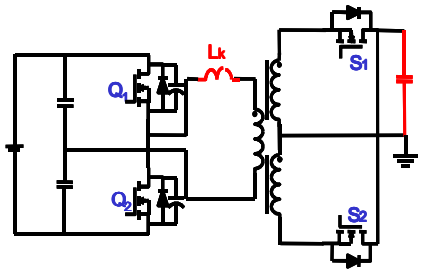


Figure A2-18. Concepts applied to half-bridge converter.

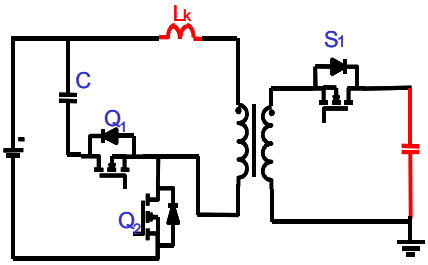


Figure A2-19. Concepts applied to active-clamped forward converter.

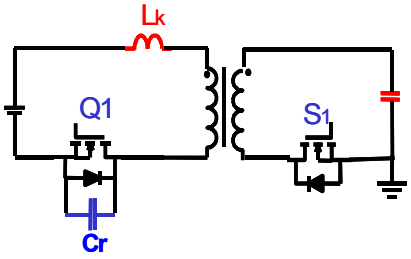


Figure A2-20. Concepts applied to resonant-reset forward converter.

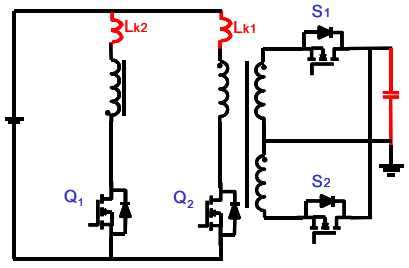


Figure A2-21. Concepts applied to push-pull converter.

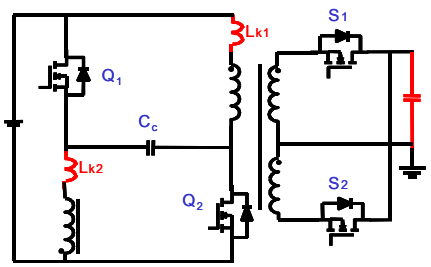
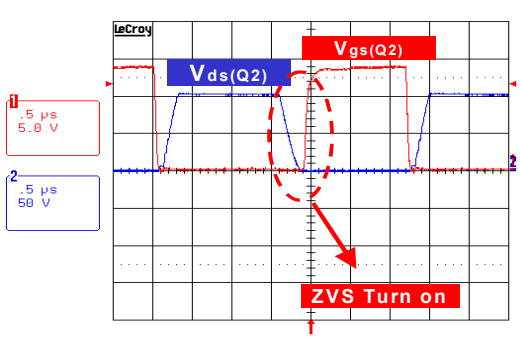
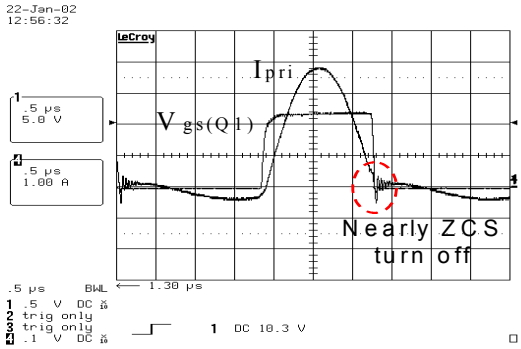


Figure A2-22. Concepts applied to push-pull forward converter.

In order to verify the generic characteristics of these concepts, hardware is built. The experimental waveforms of active-clamped forward and resonant-reset forward converters are provided in Figure A2-23 and Figure A2-24. It is obvious that the ZVS and nearly ZCS condition is achieved. Therefore high efficiency and high power density can be accomplished.

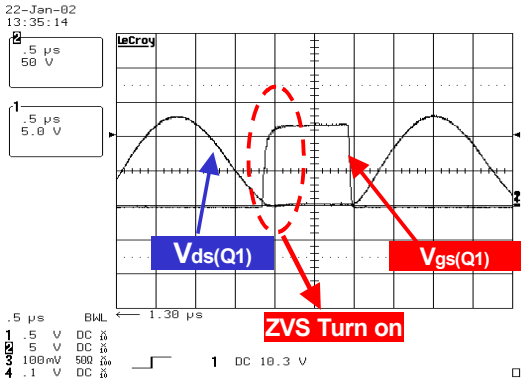


(a)

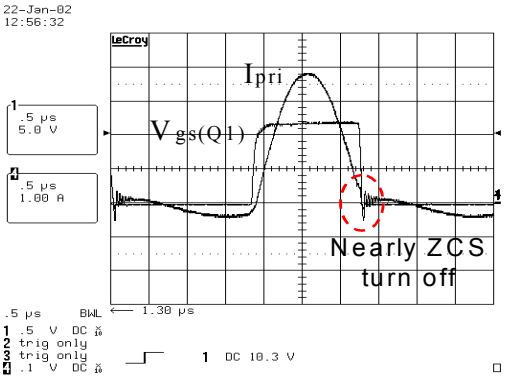


(b)

Figure A2-23. Waveforms of inductor-less active-clamped forward with resonant operation, (a) drain-source voltage and gate signal of switch Q_2 and (b) current and gate signal of Q_2.



(a)



(b)

Figure A2-24. Waveforms of inductor-less resonant-reset forward with resonant operation, (a) drain-source voltage and gate signal of switch Q_1 and (b) current and gate signal of Q_1.

A2-5-2. Non-isolated Bus Converter

Same as the isolated bus converter, the concepts can also be applied to a lot of non-isolated DC/DC converters, such as half-bridge (Figure A2-25 (a) and (b)), full bridge (Figure A2-25 (c)), push-pull (Figure A2-25 (d)) and forward converters (Figure A2-25 (e)). For the forward converter, only conceptual diagram is shown. Actually, there are a lot of different structures according to the different magnetizing current reset methods.

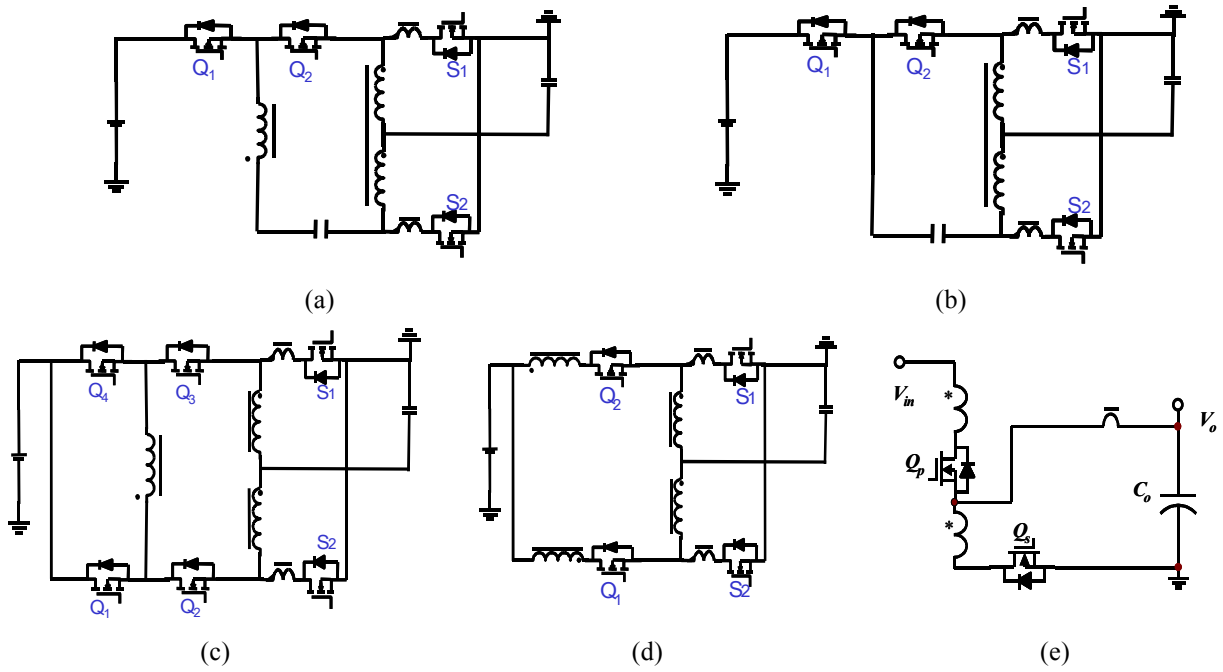


Figure A2-25. The concepts applied to the non-isolated DC/DC converters: (a) half-bridge with transformer version; (b) half-bridge with autotransformer version; (c) full bridge; (d) push-pull and (e) forward.

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Chapter 1

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