High Frequency, High Current Density Voltage Regulators

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(ABSTRACT)

As a very special DC-DC converter, VRM (Voltage Regulator Module) design must follow the fast-developing trend of microprocessors. The design challenges are the high current, high di/dt, and stringent load-line requirement. When the energy is transferred from the input of a VRM, through the VRM, then through the power delivery path to the processor, it needs sufficient capacitors to relay this energy. The capacitors' number appears to be unrealistically large if we follow today's approach for the future processors. High frequency VRM with high control bandwidth can solve this problem, however, the degradation of efficiency makes the conventional buck converter and the hard-switching isolated topologies incapable of operating at higher frequency. The research goal is to develop novel means that can help a high-output-current VRM run efficiently at high frequency.

A novel Complementary Controlled Bridge (CCB) self-driven concept is proposed. With the proposed self-driven scheme, the combination of the ZVS technique and the self-driven technique recycles the gate driving energy by making use of the input capacitor of the secondary-side synchronous rectifier (SR) as the snubber capacitor of the primary-side switches. Compared to the external driver, the proposed converter can save driving loss and synchronous rectifier body diode conduction loss. Additionally, compared to the existing level-shifted self-driven scheme for bridge-type symmetrical topologies, its gate signal ringing is small and suitable for high-frequency applications.

Although the CCB self-driven VRM reduces the switching frequency-related losses significantly, the conduction loss is still high. Inspired by the current-doubler concept, a novel ZVS current-tripler DC-DC converter is proposed in this work. By utilizing more SR devices to share the current during the freewheeling period, the SR conduction loss is reduced. The current-tripler DC-DC converter has a delta/delta connected transformer that can be implemented with integrated magnetics. The transformer then becomes an integrated magnetic with distributed windings, which is preferred in high current applications. The current-tripler DC-DC converter in

fact meets the requirements for the CCB self-driven scheme. The two concepts are then combined with an integrated gate drive transformer.

The proposed CCB self-driven concept and current-tripler concept can both be applied to the 12V non-isolated VRMs. The proposed topology is basically a buck-derived soft-switching topology with duty cycle extension and SR device self-driven capabilities. Because there is no isolation requirement, the SR gate driving becomes so simple that the voltage at the complementary controlled bridge can be used to directly drive the SR gate. Both the gate driving loss and the SR body diode conduction loss are reduced. The proposed circuit achieves similar overall efficiency to a conventional 300kHz buck converter running at 1MHz.

All the circuits proposed in this dissertation can use coupling inductors to improve both the steady-state efficiency and dynamic performances. The essence of the coupling inductors concept is to provide different equivalent inductances for the steady state and the transient. Moreover, when a current loop becomes necessary to achieve proper current sharing among phases, the current loop sample hold effect will make it difficult to push the bandwidth. The sample hold effect is alleviated by the coupling inductors concept. A small-signal model is proposed to study the system dynamic performance difference with different coupling inductor designs. As the verification, the coupling concept is applied to the 12V non-isolated CCB self-driven VRM and the bandwidth as high as one third of the switching frequency is achieved, which means a significant output capacitor reduction.

TO MY PARENTS

SHENGYANG CHEN
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Chapter 1. Introduction

1.1. Research Background

The modern technologies with which we are so familiar, such as computers, the internet, wireless communications, etc, all started from the invention of integrated circuits. The more the transistors are integrated into a single die, the more functions that die can perform. Just as Moore's Law predicts that transistor density doubles every eighteen months, the transistors per die in microprocessors have increased steadily in the past decade. Taking the world leading CPU company Intel as an example, the transistors per die is heading towards one billion in 2007, which is one million times more than the first CPU it developed thirty years ago (Figure 1.1) [1].

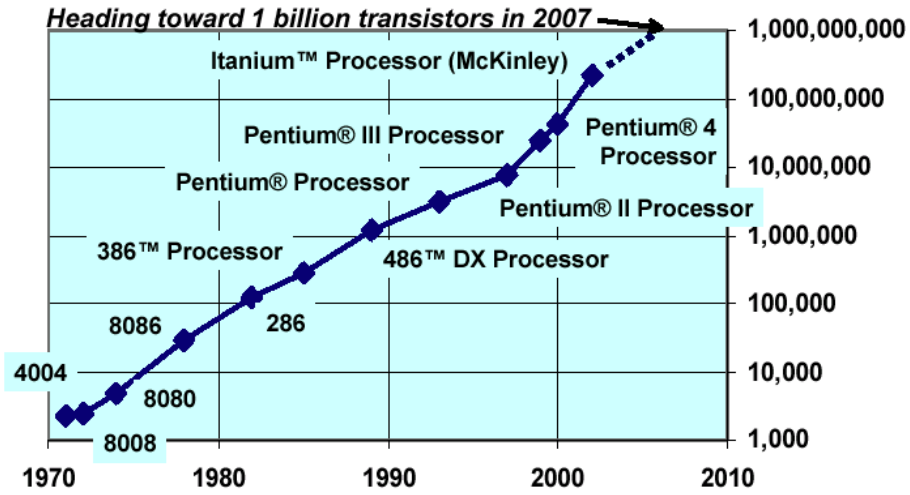


Figure 1.1 Transistors per die in Intel microprocessors

Transistor density is not the only factor that determines the performance of a microprocessor. How fast a transistor can switch, or clock frequency, represents the performance of the CPU. For example, an i486 processor can run at 25MHz, while today's Pentium4 processor is running in the 3-4GHz range.

The increases in the microprocessors' speed and transistor number have resulted in an increase in power demands. Figure 1.2 shows the average power of different Intel processors.

Currently, for cost-performance CPUs in desktop applications, the power consumption is about 100W. For high-performance CPUs, such as the Itanium® processor, it goes up to 130W. It is no longer an easy task to deal with these losses. According to the International Technology Roadmap of Semiconductors (ITRS), the high performance CPU power will exceed 200W by year 2010. Moore's Law eventually will have to confront the laws of physics — the power and thermal limitations. This phenomenon is often referred to by Intel as the "power wall" [2].

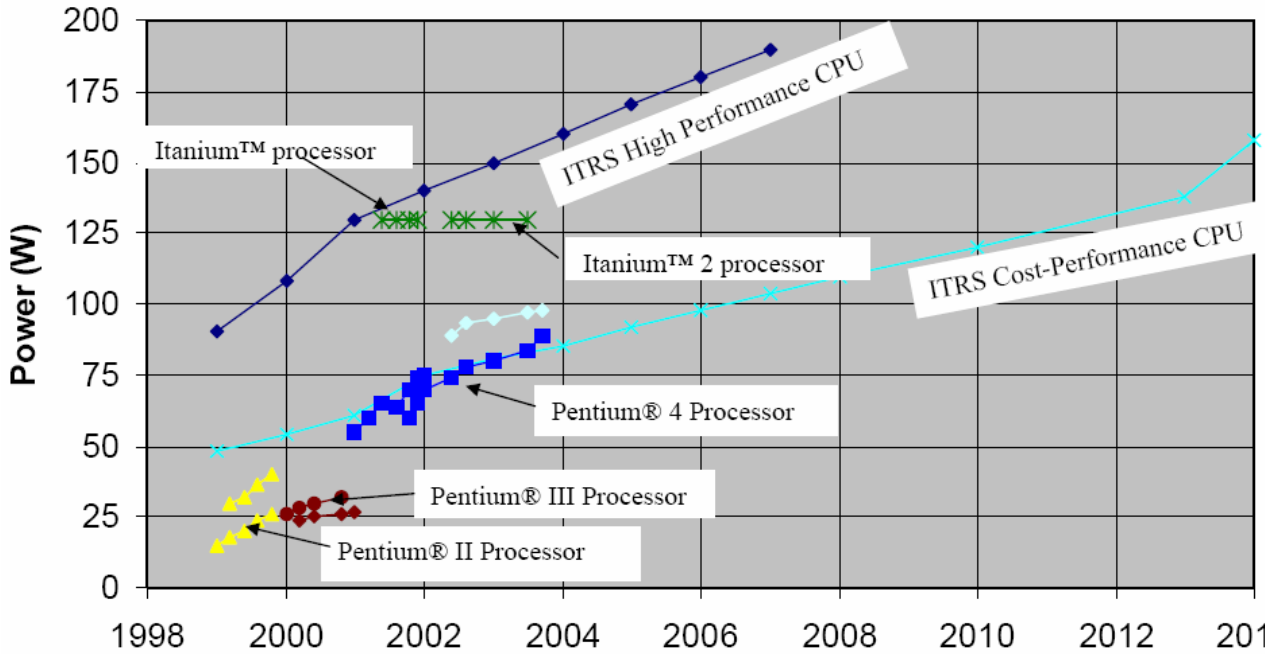


Figure 1.2 Processor power consumptions

In order to minimize the power consumption of the microprocessors, the supply voltage V_{dd} has to be decreased so that the energy dissipated during one clock cycle, CV_{dd}^2, is reduced significantly. However, lower V_{dd} means even higher supply current because the CPU power is also increasing. Figure 1.3 shows the power supply roadmap of Intel's processors. A 120A/0.8V power supply will be needed by year 2010 [5][6].

Moreover, due to the high clock frequencies, the microprocessors' load transition speeds also increase. The trends for microprocessor load current slew rates are also shown in Figure 1.3. The low voltage, high current, and fast load-transition speeds are the challenges imposed on microprocessors' power supplies. Determining how to efficiently deliver the large amount of

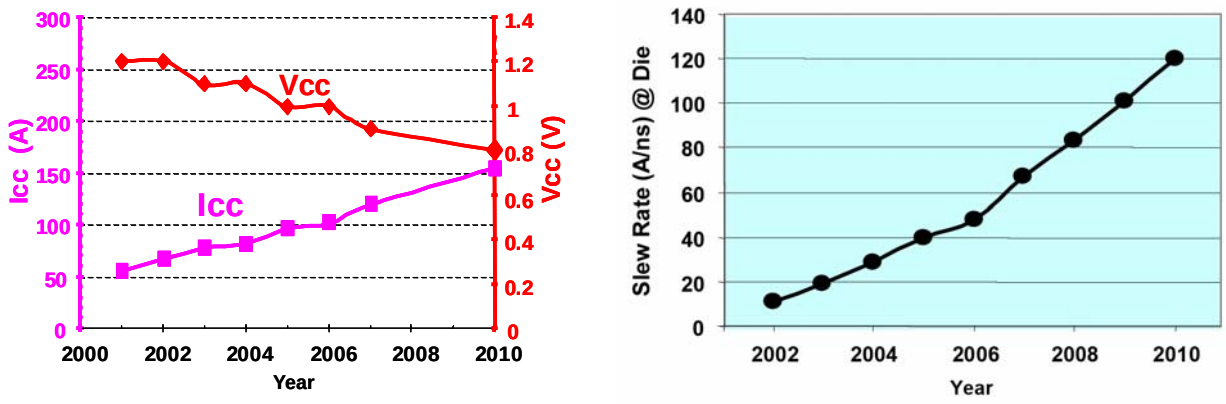


Figure 1.3 The road map of Intel's microprocessors' power supplies

energy to the processor as fast as possible is a big task for power electronics researchers and engineers.

Figure 1.4 shows the centralized power architecture of a typical low-end computer system, such as a desktop, workstation or entry-level server. The silver box, which was the original power supply structure, could no longer satisfy the new processor's requirements of decent efficiency with high current and fast transient response with tight tolerance. A voltage regulator module (VRM), which can be physically located on the motherboard next to the microprocessor, was introduced to convert 12V bus voltage to the required output power. The VRM must feature fast transient response, good voltage regulation, a small size, and high efficiency [7~15]. Isolation is not required for VRMs in this architecture.

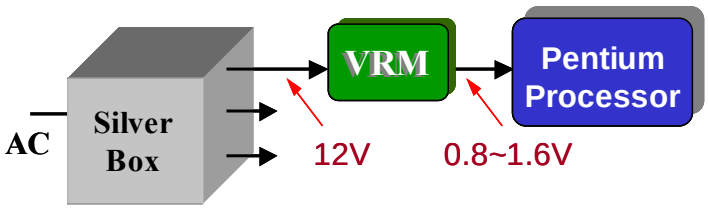
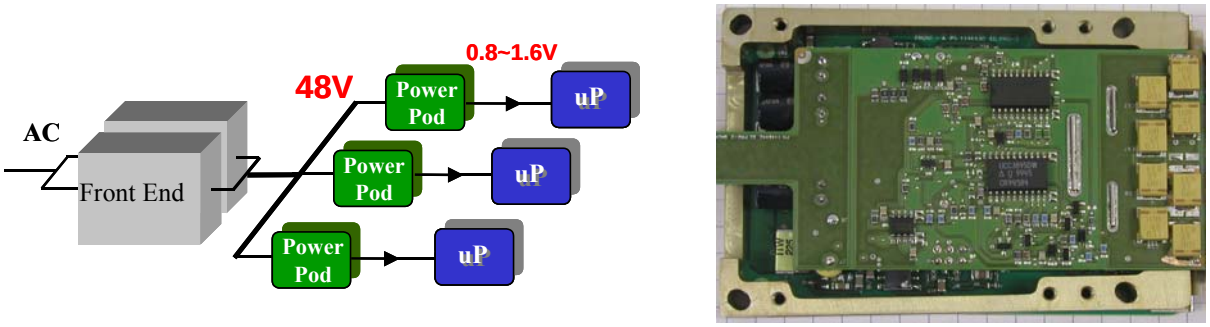


Figure 1.4 Processor power path of low-end computer systems

For data communication and high-end computing applications, multiple processors are commonly used on one motherboard, and the motherboard is then inserted into the rack, which has many slots for these processor boards. The entire system consumes much more power than the desktop. As a result, in order to reduce the loss on the distributed bus, the power architecture of a data center or a high-end server is a 48V distributed power architecture (DPA), a structure

widely used in the telecommunication systems. Each processor has its own VRM in close proximity. The VRM, which has its own isolation, is directly connected to the processor through power tabs. This 48V input isolated VRM is also called a power pod by Intel, as shown in Figure 1.5(b). Besides the lower conduction loss on the bus, in a high-voltage DPA the transient response of the load has less effect on the bus voltage, as well as less effect on the other loads. Another merit of the 48V-input power pod is that because transformers are used, the duty cycle can be optimized for efficiency, ripple-canceling effect and transient by adjusting the turn's ratio.



(a) DPS architecture (b) A power pod

Figure 1.5 Processor power path for high-end server/ data communication systems

The DPA system is a relatively high-cost system compared to a centralized power solution because of the large number of isolated DC-DC converters. In 1996, Narveson asked how many isolated dc-dc converters were really necessary [29]. In most cases, only one isolated DC-DC converter is needed. In the past years, this idea of one isolated converter and many non-isolated DC-DC converters has been widely adopted under the name Intermediate Bus Architecture (IBA). In an IBA system, the non-isolated point of load (POL) converters are powered from an intermediate bus converter (IBC) as shown in Figure 1.6. In the traditional isolated power pod, the output voltage is typically regulated by comparing the output voltage to a reference, transmitting the error signal from the secondary side to the primary side using an optocoupler, and then using a PWM controller to vary duty cycle in proportion to the error signal. "The regulation requirements for an IBC are not as stringent as those required in the traditional DC-DC converter because the output of a POL is tightly regulated. Therefore the IBC designer has the option to incur less cost by providing moderate regulation or by operating at a fixed duty cycle over all line and load conditions" [30, 31].

One important design parameter in an IBA system is the intermediate bus voltage. It is highly dependent on the power levels, the number of POLs connected to the intermediate bus and their locations, and the efficiencies of both the bus converters and the POLs. For most of today's bus converter products, their nominal output voltages are 12V but actually vary from 9.7V to 13.5V according to the input voltage change and the load condition change. There are also vendors providing 8V bus converter solutions claiming better overall efficiency (such as International Rectifier). Since the bus converter itself is a low-cost, easy-to-implement DC-DC converter, this dissertation will not discuss it at length. The most challenging part of the IBA structure is the POL converter, which needs to deliver high-current, low-voltage, and fast transient output to the processor. Generally speaking, a POL converter is a non-isolated VRM at the point of load. Since the 12V intermediate bus is the mainstream, this dissertation will focus on the 12V non-isolated POLs.

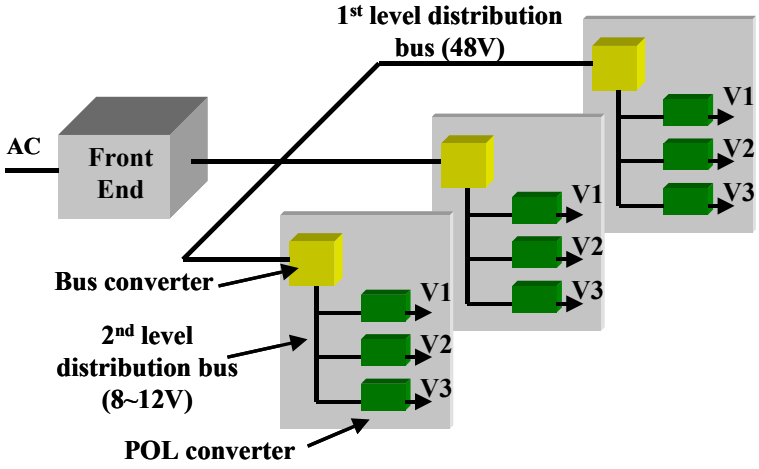


Figure 1.6 IBA power delivery architecture for high-end server/ data communication systems [30]

Although VRMs take a variety of form factors for different computer systems, the fundamental requirements for VRMs are generally the same. The fast dynamic transients happen when the microprocessor chip switches from sleep mode to active mode and vice-versa. The small transient voltage deviation under high currents and high slew rates is the most stringent requirement. As the operating voltage is reduced to below 1V, the transient voltage tolerance is also expected to decrease and become much tighter. Because of the high cost of space in the motherboard, power density and efficiency are also very important for VRMs. These performance requirements pose serious challenges for VRM design.

1.2. A Close Look at Today's VRMs

A. 12V Non-isolated VRM

In low-end computer systems, since there is no isolation requirement, the synchronous buck converter is widely used for VRMs because of its simple structure, low cost and low conduction loss. A further improvement is the adoption of the multiphase interleaving technique (illustrated in Figure 1.7). By paralleling several synchronous buck converters and phase shifting their drive signals, the interleaving approach can reduce both the input and output current ripples, improve the transient response, and distribute the power and heat. As a practical design, two or more SR devices are usually in parallel for each phase to reduce the on resistance. Table 1.1 lists the latest VRD and VRM products from major vendors in the world. (VRD refers to the onboard VRM built directly onto the motherboard). Most of today's VRMs consist of 3 or 4 phases, operating at about 200~300KHz switching frequency per phase.

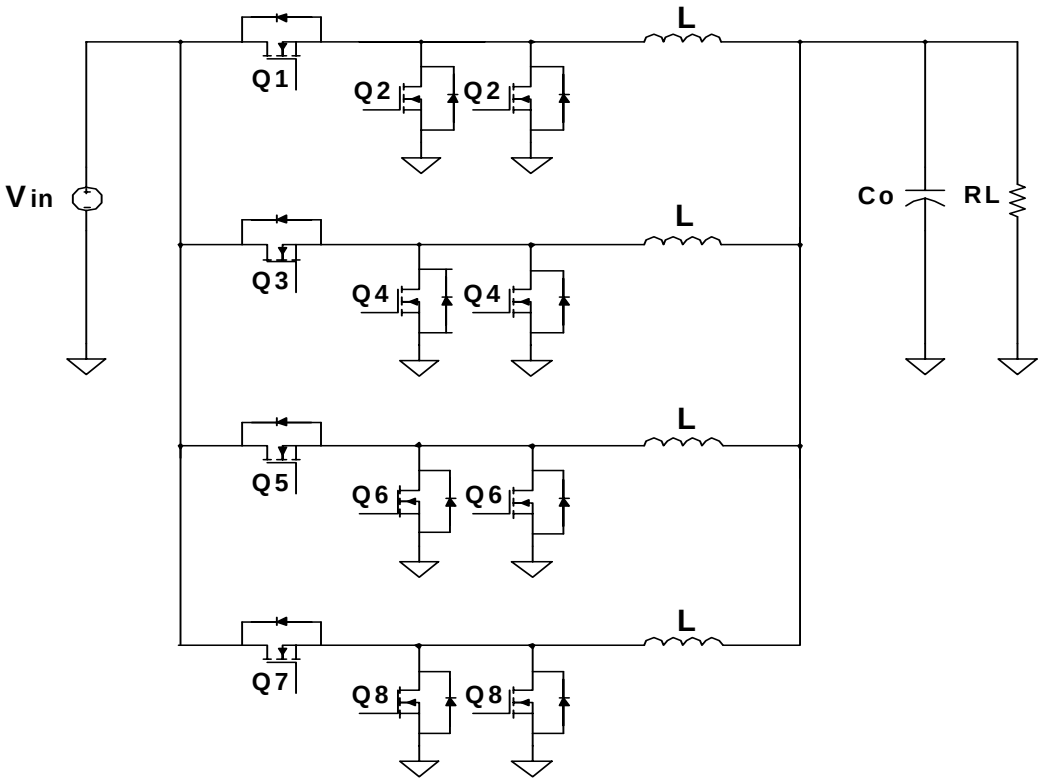


Figure 1.7 A four-phase interleaving VRM

All the VRMs built for today's Intel processors need to meet the stringent transient response requirement. Figure 1.8 shows a VR load line example from the Intel VR 10.0 spec. The load line contains static and transient voltage regulation data as well as maximum and minimum voltage levels. According to Intel's recommendation, the voltage in Figure 1.8 is the voltage of the regulator's differential remote sense point located at the center of the processor's socket cavity. The upper and lower load lines represent the allowable range of voltages that must be presented to the processor. The voltage must never exceed these boundaries for proper operation of the processor [3].

Table 1.1 List of today's VR products

	Company	Io(A)	Fs(kHz)	Phase No.	L_o(nH)
VRD	Intersil	100	300	4	300
	Fairchild	65	228	3	650
	Infineon	100	200	4	600
	National	70	300	4	690
	ADI	65	300	3	600
VRM	Maxim	100	210	4	600
	C&D Tech	150	300	-	-
	Artesyn	85	550	4	-

However, in a CPU, the high clock speed circuits and power conservation design techniques such as clock gating and sleep modes result in fast, unpredictable, and large magnitude changes in the supply current. The rate of change could be many amps per nanosecond. If not well-managed, these current transients may cause the VR output voltage to go outside the regulation band and manifest them as power supply noise that ultimately limits how fast the CPU can operate. This is further compounded by the reduced noise margin in the CMOS logic circuits that result from power supply voltage scaling. While voltage overshoots may cause

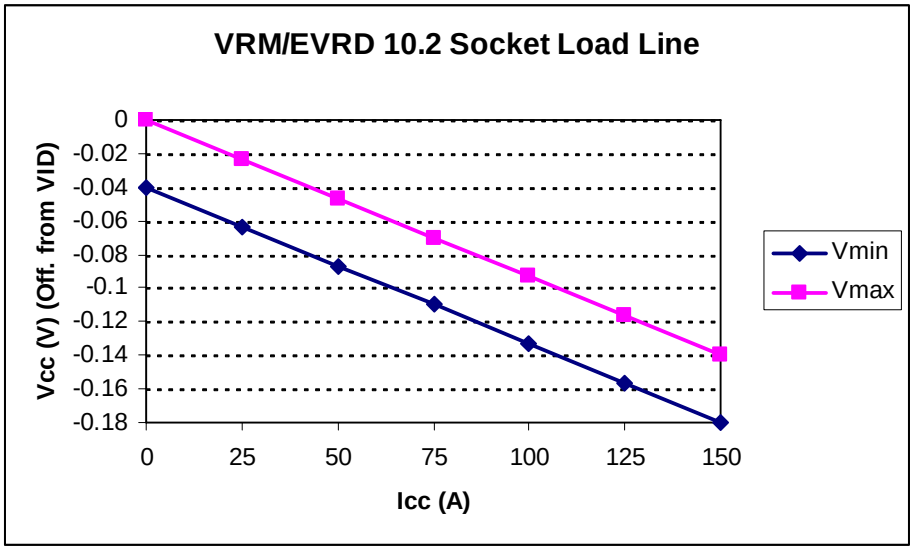


Figure 1.8 Load line specified by Intel VRM/EVRD 10.2

the CPU reliability to degrade, undershoots may cause malfunctions of the CPU, often resulting in the "blue screen" indicating the PC is about to crash.

This is why output filter capacitors are so important for a processor to operate properly. Figure 1.9 shows a typical power delivery path for today's processors. In order to supply sufficient energy to the processor, sufficient energy storage components have to be placed in different locations.

The closest capacitors to the VRM are so called "bulk" capacitors. In most of today's designs, a special type of electrolytic capacitor — the Oscon capacitor — is widely used as the bulk capacitor. It has relatively low ESR and ESL values compared to the general purpose electrolytic capacitor while still having a large capacitance; for example: C=560μF, ESR=7~10mΩ, ESL=8nH. Following the Oscon capacitors in the power path, Multi-Layer Ceramic Capacitors (MLCCs) are used as the decoupling capacitors. The MLCC has even lower ESR and ESL values than the Oscon capacitors, but the capacitance is also small. A typical value would be: C=47μF, ESR=3.5mΩ, ESL=2nH. Because of their small package sizes, these MLCCs are usually located in the socket cavity. The packaging capacitors are those included in the CPU package. They are also ceramic capacitors.

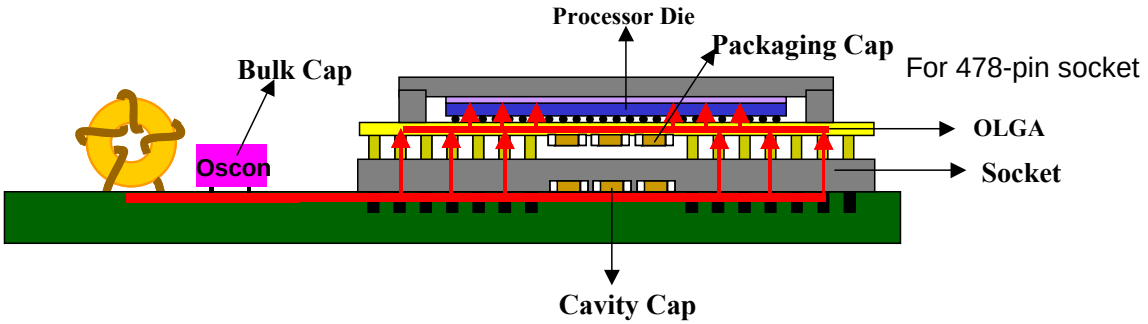


Figure 1.9 A typical power delivery path for today's processors

Figure 1.10 shows a lumped circuit model of the power delivery path of today's microprocessor. For a 300kHz VRM, there should be twelve 560uF Oscon capacitors and eighteen 47uF MLCC capacitors. These capacitors account for about 40% of the total VRM cost. Moreover, the sizes of those Oscon capacitors are so large that the overall footprint of the VRM occupies 12% of the motherboard [19].

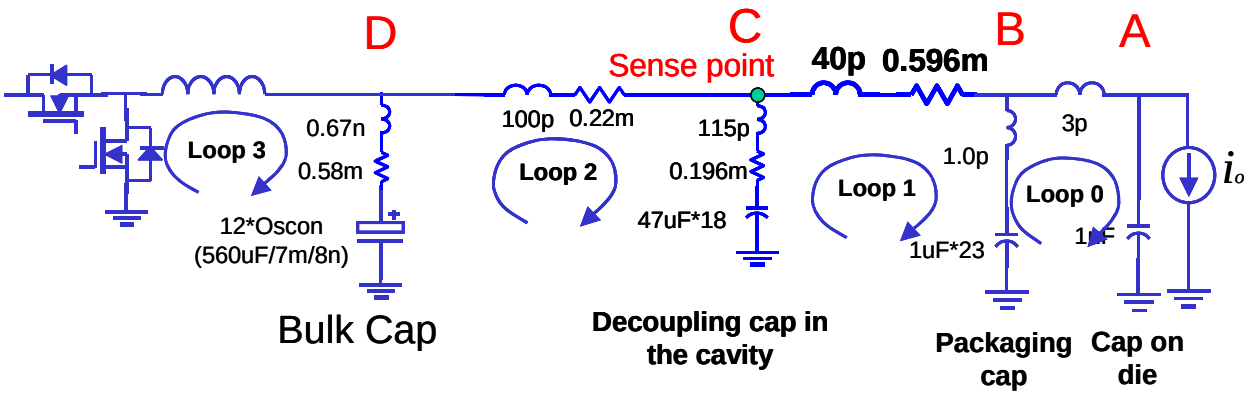


Figure 1.10 A lumped circuit model of the power delivery path of today's microprocessor

B. 48V Isolated VRM (PowerPod)

Most of today's 48V VRMs use pulse width modulation (PWM) hard-switching topologies with synchronous rectifiers (SR), such as the active clamp forward, the symmetrical or asymmetrical half bridges [33, 44], push-pull, push-pull forward [50], etc (Figure 1.11).

The active clamped forward converter shown in Figure 1.11(a) has become a suitable topology in low-voltage DC-DC converter applications because it recovers the magnetizing energy as well as the leakage energy of the transformer and minimizes the voltage and current

stresses of the primary switches and those of the rectifiers [32]. However, when a fast transient is at the top of the priority list, this topology loses its competitive power because it is a fourth-order system [50].

The symmetrical half-bridge topology with the synchronous rectifier (Figure 1.11(b)) is another widely-used approach for this application. With a power stage transfer function very similar to a two-phase interleaving buck converter, the symmetrical half-bridge can utilize the control methods for a buck converter and deliver energy quickly.

Another interesting topology for 48V VRM is the push-pull forward converter, proposed by CPES in 1998. As shown in Figure 1.11(d), it is basically a push-pull converter (Figure 1.11(c)) with a clamp capacitor to clamp the voltage overshoot and to recover the transformer leakage energy. This topology also provides a reduced input current ripple and requires a smaller input filter.

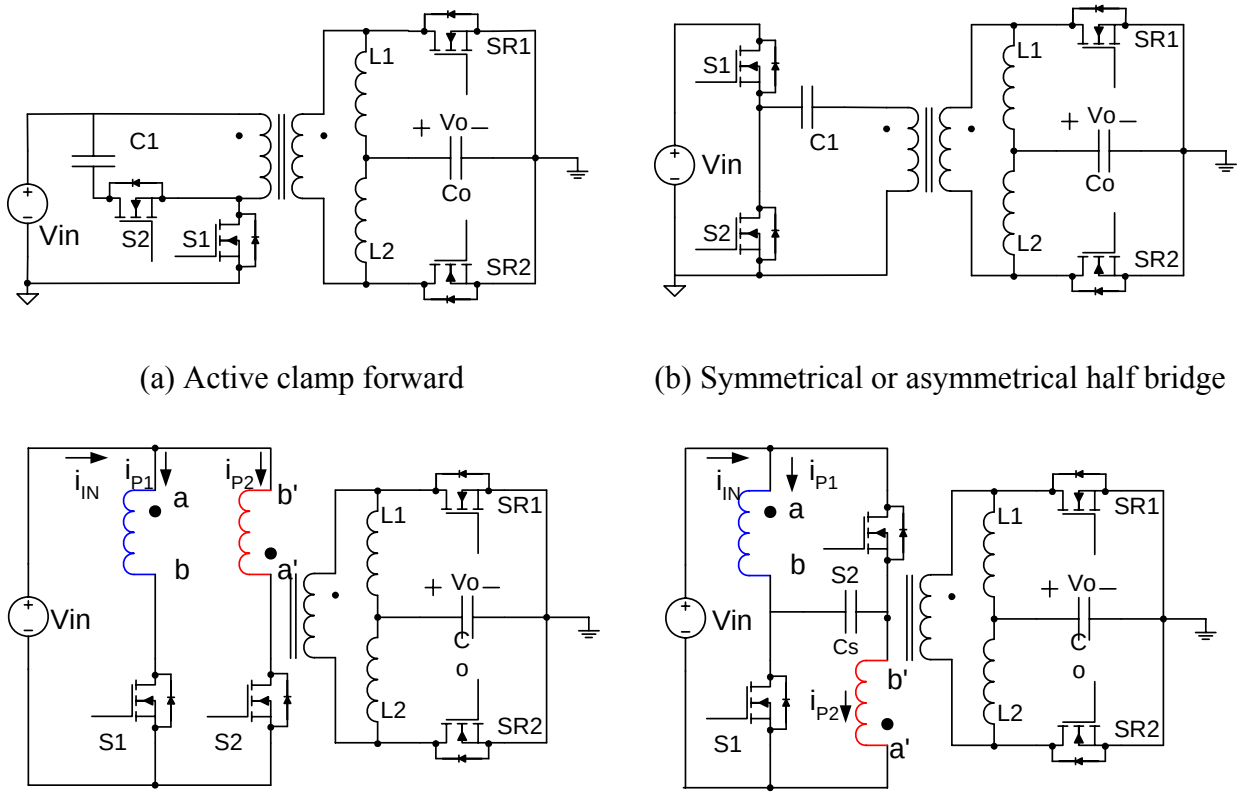


Figure 1.11 Hard-switching topologies for 48V isolated VRMs

The selection of the secondary-side topology is also critical because the secondary-side conduction losses have a major impact on efficiency for low-voltage and high-current applications. Because of its simpler transformer structure and two-times-lower inductor currents and transformer secondary currents, the current-doubler topology can offer lower conduction losses than the conventional center-tapped or forward-type rectifiers [37, 39-42, 45-49].

The topologies listed in Figure 1.11 are all PWM-type hard-switching isolated topologies. A switching frequency of 100kHz is usually adopted by today's industry to get a good balance between performance and cost. A thorough comparison has been made among these topologies [36]. The push-pull forward converter with integrated magnetics shows better performance than other topologies, as is demonstrated by the measured overall efficiency curves shown in Figure 1.12.

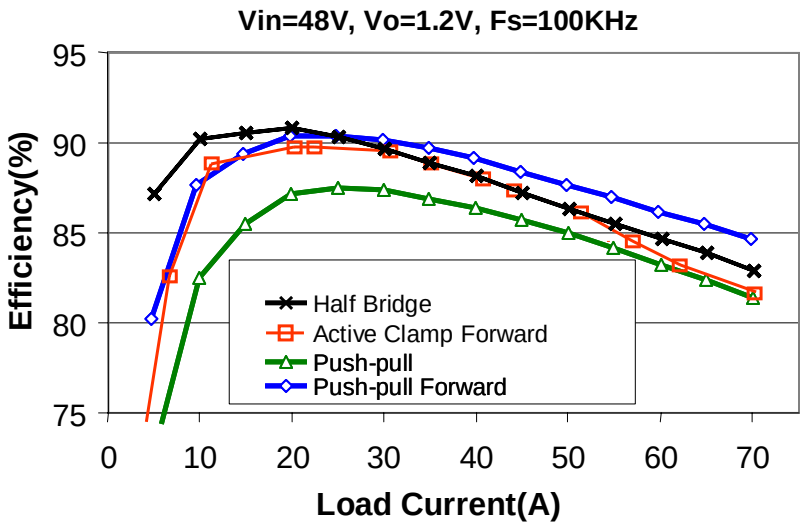


Figure 1.12 Measured efficiency curves of the different isolated topologies

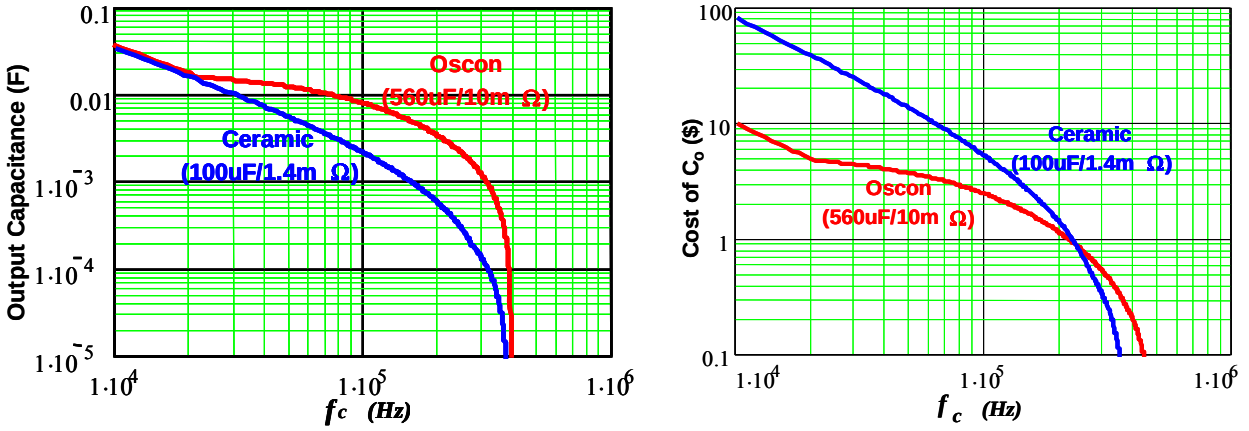
In all, for a 12V VRM, the multi-phase buck seems to be the only topology used by industries; for 48V VRM, there are several choices. All these solutions for today are pretty efficient at a relatively low frequency range.

1.3. Limitations of Today's Approach for Future Processors and the Possible Solutions

In general, whether it's a desktop, which has 12V input non-isolated VRM, or a high-performance server, which has a 48V isolated VRM, today's approach stays around 100-300kHz switching frequency range. There are cost reasons for industry to pick up this frequency range; however, if this approach is followed, by the year 2010, a VRM will employ large numbers of output electrolytic capacitors—approximately 168,000 μF—which is about 2.5 times the value used today, and five times the number of decoupling cavity capacitors in order to meet the processor load line requirement. Obviously, the motherboard cannot accommodate so many bulk capacitors. In terms of cost, the capacitors will cost six times more assuming the price per capacitor stays constant. The motherboard real estate and the capacitor cost are two major roadblocks for the future microprocessor VRMs.

A lot of analysis of the power delivery path and its relationship with the VRM design has been done in order to find a way to reduce the number of capacitors [19]. According to these analyses, the VRM control bandwidth has a dramatic impact on the number of capacitors needed. Figure 1.13(a) shows the total capacitance of bulk capacitors needed to meet future processor requirements as a function of the control bandwidth. Two types of bulk capacitors are evaluated: one is the aforementioned Oscon capacitor; the other is the newly-developed large-value MLCC (100μF/1.4mΩ). The number of both kinds of capacitors can be reduced significantly as the bandwidth f_c increases. The MLCC seems to be able to be reduced more effectively because it has much smaller ESR. However, the price for a 100μF MLCC is even higher than an Oscon capacitor with much larger capacitance (560μF). Considering this factor, the capacitance in Figure 1.13(a) is translated to the total cost of the bulk capacitors, as shown in Figure 1.13(b). One conclusion made by [19] is that when f_c is higher than 200kHz, using an MLCC as the bulk capacitor will have both cost and footprint benefits. In Figure 1.13, there is another piece of important information: the bulk capacitors can eventually be eliminated when the bandwidth reaches 330kHz.

Further increasing the bandwidth can even help to reduce the cavity capacitors, as shown in Figure 1.14. From point A to point B, the bandwidth changes from 330kHz to 650kHz.



(a) Capacitance vs. bandwidth (b) Cost vs. bandwidth

Figure 1.13 Bulk capacitors for future processors

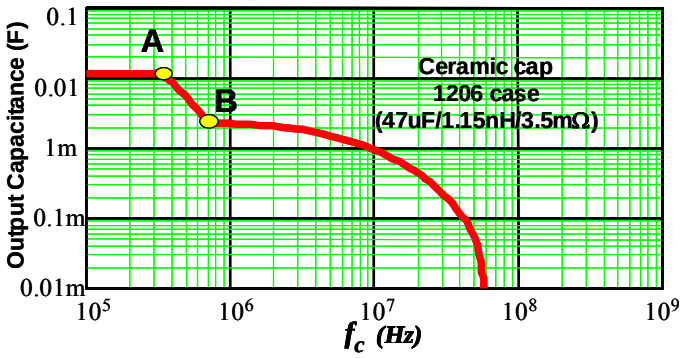


Figure 1.14 Cavity capacitance vs. bandwidth

Meanwhile, the cavity capacitance reduces by almost five times. However, continuously increasing f_c beyond 650kHz will not help too much unless it can be pushed into the tens of MHz range. The reason for this is that the ESL of the capacitor now becomes the dominant factor determining the capacitor number.

Based on these analysis results, the only possible solution for future VRMs is to increase the control bandwidth. The most straightforward method of doing this is to run the converter at a higher switching frequency. Common sense tells us that the higher the switching frequency, the larger the switching losses will be. On the other hand, the higher load current demand causes larger conduction losses as well. All these loss increases make balancing the already tight thermal budget an impossible task.

1.4. Technical Barriers for High-Frequency, High-Current VRMs

In order to identify the barriers for high-frequency high-current VRMs, an accurate loss breakdown is crucial. This is accomplished by FEA simulation. The device model is given by device vendors in a form of physical dimensions and doping densities. The parasitic inductance and resistance are extracted from a layout by Maxwell simulations. A scaled-down buck converter with Renesas Generation8 devices was built as shown in Figure 1.15. Table 1.2 lists the circuit specifications.

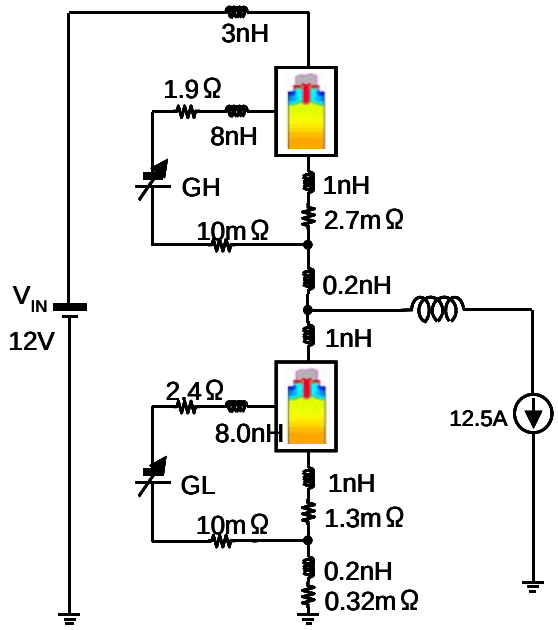


Figure 1.15 FEA simulation circuit with physical device models and circuit parasitics

Table 1.2 Circuit specifications

Switching frequency	300kHz	1MHz
Input voltage	12V	12V
Output voltage	1.3V	1.3V
Load current	12.5A	12.5A
Output inductor	667nH	200nH

The loss breakdown shown in Figure 1.16 clearly shows that the top switch turn-off loss is the dominant loss bar as a result of increasing the switching frequency. The bottom switch conduction loss is the second dominant bar due to the large load current.

Similar situations exist in the 48V isolated VRMs. Take the symmetrical half-bridge as an example: when the switching frequency is pushed from 100kHz to 500 kHz, the efficiency drops dramatically (around 10%) at 1.2V/70A output. Loss analysis indicates that high switching loss, high body-diode loss, and high SR gate driving loss are three major switching-frequency-related losses. In addition, large conduction losses also have a big impact on system efficiency (Figure 1.17).

This dissertation focuses on overcoming the barriers of today's state-of-the-art technologies and to propose novel concepts enabling high-frequency, high-current density VRMs for future microprocessors.

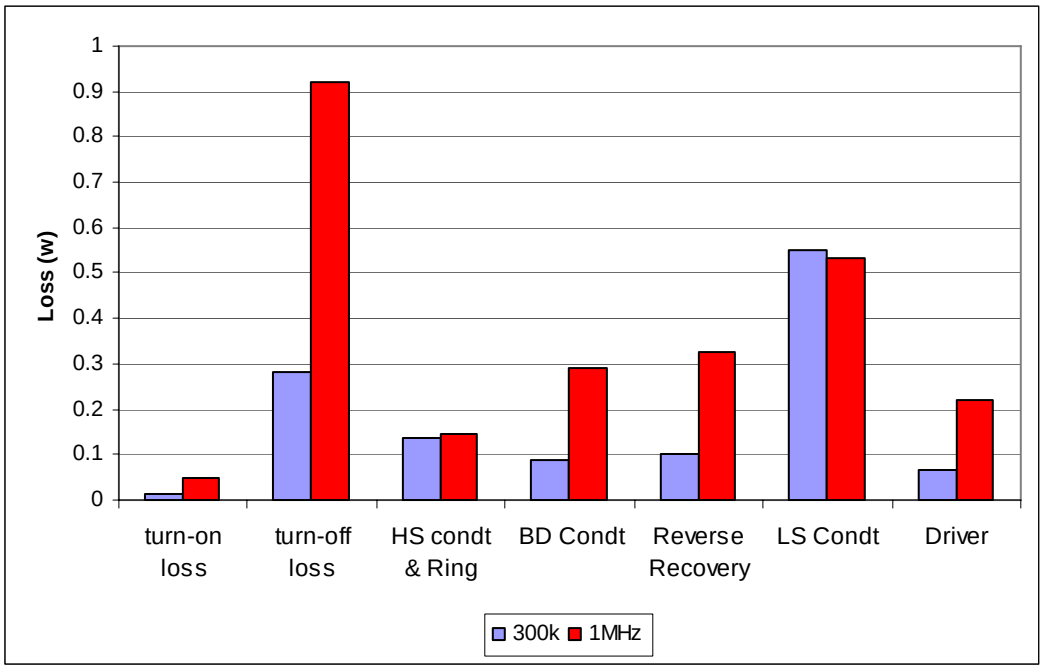


Figure 1.16 Loss breakdown of a buck converter running at 300kHz and 1MHz

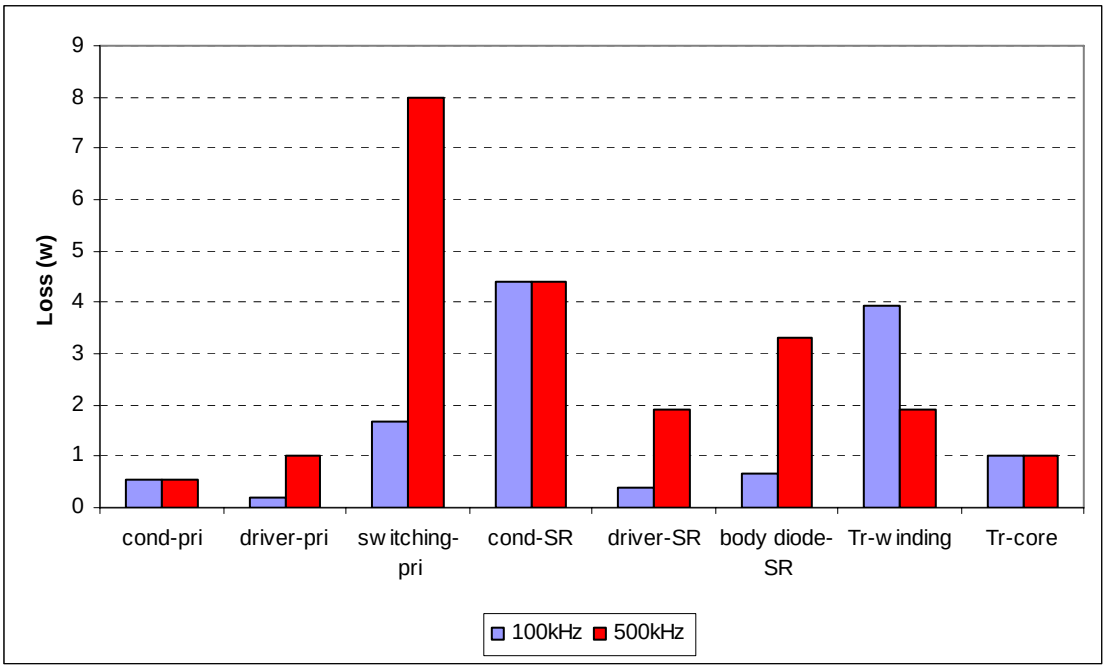


Figure 1.17 Loss breakdown of a symmetrical half bridge converter running at 100kHz and 500kHz

1.5. Dissertation Outline

This dissertation consists of five chapters organized as follows:

Chapter 1 gives an introduction of the research background. As a very special DC-DC converter, VRM design must follow the fast-developing trend of microprocessors. The design challenges are the high current, high di/dt, and stringent load-line requirement. For 12V non-isolated VRM, the multiphase synchronous buck converter is so far the best choice for today's VRM. For the 48V isolated VRM, there are several topologies available; all of these are based on isolated topologies with the current doubler and the synchronous rectifier. When the energy is transferred from the input of a VRM, through the VRM, then through the power delivery path to the processor, it needs sufficient capacitors to relay this energy. Those capacitors' cost appears to be the most significant cost in a VRM. Studies already completed show that there is a close relationship between the VRM's designed control bandwidth and those capacitor numbers. To run a VRM at a higher switching frequency becomes the most important objective of this research. However, the degradation of efficiency makes the conventional buck converter and the hard-switching isolated topologies incapable of operating at a higher frequency. The research

goal is determined: to develop novel means that can help a high-output-current VRM run efficiently at high frequency.

In Chapter 2, concepts for high-frequency, high-current 48V isolated VRMs are proposed. It starts from how to tackle the highest loss bar, the switching loss. Zero-Voltage-Switching (ZVS) is the preferred method for effectively reducing the switching loss. The consequence is additional conduction loss on top of the already high conduction loss due to the high current. A novel Complementary Controlled Bridge (CCB) self-driven concept is proposed to solve this dilemma. With the proposed self-driven scheme, the combination of the ZVS technique and the self-driven technique recycles the gate driving energy by making use of the input capacitor of the secondary-side synchronous rectifier (SR) as the snubber capacitor of the primary-side switches. Compared to the external driver, the proposed converter can save driving loss and synchronous rectifier body diode conduction loss. Additionally, compared with the existing level-shifted self-driven scheme for bridge-type symmetrical topologies, its gate signal ringing is small and suitable for high-frequency applications.

Although the CCB self-driven VRM reduces the switching frequency related losses significantly, the conduction loss is still high. Inspired by the current-doubler concept, a novel ZVS current-tripler DC-DC converter is proposed in this chapter as well. By utilizing more SR devices to share the current during the freewheeling period, the SR conduction loss is reduced. The current-tripler DC-DC converter has a delta/delta connected transformer that can be implemented with integrated magnetics. The transformer then becomes an integrated magnetic with distributed windings, which is preferred in high current applications. The current-tripler DC-DC converter in fact meets the requirements for the CCB self-driven sceme. The two concepts are then combined with an integrated gate drive transformer.

In Chapter 3, the application of the proposed CCB self-driven scheme to the 12V non-isolated VRM is discussed first. The proposed topology is basically a buck-derived soft-switching topology with duty cycle extension and SR device self-driven capabilities. Because there is no isolation requirement, the SR gate driving becomes so simple that the voltage at the complementary controlled bridge can be used to directly drive the SR gate. Both the gate driving loss and the SR body diode conduction loss are reduced. The proposed circuit achieves similar overall efficiency to a conventional 300kHz buck converter running at 1MHz.

There are several derivative circuits proposed in Chapter 3 following the CCB self-driven concept. One is the autotransformer version of the circuit, mainly designed to deal with the transformer winding loss. Another derivative circuit integrates the output filter inductors with the transformer.

The proposed current-tripler DC-DC converter can also be extended to the 12V non-isolated VRMs. The derivation from the isolated current-tripler to the non-isolated current-tripler is discussed. There are two ways to drive its synchronous rectifiers. The first method is to drive externally, which is simple to implement but dissipative. The other method is to use the CCB self-driven scheme. In order to meet the requirements of the CCB self-driven method, we have to modify the non-isolated current-tripler to an autotransformer version. The SR driver loss is lower than the first method, but an additional level shift circuit is needed in the driving path, which somewhat increases the complexity.

The circuits proposed in Chapter 2 and Chapter 3 have one feature in common: their output inductors are equivalent to those in buck converters (two or three phases). It has already been demonstrated in [74] that the use of integrated coupling inductors between the interleaving channels of a buck converter can improve both the steady-state efficiency and dynamic performances. The essence of the coupling inductors concept is to provide different equivalent inductances for the steady state and the transient. It is straightforward to apply the coupling inductors concept to various topologies proposed in Chapter 2 and Chapter 3 to improve performance. In Chapter 4, more benefits are discovered when a current loop becomes necessary to achieve Adaptive Voltage Positioning (AVP) as well as proper current sharing among phases. The current loop sample hold effect is alleviated by the coupling L concept. A small-signal model is proposed to study the system dynamic performance difference with different coupling inductor designs. As verification, the coupling concept is applied to the 12V non-isolated CCB self-driven VRM and the bandwidth as high as one-third of the switching frequency is achieved, which means a significant output capacitor reduction.

Chapter 4 also gives the derivation of the small-signal model for the current-tripler case. Similar benefits can be obtained by coupling the inductors. The last chapter summarized the dissertation and proposes some ideas for future work.

Chapter 2. High-Frequency High-Current 48V Isolated VRMs

Most of today's power pods use pulse width modulation (PWM) hard-switching topologies with synchronous rectifiers (SR), such as the symmetrical or asymmetrical half bridges, active clamp forward, push-pull, push-pull forward, etc. All of these are efficient at relatively low switching frequencies, such as 100kHz.

However, when the switching frequency is pushed to 500 kHz, the efficiency drops dramatically (around 10%). Loss analysis in Figure 1.17 indicates that high switching loss, high body diode loss, and high SR gate driving loss are three major switching-frequency-related losses. In addition, large conduction losses also have a big impact on system efficiency.

Because none of these hard-switching 48V PWM topologies are able to achieve high switching frequency, a large transformer as well as large output inductance and capacitance must be used, which results in a large footprint and high cost.

The phase-shifted full-bridge then becomes an attractive alternative because it can achieve zero voltage switching to minimize the switching loss [35], as shown in Figure 2.1. The circuit itself resembles the conventional hard-switching full-bridge converter with a current doubler rectifier. The difference is the control of the primary switches: each leg has 50% duty cycle

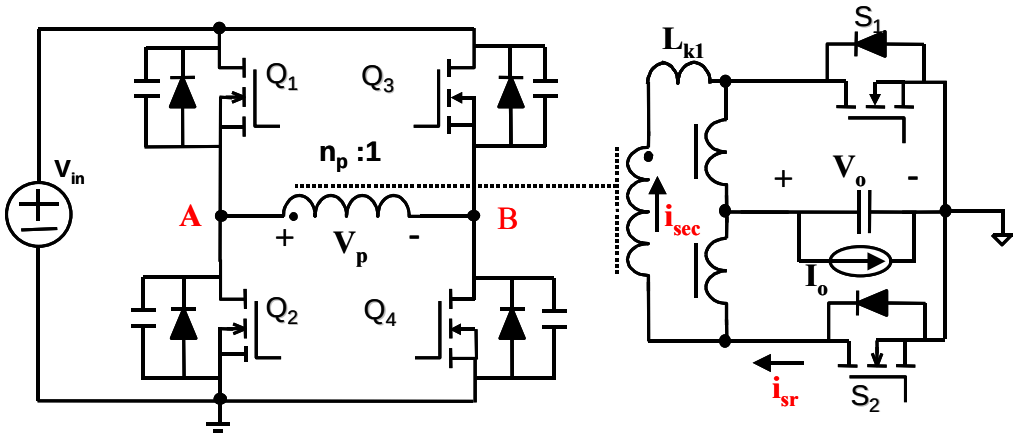


Figure 2.1 Phase-shifted full-bridge dc-dc converter with current doubler rectifie

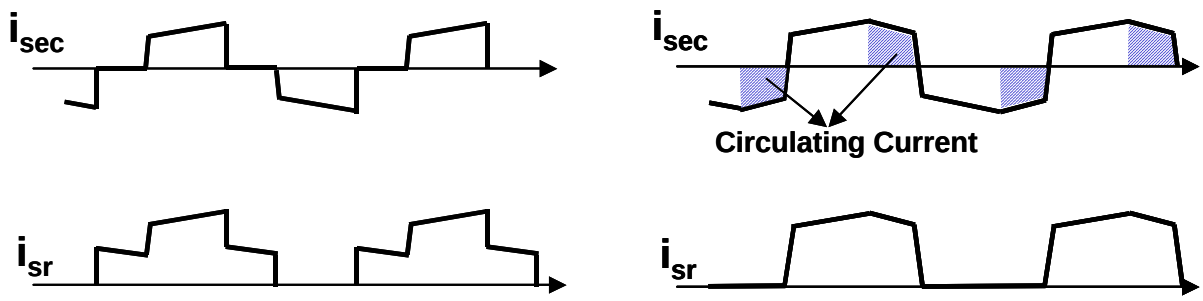


Figure 2.2 the transformer winding current and SR current for the symmetrical hard-switching converter and the phase-shifted full-bridge converter

while the output is regulated by the phase shifting between the two legs. However, there is a circulating energy stored in the transformer leakage inductor that will cause larger conduction loss on the transformer windings and the SRs. Figure 2.2 (a) and (b) show the transformer winding current and SR current for the symmetrical hard switching converter and the phase-shifted full-bridge converter, respectively. One possible solution to this problem is to drive the SR with higher gate voltage, such as 10V. The consequence is the increased gate drive loss, which is also a function of the switching frequency.

The self-driven technique appears to be the remedy for the aforementioned issues [55-60]. A typical self-driven scheme can partially recover the gate drive loss. additionally, due to its "self-adaptive" feature, the SR body diode conduction time can be reduced. Moreover, a self-driven circuit is usually simpler than the external-driven scheme, especially in the 48V isolated case.

In this chapter, a complementary controlled bridge (CCB) self-driven concept is proposed, which can be applied to the existing soft switching topologies so that not only is the switching loss dramatically reduced, but the body diode loss and gate driver loss are also reduced. A current-tripler DC-DC converter is then proposed to further improve the system efficiency by reducing the conduction losses. The derivations of the concept are discussed, and the benefits of the concepts in typical applications are theoretically and experimentally verified.

2.1. Limitations of the Conventional Self-Driven Schemes

Self-driven synchronous rectification has proven to be an effective method of driving the secondary-side SRs. Cross-coupling the gates of the SRs to the main power transformer to

realize the gate drive signal is the simplest way of driving the secondary-side SRs[56, 59]. Figure 2.3 shows a conventional cross-coupling self-driven active clamped forward converter. The transformer leakage inductance is represented by a lumped inductance, L_{leak}, in series with the secondary side winding. Because of L_{leak}, the current through S_1 as well as the secondary side winding i_{s1} cannot change instantaneously, which leads to the commutation time between S_1 and S_2, as t_1 and t_2 shown in Figure 2.4. The dead time between G_{s1} and G_{s2} causes the body diode

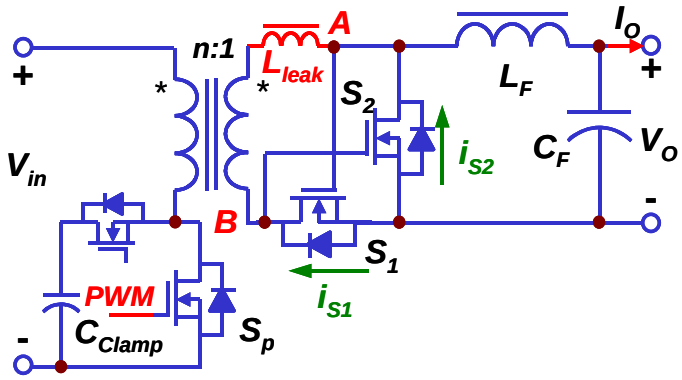


Figure 2.3 A conventional cross-coupling self-driven active clamped forward converter

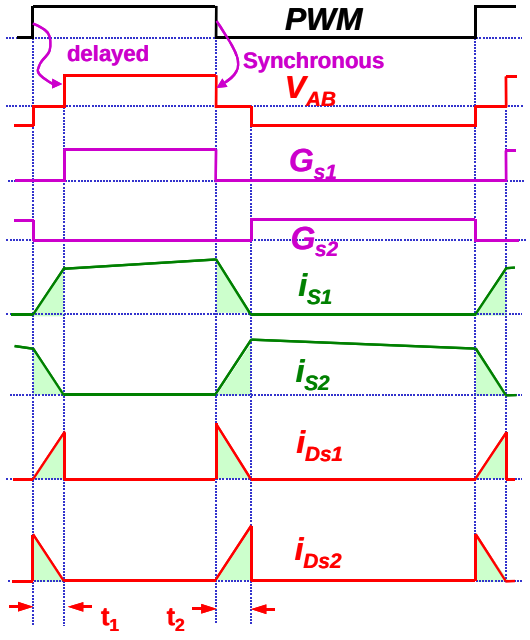


Figure 2.4 Key waveforms of the circuit in Figure 2.3

conduction that is not acceptable in high-frequency DC-DC converters. There is another problem with cross coupling the SR gate drive signals: when the output voltage of the converter is a low voltage, such as 1V, the voltage across the secondary winding of the transformer is not high enough for the SRs.

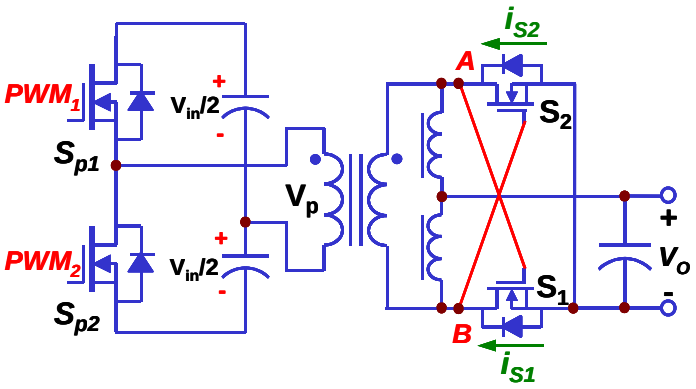


Figure 2.5 A symmetric half-bridge converter using simple cross-coupling self-driven scheme

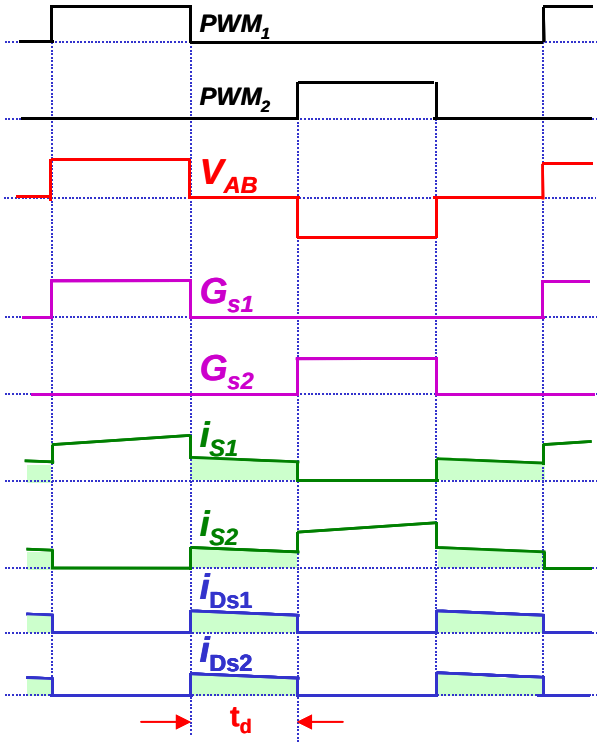


Figure 2.6 The switching waveforms of the circuit in Figure 2.5

For a symmetric topology, such as the symmetric half-bridge converter shown in Figure 2.5, the simple cross-coupling self-driven concept has one more problem. Here we exclude the

body-diode conduction due to the leakage inductance, which is the same as the previous case. Figure 2.6 shows its switching waveforms. During the dead time t_d, there is no voltage across the transformer. The gate voltages of both SRs are zero, resulting in the body diodes conducting.

One solution to this problem is the level-shifted self-driven concept proposed by J. Cobos as shown in Figure 2.7 [57]. Two diodes, D_1 and D_2, and one driver winding, W_{dr}, are added to level-shift the gate voltage during the dead times. W_{dr} is coupled to the power transformer TR. Its waveforms are shown in Figure 2.8, which unfortunately illustrate that this configuration still has several problems. First of all, during dead time, the gate source voltages of the SRs are much lower than during the other time periods, so larger conduction loss is unavoidable. Secondly, whenever PWM_1 or PWM_2 changes from a high to a low level, the transformer voltage will see an oscillation that will cause unwanted turnoff of the SR devices. These issues prevent the level-shifted self-driven concept from being used in high-frequency applications.

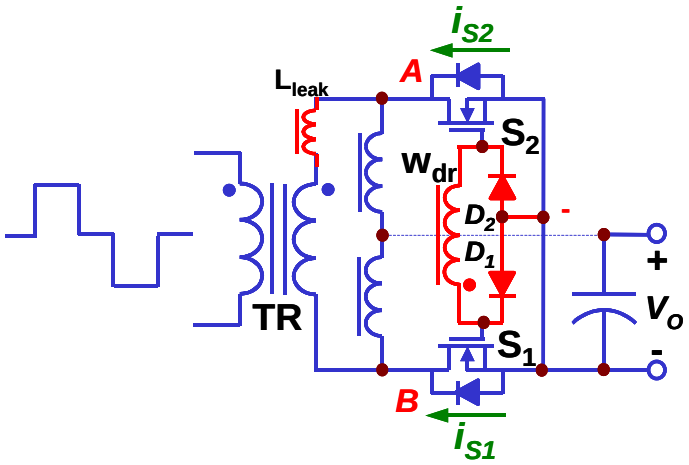


Figure 2.7 The level-shifted self-driven concept proposed by J. Cobos

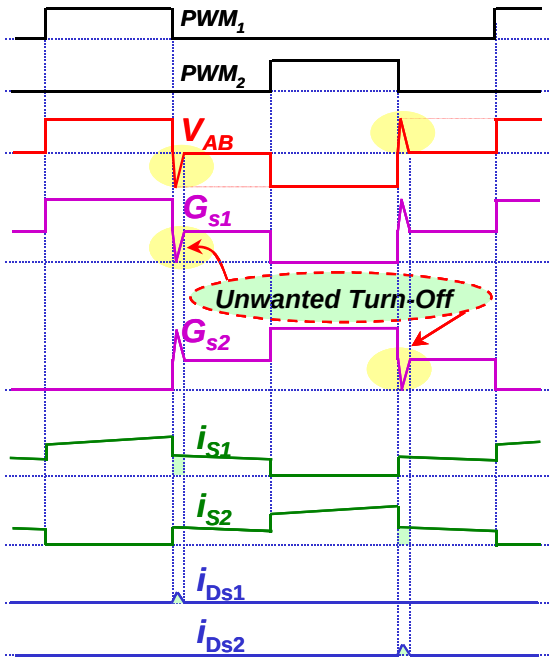


Figure 2.8 The switching waveforms of the level-shifted self-driven concept

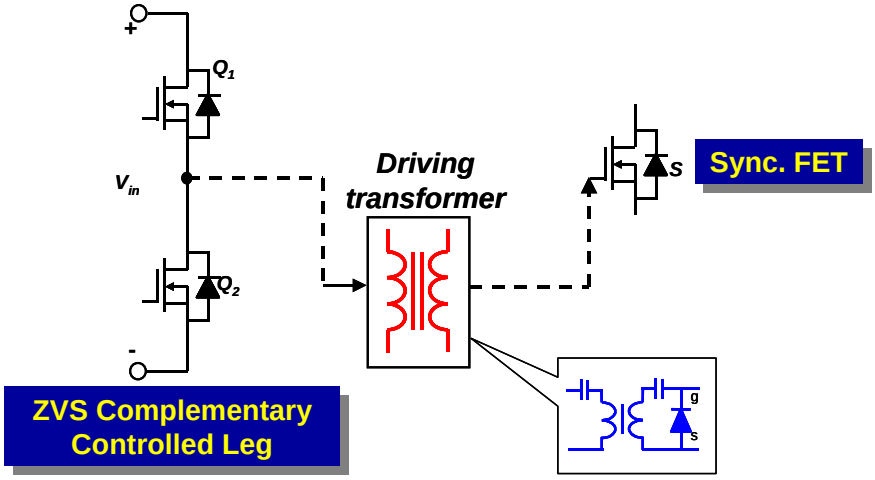


Figure 2.9 Complementary Controlled Bridge (CCB) self-driven concept

All these self-driven schemes have a common feature: The driving source is from the power transformer windings, which either directly use the power transformer windings or couple auxiliary driver windings to the power transformer windings. This feature inevitably causes the aforementioned problems.

This dissertation proposed a novel Complementary Controlled Bridge (CCB) Self-driven scheme, as conceptually shown in Figure 2.9. Unlike the conventional self-driven methods, here

the gate drive source is obtained from a complementary controlled bridge. Because using complementary control can easily achieve Zero Voltage Switching (ZVS), the voltage waveform at the bridge middle point is free of ringing, and so is ideal for driving the SRs. Furthermore, the input capacitor of the SR partially serves as a snubber capacitor for the ZVS complementary controlled bridge.

In the following section, this CCB self-driven scheme will be applied to 48V isolated VRMs. Because of the isolation barrier of the driver transformer, the leakage inductance of this transformer will have an impact on the driver performance, such as the gate-to-source voltage ringing, body diode conduction time, the gate driving loss, etc. The analysis of these issues will be given after the circuit operating principle is illustrated.

2.2. CCB Self-Driven Technology in 48V Input Isolated Topologies

2.2.1. Operating Principles

A typical application of the CCB self-driven concept is as part of a full-bridge configuration with a current-doubler rectifier, as shown in Figure 2.10. Its control strategy is shown in Figure 2.11. For each leg of the primary side, the control is asymmetrical. But for the main transformer, the voltage is still symmetrical. Therefore, this control has the same transient response performance as the phase-shifted and other symmetrical PWM controls. The detailed operation principle is illustrated in Figure 2.12.

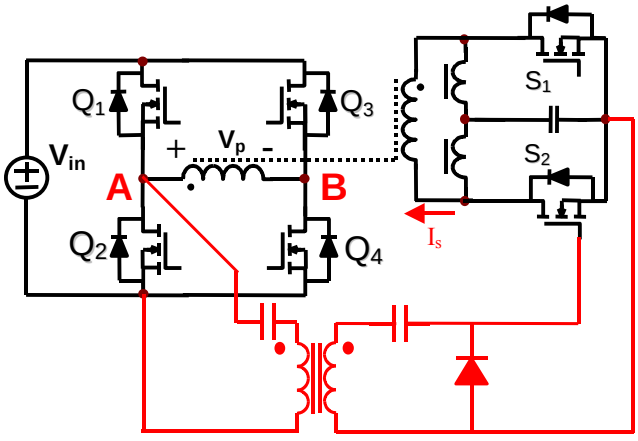


Figure 2.10 Proposed self-driven ZVS full-bridge converter

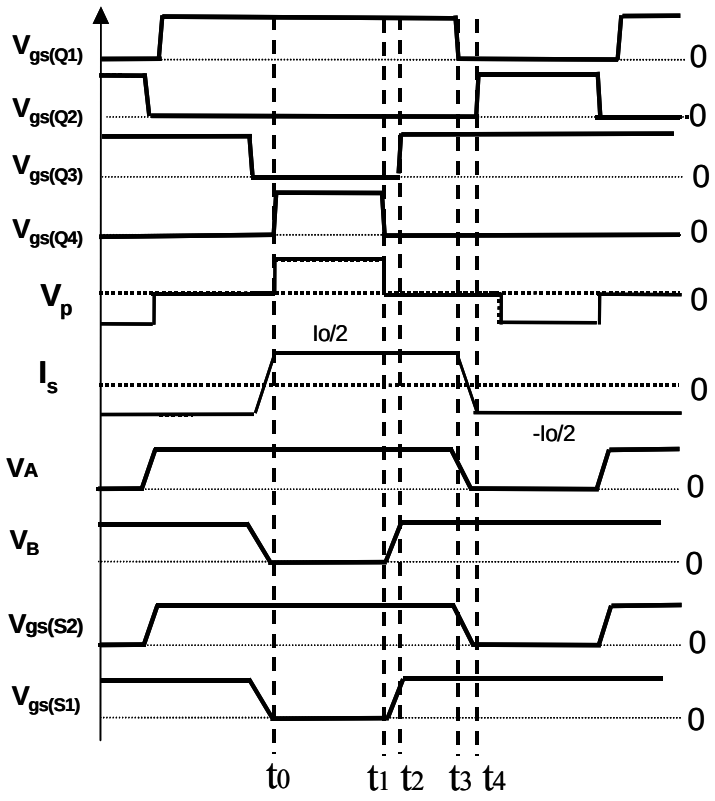
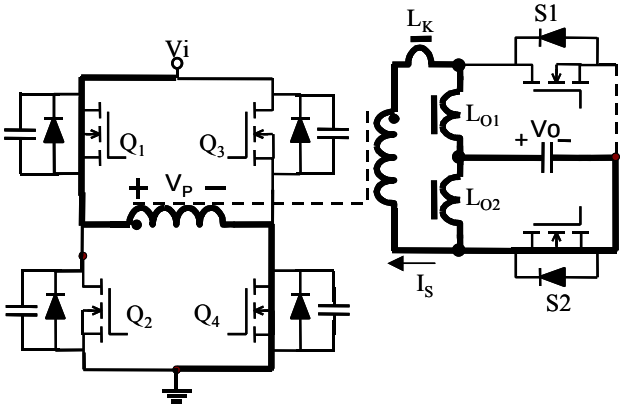


Figure 2.11 Control strategy of proposed self-driven ZVS full-bridge converter

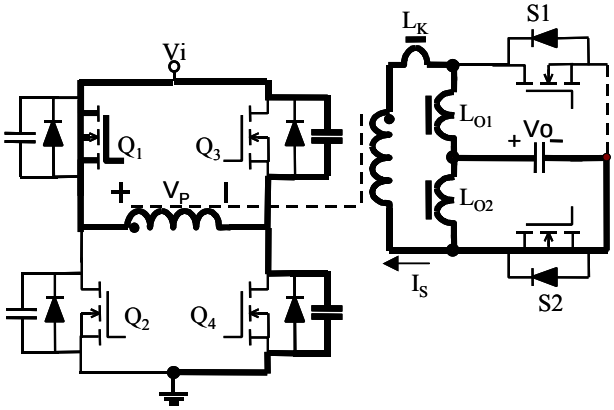
In mode 1 (t0-t1), Q1 and Q4 are on, and S1 is off. The energy is transferred from the primary side to the output, which is the same as in the conventional phase-shifted full-bridge (PS-FB) converter.

In mode 2 (t1-t2), Q4 turns off at t1, and the reflected output current discharges and charges the output capacitor of Q3 and Q4, respectively. Given a suitable dead time, ZVS can be achieved. This mode is the same as the ZVS realization of the leading leg of the conventional PS-FB converter.

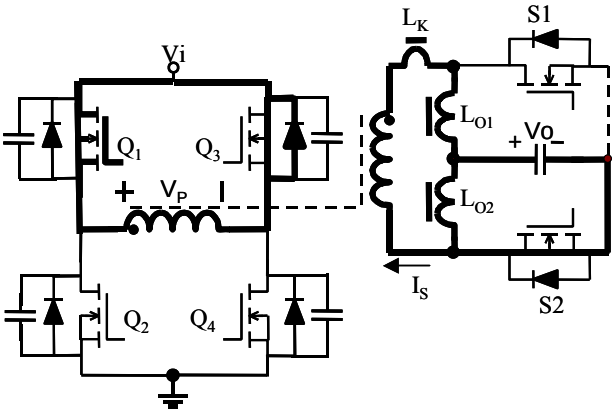
In mode 3 (t2-t3), the energy stored in the leakage inductor of the transformer freewheels through Q1 and Q3.


Vi
Q1
Q3
VP
Q2
Q4
LK
S1
LO1
Vo
LO2
IS
S2

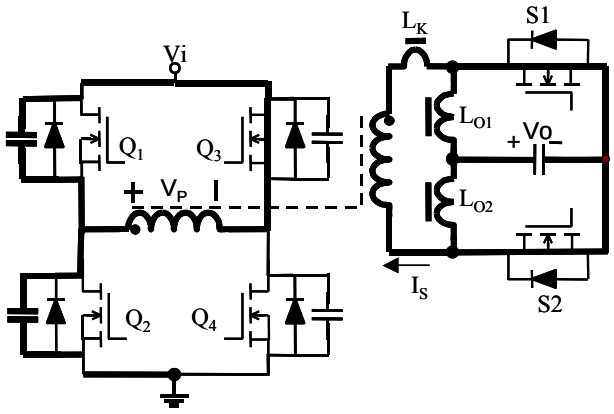
(a)


Vi
Q1
Q3
VP
Q2
Q4
LK
S1
LO1
Vo
LO2
IS
S2

(b)


Vi
Q1
Q3
VP
Q2
Q4
LK
S1
LO1
Vo
LO2
IS
S2

(c)



(d)

Figure 2.12 Operation modes of ZVS self-driven FB: (a) mode 1 (t0~t1), (b) mode 2 (t1~t2), (c) mode 3 (t2~t3), and (d) mode 4 (t3~t4).

In mode 4 (t3-t4), Q1 turns off at t3. The leakage inductor of the transformer resonates with the output capacitors of Q1 and Q2. At certain load conditions, energy stored in the leakage inductor is high enough to achieve ZVS for Q2. This mode is the same as the ZVS realization of the lagging leg of the conventional PS-FB.

After t4, another half period starts, and the operation principle is the same except for polarity changes. From the description of the operation principles, it is obvious that this asymmetrical control strategy still achieves ZVS for the primary switches, which is very important for high-frequency applications.

2.2.2. Implementation of the Self-Driven Scheme

Figure 2.11 shows that the gate signal for SR is the same as the voltage waveform at point A or B, and so the signal and energy from these points can be used to drive the SRs. Taking the Q3-Q4-bridge as an example, a traditional level-shifted gate drive scheme that can transfer a wide range of duty cycles is shown in Figure 2.13. C_{oss3} and C_{oss4} represent the output capacitors of Q3 and Q4 respectively. C_s is an additional snubber capacitor that is commonly seen in ZVS type converters. C_{bp} is the input side dc blocking capacitor with a bias voltage Vin*D. The purpose of C_{bs} is to level-shift the transformer secondary voltage so that the gate voltage has the same waveform as V_B. Usually a diode D_g is parallel with the gate to provide a charging path for C_{bs} during the Q3 off period.

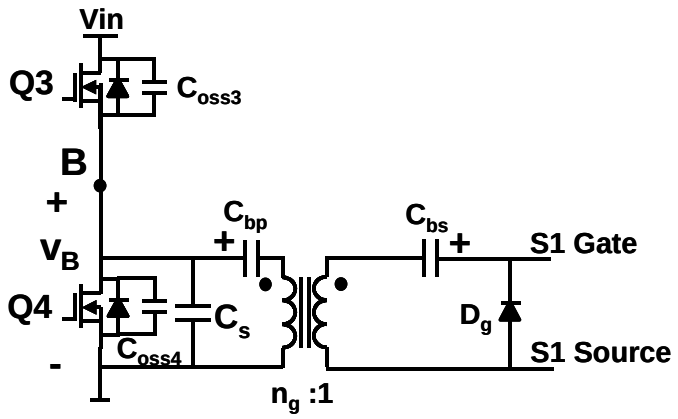
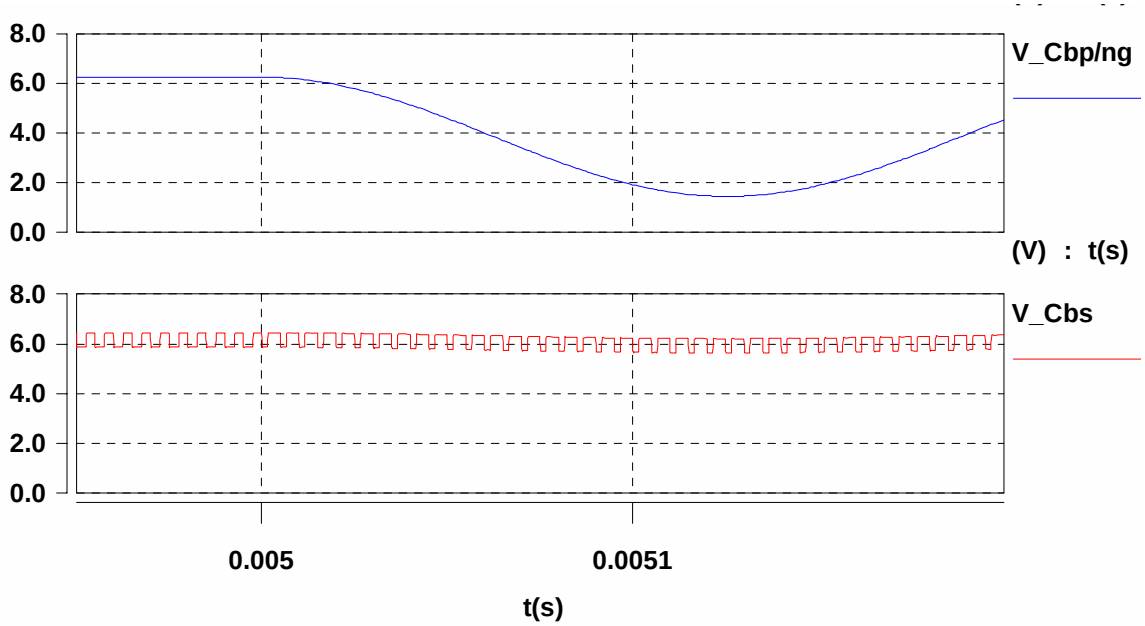


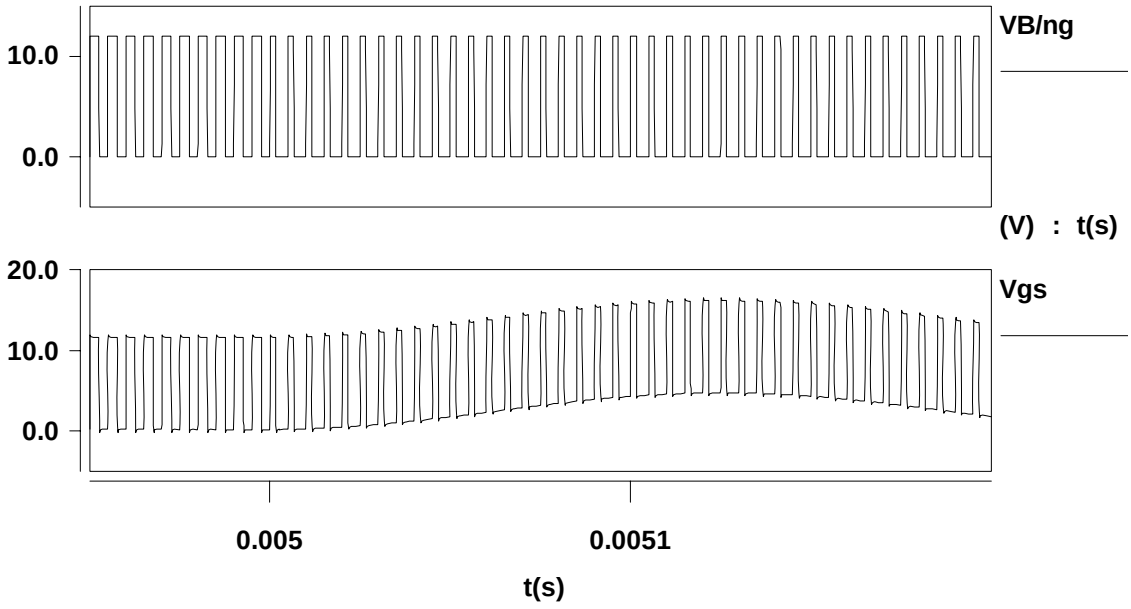
Figure 2.13 Level-shifted driving scheme used in the isolated topologies

When the duty cycle of V_B falls during the step-down transient, for example, from D1 (=0.5) to D2 (=0.3) at time t (=5ms), the voltage across C_{bp} will change from V_{in}*D1 to its new steady state, V_{in}*D2. This excites an oscillation between C_{bp} and L_m, the magnetizing inductance of the driver transformer. The peak-to-peak amplitude will be $2*V_{in}*(D1-D2)$. However, on the secondary side, C_{bs} lacks a current path to discharge it, thus its voltage stays unchanged (Figure 2.14(a)). This mismatch between the bias voltages across C_{bp} and C_{bs} causes severe problems, as shown in Figure 2.14(b). The SR gate voltage fluctuates during the transient and the SR cannot be turned off properly.

To solve this problem, a new driver scheme is proposed, as shown in Figure 2.15. A small MOSFET, T_g (TSOP-6 package), replaces the diode D_g in Figure 2.13, and a third winding is used to drive it. During the Q4 on time, the bias voltage across C_{bp} will cause T_g to be on, which causes C_{bs} to be parallel with C_{bp}, and the voltage across C_{bs} can follow that across C_{bp} instantaneously. Because the gate of T_g sees a negative voltage during its off time, a low-threshold MOSFET is preferred in order to guarantee turning on when C_{bp} has a very low bias voltage. Adding T_g also provides fairly low gate-to-source impedance during the SR off period to avoid any false trigger due to the Miller effect. The simulation waveforms in Figure 2.16(a) show that the bias voltages across C_{bp} and C_{bs} match well after a sudden duty cycle change. The SR gate voltage duplicates the input voltage V_B all the time, as shown in Figure 2.16(b).



(a) Voltage across C_{bp} (top) and across C_{bs} (bottom)



(b) Input signal V_B (top) and gate voltage V_{gs} (bottom)

Figure 2.14 Waveforms of the driver shown in Figure 2.13

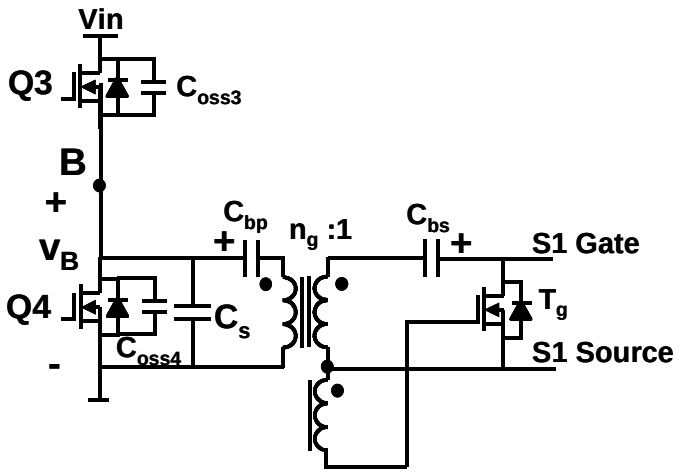
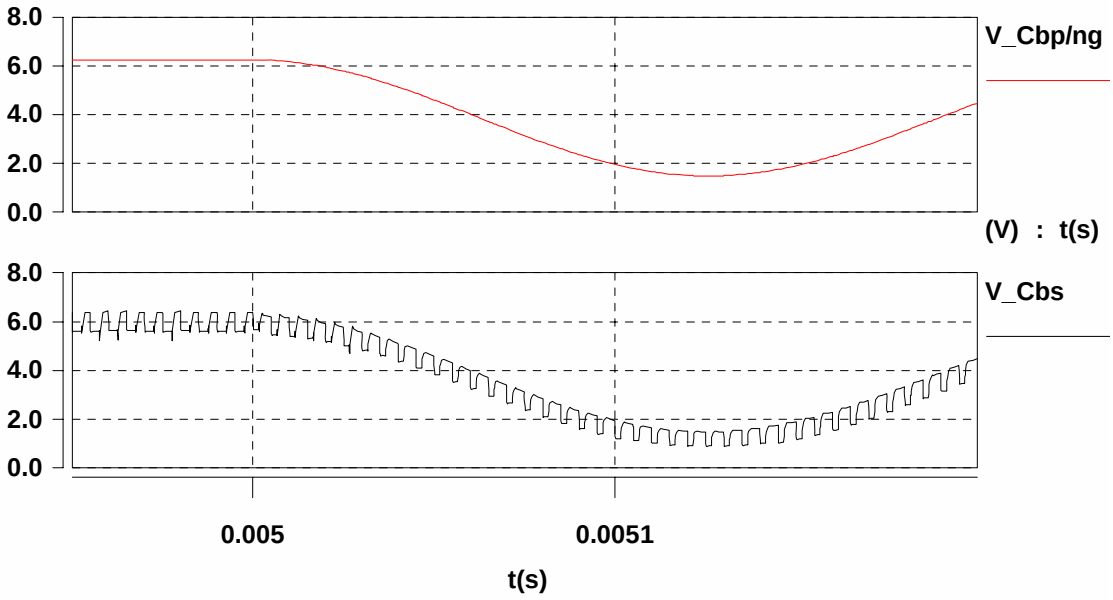
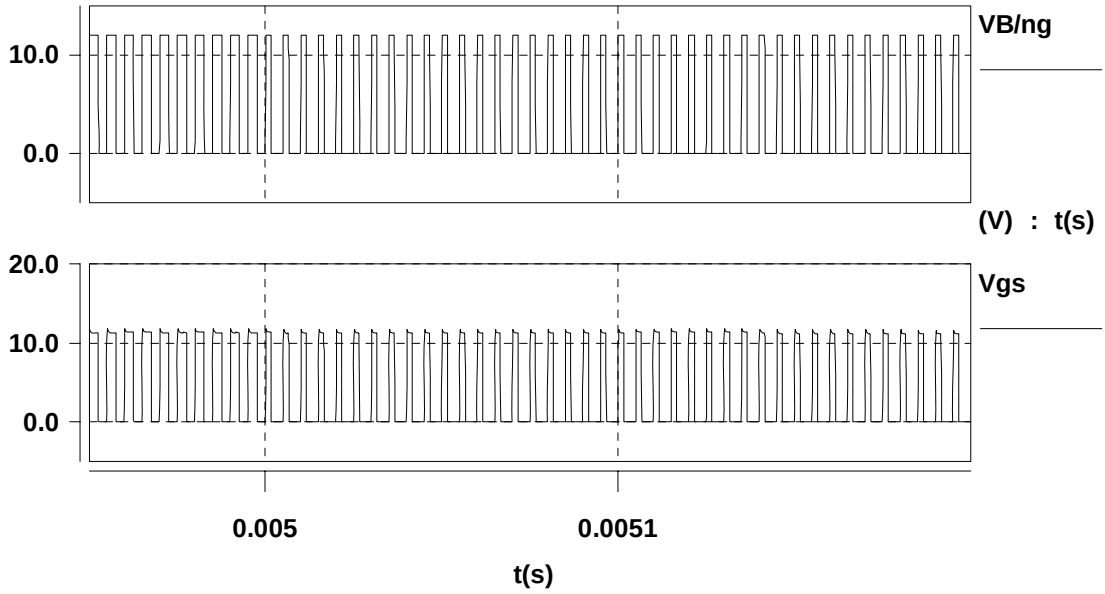


Figure 2.15 Proposed self-driven circuit for the ZVS FB topology



(a) Voltage across C_{bp} (top) and across C_{bs} (bottom)



(b) Input signal V_B (top) and gate voltage V_{gs} (bottom)

Figure 2.16 Waveforms of the driver shown in Figure 2.15

Besides the full-bridge converter, the proposed self-driven method can also be applied to any other asymmetrically-controlled topologies, such as the active-clamped forward (Figure 2.17), forward-flyback and asymmetrical half-bridge topologies (Figure 2.18). The secondary side can be a current doubler, a half-wave rectifier or a center-tapped rectifier. The cross-coupled

structure can be applied in the proposed self-driven topology, and unlike the self-driven application in the full-bridge converter, no additional windings are needed to deal with the transient issue.

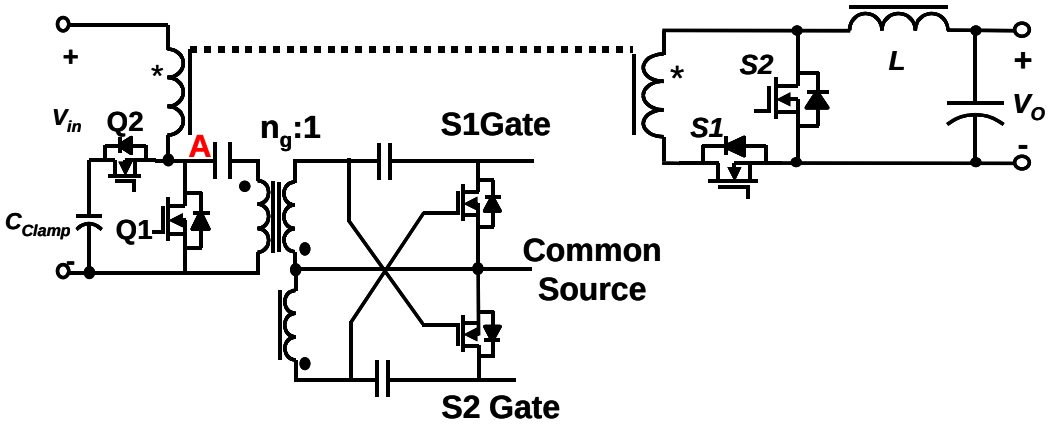


Figure 2.17 Active-clamped forward converter with the proposed driver scheme

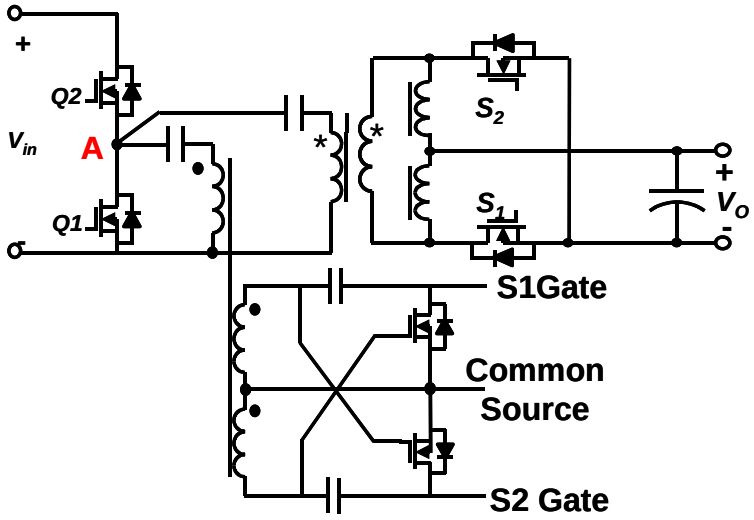


Figure 2.18 Asymmetrical half-bridge converter with the proposed driver scheme

2.2.3. SR Gate Voltage Ringing Analysis

The addition of the driver transformer leakage and parasitic trace inductances may cause an oscillation between the leakage inductors and the gate capacitor of the SRs. This gate voltage ringing not only causes reliability problems in the SR devices, but also increases the on

resistance of the SR devices when it resonates back to its valley, as illustrated in Figure 2.19. The ringing occurs only at the rising edge, because the tiny MOSFET across the SR gate and source clamps the ringing at the falling edge. The percentage of the overshoot voltage over the steady state gate drive voltage is used to quantify the ringing, which is:

$$\text{Overshoot} = \frac{V_{ov}}{V_{g_steady}} \times 100\% \tag{2.1}$$

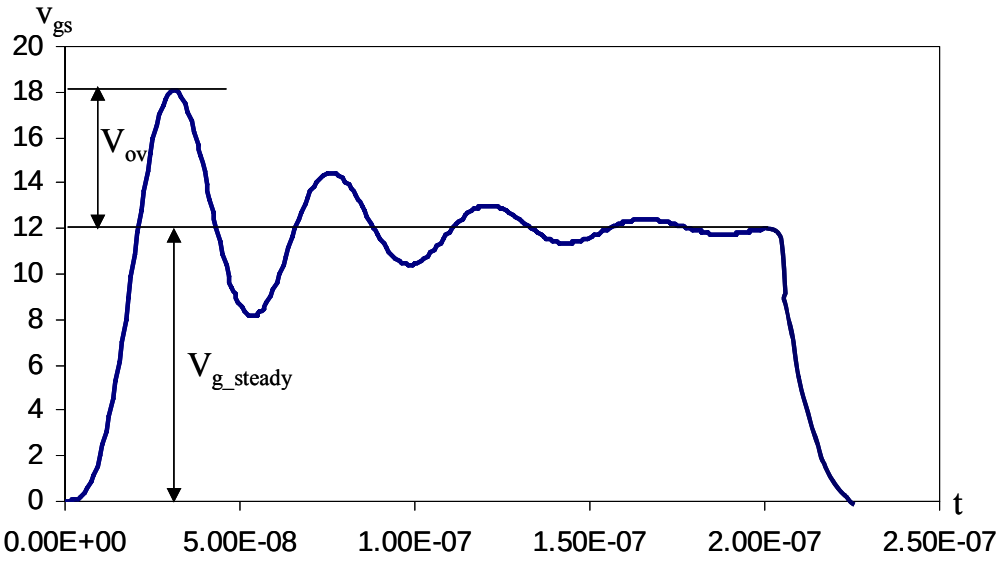
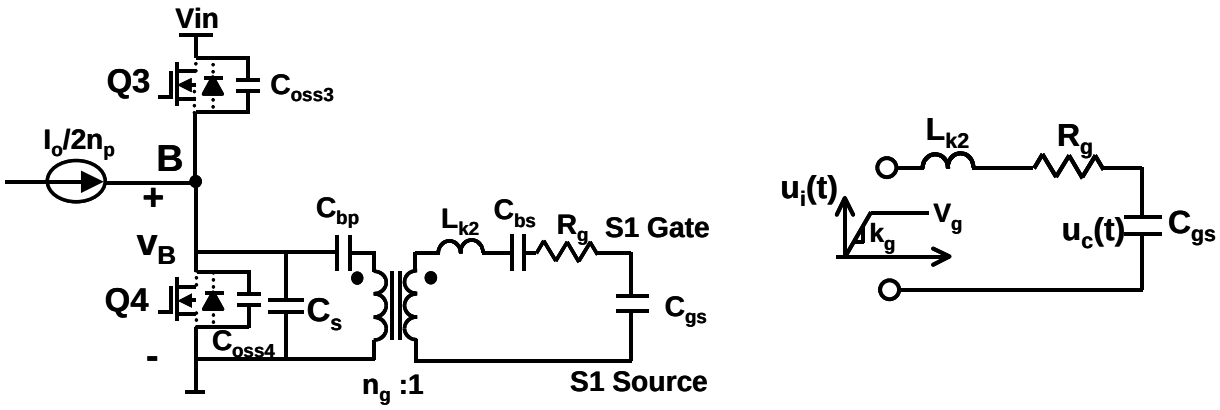


Figure 2.19 SR gate voltage when parasitic inductance and resistance are considered

An additional gate resistor R_g is used to dampen these oscillations, seen in Figure 2.20(a). Since the analysis focuses on SR turn-on interval, the tiny MOSFET T_g has no effect and is not shown in the circuit. The insertion of R_g increases the gate drive loss, which will be discussed in the latter part of the paper. Here, the relationships of the gate voltage overshoot with R_g, L_{k2}, and t_r, the rise-time of the voltage at node B, are analyzed first. In Figure 2.20(a), the voltage at node B, V_B, is actually the input source of the SR gate drive circuit. During the rising edge of V_B, Q_4 turns off. The reflected output inductor current discharges output capacitor of Q_3, C_{oss3}, and charges that of Q_4, C_{oss4}. Meanwhile, the snubber capacitor C_s and the gate capacitor C_{gs} are also charged by this current. The reflected filter inductor has fairly high impedance, and therefore can be modeled as a constant current source. To simplify the analysis, we assume that V_B increases linearly with a slope of k_p, which is:

$$k_p = \frac{I_o}{n_p C_{eff}} \tag{2.2}$$

where I_o is the load current, n_p is the power transformer turns ratio, and C_{eff} is the sum of C_{oss3}, C_{oss4}, C_s and the reflected C_{gs}. Also, the rise time of V_B, t_r, can be calculated as V_{in}/k_p. Now we can stimulate the gate drive circuit using V_B, a ramp step signal. Figure 2.20(b) shows an equivalent circuit when V_B is reflected to the secondary side of the driver transformer in which $k_g=k_p/n_g$, and $V_g=V_{in}/n_g$.



(a) Turn-on equivalent circuit (b) Simplified circuit

Figure 2.20 Turn-on equivalent circuit with L_{k2} and R_g

Defining a function $\Phi(t)$ as:

$$\Phi(t) = \begin{cases} 0 & \text{if } t < 0 \\ 1 & \text{if } t \geq 0 \end{cases} \tag{2.3}$$

then, the input signal in Figure 2.20(b) can then be represented as:

$$u_i(t) = k_g t - k_g (t - t_r) \cdot \Phi(t - t_r) \tag{2.4}$$

where $k=k_p/n_g$, and n_g is the turns ratio of the gate driver transformer. One can derive the time domain voltage waveforms across the gate capacitor, $u_c(t)$, by the Laplace transformation, as follows:

$$u_c(t) = k_g\left(t - \frac{2\xi}{\omega_0} + \frac{1}{\omega_d} e^{-\xi\omega_0 t}\sin(\omega_d t + 2\theta)\right)$$
$$-k_g\left(t - t_r - \frac{2\xi}{\omega_0} + \frac{1}{\omega_d} e^{-\xi\omega_0 (t-t_r)}\sin(\omega_d (t-t_r) + 2\theta)\right)\Phi(t-t_r) \quad (2.5)$$

where

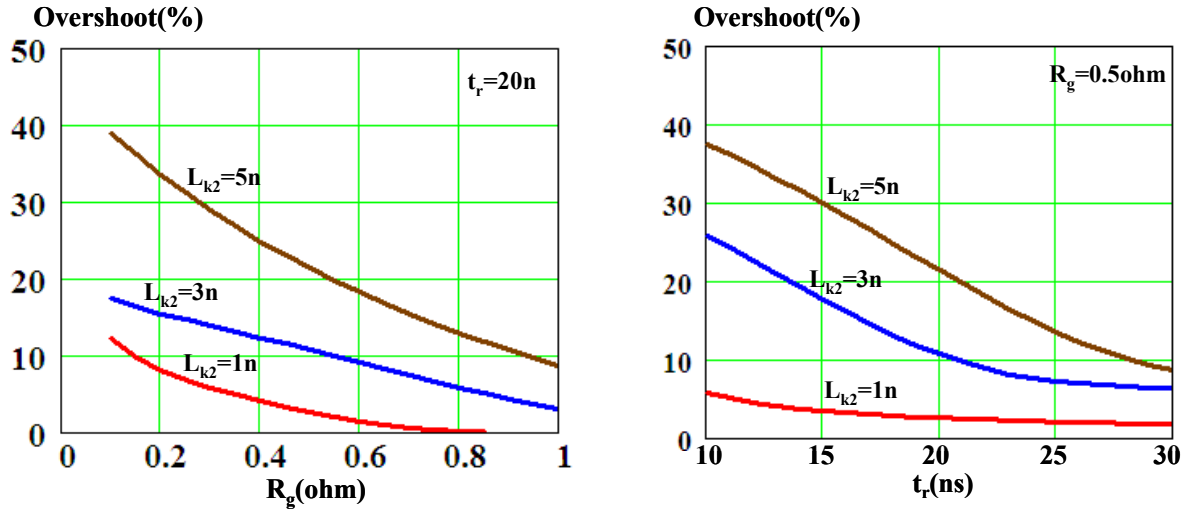
$$\omega_0 = \frac{1}{\sqrt{L_{k2}C_{gs}}} \quad (2.6)$$

$$\xi = \frac{R_g}{2\sqrt{L_{k2}/C_{gs}}} \quad (2.7)$$

$$\omega_d = \omega_0\sqrt{1-\xi^2} \quad (2.8)$$

$$\theta = tg^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right) \quad (2.9)$$

According to Equation (2.5), the peak value of the gate voltage $u_c(t)$ is calculated and plotted as a form of overshoot percentage over the different R_g, L_{k2}, and t_r in Figure 2.21. In the



(a) (b)

Figure 2.21 Gate voltage overshoot

plot, we assume that the circuit drives two ST160NF02L MOSFETs from ST Semiconductors, which has a total input capacitance of 10nF. Figure 2.21(a) fixes t_r=20ns while varying R_g and L_{k2}. When R_g increases, or L_{k2} decreases, the overshoot will be less. Figure 2.21(b) shows the overshoot with a fixed R_g (0.5ohm) and varying t_r and L_{k2}. It is an important characteristic of this driving scheme that the ZVS operation of the power stage reduces the gate ringing by increasing t_r.

2.2.4. SR Gate Drive Loss Analysis

Turn-on of SR: The equivalent circuit shown in Figure 2.20 can also be used to calculate the gate drive loss during the turn-on transition, which is the total energy dissipation on R_g when the voltage across C_{gs} rises from zero to its steady state. The instantaneous current in the driver loop during the turn-on transition is calculated as:

$$i_c(t) = k_g C_{gs}\left(1-\frac{\omega_0}{\omega_d}e^{-\xi\omega_0 t}\sin(\omega_d t+\theta\right)$$
$$-k_g C_{gs}\left(1-\frac{\omega_0}{\omega_d}e^{-\xi\omega_0 (t-t_r)}\sin\left(\omega_d (t-t_r)+\theta\right)\right)\Phi(t-t_r) \qquad (2.10)$$

so that the turn-on gate drive loss is:

$$P_{on} = \int i_c^2 \cdot R_g dt \cdot f_s \qquad (2.11)$$

For a conventional external gate driver circuit as shown in Figure 2.22, V_g is the supply for the driver, K_1 is the pull-up switch, and K_2 is the pull-down device. When K_1 turns on, energy flows from V_g to C_{gs} until the voltage across C_{gs} reaches V_g. The total energy dissipation during this interval is calculated as:

$$P_{on-ex} = 0.5 C_{gs} V_g^2 \cdot f_s \qquad (2.12)$$

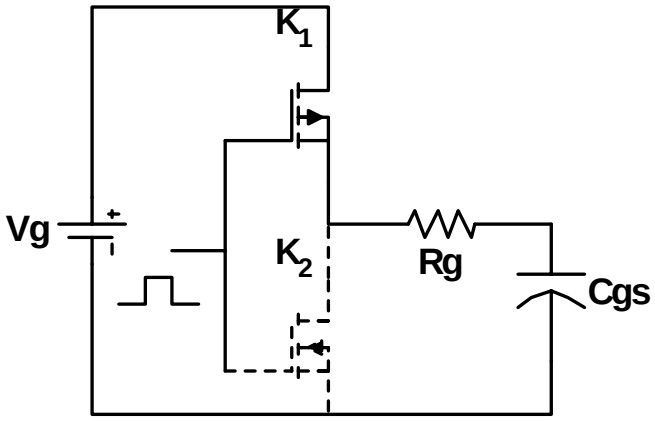


Figure 2.22 A conventional external gate driver circuit

Note that $P_{on\text{-}ex}$ is a Rg independent variable. To drive a pair of ST160NF02L at a switching frequency of 1MHz, the gate driver losses during turn-on by the proposed self-driven scheme and by the conventional method are plotted in Figure 2.23. It also shows that the larger the L_{k2}, the less the loss savings. Considering the overshoot as discussed previously, a smaller L_{k2} is also preferred. It is very important to minimize L_{k2} by all means possible.

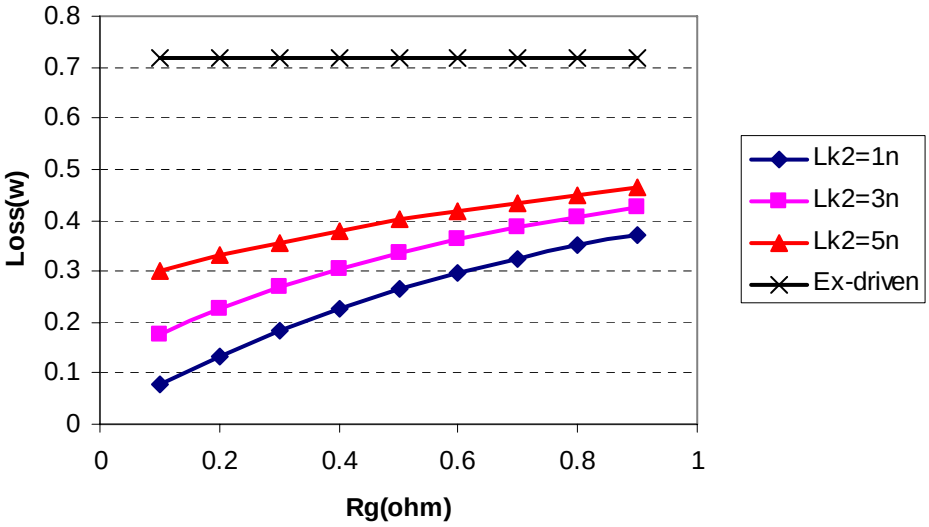


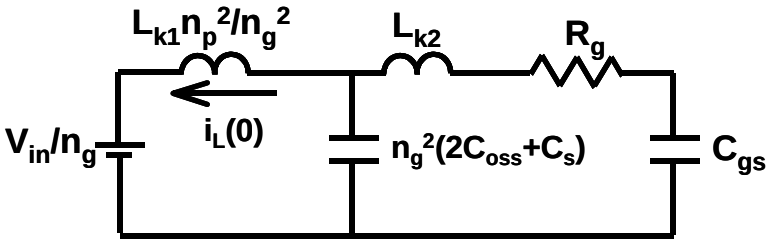
Figure 2.23 Calculated turn-on gate driver loss

Turn-off of SR: The equivalent gate driver circuit of the turn-off of SR is shown in Figure 2.24(a). The energy stored in the transformer leakage inductor L_{k1} helps to charge C_{oss3}, and to discharge C_{oss4}, C_s and C_{gs}. Ideally, if the gate driver path has zero inductance and zero

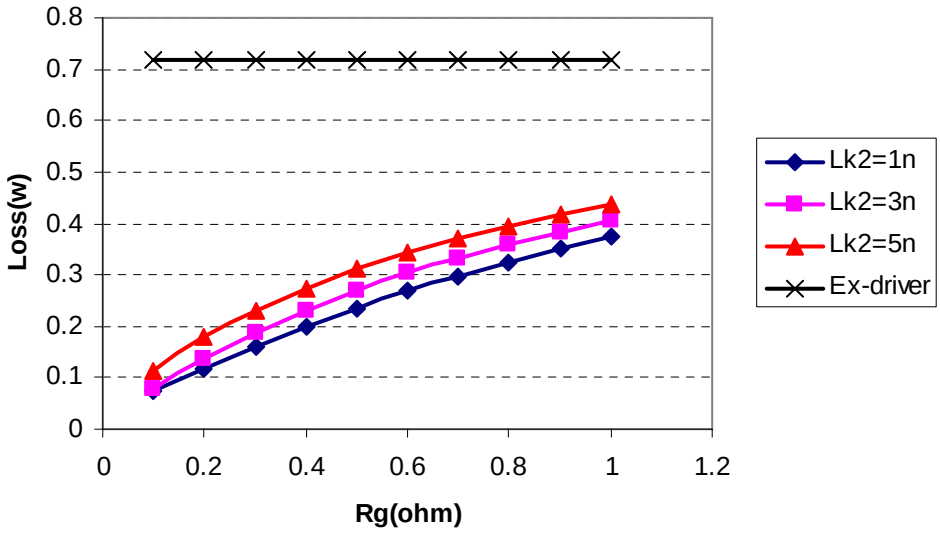
resistance, C_{oss4}, C_s and the reflected C_{gs} are all in parallel and serve as a snubber capacitor of Q4. As long as the ZVS condition is met, the entire gate charge can be recovered. The ZVS condition can be simplified as:

$$I_{o_min} = \sqrt{\frac{2n_p C_{eff} V_{in}^2}{L_{k1}}} \tag{2.13}$$

where I_{o_min} is the minimum load current required to achieve ZVS for Q4. However, because of L_g and R_g, not all of the gate capacitor energy can be recovered. In Figure 2.24(a), there are four energy storage components, and getting an analytical solution becomes extremely complicated. As an alternative method, the circuit was simulated using the SABER simulation tool to analyze



(a)



(b)

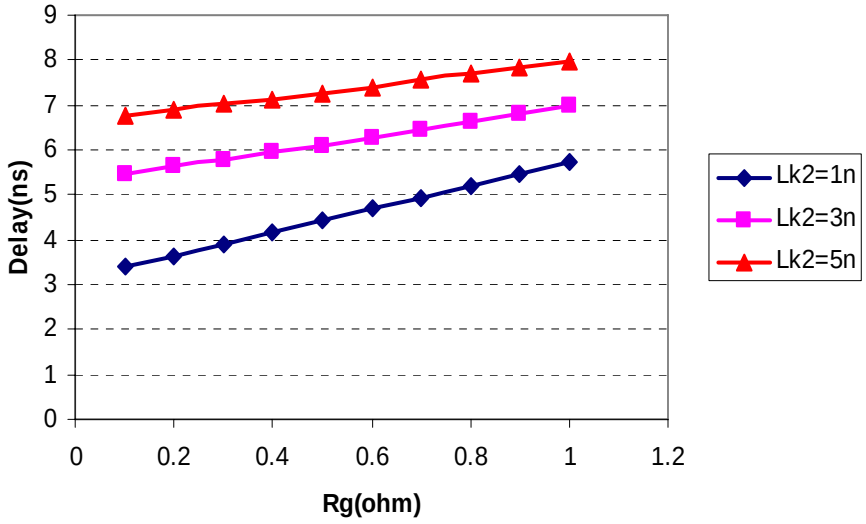
Figure 2.24 Turn-off equivalent circuit and the simulated turn-off gate driver loss

the turn-off loss savings. The simulation was set up with the following conditions: f_s=1MHz, V_{in}=48V, n_p=8, n_g=4, I_o=70A, L_{k1}=4nH; the primary devices are Hitachi's HAT2175, which has a C_{oss} of 185pF; C_s=1nF, and there are 2 ST160NF02L SRs in parallel. Figure 2.24(b) shows the turn-off losses of the self-driven circuit vs. a conventional external voltage driver for one leg of the current doubler. The simulation was run while varying the gate drive resistor R_g and the gate drive transformer leakage inductor L_{k2}. For an externally-driven scheme, as shown in Figure 2.22, the pull-down switch K_2 will short the gate to the ground so that all the energy stored in C_{gs} will be dissipated, no matter how small R_g is. According to Figure 2.24, the turn-off gate drive loss has a similar relationship with R_g and L_g as the turn-on case.

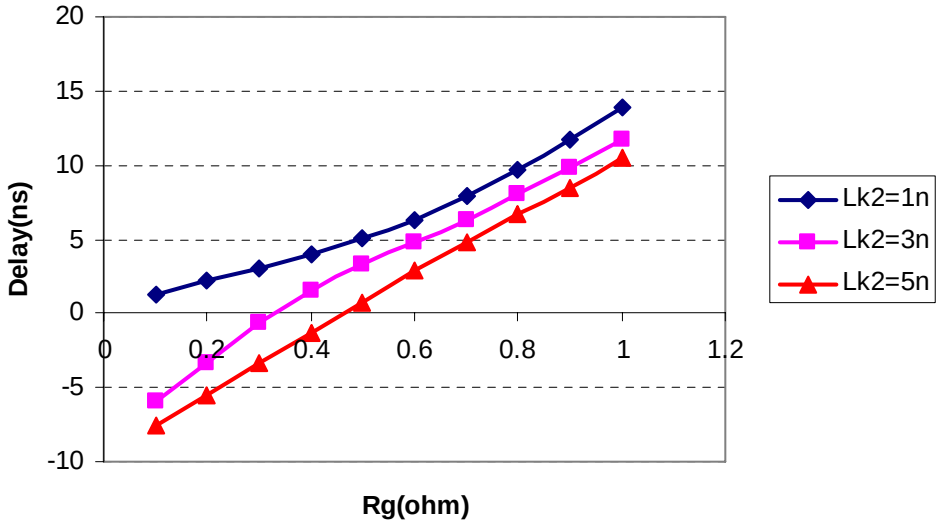
2.2.5. SR Gate Driving Delay and Body Diode Conduction Analysis

Due to the existence of L_g and R_g, there is a time delay from the primary side node B to the SR gate. This time delay has to be taken into account because it may cause additional body diode conduction or shoot-through problems. For the rising edge, according to Equation (2.4) and Equation (2.5), the voltage waveforms at node B and the SR gate are determined. For a given threshold voltage, 1V for ST160NF02L, the delay time is plotted as a function of R_g with different L_g in Figure 2.25(a).

For the falling edge, since we cannot get a simple analytical solution for V_B and V_{gs}, the SABER simulation tool is used again. The curves in Figure 2.25(b) show the relationship between the falling edge delay time, R_g and L_g. It is interesting that there are cases with negative delay time, which means that V_{gs} actually drops to V_{th} earlier than V_B. The reason for this is that when R_g is small, the oscillation between L_g and C_{gs} is not dampened well, so that V_{gs} may go below V_B at some point.



(a) Turn-on delay time



(b) Turn-off delay time

Figure 2.25 Turn-on and turn-off delay time

The delay time for two edges has different impact on the SR operations. To begin analyzing this, let us go back to Figure 2.11 to see how current flows at the secondary side before and after S_1 turns on (rising edge). Before t_1, S_1 is off, I_s is positive and equal to half the load current. After a very short transition period (t_1~t_2), S_1 turns on so that both the primary and the secondary sides of the power transformer are shorted. There is no voltage applied to the leakage inductance L_k; therefore I_s continues to flow through its previous path before t_1. In other words,

no current flows through S_1 although it is ready to take the current. This Zero-Current-Turn-on feature makes the rising edge of its gate signal less critical as long as the delay does not exceed the overlapping time (t_2~t_3).

For the falling edge of the gate signal, the delay time may in fact help to reduce the body diode conduction period. On the other hand, too much delay time will cause a severe shoot-through problem. The following analysis gives the maximum falling edge delay time. Assuming R_g and L_g are all zero, the gate voltage of an SR exactly follows V_B with no delay, as shown in Figure 2.26(a).

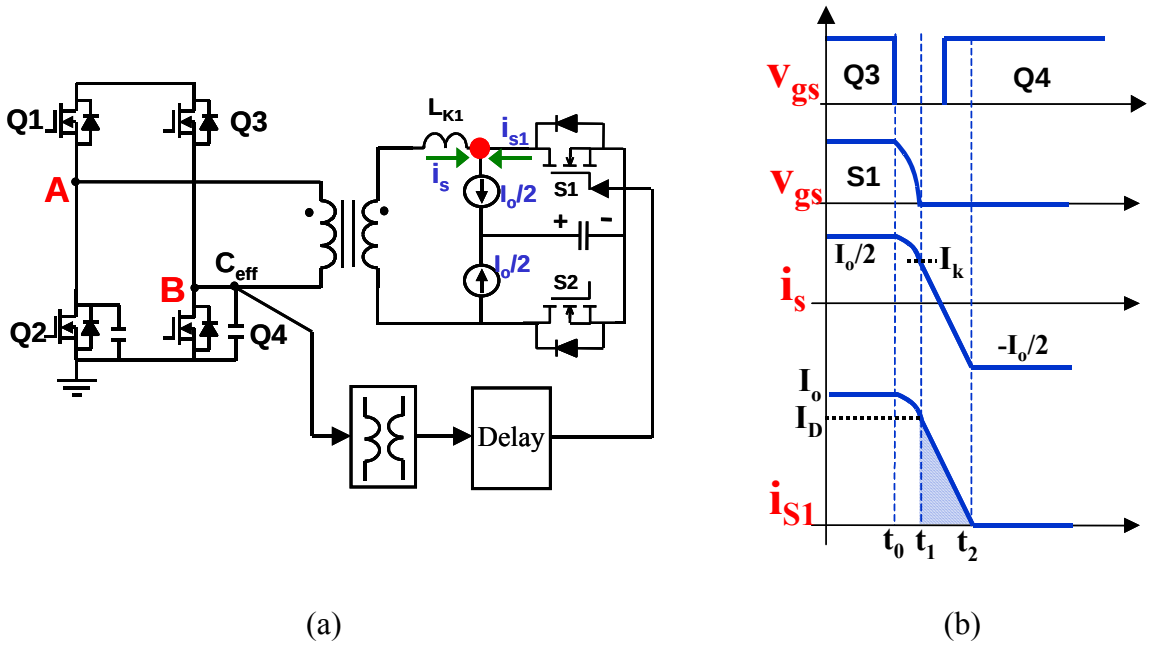


Figure 2.26 Equivalent circuit and key waveforms during S1 turn-off interval

When Q3 is turned off at t_0, the transformer leakage inductor L_{k1} begins to resonate with C_{eff} until the voltage at point B drops to zero at t_1. At the same time, S1 is turned off if the delay time is zero. However, the current through S1 continues to flow until the current through the transformer secondary side winding i_s changes its polarity from I_k to $-I_o/2$ at t_2. From t_1 to t_2, the body diode of S1 conducts the current, and the body diode conduction loss for S1 can be calculated as follows:

$$P_D = 0.5 I_D \cdot \Delta t \cdot V_F \cdot f_s \qquad (2.14)$$

where V_F is the body diode forward voltage drop, typically 0.7V, and f_s is the converter switching frequency.

$$I_D = \frac{I_o}{2} \cdot \left(1 + \sqrt{1 - \left(\frac{2 n_p V_{in}}{I_o Z_k} \right)^2} \right) \tag{2.15}$$

$$\Delta t = t_2 - t_1 = \frac{L_{k1} n_p I_D}{V_{in}} \tag{2.16}$$

$$Z_k = \sqrt{\frac{L_{k1} n_p^2}{C_{eff}}} \tag{2.17}$$

The delay time between V_B and the SR gate, when positive, helps to reduce Δt, and therefore reduces the body diode conduction loss. In order to avoid severe shoot-through problems, the delay time must be less than Δt. However, Δt varies according to the differences of load current I_o. The possibility of shoot-through at light load exists. Fortunately, the inclusion of the tiny gate MOSFET, as shown in Figure 2.15, helps to prevent this from happening. The SR gate will clamp to ground as soon as V_B touches zero at time t_1 in Figure 2.26, no matter how much delay time there is.

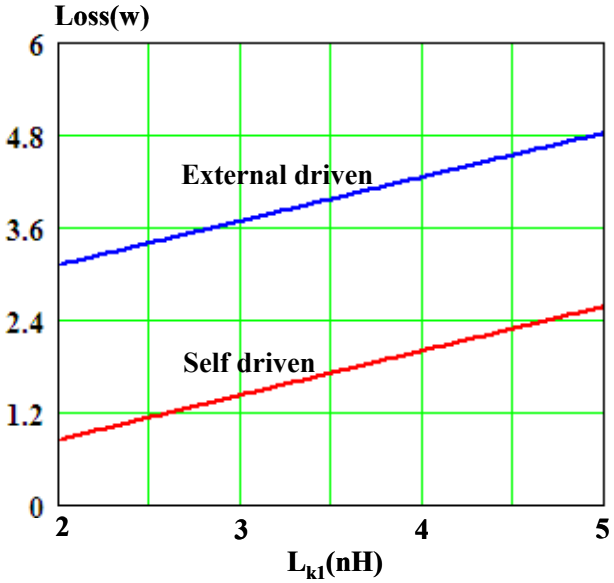


Figure 2.27 Body diode conduction loss compared with the conventional phase-shifted FB converter

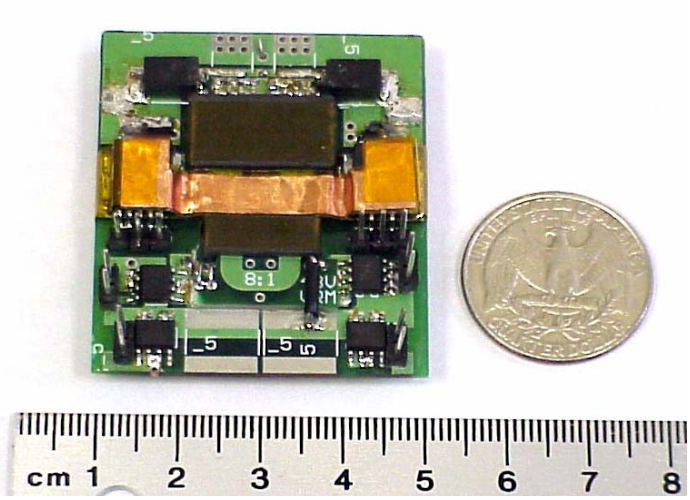
Figure 2.27 shows the total body diode conduction loss comparison between a phase-shifted FB converter with an externally driven scheme and the proposed circuit. A typical gate dead time of 20ns is set for the external driver. The transformer leakage inductance is the variable. Both systems run at 1MHz, 70A load current.

2.2.6. Experimental Results

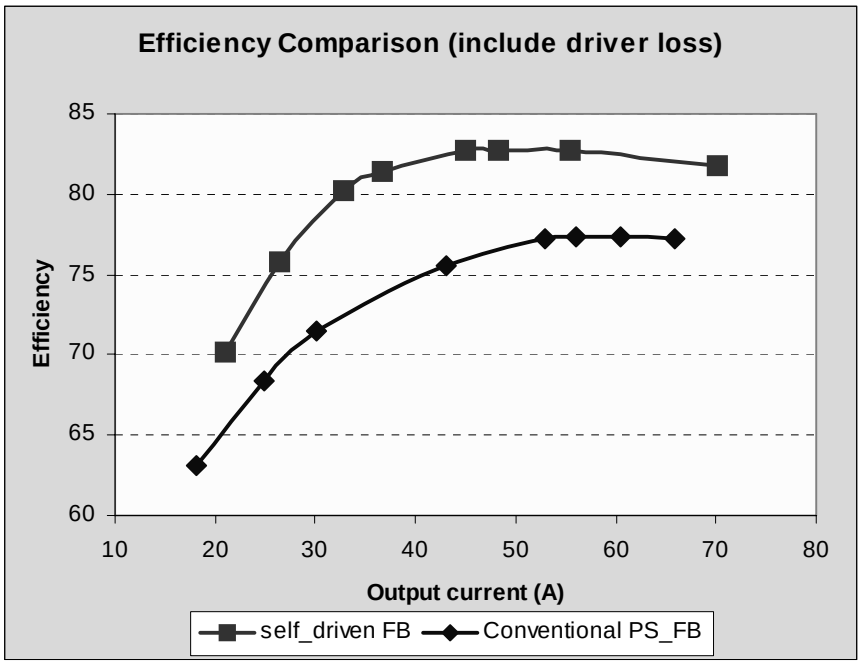
A 1.2V/70A 1MHz prototype is built to verify the analysis. The components are listed as follows: Primary switch: Si4850, secondary switch: ST160NF02LA*2 for each branch of a current doubler, transformer: nine-layer (2 oz), Philips EI-14 core, inductor: 150nH, nine-layer (2 oz), Philips EI-18 core, output capacitor: 4*ESRE 270uF, gate resistance: 0.5 Ohm, gate transformer: TDK EE9.5, gate MOSFET: Si3900.

A picture of the prototype is shown in Figure 2.28(a). Figure 2.28(b) shows the efficiency comparison. Including the driver loss, the proposed self-driven ZVS full-bridge converter can achieve 81.7% efficiency. There is an efficiency improvement of 4.7% over the conventional phase-shifted full-bridge converter with an external driver. Figure 2.29(a) shows the ZVS condition of the primary switches. Figure 2.29(b) shows the gate signal for the SR. The waveform of the gate signal follows the voltage at point B, and is very clean.

Figure 2.30 illustrates the different experimental results achieved with the conventional driver scheme (Figure 2.13) and the proposed driver scheme (Figure 2.15). It is obvious that the secondary-side gate signal of the conventional driver cannot go back to the zero level when the primary-side signal has a sudden duty-cycle change. The proposed driver scheme can solve this problem. Additionally, compared with the diode paralleled with the gate of SRs, the tiny MOSFET can help SRs achieve faster turn-off due to the low-impedance turn-off path.

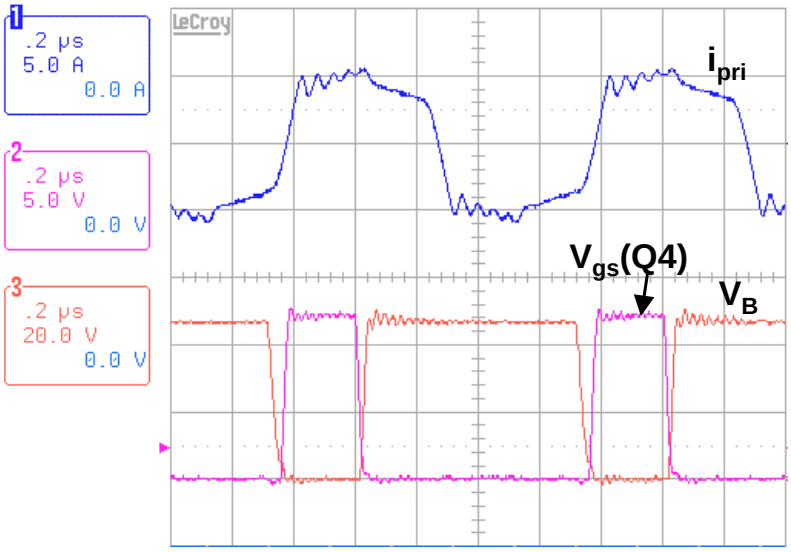


(a) Prototype of the proposed circuit with coin for size reference

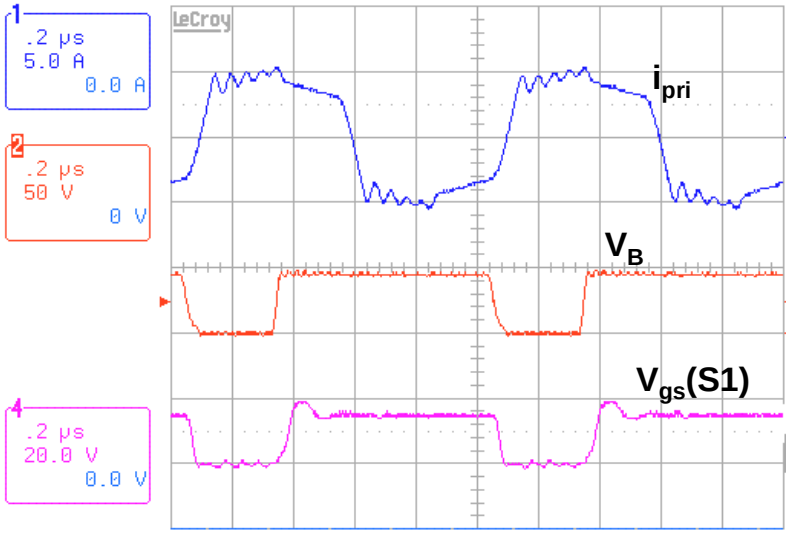


(b) Efficiency comparison

Figure 2.28 The prototype of the proposed self-driven ZVS FB and its efficiency curve

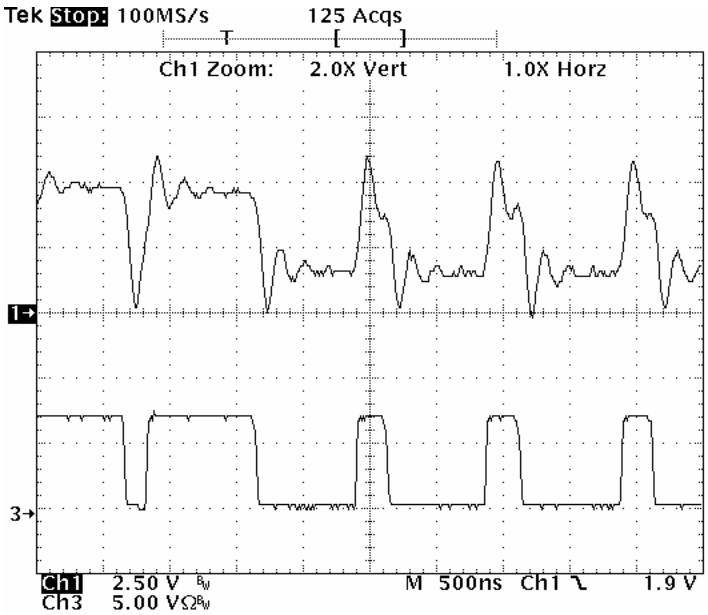


(a) ZVS condition for the primary switches

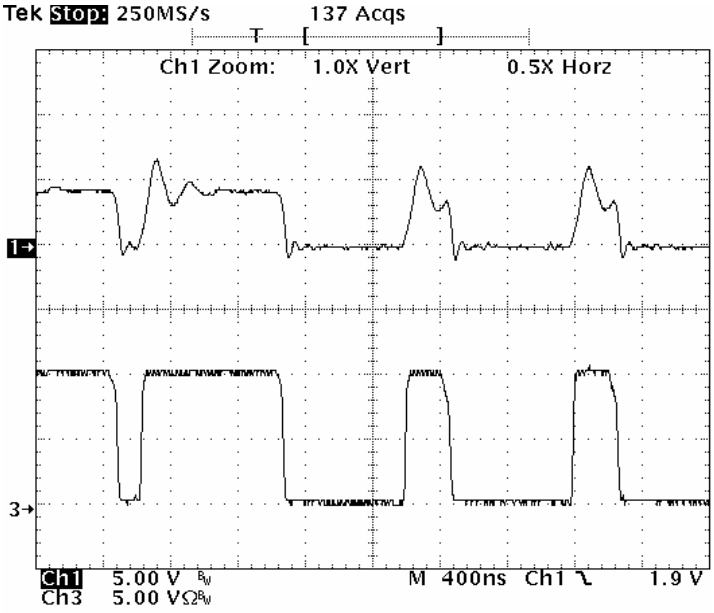


(b) The transformer primary current I_{pri}, the voltage at point B V_B, and the gate signal for the SR $V_{gs(S1)}$

Figure 2.29 Circuit waveforms



(a) Conventional driver scheme in Figure 2.13



(b) Proposed driver scheme in Figure 2.15

Figure 2.30 Gate voltage waveforms during a duty change

2.3. Current-Tripler DC-DC Converters for High Current 48V Isolated VRMs

For low-voltage and high-current applications, the secondary-side power losses have a major impact on efficiency. First, synchronous rectification, with specifically designed low-voltage MOSFETs, is widely used to dramatically improve the efficiency of low-voltage DC-DC converters. Second, proper secondary-side topologies should be selected to reduce the RMS current through the SRs. There are three major secondary-side topologies: forward rectifier, center-tapped rectifier and current-doubler rectifier (Figure 2.31). Among these three topologies, the current-doubler rectifier is the most suitable for high-current, low-voltage applications. Because of its simpler transformer structure and two-times-lower inductor currents and

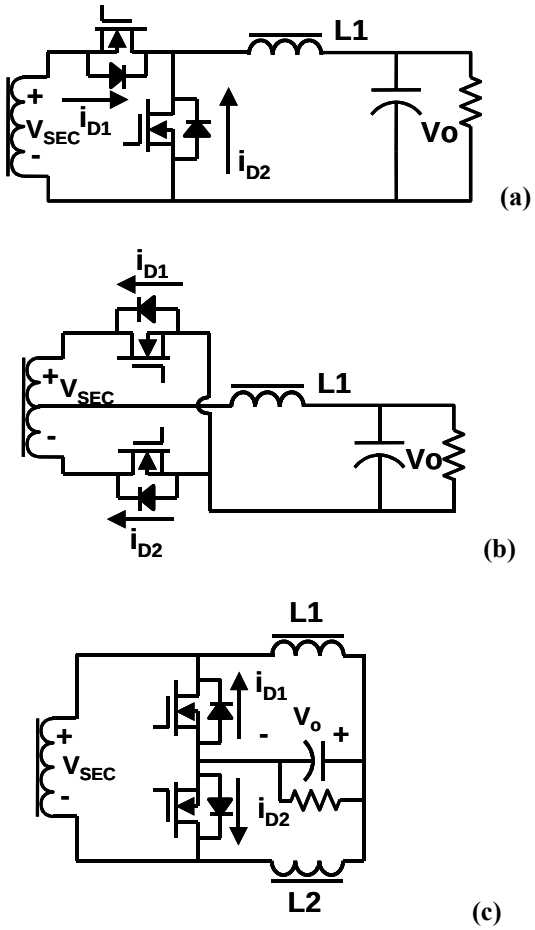
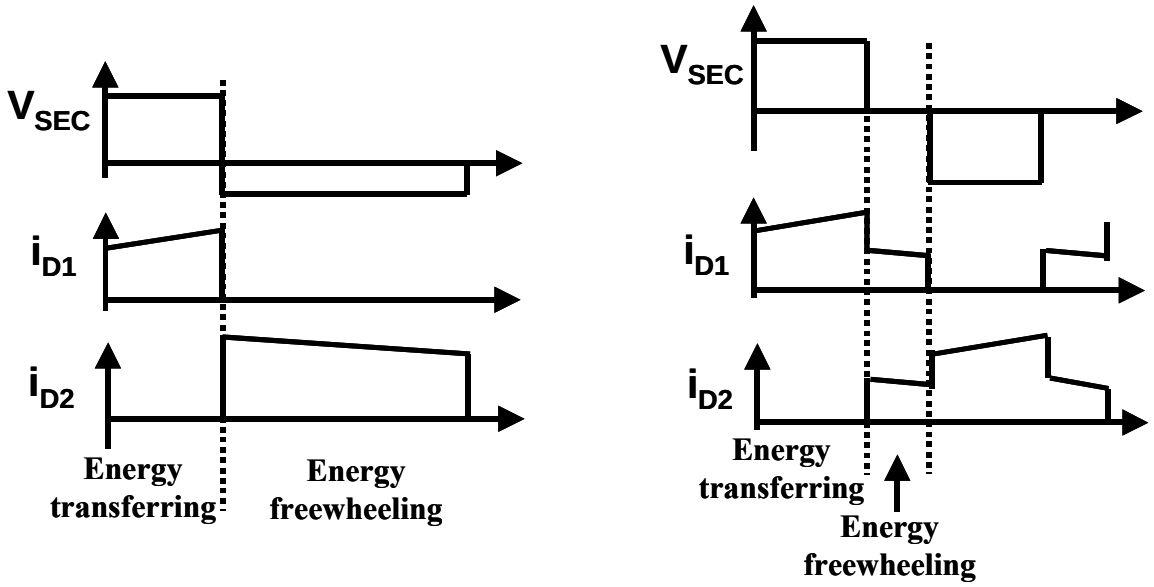


Figure 2.31 Three conventional rectifier topologies: (a) Forward rectifier; (b) Center-tap rectifier; (c) Current-doubler rectifier

transformer secondary currents, the current-doubler topology can offer lower conduction losses than the conventional center-tapped topology.

There is lower RMS current of the current-doubler rectifier because during the freewheeling period (when there is no input-output energy transfer), the two SR switches share the load current, as shown in Figure 2.32(b). As a result, the total rectifier conduction loss during the freewheeling period is reduced. On the other hand, for the forward rectifier in Figure 2.31(a), only one SR switch conducts the total load current, as shown in Figure 2.32(a).



(a) Forward (b) Current-doubler

Figure 2.32 Current through a forward rectifier and a current-doubler rectifier

Conventionally, the current-doubler with more semiconductor devices in parallel is used to reduce the on-resistance of the SR, and a distributed magnetic structure is also used to reduce the transformer winding losses. However, those solutions have their limitations, such as (a) increased cost, (b) larger footprint and lower power density, and (c) larger driver loss. These issues pose significant challenges for future high-current, low-voltage DC-DC converters for microprocessors.

The forward rectifier can be considered as a single-phase secondary topology, and the current-doubler can be treated as a two-phase interleaving topology. Can the current-doubler be extended to three phases so that there are three MOSFETs sharing the load current during the

freewheeling period? Theoretically, the current-doubler will have lower RMS current through each device, and lower secondary conduction loss is expected. The remaining questions are the transformer structure and the control of the primary side switches. The following sections will first derive the current-tripler topology. Then the detailed operation principle will be discussed. The benefits of the proposed topology over the conventional current-doubler topology is also investigated. Experimental results are given to verify those advantages.

2.3.1. Derivation of the Current-Tripler DC-DC Converter

A current-doubler rectifier is basically a two-phase interleaving topology. Figure 2.33(a) shows a redrawn current-doubler of Figure 2.31(c), which has a rectification stage identical to

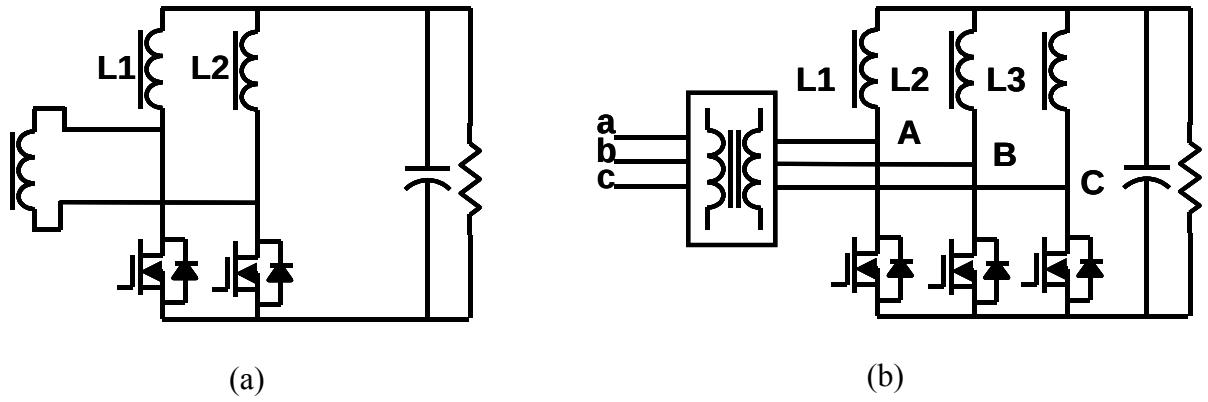


Figure 2.33 A current-doubler rectifier (a) and a current-tripler rectifier (b)

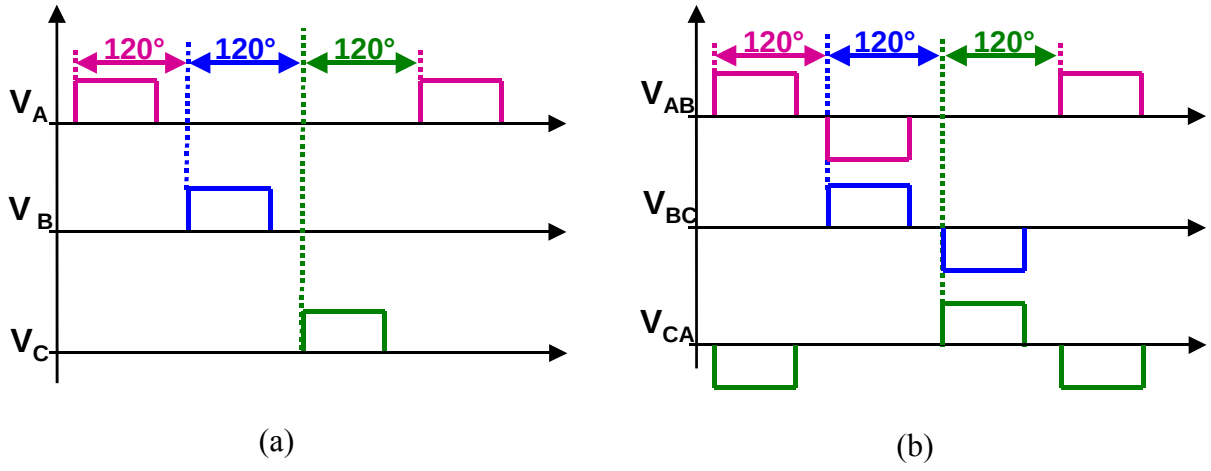
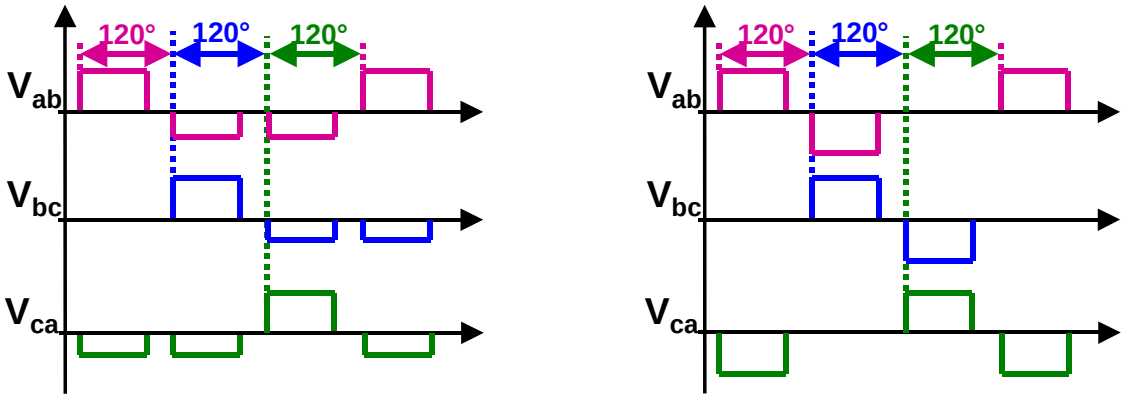


Figure 2.34 Required phase-node voltages (a) and secondary side line-to-line voltages (b)

that of a two-phase buck. Now it is very simple to configure a three-phase rectifier structure (Figure 2.33(b)), an inspiration from the three-phase interleaving buck converter. But it is unclear how the primary side switches are controlled and what the transformer looks like. The only thing we know is a topology as shown in Figure 2.33(b), which has phase-nodes voltage waveforms identical to those of a three-phase buck converter (Figure 2.34(a)).

According to the required phase-nodes voltage waveforms, one can derive the line-to-line voltage waveforms by subtracting one phase voltage from the other, as shown in Figure 2.34(b). There are four combinations of a three-phase transformer winding connection: Y/Δ, Δ/Y, Δ/Δ, and Y/Y. Since we already know the required secondary side line-to-line voltages (V_{AB}, V_{BC}, V_{CA}), the primary side line-to-line voltages (V_{ab}, V_{bc}, V_{ca}) for different winding connections can be derived. Figure 2.35 shows the derivation results in which the voltages of Y/Δ and Δ/Y connections have different positive and negative levels (Figure 2.35(a)). On the other hand, the voltages of Y/Y and Δ/Δ connections have equal positive and negative levels (Figure 2.35(b)). To generate a voltage with different levels will need more complicated primary circuitry so that only Y/Y and Δ/Δ connections are considered for the current-tripler DC-DC converter.



(a) Y/Δ and Δ/Y connections (b) Y/Y and Δ/Δ connections

Figure 2.35 Primary side line-to-line voltages of different winding connections

For the high-current low-voltage DC-DC conversion, the transformer's secondary winding's turn is always one. Assuming the resistance of a single-turn winding is R for both Y/Y and Δ/Δ connections, one can transform the Δ/Δ to Y/Y connection with R/3 equivalent winding

resistance. In order to minimize the winding conduction loss, it is necessary to use Δ/Δ connection for the current-tripler DC-DC converters.

In order to get the primary side line-to-line voltage as shown in Figure 2.35(b), a three-phase bridge is used as shown in Figure 2.36. There are two control schemes we can use to control Q1~Q6: a PWM hard-switching control scheme or a PWM complementary control scheme. Their gate signals are shown in Figure 2.37(a) and (b), respectively.

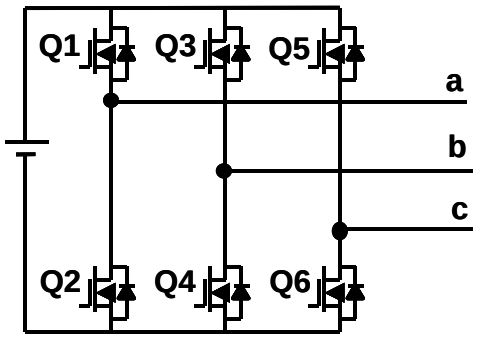
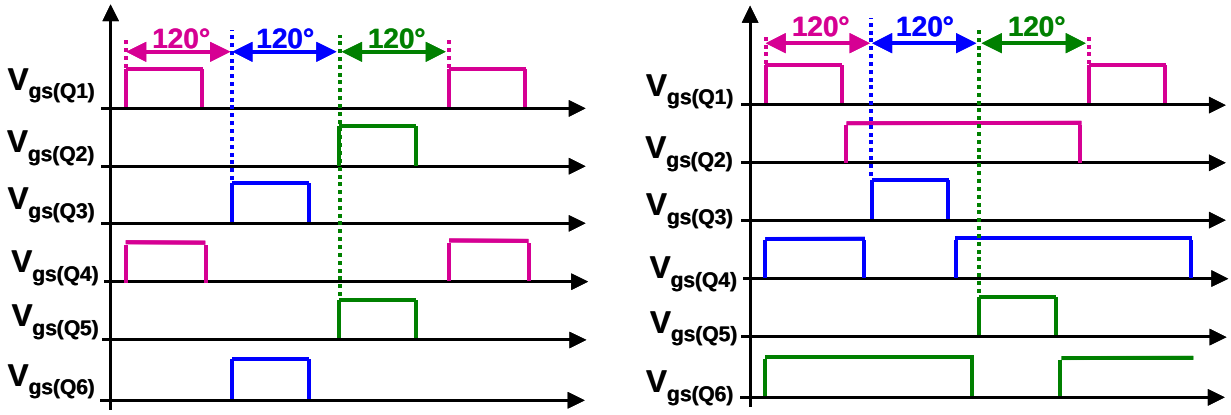


Figure 2.36 A three-phase bridge primary for the current-tripler DC-DC converter



(a) PWM hard switching converter (b) Complementary control

Figure 2.37 Two control schemes for the current-tripler DC-DC converter

2.3.2. Operating Principle of the Current-Tripler DC-DC Converter

According to the derivation in the previous section, a complete current-tripler DC-DC converter is shown in Figure 2.38. There are three switch legs at the primary side. In each switch leg, the top and bottom switches are operating complementarily to realize zero voltage switching

for the switches. The required isolation of the primary side and the secondary side is achieved by a high-frequency three-phase transformer, which has delta connections at both sides. The transformer leakage inductors are reflected to the primary side as L_{ka}, L_{kb}, and L_{kc}. At the secondary side, a structure including three SRs, which is called the current-tripler, is proposed to reduce the conduction loss of the secondary side.

The switch-timing diagrams for the primary switches Q1~Q6 and secondary SR switches S1~S3 are shown in Figure 2.39. Based on the switch-timing diagram, there are 12 operating modes during one switching cycle. In order to simplify the analysis, the following assumptions are made:

1. Assume L1-L3 are large enough so that the current ripple is ignored;

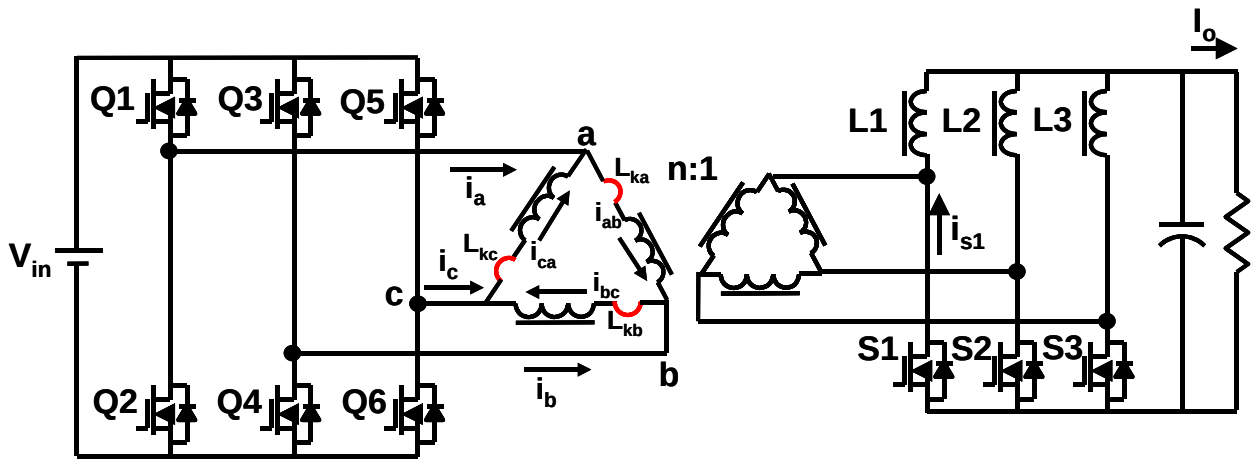


Figure 2.38 Proposed ZVS current-tripler DC-DC converter

2. All the switches are ideal switches, and all the windings are ideal as well.

Mode1 [t_0~t_1]: In this mode, Q1, Q4 and Q6 are on. On the secondary side, S2 and S3 are on. The equivalent circuit is shown in Figure 2.40. The energy is transferred from the primary side to the secondary side. According to the energy balance, the input current i_a can be calculated as $\frac{I_o}{3n}$. How the current flows in the Δ-connected windings is so far unknown. We define the current in the three windings during this mode as $i_{ab(0)}$, $i_{bc(0)}$, and $i_{ca(0)}$. Meanwhile, the line current are $i_{a(0)}$, $i_{b(0)}$, and $i_{c(0)}$.

Mode2 [t_1~t_2]: At t_1, Q1 is turned off. The reflected load current, i_a, is used to charge the output capacitor of Q1, C_{oss1}, and to discharge the output capacitor of Q2, C_{oss2}. Since we assume that the output inductors are large enough, i_a stays constant and the winding current does not change during this short period. The voltage at node a decreases to zero and prepares for the zero voltage turn-on of Q2.

Mode3 [t_2~t_3]: During this interval, Q2, Q4, Q6, S1, S2, and S3 are all on, which shorts both the primary and secondary windings. Due to the presence of the transformer leakage inductors, the winding current will not change. The energy stored in the leakage inductors of the transformer is freewheeling through the three bottom switches of the primary side.

Mode4 [t_3 ~t_4]: At t_3, Q4 turns off. The gate signal of S2 is also removed; however, S2 still conducts current through its body diode. The secondary windings are therefore still shorted. The energy stored in the leakage inductors of the transformer is used to charge C_{oss4} and to discharge C_{oss3}. At certain load conditions, the energy stored in the leakage inductors is sufficient to achieve ZVS for Q3. Note that node a and node c are both grounded so that there is no voltage applied to the leakage inductor L_{kc}. The current through winding ac, i_{ca}, remains unchanged. Also, because the same voltages apply to L_{ka} and L_{kb}, the changes of the current through L_{ka} and L_{kb} are the same. At the end of this period, t_4, Q3 turns on so that i_b will take the reflected load current, $\frac{I_o}{3n}$. This starts another 4-mode cycle for the Q3-Q4-bridge. We define the current in the three windings during Mode 5 following Mode 4 as $i_{ab(1)}$, $i_{bc(1)}$, and $i_{ca(1)}$. Meanwhile, the line currents are $i_{a(1)}$, $i_{b(1)}$, and $i_{c(1)}$. Mode 5 is in fact equivalent to Mode 1 in terms of input-output energy transfer. The repeat description of Mode 5- Mode 12 is ignored here.

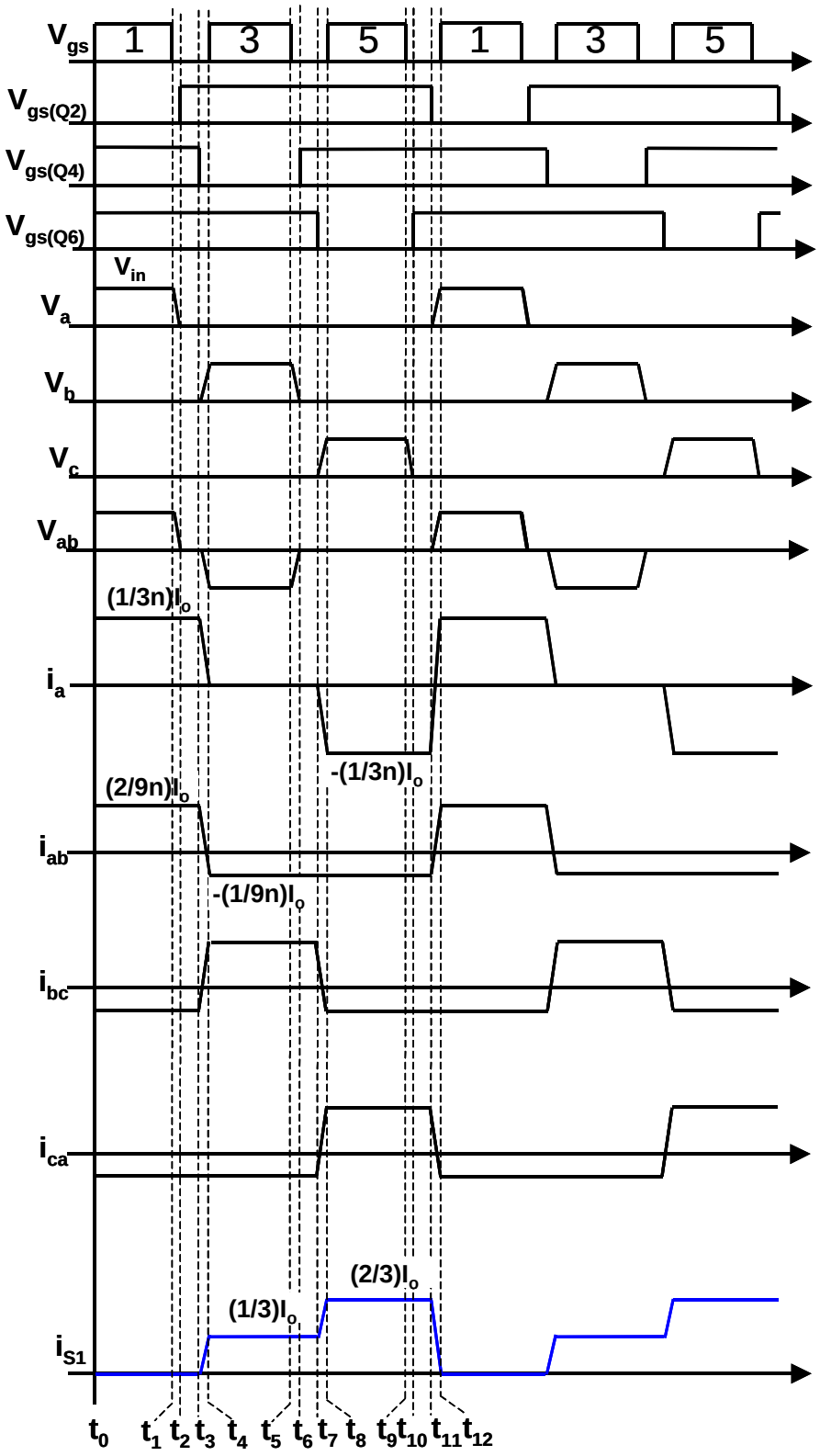


Figure 2.39 Control strategy of proposed current-tripler DC-DC converter

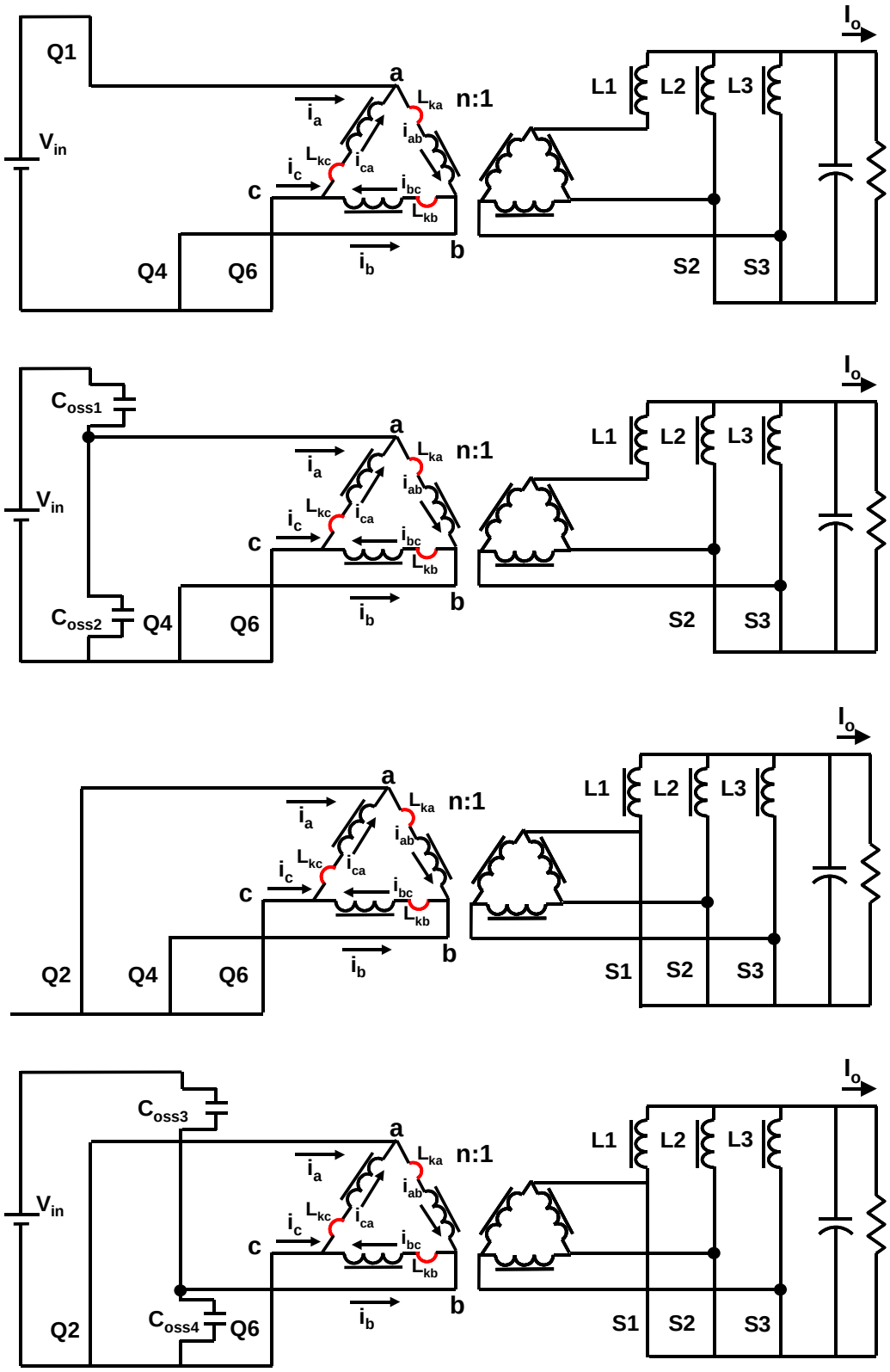


Figure 2.40 Equivalent circuits for Model 1~Mode 4

Now it's time to derive the winding current, and based on that the current the SRs can be easily derived. In Mode 1, we have:

$$i_{a(0)} = i_{ab(0)} - i_{ca(0)} \tag{2.18}$$

$$i_{c(0)} = i_{ca(0)} - i_{bc(0)} \tag{2.19}$$

In Mode 5, we have:

$$i_{b(1)} = i_{bc(1)} - i_{ab(1)} \tag{2.20}$$

$$i_{a(1)} = i_{ab(1)} - i_{ca(1)} \tag{2.21}$$

According to the voltages applied to the three leakage inductors during Mode 4, we have:

$$i_{ca(1)} = i_{ca(0)} \tag{2.22}$$

$$i_{bc(1)} - i_{bc(0)} = -\left(i_{ab(1)} - i_{ab(0)}\right) \tag{2.23}$$

According to the symmetry of the connection, we have:

$$i_{a(0)} = i_{b(1)} = \frac{I_o}{3n} \tag{2.24}$$

$$i_{c(0)} = i_{a(1)} \tag{2.25}$$

Solving these equations gives $i_{ca(0)}$=$i_{bc(0)}$. The winding current i_{ab}, i_{bc} , and i_{ca} can then be derived as shown in Figure 2.39. Note that there is no DC current component for each winding.

2.3.3. Compact Magnetic Structure for the Current-Tripler DC-DC Converter

One of the major benefits of the current-tripler concept is the magnetic structure of the transformer. It is basically an integrated magnetic core with distributed windings. In Figure 2.38, the three-phase transformer has three sets of primary-secondary windings. Both the primary and secondary windings are delta-connected. A simple way to implement this transformer structure is to use three separated cores, as shown in Figure 2.41. In Figure 2.41, aa', bb' and cc' represent the three primary windings. AA', BB' and CC' are the secondary windings. Φ_a, Φ_b and Φ_c represent the AC flux through the magnetic cores.

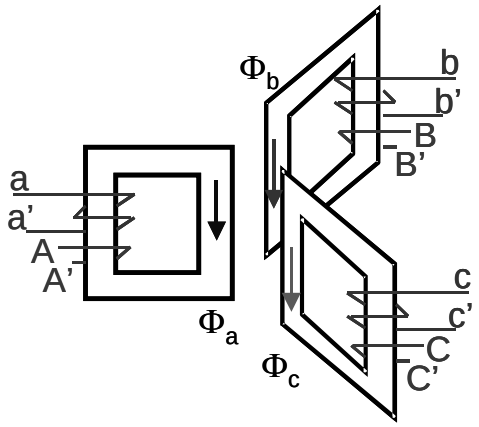


Figure 2.41 Implementation by three discrete cores

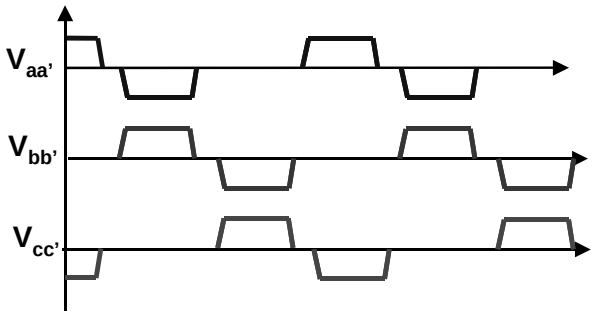


Figure 2.42 Voltage waveforms of three primary windings

Figure 2.42 shows the voltage waveforms across the three primary windings at steady state. It is easily observed that:

$$V_{aa'} + V_{bb'} + V_{cc'} = 0 \quad (2.26)$$

According to Faraday's law, the induced voltage (V) of an N-turns winding from a time-changing magnetic field (Φ) is:

$$V = N * (d\Phi/dt) \quad (2.27)$$

Therefore, for each primary winding, the winding voltage is:

$$V_{aa'} = N * (d\Phi_a/dt) \quad (2.28)$$

$$V_{bb'} = N * (d\Phi_b/dt) \quad (2.29)$$

$$V_{cc'} = N * (d\Phi_c/dt) \quad (2.30)$$

Adding (2.28), (2.29) and (2.30), and substituting the left side of the equation with (2.26) yields:

$$d\Phi_a/dt + d\Phi_b/dt + d\Phi_c/dt = 0 \tag{2.31}$$

which means that the AC flux of the three magnetic cores is cancelled out. The magnetic structure can be simplified as one core with three legs, as shown in Figure 2.43. This structure is very similar to a three-phase 60Hz transformer with three magnetic legs [43]. The removal of the fourth leg is possible due to the automatic AC flux balance between the three legs, as derived above.

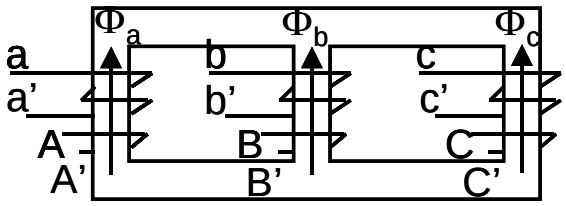


Figure 2.43 Implementation by a three-leg core

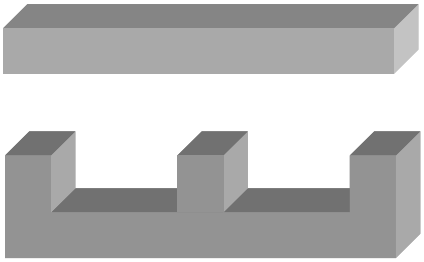


Figure 2.44 Magnetic core structure

This compact transformer structure reduces the core loss because the total volume of the core is reduced. Figure 2.44 shows an example of this core structure. The cross-sections of the three legs are identical, so the flux density of each leg is the same.

One concern in the delta-delta connection is the loop current around the windings. According to the voltage waveforms in Figure 2.42, Fourier analysis can determine whether or not there are any 3n harmonics that will cause loop current along the windings. For one winding voltage, $V_{aa'}$, the Fourier expression is:

$$V_{aa'}(t) = C_0 + 2\sum_{k=1}^{\infty} |C_k| \cos(2\pi k f_0 t + \theta_k) \tag{2.32}$$

and

$$C_k = \frac{1}{T}\int_0^T x(t)e^{-j2\pi k f_0 t}dt = \frac{(e^{-j2\pi k\cdot\frac{1}{3}} - 1)(e^{-j2\pi kD} - 1)}{j2\pi k} \tag{2.33}$$

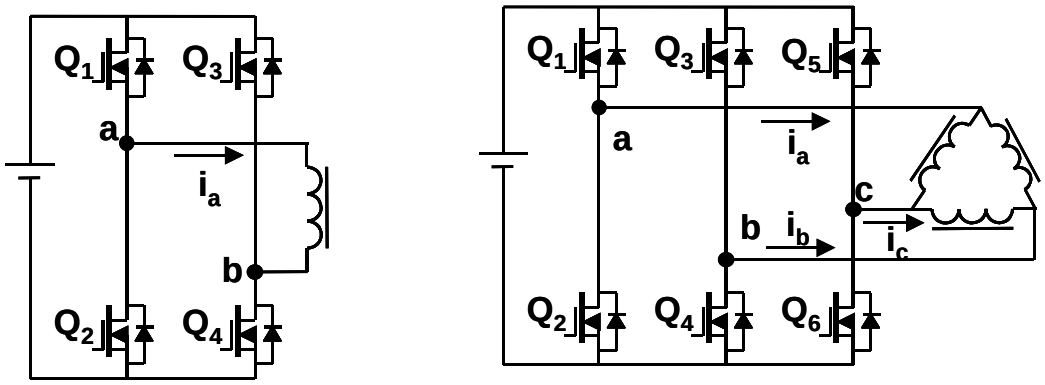
where C_0 is the DC component, and C_k is the magnitude of the k^{th} harmonic. f_0 is the frequency of the fundamental component. Substituting k=3n into (2.33) yields:

$$C_{3n} = 0 \tag{2.34}$$

There is no loop current along the windings as long as the winding voltages have the waveforms as shown in Figure 2.42.

2.3.4. Primary-Side Loss Analysis

The primary-side conduction loss and switching loss of two topologies are compared: one topology is the conventional phase-shift full-bridge converter with a current-doubler rectifier, and the other is the proposed three-phase converter with a current-tripler rectifier. Both can achieve ZVS under certain load conditions. It is assumed that the output current is the same, and the output inductor current ripple is ignored for simplification. The primary-side topologies are illustrated in Figure 2.45.



(a) Conventional full bridge primary **(b) Three-phase bridge primary**

Figure 2.45 Two primary topologies for DC-DC converters

For a given input voltage range, both of the circuits need to meet the following requirement for a same output voltage:

$$n = \frac{V_{in_min}}{V_{out}} D_{max} \tag{2.35}$$

where n is the transformer turns ratio, and D_{max} is the maximum duty cycle at which the converter can run. Based on the previous analysis, D_{max} for the current-tripler converter is $\frac{1}{3}$, while for the current-doubler converter is $\frac{1}{2}$. Therefore,

$$\frac{n_3}{n_2} = \frac{2}{3} \tag{2.36}$$

where n3 and n2 are the transformer turns ratios for the current-tripler and the current-doubler converters, respectively. Table 2.1 lists the RMS current through each device and the turn-off current of each device, in which I_o is the load current.

Table 2.1 The RMS current and the turn off current of each device

	Current-doubler DC-DC converter				Current-tripler DC-DC converter					
	Q_1	Q_2	Q_3	Q_4	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6
I_{rms}	$\frac{\sqrt{2}}{4n_2} I_o$	$\frac{\sqrt{2}}{4n_2} I_o$	$\frac{\sqrt{2}}{4n_2} I_o$	$\frac{\sqrt{2}}{4n_2} I_o$	$\frac{\sqrt{D}}{3n_3} I_o$	$\frac{\sqrt{\frac{2}{3}-D}}{3n_3} I_o$	$\frac{\sqrt{D}}{3n_3} I_o$	$\frac{\sqrt{\frac{2}{3}-D}}{3n_3} I_o$	$\frac{\sqrt{D}}{3n_3} I_o$	$\frac{\sqrt{\frac{2}{3}-D}}{3n_3} I_o$
I_{off}	$\frac{1}{2n_2} I_o$	$\frac{1}{2n_2} I_o$	$\frac{1}{2n_2} I_o$	$\frac{1}{2n_2} I_o$	$\frac{1}{3n_3} I_o$	$\frac{1}{3n_3} I_o$	$\frac{1}{3n_3} I_o$	$\frac{1}{3n_3} I_o$	$\frac{1}{3n_3} I_o$	$\frac{1}{3n_3} I_o$

According to Table 2.1, the total conduction loss of the phase-shift full bridge primary is:

$$P_{cond1} = \frac{I_o^2 R_{on}}{2n_2^2} \tag{2.37}$$

and the total conduction loss of the current-tripler converter primary is:

$$P_{cond2} = \frac{2I_o^2 R_{on}}{9n_3^2} \tag{2.38}$$

where R_{on} is the on resistance of the primary-side MOSFET. According to Equation (2.36), Equation (2.37) and (2.38) are identical, which means that the current-tripler can not reduce the primary-side conduction loss. Fortunately, in the 48V input application, the primary-side conduction loss is not the major part of the total power loss; the tradeoff is made to reduce the secondary-side conduction loss as discussed in the following session.

2.3.5. Secondary-Side Conduction Loss Analysis

The secondary-side conduction loss of two topologies is compared: one topology is the phase-shift full-bridge converter with a current-doubler rectifier, and the other is the proposed three-phase converter with a current-tripler rectifier. It is assumed that the output current is the same, and the number of rectifier devices is also the same, as illustrated in Figure 2.46. For the current-doubler topology (Figure 2.46(a)), each switch leg has three MOSFETs in parallel. For the current-tripler topology (Figure 2.46(b)), two MOSFETs in parallel form one switch leg. The average current through each MOSFET is $\frac{I_o}{6}$ for both the current-doubler and the current-tripler.

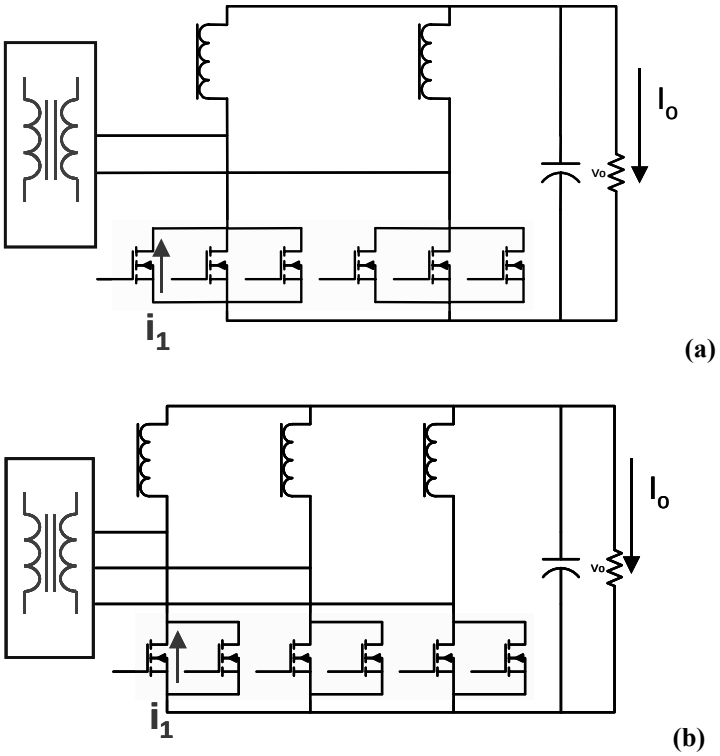
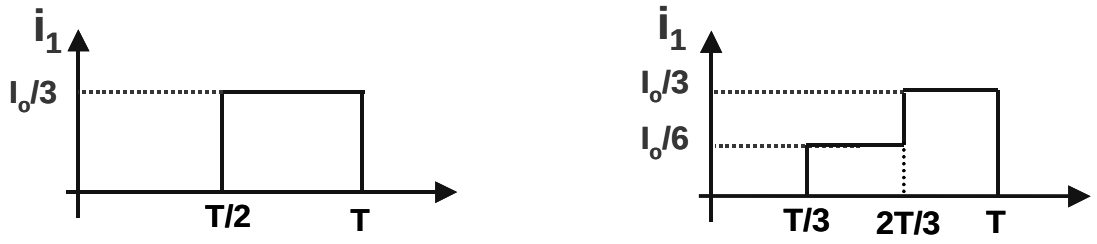


Figure 2.46 SR conduction loss comparison: (a) current-doubler; (b) current-tripler



(a) (b)

Figure 2.47 Current waveforms through one MOSFET: (a) current-doubler; (b) current-tripler

However, the RMS current is different. In order to simplify the calculation of RMS current through one MOSFET, the current ripple of the inductor current is ignored. Therefore, for both topologies the current waveforms through one MOSFET can be derived, as shown in Figure 2.47. The RMS current through one device can be calculated as follows: For the current-doubler, the RMS current through one MOSFET is $\frac{I_o}{6}\sqrt{2}$. For the current-tripler, the RMS current is $\frac{I_o}{6}\sqrt{\frac{5}{3}}$. The total SR conduction loss savings of the current-tripler is about 20%.

Similarly, the transformer secondary winding conduction losses need to be considered. A current-doubler single secondary winding transformer is analyzed first. We assume the winding shapes are round, as shown in Figure 2.48. We also assume the winding copper thickness t is smaller than the skin depth. The DC resistance of the winding can be calculated by integrating the incremental admittance of the slim copper loop with the width of dx. The incremental admittance dY of a copper loop with radius x and width dx is:

$$dY = \frac{t \cdot dx}{\rho \cdot 2 \cdot \pi x} \tag{2.39}$$

where r is the resistivity of the copper. The winding admittance is the integration of dY from r_1 to r_2, such that:

$$Y = \int_{r_1}^{r_2} \frac{t}{\rho \cdot 2 \cdot \pi x} dx = \frac{t \cdot \ln r_2 / r_1}{\rho \cdot 2\pi} \tag{2.40}$$

So the DC resistance R is:

$$R = \frac{\rho \cdot 2\pi}{t \cdot \ln r_2 / r_1} \tag{2.41}$$

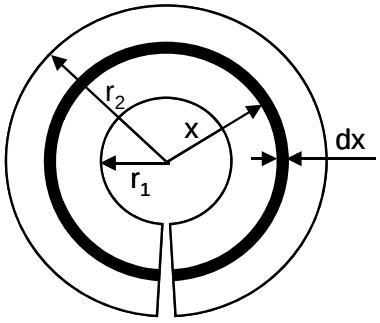


Figure 2.48 Copper winding DC resistance calculation

Equation (2.41) shows that the DC resistance of a round winding is inversely proportional to $\ln(r_2/r_1)$. If the current doubles, for example, in order to keep the same conduction loss, the DC resistance needs to be reduced to one quarter. The outer radius r_2' must increase so that:

$$r_2' = \frac{r_2^4}{r_1^3} \tag{2.42}$$

Supposing $r_2=2r_1$, r_2' will be $16*r_1$. The outer radius of the winding increases significantly in order to maintain the same conduction loss. This is also true for other winding shapes. One solution for this issue is distributed windings. For the current-doubler, three secondary-windings are in parallel. For the current-tripler, three secondary windings are delta-connected, as shown in Figure 2.49. The secondary-side winding current waveforms for both topologies are shown in Figure 2.50. The RMS current through one current-doubler transformer secondary-side winding is $\frac{1}{6}I_o$, and that for the current-tripler is $\frac{\sqrt{2}}{9}I_o$. The total winding conduction loss savings of the current-tripler is about 12.5%.

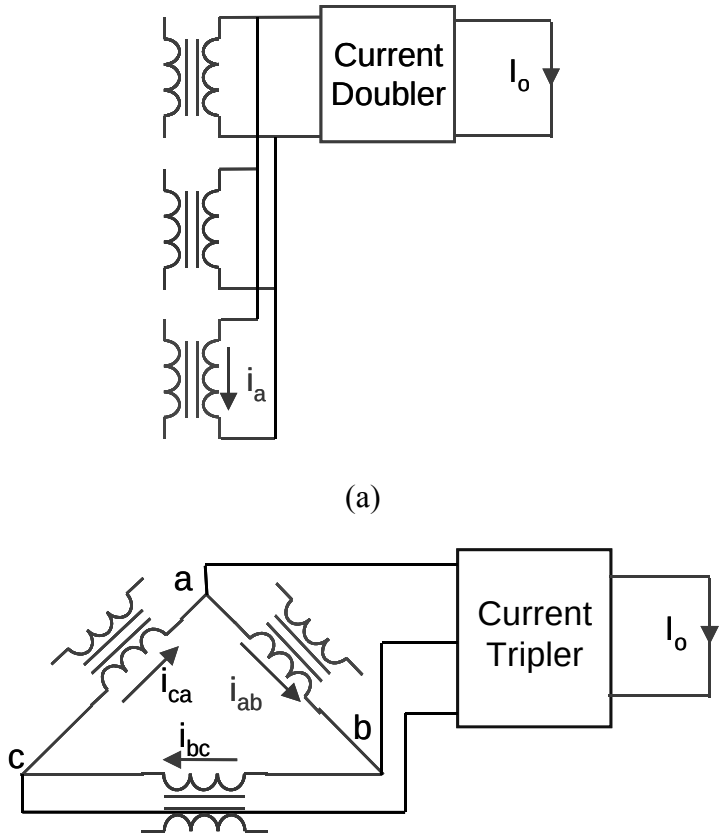


Figure 2.49 Secondary winding structures: (a) current-doubler; (b) current-tripler

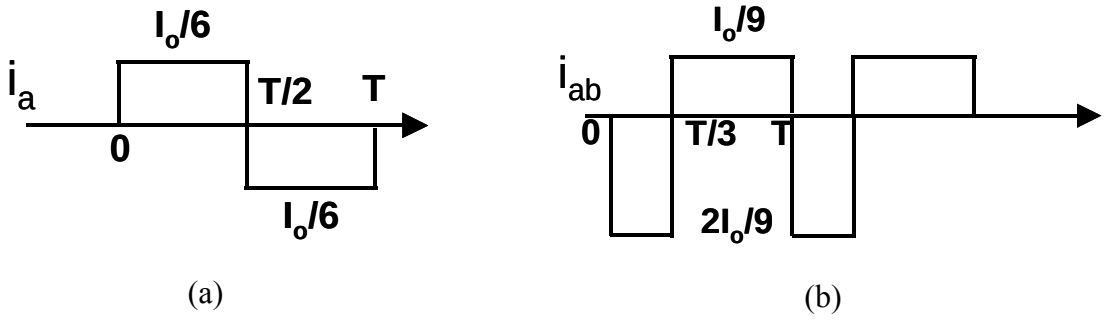


Figure 2.50 Current waveforms through secondary windings: (a) current-doubler; (b) current-tripler

2.3.6. Experimental Results

A prototype is developed to verify the theoretical analysis. The specifications are listed in Table 2.2.

Table 2.2 Prototype specifications

Input voltage	48V
Output voltage	1.0V
Maximum load current	100A
Switching frequency	300kHz

A customized core is used as the current-tripler transformer. A conventional EI32 core is manufactured as follows: First, the center leg is symmetrically grounded so that the cross-sectional areas of the three legs are identical; then, because the effective cross-sectional area of the EI32 core is much larger than what is needed here, it is cut into one-third, so the high-current winding length is reduced. Figure 2.51 shows a picture of the developed prototype. The six primary MOSFETs are Hitachi's HAT2173H, and the 12 secondary devices are HAT2160H. Four MOSFETs in parallel form one switch leg. The inductance of the output inductor is 200nH/channel.

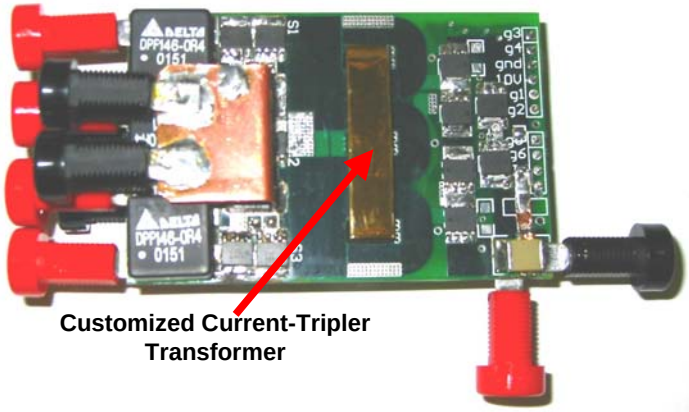


Figure 2.51 Prototype using a customized current-tripler transformer

Figure 2.52 shows the drain-source voltages of the three control MOSFETs at the primary side. They have a 120° phase shift. Basically, it is a three-phase interleaving topology, which means that it has all the benefits of the multiphase interleaving technique that is widely-used for non-isolated 12V-input voltage regulators.

Figure 2.53 shows the primary-side transformer winding voltages. Due to the ZVS, the waveforms are very clean. Figure 2.53 also matches the theoretical waveforms given in Figure 2.42.

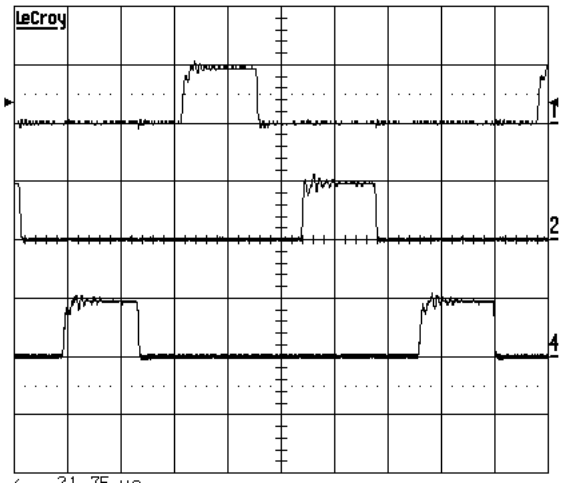


Figure 2.52 Drain-source voltages of three switch legs (50V/div, 0.5ms/div)

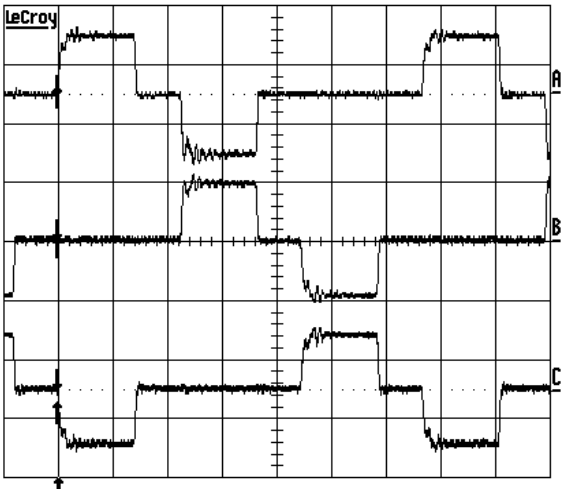


Figure 2.53 Transformer winding voltage (50V/div, 0.5ms/div)

A typical industry design is chosen as the benchmark to compare the efficiency, size and cost with the proposed current-tripler DC-DC converter. It is a phase-shift ZVS full-bridge primary-side topology with conventional current-doubler SRs. Figure 2.54 shows the efficiency curves of the proposed current-tripler DC-DC converter and the conventional current-doubler

DC-DC converter. Both of them are running at 300kHz switching frequency, and have the same output voltage, 1.0V. About 4% efficiency improvement is achieved.

Table 2.3 shows the major component counts breakdown for both converters. It can be seen that in terms of the cost of the components, the two converters are very similar. However, the current-tripler DC-DC converter can deliver more current under the same thermal limitation due to higher efficiency and better thermal distribution than its current-doubler counterpart, which means less dollar per ampere.

Another comparison is made about the total size of the two circuits. Each of them are a two-board structure with the control and protection circuit in one board and the power stage in the other. The measured footprint of the current-tripler is 4.86in^2, which is about a 45% footprint reduction compared with the current-doubler benchmark.

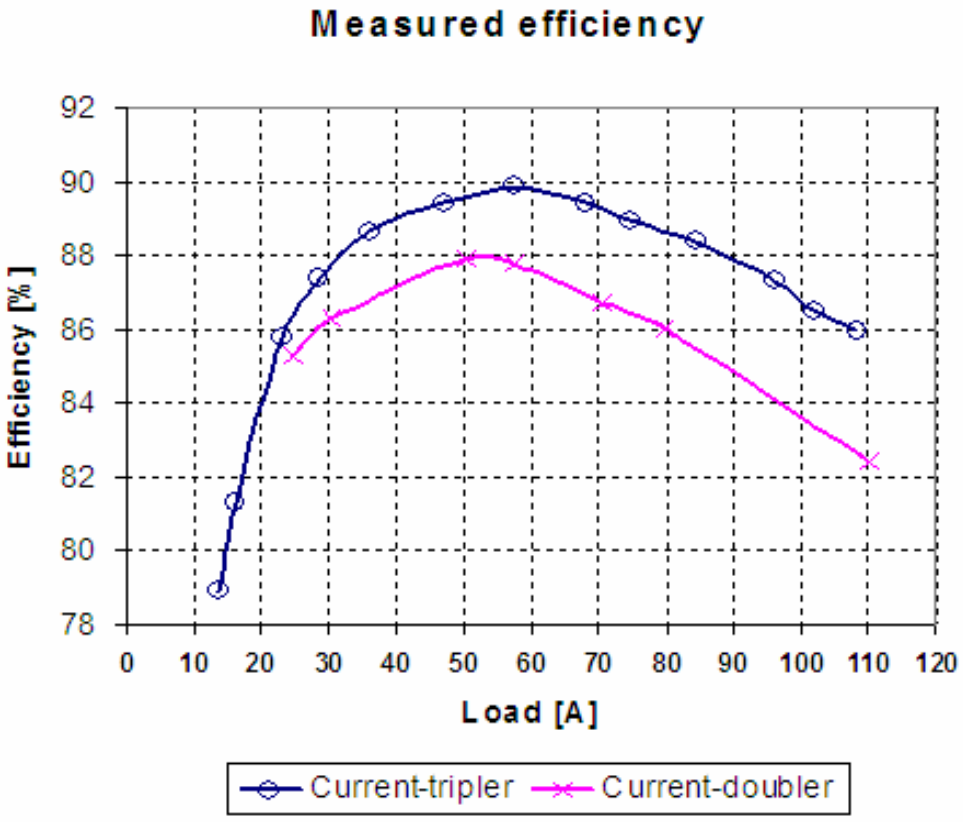


Figure 2.54 Measured efficiency

Table 2.3 Component counts breakdown

	Prim. MOS	Prim. Driver	Sync. Rectifier	Sync. Driver	Transformer	Inductor
Current-tripler	6	3	4x3	6	1/3 of EI32	3, each carries 1/3 of I_o
Current-doubler	4	2	6x2	6	1 EI32	2, each carries 1/2 of I_o

2.4. Combining CCB Self-Driven and Current-Tripler Concepts

Because the proposed current-tripler 48V VRM has three complementary controlled legs at the primary side, it follows the rule of the CCB self-driven concept. Figure 2.55 shows a 48V current-tripler converter with a CCB self-driven scheme. To simplify the implementation, the three drive transformers can be integrated into one magnetic core, as shown in Figure 2.56.

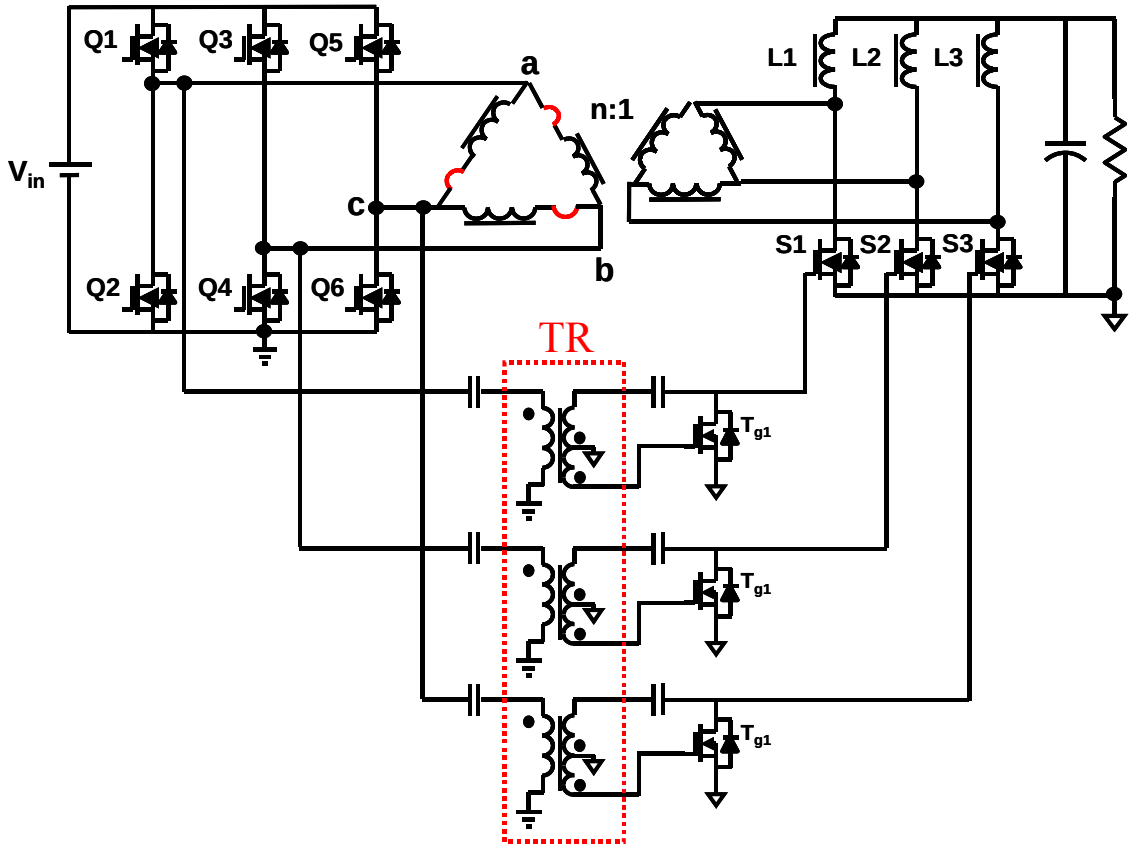


Figure 2.55 48V current-tripler converter with CCB self-driven

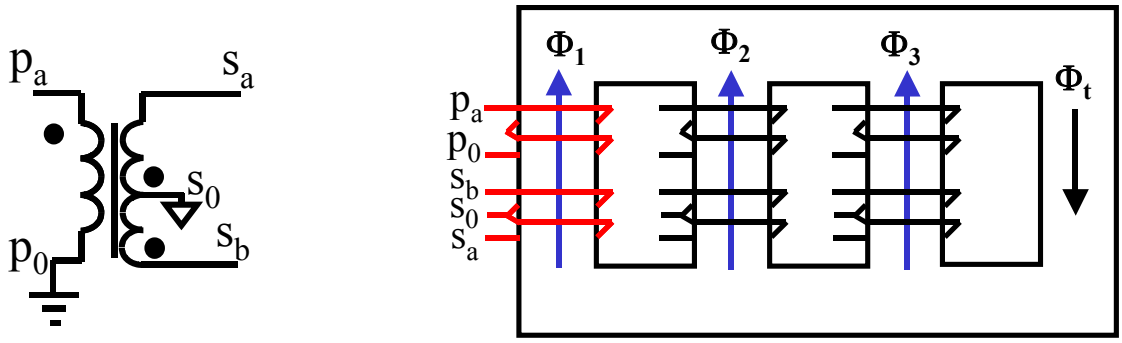
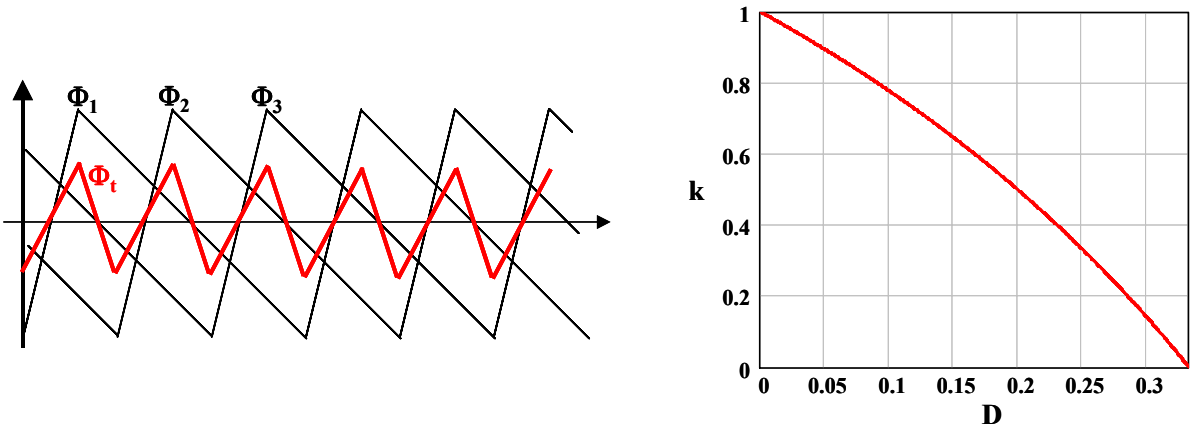


Figure 2.56 The driver transformer and its implementation

The AC component of flux Φ_1 is solely determined by the volt-second applied to the winding p_a-p_0. The DC component of flux Φ_1 is zero because the DC blocking capacitor in series with the winding. Φ_2 and Φ_3 have the same magnitude as that of Φ_1 except for the 120° phase



(a) (b)

Figure 2.57 Flux in each leg (a) and cancellation effect (b)

shift. Figure 2.57(a) illustrates the fluxes through the four transformer legs. The flux cancellation effect is related to the duty cycle D (D<1/3):

$$k = \frac{\Phi_{t_pk}}{\Phi_{1_pk}} = \frac{1-3D}{1-D} \tag{2.43}$$

Figure 2.57(b) shows the relationship between k and D. For a practical design, D is in the range of 1/6-1/3. According to Figure 2.57(b), Φ_t is less than half of Φ_1, therefore, a core leg with a cross section equal to the other legs is sufficient.

2.5. Summary

There are two novel concepts proposed in this chapter: one is the complementary controlled bridge (CCB) self-driven technique which can be applied to the existing soft-switching isolated topologies so that not only is the switching loss dramatically reduced, but the body diode loss and gate driver loss are also reduced; the other concept is the current-tripler DC-DC converter to further improve the system efficiency by reducing the conduction losses. The derivations of the concepts are discussed, and the benefits of the concepts in typical applications are theoretically and experimentally verified.

Chapter 3. High-Frequency High-Current 12V Non-Isolated VRMs

The non-isolated 12V input voltage regulators have much more stringent requirements than the isolated 48V VRMs. This is due to the extreme duty cycle of the conventional multi-phase buck converter running at a higher frequency. Because of the very low output voltage, the duty cycle is narrow, and is predicted to be smaller than 0.1 in the future. This extreme duty cycle impairs the VR's efficiency and imposes obstacles for the transient response [8, 12, 14]. Also, in terms of control, to generate the very narrow duty cycle the control IC must incorporate a very fast comparator, which may cause some cost increase. Moreover, the extreme duty cycle may even cause malfunctions at high switching frequencies due to the very short conduction time for the top switch. The natural solution is to extend the duty cycle by means of inserting a step-down transformer. For instance, if the duty cycle is extended, as shown in Figure 3.1, the top switch

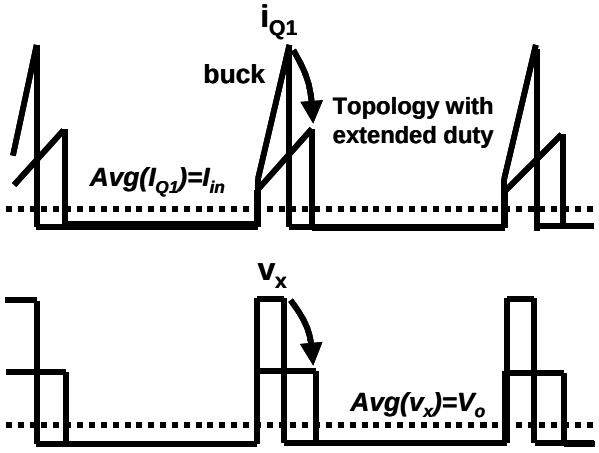


Figure 3.1 Waveforms when the duty cycle is extended

average current remains the same because it is determined only by the output power. But with a larger duty cycle, the peak value is dramatically reduced, which means there will be much less switching loss. In the meantime, the "phase" voltage waveform is also different. To obtain the same average value—the specified output voltage—with a larger duty cycle means that V_x is lower. This reduces the bottom switch reverse-recovery loss as well.

The duty cycle extension concept was implemented by various type of converters, such as the tapped-inductor buck converter [21], the active-clamp couple-buck converter [22], the push-pull buck converter [26], the winding coupled buck converter [27], and the phase-shifted buck converter [28]. Among these converters, the phase-shifted buck appears to be the most efficient topology for high frequency applications due to its soft switching capability.

One major concern of the phase-shifted buck is that the driving scheme for both the phase-shifted bridges and the SRs are very complicated. Meanwhile, the large circulating energy helps to achieve soft switching, but increases the conduction losses. As discussed in the previous chapter, self-driven scheme can help solving these problems.

The CCB self-driven concept and the current-tripler concept can also be applied to the non-isolated 12V input voltage regulators. In this chapter, a novel 12V non-isolated VRM with the CCB self-driven scheme is derived. The proposed topology is basically a buck-derived soft-switching topology with duty cycle extension and SR device self-driven capabilities. Because there is no isolation requirement, the SR gate driving becomes so simple that the voltage at the complementary controlled bridge can be used to drive the SR gate. Both the gate driving loss and the SR body diode conduction loss are reduced. When compared to a conventional 300kHz buck converter, the proposed circuit achieves similar overall efficiency running at 1MHz.

There are several derivative circuits proposed in Chapter 3 following the CCB self-driven concept. One is the autotransformer version of the circuit, which is designed mainly to deal with the transformer winding loss. The other one integrates the output filter inductors with the transformer to further simplify the circuit.

Finally, the derivation from the isolated current-tripler to the non-isolated current-tripler is discussed. There are two ways to drive its synchronous rectifiers. The first method is to drive externally, which is simple to implement but dissipative. The other method is to use a CCB self-driven idea. In order to meet the requirements of the CCB self-driven scheme, we have to modify the non-isolated current-tripler to an autotransformer version. The SR driver loss is lower than the first method, but an additional level shift circuit is needed in the driving path, which somewhat increases the complexity.

3.1. 12V Non-Isolated VRM with CCB Self-Driven Scheme

3.1.1. Derivation of the 12V Non-Isolated VRM with CCB Self-Driven Scheme

The 48V isolated VRM with CCB self-driven scheme is redrawn in Figure 3.2(a). When the input becomes 12V, isolation is no longer required. Therefore, the primary and the secondary sides share the same ground, and the gate driver transformers are eliminated, as shown in Figure 3.2(b). Figure 3.2(b) is then rearranged as shown in Figure 3.2(c).

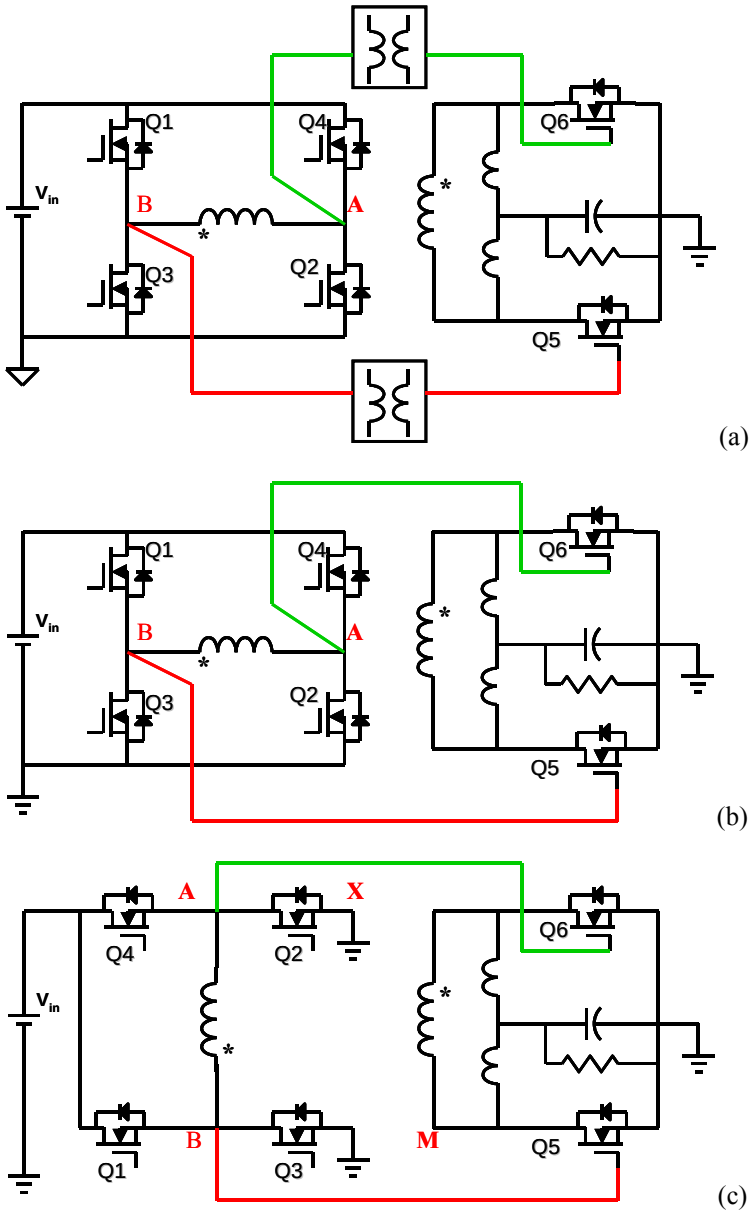


Figure 3.2 Derivation from isolated CCB self-driven converter to non-isolated version

The circuit shown in Figure 3.2(c) can be further simplified. Node X needs grounding only when Q2 is on. Otherwise it can be connected to any potential lower than V_{in}. Meanwhile, Q5 is always on during the Q2 on period. Disconnecting node X and the ground in Figure 3.2(c) then connecting node X with node M will not influence the circuit operation. Figure 3.3 shows the complete circuit of the proposed CCB self-driven 12V VRM.

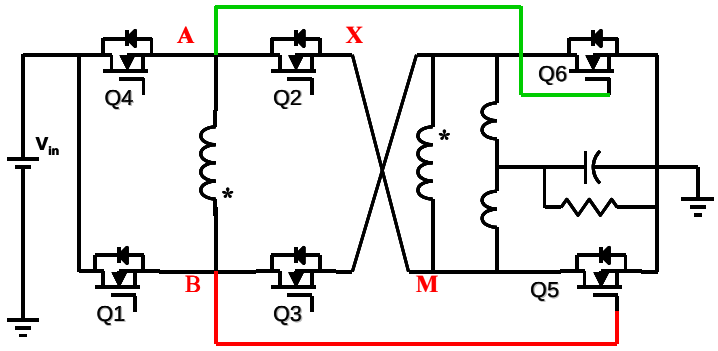


Figure 3.3 Proposed CCB Self-driven 12V VRM

3.1.2. Operating Principles

Figure 3.4 redraws the circuit shown in Figure 3.3. The following analysis in this chapter will use this schematic drawing.

In order to achieve zero voltage switching and to find suitable voltage waveforms in the power stage to drive the synchronous rectifier MOSFETs, a complementary control strategy for Q1-Q4 is used. The switch timing diagram for the switches Q1-Q4 and secondary synchronous

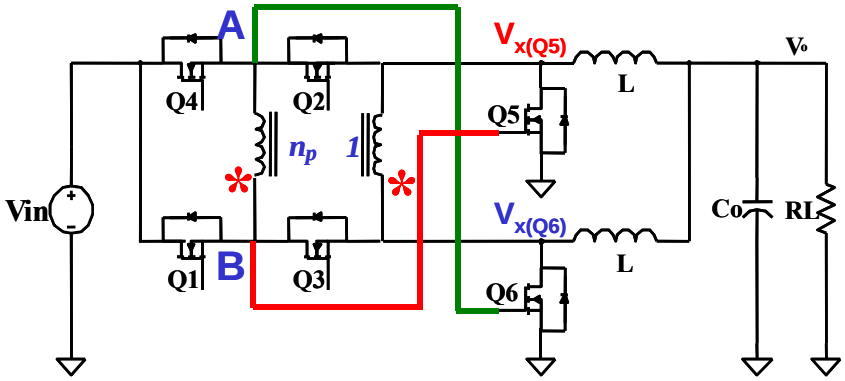


Figure 3.4 Proposed CCB Self-driven 12V VRM (redrawn)

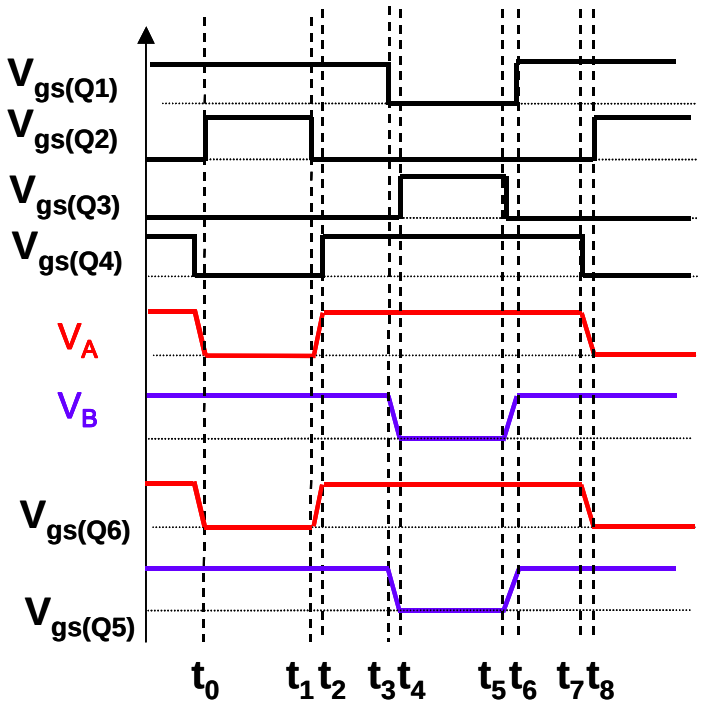


Figure 3.5 Control strategy of ZVS Self-driven 12V VR

rectifier switches Q5-Q6 are shown in Figure 3.5. From Figure 3.5, the on time of Q1 is complementary to that of Q3, with a fixed dead time to achieve ZVS. The same is true of the switches Q2 and Q4. Here, the output voltage is regulated by control of the duty cycle of Q2 and Q3. The larger the duty cycle is, the higher the output voltage will be.

Since Q1, Q2, Q3 and Q4 are not connected to ground, and all of them need external driver circuitry, it seems very complex. However, due to the complementary control we use, a simple boot-strap driving scheme can be adopted to drive the control MOSFETs Q1(Q4) and Q3(Q2), as shown in Figure 3.6(a). Take the Q1-Q3 leg as an example. According to Figure 3.5, when Q3 is on, Q6 is also on so that the source of Q3 is actually connected to ground through Q6. Meanwhile, the bootstrap capacitor C_{boot} is charged by Vcc through Q3 and Q6. During Q3's off period, the gate voltage of Q3 is pulled to zero by the driver IC, and its source voltage is either zero when Q6 is on, or equal to V_{in}/n_p when Q6 is off. In both cases, Q3 can be turned off properly. Figure 3.6(b) illustrates the gate-to-source voltages of Q1 and Q3 respectively. The same driving circuitry is used for the Q2-Q4 leg.

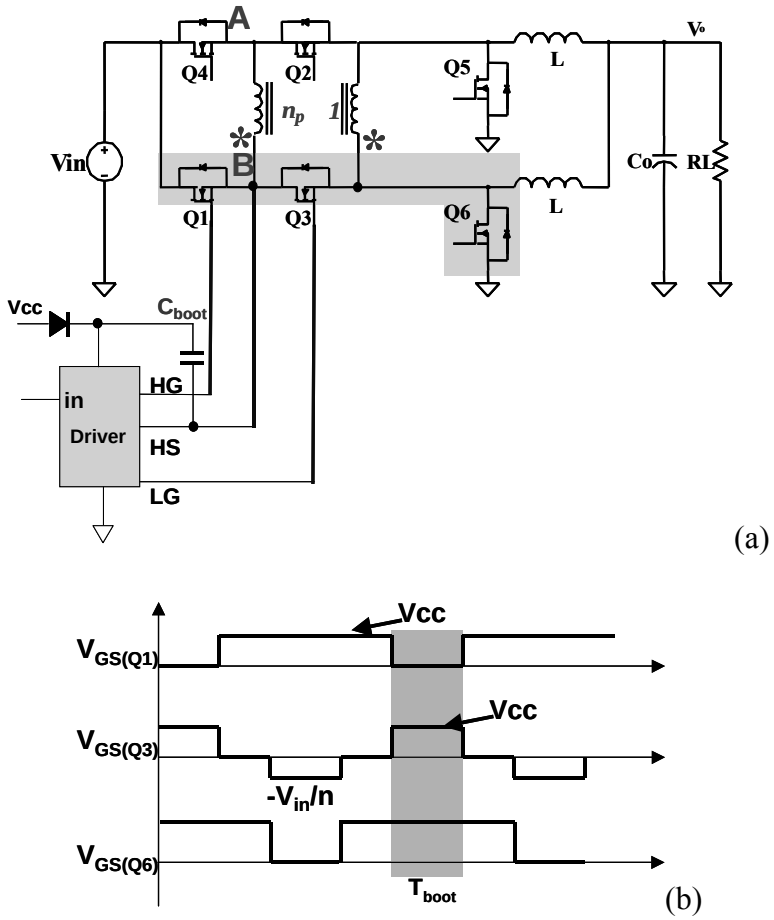


Figure 3.6 Simple boot-strap driving scheme for control MOSFETs. (a) Schematic; (b) Gate-to-source voltage waveforms of Q1, Q3 and Q6

Based on the switch-timing diagram, there are eight operating modes during one switching cycle. Figure 3.7 illustrates the equivalent circuits for Mode1 through Mode4. During the other half of the switching cycle, the circuit operates in the same way as in Mode1 to Mode4.

In Mode1 [t_0-t_1], Q1 and Q2 are on. The voltage at point B is actually the input voltage, which is 12V. Because point B is directly connected to the gate of Q5, Q5 is self-driven to be on. On the other hand, since Q2 and Q5 are both on, point A is connected to the ground that automatically keeps Q6 off during this operating mode. The energy is transferred from the input to the output through the transformer.

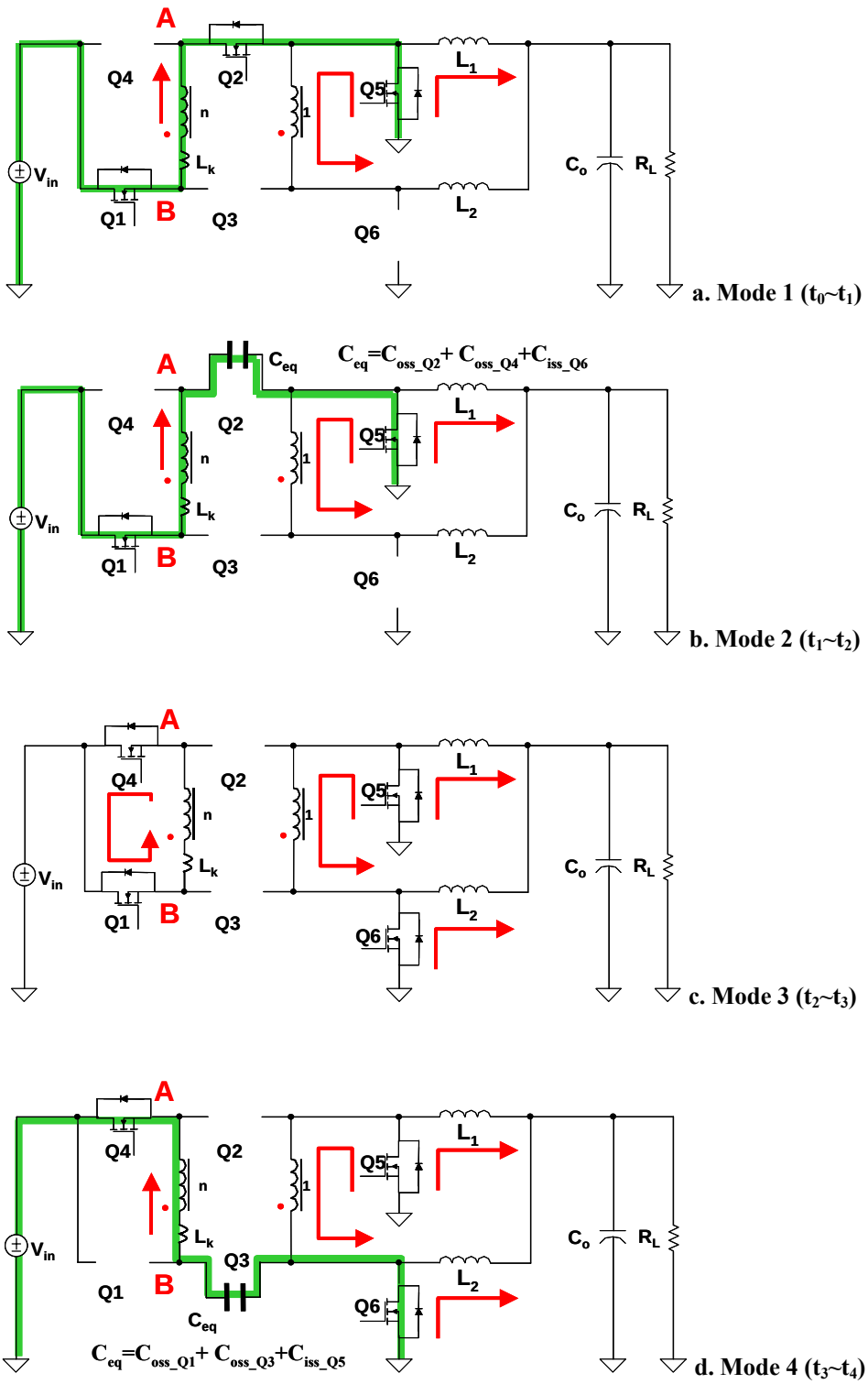


Figure 3.7 Operation modes of the 12V self-driven VR

In Mode2 [t_1-t_2], Q2 turns off at t_1, and the reflected output current discharges and charges the output capacitor of Q4 and Q2, respectively. Meanwhile, because Q5 stays on during this interval, the gate capacitor of Q6 is actually in parallel with the output capacitor of Q2, and is charged by the reflected load current as well. Given a suitable dead time t_{d1}, which is:

$$t_{d1} = \frac{2n_p C_{eq} V_{in}}{I_{o_min}} \tag{3.1}$$

the drain-to-source voltage of Q4 will drop to zero so that Q4 can be turned on under zero voltage switching. Where n_p is the transformer turn's ratio, C_{eq} is the sum of the output capacitance of Q2 and Q4 plus the gate-to-source capacitance of Q6, V_{in} is the input voltage, and I_{o_min} is the minimum load current at which the ZVS can still be achieved. The gate capacitor of Q6 serves as a lossless snubber of Q2.

In Mode3 [t_2-t_3], The energy stored in the transformer leakage inductor freewheels through Q1 and Q4. Since both point A and point B are connected to the input, Q5 and Q6 are on during this mode, which provide the current freewheeling paths for the synchronous rectifier.

In Mode4 [t_3 -t_4], Q1 turns off at t_3. The leakage inductor of the transformer resonates with the output capacitors of Q1 and Q3, and similarly the gate capacitor of Q5 joins the resonance because it is in fact in parallel with the output capacitor of Q3. In order to achieve ZVS for Q3, two conditions are necessary: the appropriate dead time between Q1 and Q3, which is one-fourth of the self-resonant period; and the energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output capacitances as well as the gate capacitance of Q5. These two conditions can be expressed as:

$$t_{d2} = \frac{\pi\sqrt{L_k C_{eq}}}{2} \tag{3.2}$$

$$I_{o_min} = \sqrt{\frac{2n_p C_{eq} V_{in}^2}{L_k}} \tag{3.3}$$

Where L_k is the leakage inductance of the transformer reflected to the primary side, and I_{o_min} is the minimum output current needed to achieve ZVS.

From t_4 to t_8, another half-period starts, and the operation principle is the same except for polarity changes. It should be noted that not only can the proposed circuit achieve ZVS, but the voltage waveforms at point A and B are also exactly those desired to drive the synchronous rectifier MOSFETs.

3.1.3. Power Loss Analysis of the Proposed Self-Driven Scheme

The objective of the power loss analysis is to discuss the pros and cons of the proposed self-driven scheme in comparison with the conventional multi-phase buck converter. In order to make a fair comparison, both circuits are composed in such a way that exactly the same power MOSFETs are used, as shown in Figure 3.8. The additional part in the proposed circuit is the transformer.

3.1.3.1. Loss Savings by Duty Cycle Extension

As illustrated in Figure 3.1, the extension of the duty cycle can reduce switching loss as well as SR body diode reverse-recovery loss. The total switching losses of the four control FETs in Figure 3.8b can be estimated as follows: [136]

$$P_{sw} = I_o \cdot \frac{Q_{gd}}{i_g} \cdot V_{in} \cdot f_s + I_o \cdot \frac{Q_{gs2}}{i_g} \cdot V_{in} \cdot f_s + Q_{oss} \cdot V_{in} \cdot f_s \tag{3.4}$$

where Q_{gd}, Q_{gs2}, Q_{oss}, and i_g are the quantities of one control FET. Note that Q_{gs2} is a sub-element of Q_{gs}, indicating the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to the maximum value, at which time the drain voltage begins to change.

The corresponding switching losses of the four control FETs in Figure 3.8a can also be calculated. Because of the zero voltage turn-on, the turn-on loss is ignored. The total switching loss is:

$$P_{sw} = \frac{1}{n_p} \cdot \left(I_o \cdot \frac{Q_{gd}}{i_g} \cdot V_{in} \cdot f_s + I_o \cdot \frac{Q_{gs2}}{i_g} \cdot V_{in} \cdot f_s \right) \tag{3.5}$$

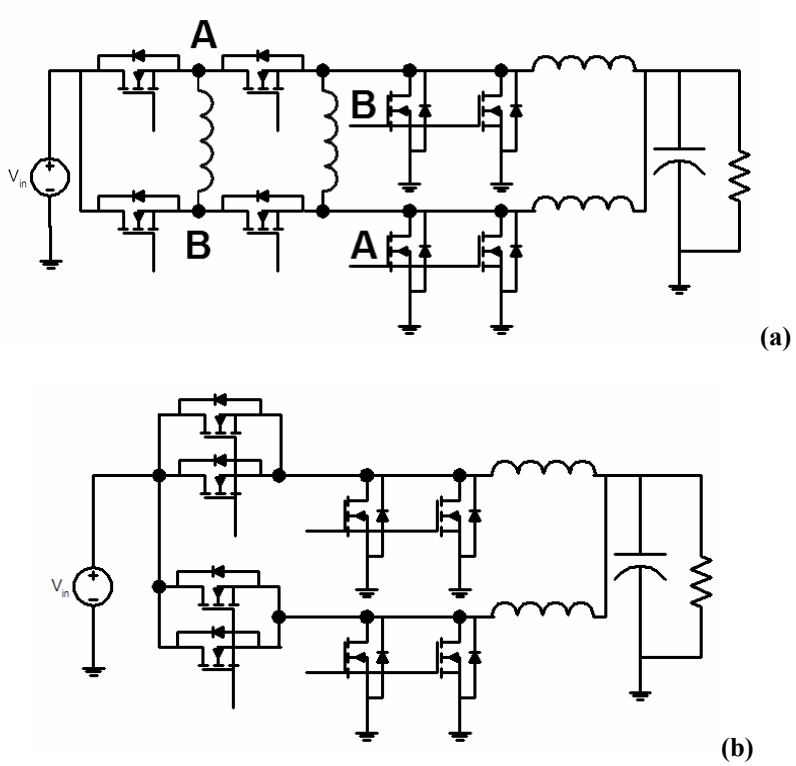


Figure 3.8 Two topologies under comparison. (a) Proposed self-driven circuit; (b) Conventional buck converter

Q_{gs2} in (3.5) is also smaller than in (3.4) because a lesser charge is needed to reach the gate voltage at which the smaller drain current is running through the switch. In a practical design with n_p=3, at least 66% of the total switching loss is saved.

The reverse recovery loss is calculated as:

$$P_{rr} = Q_{rr} \cdot V_{sw} \cdot f_s \tag{3.6}$$

where V_{sw} is the high-level voltage at the switching node. Since the proposed circuit reduces V_{sw} by n_p times, the reverse recovery loss is also reduced by n_p times.

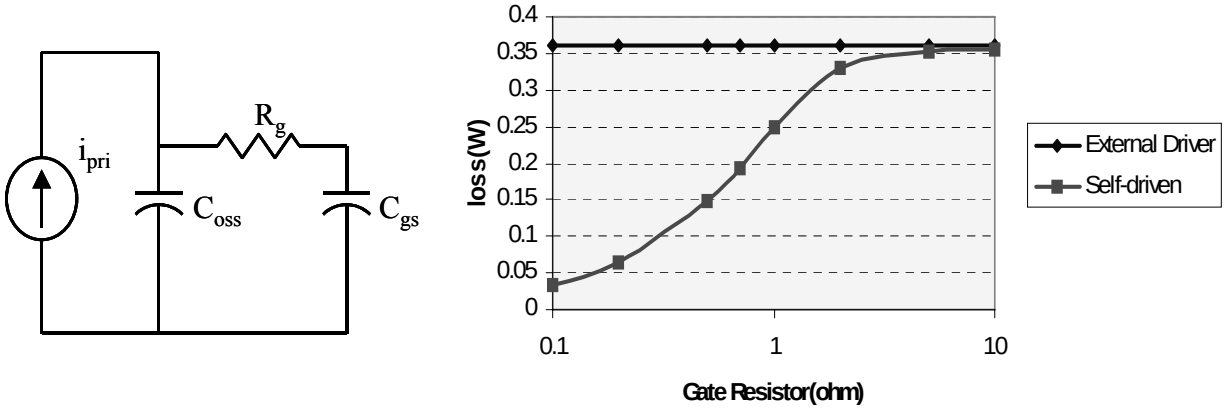
3.1.3.2. Synchronous Rectifier Driver Loss Reduced

Based on the above analysis, both turn-on and turn-off processes of the synchronous rectifiers are driven by the power stage itself: the turn-on of Q6 is illustrated in Figure 3.7(b), and the turn-off of Q5 is illustrated in Figure 3.7(d). Both the turn-on and turn-off gate driving loss can be reduced, as discussed below:

Turn-on of Q6: The equivalent gate driver circuit of the turn-on of Q6 can be easily derived from Figure 3.7(b), as shown in Figure 3.9(a). A current source I_{pri} represents the primary winding current, which is assumed to be constant during this short transition period. C_{oss} is the sum of the output capacitors of Q2 and Q4. C_{gs} is the gate capacitor of Q6. R_g is the gate resistor of Q6. The turn-on driver loss of Q6 is then calculated based on the total energy dissipation on R_g when the voltage across C_{gs} rises from zero to V_{in}.

Let us take a Renesas' HAT2165 MOSFET as an example. Operating at 1MHz, the gate driver loss reduction during turn-on by using the proposed self-driven scheme is shown in Figure 3.9(b). The typical gate resistance value for this device is 0.5ohms, which means about 60% less loss than the external driving scheme.

Turn-off of Q5: Similarly, the equivalent gate driver circuit of the turn-off of Q5 can also be derived from Figure 3.7(d), as shown in Figure 3.10(a). The energy stored in the transformer leakage inductor L_{lk} helps to discharge C_{oss} and C_{gs}. Assuming that ZVS is achieved at a certain load condition, the gate capacitor of Q5 is fully discharged to turn off the device. It is important that the energy stored in L_{lk} , C_{oss} and C_{gs} are transferred back to the source despite some portion of the energy being dissipated on R_g. Figure 3.10(b) shows the gate driver loss reduction during turn-off by using the proposed self-driven scheme. Here we again take Renesas' HAT2165 as an example, operating at 1MHz.



(a) (b)

Figure 3.9 Turn-on driver losses for self-driven and external driven SR devices. (a) Turn-on equivalent circuit of self-driven SR devices; (b) Turn-on driver loss comparison

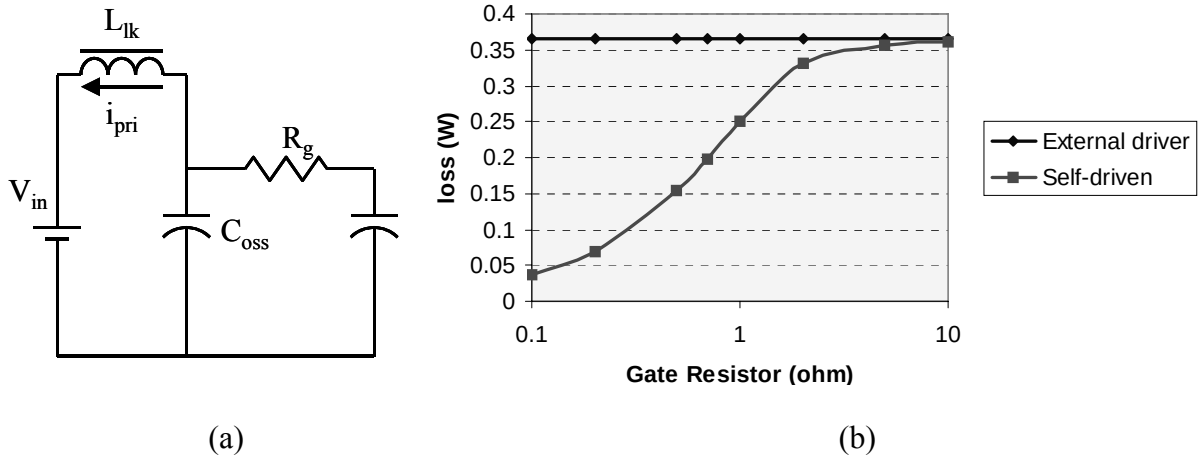


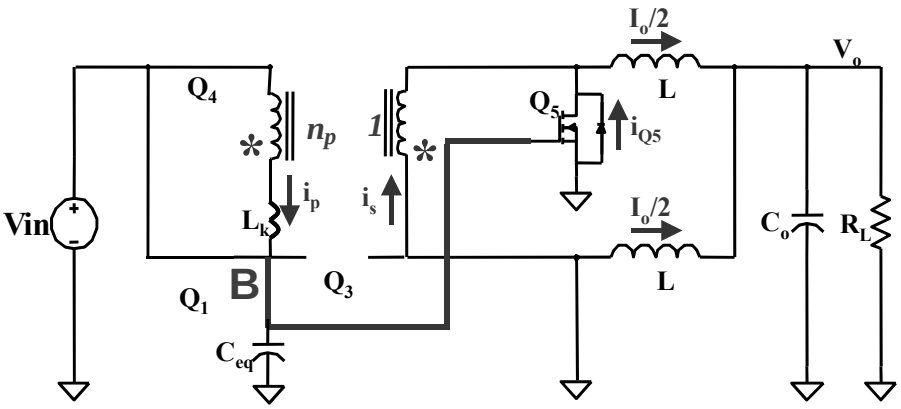
Figure 3.10 Turn-off driver losses for self-driven and external driven SR devices. (a) Turn-off equivalent circuit of self-driven SR devices; (b) Turn-off driver loss comparison

Generally speaking, as the output current continues increasing, the synchronous rectifier MOSFETs must have an extremely low on resistance, which results in a larger gate charge of those devices so that their driver ICs become hot spots. The self-driven scheme eliminates this problem because the only devices need to be externally driven are the control MOSFETs, which have much lower gate charge and consume much less power than synchronous rectifier MOSFETs.

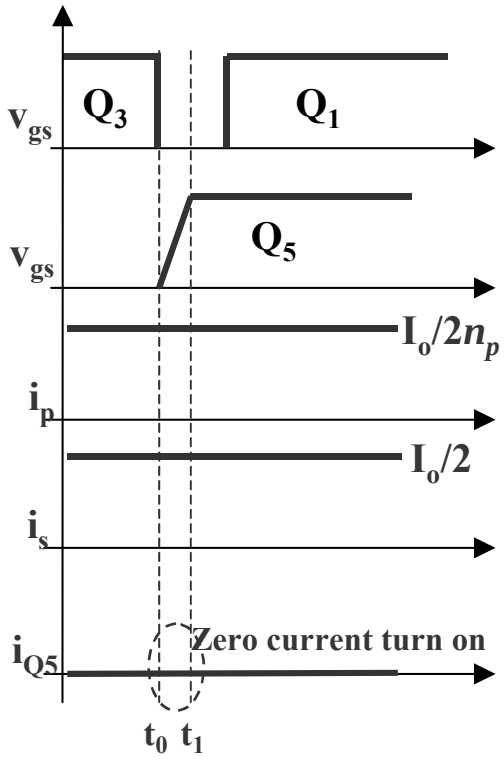
3.1.3.3. Synchronous Rectifier Body Diode Conduction Loss Reduced

Another major benefit of the self-driven concept is that it can reduce the body diode conduction loss. The basic idea is that there is no need to set a dead time between the control MOSFET and synchronous rectifier MOSFET to avoid the shoot-through problem as conventional external drivers usually do. The synchronous rectifier MOSFET is turned on and off adaptively; furthermore, there is no driver delay. Figure 3.11 and Figure 3.12 show the equivalent circuits and their key waveforms during the synchronous rectifier MOSFETs's turn-on and turn-off intervals. The transition periods are magnified in the diagram. To simplify the analysis, let us assume the inductance of the converter output inductor L_o is much larger than the transformer leakage inductor L_k, so that the output inductor current can be considered as an ideal current source. In addition, except for the transformer leakage inductor L_k and the equivalent

capacitor C_{eq} (the output capacitors of Q1 and Q3 plus the input capacitor of Q5), all other circuit parasitic components are ignored in the analysis.



(a)



(b)

Figure 3.11 Equivalent circuit and key wave forms during Q5 turn-on interval. (a) Equivalent circuit during Q5 turn-on interval; (b) Key wave forms during Q5 turn-on interval

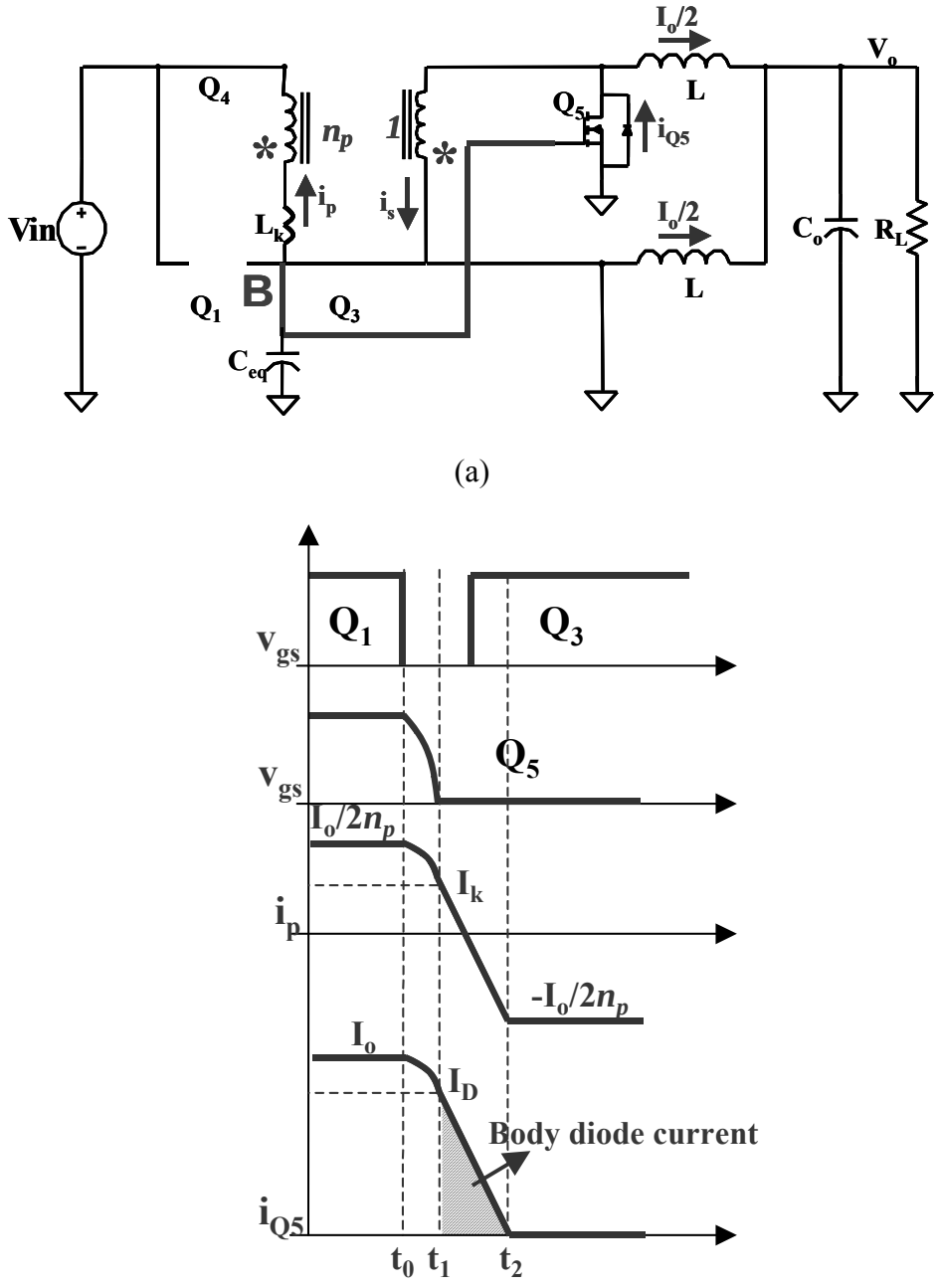


Figure 3.12 Equivalent circuit and key wave forms during Q5 turn-off interval. (a) Equivalent circuit during Q5 turn-off interval; (b) Key wave forms during Q5 turn-off interval

Figure 3.11(a) and Figure 3.11(b) show the switching interval when Q3 is turned off at t_0. The reflected current ($I_o/2n_p$) linearly charges C_{eq} until it reaches V_{in} at t_1. Q5 is automatically turned on at t_1. Because of the transformer leakage inductor, i_p continues to flow through Q4 and

Q1. Although Q5 has already been turned on during the dead time between Q1 and Q3, there is no current running through it. Therefore, the body diode of Q5 carries no current during Q5's turn-on interval.

Figure 3.12(a) and Figure 3.12(b) show the switching interval when Q1 is turned off at t_0. The transformer leakage inductor L_k begins to resonate with C_{eq} until the voltage at point B drops to zero at t_1. Q5 is automatically turned off at t_1. However, the current through Q5 continues to flow until the current through the transformer primary side winding changes its polarity from $I_o/2n_p$ to $-I_o/2n_p$ at t_2. From t_1 to t_2, the body diode of Q5 conducts the current and the body diode conduction loss for Q5 can be calculated as follows:

$$P_D = 0.5 I_D \cdot \Delta t \cdot V_F \cdot f_s \tag{3.7}$$

where V_F is the body diode forward voltage drop, typically 0.7V, and fs is the converter switching frequency.

$$I_D = \frac{I_o}{2} \cdot \left(1 + \sqrt{1 - \left(\frac{2 n_p V_{in}}{I_o Z_k} \right)^2} \right) \tag{3.8}$$

$$\Delta t = t_2 - t_1 = \frac{L_k I_o}{2 n_p V_{in}} \cdot \left(1 + \sqrt{1 - \left(\frac{2 n_p V_{in}}{I_o Z_k} \right)^2} \right) \tag{3.9}$$

I_o is the load current of two phases. Z_k is the characteristic impedance of L_k and C_{eq}. The body diode conduction loss comparison is between two specific designs: one is the conventional multi-phase buck converter, and the other is the proposed self-driven topology. The buck converter uses two phases in order to be comparable with the current-doubler structure in the self-driven topology. Assuming both of them deliver 50A current at 1MHz switching frequency, and the dead time between the top switch and the bottom switch is 20ns, the total body diode conduction loss of the buck converter is:

$$P_D = 50A \times 2 \times 20ns \times V_F \cdot f_s = 1.4W \tag{3.10}$$

For the self-driven topology, let us use the same number of synchronous rectifier devices, so that C_{eq} is about 10nF. The transformer leakage inductor, reflected to the primary side, is

estimated to be 25nH for each. The turn's ratio n_p is 3. According to equations (3.7), (3.8), and (3.9), the total body diode conduction loss of the two SRs is:

$$P_D = 2 \times 0.5 \times I_D \cdot \Delta t \cdot V_F \cdot f_s = 0.607\text{W} \tag{3.11}$$

Figure 3.13 shows the total body diode conduction loss compared with the conventional multi-phase buck converter. The key parameter here is the transformer leakage inductance. By using a fully-interleaved PCB winding, the leakage inductance can be minimized, which in turn

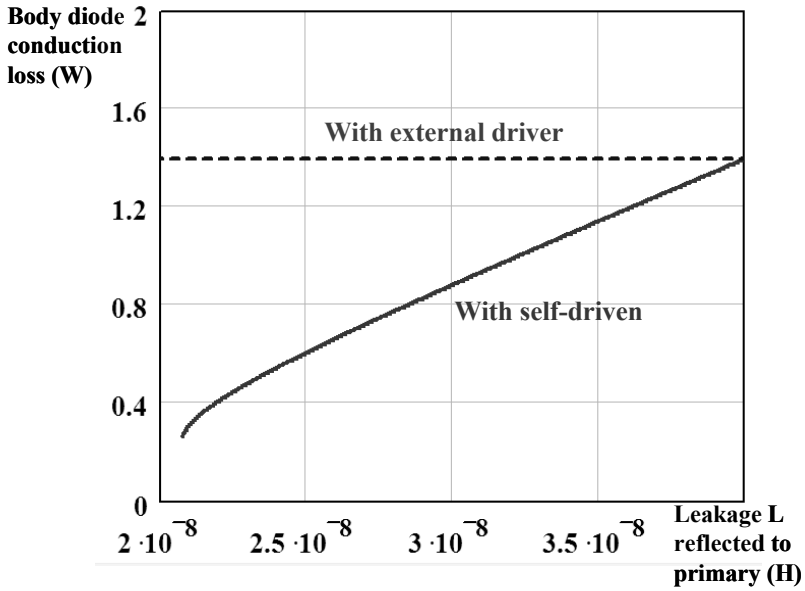


Figure 3.13 Body diode conduction loss compared with the conventional multi-phase buck converter

reduces body diode conduction loss. On the other hand, reducing the leakage inductance will also reduce the duty cycle loss, an important issue when the switching frequency is pushed higher and higher. Figure 3.14 shows the relationship between the duty cycle loss and the leakage inductance as the switching frequency varies from 1MHz to 3MHz.

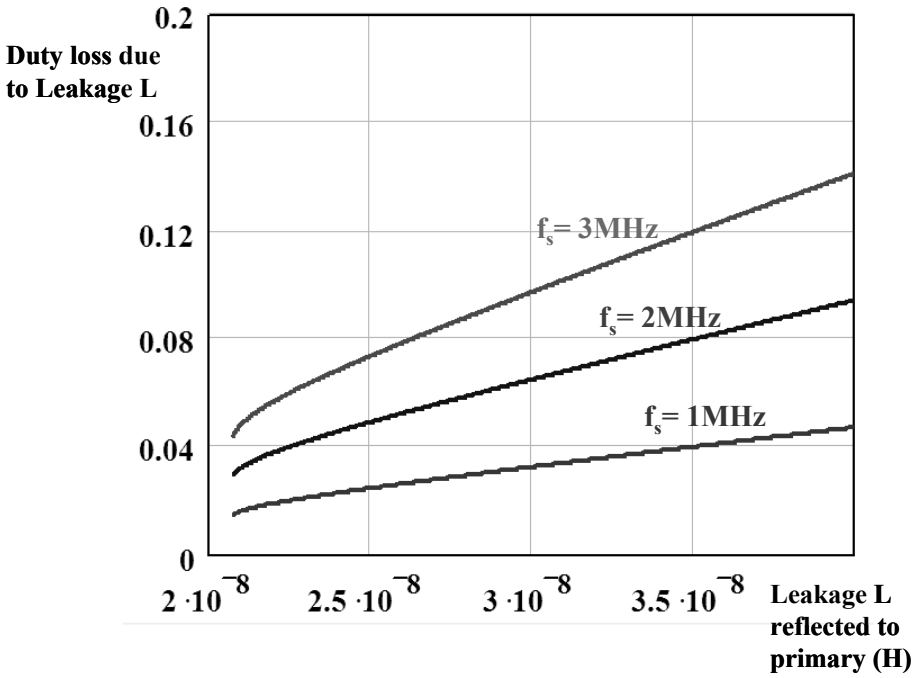


Figure 3.14 Duty cycle loss due to the leakage inductance

3.1.3.4. Additional Losses

Although there are significant loss reductions by using the proposed topology, an additional loss, transformer loss, has to be taken into account. A TDK EIR14 (PQ50 material) core is used. Primary windings have three turns, which are interleaved with the secondary windings, consisting of three parallel turns. All these windings are implemented with a printed circuit board to minimize the leakage inductance.

The winding AC resistance can be measured by an impedance analyzer. During measurement, the secondary-side winding is shorted, and the AC resistance R_{wac} measured from the primary side is actually the total resistance including the primary winding and the reflected secondary winding. The current through the primary winding can be treated as a symmetrical square wave, with an amplitude of half the load current divided by the turn's ratio. Here the output ripple current is again ignored. Thus the transformer winding conduction loss is:

$$P_{tr_cond} = \left(\frac{I_o}{2n_p}\right)^2 R_{wac} \tag{3.12}$$

The measured R_{wac} at 1MHz is 12mΩ. With a 50A load current, the winding conduction loss is about 0.83W. The transformer core loss is calculated using the empirical formula below [63]:

$$P_{tr-core} = V_e C_m f_s^{\,x} B_{pk}^{y} \tag{3.13}$$

and

$$B_{pk} = \frac{DV_{in}}{2n_p A_e f_s} \tag{3.14}$$

For the selected TDK EIR14 (PQ50 material) core, V_e =348mm3, A_e= 22.5 mm2, C_m = 0.0087, x=2.045, and y=2.98. The calculated core loss is about 0.162W.

One concern of the circuit in Figure 3.8(a) is the control FETs' conduction loss. Unlike the parallel connection of the control FETs in Figure 3.8(b), there are two control FETs in series in the proposed topology. The estimated control FETs' conduction loss of the buck converter in Figure 3.8(b) is:

$$P_{ctrl_cond} = \frac{1}{4} I_o^2 D R_{ds} \tag{3.15}$$

Where R_{ds} is the on resistance of one control FET. The estimated control FETs' conduction loss of the proposed converter in Figure 3.8(a) is:

$$P_{ctrl_cond} = \frac{1}{2n_p^2} I_o^2 R_{ds} \tag{3.16}$$

For a converter with n_p=3, I_o=50A, V_{in}=12V, V_o=1.3V, and R_{ds}=8.8mΩ, the increased conduction loss is about 0.626W.

Overall, the proposed topology significantly reduces the switching-frequency-related losses: the control FETs' switching loss, the SR gate driver loss, the SR body diode conduction loss, and the SR body diode reverse-recovery loss. Although additional conduction losses have to be taken into account, the overall performance is very promising, especially as the switching frequency increases further.

3.1.4. Experimental Results

Figure 3.15 shows the prototype of a 1U 1MHz VRM (6-layer, 2oz copper). Figure 3.16(a) shows the drain-source voltage and gate-source voltage for one control switching (Q3). The drain-source voltage drops to zero before the gate voltage begins to rise. Zero voltage switching is achieved for Q3. Figure 3.16(b) shows the drain-source voltage and gate-source voltage for one synchronous rectifier (Q5). The drive voltage level is 12V, so the MOSFET $R_{ds(on)}$ is lower than the 5V driver. It is important to observe the subtle difference between the rising edge and falling edge of the SR drain-to-source voltage. For the rising edge, there exists the dead time during which the body diode conducts, as illustrated in Figure 3.12(b). However, for the falling edge, the gate voltage applies before the SR drain voltage reaches zero. There will be no body diode conduction during this interval.

Figure 3.17 shows the efficiency of the prototype in comparison with the multi-phase buck using the same type and number of devices. Both of them have 12V input and 1.3V output, with 100A output current at 1MHz switching frequency (2MHz ripple frequency). About 3% efficiency improvement was achieved.

The transient performance of the prototypes is also tested to demonstrate the benefit of high bandwidth. Figure 3.18 shows the measured loop gain and phase plot of the converter. For this 1MHz switching frequency design, about 170kHz bandwidth is achieved with 50-degree phase margin. Figure 3.19 shows the tested load transient waveforms. A load emulator was built to generate 75A load step at a slew rate of 100A/us. Two 470uF SP capacitors from Panasonic are used as the bulk decoupling capacitors, which is about one-fifth of the capacitance of that of a conventional 300kHz VRM. The load line is designed to have 1mohm active droop resistance.

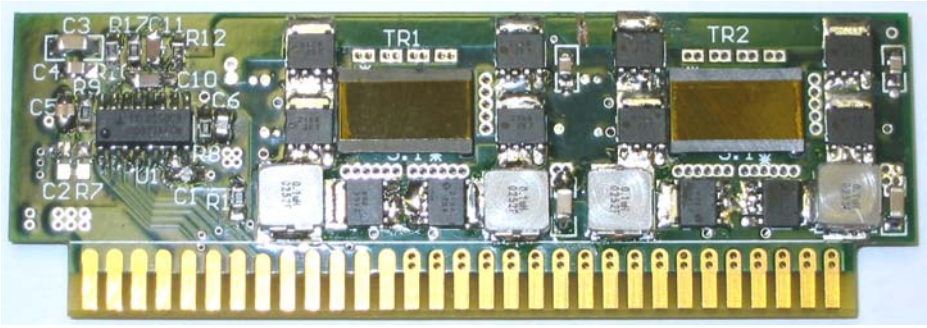
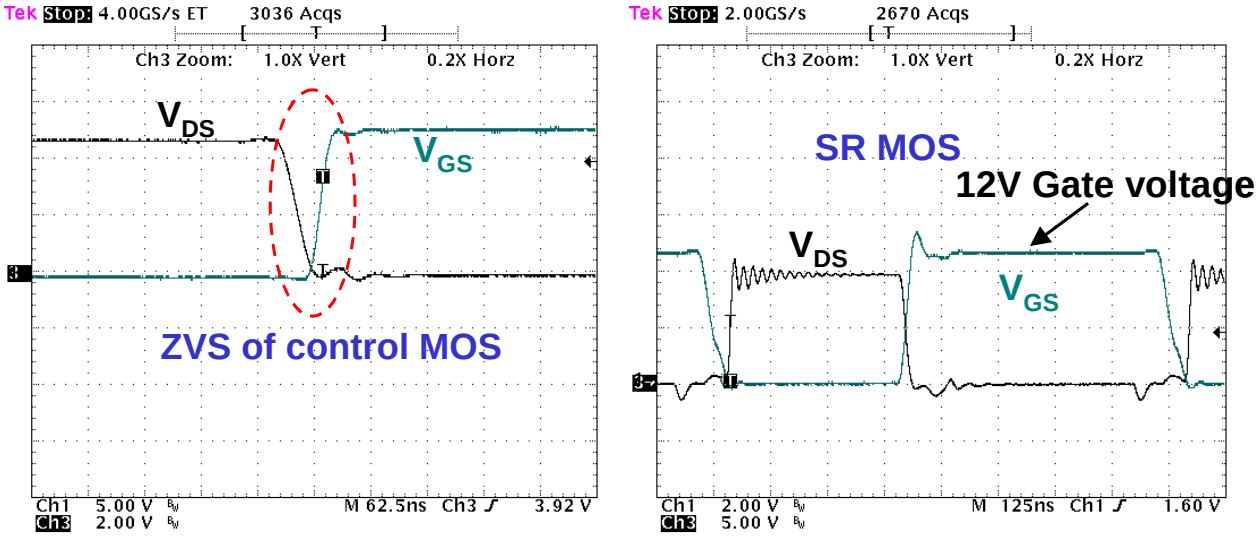


Figure 3.15 The prototype of the 1MHz 1U self-driven VRM



(a) (b)

Figure 3.16 Drain-source and gate-source voltage for (a) Q3; (b)Q5

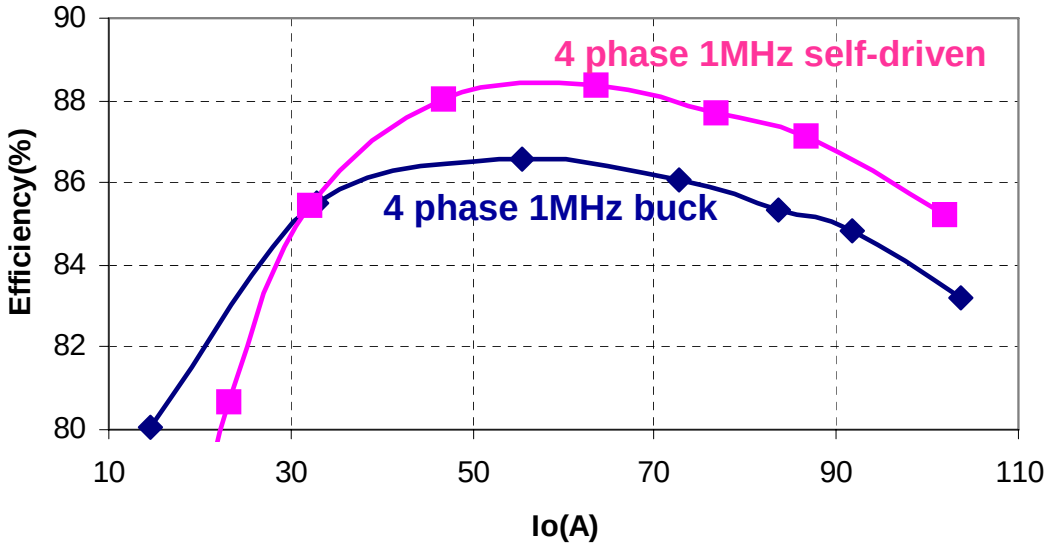


Figure 3.17 Measured efficiency at 1MHz

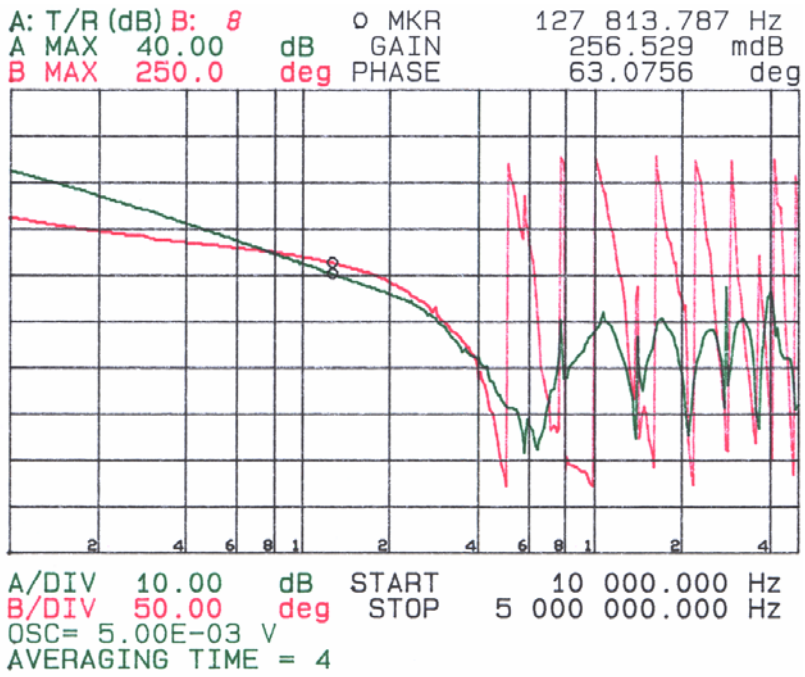


Figure 3.18 The measured loop gain and phase plot

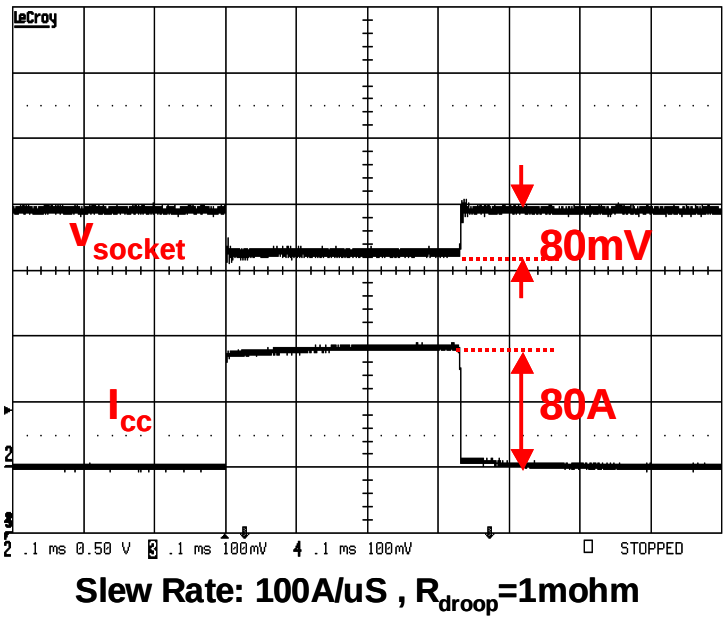


Figure 3.19 Load transient waveforms(Upper: Vo ,100mV/div; Lower: Io ,40A/div)

3.2. A Virtual Test Bed for Loss Breakdown Analysis

In order to gain a good understanding of the loss distribution of the prototype, an accurate simulation model is important. First of all, we need to have the power MOSFET models. The prototype uses Renesas's generation 8 devices: HAT2168 and HAT2165. The models provided by Renesas are basically behavior models derived through a curve-fitting method. Before applying these models into the prototype circuit, calibrations are made using a physical-based model. The physical-based model is actually an FEA model also provided by Renesas which represents the real device implementation, including physical dimensions and material information. Although the FEA model is the most accurate one, it is not practical for circuit-level simulations.

A simple single-phase buck circuit is used to calibrate the behavior models. First, the FEA model is plugged in and the simulation runs for just one switching cycle. Then the behavior model is used to run the same simulation. The rest of the circuit stays exactly the same. The switching waveforms are plotted in Figure 3.20. Figure 3.20a shows the control switch waveforms, and Figure 3.20b shows the SR waveforms. The two models give very similar results. Based on these waveforms, the loss breakdown can be done as shown in Figure 3.21. Except for the SR body diode reverse recovery loss, all the other loss bars for the two models match extremely well. Fortunately, due to the duty extension of the proposed self-driven circuit, the reverse recovery loss is insignificant.

The behavior model is a good tradeoff between accuracy and simulation time. According to the calibration results, the vendor-provided behavior model is suitable for the virtual simulation testbed of the proposed circuits.

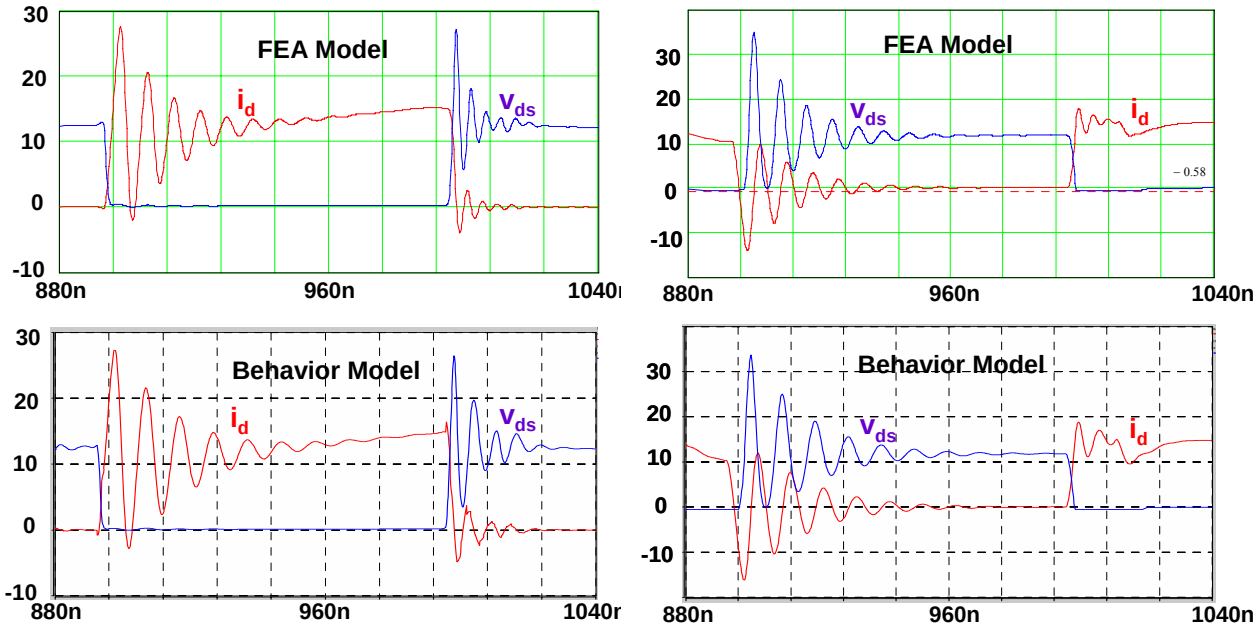


Figure 3.20 Simulated switching waveforms by FEA and behavior models: (a) top switch; (b) bottom switch

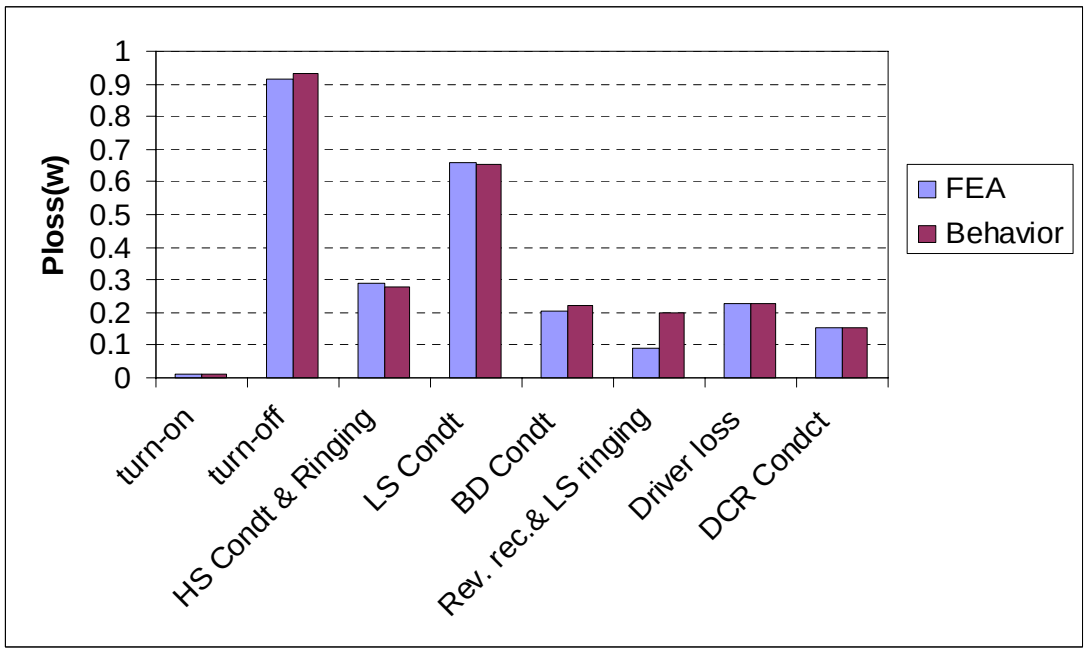


Figure 3.21 Loss breakdown comparison of the FEA model and behavior model (1MHz, 12.5A, 1.3V)

The proposed 12V self-driven VRM is then evaluated with the verified simulation testbed. The transformer winding resistance and its leakage inductance between the primary side and the

secondary side are measured with an impedance analyzer, and the values reflected to the primary side are 20mΩ and 60nH, respectively. Since the transformer core loss is very small, as we estimated earlier, it is ignored in the simulation. The overall efficiency under the same specifications as the prototype obtained by simulation over the entire load range is plotted in Figure 3.22. The simulation results match the experimental results very well.

Loss breakdowns are made for both the conventional buck and the proposed self-driven VRM, as shown in Figure 3.23. In order to make a fair comparison, the same number and type of devices are used. For the buck converter, eight pairs of devices (HAT2168+HAT2165) are used for the eight phases, with each phase carrying 12.5A current. For the self-driven VRM, there are two full bridges. Each of them consists of four HAT2168s. Also, there are four SR branches, and each of them has two HAT2165s in parallel.

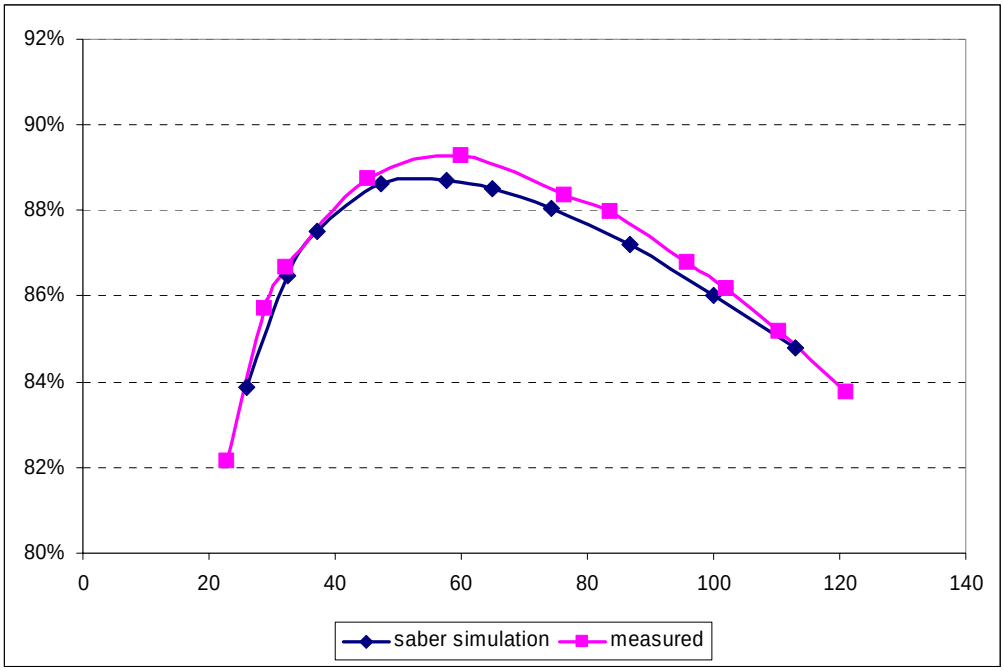


Figure 3.22 Efficiency curves obtained from the measurement and the simulation

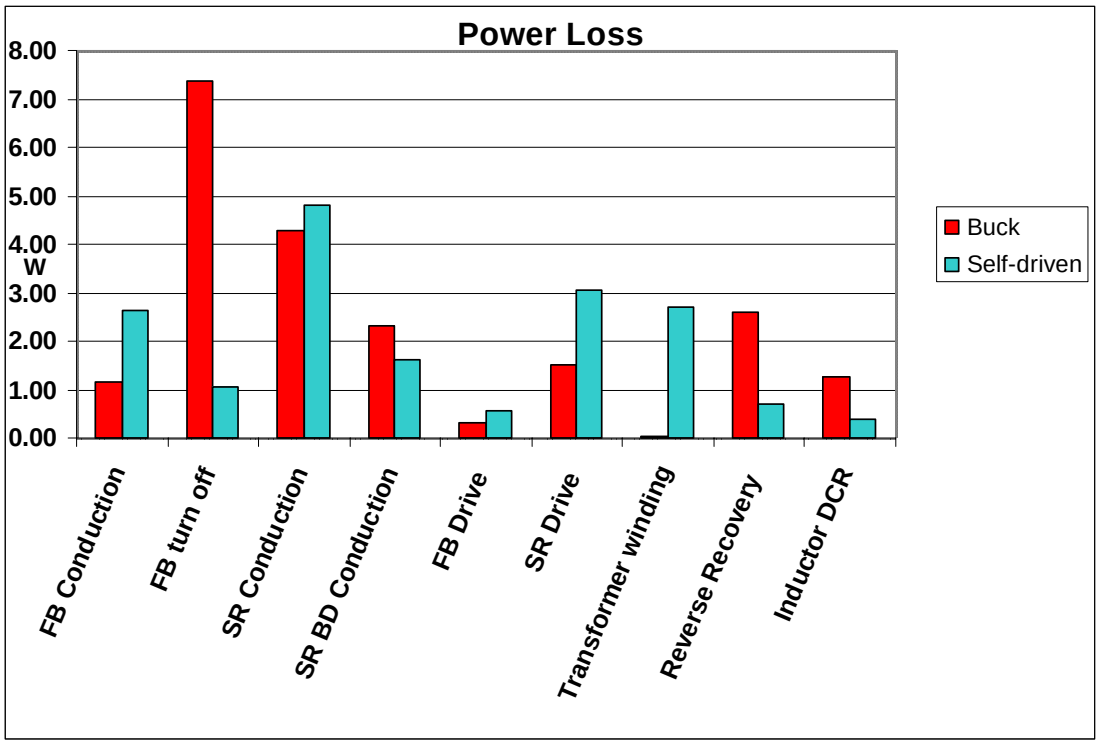


Figure 3.23 Loss breakdowns of a conventional buck and a self-driven VRM

The proposed CCB self-driven concept significantly reduces the top switch turn-off loss in the buck converter. The body diode loss, the reverse-recovery loss, and the inductor winding loss are also reduced. However, because of the ZVS operation, the system has a certain amount of circulating energy which inherently increases the primary side full-bridge conduction loss as well as the SR conduction loss. The increase of the SR conduction loss is compensated by the high gate voltage under which the SR on resistance is relatively smaller. At the same time, the higher gate voltage (12V instead of 5V) introduces a large gate drive loss, which will be about five times higher if an external driver is used. The gate drive loss saving mechanism of the CCB self-driven scheme plays an important role in minimizing the gate loss. Figure 3.24 shows the integration of the energy going into the gates of a pair of HAT2165. The positive steps are the energies into the gates, and the negative steps are those being recycled. About 50% of gate drive losses are saved.

It should be noted that the transformer winding loss of the proposed self-driven VRM is an additional loss that a conventional buck converter does not have. The following sections will

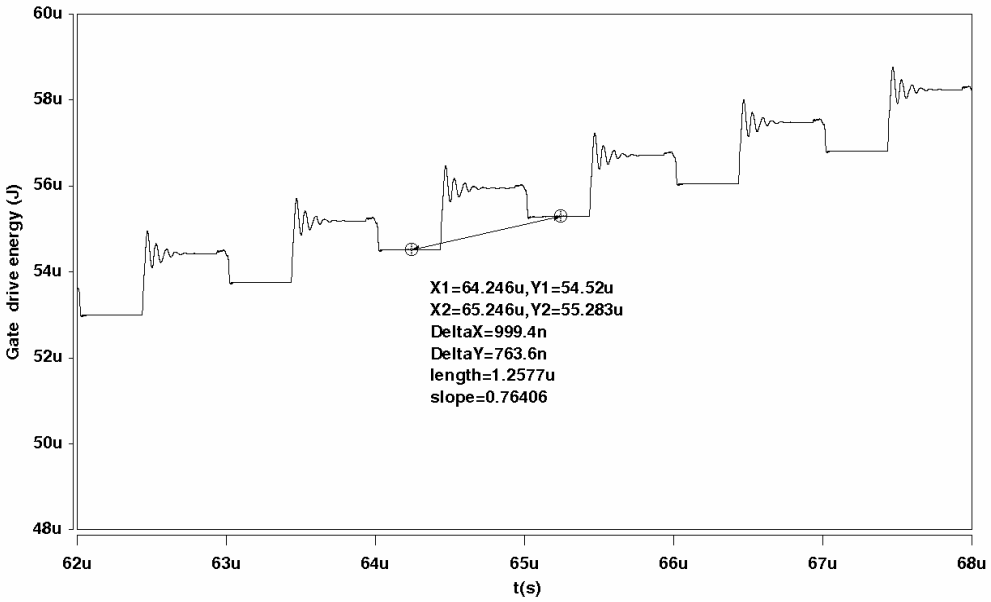


Figure 3.24 Integration of the energy going into the gates of a pair of HAT2165

investigate the possibilities of improving the magnetic components so that the overall efficiency is further improved and the component cost is reduced.

3.3. Further Improvement with Magnetic Integration

In this section, an integrated magnetic 12V self-driven circuit is proposed mainly to reduce the transformer winding loss. After integrating the two output inductors with the transformer, the footprints of the inductors are utilized to increase the transformer winding width. First the idea of magnetic integration is discussed, then implementations of the windings are studied in detail. Experimental results show substantial efficiency improvement over the discrete magnetic prototype.

As previously mentioned, the proposed 12V self-driven VRM has one more transformer than the conventional multi-phase buck converter. This is of concern when the overall circuit cost is taken into account. The purpose of using integrated magnetics is to minimize the magnetic components.

First, the original 12V self-driven circuit is modified by splitting the transformer into two separate transformers, Tr1 and Tr2. Each of them has a n_p:1 turn's ratio, as shown in Figure 3.25(a). In the figure, M1 and M2 represent the magnetizing inductances of Tr1 and Tr2. If we

design the M1 and M2 values to be equal to that of L1 and L2, we are able to use the magnetizing inductors as the output filter inductors, as shown in Figure 3.25(b). Instead of using one transformer and two inductors, the integrated structure uses two transformers to do the job. The winding and core implementation will be discussed in the next section. Figure 3.26 shows the voltage and current waveforms of the transformer's secondary side. According to the waveforms, the magnetizing inductors have the exactly same voltage and current as those of the discrete inductors in the original circuit.

The rms current through each secondary winding is about $\frac{I_o}{\sqrt{2}}$, which is $\sqrt{2}$ times higher than the discrete magnetic implementation. The only way to reduce the winding loss is to enlarge the winding width by utilizing the area occupied by the inductors previously. Proper winding structure design, as discussed next, is the key factor to this integrated magnetic implementation.

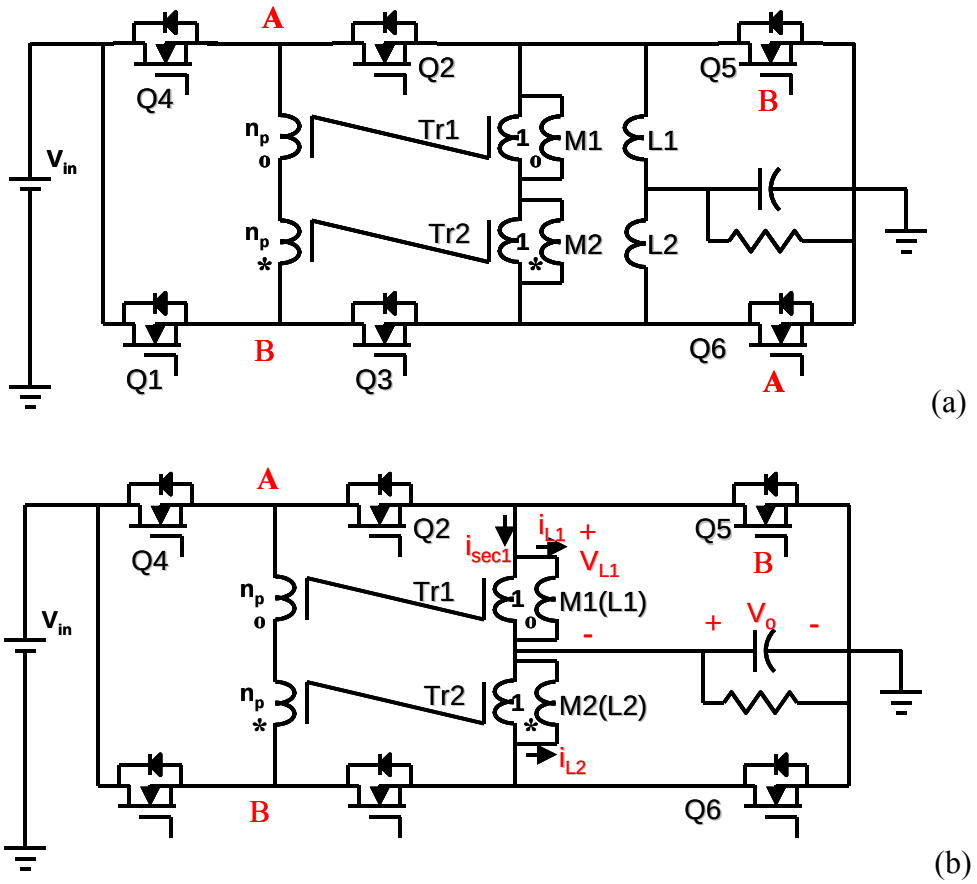


Figure 3.25 Derivation of the 12V self-driven VRM with integrated magnetics

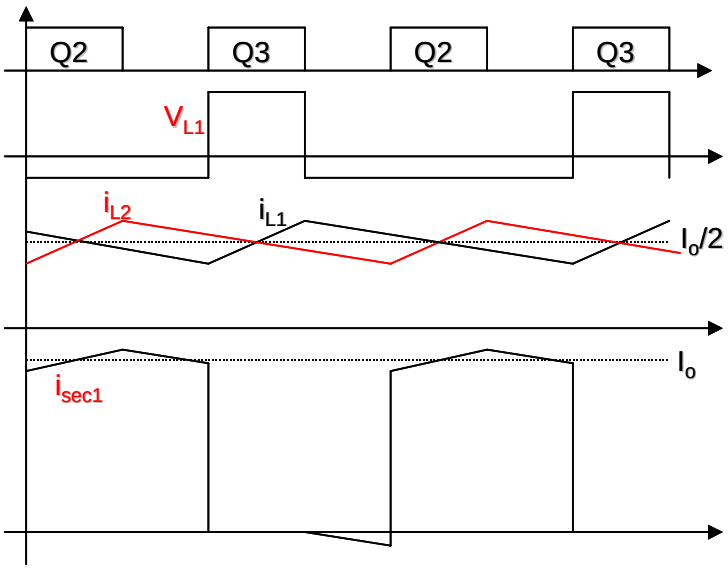


Figure 3.26 Key waveforms of the integrated magnetic structure

The implementation of the integrated magnetics in Figure 3.27(a) can be realized by two UI cores and a six-layer PCB winding. For the secondary winding, only one turn for each transformer is needed. The shortest path is shown in Figure 3.27(b). As for the primary side windings, they are either interleaved with the secondary side windings of the same transformer, or interleaved with the other transformer primary side windings. The purpose of doing this is to minimize the proximity effect between the windings carrying the same direction of current. The winding stack pattern is illustrated in Figure 3.27(c). In the figure, p_{11} means the primary side, transformer1, the first turn. S_1 means the secondary side, transformer1, in parallel.

Using the same devices as the discrete magnetic version of the VRM, the integrated magnetic self-driven VRM is more efficient, as shown in Figure 3.28. The measurement is based on a two-phase prototype running with open loop. The efficiency gain is mainly due to the shorter winding length and the elimination of the discrete output inductors. The better efficiency can be then used for higher output current. For this two-phase design, 10A more current can be delivered at relatively the same efficiency as the discrete version of the VRM.

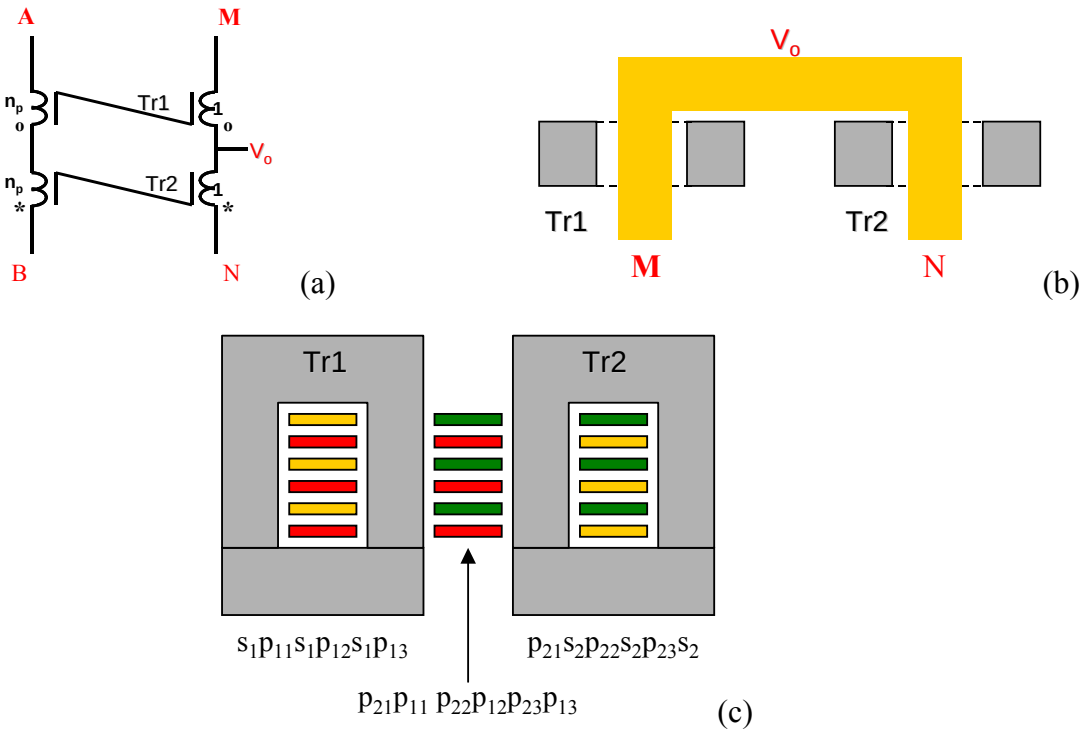


Figure 3.27 Winding structures of the integrated magnetics

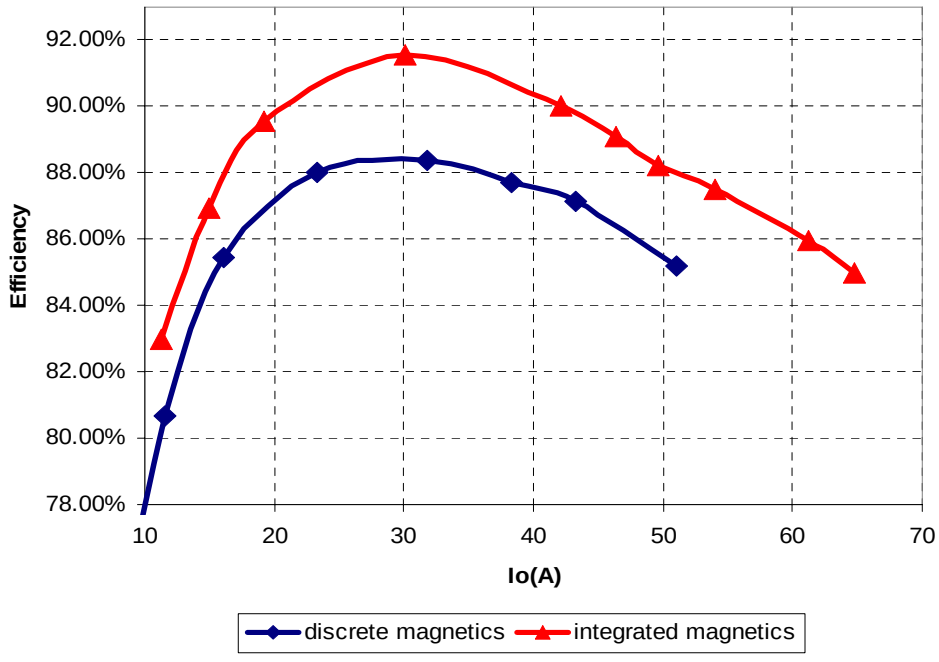


Figure 3.28 Measured efficiency of the 12V self-driven VRM with and without integrated magnetics

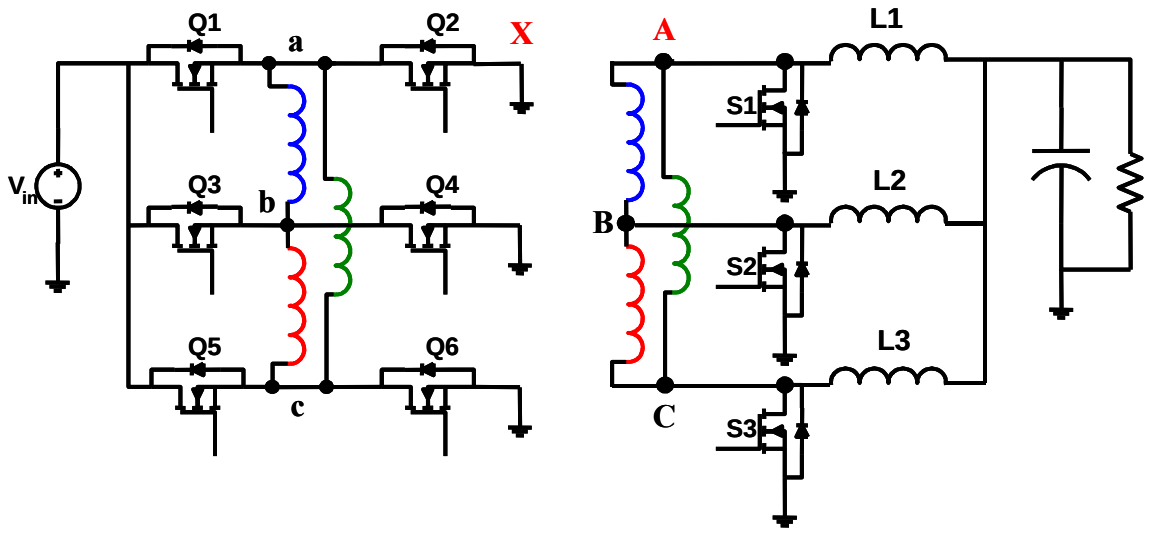
3.4. Current-Tripler Concept Extended to 12V Non-isolated VRMs

The proposed current-tripler converter can be extended to the 12V non-isolated VRMs. The concept of the current-tripler was inspired by the three-phase interleaving buck converter, which is a hard-switching topology. We modified the control strategy to achieve ZVS for the 48V-isolated case, which was then transformed into a 12V ZVS current-tripler converter. Compared to the conventional three-phase interleaving buck converter, it adds one three-phase transformer that extends the duty cycle for better efficiency. The following part first illustrates the method of transforming the isolated current-tripler into its non-isolated counterpart, then shows the experimental results. Afterward, the possibilities of applying the proposed CCB self-driven concept into this 12V non-isolated current-tripler VRM are investigated.

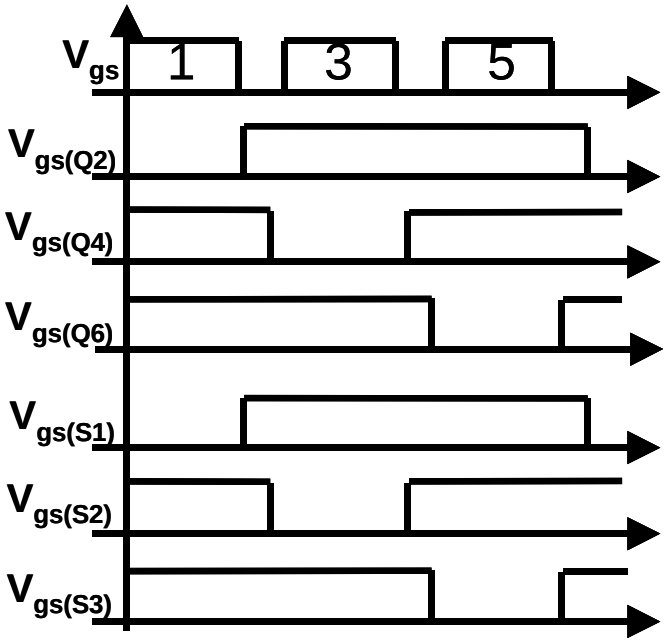
3.4.1. Transformation from Isolated Current-Tripler to Non-Isolated Current-Tripler

In order to do the transformation, the isolated current-tripler converter shown in Figure 2.38 is redrawn in Figure 3.29. The orientation of the components is rearranged. Note that point X only needs to be grounded when Q2 is on; when Q2 is off, point X could be connected to any other point in the circuit that has a voltage potential lower than the input voltage. On the other hand, point A is grounded when S1 is on. One observation can be made from Figure 3.29(b): gate signal of Q2 is identical to that of S1, which means S1 can provide the proper grounding path for Q2 when it needs to be grounded. By simply connecting point X and point A, the non-isolated current-tripler converter is derived as shown in Figure 3.30.

One can use a simple boot-strap driver to externally drive the MOSFETs. Let us take the Q5-Q6-S3 bridge as an example. Because we can connect the gate of Q6 and S3 together, the conventionally available adaptive gate driver can be easily used, as shown in Figure 3.30.



(a)



(b)

Figure 3.29 Transformation from isolated current-tripler to non-isolated current-tripler

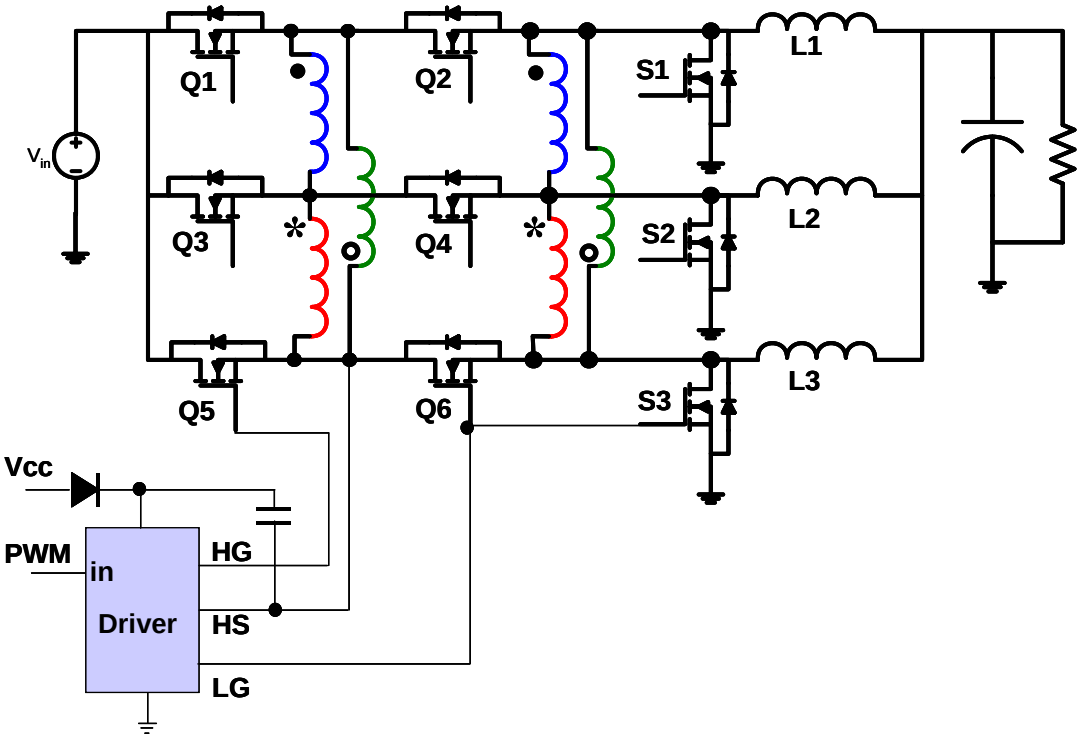


Figure 3.30 Proposed non-isolated current-tripler DC-DC converter

3.4.2. Experimental Results

The 12V current-tripler prototype is shown in Figure 3.31. The transformer is mounted on the backside of the board. An efficiency comparison is made between the current-tripler and a

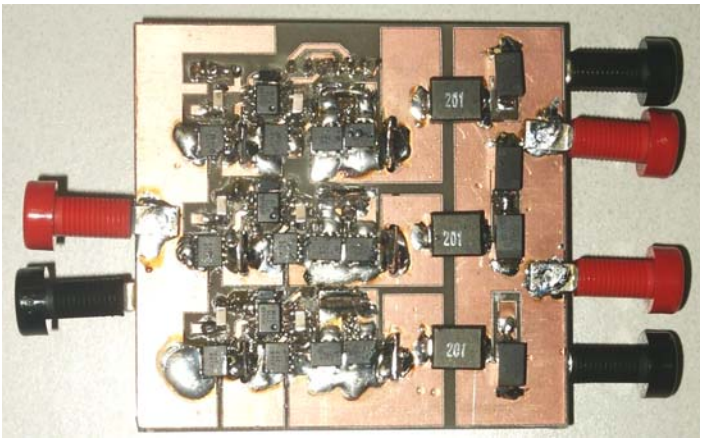


Figure 3.31 Prototype of a 12V current-tripler VRM

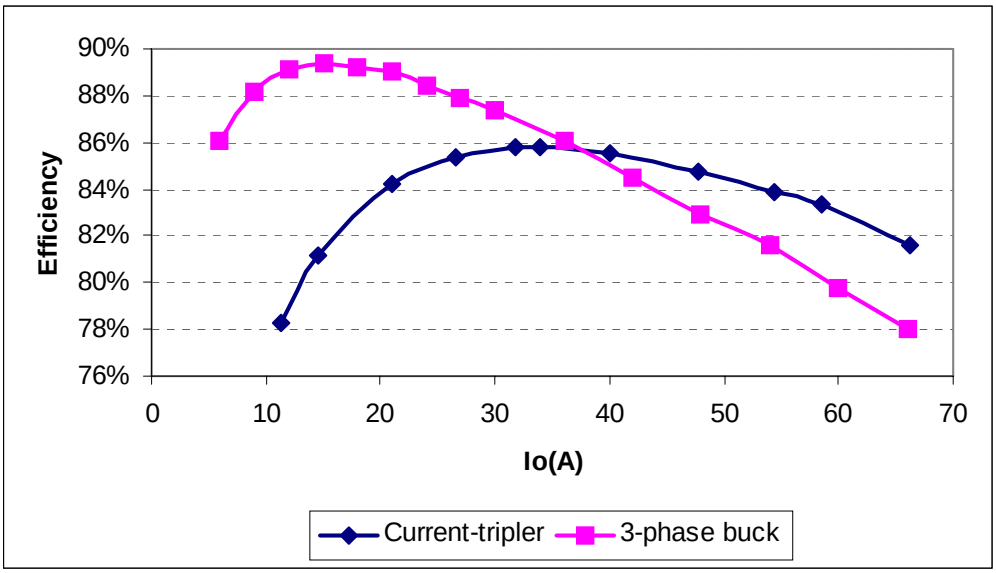


Figure 3.32 Measured efficiency

three-phase buck converter, as shown in Figure 3.32. Both are running at 300kHz with 1.0V output voltage. Note that the same number and type of devices are used for the comparison (1 HAT2168 & 2 HAT2166s). The current-tripler converter can effectively reduce the conduction losses.

3.4.3. Applying the CCB Self-Driven Concept to 12V Non-Isolated Current-Tripler VRM

The previous section discussed a non-isolated current-tripler DC-DC converter, where the SRs are externally driven by the designated drivers. Although the three-phase bridges are complementarily controlled, which is the criteria for the CCB self-driven concept, their middle point voltages (V_A, V_B, V_C) cannot be used directly to drive the SRs. Figure 3.33 shows two complementary control schemes. The first one shown in Figure 3.33(a) is to set Q1, Q3, Q5 as the control switches (D<1/3). The required SR gate voltages are in fact the inversion of the middle point voltages. Unless one uses driver transformers to inverse the signals, which is undesirable for a non-isolated converter, the simple self-driven scheme is not achievable. In Figure 3.33(b), there is another complementary control scheme. Q2, Q4, and Q6 are set to be the control switches. Unfortunately, achieving the required SR gate voltages in order to make the

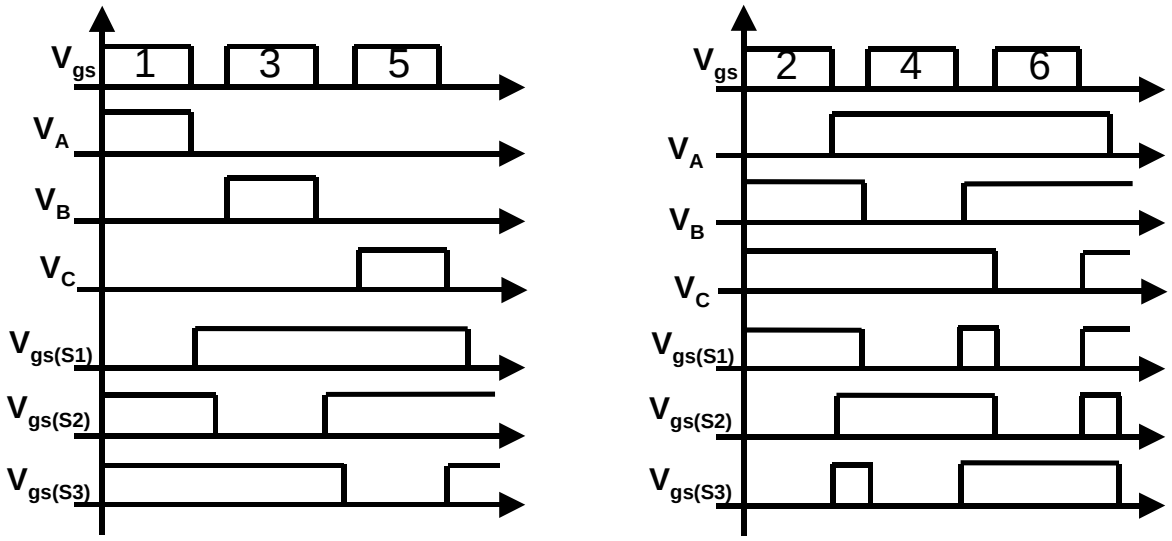


Figure 3.33 Two complementary control schemes for non-isolated current-tripler DC-DC converter

circuit function properly becomes more complicated. Can the winding polarities of the circuit be changed so that the proper gate signals are generated? In order to investigate this possibility, the following sections will discuss the autotransformer version for the two-phase self-driven topology first. The experimental results verify this topological transformation. Then using the same method, a self-driven 12V current-tripler is proposed. The loss reduction is demonstrated by a SABER simulation model.

3.4.3.1. An Autotransformer Version of the 2-Phase Self-Driven VRM

A transformer in a DC-DC converter usually serves two purposes: isolation and input-to-output gain adjustment. In the 12V VRM application, no isolation is needed. The only reason for using the transformer in the proposed circuit is to step down the input voltage so that the duty cycle can be extended.

An autotransformer is a special type of transformer that does not have isolation. The secondary side winding is part of the primary side winding. Figure 3.34 shows the differences between a transformer and an autotransformer. Both of them have the same turn's ratio. It is easy to see that the secondary winding of the autotransformer has less current than that of the transformer. Moreover, the primary winding turns are reduced as well.

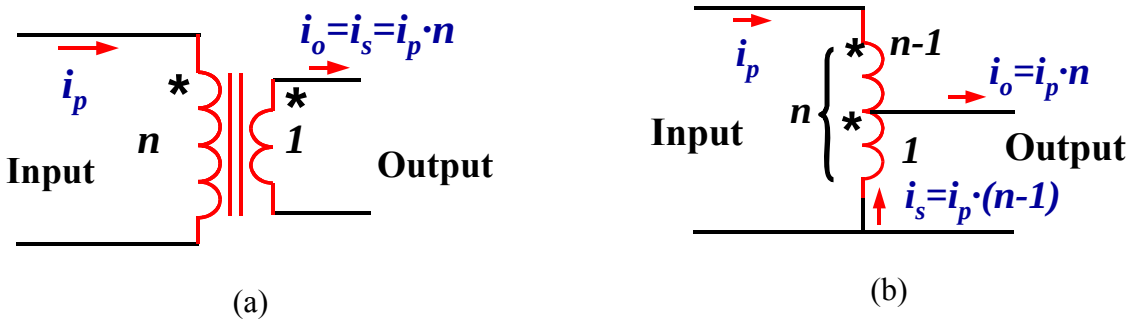


Figure 3.34 Transformer (a) and autotransformer (b)

By replacing the transformer in Figure 3.4 with an autotransformer, one can get the circuit shown in Figure 3.35. According to the key waveforms shown in Figure 3.36, the CCB self-driven scheme cannot be used without modification because V_A and V_B are either 12V or (12/n) V, which means the SRs cannot be turned off if V_A and V_B are directly connected to the SRs' gates. Taking the Q1-Q3 leg as an example, the PMOS-NMOS pair in the driving path helps to clamp Q6's gate voltage to ground. The gates of the PMOS-NMOS pair are connected to the gate of Q3. When Q3 turns off, PMOS conducts. Q6 is self-driven to be on by V_B. On the other hand, when Q1 turns off, there is dead time before Q3 turns on. During this dead time, PMOS stays on. The gate of Q6 will decrease to (12/n) V. Until this point, it is still self-driven. After that, the gate of Q6 is connected to the ground by the NMOS, a process of external driving. Generally speaking, it is a hybrid-driving scheme.

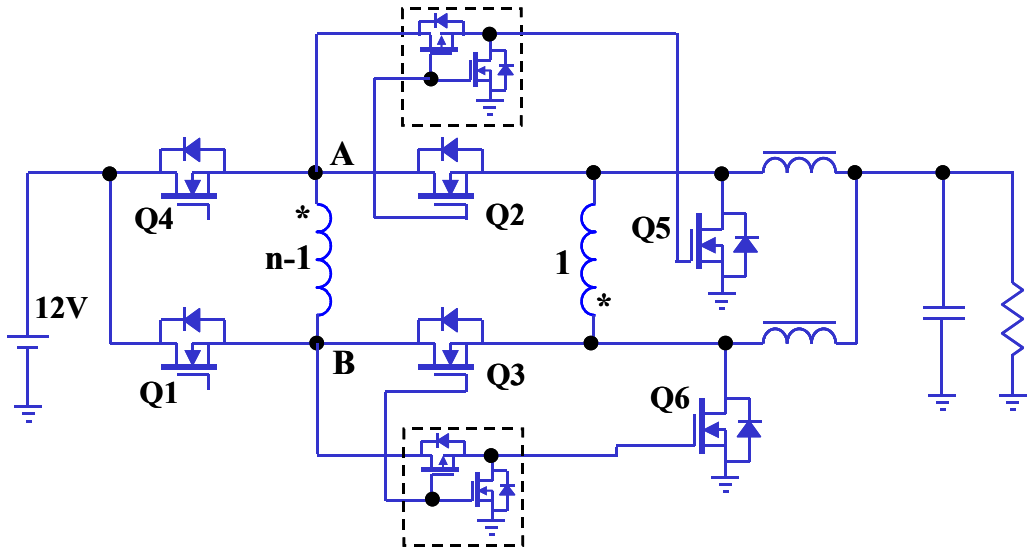


Figure 3.35 An autotransformer self-driven VRM

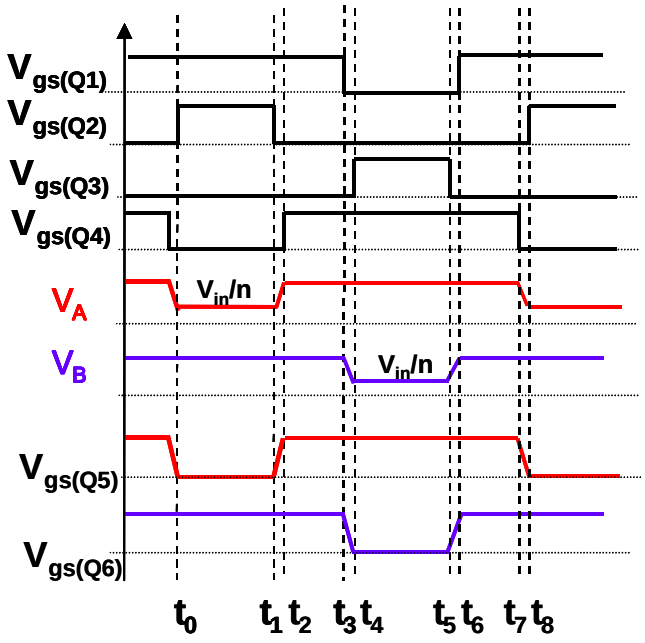


Figure 3.36 Key waveforms of the circuit in Figure 3.35

3.4.3.2. Pros and Cons of the Autotransformer Version of the 12V Self-Driven VRM

The major benefit of the autotransformer version of the circuit is the reduction of the transformer winding loss. According to Figure 3.34, the secondary winding current changes from ni_p to $(n-1)i_p$. Meanwhile, the primary winding changes from n turns to (n-1) turns. Figure 3.37 shows the normalized primary and secondary winding conduction loss savings for n=3.

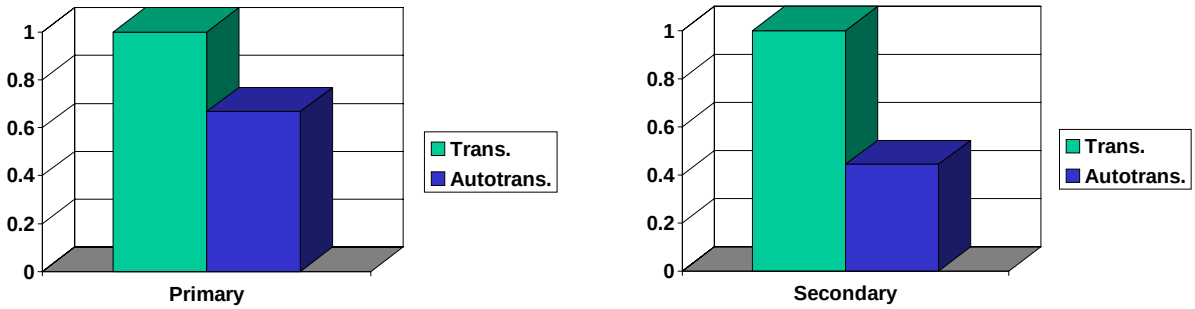
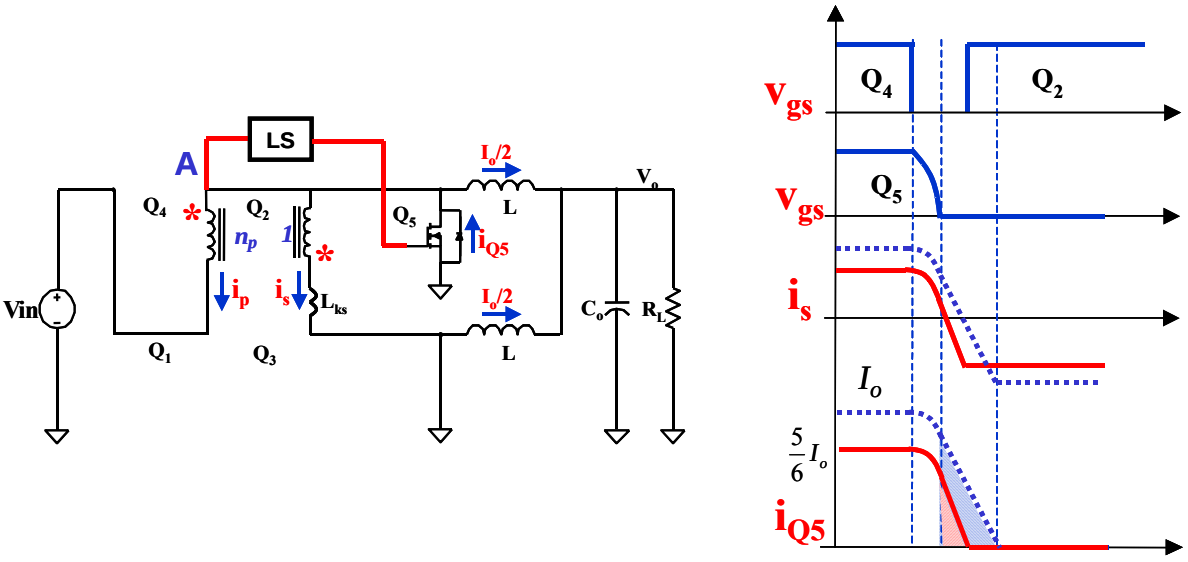


Figure 3.37 Winding loss comparison

Another benefit of the autotransformer version is the reduction of the body diode conduction loss. Figure 3.38(a) shows an equivalent circuit when Q5 turns off. The LS block

represents the PMOS-NMOS pair. For a turn's ratio of n=3, n_p is equal to 2. The current through Q5, i_{Q5}, and the current through the secondary winding, i_s, are shown in Figure 3.38(b). Because of the reduction of the winding current, the commuting time needed to reverse the polarity of i_s is also reduced. Therefore, the body diode conduction loss is reduced.

Although there is loss reduction by using an autotransformer, one must pay attention to the increased complexity of the SR driving path. In addition, the driver circuitry for Q1-Q4 is also complicated. The simple boot-strap driver shown in Figure 3.6 is no longer valid because the source voltage of Q3 is V_{in}/n during its on time. The gate voltage of Q3 also needs a level shift to $(5V+V_{in}/n)$. All of these will be the practical concerns for the autotransformer version self-driven VRM.



(a) Equivalent circuit (b) Waveforms

Figure 3.38 Body diode conduction of the autotransformer self-driven VRM

3.4.3.3. Experimental Results of the Autotransformer 12V Self-Driven VRM

In order to verify the feasibility of the autotransformer self-driven scheme, a two-phase prototype is built with the power stage only, as shown in Figure 3.39. The specifications are the same as the prototype shown in Figure 3.15, except that the maximum output current is 50A. Figure 3.40 shows the schematic of the circuit in which a practical way of driving the full-bridge switches Q1-Q4 is illustrated.

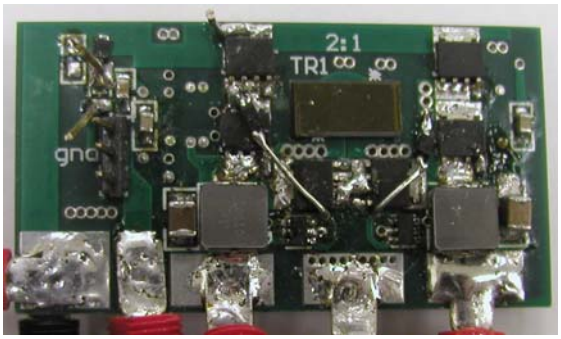


Figure 3.39 A two-phase prototype of the autotransformer self-driven VRM

Figure 3.41 shows the waveforms of V_A and V_{ds}(Q6). As mentioned before, V_A stays at 4V during the Q2 on time, which makes its self-driven scheme more complex than the transformer version. The measured efficiency is shown in Figure 3.42. Note that in the prototype, only one SR is used for each phase. To parallel more SR devices during the test is not as effective as in the transformer version prototype. One possible reason could be the gate energy is not effectively recycled due to the insertion of the PMOS-NMOS pair in the driver path.

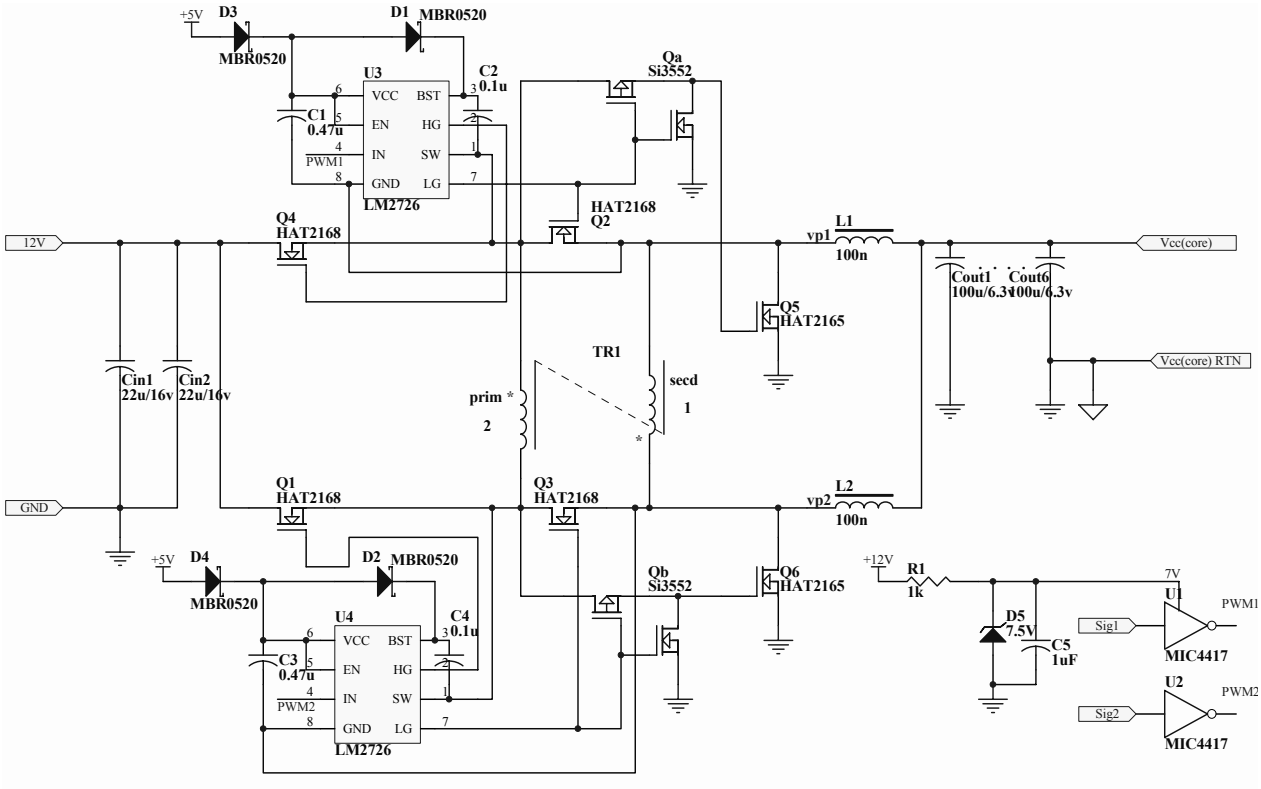


Figure 3.40 The schematic of the autotransformer self-driven VRM prototype

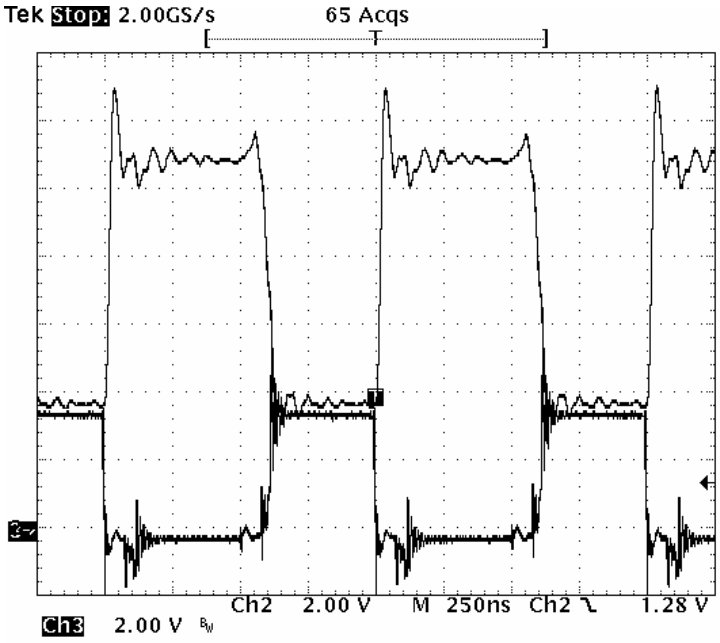


Figure 3.41 Switching waveforms: V_A (top) and V_{ds}(Q6) (bottom)

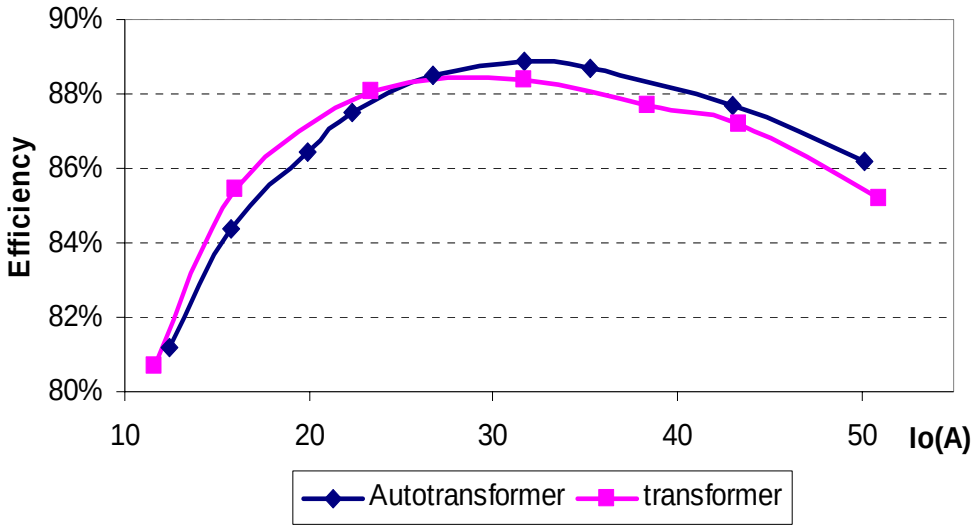


Figure 3.42 Measured efficiency of a two-phase autotransformer version

3.4.3.4. Applying the Autotransformer Self-Driven Scheme to the Current-Tripler Converter

One can use the previously-discussed autotransformer self-driven scheme to modify the circuit in Figure 3.30. The transformer winding polarities are rearranged to form autotransformer connections, as shown in Figure 3.43.

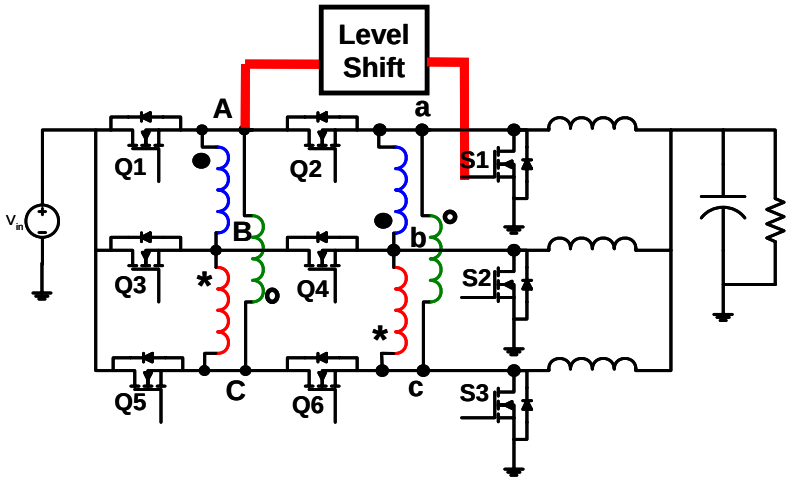


Figure 3.43 Proposed non-isolated current-tripler DC-DC converter with CCB self-driven scheme

The middle point of each leg provides a suitable driving source for its corresponding SR device through a simple level-shift circuitry. The level shift circuit consists of a PMOS and NMOS pair that is the same as that used in Figure 3.35. Figure 3.44 illustrates the control timing for all the switches as well as the key waveforms. This proposed topology has all the benefits of current-tripler as well as the CCB self-driven converter.

The loss comparison between the CCB self-driven VRM and the conventional buck converter is based on the virtual test bed verified in Section 3.2. The two circuits being compared are shown in Figure 3.45. Both of them have six pairs of devices (HAT2168 & HAT2165). For a 100A output current, running at 1MHz, the loss breakdown comparison between the 12V self-driven current-tripler and the conventional buck converter is shown in Figure 3.46. The major benefit of the CCB self-driven VRM is the reduction of the full-bridge turn-off loss (corresponding to the top switch turn-off loss) and other f_s-related losses at the cost of increased

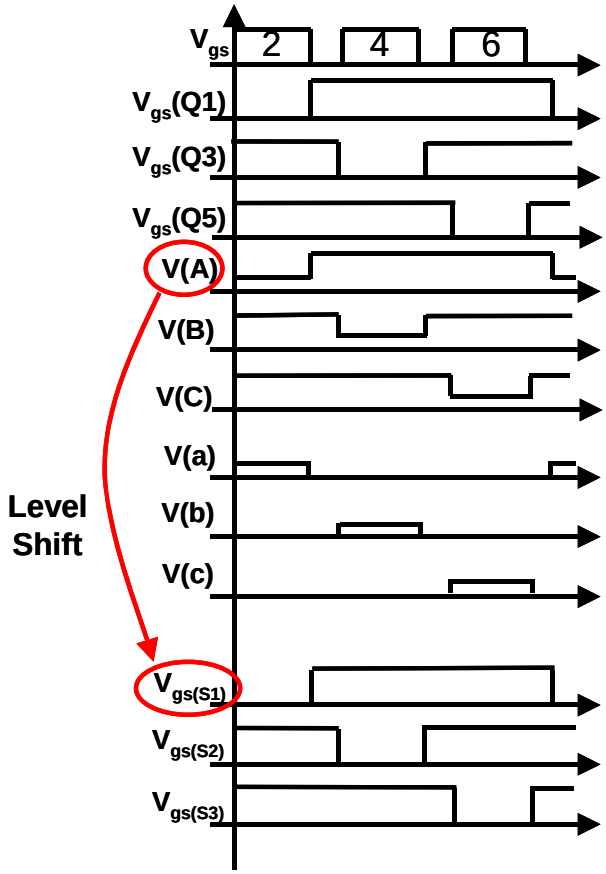


Figure 3.44 Control timing for current-tripler 12V VRM with CCB self-driven

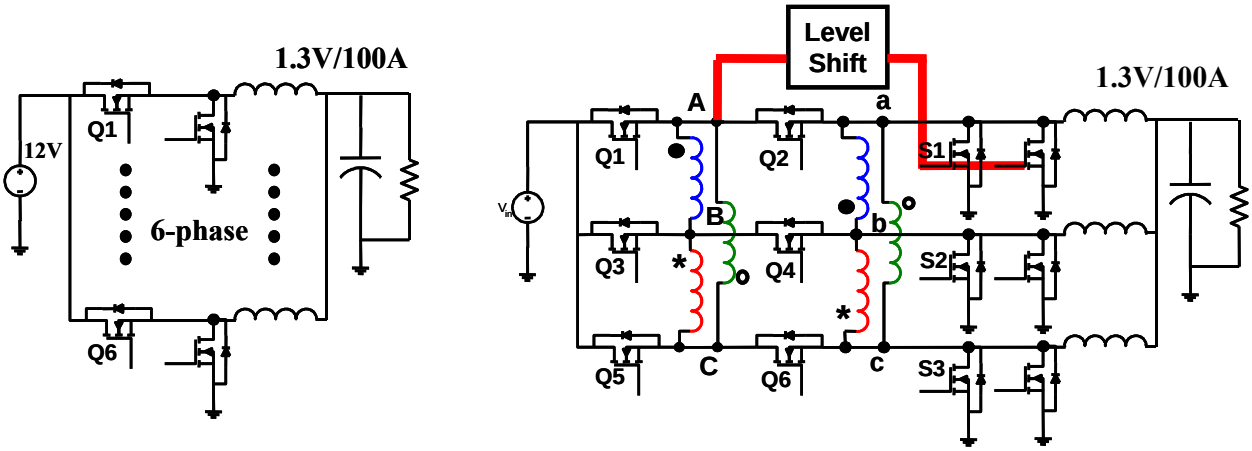


Figure 3.45 The buck and current-tripler converters under comparison

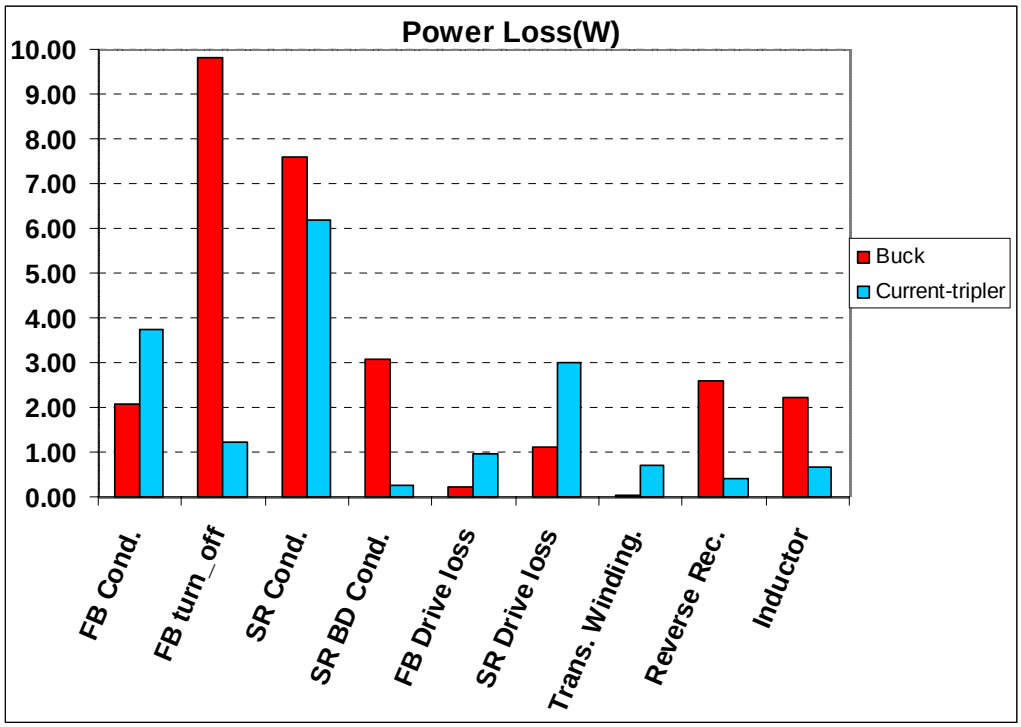


Figure 3.46 Loss breakdown comparison between 12V self-driven current-tripler and buck converter

conduction losses. The adoption of the current-tripler concept is able to minimize the secondary-side conduction losses. Also, the adoption of autotransformer helps reducing the body diode

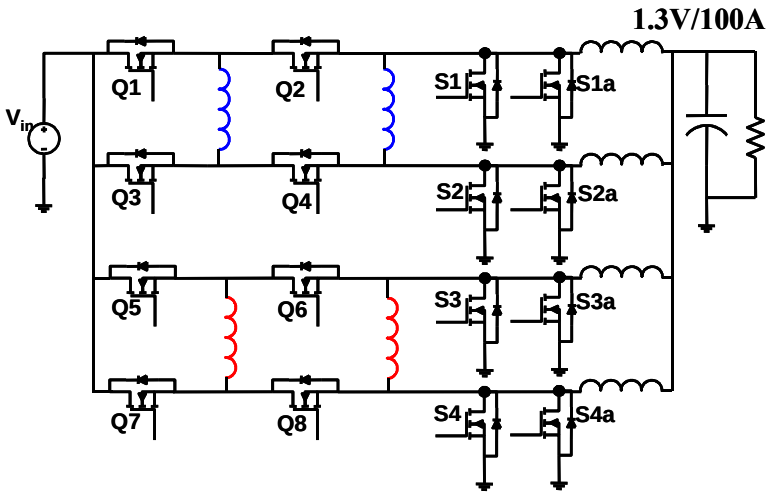


Figure 3.47 The dual current-doubler configuration of the proposed self-driven VRM

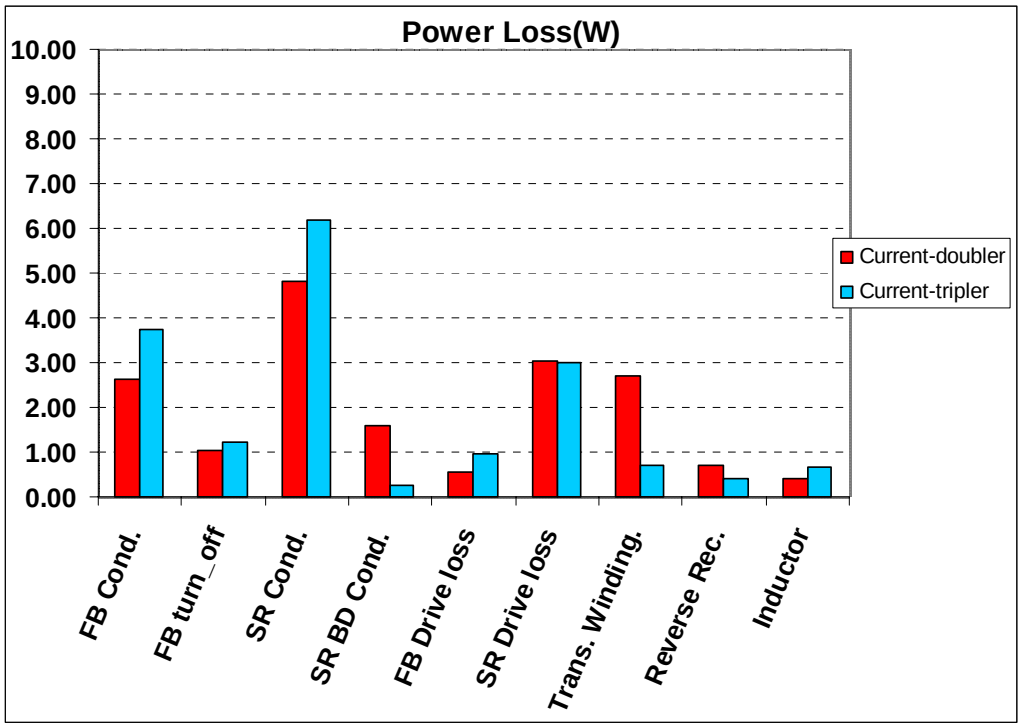


Figure 3.48 Loss breakdown comparison between 12V self-driven current-tripler and 12V self-driven with two current-doublers

conduction loss and the winding loss as well. However, both the full bridge and the SR driver losses are higher than the conventional buck converter because higher gate voltage is used in the circuit.

Another comparison is made between the 4-phase self-driven topology using two current-doubler type rectifiers (Figure 3.47) and the current-tripler configuration (Figure 3.45). Both of them deliver 100A current. The loss breakdown is shown in Figure 3.48. Although the total losses for both circuits are similar, the current-tripler converter has less devices. Based on these simulation results, the 12V current-tripler with CCB self-driven is a promising topology for high frequency and high current VRMs, however, its layout complexity has to be taken into account for a practical VRM design.

3.5. Summary

This chapter proposes novel topologies for 12V non-isolated VRMs. The CCB self-driven and current-tripler techniques are utilized to reduce both switching related losses and conduction losses. These topologies have the following features in common:

1. Duty cycle extension, an important feature for the 12V VRM with low output voltage;
2. Zero voltage switching to alleviate the large turn off loss at high frequency;
3. SR gate charge recycling and body diode conduction loss reduction by the self-driven technique;
4. Applicability for coupled inductors for better transient performance.

Chapter 4. Performance Enhancements of the Proposed VRMs with Coupling Inductors

In the previous chapters, the CCB self-driven VRs for both the 48V isolated application and 12V non-isolated application have the same output rectifier stages: current-doubler rectifiers. The two output inductors in the current-doubler rectifier have the same voltage waveforms as those in a two-phase buck converter. This is also true for the current-tripler rectifiers, which have a three-inductor structure comparable to that of a three-phase buck converter.

For steady-state operation, a large inductance is preferred so that the current ripples can be reduced. However, for the transient response, a small inductance is preferred so that a high transient inductor current slew rate can be achieved. As previously discussed, the steady-state and dynamic performances have contradictory requirements of the inductance. For non-coupling inductors, there is only one inductance in the two formulas. The steady-state performance must be sacrificed to achieve fast transient responses.

It has already been demonstrated in [74] that the use of integrated coupling inductors between the interleaving channels of a buck converter can improve both the steady-state efficiency and dynamic performances. The essence of the coupling inductors concept is to provide different equivalent inductances for the steady state and the transient. It is straightforward that the coupling inductors concept can be applied to various topologies proposed in Chapter 2 and Chapter 3 to improve performance. For a fixed inductor current ripple, the larger the coupling coefficient, the smaller the equivalent transient inductance, therefore the lower the output voltage spike. According to the discussion in Chapter 3 in [74], as the transient inductance continues decreasing, it will eventually meet a critical value, the so-called critical inductance, below which the output voltage spike is solely determined by the control bandwidth.

To begin with, this chapter reviews the basic concept of coupling inductors in VRM applications. Several implementations are discussed, including a proposed core structure with much less winding resistance than other core structures. After that, the benefits of using coupling

inductors in addition to those that have been demonstrated are studied. Because the current loop control is necessary to guarantee the proper current sharing between phases, the current loop sample hold effect will limit the control bandwidth to be practically pushed beyond 1/6 of the switching frequency. This limitation can be overcome by coupling the output inductors. To simplify the analysis, a two-phase buck converter is studied. A small signal model with peak current control is proposed to study the sample hold effect in two different coupled-inductor implementations: 1) a center-tap winding wound in one magnetic core plus an additional output inductor, and 2) a fully integrated structure with both inductor windings in one magnetic component. The relationship between the coupling coefficient and the sample hold effect is then discussed. Based on these understandings, it is determined that a CCB 12V self-driven VR with the center-tap version coupling inductors has double the bandwidth of the non-coupled VR; and this is experimentally verified. A three-phase buck converter with coupling output inductors is then studied, which is applicable to the current-tripler converters as well.

4.1. An Overview of the Coupling Inductors in VRM Applications

4.1.1. Basic Principles of the Coupling Inductors for Interleaving VRMs

The basic principles of the coupling inductors for interleaving VRMs have been thoroughly studied by Pit-leong Wong in his dissertation [74]. This section gives a quick summary of the coupling inductors concept he proposed.

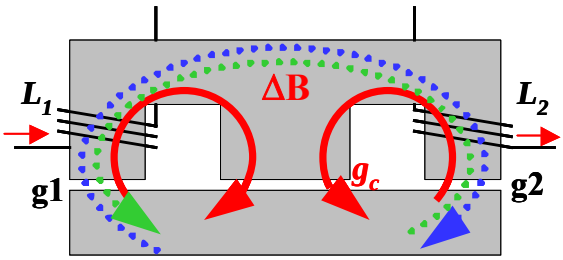


Figure 4.1 Integrated coupling inductors proposed in [74]

The coupling inductors are implemented by two sets of windings on one magnetic core, as shown in Figure 4.1. There are three air gaps in the three legs, g_1, g_2, and g_c. Because of the air gap, the center leg is no longer a low-magnetic-reluctance path for flux. The flux generated by

the winding of L_1 can go through all three legs if the winding of L_2 is an open circuit. The flux generated by the winding of L_2 has a similar path. The flux interaction between the windings, the dotted line in Figure 4.1, indicates the coupling effect between these two inductors.

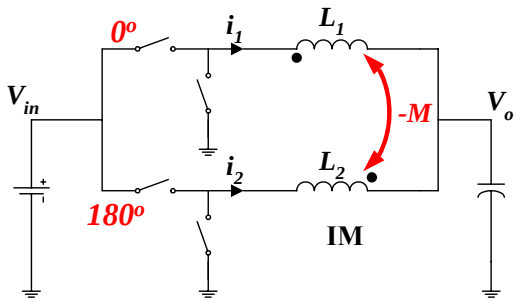


Figure 4.2 A typical 2-phase VRM with coupling inductors

A typical 2-phase VRM with coupling inductors is shown in Figure 4.2. The direction of the two windings' connection shown in Figure 4.2 is defined as an inverse coupling (M>0). Coupling inductors have different equivalent inductances for steady-state and transient responses. Inverse coupling inductors between the interleaving channels reduce the steady-state current ripples while maintaining the same transient responses. Both the conduction and switching losses of the MOSFETs can be reduced because of the small current ripples in inverse coupling inductors.

For simplicity, the two self-inductances built on the same core are considered to be the same (L_1=L_2=L_s). There exists

$$M = \alpha L_s \tag{4.1}$$

where α is the coupling coefficient between the two windings ($0<\alpha<1$).

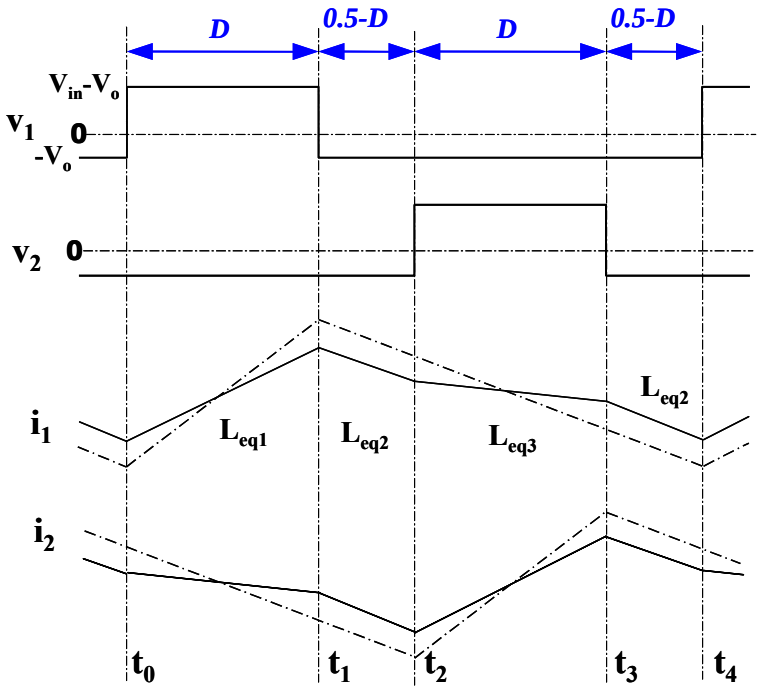


Figure 4.3 steady-state inductor voltage and current waveforms for the non-coupling and coupling inductors

Figure 4.3 shows the steady-state inductor voltage and current waveforms for the non-coupling and coupling inductors. The inductor voltage waveforms for both cases are the same. For the inductor current waveforms, the solid lines corresponds to the coupling case, while the dashed lines corresponds to the non-coupling case.

There are four switching intervals during one switching cycle. Due to the different voltages across the coupling inductors in these four intervals, the inductors equivalent to those in non-coupling case are different for the four intervals. For simplification, only the equivalent inductance in the first phase, corresponding to coupled inductor L_1, is discussed. The equivalent inductance in the second phase, corresponding to coupled inductor L_2, is similar except for a phase shift. For the first phase, the equivalent inductances are derived as follows:

$$L_{eq1} = \frac{L_s^2 - M^2}{L_s - \frac{D}{D'} \cdot M} \tag{4.2}$$

$$L_{eq2} = L_s - M \tag{4.3}$$

$$L_{eq3} = \frac{L_s^2 - M^2}{L_s - \frac{D'}{D} \cdot M} \tag{4.4}$$

During time interval (t_3-t_4), the voltages applied to the two inductors are exactly the same as during time interval (t_1-t_2). Thus, the equivalent inductance in this time interval should equal L_{eq2}. There are three different equivalent inductances in a switching cycle.

Following the same process as when D<0.5, it can be found that the equivalent inductances for all the four time intervals in the case of D>0.5 are exactly the same as those when D<0.5.

Based on the equivalent inductances, the effects of the coupling inductors on converter performance both in steady-state operations and during transient responses can be analyzed. The steady-state criterion is the current ripple because it has a direct impact on converter efficiency. The transient criterion is the current slew rate during transient responses. It is the L_{eq1} that determines the steady state ripple, and L_{eq2} that determines the transient responses.

With the same transient equivalent inductance L_{eq2}, the transient responses are expected to be the same. The coupling inductors can improve the steady-state efficiency. Based on the same transient equivalent inductance, the relationship between the steady-state inductor peak-to-peak currents of non-coupling and coupling inductors can be determined and compared as follows:

$$\frac{I_{pp_cp}}{I_{pp_nc}} = \frac{L_{nc}}{L_{eq1}} = \frac{1 - \frac{D}{D'} \cdot \alpha}{1 + \alpha} \tag{4.5}$$

where L_{nc} is the inductance of the non-coupling case.

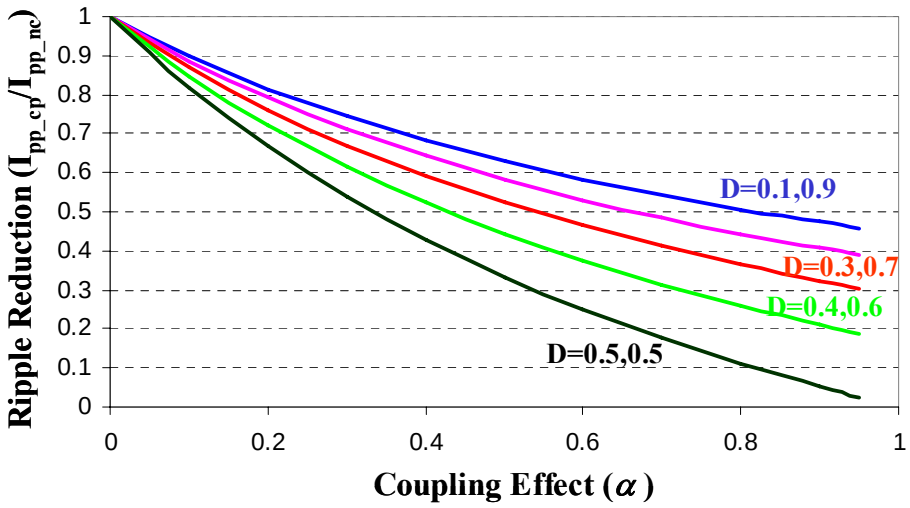


Figure 4.4 Steady-state current ripple reduction in coupling inductors

The current ripple reductions by the coupling inductors are functions of steady-state duty cycle *D* and coupling effects α. The relationship shown in (4.25) is plotted in Fig. 4.17. The steady-state duty cycle closer to 0.5 results in more effective current ripple reduction. Stronger coupling effects give smaller current ripples. The conclusion of Pit-Leong's study is that in order to have the same transient responses and achieve smaller steady-state current ripples, the coupling inductors should be designed to have L_s and α as large as possible while maintaining the same L_{eq2}.

4.1.2. Strong Coupling and its Design Considerations

Although the potential benefits of strong coupling are well understood in [74], there are two questions remaining: 1. How to adjust the air gaps to get larger α, and 2. How to keep the phase current balanced otherwise severe flux asymmetry will occur in the strong coupling magnetics.

4.1.2.1. How to Adjust the Air Gaps to Get Larger α

The integrated coupling inductor structure shown in Figure 4.1 has equal air gaps for the three legs. This coupling inductor can be represented by a magnetic analog circuit consisting of two parts: the reluctance of the magnetic path and the representation of the windings. The

reluctance is represented by a resistor that is solely determined by the physical dimensions and the materials of the magnetic core. The windings are represented as the magnetomotive force (MMF) sources. The characteristics of MMF sources are similar to those of the voltage sources in electric circuits. The magnetic circuit, with MMF sources representing the windings, is shown in Figure 4.5.

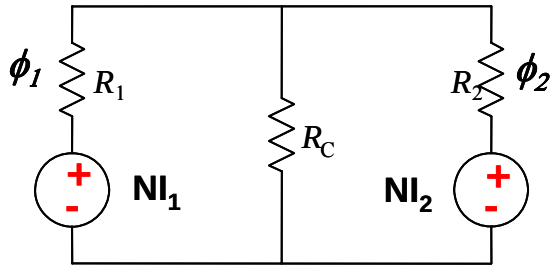


Figure 4.5 The magnetic circuit of a two-phase integrated coupling inductors

From the magnetic reluctance circuit shown in Figure 4.5, the inductances can be derived as follows (assuming $L_1=L_2=L$ and $R_1=R_2=R$):

$$L = L_1 = \frac{N_1}{i_1}\Phi_1 = \frac{N_1}{i_1}\cdot\frac{N_1 i_1}{R_1 + R_c \| R_2} = \frac{N^2(R+R_c)}{R(R+2R_c)} \tag{4.6}$$

$$M = \frac{N^2 R_c}{R(R+2R_c)} \tag{4.7}$$

$$L_k = \frac{N^2}{R+2R_c} \tag{4.8}$$

$$\alpha = \frac{M}{L} = \frac{R_c}{R+R_c} \tag{4.9}$$

By observing (4.9), α can be increased as R/R_c decreases. Because it is L_k that determines the transient inductance, we should keep L_k constant when R and R_c are changing. Let's assume the reluctance of the ferrite core is much smaller than that of the air gap so that only the air gap reluctances are taken into account. We also assume no fringing effect around the gap. For a core structure with a cross section area of A in the outer leg, and 2A in the center leg the reluctances of the gaps (l_g) are:

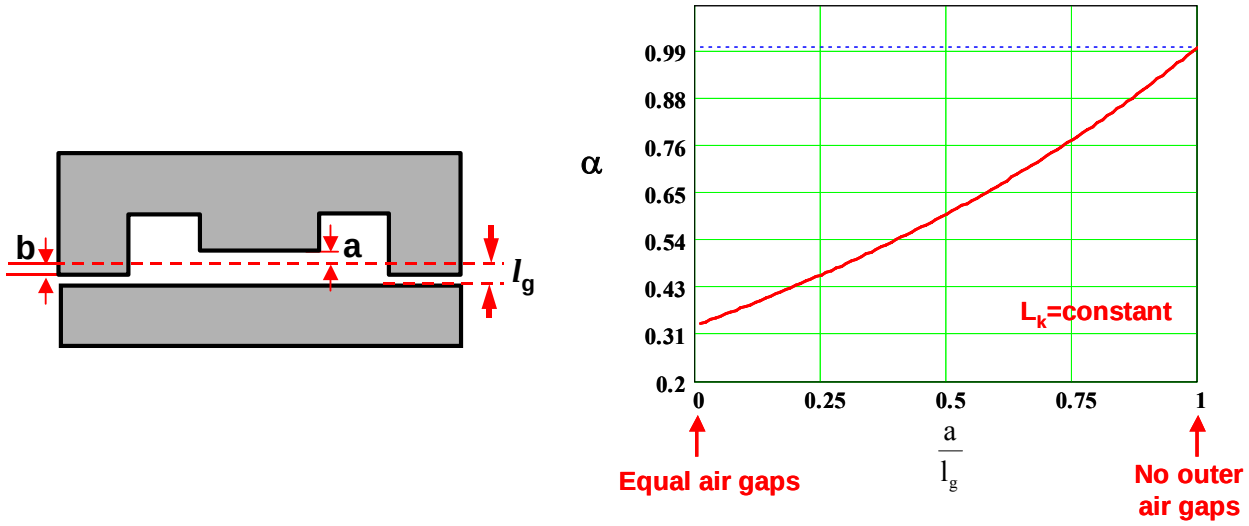
$$R = \frac{l_g}{\mu_0 A} \tag{4.10}$$

$$R_c = \frac{l_g}{2\mu_0 A} \tag{4.11}$$

As mentioned earlier, in order to increase α, R/R_c should decrease. Assuming the outer leg gap reduces by b, and the center leg gap increase by a, as shown in Figure 4.6(a), the leakage inductance becomes:

$$L_k = \frac{N^2 \mu_0 A}{2l_g + a - b} \tag{4.12}$$

As long as a and b are equal, L_k keeps constant. Meanwhile, α increases when a(=b) increases, as shown in Figure 4.6(b).



(a) (b)

Figure 4.6 Adjusting air gaps(a) and its impact on the coupling coefficient(b)

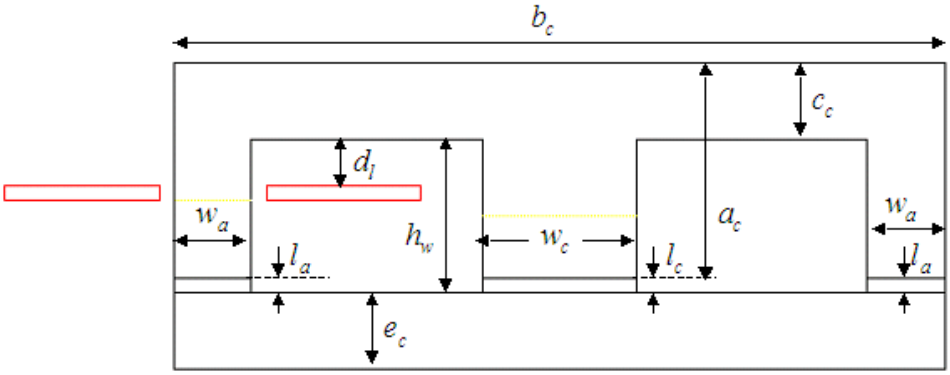
The previous analysis is based on the assumptions that the core reluctance is zero and the fringing effect is ignored. If we were to take these into consideration, the results could be different. A 2D air gap reluctance model considering the fringing effect was proposed by T. G. Wilson [80], which is used here to analyze the circuit. Figure 4.7(a) shows the definitions of the

dimensions for the calculation, and Figure 4.7(b) gives the corresponding reluctance model. In the model, Rmu, Rmc, and Rmi are the reluctances of the core pieces, and Rao, Rac, and Rw are the air gap reluctances with fringing effect. The expressions according to [80] are:

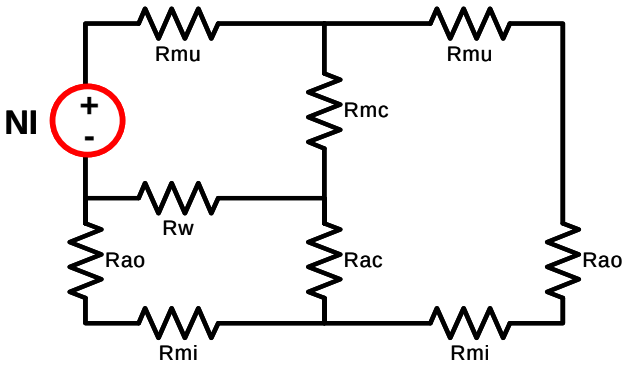
$$\mathrm{Rmu} = \frac{1}{\mu_0 \mu_r}\left(\frac{a_c - c_c}{w_a} + \frac{b_c - w_c - 2w_a}{2c_c} + \frac{\pi}{2}\right) \tag{4.13}$$

$$\mathrm{Rmc} = \frac{1}{\mu_0 \mu_r}\left(\frac{a_c - c_c}{w_c}\right) \tag{4.14}$$

$$\mathrm{Rmi} = \frac{1}{\mu_0 \mu_r}\left(\frac{b_c - w_c - 2w_a}{2e_c} + \frac{\pi}{2}\right) \tag{4.15}$$



(a) Core dimensions



(b) The reluctance model

Figure 4.7 The reluctance model considering core reluctance and the fringing effect

$$Rac = \frac{1}{\mu_0\left[\frac{w_c}{l_c} + \frac{4}{\pi}\left[1 + \ln\left(\pi\frac{(a_c - c_c)}{4l_c}\right)\right]\right]} \tag{4.16}$$

$$Rao = \frac{1}{\mu_0\left[\frac{w_a}{2l_a} + \frac{1}{\pi}\left[1 + \ln\left(\pi\frac{e_c}{2l_a}\right)\right]\right] + \mu_0\left[\frac{w_a}{2l_a} + \frac{2}{\pi}\left[1 + \ln\left(\pi\frac{(a_c - c_c)}{4l_c}\right)\right]\right]} \tag{4.17}$$

$$R_w = \frac{w_w}{\mu_{0(h_w - d_1)}} \tag{4.18}$$

Now we can use this more accurate model to analyze the relationship between the transient inductance (L_k), the coupling coefficient (α) and the air gaps (l_a, l_c). According to the result of the previous analysis, if we want the transient L be fixed, we should keep the sum of one outer leg air gap and the center leg air gap a constant value (l_a+l_c=constant). Table 4.1 lists the core dimensions of one specific design example. The relative permeability of the core, μ_r, is 1800. L_k and α are the functions of l_c, as shown in Figure 4.8. The same core structure was simulated by Maxwell 2D simulation. This result is also shown in Figure 4.8. Both the analytical model and the FEA model show that by adjusting the air gaps of a core, one can get a stronger coupling effect between windings while keeping a relatively fixed value of L_k.

Table 4.1 Dimension parameters of a design example (unit:mm)

w_a	b_c	w_c	e_c	a_c	c_c	d_1	h_w	l_a+l_c
1.5	14	3	1.5	3.5	1.5	1	2	0.3

4.1.2.2. The Phase Current Balance Issue

The major concern of a strongly-coupled inductor is the imbalance of the DC flux. As stated in [74], "For stronger coupling effects, the DC flux differences in the two outer legs are larger. This is the disadvantage of the inverse coupling core structure. This problem can be avoided by using current-sharing control between the two channels." This section studies both

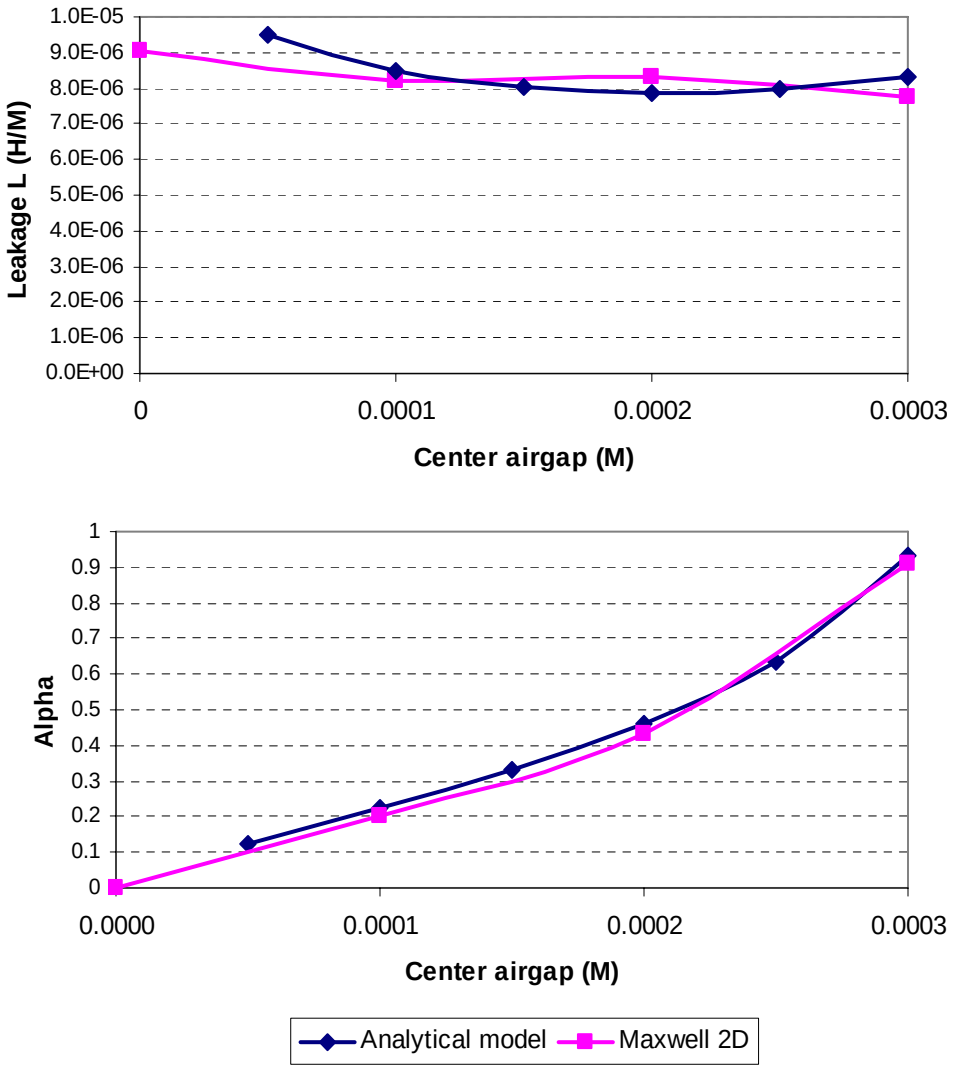


Figure 4.8 L_k and α as functions of l_c when l_a+l_c is constant

the steady state and the dynamic current sharing between two phases of a buck converter with strong coupling inductors (α=0.9). Peak current mode control is used in the analysis.

The case under study is a two-phase buck as shown in Figure 4.9. The power stage along with a peak current controller was simulated in Simplis. Table 4.2 lists the specifications of the circuit. For the steady-state current sharing, the average inductor current, $i_{1(avg)}$ and $i_{2(avg)}$, are measured for different DC resistance ΔR and self-inductance ΔL. ΔR includes the unmatched inductor winding resistance as well as the MOSFETs' on-resistance. The results are shown in Figure 4.10. In Figure 4.10(a), ΔL is zero; in Figure 4.10(b), ΔR is zero. The impact from ΔL to

the phase current sharing is larger than that from ΔR; however, both of them show good current sharing within the large component parameter variation.

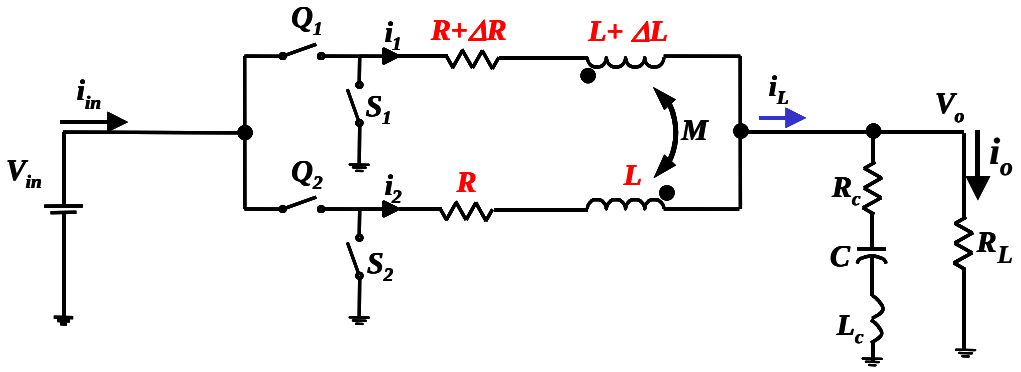


Figure 4.9 A two-phase buck with unmatched parameters

Table 4.2 Specifications of the circuit in Figure 4.9

V_{in}	V_o	I_o	f_s	f_c	R_{droop}	C	R	L	M	α
12V	1.1V	25A	1MHz	330kHz	2mΩ	270μF	2mΩ	1μH	900nH	0.9

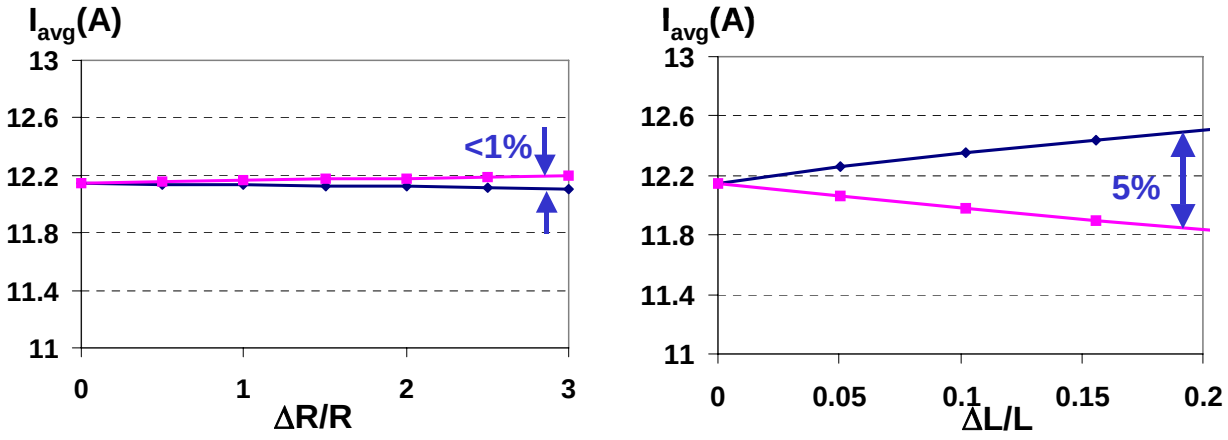


Figure 4.10 The average inductor current for different DC resistance ΔR and self inductance ΔL

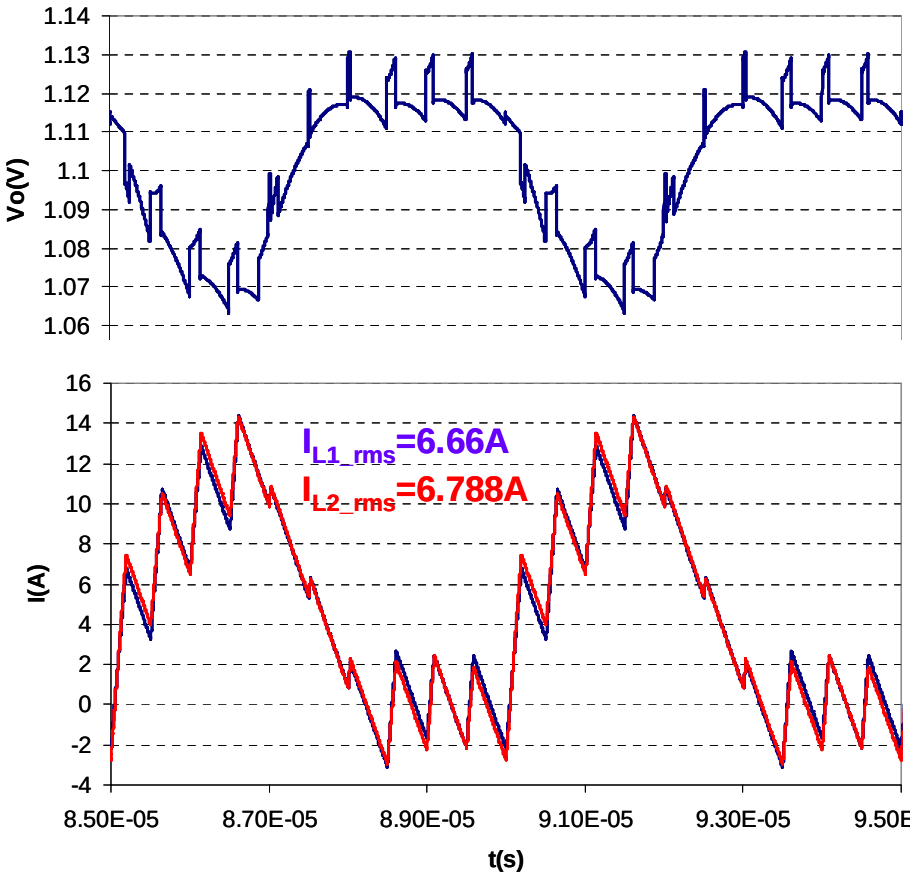


Figure 4.11 Dynamic current sharing

During the transient, the two phases can share the current effectively. Using the same parameters as those listed in Table 4.2, a 25A load step at 100A/us slew rate is applied to the circuit. When the load transient repetitive rate increases, the current sharing is still good, as shown in Figure 4.11, in which the repetitive rate is 200kHz.

Generally speaking, the conventional peak current mode control is capable of sharing the phase current. As long as good current sharing is maintained, the stronger coupling between the inductors will not have any detrimental impact on the circuit, such as severe DC flux imbalance.

4.1.3. Existing Strong Coupling Implementations

Pit-Leong's analysis reveals the benefit of strong coupling. As a special case, the strongest coupling is α=1, which means M=L_s in Figure 4.12a. This can be simply represented by a transformer model, as shown in Figure 4.12b. According to equations (4.2) (4.3) and (4.4), the

three equivalent inductances are all zero. To filter the switching pulse into the output voltage, an additional filter inductor has to be added. The complete coupling inductor circuit is actually implemented by two magnetic components: a well-coupled center-tapped autotransformer and a separate output inductor (Figure 4.13a). The physical structure is shown in Figure 4.13b. The structure is also called a "combining transformer" as in [79]. In the following discussions, this structure is referred as "center-tap coupling inductors".

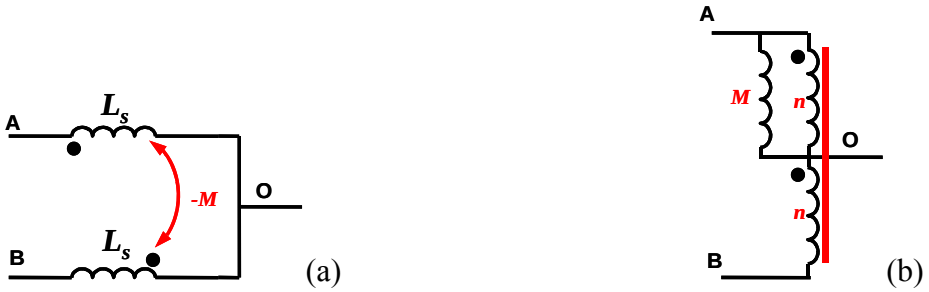


Figure 4.12 Two-winding coupled inductors (a) and the equivalent circuit when L_s=M (b)

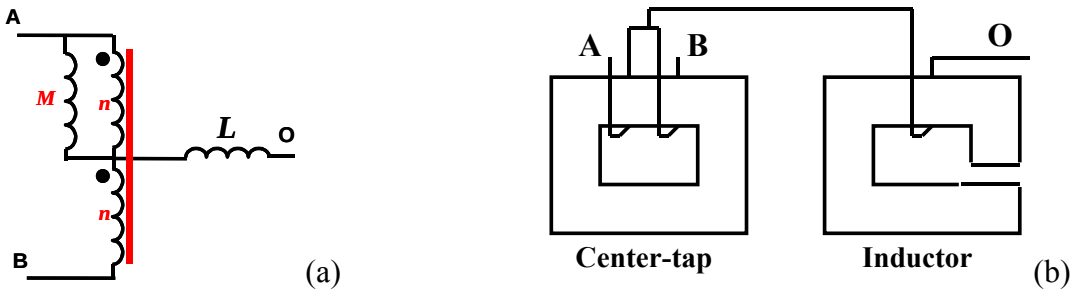
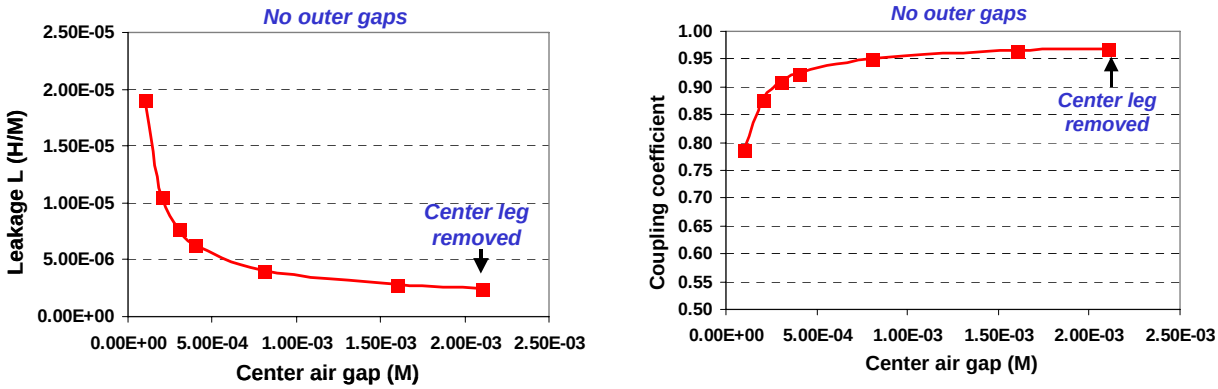


Figure 4.13 Center-tap coupling inductors (a) and the implementations (b)

There is another special case for the coupling inductor shown in Figure 4.1. According to the analysis in section 4.1.2.1, the coupling coefficient approaches one when the outer leg air gaps move to the center leg. Eventually, there will be no outer leg air gap at all. The leakage inductance L_k stays the same during this air gap redistribution. The center leg air gap can be further increased until the entire center leg is removed. Figure 4.14a shows the leakage inductance as a function of the center leg air gap based on the core dimensions in Table 4.1. Meanwhile, the coupling coefficient increases as the center leg becomes shorter and shorter, as illustrated in Figure 4.14b.



(a) (b)

Figure 4.14 Effect of removing the center leg

Based on this understanding, a scalable multi-phase surface mount coupling inductor structure is proposed by [77, 78], as shown in Figure 4.15. For each phase, there is one copper winding around the H-core so that the leg for leakage flux path (center leg in Figure 4.1) is eliminated.

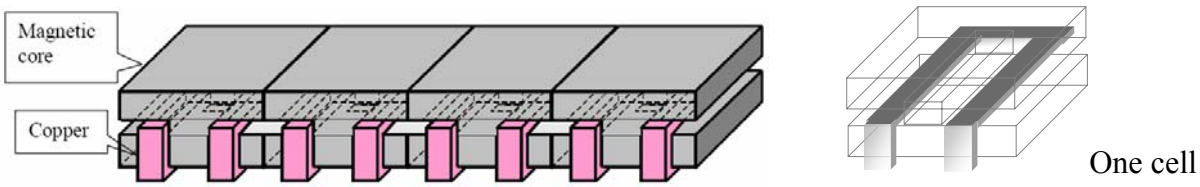


Figure 4.15 A scalable multi-phase surface mount coupling inductor structure proposed by Volterra in [77]

4.2. Proposed Strong Coupling Inductor Structure with Short Winding Length

The coupling inductor structure shown in Figure 4.15 has one disadvantage: in order to make the inverse coupling between phases, the windings must be around the core legs. The winding length is longer than in the non-coupled inductor, and one more copper layer is needed in the layout to connect to the switching node, as illustrated in Figure 4.16.

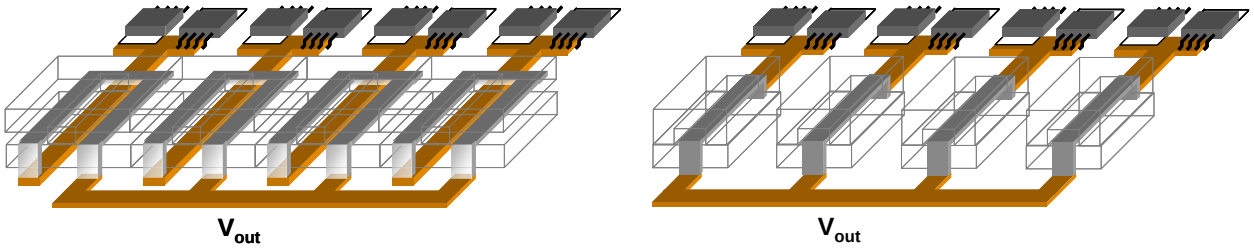


Figure 4.16 Winding length comparison between coupled and non-coupled inductors

To solve this problem, a new core structure is proposed. Figure 4.17 shows the implementation of a three-phase inverse coupling inductor. The two I-bars are actually attached to the three bottom cores without any air gaps to form strong coupling. The inverse coupling between phases is also illustrated in the figure. Assuming the phase currents, i_A, i_B and i_C have the same directions, the flux generated by i_A has the opposite flowing direction of the flux generated by i_B. The same relationship exists between the other two phases. The coupling effect is also experimentally verified as the inductor currents shown in Figure 4.18. Phases A and C have larger ripple currents because the physical asymmetry of the three phases.

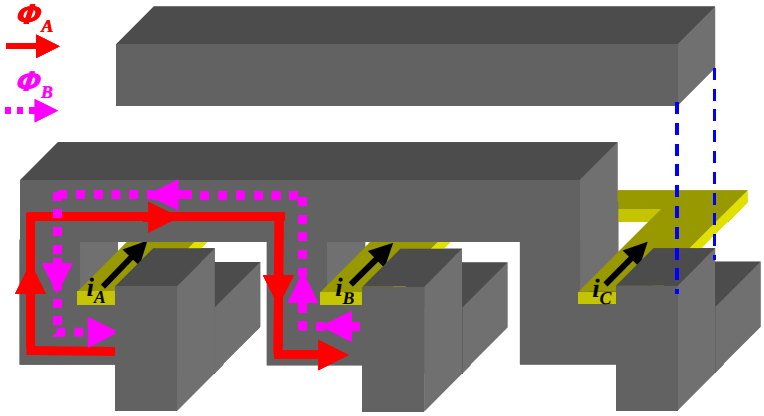


Figure 4.17 Proposed coupled inductor structure

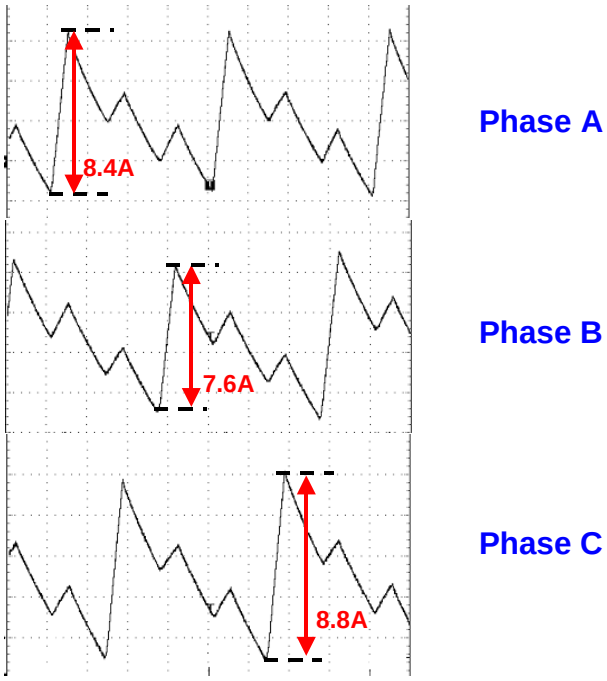


Figure 4.18 Measured inductor current waveforms

The proposed coupling inductor structure has a much smaller winding resistance than the one in Figure 4.15, as shown in Figure 4.19a and b respectively. The winding DC resistance for each phase of Volterra's structure is estimated to be 0.9mΩ, and, in addition, there is about 0.3mΩ PCB trace resistance between the switching node and the inductor terminal. The proposed structure has the windings directly connecting the switching nodes and the output. Based on a design which has the same transient and steady-state inductances, the winding DC resistance for each phase is reduced to 0.3mΩ. The winding loss reduction can contribute about 1.6% efficiency improvement for a 1.2V/100A 4-phase VRM running at 1MHz.

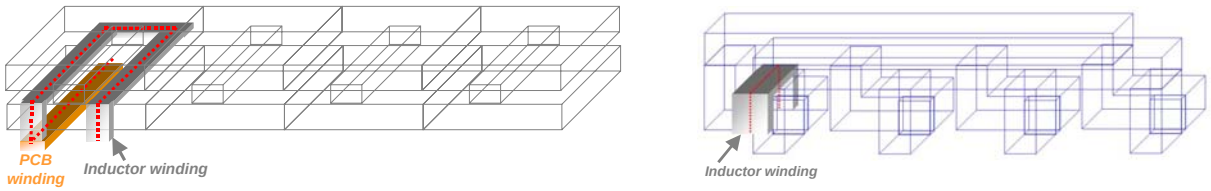


Figure 4.19 The proposed structure reduces the winding length

4.3. Two-phase Coupling Inductors Enhance the VRM Bandwidth

The previous sections reviewed the basic concept about the coupling inductors in VRM applications proposed by Pit-Leong Wong. New implementations emerge following that basic concept. The following sections will tackle another potential benefit of coupling inductors: the control bandwidth is extended by reducing the impact from the current loop sample-hold effect at half the switching frequency.

4.3.1. The Bandwidth Limitation of A Two-Phase Buck Converter Using Peak Current Mode Control

Figure 4.20 shows a two-phase buck converter using peak current mode control. The peak current control scheme is used in order to achieve adaptive voltage positioning as well as the phase current sharing. A current sensing resistor, R_i, is inserted into the converter input side so that the input current is fed back to the controller. The two output inductor currents are decoupled and are separately regulated by the duties of the two phases (Figure 4.21). For example, there is a perturbation of one inductor current at time t. This perturbation will be responded only after one switching cycle, T_s. There will be no change in the other inductor's current. For one phase, the inductor current is "sampled" at time t, and then "held" for a period

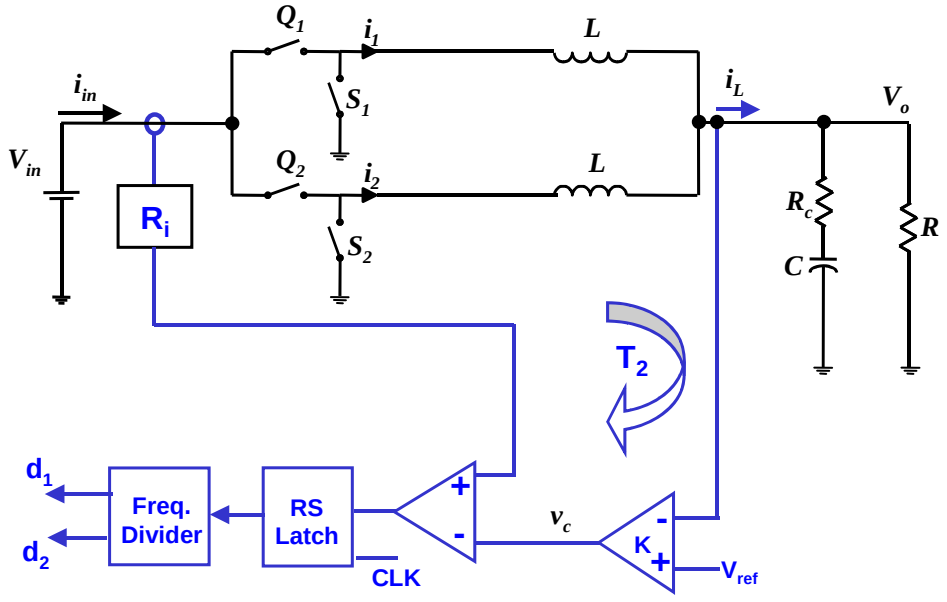


Figure 4.20 A two-phase buck converter using peak current control

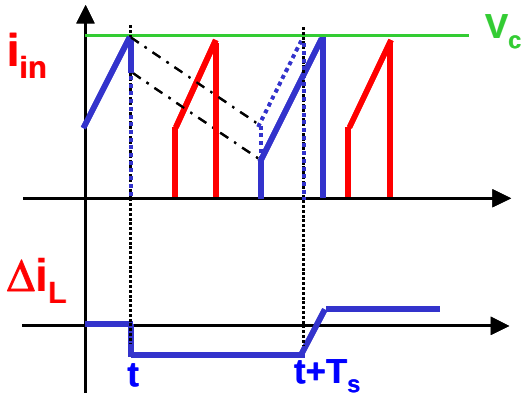


Figure 4.21 Response to the inductor current perturbation

of T_s. This phenomenon is called "sample hold effect" in peak current mode control systems [105, 106]. Although the input current sensing method senses the current information of two-phase current, at any time this sensed signal represents one inductor current or the other, but not both. A small signal model can be derived considering the sample hold effect as shown in Figure 4.22, assuming the input voltage is constant. The sample hold effects are represented by two H_e functions, $H_{e1}(s)$ and $H_{e2}(s)$.

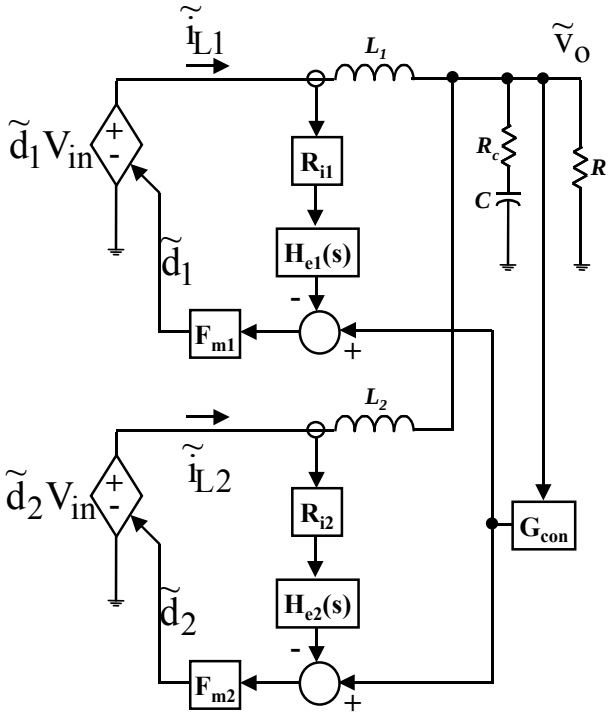


Figure 4.22 Small signal model of a two-phase buck with peak current mode control

Because of the symmetry of the two channels, $L_1=L_2=L$, $F_{m1}=F_{m2}=F_m$, $R_{i1}=R_{i2}=R_i$, and

$$H_{e1}(s)=H_{e2}(s)=\frac{s\cdot T_s}{e^{s\cdot T_s}-1} \tag{4.19}$$

The small signal model in Figure 4.22 can be simplified as a single-phase buck with equivalent parameters as shown in Figure 4.23(a). Therefore:

$$L_e=\frac{L}{2} \tag{4.20}$$

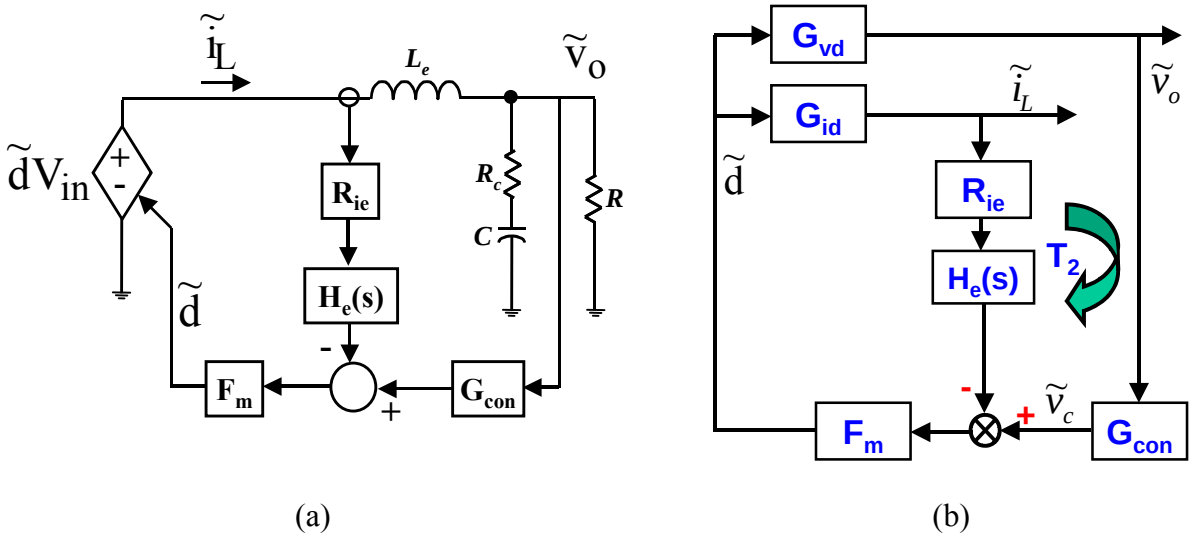


Figure 4.23 Simplified small signal model of Figure 4.22 and its block diagram

$$R_{ie}=\frac{R_i}{2} \tag{4.21}$$

Figure 4.23(b) also gives a control block diagram of the model. The functions in each block can be derived from the model, as follows:

$$G_{vd}=\frac{\tilde{v}_o}{\tilde{d}}=\frac{V_{in}(R+sRR_cC)}{s^2L_eC(R+R_c)+s(L_e+RR_cC)+R} \tag{4.22}$$

$$G_{id}=\frac{\tilde{i}_L}{\tilde{d}}=\frac{V_{in}(1+s(R+R_c)C)}{s^2L_eC(R+R_c)+s(L_e+RR_cC)+R} \tag{4.23}$$

$$F_m=\frac{1}{S_nT_s} \tag{4.24}$$

$$S_n = \frac{V_{in} - V_o}{L_e} R_{ie} \tag{4.25}$$

$$T_2 = \frac{G_{vd} G_{con} F_m}{1 + G_{id} R_{ie} H_e F_m} \tag{4.26}$$

$$T_i = F_m G_{id} R_{ie} H_e \tag{4.27}$$

The current loop sample hold effect is clearly shown in the T_i loop gain and phase in Figure 4.24. Although the two-phase interleaving buck doubles the frequency of the total output current ripple, the phase of T_i still drops to -180° at half the switching frequency.

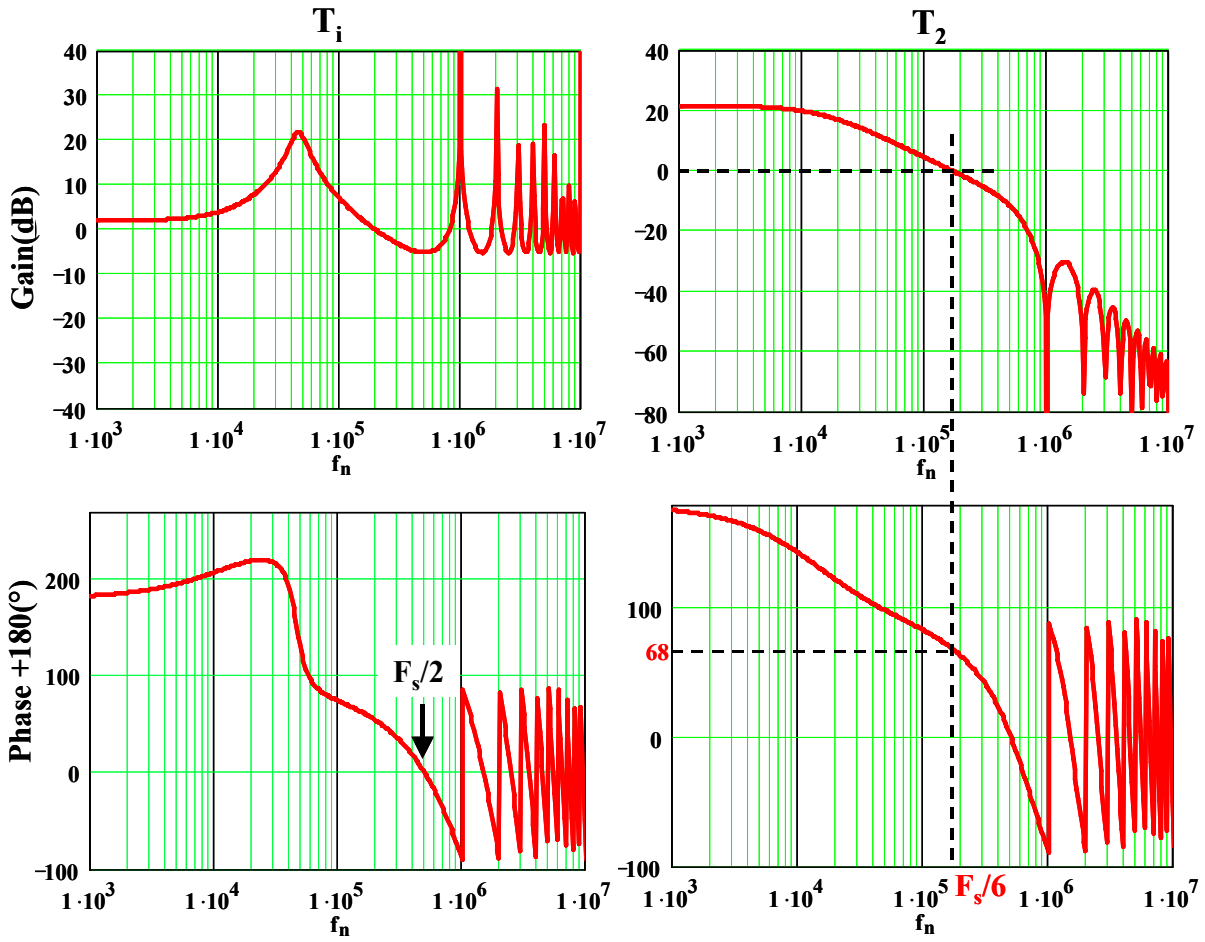


Figure 4.24 T_i and T_2 gain-phase of a conventional two-phase buck with peak current mode control

The system loop gain T_2 and its phase of the converter running at 1MHz with the current loop closed is plotted in Figure 4.24. The phase quickly drops to -180° at half the switching

frequency. Therefore, the system bandwidth is limited by this large phase-drop and, practically, a bandwidth cannot exceed 1/6 of the switching frequency that gives enough phase-margin for a stable system.

4.3.2. Inductor Coupling Impacts the Current Loop Sample Hold Effect

In Figure 4.21, the current perturbation in one phase will not influence the other phase within one switching cycle. The reason for this is the decoupling of the two-phase current. What if the inductor current for one phase has some information of the other phase current? The most straightforward implementation is a center-tap structure, as shown in Figure 4.25. Two magnetic components are needed for this implementation. The first magnetic component Tr1 is basically a transformer with two equal-turn windings ideally coupled (i.e. the coupling coefficient is 1). The second magnetic component L is a conventional inductor that serves as the output filter. In Figure 4.25, phase current i_1 and i_2 are fully coupled by Tr_1. Let's assume that Tr_1 has infinitely large magnetizing inductance. Practically, large RMS current goes through those windings so that a single-turn structure is usually used in order to minimize the winding conduction loss. The magnetizing inductance could not be infinite. The impact of the magnetizing inductor will be discussed in detail later. The current waveforms are illustrated in Figure 4.26 (a). At time t, one phase current i_1 is perturbed. This perturbation will be held for half the switching cycle and then be responded by i_2, as shown in Figure 4.26(b). In other words, the frequency at which there is –180-degree phase drop caused by the sample hold effect will be pushed to the switching frequency, which is twice the frequency as with a non-coupled inductor.

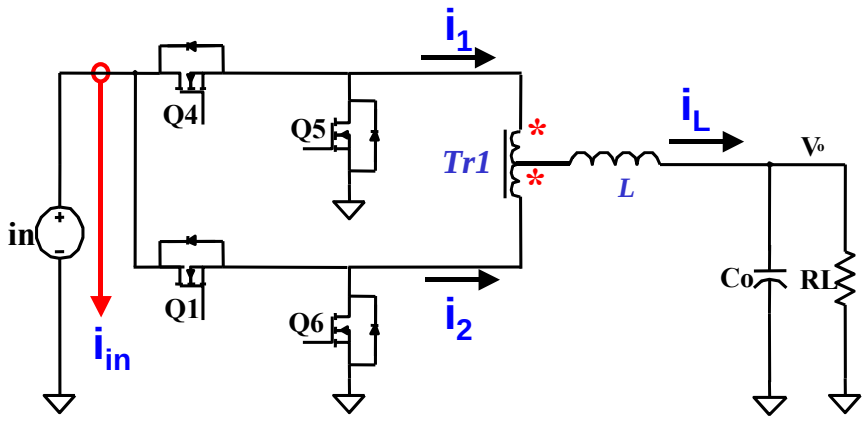


Figure 4.25 Two-phase buck with center-tap coupling inductors

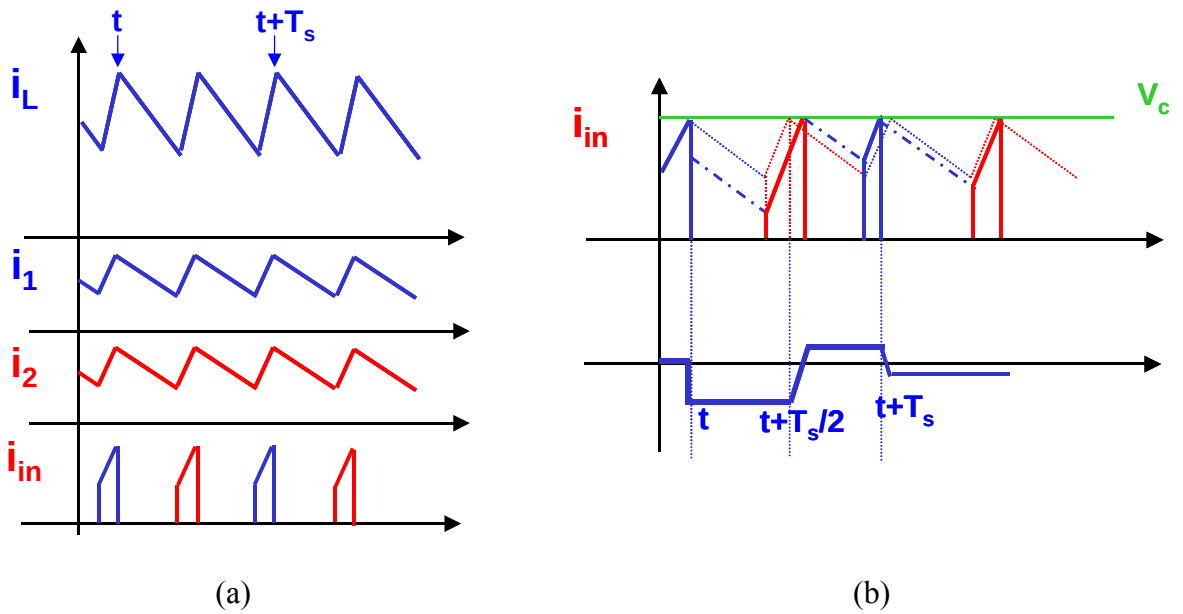


Figure 4.26 Current waveforms and its response to a perturbation of the circuit in Figure 4.25

The circuit in Figure 4.25 can be considered as a single-phase buck running at twice the switching frequency. Its small signal model is shown in Figure 4.27. The equivalent input voltage is reduced to half because Tr1 in Figure 4.25 serves as a 2:1 transformer. The control block functions in Figure 4.27 is listed below:

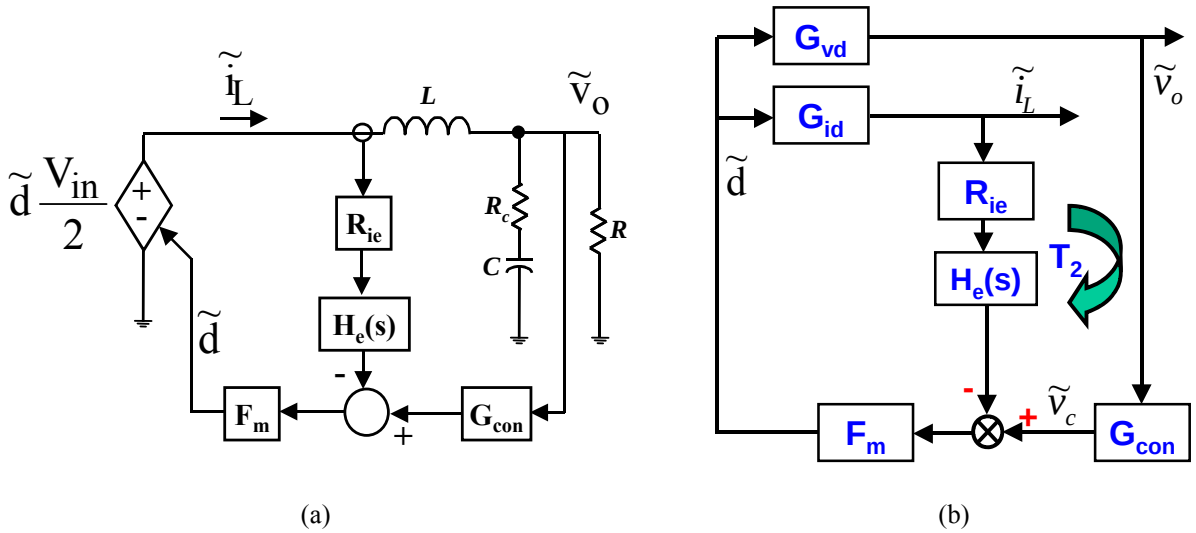


Figure 4.27 Small signal model of the circuit in Figure 4.25

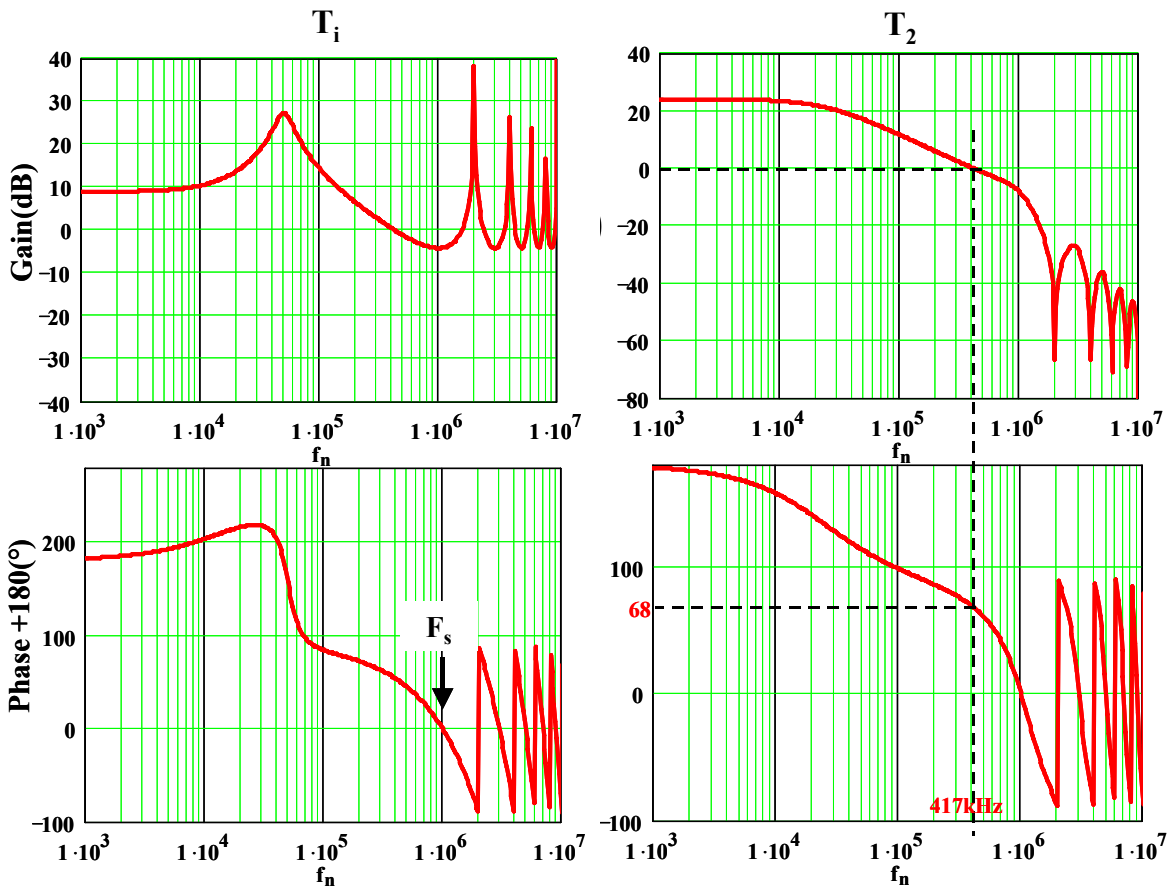


Figure 4.28 T_i and T_2 gain-phase of a two-phase buck with center-tap coupled inductors

$$H_e(s) = \frac{s \cdot \frac{T_s}{2}}{e^{s \cdot \frac{T_s}{2}} - 1} \tag{4.28}$$

$$G_{vd} = \frac{\tilde{v}_o}{\tilde{d}} = \frac{\frac{V_{in}}{2}\left(R + sRR_cC\right)}{s^2LC\left(R + R_c\right) + s\left(L + RR_cC\right) + R} \tag{4.29}$$

$$G_{id} = \frac{\tilde{i}_L}{\tilde{d}} = \frac{\frac{V_{in}}{2}\left(1 + s\left(R + R_c\right)C\right)}{s^2LC\left(R + R_c\right) + s\left(L + RR_cC\right) + R} \tag{4.30}$$

$$F_m = \frac{2}{S_n T_s} \tag{4.31}$$

$$S_n = \frac{\frac{V_{in}}{2} - V_o}{L} R_{ie} \tag{4.32}$$

According to the model, the gain-phase of the current loop T_i and the system loop T_2 are plotted in Figure 4.28. Compared to Figure 4.24—the non-coupled case—the -180° phase frequency is doubled. The system bandwidth is pushed over 1/3 of the switching frequency with the same phase margin as with the non-coupled inductor.

All the discussions above are based on one assumption: the magnetizing inductance is infinitely large. This is not always true in a real coupled inductor implementation. The existence of the magnetizing inductor will have influence on the system loop gain and its phase. The following section will propose a small-signal model considering the magnetizing inductor in the center-tap coupling inductor implementation.

4.3.3. Proposed Small-Signal Model of A Two-phase VR Using the Center-tap Inductor Coupling

The magnetizing inductor of the transformer should be taken into account in a real case. Figure 4.29 shows a simplified circuit of Figure 4.25 when magnetizing inductor L_m is considered. In Figure 4.29, i_m represents the magnetizing current with the direction shown in the figure. When Q_1 is on, i_m increases linearly at a slope of S_m. When Q_1 and Q_2 are both off, i_m stays constant. After that, Q_2 turns on, and i_m decreases linearly with the same slope S_m, and then reverses its direction. Therefore:

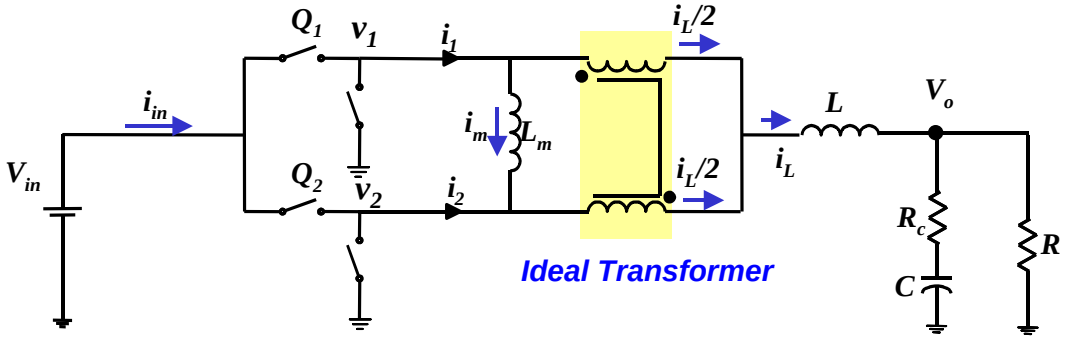


Figure 4.29 Equivalent circuit of a two-phase buck with center-tap coupling inductor considering its magnetizing inductance

$$S_m = \frac{V_{in}}{L_m} R_i \tag{4.33}$$

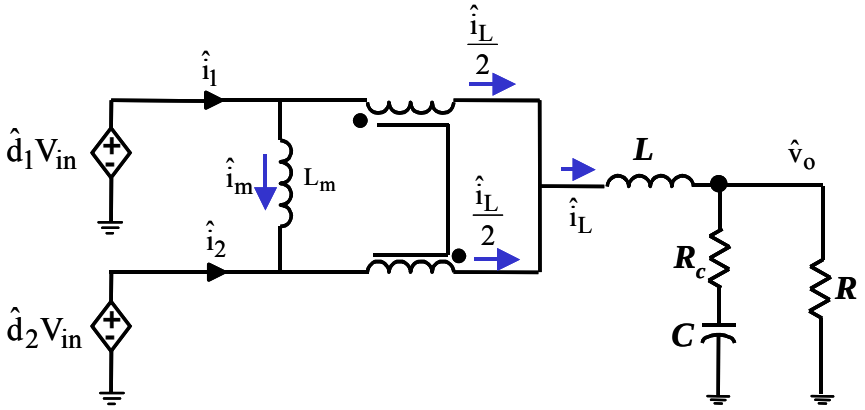
Applying the PWM switch model to the circuit, a small-signal-average model of the power stage shown in Figure 4.29 is derived and shown in Figure 4.30(a). We assume that the input voltage stays constant. Therefore,

$$\hat{i}_1 = \hat{i}_m + \frac{i_L}{2} = \frac{V_{in}}{sL_m}(\hat{d}_1 - \hat{d}_2) + \frac{\hat{i}_L}{2} = \hat{i}_{m1} - \hat{i}_{m2} + \frac{\hat{i}_L}{2} \tag{4.34}$$

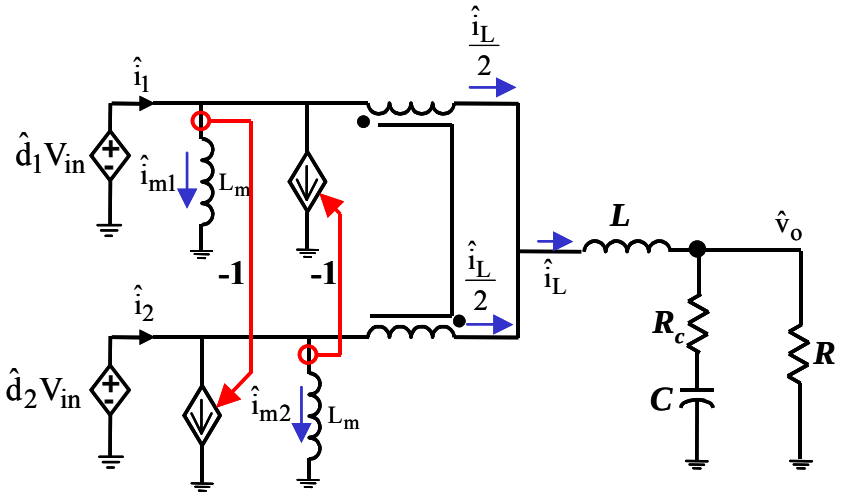
and

$$\hat{i}_2 = -\hat{i}_m + \frac{i_L}{2} = \frac{V_{in}}{sL_m}(\hat{d}_2 - \hat{d}_1) + \frac{\hat{i}_L}{2} = \hat{i}_{m2} - \hat{i}_{m1} + \frac{\hat{i}_L}{2}. \tag{4.35}$$

According to (4.34) and (4.35), the circuit in Figure 4.30(a) can be transformed into the equivalent circuit in Figure 4.30(b). The sensed currents for peak current control are $\hat{i}_1$ and $\hat{i}_2$, in an interleaved manner. For example, the duty cycle of the first phase, $\hat{d}_1$, is determined by $\hat{i}_{m1}$, $\hat{i}_{m2}$, $\hat{i}_L$, and $\hat{v}_o$ so that there are four state variables in the system. Figure 4.31 shows a control block diagram illustrating the relationships among these four variables. The cross-coupled function block H_{es} represents the influence from one phase's duty cycle to the other phase's current.



(a)



(b)

Figure 4.30 The average models of a two-phase buck with center-tap coupling inductor considering its magnetizing inductance

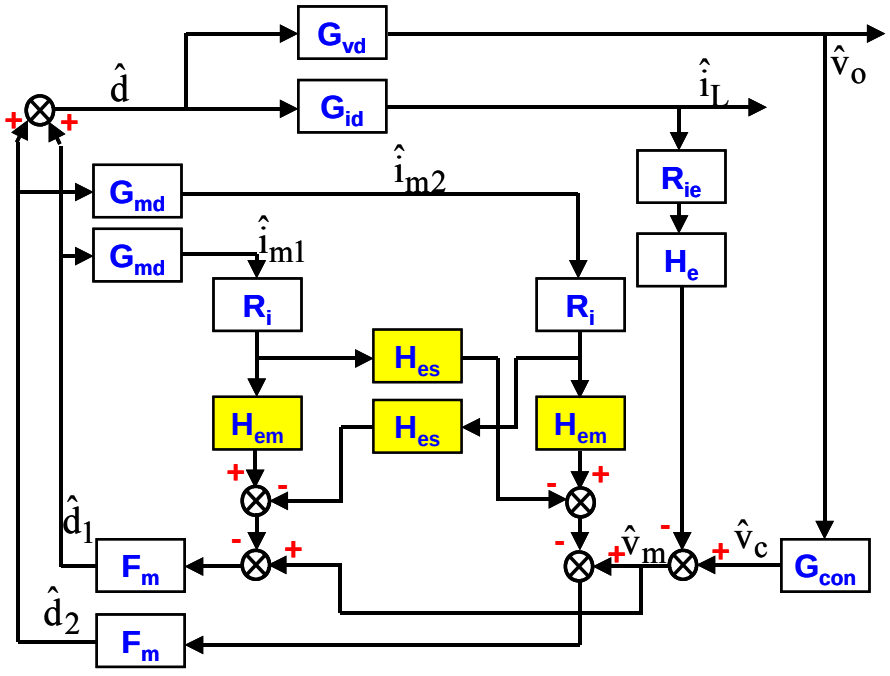


Figure 4.31 Complete model for a two-phase buck with center-tap coupling inductor considering its magnetizing inductance

In Figure 4.31, G_{vd}, G_{id}, R_{ie}, H_e, and G_{con} are the same as those in Figure 4.27. The rest of the blocks need to be derived. According to Figure 4.30(b), the two phases have two separate

variables, $\hat{i}_{m1}$ and $\hat{i}_{m2}$; therefore, the control loops for these two variables are separated as well. Thus:

$$R_i = 2R_{ie} \tag{4.36}$$

$$F_m = \frac{1}{(S_n + S_m)\cdot T_s} \tag{4.37}$$

$$S_n = \frac{\frac{V_{in}}{2} - V_o}{2L} R_i \tag{4.38}$$

In Figure 4.31, $\hat{i}_{m1}$ and $\hat{i}_{m2}$ are the responses of $\hat{d}_1$ and $\hat{d}_2$ based on one-switching-cycle averaging. Figure 4.32 shows the relationship among $\hat{d}_1$, $\hat{i}_{m1}$, and $\frac{d\hat{i}_{m1}}{dt}$, which gives:

$$G_{md} = \frac{\hat{i}_{m1}}{\hat{d}_1} = \frac{V_{in}}{sL_m} \tag{4.39}$$

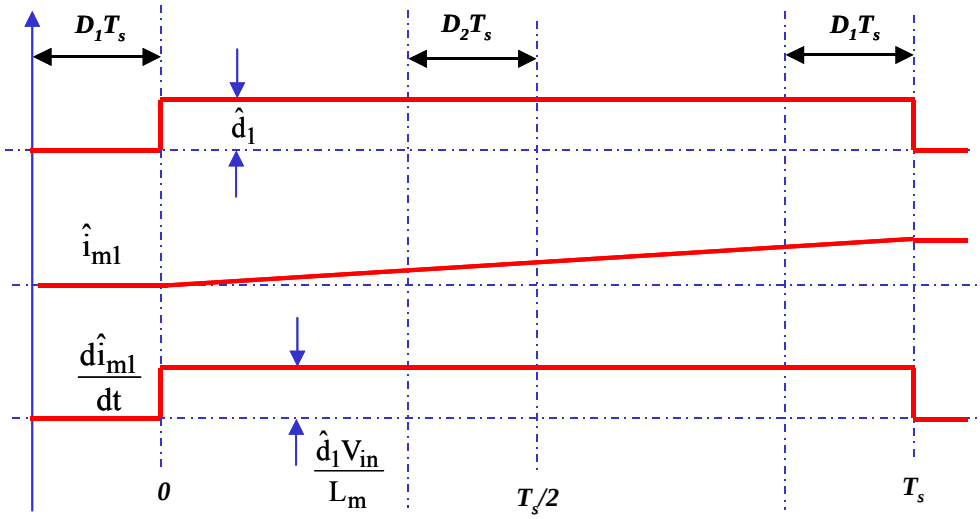


Figure 4.32 The relationship among $\hat{d}_1$, $\hat{i}_{m1}$, and $\frac{d\hat{i}_{m1}}{dt}$, on switching-cycle averaging basis

However, due to the cross-coupling of $\hat{i}_{m1}$ and $\hat{i}_{m2}$, and the 180° phase difference between d_1 and d_2, the system needs to sample $\hat{i}_{m1}$ (actually $\frac{d\hat{i}_{m1}}{dt}$) within the half-period from 0

to $\frac{T_s}{2}$. The reason for this is that the overall change of $\hat{i}_{m1}$ happens within the half-period from 0 to $\frac{T_s}{2}$, and this change has to be sampled and used to influence the other channel duty cycle, d_2. By averaging the switching cycle in Figure 4.32, we are not able to model the behavior between the two phases.

One modification can be made to the control block diagram in Figure 4.31. Since we already know that the perturbation of d_1 occurs only during the [0, $\frac{T_s}{2}$] interval, the averaging can be done within half the cycle, as shown in Figure 4.33.

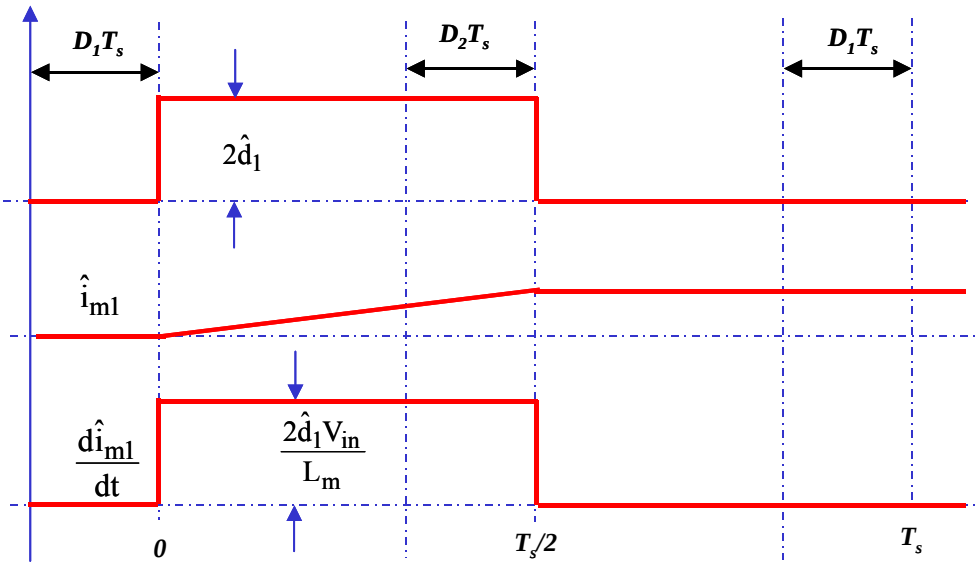


Figure 4.33 The relationship among $\hat{d}_1$, $\hat{i}_{m1}$, and $\frac{d\hat{i}_{m1}}{dt}$, on half-switching-cycle averaging basis

According to Figure 4.33:

$$\frac{d\hat{i}_{m1}}{dt} = \frac{2\hat{d}_1 V_{in}}{L_m} \tag{4.40}$$

By applying the Laplace transformation, we have:

$$G_{md} = \frac{\hat{i}_{m1}}{\hat{d}_1} = \frac{V_{in}}{s(L_m/2)} \tag{4.41}$$

Note that $\hat{i}_{m1}$ and $\hat{d}_1$ are both based on half-switching-cycle averaging. Equation (4.41) is used instead of (4.39) in the proposed model for G_{md}.

The function blocks H_{em} and H_{es} representing the sample hold effect of the magnetizing current within and between phases. Based on the previous analysis, the holding time for H_{em} is T_s, so that:

$$H_{em}(s) = \frac{sT_s}{e^{sT_s} - 1} \tag{4.42}$$

The holding time for H_{es} is $\frac{T_s}{2}$, which gives:

$$H_{es}(s) = \frac{sT_s/2}{e^{sT_s/2} - 1} \tag{4.43}$$

According to Figure 4.31, the transfer function from $\hat{v}_m$ to $\hat{d}$ is:

$$G_m = \frac{2F_m}{1 + F_m G_{md} R_i (H_{em} - H_{es})} \tag{4.44}$$

and the system loop gain T_2 with all the loops closed is:

$$T_2 = \frac{G_{vd} G_m G_{con}}{1 + G_m G_{id} R_i H_e}. \tag{4.45}$$

4.3.4. Using the Proposed Model to Evaluate the Performance of the Center-tap Coupling Inductor

The previous section proposed a small-signal model for a peak-current-controlled 2-phase buck with center-tap coupling inductors. The finite magnetizing inductance will play an important role, as the model indicates. In this section, a specific design will be evaluated in terms of control bandwidth. Table 4.3 lists the specifications of the 2-phase buck under consideration.

Using the proposed model, the loop-gain and phase of the circuit in Figure 4.29 with different magnetizing inductors is shown in Figure 4.34. The impact of the magnetizing inductor L_m can be clearly observed. When L_m decreases, the phase decreases as well. It is because the sample hold effect caused by $H_{em}(s)$ becomes dominant. As verification, the circuit is also built

Table 4.3 Design specifications

V_{in}	Input voltage	12V
V_o	Output voltage	1.1V
I_o	Max load current	25A
f_s	Switching frequency per phase	1MHz
R_o	Closed loop output impedance	2mΩ
L	Output inductor	50nH
C	Output capacitor	270uF
R_i	Current sensing resistor	5mΩ

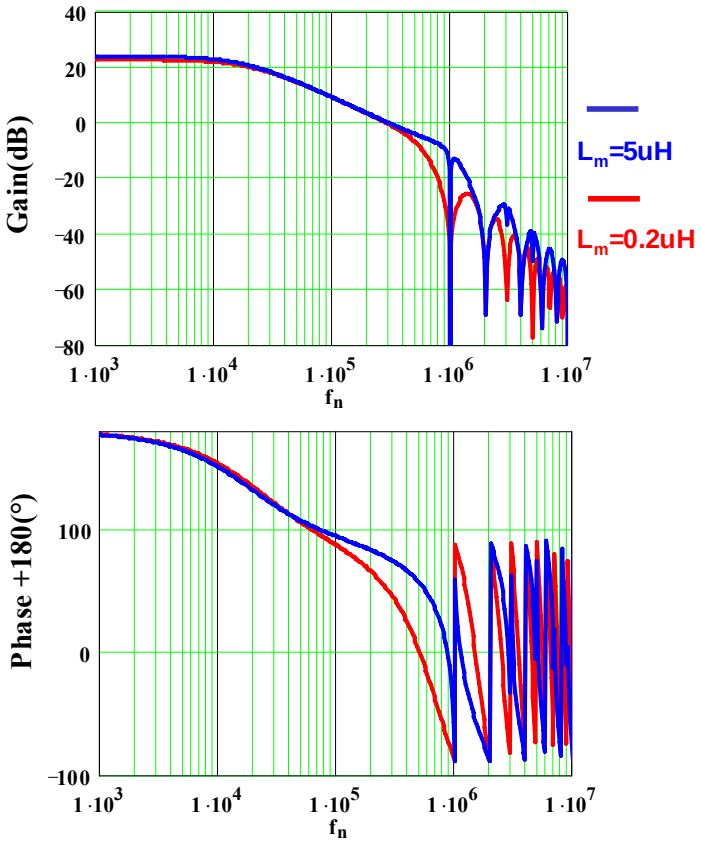


Figure 4.34 The loop gain and phase with different magnetizing inductors (from the model)

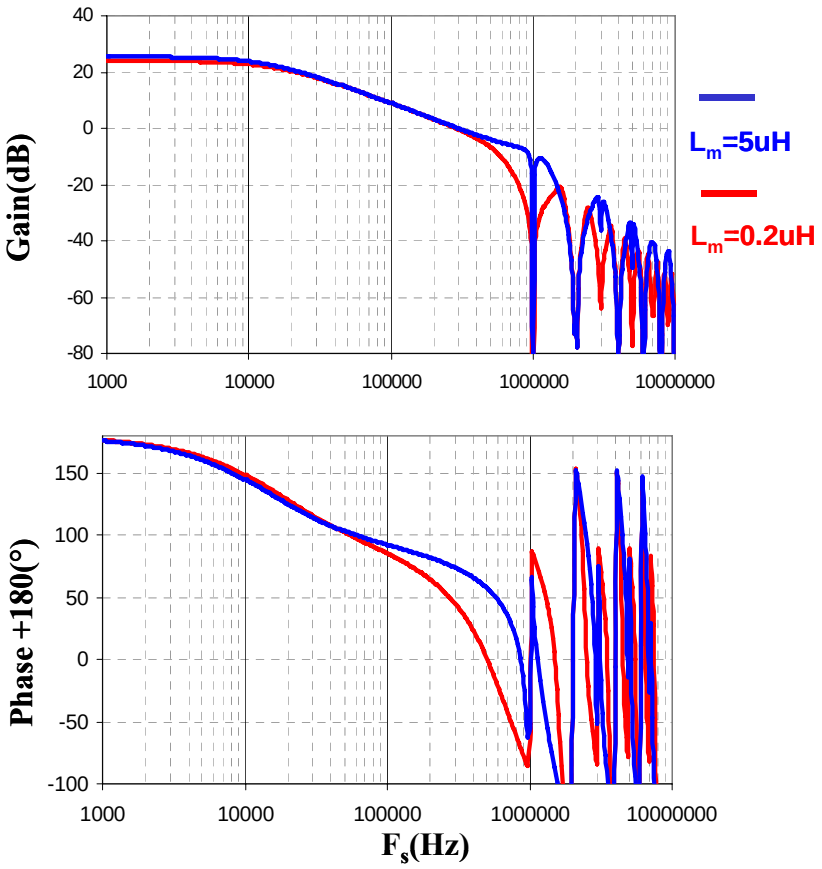


Figure 4.35 The loop gain and phase with different magnetizing inductors (from Simplis)

in Simplis simulator. The loop gain and the phase are plotted in Figure 4.35, and match the results from the proposed model very well.

4.3.5. Experimental Verifications

The derivation of the small-signal model is based on a two-phase buck converter; however, the concept of the center-tap coupling inductors to enhance the control bandwidth can easily be applied to the proposed CCB self-driven VRs, which is the main objective of this study. As opposed to the topology shown in Figure 3.4, which has a current-doubler output stage, the circuit shown in Figure 4.36 contains a center-tap output stage.

A prototype of the CCB self-driven VR with center-tap coupling inductor was built, as shown in Figure 4.37. The magnetizing inductance reflected to the secondary side is about 2uH. The switching frequency is 700kHz. Figure 4.38(a) shows the loop gain and phase of the current-

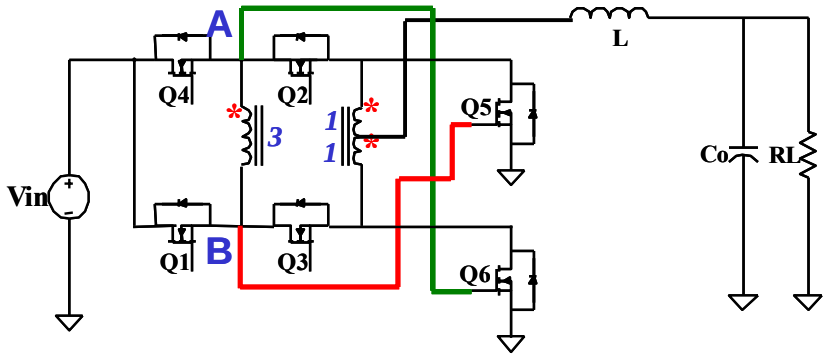


Figure 4.36 Proposed CCB self-driven VR with center-tap coupling inductors

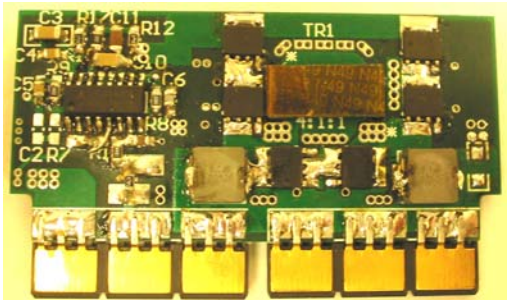
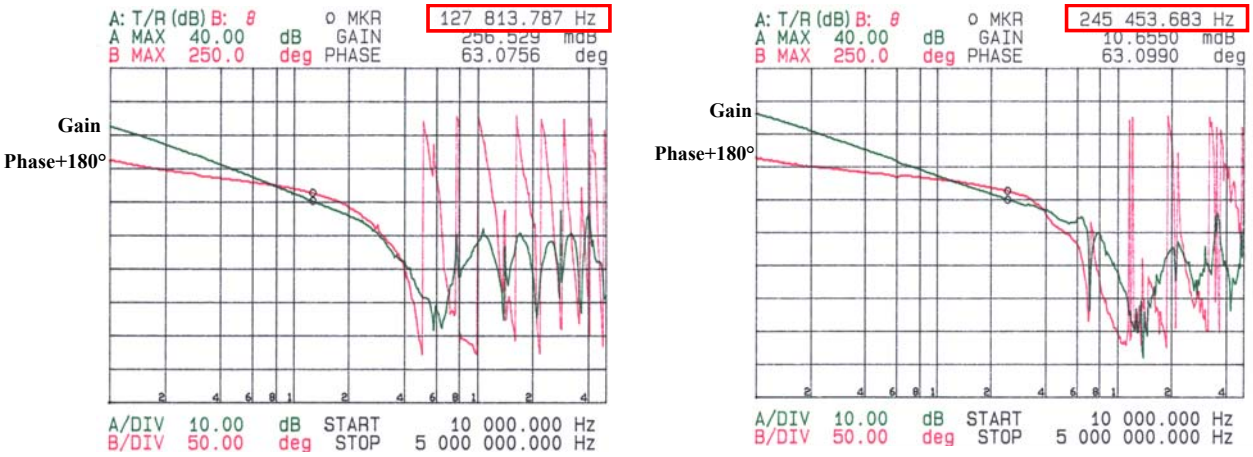


Figure 4.37 Prototype of the CCB self-driven VR with center-tap coupling inductors



(a) Self-driven VR with current-doubler (b) Self-driven VR with center-tap

Figure 4.38 Measured T_2 loop gain and phase

doubler case. The bandwidth is 128kHz ($\approx 1/6f_s$) with 63-degree phase margin. Figure 4.38(b) shows the loop gain and phase margin of the center-tap structure. The bandwidth is pushed to 245kHz ($\approx 1/3f_s$) with the same phase margin. One can still see a phase drop at f_s in Figure

4.38(b), which is due to the sampling hold function H_{em} as shown in the model. Figure 4.39 shows the step-up and step-down transient of the coupled inductor VR. The current step is 30A with 100A/us slew rate. The designed droop resistance is 2mohm. A 270uF decoupling capacitor is used in the test.

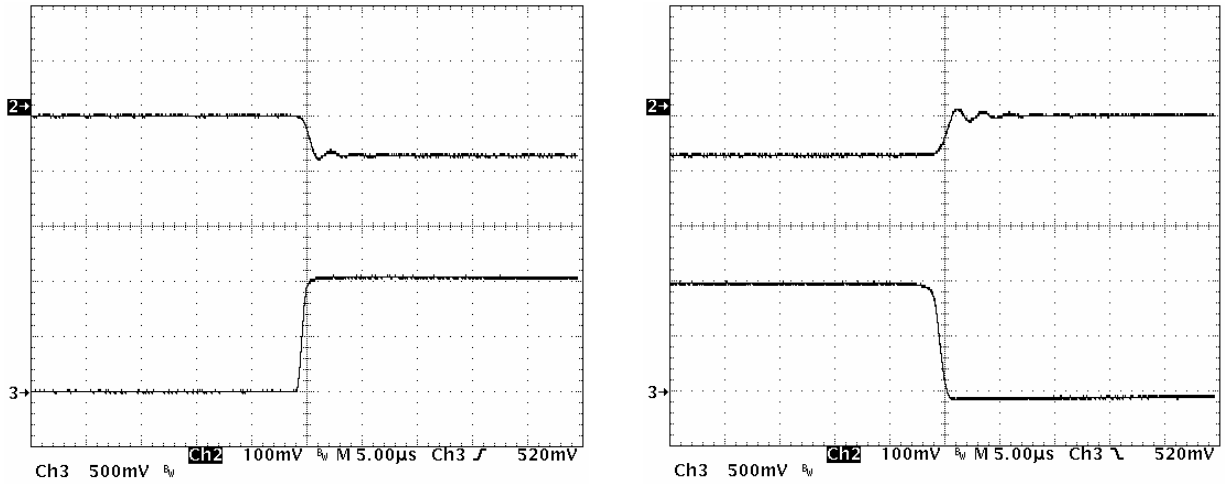


Figure 4.39 The step-up and step-down transient of the coupled inductor VR

4.3.6. Proposed Small Signal Model Applies to Integrated Coupling Inductors

The proposed small-signal model is also valid for integrated coupling inductors proposed by Pit-Leong Wong. The magnetic structure shown in Figure 4.1 can also be represented by a two-winding transformer model, as shown in Figure 4.40(b). The inductors, L_s-M, actually represent the leakage inductances for both primary and secondary windings.

The equivalent circuit in Figure 4.40(b) can be further transformed into the one in Figure 4.40(c), because the magnetizing inductance M across one winding is now enlarged by 4 times when it is replaced by one inductor across the two windings. The validity of the transformations is verified by simulations. Identical current waveforms are observed by replacing the coupling inductors in Figure 4.40(a) with the one in Figure 4.40(c). In order to make the comparison, a center-tap coupling inductor is also shown in Figure 4.40(d).

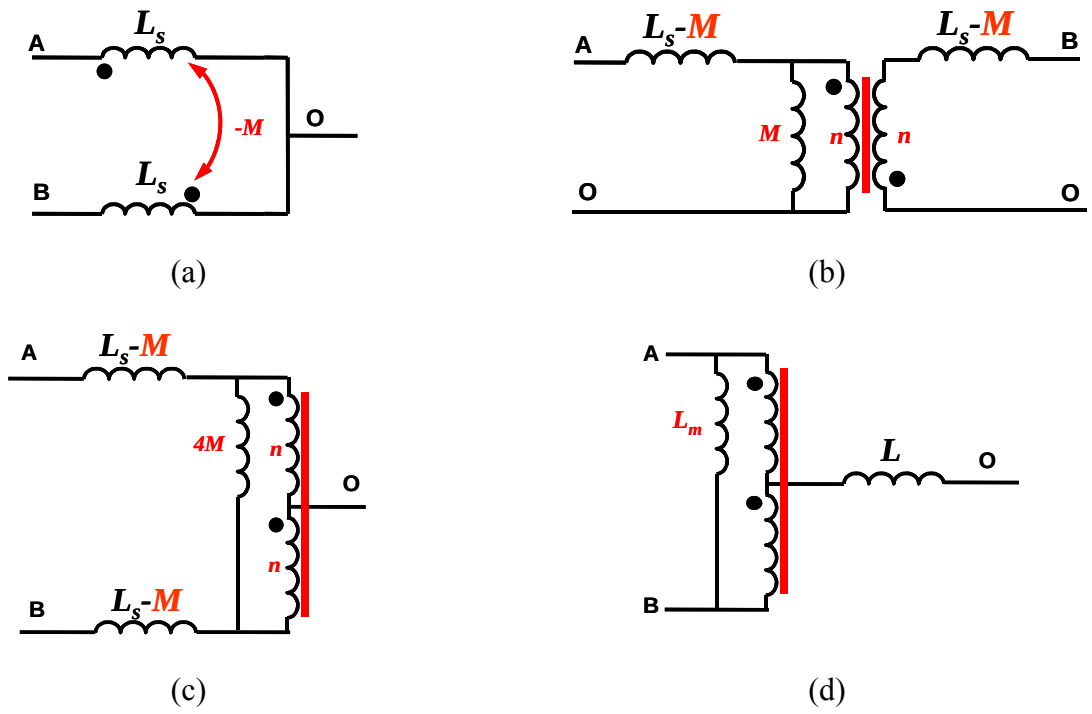


Figure 4.40 The equivalent circuits of the integrated coupling inductors (a) and the center-tap coupling inductors (d)

By comparing Figure 4.40(c) and (d), the difference between the integrated coupling L and the center-tap structure is clearly seen. The small-signal model derived for the center-tap coupling inductors (Figure 4.31) can also be used for the integrated case. Table 4.4 gives the different model parameters for the two structures.

Table 4.4 The different model parameters for the two coupling methods in Figure 4.40(a) and (d)

	S_n	S_m
Center-tap	$\frac{V_{in}/2 - V_o}{2L} R_i$	$\frac{V_{in}}{L_m} R_i$
Integrated coupling L	$\frac{V_{in}/2 - V_o}{L_s - M} R_i$	$\frac{V_{in}}{2L_s + 2M} R_i$

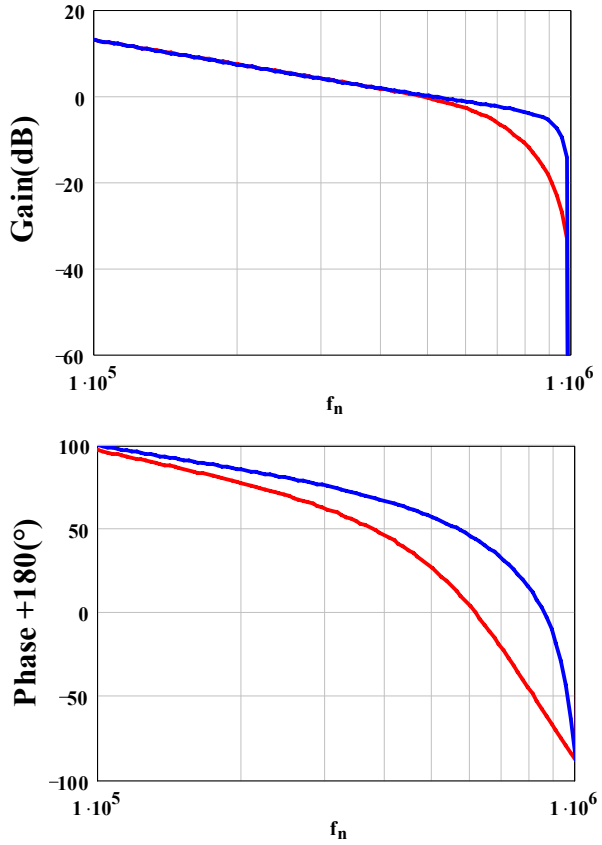


Figure 4.41 The loop gain and phase with different coupling coefficient

For a fixed transient inductance L_s-M, S_n is fixed. However, S_m will decrease when α increases because the denominator of S_m, $2L_s+2M$, increases:

$$L_S + M = \frac{1+\alpha}{1-\alpha}(L_S - M) \tag{4.46}$$

In other words, the inductor equivalent to L_m in the center-tap structure, $2L_s+2M$, will increase when the coupling becomes stronger. As we discussed before, larger L_m will have less phase drop because the impact from $H_{em}(s)$ is reduced.

Figure 4.41 shows the different loop gain and phase for the two coupling coefficients. One is 0.33, as obtained by the implementation shown in Figure 4.1 with three equally distributed air gaps; the other one is 0.9, as we attempted to get strong coupling by adjusting the air gaps. The transient inductance is fixed at 100nH per phase. There is about 30° phase difference at half the switching frequency, which means higher bandwidth can be achieved by strong coupling.

4.4. Three-phase Coupling Inductors in Current-Tripler Converters

The previous sections analyze the small-signal behavior of the two-phase buck with coupling inductors. Since the CCB self-driven 12V VR is basically a buck-derived two-phase interleaving soft switching topology, in terms of control, it has the same features as the two-phase buck. Therefore, the analysis according to the small signal model derived from the two-phase buck is verified by the hardware of a CCB self-driven 12V VR. In this section, a small signal model for a three-phase buck with integrated coupling inductors will be derived following a method similar to the one used for the two-phase case. The results are applicable for the proposed current-tripler converters.

4.4.1. Equivalent Circuits of the Three-phase Coupling Inductors

Figure 4.40 illustrates the two equivalent circuits for the two coupling L implementations. The feature they share is that each of them consists three elements: an ideal transformer, a magnetizing inductor, and the inductors controlling the transient (normally the leakage inductor in the integrated implementation).

A typical implementation of the three-phase coupling inductors is shown in Figure 4.42(a). Its magnetic reluctance model is also shown in Figure 4.42(b). The assumption we made is that the reluctance of the core is much smaller than that of the air gap, so that only the air gap reluctance is considered in the model. The three windings in Figure 4.42(a) are inversely coupled with each other. For example, when the winding currents i_1, i_2, and i_3 are applied with the direction shown in the figure, the flux generated by i_2 and i_3 through the winding1 leg has the opposite direction, with the flux generated by i_1 itself.

Let's define the self-inductance, mutual inductance, and leakage inductance of the three-phase inverse coupling inductors. We apply a current i_1 to winding 1 and keep the other two windings open, as shown in Figure 4.43. The self-inductance of winding 1 is:

$$L_{s1} = \frac{N_1 \Phi_1}{i_1} \tag{4.47}$$

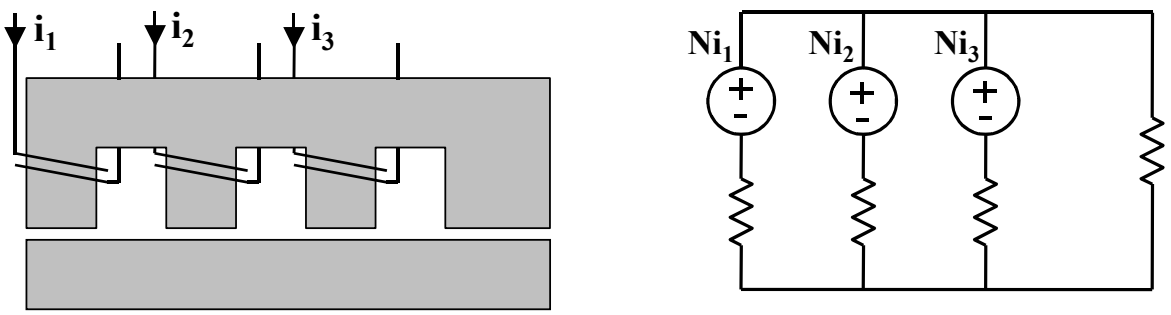


Figure 4.42 A typical implementation of three-phase coupling inductors and its reluctance model

The mutual inductance between winding 1 and winding 2 is:

$$M_{12} = \frac{N_1 \Phi_2}{i_1} \tag{4.48}$$

The mutual inductance between winding 1 and winding 3 is:

$$M_{13} = \frac{N_1 \Phi_3}{i_1} \tag{4.49}$$

The leakage inductance of winding 1 is:

$$L_{k1} = \frac{N_1 \Phi_{k1}}{i_1} = \frac{N_1 (\Phi_1 - \Phi_2 - \Phi_3)}{i_1} = L_{s1} - M_{12} - M_{13} \tag{4.50}$$

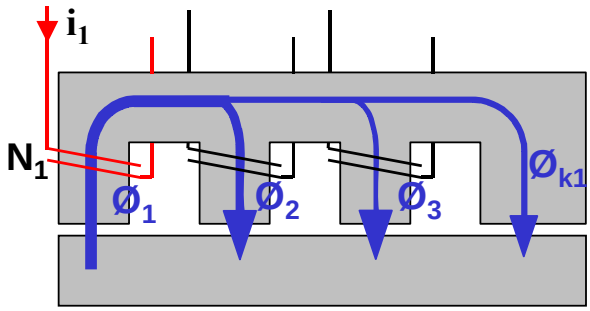


Figure 4.43 Flux distribution when only i_1 is applied

One can define L_{s2}, M_{21}, M_{23}, L_{k2} when only i_2 is applied, or L_{s3}, M_{31}, M_{32}, L_{k3} when only i_3 is applied. Because of the structure symmetry when we ignore the core reluctance:

$$L_{s1} = L_{s2} = L_{s3} = L_s \tag{4.51}$$

$$M_{12} = M_{13} = M_{21} = M_{23} = M_{31} = M_{32} = M \tag{4.52}$$

$$L_{k1} = L_{k2} = L_{k3} = L_k = L_s - 2M \tag{4.53}$$

The structure shown in Figure 4.42(a) can be represented by an equivalent circuit as shown in Figure 4.44. The negative sign before M represents the inverse coupling.

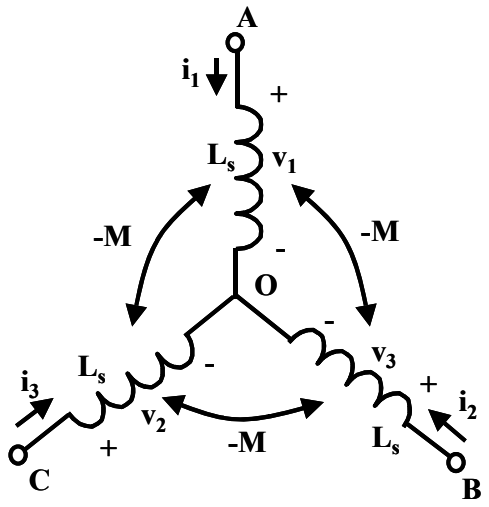


Figure 4.44 An electrical circuit representation of the three-phase coupling inductors

According to Figure 4.44, the voltages across the three windings can be expressed by:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} L_s & -M & -M \\ -M & L_s & -M \\ -M & -M & L_s \end{bmatrix} \cdot \begin{bmatrix} di_1/dt \\ di_2/dt \\ di_3/dt \end{bmatrix} \tag{4.54}$$

As we mentioned previously, to make an equivalent circuit of the coupling inductors with three components—the ideal transformer, the magnetizing inductor, and the inductors controlling the transient (normally the leakage inductor in the integrated implementation) —the following transformation is made:

$$v_1 = (L_s - 2M)\frac{di_1}{dt} + M\left(\frac{di_1}{dt} - \frac{di_2}{dt}\right) + M\left(\frac{di_1}{dt} - \frac{di_3}{dt}\right) \tag{4.55}$$

$$v_2 = (L_s - 2M)\frac{di_2}{dt} + M\left(\frac{di_2}{dt} - \frac{di_1}{dt}\right) + M\left(\frac{di_2}{dt} - \frac{di_3}{dt}\right) \tag{4.56}$$

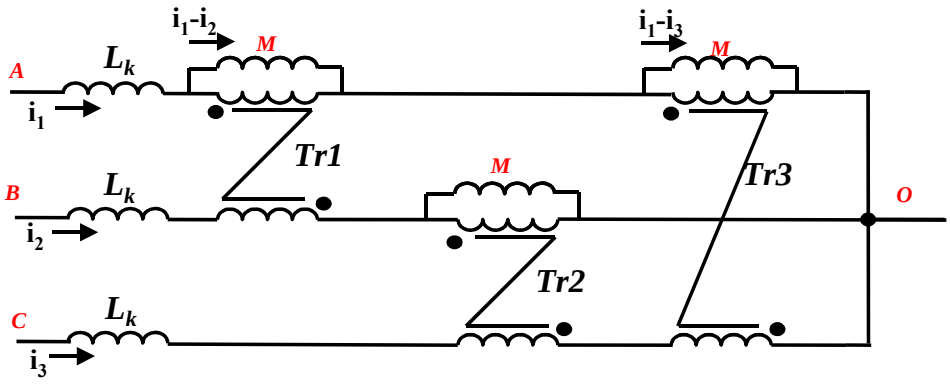


Figure 4.45 Equivalent circuit of three-phase coupling inductors

$$v_3 = (L_s - 2M)\frac{di_3}{dt} + M\left(\frac{di_3}{dt} - \frac{di_1}{dt}\right) + M\left(\frac{di_3}{dt} - \frac{di_2}{dt}\right) \tag{4.57}$$

According to (4.37), (4.38), (4.39), an equivalent circuit is drawn as shown in Figure 4.45. Tr1-Tr3 are three ideal transformers. Figure 4.45 can easily be included in an electric circuit simulation to simulate the behavior of the three-phase coupling inductors.

Equations (4.37), (4.38), (4.39) can be further modified as follows:

$$v_1 = (L_s - 2M)\frac{di_1}{dt} + 3M\left(\frac{di_1}{dt} - \frac{1}{3}\left(\frac{di_1}{dt} + \frac{di_2}{dt} + \frac{di_3}{dt}\right)\right) \tag{4.58}$$

$$v_2 = (L_s - 2M)\frac{di_2}{dt} + 3M\left(\frac{di_2}{dt} - \frac{1}{3}\left(\frac{di_1}{dt} + \frac{di_2}{dt} + \frac{di_3}{dt}\right)\right) \tag{4.59}$$

$$v_3 = (L_s - 2M)\frac{di_3}{dt} + 3M\left(\frac{di_3}{dt} - \frac{1}{3}\left(\frac{di_1}{dt} + \frac{di_2}{dt} + \frac{di_3}{dt}\right)\right) \tag{4.60}$$

According to (4.40), (4.41), and (4.42), one can draw a new equivalent circuit including an ideal three-phase autotransformer, Tr, as shown in Figure 4.46. One important feature of Tr is that the instantaneous currents through its windings i_a, i_b, and i_c are always identical. In order to verify that the circuits in Figure 4.45 and in Figure 4.46 are equivalent, both are plugged into a three-phase buck converter simulation circuit and the exactly same current waveforms are observed, as shown in Figure 4.47. Note that the ideal three-phase autotransformer in Figure 4.46 is configured as a three-phase Gyrator model introduced by David [104]. The equivalent circuit

shown in Figure 4.46 is just like the one for the two-phase case in Figure 4.40, which has the leakage inductors, the magnetizing inductors, and the ideal two-phase autotransformer.

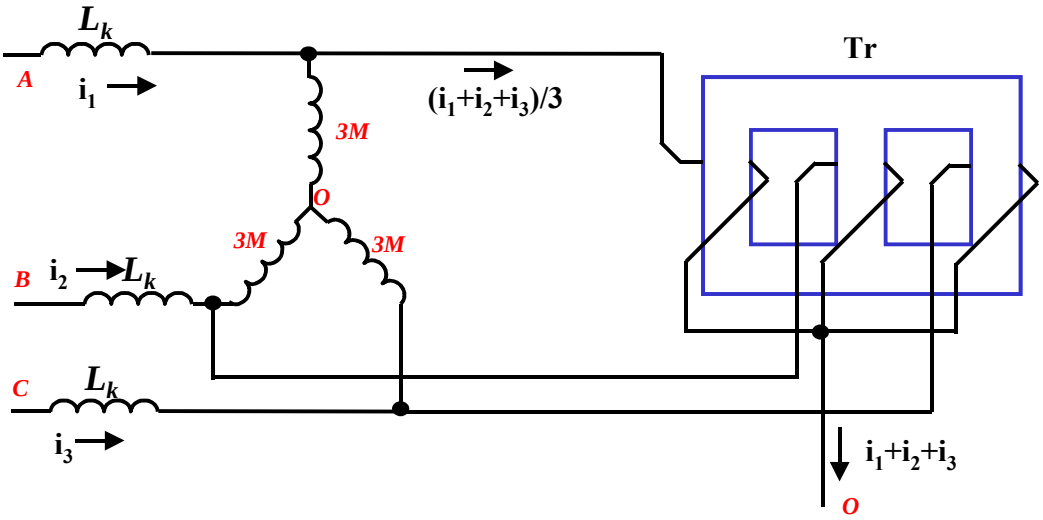


Figure 4.46 Equivalent circuit of three-phase coupling inductors with an ideal three-phase autotransformer

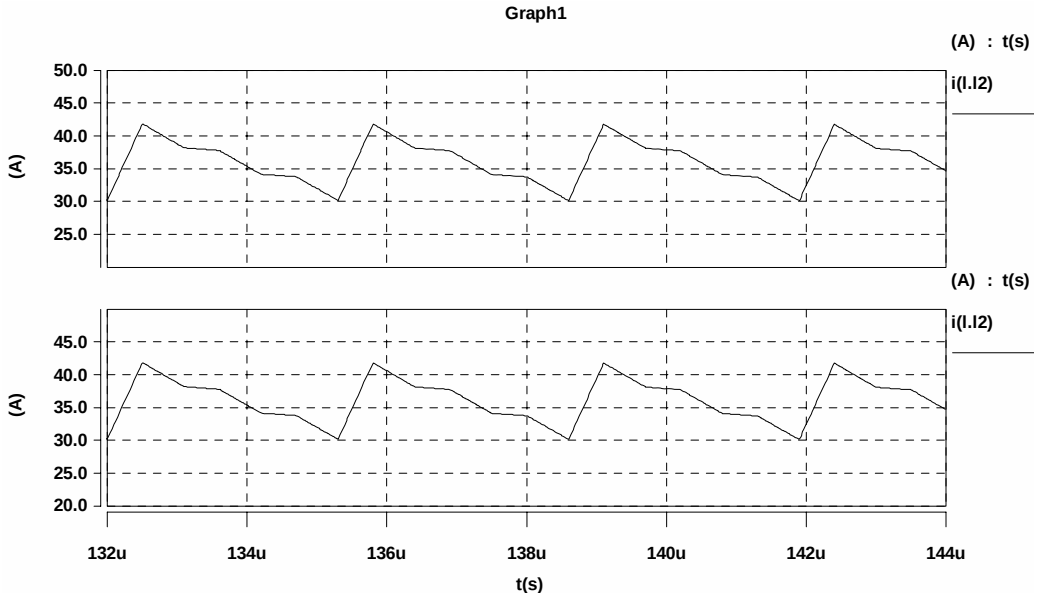


Figure 4.47 Equivalence verification of Figure 4.45 and Figure 4.46

4.4.2. Small-Signal Model for the Three-phase Buck Converter with Coupling Inductors

A three-phase buck with coupling inductors is shown in Figure 4.48. Its small-signal model is derived according to the same method we used to derive the two-phase converter model. Figure 4.49 shows the proposed model. Compared to Figure 4.31, Figure 4.49 has one more state variable, $\hat{i}_{m3}$. The three magnetizing currents, $\hat{i}_{m1}$, $\hat{i}_{m2}$, and $\hat{i}_{m3}$ interact among each other.

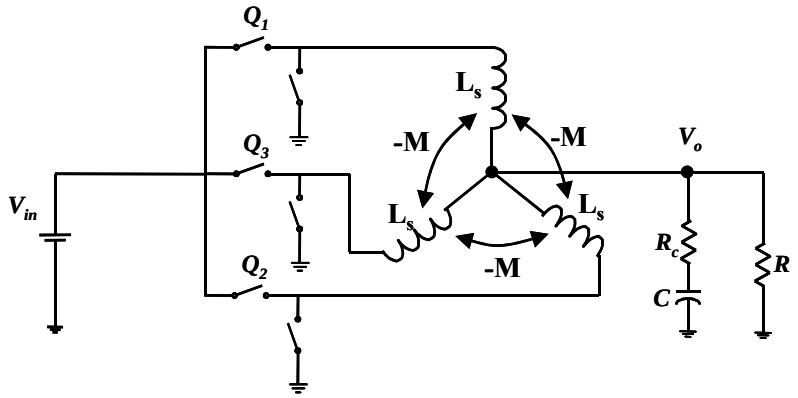


Figure 4.48 A three-phase buck converter with coupling inductors

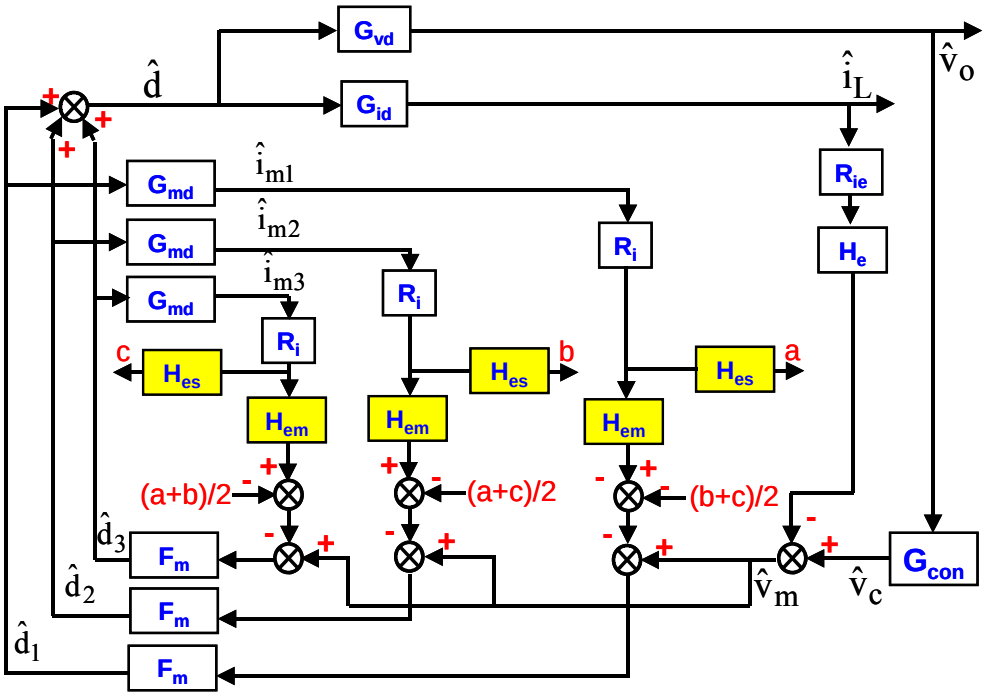


Figure 4.49 Small-signal model of a three-phase buck converter with coupling inductors

Table 4.5 lists all the transfer functions of the block diagram. In the table, $L=(L_s-2M)/3$. Please note that the model is derived based on one assumption: The three phases are symmetrical. According to Figure 4.49, the transfer function from $\hat{v}_m$ to $\hat{d}$ is:

$$G_m = \frac{3F_m}{1+F_m G_{md} R_i (H_{em} - H_{es})} \tag{4.61}$$

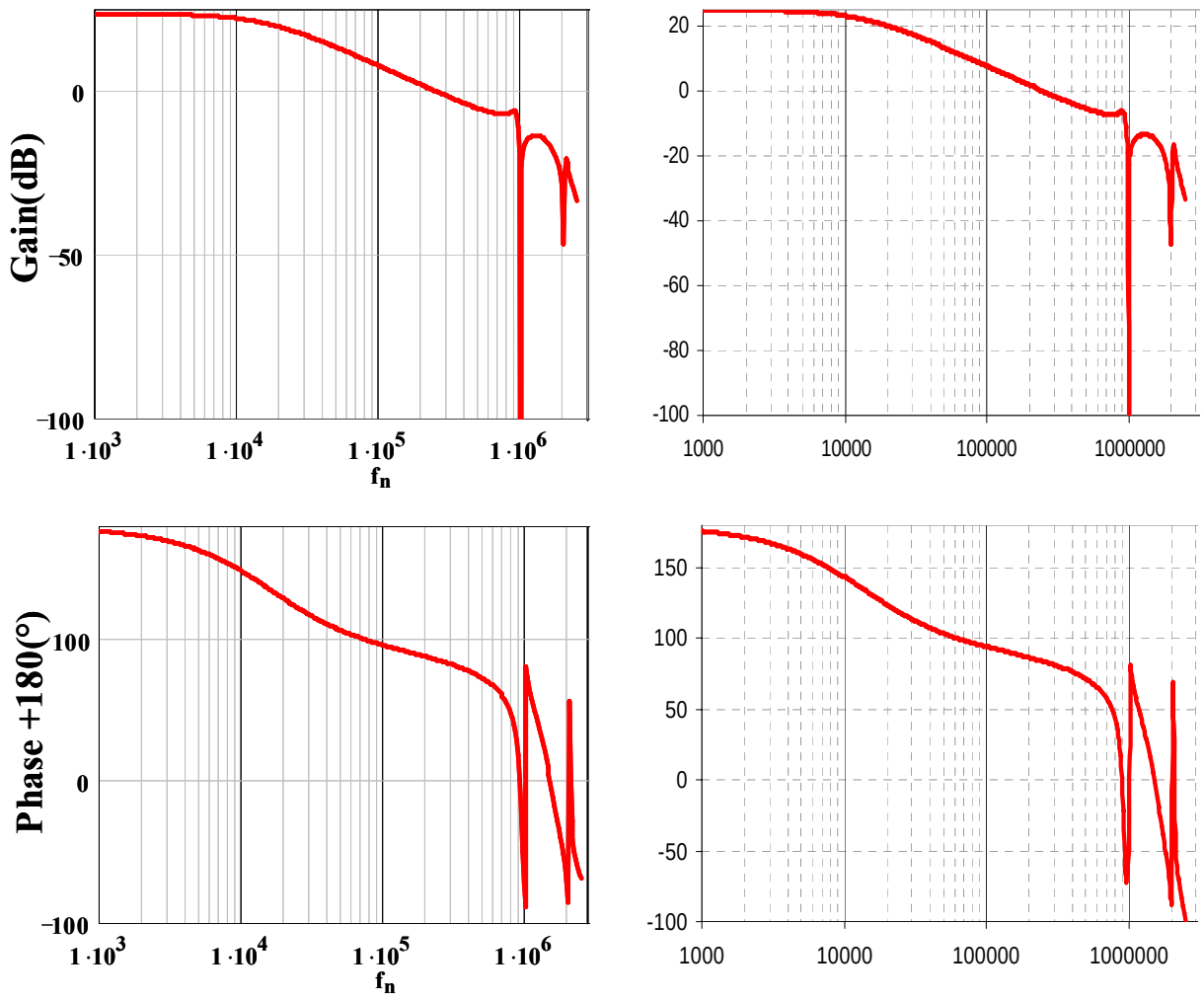
and the system loop gain T_2 with all the loops closed is:

$$T_2 = \frac{G_{vd} G_m G_{con}}{1+G_m G_{id} R_i H_e} \tag{4.62}$$

Table 4.5 Transfer functions of the three-phase model

G_{vd}	$\frac{\frac{V_{in}}{3}(R+sRR_cC)}{s^2LC(R+R_c)+s(L+RR_cC)+R}$	G_{md}	$\frac{V_{in}}{s(L_s+M)}$
G_{id}	$\frac{\frac{V_{in}}{3}(1+s(R+R_c)C)}{s^2LC(R+R_c)+s(L+RR_cC)+R}$	H_{em}	$\frac{sT_s}{e^{sT_s}-1}$
S_n	$\frac{\frac{V_{in}}{3}-V_o}{L_s-2M}R_i$	H_{es}	$\frac{sT_s/3}{e^{sT_s/3}-1}$
S_m	$\frac{V_{in}}{1.5(L_s+M)}R_i$	F_m	$\frac{1}{(S_n+S_m)T_s}$
R_{ie}	$R_i/3$	H_e	$\frac{sT_s/3}{e^{sT_s/3}-1}$

The verification of the three-phase model is done by the Simplis simulation. The parameters of the coupling inductors are: L_s=1.1uH, M=0.5uH. Figure 4.50 shows the T_2 gain and phase plots from the model, which is almost identical to the one from the Simplis simulation. The model proposed in this section provides a useful tool to evaluate the transient performance of a symmetrical three-phase coupling inductor. However, how to practically implement the inductor would be another research subject.



(a) (b)

Figure 4.50 The loop gain and phase plots from (a) the model (b) the Simplis simulation

4.4.3. Integration of Coupling Inductors and the Current-tripler Transformer

The three-phase coupling inductor structure shown in Figure 4.42 can be integrated with the current-tripler transformer when the transformer windings are rearranged. One can plug the three-phase coupling inductors shown in Figure 4.44 into the current-tripler converter to replace the three non-coupled inductors (Figure 4.51). The model derived previously is still applicable, except that V_{in} is now equal to V_{in}/n.

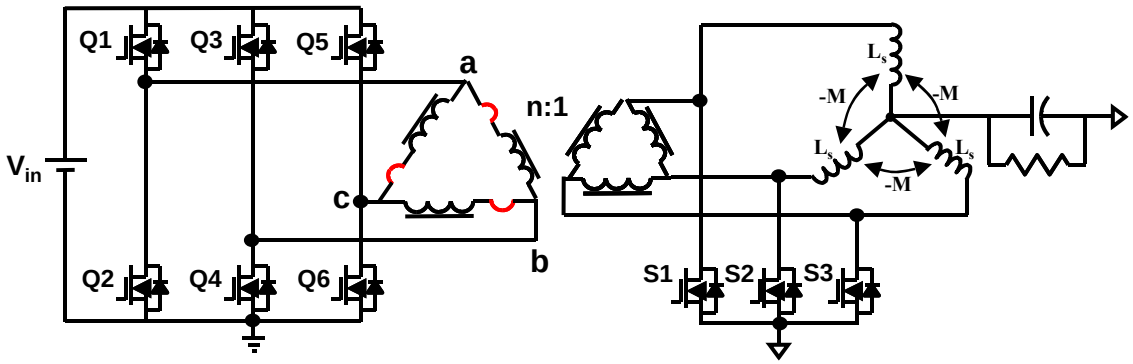


Figure 4.51 Current-tripler dc-dc converter with coupled inductors

In Figure 4.51, the current-tripler transformer and the coupled inductors are separate magnetic components, which increases the overall size and cost. In order to integrate the two magnetic components together, the transformer windings are changed from a delta connection to a Wye connection. The magnetizing inductors are utilized as the output inductors, which also have inverse coupling inductors M between each two windings. Figure 4.52 shows the proposed current-tripler DC-DC converter with integrated and coupled magnetic structure.

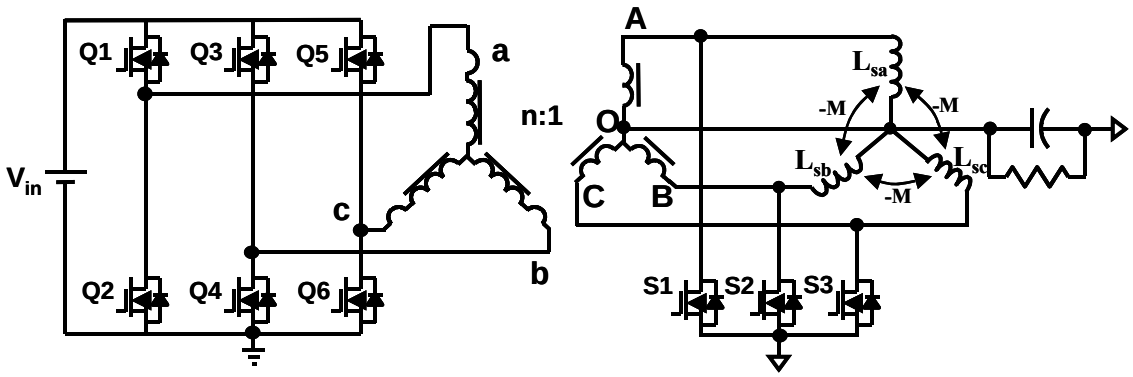


Figure 4.52 The proposed current-tripler DC-DC converter with integrated/coupled magnetics

In Figure 4.52, L_{sa}, L_{sb}, and L_{sc} represent the magnetizing inductors of winding AO, BO, and CO, respectively. The coupling among L_{sa}, L_{sb} and L_{sc} are represented by –M. The benefits of inverse coupling as discussed previously are maintained.

The physical implementation of the integrated magnetics with coupling inductors is illustrated in Figure 4.53. If one ignores the primary side windings, the implementation is exactly the same as that shown in Figure 4.42. The air gaps determine the secondary side magnetizing

inductances (L_{sa}, L_{sb}, L_{sc}) as well as the mutual inductances (M). The primary side winding of each phase is then wound around the same leg where the secondary side winding for that phase is placed.

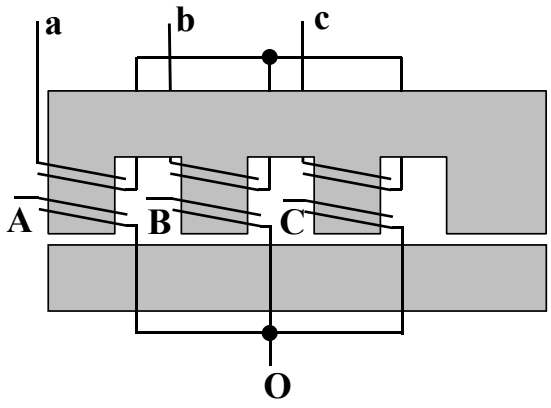


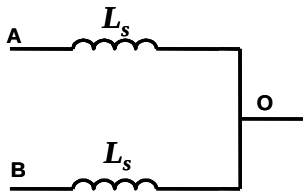
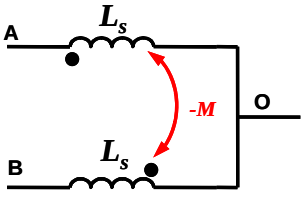
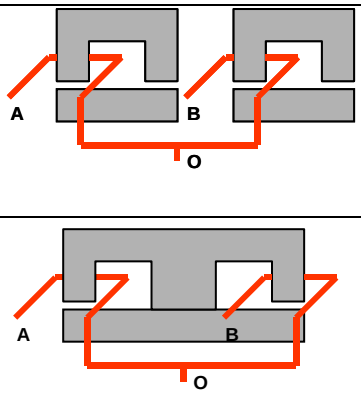
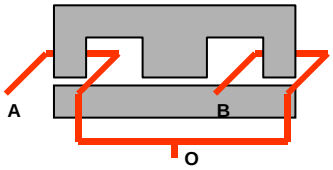
Figure 4.53 The physical implementation of the integrated/coupled magnetics

4.5. Summary of the Coupling Inductors and the Integrated Magnetics

In this chapter, different implementations of coupling inductors are studied. According to the proposed small-signal model, coupling inductors can attenuate the current loop sample hold effect at half the switching frequency. Therefore, higher bandwidth can be achieved without increasing the switching frequency.

Because the proposed VRM topologies all have a step-down transformer whether it is an isolated or non-isolated version, the coupled inductors can be integrated into the transformers. In summary, Table 4.6 to Table 4.9 list the different implementations of non-coupled and coupled inductors with or without transformers. Both the two- and three-phase inductors are included in the tables. The model proposed in this chapter is generally applicable to all of these implementations.

Table 4.6 Two-phase inductors

	Non-coupled L	Coupled L
Schematic		 (note1, 2)
Steady state L (per phase)	L_s	$\frac{L_s^2 - M^2}{L_s - \frac{D}{D'}M}$
Transient L (per phase)	L_s	L_s-M
Typical implemen-tations		

Note1: M is the absolute value of the mutual inductance, $0 \le M \le L_s$.

Note2: The center-tap coupling inductor is a special case in that $M=L_s$, therefore both the steady-state and transient inductors are zero. An additional inductor needs to be added for filtering purposes.

Table 4.7 Two-phase integrated magnetics with inductors and transformers

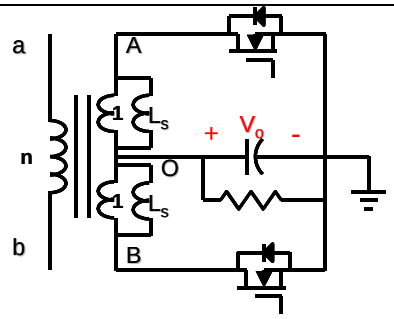
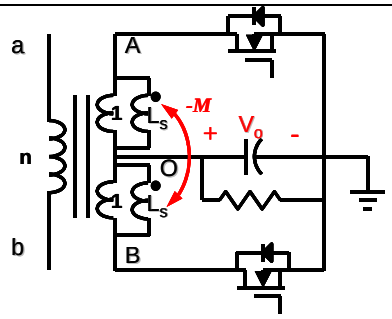
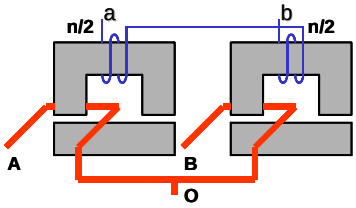
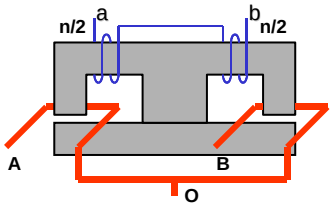
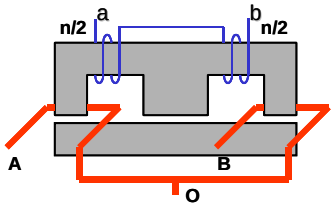
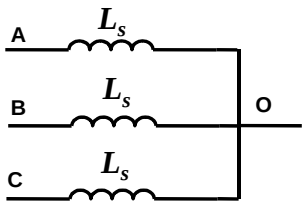
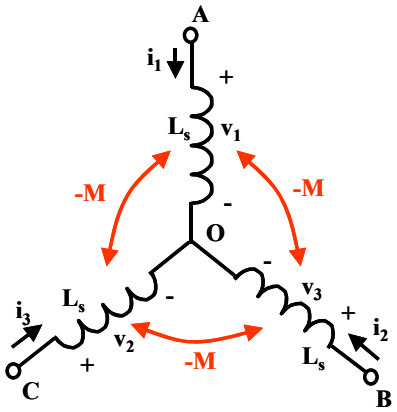
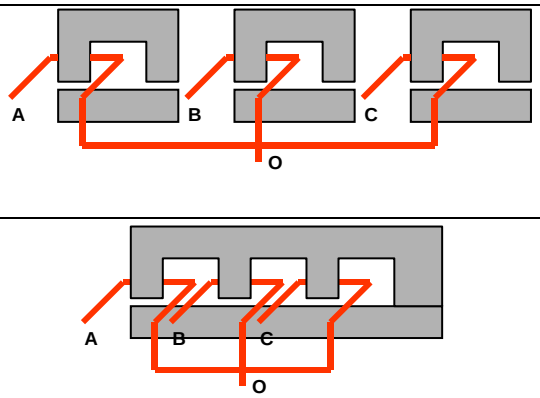
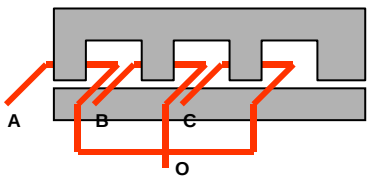
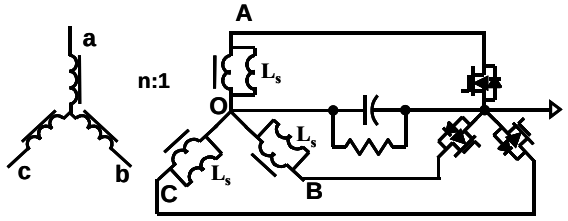
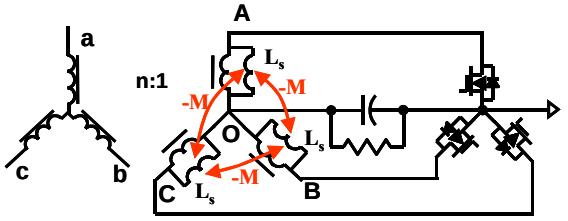
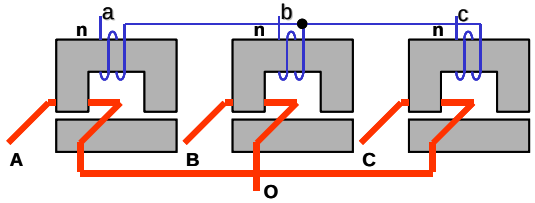
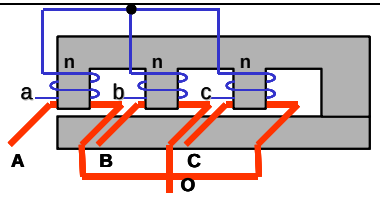
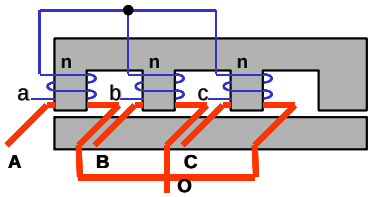
	Non-coupled L	Coupled L
Schematic		
Steady state L (per phase)	L_s	$\frac{L_s^2 - M^2}{L_s - \frac{D}{D'}M}$
Transient L (per phase)	L_s	L_s-M
Typical implementations	 	

Table 4.8 Three-phase inductors

	Inductors only	
	Non-coupled L	Coupled L
Schematic		 (note1)
Steady state L (per phase)	L_s	$\frac{(L_S+M)(L_S-2M)}{L_S-(1+2D/D')M}$
Transient L (per phase)	L_s	L_s-2M
Typical implemen-tations		

Note1: M is the absolute value of the mutual inductance, $0 \le M \le 0.5L_s$.

Table 4.9 Three-phase integrated magnetics with inductors and transformers

	Non-coupled L	Coupled L
Schematic		
Steady state L (per phase)	L_S	$\frac{(L_S+M)(L_S-2M)}{L_S-(1+2D/D')M}$
Transient L (per phase)	L_S	L_S-2M
Typical implementations	 	

Chapter 5. Conclusions and Future Work

The real challenges for a voltage regulator for the future microprocessors are dealing with fast transient, high current, and extremely low output voltage. If one follows today's approaches, a huge number of output decoupling capacitors are needed to keep the voltage within the specified window. Running the converter at a much higher frequency appears to be an ultimate solution to reducing the cost and size of those expensive capacitors. However, when the converter switching frequency increases, the switching-frequency-related power loss of the converter increases as well. Meanwhile, due to the increasing current demand, conduction losses also increase. All of this loss poses severe thermal problems to the VRM designers.

5.1. Summary

This dissertation is engaged in exploring the novel solutions for high-frequency, high-current VRMs. Starting from the 48V isolated DC-DC converter, a novel Complementary Controlled Bridge (CCB) self-driven concept is proposed to reduce all the switching-frequency-related losses. With the proposed self-driven scheme, the combination of the ZVS technique and self-driven technique recycles the gate driving energy by making use of the input capacitor of the secondary-side synchronous rectifier (SR) as the snubber capacitor of the primary-side switches. The proposed converter can save more driving loss and synchronous rectifier body diode conduction loss than the external driver. Additionally, compared with the existed level-shifted self-driven scheme for bridge-type symmetrical topologies, its gate signal ringing is small, and suitable for high-frequency applications.

Although the CCB self-driven VRM significantly reduces the switching-frequency-related losses, the conduction loss is still high. A novel ZVS current-tripler DC-DC converter is proposed to utilize more SR devices to share the current during the freewheeling period so that the SR conduction loss is reduced. The current-tripler DC-DC converter has a delta/delta-connected transformer that can be implemented with integrated magnetics. The transformer then becomes an integrated magnetic with distributed windings, which is preferable in high-current

applications. The current-tripler DC-DC converter in fact meets the requirements for CCB self-driven VRM. The two concepts are then combined with an integrated gate drive transformer.

For the 12V input non-isolated VRMs, one of the biggest issues is the extremely small duty cycle for a conventional buck converter. By adding a step-down transformer, not only is the duty cycle extended, but the proposed CCB self-driven concept can be extended as well. The proposed topology is basically a buck-derived soft-switching topology with duty-cycle extension and SR device self-driven capabilities. Because there is no isolation requirement, the SR gate driving becomes so simple that the voltage at the complementary controlled bridge can be used to drive the SR gate. Both the gate driving loss and the SR body-diode conduction loss are reduced.

The addition of the step-down transformer adds additional winding loss and cost to the circuit. An autotransformer version of the circuit is proposed, mainly to deal with the transformer winding loss. Moreover, by integrating the output filter inductors with the transformer, the total magnetic components count stays the same as the conventional multiphase buck converters.

The proposed current-tripler DC-DC converter can also be extended to the 12V non-isolated VRMs. The derivation from the isolated current-tripler to the non-isolated current-tripler is discussed. There are two ways to drive its synchronous rectifiers. The first method is to drive externally, which is simple to implement but dissipative. The other method is to use the CCB self-driven scheme. In order to meet the requirements of CCB self-driven method, we have to modify the non-isolated current-tripler to an autotransformer version. The SR driver loss is less than the first method, but an additional level shift circuit is needed in the driving path, which somewhat increases the circuit complexity.

All the circuits proposed previously have one feature in common: their output inductors are equivalent to those in buck converters (either two or three phases). The use of integrated coupling inductors between the interleaving channels of a buck converter can improve both the steady-state efficiency and dynamic performances. The essence of the coupling inductors concept is to provide different equivalent inductances for the steady state and the transient. More benefits are discovered when a current loop becomes a mandatory function to achieve Adaptive Voltage Positioning (AVP) as well as proper current sharing among phases. The current loop sample hold effect is alleviated by the coupling L concept. A small-signal model is proposed to

study the system dynamic performance difference with different coupling inductor designs. As verification, the coupling concept is applied to the 12V non-isolated CCB self-driven VRM and bandwidth as high as one third of the switching frequency is achieved, which indicates a significant output capacitor reduction.

In conclusion, this dissertation proposes a variety of new topologies for both 12V and 48V voltage regulators. All of them can share the following three concepts:

1. Complementary controlled bridge self-driven VR;
2. Current-tripler;
3. Multiphase-coupling inductors.

Throughout the entire dissertation, these three concepts are interconnected to deliver the most advanced topologies for future high frequency high current VRMs.

5.2. Future Work

In accordance with the model derived in Chapter 4, the coupling inductors can help to boost the control bandwidth. The concept was demonstrated in the proposed 12V self-driven VRM at a relatively low switching frequency (700kHz) with a 245kHz control bandwidth. At this bandwidth, there are still quite a few bulk capacitors and cavity capacitors needed.

According to the research work done by others [19], a 650kHz bandwidth can give us the elimination of the bulk capacitors and a significant reduction of the cavity capacitor (from 230 to 50). To achieve this goal, there are several technical challenges:

1. A 2MHz or higher switching frequency converter is needed, which is beyond the capability of the proposed CCB self-driven VR topologies.
2. The impact from the controller and driver delays, the error amplifier bandwidth etc, needs to be analyzed.
3. A novel integrated coupling inductor design is necessary to minimize both the core loss and the winding conduction loss. For multiphase coupling, the asymmetry issue has to be addressed in order to get better performance.

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