

# SiGe BiCMOS RF ICs and Components for High Speed Wireless Data Networks

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(ABSTRACT)

**T**HE advent of high- $f_T$  silicon CMOS/BiCMOS technologies has led to a dramatic upsurge in the research and development of radio and microwave frequency integrated circuits (ICs) in silicon. The integration of silicon-germanium heterojunction bipolar transistors (SiGe HBTs) into established “digital” CMOS processes has provided analog performance in silicon that is not only competitive with III-V compound-semiconductor technologies, but is also potentially lower in cost. Combined with improvements in silicon on-chip passives, such as high- $Q$  metal-insulator-metal (MIM) capacitors and monolithic spiral inductors, these advanced RF CMOS and SiGe BiCMOS technologies have enabled complete silicon-based RF integrated circuit (RFIC) solutions for emerging wireless communication standards; indeed, both the analog and digital functionalities of an entire wireless system can now be combined in a single IC, also known as a wireless “system-on-a-chip” (SoC). This approach offers a number of potential benefits over multi-chip solutions, such as reductions of parasitics, size, power consumption, and bill-of-materials; however, a number of critical challenges must be considered in the integration of such SoC solutions.

The focus of this research is the application of SiGe BiCMOS technology to ongoing challenges in the development of receiver components for high speed wireless data networks. The research seeks to drive SoC integration by investigating circuit topologies that eliminate the need for off-chip components and are amenable to complete on-chip integration. The first part of this dissertation presents the design, fabrication, and measurement of a 5–6 GHz sub-harmonic direct-conversion-receiver (DCR) front-end, implemented in the IBM 0.5  $\mu\text{m}$  5HP SiGe BiCMOS process. The design consists of a fully-differential low-noise amplifier (LNA), a set of quadrature (I and Q)  $\times 2$  sub-harmonic mixers, and an LO conditioning chain. The front-end design provides a means to address performance limitations of the DCR architecture (such as DC-offsets, second-order distortion, and quadrature phase and amplitude

imbalances) while enabling the investigation of high-frequency IC design complications, such as package parasitics and limited on-chip isolation. The receiver front-end has a measured conversion gain of  $\sim 18$  dB, an input second-order intercept point of  $+17.5$  dBm, and a noise figure of 7.2 dB. The quadrature phase balance at the sub-harmonic mixer IF outputs was measured in the presence of digital switching noise;  $90^\circ$  balance was achieved, over a specific range of LO power levels, with a square wave noise signal injected onto the mixer DC supply rails.

The susceptibility of receiver I/Q balance to mixed-signal effects in a SoC environment motivates the second part of this dissertation — the design of a phase and amplitude tunable, quadrature voltage-controlled oscillator (QVCO) for the on-chip synthesis of quadrature signals. The QVCO design, implemented in the Freescale (formerly Motorola)  $0.18\ \mu\text{m}$  SiGe:C RFBiCMOS process, uses two identical, differential  $LC$ -tank VCOs connected such that the two oscillator outputs lock in quadrature to the same frequency. The QVCO designs proposed in this work provide the additional feature of phase-tunability, i.e. the relative phase balance between the quadrature outputs can be adjusted dynamically, offering a simulated tuning range of  $\sim 90^\circ \pm 10^\circ$ ; in addition, a variable-gain buffer/amplifier circuit that provides amplitude tunability is introduced. One potential application of the QVCO is in a self-correcting RF receiver architecture, which, using the phase and amplitude tunability of the QVCO, could dynamically adjust the IF output quadrature phase and amplitude balance, in near real-time, in the analog-domain.

The need for high-quality inductors in both the DCR and QVCO designs motivates the third aspect of this dissertation — the characterization and modeling of on-chip spiral inductors with patterned ground shields, which are placed between the inductor coil and the underlying substrate in order to improve the inductor quality factor ( $Q$ ). The shield prevents the coupling of energy away from the inductor spiral to the typically lossy Si substrate, while the patterning disrupts the flow of induced image currents within the shield. The experimental effort includes the fabrication and testing of a range of inductors with different values, and different types of patterned ground shields in different materials. Two-port measurements show a  $\sim 50\%$  improvement in peak- $Q$  and a  $\sim 20\%$  degradation in self-resonant frequency for inductors with shields. From the measured results, a scalable lumped element model is developed for the rapid simulation of spiral inductors with and without patterned ground shields.

The knowledge gained from this work can be combined and applied to a range of future RF/wireless SoC applications. The designs developed in this dissertation can be ported to other technologies (e.g. RF CMOS) and scaled to other frequency ranges (e.g. 24 GHz ISM band) to provide solutions for emerging applications that require low-cost, low-power RF/microwave circuit implementations.

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# Chapter 1

## Introduction

**A**S the availability of wireless technologies continues to explode, the vision of ubiquitous, untethered communication systems is becoming a reality. Mobile phones, now nearly universal, are emerging as more than just a means of voice communication, incorporating capabilities such as GPS or Bluetooth and providing an interface to high-speed data networks. Wireless local area networks (WLAN), growing in popularity, have advanced from virtually no users in 2000 to roughly 39 million by the end of 2004 [1], [2]. Furthermore, next-generation wireless technologies, such as 4G, wireless broadband access (IEEE 802.16), and ultra-wideband (UWB, a subset of IEEE 802.15), are being pursued to provide “always-on” wireless, high-speed data connections.

A number of important technological developments have enabled this rapid deployment of wireless high-speed networks, with some of the most significant advances occurring in the area of silicon (Si) integrated circuits (ICs). Over the last several decades, the mass production of digital ICs (such as microprocessors and memory chips) using Si processes has driven the majority of semiconductor manufacturers to focus on improving the performance of Si technology. In particular, Si complementary metal-oxide semiconductor (CMOS) technology, which has been employed extensively for digital circuitry, has evolved quickly into a technology capable of low-power operation, high levels of integration, and considerable design flexibility. Yet, despite this evolution, and the dominance of Si within the global semiconductor market in general, the use of Si technology for high-frequency systems, such as the radio frequency

(RF) transceivers required for high-speed wireless data networks, is relatively new.

The path to Si dominance in semiconductor manufacturing can be traced back to a number of advantages Si offers over other semiconductor materials [3]:

- The ability to grow large, nearly defect-free single-crystal wafers, yielding dramatic economies of scale;
- The ability to grow a high-quality dielectric for isolation and passivation (i.e. silicon dioxide,  $\text{SiO}_2$  on such wafers) simply through thermal oxidation;
- Superior thermal conductivity for the removal of dissipated heat;
- Controlled doping with both n- and p-type impurities over a wide dynamic range, at moderate incorporation temperatures;
- The tremendous abundance of the element on Earth.

Nevertheless, for high frequency circuit design, silicon is not necessarily the optimal semiconductor technology. In Si, the electron and hole carrier mobilities are relatively low under active bias [3]<sup>1</sup>. The typically low resistivity of Si substrates ( $1\text{--}20\ \Omega \cdot \text{cm}$ ) degrades the quality factors of passive components and lowers the inter-circuit signal isolation at higher frequencies [5]<sup>2</sup>. Additionally, the low breakdown voltage of silicon devices limits their use in power amplifiers (PAs) — an essential component in wireless transmitters — while the indirect bandgap of Si makes light emissions difficult and optical devices, such as diode lasers, impractical. Thus, alternative, more exotic, semiconductor technologies have historically met the performance demands for high frequency applications, in particular radio frequency ICs (RFICs) and monolithic microwave ICs (MMICs) for wireless communications, and optoelectronic ICs (OEICs) for optical communications.

---

<sup>1</sup>However, carrier mobilities in all semiconductor materials reach a maximum, saturated velocity on the order of  $10^7$  cm/sec under high electric fields [4]. This fact is sometimes overlooked when comparing silicon to other materials because high electric fields are not typically present in long channel devices. However, as the continued scaling of transistor dimensions has led to smaller devices, the electric field acting on the carriers has intensified. At currently used dimensions, the electric field strength is high enough to cause carriers to achieve the saturated velocity. Thus the advertised stark difference in carrier mobilities between silicon and other materials is becoming less of an issue.

<sup>2</sup>While high resistivity Si substrates can be formed, they are more expensive and can lead to latch-up concerns for digital circuitry.

Prior to the late 1990s, these high frequency ICs were fabricated using compound semiconductor materials composed of elements from the third (III) and fifth (V) columns of the periodic table (III-V semiconductors), such as gallium arsenide (GaAs) and indium phosphide (InP). At lower electric fields, these materials have significantly higher mobilities than Si. III-V materials also exhibit much higher breakdown voltages than Si (a critical parameter in power amplifier design) and their direct bandgap structure makes III-V semiconductors well-suited for optoelectronic devices [3]. GaAs, InP, etc. can be grown easily in semi-insulating form, which is advantageous for integrated passive components. However, these benefits come with drawbacks in the manufacturing of low-cost ICs. For instance, a high-quality dielectric (like silicon dioxide) cannot be grown as easily on III-V substrates as it can on Si substrates. Furthermore, III-V wafers are typically smaller, fragile, and difficult to grow with a low defect density. III-V materials also typically exhibit poor heat conduction. These inadequacies ultimately lead to lower levels of integration, more difficult fabrication, lower yield, and, as a result, overall higher costs [6].

Research and development over the last 30 years has focused on creating higher speed silicon devices for digital applications. For example, the International Technology Roadmap for Semiconductors (ITRS), a document developed by leaders in the semiconductor industry to assess present and future semiconductor technology requirements (historically with an emphasis on CMOS), projects that the need for high-speed, high-density *digital* circuits will continue to drive the development of new technology generations to occur roughly every three years. By convention, these technology generations, or nodes, are defined by the minimum metal-to-metal spacing in dynamic random access memory (DRAM) [7]; however, for analog IC design, the minimum feature-size, or physical gate-length, of a CMOS transistor is a more meaningful indicator. Thus, the ITRS node designation of 90 nm (0.090  $\mu\text{m}$ ) for the current generation of technology corresponds to devices with a minimum physical gate-length of 37 nm; similarly, the 22 nm (0.022  $\mu\text{m}$ ) technology node projected for 2016 corresponds to gate-lengths of 9 nm [8]. A by-product of this aggressive scaling is the need for thinner gate oxides, which are required to maintain the charge density within the channel of MOS devices. These thinner gate oxides have lower breakdown voltages and thus require that the supply voltage also be scaled with the devices at each technology node. The lower supply voltages can have a negative impact on analog applications, where the reduced voltage headroom can limit circuit topology

or AC signal swings. Nonetheless, the continued downward scaling of device size and supply voltage has led to the support of gigahertz operation, ultra-high levels of integration, and reduced device power consumption. These advances, along with significant improvements in integrated passive components (resistors, capacitors, and inductors) on Si substrates, have spurred an upsurge in the research and development of radio and microwave frequency integrated circuits in silicon [9].

The successful introduction of new wireless devices and technologies in the commercial marketplace is dependent on the ability of manufacturers to provide low-cost, low-power, highly-integrated, multi-functional solutions. With that in mind, the remainder of this chapter introduces basic concepts underlying the motivation for this work. An overview of “system on a chip” integration — the combination of various functional blocks of an entire system onto a single IC — is discussed from the RF point of view. Next, integrated circuit technologies are briefly introduced, including CMOS, III-V heterojunction bipolar transistors (HBTs), and the newest technology advance, CMOS-compatible silicon germanium (SiGe) HBTs. Using SiGe technology, with a vision for a fully-integrated, system on a chip, wireless transceiver, the remainder of the chapter offers a discussion of the tradeoffs between different receiver architectures, with particular attention on the direct-conversion architecture and its suitability for SoC integration. The chapter concludes with an overview of the research that is the focus of this dissertation.

## 1.1 Wireless System on a Chip

The diverse performance requirements in wireless receiver and transmitter building blocks has historically dictated the use of different semiconductor technologies for different components, such as CMOS for digital processors and memory, GaAs for power amplifiers, and SiGe for low-noise amplifiers and mixers. A primary example of this is the modern digital cellular phone, where three or four separate integrated circuits, fabricated in different technologies, are employed to meet the stringent performance specifications of contemporary cellular systems, such as the Global System for Mobile Communications (GSM) or code division multiple access (CDMA). However, the demand for higher levels of integration and increased functionality, and the need for multi-mode, multi-band products (for inter-operability between differ-

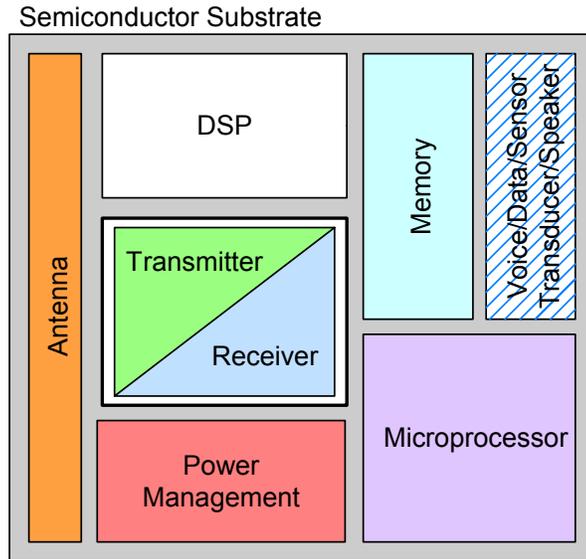


Figure 1.1: Simplified block diagram of a generic, SoC-integrated, electronic device.

ent wireless standards and services) is pushing forward new approaches in complex communications and networking systems.

One proposed solution for improving performance, while lowering overall costs, is to eliminate all external components and integrate a complete wireless system — including all analog and digital functions — onto a single, mixed-signal IC, an approach known as “system on a chip” (SoC) integration [10–12]. Figure 1.1 shows a conceptual block diagram of such a single-chip design — from the antenna and RF transceiver to the microprocessor and baseband input/output, all components are integrated in a single semiconductor technology on a common substrate.

Focusing on just one part of the entire system shown in Figure 1.1, Figure 1.2 shows the block diagram of a generic RF transceiver (transmitter and receiver) categorized by integrated circuit technology and circuit type (RF, analog, or digital). While the digital components are implemented in Si CMOS, the RF sections of the receiver and transmitter, along with the frequency synthesizer, can be realized with different technology options. The optimum choice of semiconductor technology is a complicated issue, involving performance, wafer cost, level of integration, and time-to-market [9]. Although the use of multiple technologies is ultimately not cost effective, it has traditionally been necessary to meet the stringent performance standards of wireless

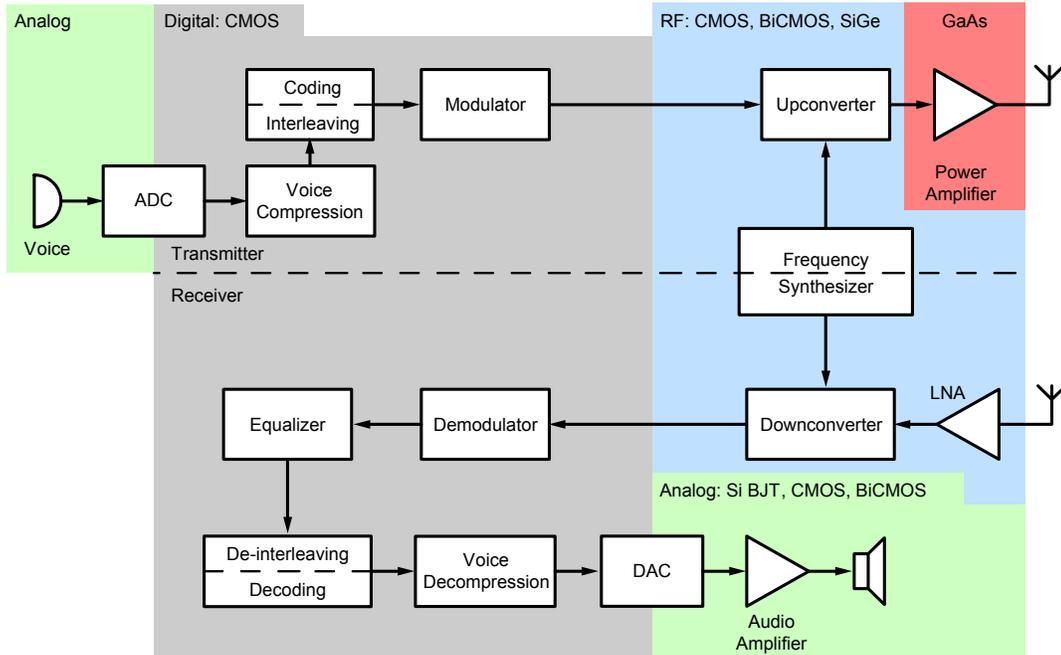


Figure 1.2: Block diagram of a generic digital wireless transceiver, i.e. the “Transmitter/Receiver” block from Figure 1.1. Blocks are categorized by circuit type and process (after [13]).

communication systems. In contrast, “system on a chip” (SoC) integration offers the possibility of a low-cost, low-power, single-chip solution where all the functions of a wireless communication system are fully integrated in a single technology on a single IC.

One of the biggest drivers for SoC integration has been the mobile phone. The merging of the “cell phone” and the personal digital assistant (PDA), along with the desire for pervasive, high-speed connections to the Internet, is currently driving the commercial marketplace [14]. Yet, to maintain a constant pace of improving cost and performance, more than simple transistor scaling is required; rather, computation and digital signal processing and analog functionality must be married into an integrated, mixed-signal system [15]. By incorporating multiple diverse functions on the same chip, a mixed-signal system offers a number of important advantages [5]:

- packaging and handling costs are reduced because fewer separate circuits are required;

- reactive parasitics associated with packaging are reduced since all circuits are integrated on the same chip;
- overall size of the system is reduced;
- overall power consumption can be reduced;
- digital techniques for filtering, frequency synthesis, and control systems can be seamlessly used with analog techniques for frequency conversion and signal amplification.

Still, a number of unique challenges must be overcome before a true single-chip solution is commercially viable. For instance, the substrate of the IC has a significant impact on the performance of an RF-SoC. For Si CMOS-based technologies, the relatively conductive substrate typically employed in commercially available processes can couple undesired spurious signals into the sensitive receiver front-end and corrupt signal reception. Likewise, switching noise from high-speed *digital* circuitry can leak through the substrate into the *RF/analog* receiver front-end in the mixed-signal environment. The conductive substrate also hampers the formation of high-quality on-chip passive components, which are required to meet the high-frequency performance specifications of wireless systems. Integration issues, such as the off-chip filters (e.g. SAW filters) used for image rejection in heterodyne receivers, motivate the exploration of alternative receiver architectures [16]. Therefore, SoC integration is being attacked by a combination of approaches that address these limitations:

- Using CMOS technology so that both digital and RF circuitry can be fabricated together at extremely low-costs.
- Substituting advanced semiconductor processes when CMOS alone cannot meet the required performance of a given system. In particular, technologies that offer excellent RF capabilities while maintaining compatibility with high-speed CMOS digital technology, like SiGe BiCMOS<sup>3</sup>, are of interest. Such technologies avoid the high frequency performance limitations of CMOS-only solutions, such as low sensitivity, low transconductance, and large mismatch voltages, but still provide CMOS for digital sub-circuits.

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<sup>3</sup>The term BiCMOS refers to the integration of both bipolar and CMOS devices in the same process.

- The judicious use of “guard rings” to increase substrate isolation around sensitive circuitry [17–19].
- The application of transceiver architectures that are more amenable to monolithic integration, such as direct-conversion or low-IF, which circumvent the need for multiple, highly-selective bandpass filters and thereby reduce the total number of off-chip components [20].

With regard to this last point, an alternative approach to such analog receiver-architectures is digital downconversion (also known as bandpass sampling [21]). With this technique, the modulated RF signal is under-sampled to alias (or essentially copy) the desired spectrum directly down to baseband for subsequent digital signal processing [22]. The main benefit of this approach is that a larger portion of the receive chain (starting with the downconverter shown in Figure 1.2) is implemented using digital hardware, potentially enabling software-defined radios [23]. Sub-sampling also exhibits extremely high linearity in comparison with analog-based counterparts [24]. However, since modern analog-to-digital converters (ADCs) suitable for wireless communications systems have limited analog input bandwidths (approximately a few hundred megahertz), this approach cannot be used for high-speed data networks, such as IEEE 802.11a WLAN [25]. Furthermore, since all energy from DC to the bandwidth of the ADC is aliased together into the baseband signal, the noise performance of sub-sampling architectures is significantly worse than that of typical analog approaches [13, 25, 26]. Therefore, sub-sampling is not amenable for the objectives of this research to be discussed in Section 1.4.

## 1.2 Silicon Technologies

As discussed above, Si CMOS technologies have become the de facto choice for digital and low-frequency analog circuit manufacturing. However, the requirements for RF circuits include more than just high-speed devices. A technology suitable for RFICs must also offer low noise transistors capable of gain, high linearity, and output power; high-quality RF passives (inductors and capacitors); and accurate device models. Until recently, these demands received little attention in the development of advanced CMOS technologies. Motivated by the emerging wireless market though, the 2003

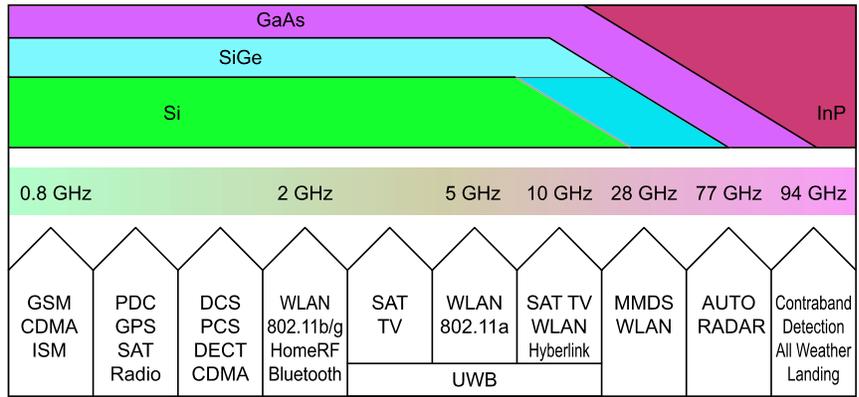


Figure 1.3: Approximate semiconductor technology breakdown vs. application spectrum (after [7]).

ITRS updated its list of economic drivers for technological development and now include these new market forces. System drivers for technology advancement are presently divided into four main categories: microprocessors, embedded memory, *SoC*, and *RF and analog/mixed-signal (AMS)*. The last two drivers are directly targeted by this work.

Established silicon fabrication facilities can produce integrated circuits at relatively low costs in massive quantities. From an economic standpoint, extending a silicon-based process to facilitate high frequency circuits is very attractive. Furthermore, directly integrating high frequency analog circuits alongside high-speed digital components offers exciting possibilities, as discussed in Section 1.1. Therefore, methods to extend the capabilities of Si to the high frequency regime, in direct competition with III-V materials, have been sought.

Figure 1.3 shows the RF/microwave/millimeter-wave frequency spectrum divided by application with an approximate breakdown of the relevant semiconductor technologies. Recent advances in CMOS technology, specifically so-called “RF CMOS,” have pushed the applicable region of Si of Figure 1.3 further to the right. Today, Si CMOS technology dominates at frequencies below 10 GHz and active research is focused on circuit applications in the 28 and 60 GHz bands; similarly, advances in SiGe have pushed its application to frequencies further to the right, encroaching on the range once dominated solely by III-V technologies such as GaAs.

This section begins with a brief introduction to bandgap engineering in compound semiconductor HBTs. The concept of bandgap engineering is then extended to Group IV semiconductors, where, using silicon-germanium ( $\text{Si}_{1-x}\text{Ge}_x$  or simply SiGe) alloys, SiGe HBTs can be realized and the RF/analog characteristics of silicon can be enhanced. The section ends with an overview of two SiGe commercially available processes employed in this work.

### 1.2.1 The Conventional Wide Bandgap Emitter HBT

A heterojunction is defined as a  $p$ - $n$  junction where the  $p$ - and  $n$ -materials have different energy band gaps. This structure is in contrast to the traditional homojunction structure where both sides of the  $p$ - $n$  junction are composed of the same material with a constant bandgap across the junction. Despite the difference, the conventional heterojunction bipolar transistor is similar to its homojunction counterpart in that device operation is determined by the flow of carriers through the base region. However, the heterojunction offers the ability to “bandgap engineer” the device such that the flow of electrons and holes can be controlled independently. For the conventional HBT, this control is achieved by using a wide-bandgap material for the emitter as compared to the base; the resulting structure allows for an improved flow of electrons into the base while simultaneously restricting the flow of holes back into the emitter [27]. The wide-bandgap emitter has a number of advantages, particularly over traditional homojunction devices:

- lower base resistance as a result of higher base doping;
- higher Early voltage due to higher base doping, which results in a smaller device output conductance (higher output resistance);
- lower emitter-base junction capacitance since emitter doping can be lowered;
- higher-speed devices, since the distances that govern carrier transport, and hence device speed, are established through vertical epitaxial growth, not lateral lithography.

The advantages of the bandgap-engineered emitter can be explained with a simplified energy band diagram for a conventional  $N$ - $p$ - $n$  HBT (where the capital N denotes the

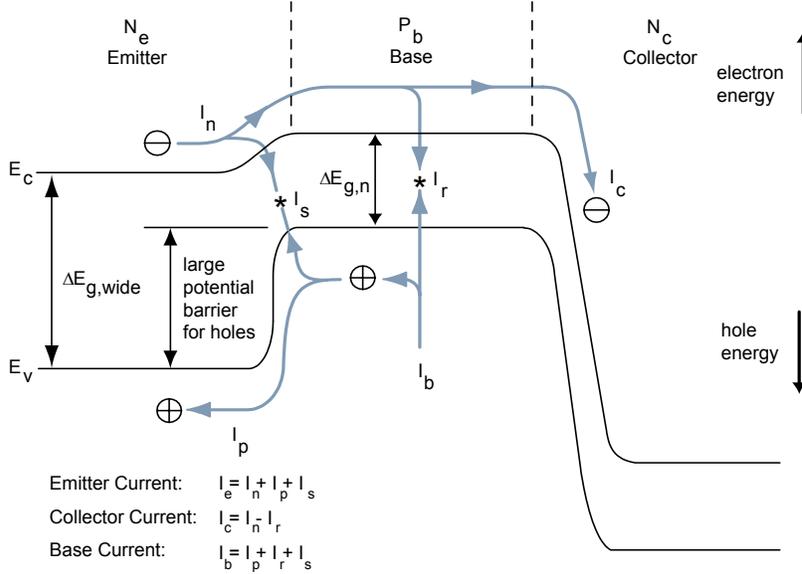


Figure 1.4: Simplified band diagram for a conventional HBT (after [28]).

wide bandgap emitter), as shown in Figure 1.4. Under active bias, the wide-bandgap emitter generates a large valence band discontinuity at the emitter-base junction, which presents a significant potential barrier for holes originating in the base to diffuse into the emitter. The diffusion of carriers from base to emitter is known as back-injection. As discussed in more detail below, the reduction of *hole* back-injection (for the case of  $N$ - $p$ - $n$  devices) enables most of the performance improvements associated with HBTs.

The operation of an HBT is determined by the flow of several different currents within the device, including: the current from electrons injected from the emitter into the base,  $I_n$ ; the current from injected electrons within the base flowing into the collector,  $I_c$ ; and the base current  $I_b$ , which is the sum of the hole current due to back-injection,  $I_p$ , and the two recombination currents,  $I_s$  and  $I_r$ .  $I_s$  is the current induced by electron-hole recombination at the emitter-base interface, and  $I_r$  is the current due to electron-hole bulk recombination in the base [27].

The emitter injection efficiency ( $\gamma$ ) is the fraction of total emitter current injected into the base region that contributes to the collector current  $I_c$ .  $\gamma$  is defined as:

$$\gamma = \frac{I_n}{I_e} = \frac{I_n}{I_n + I_p + I_s} \quad (1.1)$$

and is ideally equal to 1. With the wider bandgap emitter, the hole back-injection current,  $I_p$ , is reduced because of the large potential barrier against holes entering from the base into the emitter. The reduction in  $I_p$  means that fewer holes are present in the emitter-base space-charge layer, which correspondingly reduces the recombination current  $I_s$ . With less recombination at the emitter-base interface, the electron current  $I_n$  increases, which in turn increases the collector current  $I_c$ . Therefore, the increase in  $I_n$  and the decrease in  $I_p$  and  $I_s$  enable near-unity values of  $\gamma$ . Furthermore, the reduction in  $I_p$  and  $I_s$  lowers the overall base current  $I_b$ , resulting in a higher current gain,  $\beta$ , given by:

$$\beta = \frac{I_c}{I_b}. \quad (1.2)$$

Values of  $\gamma$  approaching 1 allow for emitter and base doping levels to be somewhat arbitrary, set by the required performance metrics of the device — such as speed, frequency response, and base resistance — and relatively free from the constraints of emitter injection efficiency [29]. In contrast, the *emitter* of a homojunction device must be heavily doped to increase electron flow from the emitter to the base and to keep  $\gamma$  at a reasonable level. Reasonable  $\gamma$  values also require that the doping levels of a homojunction base be kept relatively low to prevent large recombination currents that also detract from  $I_n$ . However, the lower base doping levels result in a greater series input resistance as seen looking into the base. This large series base resistance, denoted as  $r_b$ , has detrimental effects on the frequency response and noise performance of the device. For an HBT though, the high injection efficiency allows for nearly independent doping of the emitter and base. Thus, the doping level of the base can be increased so as to reduce  $r_b$  while the parasitic base-emitter capacitance,  $C_{be}$ , can be reduced by lowering the emitter doping level below that of the base, given that the parasitic capacitance of an asymmetrically doped  $p$ - $n$  junction depends on the doping level of the less heavily doped side [29]. The reductions of  $C_{be}$  and  $r_b$  provide significant improvements in device-speed and noise performance.

The frequency performance of a transistor is typically characterized by two figures of merit, which indicate how fast a device can operate [30]. The small signal unity-gain cut-off frequency, otherwise known as the transit frequency, or  $f_T$ , is the frequency at which the short-circuit AC current gain is equal to 1. Using hybrid-parameter

notation, the AC current gain is given by:

$$h_{21} = h_{fe} = \left. \frac{i_c}{i_b} \right|_{v_c=0} \quad (1.3)$$

where  $i_c$  and  $i_b$  are AC currents and  $v_c$  is the collector voltage. The value of  $f_T$  is found by plotting the magnitude of  $h_{fe}$  versus frequency and noting the frequency at which  $|h_{fe}| = 1$ . An approximate value of  $f_T$  for a device can be found as:

$$f_T \approx \frac{g_m}{2\pi(C_{be} + C_{bc})} \quad (1.4)$$

The other figure of merit is the maximum frequency of oscillation, or  $f_{max}$ .  $f_{max}$  represents the frequency where the maximum available power gain ( $G_{p,max}$ ) for a device is unity. The specific equations for the  $f_T$  and  $f_{max}$  of a bipolar device are discussed below.

One potential advantage of the III-V materials used for conventional HBTs is the typically higher electron mobilities compared to Si, a consequence of the direct-bandgap structure of the III-V materials [31]. The higher mobilities correspond to faster electron transit times, which directly translates into higher  $f_T$ 's. The reduction in transit times is further enhanced by the ability to grow very thin epitaxial base layers, which also minimizes the probability that a given electron is lost to recombination in the base. The schematic view of a mesa-defined AlInAs/GaInAs HBT structure on an InP substrate is shown in Figure 1.5 as an example of a conventional III-V HBT. For this device, the emitter and base are kept very thin for ultra-low current consumption and high-speed operation [27]. A layer of  $n+$  GaInAs polysilicon is added on top of the emitter for low-resistance contacting. The performance of this device, published in 1997 with an  $f_T$  and  $f_{max}$  of 120 GHz and 130 GHz, respectively, is described in [32]. Typical values for  $f_T$  and  $f_{max}$  for modern III-V HBTs are in the 300–400 GHz range [33], [34].

### 1.2.2 The SiGe HBT

Although the concept of SiGe semiconductors dates back to the early 1960s, the ability to epitaxially grow active device regions at reasonable temperatures (in the range  $\ll 800^\circ\text{C}$ ) in silicon-based technology was not realized until the late 1980s

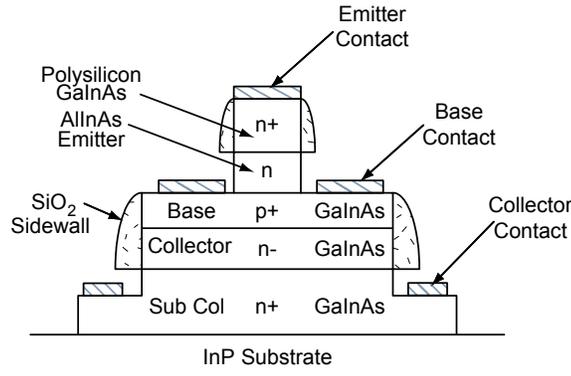


Figure 1.5: Schematic view of mesa-defined AlInAs/GaInAs HBT structure on InP substrate (after [32])

[35], [36]. However, with the advent of ultra-high vacuum chemical vapor deposition (UHV/CVD) [37], the development of defect-free, device quality SiGe films, on standard silicon substrates, rapidly moved from the realm of research laboratories, where the first working device was published in December 1987 [38], to commercial availability, with the first production technology on 200 mm wafers qualified in 1996 [39]. The improved performance of SiGe HBT devices and their integration with proven submicron CMOS processes has sparked significant interest in the capabilities of SiGe and has made Si a strong competitor with III-V HBTs in the high frequency domain.

Today's SiGe HBTs are somewhat different from the conventional III-V HBTs described above. Instead of using a wide-bandgap emitter to enhance device performance, the SiGe HBT relies on an epitaxially grown layer of SiGe to narrow the bandgap of the base. The addition of germanium (which has a bandgap of 0.66 eV) to silicon (which has a bandgap of 1.12 eV) reduces the bandgap of the resulting material by roughly 75 meV (relative to pure Si) for each 10% addition of Ge [40]. The resulting *n-p-n* heterostructure, composed of an *n*-type Si emitter, a narrow-bandgap, *p*-type SiGe base, and an *n*-type collector, provides three main advantages over the conventional Si *n-p-n* homojunction transistor: (1) a reduction in base transit time resulting in greater device speed, (i.e. higher  $f_T$  and  $f_{max}$ ); (2) an increase in collector current density resulting in higher current gain ( $\beta$ ), which can in turn be traded off for lower intrinsic base resistance and lower noise figure; and (3) an increase in Early voltage for a given cutoff frequency ( $f_T$ ), which provides a higher device output

resistance [41]. In fact, the introduction of germanium to the base of Si bipolar transistors provides an extra degree of freedom for tailoring the device operation and performance for specific RF and analog applications.

**Bandgap Engineering in Silicon** The bandgap narrowing of the SiGe HBT base is controlled with the shape and concentration of the Ge doping profile. This profile can be optimized to tune the device performance by varying the Ge concentration across the width of the base [41]. For example, three realizable Ge profiles (with the same total germanium content and base-width) as a function of position ( $x$ ) across the base are shown in Figure 1.6. Although different shapes are possible, the three fairly common ones of SiGe HBT experiments — the box, the triangle, and the intermediate case, the trapezoid — are shown. The impact of these doping profiles can be viewed in terms of a band diagram [3], such as Figure 1.7. Here, the band diagram for a SiGe HBT with the triangle-shaped doping profile is compared with the band diagram for a Si homojunction BJT with a constant doping, or box, profile. For the SiGe HBT, the band discontinuities at the emitter-base junction are virtually unchanged from those of the Si homojunction BJT while at the base-collector junction, the bandgap is significantly reduced for the SiGe HBT due to the increasing concentration of Ge. The triangular doping profile is of particular interest because the grading of Ge content across the base (from emitter to collector) establishes a built-in electric field within the neutral base region. This electric field helps speed injected-electrons from the emitter directly to the collector, which improves the minority carrier flow and the frequency response of the device [3].

For the triangular profile, the reduction in the bandgap closer to the collector-base junction also reduces the potential barrier to electron injection from the emitter, which enhances the collector current density ( $J_c$ ) for a fixed  $V_{BE}$  in comparison to a Si BJT [41]. In other words, the narrower bandgap yields more charge transport from emitter to collector for a given emitter-base bias [3]. On the other hand, the emitter region of the SiGe HBT and the Si BJT are virtually identical and thus, the base current density ( $J_B$ ) is nearly the same for both devices [3]. In effect, only the collector current, which is dependent on the parameters of base, is affected by the Ge profile in the base [42]; the emitter can be designed in the same manner as that of a conventional Si BJT. The increased collector current, at a fixed bias level, leads to

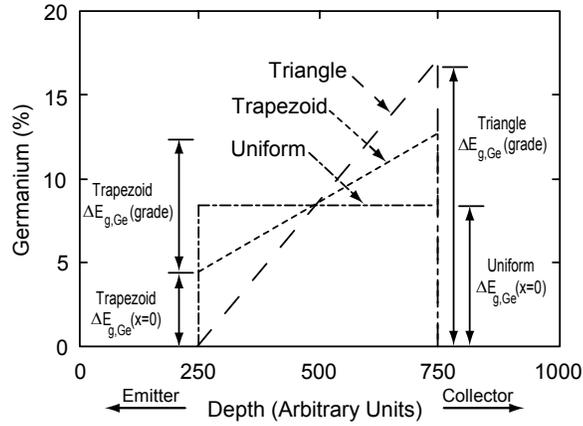


Figure 1.6: Practical Ge profiles for the base of a SiGe HBT (after [41]). The  $\sim 75\text{meV}$  change in bandgap energy for each 10% increase of Ge content,  $\Delta E_{g,\text{Ge}}(x)$ , is shown for each profile, where  $x$  represents a one-dimensional position across the base-width, referenced to the emitter-side of the base.

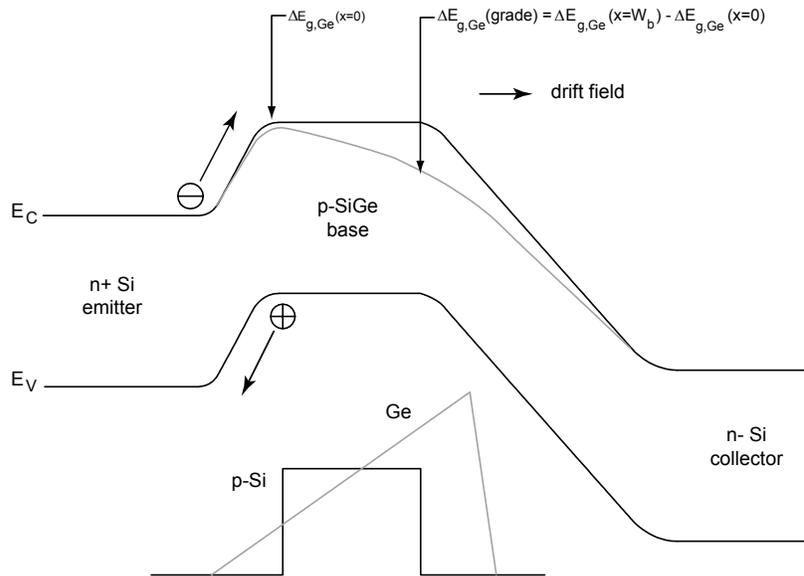


Figure 1.7: Energy band diagram for a graded-base SiGe HBT (gray line) compared to a Si BJT with a constant doping profile (solid line). Note that the emitter-base junction of the SiGe HBT is unchanged compared to that of the Si BJT (after [3])

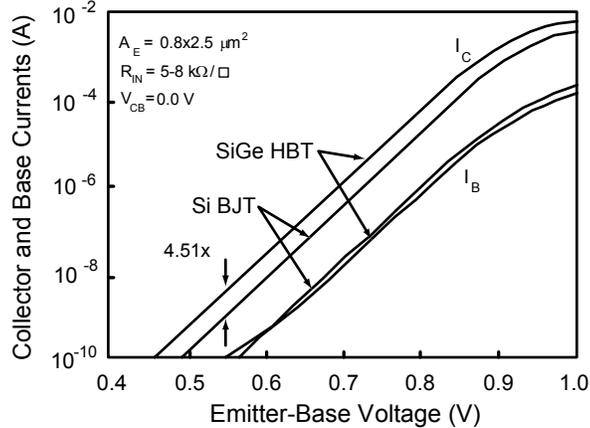


Figure 1.8: Collector and base currents for a Si BJT vs. SiGe HBT with a triangular Ge profile. The base currents are nearly identical, while the collector current of the SiGe HBT is  $4.5\times$  better than that of the Si BJT (after [41]).

greater current gain ( $\beta$ ). As shown in Figure 1.8, which compares the DC collector and base currents for similarly sized SiGe HBT and Si BJT devices as measured in [41], the SiGe HBT exhibits a collector current that is 4.5 times larger than the Si BJT while the base currents are roughly the same; this corresponds to a  $\beta$  that is 4.5 times greater.

The dynamic, or high-frequency, operation of the SiGe HBT is critical to RF applications. For a bipolar device, the  $f_T$  is given by:

$$f_T = \frac{1}{2\pi} \left[ \frac{g_m}{(C_{eb} + C_{cb}) + \tau_b + \tau_e + \tau_c} \right] \quad (1.5)$$

where  $g_m$  is the small-signal transconductance of the device (which is a function of collector current,  $I_C$ );  $C_{eb}$  and  $C_{cb}$  are the emitter-base and collector-base capacitances, respectively; and  $\tau_b$ ,  $\tau_e$ , and  $\tau_c$  are the base, emitter, and collector transit times, respectively [3]. In conventional Si BJTs,  $\tau_b$  typically limits the maximum achievable  $f_T$  [3]. However, in SiGe HBTs with a triangular Ge profile, the built-in drift-field, which is a consequence of the graded Ge content across the base region, accelerates injected electrons from the emitter directly to the collector, thereby decreasing  $\tau_b$  and increasing the achievable  $f_T$  [41]. As more germanium is added closer to the collector-base junction, the drift-field increases in strength and even faster transit times can be achieved.

Alternatively, for the uniform (or box) profile shown in Figure 1.6, the base-emitter junction is engineered in a similar fashion to conventional HBTs: the valence band discontinuity is increased creating a larger potential barrier for hole back-injection, while the conduction band is flattened leading to more efficient electron-injection. This bandgap structure results in a lower base current, larger collector current and, consequently, an even higher  $\beta$  — roughly 11 times the  $\beta$  of a Si BJT. However, the RF performance and operating speed of a SiGe HBT device is inversely proportional to the base transit time,  $\tau_b$ , which depends only on the *grading* of the Ge content across the base. Since the Ge content is constant across the base region for the box profile, these devices rely solely on electron diffusion current through the base. The large  $\tau_b$ , when compared with the triangular profile, results in no significant improvement in RF performance over that of the Si BJT with this profile [41]. Furthermore, since the minimum noise figure for a device ( $F_{min}$ ) is related to  $1/f_T^2$ , the noise performance for the box profile is only moderately improved compared to the Si BJT and is inferior compared to the SiGe HBT with a triangular profile, as a result of the limited  $f_T$  provided by the box profile.

$f_{max}$  is perhaps a more useful performance indicator for RF and microwave applications as it accounts for the inherent series resistance of the base,  $r_b$ .  $f_{max}$  for bipolar devices is given by:

$$f_{max} = \left[ \frac{f_T}{8\pi C_{cb} r_b r_\pi} \right]^{\frac{1}{2}} \quad (1.6)$$

where  $C_{cb}$  is the total collector-base junction capacitance and  $r_b$  is again the parasitic series base resistance [6]. With a triangularly graded Ge base, the  $p+$ -doping of the base (which is typically done with boron) can be increased to reduce  $r_b$  and therefore increase  $f_{max}$ . Reducing the base resistance also directly improves the noise figure of SiGe HBTs [43].

The graded Ge profile in a SiGe HBT also enhances the Early voltage ( $V_A$ ). The Early effect in bipolar devices describes the change in  $\beta$  due to base-width modulation. As the voltage across the collector-base junction ( $V_{CB}$ ) is increased, the depletion region at that junction, which is set up by the reverse bias across  $CB$ , grows further into the base, thereby reducing the width of the quasi-neutral base [44], [45]. The reduction of the base width increases the collector current, and consequently  $\beta$ , since a narrower base region results in increased charge transport between the emitter and collector

(reduced recombination in the base). The change in  $\beta$  due to the decreasing base width is manifested in the device as a non-zero output conductance (finite output resistance). Compared to an identical Si BJT, the Ge grading in a SiGe HBT base makes the collector-base region harder to deplete for a given bias because the base profile is essentially weighted toward the collector [3]. By limiting the expansion of the depletion region, the graded Ge content in the base significantly increases the Early voltage of a device.

**SiGe Fabrication and CMOS Compatibility** SiGe HBTs have become a viable alternative to III-V HBTs for integrated circuits because of their compatibility with standard Si CMOS processes [43]. However, to ensure this compatibility, the device structure departs significantly from traditional fully-epitaxial III-V HBT structure. In these latter devices, the emitter, base, and collector are grown epitaxially, and then etched sequentially to create a mesa-structure (see Figure 1.5). However, these types of structures are generally unsuitable for reliable integration in a BiCMOS technology as the long thermal cycle for dopant activation in CMOS processes can increase defects, cause epitaxial layers to relax, and force the extrinsic doping used for terminal contacts to diffuse into adjacent areas, all of which degrade performance.

A typical CMOS-compatible SiGe HBT structure is shown in Figure 1.9. The  $n+$  sub-collector is formed by patterning of the  $p$ - epitaxial layer that is initially grown on a  $p+$  substrate. A thin  $n$ -epitaxial layer is grown everywhere and is selectively etched to form the collector (while also providing the CMOS active device layer). The surface is cleaned and passivated before the SiGe base layer is epitaxially grown using UHV/CVD. The emitter window to the SiGe base is defined during heavy extrinsic base doping using a disposable emitter “mandrel.” The mandrel is formed with a combination of nitride and thick oxide and provides a spacer between the emitter opening and the extrinsic base during base boron implantation. After implantation, the mandrel is etched away and the polysilicon emitter is deposited, implanted, and annealed to complete the device [46]. An n-type MOSFET device is also depicted in Figure 1.9 to illustrate the integration of MOS devices with HBTs. The oxidation and polysilicon deposition for the gates of the CMOS devices are completed before the HBT processing steps; the source and drain implants are completed after the HBTs are completed. This approach is known as “base-during-gate” (BDG) integration.



Table 1.1: Characteristics of devices in the IBM 5HP SiGe BiCMOS Technology [47].

Device	Characteristics
Standard NPN SiGe HBT	$f_t/f_{max}=47/65$ GHz at $BV_{CEO}=3.35$ V
High-breakdown NPN SiGe HBT	$f_t/f_{max}=22/55$ GHz at $BV_{CEO}=5.3$ V
Si n-FET	$L_{eff}=0.39$ $\mu\text{m}$ , $f_T/f_{max}=20/22$ GHz
Si p-FET	$L_{eff}=0.36$ $\mu\text{m}$ , $f_T/f_{max}=10/17$ GHz
Schottky Diode	$V_f=0.31$ V
Varactor	$C_J=1.2$ fF/ $\mu\text{m}^2$
DCAP	$C=1.5$ fF/ $\mu\text{m}^2$
MIM Capacitor	$C=0.7$ fF/ $\mu\text{m}^2$
Inductor	$L=1$ nH, $Q=9@5$ GHz
PolySi Resistor	$R_s=220$ $\Omega/\square$

stack is referred to as “last metal” and is  $\sim 2$   $\mu\text{m}$  thick, which results in a relatively low sheet resistance; moreover, this sheet resistance is significantly less than that of the lower metal layers, which are only 0.8  $\mu\text{m}$  thick. Therefore, last metal is typically used for interconnects that carry large DC currents or RF signals. The lossy substrate in SiGe 5HP (which has a resistivity of around 10–20  $\Omega \cdot \text{cm}$ ) can be broken up with deep trench isolation. The deep trenches are etched into the substrate and refilled with undoped polysilicon to provide a high resistance barrier within the substrate. By default, deep trench isolation grids are placed under passive components, such as MIM capacitors, inductors, and bondpads, to limit the degradation in performance that results from substrate coupling.

### 1.2.4 The Freescale SiGe:C RFBiCMOS Process

HiP6WRF is the Freescale (formerly Motorola) name for their 0.18  $\mu\text{m}$  SiGe:C RF-BiCMOS process [49]. The “:C” denotes the incorporation of carbon during the epitaxial growth of the SiGe base. The addition of carbon has been shown to reduce transient enhanced diffusion (TED) effects that can corrupt the narrow boron doping profile in the SiGe base. The desired base doping profile is difficult to achieve in practice without the addition of carbon [6].

The integrated 0.18  $\mu\text{m}$  NMOS devices have an  $f_T$  of 60 GHz, making them suitable for RF applications through the 5–6 GHz frequency band. The SiGe HBT devices

Table 1.2: Characteristics of devices in the Motorola SiGe:C RFBiCMOS Technology [49].

Device	Characteristics
Standard NPN SiGe HBT	$f_t/f_{max}=49/93$ GHz at $BV_{CEO}=3.3$ V
Si n-FET	$L_{eff}=0.0892$ $\mu\text{m}$ , $f_T/f_{max}=60/50$ GHz
Si p-FET	$L_{eff}=0.36$ $\mu\text{m}$ , $f_T/f_{max}=\text{Not Reported}$
Gate Capacitor	$C=8$ fF/ $\mu\text{m}^2$
MIM Capacitor	$C=1.6$ fF/ $\mu\text{m}^2$
Inductor	$L=3$ nH, $Q=18@2$ GHz
PolySi Resistor	$R_s=1500$ $\Omega/\square$
Thin-film Resistor	$R_s=50$ $\Omega/\square$

are comparable to the IBM 5HP devices, with an  $f_T$  of 49 GHz and an  $f_{max}$  of 93 GHz at a  $BV_{CEO}$  of 3.3 V. Table 1.2 shows the published characteristics of some of the components offered within the technology. Though not shown in the table, the technology also includes accumulation mode varactors, which are important for VCO tuning applications.

The HiP6WRF layer stack is made up of five copper interconnect layers. The top three, M3-M5, are  $\sim 0.4$   $\mu\text{m}$  thick while the bottom two, M1-M2, are  $\sim 0.2$   $\mu\text{m}$  thick. Because thin-film copper retains a larger percentage of its bulk conductivity than aluminum, the interconnect metal layers can afford to be thinner compared to the metal layers in the 5HP process above. However, at the minimum metal widths, the nominal sheet resistance of M3, M4, or M5 is 64 m $\Omega/\square$ , which is slightly higher than the aluminum “last metal” layer in 5HP. HiP6WRF also includes an additional copper layer, known as the “bump” layer, that is deposited by electroplating after the chip passivation layer. This 10  $\mu\text{m}$  thick electroplated copper is ideal for on-chip inductor structures.

### 1.3 Receiver Architectures

The ability of RF wireless receivers to distinguish a desired, faint signal from a spectrum of undesired and potentially interfering signals is a remarkable feat in electrical engineering. For more than 70 years, this reception of transmitted information was accomplished primarily with Edwin Armstrong’s superheterodyne receiver topology.

However, recent advances in IC technology have generated a great deal of interest in alternative receiver architectures that can provide higher levels of integration. The following sections give an overview of the dominant receiver architectures in use today.

### 1.3.1 Superheterodyne Receivers

Traditionally favored for their high selectivity and sensitivity, heterodyne receivers down-convert an RF signal to sequentially lower intermediate frequencies (IFs) for amplification and filtering prior to baseband processing [50]. The block diagram of a generic heterodyne receiver chain is shown in Figure 1.10 and illustrates its operation: the RF spectrum received by the antenna is first filtered (1) to select the overall frequency band of the communications system of interest; a low-noise amplifier (2) follows to boost the weak, desired signal and offset the typically high noise figure of the subsequent filter (3) and mixer (4); the mixer performs the frequency down-conversion, translating the RF spectrum to an intermediate frequency determined by the local oscillator (LO); a channel selection filter (5) is then employed to remove nearby, in-band interferers; finally, a series of high gain stages (6) amplify the signal for envelope detection, demodulation, or conversion to the digital domain. In practice, multiple IF stages are used as discussed below.

#### The Superheterodyne Approach

The process of down-converting the signal to a lower, intermediate frequency provides at least two important advantages: selectivity and tunability. The first is related to the use of an intermediate frequency — by translating the desired signal to a lower frequency, the need for prohibitively high filter  $Q$ s is alleviated. As illustrated in Figure 1.10, sharp cutoff filters (“high- $Q$ ”) are needed at some point in the receiver chain to attenuate any nearby interferers that can corrupt the reception of the desired signal. Since typical filters exhibit a tradeoff between their insertion loss and the  $Q$  of their component resonators [13], placing a highly selective filter for channel selection at the front of the receiver introduces a significant amount of loss. This loss requires a large amount of gain from the first stage of amplification and significantly degrades the overall receiver noise figure since the first stage sets the minimum noise figure in a cascade of components (see Section 4.1 for further discussion). In other words,

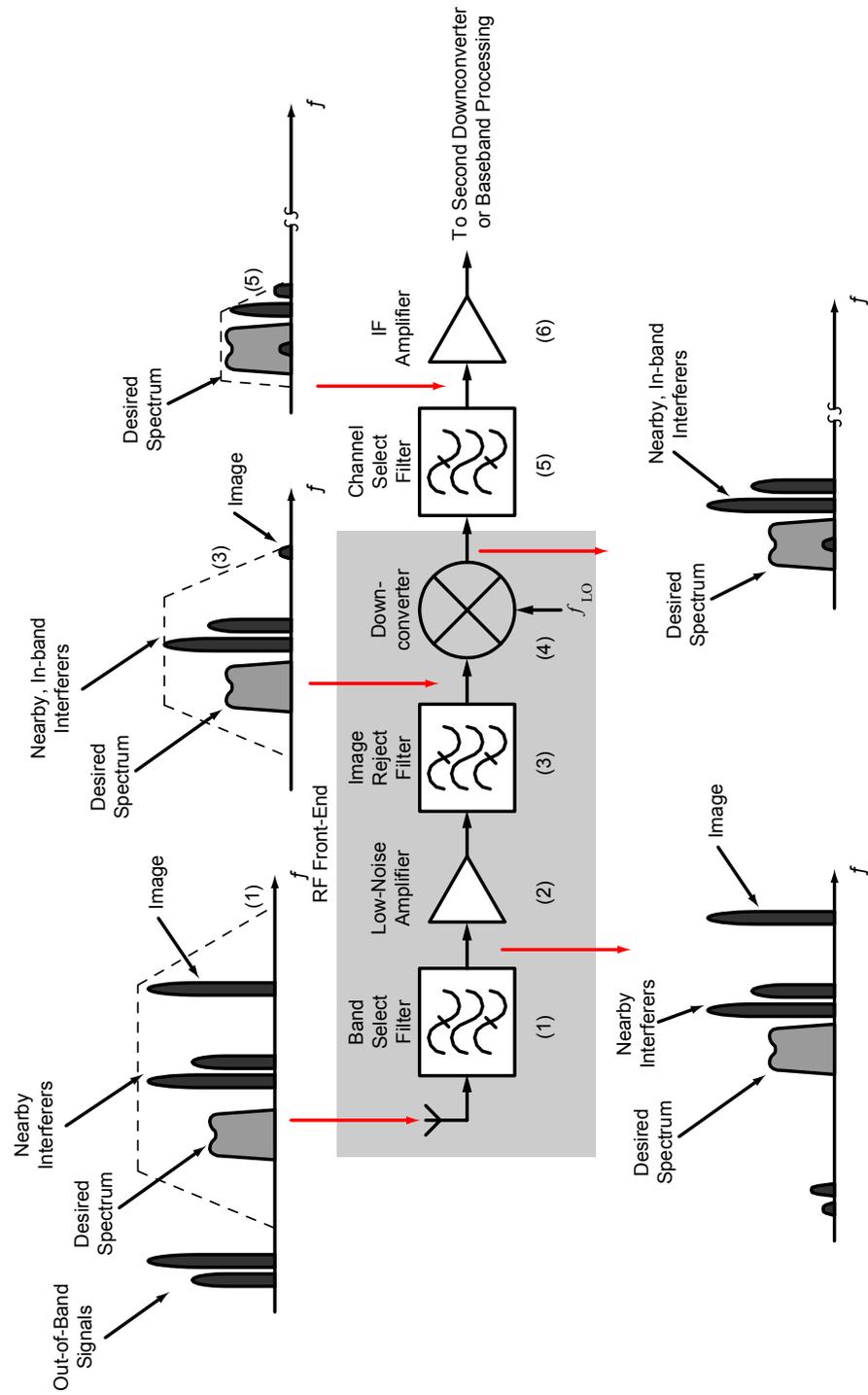


Figure 1.10: Block diagram of the super heterodyne receiver topology (after [13]).

the ability of the receiver to detect very low-power signals, known as sensitivity, is degraded by the increase in noise.

A second advantage of the superheterodyne is in the tunability of the receiver. Since the IF is determined by the frequency of the LO, the center frequencies of the filtering components after the mixer can remain fixed and the LO tuned to give a fixed IF for a range of RF frequencies. LO generation is typically done with a voltage-controlled oscillator (VCO) (often embedded within a phase-locked loop). In practice, VCO tunability is considerably easier than re-tuning the bandpass filter used for channel selection each time the RF frequency to be received changes.

A major drawback to the superheterodyne topology arises from the problem of *image* frequencies. In the mixing process, the intermediate frequency is defined as:

$$f_{IF} = |f_{RF} - f_{LO}| \quad (1.7)$$

where  $f_{RF}$  and  $f_{LO}$  are the frequency of the RF and local oscillator signals, respectively. After mixing the RF and LO signals (that is, the analog multiplication of the two), the polarity of the difference between the two signal frequencies is not maintained; thus,  $f_{RF} - f_{LO}$  yields the same IF as  $f_{LO} - f_{RF}$ . In other words, the superheterodyne architecture down-converts the bands located an equal  $\Delta f$  on either side of the LO to the same IF frequency (Figure 1.11). In terms of the IF, the image frequency ( $f_{IM}$ ) is located at:

$$f_{IM} = f_{LO} - f_{IF} = 2f_{LO} - f_{RF} \quad (1.8)$$

for low-side injection (i.e. the LO is lower in frequency than the RF) and

$$f_{IM} = f_{LO} + f_{IF} = 2f_{LO} - f_{RF} \quad (1.9)$$

for high-side injection (i.e. the LO is higher in frequency than the RF, as depicted in Figure 1.11). The desired RF signal and the image are separated in frequency by  $2f_{IF}$ . With the image and the RF signal translated to the same IF, the image signal represents an unwanted interference component corrupting the desired RF spectrum. Furthermore, if at a significantly high power level, the image acts like an in-band interferer, potentially desensitizing the receiver front-end from the desired signal due

to gain compression [51]. To mitigate these effects, an image-reject filter (IRF) must be placed before the mixer to sufficiently attenuate the image. This filter is designed to have minimal loss for the desired channel and large suppression of the image.

The choice of the IF frequency determines the image frequency and impacts the rejection of the image signal. A low IF allows for high selectivity and suppression of nearby interferers since the channel selection occurs at a low frequency. With an IF close to baseband, highly-selective, active, analog filters, which are straightforwardly integrated on-chip, can perform the channel filtering. However, a low IF places the image close to the desired RF signal and limits the image rejection that can be achieved with practical filters at the RF frequency. Therefore, alternative methods of image rejection (to be discussed below) must be employed to reduce the image; otherwise, since the image cannot be attenuated without affecting the desired signal, greater image corruption must be tolerated within the communication system. On the other hand, a high IF results in substantial image rejection with an RF filter, since the image is far away in frequency from the desired RF spectrum and thus, well into the rejection-band of the (properly designed) image reject filter. However, with such a high IF, the receiver selectivity suffers because at a higher frequency, highly selective — but very lossy — filters cannot be employed for channel selection and thus, nearby interferers are poorly attenuated. Basically, heterodyne receivers exhibit a tradeoff between sensitivity (image rejection) and selectivity.

To ease the tradeoff between selectivity and image rejection, additional stages of down-conversion with successively lower IFs are used. The sequence of IFs allows for partial channel selection with increasing filter  $Q$ s at each lower IF and thus provides greater selectivity without requiring highly-selective, lossy filters [52]. In modern heterodyne receivers, the image-reject filter is typically a surface acoustic wave device (SAW) [53] that is relatively large and expensive, sensitive to impedance mismatches, and currently not suitable for on-chip integration <sup>4</sup>. Given the push for higher levels of integration, this disadvantage has motivated designers to look at alternative receiver architectures.

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<sup>4</sup>However, there is significant research on integrating such devices on chip.

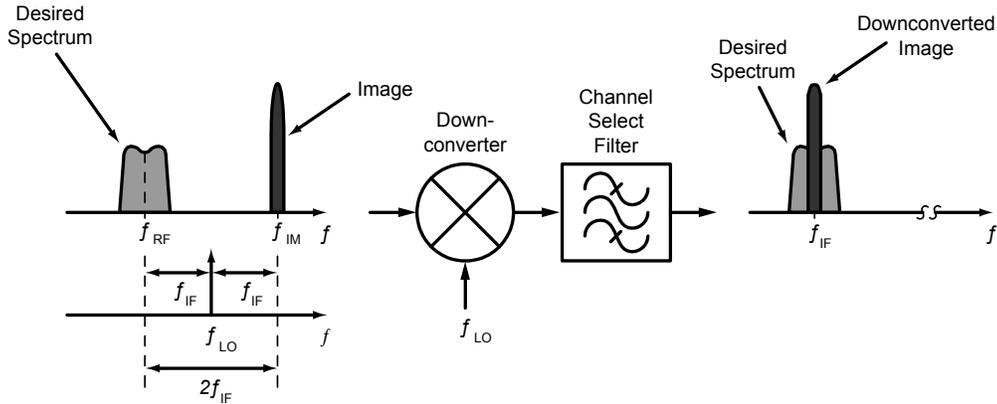


Figure 1.11: Illustration of the image problem in heterodyne receivers.

### 1.3.2 Low-IF Image-Reject Receivers

The low-IF receiver architecture is an extension of the superheterodyne approach, where the intermediate frequency is very near baseband [54]. As mentioned in the previous section, the choice of a lower IF allows for the substitution of the RF image rejection filter with an IC-based approach for removing the image — for example, an analog technique such as the Hartley [55] or Weaver [56] architectures, or a “mixer-free” digital technique like sub-sampling with delay processing [57]. The performance of an image-rejection methodology can be quantified with the image rejection ratio ( $IRR$ ), the ratio between the power of the desired signal,  $P_{sig}$ , and the power of the image,  $P_{im}$ :

$$IRR \text{ (dB)} = 10 \log \left( \frac{P_{sig}}{P_{im}} \right) \quad (1.10)$$

An  $IRR$  on the order of 70 to 80 dB is typically required in modern RF applications [13], [58].

In a Hartley receiver, depicted in Figure 1.12, the desired RF signal is first downconverted in quadrature to a low-IF ( $A$ ) and low-pass filtered, typically with an active filter ( $B$ ). The resulting Q channel signal is shifted by  $90^\circ$  relative to the I channel ( $C$ ), and the two channel signals are then added together ( $D$ ) [13]. The in-line  $90^\circ$ -shift operation of the Q branch signal reverses the polarity of the image component so that when the I and Q signals are summed together, the images in each branch cancel; meanwhile, the desired signal is unaffected by the  $90^\circ$ -shift and the RF spectrum is

theoretically downconverted without corruption by the image [13]. Appendix A.1 provides a mathematical derivation of each step of this operation.

Alternatively, the Weaver architecture replaces the in-line  $90^\circ$ -shift operation with an additional set of quadrature mixers at the IF to achieve the same result. Basically, the second I/Q mixing stage provides the additional  $90^\circ$  phase shift needed to give image subtraction. Figure 1.13 shows the block diagram of a low-IF receiver with quadrature outputs with the Weaver architecture providing analog image-rejection. Appendix A.2 provides a mathematical derivation of each step of the Weaver architecture.

However, since the second set of mixers downconverts the signal to a second IF, a second image signal exists and must be accounted for [59]. Similar to the first image, and relative to the first IF, the second image is located at

$$f_{IM_2} = 2f_{LO_2} - f_{IF_1} = 2f_{LO_2} - f_{RF} + f_{LO_1} = f_{IF_1} - 2f_{IF_2} \quad (1.11)$$

for low-side injection and

$$f_{IM_2} = 2f_{LO_2} - f_{IF_1} = 2f_{LO_2} - f_{LO_1} + f_{RF} = f_{IF_1} + 2f_{IF_2} \quad (1.12)$$

for high-side injection. To suppress this image, the signal after the first downconversion is passed through a bandpass filter rather than a low-pass filter. Further suppression can be achieved by choosing the first and second IFs so that the location of the second image frequency before any downconversion, which is given by:

$$f_{IM_2} = 2f_{LO_2} - f_{RF} + 2f_{LO_1}, \quad (1.13)$$

is in an unused band that is not expected to have a significant amount of energy.

The downside of analog image-rejection architectures is their sensitivity to amplitude ( $\epsilon$ ) and phase ( $\Delta\phi$ ) errors. In the case of the Hartley architecture, the realization of a constant-gain, frequency-independent  $90^\circ$ -phase shifter is extremely difficult; for the Weaver architecture, the LO signals must be exactly in quadrature, or image suppression degrades significantly. The image-rejection ratio can be expressed in

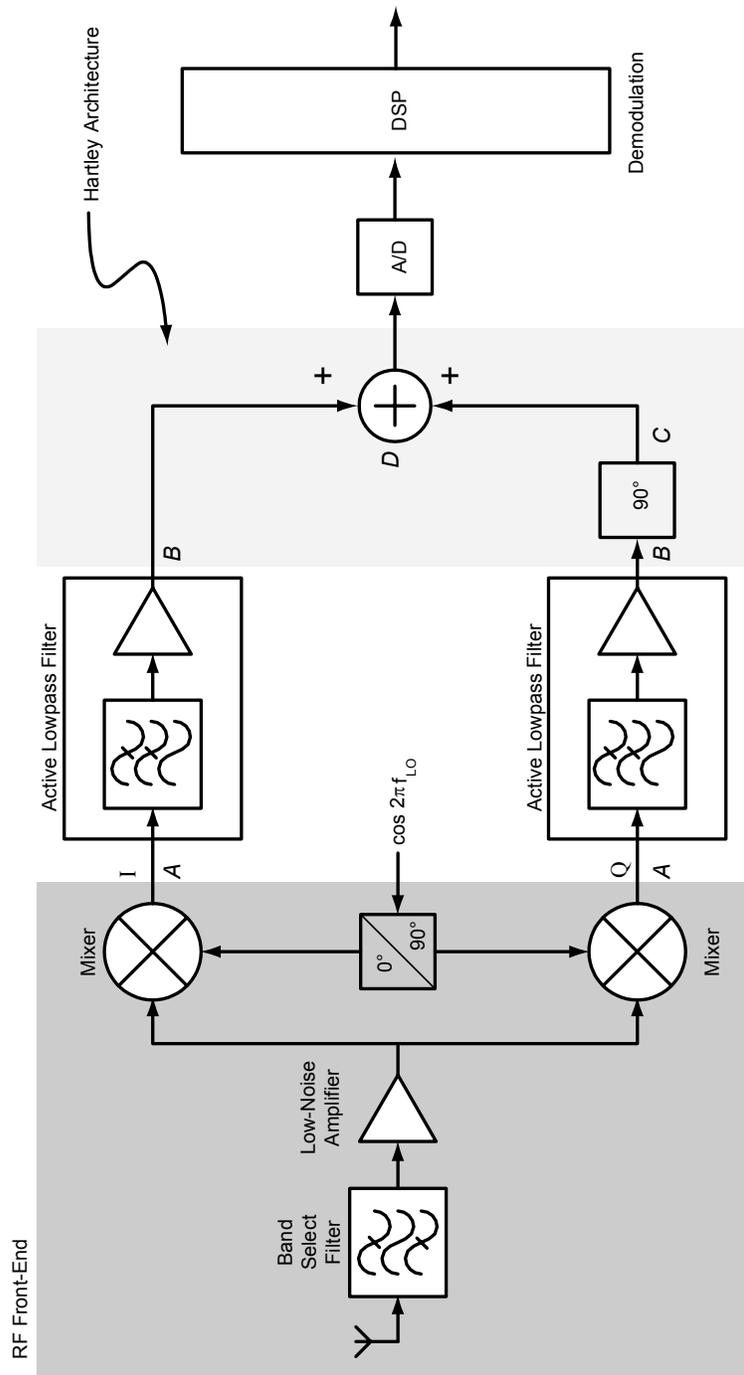


Figure 1.12: Block diagram of a low-IF receiver with Hartley image-reject architecture.

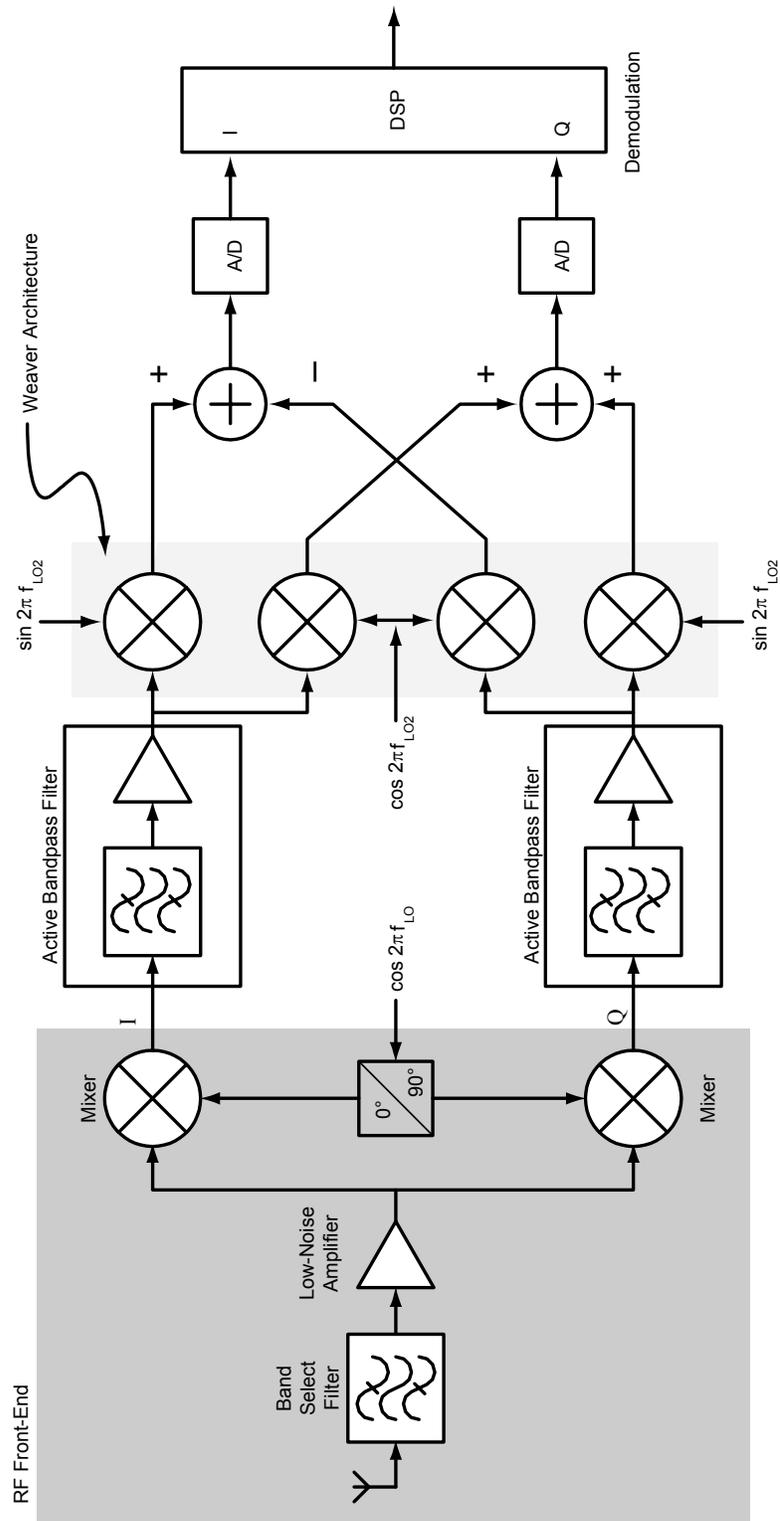


Figure 1.13: Block diagram of the low-IF receiver with Weaver image-rejection architecture.

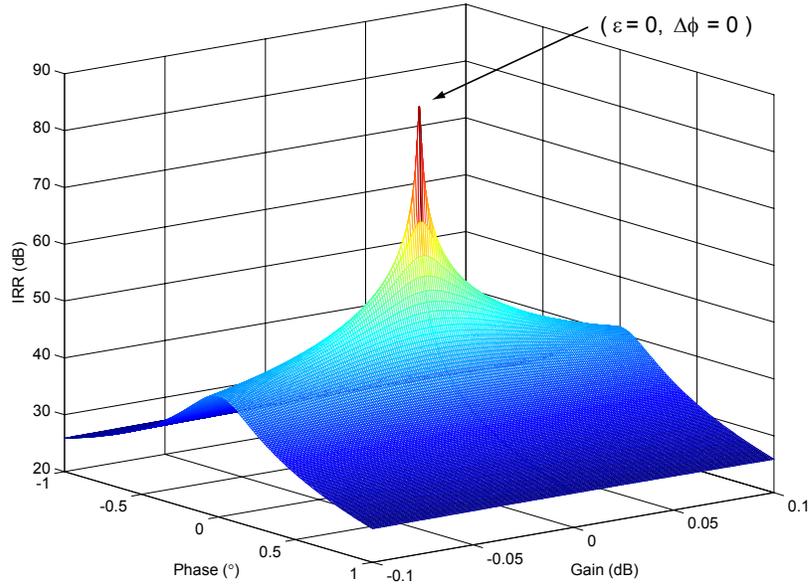


Figure 1.14: Image rejection ratio as a function of I/Q gain and phase errors.

terms of  $\epsilon$  and  $\Delta\phi$  to show the impact of such errors [60]:

$$IRR(\text{dB}) = 10 \log \left( \frac{4}{\epsilon^2 + (\Delta\phi)^2} \right) \quad (1.14)$$

Figure 1.14 shows a three-dimensional plot of Equation 1.14 over ranges of  $\epsilon$  and  $\Delta\phi$ . For example, a gain mismatch of 0.1% and a phase imbalance of  $1^\circ$  results in an image rejection ( $\sim 41$  dB) that is far less than what is normally required. Thus, in practice, neither the Weaver nor the Hartley architectures alone are sufficient. Other methods, such as additional filtering or digital correction/calibration in DSP, are necessary<sup>5</sup>. Nevertheless, since modern ADCs and DSPs can easily operate at low megahertz frequencies, low-IF architectures are an extremely viable alternative to the superheterodyne architecture [61], although excessive power consumption issues must be addressed.

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<sup>5</sup>A variation on these purely analog approaches is to place the analog-to-digital converters (ADCs) immediately after the bandpass filters, thus allowing for image rejection to be performed digitally with the Weaver architecture. Converting the low-IF signal to the digital domain directly allows the Weaver mixers to be implemented with a digital signal processor (DSP), which can also provide a simple method for correcting the amplitude and phase errors introduced in the analog portion of the receiver [54].

Low-IF receiver architectures also have stringent requirements for linearity [62]. Second-order distortions, resulting from receiver nonlinearities, can generate a frequency component that appears in the downconverted band, thereby corrupting the received signal [63] (see Section 1.3.3). Likewise, any gain and phase imbalance between the I and Q channels not only results in poor image rejection, but also causes high bit error rates (BER) in the demodulation of the received signal (see Section 1.3.3).

### 1.3.3 Direct-Conversion Receivers

*Direct-conversion receivers* (DCRs), also known as *zero-IF* or *homodyne* receivers, are a special case of the heterodyne approach. Instead of down-converting to a finite IF, DCRs translate the desired RF spectrum directly to DC, or 0 Hz, using an LO frequency exactly equal to the RF. The simplicity of this architecture affords two major advantages over the classical superheterodyne topology. First, because the IF frequency is zero, the image to the desired RF signal is the desired signal itself. In other words, the RF bands on both sides of the LO signal contain transmitted information and need to be detected (see the section below on *I/Q Mismatch*). Thus, the bulky, off-chip, front-end image-reject filters required in the superheterodyne topology can be eliminated [64]. Second, with the desired spectrum down-converted directly to baseband, channel selection can be performed either with a simple low pass filter or by converting to the digital domain with an ADC and digitally performing channel selection in DSP. The capability of using a DSP raises the possibility of having a universal RF front-end, where any type of wireless standard (e.g. GSM, CDMA, 802.11a, etc.) can be received with the same analog blocks and decoded using digital methods. A fundamental, unchanging RF front-end is one of the keys in realizing multi-mode, multi-standard software radios [65]. The block diagram of a DCR is shown in Figure 1.15.

Consequently, the direct-conversion architecture is highly attractive for integrated RF receivers. The reduction in off-chip components results in higher levels of integration and lower costs. Furthermore, the elimination of off-chip filters simplifies inter-stage matching, since the need to match to the input and output impedances of the off-chip filter is eliminated. By filtering at baseband frequencies, device parasitics are less severe and less current is needed for amplification; thus, DCRs also offer the potential

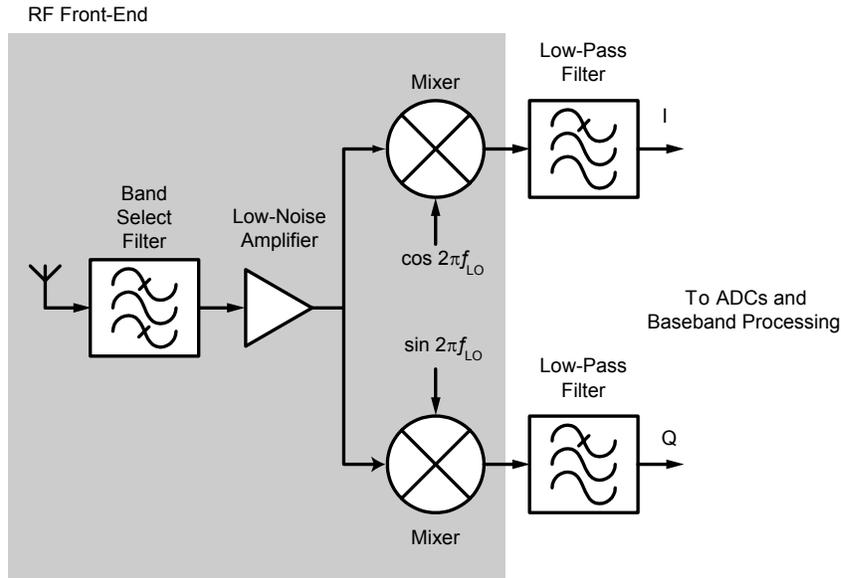


Figure 1.15: Block diagram of the direct conversion receiver.

for low-power consumption. However, DCRs suffer from a number of unique issues, making their actual implementation less than straightforward.

### DC Offsets

RF band selection is the only filtering performed in the receive chain of a DCR before the signal is down-converted to baseband. Therefore, strong, nearby signals, including the receiver's own LO, can mix with themselves (self-mixing) down to zero-IF, generating DC levels (potentially time-varying) that appear as interference at the center of the desired band. Figure 1.16 shows three potential self-mixing mechanisms for creating DC-offsets.

Figure 1.16(a) shows self-mixing due to the finite isolation between the LO and RF ports of a mixer in one branch of the DCR. For an integrated mixer, port-to-port isolation is limited by substrate coupling, bondwire radiation, and capacitive and magnetic coupling [65]. Since the LO is typically a strong signal, in order to provide sufficient drive for the mixer switching core, the LO can leak through these unintended paths with sufficiently high amplitude back to the LNA. There, the LO signal can reflect off the LNA output back into the mixer input and mix with itself

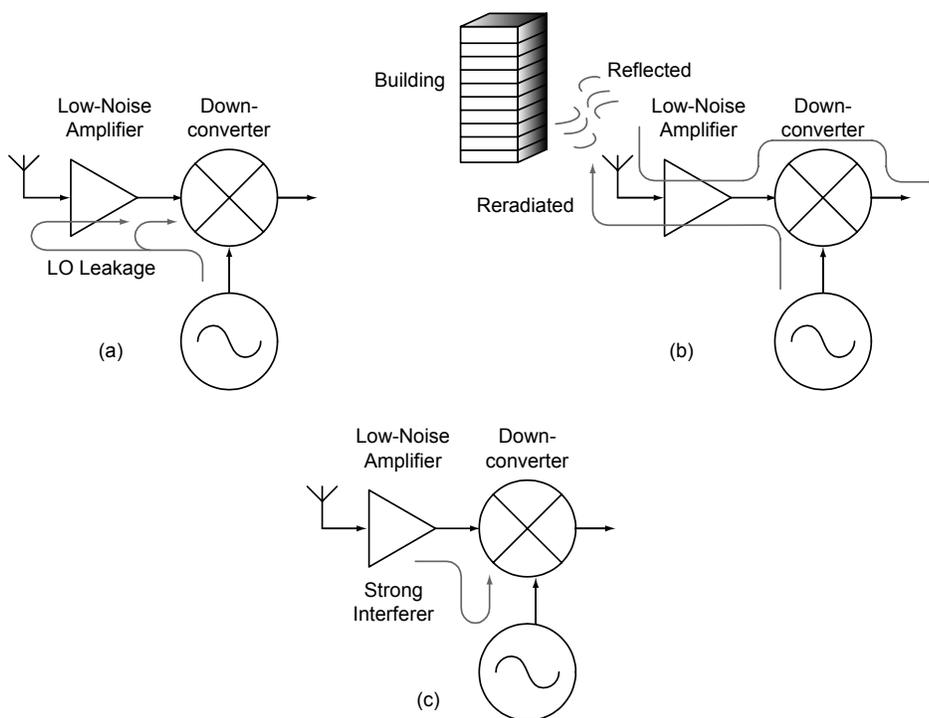


Figure 1.16: DC offset mechanisms: (a) LO leakage, (b) LO reradiation, (c) strong in-band interferer (after [65]).

generating a static DC level. Furthermore, if the LO signal leaks back to the LNA input, the situation is exacerbated since the LO is amplified. The LO signal can also be reradiated by the antenna, reflect off obstructions such as a building or a moving vehicle, and be recaptured by the front-end. With fading and multi-path reception, the received power level can therefore rapidly vary, resulting in a time-varying or dynamic DC-offset [Figure 1.16(b)]. The reradiation of the LO can also cause problems for other users in the same receive band. Since the LO is at the same frequency as the RF, it appears in the passband of the RF band select filter of other users in the system. Thus, as shown in Figure 1.16(c), a strong nearby interferer such as another user's LO, can also generate DC-offsets by finding a path to the mixer LO port and mixing with itself.

The impact of such DC-offsets on a communication system depends on the type of modulation being employed. For example, Gaussian minimum phase shift keying (GMSK) modulation, used in the Global System for Mobile Communications (GSM), has significant signal content near DC. Thus, a time varying DC-offset can lead to fatal signal corruption. On the other hand, quadrature phase shift keying (QPSK), used in code division multiple access (CDMA) schemes, is less susceptible to DC-offsets [64]. Nonetheless, DC-offsets appearing at the center of the down-converted spectrum can dominate the output of the mixer. If large enough, the DC levels can saturate or desensitize the baseband components after the mixer, degrading amplification of the desired signal thereby reducing sensitivity.

While the simplest solution for removing DC-offsets is to high pass filter the spectrum with a series AC coupling capacitor, this method is not always feasible. As mentioned above, GMSK (and many other modulation schemes) has significant signal content at DC; capacitively coupling the mixer output can lead to a loss of information and higher BER. Furthermore, the corner frequency of the high-pass filter has to be extremely low, on the order of 10s of Hertz; the required on-chip area for a series capacitor at these frequencies is prohibitively large. Large size capacitors also tend to react slowly to dynamically changing DC levels. Therefore, other methods, or combinations of methods, are employed to mitigate unwanted DC levels, including:

- improving isolation between RF and LO paths [19];
- sub-harmonic or super-harmonic mixing — with an LO at some integer multiple

or fraction of the RF, DC-offsets due to LO self-mixing can be significantly suppressed [66];

- DC-free coding at the transmitter — by removing the signal content at DC, reasonable high pass filtering can be employed, particularly for wideband channels (e.g. CDMA) [13];
- offset calibration techniques — digital sample-and-hold feedback, offset estimation with corrective feedback at baseband, and servo loops, can be used to track the DC-offset and remove it from the desired spectrum [64].

### **Flicker ( $1/f$ ) Noise**

Flicker noise describes the ubiquitous low frequency noise that increases as frequency decreases, i.e.  $1/f$  noise. Flicker noise is a significant problem in RF systems in general because nonlinear devices and circuits can up-convert this noise spectrum into the RF range, such as in an RF oscillator where the close-in phase noise is set by the  $1/f$  noise of the active devices [6], [13]. However, in the direct-conversion case, low frequency noise presents an additional challenge as it can appear directly in the down-converted band and therefore degrade the overall  $SNR$ .

The  $1/f$  corner frequency  $f_\alpha$ , is the frequency at which the flicker noise and the receiver thermal noise floor are equal and is often used to compare device noise performance [58]. The value of  $f_\alpha$  is dependent on the semiconductor process [64]: for bipolar devices, a corner frequency as low as  $\sim 8$  kHz can be achieved, while with metal-oxide silicon field-effect transistors (MOSFETs),  $f_\alpha$  can range from tens of kilohertz to a few megahertz [64], [58]. Flicker noise in semiconductor devices is believed to result from traps existing at interfaces between different material layers. The exact effect of the traps on the carriers of a device is still subject to some debate [67], [68], [69]. Nevertheless, the disparity in  $f_\alpha$  between the two different device types can be understood from the illustration in Figure 1.17. In the case of an HBT device, more carriers flow perpendicular to material interfaces, which lowers the probability of a carrier seeing a trap; in a MOSFET device, on the other hand, carriers flow parallel to the interface and the potential for carriers to be trapped/de-trapped increases, thereby increasing flicker noise.

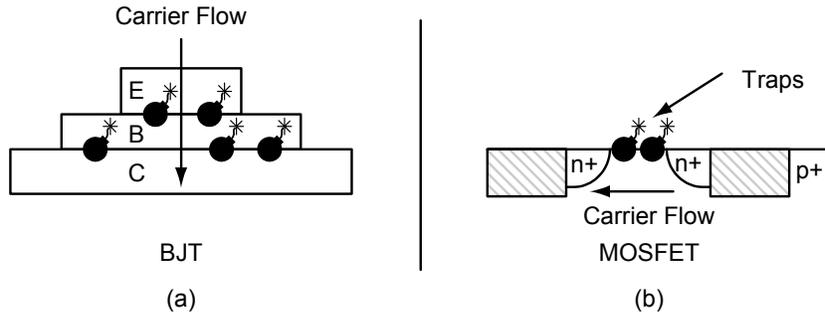


Figure 1.17: Illustration of device carrier flow (a) perpendicular to material interfaces for a BJT; (b) parallel to material interfaces for a MOSFET.

Like DC-offsets, the impact of  $1/f$  noise depends on the modulation scheme. For narrowband systems like GSM, high corner frequencies can effectively raise the noise figure and degrade the SNR of the received signal; on the other hand, in wideband systems, such as CDMA,  $1/f$  noise has minimal effect.

### Even-order Distortion

Intermodulation distortion (IMD) can have deleterious effects on the system performance of a radio transceiver. IMD products result from the interaction of large signals with circuit nonlinearities, resulting in signal components arising at frequencies in or near the passband of a receiver or at baseband frequencies. IMD products can cause an increase in bit errors, suppress receiver sensitivity, and/or generate interference to other users or systems [70]. Products due to odd-order distortion (in particular third-order) are a significant problem in the design of all receivers as third-order intermodulation products (e.g. IM3) fall directly within the band of interest and cannot be filtered easily. For direct-conversion receivers, even-order distortions must also be considered as they lead to second-order intermodulation products (e.g. IM2) that either fall within the down-converted baseband spectrum [71] or, in the case of a large single-tone interferer, generate a time-varying DC-offset [72]. Second order nonlinearities are also problematic for signals with strong envelope variations, such as a signal that undergoes fading during propagation, since these amplitude modulations (AM) are essentially demodulated into baseband components by even order nonlinearities [52, 73].

To see the effects of second order distortion on a direct-conversion receiver, Figure 1.18(a) shows the front-end of a generic DCR that suffers a second-order nonlinearity within the LNA. For analysis purposes, the nonlinear response of the LNA can be approximated with the following power series:

$$y(t) = k_1x(t) + k_2x^2(t) + k_3x^3(t) + \dots \quad (1.15)$$

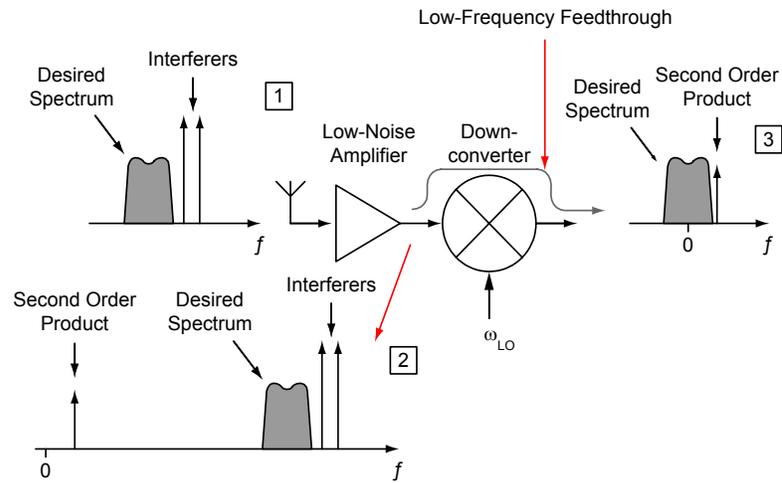
Applying two tones of equal power ( $A_1 = A_2 = A$ ) at the LNA input, where the tones are given as  $x(t) = A \cos 2\pi f_1t + A \cos 2\pi f_2t$ , the resulting output spectrum can be found by substituting  $x(t)$  into Equation 1.15. Using trigonometric identities, Equation 1.15 can be simplified and leads to the second-order product  $k_2 \cos(2\pi(f_1 - f_2)t)$ . This frequency component can then leak through the mixer (due to finite RF-to-IF isolation) and appear at baseband, as shown in 3 of Figure 1.18(a). Though not depicted here, the mixer itself can also have second-order nonlinearities and further degrade the desired baseband signal.

In the case of a single-tone applied at the LNA input, where  $x(t) = A \cos 2\pi ft$ , the output is given by:

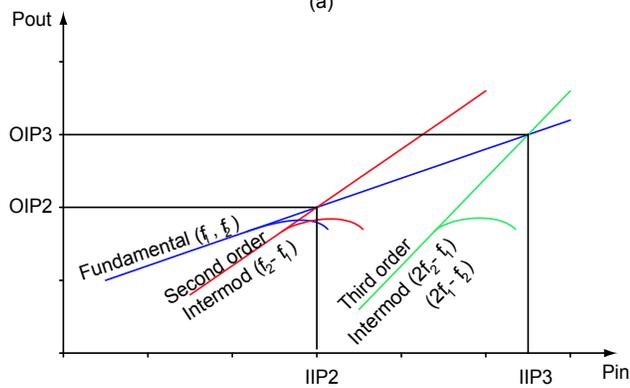
$$\begin{aligned} y(t) &= k_1A \cos(2\pi ft) + k_2A^2 \cos^2(2\pi ft) \\ &= k_1A \cos(2\pi ft) + \frac{1}{2}k_2A^2 [1 + \cos(2\pi(2f)t)] \\ &= \frac{1}{2}k_2A^2 + k_1A \cos(2\pi ft) + \frac{1}{2}k_2A^2 \cos(2\pi(2f)t). \end{aligned} \quad (1.16)$$

The first term in Equation 1.16 is a DC component related to the second-order nonlinearity of the circuit,  $k_2$ , and is magnified by the square of the input signal amplitude. Therefore, any large signal within the passband of a direct-conversion receiver can generate a large DC-offset if the even-order performance of the receiver is poor ( $k_2$  is relatively large).

A common method for characterizing intermodulation distortion is the two tone test [74]. Here, two (conventionally) equal-amplitude tones, slightly offset in frequency, are applied to the input of a circuit. The power levels of the second and third order IM products and the fundamental tones are measured at the circuit output. The measured data is linearly extrapolated beyond compression until the IM curves intersect with the curve of the fundamental. These intersections, which are non-



(a)



(b)

Figure 1.18: Intermodulation distortion: (a) second order effect on strong interferers (after [52]), (b) extrapolation of tones to find the second and third order intercept points, IP2 and IP3, respectively.

physical since they lie beyond the compression point, are known as the intercept points (IPs) for the different IM products. Figure 1.18(b) shows the extrapolation and the location of the input second order intercept point (IIP2) and the input third order intercept point (IIP3). Assuming the slope of the second-order IM product is roughly 2 and the slope of the third-order IM product is roughly 3, the intercept points can be calculated from a two-tone test at a single input power level ( $P_{in}$ ) using the following equations:

$$IIP_2 = 2P_{in} - IM_2 \quad (1.17)$$

$$IIP_3 = \frac{3}{2}P_{in} - \frac{IM_3}{2}. \quad (1.18)$$

Since any large signal can generate a DC offset from a second-order nonlinearity, as shown in Equation 1.16, the second-order intermodulation product and the IIP2 of a circuit can also be found using a single-tone test [75]. In this case, a single tone is applied to the circuit input and the DC-offset generated by the second-order nonlinearity is measured. The IIP2 is related to the IM2 at DC by:

$$IIP_2 = 2P_{in} - (IM_{2_{DC}} + 3 \text{ dB}) \quad (1.19)$$

where the 3 dB term is added so that the results are consistent with two-tone tests, which have twice as much total input power (3 dB) due to the second tone. The intercept points give the absolute power level of the IM products for a given input power level. From these, the relative suppression (RS) of the unwanted products with respect to the fundamental can be determined:

$$RS_2 = P_{in} - IIP_2 \quad (1.20)$$

$$RS_3 = 2(P_{in} - IIP_3). \quad (1.21)$$

The required relative suppression for each block in a receiver chain is determined by the overall system design.

Two common ways to combat even-order distortion include the use of well-balanced, or differential circuitry, and the use of feedback. Balanced circuitry is effective because ideally common-mode signals are rejected and thus, second order nonlinearities become a non-issue [76]. Although device mismatches make the actual nonlinear-

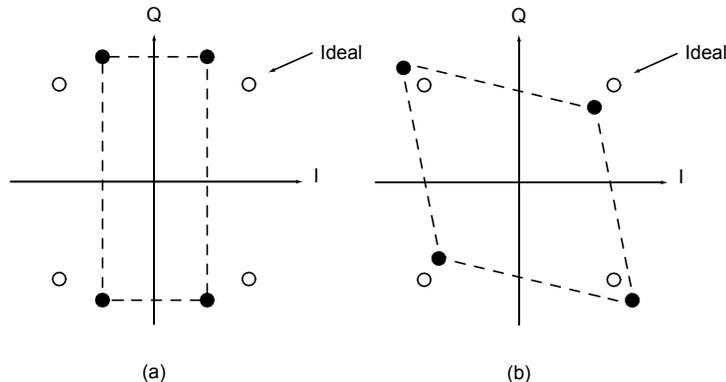


Figure 1.19: Effect of I/Q mismatch on signal constellation: (a) gain error, (b) phase error (after [13]).

ities non-zero, balanced circuitry is still extremely effective. The downside of this approach is the increased power consumption and die area required for essentially twice as much circuitry. For an LNA in particular, a differential topology requires two-times the power of its single-ended counterpart to achieve the same noise figure.

### I/Q Mismatch

The translation of the desired RF spectrum to DC mandates the use of quadrature down-conversion to recover the negative-frequency portion of the spectrum [77], [50]. Because the LO is at the same frequency as the RF, the negative-frequency spectrum, an equal but mirrored image of the desired spectrum, is also converted to DC, making it impossible to differentiate between the two spectra. Therefore, analog I/Q demodulation (which is subject to mismatches that lead to non-zero gain and phase imbalances as mentioned above in the context of image IRR) is necessary to properly receive the desired signal. These imbalances introduce distortions into the received I/Q constellation and result in an increased BER [78]. An example of distorted I/Q constellations is shown in Figure 1.19.

Figure 1.20 illustrates the use of quadrature downconversion in an ideal DCR to remove the negative frequency portion of the spectrum. Here, the I and Q branches are assumed to have perfect amplitude and phase balance and the system is assumed to be noise free. For the in-phase channel, which customarily denotes the side

multiplied by  $\cos(2\pi f_{LO}t)$ , an equal but mirrored image of the desired spectrum is centered at  $-f_{RF}$ ; after downconversion, this negative spectrum falls at DC on top of the desired signal. Without a quadrature channel, the resulting IF spectrum is a mixture of the two halves of bandwidth on either side of the LO, each half indistinguishable from the other, as in Figure 1.20(c.i). On the other hand, with an orthogonal quadrature channel, where the input signal is multiplied by  $\sin(2\pi f_{LO}t)$ , the negative frequency portion of the spectrum can be removed, as shown in Figure 1.20(d.i) or Figure 1.20(d.ii). The inset of Figure 1.20 shows how the I and Q channels interact to remove the image.

The  $90^\circ$  separation between the I and Q paths is typically accomplished in the LO path of the downconversion mixers, as shown in Figure 1.20<sup>6</sup>. Quadrature signals are generated with one of several different methods: *RC* polyphase filters [79], quadrature VCOs [80], divide-by-2 stages [81], and ring oscillators [82]. To remove the negative-frequency portion of the spectrum completely, the amplitude and balance of the I and Q branches must be perfect; otherwise, imbalances between either the I and Q amplitudes or the phase (or both) result in greater corruption of the desired signal by the negative frequency spectrum. Although all components in the receive path contribute to gain and phase errors, the balance of the LO is critical. Negative frequency rejection (NFR) is one way to characterize the effects of I/Q amplitude ( $\epsilon$ ) and phase ( $\Delta\phi$ ) imbalances. Given in dBc, the NFR for a receiver is approximately:

$$NFR \approx 10 \log(\epsilon^2 + \tan^2 \Delta\phi). \quad (1.22)$$

For an amplitude and phase imbalance of 0.1 dB and  $1^\circ$ , respectively, the associated NFR is  $\sim 35$  dBc. With careful design techniques, gain and phase imbalances can be minimized [83], [59]. Furthermore, since the imbalances tend to be static, digital (DSP) calibration and adaptation methods can be used to correct the mismatches [84]. A method for performing analog I/Q amplitude/phase correction in real-time is proposed in Chapter 6.

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<sup>6</sup>In certain instances, the shift is performed directly in the RF path, as in [72]. In this case, the receiver LO frequency is fed through a  $\times 2$  multiplier; while this doubles the frequency, it also doubles the phase-shift, changing a  $90^\circ$  phase change to  $180^\circ$ .

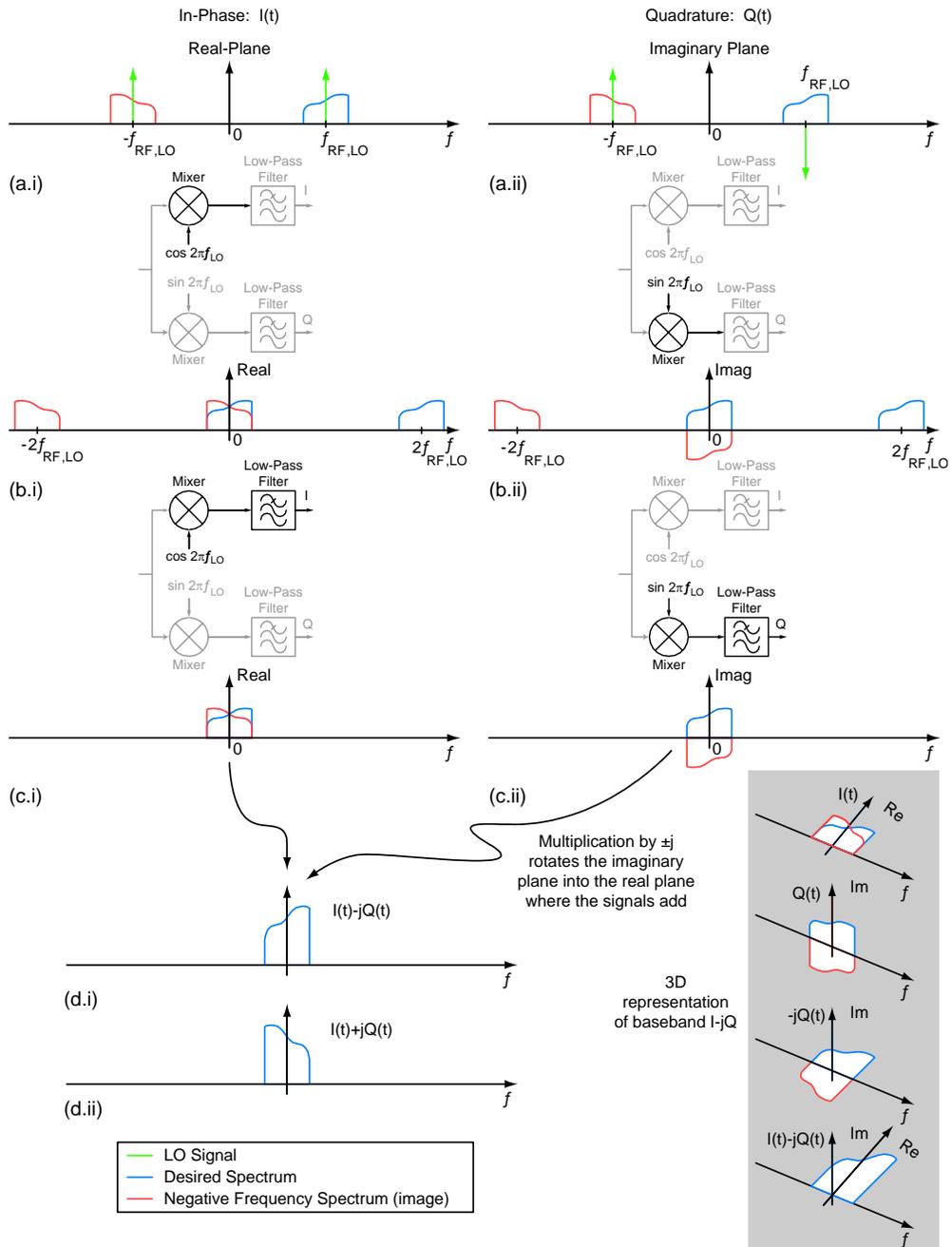


Figure 1.20: Illustration of quadrature down conversion and the removal of the negative "image" frequency. Note, only the magnitude of the spectrum is shown in the picture. Both magnitude and phase portions lead to the removal of the negative frequency components. Gain and phase imbalances result in less rejection of the negative frequency and increases in the BER.

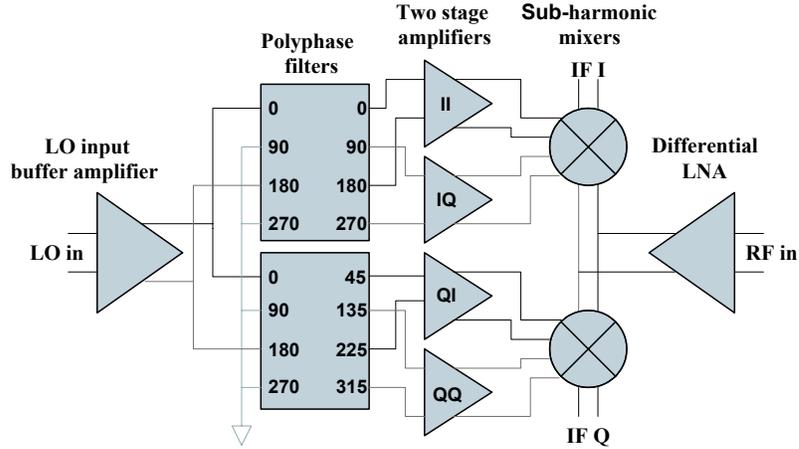


Figure 1.21: Block diagram of the receiver front-end.

## 1.4 Objectives and Overview

The objective of the research presented in this dissertation is the development of wireless receiver components in SiGe BiCMOS technology for use in high-speed wireless data networks. The first part of this work involves the design, fabrication, and testing of a 5–6 GHz sub-harmonic, direct-conversion receiver front-end, which was undertaken as a means to explore potential receiver architectures for SoC integration. The receiver front-end investigates the use of a sub-harmonic mixer — which performs frequency translation by mixing the desired input signal with an LO signal that operates at half the frequency of the input signal — as a potential solution to address the limited on-chip LO→RF isolation that can lead to unwanted DC-offsets in a direct-conversion receiver. Furthermore, the design is used to study the effects of limited isolation on the quadrature phase balance between the IF outputs. The receiver front-end includes two sub-harmonic mixers for quadrature (I and Q) down-conversion, a differential cascode LNA, and an LO conditioning chain, which splits the LO signal into the required eight different phases for quadrature sub-harmonic mixing. The design was implemented in the IBM SiGe 5HP 0.5  $\mu\text{m}$  BiCMOS process described in Section 1.2.3. Figure 1.21 shows the block of the receiver front-end.

This sub-harmonic DCR design is intended for high-speed wireless data networks, offering a highly-integrated, potentially low-cost solution. Although the DCR design is not specific to a particular standard, wireless high-speed data networks in general

require moderate sensitivities ( $\sim -60$ – $-80$  dBm) and high linearity. Furthermore, in order to achieve high-speed data transmission, these networks use complex digital modulation schemes, such as quadrature amplitude modulation (QAM), that are sensitive to I/Q mismatches and DC-offsets. Thus, the DCR design in this work addresses the needs of high-speed data networks by:

- providing sufficient noise figure to meet sensitivity requirements;
- using circuit techniques to improve the linearity ( $IIP_3$  and  $IIP_2$ ) of the receive chain components;
- minimizing I/Q phase and amplitude imbalances and maximizing the receiver negative frequency rejection;
- and enhancing LO $\rightarrow$ RF isolation to reduce or eliminate DC-offsets.

The results of the DCR work expose the need for a new method of quadrature LO signal generation, as the LO conditioning approach taken in the DCR design is sub-optimal due to excessive power consumption, a large die area, and limited bandwidth. Moreover, with this latter approach to quadrature generation, dynamically adjustable outputs, which can be used to tune the I/Q amplitude and phase balance at the IF outputs of the front-end, are not easy to implement. Thus, the second part of this work is the design, simulation, and layout of a phase-tunable/amplitude-tunable quadrature VCO (QVCO), implemented in the Freescale (formerly Motorola) SiGe:C HIP6WRF 0.18  $\mu\text{m}$  BiCMOS process (Section 1.2.4). The QVCO design is based on two differential *LC*-tank VCOs that, when appropriately cross-connected, are forced to lock to each other at the same frequency and oscillate in quadrature. This method of quadrature synthesis is chosen over other possible schemes due to its use of the common *LC*-tank VCO, which has been extensively researched and optimized for IC applications. Two different proposed QVCO designs (block diagrams of which are shown in Figure 1.22) offer two different methods for dynamically adjusting the output quadrature phase balance.

The proposed QVCO has a number of applications in high-speed data networks. For example, a dynamically tunable QVCO can be used in a wireless receiver to eliminate I/Q phase and amplitude imbalances (in near real-time) as a means to improve signal *SNR* at the ADCs (which in turn improves the BER of the received data), and

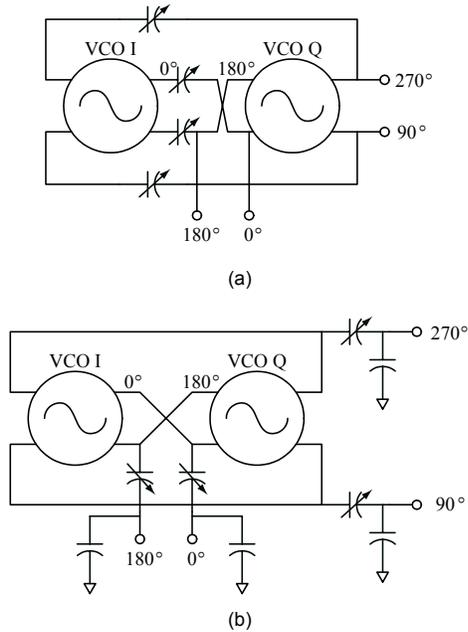


Figure 1.22: Block diagrams of the two proposed methods for providing phase-tunable outputs from a quadrature VCO.

to eliminate inter-channel interference (ICI) in systems using, for example, orthogonal frequency-division multiplexing (OFDM). The phase and amplitude tunability of the QVCO can also be used on the transmitter-side to correct I/Q imbalances within the modulation chain that directly affect the error vector magnitude (EVM)<sup>7</sup> of the transmitted signal, particularly at low power levels [85, 86]. For high-speed wireless networks, very low EVMs are required to achieve reliable, high data-rate transmissions.

From the designs of both the QVCO and the sub-harmonic DCR, the need for high- $Q$ , on-chip inductors emerges as a critical aspect of integrated circuit design. Therefore, the final aspect of this work is the in-depth investigation of one method, proposed in the literature, for improving the peak- $Q$  of integrated inductor structures: the insertion of a patterned ground shield between the inductor coil and the underlying substrate. As shown in Figure 1.23, a 5 mm  $\times$  5 mm reticle was designed in the Freescale SiGe:C HIP6WRF 0.18  $\mu$ m BiCMOS process (Section 1.2.4) to include

<sup>7</sup>Error vector magnitude is typically used to characterize the modulation accuracy of a transmitter. It is a measure of the root-mean-square error between an ideal modulated waveform and the actual (measured) waveform that is transmitted or received.

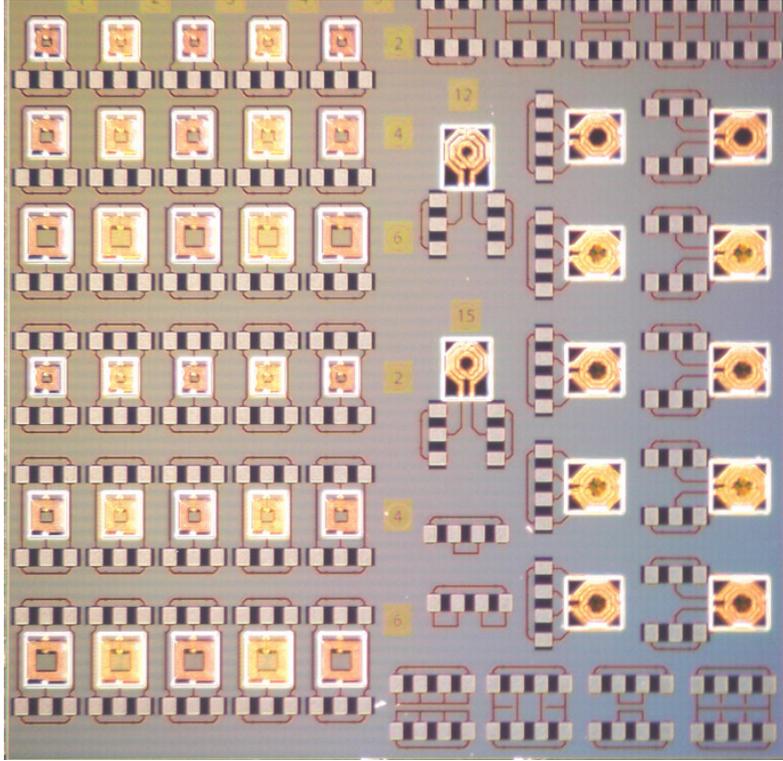


Figure 1.23: Photograph of the fabricated 5 mm  $\times$  5 mm reticle containing the patterned ground shield inductor experiment.

inductors of various values — in both a one-port and two-port measurement configuration — with different types of ground shields. From the measured results, a scalable, lumped-element model is developed to allow quick simulation of the pattern ground shield effects during the design phase of a circuit, thereby eliminating the need for computationally-demanding, full-wave electromagnetic (EM) simulators.

Since the phase noise of a transceiver VCO can have negative effects on high-speed transmission of data (particularly for systems using OFDM [87,88]) and since inductor quality factor has a large impact on the phase noise of  $LC$ -tank VCOs, the results of the inductor effort, including the measured improvement in inductor  $Q$ , can greatly improve the performance of wireless high-speed data networks.

This chapter has introduced background information on the motivation for designing highly integrated wireless receiver components. The remainder of this dissertation is organized as follows:

- Chapter 2 introduces the concept of sub-harmonic mixing and describes the design and simulation of the standalone mixer circuit, which was implemented with two different LO conditioning chains.
- Chapter 3 presents the fabrication, test plan, and measured results for these two standalone mixer designs.
- Chapter 4 describes the design and simulation of the DCR front-end and includes the design details of the cascode LNA and its incorporation with the sub-harmonic mixers of the previous two chapters.
- Chapter 5 presents the fabrication and measured results for the RF receiver front-end.
- Chapter 6 discusses the limitations of the quadrature generation scheme used in the front-end, presents other possible methods for quadrature generation, and presents the design and simulations of two proposed phase-tunable QVCOs. Methods for measuring the phase and amplitude balance of these QVCOs and potential applications of the circuit in modern receiver architectures are also presented.
- Chapter 7 presents the measured results of the pattern ground shield inductor experiment and the achievable improvement in inductor  $Q$ . A *scalable* lumped element model that closely matches the measured results is proposed.
- Chapter 8 offers conclusions on this work and proposes future directions based on the results of the presented designs.

# Chapter 2

## 5-6 GHz $\times 2$ Sub-Harmonic Mixer Design and Simulation

**A**S discussed in the previous chapter, sub-harmonic mixing is a potential approach that can reduce or eliminate unwanted DC-offsets in direct-conversion (zero-IF) receivers. This chapter introduces the concept of sub-harmonic mixing and presents the design and simulation of the active sub-harmonic mixer used in the proposed DCR front-end. Details on the LO conditioning chain required for the sub-harmonic mixing process are also covered. Two different LO chain designs are presented: (1) a fully differential design with differential LO input; and (2) a design incorporating single-ended to differential conversion of the LO input on-chip.

### 2.1 Sub-harmonic Mixing

The intermediate frequency resulting from a mixing process as given by Equation 1.7 is a specific case known as fundamental mixing, i.e. the IF is equal to the magnitude of the frequency difference between the RF and LO signals. However, in general, the mixing process can be described by

$$f_{IF} = |m \cdot f_{RF} \pm n \cdot f_{LO}|, \quad (2.1)$$

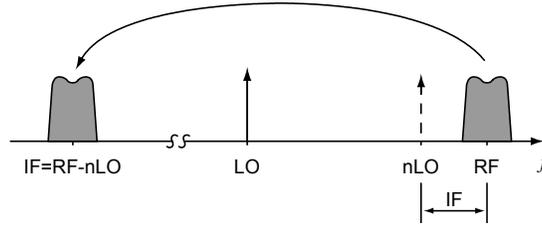


Figure 2.1: Illustration of sub-harmonic mixing. The RF is translated to an IF by mixing with an integer multiple ( $n$ ) of the LO.

where  $m$  and  $n$  are harmonic multipliers of  $f_{RF}$  and  $f_{LO}$ , respectively. In this equation, the subtraction represents downconversion mixing. Equation 2.1 shows that any combination of harmonics (e.g.  $m$  and/or  $n$  greater than 1) of the RF and LO signals results in a mixing product; these products represent the *spurious response* of the mixer. In general, such higher-order mixing products are unwanted and must be reduced or eliminated through appropriate channel selection filtering and/or the choice of the RF, LO, and IF frequencies [89].

However, intentionally mixing the RF with a harmonic of the LO ( $n > 1$ ) can in fact be desirable. Giving an IF at  $|f_{RF} - n \cdot f_{LO}|$ , such harmonic mixing uses a higher-order LO harmonic instead of the fundamental LO frequency. More specifically, the term *sub-harmonic* mixing describes when the fundamental LO signal is an integer fraction of the RF frequency while *super-harmonic* mixing describes when the LO is an integer multiple of the RF frequency. Figure 2.1 shows the translation of an RF spectrum to an arbitrary IF through sub-harmonic mixing.

Sub-harmonic mixing has a number of appealing advantages over fundamental mixing, particularly for direct-conversion applications. With the LO at a fraction of the RF frequency, the RF port of the mixer is less responsive to the LO frequency, which means higher LO→RF isolation can in principle be achieved. As described in Section 1.3.3, increasing LO-RF isolation — i.e. reducing LO leakage to the RF input of the mixer/LNA — is necessary for reducing LO self-mixing and the resulting unwanted DC-offsets [90]. Sub-harmonic mixing also relaxes the requirements of the VCO and frequency synthesizer, which generate the LO signal. Given the lower fundamental LO frequency, higher performance and lower cost VCOs can be implemented, especially for millimeter wave applications. In addition, VCO pulling, whereby the

oscillator injection-locks to an interfering signal leaking through the RF port causes the center frequency of the VCO to shift, is also mitigated by the RF→LO isolation achieved with sub-harmonic mixing. The use of even-harmonic mixing (where  $n$  is an even integer) strongly attenuates second order mixing products, which is also important for direct-conversion receivers [91]. Incidentally for U-NII band DCR applications, using the second harmonic ( $n = 2$ ,  $f_{LO} = \frac{1}{2}f_{RF}$ ) allows for the use of existing VCOs and frequency synthesizers designed for the 2.4 GHz ISM band [92].

Passive mixers using anti-parallel diode pairs (APDP), diode rings, and resistive pseudomorphic high-electron mobility transistors (PHEMTs) have been reported in [93–97] while active mixers have been explored in [98–102]. Active mixing is very attractive for direct-conversion receivers since the LNA and mixer are potentially the only gain blocks prior to translation of the information to baseband. In order to overcome the noise generated by baseband processing, the RF front-end must provide at least 25–30 dB of gain; therefore, active mixers are appealing since they provide conversion *gain*, decreasing the demands on the LNA design. However, the benefit of additional gain from active mixing comes at the expense of linearity and power consumption. In this dissertation research, an active sub-harmonic mixer is employed for the direct-conversion receiver front-end to mitigate LO leakage while providing conversion gain.

## 2.2 Sub-Harmonic Mixer Design

### 2.2.1 Topology

The active sub-harmonic mixer (SHM) topology used in this work is an extension of the design originally published in [103] and modified in [92], [104]. The design is based on the well-known “Gilbert cell”, an active, double-balanced mixer that offers a number of important advantages for integrated circuit design, including: conversion gain, low LO drive level, good port-to-port isolation, and minimal requirements for impedance matching [105]. A simplified schematic of the standard Gilbert cell mixer is shown in Figure 2.2.

The Gilbert cell is a current-mode circuit, where state variables and circuit function

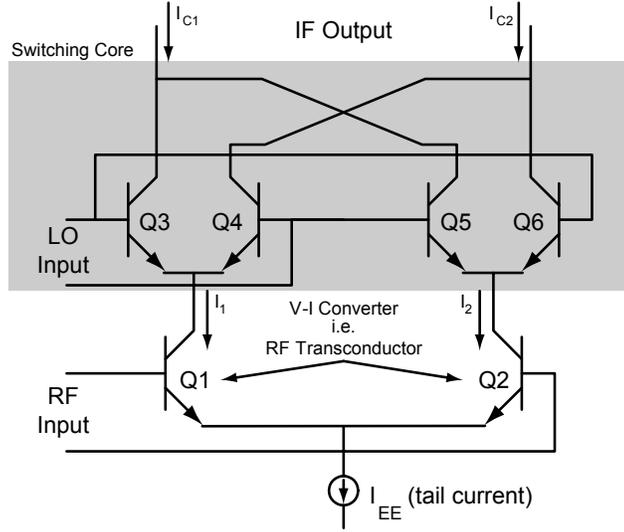


Figure 2.2: Simplified schematic of the Gilbert cell mixer.

are determined by current flow [106]. The input RF voltage is applied to the bases of transistors  $Q1$  and  $Q2$ , which convert the voltage into a current at the transistor collectors ( $I_1$  and  $I_2$  in Figure 2.2). These currents, in turn, are directed by the switching transistors  $Q3$  through  $Q6$ , which, assuming the LO signal is sufficiently large, act as current-steering switches and determine the current at the IF output. This output current is usually converted back to a voltage by a load impedance, thus realizing an RF to IF voltage (or power) conversion gain [105]. The term "double-balanced" indicates that both the RF and LO signals are applied differentially. The fully differential and symmetric nature of the structure results in high port-to-port isolation and a reduction in second order effects.

As described in [100], an additional set of switching transistors can be stacked above the standard Gilbert cell switching core, such that when the LO signal is applied in quadrature, sub-harmonic mixing can be obtained. The mixer operates essentially as a three stage analog multiplier giving the following output:

$$v_{out}(t) = v_{RF}(t) \cdot v_{LOI}(t) \cdot v_{LOQ}(t) \quad (2.2)$$

where  $v_{LOI}(t)$  and  $v_{LOQ}(t)$  represent the quadrature LO signal. The stacked switching core acts analogously to an exclusive-OR, switching the RF current ( $I_1/I_2$ ) at a frequency effectively twice the LO frequency ( $LO_I \cdot LO_Q = 2LO$ ). Figure 2.3 shows the

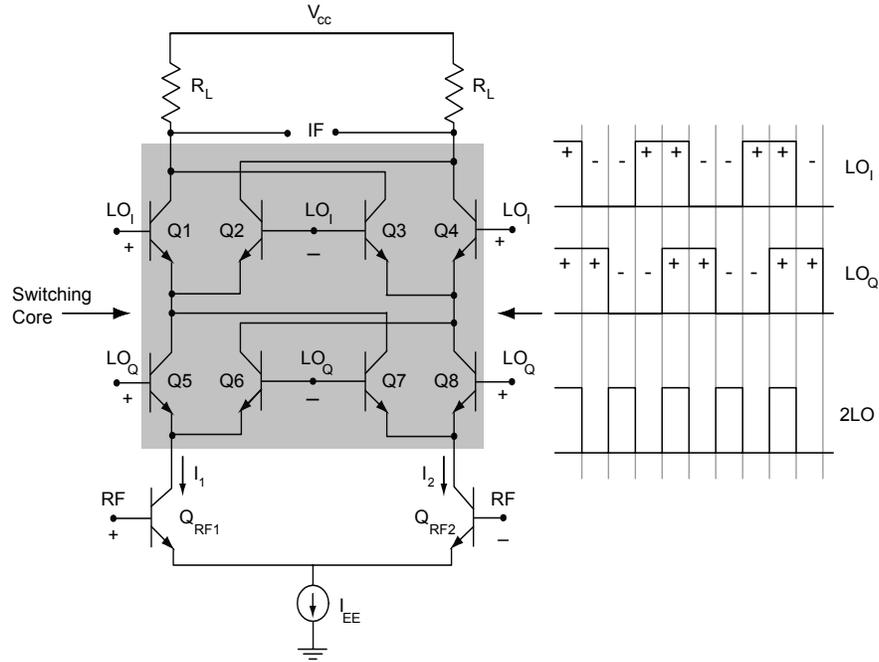


Figure 2.3: Simplified schematic of the  $\times 2$  sub-harmonic mixer. Generation of the 2LO component from quadrature signals is shown to the right of the circuit.

simplified schematic of the active sub-harmonic mixer and illustrates how the 2LO component is generated from the two quadrature waveforms. While the absolute phase of the LO signal is arbitrary, the relative  $90^\circ$  phase between the switching core LO inputs results in the sub-harmonic mixing. However, as shown in [100], the duty cycle of the quadrature LO is more important than the actual  $90^\circ$  phase relationship, giving some margin for error in the quadrature LO signal generation. For the purposes of discussion, the phases of the LO signal applied to the switching core of Figure 2.3 are labeled as follows:  $LO_{I+} = 0^\circ$ ,  $LO_{Q+} = 90^\circ$ ,  $LO_{I-} = 180^\circ$ , and  $LO_{Q-} = 270^\circ$ .

The ability to provide conversion gain while requiring relatively low LO power levels is one of the key advantages to the Gilbert cell mixer. This methodology of sub-harmonic mixing is a departure from the classical passive sub-harmonic mixer used at millimeter-wave frequencies. Traditionally, passive sub-harmonic mixing is performed using a nonlinear device with an antisymmetric current-voltage characteristic, where the device is driven by a large LO signal to generate higher harmonics of the LO frequency for multiplication with the RF [107].

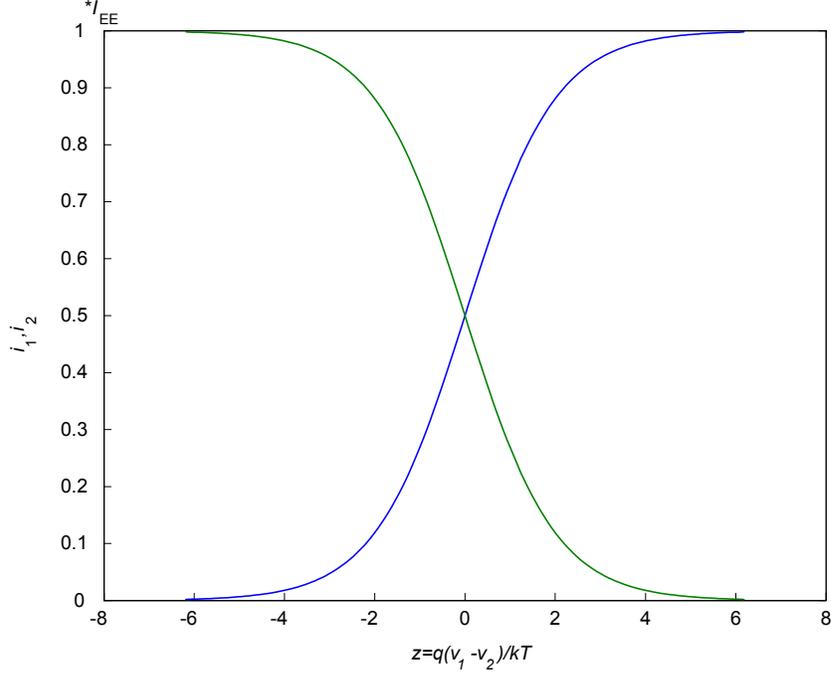


Figure 2.4: Output current at each collector of a differential pair for different input drive levels  $z$ . For  $z < -6V_T$  and  $z > 6V_T$ , the differential pair transistors swing between the cutoff and saturation regions of transistor operation.

The collector currents of an ideal differential pair are given by [76]

$$\begin{aligned} i_1 &= \frac{I_{EE}}{2} \left[ 1 + \tanh\left(\frac{z}{2}\right) \right] \\ i_2 &= \frac{I_{EE}}{2} \left[ 1 - \tanh\left(\frac{z}{2}\right) \right] \end{aligned} \quad (2.3)$$

where  $z = q(v_1 - v_2)/kT = (v_1 - v_2)/V_T$  and  $v_1 - v_2$  represents the differential input signal. As shown in Figure 2.3, the output current of the differential pair is centered around the DC bias current and saturates for an input voltage of  $\sim \pm 6V_T$ . Therefore, relatively low LO signal swings ( $160 \text{ mV}_{p,min}$ ) are necessary to turn the switching core transistors off and on; however, the LO is typically generated with a VCO, which provides a sinusoidal signal. As a result, during the interval of  $-6V_T < v_{LO} < 6V_T$  both transistors of the differential pair are turned on, leading to mixer nonlinearities [13], an increase in LO $\rightarrow$ IF feedthrough [108], and a degradation in noise performance [58], [109].

## 2.2.2 Mixer Design

A significant drawback to the stacked switching core shown in Figure 2.3 is the reduction in voltage headroom. Applying Kirchoff's voltage law to one branch of the mixer (assuming the other branch is turned off), the total voltage for that branch can be found in terms of the bias current  $I_{EE}$ , to be:

$$V_{CC} = \alpha I_{EE} R_L + V_{CE_I} + V_{CE_Q} + V_{CE_{RF}} + I_{EE} R_{EE}. \quad (2.4)$$

Since the LO signal is a sinusoid and not a perfect square wave, transistors  $Q_1 - Q_8$  operate in the active region during the zero crossings of their respective LO signals. During these transition times, assuming a 3.3 V supply and a nominal 1 V drop for each  $V_{CE}$ , the design leaves only 0.3 V to split between the collector load resistors and the bias circuitry. This insufficient headroom can lead to gain compression, strong nonlinearities, and/or incorrect operation of the circuit due to improper biasing.

One method for improving the headroom is to replace the load resistors with load inductors. The inductors are essentially short circuits at DC and largely remove the  $\alpha I_{EE} R_L$  term from Equation 2.4, which relieves the limited headroom. Unfortunately, the lack of small-footprint monolithic inductors in the 5HP process renders this solution unfavorable. While some inductance can be harvested from the parasitics associated with package bondwires, this inductance is too small to provide an adequate load impedance alone.

An alternative method, as demonstrated in [92], is to bias the RF transconductor in parallel with the LO switching stage and AC coupling the two sections together with on-chip capacitors. Though the power consumption increases, since the current is no longer shared between the two stages (as in Figure 2.3), significant gains in voltage headroom are obtained since the parallel bias scheme allows both the RF and the LO sections to operate from the full supply rail. Figure 2.5 shows the simplified schematic of the parallel-biased sub-harmonic mixer. Note that the design shown is implemented using SiGe HBTs only.

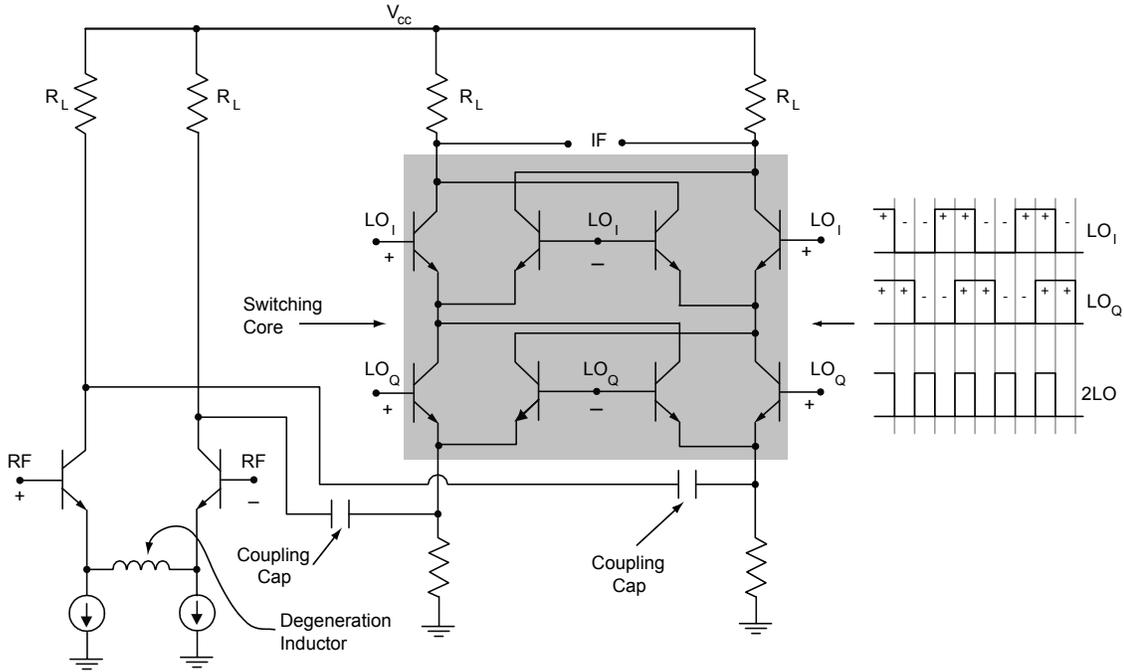


Figure 2.5: Simplified schematic of the parallel-biased sub-harmonic mixer.

### LO Switching Core

To further ease the headroom limitation, the current through the switching core is set with resistors rather than a tail current source. Resistors require only hundreds of millivolts to fix the emitter current, which leaves the majority of the headroom for the remaining three voltage drops. In this form, the mixer circuit can be regarded as a differential RF pre-amplifier driving a double-stacked Gilbert cell mixer with a resistive RF stage [92]. Unfortunately, the additional headroom gained from the resistive bias comes at the expense of conversion gain, isolation, and noise. Another option to increase headroom is to replace these resistors with inductors, which provide additional voltage headroom due to the lack of a DC voltage drop. However, on-chip inductors of a practical size present a low impedance between the cross-coupled transistor emitters and ground, which results in inferior isolation and poor common mode rejection (manifested in more severe second order nonlinearities) [110]. The required surface area for the inductor implementation and the difficulty in establishing a fixed tail current also restrict this scheme. Perhaps the best approach is to set the bias current of the switching core with a current mirror, particularly one

that incorporates low-threshold voltage ( $V_t$ ) NMOS transistors. With low-threshold voltage devices, the required voltage drop ( $V_{DS}$ ) for proper current mirror operation has approximately the same impact on voltage headroom as the resistor-based approach, but the mirror provides better isolation and, since the output resistance of the mirror is significantly greater than the maximum possible resistance-values in the resistor-based approach, better linearity [110]. However, this mixer is designed in a first generation SiGe BiCMOS process where low-threshold voltage devices are not available. Therefore, an NMOS-mirror approach would have the same headroom restrictions as the original stacked core, picture in Figure 2.3.

The emitter currents  $i_{EE_1}$  and  $i_{EE_2}$ , which represent the total (AC + DC) current through each emitter, can be approximated as:

$$i_{EE_1} = i_{ee_1} + I_{EE_1} \approx \frac{v_{rf} \sin \omega_{rf} t}{Z_{out,tran} + Z_{in}} + \frac{V_{E_1}}{R_{E_1}} \quad (2.5)$$

$$i_{EE_2} = i_{ee_2} + I_{EE_2} \approx \frac{v_{rf} \sin \omega_{rf} t}{Z_{out,tran} + Z_{in}} + \frac{V_{E_2}}{R_{E_2}} \quad (2.6)$$

where the first term is the AC current and the second term is the DC,  $Z_{out,tran}$  is the output impedance of the RF transconductor stage, and  $Z_{in}$  is the input impedance looking into the emitters of the switching core. Assuming the DC current gain ( $\beta$ ) approaches infinity (i.e.  $\alpha = 1$ ,  $i_C = i_E$ ) while neglecting higher-order harmonics/mixing products, the IF output voltage can be approximated by:

$$v_{IF} \approx (i_{EE_1} - i_{EE_2}) \cdot R_L \cdot v_{LO_I} \cdot v_{LO_Q} \quad (2.7)$$

$$v_{IF} \approx \text{DC}_{bias \text{ current}} + \left(\frac{4}{\pi}\right)^2 \frac{v_{RF} v_{LO_I} v_{LO_Q} R_L}{2(Z_{out,tran} + Z_{in})} [\cos(\omega_{rf} - 2\omega_{LO}) + \cos(\omega_{rf} + 2\omega_{LO})]$$

where the simplification is based on the assumption that the LO is a square wave (with  $\pm v_{LO_I}$  and  $\pm v_{LO_Q}$  peak-to-peak voltages) that simply steers the RF signal between the two sides. This square wave is represented in the equation by the Fourier series approximation  $v_{LO} = [1 + \frac{4}{\pi} \cos(\omega_{LO} t) + \frac{4}{3\pi} \cos(3\omega_{LO} t) + \dots]$ , with the higher-order terms ( $n \geq 3$ ) neglected. Equation 2.7 shows that the load resistors ( $R_L$ ) impact the conversion gain directly. With the extra headroom obtained from resistor biasing of the switching core, the value of  $R_L$  can be increased and consequently, higher conversion gains can be achieved. Providing for some additional margin for  $V_{CE_I}$  and

$V_{CEQ}$ ,  $R_L$  values of  $1.5\text{ k}\Omega$  are found to be the maximum working value. Assuming that the impedance looking into the collectors is significantly higher than  $R_L$ , the IF output impedance of the mixer is roughly  $1.5\text{ k}\Omega$  single-ended, or  $3\text{ k}\Omega$  differential. However, as will be discussed later, this high output impedance has a direct impact on the measurements in a  $50\ \Omega$  system.

## RF Transconductor

The RF transconductor is simply a differential amplifier stage responsible for converting the RF input voltage to a current for subsequent mixing with the LO. The design of the RF transconductor stage is similar to the design of any RF differential amplifier, consisting of tradeoffs between linearity, gain, power consumption, noise, and input matching. In the case of the RF transconductor design presented here, higher linearity is achieved at the expense of lower conversion gain and higher noise. As opposed to noise figure in a cascaded system, linearity is determined by the latter stages in the chain, not the first. Therefore, the linearity of the mixer is extremely important as it appears further along in the receive chain. The lower gain and higher noise that results can be compensated for with the design of the preceding LNA. Thus, this tradeoff is made to improve the performance of the overall receiver.

One method for addressing linearity in the transconductor is to apply the multi-*tanh* approach to the differential input [111]. This method uses several parallel-connected differential pairs of varying emitter areas to flatten the overall transconductance versus the input voltage transfer function. The multi-*tanh* name arises from the hyperbolic tangent relationship between the differential pair input voltage and its output current (Equation 2.3). While this method is applied in [100] with success in extending the mixer linear range, it comes at the cost of higher noise figure and greater power consumption. The input of a multi-*tanh* circuit also includes more parasitic capacitance, making it difficult to match at 5–6 GHz, particularly to a  $100\ \Omega$  differential source impedance [92].

Another option for increasing the linearity of the differential pair is emitter degeneration. The negative feedback provided by placing an impedance between the emitter of a transistor and the AC ground reduces the overall input voltage to the transistors, which increases the linearity [105]. The feedback is a result of the transistor

output current passing through the degenerative impedance and producing a voltage at the transistor emitter. This emitter voltage is subtracted directly from the input voltage at the transistor base, reducing  $v_{be}$  and keeping the device in the linear regime ( $v_{be} = v_{in} - v_e$ , where  $v_e$  is the voltage across the degenerative component) over a larger range. The downside of emitter degeneration is degraded noise and gain performance.

While resistors are often used for degeneration to save chip area, it is beneficial to use inductors when possible. Inductive degeneration contributes less noise compared to resistors and does not affect DC voltage headroom. Furthermore, inductive degeneration directly impacts the input match, helping to resonate out the parasitic base-emitter junction capacitance  $C_{be}$  ( $C_\pi$ ) while simultaneously setting the real part of the input impedance [13]. Figure 2.6(a) shows an inductively degenerated differential pair. One inductor and two tail current sources are employed, rather than the typical two inductors (one in each emitter) with one current source between them, to minimize inductor parasitics and to reduce overall die area. This approach is less than ideal however since the output impedance of the tail current source is effectively cut in half with the two current mirror transistors in parallel; with the tail current source split between multiple transistors, this approach is also more susceptible to device mismatches. Furthermore, the two-port inductors available for this design are not perfectly symmetric<sup>1</sup>. These drawbacks together reduce the balance and symmetry of the circuit, which in turn degrades the rejection of common-mode signals and results in greater second order nonlinearities.

Circuit symmetry simplifies analysis since the circuit can be split in half at the plane of symmetry, where a virtual ground ideally exists, and each portion can be analyzed separately following the principle of superposition. Figure 2.6(b) shows the small signal circuit model for one transistor from which the single-ended  $Z_{in}$  can be calculated. Neglecting  $r_\pi$  (since it is  $\lesssim 100 \Omega$  at the transconductor bias current) and  $C_{be}$  ( $C_\mu$ ) (since including it complicates the analysis, but does not affect the end result), the single-ended input impedance can be written as:

$$Z_{in} = \frac{v_{in}}{i_b} = r_b + \frac{g_m L_e}{C_{be}} + j\omega L_e + \frac{1}{j\omega C_{be}} \quad (2.8)$$

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<sup>1</sup>A three-port, symmetric inductor can be used instead to resolve the limitations in die area and remove the need to split the tail current source [112]. This topic will be addressed in Chapter 7.

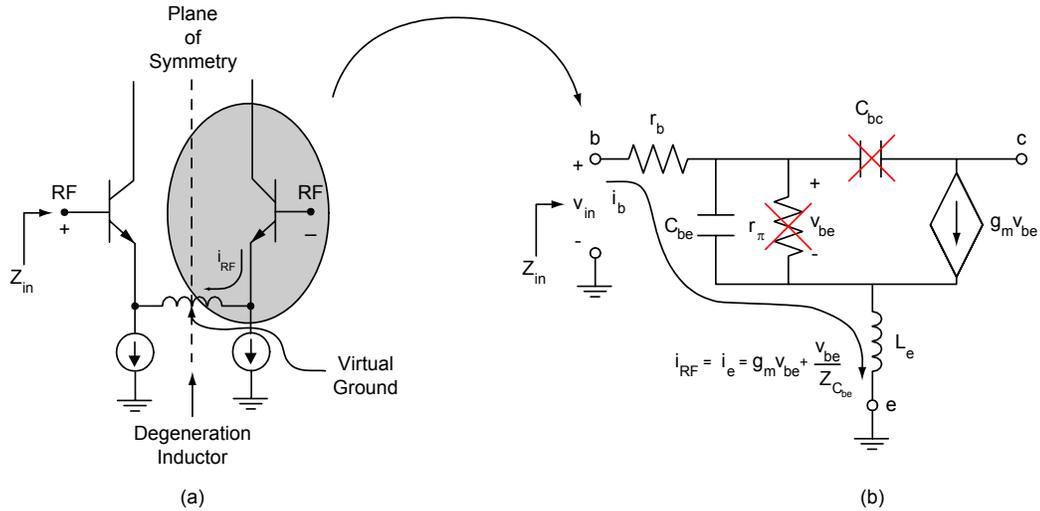


Figure 2.6: Illustration of inductive emitter degeneration: (a) differential pair with single inductor degeneration, (b) by symmetry, analysis of small signal model for one transistor to find  $Z_{in}$ . The "Xs" show components neglected.

The first two terms set the real part of the input impedance while the last two imaginary terms are designed to cancel each other. The differential input impedance, neglecting any device mismatch, is twice this value. Therefore, the use of inductive degeneration affords an increase in linearity *and* an extra degree of freedom in setting the input impedance. Each transistor in the RF transconductor pair is sized to  $25 \mu\text{m} \times 0.5 \mu\text{m} \times 2$ , providing a fair size to handle relatively large inputs. The choice of the value of  $L_e$  is described later in Section 4.1.2.

## Mixer Biasing

Current mirrors are basic elements in analog/RF integrated circuit design. Mirrors, used for both biasing and active loading, provide isolation from variations in the power supply and lend insensitivity to temperature changes in a simple, compact form [76]. The basic bipolar current mirror is shown in 2.7(a) and consists of an input (or reference) current  $I_{ref}$  and one or more output currents, shown in the figure as  $I_{C_4}$  and  $I_{C_5}$ . The gain of the mirror is defined as  $I_{out}/I_{in} = I_{C_n}/I_{ref}$  (where  $n$  represents the mirror outputs; in this case,  $n = 4$  or  $5$  for transistors  $Q_4$  and  $Q_5$ ) and is ideally unity if the emitter areas of transistors  $Q_1$ ,  $Q_4$ , and  $Q_5$  are identical; if the

emitter area of  $Q_4$  or  $Q_5$  is different from  $Q_1$  then the current gain is a function of the ratio of the two areas,  $I_{out}/I_{in} = A_n I_{C_n}/A_{ref} I_{ref}$ . Ideally, the output current of the mirror equals the input (reference) current multiplied by this gain term.

The current through the RF transconductor stage is set using an HBT current mirror. Figure 2.7(b) shows the bias circuitry for the RF transconductor. Transistors  $Q_1$  and  $Q_2$  (each  $2\ \mu\text{m} \times 0.5\ \mu\text{m}$ ) and resistor  $R_{bias}$  form the reference circuit and set the input current of the mirror. Transistors  $Q_4$  and  $Q_5$  are sized to have an emitter area that is 2.5 times the size of  $Q_1$ , or  $5\ \mu\text{m} \times 0.5\ \mu\text{m}$ , which allows less total current (0.42 mA) to be drawn through the reference section while providing 1.35 mA of current to each half of the transconductor pair (2.7 mA total)<sup>2</sup>. The third mirror transistor  $Q_3$  supplies the bias voltage to the bases of the RF transistors by drawing current through  $R_{base}$ , which sets the voltage at the collector of  $Q_3$ . This voltage is applied to the bases of the RF transconductor through large value resistors ( $R_{BB_1}$  and  $R_{BB_2}$ ). These base resistors present a high impedance to the RF signal — thereby providing isolation from the DC path — while a large capacitor ( $C_1$ ) is placed on the DC side of the resistors to provide an AC ground to any RF signal that leaks through.  $Q_3$  is identical in size to  $Q_1$  and  $Q_2$  and consumes 0.4 mA total.

To improve the performance of the bipolar current mirror, the emitters of the mirror devices are resistively degenerated. Degeneration serves two purposes in a bipolar current mirror. First, the resistors improve the matching between the input current  $I_{ref}$  and the output currents  $I_{C_3}$ ,  $I_{C_4}$ , and  $I_{C_5}$ , and second, the resistors improve the output impedance of the current mirror [76]. This latter aspect enhances the balance of the circuit by forcing a virtual ground at the plane of symmetry, which in turn improves the common mode rejection. The resistors also provide a means to limit the current without adjusting the mirror area ratio. Notably, if the mirror is implemented with MOS devices, degeneration resistors are not required since the adjustment of output impedance in a MOS mirror is a simple matter of increasing the overall gate length while keeping the ratio of channel width to channel length ( $W/L$ )

---

<sup>2</sup>It should be noted that the bias current  $I_C$  of 1.35 mA is significantly less than the bias current for peak  $f_T$  in a device with a size of  $25\ \mu\text{m} \times 0.5\ \mu\text{m} \times 2$ , where the peak  $f_T$  occurs at a current of tens of milliamps. The order of magnitude difference in collector current suggests that the transistor is biased well below peak  $f_T$ , thereby limiting the gain and bandwidth of the transconductor stage. At the time of design, a device capable of handling large input power seemed necessary and thus, a lower  $f_T$  was deemed acceptable. In retrospect however, this decision was in error; the device should have been resized to maximize  $f_T$  at a similarly low current level.

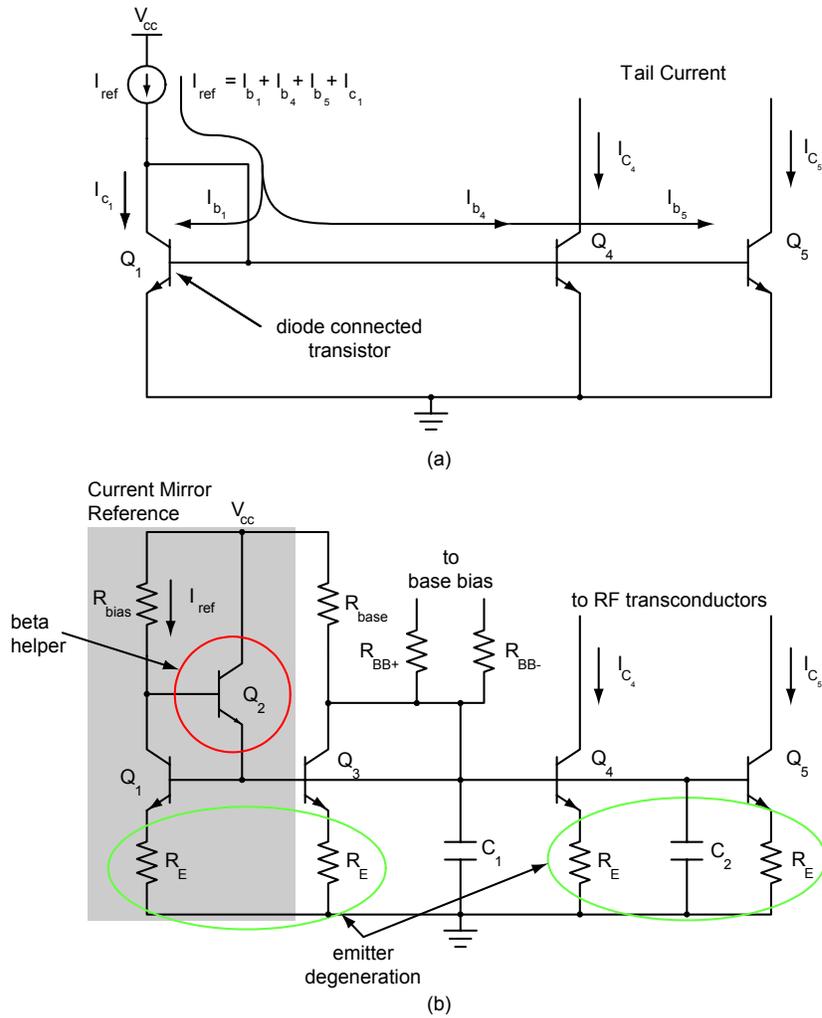


Figure 2.7: Current mirror circuits: (a) a simple current mirror with emitter degeneration; (b) the schematic of RF transconductor biasing. The same biasing scheme shown here is used in the other active circuits of the RF front-end.

constant [76].

The resistor  $R_{bias}$  in Figure 2.7(b) essentially provides the reference current  $I_{ref}$  shown as a current source in Figure 2.7(a). For an ideal mirror, the base currents of the bipolar transistors would be negligible, the current gain ( $\beta$ ) of each device would be infinite, and the reference current through  $R_{bias}$  and the collector current  $I_{C_1}$  through the reference transistor would be equal. However, in a real bipolar device, the base current is non-zero and  $\beta$  is finite, which can lead to substantial errors in the current mirror ratio, particularly if the mirror has multiple outputs as shown in Figure 2.7(b). For the mirror with a diode-connected reference transistor [Figure 2.7(a)], the base currents of transistors  $Q_1$ ,  $Q_4$ , and  $Q_5$  are supplied by  $I_{ref}$ , which means the total collector current of  $Q_1$  cannot be equal to  $I_{ref}$ . This mismatch between  $I_{C_1}$  and  $I_{ref}$  results in gain errors proportional to  $1/\beta$  (as shown in Equation 2.9) and inexact mirroring [76].

$$\frac{I_{C_1}}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta}} \quad (2.9)$$

To reduce the current draw on  $I_{ref}$ ,  $Q_2$  is added in place of the diode connection [Figure 2.7(b)]. With this minor modification, the emitter of  $Q_2$  supplies the base current to transistors  $Q_1$ ,  $Q_3$ ,  $Q_4$ , and  $Q_5$ , and as a result, resistor  $R_{bias}$  only supplies the small base current to  $Q_2$  beyond the desired reference current of the mirror. Transistor  $Q_2$  is often referred to as the "beta-helper" since it helps reduce the effects of finite  $\beta$ . The inclusion of  $Q_2$  reduces the gain error to an  $\sim 1/\beta^2$  dependence [113] as shown in Equation 2.10:

$$\begin{aligned} \frac{I_{C_1}}{I_{ref}} &= \frac{1}{1 + \frac{2}{\beta(\beta+1)}} \\ &\cong \frac{1}{1 + \frac{2}{\beta^2}}, \text{ if } \beta \gg 1 \end{aligned} \quad (2.10)$$

## Mixer Grounding and DC Supply

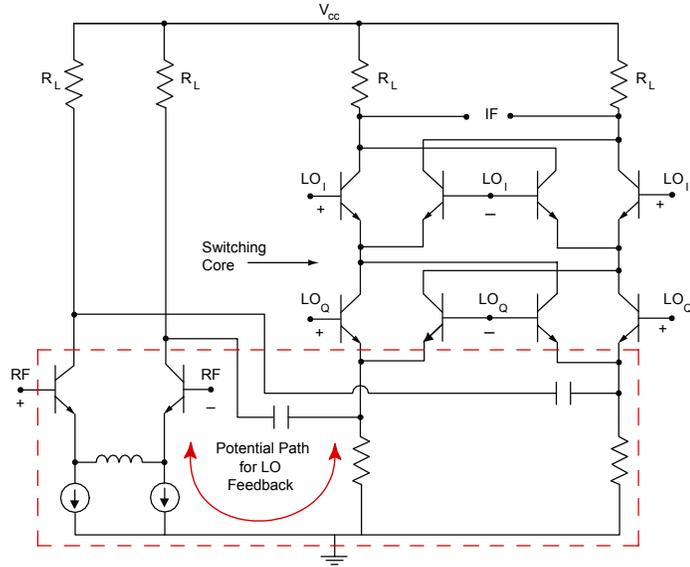
In the original sub-harmonic mixer design of [92], the LO and RF sections are connected together through a common ground point as illustrated in Figure 2.8(a). Due to parasitics at the frequency of interest and the low resistivity of the substrate, the potential at the common point on-chip may not necessarily be zero as expected; thus,

a feedback path between the LO and RF sections that effectively reduces the desired LO/RF isolation could exist. To increase the isolation, which is critical for DCR applications, the ground node is separated into two different nets, with a unique ground connection for the LO section and another for the RF. The isolated sections are shown in Figure 2.8(b).

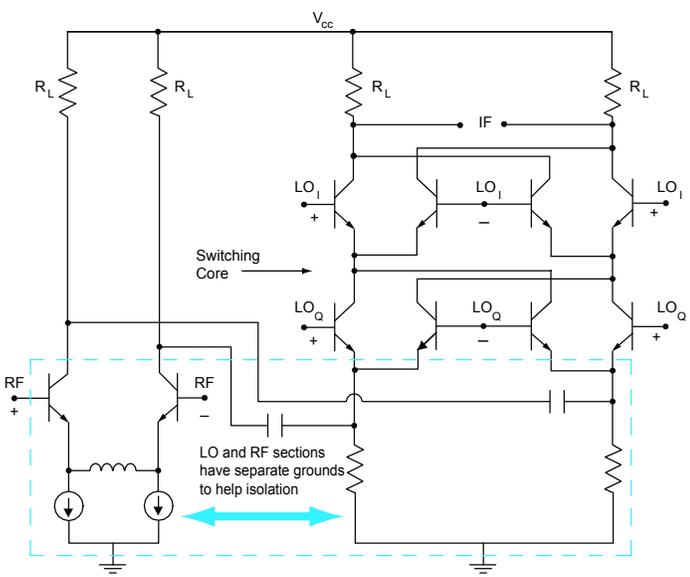
The full mixer Cadence schematic is shown in Figure 2.9. The DC supply rail is divided into two separate off-chip connections, one for the main RF signal transistors and one for the biasing networks. This additional feature allowed for adjustment to the bias current off-chip with no need to change the main supply voltage of the RF circuit. The two DC connections are visible in the upper left corner of Figure 2.9. From a 3.3 V supply, each mixer draws 5.00 mA of current, setting the total power dissipation of the I and Q mixers at 33 mW. This power consumption was reasonable at the time the design was completed, but is quite large by modern-day standards.

## 2.3 LO Conditioning Chain

Analog quadrature downconversion, a necessity in direct-conversion receivers as discussed above, is typically performed by placing a  $90^\circ$  phase shift in the LO path to the quadrature (or “Q”) mixer. However, the sub-harmonic mixer described in Section 2.2.2 itself uses quadrature LO signals to generate the  $2\text{LO}$  component; therefore, a *pair* of quadrature phase shifters are needed in order to supply the required quadrature phases for the sub-harmonic in-phase (or “I”) and Q mixers, separately. Figure 2.10 illustrates the required phases for simultaneous sub-harmonic mixing and quadrature downconversion. In this work, the necessary conditioning of the input LO signal is done entirely on-chip. Figure 2.11 shows a block diagram of the LO conditioning circuitry. The LO chain is built around the two polyphase filters, also known as polyphase splitters, where the *A* polyphase supplies the I mixer with the quadrature phases of  $0^\circ$  and  $90^\circ$  while the *B* polyphase supplies the Q mixer with the quadrature phases of  $45^\circ$  and  $135^\circ$ . Since the mixer is fully differential, the complements of the quadrature signals are also required, which means polyphase *A* also supplies the  $180^\circ$  and  $270^\circ$  phases and polyphase *B* supplies the  $225^\circ$  and  $315^\circ$  phases. The LO chain also includes an input buffer and four two-stage output amplifiers.



(a)



(b)

Figure 2.8: (a) Illustration of potential LO feedback path in subharmonic mixer ground connection in [92]; (b) revised grounding scheme in which RF and LO sections have separate ground nets.

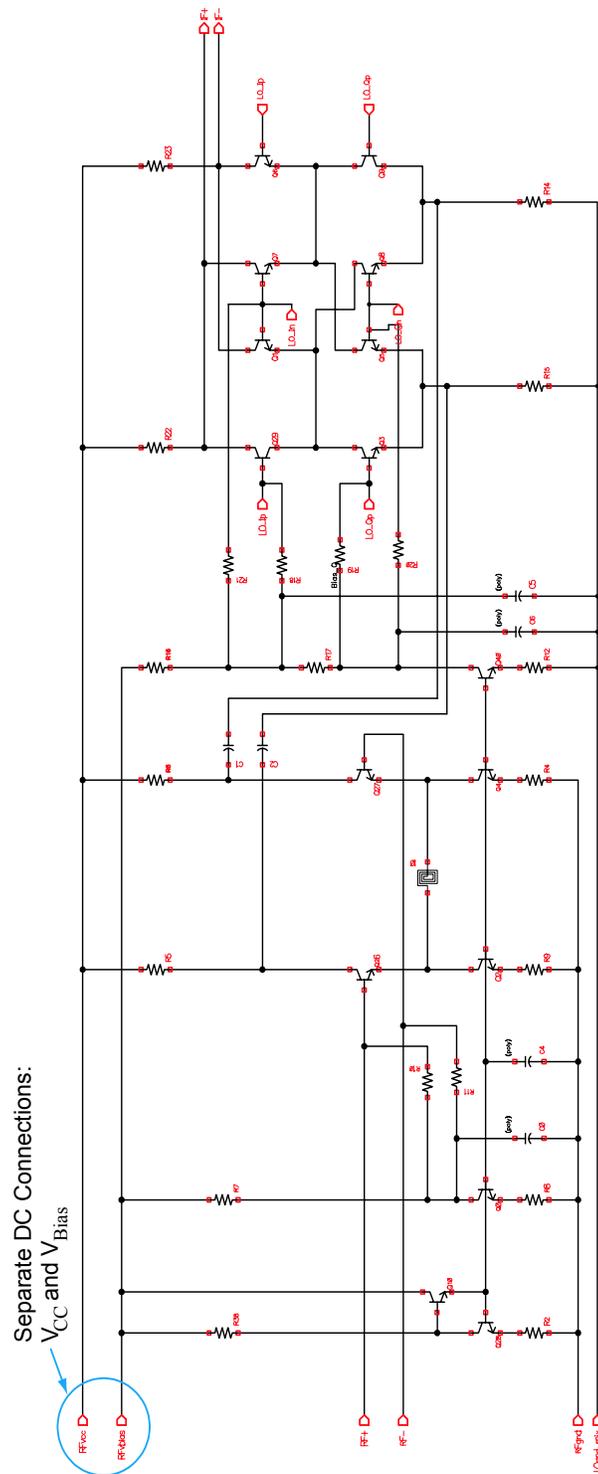


Figure 2.9: Full Cascode schematic of the mixer

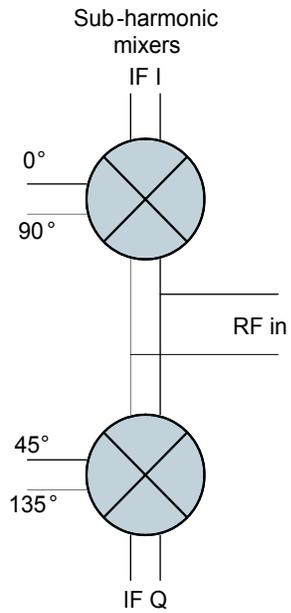


Figure 2.10: Active sub-harmonic mixer pair with required phases for full quadrature down-conversion.

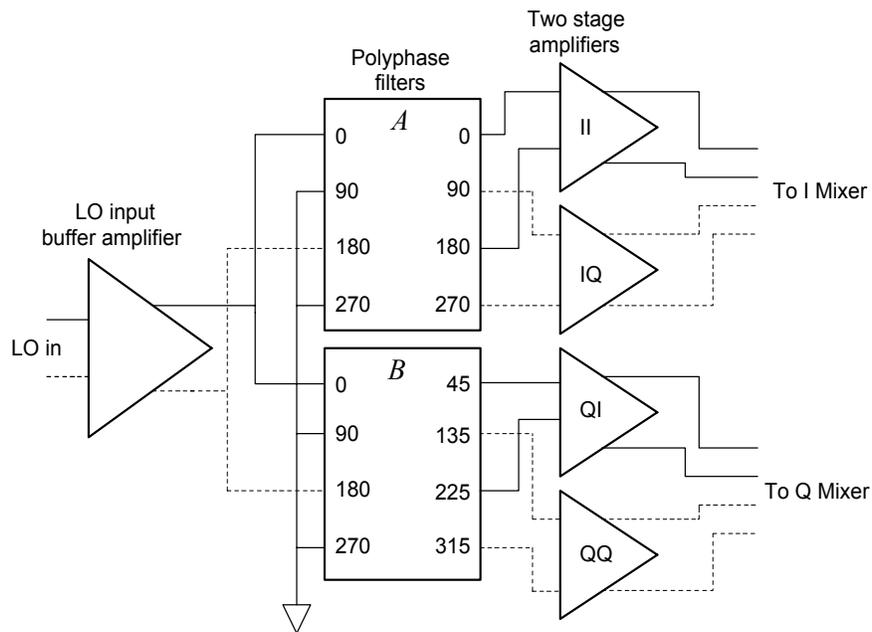


Figure 2.11: Block diagram of the LO conditioning chain.

Two different versions of the LO chain were studied. In the first version, the input buffer was designed to provide on-chip conversion of a single-ended LO signal (from an off-chip source) to a differential signal for driving the polyphase filters. In the second version of the LO chain, the input buffer was fully differential and conversion from a single-ended LO signal to a differential signal was accomplished with an off-chip  $180^\circ$  hybrid. The first version uses a topology that is similar to the LO conditioning chain in [92], which allowed for direct comparison between the two designs; the second version is more typical of an integrated receiver where the LO is supplied by an on-chip, differential VCO. The layouts of the circuit designs presented in this section are discussed in Section 2.4.

### 2.3.1 Polyphase Filters

A polyphase filter network is responsible for splitting the LO signal into the eight required phases for sub-harmonic mixing shown in Figure 2.11. The filters used in this work are an extension of the simple  $RC-CR$  phase splitter shown in Figure 2.12. Each branch of this circuit adds  $\pm 45^\circ$  of phase to the input signal without affecting the signal amplitude at the center frequency of the circuit, which is given by  $f_0 = \frac{1}{2\pi RC}$ . The phase change in each branch results in an overall phase difference between  $V_{out_1}$  and  $V_{out_2}$  of  $90^\circ$ <sup>3</sup>. The operation and mathematical description for the  $RC$  polyphase filter has been extensively documented in [13, 79, 114–117] with an excellent derivation of the voltage transfer functions in [59]. However, a simple way to consider the  $RC-CR$  phase splitter operation is to note that a path through a resistor results in a phase shift of  $-45^\circ$  while a path through a capacitor results in a shift of  $+45^\circ$ , at the center frequency of  $f_0$  [59].

To generate the differential quadrature phases shown in Figure 2.11, the circuit of Figure 2.12 is modified by adding two more  $RC$  poles [as shown in Figure 2.13(a)], which results in four signals with  $90^\circ$  of phase separation between them. With a differential signal applied to the first and third ports of the filter and with the second and fourth ports connected to ground, the output phases of the circuit in Figure

---

<sup>3</sup>The circuit basically performs the Hilbert transform, multiplying the input signal spectrum by  $-j\text{sgn}(2\pi f)$ ; as a result, an input signal of  $\sin 2\pi ft$  is converted to  $-\cos 2\pi ft$  and an input of  $\cos 2\pi ft$  is converted to  $\sin 2\pi ft$ .

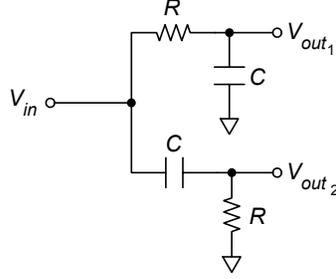


Figure 2.12: *RC-CR* filter; the phase difference between  $V_{out_1}$  and  $V_{out_2}$  is  $90^\circ$ .

2.13(a) can be written relative to the input as:

$$\begin{aligned}
 \angle V_{out,odd_1} &= 0^\circ - 45^\circ = 315^\circ \\
 \angle V_{out,odd_2} &= 0^\circ + 45^\circ = 45^\circ \\
 \angle V_{out,odd_3} &= 180^\circ - 45^\circ = 135^\circ \\
 \angle V_{out,odd_4} &= 180^\circ + 45^\circ = 225^\circ
 \end{aligned} \tag{2.11}$$

where input ports two and four do not contribute to the output phase since they are grounded. By convention, these phases are referenced here as the "Q phases", meaning they are the quadrature LO signals applied to the Q sub-harmonic mixer. The "odd" subscript denotes the odd number of poles in the filter, in this case 1.

If another set of poles is added in cascade, as in Figure 2.13(b), then an additional  $\pm 45^\circ$  phase shift occurs according to the rule above. The output phases for the two-pole filter at the center frequency  $f_0$  can be written as:

$$\begin{aligned}
 \angle V_{out,even_1} &= 0^\circ - 45^\circ - 45^\circ = 270^\circ \\
 \angle V_{out,even_2} &= 0^\circ + 45^\circ - 45^\circ = 0^\circ \\
 \angle V_{out,even_3} &= 180^\circ - 45^\circ - 45^\circ = 90^\circ \\
 \angle V_{out,even_4} &= 180^\circ + 45^\circ - 45^\circ = 180^\circ
 \end{aligned} \tag{2.12}$$

Thus, using a polyphase filter with an odd number of poles can provide the set of differential quadrature phases to the Q sub-harmonic mixer, while a polyphase filter with an even number of poles can supply the shifted set of differential quadrature phases to the I sub-harmonic mixer. The main point is the phase separation be-

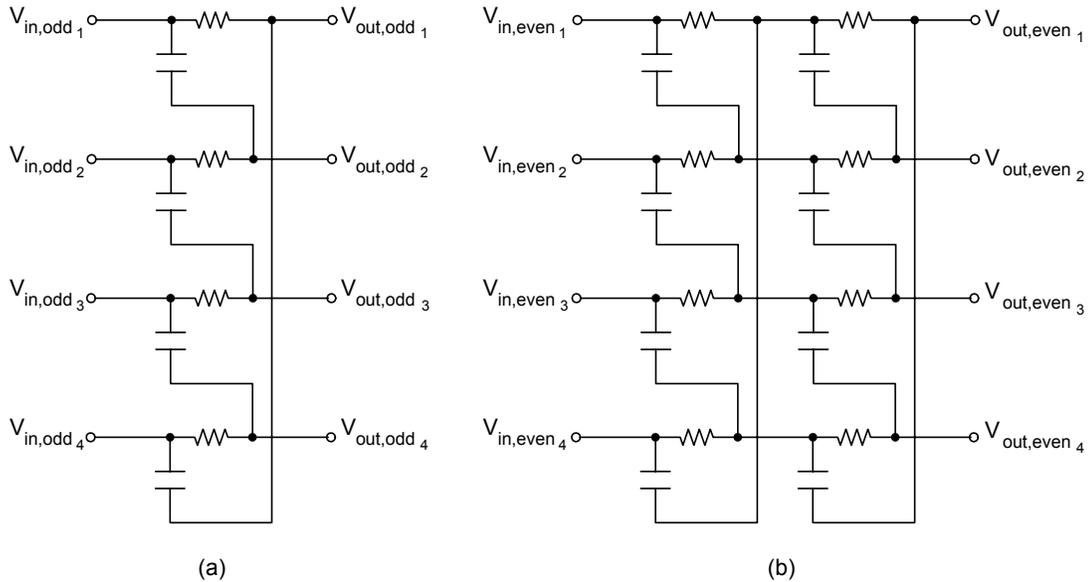


Figure 2.13: Polyphase filter: (a) basic one-pole  $RC$  filter; (b) two poles cascaded together.

tween the two polyphase filters is  $45^\circ$ , which is the phase separation needed for the generation of the 2LO signal (within the sub-harmonic mixers) and for quadrature downconversion.

Additional stages of  $RC$  poles can be added to the filter to improve the flatness of the amplitude and phase response; however, each additional pole also attenuates the amplitude of the LO signal and therefore demands more amplification at the polyphase output for proper operation of the mixer LO switching core. Therefore, a tradeoff exists between the flatness of the polyphase splitter response across the band of interest and the current consumption of the entire LO chain.

To achieve adequate phase and amplitude flatness while not consuming excessive amounts of power, a four section filter is used to generate the I phases ( $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ , and  $270^\circ$ ) and a three section filter is used to generate the Q phases ( $45^\circ$ ,  $135^\circ$ ,  $225^\circ$ , and  $315^\circ$ ). Because the LO is at half the RF frequency, the required bandwidth of the polyphase filter is also halved. The half-LO means the filter must cover from the edge of the lower U-NII band (5.15 GHz) to the edge of the upper band (5.825 GHz), or  $\Delta f/2 = \frac{5.825-5.15}{2}$ , which corresponds to roughly 340 MHz of bandwidth. The capacitor of all  $RC$  poles is fixed at 450 fF, which allows for a more compact and symmetric layout. A common capacitor value also helps match on-chip parasitics

between different polyphase paths. The first two resistor values are calculated to set the pole frequency just outside the edges of the desired band, which provides some extra margin to the bandwidth in case unaccounted for parasitics shift the frequency response of the filter by a few megahertz. The remaining resistor values are calculated to space the poles logarithmically between the band edges. The final schematic for the eight-output polyphase pair is shown in Figure 2.14.

The series capacitors at the filter outputs provide a method for adjusting the output phases of the polyphase filter to compensate for the loading effects of the following stages. By simply replacing these capacitors with varactors, a potential method for dynamically tuning the output phases of the polyphase filters can be realized. This idea of tunability was researched further in [59].

### **2.3.2 Input Buffer/Differential Amplifier**

An integrated receiver typically includes a frequency synthesizer to generate a stable LO signal. A synthesizer is basically a frequency control system based on a phase-locked loop, where the VCO, which is responsible for generating the high frequency LO, is locked to a stable reference frequency (typically well-below the RF range) by tracking the phase relationship between the two signals. In the case of this dissertation research, the goal is to provide a “proof-of-concept” for an active sub-harmonic RF front-end. Thus, the design of a fully integrated frequency synthesizer along with the other receiver components was beyond the scope of the project and not practical given the time constraints. Therefore, the LO signal is supplied by off-chip single-ended RF sources for characterization purposes. However, as discussed in the prior section, the input to the polyphase filter requires a differential signal to generate the quadrature, differential outputs for the sub-harmonic mixers. Thus, there is a need for additional circuitry (on or off chip) to convert from a single-ended LO signal to a differential one. Two different methods are explored in this work: first, the LO is applied to the chip single-endedly and converted to differential form using an on-chip buffer; second, the chip is fully differential and the conversion takes place off-chip using an off-the-shelf 180° hybrid. Regardless of the topology, a buffer is required at the inputs of the polyphase filters to provide isolation from package and wirebond parasitics, and to present a low-impedance to the filter inputs.

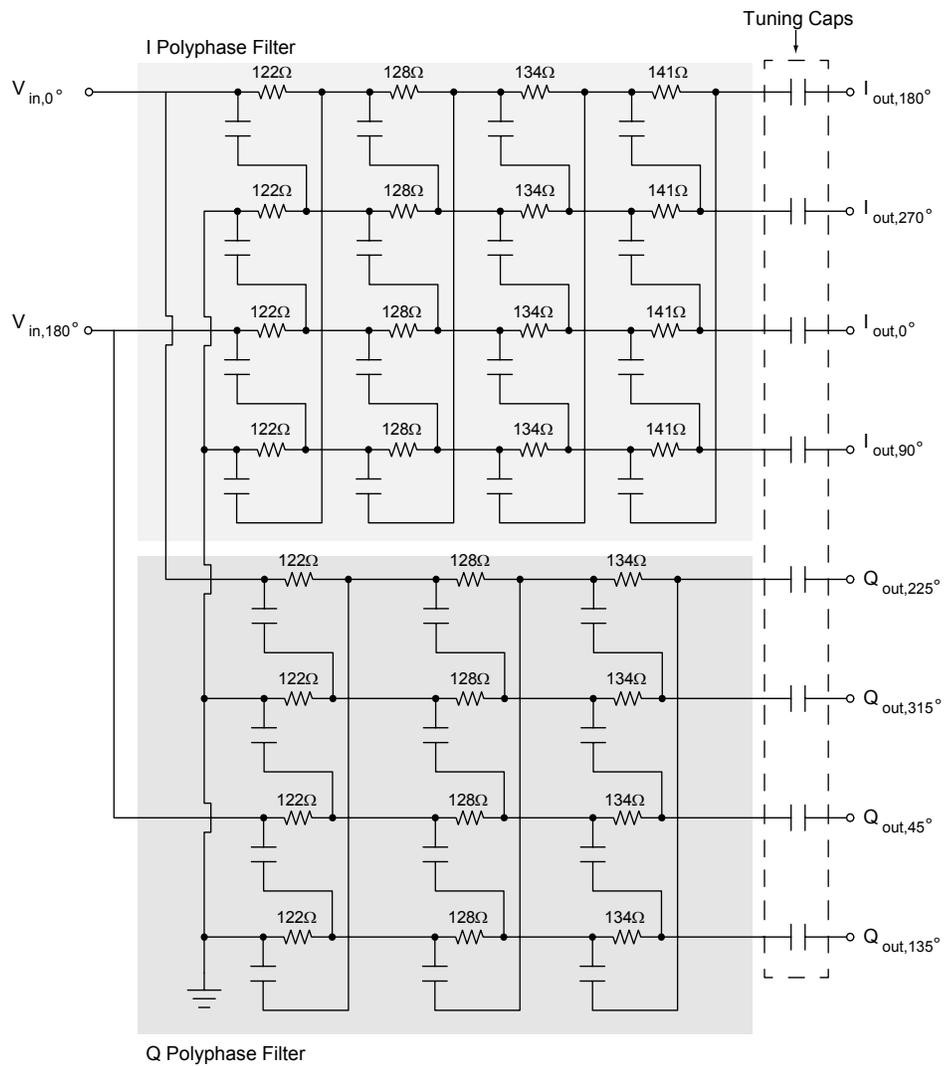


Figure 2.14: Schematic of both polyphase filter showing common inputs, separate ground, and series output tuning capacitors.

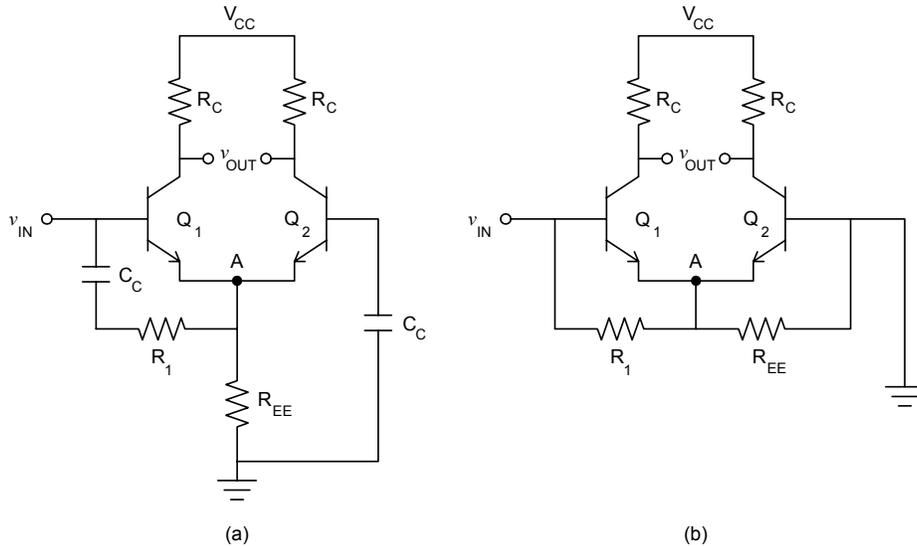


Figure 2.15: LO input buffer: (a) simplified schematic with additional resistor  $R_1$ ; (b) simplified AC equivalent circuit showing the symmetry of the circuit.

**Single-ended Buffer** In this work, *active* on-chip single-ended-to-differential conversion of the LO signal is used to interface the chip with the single-ended test equipment. Other methods, such as passive on-chip baluns [118], [119] or integrated transformers [120], [121] have been pursued, but the lack of accurate models for simulation [122] and the typical size and loss of these elements [123] limit their applicability. Furthermore, these passive approaches do not necessarily improve DC power consumption (compared to an active approach) since the input of the polyphase filters still needs to be buffered from the parasitics of the passive structure.

The single-ended-to-differential buffer used here, referred to as the input buffer, is identical to the one used in [92]. The RF signal is applied to the base of one differential pair transistor while the base of the other is tied to AC ground. A shunt resistor is added to the input of the buffer to improve the amplitude and phase balance of the output differential signal. Figure 2.15(a) shows the simplified schematic for the input buffer. The tail current of the input buffer is set with resistor  $R_{EE}$ ; by setting  $R_1 = R_{EE}$ , the phase and amplitude balance can be improved. Figure 2.15(b) shows the RF equivalent circuit of the buffer and illustrates the additional symmetry resulting from the addition of  $R_1$ .

To present a low impedance to the polyphase filters while not excessively loading

the output of the buffer, a pair of common-collector (emitter-follower) amplifiers are employed to form the output stage of the buffer. The buffer consumes 2.8 mA of current through the main differential pair and 2.2 mA through the common-collector stages. The input match to the circuit is set with an off-chip, shunt  $51\ \Omega$  (standard value) resistor. This simple method of reducing mismatch reflections does not have an impact on the receiver noise figure (since noise figure is measured at the RF port of the mixer, not the LO), but does reduce the signal power level by 3 dB. Figure 2.16 shows the full schematic of the single-ended input LO buffer.

**Differential Buffer** The phase and amplitude imbalance arising from the single-to-differential buffer is problematic since the errors feed directly into the polyphase filters. This imbalance results in imperfect quadrature phases applied to the sub-harmonic mixers and ultimately, to a large amplitude and phase imbalance between the IF I and Q branches of the receiver, which in turn leads to degraded bit-error rates [88]. An alternative approach is to move the differential signal-conversion off-chip, either at board level or using an off-the-shelf, connectorized component. The latter method is employed in this case since using off-the-shelf components reduces development time and removes the potential for fatal design errors.

Consequently, the differential input buffer is based on a simple differential pair. Similar to the single-ended buffer, the differential buffer has common-collector amplifiers at its output to present a low-impedance to the input of the polyphase filters. Again, shunt off-chip  $51\ \Omega$  resistors at each branch of the differential input are used to match the buffer input to the LO signal source. A schematic of the buffer amplifier is shown in Figure 2.17. The collector resistors are set to  $1\ \text{k}\Omega$  to provide additional voltage gain to the LO signal before the polyphase filters as a means to lower the required LO input power. The differential pair is biased in the same fashion as the RF transconductor discussed in Section 2.2.2.

### 2.3.3 Output Two-Stage Amplifiers

The cascaded loss due to the multiple-pole configuration in the polyphase filters must be compensated for through amplification to ensure the transistors of the sub-harmonic mixer switching core have sufficient drive levels. Although the input buffer

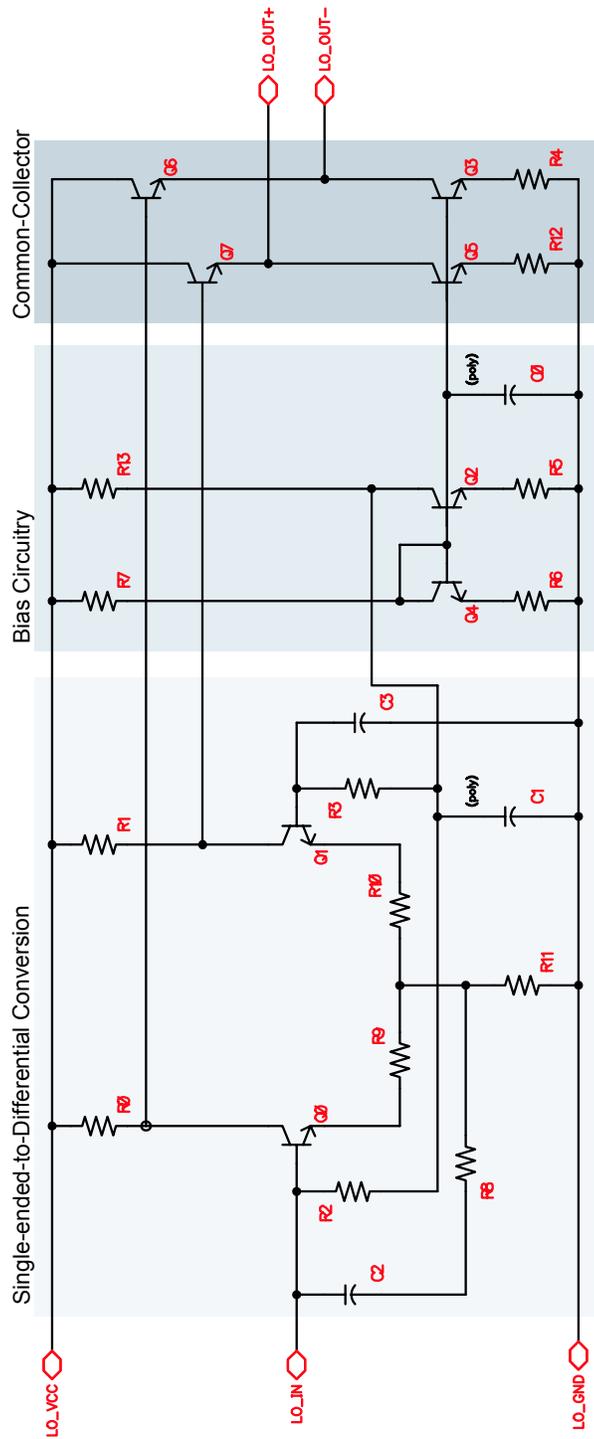


Figure 2.16: Full Cadence schematic of the single-ended input LO input buffer.

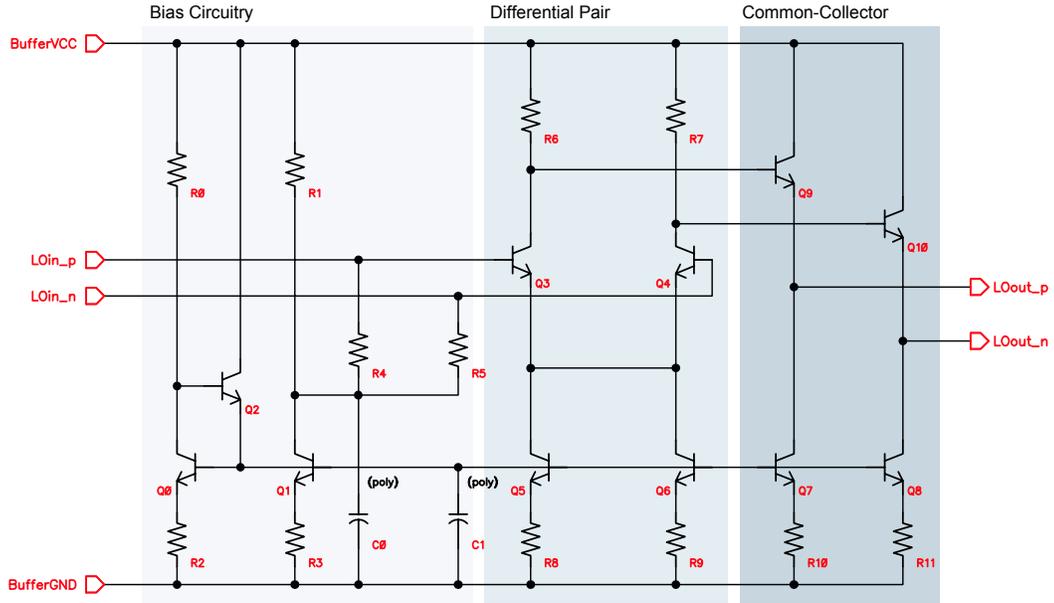


Figure 2.17: Full Cadence schematic of the differential input buffer.

discussed provides some gain for the LO signal, this amplification alone is not adequate to overcome the loss of the two multi-pole filters. Furthermore, the differing number of poles in the two polyphase filters — four for the I polyphase filter and three for the Q — means that the total loss through each of the two quadrature LO branches is not the same. Therefore, amplification of the LO signal after the polyphase filters is required and the required gain of the amplifiers following the filters is dictated by the number of poles in each filter.

To achieve the two different gain values required, two separate differential amplifiers were designed — one for the I branch and one for the Q branch. Both sets of amplifiers have two gain stages, which was found through simulation to provide the best performance with respect to phase imbalance and current consumption.

The combination of the collector load resistors and the bias current sets the gain ( $g_m R_C$ ) of each stage. However, in order to keep the desired phase balance between the eight outputs of the polyphase filter, the collector resistors in all eight gain stages (two gain stages per branch, four branches) must be kept exactly equal. Therefore, adjusting the bias current is the simplest method for controlling the gain between the

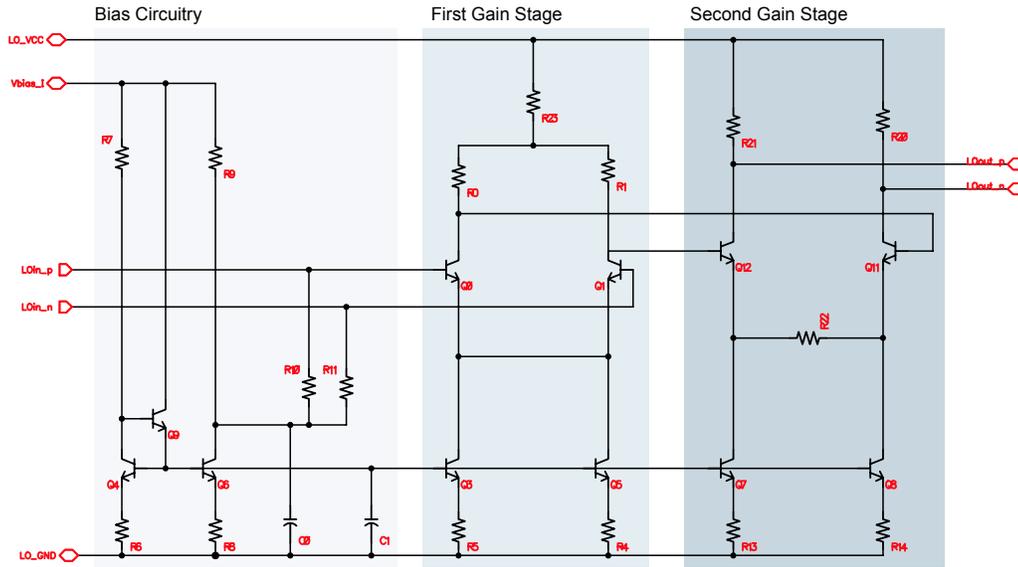


Figure 2.18: Full Cadence schematic of the two-stage differential amplifier.

I and Q branch amplifiers<sup>4</sup>. As with the input buffer, current mirrors are used to set the bias of each stage.

Figure 2.18 shows the full schematic of the two stage amplifier. The two gain stages are DC-coupled together — the DC voltage level at the collectors of the first stage sets the base bias of the second stage — which obviates the need for coupling capacitors. The elimination of these capacitors is advantageous since they would otherwise need to be very large in value (and thus area) at 2.5 GHz to provide a good AC short to the LO signal. Resistor  $R_3$  in the first stage adds an additional voltage drop before the collector resistors as a means to set the appropriate base bias to the second stage transistors. Since the second stage is driven by the amplified signal of the first, emitter degeneration is used to improve the linearity of the second stage; emitter degeneration also helps prevent the second-stage differential pair from becoming heavily saturated, where fluctuations in the amplitude could be converted to changes in phase<sup>5</sup> and in turn contribute to output I/Q imbalances. The base bias circuitry of the first stage and the current mirrors for both stages are identical to the ones used in the input

<sup>4</sup> Of course, the use of two different bias currents is not the best solution as such changes affect the high-frequency parasitics and performance of the transistors; for example, the devices of the two different amplifiers are biased at two different points along the  $f_T$  curve.

<sup>5</sup> Known as amplitude modulation to phase modulation, or AM-to-PM, conversion.

Table 2.1: Current in mA for each stage of the I/Q output amplifiers.

I AMPLIFIER		Q AMPLIFIER	
1st Stage	2nd Stage	1st Stage	2nd Stage
2.64	2.05	1.65	1.48

buffer and the RF transconductor of the mixer. The current draw of each stage is given in Table 2.1. The current for the Q amplifiers is lower since fewer poles are used in the Q polyphase and less gain is required. The complete single-ended LO chain draws 24.74 mA from a 3.3 V supply while the fully differential LO chain draws 22.5 mA.

The current consumption of the LO chain is excessive by today’s standards and is more than twice the amount of both mixers combined. The loss through the polyphase filter, which mandates amplification, is largely responsible for the high current consumption. One approach to reducing the loss, and hence, the current consumption of the buffers, is to reduce the number of poles in the filters — instead of filters with three and four poles, the filters could be designed with one and two poles, respectively. Though this results in poor overall phase and amplitude flatness, the tunable polyphase presented in [59] could be used to compensate dynamically for these errors. Furthermore, the gain requirements of the entire LO chain could be reduced if a large signal-swing VCO, capable of providing enough power to overcome some of the loss through the polyphase filters, was integrated on-chip. In Chapter 6, an alternative approach to the generation of phase-tunable quadrature signals will be described to eliminate the need for the polyphase filter bank entirely.

## 2.4 Mixer Layout

The sub-harmonic mixer and LO chain circuits were laid out using Cadence Virtuoso [124] and IBM’s design kit for Cadence 4.4.6. Other than the input buffer of the LO chain, the two different layouts for the sub-harmonic mixer circuits are identical. Figure 2.19(a) shows the layout for the single-ended version and Figure 2.19(b) shows the layout for the fully differential version; in the latter case, an extra bondpad is added on the left side of the chip for the negative input to the differential buffer. An

LNA design to be described in Chapter 4 will ultimately be included with this layout; therefore, the single-ended LO without an LNA is denoted as SLON (**S**ingle-ended **L**O, **N**o LNA) while the **D**ifferential LO without an LNA is denoted as DLON.

In both cases, the LO is injected at the left side of the die while the RF is injected at the right; the I and Q IF outputs are taken from the top and bottom of the die, respectively. This layout of the RF/LO inputs and IF outputs improves isolation since the signal bondwires are not adjacent, reducing detrimental mutual inductance. To improve LO-to-RF isolation, guardrings are placed around the RF transconductors of both the I and Q mixers. These guardrings, or isolation walls, consist of rows of substrate contacts placed between two walls of deep trench isolation. To separate and improve the isolation between the I and Q channels, an additional isolation wall spans the center of the chip. These walls help break up the conductive silicon substrate to interrupt leakage paths and reduce signal and noise coupling between circuits [125]. Figure 2.20 illustrates the basic isolation wall layout.

The three gray squares on the right of the chip are lattices of deep trench isolation. These isolation rings are used in the front-end design presented in Chapter 4 to add extra isolation to the inductors of the previously mentioned LNA. The squares are left in the standalone mixer layouts to make the mixer and front-end circuits as identical as possible. The total die size including bondpads is  $2.3\text{ mm} \times 1.8\text{ mm}$ .

In order to fully realize the benefits of differential circuitry, the layout of the circuit needs to be as symmetric as possible; otherwise, imbalances between the differential pairs can result in poor common mode rejection and reduced cancellation of even-order harmonics. Symmetry not only refers to the component placement but also to the device and interconnect parasitics. Therefore, the routing between components and between circuits is identical. For example, the metal traces that route the plus and minus inputs of the differential circuits are the same length and width and cross over the same metals or components, which ensures that the resistive and capacitive parasitics on both lines are the same. Symmetry is also present between the I and Q channels, where the circuits of each are mirrored about the horizontal center-line of the chip.

In a similar fashion, the LO polyphase filter layouts were structured with parasitics in mind. Experiments conducted by RFMD have shown that parasitics can have

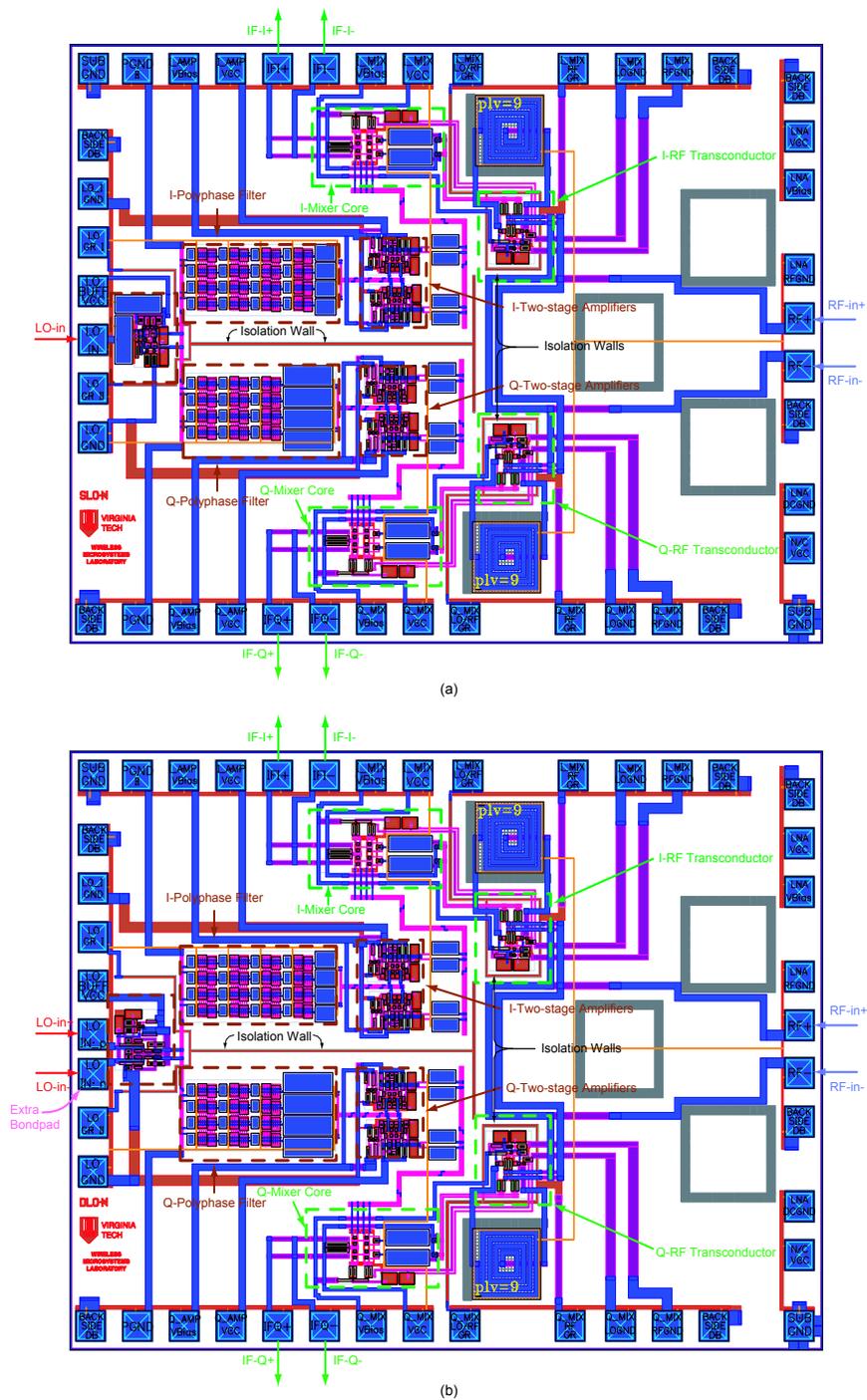


Figure 2.19: Detailed layout of (a) the single-ended LO input, standalone sub-harmonic mixers (SLON) and (b) the differential LO input, standalone sub-harmonic mixers (DLON). The die area of each is  $2.3 \text{ mm} \times 1.8 \text{ mm}$ .

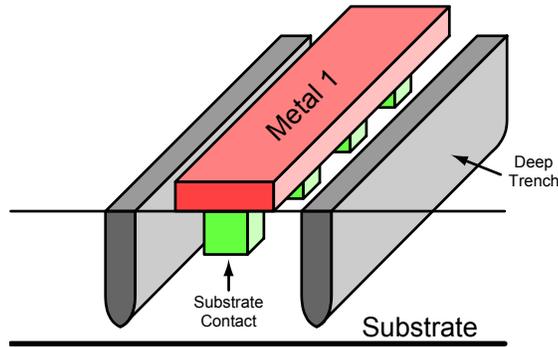


Figure 2.20: Illustration of isolation walls used in layout. Substrate contacts are sandwiched between two walls of deep trench isolation reducing substrate leakage.

a detrimental effect on the phase balance of a polyphase filter [126]. Thus, the polyphase filters are carefully laid out to guarantee that the parasitics between metal traces are nearly equal. For example, with four lines running parallel to each other in the same metal, the parasitic capacitance of the two outside lines is less than that of the two inside lines, as illustrated in the inset of Figure 2.21. To compensate for this imbalance, the lines of metal are “wrapped”, letting the outside line on the far left of the group become the outside line on the far right while the other three lines move to the left (see the inset of Figure 2.21). By essentially twisting the lines an equal number of times over the length of a routing, a metal trace occupies as much length on the outside of the group as on the inside.

Another method for ensuring that the parasitics are balanced is to double the resistor value of each filter pole and use two resistors in parallel to obtain the desired value, as shown in Figure 2.22. By mirroring the parallel resistors in both the vertical and horizontal directions, greater balance and symmetry can be achieved since the connections between components for each pole are similar. The use of the same value capacitor in each pole also helps in this regard since all resistors connect to the same metal surfaces (either the top or bottom plate of the capacitor).

The remaining bondpads shown in Figure 2.19(a) and (b) are for the separate DC supply and ground connections of each circuit. To provide a low-resistance path between these pads and the circuits connected to them, the paths are routed in “last metal” (the top,  $\sim 2\ \mu\text{m}$  thick aluminum in the layer stack) and are kept fairly wide at 10–20  $\mu\text{m}$ . Finally, the inductors used for emitter degeneration in the mixer RF

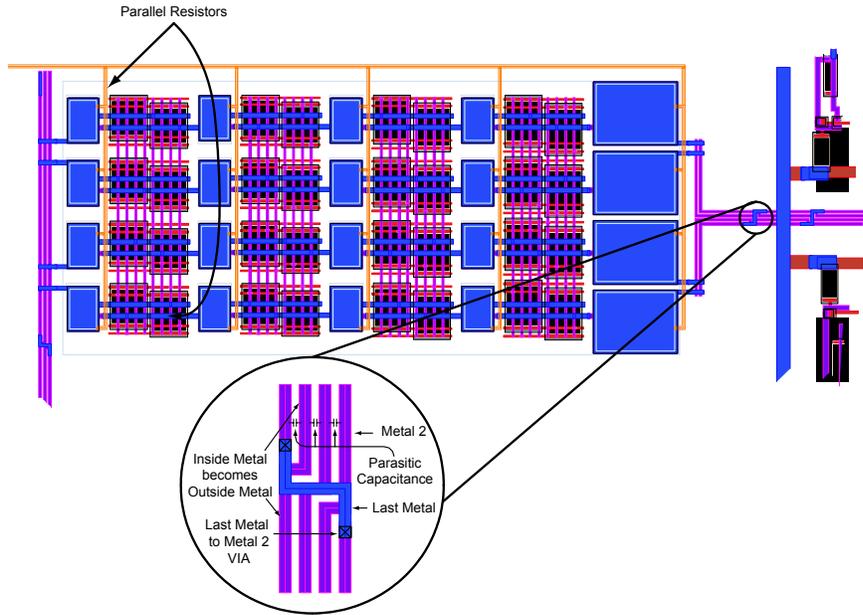


Figure 2.21: Layout of the polyphase filter. Resistors are doubled and placed in parallel to balance parasitics between all traces. Inset: The wrapping or twisting of parallel lines keeps inter-metal capacitance the same.

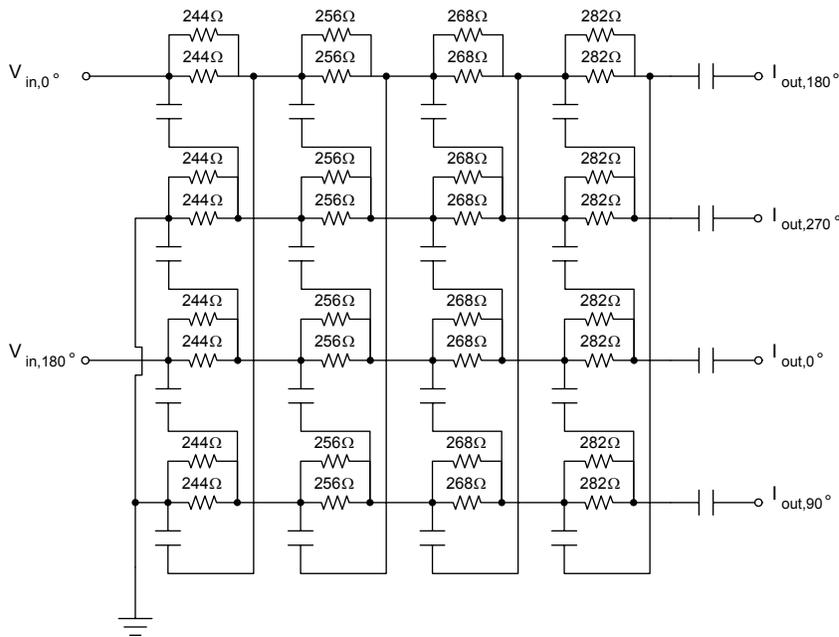


Figure 2.22: By using two resistors in parallel for each filter pole, layout asymmetries within the polyphase filters can be reduced.

transconductors are placed on opposite sides of the chip from each other to reduce mutual inductance between the two components. By default, a deep trench lattice exists under the inductors to reduce substrate coupling, thus improving the quality factor of the inductors. To enhance the isolation, the deep trench lattice is extended out beyond the edges of the inductor to provide additional substrate isolation from the rest of the mixer. Substrate contacts are kept at least  $100\ \mu\text{m}$  away from the inductors to prevent a reduction in the inductor quality factor [127].

## 2.5 Simulated Mixer Results

The  $\times 2$  sub-harmonic mixer design, including the LO conditioning chain, was simulated using Agilent's Advanced Design System (ADS), Version 1.3, which was the available version at the time this work was initiated. The design kit for the fabrication technology, supplied by IBM, included full Vertical Bipolar Intercompany (VBIC) models for the SiGe HBT devices along with models for passive devices like resistors, capacitors, inductors, and substrate contacts<sup>6</sup>.

Linear  $S$ -parameter simulations were used to determine the input match of the mixers and LO chain, while harmonic balance analysis (HBA) was used to simulate large-signal or non-linear effects and frequency translation (mixing) performance. HBA is a frequency domain technique that uses Fourier analysis to solve Kirchoff's current law (KCL) at each circuit node for all included (user specified) signal harmonics [128]. Simulations of a complex, multi-node circuit, such as the full sub-harmonic mixer design, require a great deal of time and computer resources to converge on a solution; for example, on a personal computer with 512 MB of RAM, typical simulations required more than three hours. Therefore, three RF frequency points were simulated over a 10-point sweep of LO power. To help simulator convergence, an IF of 10 MHz was chosen instead of the 0 Hz applicable for direct-conversion receivers. The non-zero IF, while being indicative of direct-conversion circuit performance, is also relevant for low-IF architectures, for which this design is also suitable. Since the simulations were conducted at a non-zero IF, single-sideband (SSB) noise analysis was included

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<sup>6</sup>Unfortunately, the design kit was not forward-compatible with more recent releases of ADS; furthermore, with the release of new tools such as RF Design Environment, which links ADS and the Cadence Design System together, IBM no longer supports standalone ADS design kits.

as part of the harmonic balance setup.

### 2.5.1 Packaging

An integrated circuit package is a chip’s electrical, thermal, and mechanical interface to the off-chip environment; the package physically protects the IC while also providing mechanisms for heat transfer and DC connections to the die [129]. Ideally, the package would have no effect on the desired electrical performance; however, high frequency parasitics associated with packaging affect the tuning/frequency response of the circuit and can have detrimental effects on circuit operation [130]. These parasitics include the bondwires, which make the physical connection between the bondpads of the circuit die and the package pins, and the package pins themselves, which interface with the external circuitry such as a printed circuit board (PCB) or a module substrate. Thus, establishing the package type and size is a critical step and should be determined as early as possible in the design process so that package effects can be accounted for in circuit simulations.

A wide selection of package types are available, with varying costs, parasitics, and assembly complexity for the IC. The size of the die and the number of input and output pins dictates the size of the package while the choice of package type — such as lead or leadless, ceramic or plastic — is a function of cost, parasitics, and power dissipation. For commercial circuits under 6 GHz, molded plastic packages are a popular choice since these packages are inexpensive and compatible with most board manufacturing processes [129]. Although plastic packages typically exhibit poor heat conductivity, the circuits presented in this work dissipate much less than 1 W of power, which makes power dissipation less of a concern. Therefore, given the cost and parasitic advantages, a leadless plastic package was chosen for this research.

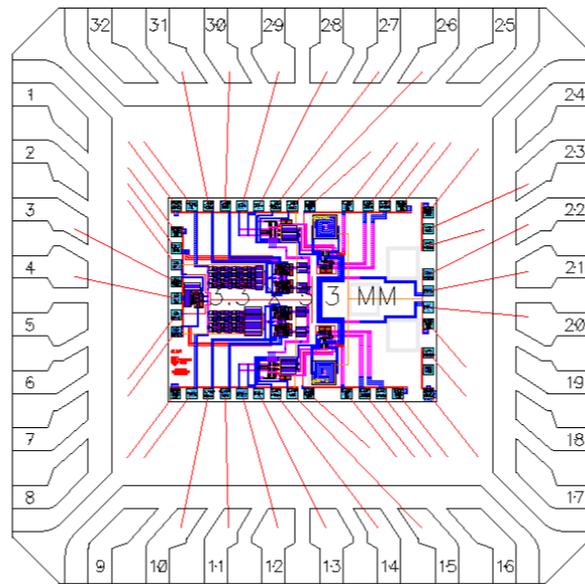
The designs presented here are housed in the Amkor MicroLeadFrame (MLF) series of plastic packages. The MLF series is comprised of leadless packages of various sizes and pin counts. The input/output (I/O) pins are exposed on the top and bottom so that the package can be wirebonded to the top of the pin and soldered to the board from underneath. This form of pin connection is preferred over the lead-form — in which strips of metal extend from the package body to connect to the external circuitry — because of reduced package parasitics. In order to have enough area for

Table 2.2: Package pin out for the SLON and DLON mixers.

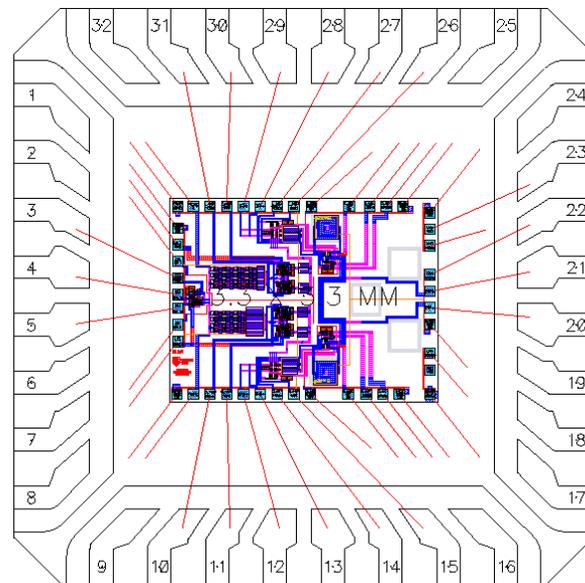
Pin#	SLON	DLON	Pin#	SLON	DLON
1	N/C	N/C	17	N/C	N/C
2	N/C	N/C	18	N/C	N/C
3	LO.buff.V <sub>CC</sub>	LO.buff.V <sub>CC</sub>	19	N/C	N/C
4	LO.IN	LO.IN+	20	RF-	RF-
5	N/C	LO.IN-	21	RF+	RF+
6	N/C	N/C	22	N/C	N/C
7	N/C	N/C	23	N/C	N/C
8	N/C	N/C	24	N/C	N/C
9	N/C	N/C	25	N/C	N/C
10	Q.amp.V <sub>BIAS</sub>	Q.amp.V <sub>BIAS</sub>	26	I.mix.V <sub>CC</sub>	I.mix.V <sub>CC</sub>
11	Q.amp.V <sub>CC</sub>	Q.amp.V <sub>CC</sub>	27	I.mix.V <sub>BIAS</sub>	I.mix.V <sub>BIAS</sub>
12	IFQ+	IFQ+	28	IFI-	IFI-
13	IFQ-	IFQ-	29	IFI+	IFI+
14	Q.mix.V <sub>BIAS</sub>	Q.mix.V <sub>BIAS</sub>	30	I.amp.V <sub>CC</sub>	I.amp.V <sub>CC</sub>
15	Q.mix.V <sub>CC</sub>	Q.mix.V <sub>CC</sub>	31	I.amp.V <sub>BIAS</sub>	I.amp.V <sub>BIAS</sub>
16	N/C	N/C	32	N/C	N/C

the  $2.3 \text{ mm} \times 1.8 \text{ mm}$  die, the chips are mounted in the  $5 \text{ mm} \times 5 \text{ mm}$  MFL package, which has a  $3.3 \text{ mm} \times 3.3 \text{ mm}$  exposed die flag (top and bottom) and 32 I/O pins. The die flag, also known as the paddle, is the ground plane of the package. The flag is fully conductive so that providing ground to the chip topside is a simple matter of soldering the entire paddle underside to the ground plane of the external system (e.g. test board). Downbonds, which connect the on-chip ground pads to the die flag, set the AC ground of the chip. The use of downbonds rather than individual package pins for grounding is advantageous for two reasons: first, the bondwires for the downbonds tend to be shorter, which results in less parasitic inductance; and second, the parasitics associated with the fully grounded die flag are significantly less than the parasitics of the package pins. These two advantages lead to a more ideal on-chip ground. Figure 2.23(a) shows the bondwire diagram for the SLON mixers while Figure 2.23(b) shows the bondwire diagram for the DLON mixers. Table 2.2 gives the pin out for both mixer circuits.

Based on an initial layout, the die footprint and the number of input and output connections were estimated; using these rough estimates, the parasitic bondwire resistances and inductances were modeled as described in Appendix B. Adding these



(a)



(b)

Figure 2.23: Bondwire diagram for (a) the SLON mixers; and (b) the DLON mixers.

parasitics into the simulation, the circuit was re-tuned and the layout modified. Once the die footprint was firmly established and the package size finalized, a more accurate model of the bondwire and package parasitics was determined using an electromagnetic (EM) field simulator [130]. The EM simulations were performed by collaborators at RFMD. The EM models were then incorporated into the original simulations and the circuit was re-tuned to account for the additional parasitics represented by this more accurate package model.

## 2.5.2 Simulated Results

For simulation purposes, the RF signal was fed through an ideal  $180^\circ$  hybrid to convert the output of the single-ended source to a differential signal for the mixer inputs. Each output of the differential IF was connected to a  $1.5\text{ k}\Omega$  resistor for maximum power transfer. The power gain was calculated as the difference between the IF+ and IF- outputs divided by the input RF power. Figure 2.25 shows the simulated conversion gain and SSB noise figure at an RF of 5.15 GHz and an IF of 10 MHz. At an LO power of 0 dBm, the conversion gain was 9.7 dB with a SSB noise figure of 10 dB. The results at the other two simulated RF frequencies (5.35 GHz and 5.825 GHz) were similar. The input return loss was better than 10 dB over the lower two U-NII bands, and better than 9.2 dB at the upper U-NII band, as shown in Figure 2.24.

Although the mixer is not designed for any specific application, most modern wireless specifications are defined with the cost of the hardware implementation in mind. One of the primary ways to reduce the cost of implementation is to limit the specified minimum power level for receiver sensitivity, which eliminates the need for expensive, ultra-low-noise circuits. Therefore, the 10 dB noise figure of the mixer is acceptable for low-cost wireless applications (such as WLAN) since the mixer noise figure can be reduced by placing a low-noise amplifier at the input (see Chapter 4) and limited sensitivity levels (on the order of  $\sim -80$  dBm) can easily be achieved.

The simulated I/Q phase balance of the single-ended LO mixers is shown in Figure 2.26. A perfect phase balance of  $90^\circ$  was achieved at an LO power of  $-3.4$  dBm with  $\pm 1^\circ$  phase error over the  $-5.8$  to  $-1$  dBm LO power range.

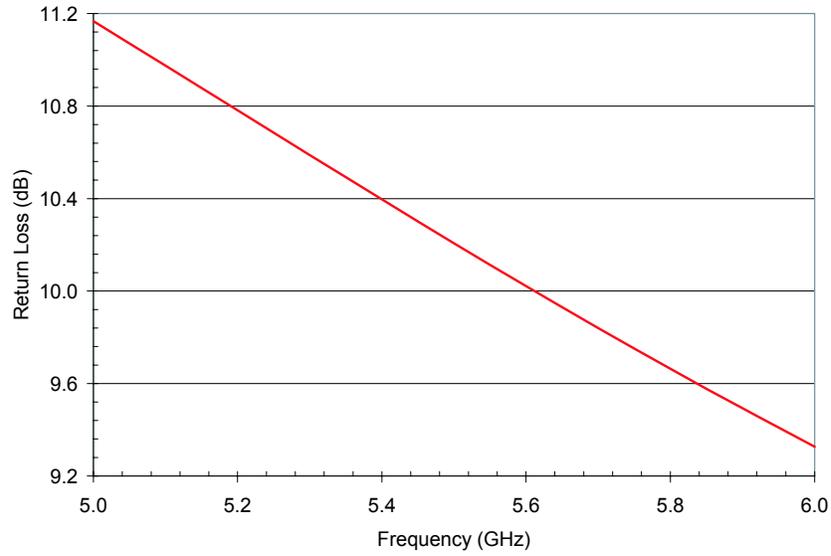


Figure 2.24: Simulated input return loss of the SLON mixer; EM model of package parasitics is included in the simulation.

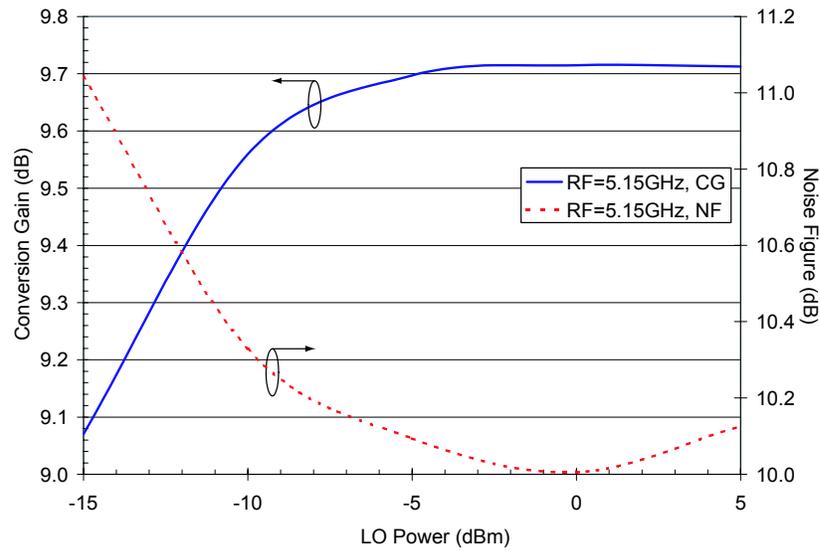


Figure 2.25: Simulated conversion gain and noise figure of the single-ended LO mixer I-channel (RF→IF-I). The RF is set to 5.15 GHz and the LO to 2.57 GHz giving an IF of 10 MHz. Q-channel results are similar.

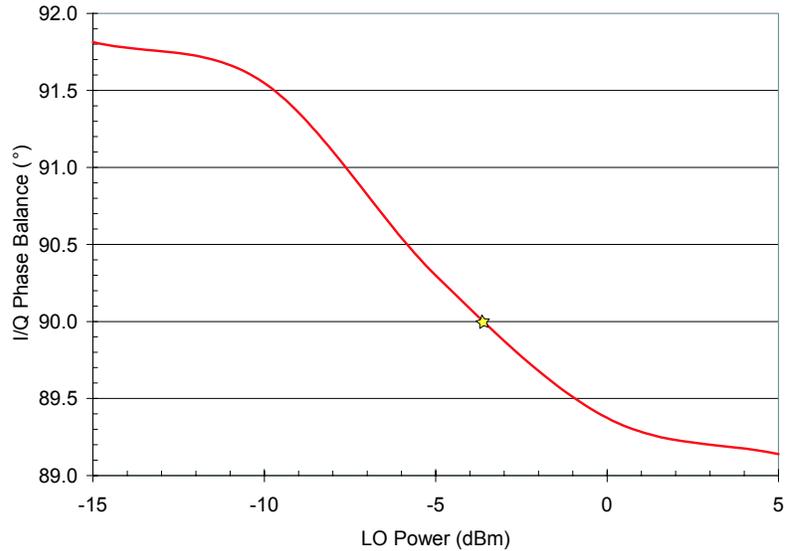


Figure 2.26: Simulated phase balance between the IF outputs of the I and Q mixers at and RF of 5.15 GHz and an IF of 10 MHz. The desired phase balance of  $90^\circ$  is noted by the star.

A two-tone test was simulated to find the third order intercept points of the I and Q mixers. Tones of 5.145 GHz and 5.151 GHz were applied to the RF input and were translated to 9 and 11 MHz IFs, respectively. The third order intercept point for the I mixer is shown in Figure 2.27. From the extrapolation of the fundamental and the conservative extrapolation of the third order products, the input third order intercept point was estimated to be +9 dBm.

The amplitude and phase response of the two LO chains are compared in Figures 2.28 and 2.29. The additional gain provided by the fully differential buffer can be seen in Figure 2.28 where the overall gain of the differential LO chain is nearly twice that of the single-ended chain. The consequence of the amplitude imbalance at the output of the single-ended-to-differential buffer is shown in Figure 2.28(a) where the LO chain output magnitudes of the eight signals are slightly different from each other. Conversely, the well-balanced differential buffer provides a near-perfect differential signal to the polyphase filter and consequently, all eight outputs have the same magnitude response [Figure 2.28(b)].

Figure 2.29 shows the deviation from the desired  $45^\circ$  of phase separation between the eight outputs. In simulation, the phase difference between the plus and minus

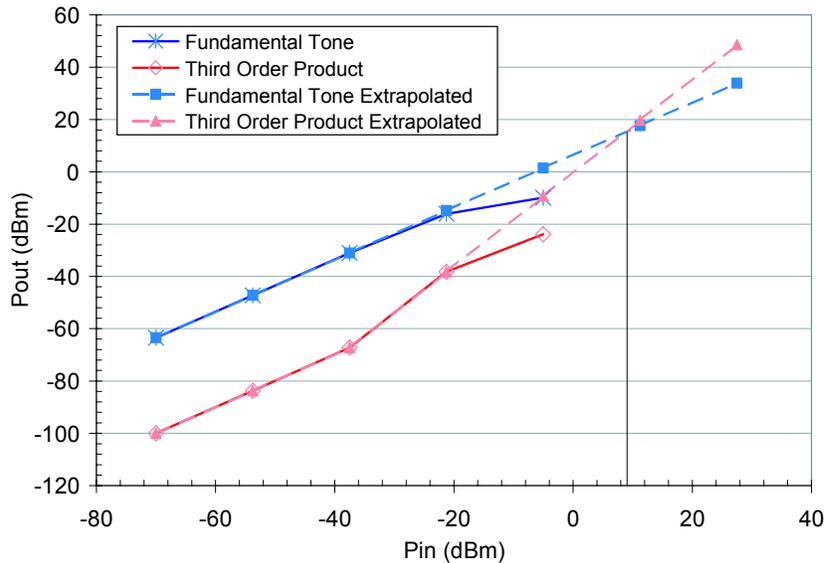


Figure 2.27: Simulated third order intercept point of the I mixer. The RF tones are set to 5.149 GHz and 5.151 GHz and are downconverted to 9 and 11 MHz, respectively. By extrapolating the fundamental and third order products, the simulated IIP3 is +9 dBm.

outputs of the single-ended input buffer is not quite  $180^\circ$ , which causes a scattering of the phases at the output of the LO chain as shown in Figure 2.29(a). The resulting phase error grows to  $\pm 1.25^\circ$  at the edges of the LO band. On the other hand, the differential buffer outputs are exactly  $180^\circ$  apart and a phase error of less than  $\pm 0.8^\circ$  is achieved at the edges of the LO band.

Unfortunately, simulation of the standalone differential LO mixers suffered from simulator convergence issues that resulted from the non-linearity of the differential LO chain input buffer. Based on a common-emitter differential pair, the buffer had a 1-dB compression point of  $-20$  dBm. In retrospect, the simulator was unable to converge to a solution since the circuit was simulated over the same LO input level ( $-15$  dBm to  $0$  dBm) as the single-ended LO simulations. At these power levels, the differential input buffer was highly compressed and operating in a nonlinear state.

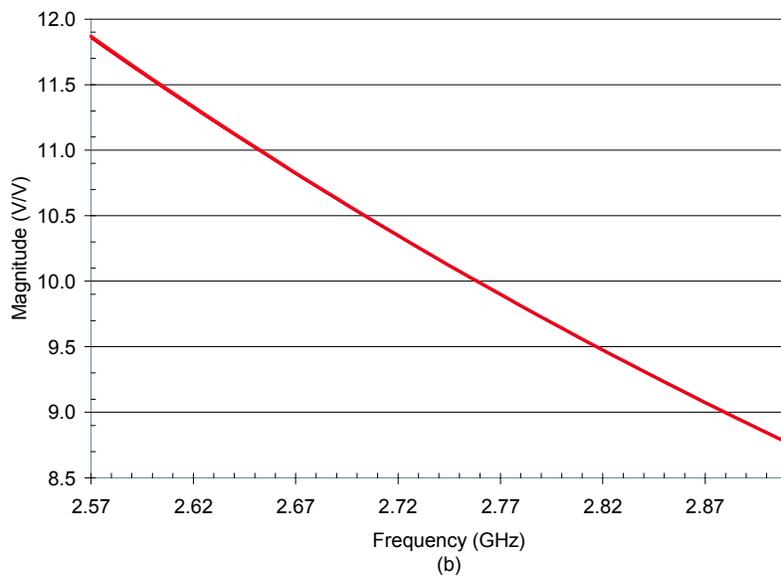
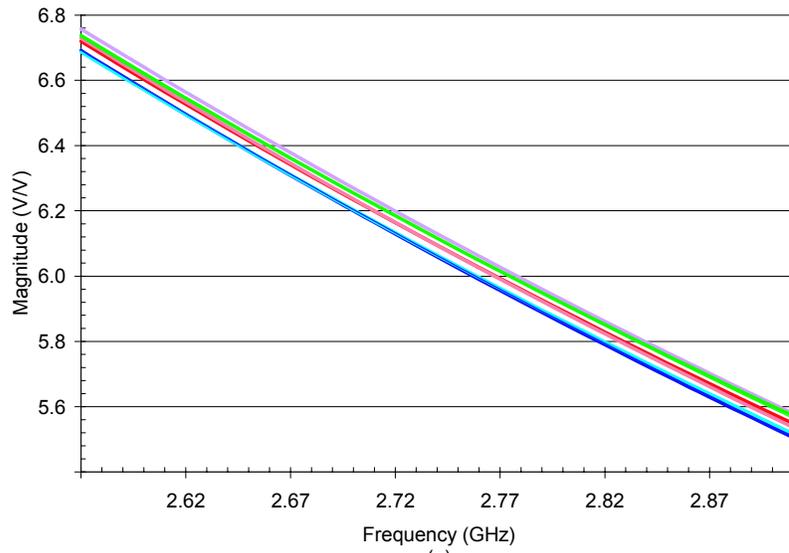


Figure 2.28: Simulated magnitude response of (a) the single-ended input LO chain and (b) the fully differential LO chain.

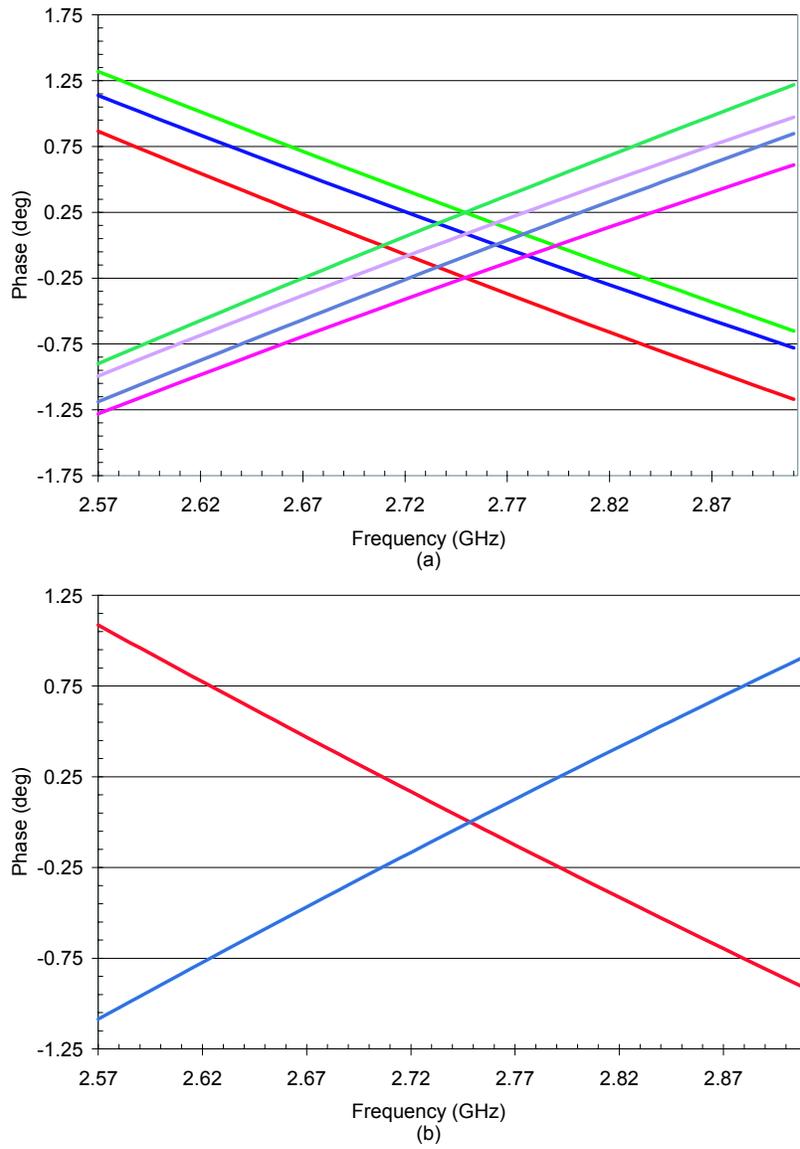


Figure 2.29: Simulated phase response of (a) the single-ended LO chain and (b) the fully differential LO chain.

## 2.6 Summary

This chapter has presented the design, simulation, and layout of two  $\times 2$  sub-harmonic quadrature mixer pairs for 5–6 GHz applications. In the first design, a single-ended LO signal was applied to the chip and converted to a differential signal by the LO chain input buffer. In the second design, the LO chain was fully differential, providing a more realistic interface for an on-chip VCO that could be integrated in future work. Simulations of the single-ended LO mixers showed a conversion gain of 9.7 dB, a noise figure of 10 dB, and an I/Q phase balance of  $90^\circ$  at an LO power level of  $-3.4$  dBm. The third order intercept point was (conservatively) simulated to be  $+9$  dBm. Simulation of the differential LO circuit was not successful because of simulator convergence problems. Both standalone mixer circuits were designed for operation from a 3.3 V supply with package parasitics included early on in the design process. Chapter 3 discusses the fabrication and measurement of these mixers.

## Chapter 3

# 5-6 GHz $\times 2$ Sub-Harmonic Mixer Fabrication and Measurement

**T**HE single-ended and differential LO input mixer designs from Chapter 2 were fabricated as standalone circuits (without an LNA<sup>1</sup>), which allowed for direct characterization of the active mixers. In this configuration, important DCR metrics, such as I/Q phase imbalance and second-order nonlinearities, could be studied without the complications introduced with cascaded components. This chapter presents the test configurations and the measured data for the mixer circuits with two different LO chains. As in the previous chapter, to simplify the discussion below, the mixers with the single-ended input LO chain are referred to as the SLON mixers, while the mixers with the differential LO input chain are referred to as the DLON mixers (the “N” indicates “no LNA”).

### 3.1 Fabrication and Test Setup

Prior to submission for fabrication, the layouts discussed in Section 2.4 were checked against the technology design rules that determine manufacturability (a process known as DRC — “design rule check”) and verified against the schematics used in simulation

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<sup>1</sup>A direct-conversion receiver design that integrated a low-noise amplifier with the mixers from Chapter 2, was fabricated on the same fabrication run; design and characterization of the LNA/receiver will be presented in Chapters 4 and 5.

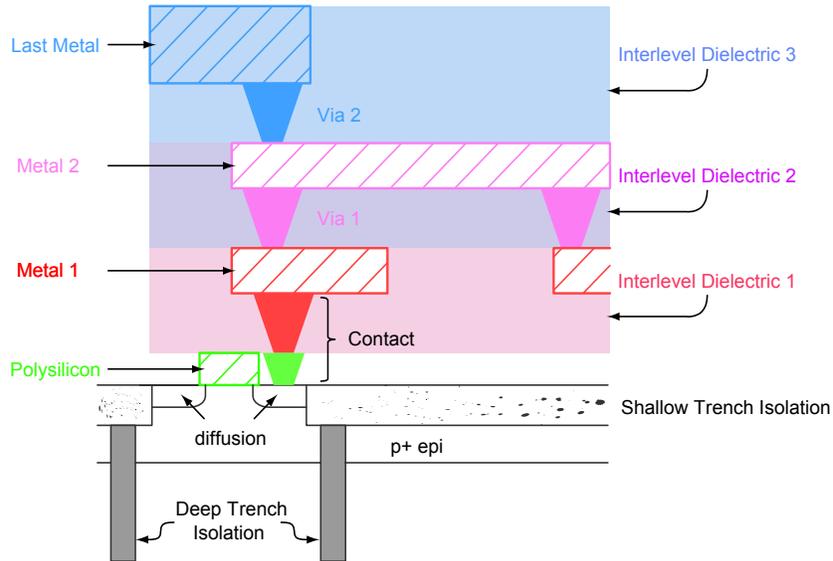


Figure 3.1: A simplified device and interconnect layer stack. Inter-level dielectric material supports and separates each metal layer.

(a process know as LVS — “layout versus schematic”). The designs were submitted to RF Microdevices (RFMD) in Greensboro, NC, integrated into an overall engineering mask-set database, and subsequently sent to IBM for fabrication.

### 3.1.1 Planarization and Metal-Fill

IC back-end processing includes the deposition of the metal/dielectric layer-stack. The stack is a combination of the interconnect metals, contacts (to connect metal to silicon/polysilicon structures) and vias (to connect different metal layers together), and layers of inter-level dielectric (ILD) material that separate the various levels from each other. A simplified device and interconnect metal/dielectric stack is shown in Figure 3.1.

Planarization of each ILD layer is accomplished with chemical mechanical polishing (CMP). The surface planarity resulting from CMP improves the lithographic resolution for subsequent layers and enables smaller layout design rules and stacked contacts/vias for better routing capabilities [127]. However, CMP processes are sensitive to the layout topography, i.e. the density of the metal pattern on each underlying

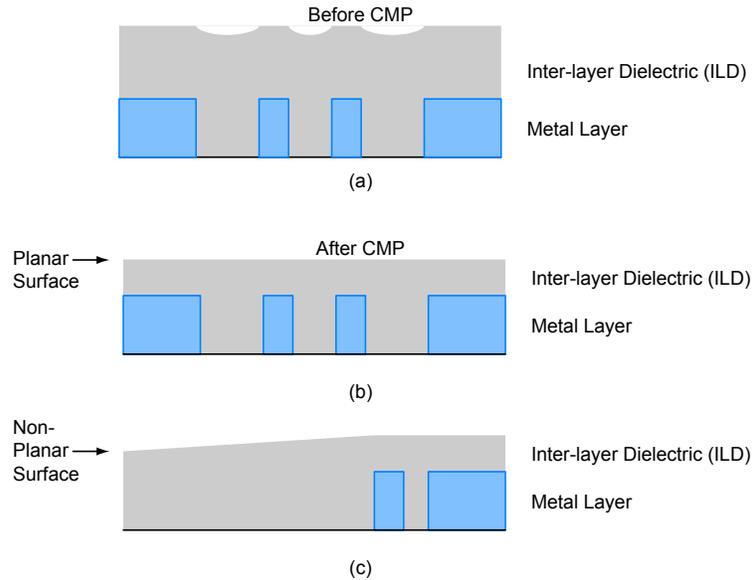


Figure 3.2: CMP planarization: (a) the surface of the inter-layer dielectric (ILD) before CMP; (b) the planarized surface after CMP; (c) the effect of variation in pattern density. The lack of metal under the left side results in more material being removed during CMP.

level affects the planarity of the higher levels. With an underlying, non-uniform topography, the dielectric layer thicknesses can vary across different regions of the chip and effect the lithographic depth of focus as well as the inter-layer capacitances, which in turn, can affect the high frequency performance of the circuit [131]. Figure 3.2 shows (a) the surface topology after the first ILD is deposited; (b) the planarization achieved after CMP processing; and (c) the CMP processing effects that result from a nonuniform underlying pattern density.

As a result, in modern process metal fill density rules are established for each layer and the pattern density of the chip is checked upon completion of the layout; in areas where the circuitry and routing are less dense, area-fill (or metal-fill) patterning is intentionally introduced. Metal-fill patterning compensates for the effects of any large, sparsely-populated areas of a chip by filling these areas with “dummy” patterns of metal [132]. By filling such unpopulated areas with lower metal layers, the pattern density of the stack is made more uniform. However, the improvements in uniformity resulting from metal-fill patterning must be balanced against the potential impact on circuit performance, since the large planes of metal can introduce para-

sitic capacitances or wave-guiding structures for high frequency signals [133]. The decision to tie the metal-fill to ground (or  $V_{CC}$ ) or to let the metal float electrically is based on circuit performance and reliability concerns. Therefore, metal-fill should be accounted for during the design phase.

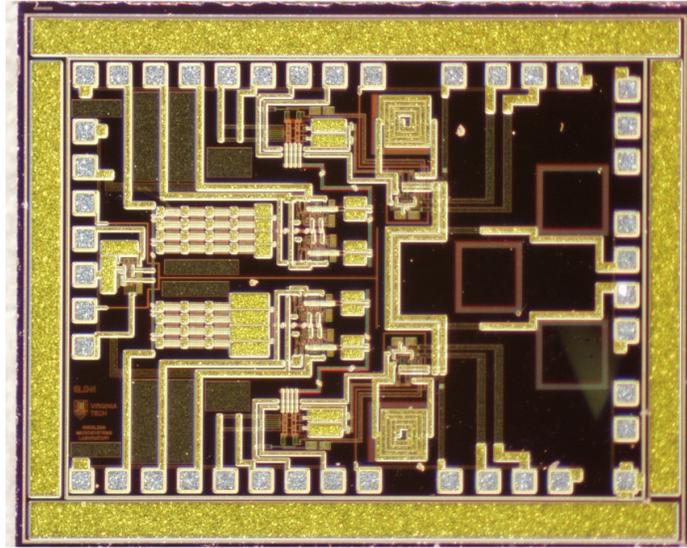
Despite the need for metal-fill patterning, in prior fabrication runs with IBM 5HP through RFMD (see [92]), pattern density, or metal-fill, rules were waived since the chips were for research purposes and ILD variations due to sparsely-populated regions were limited. When the designs in this work were submitted for fabrication, this same exemption was expected. However, during the final preparations for layout-database submission to IBM, the layout engineers at RFMD learned that IBM no longer waived the pattern density rules and that area fill was necessary. Unfortunately, this requirement was discovered just prior to the tapeout deadline, leaving no time to account for the effects of the metal-fill. The impact of the large metal-fill patterns on the circuit performance is discussed below.

A photo of the fabricated SLON mixer die is shown in Figure 3.3(a) and a photo of the open-packaged die is shown in Figure 3.3(b). Similarly, a photo of the fabricated DLON mixer die is shown in Figure 3.4(a) and a photo of the open-packaged die is shown in Figure 3.4(b). The die were packaged and mounted on test boards at RFMD. Because the die of the single-ended and differential LO designs use the same input and output package pins, the same test board design was used for both sets of mixer measurements.

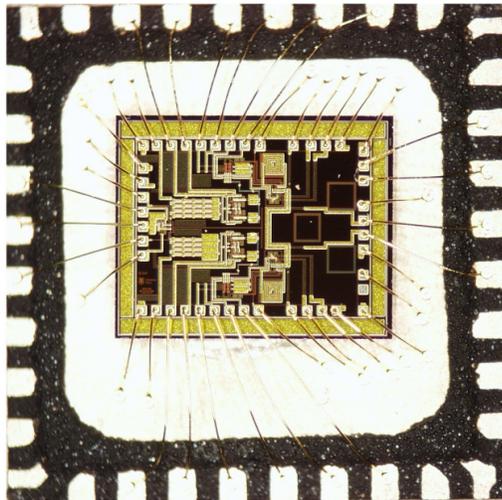
### 3.1.2 Test Boards

The packaged die were mounted on custom test boards for evaluation purposes. The test board was designed on FR-4 material with the following specifications:

- Dielectric constant:  $\epsilon_r = 4.33$
- board thickness: 29 mils (0.736 mm)
- copper thickness: 1 oz. (0.15 mils/3.81  $\mu\text{m}$ )
- layer count: 2 (top and bottom).

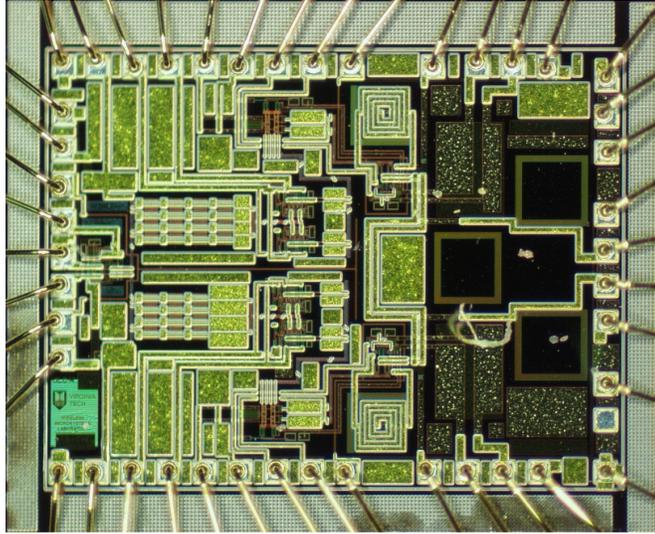


(a)

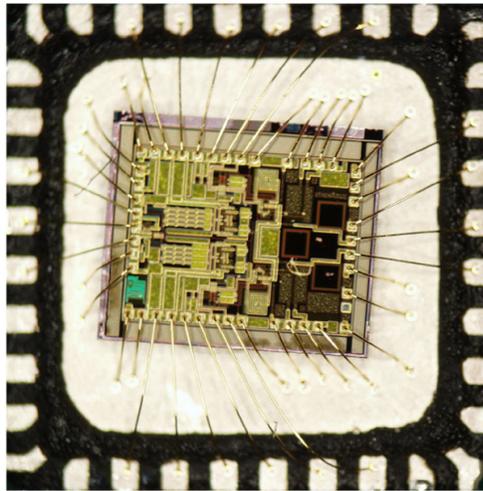


(b)

Figure 3.3: (a) Die photograph of the fabricated single-ended LO, standalone mixers (SLON). The chip area is  $2.3\text{ mm} \times 1.8\text{ mm}$ . (b) Photograph of the fabricated single-ended LO, standalone mixers (SLON) packaged in a  $5\text{ mm} \times 5\text{ mm}$  32 pin MLF package.



(a)



(b)

Figure 3.4: (a) Die photograph of the fabricated differential LO, standalone mixers (DLON). The chip area is  $2.3 \text{ mm} \times 1.8 \text{ mm}$ . (b) Photograph of the fabricated differential LO, standalone mixers packaged in a  $5 \text{ mm} \times 5 \text{ mm}$  32 pin MLF package.

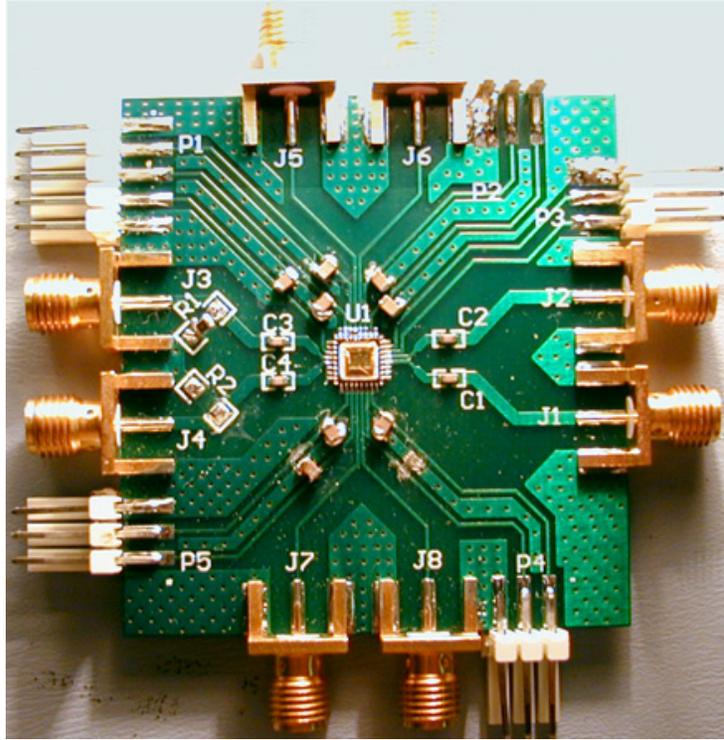


Figure 3.5: Photograph of the testboard used for measurement of the SLON and DLON mixers.

50 mil (1.27 mm) wide microstrip lines ( $\sim 50 \Omega$  characteristic impedance at 2.5–6 GHz) were used to route the differential RF and differential LO input signals from the board edge to the package<sup>2</sup>. On-board series coupling capacitors (68 pF) were used for the RF and LO inputs while the IF outputs were AC coupled using off-board coaxial DC blocks. The DC supply rails were connected to AC ground via shunt  $1 \mu\text{F}$  bypass capacitors. A photograph of the test board is shown in Figure 3.5. The eight SMA edge connectors provided the RF/LO/IF coaxial interfaces to the  $50 \Omega$  test equipment.

In order to facilitate de-embedding of the packaged die from the test board, a separate calibration board was also fabricated. The calibration board was identical to the device under test (DUT) board, but with the RF and LO input traces shorted together at the package-end. These shorted traces provided a through standard between the RF+ and RF- inputs and the LO+ and LO- inputs. Therefore, the loss contribution

<sup>2</sup>In the case of the SLON mixers, one of the two LO input traces is not connected to the package.

for the RF/LO traces leading to the IC were found by measuring the total loss between the RF+ and RF- ports and the LO+ and LO- ports on the calibration board, and dividing the result by 2 (or subtracting 3 dB) to find the loss in each individual input trace.

### 3.1.3 Basic Test Setup and Test Plan

The differential inputs and outputs of the mixer test board also required conversion to single-ended signals for compatibility with single-ended test equipment. Though on-board transmission-line circuits were an option, commercial, off-the-shelf, connectorized components were chosen to simplify characterization and to minimize board complexity. An Anaren 30057 4–6 GHz 180° hybrid was used to perform the single-ended-to-differential conversion at the RF input port, while an Anaren 30056 2–4 GHz 180° hybrid was used to provide the the differential LO signal from a single-ended source. At the IF outputs, Mini-Circuits (ZFSCJ-2-1) 1–500 MHz baluns performed the single-ended-to-differential conversion. A 4–8 GHz 10-dB Narda directional coupler (4014C-10) was inserted into the RF source chain to enable the monitoring of the input RF power with a power meter (HP-E4418B). The losses of each component within the test setup, including the cables, coupler, hybrids, and test board, were measured using the HP8510C network analyzer and accounted for in the post-processing of the measurement data.

As discussed in Section 2.2.2, the output impedance of the mixers was approximately 1.5 k $\Omega$  single-ended, in each branch, or 3 k $\Omega$  differential. In the test plan described above, this large impedance was terminated with the 50  $\Omega$  Mini-Circuits balun, resulting in poor power/voltage transfer. However, since the IF measurements were at relatively low frequencies (10–100 MHz), the impedance mismatch can be viewed as a voltage divider between the 100  $\Omega$  and 3 k $\Omega$  differential impedances. The measured IF quantities were therefore calibrated mathematically to the 3 k $\Omega$  differential output by treating this division ratio as a loss term and adding this loss back to the measured results when processing the data.

Agilent VEE code [134], a proprietary visual programming language (similar to Lab-View) for test equipment automation, was used to simplify the data collection process, allowing for a broad sweeping of data points over different ranges of mixer variables.

Applicable VEE code was written to assist with the following measurements:

- RF input return loss
- conversion gain vs. LO power and RF frequency, at different IFs
- conversion gain vs. RF power, at different IFs (1-dB compression)
- 2LO→RF isolation
- LO→RF isolation
- I/Q phase imbalance

Measurements of intermodulation products were conducted manually using a spectrum analyzer.

The mixers were designed to cover the three U-NII bands, 5.15–5.25 GHz, 5.25–5.35 GHz, and 5.725–5.825 GHz, but measurements were taken over the entire 5–6 GHz band since unaccounted for high frequency parasitics could change the frequency range of operation. The ability to apply modulated signals was not available; therefore, single-tone, continuous-wave (CW) signals were used for the RF and LO. The use of CW tones meant that a non-zero IF had to be employed — with a zero-IF signal, AC coupling the single-tone IF would have rejected the desired DC output signal. Alternatively, the output could have been DC coupled, but this would have affected the mixer DC bias current, potentially disrupting circuit operation. Another impediment to making measurements at zero-IF was the bandwidth of the available test equipment. For example, the lower cutoff frequency of the spectrum analyzer (HP 8563E) used for many of the measurements was 9 kHz; below this frequency, the analyzer’s own spectrum dominates. Therefore, a series of low IF frequencies were measured, ranging between 10–100 MHz.

To characterize the effects of the LO power level on mixer parameters like conversion gain, isolation, and I/Q phase balance, the LO power was swept from  $-15$  to  $+10$  dBm. For measurements such as 1-dB compression and intercept points, the LO power was fixed to a level where the I and Q mixer conversion gains were found to be approximately equal.

As mentioned in Section 2.2.2, each circuit had two DC supply rails: one for the RF transconductor and LO switching core ( $V_{CC}$ ), and one for current mirror biasing ( $V_{bias}$ ). The two different rails gave a post-fabrication capability of tuning the bias of each circuit if problems were encountered. For the I and Q mixers, each  $V_{CC}$  and  $V_{bias}$  rail was connected to its own DC supply (HP-E3631As), which were filtered using large 0.5 mF capacitors in parallel with large electrolytic capacitors ranging in value from 22  $\mu$ F to 100  $\mu$ F to reduce supply line noise. The DC rails of the LO chain (input buffer and two-stage output amplifiers) were tied together and connected to a single DC supply, separate from the mixers. To monitor the current draw, the  $V_{CC}$  rail of each mixer was connected through a digital multimeter (HP34401A) during testing.

## 3.2 Measured Results

### 3.2.1 Biasing

Initial measurements of the LO chain showed that it drew little current from the 3.3 V supply. Upon re-examination of simulation data, it was found that the mirror transistors that set the tail current of the two-stage amplifiers at the output of the polyphase filters had a very small  $V_{CE}$ , which placed the transistors on the edge of the saturation regime. While the circuit operated with this low voltage drop in the simulations, the lack of bias current drawn from the fabricated circuits suggested that the fabricated mirrors were not working properly. To increase the headroom, the LO chain was provided with a greater voltage supply for the  $V_{CC}$  and  $V_{Bias}$  pins of the input buffer and four two-stage amplifiers. The change in supply voltage increased the  $V_{CE}$  drop across the mirror transistors and allowed the devices to operate more fully in the active regime. Consequently, the DC supply voltage in the test setup was slowly increased until the LO chain amplifiers started to draw current, which occurred around 3.7 V. The voltage was increased further to find the optimum operating point for the LO chain. Beyond 4.3 V, the increase in bias current was minimal and the reliability of the devices under higher voltages became a concern. Therefore, the rail to the entire LO chain was raised to 4.3 V, i.e. 1 V above the designed value. The downside of this higher voltage was the increase in the power consumption of

Table 3.1: Simulated and measured bias currents for the single-ended LO mixers.

	I Mixer		Q Mixer	
	Simulated	Measured	Simulated	Measured
(V)	3.3	3.3	3.3	3.3
(mA)	5.01	5.11	5.01	4.94

Table 3.2: Simulated and measured bias currents for the differential LO mixers.

	Single-ended LO Chain		Differential LO Chain	
	Simulated	Measured	Simulated	Measured
(V)	4.3	4.3	4.3	4.3
(mA)	34.80	35.21	31.2	32.88

the LO chain, which was relatively high to start with in the original 3.3 V design. For the mixers themselves, the measured currents of the supply and bias rails were within  $100\ \mu\text{A}$  of the simulated values. Table 3.1 shows the simulated and measured supply voltages and currents for the mixer circuits while Table 3.2 shows the supply voltages and currents for the single-ended and differential LO chains. As can be seen, the differential input buffer was biased with 2.33 mA less than its single-ended counterpart — a contributing factor to the poor linearity of the differential buffers mentioned later in this chapter.

### 3.2.2 Input Matching

The input match of the RF and LO ports was measured using the HP8510C vector network analyzer (VNA). The test setup for the SLON mixers RF input match is shown in Figure 3.6(a) and the modified test setup for the DLON mixers is shown in Figure 3.6(b). The loss through the components leading up to the package pins attenuates the reflected signals. Therefore, the total loss leading up to the package was measured first and then added back into the return loss results, thereby de-embedding the packaged circuit response from that of the test setup.

Figure 3.7 shows the input return loss at the RF input of the SLON mixers across the 5–6 GHz band. The lower U-NII band return loss was shifted up in frequency by 115 MHz, and the upper U-NII band return loss by 45 MHz. The shift in frequency was likely due to unaccounted for parasitics within the layout, such as overlap capac-

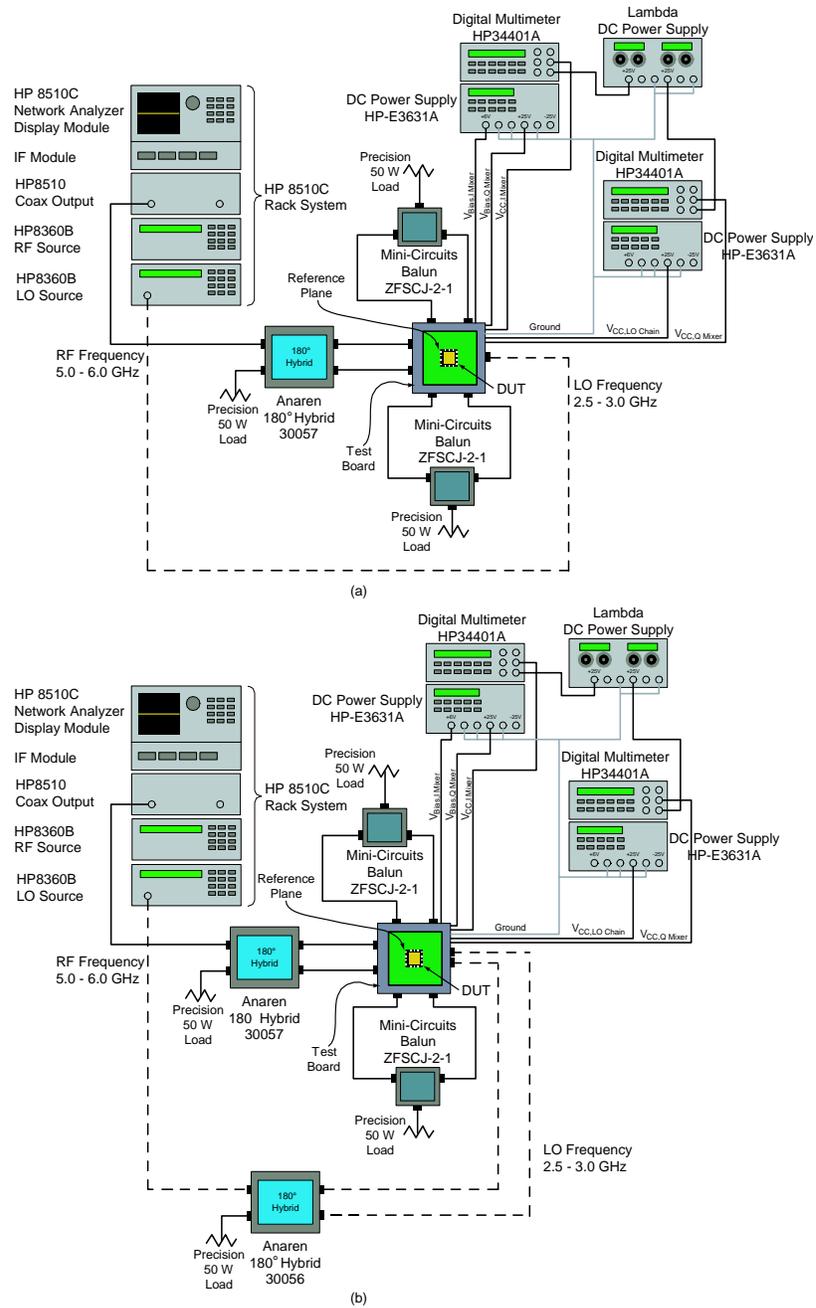


Figure 3.6: Block diagram of the RF input match test setup for: (a) the SLON mixers; (b) the DLON mixers. The Anaren 2–4 GHz 180° balun performs the single-ended-to-differential conversion of the LO signal in (b).

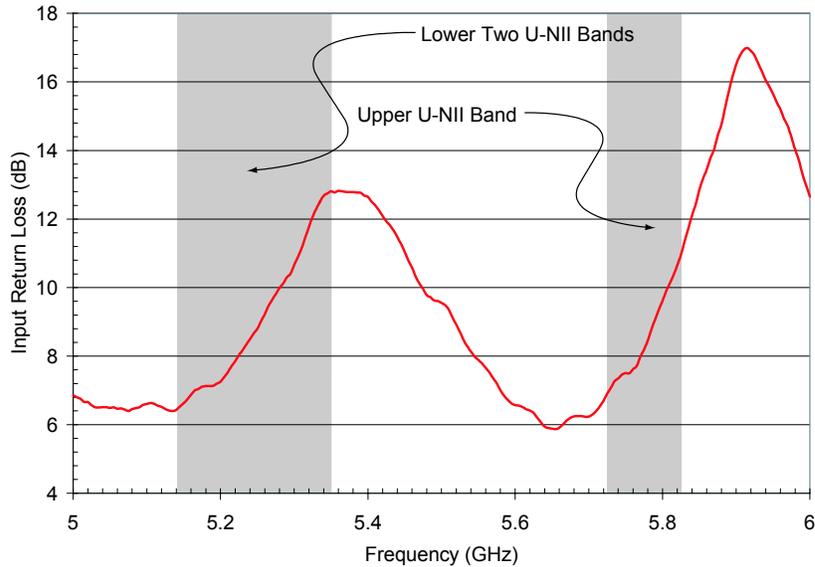
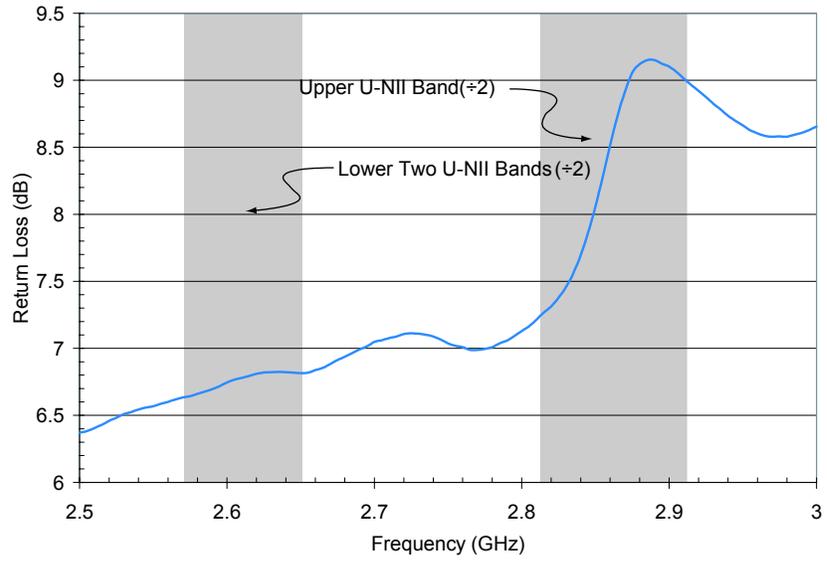


Figure 3.7: The SLON mixer measured RF input return loss over the 5–6 GHz band. The three U-NII bands are shaded in gray.

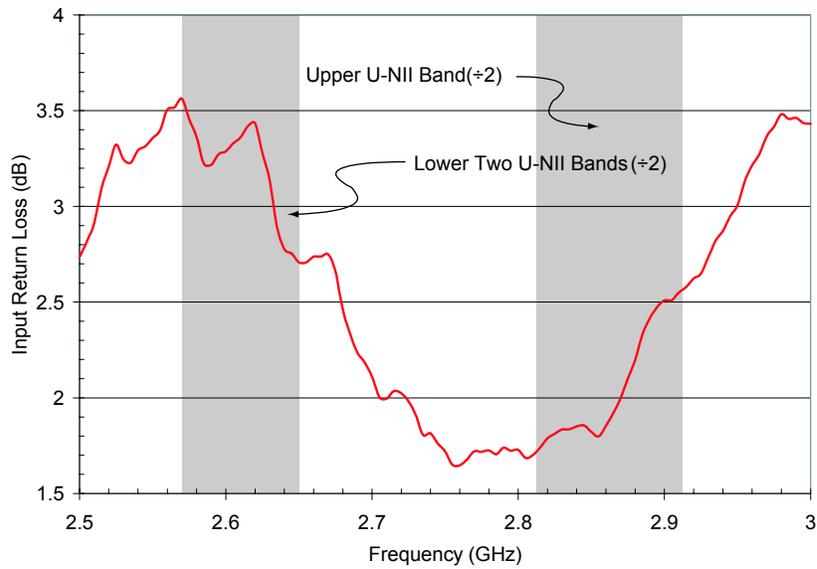
itances and trace resistances leading to the input of the mixers. For instance, since the standalone mixer die were the same size as the front-end die designed in Chapter 4, the RF inputs of the mixers were roughly 0.77 mm from the bondpads at the edge of chip; this distance was routed with simple metal traces.

The LO return loss for the single-ended LO input, which was measured at half the frequency of the RF across the three corresponding U-NII bands, was greater than 6 dB [Figure 3.8(a)]. In the case of the differential LO chain, the single-ended-to-differential conversion of the LO signal was accomplished off-board with the Anaren 2–4 GHz 180° hybrid (30056) as shown in Figure 3.6. The loss of this component was measured and de-embedded from the measured LO return loss [Figure 3.8(b)]. Otherwise, the test setup was the same as the SLON mixer setup.

The measured return loss of the RF port for the DLON mixers is shown in Figure 3.9. As was the case with the SLON mixers, better than 10 dB return loss occurred at a higher frequency range than was designed, with the lower U-NII band input match shifted by 155 MHz and the upper U-NII band by 90 MHz.



(a)



(b)

Figure 3.8: The measured LO input return loss over the 2.5–3 GHz band for (a) the SLON mixers and (b) the DLON mixers. The LO frequency ranges corresponding to the three U-NII bands are shaded in gray.

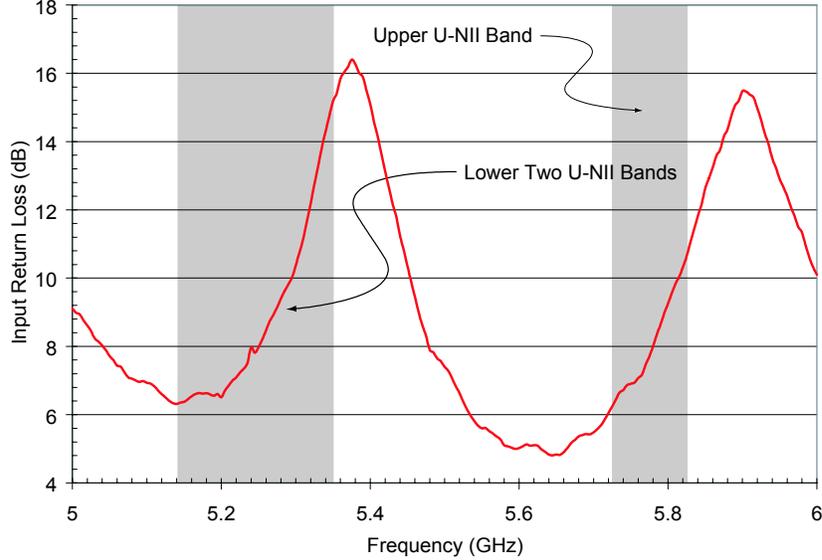


Figure 3.9: The DLON mixer measured RF input return loss over the 5–6 GHz band. The three U-NII bands are shaded in gray.

### 3.2.3 Conversion Gain

The conversion gain of the I and Q mixers was measured over the entire 5–6 GHz band at a range of LO powers and IF frequencies. The RF losses ( $L_{RF}$ )—including the cables, the  $180^\circ$  hybrid, the directional coupler, and the test board—the IF losses ( $L_{IF}$ )—including the cables and baluns—and the IF mismatch were de-embedded from the measured data, yielding the conversion gain of the packaged mixers. Equation 3.1 shows the calculation of the IF loss term,  $L_{IF,mismatch}$ , due to impedance mismatch at the output of the mixers.

$$L_{IF,mismatch} = -20 \log \left( \frac{\frac{100}{3000+100}}{\frac{3000}{3000+3000}} \right) = 23.8 \text{ dB}. \quad (3.1)$$

The conversion gain (in dB) was calculated as follows:

$$G = (P_{out} + L_{IF} + L_{IF,mismatch}) - (P_{in} - L_{RF}) \quad (3.2)$$

Figure 3.10 shows the basic test setup for the conversion gain measurements. Two spectrum analyzers, the HP 8573E and the HP E4411B, were used to measure the IF

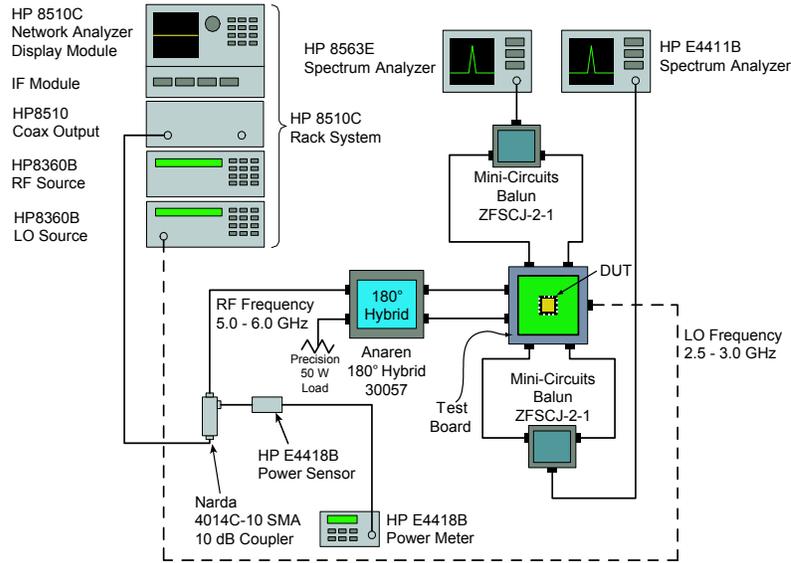


Figure 3.10: Test setup for conversion gain measurements. DC connections and instrument control/data acquisition interfaces are omitted for clarity.

outputs of the I and Q channels simultaneously. The HP8510C VNA was used to provide the small signal RF input at a power level of  $-32$  dBm while the HP8360B RF source provided the LO signal, ranging from  $-15$  to  $+10$  dBm.

Figure 3.11 shows the conversion gain of the I and Q SLON mixers versus LO power at an IF of 50 MHz and an RF of 5.2 GHz. The I and Q mixer gains were equal at an LO power of approximately  $-0.5$  dBm and differed by 0.2 dB at an LO power 0 dBm. As described in Section 2.3.1, the LO signal passed through a three-pole polyphase filter before reaching the Q two-stage, output amplifiers; on the I-side, the signal passed through a four-pole filter section before reaching the I amplifiers. By design, the I-side amplifiers had more gain than the Q-side amplifiers to compensate for the greater loss through the four-pole filter. However, the LO signal reached the inputs of the Q amplifier at a higher power level than on the I-side because of the lower loss through the three-pole filter. Therefore, the Q-side amplifiers compressed at relatively low LO signal power levels, which meant the LO signal was not fully amplified and the drive level reaching the mixer switching core was much smaller than expected. The compression of the Q-side amplifiers can be seen in Figure 3.11, where the Q mixer conversion gain rolls off above an LO power of approximately

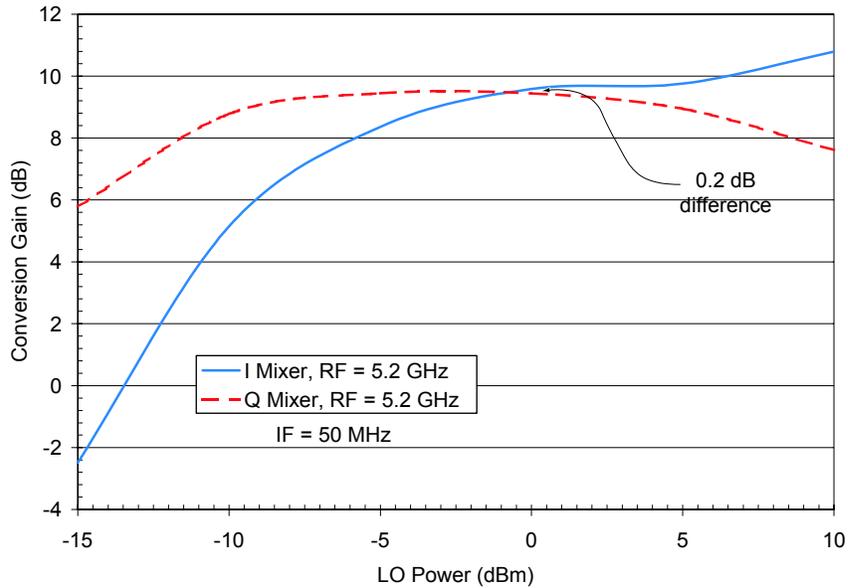


Figure 3.11: Conversion gain of the I and Q SLON mixers versus LO power at an IF of 50 MHz and an RF of 5.2 GHz. Other measurements are taken at the LO power of 0 dBm because the gain of each mixer is nearly the same.

-1 dBm; meanwhile, the I mixer conversion gain continues to increase up to an LO power of +10 dBm. The measured results for the I and Q mixers are similar to the simulated conversion gain of 9.7 dB presented in Section 2.5.

Figure 3.12 shows the conversion gain of the I and Q SLON mixers versus RF frequency at an IF of 50 MHz and an LO power of 0 dBm. The I/Q mixers provided 9–10 dB of conversion gain, over the lower two U-NII bands. The spike in the conversion gain of the I mixer in the upper U-NII band was observed over the same RF frequency range regardless of LO power or IF frequency. However, the circuit was damaged during other measurements before the cause of this discontinuity could be investigated further.

The conversion gain test setup for the DLON mixers was identical to that used for the SLON mixer setup with the exception of the 2–4 GHz 180° hybrid that performed single-ended-to-differential conversion prior to the LO port. The measurements were taken over the same ranges of RF and IF frequencies and LO power levels as described in Section 3.1.3. Equation 3.2 was applied to the measured results to de-embed the losses of the test setup. Figure 3.13 shows the conversion gain versus LO power at

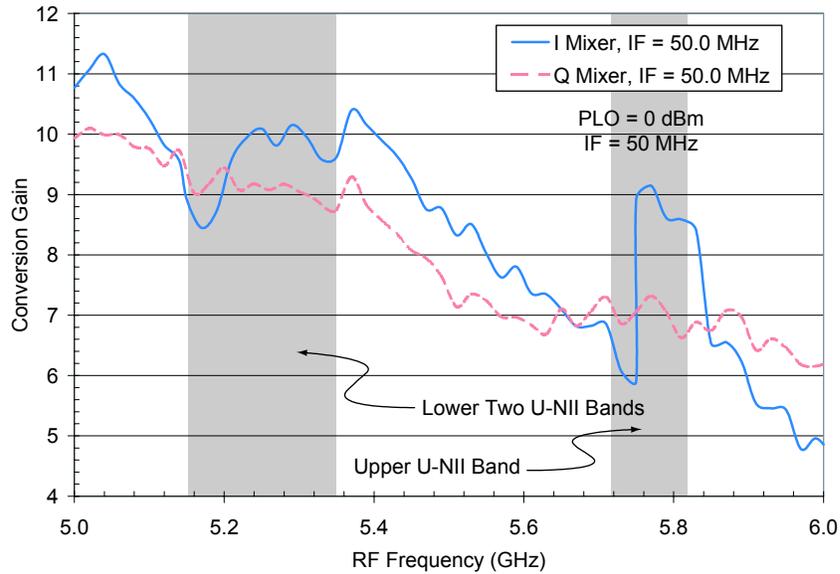


Figure 3.12: Conversion gain of the I and Q SLON mixers versus RF frequency at an IF of 50 MHz and an LO power of 0 dBm. The three U-NII bands are highlighted in gray.

an IF of 50 MHz and an RF of 5.25 GHz.

A significant problem with the differential LO chain was the linearity of the input buffer. The input buffer compressed when signals as small as  $-7$  dBm were applied to the input, which was a result of the buffer's poorly designed bias circuit. At higher LO power levels, the base bias circuit essentially clamped the base current, limiting the dynamic range of the buffer. Since good conversion gain performance of the mixers depends on the abrupt switching of its LO transistors, the small-signal swing of the LO signal led to a poor conversion gain. The compression effects of the input buffer are clearly seen in Figure 3.13 where the conversion gain decreases dramatically above  $-5$  dBm. The problem was exacerbated for the I mixer due to the extra loss within the I-side polyphase filter, which reduced the LO switching signal further.

Figure 3.14 shows the conversion gain of the DLON mixers versus RF frequency at an IF of 50 MHz and an LO power of  $-5$  dBm. Over the lowest U-NII band (5.15–5.25 GHz), the I mixer had virtually no gain; the gain improved to only 4–5 dB over the middle U-NII band; at the upper band, the gain rolled off from 3.5 dB to 0 dB and became negative in dB as the frequency increased further. The Q mixer was

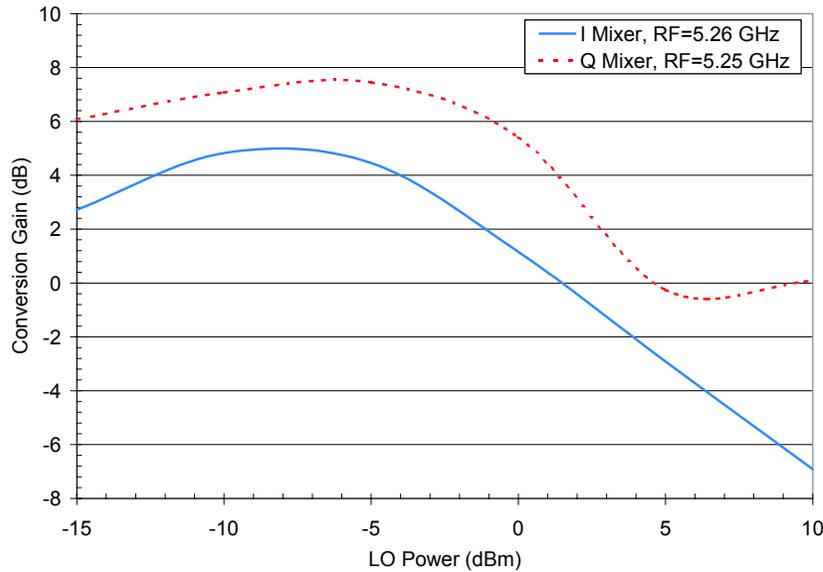


Figure 3.13: Conversion gain of the I and Q DLON mixers versus LO power at an IF of 50 MHz and an RF of 5.25 GHz.

slightly better, providing  $> 5$  dB of gain over the lower two U-NII bands and through the first third of the upper U-NII band, whereupon the mixer gain tapered off and became negative in dB at frequencies approaching 6 GHz.

As mentioned in Section 2.5, simulator convergence issues prevented completion of the DLON mixer simulations; the lack of simulator convergence was speculated to be the result of the poor linearity of the differential LO input buffer, which generated extra frequency components (harmonics and intermodulation products) that impeded the simulator convergence algorithm. The poor measured conversion gain performance of the DLON mixers presented here, particularly as the LO power is increased, supports this theory since the buffer is extremely nonlinear at LO power levels much higher than  $-7$  dBm.

### 3.2.4 Isolation

The test setup for the measurement of signal isolation at the RF port is shown in Figure 3.15. The LO was injected into the LO chain, and therefore into both the I and Q mixers, and the resulting leakage was sensed at the RF port. The 2LO-to-RF

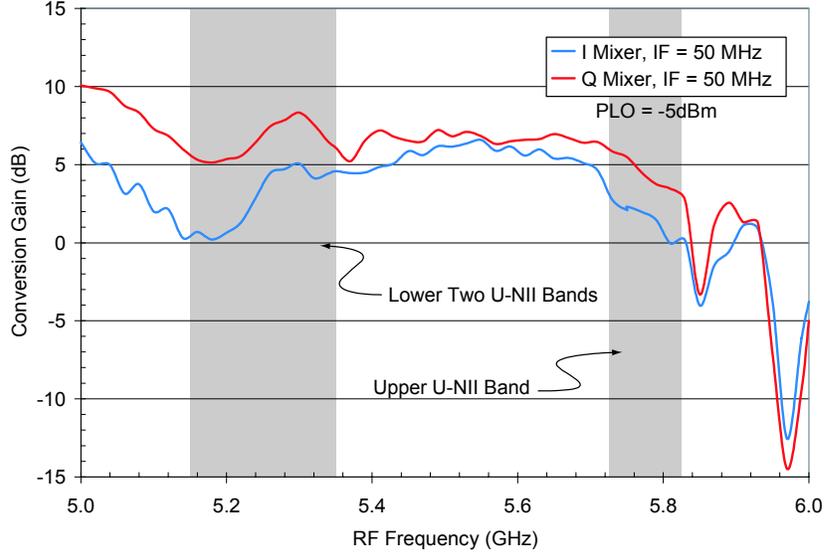


Figure 3.14: Conversion gain of the DLON I and Q mixers versus RF frequency at an IF of 50 MHz and an LO power of  $-5$  dBm. The three U-NII bands are marked in gray.

isolation was measured over the 5–6 GHz band with the 4–6 GHz Anaren  $180^\circ$  hybrid (30057) at the differential RF input, while the LO to RF isolation was measured over the 2.5–3 GHz band using the 2–4 GHz Anaren  $180^\circ$  hybrid (30056)<sup>3</sup>. The isolation ( $I_{SO}$ ) of the chip was de-embedded from the test setup using the following formula:

$$I_{SO} = (P_{RF} + L_{RF}) - (P_{LO} - L_{LO}), \quad (3.3)$$

where  $P_{RF}$  is the power measured at the RF port,  $P_{LO}$  is the input LO power, and  $L_{LO}$  is the total loss leading up to the LO input of the package, including cables, the hybrid (in the case of the DLON mixers), and the test board.

Figure 3.16 shows the measured 2LO-to-RF isolation of both the SLON and DLON mixers and Figure 3.17 shows the measured LO-to-RF isolation of the SLON mixers, all at an LO power of 0 dBm. Over the three U-NII bands, the SLON mixers had better than 54 dB of 2LO-to-RF isolation and better than 51 dB of LO-to-RF isolation, while the DLON mixers exhibited better than 52 dB of 2LO-to-RF isolation.

<sup>3</sup>Unfortunately, there was only one 2-4 GHz Anaren  $180^\circ$  hybrid available at the time this measurement was performed; thus, the LO to RF isolation of the DLON mixers could not be measured since this hybrid was also needed for the LO single-ended-to-differential conversion.

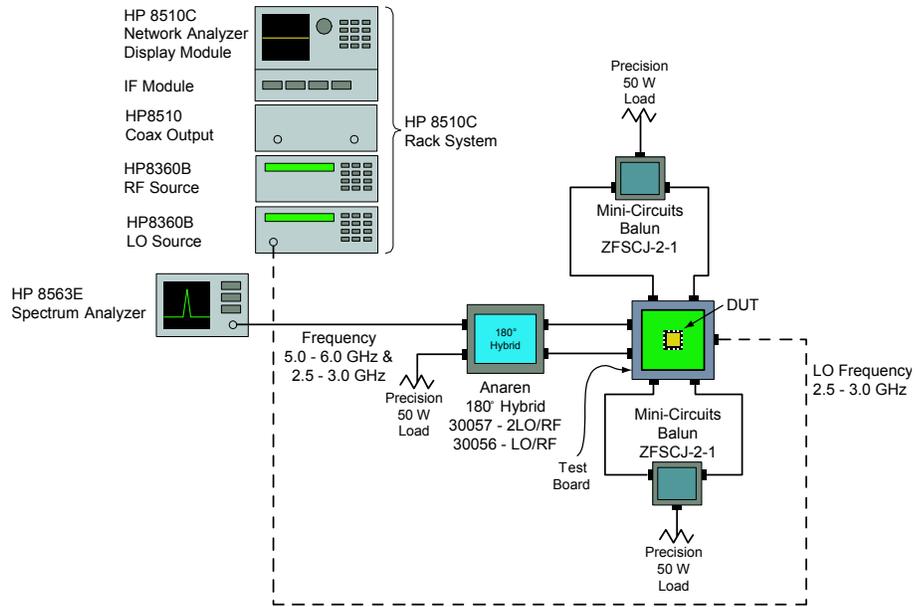


Figure 3.15: Test setup for the measurement of  $2LO \rightarrow RF$  and  $LO \rightarrow RF$  isolation.

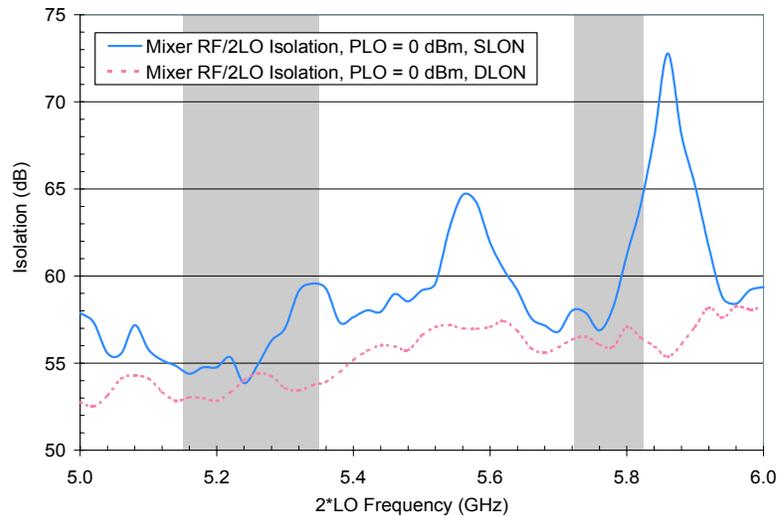


Figure 3.16: Measured  $2LO \rightarrow RF$  isolation of I/Q SLON and DLON mixers with LO power set to 0 dBm.

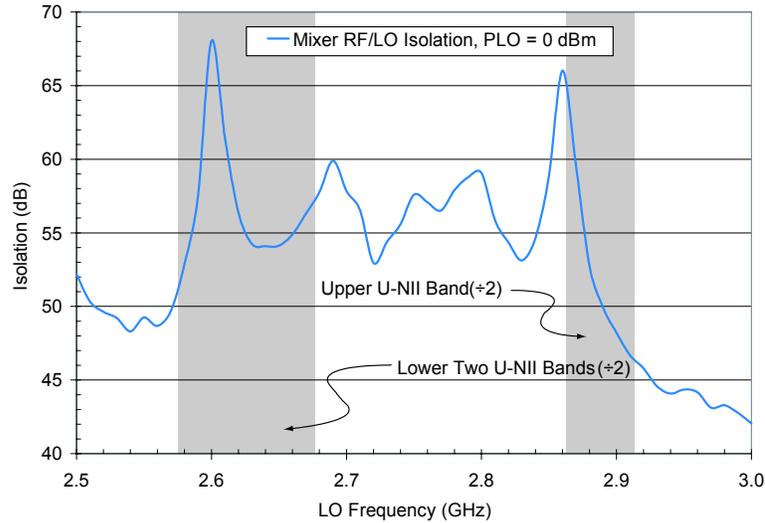


Figure 3.17: Measured LO→RF isolation of I/Q SLON mixers with LO power set to 0 dBm.

In order to be in compliance with FCC regulations for the U-NII band, spurious emissions above 1 GHz must be below  $-47$  dBm [135], a condition the sub-harmonic mixers meet since at least 50 dB of isolation is achieved. However, the effect of the 2LO→RF isolation performance on the reception of a signal is of greater interest and can be considered in terms of LO self-mixing and the resulting DC-offsets. With a 0 dBm LO signal and the worst case measured 2LO→RF isolation of 54 dB (at an LO frequency of 2.6 GHz), the signal present at the RF input of the mixers has a power level of  $-54$  dBm. This signal, after mixing with itself and undergoing a conversion gain of  $\sim 9$  dB, appears at the IF output of the mixers at  $-45$  dBm. Converting this to a voltage at the IF output impedance of the mixer ( $3\text{ k}\Omega$  differential), the resulting DC-offset due to LO self-mixing is  $\sim 13$  mV. The effect of this DC-offset level can be determined by considering a full receiver implementation, where the mixers would be followed by baseband amplifiers and filters and A/D converters. After the mixers, the signal would typically undergo an additional 50–80 dB of baseband voltage gain to achieve adequate SNR levels for conversion to the digital domain, resulting in a voltage level that would likely saturate the input of modern ADCs and mask the desired signal. Consequently, this isolation result seems to indicate that sub-harmonic mixing alone is not sufficient for the reduction of LO self-mixing. However, the isolation performance of the sub-harmonic mixers presented here is potentially degraded due to bondwire radiation and dummy metal-fill patterning.

Thus, such LO coupling paths need to be eliminated before sub-harmonic mixing can be completely effective.

### 3.2.5 Linearity

As discussed in Section 1.3.3, the two tone test is the most common method for measuring the linearity and intermodulation performance of RF circuits. For DCRs, both the second and third order intercept points are important as both second and third order intermodulation products can fall within the downconverted band.

The input third order intercept point of the mixers was measured with two tones spaced 2 MHz apart and centered at 5.25 GHz. The first tone,  $f_1 = 5.249$  GHz, was generated using an HP8510C while the second tone,  $f_2 = 5.251$  GHz, was generated by an HP8350B RF source. The two tones were combined with a 3.5–9.0 GHz Mini-Circuits power combiner (ZFSC-2-9G) at the input port of the RF hybrid and were monitored with the HP E4418B power meter, which sampled the power levels via a 10 dB coupler. By convention, intercept points are referenced to the input power level of one of the two-tones, which are equal in amplitude, in the measurement [75]. Therefore, the additional 3 dB input power resulting from the measurement of both tones at the power meter had to be calibrated out before the data was plotted. The packaged mixer was de-embedded from the test setup in the same manner as in the conversion gain measurements.

In this case, the offset frequency ( $\Delta f$ ) between the two tones was somewhat arbitrary since a particular wireless application (such as IEEE 802.11a, the IEEE standard for 5–6 GHz WLAN) was not specifically targeted by the design. However, based on the channel spacing dictated by the 802.11a standard [136], a  $\Delta f$  of 2 MHz was used to represent the adjacent edges of two 802.11a channels, as shown in Figure 3.18. The test setup is shown in Figure 3.19. The measurement was performed at an IF of 50 MHz with an LO power of 0 dBm. Figure 3.20 shows the plot of  $P_{\text{out}}$  vs.  $P_{\text{in}}$  and the linear extrapolation used for finding the intercept point between the fundamental and third order intermodulation product. From the measurement, the input IP3 of the SLON mixers is estimated to be +3.9 dBm.

Attempts were made to measure the input third order intercept point of the DLON

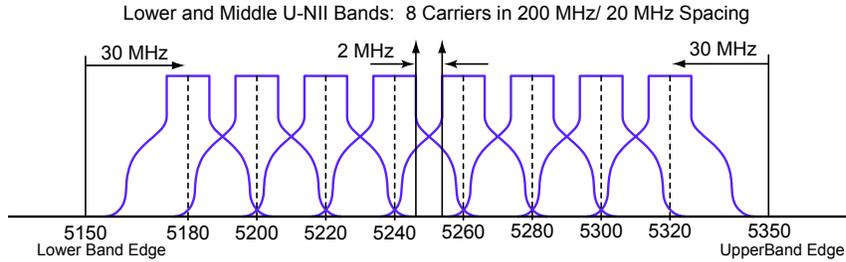


Figure 3.18: The OFDM physical layer frequency plan for 802.11a in the United States (after [136]). The vertical arrows indicated the band edges represented by with the 2 MHz offset.

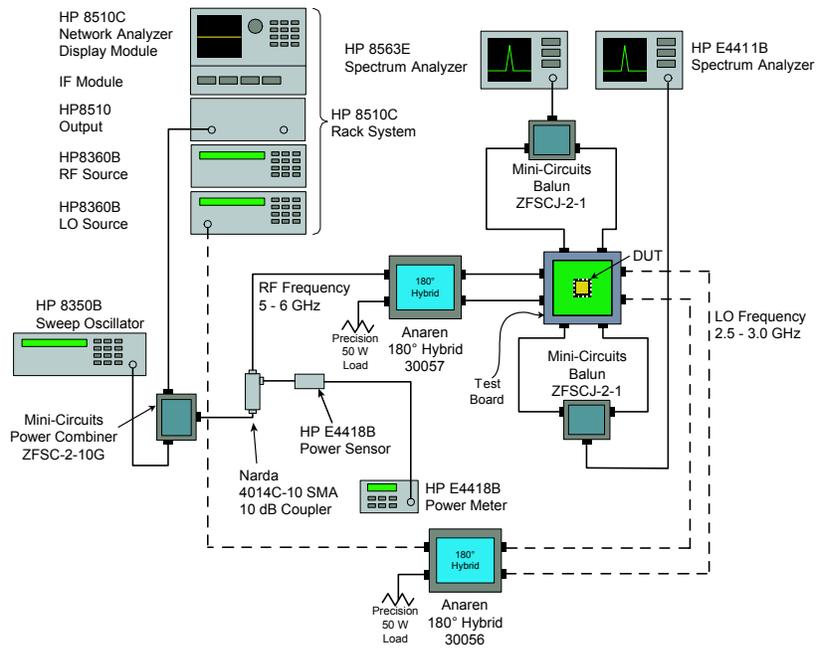


Figure 3.19: Test setup for measurement of second and third order intercept points. DC power supplies are omitted for clarity.

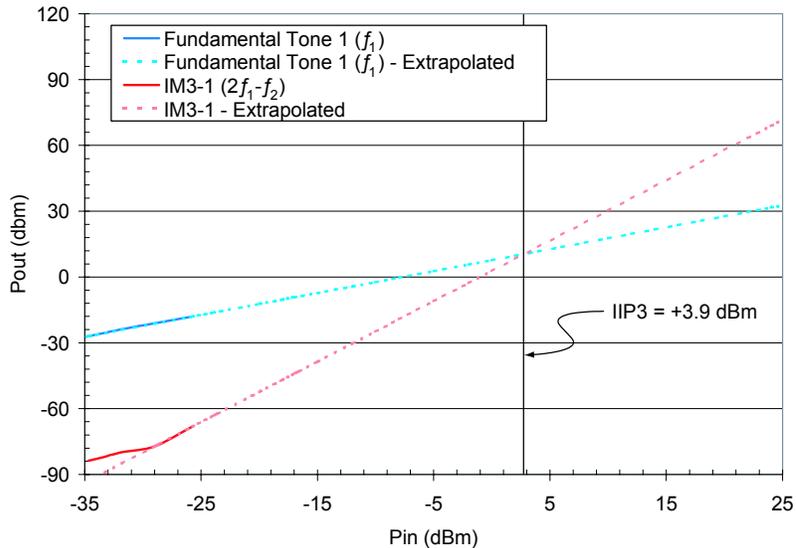


Figure 3.20: Input IP3 of the SLON mixers.  $RF_1 = 5.249$  GHz and  $RF_2 = 5.251$  GHz, IF = 50 MHz. The input-referred third order intercept point is +3.9 dBm.

mixers using the two-tone test; however, the measured results proved inconclusive because the low overall conversion gain resulted in third order products that were extremely low in power and difficult to measure. Therefore, the input IP3 was estimated by noting that the third order intercept point is related to the 1-dB compression point by a ratio of 9.6 dB [13].

The 1-dB compression point of the DLON mixers was found by measuring the IF output power while the input RF power was swept. The test setup for the compression measurements was identical to the conversion gain test setup except the LO power was fixed at  $-5$  dBm and the RF power was swept from  $-20$  to  $0$  dBm. Data was collected over the entire 5–6 GHz band at IFs ranging from 10–100 MHz. Figure 3.21 shows the extraction of the input compression point from the measured data. At an RF frequency of 5.25 GHz and an IF frequency 50 MHz, the input 1-dB compression point was measured to be  $-6.4$  dBm, which gives an estimated IIP3 of  $+5.15$  dBm. This IIP3 value is consistent with the measured value for the SLON case.

The second order intercept point was also measured using the two-tone test methodology. The first tone was set at 5.246 GHz while the second tone was at 5.254 GHz for a  $\Delta f$  of 8 MHz. The test setup is identical to the third order intercept point measurement. The tone offset of 8 MHz was chosen to circumvent the low-frequency

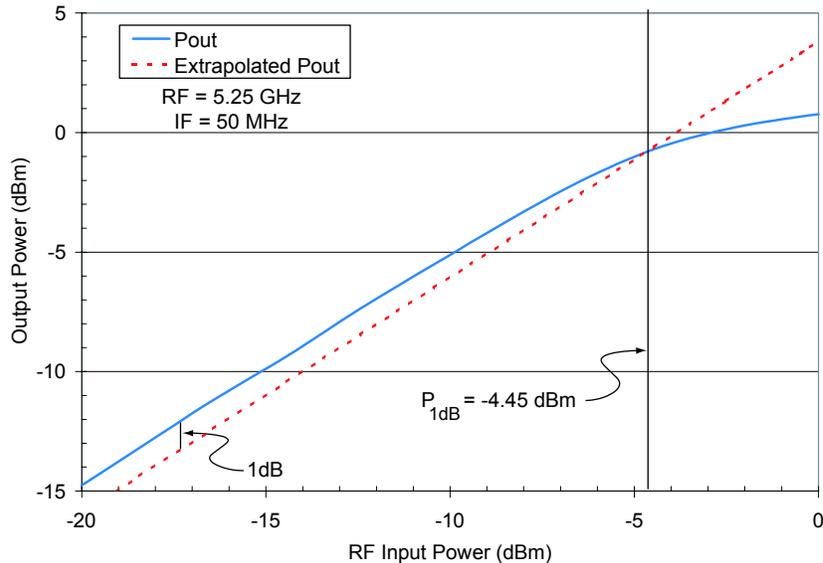


Figure 3.21: Measured RF input 1-dB compression point of the differential LO mixers at an IF of 50 MHz and an RF of 5.25 GHz. The input 1 dB compression point is -4.45 dBm.

noise-filtering limitations of the spectrum analyzer. Since the IM2 product of interest is located at  $f_2 - f_1$ , a smaller  $\Delta f$  would have placed the IM2 product closer to DC, where the noise floor of the spectrum analyzer is higher and could obscure the IM2 product to be measured. Figure 3.22 shows the measured IP2 of the differential LO mixers. At an IF of 50 MHz, with two RF tones at  $5.25 \pm 0.004$  GHz, and an LO power of  $-5$  dBm, the mixer input second order intercept point was estimated to be  $+23$  dBm.

The IIP2 performance of the DLON sub-harmonic mixers can be considered in terms of a nearby interferer, or blocking signal. Under worst-case conditions for a given system, a receiver must detect the desired signal at the specified minimum detectable input power level while a nearby interferer operates at the specified maximum input power level of the receiver. As an example, the specifications for 802.11a WLAN set the maximum input signal power level to the receiver to  $P_{in} = -30$  dBm and the minimum detectable signal power level (at the minimum data rate) ( $P_{sig}$ ) to  $-82$  dBm. Thus, the relative suppression of the IM<sub>2</sub> product ( $RS_2$ ), in comparison to the desired signal (i.e.  $RS_2 = IM_2 - P_{sig}$  in dBc), can be calculated in terms of

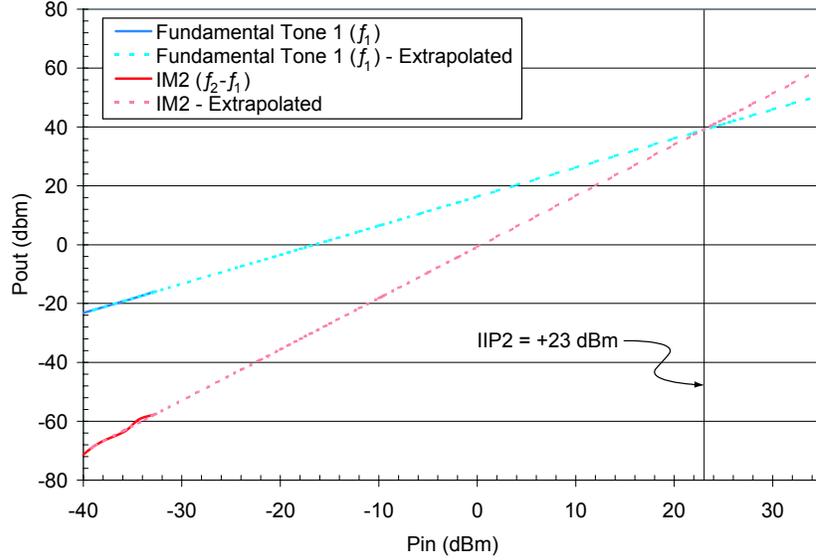


Figure 3.22: Input IP2 of the differential LO mixers.  $RF_1 = 5.246$  GHz and  $RF_2 = 5.254$  GHz,  $IF = 50$  MHz. The input-referred second order intercept point is estimated to be +23 dBm.

the measured  $IIP_2$  of the DLON mixer as follows:

$$\begin{aligned}
 IIP_2 &= 2P_{in} - IM_2 \\
 +23 &= 2P_{in} - (P_{sig} + RS_2) \\
 +23 &= 2(-30) - (-82) - RS_2
 \end{aligned} \tag{3.4}$$

$$\begin{aligned}
 RS_2 &= 2(-30) + 82 - 23 \\
 &= -1 \text{ dBc} .
 \end{aligned} \tag{3.5}$$

In other words, the resulting second order product is only 1 dB below the desired input signal, which means second order effects are not adequately suppressed. Consequently, second order products generated by this mixer design would have a significant impact on the ability of a receiver to detect low-power signals in the presence of interferers.

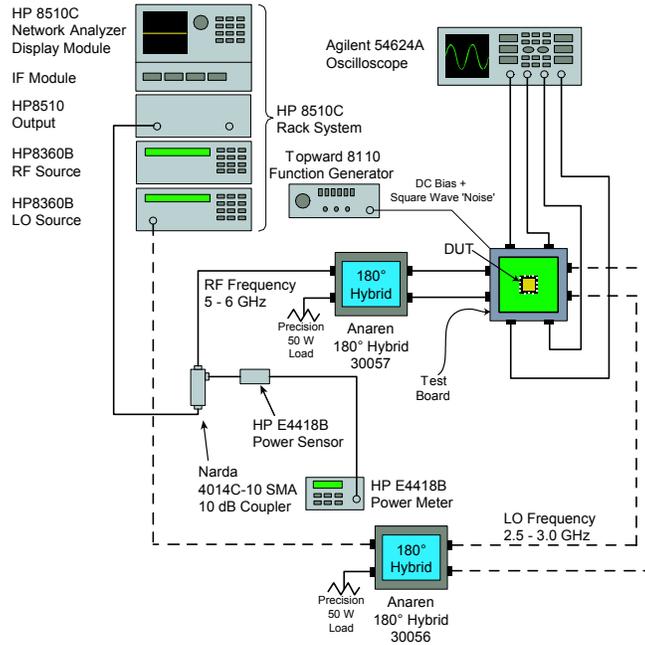


Figure 3.23: Test setup for the I/Q phase balance measurements. Power supply noise is injected onto the supply voltage lines using a waveform generator.

### 3.2.6 I/Q Phase Balance and Power Supply Noise

Figure 3.23 shows the test setup for the I/Q phase balance measurements. The 4-channel Agilent 54624A oscilloscope was used to measure the I/Q phase balance of the mixers over a range of LO power levels. To characterize the effects of an on-chip digital clock coupling into the supply voltage — a potential problem in SoC integration — a square wave of various peak amplitudes and frequencies was coupled into the voltage supply lines of the mixer. The simulated digital signal was produced with a standard waveform generator, which provided a simple method to adjust the frequency and amplitude of the signal on the supply line while measuring the phase balance between the I and Q channels.

For the SLON mixers, the best-case I/Q phase balance was measured to be  $60^\circ$  corresponding to an imbalance of  $30^\circ$ . This poor phase balance performance is attributed to the phase imbalance introduced by the single-ended-to-differential conversion. As mentioned in Section 2.5.2, the imbalance of the single-ended-to-differential input buffer affected the overall I/Q balance; though the imbalance in simulation was much

smaller, the effect was clearly visible. Therefore, further measurement of the SLON mixer I/Q phase balance was not attempted. For the DLON mixers, an I/Q phase balance of  $90^\circ$  was achieved by properly adjusting the LO input power level around the typical  $-7$  dBm value.

In Figure 3.24, the injected square-wave-noise frequency is swept from 10 Hz to 1 MHz; higher frequencies are not presented as the supply line decoupling capacitors shunted the noise to ground. The line labeled “Lambda” refers to the Lambda DC power supply in the benchmark case (no noise injected). Figure 3.25 shows the I/Q phase balance effects that resulted from amplitude noise variations in the supply to the mixer rails at 100 kHz (the results were similar at other noise frequencies). The noise amplitude was swept from 50 mV to 1 V; higher voltages began to affect the bias point of the circuit and stable phase readings were not attainable. Noise was also injected onto the LO chain supply rail, while the mixer rails were kept “noise-free.” In this second case, the noise had a much less significant effect on the I/Q phase balance. *Therefore, the I/Q phase imbalance is primarily the result of noise being introduced into the LO switching core of the mixer.* The mixers demonstrated relatively strong supply noise rejection, since a  $90^\circ$  I/Q phase balance could be achieved by adjusting the LO power by  $\pm 0.75$  dB.

### 3.3 Summary

This chapter presented the measured results for the fabricated SLON and DLON standalone  $\times 2$  sub-harmonic quadrature mixer circuits. In both designs, the I/Q mixer pairs consumed 10.2 mA of current from a 3.3 V supply for a total power dissipation of 33.6 mW. The single-ended LO chain consumed 34.8 mA from a 4.3 V supply (149.6 mW) while the differential design consumed 33.9 mA (141.4 mW). The larger 4.3 V supply was required in both cases to increase the headroom of the LO chain two-stage amplifiers, which had insufficient headroom at 3.3 V due to a design error.

The SLON mixer had better than 8 dB of conversion gain over the entire 5–6 GHz band and better than 50 dB of 2LO-to-RF and LO-to-RF isolation over all three U-NII bands. The tuning of the mixer RF input was shifted up in frequency, resulting

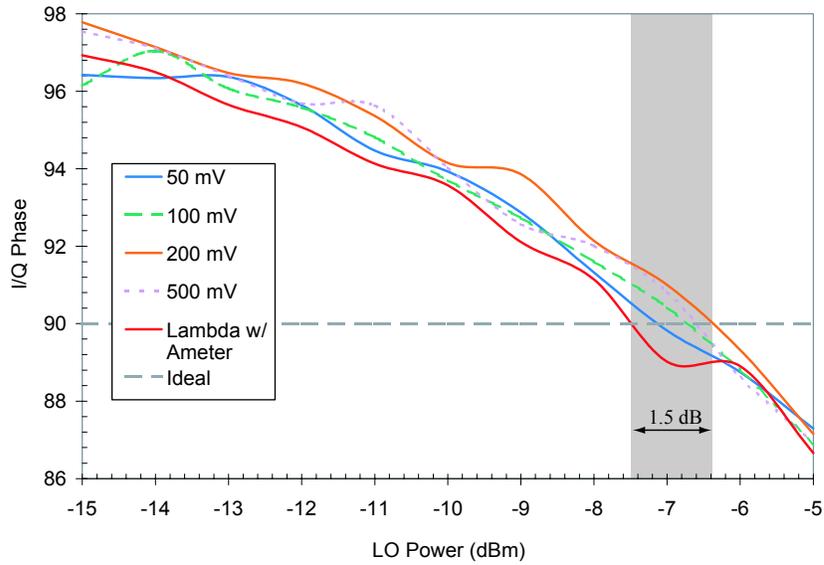


Figure 3.24: Measured I/Q phase balance of the DLON mixers versus LO power at an IF of 50 MHz. 90° balance is achieved in the presence of power supply noise (square wave) of varying frequencies.

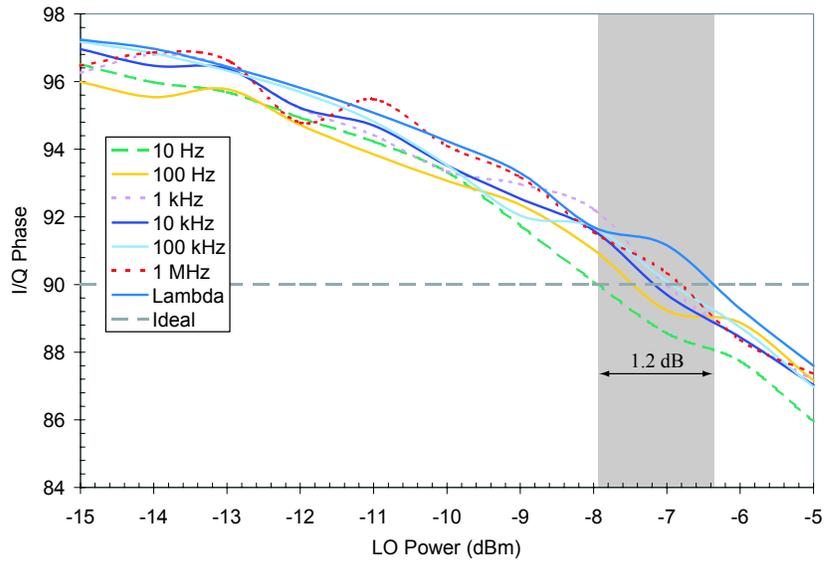


Figure 3.25: Measured I/Q phase balance of the DLON mixers versus LO power at an IF of 50 MHz. 90° balance is achieved in the presence of power supply noise (square wave) of varying amplitudes.

in an input return loss that ranged from 6 to 10 dB over the three U-NII bands. The IIP<sub>3</sub> of the SLON mixer was measured to be +3.9 dBm.

The DLON mixer conversion gain was hampered by the low compression point of the input LO buffer. The lack of linearity in the input buffer resulted in a small peak-to-peak pump signal at the mixer switching core, which lowered the overall gain. The I mixer performed best over the middle U-NII band where it had a conversion gain of 5 dB; the Q mixer was slightly better with  $\gtrsim 5$  dB conversion gain over both lower U-NII bands. The RF input match to the DLON mixers was also poor, with a return loss as low as 5 dB. Nonetheless, the fully differential nature of the design translated into a second order intercept point of +23 dBm and a 90° I/Q phase balance at a specific LO power. The phase balance was maintained in the presence of power supply noise of different frequencies and amplitudes by adjusting the LO power  $\pm 0.75$  dB.

Given that the typical RF front-end is responsible for roughly 25–30 dB of gain in DCR implementations [52], the measured 8–10 dB of conversion gain provided by the SLON mixers suggests that significant gain must be provided by an LNA if the sub-harmonic mixers are integrated into a full receiver design. However, a downside to incorporating an LNA with 20 dB of gain is that the IIP<sub>3</sub> of the SLON mixers would be scaled down significantly; in turn, the spurious-free dynamic range (SFDR) of the receiver would be limited. An increase in the conversion gain, or in the input IP<sub>3</sub>, would improve the suitability of the sub-harmonic mixers for high-speed wireless data networks.

The isolation performance of the SLON and DLON mixers was believed to be limited by bondwire radiation and unaccounted-for dummy metal-fill areas. Based on worst-case calculations, the DC-offsets due to LO self-mixing (a result of the limited isolation) are large enough to saturate the typical baseband circuitry in a DCR implementation. However, bondwire radiation would effectively be eliminated by using an on-chip VCO for the LO source and the effects of area-fill could be accounted-for in a subsequent design iteration. Therefore, the isolation of the sub-harmonic mixer design presented here is expected to be significantly improved once these issues are addressed.

With regards to the DLON mixer performance, the need to adjust the LO power to maintain 90° I/Q phase balance in the presence of switching noise is undesirable from a

system level design perspective, as the output power of the LO source — for example, an on-chip VCO — is not typically controllable. Furthermore, since the input buffer of the differential LO chain had an extremely low 1-dB compression point, which limited the LO pump signal to the mixer switching core, the conversion gain of the DLON mixers was very poor. In the case of the single-ended LO chain, the imperfect differential signal at the output of the single-ended-to-differential input buffer resulted in poor overall I/Q phase balance. For both LO chains, the limited linearity of the two-stage output amplifiers, in combination with the asymmetric pole configuration of the two polyphase filters, resulted in significant amplitude imbalances between the IF quadrature outputs. Together, the problems with the two LO chains suggest that an alternative method of quadrature LO generation, which allows for dynamic control of the I/Q balance, is required in high-speed mixed-signal SoC environments.

## Chapter 4

# 5-6 GHz $\times 2$ Sub-Harmonic Front-end Design and Simulation

**T**HE translation of the desired RF spectrum directly to zero-IF (DC) in a direct-conversion receiver suggests that the RF front-end can be very simple. Since baseband processing occurs immediately following downconversion, a direct-conversion receiver front-end can consist of as little as a low-noise amplifier, quadrature downconverters, and LO generation circuitry, such as a phase-locked VCO with polyphase filters. Figure 4.1 shows the overall block diagram for the front-end designed as part of this research, which builds on the I and Q sub-harmonic mixers and LO conditioning chain described in the previous chapters. The mixers and LO conditioning chain are combined with a differential LNA to form the receiver front-end. This chapter presents the design and simulation of the LNA, the integration of the LNA into the receiver front-end, and the simulation results for the overall fabricated front-end design.

### 4.1 Low-Noise Amplifier

The front-end low-noise amplifier is a critical component of wireless receivers. The LNA is not only responsible for amplifying the desired signal while introducing minimum additional noise, but also for largely determining the overall noise figure of the receiver chain. The importance of the LNA can be seen by examining Equation 4.1,

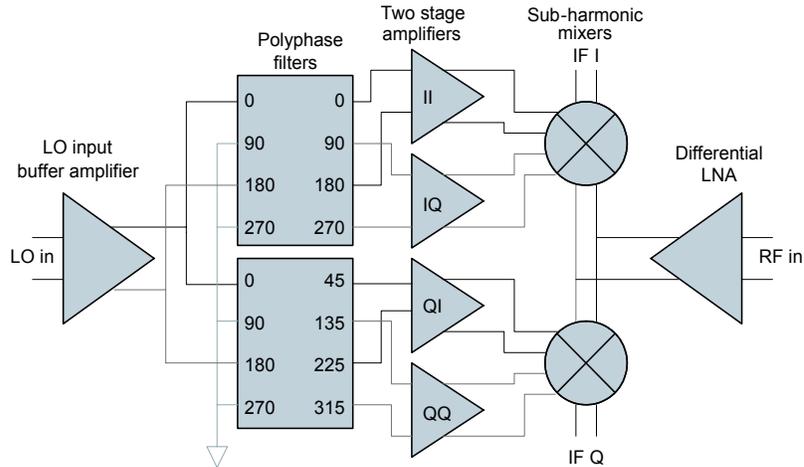


Figure 4.1: Block diagram of the receiver front-end.

by which the total noise figure for  $m$  stages in a cascaded system is determined from the noise figure ( $F^1$ ) and available power gain ( $G$ ) of each individual stage.

$$F_{tot} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_m - 1}{G_1 \dots G_{(m-1)}} \quad (4.1)$$

Notably, a significant amount of loss [linear gain ( $G < 1$ )] in the first stage of a receiver chain (i.e.  $G_1 < 1$ ) results in a poor overall noise figure while amplification ( $G_1 > 1$ ) by the first stage reduces the noise figure contribution of the following components in the chain. Of course, the reduction in noise figure due to a large  $G_1$  is offset by the noise figure of the first stage,  $F_1$ . Therefore, Equation 4.1 demonstrates the importance of having a low-noise, high-gain element at the front of the receiver, as opposed to a lossy filter or balun.

Historically, research on integrated LNAs has focused on unbalanced (or single-ended) topologies, which allow for very low noise figures at very low levels of power consumption [137–142]. Single-ended LNAs are also beneficial because they interface well with commercially available duplexers/band-select filters and switches (for switching the antenna between transmitter and receiver), both of which can precede the LNA depending on the intended application. However, differential circuits are generally favored in RF integrated circuits for their increased common-mode rejection and their

<sup>1</sup> $F$  is used to represent the *linear* noise figure of a component so as to distinguish it from noise figure in dB, which is represented here as  $NF$ .

reduced even-order distortion. Designers must therefore choose the point in the receive chain at which the circuitry converts from single-ended to differential. With a single-ended LNA input to the chip, the conversion to differential circuitry can be performed a number of ways, including: on-chip baluns [143], [144], single-balanced mixers [145], or with an off-chip, single-ended-to-differential image-reject SAW filter after the LNA [146]. Alternatively, the LNA can be designed as a two stage amplifier, with a single-ended input stage followed by a single-ended to differential amplifier stage (also known as an active balun) [147]. Unfortunately, none of these methods are optimum; substrate coupling, additional noise, and degraded second-order suppression are among the problems associated with performing single-ended-to-differential conversion on-chip. Furthermore, single-ended LNAs can be difficult to match due to their high sensitivity to parasitic ground inductance [58] (i.e., parasitic inductive emitter degeneration). An alternative approach is to use a differential implementation for the entire on-chip receive chain and perform the differential conversion either on the printed circuit board, as in [148], or using commercial, off-the-shelf components as in [149–151]. Clearly, in an ideal transceiver solution, all circuit blocks would be fully differential — from the antenna to the duplexer and RF band select filter to the LNA input — thereby eliminating the extra circuitry and/or components needed for conversion; however, high frequency differential switches and filter components are relatively new and still very expensive.

In this research, the interface between the LNA output and the differential inputs of the I/Q sub-harmonic mixers was simplified by using a fully differential LNA. This approach is also beneficial since it allows the differential conversion to be performed using a well characterized, off-chip method such as a commercial, off-the-shelf 180° hybrid. On-chip conversion to a single-ended input can be pursued in future work using one of the methods above. One potential disadvantage in using a differential LNA over a single-ended LNA designed in the same technology is that the power consumption is doubled in order to achieve the same noise figure; however, the improved linearity that results usually offsets this disadvantage [58].

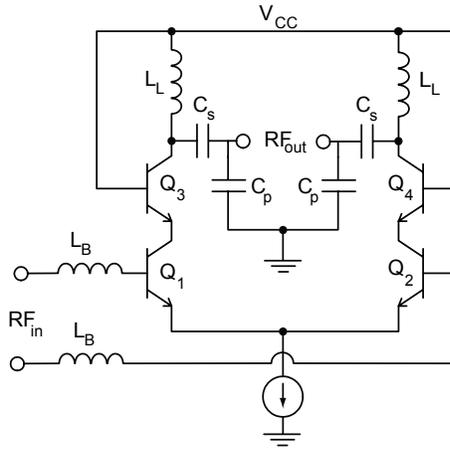


Figure 4.2: Simplified schematic of the differential LNA.

### 4.1.1 LNA Design

The LNA is based on the differential cascode structure shown in Figure 4.2. The addition of the common base transistors ( $Q_3$  and  $Q_4$ ) provides a significant improvement in reverse isolation, usually expressed in terms of the small-signal  $s$ -parameter  $s_{12}$ , between the LNA input and output. The improved reverse isolation has two benefits: first, a reduction in  $s_{12}$  corresponds to an improvement in the stability factor ( $K$ )<sup>2</sup> of the amplifier; and second, a reduction in LO leakage back to the antenna. This latter improvement is particularly important in direct-conversion receivers where the LNA is typically the only circuit block providing (in-band) isolation between the antenna and the LO source. As mentioned in Section 1.3.3, LO leakage back to the antenna can reflect back into the system and mix with itself, generating (potentially) time-varying DC-offsets.

Inductive emitter degeneration as described in Section 2.2.2 can be used to set the  $100\ \Omega$  differential input match ( $50\ \Omega$  single-ended) to the LNA. However, the real part of the single-ended input impedance, looking into each of the bases of the main

<sup>2</sup>The Stern stability factor ( $K$ ) characterizes the stability of an amplifier for any arbitrary load and source impedance, where

$$K = \frac{1 + |\Delta|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}||s_{21}|}$$

and  $\Delta = s_{11}s_{22} - s_{12}s_{21}$ . For  $K > 1$  and  $|\Delta| < 1$ , the circuit is considered unconditionally stable. That is, for any combination of load and source impedances, the circuit will not oscillate.

differential pair (transistors  $Q_1$  and  $Q_2$ ), is very close to  $50\ \Omega$  at 5–6 GHz for the  $20\ \mu\text{m} \times 0.5\ \mu\text{m} \times 2$  emitter devices; the  $50\ \Omega$  real part limits the effectiveness of emitter degeneration. In other words, adding inductors to the emitters of  $Q_1$  and  $Q_2$  of sufficient size to resonate with the  $C_{be}$  of each device at 5 GHz changes the real part of the input impedance and therefore, degrades the input match. Alternatively,  $C_{be}$  can be resonated with input series inductors  $L_B$  (for this design, 1.5 nH each) at the bases of the transistors to ensure a nearly real input impedance. Including these series inductors and eliminating the emitter degeneration term, Equation 2.8 can be rewritten as:

$$Z_{in} = \frac{v_{in}}{i_b} = r_b + j\omega L_B + \frac{1}{j\omega C_{be}}. \quad (4.2)$$

The downside of this approach is that the series input inductors have relatively poor  $Q$  factors ( $\lesssim 10$ ), which degrade the achievable isolation (due to signal-coupling between the coil and the low-resistivity substrate) and noise figure of the LNA. On the other hand, the simulated noise figure penalty was only 1 dB across the band when compared to an LNA without the series inductors; this degradation was deemed acceptable considering the improved input match. Furthermore, in the context of 802.11a WLAN specifications, the simulated noise figure was adequate as 802.11a requires a minimum noise figure for the receiver front-end of 8.6 dB<sup>3</sup>. Notably, the input bondwires to the chip contribute an additional 0.9 nH of inductance to the series match for a total input inductance of  $1.5\ \text{nH} + 0.9\ \text{nH} = 2.4\ \text{nH}$ .

The LNA differential output is loaded with inductors  $L_L$  (3.1 nH each), which provide approximately  $100\ \Omega$  of AC load impedance to improve the voltage gain ( $g_m Z_L$ ). These inductors also form part of an output L-C-C " $\pi$ " matching network (described in more detail below) that interfaces with the input of the quadrature mixers. The same biasing techniques used in the RF transconductor (Section 2.2.2) and the LO input buffer (Section 2.3.2) are used for the LNA.

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<sup>3</sup>The 802.11a specification states that the receiver must have a minimum sensitivity of  $-80\ \text{dBm}$  for a packet error rate (PER) of 10%. Assuming a direct-sequence spread-spectrum implementation — where each channel is 22 MHz wide — and a minimum  $SNR$  of  $\sim 10\ \text{dB}$  for accurate data detection, the maximum acceptable noise figure for the receiver front-end can be calculated as:

$$NF_{max} = 174\ \text{dBm/Hz} - 10\log_{10}(22\ \text{MHz}) - 80\ \text{dBm} - 10\ \text{dB}$$

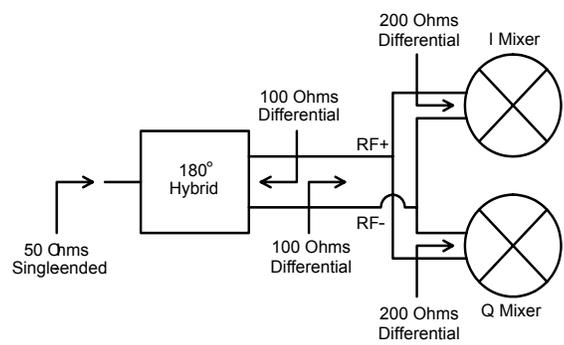
where  $[-]174\ \text{dBm/Hz}$  is the Johnson noise ( $kT$ ) in a 1 Hz bandwidth. Adding an extra 2 dB for the loss of the front-end band-select filter, the maximum noise figure is 8.6 dB.

### 4.1.2 LNA/Mixer Matching

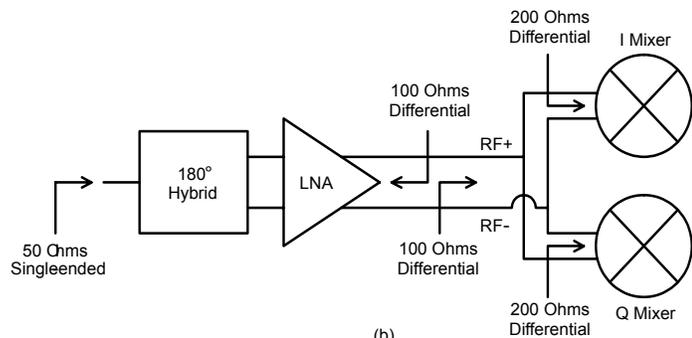
In a superheterodyne receiver, the off-chip image reject filters (IRFs) can lead to particular impedance-matching requirements between the LNA output and the filter input, and between the filter output and the mixer input since the quality of these matches can directly affect the performance of the filter [65]. Conversely, the elimination of the IRF in direct-conversion (and low-IF) receivers allows for direct, on-chip matching between the LNA and the mixers. Thus, as an example, the impedance between the inputs of a quadrature mixer pair and the output of an LNA can be optimized for gain and linearity without concern for bondwire or package parasitics or matching to off-chip components.

For the RF front-end in this work, the RF output of the LNA is fed to the inputs of both the I and Q mixers, which appear as impedances in parallel. Since the two mixers are ideally identical, the impedance presented to the LNA is half the input impedance of each individual mixer. The value of the impedance between the LNA and the mixers is relatively arbitrary and can be optimized through simulation. However, as described in Chapter 2.2.2, additional circuits were to be fabricated without the LNA to allow for the full characterization of the mixers alone. In order to accurately measure the standalone mixers in a single-ended  $50\ \Omega$  system, their parallel input impedance was set to  $100\ \Omega$  differential. In other words, the input impedance of each mixer was designed to be  $200\ \Omega$  differential, resulting in a parallel combination of  $100\ \Omega$ . To ensure that the standalone mixers would be directly comparable with the receiver front-end, the  $100\ \Omega$  parallel input impedance of the mixers was maintained for the front-end design and the LNA output was matched to this impedance. Figure 4.3(a) illustrates the impedance levels used for the standalone mixer designs of Chapter 2.2.2 while Figure 4.3(b) shows the impedance levels selected for the LNA and the mixers.

Recall that for the standalone mixer circuits, the  $200\ \Omega$  differential input impedance was set by the emitter degeneration using  $2.1\ \text{nH}$  inductors. This value of inductance is somewhat high and lowers the overall conversion gain; however, as explained in Section 2.2.2, the higher value also helps linearity. The series bondwire inductance, which was modeled during the simulation as described in Section 2.5.1, contributes to the standalone mixer input match as well.



(a)



(b)

Figure 4.3: RF matching: (a) standalone mixer impedances; (b) LNA and mixer impedances.

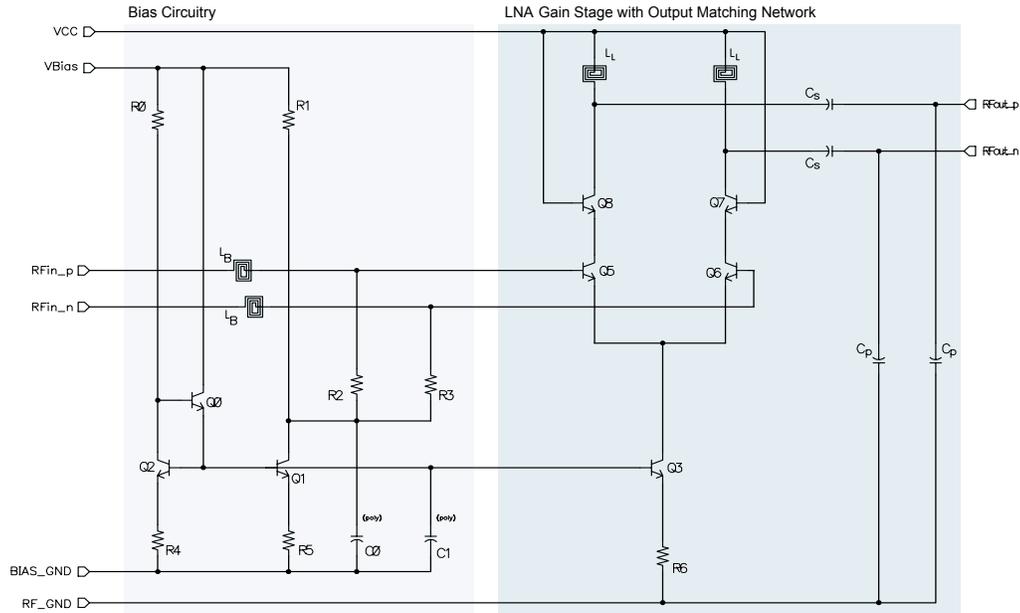


Figure 4.4: Full Cadence schematic of the differential LNA.

For the receiver front-end, the RF input bondwire inductance feeds the LNA instead of the mixers. Therefore, the matching condition between the LNA and quadrature mixers is  $100\ \Omega$  differential with a small amount of additional capacitance. To control the bandwidth of the impedance matching, a  $\pi$ -network is used at the output of the LNA; the network is designed to match the LNA output to the mixer inputs and consists of the  $3.1\ \text{nH}$  load inductors ( $L_L$ ),  $180.5\ \text{pF}$  series capacitors ( $C_S$ ), and  $180.5\ \text{pF}$  shunt capacitors ( $C_P$ ). The full Cadence schematic of the LNA is shown in Figure 4.4.

## 4.2 LNA and Front-end Layout

The front-end layout is identical to the standalone mixer layouts presented in Section 2.4 with the addition of the LNA at the RF input. Consequently, the same package and package models could be used for the front-end design as well. The four inductors of the LNA require a large amount of chip real estate, consuming at least a third of the total die area; other than the inductors, the LNA layout is small and compact. Figure 4.5 shows the layout of the LNA section alone. The  $V_{CC}$  trace wraps around

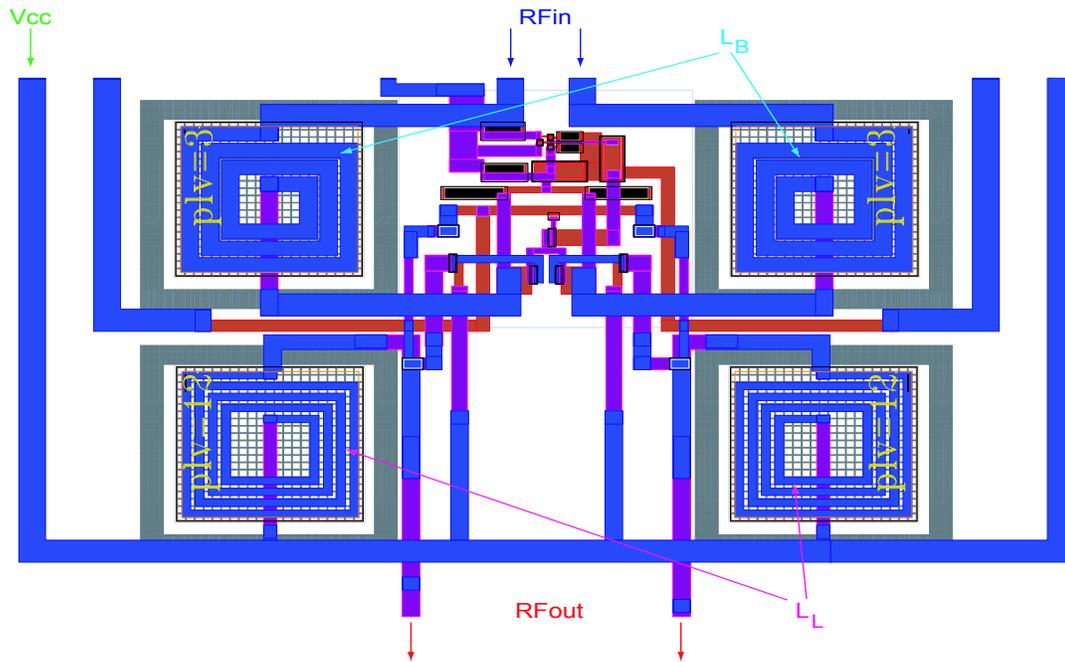


Figure 4.5: Layout of the cascode LNA.

the entire LNA to keep parasitics balanced and is realized as a  $20\ \mu\text{m}$  wide line in "last metal" (see Section 1.2.3) to provide a low-resistance path. The bias circuitry is placed between the RF inputs and the main differential pair, with the input and output of the LNA appearing on the inside of the inductors. Lattices of deep trench isolation are placed around the LNA inductors to improve the substrate isolation and to reduce signal coupling between the components. The circuit is as symmetric as possible about the vertical centerline of the layout to maintain the balance of the differential signals.

The LNA layout is placed at the RF input of the standalone mixer layouts to realize the front-end; Figure 4.6 shows the LNA with the SLON mixers. A similar layout with the DLON mixers is identical, but with a differential LO input. In both cases, the die size is the same as that of the standalone mixer die ( $2.3\ \text{mm} \times 1.8\ \text{mm}$ ).

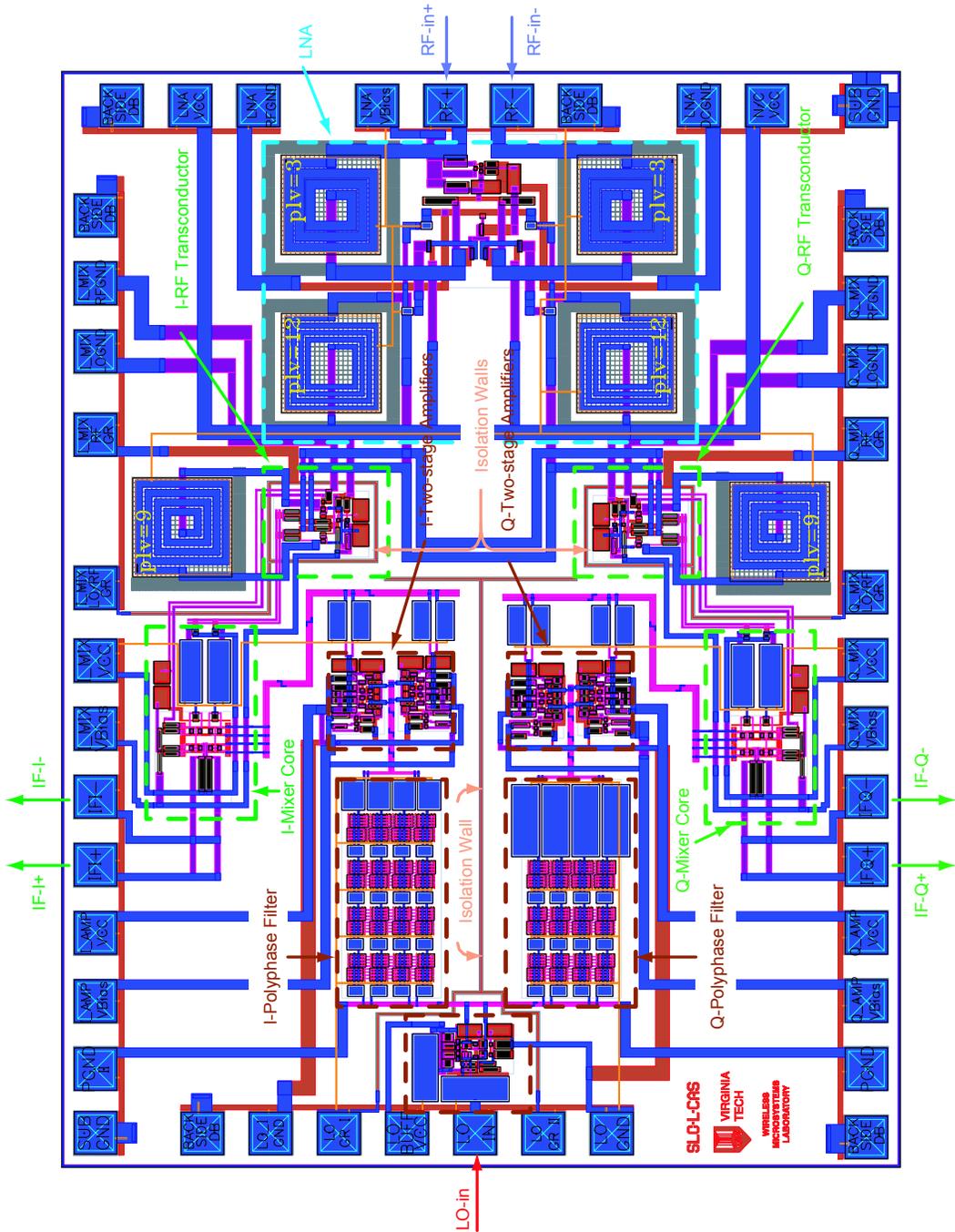


Figure 4.6: Detailed layout of the receiver front-end with single-ended LO input (SLON mixers) (2.3 mm × 1.8 mm).

### 4.3 LNA Simulation

The simulation of the LNA included both small-signal  $s$ -parameters — for small-signal gain, impedance matching, and noise figure — and harmonic balance analysis — for large signal effects such as 1-dB compression and intermodulation distortion. An ideal  $180^\circ$  hybrid was used to convert the single-ended RF source to a differential input to the LNA for the simulations. The packaging and bondwire models used in the standalone mixer simulations (described in Section 2.5.1) were also used with the LNA, since the die size and packaging of the front-end circuit were identical to those of the mixers.

Figure 4.7 shows the results of the  $s$ -parameter simulation of the cascode LNA. The LNA has a simulated small-signal gain of greater than 20 dB over the three U-NII bands and a noise figure of less than 3.6 dB. The input return loss is greater than 10 dB over the upper two U-NII bands and better than 12 dB over the lower U-NII band range. The input match can be improved by increasing the series input inductors ( $L_B$ ) but at the expense of noise figure, gain, and chip area. The minimum input to output isolation was simulated to be 57 dB.

### 4.4 Front-end Simulation

The LNA was coupled to both the single-ended and differential LO chain versions of the standalone mixers, and the circuits were denoted as SLO and DLO, respectively (the “N” in SLON and DLON was dropped since the circuit now incorporates the LNA). However, the simulation results of the DLO version are omitted since, as described in Chapter 5, this version was never fabricated. As in the case of the standalone mixer simulations, harmonic balance in ADS was used to determine the operation of the receiver. Again, a non-zero IF was used to help simulator convergence.

Figure 4.8 shows the simulated conversion gain (CG) and noise figure (NF) of the SLO RF front-end at RF frequencies of 5.15 GHz and 5.35 GHz, the upper and lower edges of the lower two (contiguous) U-NII bands. At an LO power of 0 dBm, the simulations show a front-end conversion gain of 26 dB and a noise figure of 7.5 dB at both RF

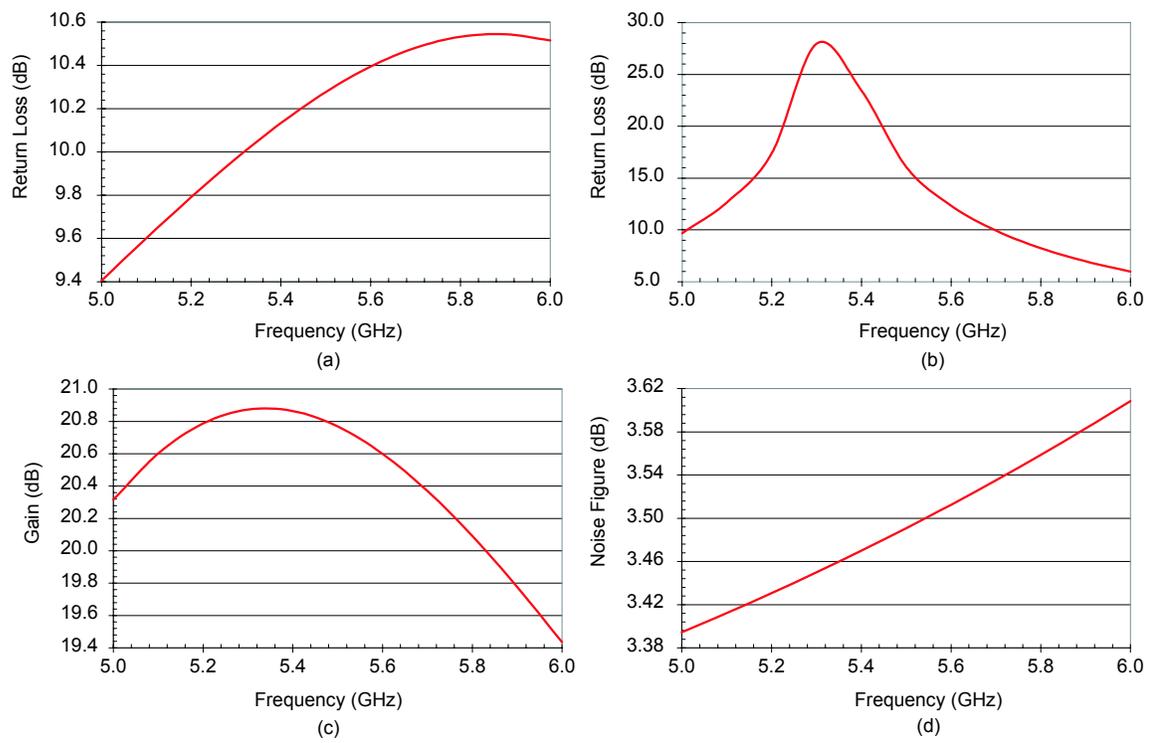


Figure 4.7: *S*-parameter simulation of the cascode LNA: (a) input match, (b) output match, (c) small-signal gain, and (d) noise figure.

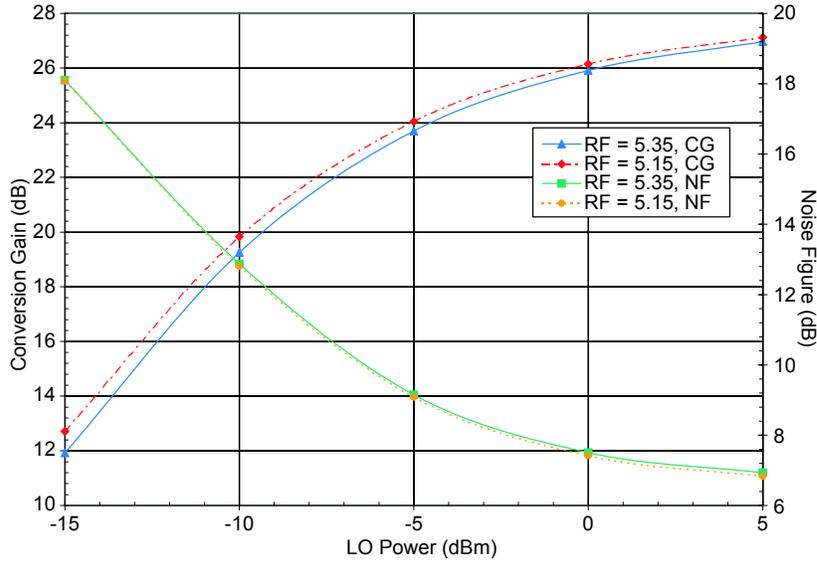


Figure 4.8: Simulated conversion gain and noise figure of the RF front-end. RF frequencies of 5.15 GHz and 5.35 GHz were downconverted to an IF of 10 MHz.

frequencies. The 1-dB compression point was simulated to be  $-20$  dBm. Simulation of the third order intercept point for the full RF front-end was not attempted due to lack of computing resources. Compared to the mixer simulations in Chapter 2, the LNA lowers the overall noise figure of the mixers by roughly 3 dB, from 10.5 dB to 7.5 dB.

The results of the I/Q phase balance simulation are shown in Figure 4.9. An ideal phase balance of  $90^\circ$  was achieved at an LO power of  $-5.5$  dBm with  $\pm 1^\circ$  phase error over the  $-9$  to  $+5$  dBm LO power range. This result is similar to the simulated result of the I/Q phase balance for the SLON mixers in Chapter 2, where  $\pm 1^\circ$  phase error was maintained over an LO power range of  $-8$  to  $+5$  dBm. Since the LNA should not have a significant impact on the IF phase balance, little difference was expected between the SLON and SLO simulated results.

## 4.5 Summary

This chapter presented the design, simulation, and layout of a 5–6 GHz range cascode LNA, and the integration of this LNA with the quadrature sub-harmonic mixers from

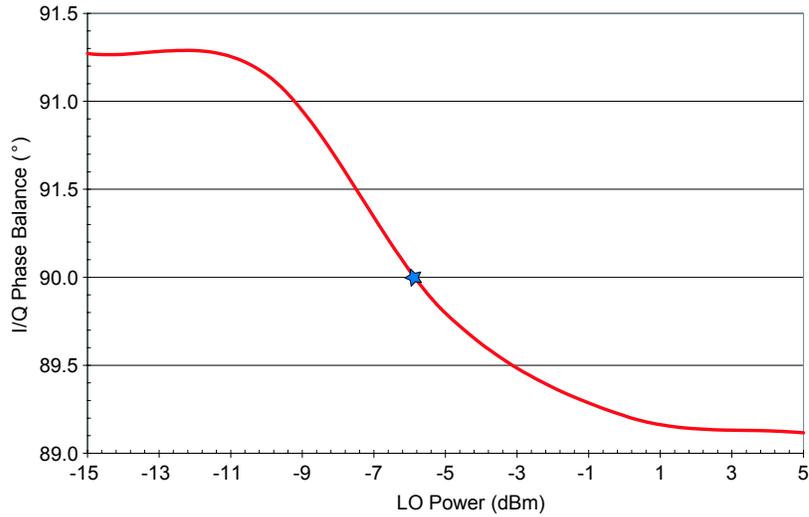


Figure 4.9: Simulated I/Q phase balance. The star marks the perfect  $90^\circ$  balance achieved at an LO power of  $-3.8$  dBm.

Chapter 2. Simulations of the LNA showed a small-signal gain of 20 dB, a noise figure of less than 3.5 dB, return loss of better than 10 dB, and a minimum reverse isolation of 57 dB. The simulated input 1-dB compression point was  $-20$  dBm. The LNA was designed for operation from a 3.3 V supply and package parasitics were included early in the design process. The LNA was matched to the inputs of the I and Q sub-harmonic mixers, which were in parallel and presented a  $100\ \Omega$  impedance to the LNA. Simulated results for the SLO receiver front-end showed an overall conversion gain of at least 22 dB with a noise figure between 6.5 and 7.2 dB over the lower two U-NII bands (5.15–5.35 GHz). The I/Q phase balance of the SLO front-end was simulated to be  $90^\circ$  at an LO power level of  $-5.5$  dBm.

## Chapter 5

# 5-6 GHz $\times 2$ Sub-Harmonic Front-end Fabrication and Measurement

**T**HIS chapter presents the measured results for the fabricated direct-conversion receiver front-end design. As was the case with the standalone mixers, the layout for the receiver front-end was submitted to RFMD, integrated into a 5HP engineering mask-set, and sent to IBM for fabrication. The metal fill and pattern density issues described in Section 3.1.1 also applied to the front-end design here. As mentioned in Chapter 4, two separate front-end circuits were designed: one where the LNA coupled to the RF input of the SLON mixer circuit and the other where the LNA was coupled to the DLON mixer circuits<sup>1</sup>. However, due to limitations in available reticle space, only the SLO design was initially fabricated; the DLO version was planned for fabrication on a subsequent engineering mask-set. Unfortunately, due to changes in strategy at RFMD, another engineering mask-set in IBM 5HP was never developed. As a result, the DLO design was never fabricated; the measured results presented below are for the front-end with the differential LNA design coupled to the single-ended LO chain I/Q mixers.

The  $\times 2$  sub-harmonic SLO front-end was fabricated, packaged, and mounted on the

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<sup>1</sup>As mentioned above, the new designation for these circuits were SLO and DLO, dropping the “N” since the LNA was included.

test board in the same manner as described in Section 3.1.2. Because the standalone mixers and the front-end used the same type of package and had the same die-to-package-pin connections, the testboard design that was used for the standalone mixers was also used for the receiver front-end. A photo of the fabricated die is shown in Figure 5.1(a) and a photo of the open-packaged die is shown in Figure 5.1(b).

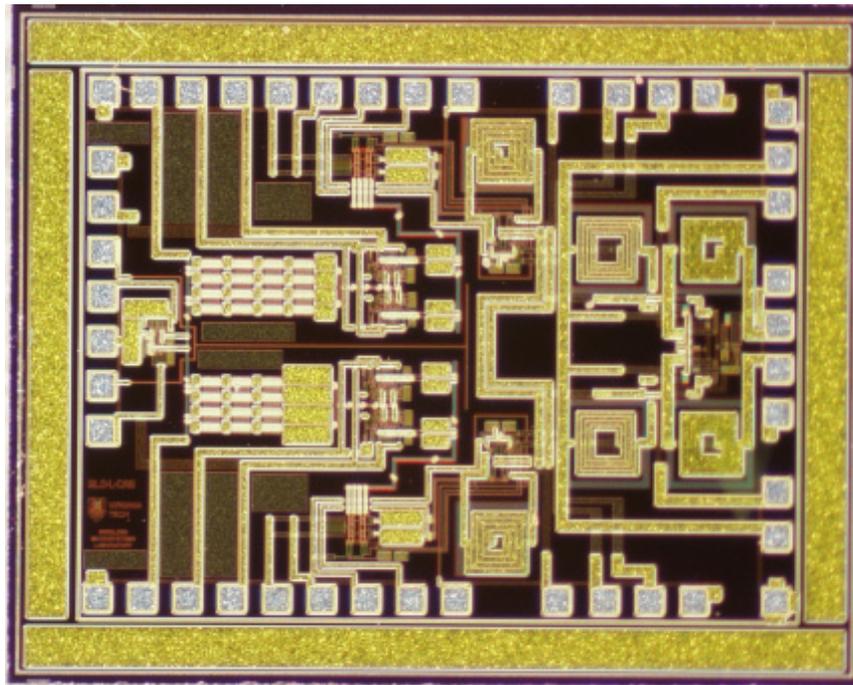
## 5.1 Measured Results

Other than the additional DC supplies required for biasing the LNA, the same basic test setup and VEE programs were used for the measurements of the SLO front-end. However, in addition to input matching, conversion gain, isolation, linearity, and I/Q phase balance, which were also measured for the standalone mixers, measurement of the DC-offsets and noise figure for the front-end was completed as well.

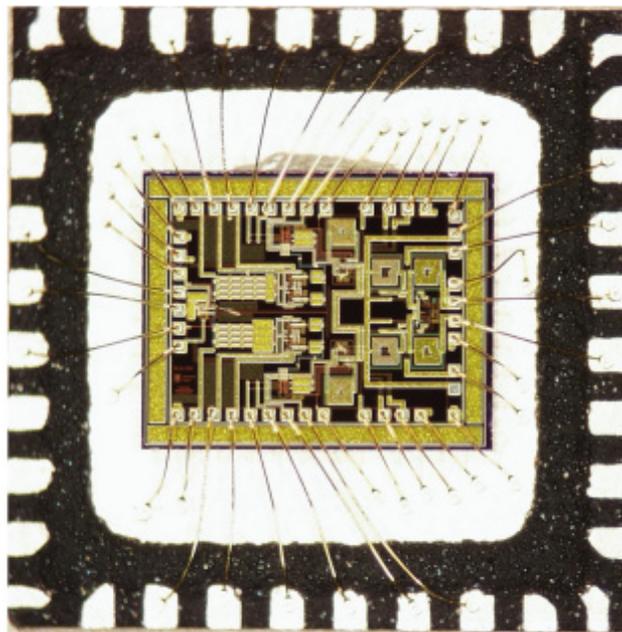
### 5.1.1 Biasing

As was the case with the standalone mixers, the supply voltage rail for the LO chain of the front-end had to be increased from the design value of 3.3 V to 4.3 V to provide sufficient headroom to the LO chain output two-stage amplifiers. Since the LNA was AC-coupled to the inputs of the I/Q sub-harmonic mixers, the bias voltages and currents of the mixers and single-ended LO chain were identical to those given in Section 3.2.1. The LNA drew 6.1 mA of current from a 3.3 V supply (compared to a simulated value of 6.6 mA from a 3.3 V supply) resulting in a DC power consumption of 20.1 mW. The total current consumption for the SLO receiver front-end was therefore:

$$\begin{aligned}
 I_{tot} &= I_{LNA} + I_{mixer|I} + I_{mixer|Q} + I_{LOChain} \\
 &= 6.1 + 5.1 + 4.9 + 35.2 \\
 &= 51.3 \text{ mA}
 \end{aligned}$$



(a)



(b)

Figure 5.1: Photographs of the fabricated  $\times 2$  sub-harmonic receiver front-end: (a) bare die ( $2.3 \text{ mm} \times 1.8 \text{ mm}$ ); (b) die packaged in a  $5 \text{ mm} \times 5 \text{ mm}$  32 pin MFL package.

for a total DC power consumption of

$$\begin{aligned} P_{DC} &= 3.3 \text{ V}(6.1 \text{ mA} + 5.1 \text{ mA} + 4.9 \text{ mA}) + 4.3 \text{ V}(35.2 \text{ mA}) \\ &= 204.5 \text{ mW}. \end{aligned}$$

The power consumption is somewhat excessive compared to more recent designs, but could be significantly reduced in a redesign of the front-end circuitry, particularly the LO chain and buffers.

### 5.1.2 Input Match

The HP8510C network analyzer was used to measure the input return loss of the SLO receiver front-end, using the same setup as with the standalone mixers in Section 3.2.2. Figure 5.2 shows the RF input match of the SLO receiver front-end. The front-end had better than 10 dB return loss over the majority of the lower two U-NII bands and greater than 12 dB return loss for the entire upper U-NII band. In the lower bands, the 10 dB return loss bandwidth should have been centered at 5.25 GHz (the middle of the lower two U-NII bands), but was shifted up in frequency by  $\sim 40$  MHz; in the upper bands, the maximum return loss should have been centered at 5.775 GHz, but was shifted up in frequency by 55 MHz. The frequency shift is likely due to the unaccounted for parasitics within the layout, such as stray capacitances between metal interconnects. Since LO chain is the same as that used in SLON mixers described in Section 3.2.2, the measured LO input match was identical to the data shown in Figure 3.8.

### 5.1.3 Conversion Gain

The conversion gain test setup for the receiver front-end was the same as the setup for the standalone mixers described in 3.2.3. Figure 5.3 shows the conversion gain as a function of LO power at an RF of 5.2 GHz and an IF of 50 MHz for both the SLO receiver front-end and the SLON mixers. A rough estimate of the LNA gain can be found by subtracting the either the two I curves or the two Q curves from each other — the LNA provides  $\sim 10$  dB of gain. Figure 5.3 again shows the LO amplitude

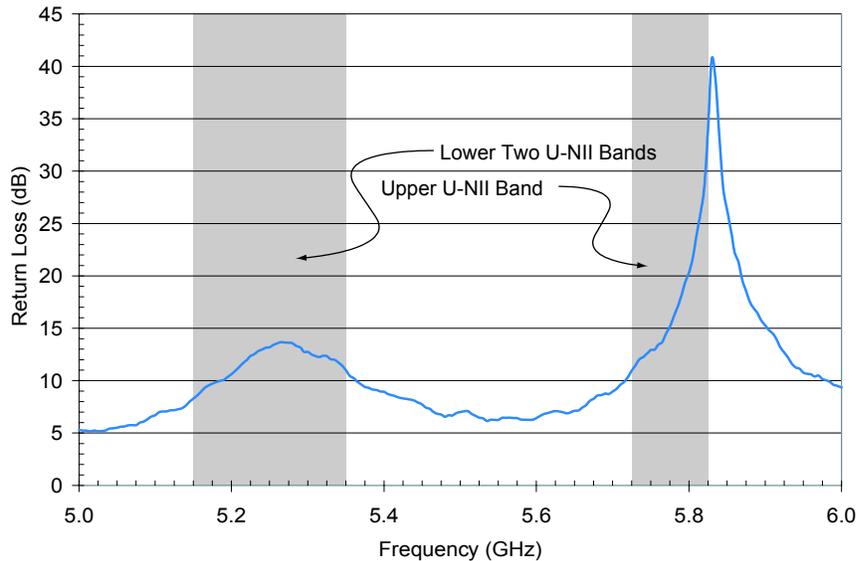


Figure 5.2: Measured RF input return loss of the SLO front-end over the 5–6 GHz band. The three U-NII bands are shaded in gray.

balance problems within the LO chain due to the compression of the Q-side two stage amplifiers.

Figure 5.4 shows the conversion gain of the receiver front-end and the SLON mixers versus RF frequency. In this case, the IF is set to 50 MHz and the LO power to  $-5$  dBm. Again, the gain of the LNA can be inferred from this plot to be  $\sim 10$  dB. The overall gain of the front-end is roughly 2 dB lower than the simulated value from harmonic balance analysis, which, at an LO power of  $-5$  dBm, was  $\sim 24$  dB.

### 5.1.4 Linearity

Figure 5.5 shows the input 1 dB compression point for the SLO receiver front-end. With the LNA input impedance of  $50\ \Omega$ , the measured input compression point of  $-19.5$  dBm corresponded to a peak differential voltage swing of 47.4 mV. As previously mentioned in Section 2.2.1 (Figure 2.4), the current of the differential pair starts to saturate as the normalized input drive level  $x$ , defined as

$$x = \frac{qV_1}{kT},$$

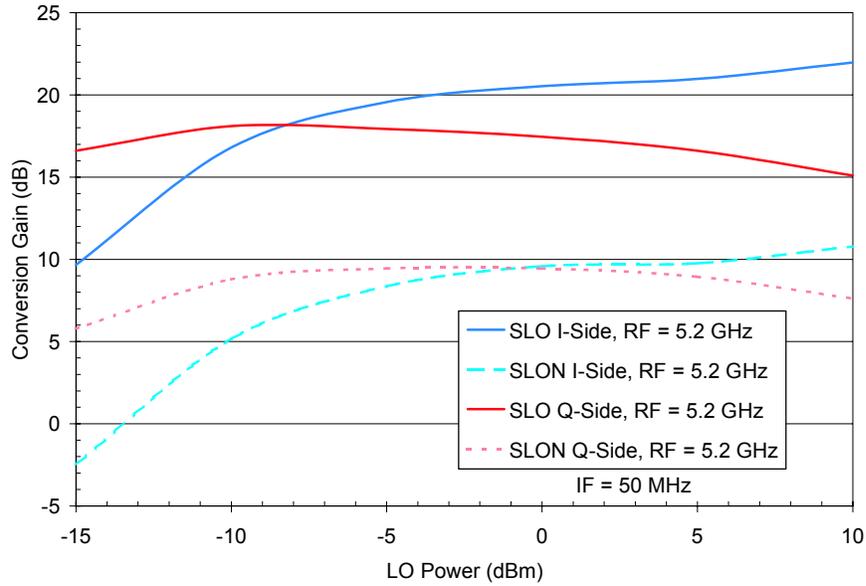


Figure 5.3: Conversion gain of the SLO RF front-end and SLON mixers versus LO power at an IF of 50 MHz and an RF of 5.2 GHz. The compression of the Q-side LO chain amplifiers is visible in both cases, as the Q conversion gain drops for increasing LO power while the I conversion gain continues to increase.

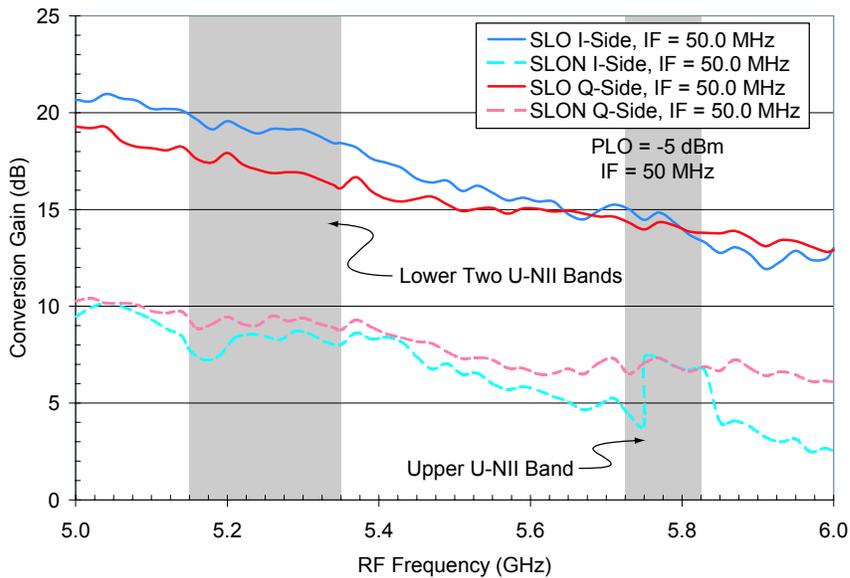


Figure 5.4: Conversion gain of the quadrature SLO RF front-end and the standalone SLON I and Q mixers versus RF frequency. The IF is 50 MHz and the LO power is 0 dBm. The three U-NII bands are shaded in gray.

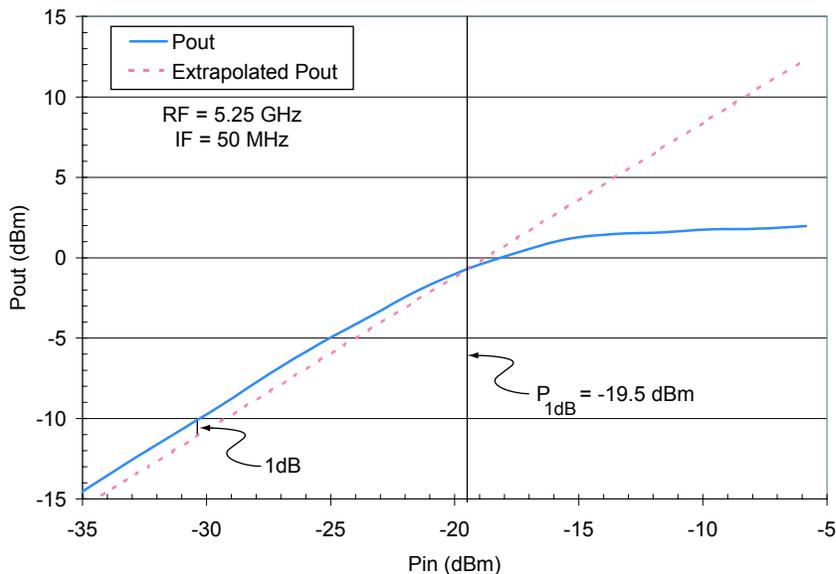


Figure 5.5: Measured 1-dB compression point of the SLO RF front-end at an IF of 50 MHz and an RF of 5.25 GHz. The LO power is fixed at 0 dBm. The input 1-dB compression point is  $-19.5$  dBm.

approaches 2, where  $V_1$  is the peak differential voltage. At an input power of  $-19.5$  dBm, the drive level is  $\frac{47.4}{26} = 1.82$ . Therefore, without a means of negative feedback, such as emitter degeneration (used in the mixer RF transconductors), or special biasing techniques [152, 153], the LNA exhibits typical bipolar, differential pair compression performance.

Figure 5.6 shows the measured input-referred IP3 and input-referred IP2 for the receiver front-end. Since the gain of the LNA effectively scales down the IIP<sub>3</sub> of the following stages [154], the overall IIP<sub>3</sub> of the SLO front-end [Figure 5.6(a)], which is estimated to be  $-8.5$  dBm, is lower than the estimated IIP<sub>3</sub> of the SLON mixers alone ( $+3.9$  dBm). The estimated input IP2 [Figure 5.6(a)] was  $+17.5$  dBm.

### 5.1.5 Noise Figure

As in the case of the standalone mixers, the mismatch between the  $3\text{ k}\Omega$  differential IF output and the  $50\ \Omega$  SMA, off-chip balun ( $100\ \Omega$  differential) was treated as a voltage divider and accounted for in post processing of the data for measurements

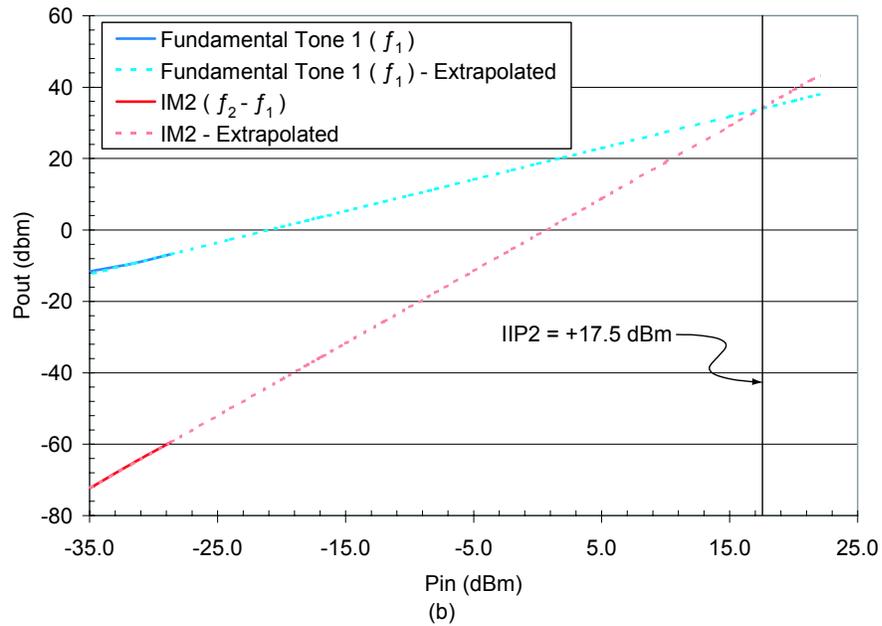
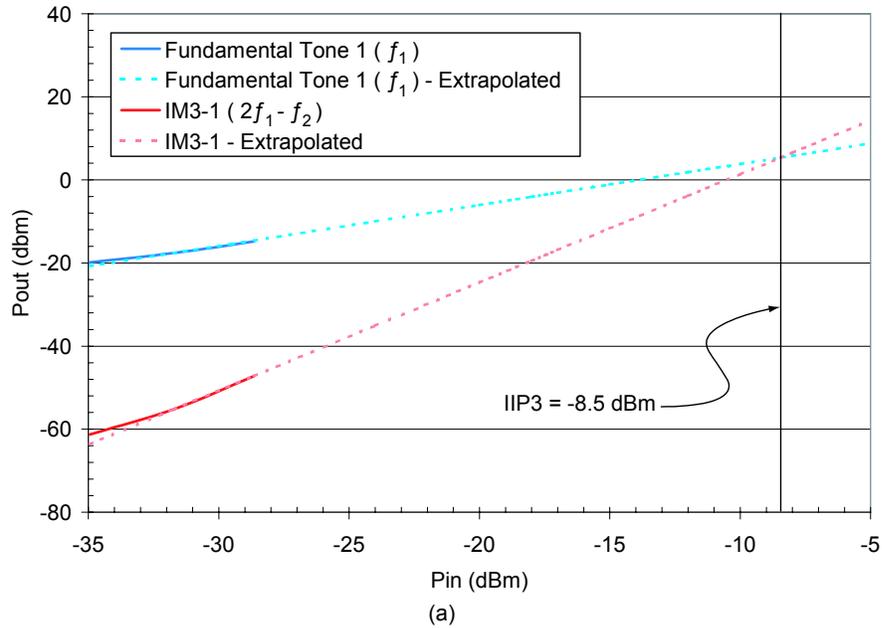


Figure 5.6: The estimated second and third order intercept points for the SLO receiver front-end under the following two-tone test conditions:  $RF_1 = 5.246$  GHz,  $RF_2 = 5.254$  GHz, and  $IF = 50$  MHz. The LO power was fixed at 0 dBm. (a) The input-referred IP3 is estimated to be  $-8.5$  dBm and (b) the input-referred IP2,  $+17.5$  dBm.

such as conversion gain and linearity. However, the IF impedance mismatch caused significant problems in the measurement of circuit noise figure, since the loss due to the voltage division lead to poor SNRs at the IF output. To eliminate the impedance mismatch between the mixer and the IF balun, the balun was replaced with a board-level difference amplifier based on an off-the-shelf, high-performance SMT op-amp (Figure 5.7). This approach allowed for control of the difference amplifier input impedance, which could be set to the desired differential input-impedance of  $3\text{ k}\Omega$  by appropriately choosing the resistor values.

Figure 5.7(a) shows a simplified schematic for the difference amplifier. The Texas Instruments THS4271 voltage feedback op-amp [155] was chosen for its low noise ( $3\text{ nV}/\sqrt{\text{Hz}}$ ,  $3\text{ pA}/\sqrt{\text{Hz}}$ ) and high slew rate ( $1\text{ kV}/\mu\text{s}$ ) characteristics, which enabled measurements at IFs up to at least  $100\text{ MHz}$ . The difference amplifier circuit was designed to have unity gain and an input impedance of  $3\text{ k}\Omega$  differential, which was achieved by setting the four resistors to  $1.5\text{ k}\Omega$  each. The low output impedance of the op-amp ( $0.1\ \Omega$ ) was well-suited for driving the  $50\ \Omega$  input of various pieces of test equipment, such as the spectrum analyzer, at low frequencies. The difference amplifier was implemented as a fully-connectorized, standalone board designed separately from that of the RF test board described in Section 3.1.2. A photo of the op-amp testboard is shown in Figure 5.7(b). Because the difference amplifier was fabricated after a significant portion of the front-end test plan had already been completed, it was only employed for the measurement of noise figure and in the measurement of DC-offsets and I/Q phase balance, which are described below in Sections 5.1.7 and 5.1.8, respectively. In all other cases, the reported results were measured using baluns at the IF outputs as described previously for the SLON and DLON sub-harmonic mixers.

Noise figure measurements of RF circuits have historically been accomplished through a variety of methods, with tradeoffs between the complexity of the test setup and the accuracy of the measurement. To simplify the procedure and to improve the accuracy of measured results, Agilent introduced the N8973A noise figure analyzer (NFA), a specialized piece of equipment dedicated to measuring the noise figure of RF circuits. With this instrument, noise figure measurements are reduced to a single calibration step followed by the actual measurement; such an approach was initially attempted for the measurement of the RF front-end noise figure. Unfortunately, the built-

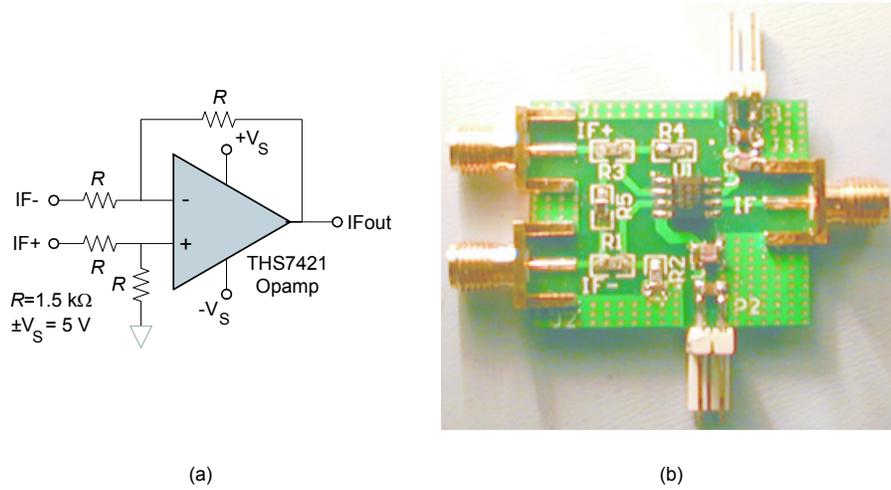


Figure 5.7: (a) Schematic of the op-amp based difference amplifier used to buffer the 3 kΩ IF differential output from the 50 Ω test equipment.  $G = 1$ . (b) Difference amplifier testboard. The board is separate from the main testboard with the DUT.

in N8973A analyzer software could not be configured to accurately account for the sub-harmonic mixing process and thus, the instrument failed to find the IF signal when making a measurement. As an alternative approach to dedicated equipment, a four step process was developed to measure the spot noise figure of the sub-harmonic receiver front-end using a spectrum analyzer.

Recall the definition of noise figure:

$$F = \frac{SNR_{in}}{SNR_{out}}. \quad (5.1)$$

Based on this definition, the test plan involves the measurement of the degradation in  $SNR$  due to each component in the test setup, followed by the calculation of the noise figure of the DUT using the cascaded noise figure equation (Equation 4.1). The  $SNR$  measurements were taken on the HP8563E spectrum analyzer with a resolution bandwidth of 3 kHz. The sweep time of the spectrum analyzer was increased to reduce noise fluctuations and to aid in finding the average noise floor of the signal. The  $SNR$  was determined by taking the difference in dB between the peak signal level and the noise floor at a 12 kHz offset. The 12 kHz offset was chosen to avoid the noise contribution of the phase noise skirts of the RF sources.

The four required steps for determining the noise figure were:

1. measurement of the output  $SNR$  of the signal sources at the RF (5.25 GHz, provided by the HP8510) and IF (10 and 50 MHz, provided by the HP83620B) frequencies [Figure 5.8(1)];
2. measurement of the output loss (or  $SNR$ ) of the 180° hybrid and the IF balun (used in Step 3) [Figure 5.8(2)];
3. measurement of the output  $SNR$  of the op-amp impedance buffer; the IF balun from Step 2 was used to convert the single-ended signal to differential form for input to the op-amp. The degradation in  $SNR$  due to the balun was removed in post processing [Figure 5.9(3)];
4. measurement of the output  $SNR$  of the entire test setup [Figure 5.9(4)].

With the data from these four measurements, the noise figure of the receiver front-end was calculated by treating the entire setup as a cascaded system. While the measurement data was in dB, the calculations must be performed with linear (not dB) values. The noise figure of the test setup ( $F_{SYS}$ ) is given by:

$$F_{SYS} = 1 + (F_{HYB} - 1) + \frac{F_{DUT} - 1}{L_{HYB}} + \frac{F_{opamp} - 1}{L_{HYB}G_{DUT}} \quad (5.2)$$

where  $F_{HYB}$  (which is the same as  $L_{HYB}$ ) is the measured loss up to the DUT input,  $F_{DUT}$  is the noise figure of the circuit (and the value of interest),  $G_{DUT}$  is the measured ratio power gain of the receiver front-end, and  $F_{opamp}$  is the measured noise figure of the op-amp circuit.

The noise figures of the hybrid and IF balun were set equal to the measured loss of each component; thus the loss of the DUT test board and cabling are also included in the value of  $F_{HYB}$ . The noise figure  $F_{SYS}$  was determined from the  $SNR$  measurements in Steps 1 and 4, where:

$$F_{SYS} = \frac{SNR_{in}}{SNR_{out}} = \frac{SNR_{out}|_{8510,Step1}}{SNR_{out}|_{sys,Step4}}. \quad (5.3)$$

$F_{opamp}$ , the noise figure of the difference amplifier alone, was calculated by treating

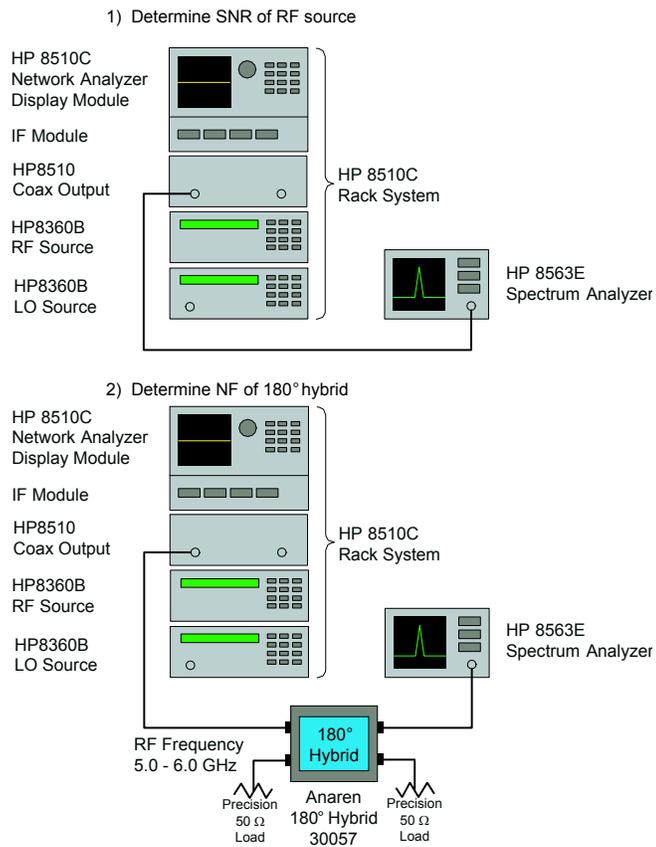
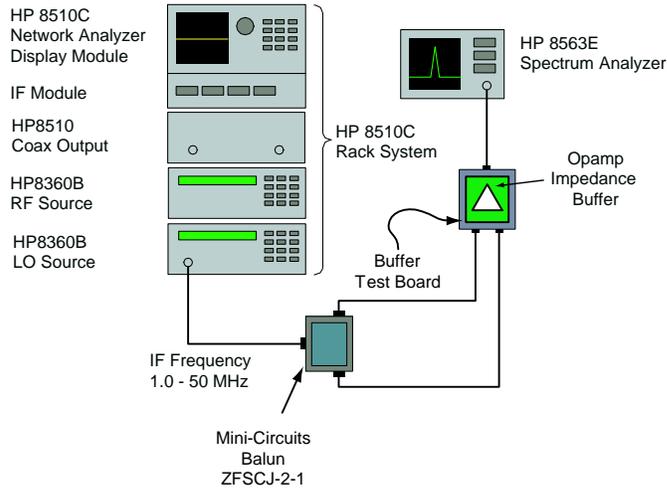


Figure 5.8: First two steps of the noise figure measurement: 1) determine the SNR of the RF sources; and 2) determine the noise figure of the RF input hybrid.

3) Determine NF of output circuit with opamp impedance buffer; subtract noise contribution of balun



4) Determine NF of DUT

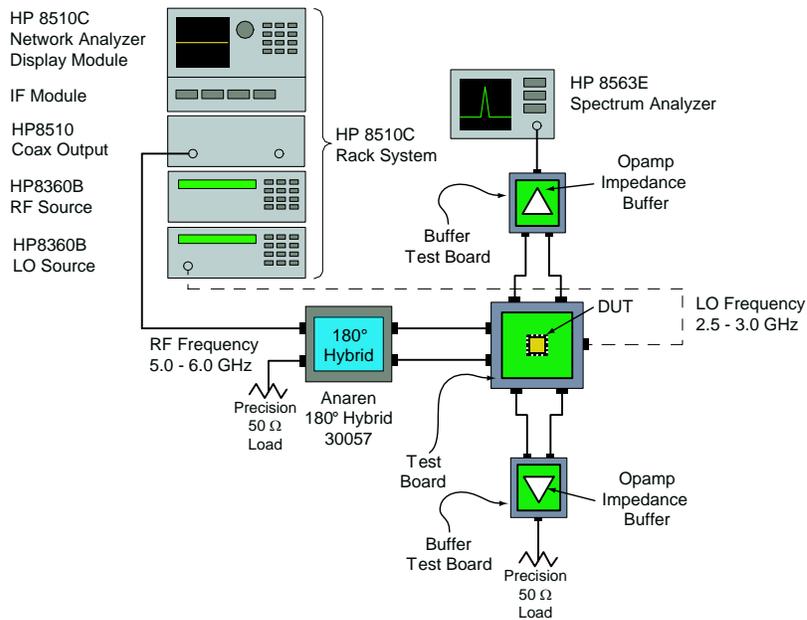


Figure 5.9: Last two steps of the noise figure measurement: 3) determine the SNR of the op-amp impedance buffer; and 4) measure the noise figure of the entire setup and calculate the noise figure of the DUT.

the measurement setup in Step 3 as a cascaded system,  $F_{opamp+}$ , where

$$\begin{aligned} F_{opamp+} &= \frac{SNR_{out}|_{83620B, Step1}}{SNR_{out}|_{opamp+, Step3}} \\ &= 1 + (F_{balun} - 1) + \frac{F_{opamp} - 1}{L_{HYB}} \end{aligned} \quad (5.4)$$

is solved for  $F_{opamp}$ . Rewriting Equation 5.2, the noise figure of the DUT is

$$F_{DUT} = L_{HYB} \left[ F_{SYS} - F_{HYB} - \frac{F_{opamp} - 1}{L_{HYB} G_{DUT}} \right] + 1$$

and the noise figure in dB is found simply as  $NF = 10 \log(F_{DUT})$ . Based on this approach, the spot noise figure of the receiver front-end was measured to be 7 dB at an IF of 10 MHz and 7.2 dB at an IF of 50 MHz. These results agree well with the simulated noise figure at an IF of 10 MHz, which was 6.5 dB. The noise figure values presented here represent the single-sideband (SSB) noise figure of the SLO receiver front-end, which is suitable since non-zero IFs were used in the measurements and simulations. However, for DCR applications the RF bands on both sides of the LO signal contain desired information and therefore, double-sideband (DSB) noise figure should be reported; consequently, the DSB values are expected to be 3 dB lower than these reported SSB results.

### 5.1.6 Isolation

The addition of the LNA significantly improved the 2LO→RF isolation across the lower third of the 5–6 GHz band when compared with the SLON mixers. Figure 5.10 shows the results for the SLO receiver front-end and the SLON mixers, both of which were measured with the test setup shown in Figure 3.15. The LNA provided an additional 15–20 dB of isolation between the LO and RF ports over that of the stand-alone mixers. However, at frequencies above the lower U-NII bands ( $\gtrsim 5.35$  GHz), the addition of the LNA had little effect on the isolation. This lack of improvement at higher frequencies can be attributed to the following LO coupling mechanisms:

1. bondwire radiation — package bondwires may have coupled the LO signal between the circuits at higher frequencies;

2. substrate coupling to the series input inductors of the LNA — the large, rectangular coil structures may have picked up the LO signal from the substrate and presented it directly to the RF port;
3. coupling via dummy area-fill patterns — the large planes of metal may have provided capacitive coupling paths for the LO from the substrate to the RF port, as described in Section 3.1.1.

The LO→RF isolation was roughly the same with or without the LNA, as shown in Figure 5.11. The isolation measurement was performed over the 2.5–3 GHz LO band, where the signal entering the chip was at a relatively large power level (in this case, 0 dBm). At these frequencies, the LO signal was well-outside the bandwidth of the LNA, which should have led to greater isolation, even more than the 15–20 dB improvement that was measured for the 2LO→RF case with the LNA. With the isolation nearly the same — regardless of the LNA — it is believed that the LO signal coupled to the RF port through unintended paths, either within the substrate, or through the large series matching inductors at the LNA input. Nevertheless, the isolation results of Figures 5.10 and 5.11 indicate that with the RF port sensitive to twice the frequency of the LO, at least 50 dB of port isolation can be achieved.

### 5.1.7 DC-offsets

Figure 5.12 shows the test setup for the DC-offset measurement. The I and Q DC offsets were measured separately; the side not being measured had its IF buffer terminated in  $50\ \Omega$  loads. Mini-Circuits bias tees (ZFBT-6G-FT) were connected to the IF outputs of the RF front-end side-under-test such that the *RF+DC* ports were connected to the DUT, the *RF-only* ports were connected to the op-amp impedance buffer inputs, and the *DC-only* ports were connected to a digital multimeter. The bias tees AC-coupled the IF signal to the impedance buffer while providing a test point for the DC voltage at the IF output.

Three DC offset voltages are of interest:

1. the front-end under DC bias only.
2. the front-end DC biased with the LO injected.

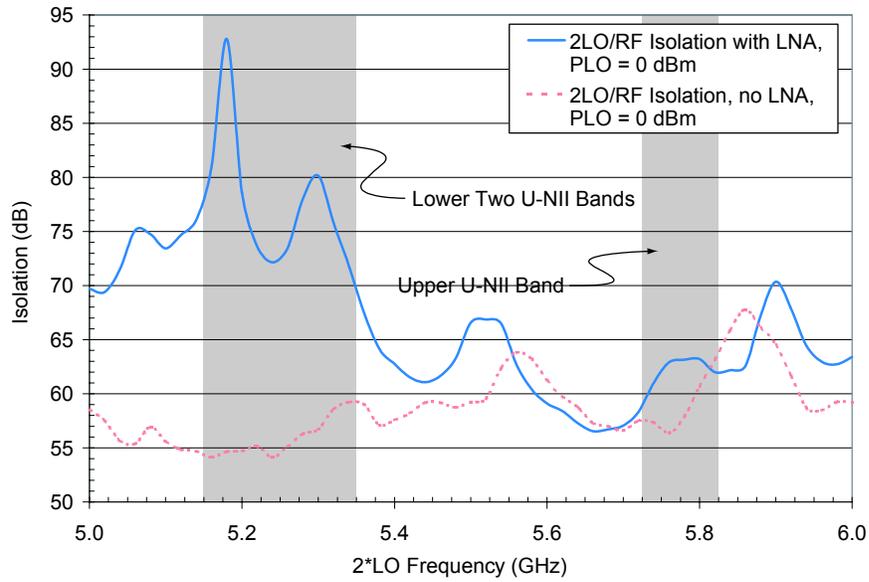


Figure 5.10: Measured 2LO→RF isolation of both the standalone SLON mixers and the SLO front-end at an LO power of 0 dBm.

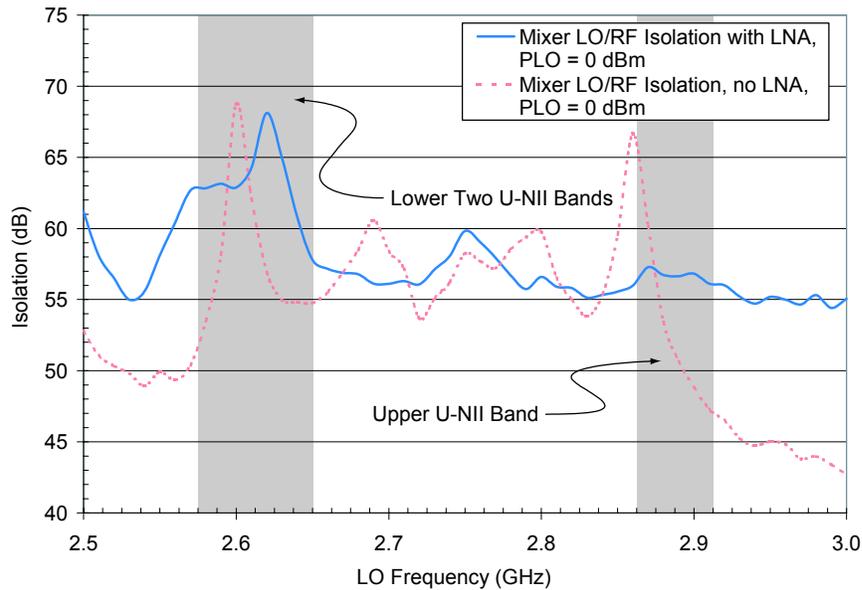


Figure 5.11: Measured LO→RF isolation of both the standalone SLON mixers and the SLO front-end at an LO power of 0 dBm.

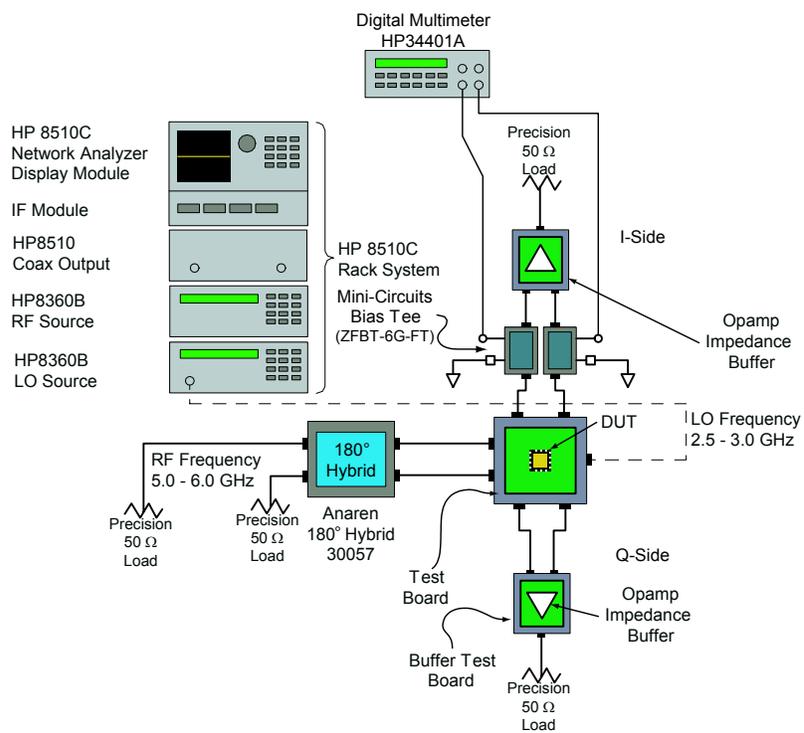


Figure 5.12: Test setup for the DC-offset measurement. The I and Q side offsets are measured separately from each other.

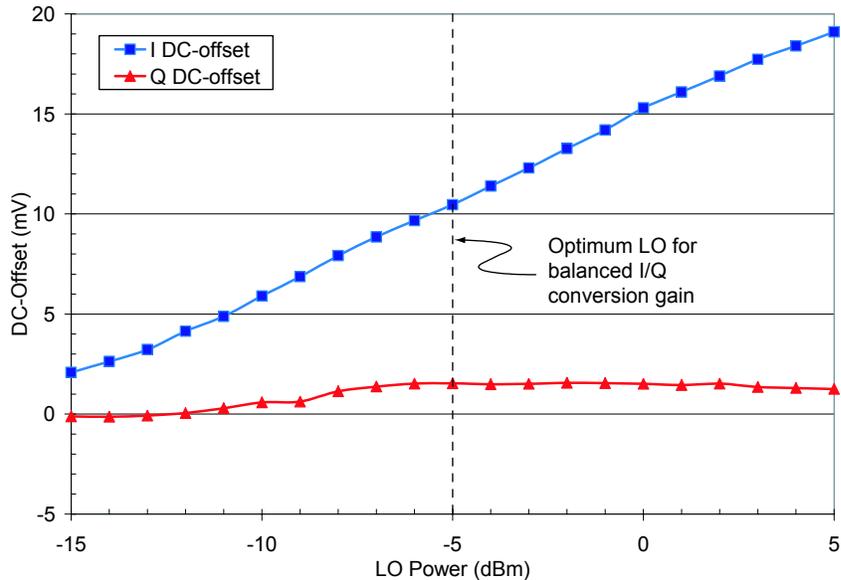


Figure 5.13: Measured DC-offset for the I and Q mixers. The larger LO signal into the I mixer results in greater LO self-mixing, as evident by the significantly larger DC-offset.

3. the front-end DC biased with the LO injected and a single RF tone input.

Because the LO switching core within the mixer is AC-coupled to the RF transconductor and the IF output is AC-coupled to the impedance buffer, the first offset listed above indicates passive/active device mismatches between the plus and minus branches of the differential switching cores. For the Q mixer, the DC-offset voltage,  $V_{off|Q}$ , was 0.8 mV while for the I mixer, the DC-offset voltage,  $V_{off|I}$ , was 4.9 mV, more than six times greater. These levels represent static offsets, which must be calibrated out of the subsequent measurements.

The second offset listed above is a measure of LO self-mixing. Figure 5.13 shows the measured DC-offset vs. LO power at the IF outputs of the I and Q sides, after removing the static offsets of 4.9 mV and 0.8 mV, respectively. The Q-side of the front-end showed strong isolation from LO self-mixing, with a maximum  $V_{off|Q}$  of 1.5 mV. On the other hand, the I mixer offset was relatively poor in comparison, with a maximum  $V_{off|I}$  of 19.1 mV.

The disparity between the offset voltages is believed to be another effect of the imbalanced LO signals between the I and Q branches of the LO chain. With the LO

chain output amplifiers on the Q-side operating in compression, the LO signal was relatively weak, reducing LO leakage to the RF port of the mixer and providing less of a pump signal to the switching core of the Q mixer. Consequently, there was less LO self-mixing. On the I-side, the output amplifiers were able to operate linearly and boost the LO signal to adequate levels for pumping the mixer switching core. This stronger LO signal in turn resulted in higher levels of leakage to the RF input of the mixer, which generated a higher DC-offset through self-mixing than the Q-side mixer. Therefore, the DC-offset for the Q-mixer would likely be  $\sim 10$  mV at an LO power of  $-5$  dBm if the Q-side amplifiers were operating properly. As discussed in Section 3.2.4, a DC-offset of 10 mV at the IF output of the mixers and a conservatively low estimate of 50 dB of baseband voltage gain, the DC level at the input of the ADCs would be  $20 \log(10 \text{ mV}) + 50 \text{ dB} = 0.5 \text{ dBV}$  or  $\sim 3$  V. This voltage level would likely saturate the input of modern ADCs and mask the desired signal.

The third offset voltage listed above provides an indication of second order nonlinearities. As described in Section 1.3.3, any signal that interacts with a second order nonlinearity can generate a DC-offset. Therefore, when a single-tone is applied at the RF input of the receiver, any DC-offset that remains after subtracting the static bias and LO self-mixing offsets is due to second order nonlinearities within the receive chain. This measurement is made with an RF of 5.25 GHz and an IF of 10 MHz, which keeps the output signal outside the bandwidth of the DC multimeter to ensure that only second-order effects are measured. This offset was 0.3 mV at the IF Q output and 1.3 mV at the IF I output with an RF signal of  $-32$  dBm. Converting the DC-offset to dBm (referenced to the  $1 \text{ M}\Omega$  input impedance of the multimeter), the IIP2 for the I-side is calculated to be:

$$\begin{aligned}
 IIP_2(\text{dBm}) &= 2P_{in}(\text{dBm}) - (IM_{2,DC}(\text{dBm}) + 3 \text{ dB}) \\
 &= 2(-32) - (-85 + 3) \\
 &= +20.7 \text{ dBm}
 \end{aligned} \tag{5.5}$$

where the 3 dB must be added to balance the difference in power levels between one-tone and two-tone tests [75]. This single-tone IIP2 level agrees relatively well with the estimated value (+17.5 dBm) from the two-tone IIP2 measurement presented in Section 5.1.4.

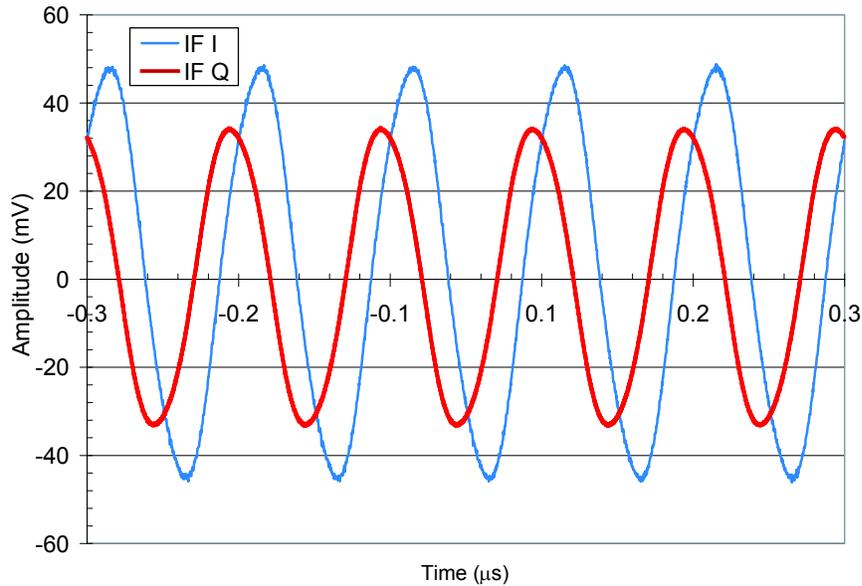


Figure 5.14: Measured time-domain waveforms for the SLO I and Q IF outputs. The phase balance is  $63^\circ$ .

### 5.1.8 I/Q Phase Balance

Because the I/Q phase balance between the IF I and IF Q outputs is primarily determined by the LO chain, the phase balance for the receiver front-end was expected to be similar to the measured phase balance of the SLON mixer in Section 3.2.6. Figure 5.14 shows the time-domain waveforms at the IF I and IF Q outputs of the receiver front-end with an RF of 5.25 GHz and an IF of 10 MHz, at an LO power of  $-5$  dBm. As was the case with the SLON mixers, the measured I/Q phase balance of the receiver front-end was  $63^\circ$ , corresponding to an imbalance of  $27^\circ$ . Again, this poor phase balance was the result of the imbalance introduced by the single-ended-to-differential input buffer of the LO chain. It is expected that the DLO version of the front-end would have exhibited significantly improved I/Q phase balance.

## 5.2 Summary

This chapter has presented the measured results for the fabricated  $\times 2$  sub-harmonic quadrature receiver front-end (LNA and sub-harmonic I/Q mixer pairs). Though

the LNA was designed with both the single-ended and differential LO chain mixers (SLO and DLO, respectively), only the SLO design was fabricated. The front-end consumed 51.3 mA of current and had a power dissipation of 204.5 mW, although this power consumption could be improved in a subsequent design iteration with modified buffer/amplifier designs.

The receiver front-end return loss was greater than 10 dB over the majority of the lower two U-NII bands and over the entire upper U-NII band. The front-end had a minimum conversion gain of 16 dB over the lower two U-NII bands and better than 13 dB over the upper band. The LNA provided a minimum, additional 20 dB of isolation over the lower two U-NII bands with more than 74 dB of 2LO-to-RF isolation; the LO-to-RF isolation was better than 55 dB over the LO frequencies corresponding to the three U-NII bands (2.575–2.625, 2.625–2.675, and 2.8625–2.9125 GHz). Although the LO→RF isolation was expected to improve in the RF front-end case due to the additional reverse isolation of the LNA, the measured isolation was roughly the same as that of the standalone mixers. The lack of improvement in isolation is believed to be the result of the large inductors at the input of the LNA, which provided a coupling path between the LO and RF front-end input.

The receiver front-end had a 1 dB compression point of  $-19.5$  dBm, an estimated IIP3 of  $-8.5$  dBm, and an estimated IP2 of  $+17.5$  dBm. The IF I/Q phase balance was  $63^\circ$ . This poor phase balance would be significantly improved with the use of a fully differential LO chain, as in the DLO version of the RF front-end.

The I mixer exhibited much higher DC-offsets due to LO self-mixing (10.5 mV) than the Q-mixer (1.5 mV) at an LO power of  $-5$  dBm. The large difference in offset voltage was due to the amplitude imbalance within the LO chain, since the LO signal on I-side of the chain did not suffer from compression. The amplitude imbalance of the LO chain could be corrected by increasing the emitter degeneration of the Q-side output amplifier, which requires less gain and greater linearity than the I-side due to the polyphase filter configuration. The DC-offset due to second-order nonlinearities was measured to be 0.3 mV for the Q mixer and 1.3 mV for the I mixer, which corresponded to a single-tone IIP2 of  $+20.7$  dBm. The spot noise figure of the receiver front-end was measured at a single RF of 5.25 GHz to be 6.5 dB at an IF of 10 MHz and 7.2 dB at an IF of 50 MHz.

Table 5.1: Simulated and measured results of the standalone SLON mixers.

FUNCTION	SIMULATED			MEASURED			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
I/Q Mixer Voltage		3.3			3.3		V
Current Consumption (I/Q mixers)		10			10.1		mA
LO Chain Voltage		3.3				4.3	V
Current Consumption (LO Chain)		24.7			35.2		mA
RF Frequency Range	5.0		6.0	5.0		6.0	GHz
IF Frequency Range		10		10		100	MHz
Noise Figure @ LO = 0 dBm	10		10.5		NM		dB
Conversion Gain @ LO = 0 dBm	8.2		9.7	6.0		10.1	dB
Input IP3 <sup>†</sup>		+9			+3.9		dBm
Input IP2 <sup>*</sup>		N/A			NM <sup>‡</sup>		dBm
Input Return Loss		>10		6.4	8.2	12.8	dB
LO Level	-5	-2	0	-15	0	5	dBm
2LO-RF Isolation		>80		54	57	65	dB
LO-RF Isolation		>60		47	55	65	dB
I/Q Phase Balance		0			60		°

\*specified at 5.25 GHz, and IF=50 MHz, I mixer

<sup>†</sup>with tone spacing of  $\Delta f=8$  MHz

<sup>‡</sup>not measured or could not be determined

Tables 5.1, 5.2, and 5.3 summarize the measured data for the two standalone mixer circuits and the SLO receiver front-end. Based on the relatively large power dissipation, the poor I/Q phase and amplitude imbalance at the IF outputs, the degraded IIP2, and the unbalanced compression effects between the I and Q two-stage amplifiers, the LO chain used in the receiver front-end needs to be improved. Although methods to enhance the linearity of the LO chain buffer and amplifiers could be employed and the loss through the polyphase filters could be reduced (by lowering the number of poles in each structure), the LO chain would still need to incorporate a VCO to generate the LO signal on-chip. The entire LO quadrature generation scheme would require a significant amount of power alone. Therefore, the drawbacks of the LO chain presented here motivated the development of an alternative method for generating quadrature signals, pursued in the next chapter.

Table 5.2: Simulated and measured results of the standalone DLON mixers.

FUNCTION	SIMULATED			MEASURED			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
I/Q Mixer Voltage		3.3			3.3		V
Current Consumption (I/Q mixers)		10			10.1		mA
LO Chain Voltage		3.3				4.3	V
Current Consumption (LO Chain)		20.4			32.9		mA
RF Frequency Range	5.0		6.0	5.0		6.0	GHz
IF Frequency Range		10		10		100	MHz
Conversion Gain @ LO = -5 dBm*		N/A		0.1	3	5	dB
Input IP3*		N/A			+5.2		dBm
Input IP2*		N/A			+23		dBm
Input Return Loss		>10		6.4	9	14.4	dB
LO Level	-5	-2	0	-15	0	5	dBm
2LO-RF Isolation		>80		51	53	56	dB
LO-RF Isolation		>60			NM <sup>‡</sup>		dB
I/Q Phase Balance		0			90		°

\*specified at 5.25 GHz, and IF=50 MHz, I mixer

†with tone spacing of  $\Delta f=8$  MHz

‡not measured or could not be determined

Table 5.3: Simulated and measured results of the receiver front-end.

FUNCTION	SIMULATED			MEASURED			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
I/Q Mixer Voltage		3.3			3.3		V
Current Consumption (I/Q mixers)		10			10.1		mA
LO Chain Voltage		3.3				4.3	V
Current Consumption (LO Chain)		24.7			35.2		mA
LNA Voltage		3.3			3.3		mA
Current Consumption (LNA)		6.6			6.1		mA
RF Frequency Range	5.0		6.0	5.0		6.0	GHz
IF Frequency Range		10		10		100	MHz
Noise Figure @ LO = 0 dBm*	7.1		7.6		7.2		dB
Conversion Gain @ LO = 0 dBm	9.7		8.2	14	18	20	dB
DC-offsets (LO self-mixing)		N/A		2	10.1	19.1	mV
Input IP3*†	+9				-8.5		dBm
Input IP2*†		N/A			+17.5		dBm
Input Return Loss		>10		8	12	30	dB
LO Level	-5	-2	0	-15	0	5	dBm
2LO-RF Isolation		>80		60	70	90	dB
LO-RF Isolation		>60		56	60	68	dB
I/Q Phase Balance		0			63		°

\*specified at 5.25 GHz, and IF=50 MHz, I mixer

†with tone spacing of  $\Delta f=2$  MHz

‡not measured or could not be determined

## Chapter 6

# Quadrature Voltage Controlled Oscillator with Tunable I/Q Balance

**A**S discussed in Chapter 1, the amplitude and phase errors introduced during the synthesis of a quadrature LO signal directly affect the amplitude and phase balance at the IF outputs of quadrature downconversion mixers. In the direct-conversion receiver mixers and front-end described in Chapters 2–5, LO conditioning chains with  $RC$  polyphase filters (Section 2.3) generate the required LO quadrature phases from an off-chip signal source. While the measured results show that an IF I/Q balance of  $90^\circ$  can be achieved over a specific range of LO powers using a fully-differential LO chain and an off-chip LO source, the solution has a number of drawbacks that make it undesirable for low-cost, low-power, highly-integrated receivers, including:

- ideal amplitude and phase balance (i.e.  $\varepsilon = 0$  dB,  $\Delta\phi = 90^\circ$ ) between the outputs of a single-stage polyphase filter occur only at a single frequency,  $f_0 = \frac{1}{2\pi RC}$  — at frequencies away from  $f_0$ , the amplitude balance is significantly degraded;
- on-chip resistor and capacitor tolerances and mismatches can have a significant impact on the center frequency of the polyphase filter stage, which can lead to an unpredictable frequency response;

- multiple  $RC$  poles can improve the bandwidth of the amplitude and phase balance and also mitigate the effects of component mismatches, but multiple poles result in greater loss through the filter structure — thus, high gain (and consequently high power consumption) output amplifiers are required to offset the loss through the polyphase filters and to provide sufficient drive levels to the mixer switching core (even if only one  $RC$  stage is used); and
- the multiple-pole polyphase conditioning circuitry occupies a relatively large amount of die area.

The LO chain used in the DCR front-end design in this work also lacks a means to dynamically compensate for the amplitude and phase errors that can result from component mismatches, stray parasitics, or imbalances within the mixer switching core, or from imbalances within the LO chain itself. Similarly, a method for dynamically adjusting the IF I/Q phase balance by tuning the output quadrature LO signal of the polyphase filter is not easy to implement, which limits the achievable accuracy of the IF quadrature signal [83].

This chapter presents a new approach for on-chip quadrature signal generation that addresses the above issues, while providing the additional functionality of dynamic amplitude and phase tunability. The chapter begins with an overview of techniques for quadrature signal generation. Next, the operation, design and layout, and simulation of two *phase-tunable* QVCOs with an amplitude-adjustable buffer are presented. Finally, measurement issues and methods for characterizing the circuits are proposed.

## 6.1 Quadrature Signal Generation

As mentioned in Section 1.3.3, there are a number of different techniques available for generating quadrature LO signals — including  $RC$  polyphase filters<sup>1</sup>, divide-by-2 stages, quadrature VCOs (that is, VCOs with direct quadrature outputs), and ring oscillators — presenting tradeoffs between phase noise, power consumption, drive level, quadrature accuracy, and complexity. The simplest approach to quadrature

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<sup>1</sup> $LC$  polyphase filters can also be used to generate quadrature signals, as in [156]. However, these circuits can consume significant die area (due to the on-chip inductors), are sensitive to parasitics, and have a relatively narrow band over which the amplitude and phase are balanced.

generation is to place an  $RC$  polyphase filter at the output of a differential  $LC$ -tank VCO, as demonstrated in the DCR front-end design above (using an off-chip signal source in place of an on-chip VCO). The operation and design of polyphase filters was described in Chapter 2. The polyphase filter/VCO technique has been used in numerous other applications because of its simplicity and relatively good performance [83, 101, 115, 117, 157–162]. However, the previously noted drawbacks, particularly the high power consumption of the required input buffer and output amplifiers and the sensitivity to component mismatches, have motivated the development of other techniques.

### 6.1.1 Ring Oscillator

The simplest ring oscillators consist of an odd number of simple inverters connected in a ring as shown in Figure 6.1(a). This topology produces an oscillating signal as dictated by the Barkhausen criterion, i.e. a self-sustaining oscillation will arise if the phase shift around the loop is a multiple of  $360^\circ$  (or  $0^\circ$ ) and the gain around the loop is  $\sim 1$ . Thus, for the three-stage ring in Figure 6.1(a), each inverter must be responsible for a phase shift of  $120^\circ$  and has a gain of 1. These types of oscillators are particularly useful for digital clock generation since they do not require an  $LC$  tank circuit to provide the frequency reference; the frequency of the oscillator is determined by the delay of each inverter stage ( $\tau_d$ ) and the number of stages in the ring ( $N$ ), such that  $f_0 = \frac{1}{2N\tau_d}$  [163]. Therefore, these oscillators tend to have large frequency tuning ranges (the frequency can be tuned by adjusting the time-delay of each stage in the ring) and consume minimal amounts of die area. However, since they do not incorporate a tuned, high- $Q$  resonant circuit, the phase noise performance of these oscillators is determined solely by the characteristics of the inverters, which typically exhibit poor phase noise performance [164]. Furthermore, the free running frequency of oscillation is very sensitive to process variations since such variations have a direct impact on  $\tau_d$ . Historically, LO signals generated with ring oscillator topologies have been unsuitable for RF communication systems with stringent phase noise requirements [13].

A potentially more useful topology for analog applications uses differential stages to form the ring oscillator. With this configuration, an even number of stages can

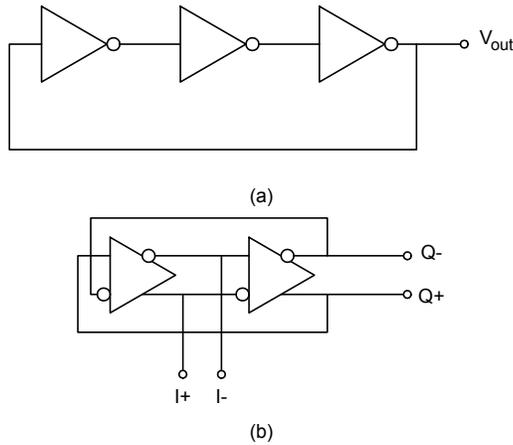


Figure 6.1: Ring oscillator topology: (a) digital, inverted-based ring oscillator; (b) differential ring oscillator with quadrature outputs.

generate a signal if one of the connections between the stages is cross-coupled [165], as in Figure 6.1(b). With as few as two differential stages, quadrature outputs can be obtained due to the reversal of the signal polarity at the input of one of the stages. The ring performance can be further improved by injection-locking the ring to a high quality signal source, as in [166–169]. In this case, excellent I/Q phase balance can be achieved and the phase noise of the ring oscillator can be improved — the output phase noise tracks the phase noise characteristic of the locking-source. Since ring oscillators can easily be integrated with digital circuitry, significant research has focused on this quadrature generation topology as a potential solution for SoC integration [82, 170–176].

### 6.1.2 Frequency Division

A digital “divide-by-2” frequency divider can be connected at the output of an  $LC$ -tank VCO to yield quadrature signals at one-half the free running frequency of the VCO. This scheme requires not only that the input signal to the divider be twice the desired frequency ( $2f_0$ ), but also that it has a duty cycle of exactly 50% [13]. The divide-by-2 method of quadrature generation has several advantages for RF transceiver applications:

- since the oscillator operates at a higher frequency, generally speaking, smaller

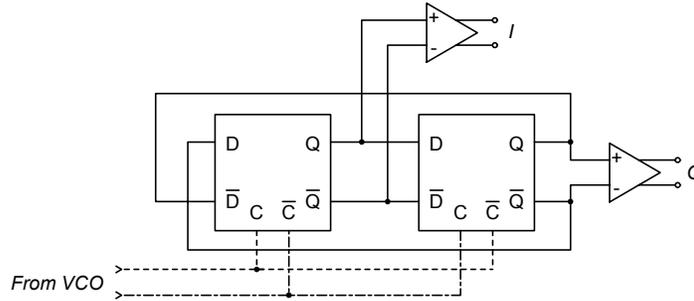


Figure 6.2: Differential digital divide-by-2 circuit with master-slave flip-flops.

size (and consequently, higher- $Q$ ) monolithic inductors and capacitors can be used for the VCO tank, which reduces the overall die area of the oscillator while also improving the phase noise performance;

- the dividers themselves are very compact and thus, consume far less die area than, for example, the  $RC$  polyphase filter approach; and
- the dividers produce square wave outputs, which are ideal for driving a mixer switching core, whereas  $RC$  polyphase filters operate on sinusoidal signals.

Digital divider circuits typically rely on master-slave flip-flops to provide instantaneous frequency division on a cycle-by-cycle basis; an example block diagram is shown in Figure 6.2. These circuits can be implemented with current mode logic (CML) topologies (or variants, such as emitter-coupled logic for bipolars, or source-coupled logic for FETs), to achieve high-speed operation while also providing differential inputs and outputs. CML flip-flops can operate over an input range of frequencies from DC to approximately one-half the  $f_T$  of the device technology [177]. Flip-flop-based dividers do not require any passive components and rely solely on the speed of the transistors [178]. However, the active devices generally need to be biased near peak  $f_T$  to achieve operation in the gigahertz range. As a result, such digital dividers are often deemed too power consumptive compared to other methods of quadrature generation. Digital dividers and their application in transceiver circuits have been reported extensively in [179–190].

The regenerative analog divider, sometimes referred to as the “Miller divider,” can also perform the divide-by-2 operation [191] and can be extended to provide quadra-

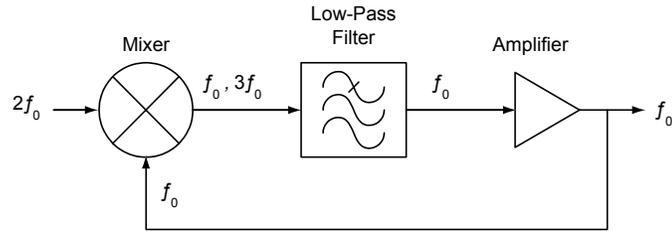


Figure 6.3: Block diagram of an analog regenerative divider. In continuous operation, the input frequency of  $2f_0$  is mixed with a lower sideband of itself located at  $f_0$ , which generates two frequency components,  $f_0$  and  $3f_0$  at the output of the mixer. The low-pass filter removes the  $3f_0$  component and the amplifier and mixer together provide sufficient loop gain to ensure continuous operation.

ture outputs. Figure 6.3 shows a block diagram of the regenerative divider. Under the proper gain and phase conditions, the  $2f_0$  input signal is mixed with a signal at  $f_0$ , which in turn, generates the sum and difference components,  $f_0$  and  $3f_0$  at the mixer output. The unwanted  $3f_0$  component is eliminated with a low-pass filter, while the required loop gain for the divider to sustain operation is provided by the combined gain of the mixer and amplifier [192], [193]. For startup, a finite signal (e.g. thermal noise) must be present within the system near  $f_0$  [194].

Regenerative analog dividers can operate close to the peak  $f_T$  of the device technology [195], [196], which means the maximum operating frequency is nearly twice that of digital dividers if designed in the same technology. Furthermore, regenerative dividers can be realized with fewer active devices, and thus, typically consume less DC power than their digital counterparts [177]. Quadrature outputs can be obtained from this architecture by connecting two active mixers as shown in Figure 6.4. In this case, the mixers perform all three functions of the regenerative divider and can provide signals with less than 0.25 dB of amplitude imbalance and within  $1^\circ$  of phase error [197].

Injection-locked frequency dividers (ILFDs) provide another (low-power) method for generating accurate quadrature signals from a  $2f_0$  source. ILFDs contain a narrowband  $LC$  resonator, enabling these circuits to essentially trade bandwidth for ultra-low levels of power consumption [198]. ILFDs have traditionally been treated as a unique circuit in both analysis and modeling, yet are very similar to regenerative

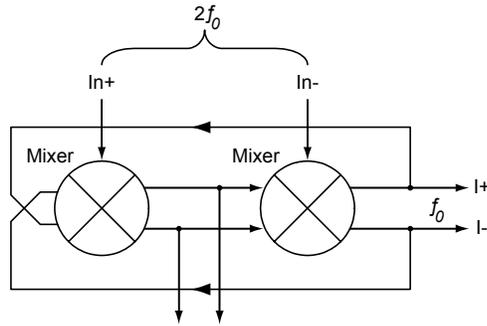


Figure 6.4: Analog regenerative divider with quadrature outputs.

analog dividers [199]<sup>2</sup>. In fact, the traditional block diagram of an ILFD, shown in Figure 6.5(a), can be adapted to the analog regenerative divider block diagram from Figure 6.3, as in Figure 6.5(b). In fitting the ILFD to the model of a regenerative divider, the mixer provides the nonlinearity for frequency division while the band-pass characteristic of the  $LC$  resonator (centered at  $f_0$ ) replaces the low-pass filter. When in lock, the dividers track the frequency and phase of the injected VCO signal and generate a spectrum with frequency components at multiples of the injected frequency. The filter is designed to select the sub-harmonic of the injected signal located at  $f_0$ .

Figure 6.5(c) shows an implementation in CMOS of an ILFD with quadrature outputs [201]. The full operation and mathematical description of injection-locking can be found in [202–205] while examples of injection-locked quadrature dividers can be found in [81, 166, 200].

### 6.1.3 Quadrature VCO

A final technique for synthesizing quadrature signals uses a property of the differential  $LC$ -tank VCO to generate I/Q signals — by appropriately coupling two identical VCOs to each other, the two oscillators synchronize to the same frequency, but with outputs that exhibit a  $90^\circ$  phase difference between them [206]. This approach is of particular interest since  $LC$ -VCOs are commonly employed for generating the

<sup>2</sup>In reality, injection-locked dividers are topologically identical to the flip-flop dividers above, but with inductive loads [200].

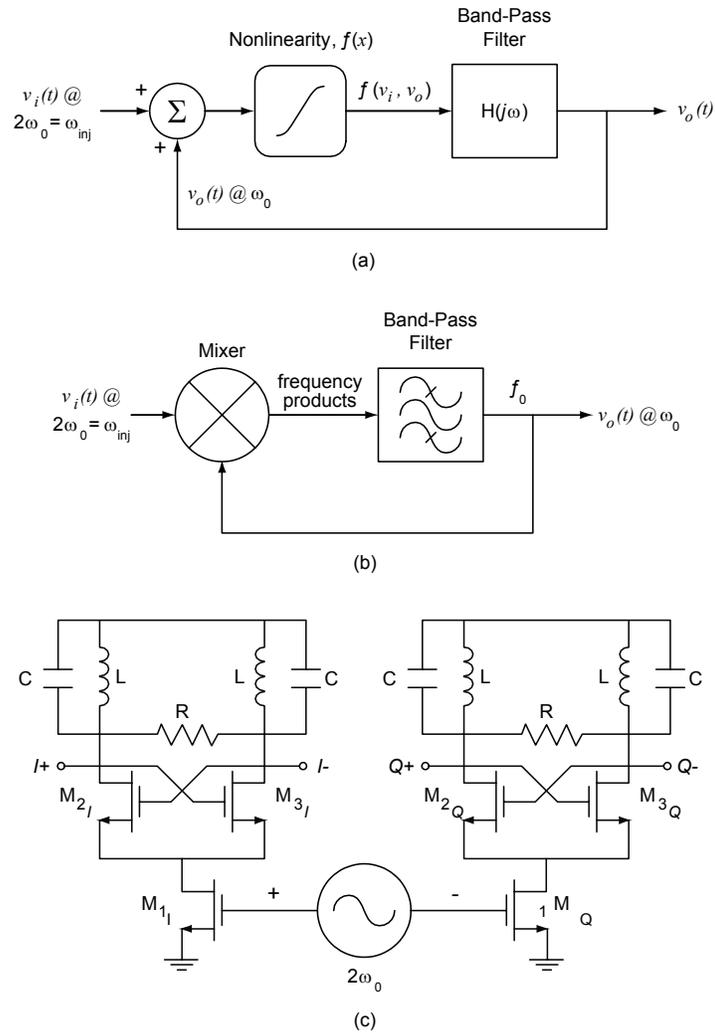


Figure 6.5: Injection-locked frequency divider: (a) traditional model of the injection-locked circuit; (b) regenerative analog divider model extended for ILFDs; (c) CMOS implementation of an IFLD with quadrature outputs.

on-chip signals required for both upconversion and downconversion. Furthermore, the fully differential  $LC$ -tank VCO can reject common-mode signals (e.g. noise) and is well-suited for driving mixer switching stages and single-sideband modulators [207]. Consequently, extensive research has been performed on the design, analysis, modeling, and characterization of this circuit, including fundamental operation [83, 208–212], the definition and sources of phase noise [164, 213–216], and methods to enhance VCO performance, e.g. increased tuning range [217–219], reduced sensitivity to power supply noise [220, 221], and lower power consumption [222]. Therefore, pursuing this method of quadrature generation can leverage the recent developments and improvements in  $LC$ -tank VCO design to obtain low phase noise and low-power quadrature signal generation.

The typical  $LC$ -tank VCO can be understood by breaking the circuit into two parts: (1) an  $LC$  resonator (or tank) and (2) a negative resistance circuit. Ideally, any energy stored within the tank will oscillate without loss between the inductor and capacitor at a frequency of

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (6.1)$$

However, the loss resistances associated with the inductor and capacitor dissipate the stored energy on each cycle of oscillation until, ultimately, all of the energy is lost and the oscillation is completely damped out. This situation can be modeled with a parallel  $R$ - $L$ - $C$  circuit where the losses of the inductor and capacitor are represented by an equivalent parallel resistance. To sustain oscillation, the loss of the tank can be offset by connecting it to a negative resistance, or  $-G_m$  circuit. Basically, such a circuit uses positive feedback to effectively restore the energy lost within the tank. A differential  $-G_m$  circuit is often comprised of a pair of cross-coupled transistors (the output of one device feeds into the input of the other) that presents a differential resistance of  $-\frac{2}{G_m}$  to the tank. Figure 6.6(a) shows a simplified block diagram of the  $LC$ -tank VCO. Noting that a larger resistance in the  $R$ - $L$ - $C$  model is indicative of *less* loss, the conditions under which the combined  $LC$  resonator and  $-G_m$  circuit will oscillate can be determined by the ratio of the equivalent tank resistance,  $R_{eq}$ , to the magnitude of the negative resistance of the  $-G_m$  circuit,  $R_{G_m}$ . This ratio is known as the “startup safety factor” ( $\alpha$ ) and, from empirical results, must be greater

than 2 to sustain oscillation [209]:

$$\alpha = \frac{R_{eq}}{R_{G_m}} \gtrsim 2 \quad (6.2)$$

Figure 6.6(b) shows the typical CMOS implementation. The  $LC$ -tank consists of on-chip spiral inductors and tunable capacitors, such as MOS-based varactors. The cross-coupled transistor pair  $M_1$  and  $M_2$  generate the negative resistance, which acts to restore the energy lost within the  $LC$ -tank.

Quadrature generation using an  $LC$ -tank VCO can be implemented in at least two distinct methods. The first method utilizes the second harmonic inherently generated within the  $LC$ -tank VCO. In this case, the two identical, differential oscillators are coupled between any one of the circuit's virtual ground points shown as  $\boxed{1}$ – $\boxed{4}$  in Figure 6.6(b). At these points, the fundamental signal at  $f_0$  and its odd harmonics ( $3f_0, 5f_0, \dots$ ) are equal to zero while the even order harmonics, particularly  $2f_0$ , add in phase. By connecting the two VCOs at one of the virtual grounds, the oscillators mutually lock to each other's second harmonics with a  $180^\circ$  phase-shift between them, which enables the generation of quadrature signals [224]. This circuit is very similar to the injection-locked frequency dividers above, but instead of locking to a standalone VCO running at  $2f_0$ , the oscillators lock to each other's  $2^{nd}$  harmonic. The coupling at the virtual ground points can be implemented with either transistors or with integrated transformers. Anti-phase transformers provide the required  $180^\circ$  phase shift between the two oscillators and can be placed between the tank circuits of the two VCOs [points  $\boxed{1}$  or  $\boxed{2}$  in Figure 6.6(b)] [225–227] or between the sources (or emitters) of the cross-coupled  $-G_m$  transistors [point  $\boxed{4}$  in Figure 6.6(b)] [228, 229]. With transistors, the coupling can be implemented by cross-coupling the tail current transistors ( $M_1$ ) of each VCO together [223], as in Figure 6.6(c).

A second method to couple the two VCOs for quadrature synthesis is shown in Figure 6.7; the combination of a direct connection and a cross connection between the two VCOs forces them to lock to each other and oscillate in quadrature [230, 231]. However, since the  $LC$ -tank VCO is generally an autonomous circuit (i.e. it does not require an input signal to generate an output signal), the circuit requires some additional mechanism within the VCO core to inject a signal. This injection is usually achieved with coupling transistors (denoted as  $M_{cpl}$ ), which are placed either in

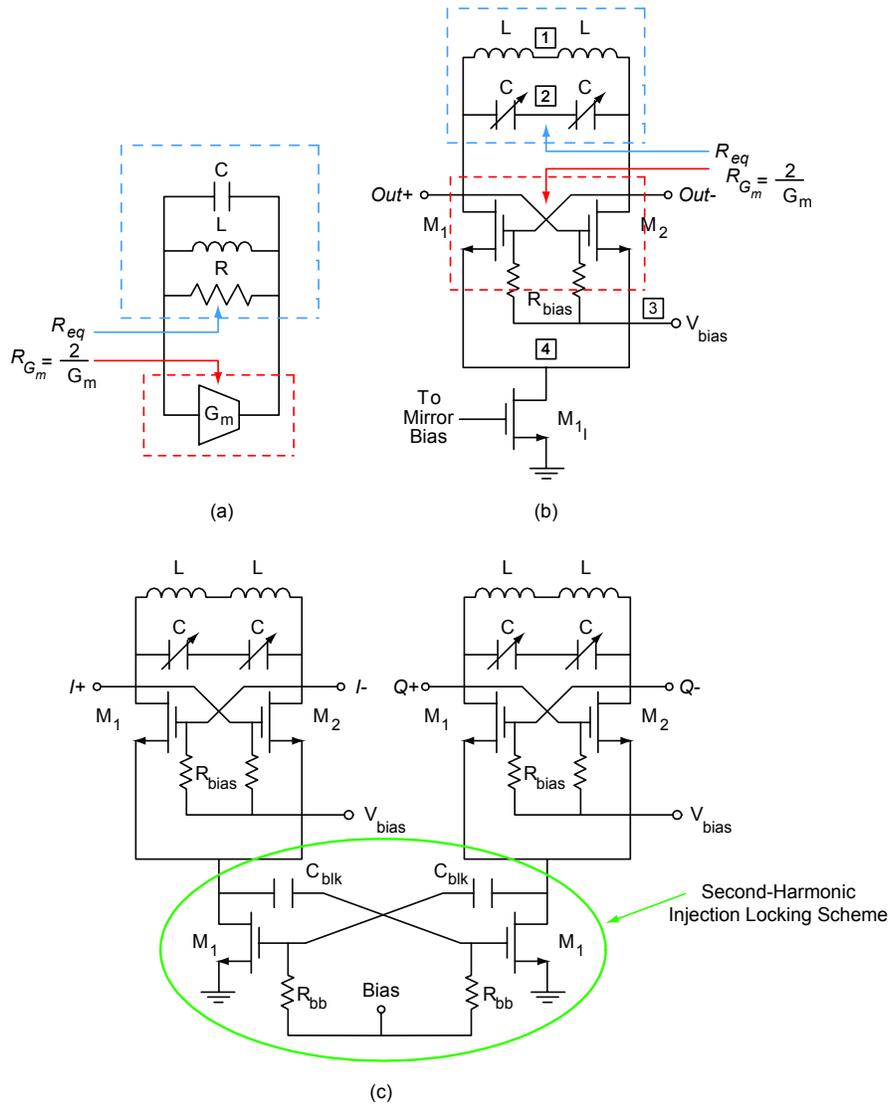


Figure 6.6: Simplified diagram of the  $LC$ -tank  $-G_m$  oscillator (a) block diagram; (b) symmetric, differential implementation with notation of virtual ground points; and (c) quadrature  $LC$ -tank VCO using transistor coupling of second harmonic (after [223]).

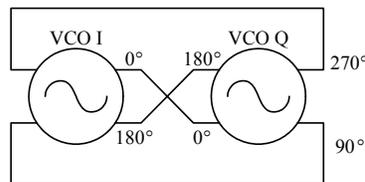


Figure 6.7: Block diagram showing direct- and cross-connection of the two VCO cores.

parallel (PQVCO) or in series (SQVCO) with the negative-resistance transistors, as shown in Figures 6.8(a) and 6.8(b), respectively.

The use of coupling transistors for quadrature generation also provides a simple way to improve quadrature accuracy: increasing the large-signal transconductance ( $G_{m_c}$ ) of the coupling transistors improves the quality of the locking between the oscillators, which improves the output quadrature phase balance [233]. However, the coupling transistors do not contribute to the negative resistance of the circuit and actually lower the quality factor of the tank, which in turn, reduces the output amplitude of the signal [234]. Furthermore, a lower tank quality factor results in a degradation of the oscillator phase noise performance. These drawbacks can be offset to some extent by increasing the DC bias current and the device sizes, which can improve both  $G_{m_c}$  and  $G_m$ . For a pure CMOS implementation, the coupling strength ( $s_c$ ) between the two VCOs can be found from the ratio between the size of the coupling transistors and the the size of the  $-G_m$  pair. Assuming the device lengths are equal, the coupling strength is simply:

$$s_c = \frac{W_{cpl}}{W_{G_m}}, \quad (6.3)$$

where  $W_{cpl}$  represents the device width of the coupling transistors and  $W_{G_m}$  represents the device width of the  $-G_m$  transistors. Unfortunately, the increase of device size and current only works up to a point, beyond which the approach leads to greater power consumption, increase in device noise, and lower signal swing, which together lead to unacceptable phase noise performance. Therefore, the coupling strength and the DC bias current of the oscillator must be carefully chosen to provide optimum phase noise and adequate signal swing while also considering the accuracy of the quadrature outputs.

Comparing the parallel and series coupling techniques, the series technique provides superior phase noise performance (with a minor penalty in voltage headroom) because the series devices contribute less overall noise to the circuit when connected in cascode with the negative transconductance pair. Therefore, the series coupling technique is used in the QVCO design to be described in this chapter. QVCOs with parallel coupling transistors have been reported in [206, 235–237].

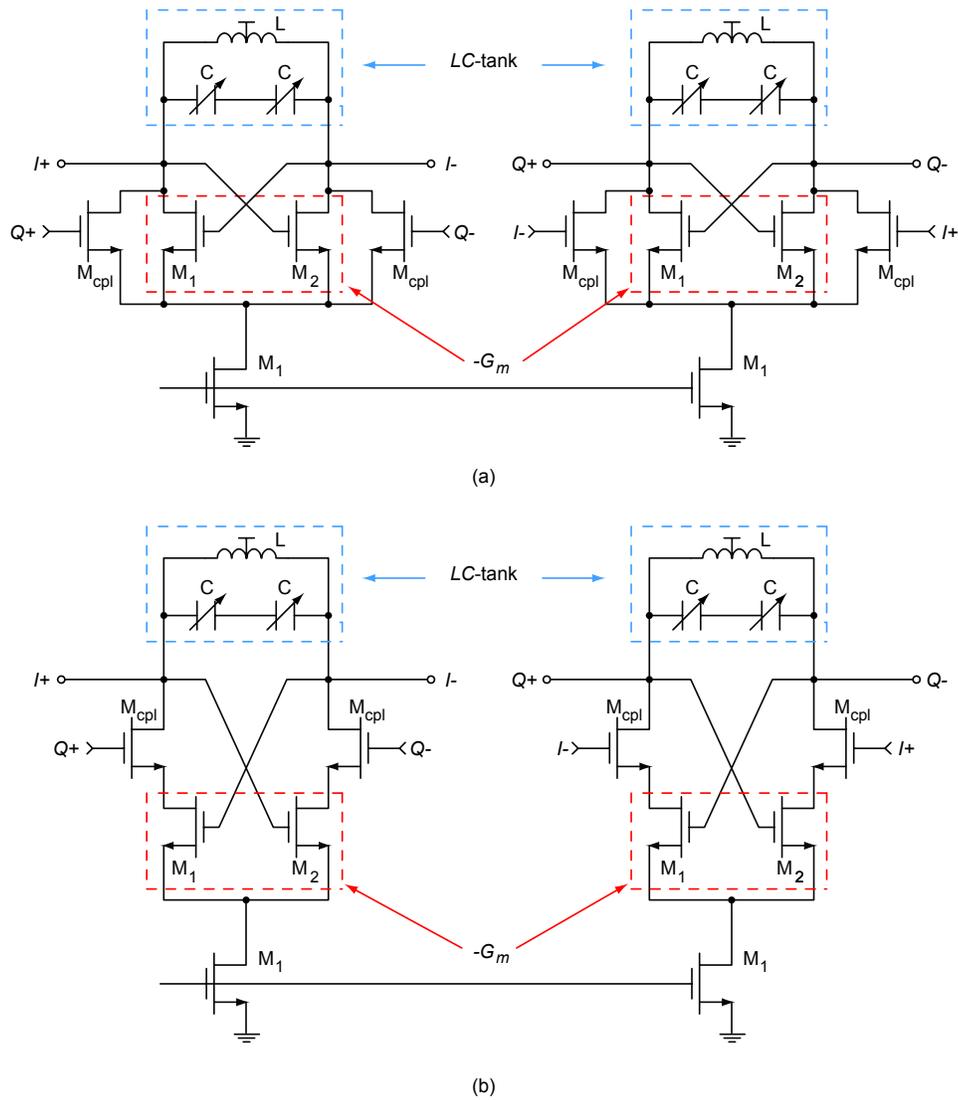


Figure 6.8: Transistor-coupled quadrature VCO topologies: (a) coupling transistors in parallel with the  $-G_m$  circuit (PQVCO); and (b) coupling transistors in series with the  $-G_m$  circuit (SQVCO). Here, the tank inductors have been replaced with symmetric, differential inductors [232].

## 6.2 Quadrature VCO Design

The operation of the QVCO can be explained in terms of a linear feedback loop, such as the one shown in Figure 6.9(a). As was shown in Section 6.1.3, the two  $LC$ -tank VCOs are represented by the combination of an  $R$ - $L$ - $C$  parallel circuit (which sets the desired oscillation frequency) and a large signal transconductance ( $G_m$ , which provides the negative resistance). The additional coupling transistors required for quadrature signal generation are represented by the transconductances  $G_{m_c}$ . The diagram can be simplified further by noting that the  $-G_m$  circuit essentially cancels the loss of the tank (i.e. approximately negates the tank resistance  $R$ ). Therefore, the diagram can be reduced to four ideal parallel  $LC$  tanks connected together through the coupling transconductances  $G_{m_c}$ , as in Figure 6.9(b). Given these simplifications, the operation of the QVCO can be deduced by inspection: starting at Tank [1], and assuming energy is already present within the loop, the parallel  $LC$  resonates at a frequency of  $\frac{1}{2\pi\sqrt{LC}}$  and generates the voltage  $I+$ ; this voltage is then transferred as a current into Tank [4] through  $G_{m_c}$ . This current, which enters Tank [4], must be  $90^\circ$  out of phase with the voltage  $Q-$  across the tank, due to the parallel  $LC$  resonance; thus,  $I+$  and  $Q-$  are in quadrature. The process continues on in the same fashion around the loop<sup>3</sup>. Hence, the signals from  $I+ \rightarrow Q-$ ,  $Q- \rightarrow I-$ ,  $I- \rightarrow Q+$ , and  $Q+ \rightarrow I+$  are each shifted by  $-90^\circ$ , resulting in quadrature output signals at  $I+$ ,  $Q-$ ,  $I-$ , and  $Q+$ , with relative phases  $0^\circ$ ,  $270^\circ$ ,  $180^\circ$ , and  $90^\circ$ , respectively.

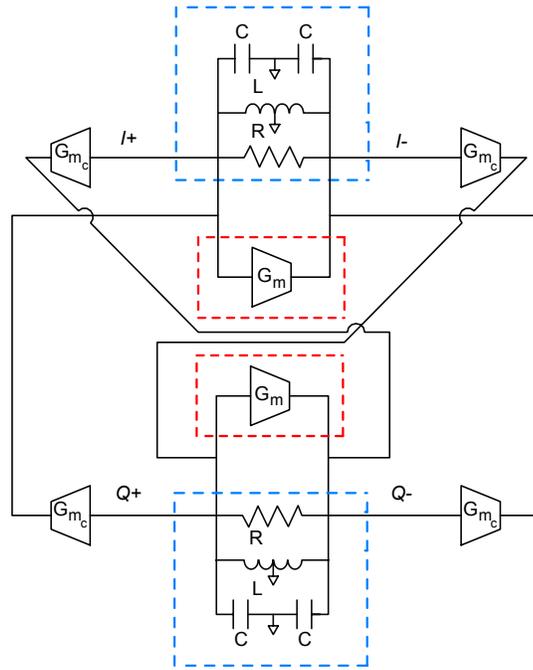
One potential drawback to this approach is the undesirable effect of the coupling transconductance on the center frequency of the oscillator. With the coupling-transconductances attached directly to the tank circuits, the resonant frequency of the oscillator ( $f_0$ ) can be shifted either up or down in frequency by a factor of  $\Delta f$ . The shift results from the pole generated by the transconductance/tank-capacitance combination and is given by [230]:

$$\Delta f = \pm \frac{G_{m_c}}{4\pi C}. \quad (6.4)$$

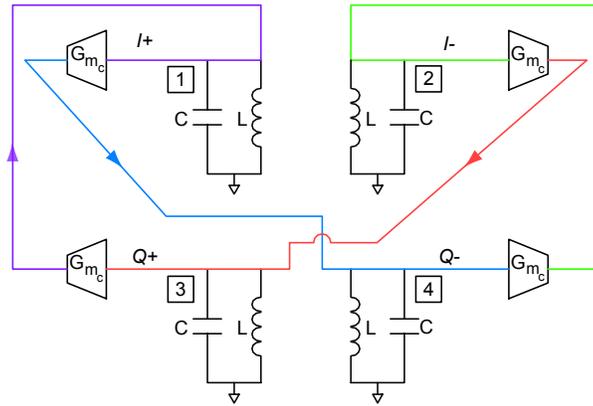
The asymmetrical frequency characteristic of  $LC$ -tank influences the direction of the frequency shift and causes one of the modes to dominate over the other [206]. The

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<sup>3</sup>Note that the total phase shift around the loop must be  $360^\circ$  and the gain is designed to be greater than 1, thus meeting the Barkhausen criteria for oscillation.



(a)



(b)

Figure 6.9: (a) Differential block diagram of the quadrature VCO with  $LC$ -tank,  $-G_m$  circuit, and coupling transistors. (b) simplified diagram assuming the loss of the tank is completely offset by the  $-G_m$  circuit.

direction of the shift actually depends on the series loss of the individual tank components — when the inductor exhibits greater series loss (lower  $Q$ ) than the capacitor, the positive frequency-shift occurs and when the capacitor loss dominates, the positive shift occurs [238]. However, bimodal oscillation (where the QVCO oscillates at *both* frequencies) can occur in cases where the tank losses are relatively balanced [239]. The actual center frequency ( $f'_0$ ) of the QVCO is given by:

$$\begin{aligned} f'_0 &= f_0 \pm \Delta f \\ &= \frac{1}{2\pi\sqrt{LC}} \pm \frac{G_{mc}}{4\pi C}. \end{aligned} \quad (6.5)$$

Figure 6.10 shows a simplified Cadence schematic of the cross-coupled QVCO (the mirror bias circuitry has been removed for clarity). Aside from the series (or cascode) coupling transistors (M0-M3), the familiar  $LC$ -tank VCO can be readily identified: the center-tapped, symmetric inductors (L0 and L1), PMOS accumulation mode varactors (C8-C11), and small fixed-value MIM capacitors (C4-C7) make up the tank circuit; the cross-coupled SiGe HBT transistor pairs (Q0, Q1) and (Q2, Q3) generate the differential negative resistance; and transistors M4 and M5 set the tail currents of each VCO.

The QVCO designs in this chapter are based on the Freescale (formerly Motorola) HIP6WRF 0.18  $\mu\text{m}$  SiGe:C RF BiCMOS technology described in Section 1.2.4 and are simulated using Cadence Design Systems, version 5.0.33 [240]. The design kit for the fabrication technology, supplied by Freescale Semiconductor, includes full VBIC models for the SiGe HBT devices, Berkeley Short Channel IGFET Models (BSIM) for the NMOS/PMOS devices and the PMOS varactors, and models for passive devices like resistors, capacitors, and inductors.

### 6.2.1 Phase Tunability

As discussed above, the ability to dynamically change the output phase balance of the quadrature generation scheme is highly desirable. In other methods of quadrature generation, phase tunability has been achieved in a number of different ways. For example, a polyphase filter can be modified to provide phase tunability by adding series varactors in each of the filter output lines, thereby allowing independent tuning

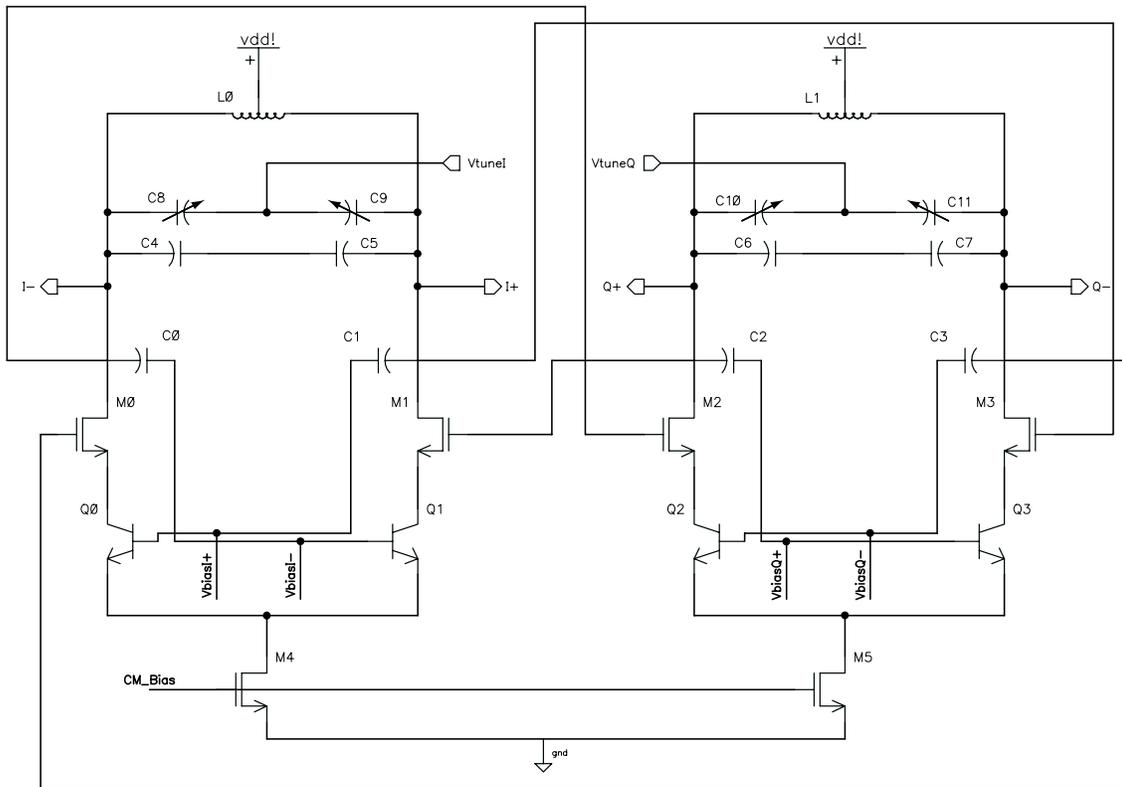


Figure 6.10: Simplified Cadence schematic of the series cross coupled quadrature VCO.

of the phase balance [83]. Alternatively, the phase balance can be adjusted with source-follower (or emitter-follower) buffers placed at the polyphase filter outputs; for the source-follower implementation, the bias current of the common drain transistor in each buffer is varied to produce small changes in the gate-source capacitance, which leads to small changes in the phase balance [241]. In [177], the phase balance of the injection-locked divider is tuned by introducing asymmetries in the biasing of the RF transconductors at the input of the divider.

For the quadrature VCO presented here, two methods for providing quadrature tunability are proposed. *Method 1* places series varactors in the four coupling paths between the two  $LC$ -tank VCOs. The  $RC$  pole generated by the capacitance and the parasitic resistance of the varactor introduces a phase asymmetry into the QVCO that can be adjusted to affect the phase balance between the QVCO outputs. *Method 2*, on the other hand, uses simple capacitive dividers at the differential outputs of the two VCOs; in this case, the series elements of the dividers are varactors, which provide tunable  $RC$  poles to adjust the phase balance of the outputs, similar to the work in [83]. Figure 6.11(a) shows the QVCO block diagram with the *Method 1* phase tuning scheme, which is referred to as the **Coupling Path Phase Tunable** or CPPT-QVCO; Figure 6.11(b) shows the *Method 2* scheme, which is referred to as the **Output Divider Phase Tunable** or ODPT-QVCO.

The  $LC$ -tank design is based on the principles in [59]. To reduce the number of inductors (from four, i.e. one for each tank) and to achieve a relatively high quality factor, symmetric, differential inductors (effective inductance of 1.7 nH each) are used for the tank inductors [112]. Small, fixed-value MIM capacitors (4 fF each) are placed in parallel to the frequency-tuning varactors ( $C_{max} = 396$  fF each) to set a maximum resonant frequency for the tank. Accounting for the frequency shift caused by the coupling transistors, and for the effects of the phase-tuning varactors, the  $LC$ -tank alone is designed for a center frequency of 8.8 GHz at the maximum of the frequency-tuning range (i.e. the frequency-tuning varactor control voltage is set to 1.8 V); when the capacitances of the coupling transistors and phase-tuning varactors are included, the simulated output frequencies are 5.6 GHz and 5.1 GHz for the CPPT-QVCO and ODPT-QVCO, respectively.

SiGe HBTs are chosen for the implementation of the negative resistance core since they exhibit lower  $1/f$  noise and greater negative transconductance (at a fixed bias

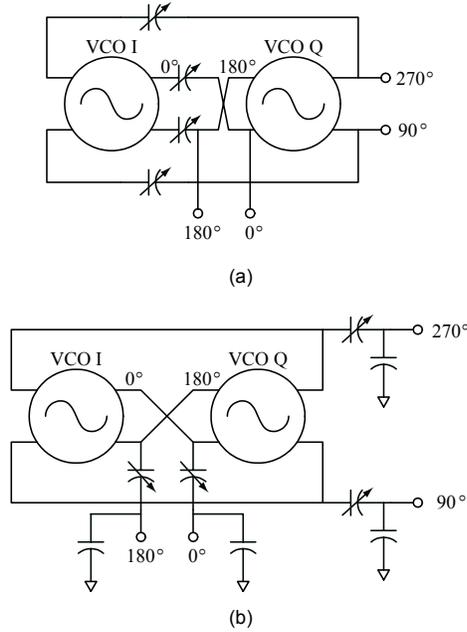


Figure 6.11: Phase tunable QVCO: (a) *Method 1* phase-tuning scheme (CPPT-QVCO); (b) *Method 2* phase-tuning scheme (ODPT-QVCO).

level) compared to NMOS devices in the  $0.18\ \mu\text{m}$  technology. The HBT emitters are sized to be  $9.8\ \mu\text{m} \times 0.245\ \mu\text{m}$ ; the devices are biased at peak- $f_T$  to ensure a large output signal-swing, which reduces close-in phase noise [59]. However, to keep the HBTs active-biased — even under large signal conditions — and to allow individual biasing of each transistor base and collector, 5 pF capacitors are inserted into the cross-coupling paths between the HBTs (capacitors C0-C3 in Figure 6.10). These capacitors are relatively large, but are necessary since bipolar devices draw DC base current<sup>4</sup>. Low-threshold-voltage NMOS FETs, which consume less voltage headroom than the standard NMOS FETs offered in the process, are used to set the tail current of the two VCO cores, and are sized at  $14.7\ \mu\text{m} \times 0.18\ \mu\text{m} \times 3$ . The bias currents to the bases of the cross-coupled HBTs are supplied by a separate PMOS FET current mirror. Low-threshold-voltage NMOS FETs are also used for the cascode coupling transistors and are sized to be relatively large, at  $31.4\ \mu\text{m} \times 0.18\ \mu\text{m} \times 5$ . Since the size of the coupling transistors directly influences the large signal coupling transconductance,  $G_{m_c}$ , and since  $G_{m_c}$  directly affects the output

<sup>4</sup>These DC blocking capacitors can be eliminated if the  $-G_m$  circuit is implemented with NMOS FETs.

quadrature accuracy, the size is chosen to provide enough coupling between the VCO cores to achieve near quadrature output phases; the phase tuning feature is used to correct for any small quadrature errors. Including the coupling transistors with the tank circuit, simulations show the startup safety factor ( $\alpha$ ) is  $\sim 2$ .

For labeling purposes, the VCO core responsible for the  $0^\circ$  and  $180^\circ$  outputs is considered to be the “I-side” VCO, and the other VCO core responsible for the  $90^\circ$  and  $270^\circ$  outputs is considered to be the “Q-side” VCO. Figure 6.12 shows the full Cadence schematic of the CPPT-QVCO including the biasing and phase-tuning varactors. Figure 6.13 shows the full Cadence schematic of the ODPT-QVCO.

## 6.2.2 Amplifier/Buffer and Amplitude Tunability

For the QVCO to be an effective LO source, the oscillator cores must be able to drive low impedance loads; in particular, the VCO should not be affected by the large input capacitances of a mixer switching core, which can range from several hundred femtofarads to as much as 1 pF [201]. Since this capacitance can vary due to device technology, parasitics, and process variations, it is difficult to reliably incorporate the capacitance directly into the VCO tank. Moreover, a low impedance load can severely degrade the output drive level and alter the desired frequency tuning range of the oscillator. Therefore, buffers, such as emitter- or source-followers, which present a high impedance to the VCO, are typically employed at the outputs of the VCO, thereby buffering it from the low load impedance.

For the QVCO designed here, common collector buffers using SiGe HBTs ( $4.9 \mu\text{m} \times 0.245 \mu\text{m}$ ) are employed at the outputs of the QVCO. However, to remove amplitude imbalances between the outputs, a differential variable-gain stage is added at the output of each buffer. The adjustable gain is achieved with PMOS active-load transistors ( $6.74 \mu\text{m} \times 0.18 \mu\text{m} \times 4$ ), which are located at the collectors of the differential pair; by changing the gate voltage of the PMOS devices over the range of 0.2–1.8 V, the current through the differential pair can be adjusted so as to change the gain of the circuit. The differential pair is also realized with SiGe HBTs, sized to be  $9.8 \mu\text{m} \times 0.245 \mu\text{m}$ . Since the signal swing from the buffered output of the QVCO is relatively large, resistive degeneration ( $25 \Omega$ ) in each emitter of the differential pair is used to extend the compression point of the amplifier. Figure 6.14 shows the full

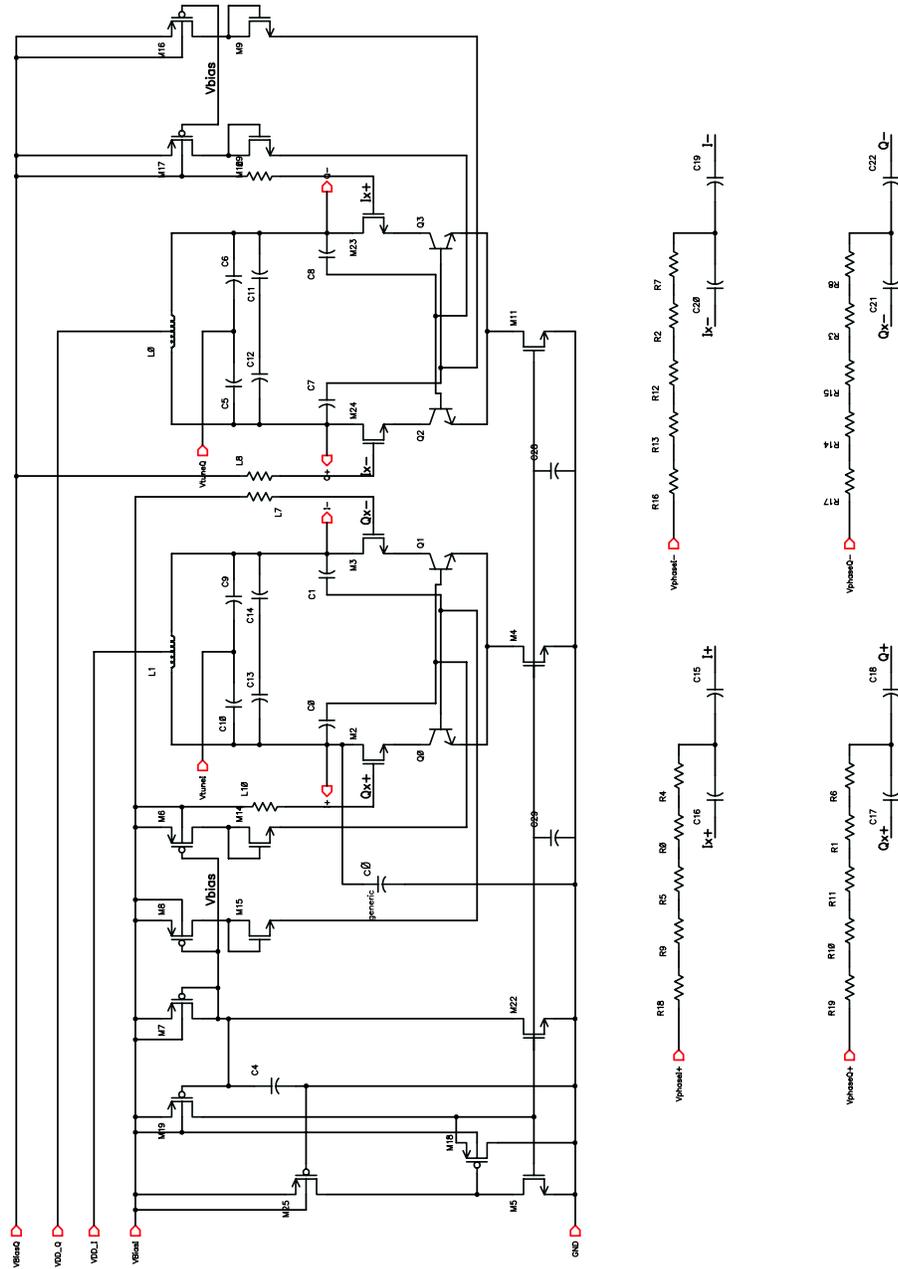


Figure 6.12: Full Cadence schematic of the CPPT-QVCO.

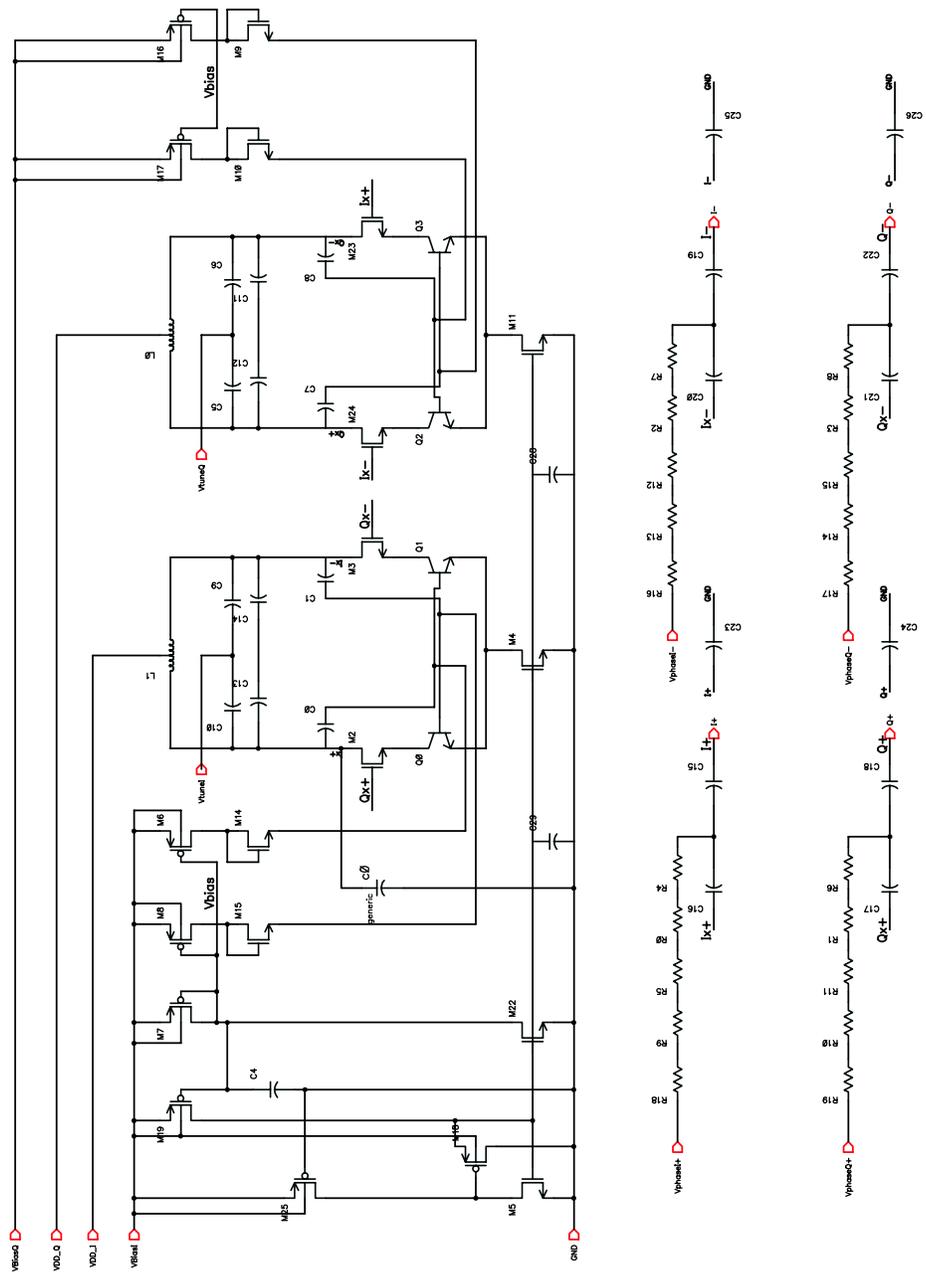


Figure 6.13: Full Cadence schematic of the ODPT-QVCO.

schematic of the buffer/amplifier circuit. The bias circuit topology is identical to that of the QVCO designs.

### 6.2.3 Quadrature VCO Layout

The layouts of the two phase-tunable QVCOs are nearly identical, which allows for the direct comparison between the two proposed methods of phase tuning. Figure 6.15 shows the Cadence Virtuoso layout of the CPPT-QVCO<sup>5</sup>. The layout is symmetric about the  $y$ -axis to maximize the benefits of the differential circuitry while the I and Q VCO cores are mirrored about the  $x$ -axis. This latter mirroring ensures that the distance between the two differential inductors is maximized, which reduces the potential for mutual coupling between them. The QVCO outputs are connected directly to the variable-gain buffer/amplifier with the I outputs on the right-side of the die and the Q outputs on the left-side for the CPPT-QVCO and vice versa for the ODPT-QVCO. The outputs switch sides due to the placement of the varactors for the two different phase tuning schemes; the switch allows the layout to maintain symmetry while also keeping the two VCOs in consistent positions on the die, i.e. the top VCO provides the “I” phases and the bottom VCO provides the “Q” phases. Secondary I and Q outputs from the buffer/amplifiers are located at the top and bottom of the chip and are included for a proposed time-domain test setup, to be described below in Section 6.2.5. The phase tuning voltages are denoted as  $VPhaseI+$ ,  $VPhaseI-$ ,  $VPhaseQ+$ , and  $VPhaseQ-$ ; the amplitude tuning voltages are labeled as  $VAmpTI$  and  $VAmpTQ$ ; and the frequency tuning voltages are marked  $VTuneI$  and  $VTuneQ$ .

The Freescale HIP6WRF process provides “tile block” layers that can be used to control the placement of dummy metal-fill patterns. To prevent area-fill around the VCO cores, the tank components and the  $-G_m$  circuits are surrounded by the “all tile block” layer, which prevents area-fill on all five metal layers. In areas where the density of components is low, selective tile blocking is used to prevent area-fill on the metal layers directly above and/or below signal routings. Since the metal-fill patterns are accounted for in the layout by ensuring that sensitive areas of the circuit are protected, in principle, there should be no detrimental effects from metal patterning (as was seen with the SHMs and DCR front-end in Chapters 3 and 5).

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<sup>5</sup>The layout of the ODPT-QVCO is not discernibly different and is therefore not shown.

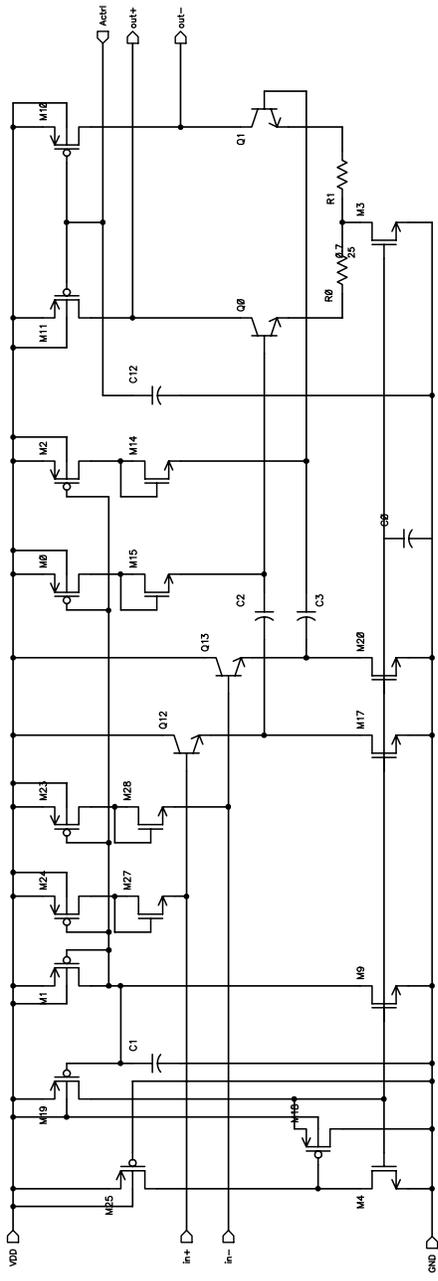


Figure 6.14: Full Cadence schematic of the buffer/amplifier circuit.

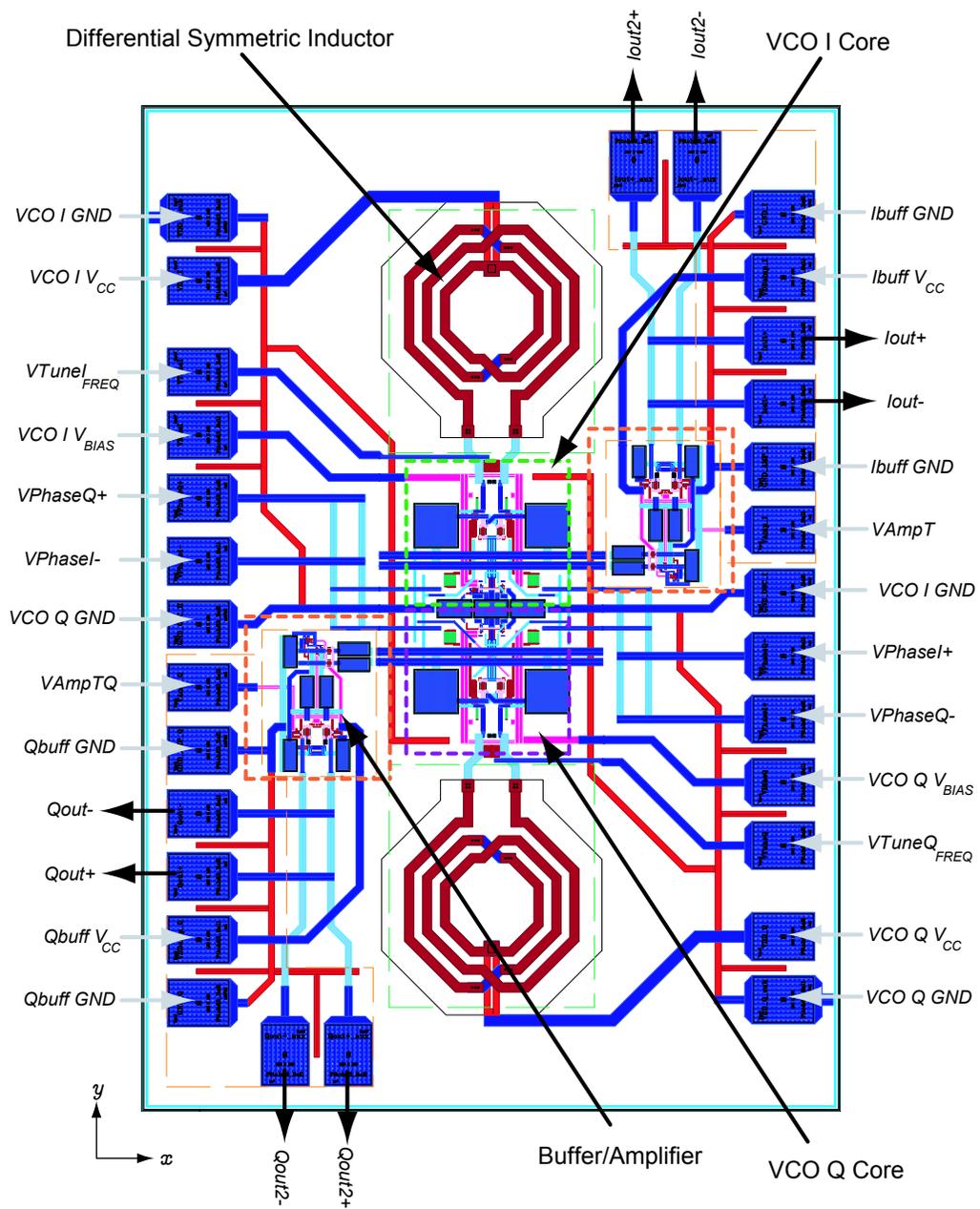


Figure 6.15: Layout of the CPPT-QVCO. The layout of the ODPT-QVCO is virtually identical.

The pad assignments for the two QVCOs are given in Table 6.1. The upper left corner of the die (as shown in Figure 6.15) is considered *Pad 1* and the pad numbers proceed in a counter-clockwise fashion. Because of the different phase tuning schemes, the I and Q outputs switch sides for the ODPT-QVCO. Otherwise, the pad assignments are identical. A separate DC voltage rail, denoted as  $V_{BIAS}$ , is included for the I and Q oscillators. As in the mixers of Section 2.2.2, this additional rail connects to the current mirror reference of each oscillator and allows for an extra degree of control over the bias current of each VCO core.

## 6.2.4 Quadrature VCO Simulations

Using Cadence Design Systems, version 5.0.33 [240], transient time-domain analyses were performed to verify the output swing of the QVCOs and to ensure that the oscillation was sustained over several periods. For nonlinear analysis, PSS simulations were used and the phase-tunability, output power, and frequency of oscillation for the two QVCO designs were determined. The variable-gain buffer/amplifiers of Section 6.2.2 were included in each of these simulations. The differential outputs of the buffer/amplifier were terminated with single-ended  $50\ \Omega$  loads. The gain of the amplifier was fixed to its maximum value, which was achieved at an amplitude tuning voltage ( $V_{ampT}$ ) of  $0.23\ \text{V}$ . Although there are four phase tuning voltages, which can be tuned independently, the two I tuning voltages and the two Q tuning voltages were tied together to simplify the simulations. To ensure the phase balance could be tuned both above and below  $90^\circ$ , the I and Q tuning voltages were swept simultaneously, but in opposite directions. In other words, the phase tuning voltage for the I-side of the QVCO ( $V_{PhaseI\pm}$ ) was swept from  $0$  to  $1.8\ \text{V}$  while the Q-side of the QVCO ( $V_{PhaseQ\pm}$ ) was swept from  $1.8$  to  $0\ \text{V}$ , or  $V_{PhaseQ\pm} = 1.8\ \text{V} - V_{PhaseI\pm}$ . The simulated data discussed below are shown in terms of the positive sweep of the I-side tuning voltage to simplify the plots; however, the x-axis also represents the Q-side tuning voltage by simply subtracting the value at a given point on the  $x$ -axis from  $1.8$ .

Figure 6.16 shows the simulated output powers of (a) the CPPT-QVCO and (b) the ODPT-QVCO as functions of the phase-tuning voltage sweep. For the CPPT-QVCO, the output power level into a  $50\ \Omega$  load is roughly  $-1.8\ \text{dBm} \pm 0.085\ \text{dB}$  while

Table 6.1: Pad assignments for the CPPT-QVCO and the ODPT-QVCO.

Pad No.	CPPT-QVCO	ODPT-QVCO
1	VCO I GND	VCO I GND
2	VCO I V <sub>CC</sub>	VCO I V <sub>CC</sub>
3	VCO I V <sub>tuneFREQ</sub>	VCO I V <sub>tuneFREQ</sub>
4	VCO I V <sub>BIAS</sub>	VCO I V <sub>BIAS</sub>
5	VPhaseQ+	VPhaseQ+
6	VPhaseI-	VPhaseI+
7	VCO I GND	VCO I GND
8	VAmptQ	VAmptI
9	Qbuff GND	Ibuff GND
10	Qout-	Iout-
11	Qout+	Iout+
12	Qbuff V <sub>DD</sub>	Ibuff V <sub>DD</sub>
13	Qbuff GND	Ibuff GND
14	Qout-	Iout-
15	Qout+	Iout+
16	VCO Q GND	VCO Q GND
17	VCO Q V <sub>CC</sub>	VCO Q V <sub>CC</sub>
18	VCO Q V <sub>tuneFREQ</sub>	VCO Q V <sub>tuneFREQ</sub>
19	VCO Q V <sub>BIAS</sub>	VCO Q V <sub>BIAS</sub>
20	VPhaseQ-	VPhaseI-
21	VPhaseI+	VPhaseQ-
22	VCO Q GND	VCO Q GND
23	VAmptI	VAmptQ
24	Ibuff GND	Qbuff GND
25	Iout-	Qout-
26	Iout+	Qout+
27	Ibuff V <sub>DD</sub>	Qbuff V <sub>DD</sub>
28	Ibuff GND	Qbuff GND
29	Iout-	Qout-
30	Iout+	Qout+

the output power level for the ODPT-QVCO is  $-6 \text{ dBm} \pm 0.52 \text{ dB}$ . Both power levels should be more than sufficient for driving the switching core of a mixer, as described in Section 2.2.2. The difference in output power between the I and Q sides of the ODPT-QVCO is expected since the phase tuning varactors are embedded in a capacitive voltage divider and directly affect the output amplitude. However, the difference in output power between the I and Q sides — along with the increasing output power of the CPPT-QVCO versus tuning voltage — can be corrected by dynamically adjusting the gain of the buffer/amplifier.

The frequencies of oscillation ( $f'_0$ ) for the CPPT-QVCO and the ODPT-QVCO are shown in Figures 6.17(a) and 6.17(b), respectively. The coupling path phase-tuning varactors in the CPPT-QVCO ( $f'_0 \approx 5.70 \pm 0.003 \text{ GHz}$ ) have an order-of-magnitude smaller effect on the output frequency compared to the output divider varactors in the ODPT-QVCO ( $f'_0 \approx 5.17 \pm 0.018 \text{ GHz}$ ). The difference in frequency shift between the two phase tuning methods is a straightforward result of the output divider varactors being connected directly to the tank circuit while the coupling path varactors are isolated from the tank by the coupling transistors.

Figures 6.18(a) and 6.18(b) show the output quadrature phase balance of the CPPT-QVCO and the ODPT-QVCO, respectively. The balance is achieved by first, subtracting the plus and minus differential voltages of the I and Q sides of the VCO and second, subtracting the phase of these two signals, as shown in Equation 6.6.

$$\Delta\phi = \text{phase}(I+ - I-) - \text{phase}(Q+ - Q-) \quad (6.6)$$

The figures show that a  $90^\circ$  phase balance is achieved near the center of the tuning range, where the I tuning voltage is  $\sim 0.92 \text{ V}$  and the Q tuning voltage is  $1.8 - 0.92 = 0.88 \text{ V}$ ; the resulting ranges of phase tuning are  $[-100^\circ, -83^\circ]$  for the CPPT-QVCO and  $[-104^\circ, -81^\circ]$  for the ODPT-QVCO. Thus, the CPPT-QVCO offers  $17^\circ$  of phase tunability around  $90^\circ$  while the ODPT-QVCO offers  $23^\circ$ .

The total DC current consumption for the entire oscillator (both VCO cores together) from a  $1.8 \text{ V}$  supply is simulated to be  $10.8 \text{ mA}$  for the CPPT-QVCO and  $10.2 \text{ mA}$  for the ODPT-QVCO. As noted above, the buffer/amplifier consumes  $6.2 \text{ mA}$ . Thus, the total simulated DC current consumption for the entire chip — both the QVCO and its two buffer/amplifiers — is  $(2 \cdot 6.2 + 10.8) = 23.6 \text{ mA}$ , for a total power consumption

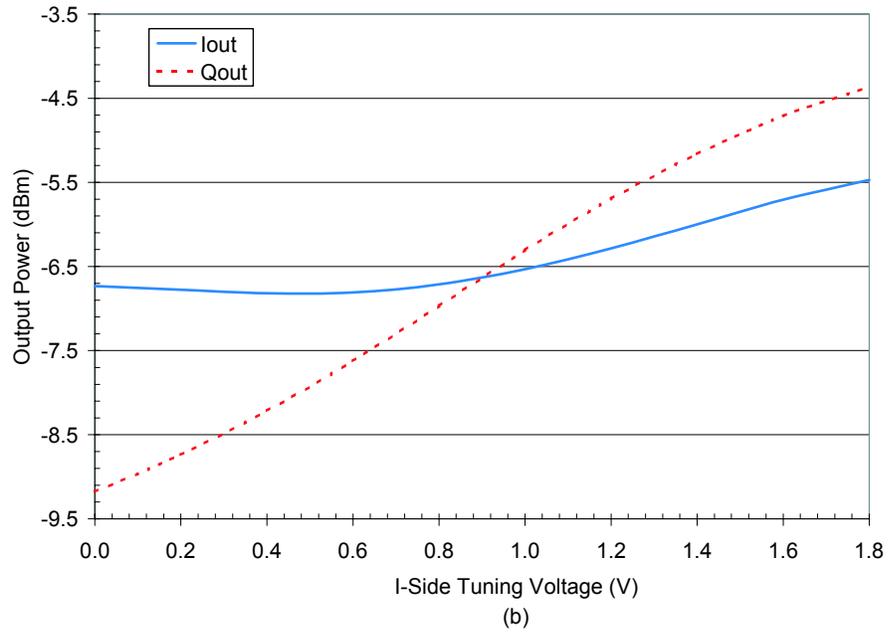
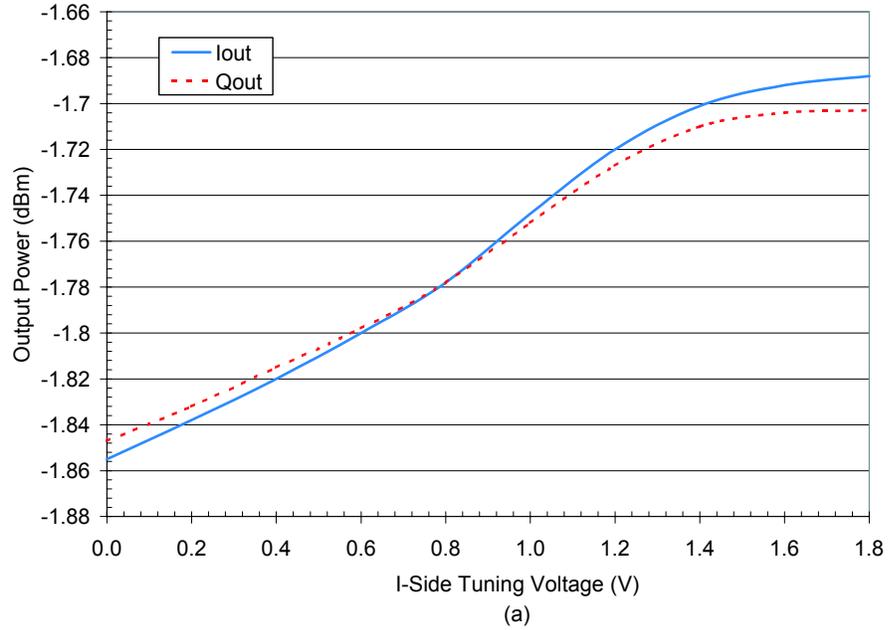


Figure 6.16: Simulated output power for (a) the CTPT-QVCO and (b) the ODPT-QVCO versus the phase tuning voltage of the I-side VCO. The Q-side tuning voltage is found by subtracting the  $x$ -axis value from 1.8 V.

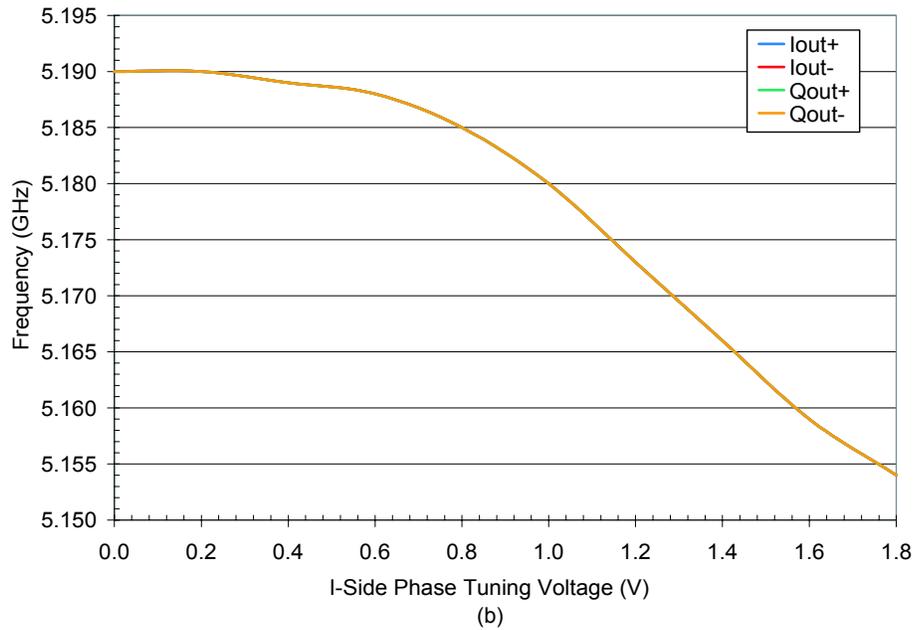
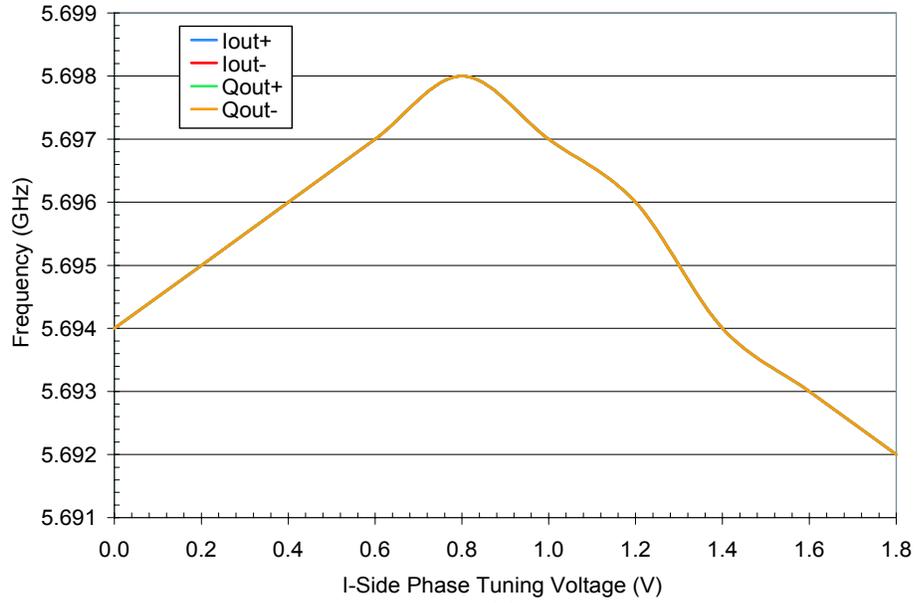


Figure 6.17: Simulated frequency of oscillation for (a) the CPPT-QVCO and (b) the ODPT-QVCO versus the phase tuning voltage of the I-side VCO. The Q-side tuning voltage is found by subtracting the  $x$ -axis value from 1.8 V. Only one line is visible in the plots since all four sets of data are identical.

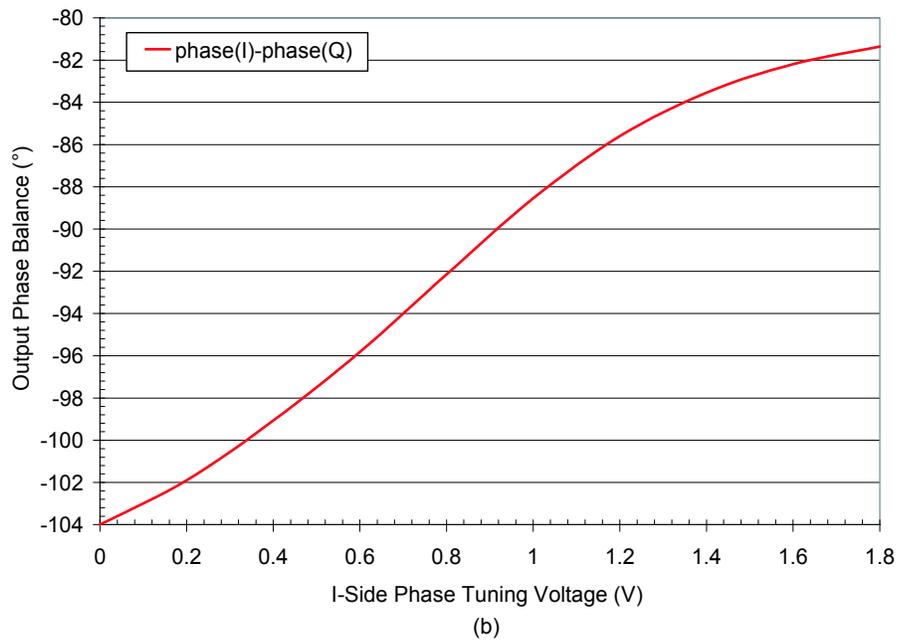
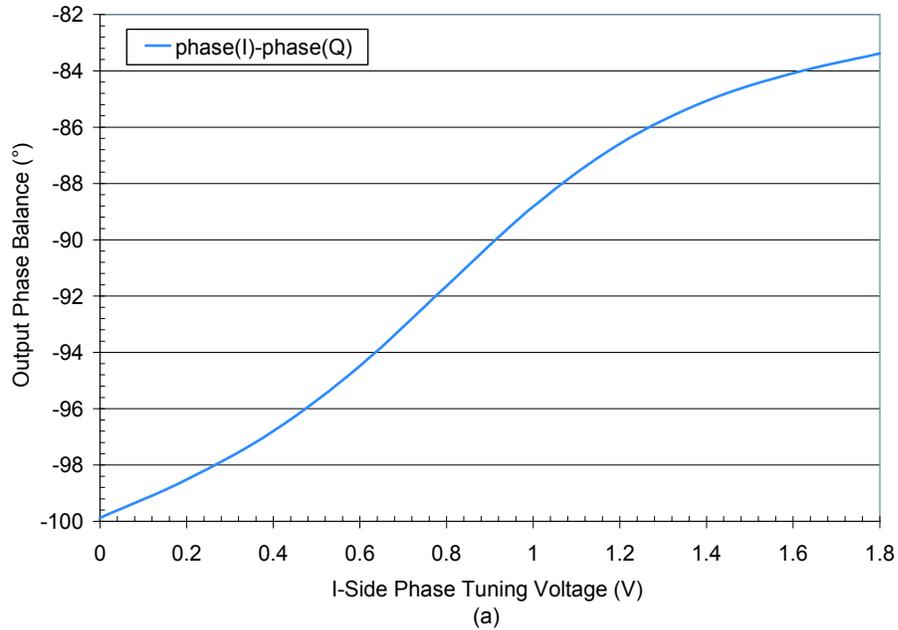


Figure 6.18: Simulated output phase balance for (a) the CPPT-QVCO and (b) the ODPT-QVCO versus the phase tuning voltage of the I-side VCO. The Q-side tuning voltage is found by subtracting the  $x$ -axis value from 1.8 V.

of 42.5 mW.

## 6.2.5 Proposed Quadrature VCO Test Setups

The typical method for measuring the I/Q amplitude and phase imbalance of QVCOs (and other quadrature generation schemes) is to use the circuit as the LO source for driving a set of Weaver image-reject upconversion mixers. Figure 6.19 shows a block diagram of the test circuit. As described in Section 1.3.2, the image-reject mixers attenuate one of the mixing sidebands based on the phase and amplitude balance of the LO signal. Therefore, this circuit can be used to *indirectly* determine the phase and amplitude imbalances of the QVCO. By measuring the IRR of the RF signal at the output of the mixers (see Equation 1.14), the overall imbalance between the QVCO outputs can be determined [242]. One drawback to this approach lies in the generation of the quadrature baseband signal, which is typically done using *RC* polyphase filters. Any phase or amplitude errors introduced to the baseband signals by these filters degrade the measured IRR. Furthermore, there is no way to distinguish the amplitude imbalances of the QVCO from the phase imbalances (or vice-versa) with this method, since only the ratio of power between the desired spectrum and the image signal is measured.

On the other hand, time domain test setups (e.g. one utilizing an oscilloscope) are well-suited for the determination of the quadrature channel imbalances. Since the QVCO generates sinusoidal signals, an oscilloscope is ideal for capturing and displaying the output waveforms, allowing the phase difference between the signals to be straightforwardly determined. However, to operate at gigahertz frequencies, modern oscilloscopes typically rely on sub-sampling of the input signal to display the waveforms<sup>6</sup>. The sub-sampling approach requires an external trigger signal at a lower frequency than the input signal. The trigger signal clocks the internal sampling circuit of the oscilloscope to take measurements of the input signal every  $T$  cycles, where  $T$  is the period of the trigger signal.

To measure quadrature phases accurately using sub-sampling scopes, the trigger signal

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<sup>6</sup>It should be noted that the maximum input signal frequency of modern oscilloscopes continues to increase; “real-time” oscilloscopes capable of measuring the signals in the 5 to 6 GHz band with trigger signals operating at the same frequency are now commercially available [243].

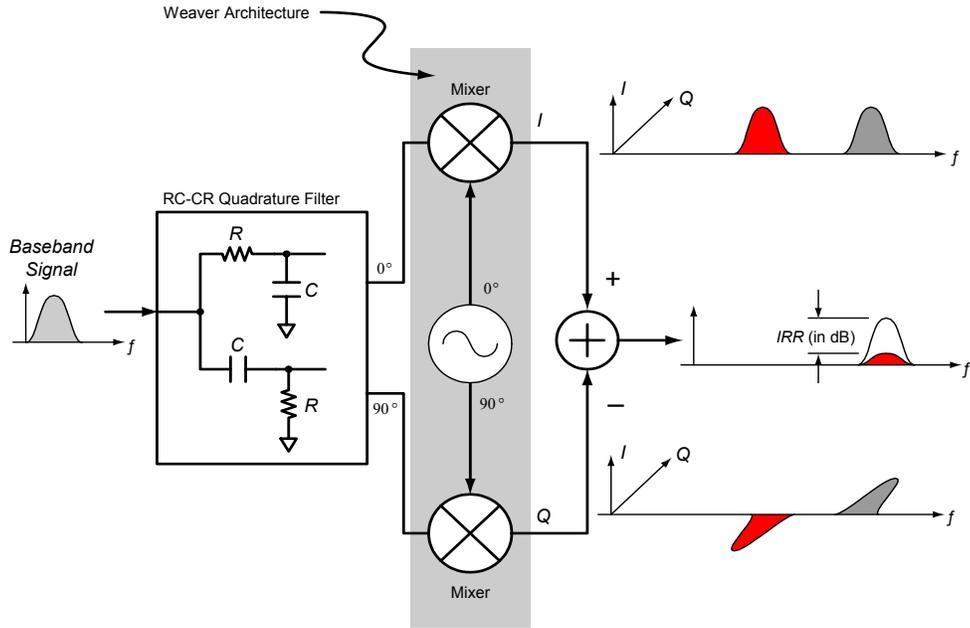


Figure 6.19: Test setup utilizing the Weaver image-rejection architecture to measure the amplitude and phase imbalances of the QVCO.

and the input signal must be phase-locked to each other to guarantee that the relative timing between the signals' zero crossings, which in turn are used to determine the phase, are correct. The zero-crossings are found by referencing the input signal to the trigger signal. The phase-lock requirement implies that the signal-of-interest cannot simply be fed into off-the-shelf components, such as a power divider, to provide both the trigger and the input signal; these components typically exhibit 3–6° of inherent phase error, which is serious enough to shift the zero-crossings of the input signals from their actual phase relationship. Thus, the need for a replica of the input signal motivates the incorporation of secondary outputs in the QVCO layouts mentioned above. With this output configuration, both the trigger and input signals are derived from the same source and, therefore, have the same phase. However, for both outputs to be usable directly, an oscilloscope capable of measuring and triggering on signals in the 5–6 GHz band must be used. Unfortunately, the sub-sampling oscilloscope presently available has a maximum trigger frequency of 2 GHz, which means the secondary QVCO outputs would have to be fed into a divide-by-2 circuit to make the measurements. A divide-by-2 circuit could be designed and included on the chip with each QVCO, but such an approach is risky for a research prototype due to the

increased complexity, mixed-signal coupling issues, etc.

For the tunable QVCO, the measurement of interest (with respect to RF receiver design) is the effect of a tunable quadrature LO signal on the quadrature IF outputs of a receiver. To investigate these effects, another set of designs was developed to measure the I/Q IF amplitude and phase balance directly by connecting the QVCO as the LO source to a set of quadrature downconversion mixers. These fundamental mixers were based on the basic Gilbert cell topology (see Section 2.2.1) and were designed for operation in the 5–6 GHz band. The mixer layouts were completed so as not to affect the floor plan of the existing QVCO layout (Figure 6.15). Figure 6.20 shows the layout of the CPPT-QVCO with the I and Q RF mixers; a similar layout was also completed for the ODPT-QVCO.

Since the mixers perform downconversion, an additional benefit of this test setup is that the output frequency from the chip is an IF, which can be in the range of tens of megahertz. Such a low frequency is well within the bandwidth of standard oscilloscopes. Thus, the Agilent 54624A oscilloscope that was used for the I/Q phase balance measurements of the DCR front-end in Section 5.1.8 can also be used to measure the I/Q amplitude and phase balance and tunability of the QVCOs. Figure 6.21 shows a block diagram of the proposed test setup. The secondary outputs are again used to provide a trigger signal to the oscilloscope to guarantee the signal zero-crossings are referenced to the same signal.

The layouts described above in Section 6.2.3 are currently awaiting fabrication; therefore, measured results utilizing the proposed test setups are not yet available.

### 6.3 Summary

This chapter presented the design, simulation, and layout of a phase and amplitude tunable quadrature voltage controlled oscillator. Two methods for achieving the phase tunability were developed: (1) using series varactors in the coupling paths between the two *LC*-tank VCOs (CPPT-QVCO); and (2) using capacitive dividers at the output of the QVCO with varactors as the series element of the divider (ODPT-QVCO). Amplitude tunability was provided by a buffer/amplifier circuit that was connected to the outputs of the QVCO. The amplifier portion included active, PMOS

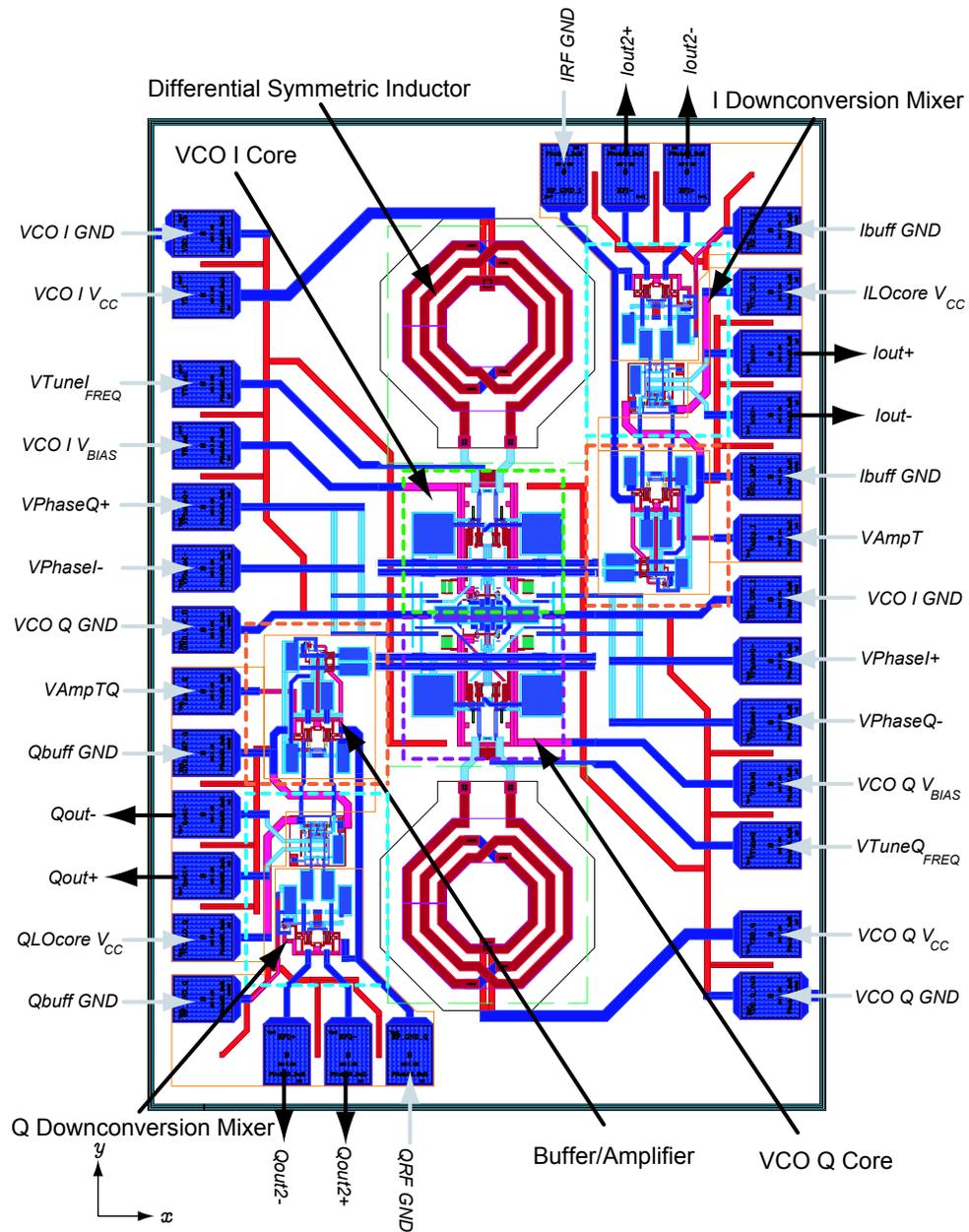


Figure 6.20: Layout of the CPPT-QVCO with fundamental mixers.

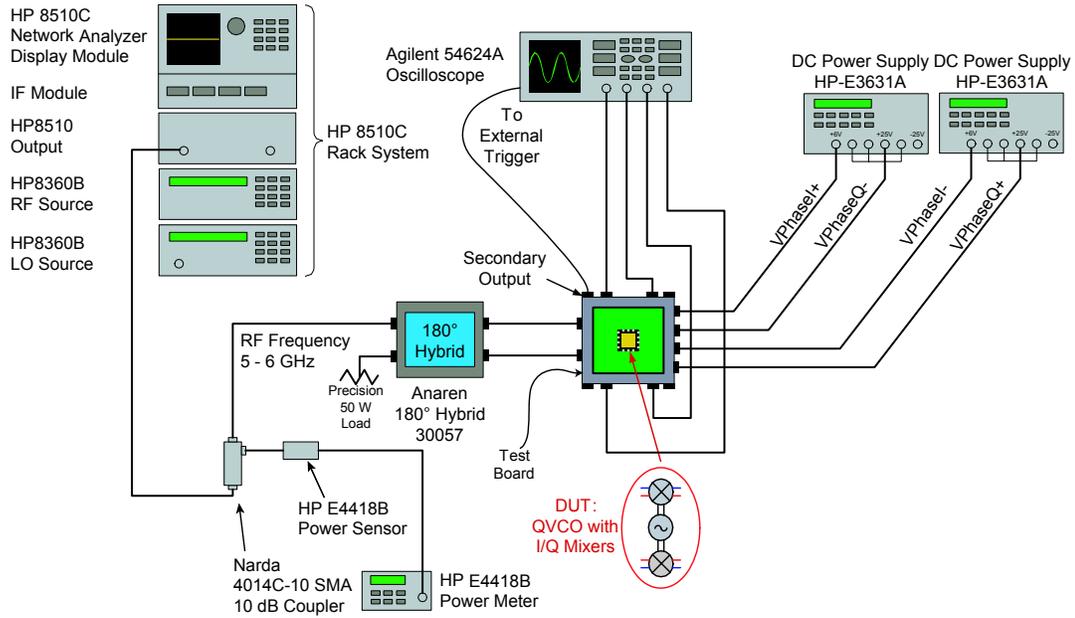


Figure 6.21: Proposed test setup for measuring the amplitude and phase tunability of the QVCO using on-chip fundamental mixers.

loads that could control the gain of the circuit, thereby providing the ability to adjust the amplitude balance between the QVCO differential outputs.

Simulations of the CPPT-QVCO showed that the I/Q phase difference could be varied from  $-100^\circ$  to  $-83^\circ$ , or a range of  $17^\circ$ , while simulations of the ODPT-QVCO showed the phase balance could be varied from  $-104^\circ$  to  $-81^\circ$ , or a range of  $23^\circ$ . The simulated output power level and center frequency of the QVCO-buffer/amplifier combination were  $\sim -1.8$  dBm and 5.7 GHz for the CPPT-QVCO and  $\sim -6$  dBm and 5.2 GHz for the ODPT-QVCO, respectively. The buffer/amplifier consumed 6.8 mA of current and since two were required for each QVCO, consumed a total of 13.6 mA; the CPTP-QVCO consumed 10.8 mA and the ODPT-QVCO consumed 10.2 mA. The total current consumption of each QVCO and the two buffer/amplifier circuits together was roughly 24 mA. The designs are currently awaiting fabrication and therefore, the measured results are not yet available.

## Chapter 7

# Patterned Ground Shield Inductors

**T**HE demand for low-cost, highly-integrated RF/mixed-signal circuits has not only driven the development of advanced high-speed transistor devices, but also high-quality, on-chip passives. For integrated resistors and capacitors, technological advances have resulted in on-chip performance that rivals that of their off-chip counterparts; however, for integrated inductors, similar performance gains have been more difficult to achieve. In fact, the modern monolithic inductor is the culmination of more than a decade of research dedicated solely to the optimization and improvement of on-chip inductor performance [244–254]. Despite this significant amount of research, the  $Q$  of on-chip inductors in silicon processes remains relatively low, typically falling within the range of 5 to 30. The importance of inductors in RF ICs can be seen in the circuit designs discussed in the previous chapters, where inductors played a critical role in impedance matching (between the LNA and mixer), emitter degeneration (for linearity improvement in the mixer), and tuning (to obtain the desired output frequency in the QVCO). In each case, the availability of higher quality inductors would have improved the overall performance of the designs.

This chapter presents the design, modeling, and characterization of an improved type of inductor — the *patterned ground shield* inductor — in the Freescale HIP6WRF SiGe:C BiCMOS process (see Section 1.2.4). The insertion of a patterned ground shield between the inductor coil and the underlying substrate has been demonstrated to mitigate substrate losses, which are a major factor in  $Q$ -degradation [255]. In addition, a scalable lumped-element model is proposed for predicting the peak- $Q$  and

self-resonant frequency ( $f_{SR}$ ) of the inductors, with and without the shield. The chapter begins with a review of the definition of  $Q$  and the inductor loss mechanisms that are typical on silicon substrates. Next, a large-scale monolithic inductor characterization-experiment is described in detail, and the measured results are presented. Finally, the scalable lumped element model is proposed and the simulated results of the model are compared with the measured results.

## 7.1 Monolithic Inductors

To date, the most effective on-chip structures for providing reasonable values of inductance in GHz-range RF circuits have been metal spirals that lie parallel to the underlying semiconductor substrate [Figure 7.1(a)]. These types of coils are advantageous since, in general, they do not require extra processing steps during fabrication when implemented in a standard multi-level interconnect Si technology. Figures 7.1(b)-7.1(d) show three single-ended planar inductor structures that are commonly used in modern ICs; in each case, at least two metal layers are required — one layer for the coil itself and another for the underpass to connect to the center of the structure. Generally speaking, the octagonal and circular structures [Figure 7.1(b) and 7.1(c)] have less overall loss when compared to rectangular structures [Figure 7.1(d)] of equivalent inductance values, but also exhibit less inductance per unit area [256]. Historically, rectangular spirals have been the only option for inductors due to their compatibility with low-cost mask generation systems, which are only able to realize features at right-angles ( $90^\circ$ ) to each other; however, as manufacturing has advanced, it has also become common for angles of  $45^\circ$  (to make octagonal structures) to be supported.

In Figure 7.1(e), a symmetric, differential inductor is shown; this structure is essentially a matched pair of inductors in series, but inter-wound such that the currents through the two coils flow in the same direction. Since these currents each generate a magnetic field, the symmetric structure ensures that the magnetic fields are oriented in the same direction, rather than opposing each other, which would tend to lower the effective inductance and  $Q$ . A layout of an octagonal symmetric differential inductor is shown in Figure 7.2. The symmetry of the layout guarantees a virtual ground point where the two coils meet (*Port 3*), which is important for differential circuitry

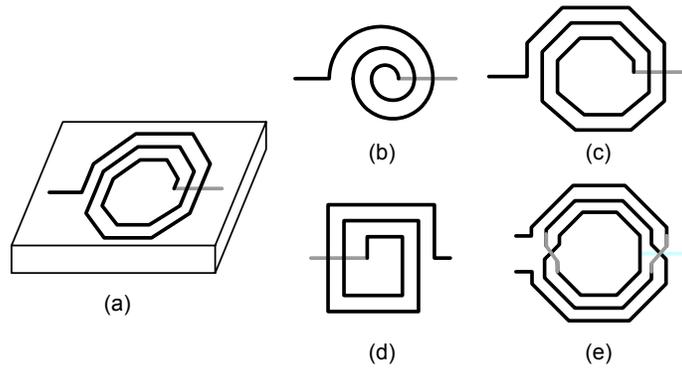


Figure 7.1: (a) View of an in-plane inductor spiral; top view of three common spirals: (b) circular; (c) octagonal; and (d) rectangular; (e) implementation of a differential symmetric inductor spiral.

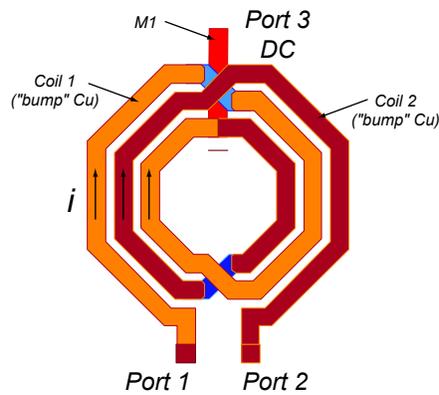


Figure 7.2: Layout of a symmetric, differential inductor.

in rejecting common mode signals. The third port also offers a connection point for DC biasing. This type of inductor was used in the QVCOs of the previous chapter.

The definition of inductor quality factor, a summary of loss mechanisms, and potential methods for improving inductor performance are discussed in the following sections.

### 7.1.1 Quality Factor ( $Q$ )

The  $Q$  of a passive component is a measure of its ability to store energy. For an ideal reactive circuit element, the energy stored over a cycle of an applied signal is theoretically infinite; however, real-world implementations of such components result

in unavoidable losses that dissipate energy and lower the  $Q$ . The fundamental definition of  $Q$  is given as a ratio of the energy stored ( $E_{\text{stored}}$ ) to the energy dissipated ( $E_{\text{diss}}$ ) per cycle of oscillation:

$$Q = 2\pi \frac{E_{\text{stored}}}{E_{\text{diss}}}. \quad (7.1)$$

More specifically, for an inductor,  $E_{\text{stored}}$  represents the fraction of injected-energy that is stored within the magnetic field of the inductor coil while  $E_{\text{diss}}$  represents the portion of total injected-energy that is lost due to parasitic resistances. Since, for an inductor, only the energy stored within the magnetic field is useful to external circuitry, any energy stored within the electric fields of the structure is essentially lost [257]. These electric fields are found in the parasitic capacitances associated with the physical implementation of the inductor as a planar structure. In this case, Equation 7.1 can be re-written in terms of the peak energy stored in the magnetic field ( $E_{\text{mag,pk}}$ ) and the peak energy lost in the electric field ( $E_{\text{elec,pk}}$ ):

$$Q = 2\pi \frac{|E_{\text{mag,pk}} - E_{\text{elec,pk}}|}{E_{\text{diss}}}. \quad (7.2)$$

Equation 7.2 also dictates the inductor self-resonant frequency ( $f_{SR}$ ) in terms of the electric and magnetic field energies: when equal amounts of energy are stored in each field, the inductor is at self-resonance and the  $Q$  drops to 0. Beyond the  $f_{SR}$ , the inductor is dominated by its parasitic capacitances and the majority of energy storage is in the electric field (capacitive).

The peak energy stored in the magnetic and electric fields and the energy dissipated per cycle can be rewritten to express them in terms of a peak applied-voltage,  $V_{\text{pk}}$ :

$$E_{\text{mag,pk}} = \frac{V_{\text{pk}}^2}{8\pi^2 f^2 L} \quad (7.3)$$

$$E_{\text{elec,pk}} = \frac{V_{\text{pk}}^2 C}{2} \quad (7.4)$$

$$E_{\text{diss}} = \left(\frac{1}{f}\right) \left(\frac{V_{\text{pk}}^2}{2R}\right) \quad (7.5)$$

where  $R$  represents the resistive losses inherent to the inductor coil. Substituting Equations 7.3-7.5 into Equation 7.2, the inductor  $Q$  can be re-written as a function

of frequency:

$$Q = \frac{R}{2\pi fL} \left[ 1 - \left( \frac{f}{f_{SR}} \right)^2 \right] \quad (7.6)$$

### 7.1.2 Inductor Loss Mechanisms

Inductor losses can be grouped in to two main categories: *conductor losses*, which are due to effects or properties of the coil conductor; and *substrate losses*, which are due to the integration of the structure on a lossy medium. Conductor losses include thin-film resistivity (or sheet resistance), skin effect, and eddy currents (current crowding), and are covered extensively in literature [59, 208, 209, 256, 258]. In the last few years, these losses have been aggressively confronted with the use of thick, metal layers (such as Al or Cu) for the top-level interconnect material, a practice that is now nearly standard in modern RF CMOS and BiCMOS processes. These various conductor loss mechanisms are typically lumped together and treated as a frequency-dependent resistance in series with the ideal inductance; this resistance directly dissipates energy from within the coil windings.

Substrate losses, on the other hand, are a result of implementing the coil structure above and in parallel to a non-insulating substrate. While this lossy substrate is undesirable for RF circuits, it has historically been necessary to prevent latch-up in digital circuits, the dominant driver of Si technology. For an inductor however, the electric and magnetic fields of the structure penetrate into the underlying lossy substrate and couple energy away from the coil, where the energy is dissipated through the resistance of the substrate. Furthermore, the time-varying magnetic field of the inductor, which is induced by high-frequency current passing through the coil, can induce eddy currents within the low-resistivity substrate and further dissipate energy through resistive heat. These eddy currents also induce their own magnetic fields, which oppose the inductor's magnetic field, and lower the overall inductance [259].

Figure 7.3 shows a cross-section of a typical rectangular inductor and illustrates the magnetic and electric field lines that couple from the inductor to the substrate. For a silicon CMOS/BiCMOS based inductor, the electric field lines represent the capacitance between the bottom of the coil and the substrate. To determine this capacitance, the area ( $A$ ) of the spiral and the underlying substrate can be approx-

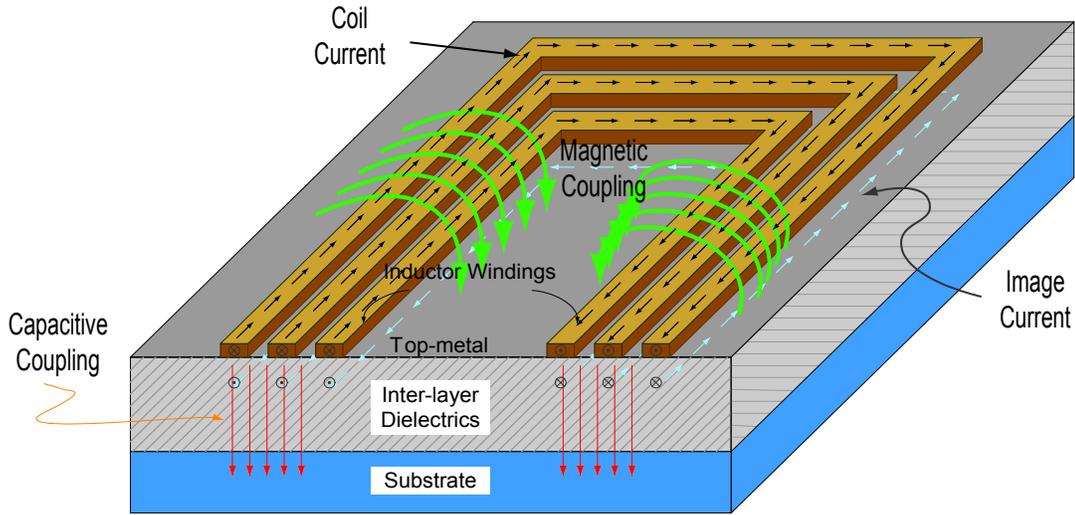


Figure 7.3: Cross-section of an integrated, rectangular inductor. The magnetic and electric field lines that result from the inductive and capacitive nature of the structure are shown.

imated as parallel plates that are separated by a combination of dielectric layers — i.e. the field oxide (which is grown directly on top of the substrate) and various inter-layer dielectrics (described in Section 3.1.1) — with a permittivity ( $\epsilon_{r,avg}$ ), which can be represented by the weighted average of the various materials. The distance between the two “plates” ( $d$ ) is determined by the number of interconnect layers and their thicknesses. Thus, the overall capacitance, typically denoted as  $C_{ox}$  for “oxide” capacitance, can be estimated as

$$C_{ox} = \epsilon_{r,avg} \epsilon_0 \frac{A}{d}, \quad (7.7)$$

where  $A$  is found from the outer diameter of the coil trace. This shunt capacitance has a significant impact on the inductor  $Q$  since it essentially AC couples RF energy from the coil down to the lossy substrate. Furthermore, the electric fields of this capacitance store energy that would otherwise be stored in the magnetic field; thus, this capacitance largely determines the self-resonant frequency of the inductor as shown in Equation 7.2.

Figure 7.3 shows that the magnetic field lines resulting from the current-flow within the coil penetrate the substrate. The time-varying RF current through the coil causes

the direction of the magnetic field to also change, which in turn, results in a time-varying magnetic flux. By Lenz’s law, an identical but opposite current to that of the coil (i.e. an image current) is induced in any conductor situated within the magnetic field of the coil — such as the lossy substrate — to resist this changing magnetic flux. Thus, the  $Q$  of the inductor is reduced since magnetic energy is dissipated by the image current passing through the resistance of the substrate. In other words, the substrate acts similar to the secondary winding of a transformer that is wound anti-phase to the primary; the magnetic field of the “primary” inductor interacts with this “secondary coil” to induce an image current in the opposite direction. Notably, the image current, while dissipating energy within the lossy substrate, also produces its own magnetic field that is opposite to that of the main coil. These two fields tend to oppose each other and lower the achievable inductance value. The combination of the above electric and magnetic substrate losses are the primary reason for the relatively poor  $Q$  values for on-chip inductors.

### 7.1.3 $Q$ -Improvement Techniques

As mentioned previously, metal losses have primarily been addressed through the use of thick upper metal layers for the coil structure. For example, IBM offers a separate “analog metal (AM)” option that provides a thick Al top metal layer specifically for analog passives and low-resistance signal paths. For the Freescale HIP6WRF process used in this portion of the research (Section 1.2.4), the addition of a  $10\ \mu\text{m}$  thick Cu “bump” layer (which projects above the chip passivation level) is provided specifically to reduce the metal losses of on-chip inductors. Alternatively, special layout/fabrication approaches, such as metal layer strapping, can be used to increase the cross-sectional area of the metal in processes where thick metal layers are not available, thereby reducing the net metal resistivity [260, 261]. These thick-metal techniques are of less value at higher frequencies ( $\gtrsim 10\ \text{GHz}$ ) though, since skin depth is significantly reduced and the additional metal thickness becomes irrelevant.

Meanwhile, various methods have been proposed to combat the losses resulting from electromagnetic coupling to the substrate, including:

- the use of high resistivity substrates [262, 263] or the selective removal of the

substrate under the inductor by micromachining [264–266] — which eliminate substrate currents and thus, energy losses due to the substrate;

- the use of active circuitry — either to enhance the quality factor of an existing spiral inductor or to replace the monolithic structure altogether — which reduces area consumption and avoids the substrate issues [267–269]; and
- the incorporation of *ground shields* — which can reduce the capacitive coupling to the lossy substrate by effectively blocking the electric field from reaching the substrate.

This last approach is particularly attractive since it does not require any changes to an established CMOS/BiCMOS process, as is the case with using high resistivity substrates or micromachining, and does not affect power consumption and noise as in the case with active enhancement.

The shielding approach uses a plane of conductive material, such as a lower interconnect metal layer or gate-polysilicon, placed between the coil and the substrate. The shield is typically connected to ground and thus, electric fields radiating from the coil couple directly to the shield — instead of the substrate — which can provide significant improvements in inductor quality factors [270]. However, a simple conductive ground shield between the inductor and substrate is subject to the flow of both image and eddy currents since the time-varying magnetic field still penetrates this layer. Like the image currents within the substrate, shield image currents degrade the overall  $Q$  factor and reduce the achievable inductance as some energy is lost in the finite resistance of the shield. To limit the induced currents, the shield can be patterned in-plane with breaks (open circuits) that are oriented perpendicular to the direction of image current flow, as introduced in [270]. Of course, the downside of the use of such ground shields is the decrease in  $f_{SR}$ , which results from the increase in shunt capacitance between the coil and the ground shield plane.

## 7.2 Experiment and Measured Results

The performance enhancement (in terms of peak- $Q$ , effective inductance, and self-resonant frequency) of shielded inductors has been studied extensively in [270–276].

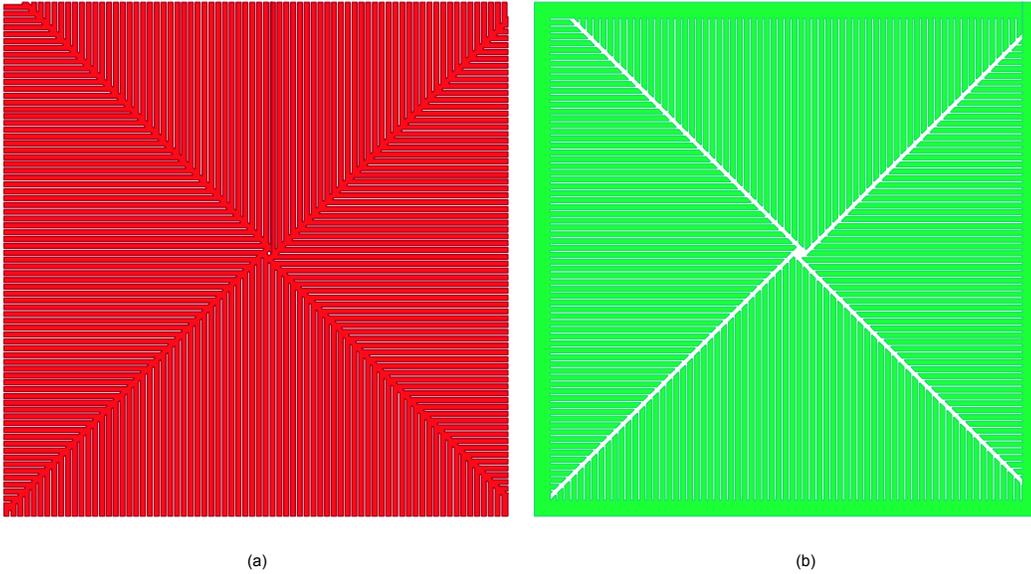


Figure 7.4: Two types of patterned ground shields: (a) the center grounded shield (CGS) and (b) the perimeter grounded shield (PGS). The shields were implemented in both metal one (M1) and polysilicon (PLY).

For example, two different methods for connecting the shield to ground were explored in [277], where the connection was made at the center of the shield (center-grounded shield, CGS) and around the perimeter of the shield (perimeter-grounded shield, PGS); the material of the shield was studied in [273, 278], with shields implemented in metal-one (M1), polysilicon (PLY), and  $N^+$ -diffusion; and the size and shape of the shield were also studied in [278]. A 30% improvement in the peak- $Q$  for inductors with a patterned shield is typical in a standard CMOS process [277].

The experimental effort presented here builds on the work in [270, 273, 277] by directly comparing both the type of ground connection — the CGS [Figure 7.4(a)] and the PGS [Figure 7.4(b)] — and the type of shield material — M1 and PLY. This effort also expands the scope of the previous work by considering the effects of the shield on structures with different values of inductance (2 nH, 4 nH, and 6 nH), which allows for the development of a scalable lumped-element model (Section 7.3) for inductors with and without a shield.

This experimental effort can be divided into two main parts: (1) the characterization of single-ended, rectangular inductor structures of different inductance values

Table 7.1: Dimensions for the various inductor structures used in the experiment.

Inductance	Number of Turns ( $N$ )	Length	Width	Spacing	Area
2 nH	3.5	1470 $\mu\text{m}$	6 $\mu\text{m}$	6 $\mu\text{m}$	20.9 $\text{mm}^2$
4 nH	4.5	2550 $\mu\text{m}$	6 $\mu\text{m}$	6 $\mu\text{m}$	37.3 $\text{mm}^2$
6 nH	4.5	3380 $\mu\text{m}$	6 $\mu\text{m}$	6 $\mu\text{m}$	57.3 $\text{mm}^2$
1.4 nH Sym. Diff.	1.5	1195 $\mu\text{m}$	6 $\mu\text{m}$	6 $\mu\text{m}$	29.0 $\text{mm}^2$

and with different patterned ground shields; and (2) the effect of patterned ground shields on an octagonal, symmetric differential inductor with a fixed value of inductance (1.4 nH). In both cases, wafer-level probing was used to measure the performance of the inductors. For the single-ended inductors, ground-signal-ground (GSG) pad configurations were used to provide access points to the inductor for the RF measurement probes while for the differential structures, both GSG and ground-signal-signal-ground (GSSG) probe configurations were used. The layout of the inductor array in the HIP6WRF technology used in this experiment is shown in Figure 7.5. The dimensions of the various rectangular inductors and the symmetric differential inductor are given in terms of the number of turns, the total length of the spiral (from one end of the copper trace to the other along the center-line of the trace), and the width of the trace in Table 7.1.

The 5 mm  $\times$  5 mm reticle (Figure 7.5) is divided roughly vertically down the center to address the two different types of inductor structures. The array on the left-hand half of the reticle is comprised of single-ended, rectangular parameterized-cell (PCELL) inductors. For each value of inductance (2 nH, 4 nH, and 6 nH), test inductors are laid out in both one-port and two-port test configurations (the top and bottom halves of the left-side, respectively) and with a different shield in a different material under each structure (30 total test structures). For example, the one-port 2 nH inductor, which lies in the upper left-hand corner of the chip, is duplicated five times across the top row with the following underlying shield configurations (moving left to right): (1) no shield; (2) M1 CGS; (3) PLY CGS; (4) M1 PGS; and (5) PLY PGS. On the bottom-half of the left-side, the two-port inductors are arranged the same way. For the one-port inductors, the underpass-side of the inductor is tied to ground via a

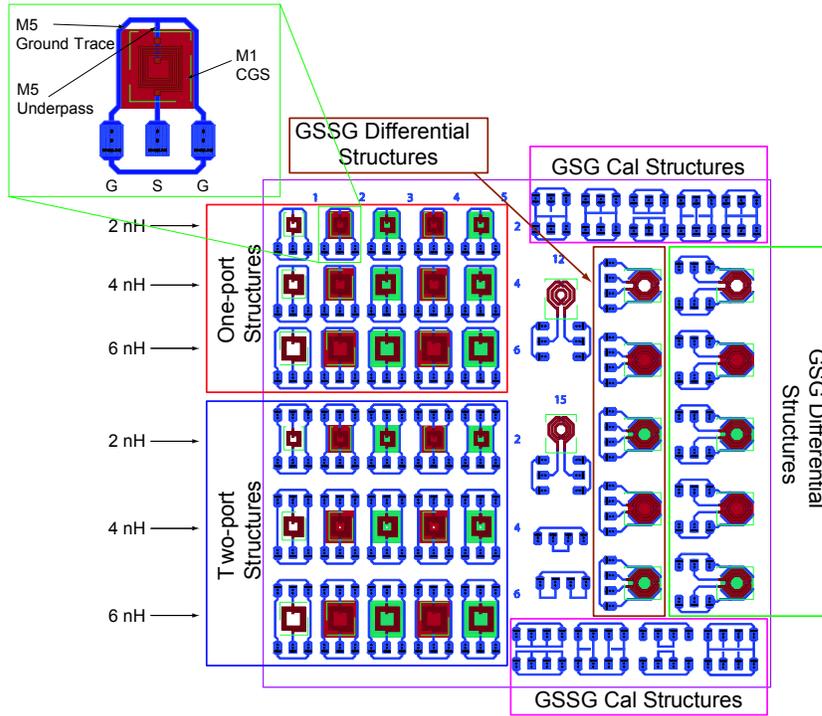


Figure 7.5: Layout of the  $5\text{ mm} \times 5\text{ mm}$  reticle of inductor structures in the HIP6WRF technology for the experiments in this chapter. Both one-port and two-port test configurations of rectangular inductors are included, with inductance values of 2 nH, 4 nH, and 6 nH (left-side). A fixed-value differential, symmetric inductor with the various ground shields is also included. Inset: a closer view of the one-port shielded inductor structure.

metal-five (M5) trace that wraps around the sides of the inductor to the two ground pads, as shown in the inset of Figure 7.5.

The differential symmetric inductors (such as those used in the QVCO of Chapter 6) and pad de-embedding structures are implemented on the right-hand half of the reticle. Normally, GSSG pad configurations can be used for the measurement of the differential structures. However, the GSSG probe configuration is not a balanced, coplanar structure — i.e. the two signal traces lie next to each other without an intermediate ground plane (as would be the case in, for example, a GSGSG probe). The lack of a ground plane between the signal traces means less shielding between the signal probes, which in turn leads to crosstalk problems, and less control of the CPW wave propagation, which increases substrate coupling and limits the high frequency response [279]. Consequently, measured results above 18 GHz are generally

not reliable [280]; therefore, inductors with GSG pad configurations at each port were also included to enable the measurement of the inductors up to frequencies of at least 20 GHz.

Calibration structures are required to de-embed the measured results of the inductors from the parasitics of the pads [281]. The inductor reticle includes both GSG and GSSG pad configurations connected to open, short, and “thru” structures; the availability of all three types of structures allowed for the exploration of different de-embedding schemes, which are discussed in more detail below.

### 7.2.1 Fabrication and Test Setup

The inductor test-chip layout shown in Figure 7.5 was submitted to Freescale Semiconductor for integration into an overall HIP6WRF 0.18  $\mu\text{m}$  SiGe:C RF BiCMOS engineering mask-set database. Five samples from the returned lot of manufactured parts were chosen for the experiment, which allowed (small) process variations over different wafers to be averaged out. The die were epoxied to brass wafer-carriers at M/A-COM, Inc. Roanoke, VA to facilitate on-wafer probe measurements. Figure 7.6 shows a photograph of the fabricated 5 mm  $\times$  5 mm reticle.

The  $s$ -parameters of the inductor and calibration structures were measured from 50 MHz to 20 GHz (to ensure resolution of the inductor self-resonant frequency) using both the HP8510C and the Agilent 8364B network analyzers<sup>1</sup>. The measured data was post-processed with a Matlab script [282] to de-embed the pad effects and calculate the effective inductance and quality factor for each inductor; these calculations were also completed in ADS2003C [283], which uses different data storage elements that simplify the mathematical manipulation of the data, as a check of the Matlab code. Measurements were taken for all five reticle samples and the results were averaged together during post-processing. Figure 7.7 shows a photograph of a one-port inductor under test with the GSG RF probe in contact.

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<sup>1</sup>The two network analyzers are interchangeable for the purposes of measuring the one- or two-port  $s$ -parameters of the inductors.

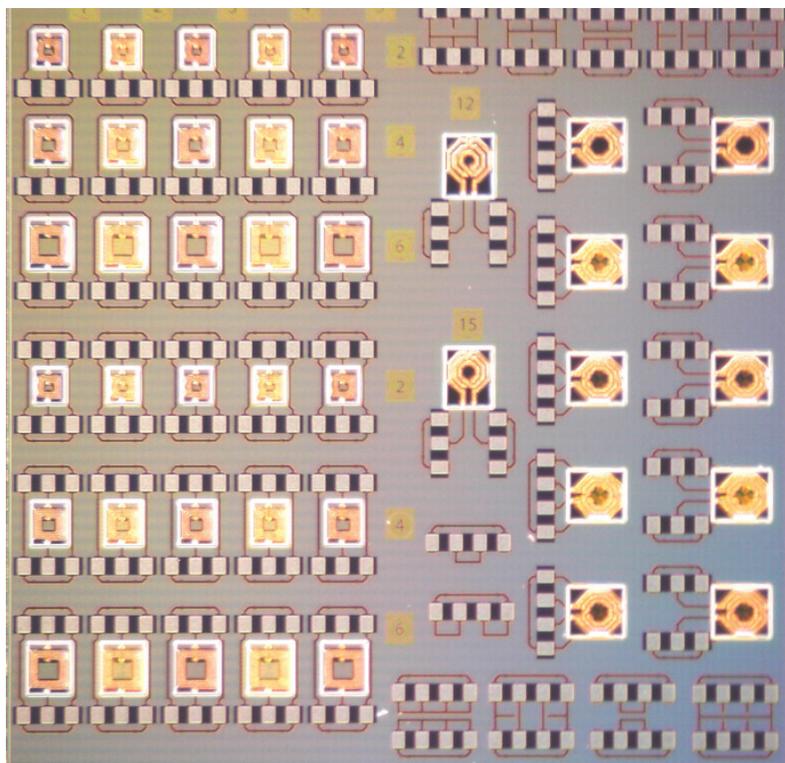


Figure 7.6: Photograph of the fabricated 5 mm × 5 mm reticle based on the layout in Figure 7.5. The reticle incorporates various types and sizes of inductors with different patterned ground shields.

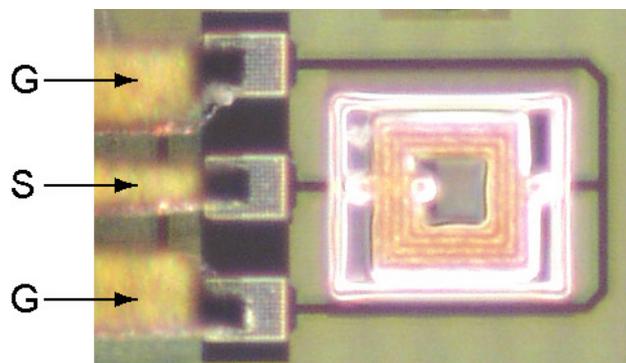


Figure 7.7: Photograph of the PLY PGS inductor being measured using a GSG RF-probe.

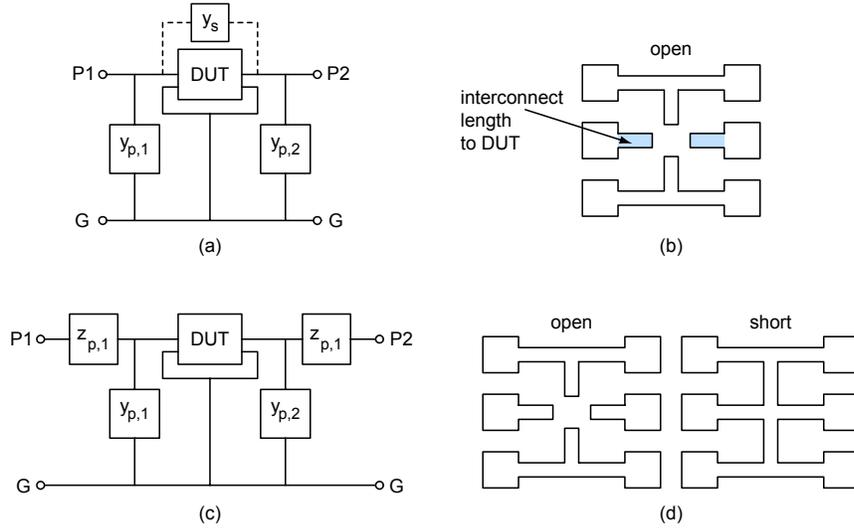


Figure 7.8: GSG calibration structures used in de-embedding process: (a) the shunt impedance of the pads ( $y_p$ ) can be eliminated using (b) the open pads; both the series impedance ( $z_p$ ) and the shunt impedance ( $y_p$ ) of the pads, shown in (c), can be eliminated using (d) the open and short pads (after [279]).

## Pad De-embedding

The parasitic effects of the RF probe pads are significant and must be removed from the measurements to realize an accurate representation of the inductor alone. Several techniques have been proposed for modeling the probe pads and de-embedding them from the DUT [279, 284–287]. The simplest model, shown Figure 7.8(a), treats the effect of the pads as shunt impedances to ground ( $y_{p,1}$  and  $y_{p,2}$ ) and uses a simple “open” pad structure [Figure 7.8(b)] to de-embed the DUT from the pads. The series impedance of the interconnect between the probe pads and the ports of the inductor, which is represented as  $y_s$  in the model, can also be de-embedded from the two-port measurements by including the same length of interconnect in the open structure, as shown in Figure 7.8(b) [279]. The two-port measurements presented in Section 7.2.3 make use of this approach.

For the symmetric differential inductors, the inductor designs were based on the work in [208]. Unfortunately, the inductor performed rather poorly using the GSG probe configuration, where an unrealistically low peak- $Q$  of  $\sim 3$  was measured. It is believed that the GSG pads for Port 1 were too close to the GSG pads of Port 2, which

allowed the high-frequency signals to couple between the probe-tips and corrupt the measurement. Attempts to measure the symmetric inductors using the GSSG probes were made, but an acceptable calibration of the VNA up to the probe-tips could not be achieved. Therefore, the measured results for the differential symmetric inductors are not included in this work.

## 7.2.2 One-Port Measurements

For the one-port measurements, the pad structures were de-embedded by subtracting the  $y_{11}$  of the open calibration-structure from the  $y_{11}$  of the inductor, thereby removing the shunt capacitance of the pads and providing the input  $y$ -parameter of the DUT ( $y_{11,DUT}$ ). The single-ended effective inductance ( $L_{eff}$ ) of each inductor was calculated from the de-embedded  $y_{11,DUT}$  according to [112]:

$$L_{eff} = \frac{\text{Im}\left(\frac{1}{y_{11,DUT}}\right)}{2\pi f} \quad (7.8)$$

and the overall  $Q$  was calculated using the real and imaginary parts of  $y_{11,DUT}$  as:

$$Q = \frac{\text{Im}\left(\frac{1}{y_{11,DUT}}\right)}{\text{Re}\left(\frac{1}{y_{11,DUT}}\right)}. \quad (7.9)$$

The self-resonant frequency was determined by plotting  $L_{eff}$  versus frequency and noting the point at which the effective-inductance crosses through zero and the reactance becomes capacitive.

Figure 7.9 shows the effective inductance and overall  $Q$  (up to the  $f_{SR}$ ) of the five 2 nH one-port inductors. The measured effective inductance of  $\sim 2.1$  nH was very close to the expected 2 nH value from the design kit. For the perimeter-grounded (PG) and center-grounded (CG) polysilicon shields, the peak- $Q$  was approximately 12.1 at a frequency of 5.4 GHz; compared to the  $Q$  of the unshielded PCELL (10.4 at 3.9 GHz), the PLY shields offered a 16% improvement in peak- $Q$ . However, the PLY shields also reduced the  $f_{SR}$  of the inductor by  $\sim 24\%$ , relative to the 20.9 GHz  $f_{SR}$  of the unshielded PCELL.

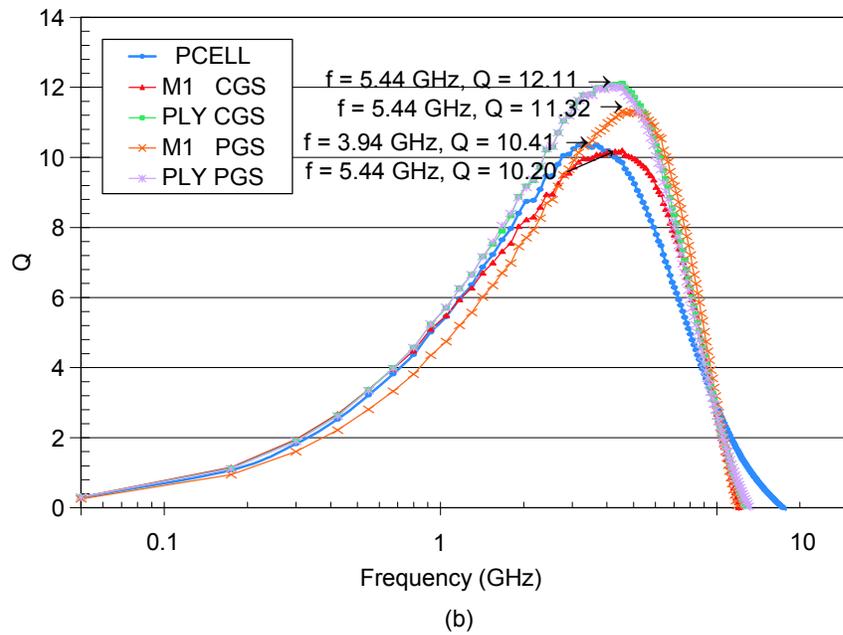
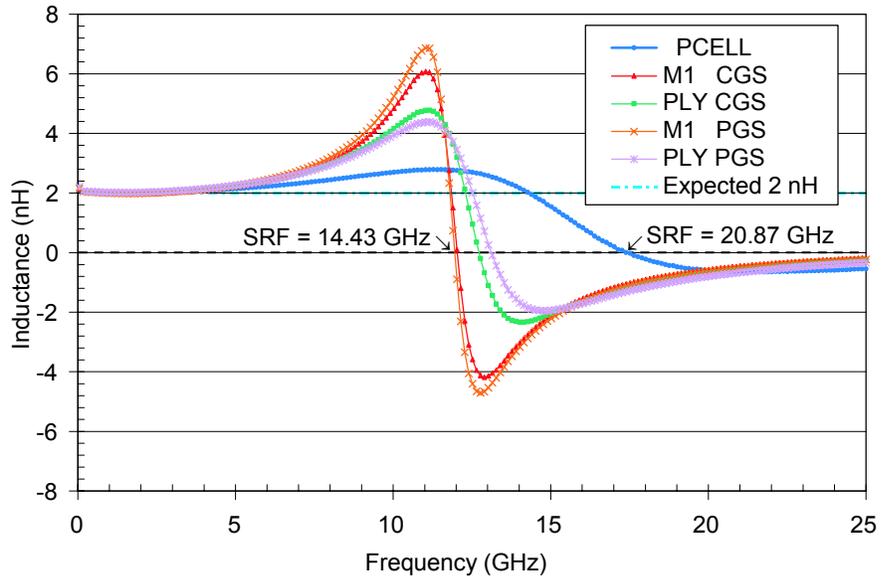
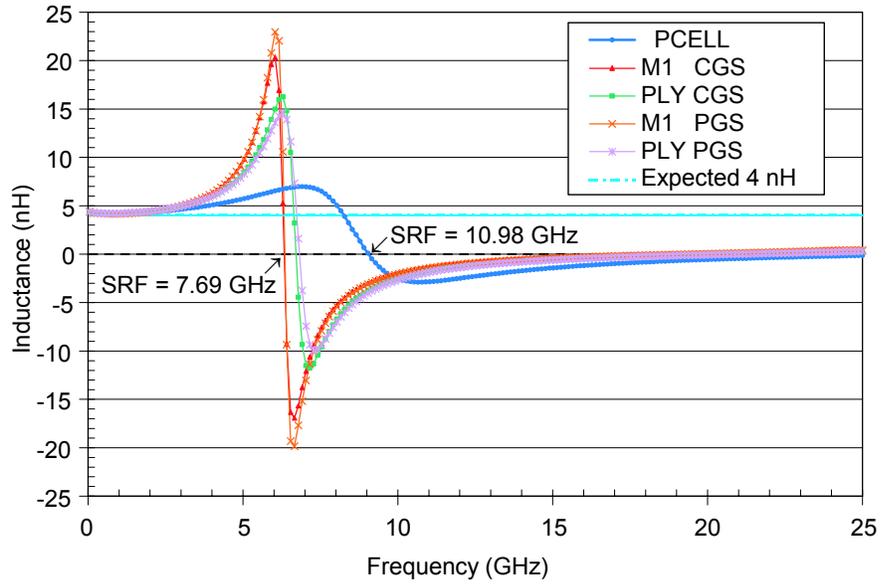


Figure 7.9: One-port measurement of the 2 nH inductor: (a) effective inductance; (b) overall quality factor.

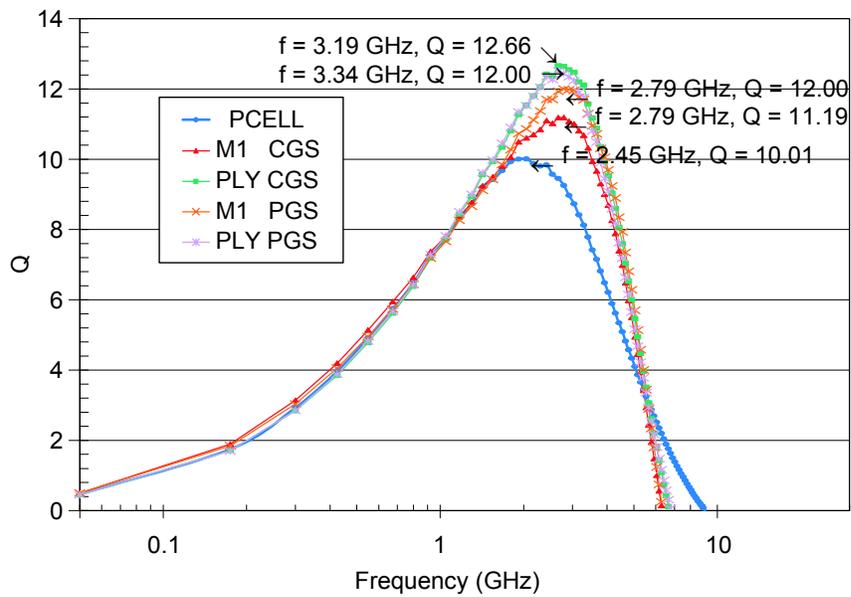
The metal-one shields were expected to have a greater impact on the  $f_{SR}$  compared to the polysilicon shields since the M1 layer is closer to the “bump” metal (used for the spiral) in the interconnect layer stack, which in turn should increase the shunt capacitance of the inductor and, thus, lower the  $f_{SR}$ . For the PG shield in metal-one, the increase in peak- $Q$  over the unshielded PCELL was only 9% (peaking at 3.9 GHz) while the  $f_{SR}$  was indeed lower, by 31%. The CGS in metal-one actually lowered the  $Q$  for the 2 nH inductor, which is the manifestation of Equation 7.6, since the large shunt capacitance between the inductor and M1 reduces the energy stored within the magnetic field of the inductor, thereby lowering the  $Q$ .

For the 4 nH inductor, the measured effective inductance [Figure 7.10(a)] of 4.2 nH from DC up to roughly 4.5 GHz was sufficiently close to the design value of 4.1 nH. As was the case with the 2 nH inductor, the PLY CGS and PGS outperformed their M1 counterparts and improved the  $Q$  [shown in Figure 7.10(b)], relative to the unshielded PCELL ( $Q = 10.4$ ,  $f_{SR} = 11$  GHz), by 27% (12.7 at 3.2 GHz); again, the downside was a 25% decrease in  $f_{SR}$ . The M1 PGS inductor exhibited a 20% improvement in peak  $Q$  (12 at 3.3 GHz), but had a  $f_{SR}$  that was 28% lower than the unshielded PCELL. The peak- $Q$  of the M1 CGS inductor was only 12% better than the peak- $Q$  of the unshielded PCELL with the same shift in  $f_{SR}$  as the M1 PGS inductor.

The lower frequencies of the peak- $Q$  and  $f_{SR}$  for the 4 nH inductors, compared to the 2 nH inductors, were due to the larger size of the 4 nH spiral, which has a greater area and experiences a larger shunt capacitance between the coil and the underlying substrate. In the case of the 6 nH inductor, the frequencies of the peak- $Q$  and  $f_{SR}$  were further shifted to down due to the even larger surface area, at  $\sim 2.6$  GHz and  $\sim 6$  GHz, respectively. Nevertheless, the measured effective inductance [Figure 7.11(a)] was 6.3 nH, which agrees with the designed value of 6.2 nH. Compared to the peak- $Q$  of the unshielded PCELL, which was 9.8 at a frequency of 1.7 GHz, the peak- $Q$  of the PLY CGS inductor exhibited the greatest increase at 12.4 (26% improvement); the  $f_{SR}$  was reduced by 27% compared to the unshielded PCELL inductor  $f_{SR}$  of 8 GHz. The PLY PGS inductor had a peak- $Q$  of 11.8 (20% improvement) and the same reduction in  $f_{SR}$ . The M1 shields on the other hand showed a more modest improvement in the quality factor, with peak- $Q$ s of 11.4 (16.2% increase) and 10.8 (10% increase) for the PG and CG shields, respectively, and caused a greater shift (30%) in  $f_{SR}$ .

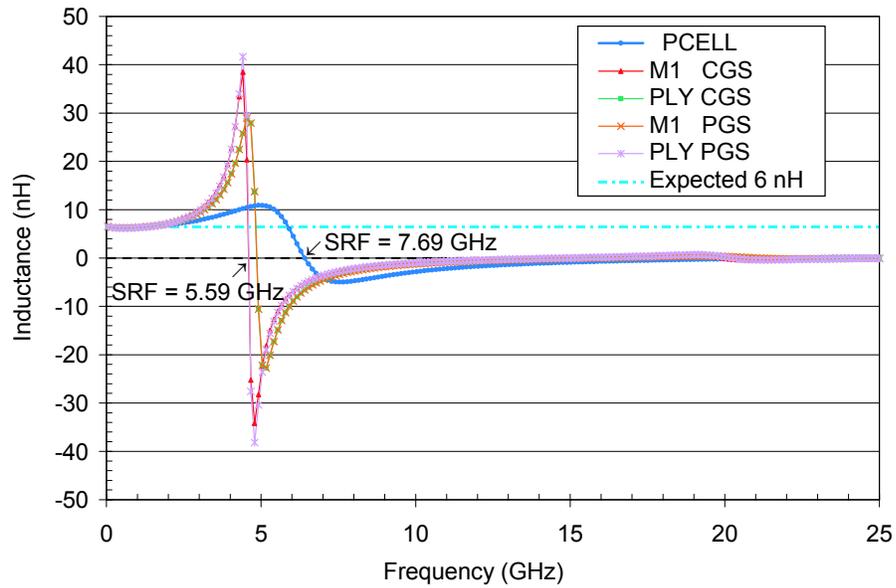


(a)

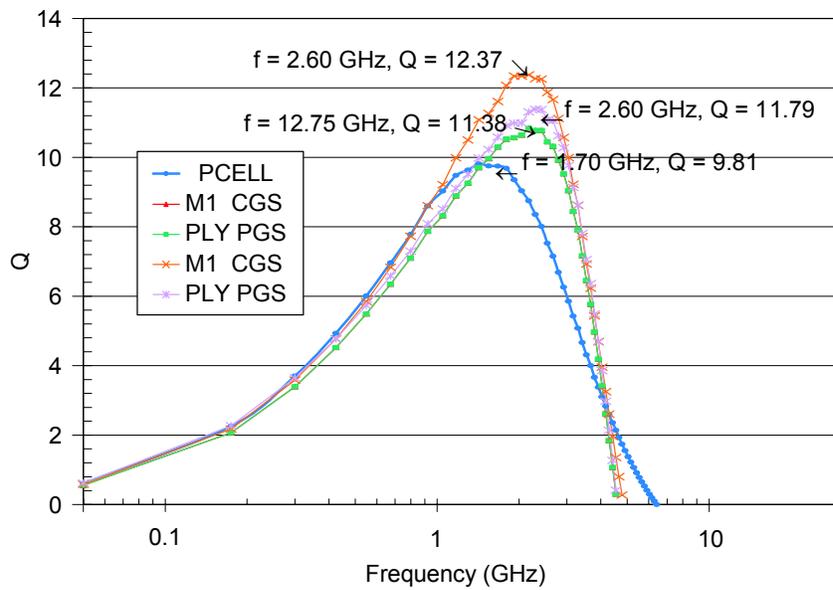


(b)

Figure 7.10: One-port measurement of the 4 nH inductor: (a) effective inductance; (b) overall quality factor.



(a)



(b)

Figure 7.11: One-port measurement of the 6 nH inductor: (a) effective inductance; (b) overall quality factor.

The one-port measurements are useful for applications where one port of the inductor is tied to AC ground, such as emitter degeneration or load inductors. However, for applications where the inductor is in series with the signal path, such as the input of an LNA, or in a differential application such as a VCO tank, two-port inductors are required.

### 7.2.3 Two-Port Measurements

As discussed in Section 7.2.1, the two-port DUT  $y$ -parameters were extracted from the measured two-port data of the inductor ( $Y_{ij,meas}$ ) and the “open” calibration structure ( $Y_{ij,open}$ ). The open-data was adjusted to fit the model of Figure 7.8(b) using [279]:

$$\begin{aligned} Y_s &= -Y_{12,open} \\ Y_{p,1} &= Y_{11,open} + Y_{12,open} \\ Y_{p,2} &= Y_{12,open} - Y_{22,open}. \end{aligned} \tag{7.10}$$

Given these parameters, which represent the shunt impedance of the pads and the series impedance of the interconnects leading up to the inductors (as mentioned in Section 7.2.1), the  $y$ -parameters for the DUT ( $Y_{ij,DUT}$ ) were calculated from:

$$\begin{aligned} Y_{11,DUT} &= Y_{11,meas} - Y_{p,1} \\ Y_{22,DUT} &= Y_{22,meas} - Y_{p,2} \\ Y_{12,DUT} &= Y_{12,meas} - Y_s \\ Y_{21,DUT} &= Y_{21,meas} - Y_s \end{aligned} \tag{7.11}$$

Since the impedance of the inductor is floating (neither port is tied to AC ground), the quality factor and effective inductance of the two-port inductors were calculated using the impedance of the inductor ( $R + jX$ ) as determined from these extracted

$y$ -parameters [112]:

$$\begin{aligned} R + jX &= \left( -\frac{1}{Y_{12,DUT}} \right) \parallel \left( \frac{1}{Y_{11,DUT} + Y_{12,DUT}} + \frac{1}{Y_{22,DUT} + Y_{12,DUT}} \right) \\ &= \frac{Y_{11,DUT} + Y_{22,DUT} + 2Y_{12,DUT}}{Y_{11,DUT}Y_{22,DUT} - Y_{12,DUT}^2}. \end{aligned} \quad (7.12)$$

The effective inductance is found from

$$L_{eff} = \frac{X}{2\pi f} \quad (7.13)$$

and the  $Q$  is found from

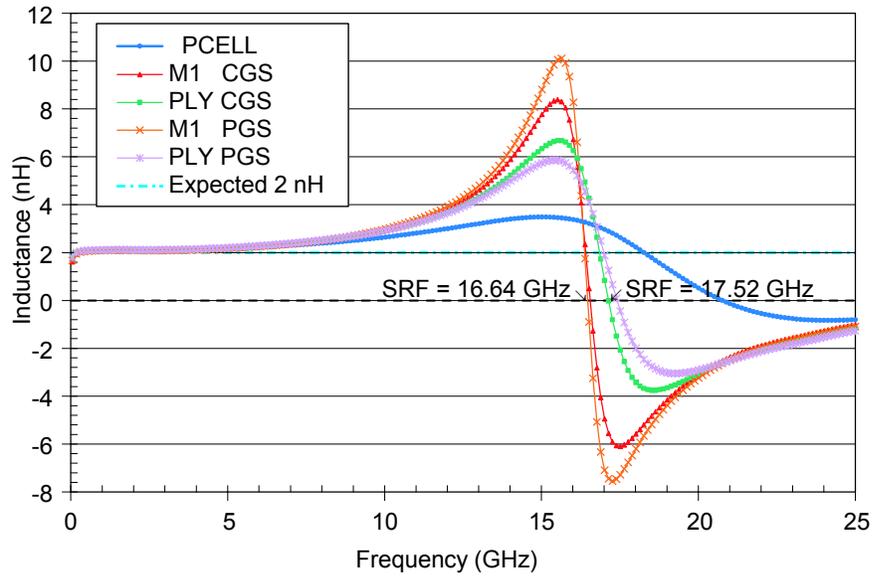
$$Q = \frac{X}{R}. \quad (7.14)$$

As with the one-port measurements, all five reticles of two-port inductors were measured and the results were averaged together before the DUT  $y$ -parameter extraction.

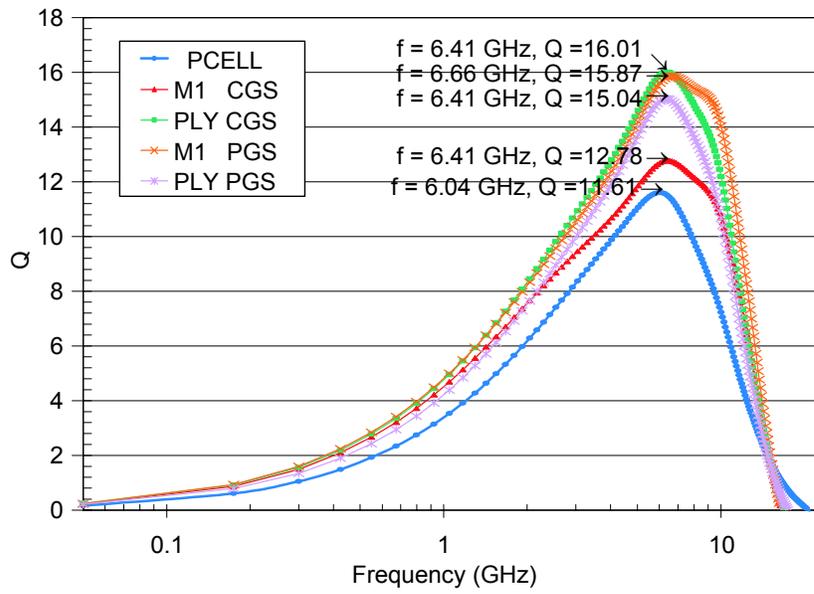
Figure 7.12 shows the effective inductance and the quality factor of the measured two-port 2 nH inductors. As was the case with the one-port inductors, the PLY CGS provided the largest increase in peak- $Q$  (16 at 6.4 GHz) with a 38% improvement over the the unshielded PCELL ( $Q = 11.6$ ,  $f_{SR} = 20.9$  GHz). Unlike the one-port inductors however, the M1 PGS shield performed almost as well with a 37% increase in peak- $Q$  (15.9 at 6.7 GHz). The reductions in  $f_{SR}$  relative to the unshielded PCELL for the PLY CGS and M1 PGS were 16% and 20%, respectively. Meanwhile, the PLY PGS improved the peak- $Q$  (15 at 6.4 GHz) by 29% with a decrease in  $f_{SR}$  of 18%, and the M1 CGS exhibited a 10% increase in peak- $Q$  and a 20% reduction in  $f_{SR}$ .

For the two-port, 4 nH inductors (Figure 7.13), the PLY PGS ( $Q = 18.9$ ,  $f_{SR} = 9.9$  GHz) and PLY CGS ( $Q = 18.1$ ,  $f_{SR} = 9.8$  GHz) showed the largest increase in peak- $Q$ , with 50% and 43% over the peak- $Q$  of the unshielded PCELL ( $Q = 12.7$ ,  $f_{SR} = 11.5$  GHz), respectively; the decline in  $f_{SR}$  was roughly the same for each at  $\sim 15\%$ . The peak- $Q$  for the M1 PGS inductor was 17, or 34% higher than the unshielded inductor while the  $f_{SR}$  was reduced by 16%. The M1 CGS inductor had a peak- $Q$  of 13.9 (10% increase) with a 16% decrease in  $f_{SR}$ .

The measured results for the 6 nH inductor (Figure 7.14) are similar to those for the 4 nH. The PLY PGS ( $Q = 21.1$ ,  $f_{SR} = 7.5$  GHz) and CGS ( $Q = 20.7$ ,  $f_{SR} =$

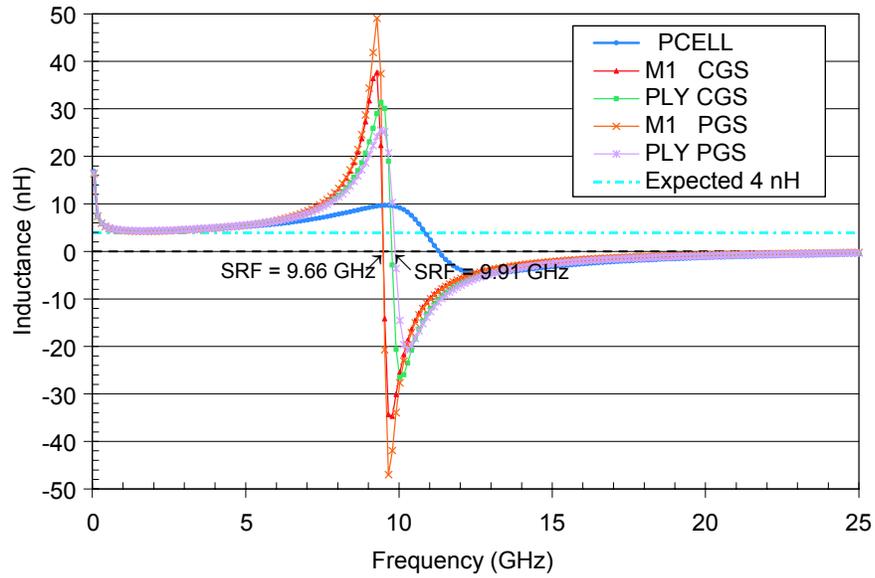


(a)

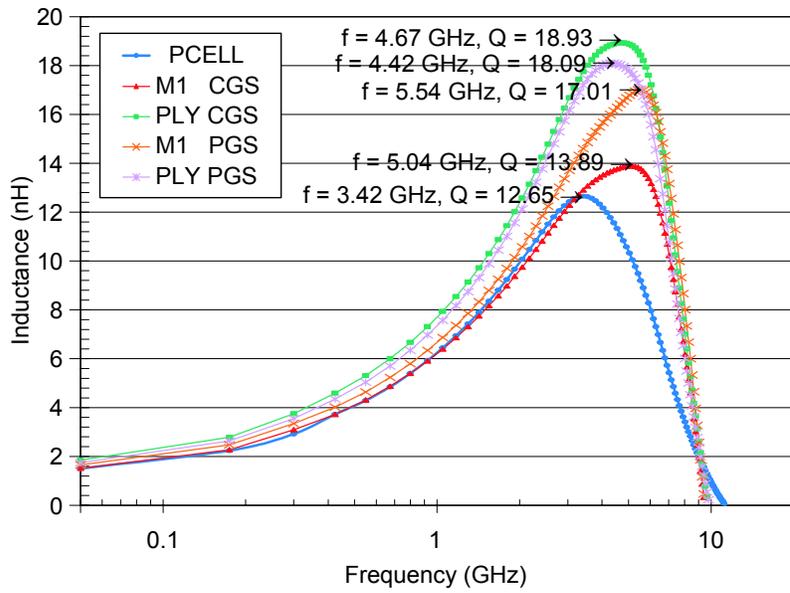


(b)

Figure 7.12: Two-port measurement of the 2 nH inductor: (a) effective inductance; (b) overall quality factor.



(a)



(b)

Figure 7.13: Two-port measurement of the 4 nH inductor: (a) effective inductance; (b) overall quality factor.

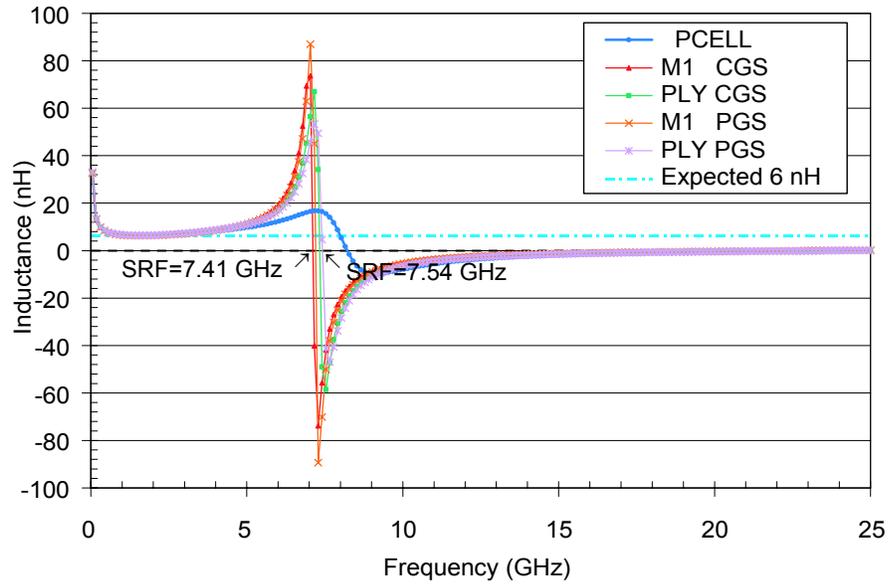
7.4 GHz) provided nearly the same improvement in peak- $Q$  over that of the unshielded PCELL ( $Q = 14.0$ ,  $f_{SR} = 8.4$  GHz), with increases of 51% and 48%, respectively; the corresponding decrease in  $f_{SR}$  for both was 11%. The M1 shields exhibited similar increases in peak- $Q$  with  $Q$ s of 17.0 and 16.3 for the PG and CG shields, respectively; the reduction in  $f_{SR}$  was 12% for both M1 shields.

From both the one-port and two-port measured results, the shields implemented in polysilicon — with either type of ground connection — provide the largest improvement in  $Q$  while having the lowest impact on the  $f_{SR}$  when compared to the shields implemented in M1. Although the PG shield reportedly exhibits a strong loop current that negatively affects the effective inductance and peak- $Q$  of the inductor [277], a significant difference between the PG and CG shields was not apparent for either the M1 or PLY shields from the measured results of this experimental effort.

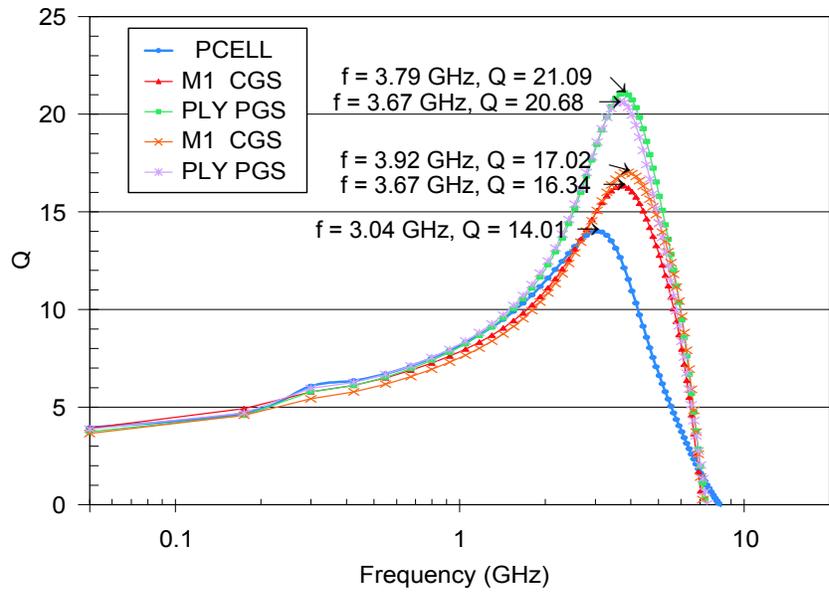
The large difference in peak- $Q$  *improvement* between the one-port ( $\sim 20\%$ ) and two-port ( $\sim 50\%$ ) measurements of inductors with polysilicon shields can be explained as follows. Since the shield effectively moves the ground-plane of the inductors closer to the coil structure, the shunt capacitances, which can be modeled as lumped element capacitors at the input and output ports of the two-port inductor, are significantly increased. In the one-port case [Figure 7.15(a)], only one of the shunt capacitances is seen by the measurement system; in the two-port case [Figure 7.15(b)], the two capacitances are seen in series and the net shunt capacitance is effectively halved. This lower capacitance reduces the energy coupling and loss of the two-port inductor, which in turn improves its peak- $Q$  compared to the one-port case. Differences in peak- $Q$  between one-port and two-port inductor measurements have been reported in the literature on the order of roughly 3–5% for unshielded inductors [112]; however, the ground-planes for these inductors are farther away from the coil structure and thus, the relative decrease in shunt capacitance is less dramatic.

### 7.3 Scalable Lumped-Element Models

Inductor models that accurately represent the effective inductance and  $Q$  versus frequency are critical for the design of a number of RF circuits, such as VCOs, LNAs, and PAs. Within manufacturer design kits, which provide CAD models for the active



(a)



(b)

Figure 7.14: Two-port measurement of the 6 nH inductor: (a) effective inductance; (b) overall quality factor.

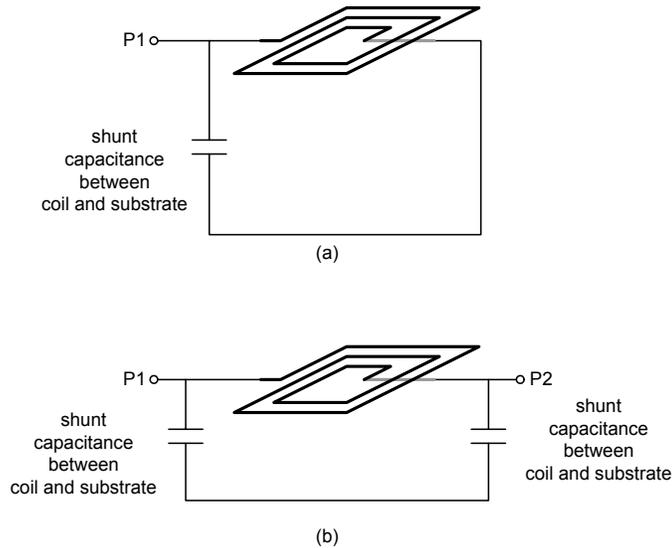


Figure 7.15: Shunt parasitic capacitance in the case of (a) a one-port measurement; (b) a two-port measurement. In the two-port case, shunt capacitances at both the input and output ports of the inductor are effectively in series, which reduces their overall effect on the peak- $Q$ .

and passive components of a given semiconductor technology, such models should give a good prediction of performance over a range of inductor values. However, since circuit performance (e.g. VCO phase noise and oscillation frequency) is often affected directly by the performance of the inductor, designers have typically relied on supplementary EM simulations of the coil structure to provide a more accurate prediction of the inductor parameters. The downside of this approach is that it requires significant amounts of CPU time for EM simulations of even a simple inductor to be completed (although significant work continues on the reduction of simulation times [288]). Furthermore, the simulation results are unique to each specific structure and small changes to the dimensions or the layout of the spiral — such as an increase of the coil inner-diameter — require re-simulation.

The computational requirements of EM simulations are significantly increased with the addition of patterned ground shields since the patterning structure adds much greater geometrical complexity. Therefore, a *scalable*, lumped-element model that can account for the presence (or lack of) a patterned ground shield is highly desirable. Given such a model, designers can rapidly evaluate the effects of different geometries on an inductor's  $f_{SR}$ ,  $Q$ , and  $L_{eff}$  and their subsequent impact on circuit performance

without resorting to time consuming EM simulation iterations. Furthermore, lumped element models can straightforwardly be integrated into a CAD environment and do not require special simulation components, such as  $N$ -ports<sup>2</sup>. The next section presents an overview of the standard model for integrated inductors and equations for calculating the different model parameters. An extension of that model is proposed in the following section to include the effects of the patterned ground shields. A comparison of the modeled and measured results is presented to validate the model.

### 7.3.1 Standard Two-Port Model

Figure 7.16(a) shows the standard two-port lumped-element model of an unshielded, integrated inductor on Si substrates [289]. The model accounts for the losses of the conductor with the series resistance,  $R_s(f)$ , which is frequency-dependent to account for high-frequency skin effect. The capacitor  $C_f$  represents the capacitance between each turn of the coil metal ( $n$ ) and the lower-metal underpass;  $C_f$  can also be used to include the fringing capacitance that can occur between the inter-windings of the coil [270]. The parallel-plate capacitance between the coil and the substrate is represented with  $C_{ox\_in}$  and  $C_{ox\_out}$ ; since the underpass that connects to the center of the inductor lies in a lower metal layer (which is closer to the substrate than the metal layer of coil), the inductor structure is not necessarily symmetric. The substrate parameters  $C_{sub}$  and  $R_{sub}$  represent the losses within the substrate due to the energy coupling of the electric field through  $C_{ox}$ . These values can also be broken up in terms of the input and output ports of the model ( $R_{sub\_in}$ ,  $C_{sub\_in}$ ) and ( $R_{sub\_out}$ ,  $C_{sub\_out}$ ) to account for imbalances within the structure. The value of  $L$  is modeled as a constant (since high-frequency conductor losses, such as skin effect, do not change the magnetic flux external to the conductor [289]) and can be calculated using either the Greenhouse method [290], or Wheeler's approximation [291]:

$$L \approx \frac{37.5\mu_0 n^2 a^2}{22r - 14a}, \quad (7.15)$$

where  $\mu_0$  is the magnetic permeability of free space,  $n$  is the number of turns,  $a$  is the mean radius of the spiral (defined as the distance from the center of the inductor to

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<sup>2</sup> $N$ -ports are used to import the  $s$ -parameter data of a circuit component (e.g. an inductor) into a CAD schematic for subsequent simulation.

the middle of the windings), and  $2r$  is the length of one side of the coil (Figure 7.17); with both  $a$  and  $r$  expressed in microns, the resulting  $L$  is in nanohenries [58].

Figure 7.16(b) shows a modified version of the two-port lumped-element model for the unshielded inductor [245]. This version, which is an extension of the ideal transformer version proposed in [292], features a secondary inductor ( $L_{sub}$ ) and a parallel resistor ( $R_{sub}$ ) to represent the energy lost through the penetration of the magnetic field into a lossy substrate. The model also includes the finite resistance of substrate contacts, which are typically spread around the inductor to fix the substrate to ground potential, with the addition of the resistor  $R_{cont}$  [245].

The secondary inductor ( $L_{sub}$ ) and the main inductor ( $L$ ) of the modified model are coupled through their mutual inductance ( $M_{sub}$ ) such that the current induced in the  $L_{sub}$ - $R_{sub}$  loop results in a magnetic field that opposes the field of the main inductor. Neglecting the components related to the electric-field losses, as in Figure 7.18, and treating the substrate impedance seen by the magnetic field ( $Z_{sub,mag}$ ) as a simple resistor ( $R_{sub,mag}$ ), the  $Z_{in}$  of the model with only magnetic losses is

$$Z_{in} = \frac{\bar{V}_i}{\bar{I}_1} = (R_s + j\omega L) + \frac{\omega^2 M_{sub}^2}{R_{sub,mag} + j\omega L_{sub}} \quad (7.16)$$

where the first term is simply the impedance of the series combination of  $R_s(f)$  and  $L$  and the second term represents the coupled impedance of the  $L_{sub}$ - $R_{sub}$  loop (which is denoted as  $Z_r$ ). In the equation, the impedance of the substrate loop is reflected back into the series combination of  $R_s(f)$  and  $L$  and tends to decrease the effective inductance (since the imaginary part of  $Z_r$  is negative) and increase the overall loss (since the real part of  $Z_r$  is positive and adds directly to  $R_s$ ). Thus, by combining both the magnetic and electric field losses, the lumped-element circuit of Figure 7.16(b) provides a reasonable accurate model of on-chip inductor performance.

For the inductors fabricated in this experiment, the model in Figure 7.16(b) is used to represent the inductors without patterned ground shields. A scalable model for the inductors *with* patterned ground shields was developed from this initial representation, as described in the next section. Table 7.2 gives a summary of the equations used for calculating the component values of the model for the two-port unshielded inductors that were measured above. The width ( $w$ ) and end-to-end length ( $l$ ) of the spiral trace are the main variables for each parameter while the other values are de-

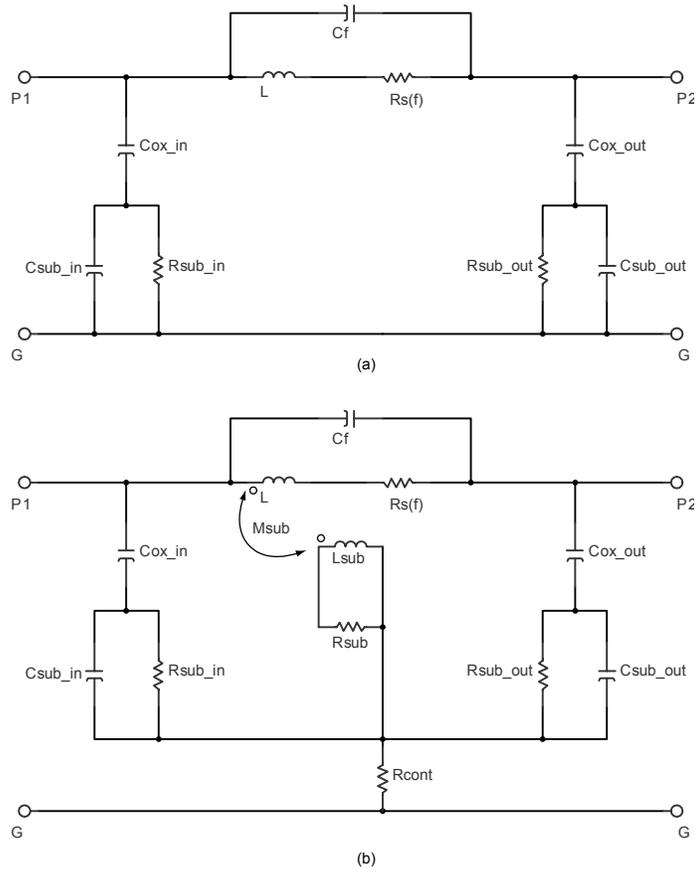


Figure 7.16: Two-port lumped-element models for the integrated inductor. (a) Traditional version, where  $R_s(f)$  represents the frequency-dependent losses of the conductor;  $C_f$  is the capacitance between the coil and the underpass and can include any capacitance between the windings of the coil;  $C_{ox\_in}$  and  $C_{ox\_out}$  represent the oxide capacitance between the coil and the substrate; and  $C_{sub}$  and  $R_{sub}$  represent the losses within the substrate where coupled energy through the electric field is dissipated. (b) Modified version, where a mutual inductance component ( $M_{sub}$ ) is added to represent the coupling of energy via the magnetic field to the lossy substrate ( $R_{sub}$ ). The resistance of the substrate contacts, which tie the substrate to ground, is also added with  $R_{cont}$ .

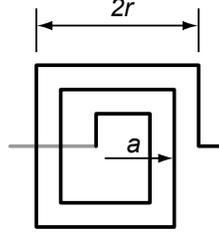


Figure 7.17: Dimension of the inductor (in microns) used in the calculation of the effective inductance for the model.

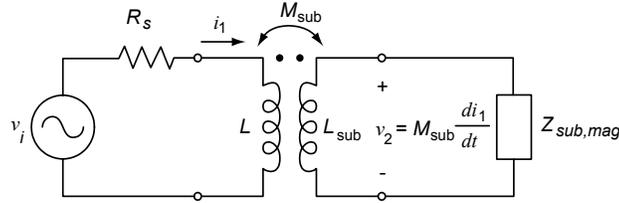


Figure 7.18: The mutual coupling between the main inductor ( $L$ ) and the secondary inductor ( $L_{sub}$ ) lowers the effective inductance and increases the resistance.

terminated by the IC technology, such as the permittivities of the oxide and inter-layer dielectrics (which are combined in a weighted average,  $\varepsilon_{ox}$ ), the combined thickness of those layers ( $t_{ox}$ ), the metal conductivity of the spiral trace ( $\sigma$ ), and the skin depth ( $\delta$ ), which is calculated as

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}}. \quad (7.17)$$

The substrate parameters  $G_{sub\_in}$ ,  $G_{sub\_out}$ ,  $C_{sub\_in}$ , and  $C_{sub\_out}$  are typically calculated using separate fitting parameters (which are denoted as  $G_1$ ,  $G_2$ ,  $C_1$ , and  $C_2$ , respectively) that are unique to the given substrate and therefore determined empirically. For the low-resistivity substrates found in modern CMOS processes, typical values for  $G_1$  and  $G_2$  are  $\sim 10^{-7} \text{ S} / \mu\text{m}^2$  and for  $C_1$  and  $C_2 \sim 10^{-2} \text{ fF} / \mu\text{m}^2$  [58]. However, to simplify the model, these fitting parameters ( $G_1$ ,  $G_2$ ) and ( $C_1$ ,  $C_2$ ) are equated so that  $G_1 = G_2 = G_{fit}$  and  $C_1 = C_2 = C_{fit}$ ;  $G_{fit}$  and  $C_{fit}$  are then used to calculate the substrate parameters, which means that  $G_{sub\_in}$  is equal to  $G_{sub\_out}$  and  $C_{sub\_in}$  is equal to  $C_{sub\_out}$ . Since the effect of the underpass on the shunt capacitance  $C_{ox}$  is relatively small due to the inter-layer thicknesses, the model is further simplified by equating  $C_{ox\_in} = C_{ox\_out} = C_{ox}$ .

Table 7.2: Model parameters for the unshielded inductor lumped-element model.

$L, L_{sub}$	$C_f$	$C_{ox\_in}$	$C_{ox\_out}$
$\frac{37.5\mu_0 n^2 a^2}{22r-14a}$	$\frac{(n-1) \cdot w \cdot l \cdot \epsilon_{ox, BMP-M5}}{t_{ox, BMP-M5}}$	$\frac{w \cdot l \cdot \epsilon_{ox}}{t_{ox, BMP-sub}}$	$\frac{w \cdot l \cdot \epsilon_{ox}}{t_{ox, M5-sub}}$
$R_s(f)$		$C_{sub\_in},$ $C_{sub\_out}$	$R_{sub\_in},$ $R_{sub\_out}$
$\frac{l}{w\sigma\delta(1.3-e^{-t/\delta})}$		$\frac{w \cdot l \cdot G_{fit}}{2}$	$\frac{2}{(w \cdot l \cdot G_{fit})}$

Since the values for the mutual inductance ( $M_{sub}$ ) and that magnetic substrate loss ( $R_{sub}$ ) were not initially known, these values were determined by fitting the model to the measured data. The model and measured data were imported into ADS 2003C and the built-in optimization routine was used to match the performance. To simplify the process, the image inductor was assumed to be an equivalent but opposite coil to the the main inductor; thus, the image inductance ( $L_{sub}$ ) was set equal to the inductance ( $L$ ) of the spiral. Since the original equation for  $R_s(f)$  was based on the inductor being fabricated using a thin-film conductor, it did not necessarily hold for the  $10\ \mu\text{m}$  thick copper “bump” metal used for the spirals in this experiment; therefore, the factor of 1.3 in the calculation of  $R_s(f)$ , which adjusted the overall conductor loss, was also found using the ADS optimizer. Incidentally, for simulators that do not support frequency-dependent resistors (such as the Cadence Design System),  $R_s(f)$  can be replaced by an  $L$ - $R$  ladder network that adds incremental amounts of loss to the structure over various ranges of frequencies [272].

### 7.3.2 Proposed Model with Ground Shield

As mentioned above, the purpose of the ground shield is to prevent the electric-field of the coil from reaching the lossy substrate, and the purpose of the patterning is to prevent the flow of magnetic-field-induced image currents within the shield itself. From a modeling standpoint, the shield effectively eliminates the capacitive coupling of  $C_{ox}$  to the substrate ( $R_{sub}, C_{sub}$ ), but does not change the losses due to magnetic-coupling of energy to the substrate. Therefore, the traditional two-port inductor model in Figure 7.16(b) can be simplified for inductors with patterned ground shields by removing these shunt capacitive components altogether, as shown in Figure 7.19.

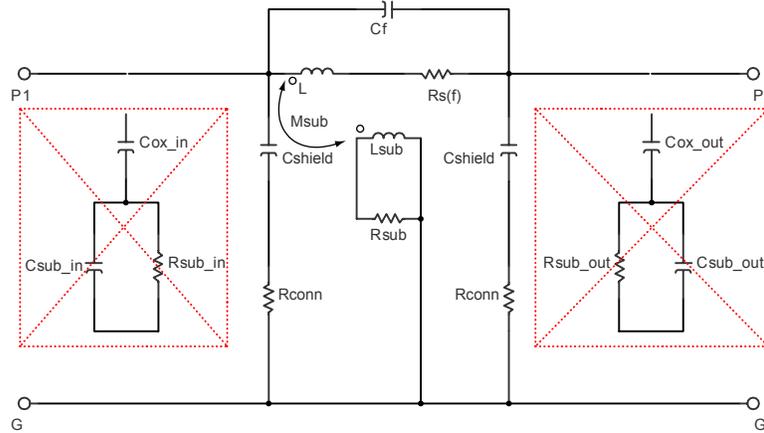


Figure 7.19: Proposed model for the pattern ground shield inductors. Since the shield reduces the electric-field coupling to the substrate, the shunt combinations of  $C_{ox}$  and the substrate parameters  $R_{sub}$ ,  $C_{sub}$  are removed. The additional capacitance between the spiral and the polysilicon or metal-one shield is represented with the new capacitor  $C_{shield}$ .  $R_{cont}$  now represents the resistance between the shield and ground that results from the via connection.

However, the inclusion of a shield results in a larger parallel-plate capacitance between the coil and the shield; this shunt capacitance is included in the model with the addition of  $C_{shield}$ . Furthermore, the distributed resistance of the shield and the connection of the shield to ground (which occurs with layers of vias that have a finite resistance) are approximated in the model with the shunt resistors,  $R_{conn}$ . A scaling factor ( $\alpha_{shield}$ ) is also introduced in the model to adjust the shunt capacitance of the shield, since neither the spiral nor the shield are actually continuous planes of metal. As a first order approximation, the model does not differentiate between the PG and CG shields.

For the smaller inductors in these experiments, the inner diameter of the coil was very tight, which results in a strong magnetic field at the center of the structure. This stronger field couples more energy from the inductor to the substrate and degrades the overall  $Q$ . When the inner diameter is increased, as in the case of the 4 nH and 6 nH inductors, the energy coupled to the substrate decreases since the magnetic field at the center of the structure is less concentrated. In the model, this effect is incorporated in the value of  $R_{sub}$ , which directly affects the inductor  $Q$  as seen in Equation 7.16. As the value of inductance increases, the value of  $R_{sub}$  decreases; si-

Table 7.3: Values for optimized model parameters  $M_{sub}$ ,  $R_{sub}$ , and  $\alpha_{shield}$ .

$M_{sub}$ (nH)				
Inductance (nH)	M1 CGS	PLY CGS	M1 PGS	PLY PGS
2	0.65	0.55	0.60	0.60
4	1.20	1.10	0.90	1.25
6	1.20	0.95	1.30	1.14

$R_{sub}$ (nH)				
Inductance (nH)	M1 CGS	PLY CGS	M1 PGS	PLY PGS
2	8.40	8.40	8.40	8.40
4	5.78	5.78	5.78	5.78
6	1.10	1.10	1.10	1.10

$\alpha_{shield}$				
Inductance (nH)	M1 CGS	PLY CGS	M1 PGS	PLY PGS
2	1.20	1.00	1.20	1.00
4	0.86	0.67	0.82	0.67
6	0.76	0.59	0.69	0.63

multaneously, the mutual inductance, which determines how much of  $R_{sub}$  is reflected into the impedance of the inductor, remains relatively flat across the different values of inductance. Although the value of  $M_{sub}$ ,  $R_{sub}$ , and the shield capacitance scaling factor ( $\alpha_{shield}$ ) can be optimized to help fit the model to the measured data and are not necessarily calculated, nearly linear trends can be observed from the resulting values (Figure 7.20). Therefore, values for these parameters can be interpolated for inductors in the 2 nH–6 nH range. Table 7.3 shows the extracted values of these model parameters for the pattern ground shield inductors.

The next section compares the measured data of the unshielded PCELL inductor with the unshielded model of Section 7.3.1 and the measured data of the shielded inductors with the modified model developed in this section.

### 7.3.3 Model Versus Measured Results

Figures 7.21(a)-7.21(e) show the two-port modeled and measured  $L_{eff}$  and  $Q$  plots for the five different 2 nH inductors. Figure 7.21(f) shows the percentage error of the

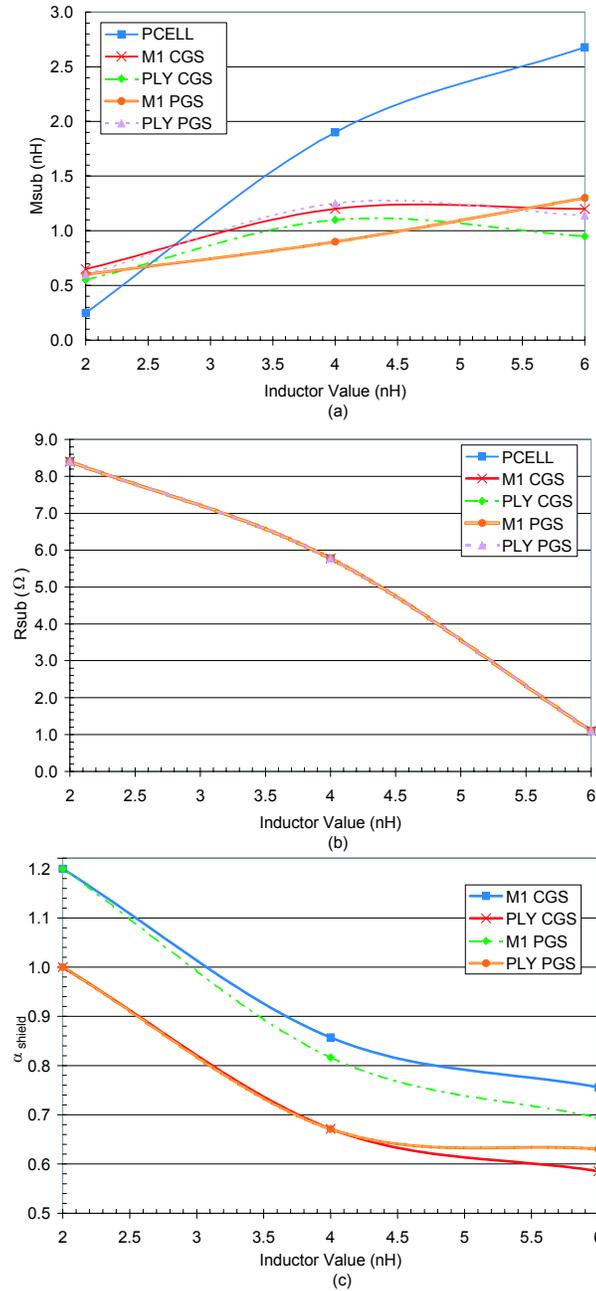


Figure 7.20: Plot of optimized model parameters versus inductance value: (a)  $M_{sub}$ ; (b)  $R_{sub}$ ; and (c)  $\alpha_{shield}$ .

model relative to the measured data. At low frequencies, where the series resistance of the coil dominates the frequency response, the model results are slightly higher than the measured results for all five inductors. However, due to de-embedding problems using the “short” calibration standard (Section 7.2.1), the series losses of the pads are not extracted from the measured results and these losses may account for the steep transition of the inductor  $Q$  at low frequencies.

For the ground-shield inductors at high frequencies, the model is very accurate, since the  $Q$  and  $L_{eff}$  are dominated by the shunt capacitance between the shield and the inductor. The strong match between the simplified model of Figure 7.19 (where the capacitances between the coil and substrate are removed) and the corresponding measured results indicate that the shields block the electric-field from reaching the substrate reasonably well as the overall loss of the structure is improved with the shield. The model provides less than 10% error from roughly the peak- $Q$  frequency to the  $f_{SR}$ . The model also accurately captures the effective inductance and the self-resonant frequency is within a few megahertz. For circuit applications in the  $4\text{ GHz} \lesssim f \lesssim f_{SR}$  range, the model is sufficient for a first-pass design, where the effects of adding a ground shield to various inductor components within a design can be determined very rapidly. Table 7.4 gives the values for the peak- $Q$ , the center frequency of the peak- $Q$  ( $f_c$ ), and the  $f_{SR}$  for the modeled and measured inductors for comparison.

## 7.4 Summary

This chapter presented the characterization and modeling of patterned ground shield inductors fabricated in the Freescale  $0.18\ \mu\text{m}$  SiGe:C RF BiCMOS process. Two different types of shields (the center grounded shield and the perimeter grounded shield) in two different types of materials (metal-one and polysilicon) were fabricated under inductors with values of 2, 4, and 6 nH in both one-port and two-port measurement configurations. The shields were incorporated under the inductors to prevent the electric field from coupling to the lossy silicon substrate by terminating the fields to ground, and the patterning of the shields prevented the magnetic field from inducing image currents within the shield material, which would dissipate energy through the sheet resistance of the shield material. Based on the two-port measurements, the

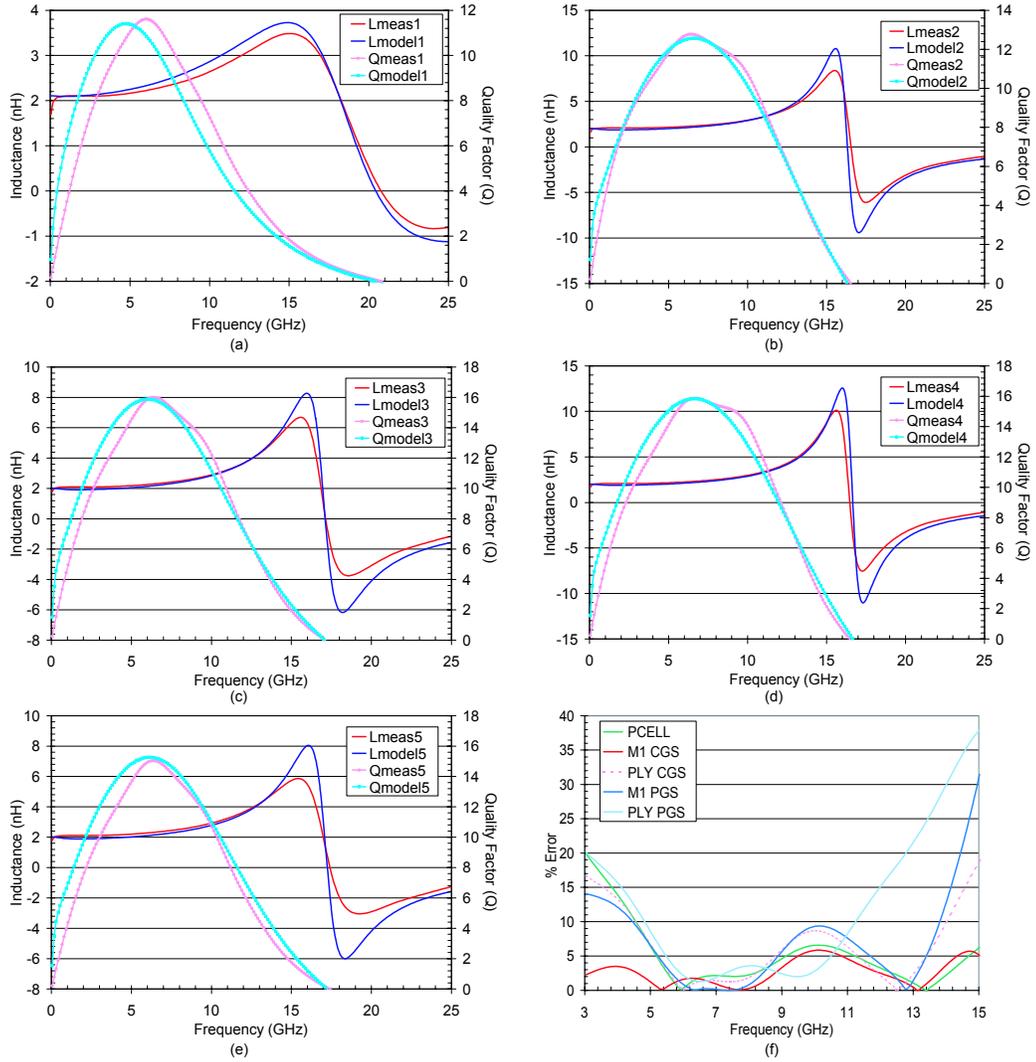


Figure 7.21: Plots of the measured and modeled  $L_{eff}$  and  $Q$  for the 2 nH inductor: (a) unshielded PCELL; (b) M1 CGS; (c) PLY CGS; (d) M1 PGS; and (e) PLY PGS. In (f), a plot of the model error percentage with respect to the measured data.

Table 7.4: Measured and modeled peak- $Q$  and  $f_{SR}$ .

2 nH						
	Measured $f_c$ of Peak- $Q$ ( GHz )	Measured Peak- $Q$	Modeled $f_c$ of Peak- $Q$ ( GHz )	Modeled Peak- $Q$	Measured $f_{SR}$ ( GHz )	Modeled $f_{SR}$ ( GHz )
PCELL	6.04	11.61	4.79	11.40	20.88	20.51
M1 CGS	6.41	12.78	6.66	12.56	16.64	16.39
PLY CGS	6.41	16.01	6.04	15.88	17.14	17.14
M1 PGS	6.66	15.87	6.66	15.83	16.52	16.77
PLY PGS	6.41	15.04	6.16	15.26	17.52	17.27
4 nH						
	Measured $f_c$ of Peak- $Q$ ( GHz )	Measured Peak- $Q$	Modeled $f_c$ of Peak- $Q$ ( GHz )	Modeled Peak- $Q$	Measured $f_{SR}$ ( GHz )	Modeled $f_{SR}$ ( GHz )
PCELL	3.42	12.65	3.54	12.54	11.40	11.40
M1 CGS	5.04	13.89	4.42	13.80	9.53	9.66
PLY CGS	4.67	18.93	4.04	18.79	9.78	9.91
M1 PGS	5.54	17.01	4.29	16.59	9.53	9.53
PLY PGS	4.42	18.09	4.17	18.08	9.91	9.91
6 nH						
	Measured $f_c$ of Peak- $Q$ ( GHz )	Measured Peak- $Q$	Modeled $f_c$ of Peak- $Q$ ( GHz )	Modeled Peak- $Q$	Measured $f_{SR}$ ( GHz )	Modeled $f_{SR}$ ( GHz )
PCELL	3.04	14.01	2.67	14.37	8.28	8.28
M1 CGS	3.67	16.34	3.17	16.89	7.16	7.16
PLY CGS	3.79	21.09	3.04	21.90	7.41	7.41
M1 PGS	3.92	17.02	3.29	17.10	7.29	7.29
PLY PGS	3.67	20.68	3.17	20.61	7.53	7.53

polysilicon shields provided up to a 50% improvement in peak- $Q$  over an unshielded inductor of the same value, though at a cost of a  $\sim 15\%$  decrease in  $f_{SR}$ ; the improvement in the peak- $Q$  of the metal-one shields was more modest ( $\sim 30\%$  increase in peak- $Q$ ) in comparison while the reduction in  $f_{SR}$  was closer to 20%. The greater improvement in the peak- $Q$  for the two-port inductors with polysilicon shields (50%) compared to the one-port inductors ( $\sim 20\%$ ) is due to the reduction in the shunt capacitance at the input and output ports of the inductor. This reduction occurs in the two-port case since these capacitors are effectively in series with each other from the perspective of the embedding system. The dramatic difference between the one-port and two-port measurements is readily apparent in the case of the shielded inductors because the patterned ground shield effectively moves the ground-plane of the inductor closer to the coil, which strengthens the series connection between the shunt capacitances.

A lumped-element model that can be used to quickly simulate the performance of an inductor with and without a patterned ground shield was also introduced. The model matched the  $Q$  and  $f_{SR}$  of the measured data with less than 10% error from  $\sim 4$  GHz up to the  $f_{SR}$  of the inductor. The model parameters are based on the length and width of the spiral material, allowing the parameters to be scaled to other values of inductance. The model provides a good first-order approximation of the performance of a spiral inductor for the rapid design of RF ICs. Although the specific results of the experiments presented here are dependent on the specific process of implementation (e.g. the number of metal layers, the distance between the inductor coil and the substrate, etc.), general trends applicable to modern Si RFIC technologies can be observed.

## Chapter 8

# Conclusions and Future Work

**T**HE primary objective of this research was to develop receiver components in SiGe BiCMOS technology for applications in high-speed wireless data networks; this work also sought to address on-going challenges in achieving high levels of integration in RF/wireless ICs. The first part of this research involved the design, layout, and testing of a  $\times 2$  sub-harmonic direct-conversion receiver RF front-end, fabricated in the IBM  $0.5\ \mu\text{m}$  5HP SiGe BiCMOS process. The RF front-end design enabled the investigation of sub-harmonic mixing as a potential solution to limited on-chip LO $\rightarrow$ RF isolation, and as a means to mitigate unwanted DC-offsets in direct-conversion receivers. The implementation of the sub-harmonic mixer, which uses a  $2f_{LO}$  frequency component generated from quadrature fundamental LO signals to downconvert the RF ( $\approx 2f_{LO}$ ), required a new approach for the synthesis of quadrature LO signals. Consequently, a new LO conditioning chain based on a pair of asymmetric polyphase filters was developed with the effects of amplitude and phase errors on the output IF quadrature balance in mind. An important contribution of this DCR research was an understanding of the achievable quadrature phase balance between the I and Q IF outputs as a function of the LO signal and mixed-signal effects in a SoC environment.

The second part of this work grew out of the need to compensate for such quadrature phase and amplitude imbalances in highly-integrated RF receivers. In addition, the excessive power consumption of the aforementioned DCR LO chain motivated the search for a new, more flexible approach to quadrature signal generation. There-

fore, the design, simulation, and layout of a novel phase-tunable/amplitude-tunable quadrature VCO (QVCO), implemented in the Freescale SiGe:C HIP6WRF 0.18  $\mu\text{m}$  BiCMOS process, was completed. The QVCO design was implemented with two differential  $LC$ -tank VCOs connected such that the two oscillator outputs lock in quadrature to the same frequency. Two different QVCO designs were offered, providing two different methods for dynamically adjusting the output quadrature phase balance. A variable gain buffer/amplifier was also included, which provides a means to dynamically tune the amplitude of output signals from the QVCO.

The need for high quality inductors in both the DCR and the QVCO designs motivated the third part of this research — the investigation of patterned ground shield inductors to achieve improvements in peak- $Q$ . A 5 mm  $\times$  5 mm inductor test chip, containing a range of different-valued, rectangular inductors, as well as a set of symmetric, octagonal, differential inductors — each implemented with four different patterned ground shield structures — was designed in the Freescale SiGe:C HIP6WRF 0.18  $\mu\text{m}$  BiCMOS process. Based on the measured results, a scalable, lumped-element model was developed to allow rapid simulation of the pattern ground shield effects during the design phase of a circuit, thereby eliminating the need for computationally-demanding electromagnetic (EM) simulations.

The remainder of this chapter presents the conclusions drawn from the three main parts of this dissertation. The contributions of each research component are enumerated at the end of each section. Future work based on this research is discussed at the conclusion of the chapter.

## 8.1 Conclusions

### 8.1.1 Direct Conversion Receiver Front-end

When the 5–6 GHz U-NII bands were released by the FCC in 1997, the application space in this frequency range was initially undeveloped and few commercial products were available on the market. Around this same time, SiGe BiCMOS technology was reaching commercial viability and offered sufficient high-frequency performance to easily cover the U-NII bands with potentially lower costs when compared with III-V

semiconductor solutions, such as Gallium Arsenide. Therefore, the 5–6 GHz DCR front-end in SiGe BiCMOS technology was a good candidate for research at the outset of this work. Of course today, RF CMOS is being readily applied to circuit designs at frequencies greater than 6 GHz. Nevertheless, the DCR front-end presented in this work was relatively unique, and served as a springboard for subsequent work in this dissertation.

As discussed in Chapter 2, the use of  $\times 2$  sub-harmonic mixers for the DCR front-end necessitated the design of an LO conditioning chain capable of dividing the LO signal into eight output channels, with  $45^\circ$  of phase-separation between them. A new method was developed for generating these signals using a combination of two polyphase filters, one with an odd number of poles and one with an even number of poles. An additional goal of this research was to explore the effects of this quadrature synthesis scheme on the I/Q phase balance at the IF outputs of the mixers. From the results presented in Chapter 3, for this approach to be effective, the entire LO chain from input to output must be fully differential; given this requirement, the measured quadrature phase balance of the mixers with such an LO chain was  $90^\circ$  at a specific LO power level. In addition, the mixers with a fully differential LO chain demonstrated strong supply noise rejection, since the  $90^\circ$  I/Q phase balance could be maintained in the presence of digital switching noise, injected on the mixer DC supply rails. However, this  $90^\circ$  phase balance was obtained by adjusting the power level of the LO signal to compensate for the effects of the injected noise, which is undesirable from the standpoint of an RF system implementation. This result illuminates the need for a new method to dynamically control the I/Q balance in mixed-signal SoC environments. Meanwhile, in the case of the single-ended-input LO chain, the imperfect differential signal generated by the LO single-ended-to-differential input buffer, which was also used in the LO chain of the receiver front-end circuit, led to a very large I/Q phase imbalance of  $\sim 30^\circ$ .

The  $\times 2$  sub-harmonic approach was originally chosen to help overcome the finite LO $\rightarrow$ RF port isolation typical of lossy silicon substrates, and thereby reduce or eliminate DC-offsets that result from LO self-mixing. For the front-end design, the DC-offset was measured to be  $\sim 10$  mV at an LO power of 0 dBm, which indicates that the sub-harmonic mixing approach alone is not sufficient for mitigating LO leakage. Although the mixers provided better than 50 dB of both  $2\text{LO}\rightarrow\text{RF}$  and  $\text{LO}\rightarrow\text{RF}$  iso-

lation, other factors, such as dummy metal-fill areas and bondwire radiation limited the on-chip isolation and contributed to LO self-mixing. Thus, these factors would need to be eliminated before the demonstrated sub-harmonic mixing approach could be completely effective. Nevertheless, the sub-harmonic mixer topology presented in Chapter 2 has been used as a reference design for active sub-harmonic mixers [51] and has been successfully scaled to the 24 GHz ISM band using a more advanced SiGe HBT technology [293].

The main contributions of this work include: the design of a new  $45^\circ$  quadrature generation scheme; the study of IF I/Q phase balance in the presence of power supply switching noise (a potential problem in high-speed, mixed-signal SoC environments) as a function of the LO signal; the investigation of sub-harmonic mixing as a means to reduce DC-offsets and improve LO $\rightarrow$ RF isolation for U-NII band applications; and the use of package and bondwire models, generated with an EM simulator, during the design process to obtain proper input matching at 5–6 GHz [294–297].

### 8.1.2 Quadrature VCO

The QVCO design presented in Chapter 6 proposed a novel method for generating quadrature signals that could be dynamically tuned, i.e. the phase and amplitude balance between the QVCO outputs could be adjusted in near real-time, in the analog domain. This tunability was achieved with two different designs — one in which phase tuning varactors were placed in the coupling paths of the *LC*-tank QVCO, and one in which phase tuning varactors were incorporated in a capacitive divider at the output of the *LC*-tank QVCO. The two designs provide a means to compare the phase-tuning effects on the oscillator phase noise, frequency tuning, and output signal swing. The QVCO designs are still awaiting fabrication; however, based on the simulated achievable tuning range, a patent disclosure was filed on the phase and amplitude tunable QVCO and a provisional patent was subsequently issued [298]. Future work includes the characterization of the prototype circuits to be fabricated.

As described in Section 6.2, the center-frequency of the oscillator is shifted away from the resonant frequency of the *LC*-tanks due to the addition of the coupling transistors; the direction of the frequency shift is determined by the series losses of the tank components [238]. In current published work on QVCOs, the series loss of

the tank inductor(s) is typically greater than the series loss of the tank capacitors and therefore, the QVCOs have exhibited a positive shift, or in other words, a higher center-frequency of oscillation. However, for the QVCO presented in this work, the phase-tuning varactors effectively add to the series loss of the tank capacitors, thereby causing a negative shift in the oscillator center-frequency — an effect verified in simulation. The negative frequency shift means the  $LC$ -tanks of the QVCO must be designed for a higher resonant frequency, which can actually be beneficial, since, generally speaking, the higher frequency results in smaller tank component values and a reduction in the physical area consumed by the component layouts. In addition, the two different phase-tuning methods had minimal effect on the output power of the oscillator; small variations in the output signal-swing can be corrected using the amplitude tunability of the output buffer/amplifier. The main contributions of this work include the design of RF QVCOs with phase-tunable quadrature outputs and the amplitude-tunable buffer/amplifier. This research offers the potential for future work (discussed in Section 8.2.2 below) in self-correcting RF transceiver circuit technology.

### 8.1.3 Patterned Ground Shield Inductors

The insertion of a patterned ground shield between an inductor coil and the underlying substrate is one approach for improving the quality factor of monolithic inductors. The ground shield helps reduce capacitive coupling to the lossy substrate by effectively screening the electric field from the substrate, while the patterning of the ground shield helps prevent the inductor’s magnetic field from inducing image currents in the shield, which would also tend to dissipate energy. Based on a range of two-port measurements, the polysilicon shields, which provided up to a 50% improvement in peak- $Q$  and a  $\sim 15\%$  degradation in  $f_{SR}$ , were a more suitable material for the patterned ground shields when compared to the metal-one shields, which had an improvement in the peak- $Q$  of  $\sim 30\%$  and a reduction in  $f_{SR}$  closer to 20%. Although two different shield-patterns were implemented — the center-grounded shield and the perimeter-grounded shield — the effects on peak- $Q$  and  $f_{SR}$  were similar for both shields.

One important conclusion from this research is the explanation for the difference seen in measured peak- $Q$  between one-port and two-port measurements. From the

perspective of the embedding system, the shunt capacitances at the input and output ports of the two-port inductors are tied together through the grounded shield and, as a result, are effectively in series with each other, which lowers their value and overall impact on inductor performance. This concept is verified when comparing the  $f_{SR}$  data of the one-port and two-port inductors; the  $f_{SR}$  of the two-port inductors is 26% higher than that of the one-port inductors, which indicates that the one-port inductors suffer from greater shunt capacitance.

A scalable lumped-element model that was developed based on the inductor measurements, and matched the  $Q$  and  $f_{SR}$  of the measured data with less than 10% error, from  $\sim 4$  GHz up to the  $f_{SR}$  of the inductors. Since the model parameters were based on the length and width of the spiral material, the parameters could be scaled to simulate other values of inductance. The proposed model provides accurate simulations of monolithic inductor performance, which enables the rapid design of RF ICs. Although the specific model parameters drawn from this experimental effort depend on the specific process of implementation (e.g. thickness of interconnect metals, number of interconnect layers/inter-layer dielectrics, the distance between the inductor coil and the substrate, etc.), the general modeling approach can be applied to other modern Si RFIC technologies. The main contributions of this work include the investigation of different patterned shields in different materials; the development of a scalable lumped element model to represent monolithic inductors with and without a patterned ground shield; and a valid explanation for the difference between one-port and two-port measurements of monolithic inductors over conductive ground planes [299, 300].

## 8.2 Future Work

The following sections detail improvements and future work based on the RF circuit and component concepts presented in this work.

### 8.2.1 Direct Conversion Receiver Front-end

For the DCR front-end, continuous-time DC-offset cancellation loops [150] and DSP-based, feed-forward approaches [301] have become the preferred method for mitigating DC-offsets generated by LO self-mixing. Furthermore, many of the new wireless communication standards are wide-band, or avoid modulation schemes that have significant signal content at DC; therefore, AC-coupling between the front-end mixers and the follow-on baseband amplifiers/low-pass filters can be safely employed. Still, sub-harmonic mixing has a number of other benefits, as described in Section 2.1, to warrant further study of the approach. In the case of this particular sub-harmonic mixer, future work could include the following topics.

- Porting the designs over to RF CMOS. Since CMOS is currently cheaper compared to other semiconductor processes, and is now quite capable of operation at 5–6 GHz frequencies, transitioning from a SiGe BiCMOS process would make the design more attractive for commercial products.
- Scaling the design to higher (millimeter-wave) frequencies; for example, W-band, where applications such as 77 GHz automotive radar will eventually migrate [302].
- Combining the RF transconductors of the I and Q mixers into a single, pre-amplifier stage; this single-stage could then be AC-coupled to the I and Q LO switching cores [293]. In essence, this topology can be viewed as a set of passive quadrature mixers fed by a single, differential RF pre-amplifier.
- Re-design of the LO signal generation. The multiple poles in the two polyphase filters resulted in significant amplitude imbalances between the I and Q LO signals, and the excessive insertion loss of this structure required the use of power-consumptive buffers/amplifiers. The quadrature LO signals could be generated by the QVCO with tunable I/Q balance, which would allow amplitude and phase imbalances to be corrected dynamically.

## 8.2.2 Quadrature VCO with Tunable I/Q Balance

The QVCO design offers several important areas for future work, foremost its pending fabrication and measurement. However, as with the DCR front-end, the existing design in SiGe BiCMOS could first be ported to a newer RF CMOS process for fabrication. This change in technology would require re-designing the  $-G_m$  transconductors and the variable-gain buffer/amplifier, and would likely require changes to the coupling transistor sizes and to the component values of the  $LC$ -tank. However, the overall RF CMOS design should be somewhat simplified in comparison to the BiCMOS version, since complications, such as DC-blocking capacitors in the base of the  $-G_m$  circuit and base-current biasing schemes, could be eliminated with the use of CMOS devices.

Assuming that phase-tunability is successfully demonstrated experimentally, the most significant future work relates to system applications of the QVCO circuit, particularly in receiver architectures suitable for SoC integration.

### Applications of the Quadrature VCO with Tunable I/Q Balance

A quadrature VCO with the ability to dynamically adjust the amplitude and phase of its outputs is extremely desirable for modern communication systems, particularly in modulation schemes where the amplitude and phase balance are critical for accurate transmission and reception of data. Quadrature amplitude modulation (QAM) and orthogonal frequency division multiplexing (OFDM) are two examples of modulation schemes where the accuracy of the quadrature signal is extremely important [78, 88]. Two potential applications of the QVCO are shown in Figure 8.1. In the first [Figure 8.1(a)], the QVCO is shown as the LO source in a direct-conversion receiver. The receiver would require additional circuitry to detect and process the IF amplitude and phase balance so as to generate the appropriate tuning voltages for the QVCO to obtain perfect quadrature signals at the IF. For example, a frequency/phase detector could determine the IF phase balance while an envelope detector could sense the differences in amplitude; the resulting signals from these two circuits could feed into a control circuit (possibly lookup table based) that would determine the required adjustment of the QVCO phase and amplitude tuning-voltages to remove the IF phase and/or amplitude imbalances. The circuit essentially performs self-correction

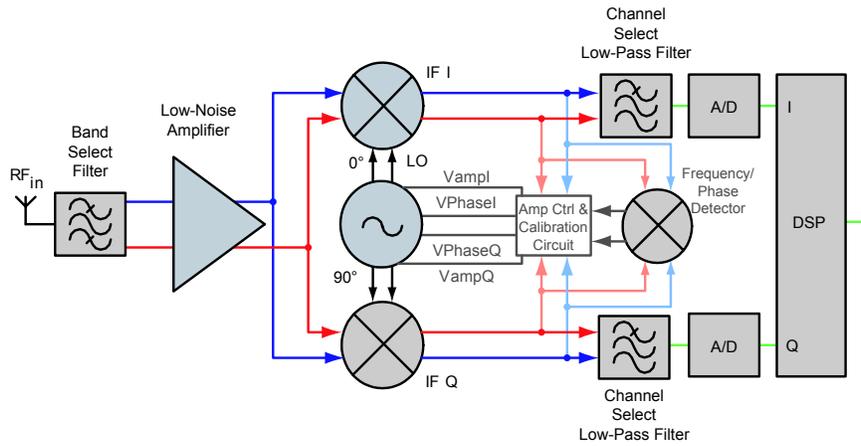
in the analog domain, which means the circuit could potentially respond faster and with greater sensitivity compared to approaches where I/Q correction processing is performed down-stream in the digital domain.

Another potential application for the QVCO is a low-IF receiver architecture employing Weaver image-rejection. As discussed in Section 1.3.2, the amplitude and phase balance of the LO signal is critical in determining the ability of the Weaver architecture to eliminate the unwanted image signal. An example implementation, which operates similar to the above DCR design, is shown in Figure 8.1(b). A key benefit to this approach is that the image-rejection mixers can now be implemented at the input RF frequency, since a wide range of amplitude and phase imbalances can be corrected using the QVCO thereby providing excellent suppression of the image signal at the front of the receiver. By directly converting the RF signal to a low-IF in one step, the QVCO-based low-IF receiver can produce near-perfect quadrature IF signals with sufficient image suppression to directly feed the signal into an ADC for digital baseband filtering and processing.

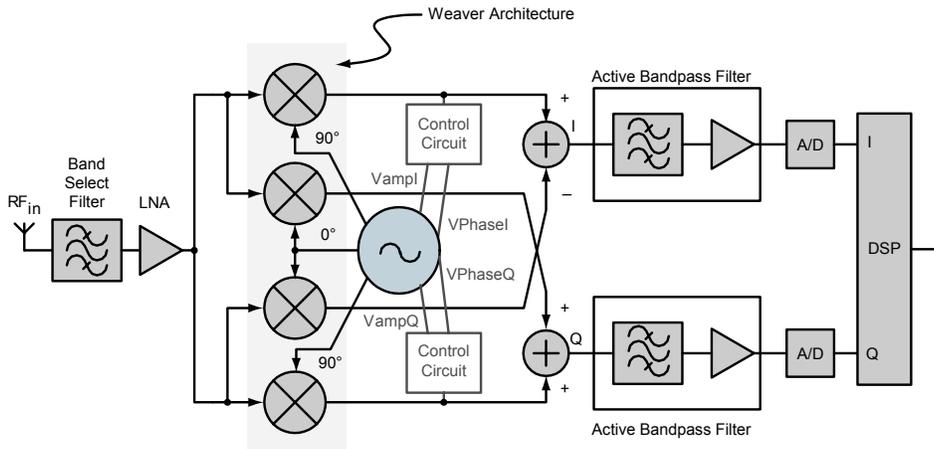
Incidentally, if two more *LC*-tank VCOs are connected to the QVCO as shown in Figure 8.2, eight phases with  $45^\circ$  of separation can be generated. As discussed in Chapter 2, these were the phases required for the sub-harmonic mixer design. Thus, the sub-harmonic direct-conversion receiver front-end from Chapters 4–5 could use this circuit in place of the polyphase filter-based LO chain and use the phase tunability of the octal-phase VCO to maintain perfect differential quadrature at the IF outputs of the sub-harmonic mixers. Based on initial simulations, the four coupled VCOs draw more current ( $\sim 46$  mA total) than the polyphase filter LO chain ( $\sim 34$  mA total); however, the eight-phase VCO uses a 1.8 V DC supply instead of the 3.3 V DC supply that was used in the original LO chain. Therefore, the simulated power consumption of the QVCO approach is roughly a third of the polyphase filter power (45 mW compared to 141 mW).

### 8.2.3 Patterned Ground Shield Inductors

With regards to the patterned ground shield inductor modeling effort, a similar study conducted in another IC technology would help verify the applicability of the developed lump-element model. By including more inductors with a greater distribution



(a)



(b)

Figure 8.1: (a) Block diagram of a direct-conversion receiver with the phase-tunable QVCO. (b) Block diagram of an image-reject receiver with the phase-tunable QVCO. Note: differential branches are omitted for simplification.

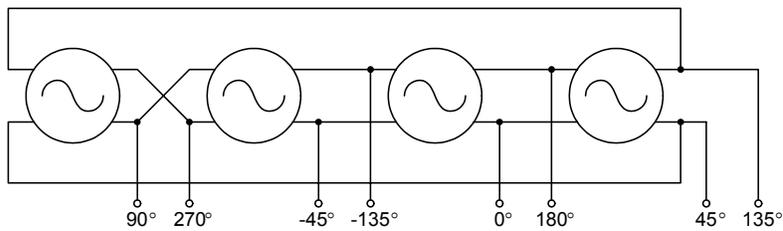


Figure 8.2: Block diagram of an eight phase quadrature oscillator. The output phases are separated by  $45^\circ$ .

of inductance values (perhaps only in a two-port measurement configuration), more accurate values for the model fitting parameters ( $M_{sub}$ ,  $R_{sub}$ , and  $\alpha_{shield}$ ) could be developed. The experiment could also be repeated on a re-designed version of the symmetric differential inductor; the appropriate spacing between the two-port GSG probe pads could be addressed using EM simulations to determine the required separation to prevent probe-tip radiation from coupling between ports. One candidate for this inductor is a new symmetric octagonal PCELL inductor included in the Freescale SiGe:C HIP6WRF 0.18  $\mu\text{m}$  BiCMOS process, which is scalable and allows for simplified layout of different inductance values.

Other future work could include the investigation of other shield materials, such as  $N^+$  diffusion (or  $P^+$  diffusion in an isolated p-well), using either of the proposed shield patterns. Finally, a more accurate model of the frequency dependent series loss within the inductor lumped-element model would improve the matching between the modeled and measured  $Q$  data at low frequencies.

# Afterword

The knowledge gained from the development of the various circuits and components of this work can be combined and implemented for a range of RF and microwave applications, including future wireless SoC solutions. It is hoped that the research presented in this document provides insight into how circuit designs and topologies can be used to meet some of the difficult integration challenges presented by emerging low-cost, low-power RF applications.

# Appendix A

## Mathematical Proof of the Hartley and Weaver Architectures

This Appendix shows mathematically the signal manipulation performed by the Hartley and Weaver architectures, which enables on-chip rejection of image signals. Alternatively, graphical analysis, which shows the signal phase and power spectral densities (PSDs) at each stage of the receiver, can also demonstrate how these architectures function. Such analysis can be found in [59] and [13].

The following analysis relies on complex envelope notation, derived from Euler's trigonometric identities:

$$e^{j\phi} = \cos(\phi) - j \sin(\phi) \quad (\text{A.1})$$

$$\cos(\phi) = \frac{e^{j\omega t} + e^{-j\omega t}}{2} \quad (\text{A.2})$$

$$\sin(\phi) = j \frac{e^{-j\omega t} - e^{j\omega t}}{2}. \quad (\text{A.3})$$

To reduce the complexity of the derivation, and for readability, simple continuous wave (CW) signals are assumed for the input RF signals (both desired and image) and for the LO. Therefore, the RF signals entering the mixers are assumed to be cosines at  $\omega_{RF} = 2\pi f_{RF}$  and  $\omega_{IM} = 2\pi f_{IM}$ , and the LO is assumed to be a cosine at  $\omega_{LO} = 2\pi f_{LO}$ . The equations that follow are based on low-side injection (thus,  $\omega_{IF} = \omega_{RF} - \omega_{LO}$ ); however, by switching the  $\omega_{RF}$  and  $\omega_{IM}$  terms, the results for

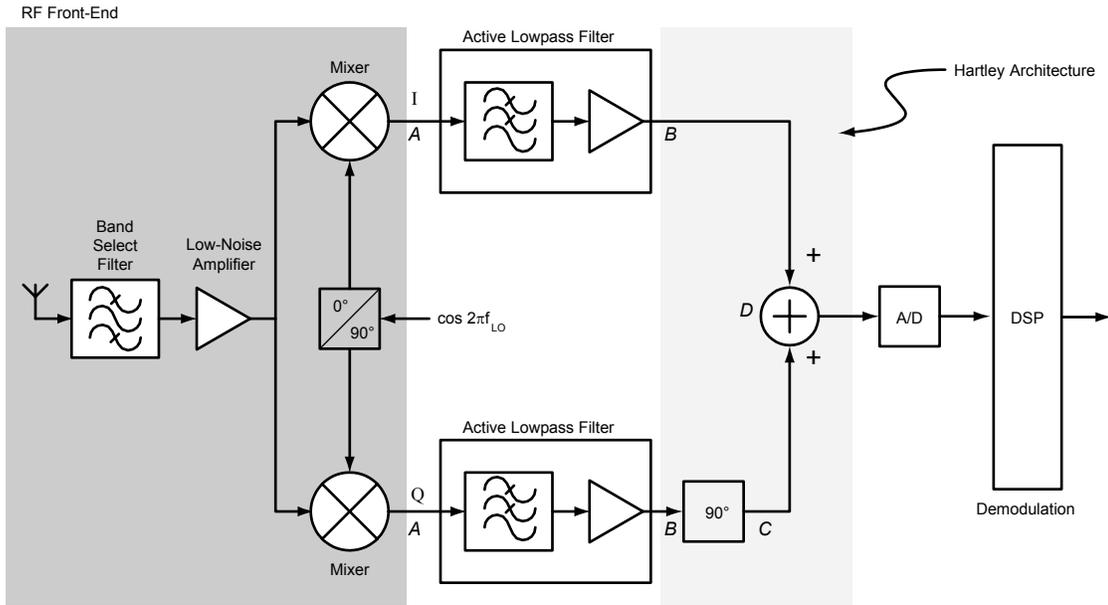


Figure A.1: Block diagram of the Hartley architecture.

high-side injection can straightforwardly be shown.

## A.1 Hartley Architecture

Figure A.1 shows the block diagram of the Hartley architecture. For the I branch of the receiver, the output of the mixers at I.A, denoted as  $IF_I$  for the desired signal and  $IM_I$  for the image, can be determined from the product of the desired signal and

the LO signal, and the product of the image and LO signal:

$$\begin{aligned} \text{IF}_I|_{@A} &= \cos(\omega_{RF}t) \cdot \cos(\omega_{LO}t) & (A.4) \\ &= \frac{e^{j\omega_{RF}t} + e^{-j\omega_{RF}t}}{2} \cdot \frac{e^{j\omega_{LO}t} + e^{-j\omega_{LO}t}}{2} \end{aligned}$$

$$\begin{aligned} &= \frac{1}{4} [e^{j(\omega_{RF}+\omega_{LO})t} + e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}+\omega_{LO})t}] \\ \text{IM}_I|_{@A} &= \cos(\omega_{IM}t) \cdot \cos(\omega_{LO}t) & (A.5) \\ &= \frac{e^{j\omega_{IM}t} + e^{-j\omega_{IM}t}}{2} \cdot \frac{e^{j\omega_{LO}t} + e^{-j\omega_{LO}t}}{2} \\ &= \frac{1}{4} [e^{j(\omega_{IM}+\omega_{LO})t} + e^{j(\omega_{IM}-\omega_{LO})t} + e^{-j(\omega_{IM}-\omega_{LO})t} + e^{-j(\omega_{IM}+\omega_{LO})t}] \\ &= \frac{1}{4} [e^{j(\omega_{LO}+\omega_{IM})t} + e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t} + e^{-j(\omega_{LO}+\omega_{IM})t}] \end{aligned}$$

Similarly, the output of the mixers at Q.A, denoted as  $\text{IF}_Q$  for the desired signal and  $\text{IM}_Q$  for the image, can be written as:

$$\begin{aligned} \text{IF}_Q|_{@A} &= \cos(\omega_{RF}t) \cdot \sin(\omega_{LO}t) & (A.6) \\ &= \frac{e^{j\omega_{RF}t} + e^{-j\omega_{RF}t}}{2} \cdot j \frac{e^{-j\omega_{LO}t} - e^{j\omega_{LO}t}}{2} \end{aligned}$$

$$\begin{aligned} &= \frac{j}{4} [e^{j(\omega_{RF}-\omega_{LO})t} - e^{j(\omega_{RF}+\omega_{LO})t} + e^{-j(\omega_{RF}+\omega_{LO})t} - e^{-j(\omega_{RF}-\omega_{LO})t}] \\ \text{IM}_Q|_{@A} &= \cos(\omega_{IM}t) \cdot \sin(\omega_{LO}t) & (A.7) \\ &= \frac{e^{j\omega_{IM}t} + e^{-j\omega_{IM}t}}{2} \cdot j \frac{e^{-j\omega_{LO}t} - e^{j\omega_{LO}t}}{2} \\ &= \frac{j}{4} [e^{j(\omega_{IM}-\omega_{LO})t} - e^{j(\omega_{IM}+\omega_{LO})t} + e^{-j(\omega_{IM}+\omega_{LO})t} - e^{-j(\omega_{IM}-\omega_{LO})t}] \\ &= \frac{j}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} - e^{j(\omega_{LO}-\omega_{IM})t} + e^{-j(\omega_{LO}+\omega_{IM})t} - e^{j(\omega_{LO}+\omega_{IM})t}] \end{aligned}$$

The low-pass filter removes the  $(\omega_{RF} + \omega_{LO})$  and  $(\omega_{LO} + \omega_{IM})$  terms, leaving the following four signals at I.B and Q.B:

$$\text{IF}_I|_{@B} = \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}] \quad (A.8)$$

$$\text{IM}_I|_{@B} = \frac{1}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t}] \quad (A.9)$$

$$\text{IF}_Q|_{@B} = \frac{j}{4} [e^{j(\omega_{RF}-\omega_{LO})t} - e^{-j(\omega_{RF}-\omega_{LO})t}] \quad (A.10)$$

$$\text{IM}_Q|_{@B} = \frac{j}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} - e^{j(\omega_{LO}-\omega_{IM})t}] \quad (A.11)$$

The in-line  $90^\circ$  phase shift in the Q branch is equivalent to taking the Hilbert transform, where the signal is multiplied by  $G(\omega) = -j \operatorname{sgn}(\omega)$ . Thus, the negative frequency terms in Equations A.8-A.11 are multiplied by  $+j$  and the positive frequency terms are multiplied by  $-j$ . The  $\text{IF}_Q$  and  $\text{IM}_Q$  signals at Q.C after the  $90^\circ$  shift are:

$$\begin{aligned}\text{IF}_Q|_{@C} &= j \times \frac{j}{4} [e^{j(\omega_{RF}-\omega_{LO})t} - e^{-j(\omega_{RF}-\omega_{LO})t}] \\ &= \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}]\end{aligned}\quad (\text{A.12})$$

$$\begin{aligned}\text{IM}_Q|_{@C} &= j \times \frac{j}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} - e^{j(\omega_{LO}-\omega_{IM})t}] \\ &= -\frac{1}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t}]\end{aligned}\quad (\text{A.13})$$

Adding the quadrature IF and IM terms, the removal of the image signal by the Hartley architecture is shown:

$$\begin{aligned}\text{IF}_I + \text{IF}_Q|_{@D} &= \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}] + \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}] \\ &= \frac{1}{2} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}]\end{aligned}\quad (\text{A.14})$$

$$\begin{aligned}\text{IM}_I + \text{IM}_Q|_{@D} &= \frac{1}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t}] + -\frac{1}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t}] \\ &= 0\end{aligned}\quad (\text{A.15})$$

Notably, the  $\frac{1}{2}$  coefficient in Equation A.14 indicates that half the power is lost to the sum frequencies  $(\omega_{RF} + \omega_{LO})$  and  $(\omega_{LO} + \omega_{IM})$  (which were neglected in the analysis by assuming low-pass filtering of the IF) in the mixing process.

## A.2 Weaver Architecture

A simplified block diagram of the Weaver architecture is shown in Figure A.2. The RF front-end is identical to that of the Hartley architecture; however, the low-pass filter is now replaced with a bandpass filter in order to eliminate the “second” image, which results from the second stage of mixing in the Weaver architecture. Therefore, the second-image is neglected in the following derivation.

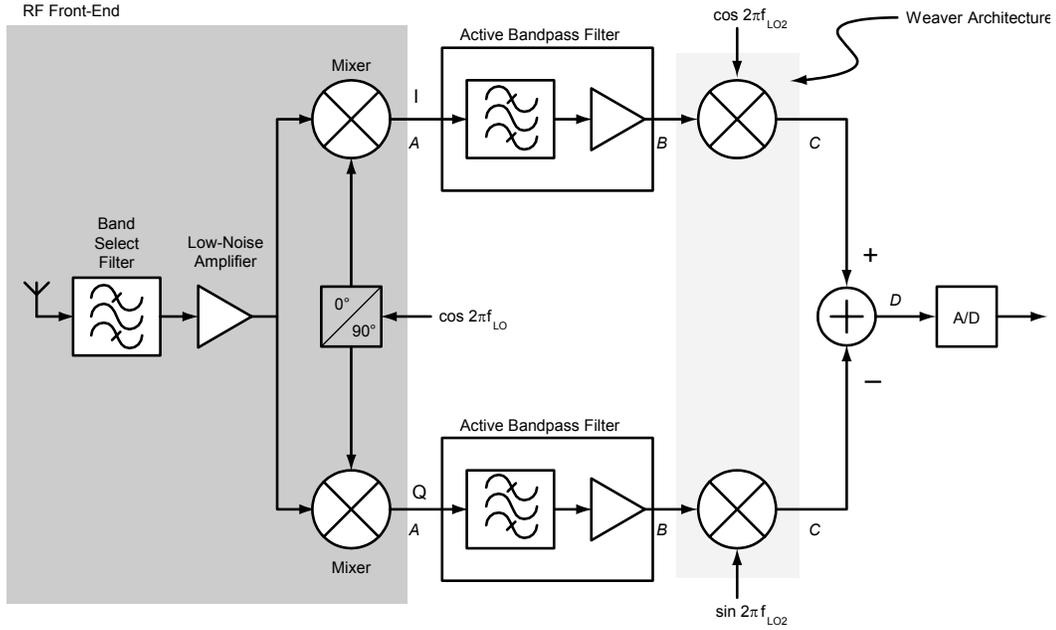


Figure A.2: Simplified block diagram of the Weaver architecture.

The IF and image signals at I.B and Q.B are the same as those expressed in Equations A.8-A.11, repeated here:

$$\text{IF}_I|_{@B} = \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}] = \frac{1}{2} \cos(\omega_{RF} - \omega_{LO})t \quad (\text{A.16})$$

$$\text{IM}_I|_{@B} = \frac{1}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t}] = \frac{1}{2} \cos(\omega_{LO} - \omega_{IM})t \quad (\text{A.17})$$

$$\text{IF}_Q|_{@B} = \frac{j}{4} [e^{j(\omega_{RF}-\omega_{LO})t} - e^{-j(\omega_{RF}-\omega_{LO})t}] = -\frac{1}{2} \sin(\omega_{RF} - \omega_{LO})t \quad (\text{A.18})$$

$$\text{IM}_Q|_{@B} = \frac{j}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} - e^{j(\omega_{LO}-\omega_{IM})t}] = -\frac{1}{2} \sin(\omega_{LO} - \omega_{IM})t \quad (\text{A.19})$$

The second stage of mixing multiplies these four signals by cos or sin of  $\omega_{LO_2}$ , which

gives the following at I.C and Q.C:

$$\begin{aligned}
\text{IF}_{I_2}|_{@C} &= \frac{1}{2} \cos(\omega_{RF} - \omega_{LO})t \cdot \cos(\omega_{LO_2}t) \\
&= \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}] \cdot \frac{e^{j\omega_{LO_2}t} + e^{-j\omega_{LO_2}t}}{2} \\
&= \frac{1}{8} \left[ \begin{array}{l} e^{j(\omega_{RF}-\omega_{LO}+\omega_{LO_2})t} + e^{j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} + \\ e^{-j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} + e^{-j(\omega_{RF}-\omega_{LO}+\omega_{LO_2})t} \end{array} \right] \quad (\text{A.20})
\end{aligned}$$

$$\begin{aligned}
\text{IM}_{I_2}|_{@C} &= \frac{1}{2} \cos(\omega_{LO} - \omega_{IM})t \cdot \cos(\omega_{LO_2}t) \\
&= \frac{1}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} + e^{j(\omega_{LO}-\omega_{IM})t}] \cdot \frac{e^{j\omega_{LO_2}t} + e^{-j\omega_{LO_2}t}}{2} \\
&= \frac{1}{8} \left[ \begin{array}{l} e^{j(\omega_{LO}-\omega_{IM}+\omega_{LO_2})t} + e^{j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + \\ e^{-j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + e^{-j(\omega_{LO}-\omega_{IM}+\omega_{LO_2})t} \end{array} \right] \quad (\text{A.21})
\end{aligned}$$

Similarly, the Q branch outputs after the second stage of mixing can be found by multiplying by the  $\sin(\omega_{LO_2}t)$ :

$$\begin{aligned}
\text{IF}_{Q_2}|_{@C} &= -\frac{1}{2} \sin(\omega_{RF} - \omega_{LO})t \cdot \sin(\omega_{LO_2}t) \\
&= \frac{j}{4} [e^{j(\omega_{RF}-\omega_{LO})t} - e^{-j(\omega_{RF}-\omega_{LO})t}] \cdot j \frac{e^{-j\omega_{LO_2}t} - e^{j\omega_{LO_2}t}}{2} \\
&= -\frac{1}{8} \left[ \begin{array}{l} e^{j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} - e^{j(\omega_{RF}-\omega_{LO}+\omega_{LO_2})t} - \\ e^{-j(\omega_{RF}-\omega_{LO}+\omega_{LO_2})t} + e^{-j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} \end{array} \right] \quad (\text{A.22})
\end{aligned}$$

$$\begin{aligned}
\text{IM}_{Q_2}|_{@C} &= -\frac{1}{2} \sin(\omega_{LO} - \omega_{IM})t \cdot \sin(\omega_{LO_2}t) \\
&= \frac{j}{4} [e^{-j(\omega_{LO}-\omega_{IM})t} - e^{j(\omega_{LO}-\omega_{IM})t}] \cdot j \frac{e^{-j\omega_{LO_2}t} - e^{j\omega_{LO_2}t}}{2} \\
&= -\frac{1}{8} \left[ \begin{array}{l} e^{-j(\omega_{LO}-\omega_{IM}+\omega_{LO_2})t} - e^{-j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} - \\ e^{j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + e^{j(\omega_{LO}-\omega_{IM}+\omega_{LO_2})t} \end{array} \right] \quad (\text{A.23})
\end{aligned}$$

The additive frequency terms  $(\omega_{RF}-\omega_{LO}+\omega_{LO_2})$  and  $(\omega_{LO}-\omega_{IM}+\omega_{LO_2})$  are typically outside the bandwidth of the baseband circuitry and therefore can be ignored. With

this simplification, the inputs of the adder are given in the following four equations:

$$\text{IF}_I|_{@C} = \frac{1}{8} [e^{j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} + e^{-j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t}] \quad (\text{A.24})$$

$$\text{IM}_I|_{@C} = \frac{1}{8} [e^{j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + e^{-j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t}] \quad (\text{A.25})$$

$$\text{IF}_Q|_{@C} = -\frac{1}{8} [e^{j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} + e^{-j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t}] \quad (\text{A.26})$$

$$\text{IM}_Q|_{@C} = \frac{1}{8} [e^{-j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + e^{j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t}] \quad (\text{A.27})$$

By subtracting the Q-side IF and IM terms, the elimination of the image signal by the Weaver architecture is shown:

$$\begin{aligned} \text{IF}_I - \text{IF}_Q|_{@D} &= \frac{1}{8} [e^{j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} + e^{-j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t}] - \\ &\quad \left( -\frac{1}{8} [e^{j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t} + e^{-j(\omega_{RF}-\omega_{LO}-\omega_{LO_2})t}] \right) \\ &= \frac{1}{4} [e^{j(\omega_{RF}-\omega_{LO})t} + e^{-j(\omega_{RF}-\omega_{LO})t}] \end{aligned} \quad (\text{A.28})$$

$$\begin{aligned} \text{IM}_I - \text{IM}_Q|_{@D} &= \frac{1}{8} [e^{j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + e^{-j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t}] - \\ &\quad \frac{1}{8} [e^{j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t} + e^{-j(\omega_{LO}-\omega_{IM}-\omega_{LO_2})t}] \\ &= 0 \end{aligned} \quad (\text{A.29})$$

The  $\frac{1}{4}$  coefficient in Equation A.28 results from the two stages of mixing, where at each stage the output power is split between the bands located at the sum and difference frequencies of the mixing process.

# Appendix B

## Bondwire Modeling

**A**S discussed in Section 2.5.1, the sub-harmonic mixer and RF front-end designs were housed in the Amkor MicroLeadFrame (MLF) series of plastic packages and the connection between the chip and package pins/die flag were made using bondwires. Initial estimates of the parasitics associated with these bondwires were made using the model presented in [303]. Since the bondwires used are electrically short compared to the wavelength of circuit operation, their parasitics could be accurately represented as an inductance and a finite series resistance. For bondwires between the chip and the package pins and for downbonds, the parasitic inductance is calculated using the length ( $\ell$ ) and diameter ( $d$ ) of the bondwire:

$$L_{BW} = \frac{\mu_0 \ell}{2\pi} \left( \ln \left\{ \frac{2\ell}{d} + \left[ 1 + \left( \frac{2\ell}{d} \right)^2 \right]^{\frac{1}{2}} \right\} + \frac{d}{2\ell} - \left[ 1 + \left( \frac{d}{2\ell} \right)^2 \right]^{\frac{1}{2}} + \mu_r \delta \right) \quad (\text{B.1})$$

where  $\delta$  is the skin effect calculated at the center frequency of the design ( $f_0 = 5.25$  GHz for the sub-harmonic mixer design) and  $\mu_r$  is the relative permeability of the bondwire material. Figure B.1 shows the approximate layout of the downbonds and bondwires to the package pins, which was used to estimate the bondwire lengths. Based on the loop height ( $h_l$ ), the height from the top of the die to the top of the package ( $h_d$ ), and the distance between the bondpad and the pin ( $l$ ), the overall length

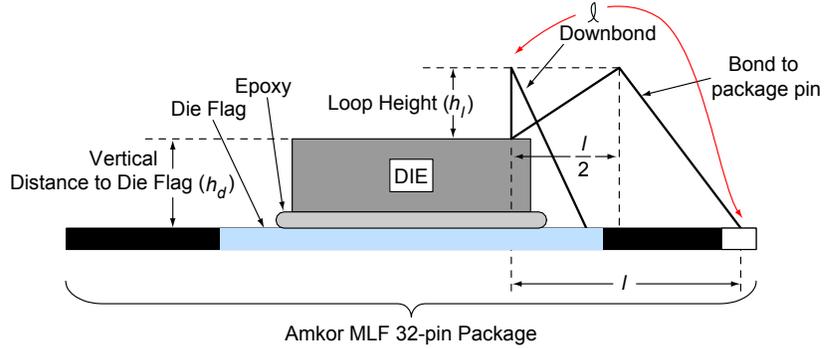


Figure B.1: Illustration of the downbonds and bonds to package pins. The length of the bondwire accounts for the height of the bondpad above the die flag.

( $\ell$ ) of the bondwire was estimated to be:

$$\ell = \left[ h_l^2 + \left( \frac{l}{2} \right)^2 \right]^{\frac{1}{2}} + \left[ (h_l + h_d)^2 + \left( \frac{l}{2} \right)^2 \right]^{\frac{1}{2}} \quad (\text{B.2})$$

The mutual inductance between two adjacent bondwires (nearest neighbors) is calculated based on the center-line-to-center-line separation between the them and the resulting effective inductance includes this coupling. The high frequency series resistance of the bondwires was determined using the curve-fitting equations given in [303]. The calculated model values for the inductance and series resistance were close to the values returned from the EM simulations discussed in Section 2.5.1.

An Excel spreadsheet [304] was developed to consolidate the model equations and to simplify the calculations of the parasitic inductance and resistance of a given bondwire. The spreadsheet accepts the  $x$ - $y$  coordinates of the bondwire endpoints (which are determined from the Cadence Virtuoso layout) and the endpoint coordinates of the nearest neighboring bondwire. From these values, the spreadsheet determines the length of each bondwire and the mutual inductance between a bondwire and its nearest neighbor, and returns the associated effective inductance and resistance. Figure B.2 shows the spreadsheet interface.

## Bondwire Model

Bondwire Diameter	Epoxy Height	Die Height	Loop Height	Permittivity of Free Space	Permeability of Free Space	Resistivity of Gold
0.0127	0.02032	0.3566	0.25155	8.85E-12	1.25664E-06	2.21239E-08
mm	mm	mm	mm	F/m	H/m	$\Omega$ m

Specific to Fabrication:

Center Frequency	Distance Between Bondwires	Length of Bondwire of Interest	Length of Adjacent Bondwire	Bondwire Type	Bondwire of Interest Start Point	Bondwire of Interest End Point	Adjacent Bondwire Start Point	Adjacent Bondwire End Point	Design Kit
5.25E+09	1.406733	1.6704404	0.936571025	0 = To Package 1 = Downbond	2758.3	2230.95	2758.3	1019.15	0 = Motorola Kit 1 = Any Other Kit
Hz	mm	mm	mm		(x/y) Cadence	(x/y) Cadence	(x/y) mm	(x/y) mm	

Specific to Design:

Inductance of Bondwire of Interest	Inductance of Adjacent Bondwire	Mutual Inductance Between Bondwire and Die Flag	Mutual Inductance Between Bondwires	Coupling Coefficient k
2.073	1.323	8.14E-08	0.234	0.141
nH	nH	nH	nH	

Intermediate Values:

Total Modeled Inductance with Mutual Coupling	Series Resistance
0.957	0.536
nH	$\Omega$

Final Model Parameters:

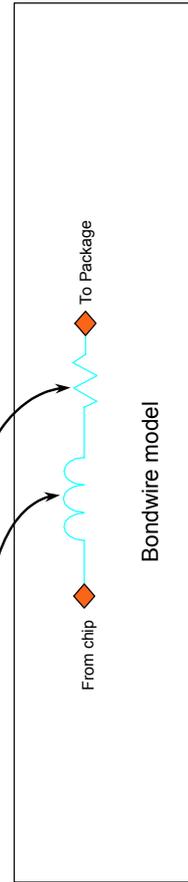


Figure B.2: The Excel spreadsheet user interface to the simplified bondwire model.

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# Vita

Richard M. Svitek was born many moons ago in Pittsburgh, Pennsylvania. After graduating from Ambridge Area High School, he attended the University of Pittsburgh; though he had intended to study computer science, he was quickly lured into electrical engineering. In 1996, he joined M/A-COM, Inc. as a co-op in Lowell, MA, where he was first introduced to the black art of RF engineering. He received his Bachelors of Science degree in December 1998 and joined Verizon Wireless as a systems performance engineer shortly after graduation.

In 2000, Rich enrolled in the electrical engineering graduate school program at Virginia Polytechnic Institute and State University and in May of 2001, he was fortunate to join Dr. Raman's Wireless Microsystems Laboratory to conduct research on wireless RF ICs. Upon completion of his graduate degree, Rich will attempt to rediscover life outside of school.