Chapter 1. Introduction

In this chapter, the reader is introduced ferroelectric materials used for digital memories and the status of this technology. The basic operation of a ferroelectric memory device is then discussed. Following this, the advantage and disadvantage of the most widely investigated ferroelectric materials are discussed. The specific objectives of this dissertation is outlined subsequent to this section and finally a brief description of the contents of this dissertation is provided.

1.1 FERROELECTRIC MEMORIES AND ITS BASIC OPERATION

Nonvolatile memory is an essential part of all computer systems. It is especially important for specific use such as military systems where vital information has to be stored in some type of a nonvolatile memory-memory that does not lose information when power is lost in a hostile environment. Among the available nonvolatile memory technologies, disk memories offer large capacities, and are widely used in such items as personal computers. However, they are slow, bulky, and susceptible to breakdown because of their mechanical nature. Magnetic core and magnetoinducive plated wire memories are very limited in capacity, are very bulky, have large power requirements and are very expensive. Erasable programmable read-only memories (EPROM) and electrically erasable programmable read-only memory (EEPROM) have slower write speed, are susceptible to radiation damage, and fatigue faster than either core or silicon random access memories. Silicon oxide nitride oxide silicon (SONOS) memory is a type of nonvolatile memory option that is fast to read and can be radiation hard. Unfortunately however, SONOS is yet to be programmed for long retention (over five years) with programmable pulses of 1 μs or shorter. Another memory option currently under development is the magnetoresistive random access memory (MRAM), which has the potential to provide high density, radiation hardness, and nondestructive readout (NDRO) operation with unlimited endurance. Major disadvantages of this device are its slower read cycle time and larger cell design. Key characteristics of some of the current and future nonvolatile memory technology are listed in Table 1-1. When one considers all the selection requirements for a nonvolatile memory, namely fastread/write, radiation hardness,

Table 1-1. Key characteristics of candidate nonvolatile memory technologies. [1]

	FLOATIN GATE EEPROM	FLASH EEPROM	SNOS nvSRAM (Shadow)	MNOS EEPROM (SNOS)	SONOS EEPROM	DRO FRAM	NDRO FRAM	MRAM	CORE
SPEED (ACCESS TIME)	150 nsec	120 nsec	35 nsec	150 nsec	150 nsec	100 nsec	200 nsec	Density Dependent 200 ns-2μs	350 nsec
WRITE TIME	10 msec Byte/Page	High	SRAM write 35 nsec; Download 11 msec	10 msec Byte	10 msec Byte	100-200 nsec	100-200 nsec	100-200 nsec	900 nsec
ENDURANCE	10E4-10E5 write cycles	10E4 Write cycles	10E5 Power cycles	10E5 Write cycles	10E6 Write cycles	10E10 Read/Write	10E10 Write cycles	No known Limitations	No Limits
RADIATION HARDNESS	Low-Moderate	Low-Moderate	Moderate	High	High	High	High	High	Moderate-High
LIMITATIONS	Write speed Endurance	Write speed Endurance	Density	Write speed	Write speed	Endurance DRO	None	Read speed, Density	Speed, Density Power
COST	Moderate	Low	Moderate to High	Low	Moderate	Potentially Low	Potentially Low to Moderate	Potentially Moderate	High

cost effectiveness and compatibility with currently used integrated circuit (IC) processing technology, high endurance and retention, and nondestructive readout capability, the ferroelectric memory stands out as the logical choice for all applications where submicro-second programming is needed [2].

Ferroelectric materials are characterized by a reversible spontaneous polarization in the absence of an electric field [3-6]. Spontaneous polarization in a ferroelectric arises from a noncentrosymmetric arrangement of ions in its unit cell that produces an electric dipole moment. Adjacent unit cells tends to polarize in the same direction and form a region called a ferroelectric domain. The most common ferroelectrics have the ABO_3 perovskite structure shown in Fig 1-1. Above the Curie temperature, these materials have a centrosymmetric structure and therefore lose all spontaneous polarization. In this state, the material is termed paraelectric. As the temperature is lowered through the Curie point, a phase transformation takes place from the paraelectric state to the ferroelectric state. The center ion is displaced from its body-centered position and the cubic unit cell deforms to assume one of the noncentrosymmetric structures such as tetragonal, rhombohedral or monoclinic structures. When an alternating electric field is applied to a ferroelectric, the polarization shows a hysteretic behavior with the applied field (Fig 1-2). In this initial stages, the ferroelectric domains that are oriented favorably with respect to the applied field direction grow at the expense of other domains. This continues until total domain growth and reorientation have occurred. At this stage, the material has reached its saturation polarization P_{sat}. If the electric field is then removed, some of the domains do not return to their random configurations and orientations. The polarization at this stage is called the remanent polarization, P_r. The strength of the electric field required to return the polarization to zero is the coercive field, E_c.

Although it is possible to utilize these ferroelectric properties for a wide variety of applications., the primary impetus of recent research activity in this field is directed towards the development of nonvolatile random access memories[3]. In principle, the memory application is based on the hysteretic behavior of polarization with electric field as shown in Fig 1-2. When an external voltage is applied to a ferroelectric capacitor, there is a net ionic displacement in the unit cells of the ferroelectric material. The individual unit cells interact constructively with their neighbors to produce domains within the material. As voltage is

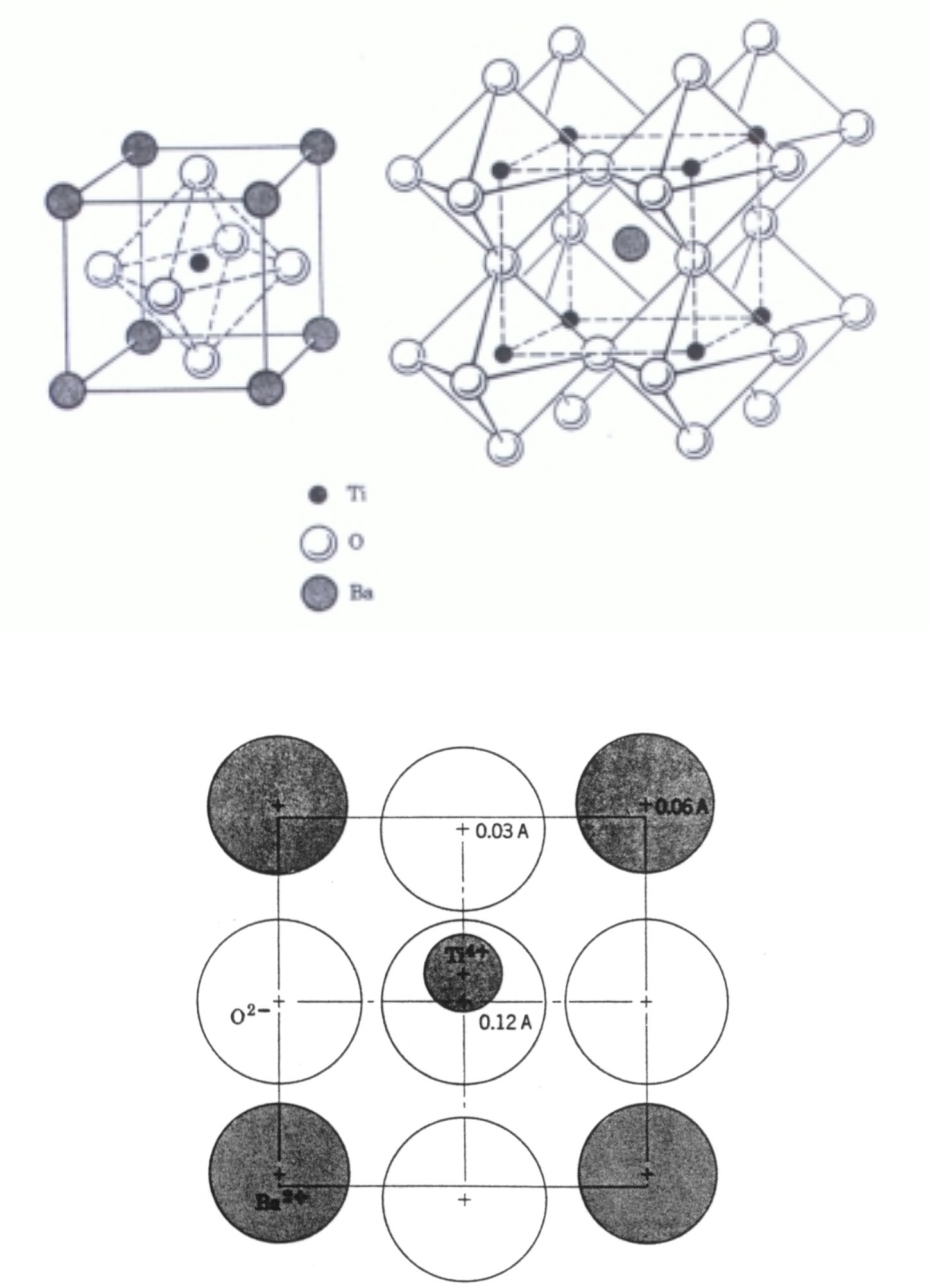

Figure 1-1. Unit cell of ABO_3 type perovskite structured material

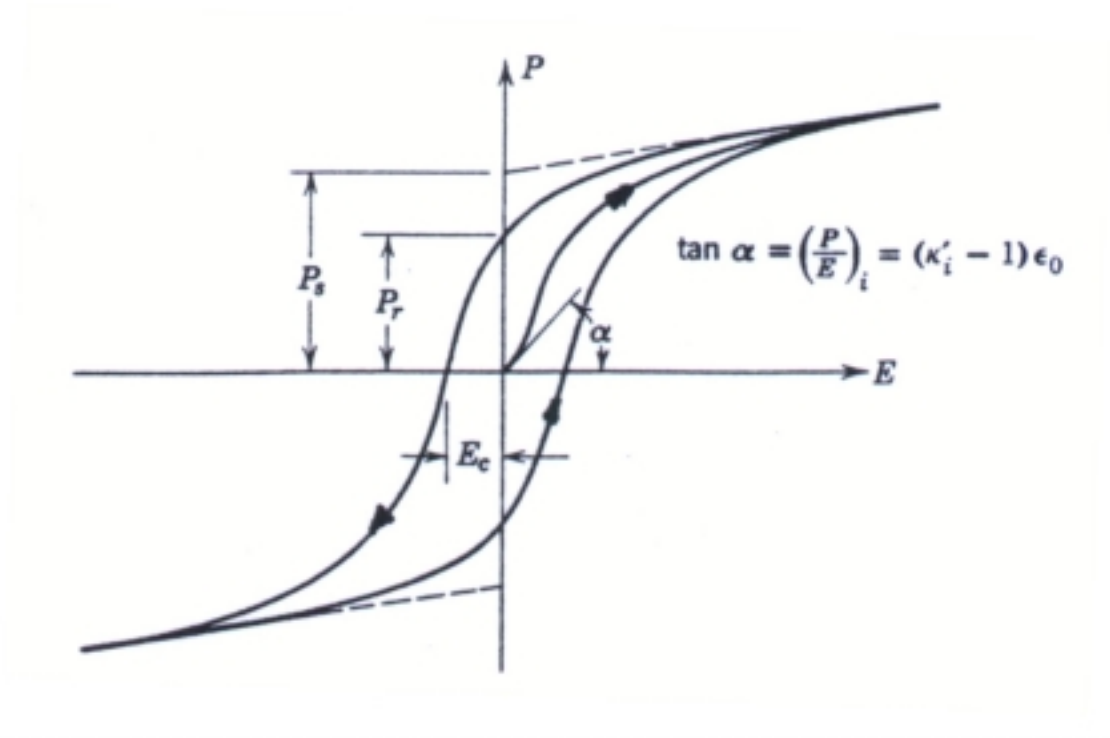

Figure 1-2. A typical ferroelectric hysterisis loop

removed, the majority of the domains will remain poled in the direction of applied field, requiring compensation charge to remain on the plates of the capacitor. It is this compensation charge that causes the hysterisis in the polarization with applied external voltage [7]. At zero applied field, there are two states of polarization, $\pm P_r$. Furthermore, these two states of polarization are equally stable. Either of these two staes could be encoded as a "1" or a "0" and since no external field is required to maintain these states, the momory device is nonvolatile. Clearly, to switch the state of the device, a threshold field greater than $\pm E_c$ is required. Additionally, in order to reduce the required applied voltage (to within 5 V) for a given E_c, the ferroelectric materials need to be processed in the form of thin films.

From a digital point of view, if a voltage is applied to a ferroelectric capacitor in a direction opposite of the previous voltage, the remanent domains will switch, requiring compensating charge to flow onto the capacitor plates [7]. If the field is applied in the direction of the previously applied field, no switching takes place, no change occurs in the compensating charge, and a reduced amount of charge flows to the capacitor. This property can be used to read the state or write a desired state into the capacitor. In most ferroelectric memories, the memory cell is read destructively by sensing the current transient that is delivered to a small load resistor when an external voltage is applied to the cell. For example, if a memory cell is in a negative state ($-P_r$) and a positive switching voltage is applied to it, there will be a switching charge given by [3-4]:

$$Q = A\varepsilon E_a + A\int_0^{\infty} \frac{dP}{dt}dt \qquad (1.1)$$

where A is area of the cell, ε is the dielectric constant of the ferroelectric material, E_a is the applied field and P is the polarization of the ferroelectric. Equation 1.1, as depicted in Fig 1-3, indicates that this current transient, known as the "switching current", consists of a linear dielectric response ($A\varepsilon E_a$) and a displacement current. A "nonswitching current" transient, for example, is the response of a memory cell in a positive state ($+P_r$) to a positive applied voltage. In this case,

$$Q = A\varepsilon E_a \qquad (1.2)$$

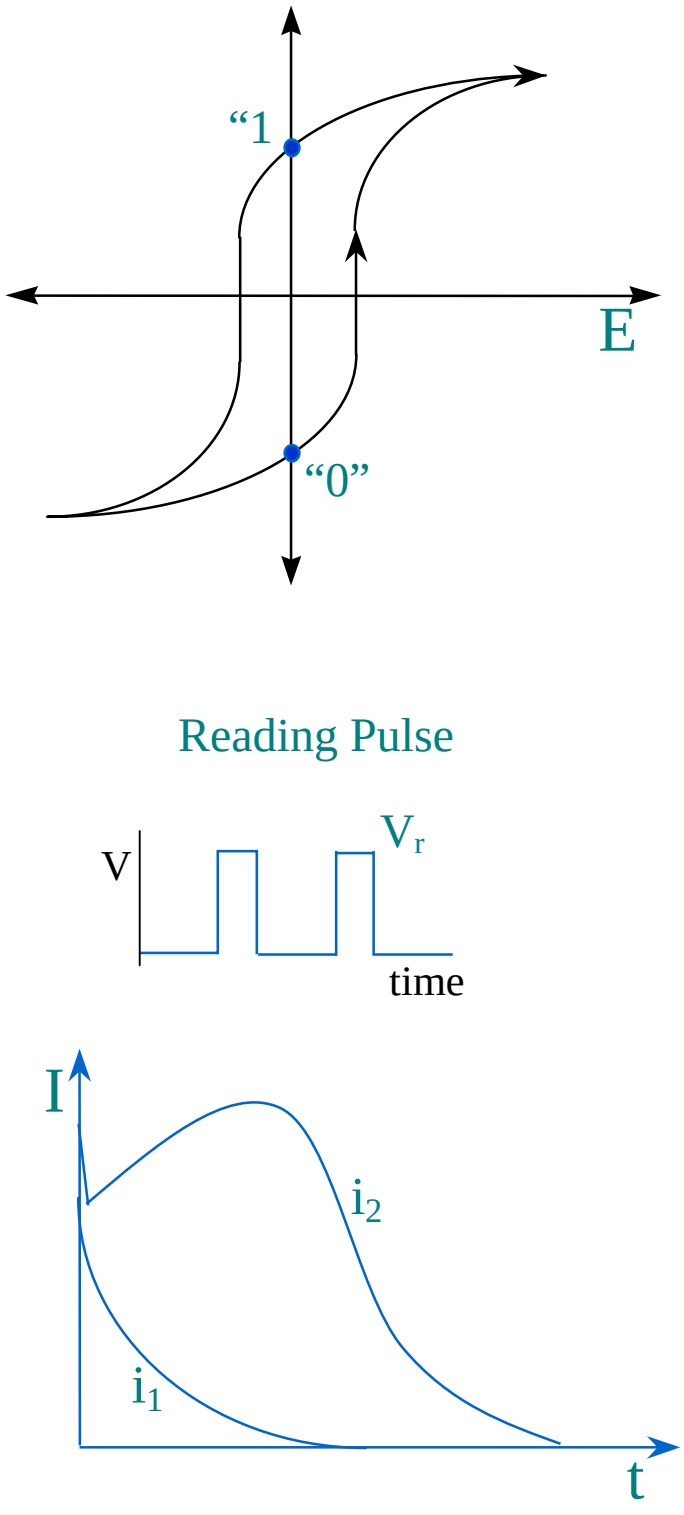

Figure 1-3. Schematic of the read/write operation in a ferroelectric memory cell

A sense amplifier and other associated circuitry is used in a FRAM device to determine these current transients and thereby read the state of the device.

The basic operation discussed so far describes the working of a typical destructive readout (DRO) single transistor-single capacitor ferroelectric. However, there are actually two basic types of integration and operation schemes utilizing the ferroelectric materials: (1) destructive readout (DRO) where the information must be rewritten after every read operation; and, (2) nondestructive readout (NDRO) where the information can be read over and over again until the next write operation. However, throughout this dissertation, our focus will be on the DRO single transistor-single capacitor ferroelectric memories. Integrated ferroelectric random access memory using the DRO scheme closely resembles dynamic random access memory (DRAM). A DRO FRAM is close to realization. The basic structure of such memory includes a thin film ferroelectric capacitor sandwiched between two chemically stable metal electrodes, integrated either on top of, in case of high density memory, or next to a semiconductor IC fabricated using existing CMOS technology as shown in Fig 1-4. The chip design consists of a matrix array of memory elements and transistors, with each memory element integrated to appropriate transistor circuitry. A typical memory element is also shown in Fig 1-4. A transistor known as the pass-gate transistor or select transistor is connected between the ferroelectric capacitor (C_f) and a sense capacitor (C_s). The need for this transistor arises from the fact that ferroelectrics do not exhibit well defined coercive fields or switching voltages, thus creating the so called "half-select disturb problem", i.e., the possibility of unintentional switching of cells adjacent to the ones being addressed in a large array of memory elements. The selected transistor provides electrical isolation to each memory cell, allowing the circuit to select which capacitor is to be switched and creating individually addressable bits. Voltage is applied to the ferroelectric capacitor by the drive line, the select transistor is controlled by the word line, and the cell is sensed via the bit line. The signal is measured by means of a sense amplifier at the end of the bit line which identifies the state of the bit [8].

1.2 MATERIALS AND PROBLEM DEFINITION

The current surge in interest in ferroelectric nonvolatile memories can be traced to the development of thin film technologies in the 1970's and 1980's allowing the fabrication of thin

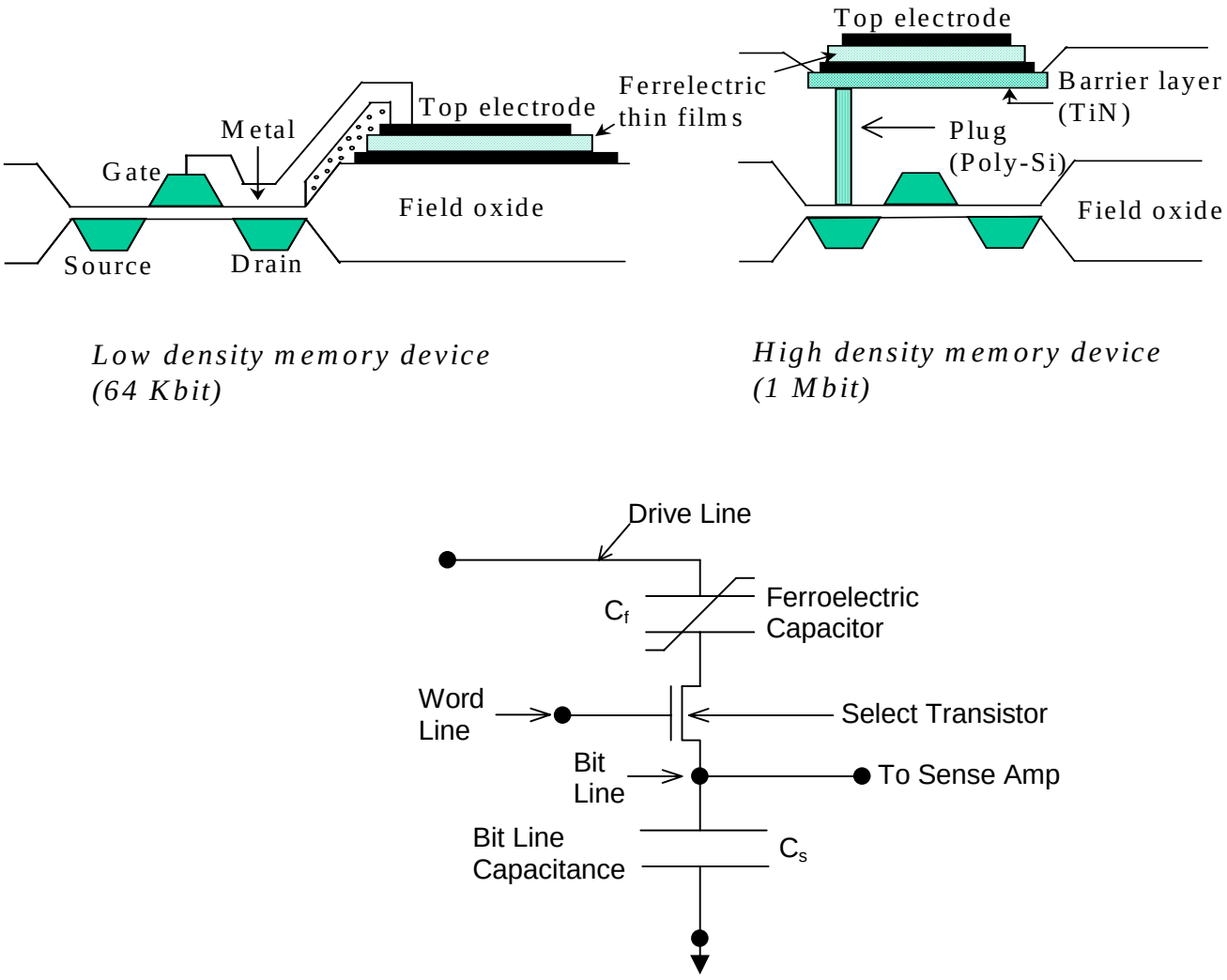

Figure 1-4. Proposed ferroelectric memory cell device configuration [8]

film capacitors at temperatures compatible with semiconductor processing. An ideal ferroelectric should have small dielectric constant, reasonable (~ 5 $\mu C/cm^2$) spontaneous polarization, and high Curie temperature (beyond the storage and operating temperature range of the device). Required low voltage operation (< 5V) necessitates submicron layer thickness with low coercive field and adequate dielectric breakdown. Inherent switching speed should be in the nanosecond range, and the ferroelectric capacitor should have good retention and endurance. Radiation hardness is another desirable property for military applications; and, of course, the material should be chemically stable. Additionally, to be useful, a ferroelectric material in a memory array must have good retention and imprint characteristics. The films must have very uniform composition and thickness over the surface of the integrated circuit (IC) so that the capacitance associated with each memory cell is the same. Also, the processing required to produce the ferroelectric thin film must not have a detrimental effect on the underlying circuitry.

Many materials show ferroelectricity and two families of materials, perovskite (e.g. $PbZr_{1-x}Ti_xO_3$) and layered perovskites (e.g. $SrBi_2Ta_2O_9$ and $SrBi_2Nb_2O_9$), have been widely investigated for memory applications. However, the realization of a commercially viable nonvolatile FRAM technology based on PZT has been hampered by the lack of reliable performance of the PZT ferroelectric capacitor or to problems related to the growth and processing of ferroelectric capacitor layers. The PZT films grown on metal electrode such as Pt show high fatigue, i.e. loss of polarization with switching cycles [4-5]. The polarization fatigue problem can be solved for all practical purposes only by replacing the metallic Pt electrodes with metal-oxide electrodes such as RuO_2, or with any array of the perovskite metal oxides such as $La_{0.5}Sr_{0.5}CoO_9$, or with hybrid metal-oxide electrodes, among others. The lead based ferroelectrics have been extensively studied, but recently issues with fatigue, environmental safety, and health concerns have prompted interest in $SrBi_2Ta_2O_9$ (SBT) which belongs to layered perovskite family. The bulk bismuth layer-type ferroelectric compounds were discovered in 1959 [9-14]. The family of bismuth layered oxides has the formula

$$(Bi_2O_2)^{2+}(Me_{m-1}R_mO_{3m+1})^{2-}$$

where

M_e = mono-, di-, or trivalent ions,

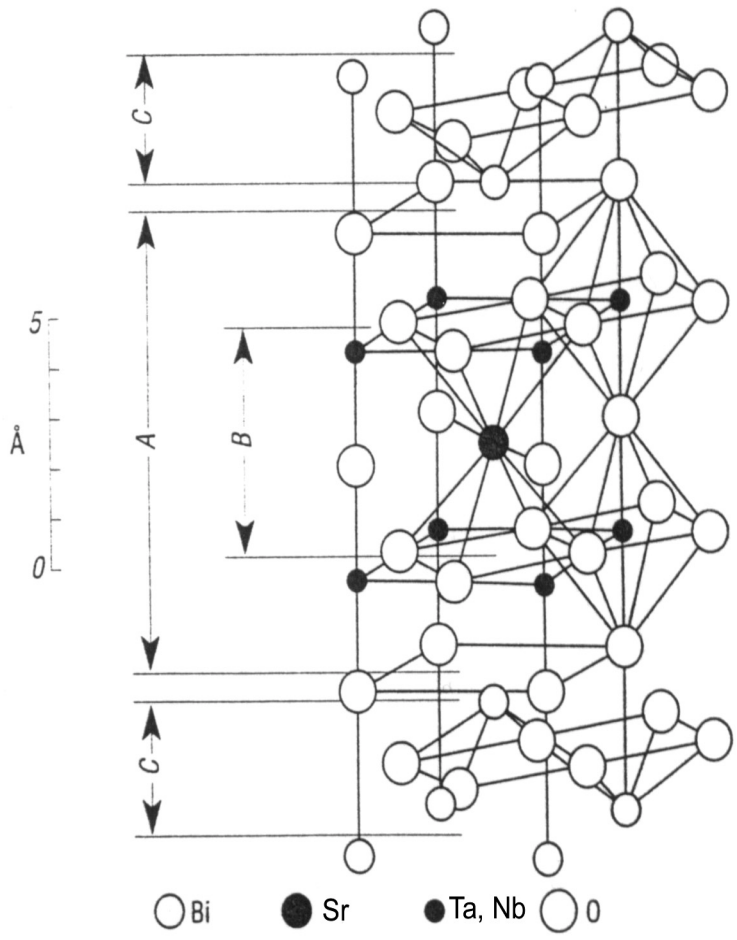

Figure 1-5. Unit cell structure of bismuth layered oxide (shown $SrBi_2Ta_2O_9$)

R = Ti^{4+}, Nb^{5+}, Ta^{5+} etc., single or in combination

m = 2, 3, 4 etc.

These compounds have a structure comprised of a stacking of *m* perovskite-like units of O-R-O chains between Bi_2O_2 layers along the pseudo-tetrahedral *c*-axis as shown in Fig. 1-5. The perovskite-like units are continuous only in the planes perpendicular to the *c*-axis; along *c*-axis, the continuous extension of O-R-O chains is interrupted not only by the presence of Bi_2O_2 layers but also by the translation of the perovskite-like units in the planes perpendicular to the *c*-axis. Because the presence of RO_6 octahedrons in perovskite-like layers, spontaneous polarization can occur in the planes of these layers.

The layered perovskite materials are attractive because of their good fatigue, retention, and electrical characteristics[15-17]. SBT is a promising material for memory applications because of its low leakage current and good fatigue and retention characteristics. The major limitation for the application of the SBT is the high processing temperature (~800 ^oC), lower P_r and low Curie temperature which make the direct integration into high density CMOS devices extremely difficult. The major points of comparison (advantages and disadvantages) between the PZT and SBT based capacitor technologies are:

- PZT based capacitors have larger switchable polarization (40–50 $\mu C/cm^2$) than the polycrystalline SBT-based capacitors (~20 $\mu C/cm^2$) hitherto developed.
- PZT layers with a pure perovskite structure and good electrical properties can be generally produces at lower temperatures (600-700 ^oC) than SBT layers (750-850 ^oC) depending on the particular film deposition technique.
- PZT based capacitors require oxide or hybrid-metal-oxide electrodes technology to yield negligible fatigue and imprint, two important electrical properties for FRAMs. These electrodes are more complicated to synthesize than pure metal electrodes such as Pt.
- PZT based capacitors involve Pb, which may present contamination and hazardous problems during fabrication.
- SBT based capacitors present negligible fatigue and imprint using the simpler Pt electrode technology.
- SBT layers maintain good electrical properties even when they are very thin (< 100 nm).

The major problems to overcome for the realization of a practical high density memory device are:

- SBT based capacitors have lower polarization than PZT based capacitors. Intrinsic high polarization values may be necessary when scaling capacitors to the submicron dimensions needed for these memories. This may be a problem in relation to the application of SBT to high-density memories.
- The synthesis of SBT layers with the appropriate layered perovskite structure requires high temperature (750-800 ^{o}C) depending on the film deposition technique. The processing temperatures are high in relation to standard semiconductor device processing temperatures, as described in Fig. 1-6, and therefore efforts are warranted to reduce it.
- The Curie temperature of SBT is low(~310 ^{o}C). A higher Curie temperature is desired for memory applications as the ferroelectric properties are strongly dependent on the Curie temperature. As the operating temperature approaches the Curie temperature the ferroelectric polarization decreases rapidly. So the Curie temperature is required to be much higher than the operating temperature range to ensure a stable constant polarization.

1.3. OBJECTIVES AND APPROACH TO THE PROBLEMS

The attempt to solve the above problems of SBT includes a new solid solution material which shows excellent properties. The approach also describes a room temperature chemical precursor solution preparation technique developed to process high quality pyrochlore-free crystalline films at a low post-deposition annealing temperature of 650 ^{o}C. The approach and considerations in selecting the proposed new solid solution material and the modified chemical preparation technique to overcome the problems with SBT based capacitor technology are the following:

A. SBT layers with appropriate layered perovskite structure requires high temperatures (750-800 ^{o}C) depending on the film deposition technique. At lower temperatures the films exhibit poor microstructural and ferroelectric properties. The polycrystalline nature of SBT layers in conjunction with the polarization direction of the SBT material may contribute to this effect. Intrinsic high polarization values may be necessary when scaling capacitors to the submicron dimensions needed for these memories. The idea of solid solution material to overcome these

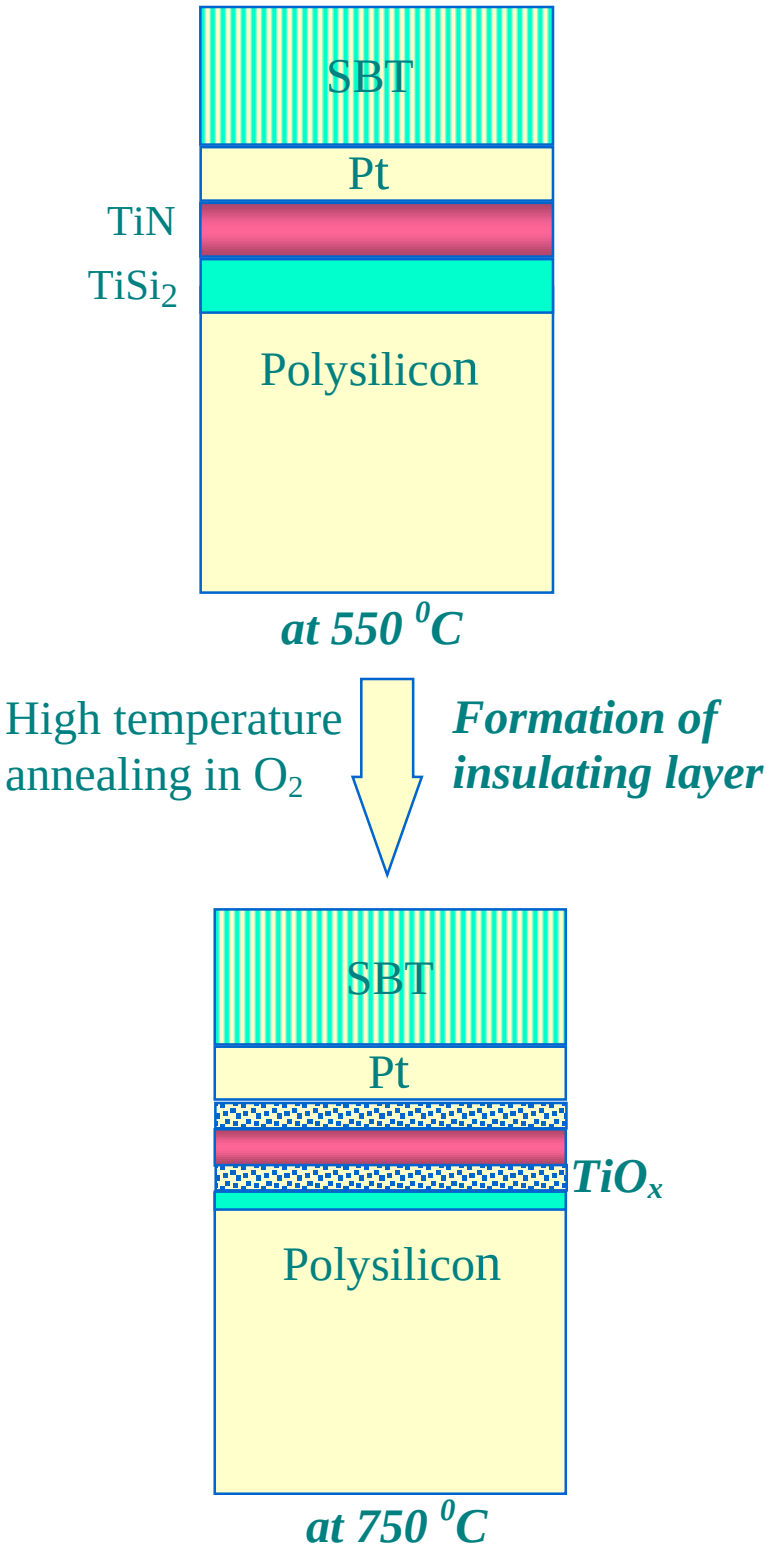

Figure 1-6. Degradation of capacitor structure due to high temperature annealing of ferroelectric thin film

problems is based on the bulk ceramic approach where the properties of a material are modified by making a solid solution with a material having different microstructure and Curie temperature characteristics but similar structure.

B. SBT and Bi_3TaTiO_9 (BTT) or Bi_3TiNbO_9 (BTN) are displacive ferroelectric compounds with layered structures as shown in Fig. 1-7. Some of chemical data are also shown in Table 1-2.

C. SBT has Curie temperature of 310 ^oC while the BTT/BTN has Curie temperature in the range 870-950 ^oC. So the solid solution of these two materials is expected to exhibit a higher Curie temperatures. Also, Curie temperature (T_c) – Saturation polarization (P_s) graph for bismuth layered structure family seems to follow a linear T_c - P_s dependence[18]. As shown in Fig. 1-8, a linear equation between T_c and P_s is fitted to the experimental data which results.

$$T_c = a + b\,(P_s) \qquad (1.3)$$

where a and b are fitting parameters. Therefore, the resulting solid solution of SBT and BTT/BTN is expected to have a higher polarization values. In addition, the intrinsic values of saturation polarization (P_s) for SBT bulk material is about 5.8 $\mu C/cm^2$ while a P_s value of 27.7 $\mu C/cm^2$ has been reported for BTN material[19]. So this is another physical fact which makes us to expect higher polarization after solid solution of those two materials.

D. It is not possible to reduce the post-deposition annealing temperature due to poor ferroelectric properties at lower annealing temperatures. This problem is intrinsic in nature and is due to small grain sizes at lower annealing temperatures[20]. The idea of solid solution may decrease the melting temperature range, hence increase atomic mobility of each species in the system. So the solid solution is expected to yield larger grain sizes at lower annealing temperature compared to SBT and hence solve the problem of reducing the processing temperature.

1.4. PRESENTATION OF RESULTS

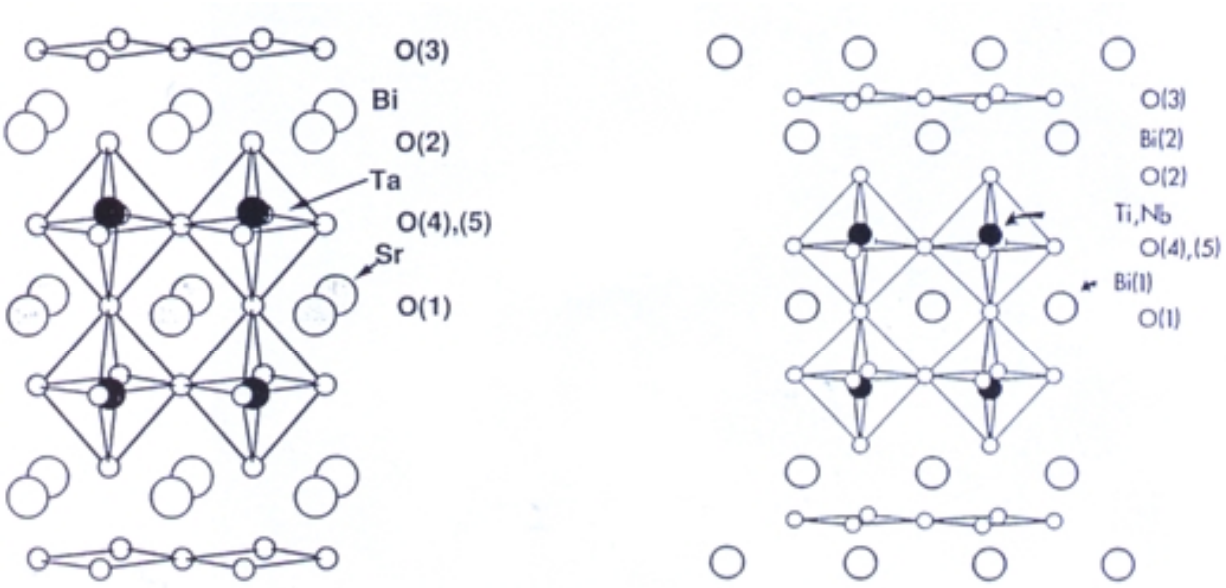

Figure 1-7. SBT and BTN crystal structures [21,22]

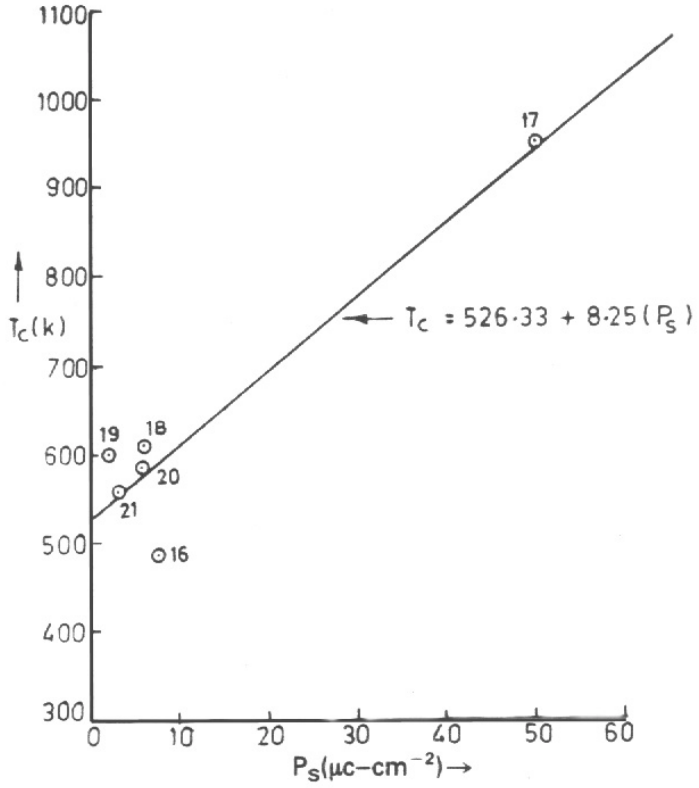

Figure 1-8. Curie temperature(T_c) and Polarization(P_s) dependence for bismuth layered family
16: (BaSr)$Bi_2Ta_2O_9$, 17: $Bi_4Ti_3O_{12}$, 18: $SrBi_2Ta_2O_9$, 19: $Ba_2Bi_4Ti_5O_{18}$
20: $Pb_2Bi_4Ti_5O_{18}$, 21: $Sr_2Bi_4Ti_5O_{18}$, after ref. [18]

Table 1-2 Crystallinity and Chemistry Data of $SrBi_2Ta_2O_9$ and Bi_3TaTiO_9

Materials	Crystal Type*	Lattice Parameters* (Å)				Ionic Radius** (Å)				
		a	*b*	*c*	Z	Sr^{+2}	Bi^{+3}	Ta^{+5}	Ti^{+4}	Nb^{+5}
$SrBi_2Ta_2O_9$	Orthorhombic	5.5306	5.5344	24.9839	4	11.3	11.6	0.66		
Bi_3TiNbO_9	Orthorhombic	5.4398	5.3941	25.0990	4		11.6		0.68	0.70

* after reference [21,22]

** after reference [23]

Chapter 2 presents the experimental details of a synthesis of the $SrBi_2Ta_2O_9$ and the (1-x)$SrBi_2Ta_2O_9$-xBi_3TaTiO_9 thin film materials. The selection of starting materials, the synthesis of precursor solution and the detailed procedure of making thin films are discussed. Also, some of the representative results are exhibited. Chapter 3 presents the optimization process of ferroelectric (1-x)$SrBi_2Ta_2O_9$-xBi_3TaTiO_9 thin films. Among the various compositional (1-x)$SrBi_2Ta_2O_9$-xBi_3TaTiO_9 thin films, the ferroelectric and electrical properties of the films as a function of x are studied and one composition, which turned out to be 0.7$SrBi_2Ta_2O_9$-0.3Bi_3TaTiO_9 composition, is chosen as the most suitable for the application of FRAM. Also, some representative properties of films made of the chosen composition (1-x)$SrBi_2Ta_2O_9$-xBi_3TaTiO_9 are presented and discussed. Chapter 4 presents the dependence of properties on thickness and temperature of 0.7$SrBi_2Ta_2O_9$-0.3Bi_3TaTiO_9 thin film dependent on its thickness and operating temperatures. In the chapter, possible growth mechanism of the solid solution thin films and grain size relationship with its ferroelectricity are discussed. Also, the thermal stability of 0.7$SrBi_2Ta_2O_9$-0.3Bi_3TaTiO_9 thin film is discussed by comparing its properties with $SrBi_2Ta_2O_9$ and Pb(Zr.Ti)O_3 thin film. Chapter 5 presents electrical conduction mechanism of ferroelectric thin films. The main focus of this chapter is made on the effect of ferroelectric polarization on its electrical conduction behavior. Finally, in the chapter 6, the 0.7$SrBi_2Ta_2O_9$-0.3Bi_3TaTiO_9 thin film is integrated on the memory cell using oxide electrode/barrier for its high density memory applications. The functional properties are investigated on the emphasis of the electrical contact of the films on the memory cell.

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