Design and Development of High Density High Temperature Power Module with Cooling System

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Abstract

In recent years, the SiC power semiconductor has emerged as an attractive alternative that pushes the limitations of junction temperature, power rating, and switching frequency of Si devices. These advanced properties will lead converters to higher power density. However, the reliability of the SiC semiconductor is still under investigation, and at the same time, the standard Si device packages do not meet the requirement of high temperature operation. In order to take full advantage of SiC semiconductor devices, high density, high temperature device packaging needs to be developed.

In this dissertation, a high temperature wirebond package for multi-chip phase-leg power module using SiC devices was designed, developed, fabricated and tested. The details of the material selection and thermo-mechanical reliability evaluation are described. High temperature power test shows that the presented package can perform well at the high junction temperature.

In order to increase the power density, reduce the parasitic parameters, and enhance the electrical, thermo-mechanical performance over wirebond packages, planar package is utilized to better take advantages of SiC device. This dissertation proposed a novel package, in which the interconnections can be formed on small dimensional pads and

enclosed pads that may baffle the regular solder based connection in other planar packages. Electrical and thermo-mechanical tests of the prototype module demonstrate the functionality and reliability of the presented planar packaging methodology.

In this dissertation, together with the design example, the manual module layout design and automatic module layout design process are also presented. Furthermore, a systematic optimal design process and parametric study of the heatsink-fan cooling system by applying the analytical model is described. This dissertation also established a systematic testing procedure which can rapidly detect defects and reduce the risk in high temperature packaging testing. Finally, a wirebond module and a planar module are designed for 175 ºC junction temperature and 250 ºC junction temperatures. All the key concepts and ideas developed in this work are implemented in the prototype module development and then verified by the experimental results.

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Chapter 1 Introduction

1.1 Motivation and Strategy

Power electronics, as defined by Thomas G. Wilson [1], is: "The technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form." The goal of power electronics is to realize power conversion from an electrical source to an electrical load in a highly efficient, highly reliable and cost-effective way.

Over the last twenty years, industrial and research efforts in electronic power conversion have been making the move toward high power density, which results in great improvement of the converter system performance, miniaturization of the physical size, and reduction of mass, weight and cost [3]. This is pushing the limits of existing control, packaging and thermal management technology for power converter systems. In order to better understand high power density converter design, it is highly important to analyze each of the components composing the converter system.

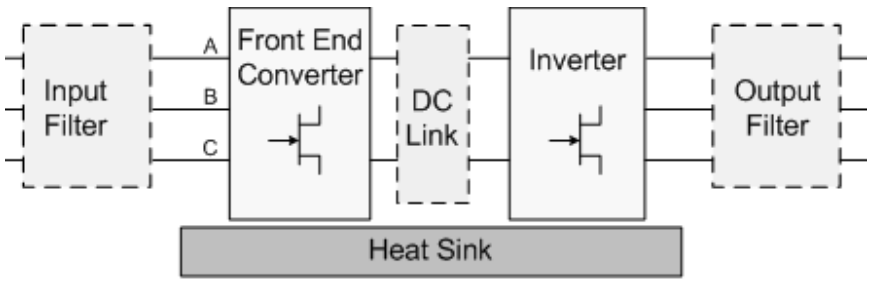


Figure 1-1. Typical three-phase AC-AC converter system.

Figure 1-1 shows a typical three-phase AC-AC converter system, which includes an input filter, a front end converter, a DC link, an inverter, an output filter and a cooling system. The front end converter and inverter are usually composed of active devices, while the filters and DC bus are mainly passive components. In the converter system design, since it is difficult to account for the air volume in each component, the weight of the components can more accurately reflect the real power density [4]. According to the literature [4, 5], the largest weight contributors are passive components and the cooling system. Because the cooling system is mainly designed based on the power loss of the active components, the design of the cooling system and the design of the active components should be considered together [4]. This report focuses on the reduction of the total weight of the active components as well as the cooling system.

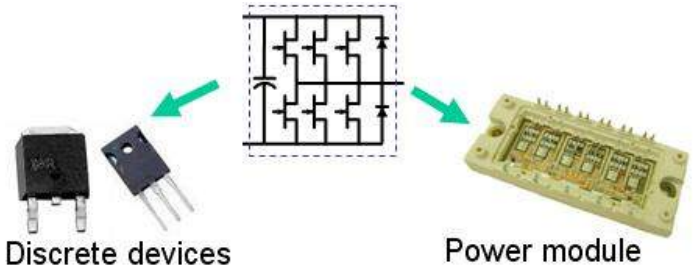


Figure 1-2. Active components.

As illustrated in Figure 1-2, in a converter system, active components can utilize discrete devices or power modules. A power electronics module can be defined as a packaging strategy that allows a single or multiple power devices to be packaged together in a single insulated structure with improved thermal performance and reliability. The power electronics module can include all or part of the control system, the protection system and the sensing system in the

structure [6]. Since the power module is the key unit [6-8] in weight reduction, this report presents the development of a high-density, high-temperature power module with a cooling system.

There are four ways to reduce the total weight of the power module and cooling system (shown in Figure 1-3). The first way is advanced thermal design; a well-designed cooling system can always achieve a smaller weight. The second way is packaging design, which demands solutions to the challenges of reducing the packaging parasitic capacitance and inductance, as well as an efficient dissipation of heat. The third way to reduce the total weight is increasing the junction temperature, and the last method is reducing the total power loss. The last two methods can increase the thermal resistance and thus directly reduce the required heat dissipation area, which usually results in the reduction of cooling system weight [9].

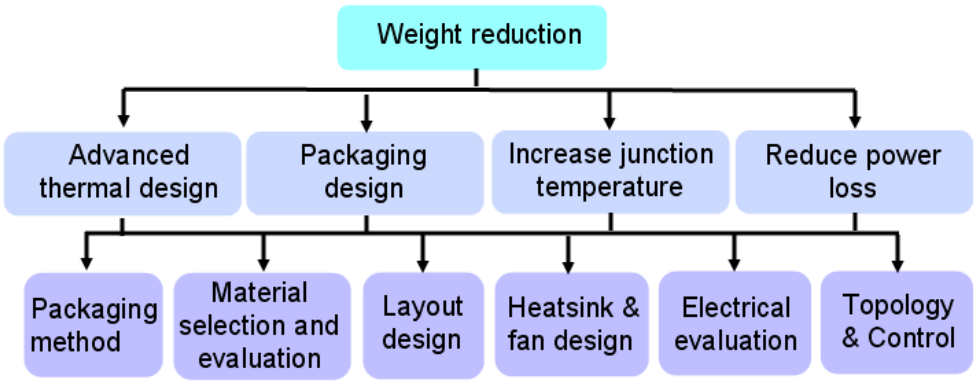


Figure 1-3. Some weight reduction strategies.

By considering the four methods listed above, the drive to increase the power density has put increasing pressure to create a more detailed design process, which includes improving the packaging method, material selection and evaluation, power module layout design, heatsink and

fan design, safe and fast electrical evaluation procedure, circuit topology selection, and control strategy selection. These detailed design strategies need to be considered from the electrical, thermal and mechanical design domains [10].

It is expected that breakthrough gains in power conversion density and thermal management in the near future will come from emerging packaging technologies, such as chip-scale and three-dimensional packaging [11]. Innovative interconnect techniques will revolutionize the traditional packaging methodology, bringing about the important benefits of lower interconnect resistance, less noise and parasitic oscillations, improved reliability, better thermal management, and a higher level of system integration of power devices [12].

It is also predicted that the power electronics implemented within the modules will have higher maximum operating temperatures in the near future [13]. However, the standard silicon-based packaging cannot support the higher junction temperature operation [14]. Power modules with advanced material technologies are required to implement the converters for high-temperature operation and for high thermo-mechanical reliability during large temperature excursions.

Another major concern in the design of a power module is the parasitic parameters in series with the power devices. This causes voltage overshoot, increasing the blocking voltage requirements of the power devices and increasing the devices' switching losses [15]. Thus, the layout of power modules is one of the key points in power module design, especially for high power densities, where couplings are increased [16].

In high power density design, it is also necessary to minimize the weight of the cooling system for a given maximum tolerable thermal resistance. Moffat [17] claims that the flow and heat transfer situations encountered in electronics cooling applications are much more challenging than those in heat exchangers, and are as complex as those encountered in gas turbine blade cooling. It is critical to identify a thermal-fluid model which can predict the heat transfer rate in the cooling system to reduce the total weight. Based on the model, the total weight can be minimized to raise the power density. Additionally, unlike conventional package technologies, novel materials and advanced packaging method always bring uncertainty in the power module electrical evaluation process [18]. This means that the potential defects need to be detected in the newly developed module before operation at the rated power. In order to quickly and safely detect the defects without destroying the whole power module, particularly the multi-chip module, a standardized electrical evaluation procedure is essential.

Converter system design also clearly depends on the converter circuit topology and control strategy [4]. In order to achieve a high-density design, it is a logical and necessary step to carry out systematic design and evaluation for the circuit topologies and the control strategy that meet the application requirements, and to select from among them the most suitable candidate.

The detailed designs above are tightly interconnected, and any change in one design may have consequences for the others. However, the elements of a detailed design process can still be decoupled from each other, especially the design methodology. In order to obtain high power density, each design must be optimized for the individual design specifications. This report focuses on the first five detailed designs for high density application.

1.2 Challenges and Objectives

In recent years, the silicon carbide (SiC) power semiconductor has emerged as an attractive alternative that pushes the limitations of Si devices [19, 20], as shown in Figure 1-4. SiC-based power converters have the potential for reliable operation at higher junction temperature, higher frequency and higher power density than can be achieved with silicon (Si) transistor technology. This indicates that a SiC technology-based converter system can be made smaller and more efficient. It has been estimated that there is a potential for up to a five-fold reduction in converter volume if high-temperature, high-frequency power electronics can be implemented with SiC. However, the reliability of the SiC semiconductor is still under investigation, but at the same time, the standard Si device packages do not meet the requirement of high temperature operation [21].

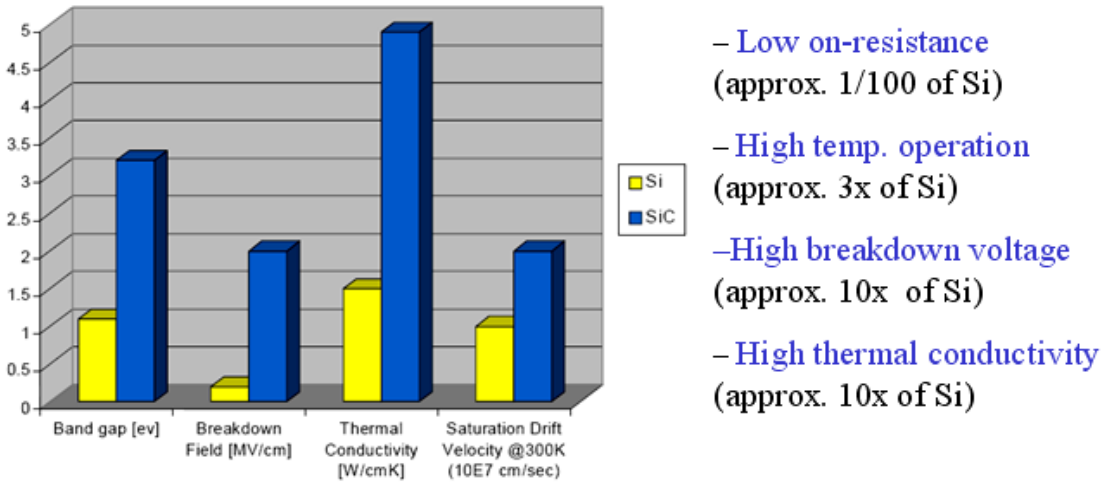


Figure 1-4. Comparison between Si and SiC semiconductor devices.

In order to take full advantages of SiC devices, researchers have put their focus on the power module packaging for high temperatures. The benchmark research is listed in Table 1-1. In [22-

25], the authors have designed, developed, packaged, and manufactured a complete multi-chip power module (MCPM) that integrates SiC power transistors with silicon-on-insulator (SOI) control electronics. A SiC JFET based three-phase inverter that was fully tested to 4 kW at 300 ºC operation. However, there were still thermo-mechanical reliability issues with the encapsulant. Reference [26] presents a 100 V, 25 W dc-dc converter using a SiC JFET and a SiC diode. The converter was designed and built in accordance with the static characteristics of the SiC devices under extremely high ambient temperatures, and then tested up to an ambient temperature of 400 ºC. In [27], design, operation, and performance evaluation of a 180 W, 100 kHz, 270 V/28 V dc-dc power converter was reported for elevated temperatures up to 200 ºC. The use of SiC power semiconductor devices and high-temperature passives are presented as well. In [28], the 600V GaN HFET was operated in a 225 ºC environment temperature. In [29], the discrete SiC JFET device was reported to operate with 300 kHz in the 300 ºC environment.

Table 1-1 Work on SiC High Temperature Power Module Development

Researcher	Material selection	Packaging design	Reliability evaluation	Thermal design	Electrical evaluation
APEI SiC JFET [22-25]	Some details, some implicit	Some details, some implicit	Some results with inexplicit analysis	Implicit	Low power at first, then 4 kW in 300ºC
Kyoto Univ. SiC JFET [26]	Some details, some implicit	Undemonstrated	Undemonstrated	Undemonstrated	25 W in 450ºC
Air Force Lab. SiC BJT [27]	Some details, some implicit	Undemonstrated	Undemonstrated	Undemonstrated	180 W in 250ºC
Furukawa Electric. GaN HFET [28]	Detailed selection	Undemonstrated	Detailed results for aging test	Undemonstrated	Inexplicit test in 225ºC
Lyon Lab. SiC JFET [29]	Discrete device	Undemonstrated	undemonstrated	Undemonstrated	Double pulse first, 150W in 300ºC

This dissertation	Detailed selection	Detailed wirbond and planar design	Experiment and simulation, acceptable lifetime	Formula based thermal model and optimization	Multi-chip phase-leg module in 250ºC

In most of these research projects, the test and evaluation procedure and methodology for the package supporting SiC devices are either not explicit described or are inadequate. References [30-31] show high-temperature packaging design in terms of material selection. However, there is not enough experimental data on high junction temperature operation and thermo-mechanical reliability evaluation for assemblies. Thus, further investigation of thermo-mechanical reliability for materials and assemblies is still required.

Furthermore, the layout design of the power module and thermal management design have also not been clearly discussed, perhaps because these papers did not focus on power loss reduction and high density design yet. Although all these papers show the rated power testing results, they still lack the detailed electrical evaluation process, as well as potential defect detection methods.

Therefore, the objective of this dissertation is to develop a systematic methodology for a high-density, high-temperature power module together with the cooling system. It requirements the combination of high temperature packaging technology, module layout design, cooling system design and electrical evaluation. Thus in this dissertation, high temperature wirebond package and high temperature planar package are first developed to withstand high temperature operation (in this report 250 ºC) and large temperature excursions (in this report from -55 ºC to 250 ºC). In addition, the layout design and thermal management design are investigated to reduce the power

loss and increase the power density. Moreover, a safe and rapid electrical evaluation procedure is also presented.

1.3 Organization of Dissertation

Corresponding to the challenges discussed above, the organization of this dissertation is listed as below.

Chapter 2 investigates materials selection and comparison to ensure the full package can function reliably at 250 ºC based on wirebond package. The thermo-mechanical reliability of substrate was evaluated and several methods were investigated to improve the lifetime. Sealing the stepped edge DBC method is utilized to improve on substrate reliability under large temperature excursion. The promising results of thermal cycling test on die-attachment and wirebond assemblies prove that the proposed package can perform well for large temperature excursion.

Chapter 3 presents the development of a phase-leg power module packaged by a novel planar packaging technique for high-temperature (250 ºC) operation. Sintered silver is chosen as the die-attach material as well as playing the key functions of electrically connecting the devices' pads. No significant changes (<5%) are found in the characterization of SiC devices before and after packaging. Thermo-mechanical reliability has also been investigated by passive cycling the module from -55 ºC to 250 ºC. Electrical and mechanical performances of the packaged module are characterized and considered to be reliable for at least 300 cycles.

Chapter 4 presented the layout design of high power density power module. Some practical considerations are introduced for the optimization of electrical performance of the module. Together with the design example, the manual design and automatic design process are presented separately. The design example shows that the automatic design procedure could be a major step to improve the overall performance for future layout design.

Chapter 5 investigates the geometry of the heatsink and the operating point of a fan the thermal performance in the force-air cooling system. An analytical model has been developed for predicting the heatsink-fan system performance. Detailed optimization procedure to minimize the total weight is presented. A typical mathematical optimization example is presented, and the results are verified via numerical simulations and experiments.

Chapter 6 presents a safe and rapid electrical evaluation procedure. The potential defects in design and fabrication procedure are detailed and their detection steps in the electrical evaluation are introduced. The established systematic testing procedure can rapidly detect defects and reduce the risk in high temperature packaging testing. The multi-chip module development procedure is also presented and demonstrated with an example.

Chapter 7 presents the high density design case based on the high density high temperature packaging technology in chapter 2 to chapter 6. Wirebond package module and planar package modules with forced air cooling system are designed for both 175 ºC junction temperature and 250 ºC junction temperature. Prototype power modules are also electrically evaluated to demonstrate the development procedure.

The dissertation is concluded in Chapter 8, which summaries the most important conclusions. Recommendations for future research on the subject are also made.

Chapter 2 Development of High-Temperature Wirebond Package

Progress in the development of SiC semiconductor has shown a strong potential to enhance the performance and improve the reliability of devices for operation in high temperatures and other harsh environments. However, the lack of a durable high temperature packaging technology is a major impediment to the implementation of SiC-based power module for high temperature applications. In this chapter, the conventional wirebond package is utilized for high temperature package technology. The details of the material comparison and selection are described, culminating a feasible solution for high temperature operation. Thermal cycling test with large temperature excursion (from -55ºC to 250ºC) was carried out to evaluate the thermo-mechanical reliability of the package. In order to analysis the lifetime improvement of DBC substrate, FEA simulation tool ANSYS is utilized to simulate the peeling stress and results agree well with experimental results.

2.1 Material Selection for Wirebond Package

In order to select materials for high temperature operation, the conventional wire-bond structure is illustrated in Figure 2-1.

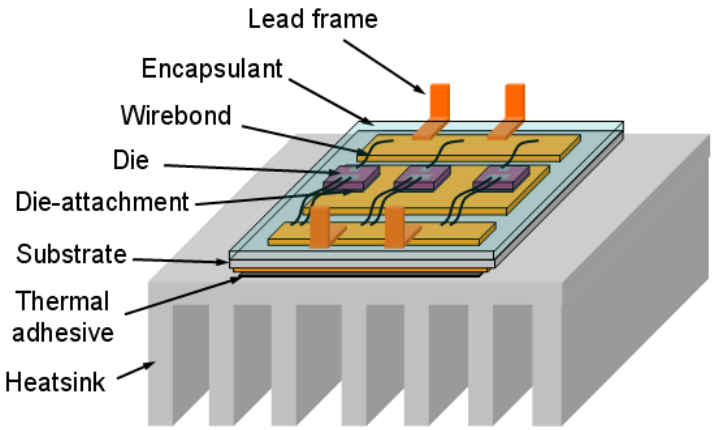


Figure 2-1. Wirebond packaging conceptual illustration.

It is crucial to identify which materials can be utilized or improved for the high temperature operation. Based on a comprehensive survey [14] and lab evaluation, the materials for each part of the power module package are compared and selected. The finally selected materials for each part are listed in Table 2-1.

Table 2-1 Material selection list

Switch	1200 V, 3 mm × 3 mm from SiCED
Diode	1200 V, 2.7 mm × 2.7 mm from SiCED
Substrate	Aluminum Nitride (AlN) Direct Bond Copper (DBC) with 25 mils thick AlN, 8 mils thick Copper
Die-attachment	Au-Ge solder (360 ºC melting point)
Wirebond	5 mils Aluminum wire for gate pads on JFET dies; 10 mils Aluminum wire for other pads
Encapsulant	Nusil R-2188
Lead frame	8 mils thick copper stripe

As shown in Table 2-2, for the 1200V high temperature power switch, there are three choices, which are SiC JFET, SiC MOSFET and SiC BJT. The SiC JFET includes normally-on device (From SiCed) and normally-off device (from SemiSouth). From the

literature [26], normally-on SiC JFET already been tested up to 450 ºC and there are several gate drive design scheme can be learned. The vital issue is the normally-on SiC JFET will cause problem when the gate signal lost or effected by noise. The normally-off SiC JFET may have the gate drive challenge because the gate threshold voltage is less than 3 V [32]. At the same time, the high temperature reliability of normally-off SiC JFET is still uncertain. SiC MOSFET is normally-off device and is produced by CREE. From the literature, so far the SiC MOSFET from CREE was tested less than 200 ºC [32]. The SiC BJT is normally-off device but requires proportional gate drive which will bring in large power loss. Finally, considering the application requirement, device characteristics and availability, 1200 V SiC JFET and diodes are selected. The dimension of SiC diode and SiC JFET are shown in Figure 2-2 and Figure 2-3.

Table 2-2 Candidates of SiC Switch

Vendor	Device	Gate-drive characteristics	Recommended temperature	Device rating
SiCed	JFET	Normally-on	200ºC~500 ºC	1200 V, 5 A
CREE	MOSFET	Normally-off	150ºC~200 ºC	1200 V, 10 A
Semisouth	JFET	Normally-off	150ºC~200 ºC	1200 V,15 A
United silicon carbide	BJT	Normally-off	150ºC~250 ºC	1200 V, 10A

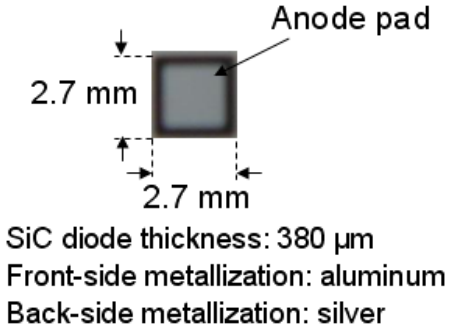


Figure 2-2. Dimensions of SiC diode die from SiCed.

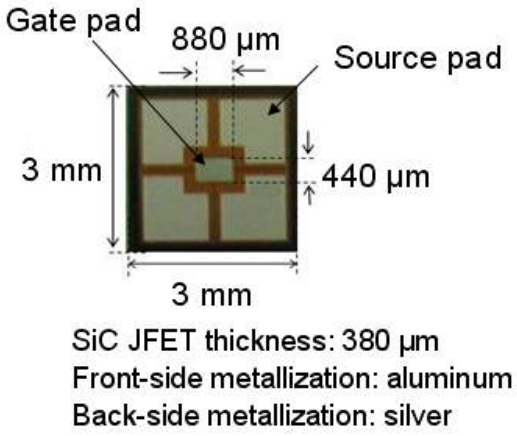


Figure 2-3. Dimensions of SiC JFET die from SiCed.

For the substrate, the first attempt was focused on the AlN DBC. From the literature survey, it was found that the coefficient of thermal expansion (CTE) of AlN DBC matches well with that of the SiC, and its other physical characteristics are average but adequate for 250 ºC operation. The properties of candidates of DBC substrate are listed in Table 2-3. The metallization of the DBC is electroplated Ni and Au, which can prevent the oxidation of the bare copper and improve the thermal reliability.

Table 2-3 Candidates of DBC Substrate

Insulation layout in substrate	CTE (ppm/ºC)	Thermal conductivity (W/m/K)	Dielectric strength (kV/mm)	Tensile strength (MPa)	Dielectric constant at 1 MHz
Al_2O_3	7.2	33	12	127	9.9
AlN	4.6	150	15	310	8.9
Si_3N_4	3.0	70	10	96	6.7
BeO	7.0	270	12	230	6.0

For the die-attachment, 95%Pb-5%Sn solder, 80%Au-20%Sn, 80%Au-20%Ge and Hysol QMI 3555 silver glass were preliminarily selected and investigated [14] . The properties of candidates of die-attachment are listed in Table 2-4. However some of them showed disappointing performance. The Hysol dries too fast once exposed to air,

rendering the die-attach procedure awkward. The solderability of 95%Pb 5%Sn is relatively poor and it is too weak to support the pressure applied to the connection. 80%Au-20%Sn has a relatively low melting temperature (280 °C), which is too close to the targeted junction temperature. Especially, when the quality of the solder is poor, the large resistance may easily result in local over heating and thus speed up the melting of the solder.

Table 2-4 Candidates of Die-Attachment

Die-attachment	Processing temperature (ºC)	Melting temperature (ºC)	Thermal conductivity (W/m/K)	Electrical resistivity ($\times 10^{-6}$ Ω•cm)
95%Pb-5%Sn solder	350	310	32	20
80%Au-20%Sn	320	280	57	17
80%Au-20%Ge	390	360	88	30
Hysol QMI 3555	400	900	40	54
Sintered silver	275	900	240	63

In the material selection process, Au-Sn solder was tried in the prototype module with inadequate performance results. By checking the soldering quality after the prototype module failed, it was found that the Au-Sn solder melted during the continuous power test that supposed to maintain the device junction temperature at 250 ºC. The failure was attributed largely to inaccurate temperature control such that the actual temperature at certain spots exceeded the Au-Sn solder melting temperature. Considering the imperfection of both temperature control and processing, Au-Sn was deemed a marginal choice for the selected junction temperature of 250 ºC. Finally, 80%Au-20%Ge was chosen as the die-attachment because of its good solderability, good mechanical

performance and suitable melting temperature (360 °C). The die shear test also showed an advanced bonding stress, which is shown in Section III. The reflow profile of 80%Au-20%Ge solder is shown in Figure 2-4.

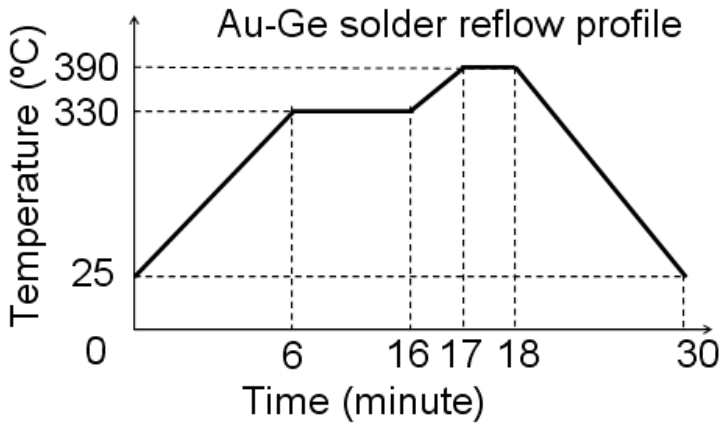


Figure 2-4. Reflow profile of Au-Ge solder.

Aluminum wires were selected for their maturity and reliable, repeatable bonding processing. Aluminum wires are bonded between the top aluminum metallization of the SiC device surface and the DBC by ultrasonic wedge bonding. Because the gate pad of the JFET is very small and easily damaged during the wire bonding process, 5 mils wire is chosen for the gate pads and the 10 mil wire is chosen for other pads. The settings of wirebonding machine are listed in Table 2-5.

Table 2-5 Settings of Wirebonding Machine

Wirebonding machine: Orthodyne M20B	Wirebonding 5 mil aluminum wire	First bonding time (ms)	2
		First bonding power (mW)	90
		Second bonding time (ms)	4
		Second bonding power (mW)	100
	Wirebonding 10 mil aluminum wire	First bonding time (ms)	4
		First bonding power (mW)	250
		Second bonding time (ms)	8
		Second bonding power (mW)	280

Because of the good electrical and thermal property and stability, Nusil R-2188 was selected to coat over the components and to protect the die against mechanical stress, dust and aerial discharge around die edges. Nusil R2188 is also easily repairable, non-corrosive, flame retardant, reversing resistant and has a low shrinkage [34]. The properties is listed in Table 2-6 and the curing profile is shown in Figure 2-5.

Table 2-6 Properties of Nusil R-2188

Durometer	Tensile strength	Elongation	Dielectric strength	Volume Resistivity
20	3.3 MPa	350 %	17.7 kV/mm	1×10^{13} Ω•cm

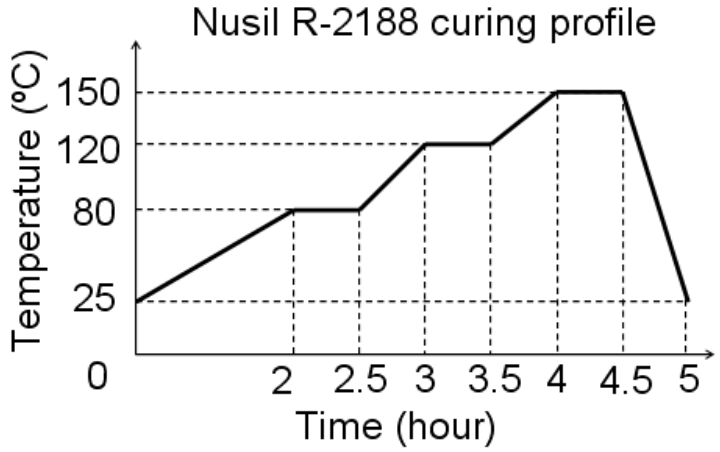


Figure 2-5. Curing profile of Nusil R-2188.

The gold plated 8 mil thick copper stripe is selected for the external connections. With the simplicity and the flexibility, it is considered better than the pin and terminal blocks from the mechanical point of view. The copper strip can also be made as the lead frame, which can be soldered to the substrate at the same time when soldering the devices. The vendors of materials in wirebond package are listed in Table 2-7.

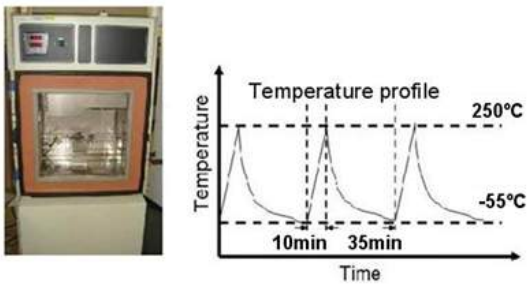
Table 2-7 Vendors of Materials in Wirebond Package

Material	SiC JFET SiC diode	Al_2O_3 DBC AlN DBC	Au-Ge solder	10 mils wire 5 mils wire	Nusil R-2188
Vendor	SiCed	Curamik	ArraySolder	Harill Aluminum	Nusil Silicone technology
Material	Epo-tek 600	Duralco 132	Heatsink		
Vendor	Epoxy technology	Cotronics	Thermaflow		

2.2 Thermo-Mechanical Reliability of Wirebond Package

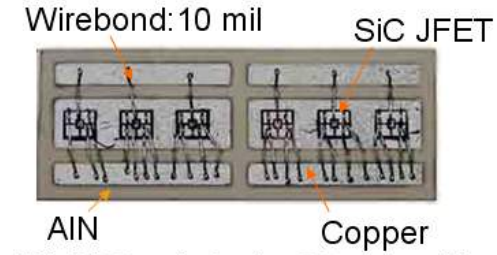
2.2.1 Thermo-mechanical Reliability of Wirebond Assembly

In order to investigate the thermal reliability of the selected materials, assemblies are fabricated including substrate, die-attachment, device and wirebonds. Six SiC JFET mechanical samples were soldered and wirebonded to the AlN DBC (33 mm × 17 mm), which is named as group A samples and shown in Figure 2-7. Three assemblies were fabricated for thermal cycling test. As shown in Table 2-8, with the help of laser cutting machine and etching machine, the DBC substrate is patterned. Then SiC JFET samples were soldered to DBC substrate with reflow process. Finally wirebonds were formed from pads of dies to traces of DBC substrate.



Thermal-cycling chamber: Tenney TUJR
Cycling capability: -70°C~300°C
Heating rate: <30°C/min
Cooling rate: <12°C/min

Figure 2-6. Thermal-cycling chamber and profile.



AlN DBC substrate: 30 mm × 17 mm
Copper thickness: 8 mil
AlN thickness: 25 mil
SiC JFET: 3 mm × 3 mm × 380 μm

Figure 2-7. Group A sample.

Table 2-8 Fabrication Procedure and Settings for Group A Samples

Machine	Processing	Settings	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting AlN	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	50
		Pulse number	2300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Vacuum reflow machine: SST	Reflowing Au-Ge	Temperature profile	Shown in Figure 2-4

MV-2200	solder		
Wirebonding machine: Orthodyne M20B	Wirebonding 5 mil aluminum wire	First bonding time (ms)	2
		First bonding power (mW)	90
		Second bonding time (ms)	4
		Second bonding power (mW)	100
	Wirebonding 10 mil aluminum wire	First bonding time (ms)	4
		First bonding power (mW)	250
		Second bonding time (ms)	8
		Second bonding power (mW)	280

Assemblies were put into the Tenney environmental chamber. As shown in Figure 2-6, the cycling profile was from -55 °C to 250 °C and each cycle takes about 45 minutes. Just after 20 cycles, copper on the substrates began to peeling off while the rest of the packaging parts visually look good, as shown in Figure 2-8. The failure results of samples are listed in Table 2-9.

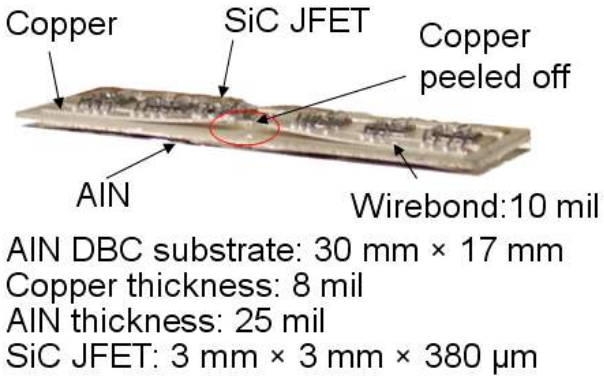


Figure 2-8. Failed group A sample.

Table 2-9 Thermal-Cycling Results of Group A Samples

Samples	Dimensions	Life time
Sample A1	30 mm ×17 mm	20 cycles
Sample A2	30 mm ×17 mm	20 cycles
Sample A3	30 mm ×17 mm	20 cycles

As described in [34], heat soaking tests were also performed in the 250 ºC ambient. The same assemblies used in thermal cycling test were put in the soaking chamber and

kept running for 300 hours. The die-shear results showed no significant degradation during the heat soaking process.

Based on the thermal cycling and heat soaking test, it can be concluded that the selected substrate materials cannot survive large temperature excursion, though they can be used at high temperature. As a result, efforts were put in the investigation on more reliable substrate, die-attachment and wirebond assemblies for large temperature excursion as to be described below.

2.2.2 Thermo-mechanical Reliability of Substrate

From [35][36], it can be learned that stepped edge, dimples or tailed edge can increase the thermal reliability because the peeling stress in the edge and corner of the substrate can be relieved considerably. The definitions of dimensions of DBC substrate in this investigation are shown in Figure 2-9.

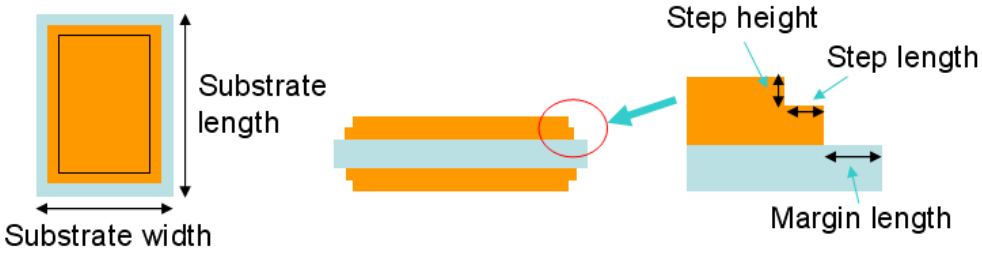


Figure 2-9. Definition of dimensions of DBC substrate.

By using the twice etching, the stepped edge can be formed to the edge of the DBC copper layer. These stepped edged samples were fabricated as shown in Figure 2-10and named as group B samples. As shown in Table 2-10, with the help of laser cutting

machine and etching machine, the DBC substrate is patterned. With the help of Kapton tape, the steps were formed with etching machine with extra 10 minutes etching. Group B samples were cycled with the same temperature profile in Figure 2-6. After 45 cycles the copper began to peeling off from the AlN ceramic layer as shown in Figure 2-11. The lifetime of group B samples is listed in Table 2-11.

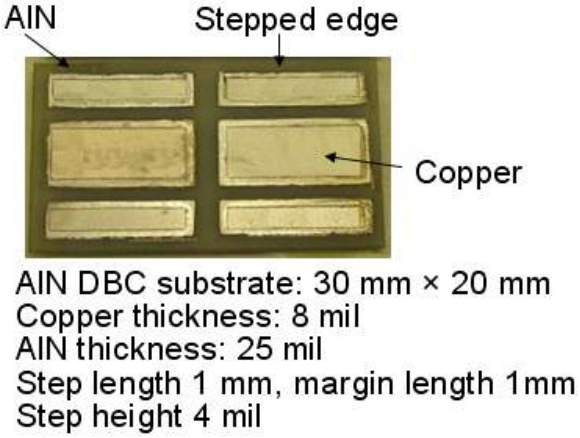


Figure 2-10. Group B sample.

Table 2-10 Fabrication Procedure and Settings for Group B Samples

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting AlN	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	50
		Pulse number	2300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
		Etching time for 4 mil copper (minute)	10

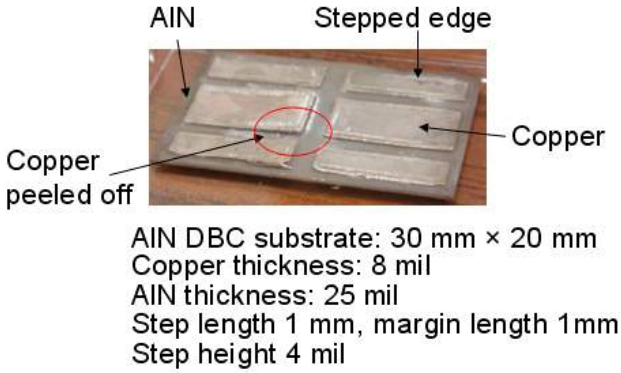


Figure 2-11. Failed group B samples results.

Table 2-11 Thermal-Cycling Results of Group B Samples

Samples	Dimensions	Life time
Sample B1	20 mm ×30 mm	45 cycles
Sample B2	20 mm ×30 mm	45 cycles
Sample B3	20 mm ×30 mm	45 cycles

In [37], the original DBC substrate survives about 1000 thermal cycles in the similar temperature profile due to the small dimensions (6 mm × 6 mm). However, this limited substrate size is difficult to be utilized in the multi-chip high power module. DBA (Direct Bond Aluminum) is another choice for high temperature operation and large temperature excursion. However, as described in [36], the surface roughness of the DBA will become a serious issue when the cycling number increases. [38] proposed another method to improve the thermal reliability of DBC substrate by covering a CTE matching encapsulant layer. Similar to this idea, in this investigation sealing materials were utilized to seal and strengthen the edges of DBC substrate. The fabrication concept is demonstrated in Figure 2-12.

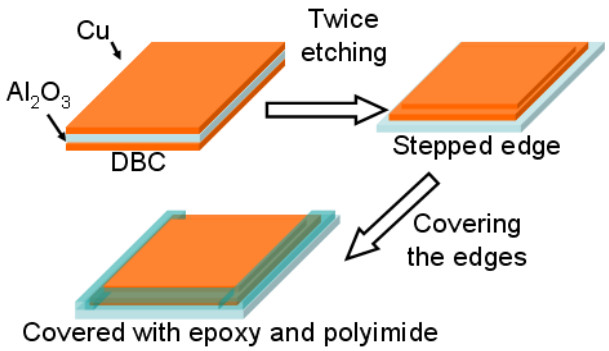


Figure 2-12. Sealed-stepped-edge DBC substrate.

For cost reasons, it was determined that Al_2O_3, with its similar thermo-mechanical properties as those of AlN, can be first used as substrate for concept demonstration. Two candidates of sealing material, Epo-tek 600 and Duralco 132 were investigated. Their properties are shown in Table 2-12 and their curing profiles are shown in Figure 2-13 and Figure 2-14.They were chosen because of their superior thermal, electrical and mechanical features.

Table 2-12 Properties of Epo-tek 600 and Duralco 132

Insulation layout in substrate	CTE (ppm/ºC)	Thermal conductivity (W/m/K)	Dielectric strength (kV/mm)	Curing temperature (ºC)	Operation temperature (ºC)
Epo-tek 600	17.2	5	18	200	<400
Duralco 132	18.3	24	15	150	<240

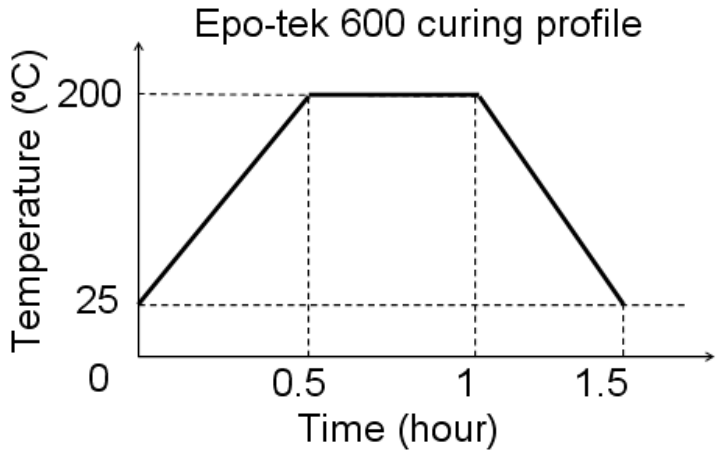


Figure 2-13. Epo-tek 600 curing profile.

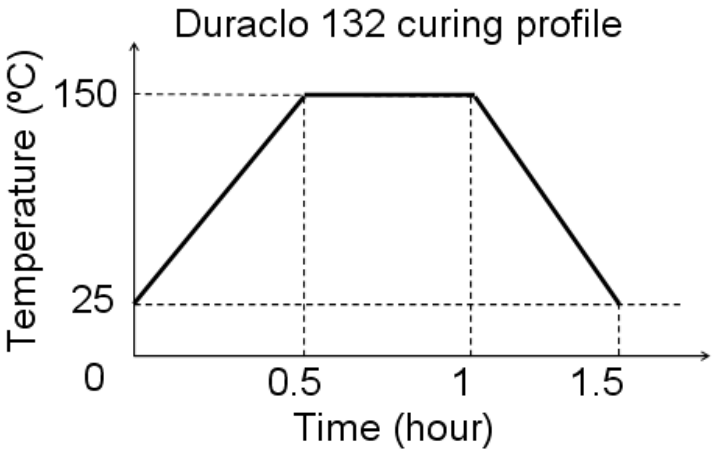


Figure 2-14. Duraclo 132 curing profile.

First, the sealing materials were applied to the DBC without stepped edge (samples shown in Figure 2-15), which is named as group C samples. As shown in Table 2-12, with the help of laser cutting machine and etching machine, the DBC substrate is patterned. Then Epo-tek 600 was dispensed to DBC substrate manually. As shown in Figure 2-16, the group C samples failed at about 60 cycles and the lifetime of group C samples is listed in Table 2-14.

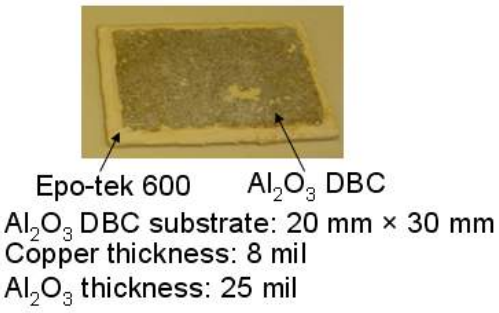


Figure 2-15. Group C sample.

Table 2-13 Fabrication Procedure and Settings of Group C Value

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting AlN	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	50
		Pulse number	2300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
		Etching time for 4 mil copper (minute)	10
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Curing profile	Shown in figure 2-13

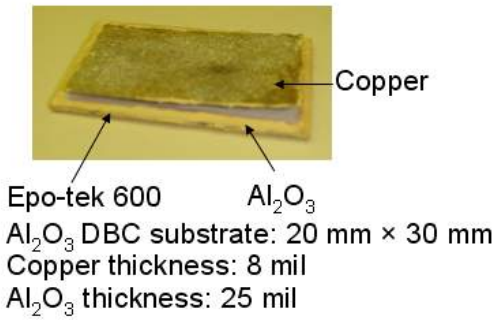


Figure 2-16. Failed group C sample.

Table 2-14 Thermo-Cycling Results of Group C Samples

Samples	Dimensions	Life time
Sample C1	20 mm ×30 mm	60 cycles
Sample C2	20 mm ×30 mm	60 cycles
Sample C3	20 mm ×30 mm	60 cycles

In the next step investigation, the stepped edge was formed before the sealing to improve the thermal reliability, as shown in Figure 2-17. These samples were named as group D samples and the fabrication procedure and settings are listed in Table 2-15. During the preliminary thermal cycling test, Duralco 132 showed relatively poor and considerably unstable performance, while Epo-tek 600 showed promising results, which was about 1000 cycles.

Figure 2-17. Group D sample.

Table 2-15 Fabrication Procedure and Settings of Group D Sample

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300

Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
		Etching time for 4 mil copper (minute)	10
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Curing profile	Shown in figure 2-13

Six pieces 30 mm × 20 mm Al_2O_3 DBC were twice etched and sealed with Epo-tek 600. Once the samples were fabricated, the surface roughness of them was measured for further comparison. As shown in Figure 2-6, the cycling temperature is between -55 °C and 250 °C, and each cycle take about 45 minutes. After 1100 cycles, one sample would be taken out to determine the surface roughness changing and then cross-sectioned to ensure that no failure happened.

During the thermal cycling tests, all the samples were cycled until failure or planned measurement. All sealed edge samples passed 800 cycles. Three of them failed at 850 cycles and two of them failed at 1200 cycles. One failed sample is shown in Figure 2-18. All tested sample materials and thermal cycling lifetimes are listed in Table 2-16.

Figure 2-18. Failed group D sample.

Table 2-16 Thermal-Cycling Results of Group D Samples

Samples	Dimensions	Life time
Sample D1	20 mm ×30 mm	850 cycles
Sample D2	20 mm ×30 mm	850 cycles
Sample D3	20 mm ×30 mm	850 cycles
Sample D4	20 mm ×30 mm	1100 cycles
Sample D5	20 mm ×30 mm	1200 cycles
Sample D6	20 mm ×30 mm	1200 cycles

Figure 2-20 illustrates the surface roughness of the sealed edge DBC sample before thermal cycling and after 1100 cycles. The settings of surface-roughness measuring machine are listed in Table 2-17. The measuring points are shown in Figure 2-19. As shown in Table 2-18, there is acceptable increase in the standard deviation of surface roughness as a result of cycling.

Table 2-17 Settings of Dektak 3 for Group D Samples

Surface roughness measurement machine	Scan length	Scan speed	Data point	Scan resolution	Display range
Dektak 3	5000 μm	25 s	5000	5 μm/sample	Auto

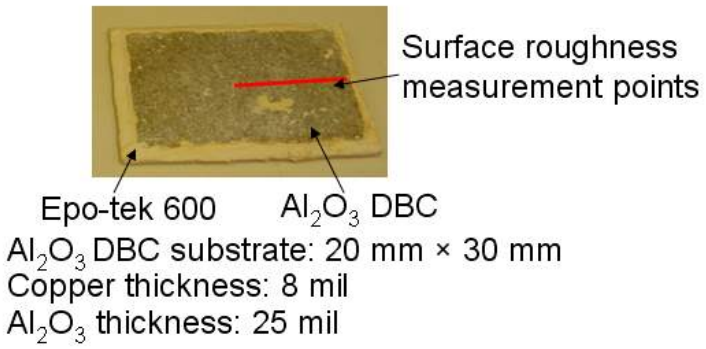


Figure 2-19. Measuring points of surface roughness for group D samples.

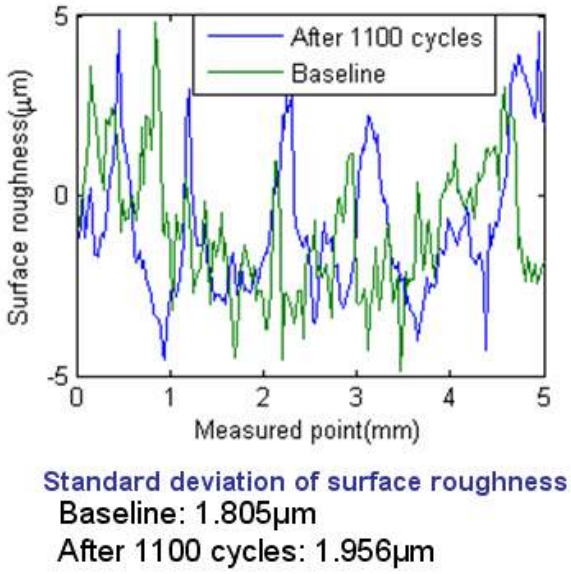


Figure 2-20. Surface roughness comparison of one group D sample.

Table 2-18 Surface Roughness of Group D Samples

Samples	Surface roughness deviation before cycling	Surface roughness deviation after 1100 cycles
Sample D4	1.805 μm	1.956 μm
Sample D5	1.958 μm	2.011 μm
Sample D6	1.798 μm	1.937 μm

Figure 2-21 shows the cross-section of the sample after 1100 cycles under microscope. It can be noticed that the copper and ceramic were bonded well without any peeling off. It proves that with the sealing process on the stepped edge, the thermal reliability of DBC substrate can be significantly improved.

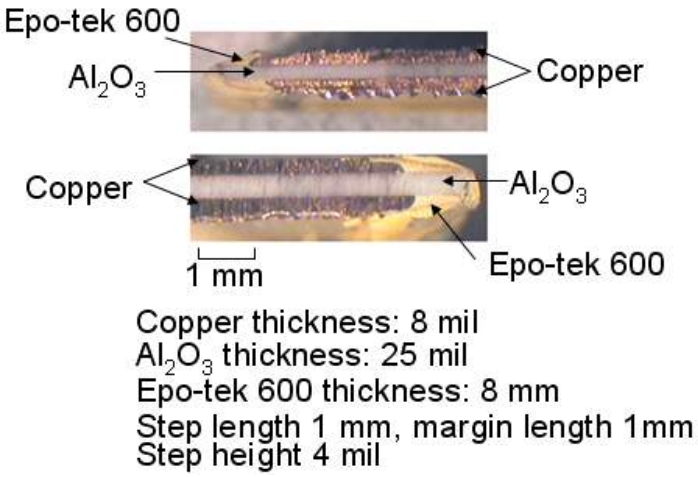


Figure 2-21. Cross-section of group D sample.

2.2.3 Reliability of Die-Attachment and Wirebond Package

As the bonding material between the device and the substrate, die-attach material plays an important role of mechanically supporting the device, conducting the electrical current as well as dissipating the generated heat from the device to substrate. Its thermal reliability needs to be determined together with the improved DBC substrate.

Figure 2-22. Group E samples.

As shown in Figure 2-22, sixteen SiC diode dies are attached to the sealed stepped edge Al_2O_3 DBC by using Au-Ge solder preform. These samples are named as group E. The fabrication procedure and settings are listed in Table 2-19. Group E samples were thermally cycled by using the same cycling chamber and same temperature profile as shown in Figure 2-6. After each 200 cycles, four dies were sheared off from the substrate to measure the die-shear strength of the die-attachment.

Table 2-19 Fabrication Procedure and Settings for Group E Samples

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Curing profile	Shown in figure 2-13
Vacuum reflow machine: SST MV-2200	Reflowing Au-Ge solder	Temperature profile	Shown in Figure 2-4

Table 2-20 Thermal-Cycling Results of Group E Samples

	After cycles	Samples	Die-shear strength (MPa)
Assembly of SiC diodes on sealed-stepped-edge Al_2O_3 DBC DBC dimensions: 30 mm ×40 mm	0	Diode E1	50.3
		Diode E2	49.2
		Diode E3	50.1
		Diode E4	48.9
	200	Diode E5	34.2
		Diode E6	33.9
		Diode E7	32.8

SiC diode: dimension: 2.7 mm × 2.7 mm		Diode E8	33.7
	400	Diode E9	17.3
		Diode E10	16.8
		Diode E11	16.5
		Diode E12	17.2
	600	Diode E13	15.9
		Diode E14	16.2
		Diode E15	15.8
		Diode E16	16.1
	800	Diode E17	13.8
		Diode E18	14.6
		Diode E19	13.9
		Diode E20	14.2

The measured die-shear strength of die-attachment are listed in Table 2-20 and plotted in Figure 2-23. A large drop of die-shear strength was found during the first couple of hundred thermal cycles. The die-shear strength then enters into a stable region after about 400 cycles. However, as the backside of the sheared-off devices observed, it was found that most of the device backside metallization layer was peeled off from the SiC layer. The cause of degradation could not be identified from the die-shear test. It is possible that the degradation of the packaging material on the backside of SiC diode, and the CTE mismatches between die, die-attachment and substrate acted together.

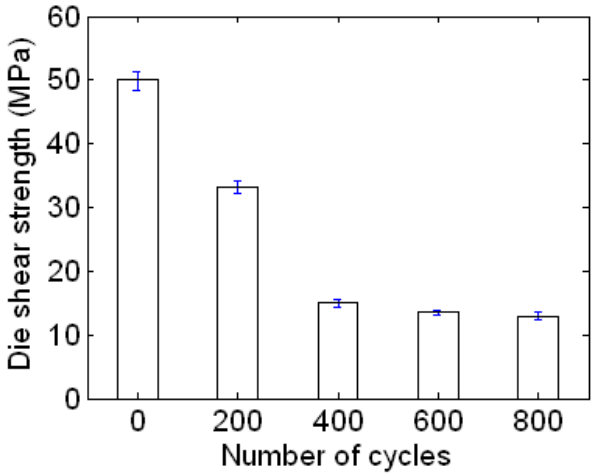


Figure 2-23. Thermal-cycling results of group E samples.

Figure 2-24 shows the backside of the sheared-off SiC devices after a certain number of thermal cycles, where silver (Ag) is the backside metallization material of the SiC devices. It is clear that after about 400 cycles, only a small area of SiC device was still covered with the silver, this explains why the die-shear strength of Au-Ge solder becomes stable after 400 cycles. The measured value of die-shear strength should be close to the bonding strength of the device backside metallization.

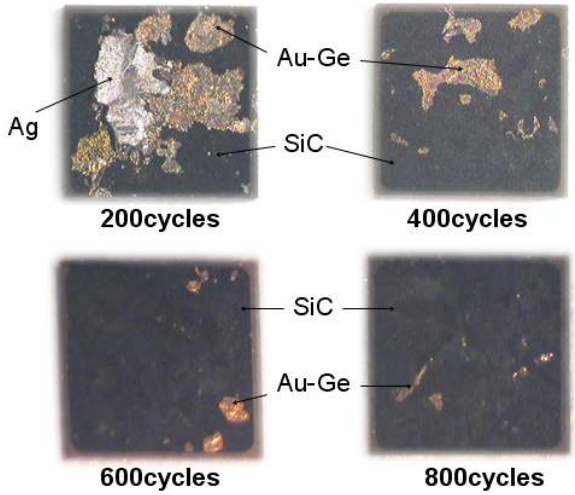


Figure 2-24. Back side of sheared-off group E diodes.

After the die-shear test, X-ray photoelectron spectroscopy system was used to identify the elements on the backside surface of the diode. Since silicon and carbon can be found at tested spots with considerable amount, it confirms that the metallization of the SiC diode peelinged off in the die-shear tests.

During the test, the thermal resistance was measured by applying dc current to the diode. The substrate temperature was measured by thermocouple while the junction temperature of the diode was estimated from its temperature-dependent voltage and current characteristics obtained with the static measurement [34]. With limited measurement accuracy, no apparent change of thermal resistance was observed. In fact, after 800 thermal cycles, the die-shear strength was about 15 MPa, which is still an acceptable value for die-attachment. It means that the devices and substrate were bonded tightly with die-attachment and there should be no significant degradation on the thermal resistance.

With the encouraging thermo-mechanical reliability results on die-attachment, further thermal reliability test on assembly including wirebond was also conducted. There were seven SiC mechanical sample dies soldered to the Epo-tek 600 sealed stepped edge DBC and four of them bonded with 10 mils aluminum wires, which is shown in Figure 2-25. These samples are named as group F samples.

As shown in Table 2-21, with the help of laser cutting machine and etching machine, the DBC substrate is patterned. Then SiC JFET samples were soldered to DBC substrate

with reflow process. Finally wirebonds were formed from pads of dies to traces of DBC substrate.

Figure 2-25. Group F samples.

Table 2-21 Fabrication Process and Setting for Group F Samples

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Curing profile	Shown in figure 2-13
Vacuum reflow machine: SST MV-2200	Reflowing Au-Ge solder	Temperature profile	Shown in Figure 2-9
Wirebonding	Wirebonding	First bonding time (ms)	2

machine: Orthodyne M20B	5 mil aluminum wire	First bonding power (mW)	90
		Second bonding time (ms)	4
		Second bonding power (mW)	100
	Wirebonding 10 mil aluminum wire	First bonding time (ms)	4
		First bonding power (mW)	250
		Second bonding time (ms)	8
		Second bonding power (mW)	280

Table 2-22 Thermal-Cycling Results of Group F Samples

Samples	Dimensions	Life time
Sample F1	17 mm ×30 mm	450 cycles
Sample F2	17 mm ×30 mm	450 cycles
Sample F3	17 mm ×30 mm	450 cycles

Group F samples were cycled with the same temperature profile as shown in Figure 2-6. As listed in Table 2-22, the substrate failed at 450 cycles while the rest of packaging parts showed no visual degradation. There was no specified test to identify the critical layers or critical parameters in the cycling. Degradation of packaging materials and the CTE mismatch between assembly layers may together affect the sample's lifetime. The Al wires should also degrade somewhat during the thermal cycling. Since they did not show as the limiting mechanism for packaged module thermal cycle failures, no wirebond pull test was conducted after the thermal cycling.

2.3 Summary of High-Temperature Wirebond Package

Based on the wirebond packaging, materials for each part of the module are compared and selected to ensure the full package can function reliably at 250 ºC. The thermo-mechanical reliability of substrate was evaluated and several methods were investigated to improve the lifetime. It is found through experiments that by sealing the stepped edge DBC, considerable improvement (50 times longer lifetime) on substrate reliability under

large temperature excursion can be achieved. The promising results of thermal cycling test on die-attachment and wirebond assemblies prove that the proposed package can perform well for large temperature excursion.

Chapter 3 Development of High-Temperature Planar Package

The overall objectives of power electronics packaging are to distribute signal and power, dissipate the heat generated from the power devices, protect the devices and circuits from mechanical damage, and ensure reliable operation of semiconductor devices. In addition, high-current capability and low packaging interconnect impedance are critical factors in the packaging design. Table 3-1 lists the requirements for the power electronics packaging for harsh environment operation [24].

Table 3-1 Desirable Attributes for a High-Temperature Package

Thermal	Low thermal resistance (<0.65 K/W) from junction to case; high junction temperature (>200 ºC) operation ability; high thermomechanical reliability for large temperature excursion (>250 ºC); double-sided cooling ability
Electrical	Small parasitic inductance (<20 nH), symmetric layout, small footprint
Manufacture	Simple fabrication process; precise interconnection of small pads (50 um resolution or feature sizes)

Although conventional wirebond packaging satisfies some of the requirements listed above, in order to take more benefit from the advantages of SiC devices, non-wirebond packaging is highly preferred for high temperature operation. There has been continuous progress in applying non-wirebond technologies to power electronics packaging in recent years [42-66]. Interconnects are constructed with metals and polymer layers that are

formed directly or indirectly on pads of top side of devices. Based on the interconnection methods, the planar package can be classified in Table 3-2.

Table 3-2 Planar Packaging Classification

Top pad inter-connection method	Technology and researcher	Advantage	Dissatisfaction
Direct soldering	PowerConnect [42], by Vishay Siliconix	Good top side heat dissipation, low parasitic parameters, small footprint	Low thermo-mechanical reliability, low voltage due to reflow process, difficult interconnection for centered pad
	Dr.MOS [43], by Fairchild		
	CopperStrap [44], PowerPack [45], DirectFET [46], by IR		
	LFPAK [47], by NXP		
	Power sandwich [48], by Nottingham Univ.		
Solder ball / solder bump	MPIPPS [49], D2BGA [50], FCOF [51], Dimple array [52], Flex-power [53], J. Xu high voltage package [54], by CPES	High thermo-mechanical reliability, high voltage capability, multilayer interconnection capability	Relatively poor top side heat dissipation, relatively larger parasitic parameters,
	SO-8 wireless [55], BGA MOSFET [56],		

	PowerTrench [57], by Fairchild		
	Power bump [58], by Alstom		
	FlipFet [59],by IR		
Pressure contact	Press-Pack [60], by Westcode of IXYS	Better reliability due to fatigue-free structure, very high voltage capability	Relatively poor top side heat dissipation, relatively larger parasitic parameters, special mechanical gadget required
	StakPak [61], Press Pack [62]by ABB		
Welding contact	SkiN [63], by Semikron	Better reliability due to fatigue-free structure, good top side heat dissipation low parasitic parameters, small footprint	Difficult interconnection for centered pad
Sputtering + electroplating	Power overlay [64], by GE	Good top side heat dissipation, low parasitic parameters, small footprint	Low thermo-mechanical reliability, high quality sputtering and electroplating required
	Embedded power [65], by CPES		
Sintered silver	Next generation Flex-	Good top side heat	Advanced sintering

	power [64], by CPES	dissipation, low parasitic parameters, small footprint, high thermo -mechanical reliability,	process required
	Diode planar package [66], by CPES		

Although efforts have been made in realizing high temperature capability, issues and shortcomings still remain in most of the packaging techniques. In this chapter, a novel high-temperature planar packaging utilizing sintered silver is proposed.

3.1 Structure, Material Selection and Fabrication of Planar Package

In the packaging process, the small dimensions of pads on the topside of power devices will increase the complexity of the interconnections for non-wirebond packages. As shown in Figure 2-3, the gate pad is only 880 μm × 440 μm and is enclosed by the source pads, which may baffle the regular solder reflow process.

Exceeding regular solder in many aspects for planar packaging, sintered silver [66] is selected as conductive connection material. With the assistant of this material, the precise interconnection of small pads can be implemented in the fabrication process. Based on this key feature, this paper describes a novel planar packaging technique for high temperature applications. The electrical and thermal reliability test results show that the combination of the material selection, packaging development and the fabrication process are feasible and reliable for harsh environment operation.

3.1.1 Structure of Planar Package

The cross-section structures of the planar package for a single SiC diode is shown in Figure 3-1 and he thickness of different layers is listed in Table 3-3.

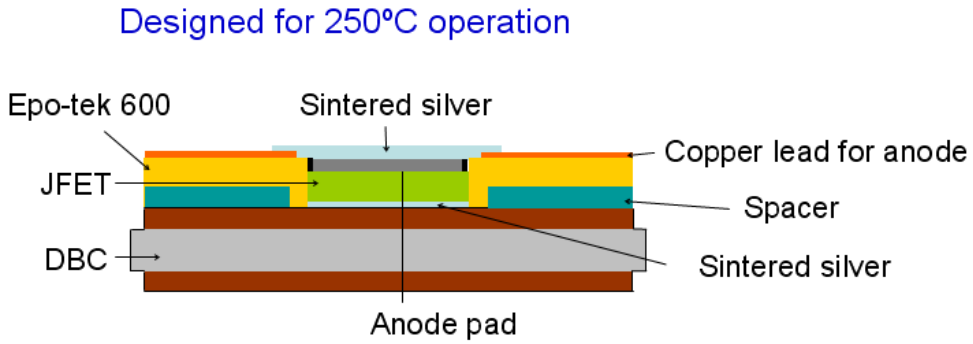


Figure 3-1. Cross-section of planar packaged SiC diode.

Table 3-3 Thickness of Planar Packaged SiC Diode

	Al_2O_3	Copper on DBC	Copper lead	Epo-tek 600	Sintered silver	Spacer (Kapton)	SiC diode
Thickness	25 mil	8 mil	8 mil	4 mil	2 mil	4 mil	380 μm

Figure 3-1 illustrates the planar package for a single diode connection. The SiC diode is sandwiched between DBC (Direct Bond Copper) substrate and the sintered silver connected copper leads. Copper leads are used as both the external lead and the internal interconnect to the semiconductor die enclosed in the power module. Sintered silver is used as the electrically conductive connecting material. Epo-tek 600 and spacer act as the insulation layer between the electrical conduction layers. Additionally, Epo-tek 600 is employed as the adhesive layer, while the spacer is used to match the height difference between different devices.

The cross-section structures of the planar package for a single SiC JFET is shown in Figure 3-2 and the thickness of different layers is listed in Table 3-4.

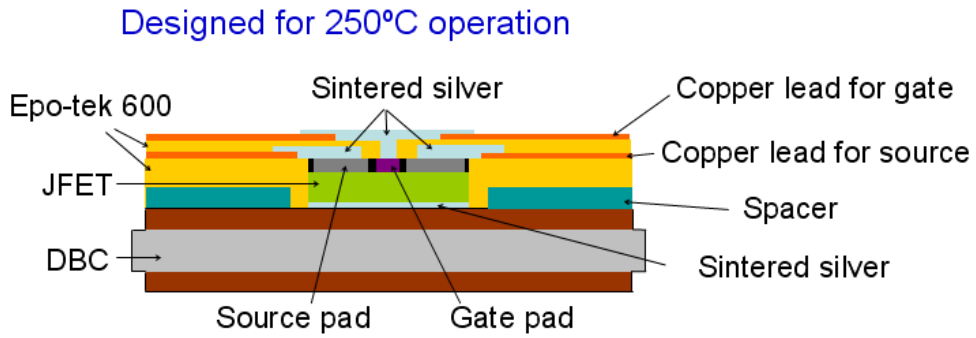


Figure 3-2. Cross-section of planar packaged SiC JFET.

Table 3-4 Thickness of Planar Packaged SiC JFET

	Al_2O_3	Copper on DBC	Copper lead	Epo-tek 600	Sintered silver	Spacer (Kapton)	SiC diode
Thickness	25 mil	8 mil	8 mil	4 mil	2 mil	4 mil	380 μm

Figure 3-2 illustrates the planar package for the JFET connection. The drain pad, source pads and gate pad of SiC JFET are separately connected to three different electrical conduction layers by sintered silver. The drain pad, which is located on the bottom of the JFET, is attached to the DBC, while the source pads and gate pads are connected to two different copper lead layers. Compared with the diode connection package there is one more Epo-tek 600 layer acting as the insulation layer between the source copper lead and the gate copper lead.

3.1.2 Material Selection for Planar Package

The top pads electrical connection layers are a key point in this planar package. Due to the high targeted operation temperature (250 ºC) and the multi-layer structure of the

module, the interconnection technique is desired to have (1) reliable high temperature capability; (2) relatively low processing temperature; and (3) excellent electrical and thermal characteristics. Three attaching techniques are considered candidates: namely, solder reflow, TLP-bonding (Transient Liquid Phase bonding), and LTJT (Low-Temperature Joining Technique).

Most of the solders are susceptible to creep and suffer significant degradation in many of the thermal, electrical and mechanical properties. For some die-attach materials, i.e. AuGe and AuSn [34], although they are capable of working beyond 250 ºC, much higher processing temperatures are generally required (>320 ºC). In addition, considering the number of reflows encountered during the module fabrication, multiple solder layer with different reflow temperatures are required. In general [14], a 40 ºC temperature gap between two reflow processes is desired to minimize the re-melting of the lower temperature solder. Therefore, the highest processing temperature can easily be beyond 400 ºC. Moreover, in the reflow process, the solder will melt and flow, and thus it is difficult to form a consistent connection between top pads and copper leads. TLP [17] is another promising technology for die-attachment that does not have re-melting issue in multilayer bonding. The bonding is formed by the atomic diffusion of one component (In) into another component (Ag) so as to change the localized composition, and therefore changes the material's melting point. However, the top pads bonding ability of TLP is yet to be studied and demonstrated.

Table 3-5 Comparison Between LTJT Using Sintered Silver, TLP and Solders

	Solder reflow	TLP-bonding	LTJT
Processing Temperature	Solders with different reflow temperature are required, which pushes the processing temperature over 400 ºC	Processed in 250 ºC, will not remelt until 400 ºC	Sinter at 275 ºC
Electrical resistivity	Typically more than $1.5 \times 10^{-7}\ \Omega \cdot m$	Implicit	$15.9 \times 10^{-9}\ \Omega \cdot m$
Thermal conductivity	Typically less than 100 W/m-K	Implicit	240 W/m-K
Accommodation	Difficult to retain the consistent topside solder connection	Capability of consistent topside bonding undemonstrated	No re-melting of the sintered silver; no chip swimming and pad alignment problem

LTJT is a relatively new technique in forming the interconnection [67][68]. Unlike solder reflow and TLP-bonding techniques, LTJT is a process involving the sintering of micro- and nano-sized metal particles [69][70]. Once the interconnection is formed, the bonding material is close to be pure metal, usually Ag, and will not melt until its melting temperature, 961^{o}C. In this study, sintered silver [71] is chosen. Different from solder

reflow process, die-attachments are formed by sintering the nano-sized silver particles at relatively low temperature, 275 ºC. During the sintering process, the sintered silver will not change the shape and the consistency of connection between top pads and copper leads can be controlled by screen-printing process. The sintering profile of sintered silver is shown in Figure 3-3. Previous studies [69, 70] have also shown that the sintered silver joint is very stable in micro-structure and shows good thermal and mechanical properties [68]. The comparisons between LTJT using sintered silver, TLP and solders are listed in Table 3-5.

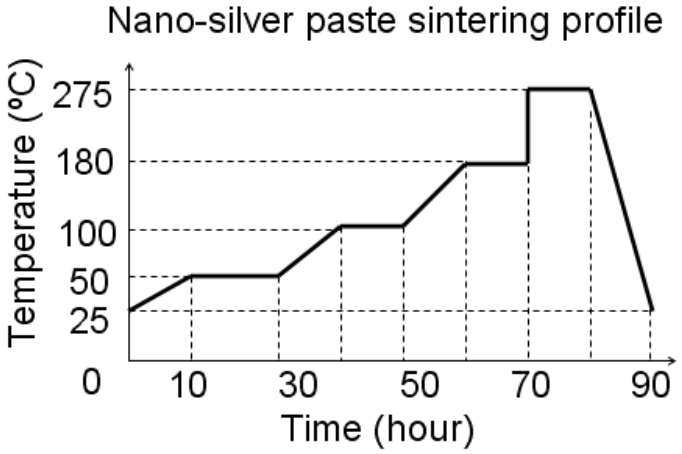


Figure 3-3. Nano-Silver paste sintering profile.

Based on the literature survey [14] and the preliminary evaluation, materials for each part of the planar package are selected and listed in Table 3-6. Properties like thermal conductivity, electrical conductivity, coefficient of thermal expansion (CTE), dielectric strength, Young's modulus, and their high-temperature capability are the main criteria for the selection.

Table 3-6 Materials Used in the Planar Package

Component	**Selection**	**Typical thickness**	**Electrical property**	**Thermal property**	**Mechanical property**
Switching device	SiC JFET from SiCed	380 μm	1200 V, 5 A	Theoretically operation capability up to 600 ºC	Young's modulus 460 GPa, Compressive strength 345 MPa
Diode	SiC Schottky diode from SiCed	380 μm	1200 V,20 A		
Interconnection layer	Sintered silver	50 μm	Electrical resistivity 15.9×10^{-9} Ωm	Sintering temperature 250 ºC, theoretically operation capability up to 961ºC	Young's modulus 9 GPa, Shear strength 20 MPa
Nonconductive connection layer	Epo-tek 600	100μm	Dielectric strength 118 kV/mm	Curing temperature 200 ºC, operation capability up to 400 ºC	
Spacer	1 mils Kapton	25 μm	Dielectric strength 255 kV/mm	Operation capability up to 260 ºC	Tensile strength 0.22 MPa

Lead	copper foil electroplated with nickel and silver	200μm	Electrical resistivity 16.8×10^{-9} Ωm	Thermal conductivity 400W/m-k, theoretically operation capability up to 1084 ºC	Tensile strength 33 MPa, Young's modulus 110 GPa
Substrate	Al_2O_3 DBC (Direct bond copper)	635 μm Al_2O_3 200 μm Cu	Electrical resistivity of copper 16.8×10^{-9} Ωm, Dielectric strength of Al_2O_3 6500 kV/mm	Thermal conductivity of copper 400W/m/k, Thermal conductivity of alumina 70W/m-k, operation capability up to 1000 ºC	Tensile strength of Al_2O_3 300 MPa, Tensile strength of Cu 33 MPa Youg's modulus of Cu 110 GPa
Encapsulant	Nusil R-2188	0.5 mm	Dielectric strength 17.7 kV/mm	Operation capability up to 300 ºC	Tensile strength 3.3 MPa

In order to demonstrate the planar package concept, 600 V, 5 A SiC JFET electrical sample from SiCED, and 600V, 10A SiC Schottky diode from CREE were selected as the power devices in the prototype power module.

Kapton tape [72] is one type of polyimide film that can remain stable in a wide range of temperatures. Its good thermal conductivity, good dielectric qualities, and availability as thin sheets have made it a favorite material in power electronics packaging research. In addition, multiple layers of tapes can be utilized to match the height difference of different devices.

Epo-tek 600 [73] is selected for the thermal adhesive and insulation layers due to its good thermal properties and high-temperature stability. The copper lead-frames are electroplated with nickel and silver. The nickle layer is 5 μm and the silver layer is 0.6 μm. They can provide high temperature stability, and adequate electrical and thermal conductivity. They are formed by selective etching or machining. All other materials in the packaging are selected to support the planar package for 250 °C operation. The vendors of the selected materials in this investigation are listed in Table 3-7.

Table 3-7 Vendors of Selected Material in Planar Package

Material	SiC JFET SiC diode	Al_2O_3 DBC AlN DBC	Sintered silver	Kapton tape	Nusil R-2188
Vendor	SiCed	Curamik	Nanotech	Kapton	Nusil Silicone technology
Material	Epo-tek 600	Duralco 132	Heatsink		
Vendor	Epoxy technology	Cotronics	Thermaflow		

3.1.3 Fabrication Process of Planar Package

In order to develop the planar package structure shown in Figure 3-1 and Figure 3-2, the fabrication process is divided into steps, as shown in Figure 3-4 and Table 3-8.

The first step is patterning the DBC substrate, which can be processed by laser cutting and acid etching. Then the spacer, multiple layers of Kapton tape, can be attached to the DBC as the insulation layer. The spacer layer can be preliminarily prepared as the designed pattern before attaching or further patterning with laser cutting machine after the attaching. At the same time, the devices can be well positioned with the assistance of spacers, and later attached to the DBC with sintered silver through sintering [68]. In order to prevent electrical breakdown around the edges of the devices, Epo-tek 600 is utilized to cover the devices' guard rings and fill the gaps between the spacer and the devices. Then the first lead-frame layer can be bonded to the spacer with Epo-tek 600.

Table 3-8 Fabrication Process and Settings for Planar Package

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Heating oven: Vulcan 3-550	Sintering nano-silver paste	Temperature profile	Shown in Figure 3-3
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Temperature profile	Shown in Figure 2-13

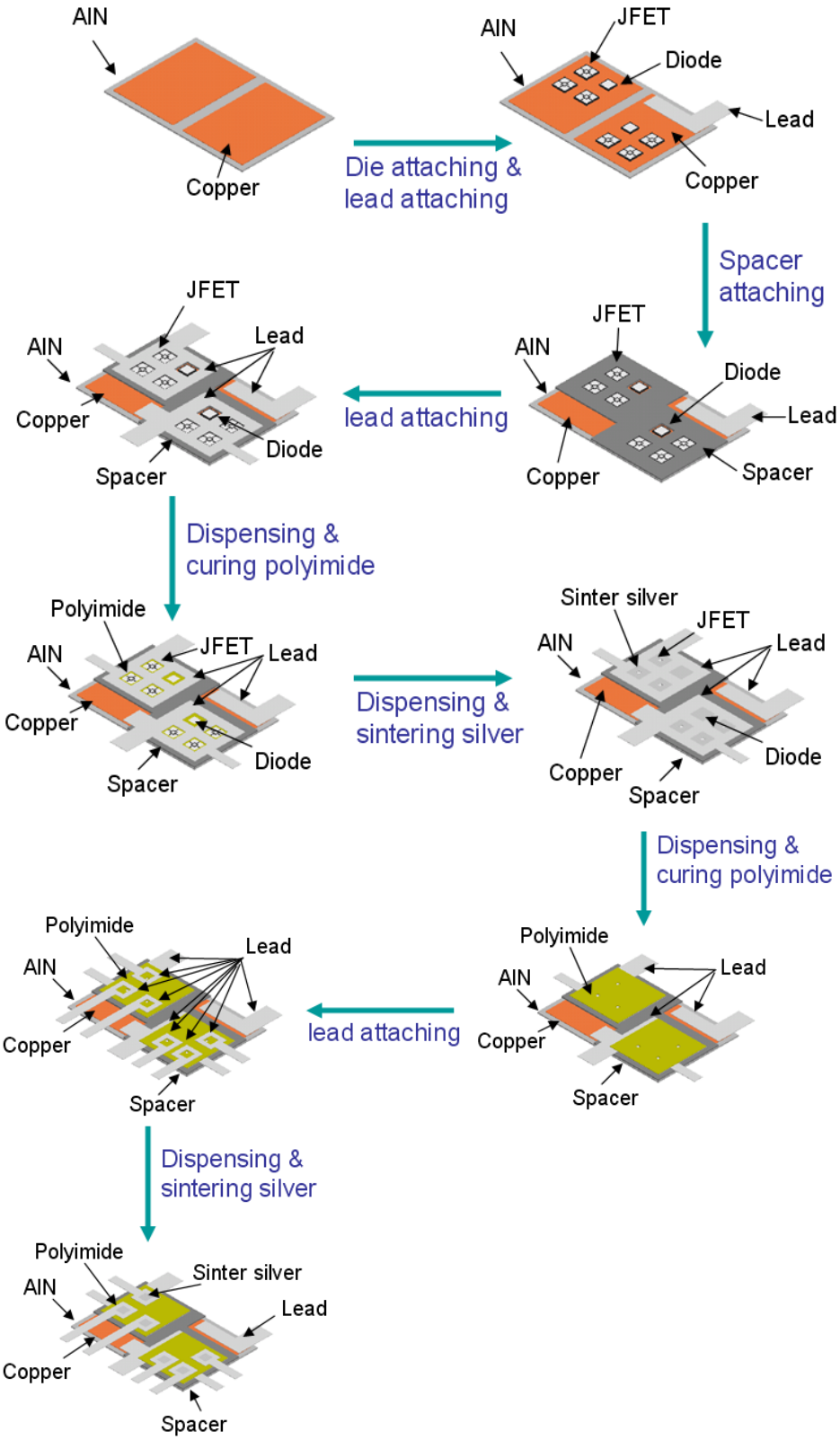


Figure 3-4. Fabrication process for planar package.

In the next step, the source pads on the JFETs and the anode pads on the diodes are individually connected with the first copper lead layer by sintered silver. Since the dies metallizations are aluminum, which is not compatible with sintered silver, the pads need to be zincated and electro-less plated with silver. The second insulation layer is then formed by Epo-tek 600, and the second lead-frame layer can be also bonded by curing the polyimide. Finally, the gate pads of the JFETs are connected with the second copper lead layer by sintering the sintered silver.

In total, there are three silver sintering steps and three polyimide curing steps included in the fabrication process. During the sintering process, direct top-side individual interconnection eliminates the misalignment problem in multiple pads and enclosed small pads. The technique is very practical for laboratory prototyping and can be precisely implemented. The cross-section of planar packaged SiC diode is shown in Figure 3-5 and the cross-section of planar packaged SiC diode is shown in Figure 3-6.

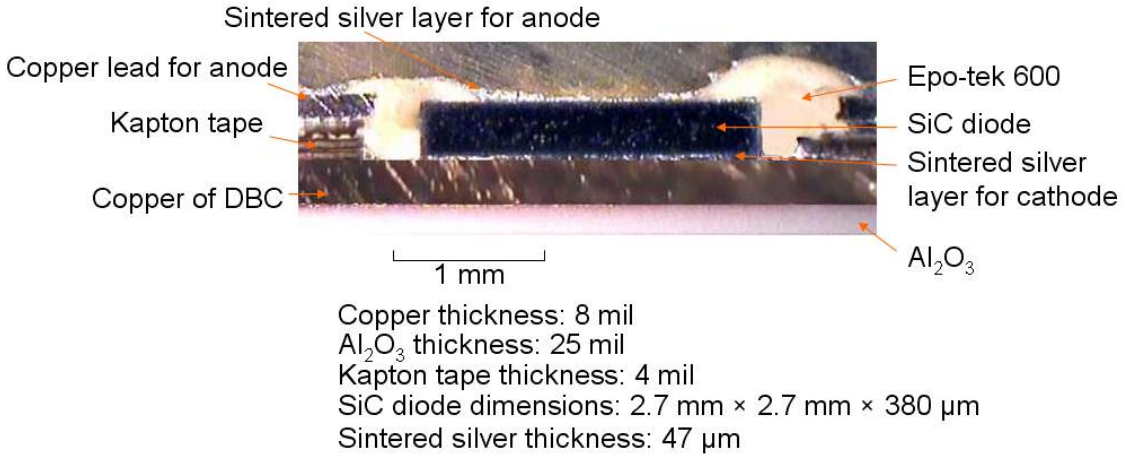


Figure 3-5. Cross-section of planar packaged SiC diode.

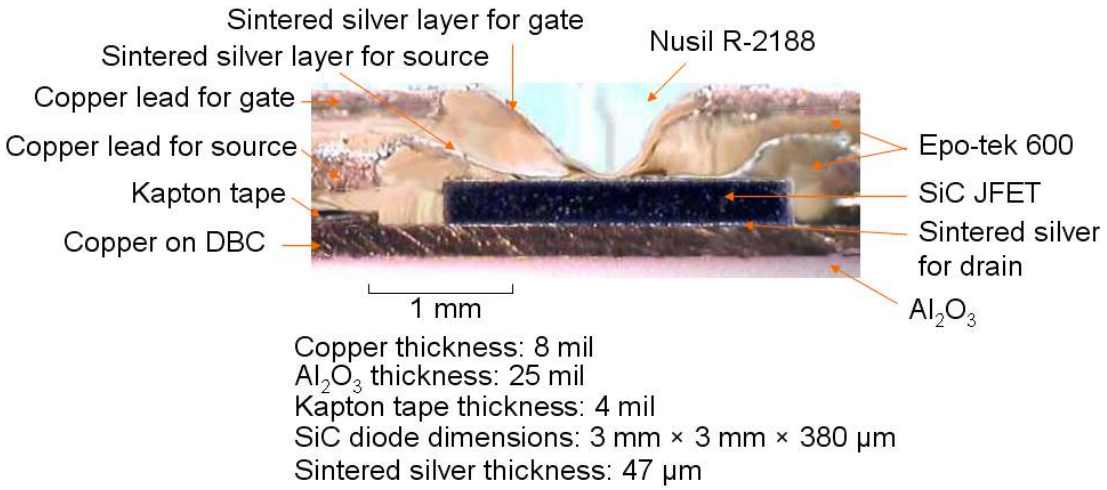


Figure 3-6. Cross-section of planar packaged SiC JFET.

3.1.4 I-V Characteristics Test

I-V characteristics before and after the packaging process are measured without continuous power operation. One JFET or one diode is employed in the test assembly. Five JFET assemblies and five diode assemblies are fabricated and tested respectively.

First the I-V characteristic curves of the bare dies are measured by curve-tracer (Tektronix 371) at room temperature. The setting of curve tracer is listed in Table 3-9.Then they are packaged and tested under 25ºC and 250ºC. In the latter group of tests, the assemblies are placed on the hot plate to keep the 250ºC environment.

Table 3-9 Settings of Curve Tracer (Tektronix 371)

Curve tracer	Measurement of forward I-V curve				
Tektronix 371	Collect supply mode	Maximum power	Current resolution	Voltage resolution	Measurement mode
	High current	30 W	1 A/div	0.5 V/div	Repeat
	Measurement of blocking I-V curve				
	Collect supply mode	Maximum power	Current resolution	Voltage resolution	Measurement mode
	High	30 W	20 μA/div	100 V/div	Repeat

	voltage				

Since it was found there is little performance difference between the five assemblies, only one diode and one JFET are selected with their I-V characteristics shown in Figure 3-7 and Figure 3-8.

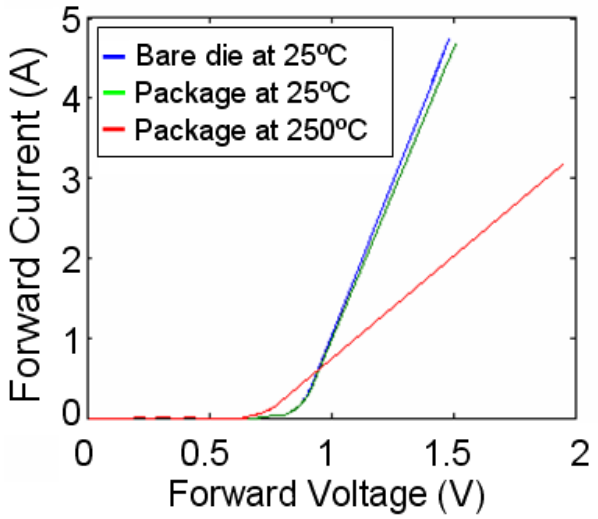


Figure 3-7. Forward I-V characteristics for planar packaged SiC diode.

Figure 3-7 shows the measured forward I-V characteristics for a SiC Schottky diode. After packaging, the linearized on-state resistor (R_{on}) increases 1.6% at 25 ˚C room temperature. The on-resistance increases to about 2.5 times at 250 ˚C due to the reduction in the electron mobility at elevated temperatures.

The leakage current was also measured for the bare diode die and the packaged devices at 25 ˚C and 250 ºC. The test results show that the planar structure can support approximately 600 V reverse voltage, the same as the bare die, and therefore there is no device degradation brought by planar package.

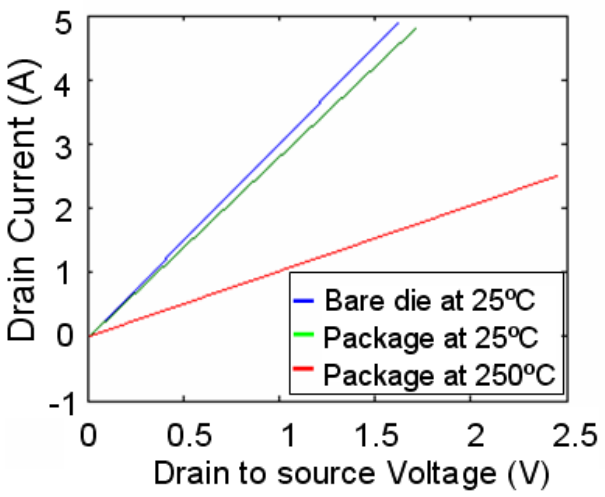


Figure 3-8. Forward I-V characteristics for planar packaged SiC JFET.

Figure 3-8 illustrates the measured drain current versus drain-to-source voltage characteristics of the SiC JFET, at 25 ˚C room temperature and 250ºC. The gate-to-source voltage was controlled as 0 V. The drain-to-source on-state resistor (R_{dson}) increases 1.4% after packaging at room temperature. R_{dson} increases to about threefold with the ambient temperature rising to 250 ºC.

During the measurement of blocking characteristics of JFET, the applied gate-to-source voltage was kept at -28 V. The leakage current was also measured for the bare JFET die and the packaged devices at room temperature and 250 ºC. The test results show that the planar structure can support approximately 600 V reverse voltage, again the same as the bare die. Therefore, there is no JFET device degradation brought by planar package that can be observed within the resolution of leakage current measuring equipment (50 μA) at room temperature or at 250 ºC.

Comparing the electrical characteristics of the bare die and the packaged device depicted in the Figure 3-7 and Figure 3-8, no noticeable changes can be found. It is proved the planar package has acceptable parasitic resistances.

3.2 Thermo-Mechanical Reliability of Planar Package

In order to evaluate the thermo-mechanical reliability of the planar package, commonly used heat soaking tests and a thermal cycling test were applied.

3.2.1 Die-Attachment Reliability in Planar Package

As the key point of power electronics packaging, it is crucial to first identify the thermo-mechanical reliability of the die-attachment operated at 250 ºC junction temperatures and temperature swinging ranging -55 ºC to 250 ºC. As shown in Figure 3-9, ten mechanical diode samples were sintered to a substrate using sintered silver as intermediate test sample. These samples were named as group G samples. The fabrication procedure and settings are listed in Table 3-10.

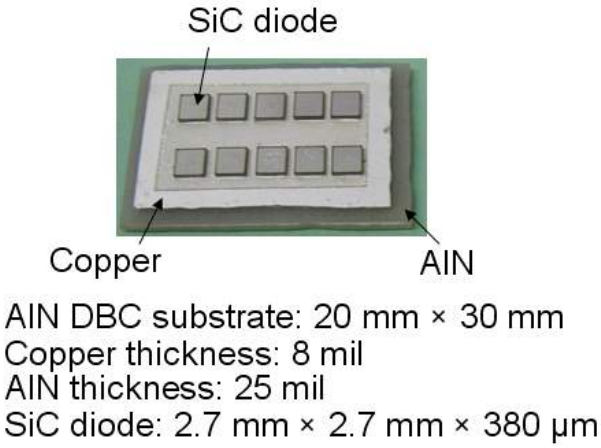


Figure 3-9. Group G samples.

Table 3-10 Fabrication Procedure and Settings of Group G Samples

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Heating oven: Vulcan 3-550	Sintering nano-silver paste	Temperature profile	Shown in Figure 3-3

In this test, two test samples were prepared. Then the heat soaking test was performed in the 250 ºC ambient. Test samples was put in the soaking chamber and kept running for 500 hours. By using the die-shear tester, each time four dies were sheared before soaking and at 100 hours, 200 hours, 300 hours and 500 hours. As shown in Table 3-11 and

Figure 3-10, compared with the samples before and after 500 hours heat soaking, there was no significant degradation.

Table 3-11 Soaking Results of Group G Samples

	Heat soaking hours	Samples	Die-shear strength (MPa)
Assembly of SiC diodes on sealed-stepped-edge Al_2O_3 DBC DBC dimensions: 30 mm ×40 mm SiC diode: dimension: 2.7 mm × 2.7 mm	0	Diode G1	25.7
		Diode G2	24.8
		Diode G3	24.3
		Diode G4	25.2
	100	Diode G5	23.6
		Diode G6	22.3
		Diode G7	23.9
		Diode G8	22.7
	200	Diode G9	21.8
		Diode G10	22.3
		Diode G11	22.7
		Diode G12	21.8
	300	Diode G13	19.3
		Diode G14	20.3
		Diode G15	18.7
		Diode G16	19.5
	500	Diode G17	19.3
		Diode G18	18.2
		Diode G19	17.9
		Diode G20	18.5

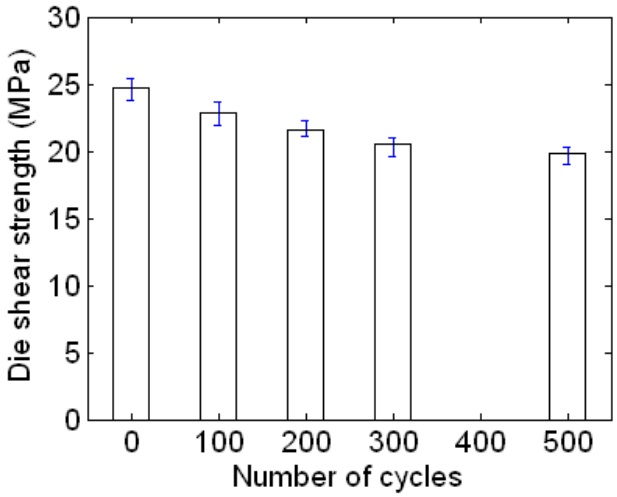


Figure 3-10. Soaking results of group G samples.

For the thermal cycling test, as shown in Figure 3-11, sixteen SiC diode dies are attached to a DBC substrate using sintered silver. These samples were named as group H samples. The fabrication procedure and settings are listed in Table 3-12. The test sample was thermally cycled in the thermal cycling chamber. The temperature profile was shown in Figure 2-6.

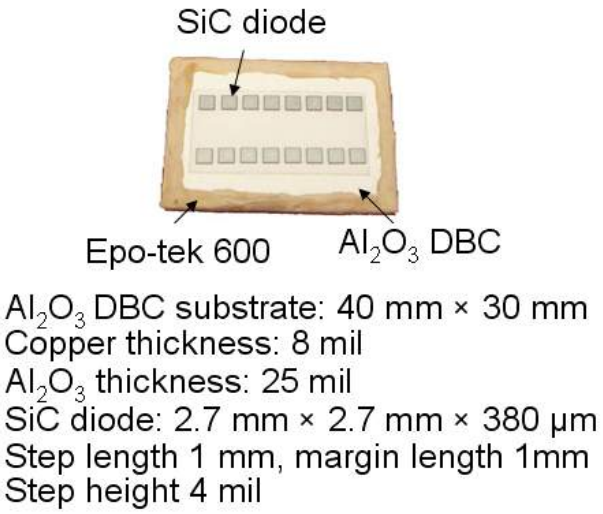


Figure 3-11. Group H samples.

Table 3-12 Fabrication Procedure and Settings for Group H

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Temperature profile	Shown in Figure 2-13

Heating oven: Vulcan 3-550	Sintering nano-silver paste	Temperature profile	Shown in Figure 3-3

After every 200 cycles, four dies were sheared off from the substrate to measure the die-shear strength of the die-attachment. Die-shear strength of group H samples are listed in Table 3-13 and plotted in Figure 3-12.

Table 3-13 Cycling Results of Group H Samples

	After cycles	Samples	Die-shear strength (MPa)
Assembly of SiC diodes on sealed-stepped-edge Al_2O_3 DBC DBC dimensions: 30 mm ×40 mm SiC diode: dimension: 2.7 mm × 2.7 mm	0	Diode H1	26.7
		Diode H2	24.9
		Diode H3	24.7
		Diode H4	25.1
	200	Diode H5	19.8
		Diode H6	21.9
		Diode H7	21.3
		Diode H8	20.1
	400	Diode H9	13.3
		Diode H10	13.8
		Diode H11	13.5
		Diode H12	13.7
	600	Diode H13	12.9
		Diode H14	13.2
		Diode H15	12.8
		Diode H16	13.1
	800	Diode H17	11.8
		Diode H18	11.6
		Diode H19	11.9
		Diode H20	11.1

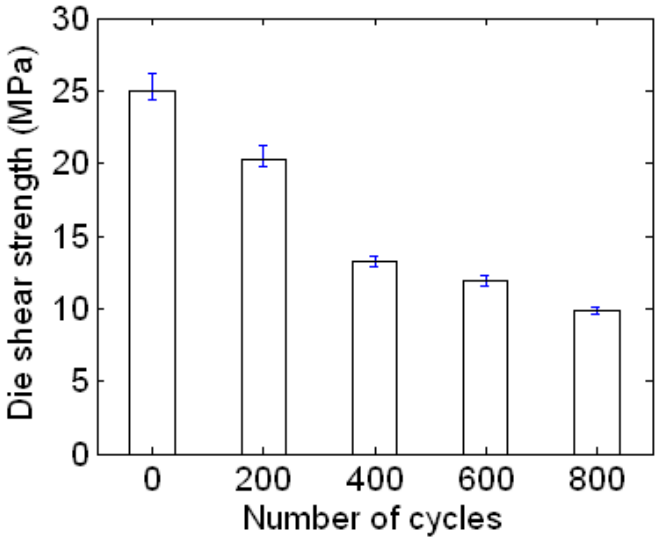


Figure 3-12. Thermal-cycling results of group H samples.

Figure 3-12 shows the die-shear strength of sintered silver versus the cycling number. The die-shear strength decreases as the cycling number increases, and reaches a relatively stable region after 400 cycles. After 800 cycles, the die shear test value dropped to below half of baseline samples, but still kept a satisfactory value. The thermal resistance of the tested sample was measured before each die-shear test. With the resolution of test equipment (0.1°C/W), there was no change observed in thermal resistance up to the tested 800 cyclers. The breakdown voltage of the tested sample was also measured before the each die-shear test. With the resolution of leakage current measurement equipment at 50 μA, there was no change observed in breakdown voltage up to the tested 800 cyclers.

Based on the thermal cycling and heat soaking test, it is concluded that the die-attachment can survive both high-temperature operation and large temperature swings.

3.2.2 Thermo-Mechanical Reliability of Full Planar Package

In order to reduce the cost and demonstrate the thermo-mechanical reliability of the planar package, five diode dies are packaged as test sample, as shown in Figure 3-13. These samples are named as group I samples. By using the same cycling chamber and temperature profile shown in Figure 2-6, the group I samples were cycled and failed after 300 cycles. The lifetime of group I samples are listed in Table 3-14.

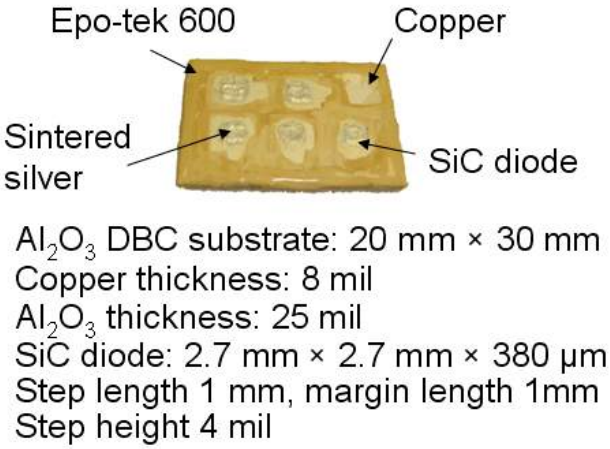


Figure 3-13. Group I sample.

Table 3-14 Fabrication Procedure and Settings of Equipments for Group I Samples

Machine	Processing	Setting	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.8
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	5
		Pulse number	5
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.05
		Stage lasing velocity (inch/s)	1
		Repeat rate	1
		Laser power (W)	40
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	20
Heating oven: Vulcan 3-550	Curing Epo-tek 600	Temperature profile	Shown in Figure 2-13

Heating oven: Vulcan 3-550	Sintering nano-silver paste	Temperature profile	Shown in Figure 3-3

The basic I-V characteristic tests were conducted to examine the interconnection quality and reverse-voltage blocking ability of the planar package before and after 200 cycles. Since there is little difference between the performances of the five diodes, one diode was selected out and its forward I-V characteristics are shown in Figure 3-14.

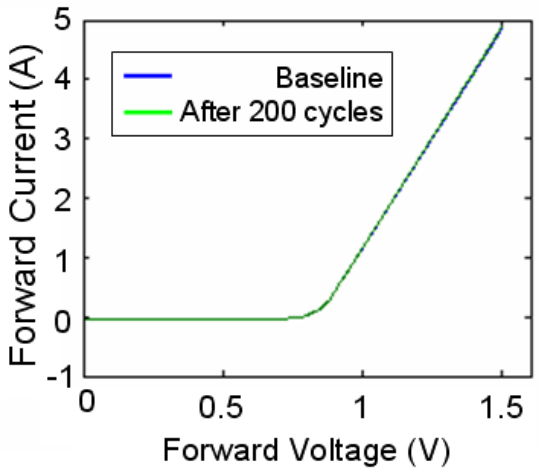


Figure 3-14. Comparison of I-V characteristics for group I sample.

Comparing the forward I-V characteristics of the diode before and after 200 cycles, no noticeable changes can be found. The reverse blocking I-V characteristics was also measured and there is no change before and after the cycling. As shown in Figure 3-15, the group I samples failed after 300 cycles and the lifetime of these samples are listed in Table 3-15.

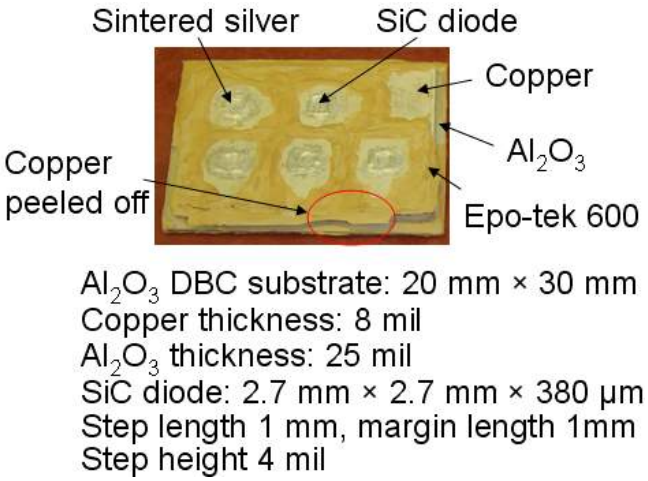


Figure 3-15. Failed group I sample.

Table 3-15 Thermal-Cycling Results of Group I Samples

Samples	Dimensions	Life time
Sample I1	20 mm ×30 mm	300 cycles
Sample I2	20 mm ×30 mm	300 cycles
Sample I3	20 mm ×30 mm	300 cycles

This proves the planar packaging can support a certain number of large temperature excursions. With the acceptable test results, the thermo-mechanical reliability of full packaged power module will be investigated in the future.

3.3 Summary of High-Temperature-Planar Package

A high-temperature (250 ºC) planar package for the power module using SiC devices is presented. Sintered silver and high-temperature polyimide are selected as the interconnection materials, which allow individual interconnection on each pad. This approach takes the advantages of the flexibility and the high-temperature capability of the sintered silver and the polyimide material, and can be implemented in other packaging applications. Electrical and thermo-mechanical tests of the prototype module demonstrate

the functionality and thermo-mechanical reliability of the planar packaging technology. The proposed planar package concept can be used in many potential high-temperature high-density applications, such as the aircraft systems intended in this paper, with further studies needed on additional advantages such as double-sided cooling and on issues such as manufacturability.

Chapter 4 Layout Design of Power Module

It has been shown that the parasitic parameters in the module have a detrimental influence on the switching loss and the dynamic behavior [74]. This phenomenon will be exacerbated when the density increases because higher switching rating leads to faster variations. In addition, power integration decreases distances, resulting in higher impact on coupling of current conduction path. In order to ensure high efficiency and high performance of high density power module, efforts are required in the layout design [75].

4.1 Guideline of Layout Design

There are basically two important layout design considerations. First, when the switching frequency is high, large voltage spikes will result due to the high di/dt. By reducing the parasitic parameters, the magnitude of these voltage spikes can be reduced [75]. Second, the parasitic parameters between paralleled devices need to be balanced. It will help to achieve equal current distribution in parallel devices, consequently affecting the performance of the whole module.

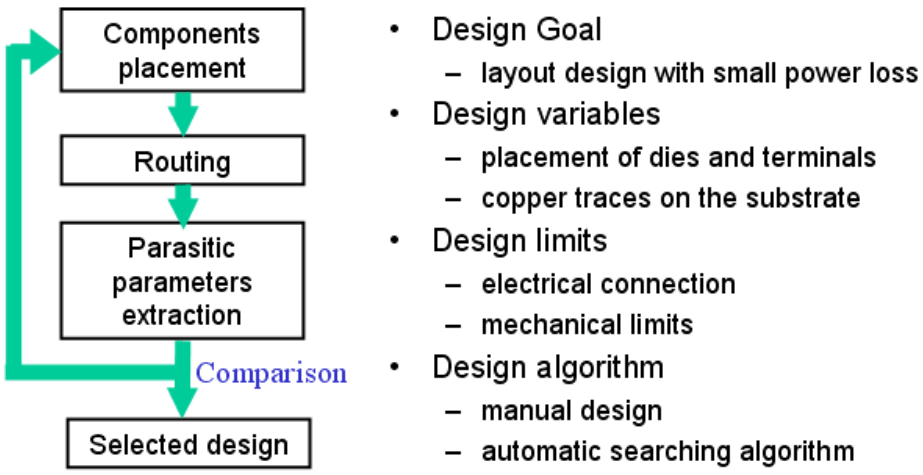


Figure 4-1. Procedure of layout design.

As described in Figure 4-1, the layout design procedure is based on the design iterations. Each cycle can generate a layout design result and will be compared with other design results. After several iterations, the best layout can be chosen in from the design candidate. Even the best candidate is usually not the best selection in the whole design space, the final selected result is still a superior layout and will be benefit in power loss reduction.

In the iterations, devices and power terminals, which are the basic components in the layout design, will be firstly geometrically placed by considering the electrical connections. The second step is the routing process, in which the dies and the pads will be connection with the copper traces and the wirebonds. Then the parasitic parameters in the designed layout can be obtained from FEA simulation tools or theoretic equation based calculation. From the literature survey, there is still no figure of merit existed for

fitness evaluation chasing minimum power loss in the layout design. The fitness can be only achieved based on the overall evaluation of the parasitic parameters.

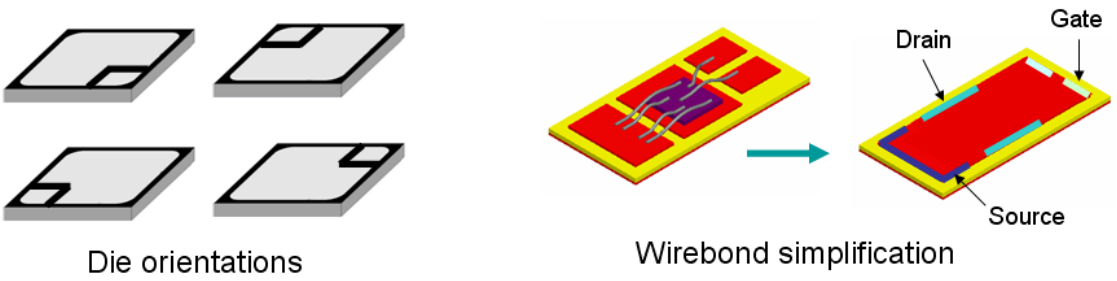


Figure 4-2. Consideration in placement and routing.

As shown in Figure 4-2, in placement process, since the pads on the die may be asymmetrically distributed while the leadframe connections are restricted by the mechanical issue or fabrication process, components in layout design should have orientations and they are always critical in the sense of the parasitic parameters reduction and balance between paralleled devices.

In the routing process, in order to simplify the process, the wirebond routing can be degraded in the components because the wirebond is the largest contributor of the parasitic parameters. As shown in Fig. 3-2, the wirebond connection provides the length reduction of the wires and the decoupling between gate loop and power loop. The pads of device are extended to the terminals of newly defined power unit. This simplification saves the placement time and routing time.

The literature survey [74-82] also shows that there is only manual layout design existing so far. The main dissatisfactions of the manual layout design are the design

speed and the limited choice of candidate. The manual design is always experience based process and lack of consistency. The automatic layout design is highly preferred during the iterations. Learned from the VLSI automatic layout design, the power module automatic layout design is developed and presented in chapter 3.3.

4.2 Basic Consideration of Layout Design

In the power module layout design, several detailed considerations need to be followed and they are listed as below.

The parasitic inductance and resistance are mainly caused by packaging, which is composed of interconnection such as bond wires and copper traces on the DBC. The parasitic capacitances in the power module, are important for the electromagnetic interference (EMI) performance, but have small influence on the switching performance [76]. Therefore, parasitic capacitance is neglected in this report. Decoupling capacitors between positive and negative terminals are embedded in the power module to decouple the possible parasitic effects of the external power connectors. Thus, the voltage overshoot will be mainly determined by the internal packaging parasitics [77].

In the module interconnections, gate paths are partly mixed with the power paths, which will have a large impact on the gate driving transient [78]. Kelvin terminals should be added to the power module to weaken this coupling, as shown in Figure 4-3. The Kelvin terminals should be close enough to the source pads of power switch to reduce the impact of the large power current.

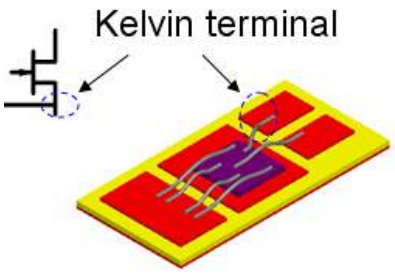


Figure 4-3. Kelvin terminal to decoupling the power path and gate path.

In the power module, the commutating loop inductances of the switch-diode must be further considered due to the impact on the current transferred from the power switch to the diode. According to the parasitic parameters study in [79], the commutating path inductances change the voltage stresses on the power switch and the diode significantly. Furthermore, the switching loss is also sensitive to the switch-diode commutating loop inductance. To minimize the voltage stress on the devices, these parasitic parameters are required to be small.

The balance of parasitic parameters for paralleled devices is also important. The electrical performance of a power module can be defined as the ability to use each die at maximum ratings [80]. Therefore, all over voltages must be reduced, and the current balance between all dies must be as precise as possible. The dissymmetry parasitic parameters of the power module will prevent a well designed layout. If one of the dies turn-on earlier than other paralleled dies, due to the coupling of gate drive path impedance, the relatively larger power path current will impact the turn-on behavior of the other dies. During this period, the switching delay between dies is further escalating.

Several design rules are adopted from [75-82] and accumulated from the design experience in CPES. They are: (1) reducing the length of the bonding wire and the conductive copper route, (2) adding more leadframes or increase the width of leadframes to the terminal to enlarge the contact area with external circuit, (3) reducing the enclosure area of the JFET-Diode commutating loop, and placing devices of this loop as close as possible to each other, (4) enlarging the width of the copper traces, (5) decoupling the power paths and gate paths as much as possible. The suitable layout is usually obtained by adjusting the tradeoff between these rules.

In the high temperature power module, both the power device and the packaging materials will be degrade. From [83], the on-resistance of SiC JFET will increase about two times when the junction temperature increases from 25 ºC to 250 ºC. At the same time, the resistance of aluminum wires and copper trace will also increase in 250 ºC. However, the design goal, design variable, design limits and design algorithm, none of them will be changed in the high temperature power module layout. It means that the layout design methodology for normal temperature module is also suitable for high temperature module.

4.3 Example of Manual Design

In order to demonstrate the layout design process, a phase-leg module was investigated. In this module, there are two power switches and two diodes. Several layouts have been proposed and four of the layouts were chosen to do the comparison (as

shown in Fig. 3-4). By using the software package Maxwell Q3D, parasitic parameters are extracted.

The FEA simulation indicated that layout 4 has the smallest resistance and inductance values, especially in the switch-diode commutation loop. Figure 4-4 shows the difference of switch-diode commutation impedance. Thus, it is expected that layout 4 will show considerable reduction of voltage stress and be more reliable.

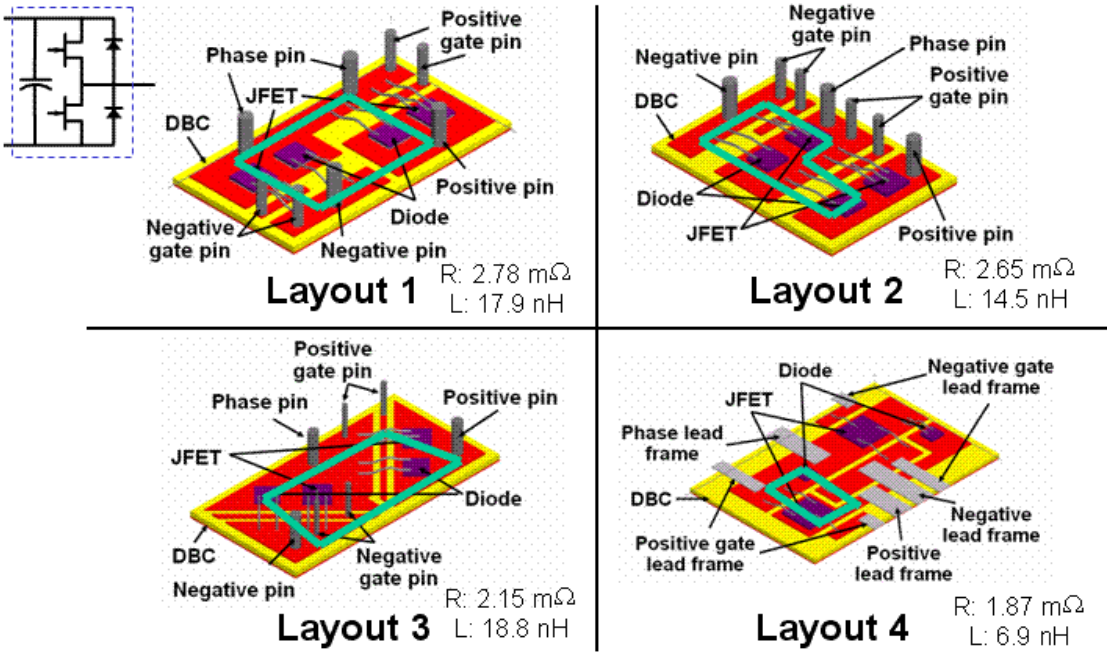


Figure 4-4. Example of manual design.

Figure 4-5 shows two different layouts of multi-chip power module. In layout 1, due to the dissymmetrical placement of the dies, and the imposed external pin location, both power and gate paths are dissymmetric. In layout 2, the symmetry is well considered in the layout design. and current sharing between paralleled dies will be improved.

Figure 4-6 presents a lumped-parameter circuit model. In order to clearly show the distribution of parasitic parameters only self inductances and resistances are explicitly shown in the figure. In layout 1, a considerable imbalance in the distribution of the parasitic parameters can be seen. In layout 2, the imbalance is improved, implying that layout 2 shows more symmetry than layout 1.

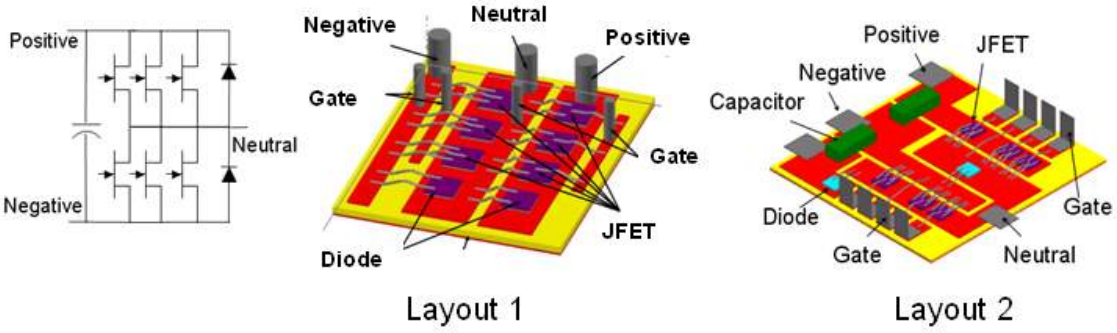


Figure 4-5. Layout results of multi-chip power module.

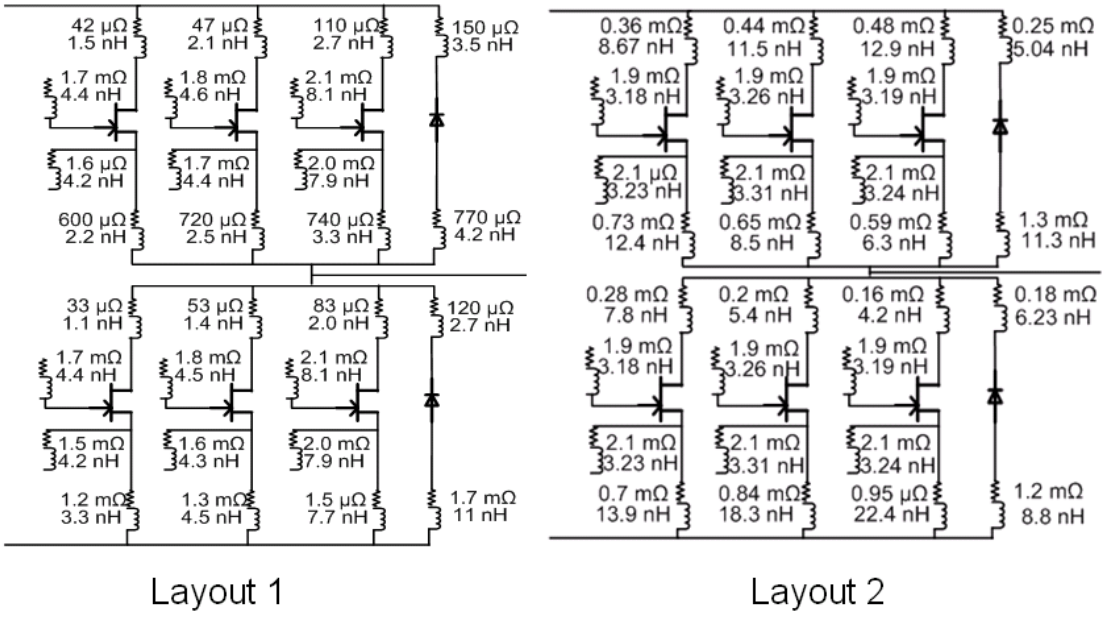


Figure 4-6. Comparison of parasitic parameters.

In order to analyze the effects of the symmetry parasitic impedance on the switching performance of the modules, a circuit simulation was performed. The module is operated as a buck converter. A huge dynamic current imbalance in the upper phase-leg, during the switching phase, can be observed in Figure 4-7. The transient current, which is approximately two times the nominal current, flows through JFET 1. Although similar uneven current distribution of paralleled dies can also observed in layout 2, the peak current amplitudes were considerably reduced and the distribution was more uniform for layout 2. Thus layout 2 is a superior design to layout 1 from symmetry point of view.

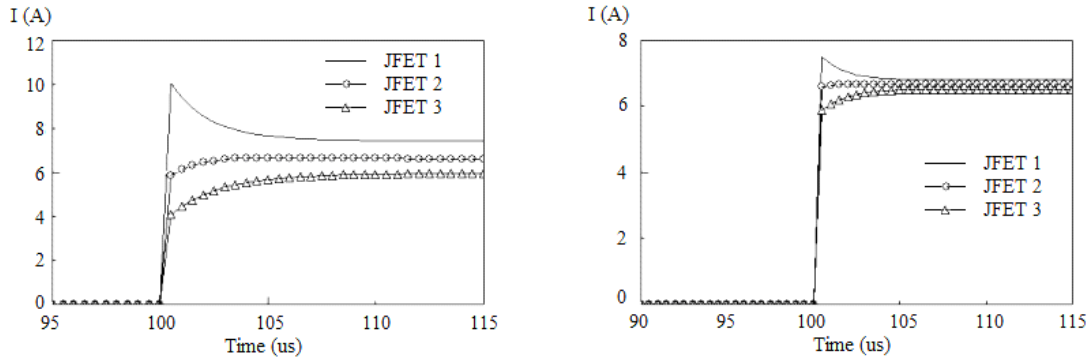


Figure 4-7. Comparison of current distribution.

From Figure 4-7, it is indicated that the influence of the symmetry of parasitic parameters are not negligible, especially the gate circuit impedance. However, limited by geometrical and electromagnetic constraints, in many cases it is difficult to obtain the ideal layout design which allows perfect currents distribution. In order to consider reduction of parasitic parameters and asymmetry layout, a more efficient and comprehensive design method is highly required.

4.4 Automatic Layout Design

4.4.1 Algorithm and Iterations of Layout Design

It is mentioned that the automatic layout design for power module can be learned from the VLSI automatic design. The purpose of VLSI design is to embed an abstract circuit description, such as a netlist, into silicon, creating a detailed geometric layout on a die [83]. In the early years of semiconductor technology, the task of laying out gates and interconnect wires was carried out manually [84]. However, as semiconductor fabrication processes improved, making it possible to incorporate large numbers of transistors onto a single chip, it became imperative for the design community to turn to the use of automation to address the resulting problem of scale. Automation was facilitated by the improvement in the speed of computers that would be used to create the next generation of computer chips resulting in their own replacement [85]. While the problems of scale have been one motivator for automation, other factors have also come into play. Most notably, improvements in technology have resulted in the invalidation of some critical assumptions made during physical design: one of these is related to the relative delay between gates and the interconnect wires used to connect gates to each other [86].

There are a lot of similar design strategies can be borrowed for the VLSI design. In order to better develop the automatic layout design for power module. The main differences between VLSI and power module design are listed in Table 4-1

Table 4-1Comparison between VLSI and Power Module Layout Design

	VLSI layout design	Power module Layout design
Components	Huge number of devices with regular dimension	Small number of devices (usually less than 20) with irregular dimension
Routing layer	Usually muiti-layer	Usually single layer (wirebond degrade to components)
Steps	Clustering, floor plan, placement, routing	Placement and routing iterations
Routing requirement	Routable	Trace thickness and coupling
Fitness	Minimum footprint, total length (time delay)	Small parasitic parameters, balance between paralleled device, small footprint

As shown in Table III-I, the power module layout design is iteration based comparison with much smaller number of components and simpler placement and routing. However, different from the fitness evaluation in the VLSI design, power module layout design requires parasitic parameters extraction process. Base on these characteristics, the genetic algorithm (GA) is chosen as the automatic design algorithm.

GA is a search technique used in computing to find exact or approximate solutions to optimization and search problems. Genetic algorithms are categorized as global search heuristics. Genetic algorithms are a particular class of evolutionary algorithms that use techniques inspired by evolutionary biology such as inheritance, mutation, selection, and crossover [87]. GA is a stochastic search method based on natural genetics, which deals with the individuals composed of candidate solutions (population), each of which is generally encoded in a problem independent representation. During the genetic process, new candidate solutions are evaluated by their fitness and reproduced using the genetic

operators such as crossover and mutation [88]. The typical GA process is described in Figure 4-8.

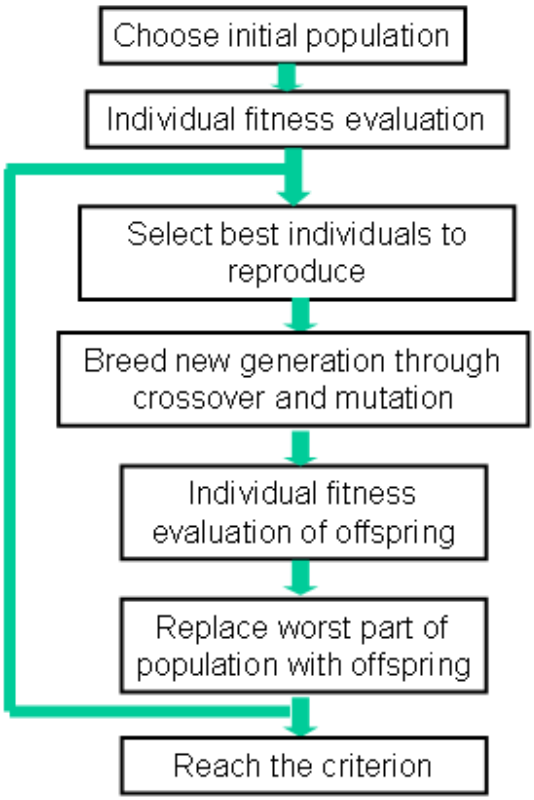


Figure 4-8. Typical genetic algorithm process.

Traditionally, solutions are represented in binary as "DNA" strings of 0s and 1s, but other encodings are also possible. The evolution usually starts from a population of randomly generated individuals and happens in generations. In each generation, the fitness of every individual in the population is evaluated, multiple individuals are stochastically selected from the current population (based on their fitness), and modified (recombined and possibly randomly mutated) to form a new population. The new population is then used in the next iteration of the algorithm. Commonly, the algorithm

terminates when either a maximum number of generations has been produced, or a satisfactory fitness level has been reached for the population [89].

As shown in Figure 4-9, in the automatic layout design, there are two loops utilizing GA. The outer loop is placement loop, in which the components will be placed and evaluated based on the design results of inner loop (routing loop). The outer loop will provide the position of layout components to the inner loop. With the certain components position, the inner loop will physically connect the components based on the electrical connection. The routing process is implemented by GA and analytical equation based parasitic parameters calculation method is utilized during the fitness evaluation step. After iterations, the best individual routing result as well as its fitness will be passed to the outer loop. The outer loop using the passed out routing results as the fitness in placement evaluation.

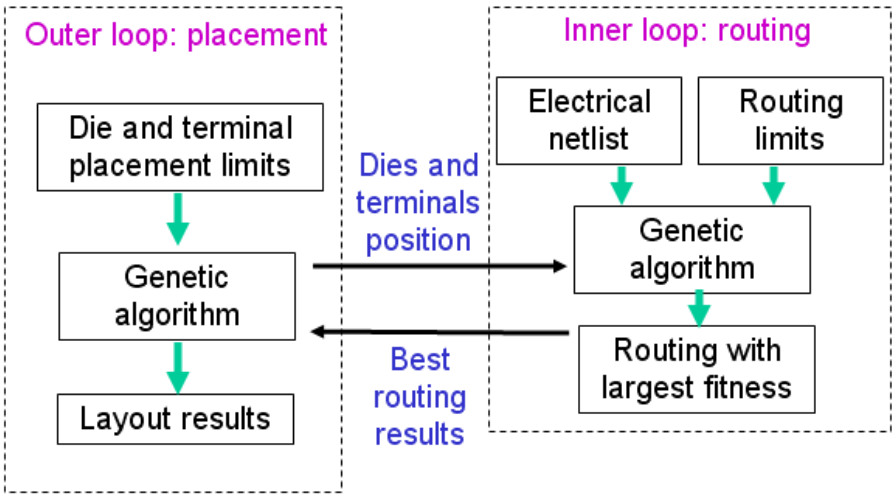


Figure 4-9. Automatic layout design process for power module.

4.4.2 Outer-Loop Implementation

In the outer loop, layout components can be substituted with a rectangle with a given height and width in real number. Then GA can help to choose the best set of non-overlapping placement of given components. One important key to solve the problem effectively is the representation of relative position. In [90], sequence-pair has been proposed as the representation of a solution of this problem, which is particularly suitable for stochastic algorithms such as GA.

The sequence-pair (SQ) for a set of n components is a pair of sequences of the n component names. A sequence-pair imposes a horizontal/vertical (H/V) constraints for every pair of components. The oblique-grid notation of a given placement visually shows H/V constraints specified by a given SQ.

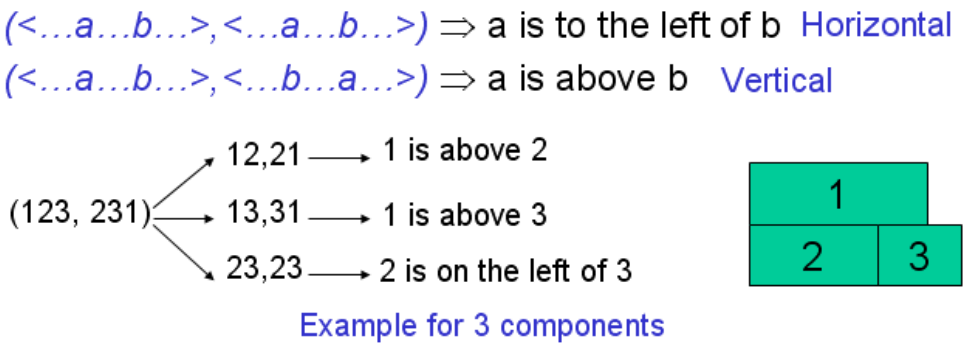


Figure 4-10. Sequence-pair representation.

Figure 4-10 shows an example for SQ representation. If two components have the same sequence in SQ, it means one component is one the left of the other component as sequence indicated. If two components have the different sequence in SQ, it means one component is one the top of the other component as sequence indicated. In the example,

SQ (123,231) has three components and each two components has the sequence (12,21), (13,31) and (23,23), which represents 1 above 2, 1 above 3, 2 on the left of 3. With the relative position, the placement of three components can be shown in the right part of Figure 4-10.

As mentioned in Chapter 4.3, the components should have orientations, which are represented with 2 digits binary in this report. 00 means facing top; 01 means facing right; 10 means facing bottom and 11 means facing left. Thus, n components orientation can be represented by a 2n digits string.

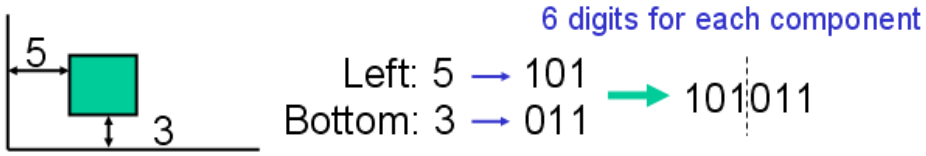


Figure 4-11. Gaps for components.

In the components placement, the gaps between them are also required. The gap here is defined the distance from the left-bottom corner of component to the left boundary or to the bottom boundary. In this report, limited by the substrate fabrication process, the minimum distance between components is 1 mm and the resolution of distance is also 1 mm. If in the placement design, the largest gap is less than 2^n mm, the gaps can be represented with n digits binary string, as shown in Figure 4-11. In this report the horizontal gap string listed before the vertical gap string.

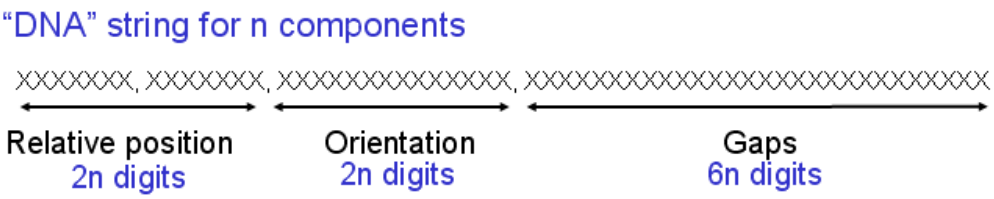


Figure 4-12. DNA string in the outer loop.

Combining relative position string, orientation string and gaps string, the whole "DNA" string with 10n digits can comprehensively represent n components placement, as shown in Figure 4-12.

The initial population is generated randomly and the size of the population is base on the components number. In this report, population is chosen as 5n if components number is n. This population is selected during the attempts. The fitness of one placement is evaluated from the inner routing loops.

In the GA process, there are two important operators, one is crossover and the other one is mutation. One point crossover and one point mutation are utilized in this report. Because orientation part and gaps part are the conventional binary strings, conventional crossover or conventional mutation will be operated if crossover point selected in these parts. The conventional crossover means that all data beyond that point in either string is swapped between the two parent strings and the resulting strings are two children. The conventional mutation means that an arbitrary bit in a genetic string will be changed from its original state. It means that original "0" changes to "1" while original "1" changes to "0".

If the crossover point selected in relative position part, special operation will be implemented. Common Topology Preserving Crossover (CTPX) is a special crossover which preserves the common characteristics of parents in relative position part [91]. In CTPX, first, the longest common subsequences (LCSs) of parents SQ are found. Then, components in the LCSs are preserved on the same sequence. Other components are exchanged so that the order of them in SQ of one offspring is the same as one parent. One example is shown in Figure 4-13.

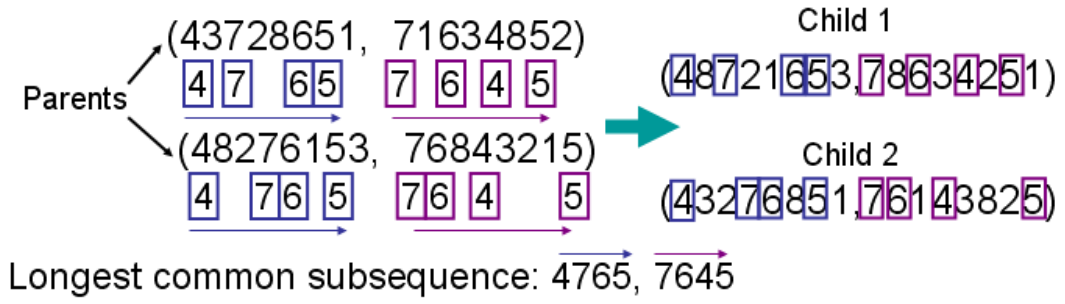


Figure 4-13. Common topology preserving crossover example.

In this example, the LCSs is (4765, 7645), whose position will not change in the crossover operation. The rest components in SQ, which are (3281, 1382) and (8213, 8321), exchange the position but still keep the same sequence. Thus two children (48721653, 78634251) and (43276841, 76143825) are generated.

If the mutation point selected in relative position part, special operation [92] will also be implemented. Compared with crossover operation, mutation is much simpler. Two components in SQ will be selected and exchange the positions. The example is shown in Figure 4-14.

Figure 4-14. Mutation example.

4.4.3 Inner-Loop Implementation

In the inner loop, with the degradation of wirebond introduced in chapter 4-1, the routing is simplified as the two-dimension copper trace connection problem. Limited by the fabrication process, the routing space can be substituted with a two-dimension binary array of 1 mm× 1mm square. “0” represent no copper trace while “1” means copper trace. The two-dimension binary array needs to be converted to one-dimension to obtain easy crossover and mutation operations. One representation example is shown in Figure 4-15.

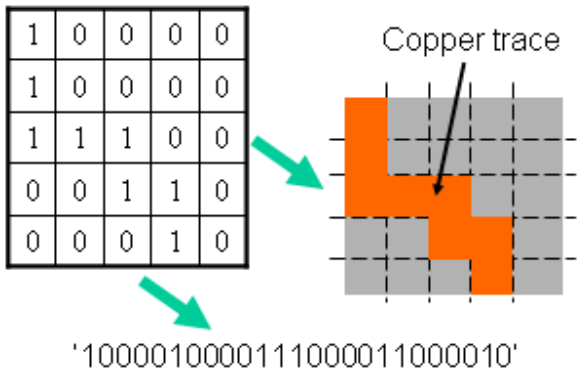


Figure 4-15. Routing area representation.

The initial population will be randomly generated and chosen from the candidates that follow the electrical connections. The size of population is chosen based on the placement rectangle area. The fitness evaluation requires considering the parasitic resistance, parasitic inductance and also footprint area. In this report the fitness is expressed in,

$$F = \frac{L_{\text{parasitc}}\, R_{\text{parasitc}}}{A_{footprint}} \tag{3-1}$$

In the equation, F is the fitness, $L_{parasitic}$ is the commutation path total parasitic inductance, $R_{parasitic}$ is the commutation path total parasitic resistance and $A_{footprint}$ is the footprint area. The parasitic resistance is calculated from circuit KCL equations while parasitic inductance is calculated based on boundary element method (BEM) to reduce the fitness evaluation time.

In order to calculate the parasitic parameters, the current conduction paths (conductor nets) need first identified based on the electrical connections as well as the physical routing results. From the literature, the external power terminals of power module (leadframe connections to substrate) are assigned as “sink” while the terminals of dies are assigned as “source”.

After identification of current conduction paths, in each conductor net the sink will be applied with 2 V, one source will be applied with 1 V and all other sources include in other conductor nets will be applied with 0 V. The routed copper traces will be gridded as small squares and each square is assumed to have an evenly distributed average voltage value. The circuit KCL equations can be listed for each square by assuming that current can only conducted from the top, bottom, right and left adjacent squares. By solving the KCL equations, the current go through each square can be obtained. The total current for can be achieved by adding up all the current in squares of terminal region. In each

conductor net, calculation for current will be implemented separately for each source. Every conductor net will go through this procedure to obtain all the currents.

As introduced in [92], the parasitic resistance matrix can be calculated based on the voltages and the currents. One example is shown in Figure 4-16.

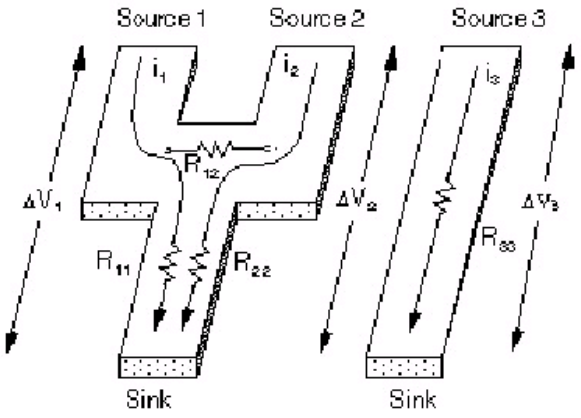


Figure 4-16. Resistance matrix calculation example.

The voltage drops are given by:

$$\begin{cases} \Delta V_1 = i_1 R_{11} + i_2 R_{12} \\ \Delta V_2 = i_2 R_{22} + i_1 R_{12} \\ \Delta V_3 = i_3 R_{33} \end{cases} \tag{3-2}$$

This can be expressed in matrix form as:

$$\begin{bmatrix} \Delta V_1 \\ \Delta V_2 \\ \Delta V_3 \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & 0 \\ R_{12} & R_{22} & 0 \\ 0 & 0 & R_{33} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{3-3}$$

Where, R_{11},R_{22} and R_{33} are the self resistance of each current path. R_{12} is the mutual resistance between path 1 and 2. Mutual resistance only applies to the current paths

within the same conductor net. The parasitic resistance can be calculated with above equations.

Next, the system computes the magnetic vector potential, A, given by:

$$A = \frac{\mu_0}{4\pi} \sum_V \frac{J}{r} dV \tag{3-4}$$

In the equation, J is the current density which can be calculated above. The inductance matrix is then computed using the relationship:

$$L_{ij} = \sum_V A \cdot J_j dV \tag{3-5}$$

With the calculated parasitic resistance and inductance, the routing results can be evaluated and the fitness can be used in GA iterations. Since the "DNA" string in routing is conventional binary string, the crossover and mutation will follow the conventional operation as introduce in Chapter 4.4.

4.4.4 Example of Automatic Layout Design

In order to better explain the GA utilized in the automatic layout design, one design example is show in Figure 4-17.

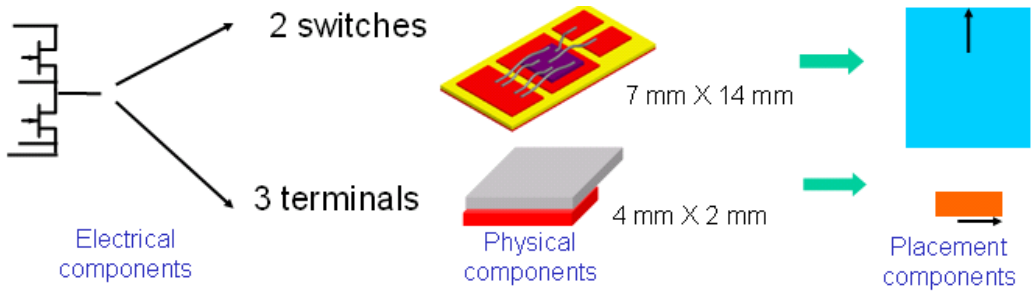


Figure 4-17. Automatic layout design example.

The example focuses on a phase-leg power module which has two power switch and three terminals. In the placement process, the switches and terminals are represented by two types of orientated rectangles. The size of initial population of outer loop is selected as 40 and the largest gaps are 4 mm in this example. After 50 iterations, the best solution is found as described in Figure 4-18.

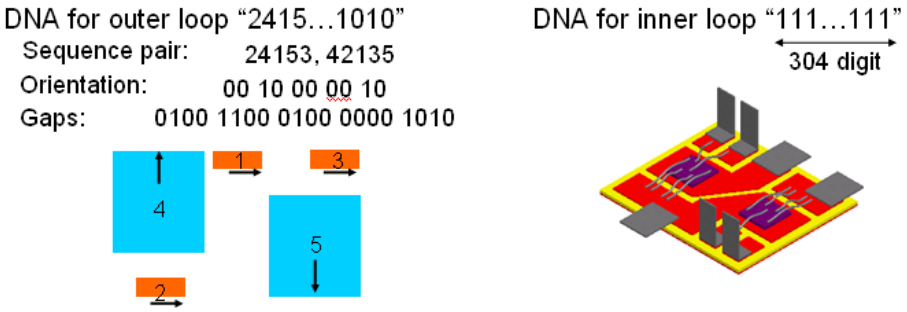


Figure 4-18. Automatic layout design result.

This example is also tried to design manually and the best solution are similar. The design results is also verified by Ansoft Q3D, and compared with other layout design the automatic design results is always better.

4.5 Summary of Layout Design for Power Module

This chapter presented the layout design of high power density power module. Some practical considerations are introduced for the optimization of electrical performance of the module. Together with the design example, the manual design and automatic design process are presented separately. The automatic design procedure could be a major step to improve the overall performance for future layout design.

Chapter 5 Thermal Management of Thermal Module

In order to design a converter with high power density, it is necessary to minimize the weight of the cooling system for a given maximum tolerable thermal resistance. Many cooling methods can be used to handle power losses in power converters. Sometimes, simple heatsink-fan cooling system can be advantageous in achieving minimum weight. This is because equipments in other cooling methods, such as pipe, pump, coolant, and coolant-to-air heat exchanger will contribute to a large increase in the weight of the total system. In this report, a power module with a forced-air cooling system will be discussed.

Optimizing the heat sink geometry for a certain fan could be done by numerical FEA-simulations. However, this process is very time consuming and often shows numerical instability. The optimization procedure using numerical simulation needs repeating try-and-error procedure with no guarantee to find all local optima [93]. As alternatives, empirical equations and analytical models are developed by people and are proven to be accurate to describe a large range of different geometries.

During the last two decades, researches have been contributed to optimal parametric study to modify the analytical models. An early work was presented by Sparrow et al. [94] for forced convection cooled and shrouded plate-fin array. Bar-Cohen and Rohsenow [95] developed a composite relation for the variation of heat transfer coefficient along the parallel plate surface to provide the analytic optimizing fins spacing. Wirtz et al. [96] presented flow bypass effects on plate-fin heat sinks. Teertstra et al. [97]

presented an analytical forced convection model for the average heat transfer rate from a plate-fin heat sink flow. Lee [98] introduced a practical guideline for selecting heat sinks and recommended the use of a developing flow correlation. In the recent optimization of heat sink contributed by Culham and Muzychka [99], a parallel- fin heat sink was parametric studied. In their paper, entropy generation is used as the criteria in the optimization. Shih in [100] presents a formal systematic optimization process to plate-fins heat sink design for dissipating the maximum heat generated from electronic component by applying the entropy generation rate to obtain the highest heat transfer efficiency. In [101,102], Kolar gave out the theoretical limit of the cooling system power density of a converter system employing forced air-cooling, and the heat sink is carefully optimized in terms of power density. A cooling system performance index (CSPI) is used to make direct comparisons of different cooling systems (heat sink plus fan) concerning the possible power density. However, flow bypass are not discussed in [93-104].

At the same time, in [103] Teertstra and Culham gave a summary of previous work on flow bypass characteristics in plate-fin heatsink and presented their own model to calculate the flow bypass. With a comprehensive analysis, Culham in [104] gave out the procedure to calculate the accurate flow bypass in the duct and simple empirical equations which is accurate enough for analytical design.

In this paper, an analytical model is presented to combine the heatsink, fan and duct together and can accurately predict the thermal performance of heatsink-fan cooling

system. Based on this model, an optimization procedure is developed to pursue the minimum weight of heatsink-fan cooling system.

5.1 Important Parameters in Thermal Management

The simplest and the most popular heatsink-fan cooling system is a plate-fin heat sink with horizontal inlet cooling stream, shown in Figure 5-1, where a suitable fan is mounted facing the fins and a vent in the opposite direction of the fan.

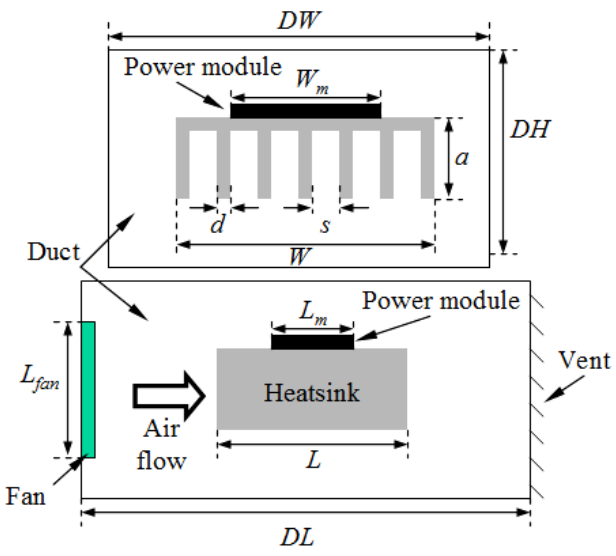


Figure 5-1. Geometrical configuration of heat sink, fan and duct.

The performance of the heatsink-fan cooling system mainly depends on the parameters which are shown in Figure 5-2. Some of the parameters are contributed to the total weight of the cooling system.

As described in [100], all parameters have tight relationship with the thermal management. The conductive thermal resistance and convection area are defined by

heatsink geometry. Heatsink geometry also works together with the fan characteristics to define an operating point (air flow at a certain pressure drop). The coefficient of convection is strongly dependent on this operating point. The effect of the heatsink geometry is parametrically discussed in section IV.

As shown in Figure 5-3, heatsink material with a high thermal conductivity and low specific weight is available for heatsink manufacture. If high thermal conductivity material is used, the fin thickness could be reduced. Therefore, the number of fins can be increased so that the total fin surface increases accordingly with a limited heatsink width while fan operating point is adapted to another optimum. A smaller value of total weight can be achieved. However presently, this potential of weight reduction is limited by manufacture capacity [101].

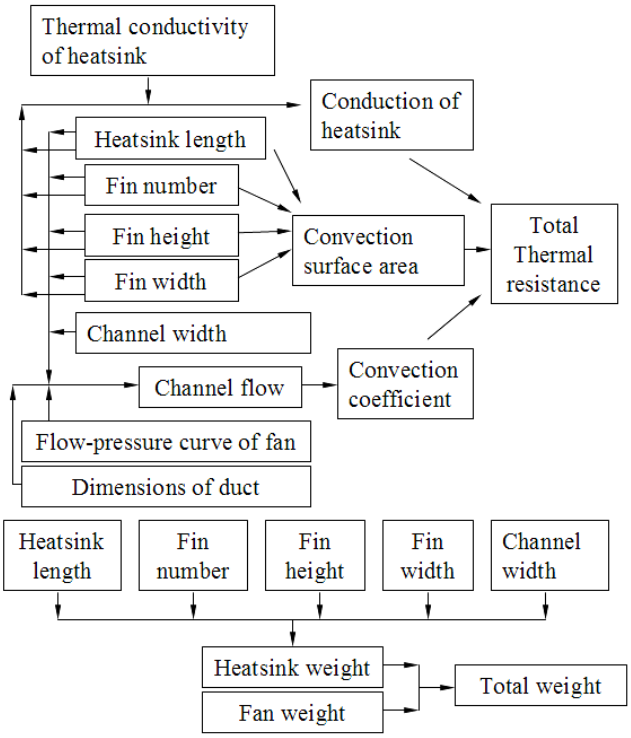


Figure 5-2. Important parameters of force-air cooling system.

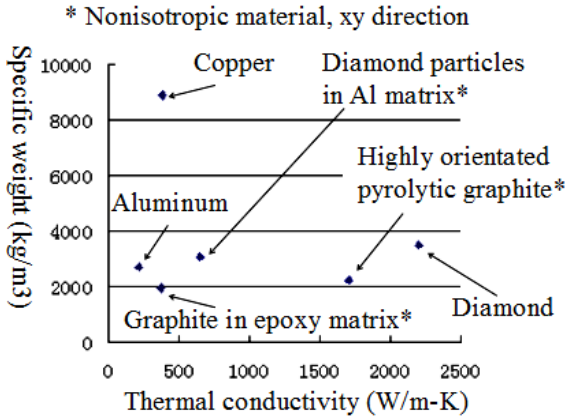


Figure 5-3. Thermal conductivity and specific weight of heatsink material.

Fan is also a crucial factor affecting both convection and weight. As shown in Figure 5-4, standard tubeaxial fan weight ranging from 7.5g to 20g showing a group of flow characteristic curves. Unlike the fan laws in [102,103], which indicate the relationship

between fan volume, air flow and static pressure [103], there is no explicit equation describes the relationship between fan weight and flow characteristic curve. However, usually larger air flow and larger static pressure require a larger fan weight.

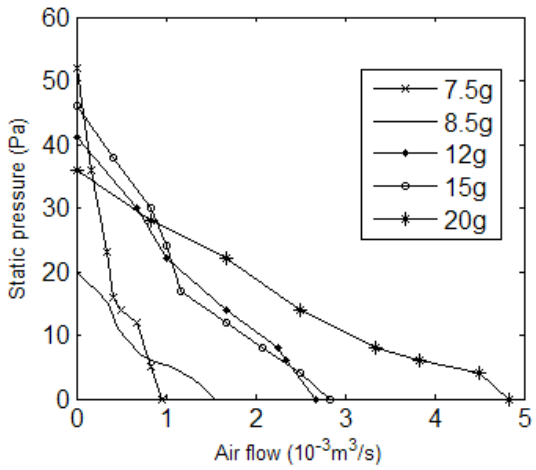


Figure 5-4. Typical relationship of fan weight, air flow and static pressure.

Usually, the cross sectional profile of flow duct is larger than those of heat-sink and fan, there will be a certain amount of flow bypass, which is strongly related to the cross sectional geometry of duct and the pressure drop across the heatsink. With the simple empirical equation given by Culham in [104] and some of the approximations, equations are derived to predict air flow produced by heatsink, fan and duct.

In general, analytical model can be built to indicate thermal resistance and the total weight defined by heatsink, fan and duct. Based on the model, by using the algorithm listed in Table 5-1, a minimum total weight can be obtained within a given thermal resistance.

Table 5-1 Optimization Algorithm for Forced-Air Cooling System

Design parameters	$X=[n,d,W,L,a,v_{ch}]^T$
Design target	W_{total}
Subject to	n is integer, n >1
	$DW > d > 1$ mm
	$DW > W > W_m$
	$DL > L > L_m$
	$DW > s > 1$ mm
	$DH > a > 0$
	$V_{ch} > 0$
	$R_{total} < (T_c - T_a)/P$
	P_{fan} and V_{fan} should be on fan curve

In this algorithm, Fin number, fin thickness, channel width, heatsink length, fin height and channel velocity are selected as the variables. The dimensions of heatsink are mainly restricted by the dimension of duct. Fin thickness and channel width is also restricted by the manufacturability. The heatsink width and length is also restricted by the dimension of power module. The total thermal resistance between power module and ambient and the fan operation point is the main nonlinear restricts in the optimization procedure.

5.2 Analytical Thermal Model

In Figure 5-5, the equivalent circuit of thermal resistances given by [66] describes the heat transfer from the heat sink base into the air for one channel. Analytical thermal resistance can be calculated based on this equivalent circuit.

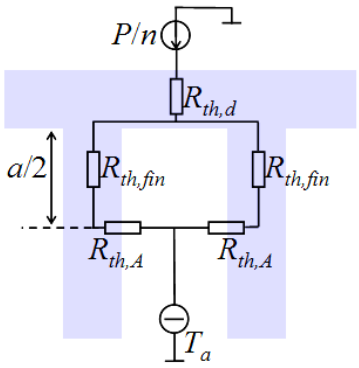


Figure 5-5. Equivalent circuit of force-air cooling system.

The overall thermal resistance of the total finned surface from the fundamental heat transfer [67] is written as

$$R_{total} = R_{th,d} + \frac{1}{2n}(R_{th,fin} + R_{th,A}) \tag{4-1}$$

where

$$R_{th,d} = \frac{b}{W \cdot L \cdot k} \tag{4-2}$$

$$R_{th,fin} = \frac{a}{d \cdot L \cdot k} \tag{4-3}$$

$$R_{th,A} = \frac{1}{h \cdot L \cdot a} \tag{4-4}$$

In (4-4), h is the convective heat transfer coefficient that can be computed using the model developed by Teertstra et al.[97]

$$h = \frac{N_u \cdot k_f}{s} \tag{4-5}$$

In (4-5), k_f represents the fluid thermal conductivity. N_u is modified from fully-developed and developing channel flow presented by Teertstra et al. [97], thus the Nusselt number can be written in the following

$$N_u = \left[\left(\frac{R_{es}^* P_r}{2} \right)^{-3} + \left(0.664 \sqrt{R_{es}^*} P_r^{\frac{1}{3}} \sqrt{1 + \frac{3.65}{\sqrt{R_{es}^*}}} \right)^{-3} \right]^{-\frac{1}{3}} \tag{4-6}$$

where the modified channel Reynolds number is defined as

$$R_{\mathrm{es}}^* = \frac{R_{es} \cdot s}{L} \tag{4-7}$$

The Reynolds number is defined as

$$R_{es} = \frac{s \cdot V_{ch}}{\nu} \tag{4-8}$$

The pressure drop of heatsink defined by heat sink geometry can be obtained by [104]

$$\Delta P = \left(f_{app} \cdot \frac{n \cdot (2a \cdot L + s \cdot L)}{a \cdot W} + K_c + K_{\mathrm{e}} \right) \frac{\rho \cdot V_{ch}^2}{2} \tag{4-9}$$

f_{app} is the apparent friction factor for a hydrodynamically developing flow. This parameter for a rectangular channel can be evaluated by using the following laminar flow formulation developed by Muzychka [99]

$$f_{app} = \frac{1}{R_{eDh}} \left[\left(\frac{3.44}{\sqrt{L^*}} \right)^2 + \left(f \cdot R_{eDh} \right)^2 \right]^{\frac{1}{2}} \tag{4-10}$$

where,

$$L^* = \frac{L}{D_h R_{eDh}} \tag{4-11}$$

$$D_h = \frac{2 \cdot s \cdot a}{s + a} \tag{4-12}$$

$$R_{eDh} = \frac{V_{chDh}}{\nu} \tag{4-13}$$

The coefficients K_c and K_e in (4-9) is a parameter for sudden contraction and expansion, respectively, can be expressed as:

$$K_c = 0.42\left[1 - \left(1 - \frac{N \cdot d}{W}\right)^2\right] \tag{4-14}$$

$$K_e = \left[1 - \left(1 - \frac{N \cdot d}{W}\right)^2\right]^2 \tag{4-15}$$

A Reynolds number group in (10) can be written in (4-16)

$$\begin{aligned} f \cdot R_{eDh} = 24 - 32.527\left(\frac{s}{a}\right) + 46.721\left(\frac{s}{a}\right)^2 - 40.829\left(\frac{s}{a}\right)^3 \\ + 22.954\left(\frac{s}{a}\right)^4 - 6.089\left(\frac{s}{a}\right)^5 \end{aligned} \tag{4-16}$$

In [104], Culham gave out a approximation equation to express the correlation of channel velocity and free stream velocity with considering the dimensions of duct.

$$V_{ch} = V_f\left(\frac{s + d}{s}\right)\left[1 - (L_1 \cdot a_1)^{0.125}\right] \tag{4-17}$$

Where,

$$L_1 = \frac{L}{R_{ed} \cdot D_{hd}} \tag{4-18}$$

$$D_{hd} = \frac{2 \cdot DW \cdot DH}{DW + DH} \tag{4-19}$$

$$a_1 = \frac{DW \cdot DH}{s \cdot a} \tag{4-20}$$

Generally, the static pressure of the fan is related to a pressure drop of heatsink and duct geometry. In this paper, an empirical expansion coefficient is adopted to indicate the relationship.

$$K_{e,fan} = \left[1 - \left(\frac{l_{\text{fan}}^2}{DH \cdot DW} \right)^2 \right]^2 \tag{4-21}$$

$$P_{fan} = \Delta P - \frac{K_{efan} \cdot \rho \cdot V_f^2}{2} \tag{4-22}$$

The air flow of the fan can be approximately obtained as,

$$V_{fan} = V_f \cdot DH \cdot DW \tag{4-23}$$

The total weight of heatsink-fan cooling system is given by

$$W_{total} = \rho_h \, (b \cdot L \cdot W + n \cdot a \cdot d \cdot L) + W_{fan} \tag{4-24}$$

With the above equations, the total thermal resistance can be calculated by given heatsink geometry and channel velocity. At the same time, the static pressure and air flow requirement of fan can also be calculated from the heatsink geometry and channel velocity. Thus, the model which can predict the thermal performance and total weight is established.

5.3 Example of Parametric Study

In this section, a practical heatsink-fan cooling design example is discussed by using the analytical model in Chapter 5.1 and the algorithm in Chapter 5.2. The task is to determine the optimal heatsink geometry and optimal fan with a given thermal resistance.

Table 5-2 Study Parameters of Design Example

Item	Description
Power module	20mm × 20mm × 2mm

	SiC devices Power loss: 80 W Junction temperature: 250 °C Case bottom temperature: 230°C
Heatsink material	Aluminum (k= 200W/m-K)
Duct dimension	60mm × 60mm × 60mm
Fan	NMB DC Series Input voltage: 12V Input power < 3.3W Noise < 40dB
Ambient temperature	30°C

Table 5-2 lists the main specification of the example. Because the duct dimensions are usually confined by other electrical and mechanical components, here a set of constant value is used. Restricted by manufacturability, the thickness of the base is also set as a constant value as 4 mm.

As shown in Table 5-3, the main properties of each type of the fan are listed [105]. By browsing datasheets of different vendors, it can be found that fans with the same size usually have the same weight but different in flow characteristic curves. The maximum air flow and maximum static pressure will simultaneously increase when the input power and noise increase. Thus within the limit of input power and noise, a most powerful fan can be directly selected as a candidate for a certain fan size.

Table 5-3 Candidate Fan Properties Sorted by Weight

Fan part number	Weight	Max air	Max static	Dimensions	Fan

	(g)	flow $\times 10^{-3}$ (m^3/s)	pressure (pa)		label
1004KL04WB50	7.5	0.057	50.6	25 mm × 25 mm ×10 mm	1
1204KL04WB50	8.5	0.110	54.0	30 mm × 30 mm ×10 mm	2
1404KL04WB50	12	0.160	41.0	35 mm × 35 mm ×10 mm	3
1604KL04WB50	15	0.17	46.0	40 mm × 40 mm ×10 mm	4
2004KL04WB50	20	0.29	35.0	30 mm × 30 mm ×10 mm	5
1608KL04WB50	25	0.27	69.4	40 mm × 40 mm ×20 mm	6
1204KL04WB50	25	0.39	109.7	40 mm × 40 mm ×28 mm	7
2106KL04WB50	25	0.4	35.0	50 mm × 50 mm ×15 mm	8
2404KL04WB50	25	0.54	30.1	60 mm × 60 mm ×10 mm	9
2406KL04WB50	45	0.52	51.2	30 mm × 30 mm ×10 mm	10
2410RL04WB80	65	0.81	69.1	30 mm × 30 mm ×10 mm	11

On the other hand, fans with different size may have a same weight but different fan characteristic curves. For example, Fan label 6,7,8,9 have a same weight as 25g and a large discrepancy in air flow and static pressure. They should be all selected as candidates because any of them can be the best with some certain heatsink geometry and duct geometry.

By using the algorithm in chapter 5.2, the optimization is conducted by using optimization toolbox of MATLAB. In order to simplify the procedure, the flow characteristic curve is expressed as a 5th order approximation.

Table 5-4 Parametric Study Example

Parameters	Normal value (mm)	Optimization range (mm)
Heatsink lengh (L)	30	20~40
Heatsink height (a)	20	15~40
Fin width (d)	1.5	1~5
Gap length (s)	2	1~5
Fin number	10	2~30

Table 5-4 lists all the parameters in the optimization. Figure 5-6 shows the optimization results for different fan labels.

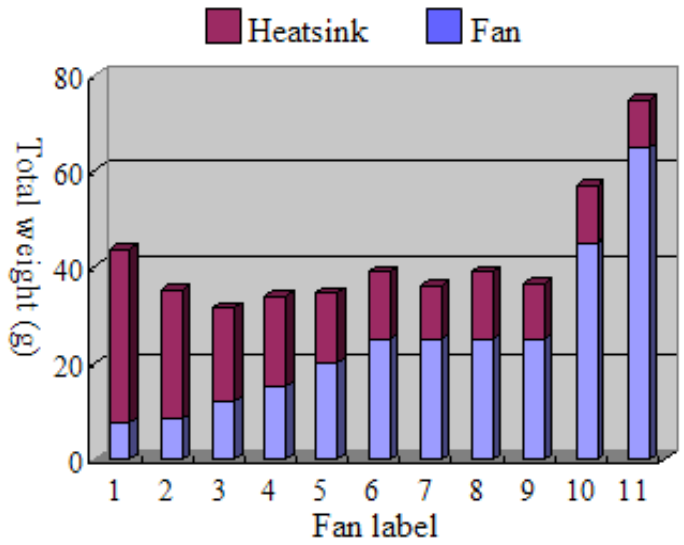


Figure 5-6. Optimized weight with the module operated in 250°C.

Initially, a light fan with a small flow capacity requires a large heatsink which also has a relatively larger weight. As the weight of fan increased and the flow capacity improved, relatively smaller heatsink is required and the total weight of cooling system is reduced. When the fan capacity continues to increase, the increasing speed of fan weight will exceed the reduction speed of heatsink weight. The total weight will rise again and an optimum value of total weight can be obtained.

A minimum value of total weight is 31.3 g by using the fan of label 3. Table 5-5 shows the detailed geometry value of heatsink with label 3 fan.

Table 5-5 Geometry of Heatsink with the Fan Label 3

n	d (mm)	s (mm)	W (mm)	L (mm)	a (mm)
13	1	1.42	30.0	20	23.4

The variables of heatsink geometry can be swept near the optimum with given thermal resistor. The relationship between variables and total weight can be analyzed.

Figure 5-7 shows the relationship between the fin number and the total weight with given thermal resistance. A larger fin number will bring larger convection area and thus reduce the thermal resistance. On other hand, larger fin weight and larger base weight will be obtained with larger fin width.

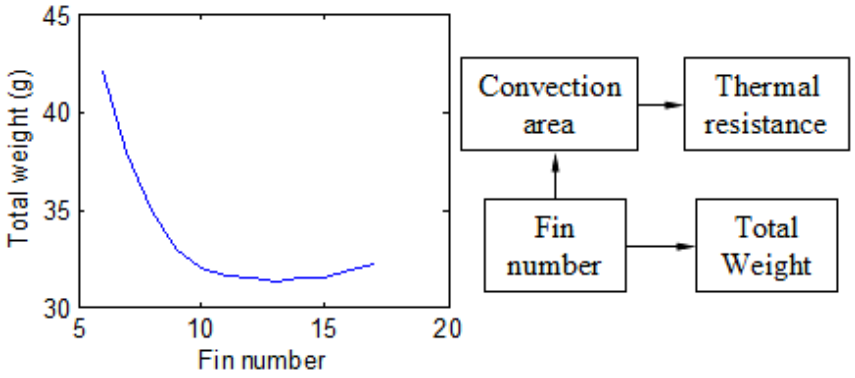


Figure 5-7. Relationship between fin number and total weight.

Figure 5-8 shows the relationship between the heatsink length and the total weight with given thermal resistance. Increasing the heatsink length L in air flow direction will increase the total fin surface and in addition the heat transfer. However the air pressure drop in the channels is also increased and it will change the fan operating point and finally brings an increasing total weight. At the same time, heat transferred by long L will increase the temperature of channel air fast.

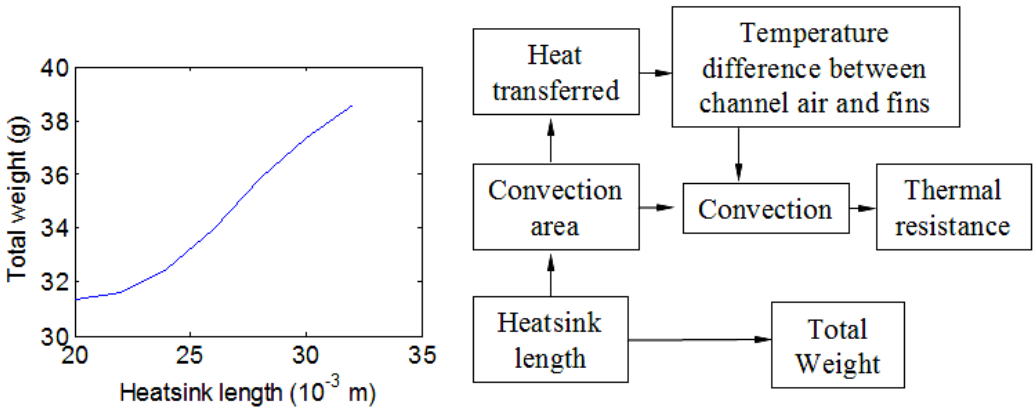


Figure 5-8. Relationship between heatsink length and total weight.

If the temperature rise along the channel is too high and results in fully developed air flow, the temperature gradient between fin surface and channel air will be very small after a certain length. The fins after this length will not contribute much to heat transfer. It will not only add useless weight but also bring an additional pressure drop with negative impact on the fan operating point.

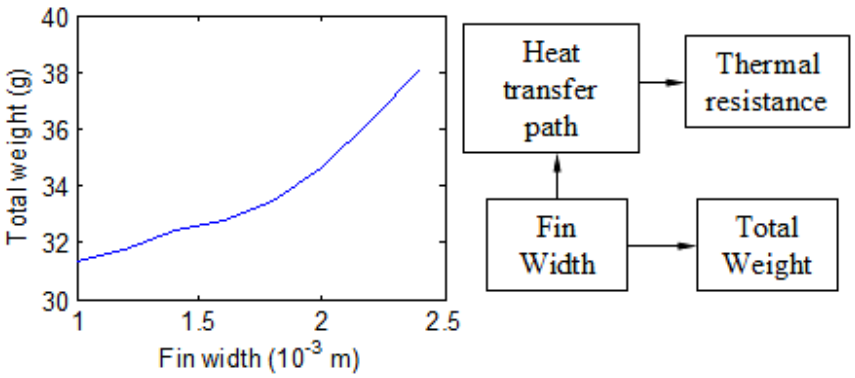


Figure 5-9. Relationship between fin width and total weight.

Figure 5-9 shows the relationship between fin width and the total weight with given thermal resistance. The fin thickness has to be large enough to allow heat flow through

the whole height of the fin. If the fin is too thin, a large conduction thermal resistance may be obtained. On the other hand, fin thickness is restricted by manufacture capacity and may change the weight of heatsink significantly.

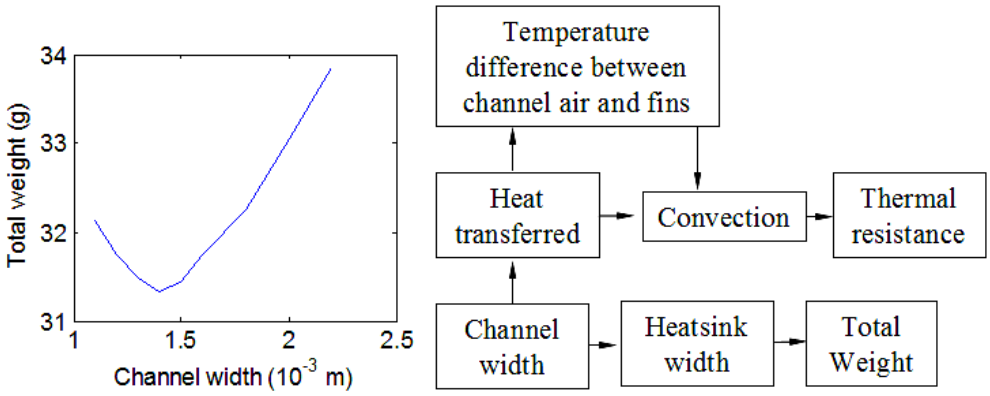


Figure 5-10. Relationship between heatsink length and total weight.

Figure 5-10 shows the relationship between heatsink length and the total weight with given thermal resistance. A small channel width s gives a large Reynolds number resulting in a large Nusselt number. This means good convective heat transfer from surface into air at the beginning parts of fins. On the other hand, it also means low speed volume flow which transfers the heat slowly. The slow heat transfer will raise the channel temperature fast, and thus brings a negative impact on convection of end parts of fins.

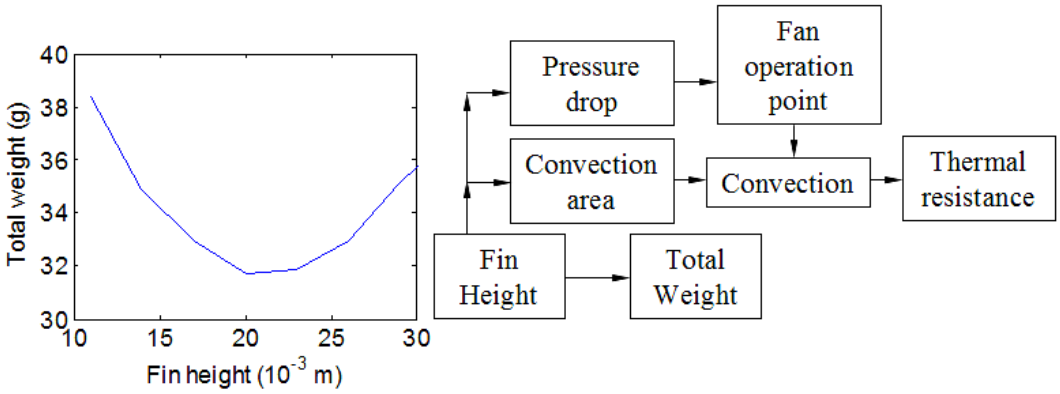


Figure 5-11. Relationship between heatsink height and total weight.

Figure 5-11 shows the relationship between heatsink height and the total weight with given thermal resistance. A larger fin height will bring larger convection area and at the same time the larger weight. The fin height also affects the hydraulic diameter which defines the pressure drop required by the heatsink. The operation point of fan is related to the hydraulic diameter and the convection will be affected.

The above variables of heatsink geometry coupled together to affect the thermal resistance and the total weight. In order to obtain the optimum, tradeoffs between variables must be balanced in the value selection.

Table 5-6 Settings in the FEA Simulation (I-DEAS)

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	473200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

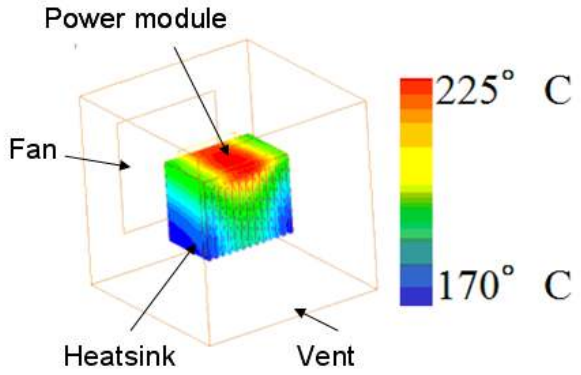


Figure 5-12. Simulation result by I-DEAS.

Numerical FEA-CFD co-simulation software I-DEAS is used in the verification. In the software, the flow curve of label 3 fan is input as the characteristic description. The settings of I-DEAS are listed in Table 5-6. Optimum geometry in section IV is set to the heatsink. Figure 5-12 shows the simulation results.

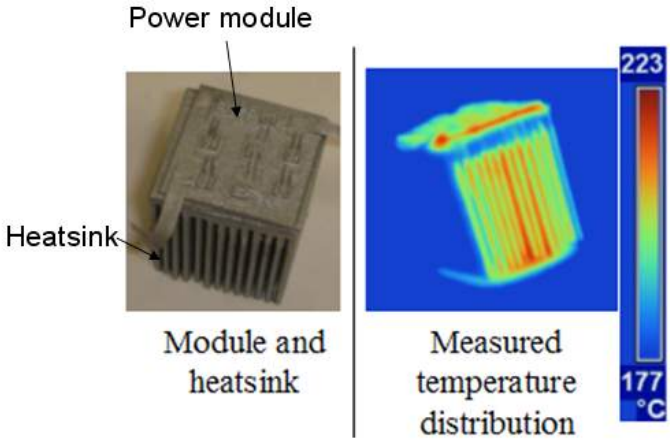


Figure 5-13. Prototype power module, heatsink and experiment results.

A prototype power module and heatsink emulating the optimum are built. Infrared camera is used to measure the temperature which is shown in Figure 5-13.

From Figure 5-12 the thermal resistance can be calculated as 2.52 K/W. From Figure 5-13 the thermal resistance can be calculated as 2.47 K/W. The analytical model in section II predicts the thermal resistance as 2.5 K/W. The analytical model agrees well with the simulation and experiment. Since the deviations are acceptable, the analytical model and optimization procedure presented can give a design guideline for finding the optimum with confidence.

5.4 Summary of Thermal Management

A systematic optimal design process and parametric study of the heatsink-fan cooling system by applying the analytical model is described in this chapter. The presented thermal design method is confirmed by numerical simulation and experiments. The optimization procedure is accurate enough to pursue a minimum weight of heatsink-fan cooling system with a given thermal resistance.

Chapter 6 Electrical Evaluation of Power Module

In most literatures [21-40], the test and evaluation procedure and methodology for the package supporting SiC devices are either not explicit described or are inadequate. As listed Table 6-1, failures happened because the lack of detection methods in the procedure presented in literatures and also not conducted in prototype tests in this dissertation.

Table 6-1 Failure in the Prototype Test

Potential defects and detection method	Testing procedure in literatures	Failure in the prototype test of this dissertation
Poor encapsulant should be detected by static I-V test	Undemonstrated in testing of SiC JFET converter of APEI [23]	Break down at 500V (should be 1800 V)
Power die-attaching should be detected by DC current conduction test	Undemonstrated in testing of SiC JFET converter of Kyoto University [26]	Die burnt by local overheat
Die degradation should be detected by double-pulse test	Undemonstrated in testing of SiC BJT converter of Air Force Lab [27]	Die destroyed in the continuous power test

In order to obtain a high quality design, it is essential to follow some procedure to determine the feasible high temperature SiC package and reduce the risk. A systematic

electrical evaluation procedure to conveniently and safely detect the potential defects in the high temperature package is highly preferred.

6.1 Potential Defects in Fabrication Process

During the power module fabrication process, many critical problems are easily encountered. Usually, the first step is the die-attaching and it is crucial because a poor die-attachment can lead to a local over-heat and thus destroy the devices (shown in Figure 6-1). It is also critical to have a high quality bonding between the leadframe and substrate, especially for the multi-chip power module. Unlike other fabrication processes, once the soldering is finished, it is difficult to repair or repeat because of the difficulty in controlling the heating up process without affecting the soldering of other components [14].

In order to obtain high quality soldering, the vacuum reflow process is recommended for die-attachment because it can significantly reduce the probability of the void and prevent the oxidations on the surface of the components in the hot environment [14]. For die-attachement, solder preform is better than solder paste since it can be more evenly distributed between components and substrate during the soldering process. In addition, it is preferable to add a certain pressure to the solder layer to reduce the void and improve quality, especially for large area die-attaching and multi-chip die-attaching.

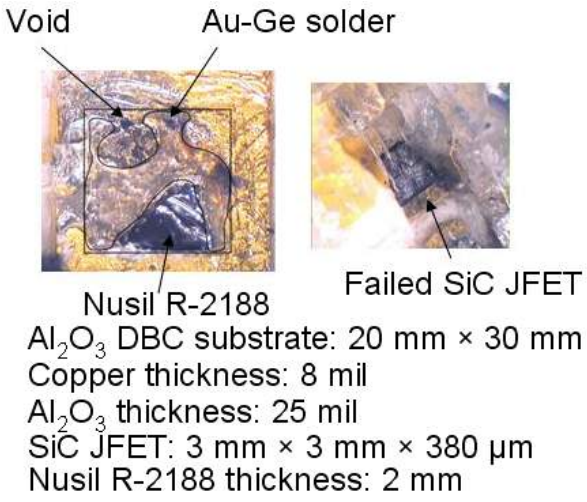


Figure 6-1. Poor die-attachment and failed device.

The next step is wirebonding, which is a mature, reliable and repeatable bonding processing. However, when bonding with new SiC chips, poor quality interconnections between top pads of device and traces on substrate can easily form without prior experience and proper control. Since the location and length of wires are difficult to be unified, it is very possible to form poor bonding. Weak interconnection and damage of pads are the most likely result of poor wirebonding.

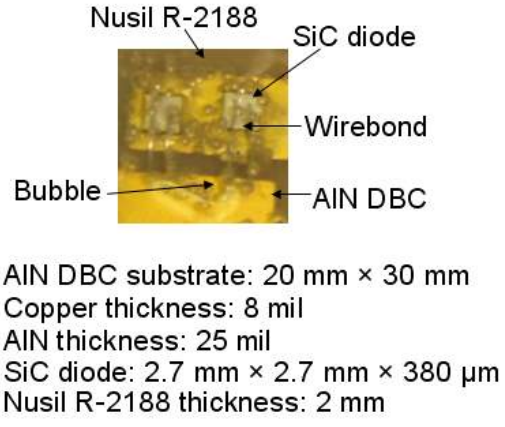


Figure 6-2. Poor encapsulant.

The last step is encapsulation. In many cases, different parts need to be mixed before coating and curing. Bubbles are easily formed (shown in Figure 6-2) in the mixing process and it is vital to pump them out. Otherwise, bubbles can cause discharge and break down, which will reduce the power rating of the power module.

Limited by the manufacturability, the stability of SiC semiconductor is still an issue, especially related to high temperature aging or thermal cycling. In the fabrication process, there is several times heating up and cooling down. The degradation of the dies may happen during the temperature changing, even though every fabrication step achieves high quality bonding or encapsulant. At the same time, limited by the material selection scope, fabrication equipments and fabrication experience, degradations of packaging materials may also exist during the temperature changing and result in power module failure.

There is also possibility of local overheat failure caused by poor layout design and thermal design, especially for multi-chip power module. The parasitic parameters in a power module may have a detrimental influence on the switching loss and the dynamic behavior. This phenomenon is exacerbated when the density increases. In the layout design procedure, limited by the design experience and choice of candidates, parasitic parameters may lack consistency and lead to local overheat, especially for paralleled devices. Moreover, power loss may be underestimated as a result of poor characteristic measurement, inadequate device model and inaccurate circuit analysis. It will cause an

incorrect cooling system design and the module may be operated higher than the design temperature.

6.2 Evaluation Procedure to Detect Potential Defects

Potential defects may exist in the power module packaging during the fabrication process as mentioned above. In the electrical evaluation tests, failures can occur due to one or more of these defects. If a power module were directly evaluated under full continuous power and failed in the test, the causes of the failure would be difficult to identify. In order to reduce the risk and detect potential defects quickly, the evaluation should follow a systematic procedure, as listed in Table 6-2.

Table 6-2 Potential Defects and Evaluation Procedure

Potential defects	Phenomenon	Evaluation procedure
Poor wirebonding	Weak interconnection	Static I-V characteristic test by curve tracer
	Device damage by stress	
Poor encapsulant	Break down below rated voltage	
Poor die-attachment	Die destroyed by local overheat	DC current conduction test
	Leadframe detached	
Die degradation in fabrication process	Slow turn-on, turn-off or incomplete switching	Double pulse test
Material degradation in long time high temperature operation	Breakdown or over current in high temperature	Continuous power test
Poor layout design	Irregular hotspot or local overheat	
Poor thermal design	Overheat	

Once the power module is fabricated, the static I-V characteristic needs to be evaluated first. As mentioned above, there are two main vital issues during the wirbonding process. One is weak interconnection, which means large contact resistance. In most of cases, it can be detected from the forward I-V curve if the on-resistance of

packaged device is much larger than that of bare die. The other issue is the damage of devices due to the over-stress in the boding process. It can be detected from the blocking I-V curve if the device cannot be turned off or the leakage current is much larger than normal value. At the same time, in the blocking I-V curve, if the leakage current suddenly increases under certain voltage which is below the rated value, it means the encapsulant is not well fabricated.

The next evaluation step is dc current conduction test, which examines the integrity and quality of die-attachment, connection to external circuit and wirebond quality. In this step, the rated dc current should be applied to the device individually and heat up the device to the rated junction temperature. In the test, a poor die-attachment will cause a local overheat and finally destroy the die. At the same time, a low quality soldering of leadframe will also lead to local overhead and will cause the sudden open circuit. If weak interconnection of wirebond is not detected in the first step, it can be found in this step by burnt wires. In this paper, each dc current test took 1 hour in steady-state to determine the quality of the die-attachment and connections.

The double pulse tests can be then conducted to examine the switching functionality of the devices with rated voltage and rated current at rated junction temperature. Without the continuous power loss, the power module needs to be heated up by a hotplate. The degradation of SiC dies during fabrication procedure can be detected if irregular slow turn-on and turn-off or incomplete switching happens. At the same time, the gate drive circuit can be iteratively adjusted to obtain the minimum power loss based on the

transient characteristics of switching. If a phase-leg module is tested, the cross-talking problem (top and bottom gate drive circuit interference due to the Miller capacitance) can also be investigated and attenuated.

Finally, continuous power test should be conducted if no failure happened in the previous tests. The power module can usually be operated as a buck converter and the continuous power loss will heat up the module. For phase-leg module, in order to determine the continuous operation capability of top devices and bottom devices separately, dc mode operation needs to be conducted before ac mode operation. In the latter test, all the switches are switched in each switching cycle and it is similar to most of the operation modes in converter system. The continuous test can help to find the degradation problem due to material selection and poor fabrication process. Furthermore, if irregularly large parasitic parameters exist in layout design, overheat will easily happen in the continuous test. Moreover, thermal design can be verified by the continuous test. In the test, switching frequency, duty cycle and other control related parameters can be adjusted to maintain the power module operation close to the real working condition. If unanticipated high temperature is detected in the test, the cooling system design needs to be modified.

As shown in Figure 6-3, the electrical evaluation circuit examples are illustrated based on the single device phase-leg power module. With the similar circuits, tests for single switch module and multi-chip power module can be easily conducted..

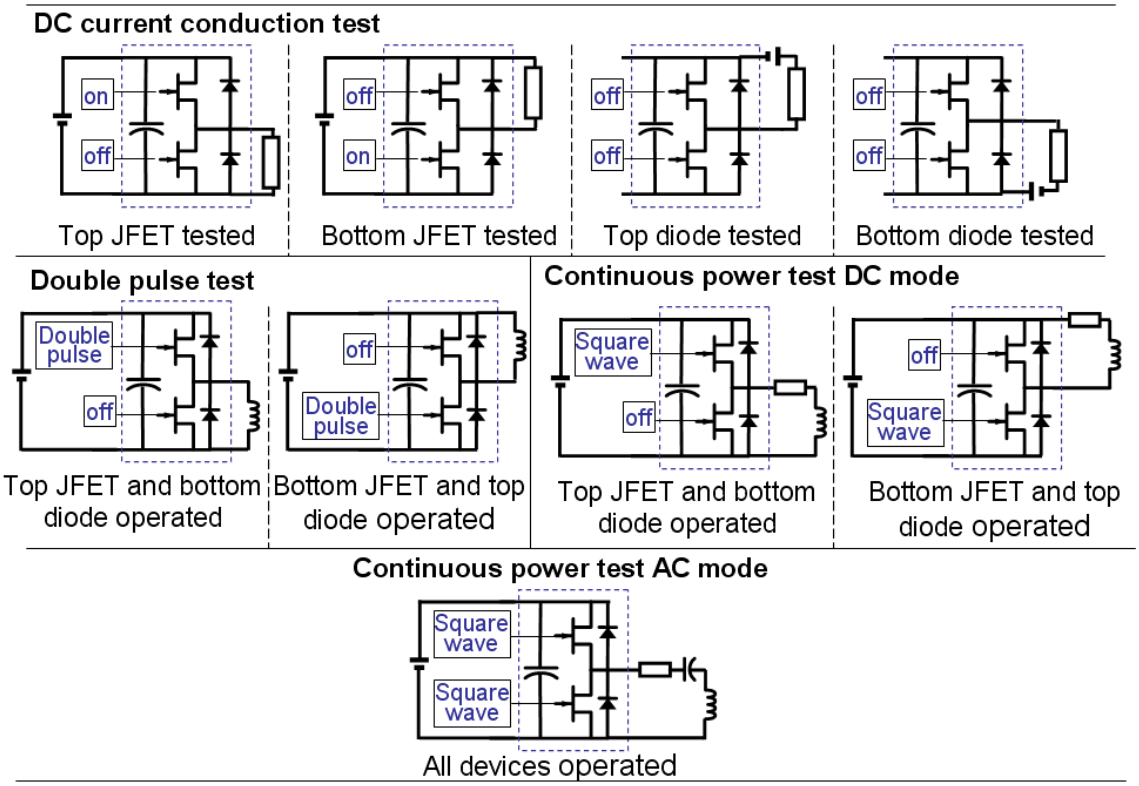


Figure 6-3. Electrical evaluation test schematic examples.

6.3 *Multi-Chip Module Development Procedure*

In order to reduce the risk of failure and get familiar with the operation characteristics, in the multi-chip phase-leg module development, some simple intermediate power module should be first fabricated and tested. For example, as multi-chip phase leg developed in this paper, a single switch power module and a single chip phase-leg module were tested before the full chip module. The test procedure and the objectives are listed in Figure 6-4.

The single switch power module uses the simplest topology, only one power switch and one diode. With this module, the selected materials and the packaging fabrication process can be electrically evaluated without involving many devices. The basic package functionality can be investigated. Especially for the unfamiliar materials, this step can help to determine the fabrication equipments, temperature profile, and environmental condition, and also improve fabrication skills.

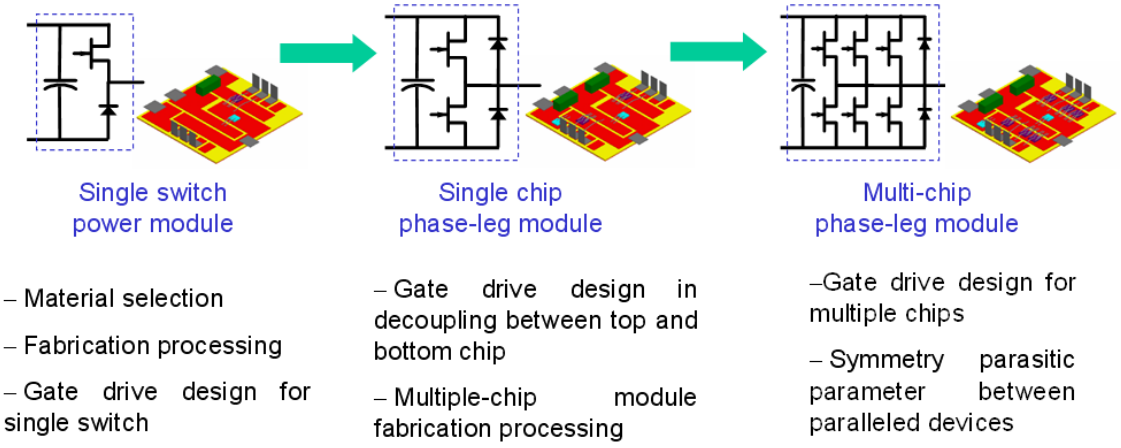


Figure 6-4. Multi-chip power module developing procedure.

In the following step, the single chip phase-leg module need to be tested. The phase-leg module is the basic building block in power electronics, with two power switches and two diodes making up the top and bottom part of the phase-legs. A phase-leg can be utilized to evaluate the gate drive circuit and also the fabrication process. Because of the Miller effect, the cross-talking problem can easily occur in the phase-leg module. Gate circuit topology and components can be adjusted to ensure no interference problems between top and bottom power switches. With more dies involved, it is difficult to heat up the individual die evenly or keep the consistency in each fabrication step. Small

unbalances in fabrication will lead to the possibility of failure. Thus, it is important to improve the details of fabrication process to make sure multiple dies have the same packaging quality.

Finally, the multi-chip power module can be fabricated and tested. From layout design point of view, in order to qualify the even distribution of parasitic parameters, the thermal couple should be embedded close to each die. In the continuous power test, the balance of gate drive circuit design can be also qualified from the thermal characteristics. The cross-talking issue and switching delay between paralleled devices need special attention.

6.4 Power Module Evaluation Example

In order to demonstrate the electrical evaluation procedure, a prototype multi-chip phase-leg module was developed (details shown in Chapter 7). The prototype power modules were fabricated as shown in Figure 6-5. Before continuous power test, all the defects detection steps and multi-chip module development procedures were went through. Several fabrication problems and gate drive circuit problems were identified and improved.

In the vacuum reflow process, the stencil to fix the substrate, perform and dies was redesigned and modified. In the meantime the stress applied to die-attachment was added to achieve the high quality soldering. In the wirebonding process, the wire thickness and settings of wirebond machine was adjusted to ensure there is no weak interconnection and device damage. The encapsulant curing temperature profile was improved based on

many trials. In double pulse test, gold wires bonded to non-gold finish were determined as unfit for high temperature operation. Gate drive circuit were also redesigned and adjusted to maintain a high speed turn-on and turn-off while not causing shoot-through.

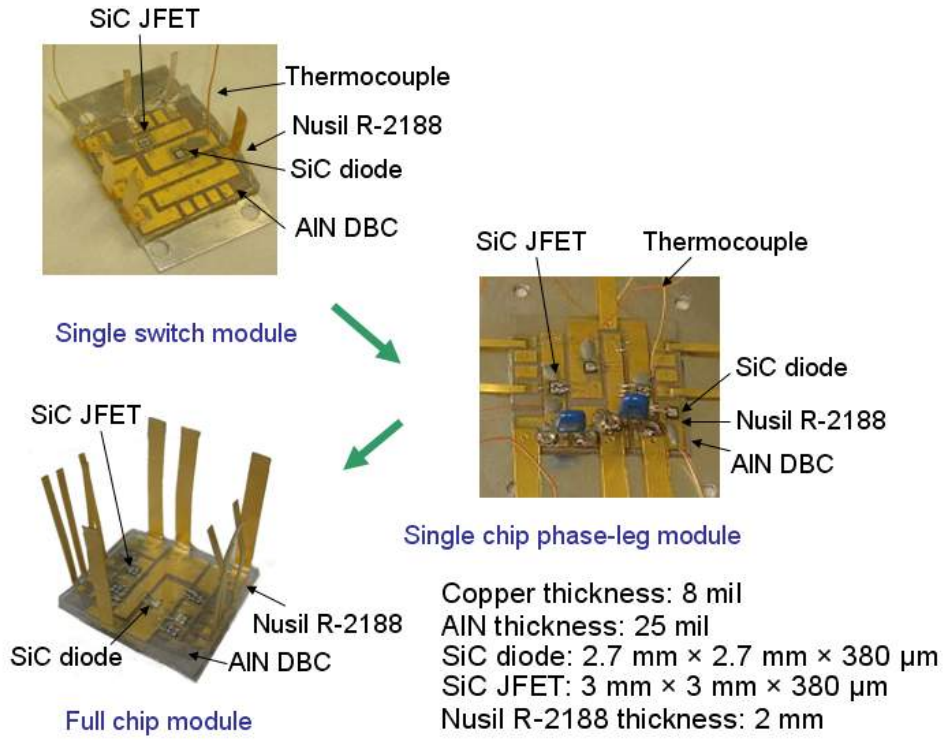


Figure 6-5. Multi-chip module development procedure.

The successful testing of prototype power module presented in Chapter 7 proves that the systematic test procedure can fast and safe detect the potential defects existing in SiC high temperature packaging and ensure the successful development of multi-chip module.

6.5 Summary of Power Module Electrical Evaluation

In this chapter, a safe and rapid electrical evaluation procedure is presented. The successful continuous power testing on prototype module demonstrates that electrical

evaluation procedure reduce the risk of failure and the designed package in chapter 2 can support the SiC semiconductor devices operating at 250 ºC junction temperature.

Chapter 7 Development Examples of High-Temperature Module

In order to demonstrate the presented SiC wirebond high temperature module and planar high temperature module development procedure, a multi-chip phase-leg module and a planar multi-chip phase-leg module were developed as examples. As shown in Figure 7-1, multi-chip phase-leg power module was selected as the design target. The phase-leg circuit is the most basic building block in power electronics, which can be used in various applications. Nevertheless, the proposed module construction concept can be easily adapted to other circuit configurations, such as three-phase inverters. The power module consists of six SiC JFETs, two SiC diodes and two high temperature decoupling capacitors.

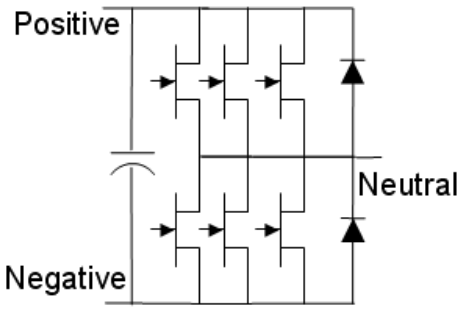


Figure 7-1. Design target of power module.

7.1 High-Temperature Module Design

7.1.1 Design of Wirbond Power Module

As introduced in Chapter 4, the layout for wirebond module was designed by considering the reduction of parasitic parameters and the balance of the paralleled devices. With the FEA simulation tools, several candidates are evaluated and compared. The final layout design is shown in Figure 7-2

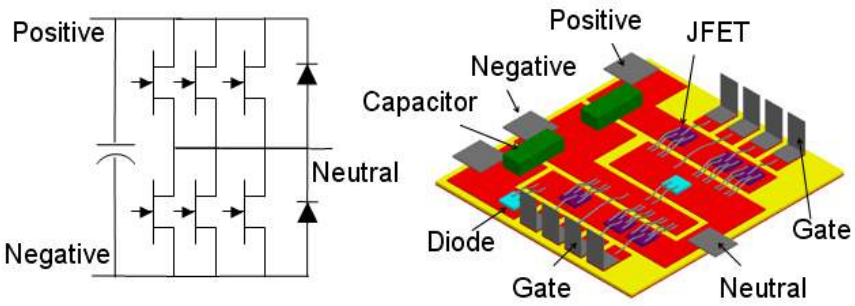


Figure 7-2. Layout design of wirebond module.

The cooling system is designed by following the process presented in Chapter 5. The conduction loss is calculated based on the static device characterization. The switching loss is calculated based on the double pulse test. The fan is still selected in Table 5-3 Candidate Fan Properties Sorted by Weight. The design based on 175 ºC junction temperature and 250 ºC junction temperature to show the advantages of high temperature converter. By consider the manufacturability, the minimum fin width is 1 mm and the minimum gap width is 2mm. Limited by the footprint of power module and the PCB mechanical supporter, the minimum width of heatsink is 50 mm and the minimum length of heatsink is 50 mm.

In 175 ºC junction temperature case, the power loss of each JFET is 10 W and power loss of each diode is 10.5 W. Figure 7-3 shows the design results of 175 ºC junction temperature. From Figure 7-3, the design case 3 have a minimum weight of 91.7 g.

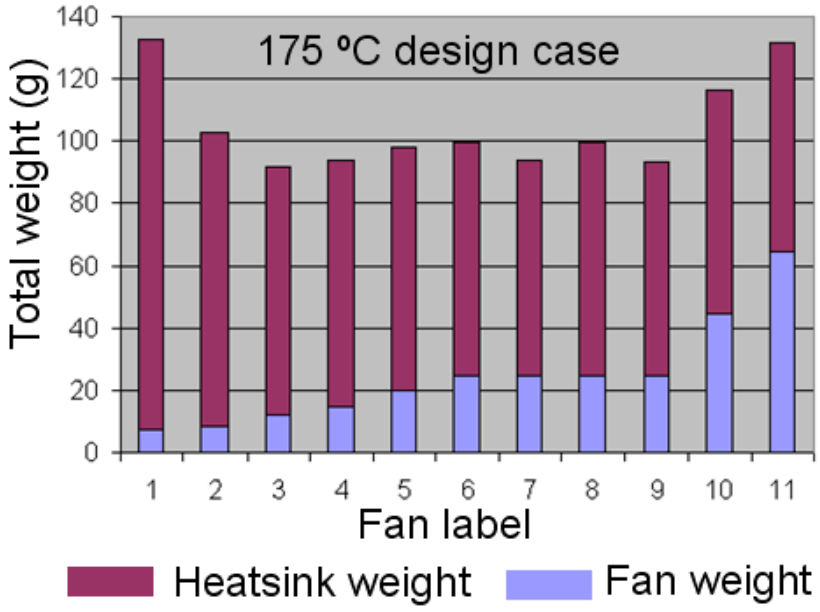


Figure 7-3. Thermal design for wirebond module at 175ºC junction temperature.

In 250 ºC junction temperature case, the power loss of each JFET is 13 W and power loss of each diode is 13.6 W. Figure 7-4 shows the design results of 250 ºC junction temperature. From Figure 7-4, the design case 9 have a minimum weight of 75.4 g.

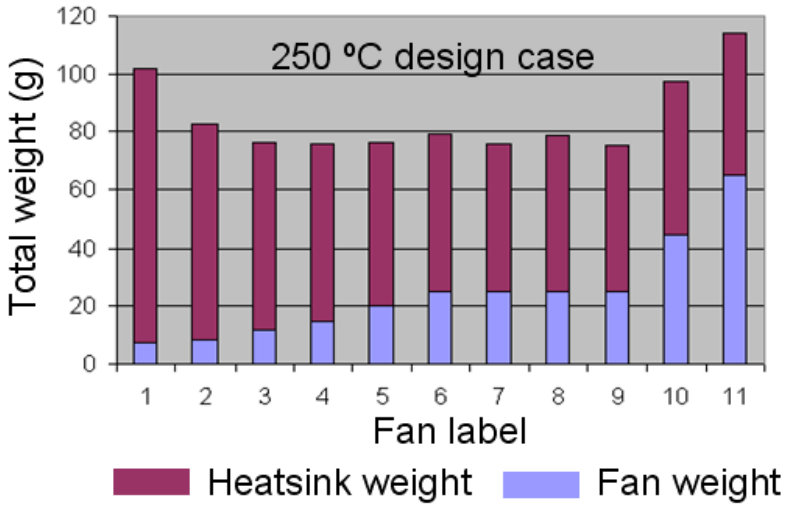


Figure 7-4. Thermal design for wirebond module at 250ºC junction temperature.

In order to analysis the relationship between the power rating and total weight of force-air cooling system, fan label 9 is selected to conduct a comparison. The power rating was increased from 6 kW to 15 kW by assuming the power loss increases linearly. The dimensions of dies and modules did not change when power rating was scaled up. The comparison are also base on optimizing design of 175 ºC junction-temperature case and 250 ºC junction-temperature case for wirebond package. The relationship of weight and total weight of cooling system are plotted in Figure 7-5 and Figure 7-6. It can be leaned that the total weight of cooling system also increases linearly with power rating.

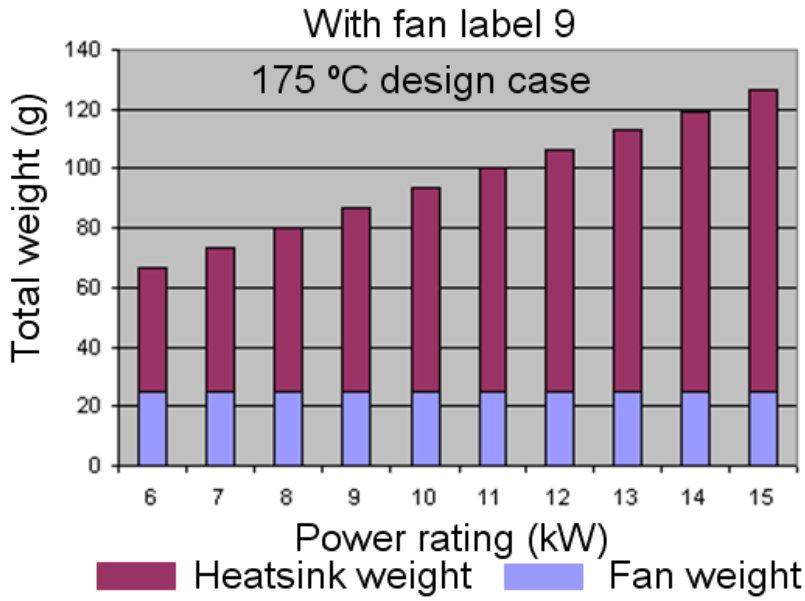


Figure 7-5. Weight vs. power for wirebond module at 175ºC junction temperature.

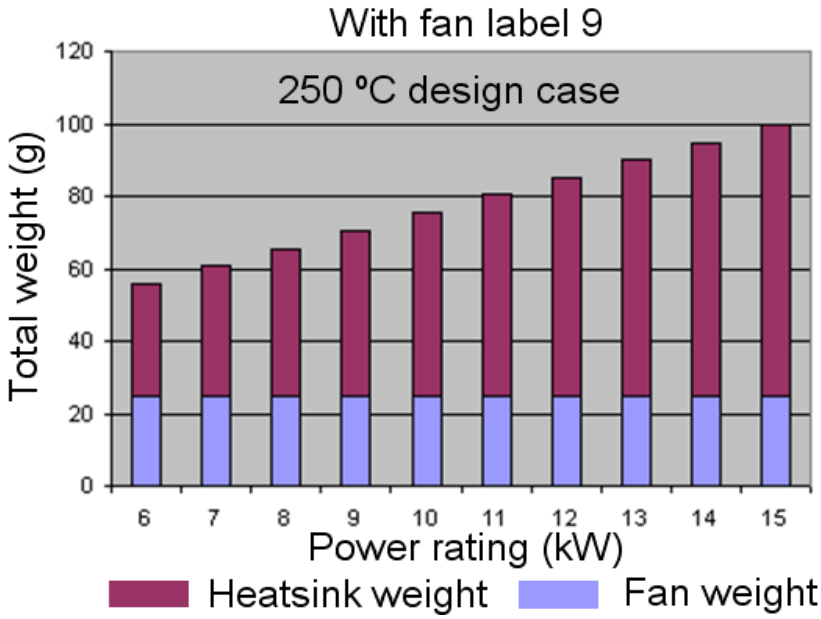


Figure 7-6. Weight vs. power for wirebond module at 250ºC junction temperature.

7.1.2 Design of Planar Power Module

As introduced in Chapter 4, the layout for planar module was designed by considering the reduction of parasitic parameters and the balance of the paralleled devices. With the FEA simulation tools, several candidates are evaluated and compared. The final layout design is shown in Figure 7-7.

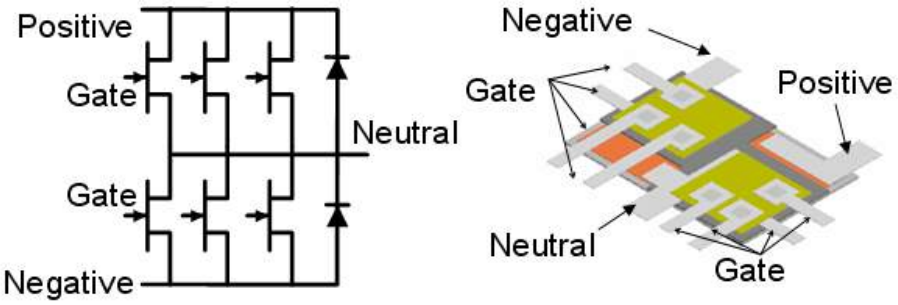


Figure 7-7. layout design of planar module.

The cooling system is also designed by following the process presented in Chapter 5. The conduction loss is calculated based on the static device characterization. The switching loss is calculated based on the double pulse test. The fan is still selected in Table 5-3. The design based on 175 ºC junction temperature and 250 ºC junction temperature to show the advantages of high temperature converter development. By consider the manufacturability, the minimum fin width is 1 mm and the minimum gap width is 2mm. Limited by the footprint of power module and the PCB mechanical supporter, the minimum width of heatsink is 40 mm and the minimum length of heatsink is 40 mm.

In 175 ºC junction temperature case, the power loss of each JFET is 9.6 W and power loss of each diode is 10 W. Figure 7-8 shows the design results of 175 ºC junction temperature. From Figure 7-8, the design case 9 have a minimum weight of 82.1 g.

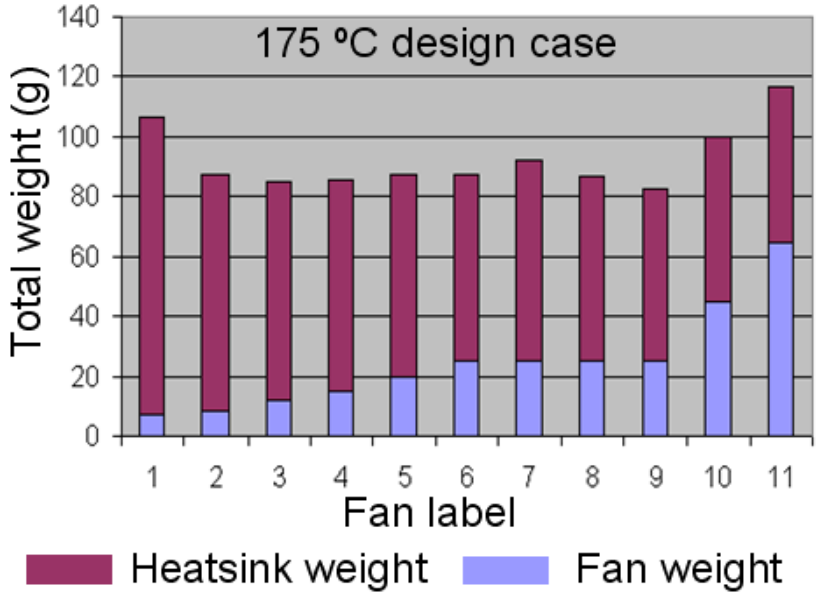


Figure 7-8. Thermal design for planar module with 175 º junction temperature.

In 250 ºC junction temperature case, the power loss of each JFET is 12.5 W and power loss of each diode is 13 W. Figure 7-9 shows the design results of 250 ºC junction temperature. From Figure 7-9, the design case 3 have a minimum weight of 67.2 g.

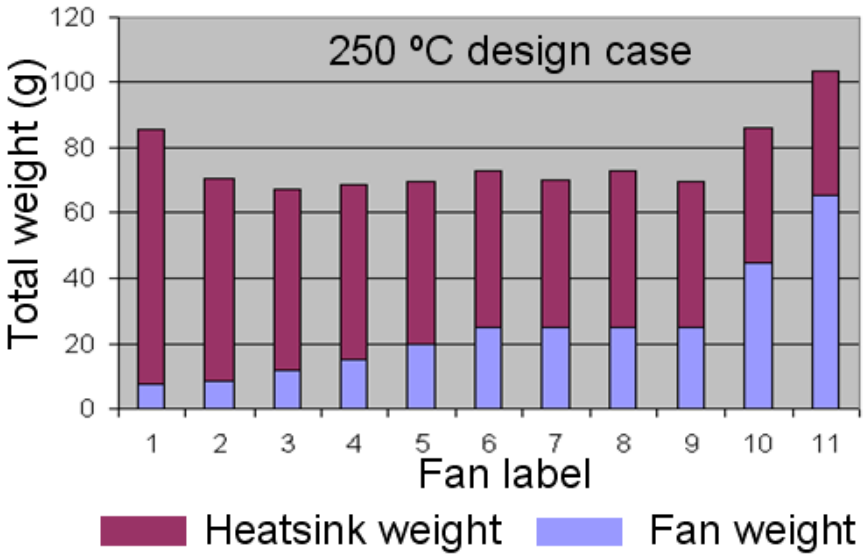


Figure 7-9. Thermal design for planar module with 250 º junction temperature.

In order to analysis the relationship between the power rating and total weight of force-air cooling system, fan label 9 is selected to conduct a comparison. The power rating was increased from 6 kW to 15 kW by assuming the power loss increases linearly. The dimensions of dies and modules did not change when power rating was scaled up. The comparison are also base on optimizing design of 175 ºC junction-temperature case and 250 ºC junction-temperature case for planar package. The relationship of weight and total weight of cooling system are plotted in Figure 7-10 and Figure 7-11. It can be leaned that the total weight of cooling system also increases linearly with power rating.

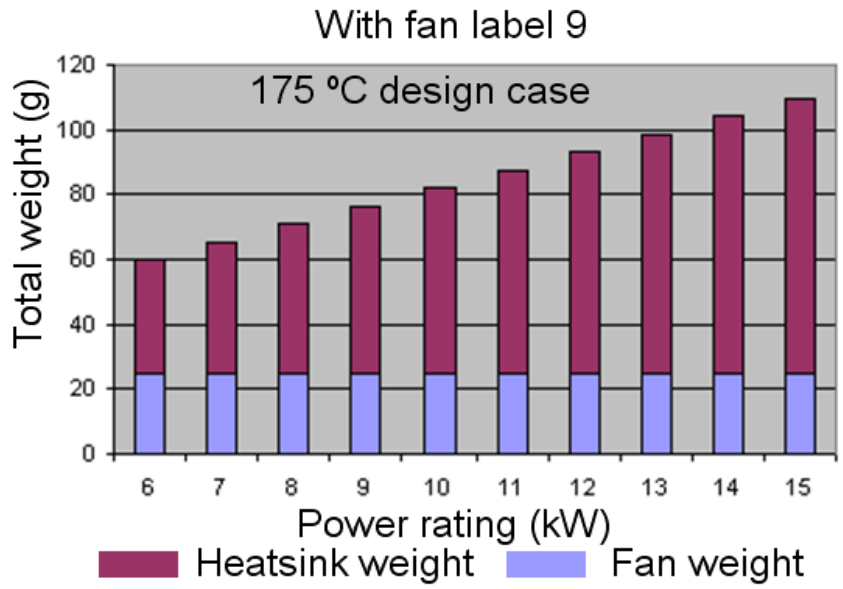


Figure 7-10. Weight vs. power for planar module at 175ºC junction temperature.

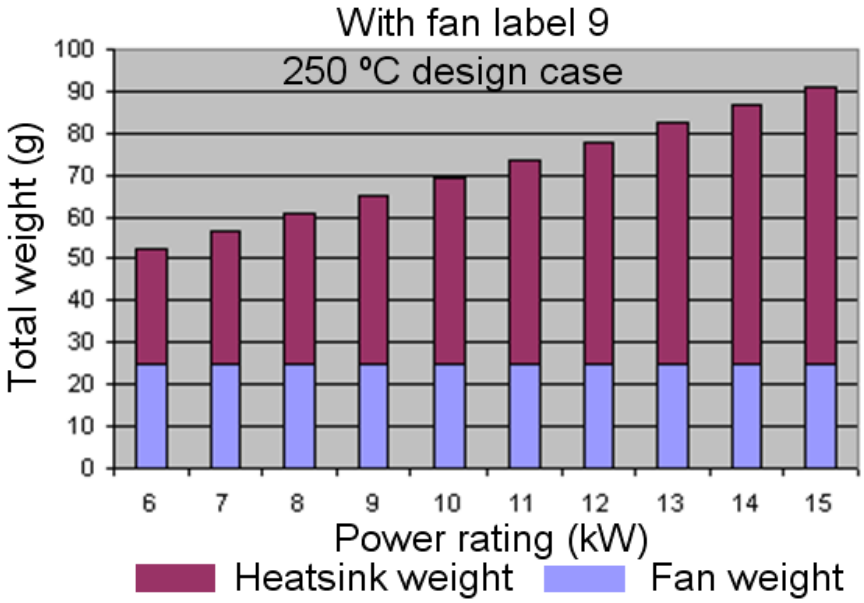


Figure 7-11. Weight vs. power for planar module at 250ºC junction temperature.

The fabricated wirbond module and planar module are put together and compared in Figure 7-12. It can be learned that the footprint of the planar module is only half of the footprint of wirebond module.

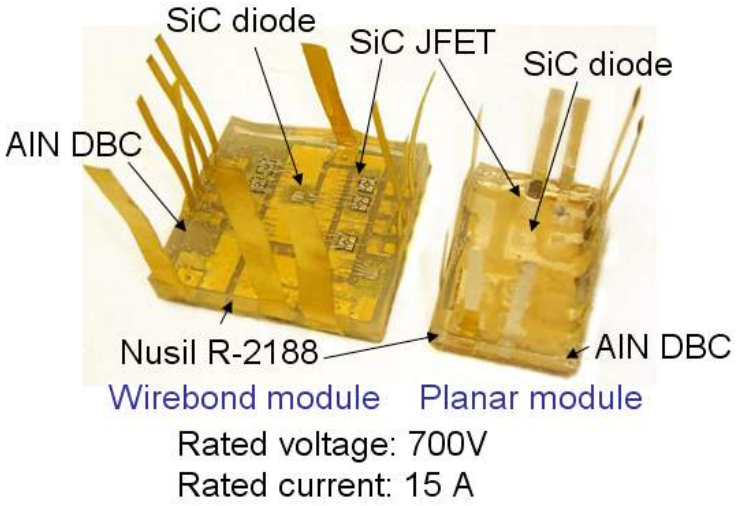


Figure 7-12. Comparison of wirebond module and planar module.

Figure 7-13 shows the comparison between wirebond module and planar module cooling system design for both 175 ºC junction temperature and 250 ºC junction temperature. The planar power module has the benefit in reducing the power loss and total weight.

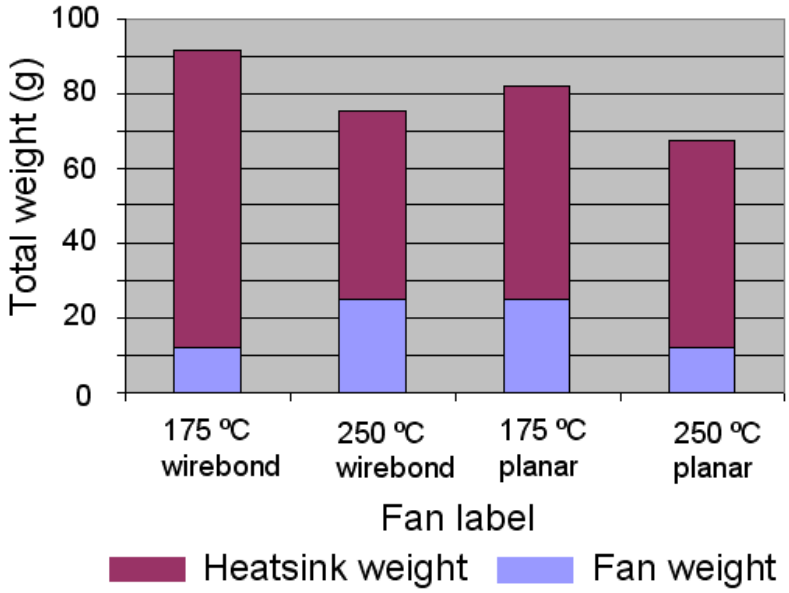


Figure 7-13. Comparison of total weight.

7.2 Power Test of High Temperature Module

7.2.1 Power Test of Wirebond Module

In order to evaluate the high temperature operation ability of designed package, the prototype multi-chip phase-leg power module following the layout design in section 7.1.1 was fabricated and amounted with gate drive PCB board, as shown in Figure 7-14.

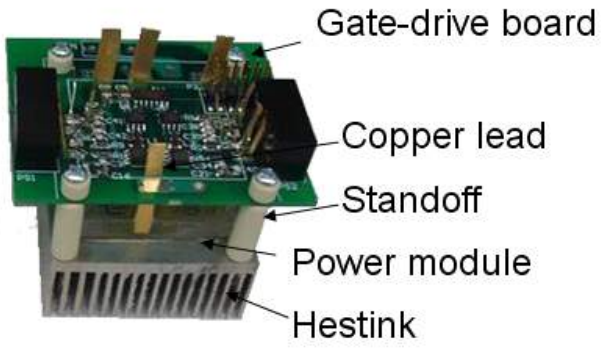


Figure 7-14. Fabricated power module.

As shown in Figure 7-15, with a simple buck converter circuit, the power module can be operated in AC mode and the power loss of devices will heat up the module. Thus, the selected materials and designed package can be evaluated to enable the high temperature operation.

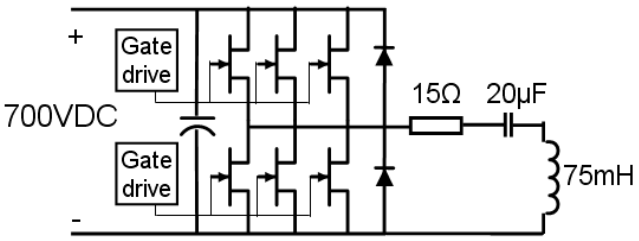


Figure 7-15. Test schematic of wirebond module.

Since the purpose of the continuous power test is to determine the feasibility of the developed packaging for high temperature operation, the heat dissipation system was not specifically designed and optimized. Forced air cooling was applied to the heatsink by a small fan. The ambient temperature was at 25 °C room temperature. In order to sense the temperature, two thermocouples were embedded in the power module, with one close to the top JFETs and the other close to the bottom diode.

The prototype power module was operated with 700 V input voltage, 5A input current and the power rating of 3.5 kW at the estimated junction temperature of 250 °C. The switching waveforms of top JFET gate signal, bottom JFET gate signal, top JFET drain to source voltage and inductor current are shown in Figure 7-16. The continuous power test lasted 20 minutes after the system was running in the steady state. The test results prove

that the designed wirebond package can support the SiC multi-chip power module operating at 250 °C junction temperature.

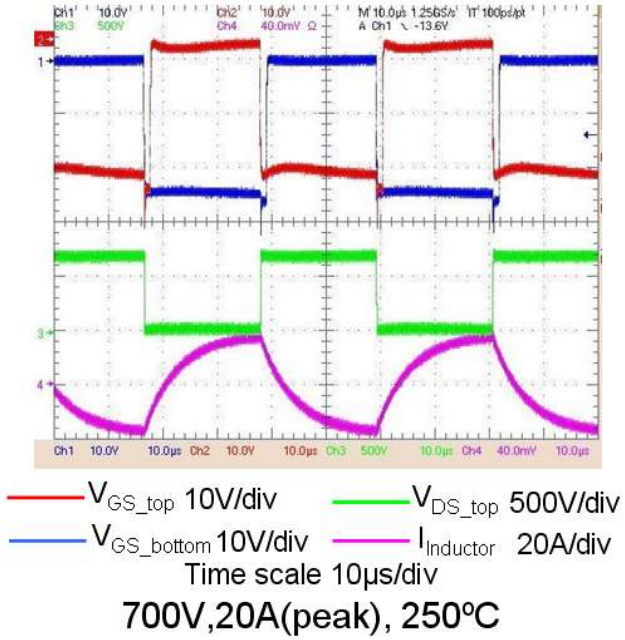


Figure 7-16. Test results of wirebond module.

The temperature rise profile during the test is shown in Table 7-1. It took about 50 minutes for the power test system to reach the steady state. With the similar assumption in [22], 25 °C temperature difference from junction to the bottom pad of die is adopted in this paper. In the test, the estimated junction temperature of JFET is about 20 °C higher than that of the diode.

Table 7-1 Measured Temperature Distribution of Wirebond Module

Time	JFET	Diode	Heatsink
0:00 minute	25 ºC	25 ºC	25 ºC
50:00 minute	223 ºC	199 ºC	180 ºC
70:00 minute	223 ºC	199 ºC	180 ºC

In order to further understand the temperature distribution of the power module and ensure the accuracy of the thermocouples, finite-element thermal simulation was carried out by the I-DEAS. The settings of I-DEAS are listed in Table 7-2. The thermal simulation result is shown in Figure 7-17.

Table 7-2 Settings in the FEA Simulation (I-DEAS)

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	453200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

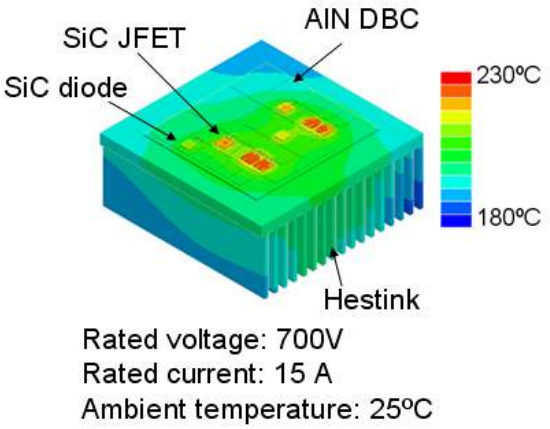


Figure 7-17. Simulated temperature distribution of wirebond module.

The simulation result agrees well with the measurements in the experiment. Since the deviations are acceptable, the thermal simulation can give a design guideline for finding the better layout with confidence in the future. Additionally, the temperature measured by the thermocouple is credible.

With a simple buck converter circuit, finally the full-chip module can be operated in AC mode and the power loss of devices will heat up the module. Thus, the selected materials and designed package enable the high temperature operation.

7.2.2 Power Test of Planar Module

Figure 7-18 illustrates the connection setup for the planar module power test. The gate drive components and the power connections were combined on the PCB, which is 19 mm higher than the power module bottom surface to provide a low-temperature operation environment for gate drive components. Ceramic stand-offs were utilized to support the PCB and reduce the thermal conduction.

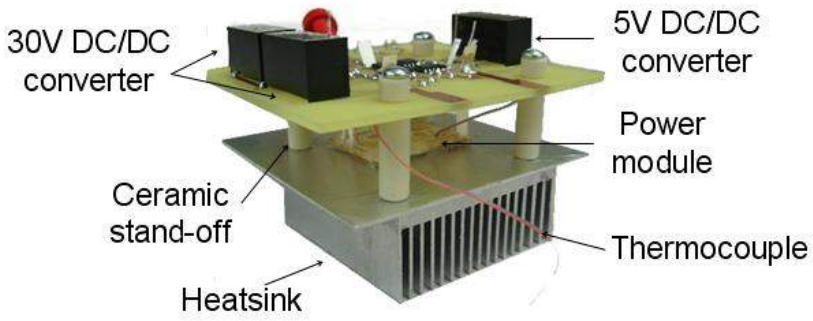


Figure 7-18. Test setup of planar module.

Since the objective of the power test is to demonstrate the functionality of the module at a high junction temperature, the dummy devices larger heatsink were used. The rated DC voltage is designed as 400 V and the output peak current value is 10 A.

As shown in Figure 7-19, with a simple buck converter circuit, the power module can be operated in AC mode and thus the current will go through the JFETs and diodes alternately in one switching period.

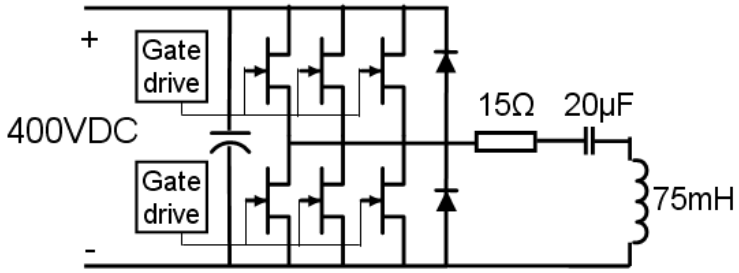


Figure 7-19. Test schematic of planar module.

By using the connection setup shown above, the multi-chip phase-leg power module was operated as a buck converter with 400 V input voltage and 3.5 A input current, with a power rating of 1.4 kW at the estimated junction temperature of 250 °C. This continuous power test lasted 20 minutes as the system run in steady state. The switching waveforms of top-leg JFET gate signal, bottom JFET gate signal, top JFET drain-to-source voltage and inductor current are shown in Figure 7-20. The test results prove that the designed planar package can support the SiC multi-chip power module operating at 250 °C junction temperature.

In the power test, the heat dissipating system was not specially designed and optimized. Only natural air cooling was applied to the heatsink. The ambient temperature was room temperature, which was 25 °C.

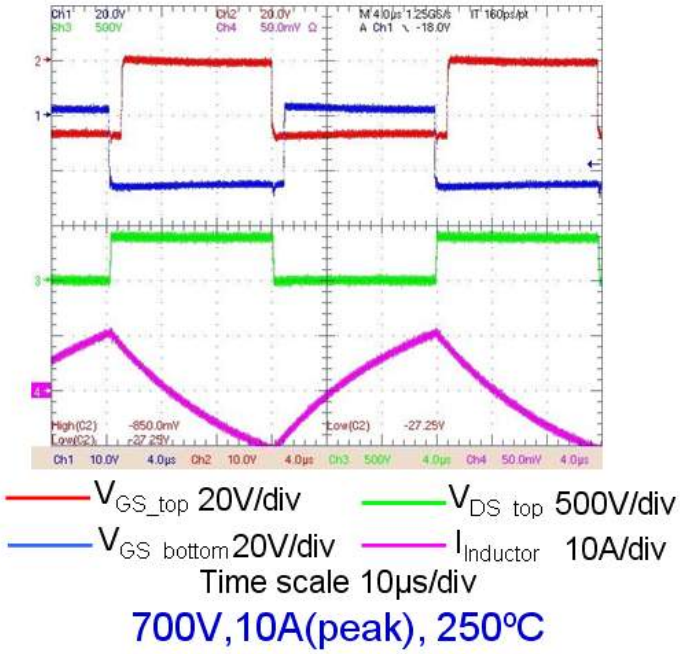


Figure 7-20. Test result of planar module.

In order to sense the temperature, there were two thermocouples embedded in the power module. One is close to the top-leg JFETs, and the other one is close to the bottom-leg diode. The temperature profile during the test is shown in Table IV. It took about 60 minutes for the power test system to reach the steady state. With the similar assumption in [22], 25 °C temperature difference from junction to the bottom pad of die is adopted in this paper.

In order to further understand the temperature distribution of the multi-chip phase-leg module and ensure the accuracy of the thermocouples, finite-element thermal simulation is carried out by I-DEAS. The settings of I-DEAS are listed in Table 7-3. The thermal simulation result is shown in Figure 7-21.

Table 7-3 Settings in the FEA Simulation (I-DEAS)

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	453200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

The simulation result agrees well with the measurements in the experiment. Since the deviations are acceptable, the thermal simulation can give a design guideline for finding a better layout with confidence in the future. Additionally, the temperature measured by the thermocouple is credible.

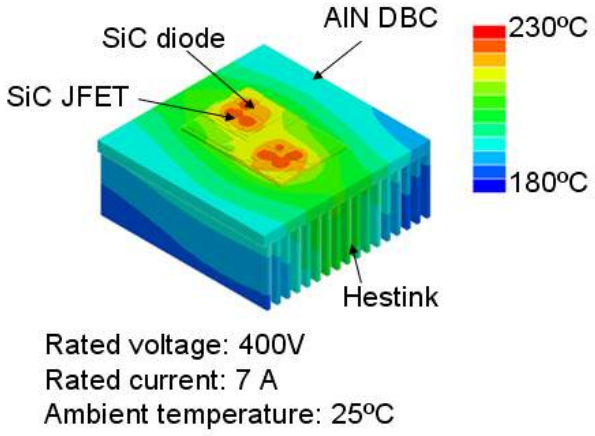


Figure 7-21. Simulated temperature distribution of planar module.

7.3 Summary

Wirebond module and planar module are designed for 175 ºC junction temperature and 250 ºC junction temperatures. The design process and tests prove that the planar

package module has smaller footprint and higher power density than wirebond package module. All the key concepts and ideas developed in previous chapters are implemented in the prototype module development and then verified by the experimental results.

Chapter 8 Summary and Future Work

8.1 Summary

This dissertation presents a systematic methodology for the high power density high temperature power module with the cooling system. Five key aspects of the power module and cooling system, including material selection and thermo-mechanical evaluation, power module layout design, thermal management design, electrical evaluation and novel planar high temperaure packaging are carefully studied.

In Chapter 2, the design, development and testing of high temperature packaging for a multi-chip phase-leg power module using SiC JFETs and diodes has been presented. Based on the wirebond packaging, materials for each part of the module are compared and selected to ensure the full package can function reliably at 250 ºC. The thermo-mechanical reliability of substrate was evaluated and several methods were investigated to improve the lifetime. It is found through experiments that by sealing the stepped edge DBC, considerable improvement on substrate reliability under large temperature excursion can be achieved. The promising results of thermal cycling test on die-attachment and wirebond assemblies prove that the proposed package can perform well for large temperature excursion.

In Chapter 3, a high-temperature (250 ºC) planar package for the power module using SiC devices is presented. Sintered silver and high-temperature polyimide are selected as

the interconnection materials, which allow individual interconnection on each pad. This approach takes the advantages of the flexibility and the high-temperature capability of the sintered silver and the polyimide material, and can be implemented in other packaging applications. Electrical and thermo-mechanical tests of the prototype module demonstrate the functionality and reliability of the planar packaging methodology.

Chapter 4 presents the layout design of high power density power module. Some practical considerations are introduced for the optimization of electrical performance of the module. Together with the design example, the manual design and automatic design process are presented separately. The automatic design procedure could be a major step to improve the overall performance for future layout design.

In Chapter 5, a systematic optimal design process and parametric study of the heatsink-fan cooling system by applying the analytical model is described in this chapter. The presented thermal design method is confirmed by numerical simulation and experiments. The optimization procedure is accurate enough to pursue a minimum weight of heatsink-fan cooling system with a given thermal resistance.

In Chapter 6, a safe and rapid electrical evaluation procedure is presented. The successful continuous power testing on prototype module demonstrates that electrical evaluation procedure reduce the risk of failure and the designed package in chapter 2 can support the SiC semiconductor devices operating at 250 ºC junction temperature.

In Chapter 7, wirebond module and planar module are designed for 175 ºC junction temperature and 250 ºC junction temperatures. All the key concepts and ideas developed

in previous chapters are implemented in the prototype module development and then verified by the experimental results.

8.2 Future Work

In order to further improve high power density high temperature power module with the cooling system, future work can be carried out in the following directions.

In the wirebond high temperaure packaging design, more detailed thermo-mechanical simulation should be conducted to better understand the cause of substrate failure. Based on the simulation, more reliable wirebond high temperature power module can be developed.

In the planar high temperaure packaging design, automatic top side bonding by dispenser machine and other assistant equipment need to be investigated. The current capability of top side bonding also needs further improvement.

In the power module layout design, the fitness evaluation methods should be further investigated to better define an optimized layout design, especially for the multi-chip power module.

In the thermal management design, the air-flow characteristic in the space between fan and heatsink should be further investigated. Correspondingly, the thermal model should be modified and verified by the FEA-CFD simulation and experimental results.

In the electrical evaluation part, the test procedure from high temperature power module to high temperature converter system needs further investigation.

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Appendix Parametric Study of Substrate

Mechanical failure of an electrical device can be the result of one or any combination of responses of the device to loads and environment. Thermal stresses in the different layers of power module packages result from mismatches in the thermal properties and stiffness of the bonded materials. The bonding interfaces suffer high stress concentrations, which eventually lead to cracking and delamination. In accordance with the features of materials used in high-temperature power modules, this section investigates the peeling stress as indicators of different failure modes. This section uses finite element analysis (FEA) to understand the package failure trend. It is important to know the effect of stress and to have a reasonably accurate estimate of the stress level in these structures when designing layered electronic assemblies.

The thermo-mechanical failure theories for power electronics modules, along with the mechanics of materials, have been developing over the last two centuries. In literature, the peeling stress is dependent on the magnitude and sign of the temperature difference, as well as the mechanical and geometrical parameters. This section hypothesizes that normal interfacial stress plays a significant role in delamination, and experiments carried out to test this hypothesis verify that there is a close relationship between delamination and peeling stress [39]. Further experiments verify that the peak tensile peeling stress, whose direction is peeling away from the layer surface, is the major driving force of delamination [40]. A smaller peeling stress will result in a longer lifetime of the substrate [41]. In this section, the relationship between peeling stress and the lifetime of the substrate is investigated by FEA simulations and tests.

Figure A- 1 to Figure A- 3 show cross-section schematics for the original DBC substrate, a stepped edge DBC substrate, and a sealed stepped edge DBC substrate, respectively. Predicting the lifetime of substrate is a challenge due to the complex nonlinear behavior of different layers and the importance of the load history. The properties used in the FEA simulation are listed in Table A- 1. Since the thermo-mechanical properties and model of DBC substrate and Epo-tek 600 are not accurate enough, FEA simulations in this dissertation can only be used to understand the trend of lifetime increasing.

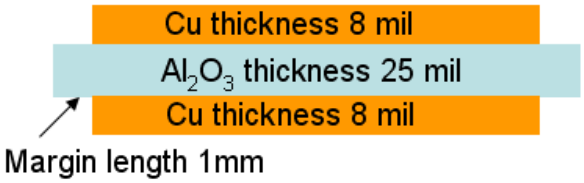


Figure A- 1. Original DBC substrate.

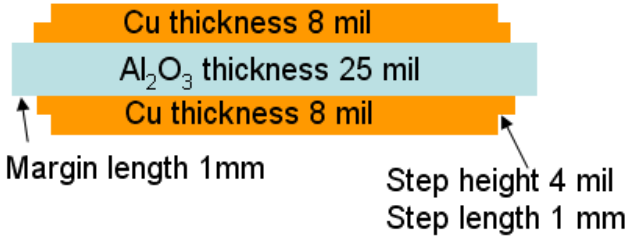


Figure A- 2. Stepped-edge DBC substrate.

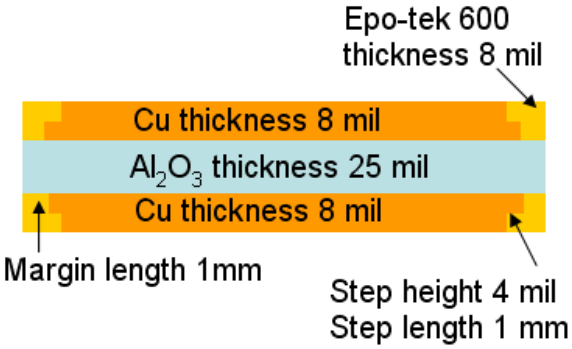


Figure A- 3. Sealed-stepped-edge DBC substrate.

The Al_2O_3 DBC substrates used in the test were purchased from Curamik. The substrates were processed at the CPES packaging laboratory with a laser cutting machine and etching bath. After the etching, a 10 μm nickel layer and a 10 μm silver layer is were electroplated on the copper layer to prevent oxidation during cycling. For the sealed stepped edge DBC substrate, Epo-tak 600 was manually dispensed on the edge.

Table A- 1 Thermo-Mechanical Properties of DBC Substrate in Simulations

	Young's modulus	CTE	Poison's ratio
Copper	110 GPa	16.4×10^{-6}	0.343
Alumina (Al_2O_3)	380 GPa	7.1×10^{-6}	0.27
Epo-Tek 600	187 GPa	11.2×10^{-6}	0.36

In the simulations and tests for parametric study, the temperature of the cycling ranges from -55 °C to -250 °C, which is the same as the temperature range used in the thermo-mechanical test in the previous section. In all the simulations listed below, the residual stress is assumed to be zero at 25 °C.

First, simulations are conducted to understand the lifetime increase of the stepped edge DBC substrate and the sealed stepped edge DBC substrate. The results of the FEA simulation tool ANSYS are shown in Figure A- 5. In the simulation, the maximum element size is 3×10^{-10} m^3. The X-axis is the midline of the substrate with the original zero point in the substrate center. The Y-axis is the peeling stress.

Table A- 2 Dimensions of DBC Substrates

	DBC substrate	Dimensions
Case 1	Original	20 mm × 30 mm
Case 2	Stepped edge	20 mm × 30 mm Step length 1mm Margin length 1mm
Case 3	Sealed stepped edge	20 mm × 30 mm Step length 1mm

		Step height 4 mil Margin length 1mm Polyimide thickness 1mm

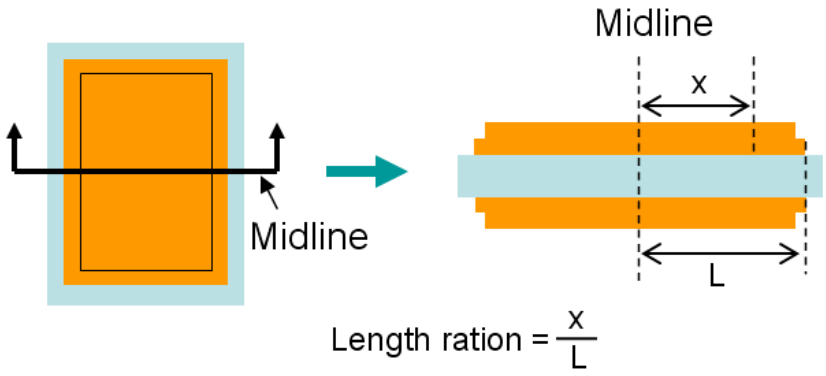


Figure A- 4. Definition of length ratio.

Table A- 3 Settings of FEA Simulation for DBC Substrate in Table 8-2

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	273200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

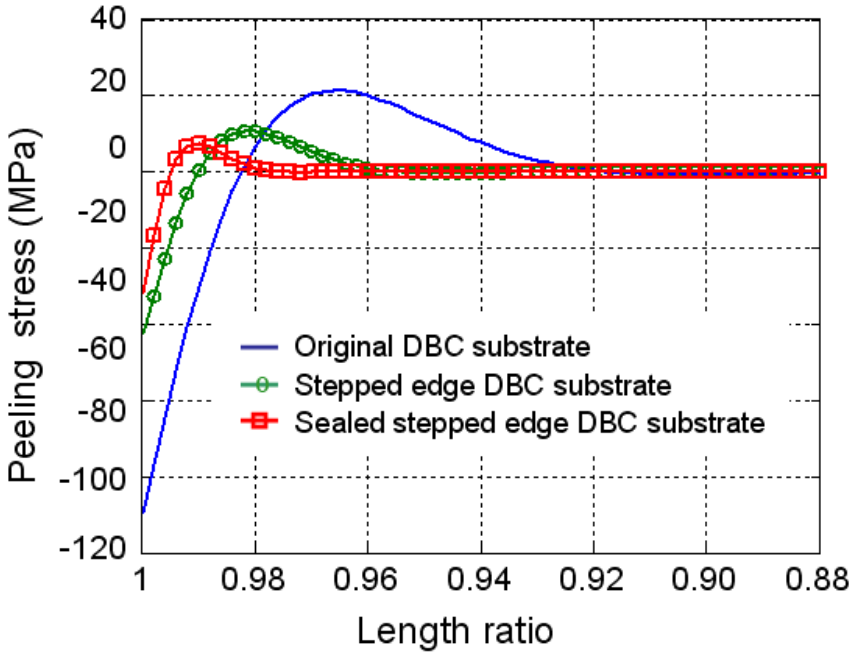


Figure A- 5. Simulation results of DBC substrates.

From the simulation results, it can be noticed that with stepped edge method the peeling stress can be reduced a lot and then with sealed stepped edge method, the peeling stress can be reduced more. Although simulations can't directly predict the lifetime of the substrates, the trend for stress reduction and lifetime increasing can be learned.

In order to better understand the effects of the thickness ratio, length ratio and copper layer thickness on the lifetime of DBC substrate, FEA simulation and tests were conducted to show the trend. Since the lifetime of original DBC substrate is too short (20 – 30 cycles, about 1 day) to compare different samples while the lifetime of sealed stepped edge DBC sbustrate is long (800 – 1300 cycles, up to 4 month). Stepped edge DBC substrates were utilized in the study.

In the first group, the length of substrate is utilized as a variable. Square substrates were used as samples. As shown in Table A- 5, the dimensions change; the dimensions used are 40 × 40 mm^2, 30 × 30 mm^2, 20 × 20 mm^2 , and to 10 × 10 mm^2. All other

parameters stay the same. The margin length (the distance between the root edge of the copper to the edge of the Al_2O_3) is kept at 1 mm. The step length is 1 mm, and the step height is 4 mils. The dimensions of group J sample are listed in Table A- 4 and Table A- 5. In Table A- 6, the test results show that the lifetime of the substrate decreases when the length of the sample decreases.

Table A- 4 Fixed Dimensions of Group J Sample

Al_2O_3 thickness	Copper thickness	Margin length	Step length	Step height
25 mil	8 mil	1 mm	1 mm	4 mil

Table A- 5 Group J Sample

Sample	Case 1	Case 2	Case 3	Case 4
Variable Dimension (mm^2)	40 × 40	30 × 30	20 × 20	10 × 10
				

Table A- 6 Test Results of Group J Sample

	Sample variables width and length	Samples	Lifetime
Group J samples	40 mm ×40 mm	Sample J1	250 cycles
		Sample J2	250 cycles
		Sample J3	250 cycles
	30 mm ×30 mm	Sample J4	220 cycles
		Sample J5	220 cycles
		Sample J6	220 cycles
	20 mm ×10 mm	Sample J7	190 cycles
		Sample J8	190 cycles
		Sample J9	190 cycles
	10 mm ×10 mm	Sample J10	170 cycles
		Sample J11	170 cycles
		Sample J12	170 cycles

The simulation results by ANSYS are shown in Figure A- 6. The setting s of ANSYS is listed in Table A- 7. The X-axis is the midline of the substrate with the original zero point in the substrate center. The Y-axis is the peeling stress. The simulation results show that the peeling stress decreases when sample length increases, which agrees well with the test results.

Table A- 7 Settings of FEA Simulation for Group J Samples

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	273200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

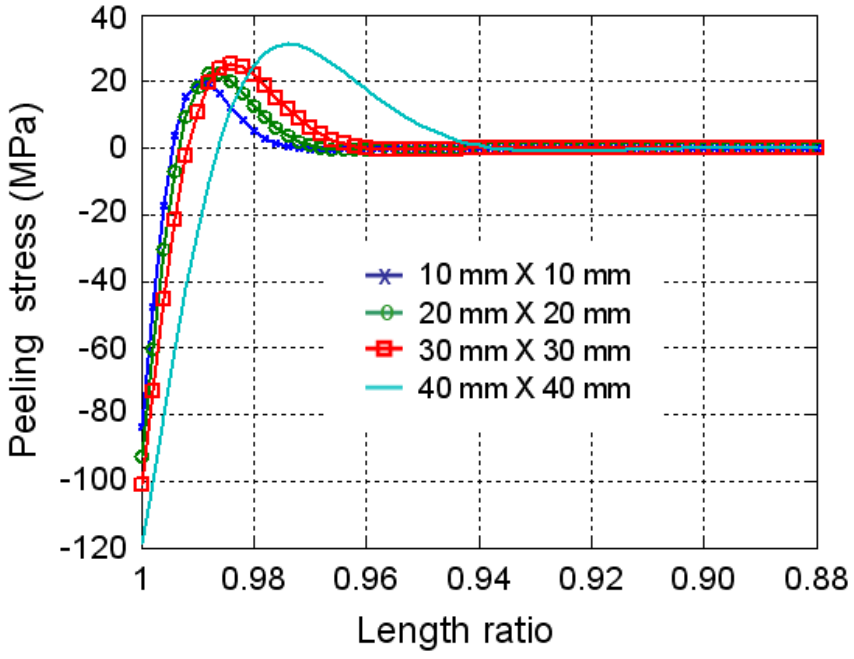


Figure A- 6. Simulation results of group J sample.

In the second group, the step length is utilized as a variable. As shown in Table A- 8 and Table A- 9, the distances change from 0.5 mm, to 1mm, to 2mm. All other parameters stay the same. The length of the substrate is 30 mm and the width of the substrate is 20 mm. The margin length is kept at 1 mm, and the step height is 4 mils. In Table A- 10, the cycling test results show that the lifetime of the substrate decreases when the step length decreases.

Table A- 8 Fixed Dimensions of Group K Sample

Al_2O_3 thickness	Copper thickness	Dimension	Margin length	Step height
25 mil	8 mil	20 mm × 30 mm	1 mm	4 mil

Table A- 9 Group K Sample

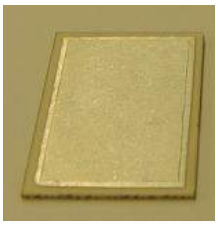
Sample	Case 1	Case 2	Case 3
Variable: Step length (mm)	0.5	1	2
			

Table A- 10 Thermal-Cycling Results of Group K Samples

	Sample variables width and length	Samples	Lifetime
Group K samples	40 mm ×40 mm	Sample K1	130 cycles
		Sample K2	130 cycles
		Sample K3	130 cycles
	30 mm ×30 mm	Sample K4	180 cycles
		Sample K5	180 cycles
		Sample K6	180 cycles
	20 mm ×10 mm	Sample K7	220 cycles
		Sample K8	220 cycles
		Sample K9	220 cycles

The simulation results by ANSYS are shown in Figure A- 7. The setting s of ANSYS is listed in Table A- 11. The X-axis is the midline of the substrate with the original zero point in the substrate center. The Y-axis is the peeling stress. The simulation results show that the peeling stress decreases when the step length increases, which agrees well with the test results.

Table A- 11 Settings of FEA Simulation for Group K Samples

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	269400	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

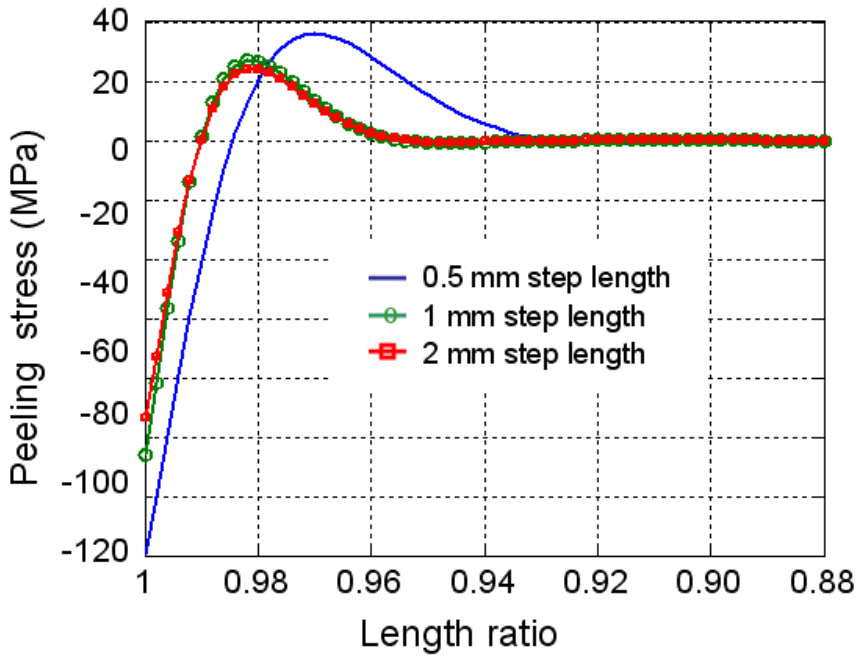


Figure A- 7. Simulation results of group K samples.

In the third group, the margin length is used as variable. As shown in Table A- 12 and Table A- 13, the margin length changes from 1 mm to 5 mm to 10 mm. All other parameters stay the same. The copper is 18 mm × 18 mm square. The step length is 1 mm, and the step height is 4 mils. In Table A- 14, the test results show that the lifetime of the substrate decreases when the margin length decreases.

Table A- 12 Fixed Dimensions of Group L Sample

Al_2O_3 thickness	Copper thickness	Dimension	Step length 1 mm	Step height
25 mil	8 mil	20 mm × 20 mm	1 mm	4 mil

Table A- 13 Group L Samples

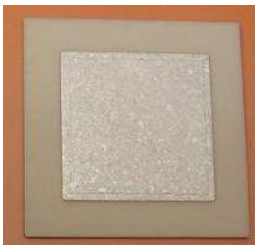
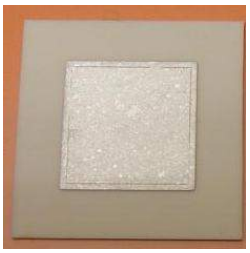
Sample	Case 1	Case 2	Case 3
Variables: Margin length (mm)	1	5	10
			

Table A- 14 Thermal-Cycling Results of Group L Samples

	Sample variables width and length	Samples	Lifetime
Group L samples	40 mm ×40 mm	Sample L1	130 cycles
		Sample L2	130 cycles
		Sample L3	130 cycles
	30 mm ×30 mm	Sample L4	180 cycles
		Sample L5	180 cycles
		Sample L6	180 cycles
	20 mm ×10 mm	Sample L7	220 cycles
		Sample L8	220 cycles
		Sample L9	220 cycles

The simulation results by ANSYS are shown in Figure A- 8. The setting s of ANSYS is listed in Table A- 15.The X-axis is the midline of the substrate with the original zero

point in the substrate center. The simulation results show that the peeling stress decreases when the margin length increases, which agrees well with the test results.

Table A- 15 Settings of FEA Simulation for Group L Samples

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	253200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

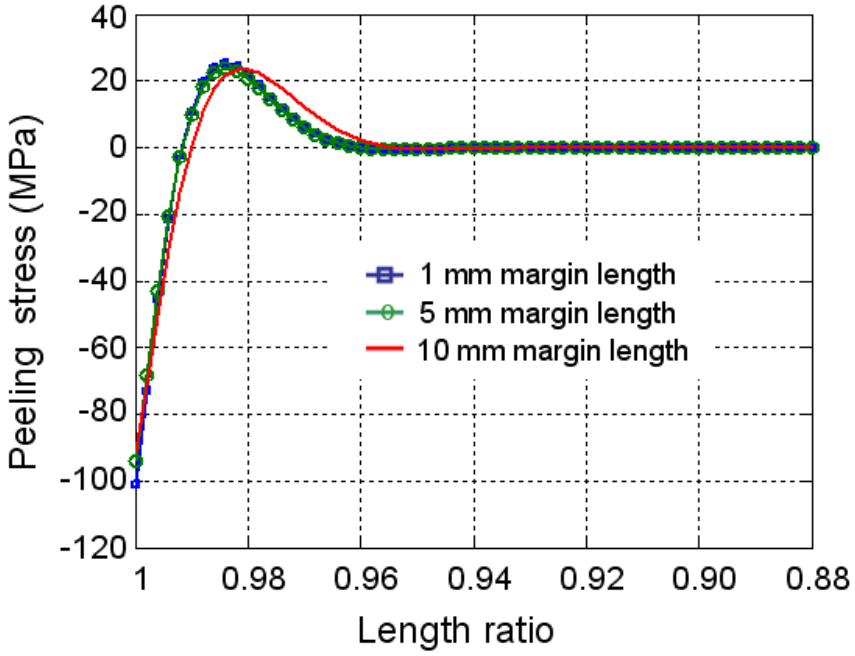


Figure A- 8. Simulation results of group L samples.

In the fourth group, the thickness of the copper is utilized as a variable. As shown in Table A- 16 and Table A- 17, the thicknesses of copper change from 6 mils to 8 mils while all other parameters stay the same. The length of the substrate is 30 mm while the width of the substrate is 20 mm. The margin length is kept at 1 mm. The step length is 1

mm, while the step height is 4 mils for the samples with 8 mils thick copper, and 3 mils for the samples with 6 mils thick copper. In Table A- 18, the cycling results show that the lifetime of the substrate decreases when the copper thickness increases.

Table A- 16 Fixed Dimensions of Group M Sample

Al_2O_3 thickness	Dimension	Margin length	Step length	Step height
25 mil	20 mm × 20 mm	1 mm	1mm	4 mil

Table A- 17 Group M Samples

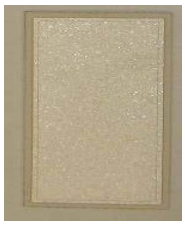
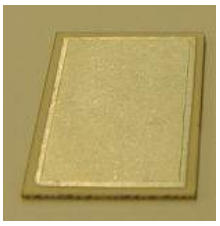
Sample	Case 1	Case 2
Variables: copper thickness (mil)	8	6
		

Table A- 18 Thermal-Cycling Results of Group M Samples

	Sample variables: width and length	Samples	Lifetime
Group M samples	40 mm ×40 mm	Sample M1	130 cycles
		Sample M2	130 cycles
		Sample M3	130 cycles
	30 mm ×30 mm	Sample M4	180 cycles
		Sample M5	180 cycles
		Sample M6	180 cycles

The simulation results by ANSYS are shown in Figure A- 9. The setting s of ANSYS is listed in Table A- 19. The X axis is the midline of the substrate with original zero point in the substrate center. The Y axis is the peeling stress. The simulation results show that the peeling stress reduces when copper thickness reduces, which agrees well with the test results.

Table A- 19 Setting of FEA Simulation for Group M Samples

Element type	Maximum	Minimum	Total element	Maximum

	element length	element length	number	iterations
tetrahedron linear element	1 mm	0.05 mm	286100	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

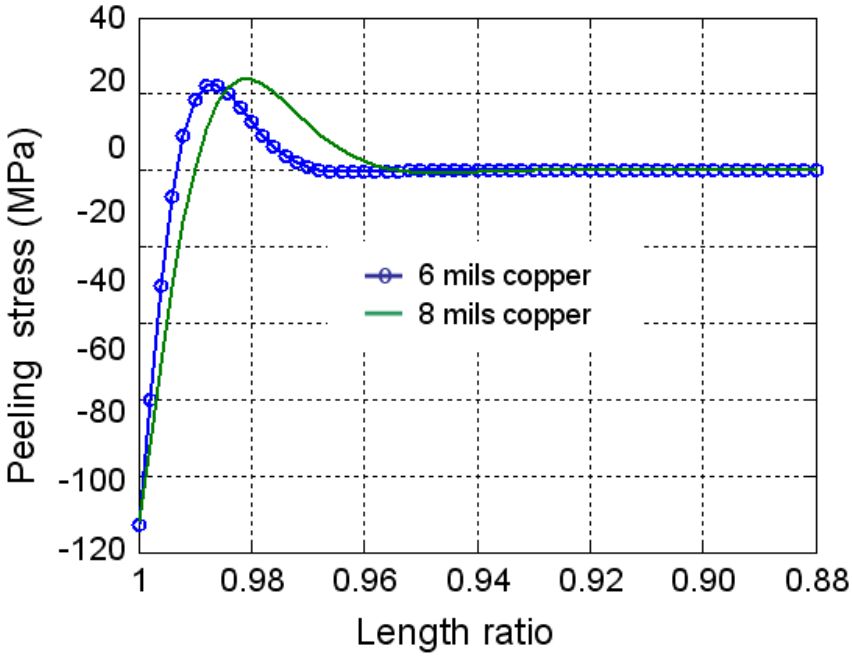


Figure A- 9. Simulation results of group M samples.

In order to better understand the effect of step dimensions, the step height and step length were swept in the simulation, and the simulation results were drawn as a surface. As shown in Table A- 20, the step height and the margin length are used as variable. This investigation is named as group N study. The settings of FEA simulation is listed in Table A- 21. The step height changes from 1mil mm to 8 mil swept by the step of 1 mil. The step length changes from 1 mm to 2 mm swept by the step of 0.1 mm. The substrate is 30 mm × 30 mm square. All other parameters stay the same. The margin length is 1 mm.

Table A- 20 Dimensions for Group N Study

Al_2O_3 thickness	Copper thickness	Dimension	Margin length	Step length	Step height
25 mil	8 mil	30 mm × 30 mm	1 mm	1 mm to 2mm	1 mil to 8 mil

Table A- 21 Settings of FEA Simulation for Group N Study

Element type	Maximum element length	Minimum element length	Total element number	Maximum iterations
tetrahedron linear element	1 mm	0.05 mm	273200	20
Equation solver	Analysis type	Convergence limit	Properties of materials	
Jacobi Conjugate Gradient iterative equation solver	Static simulation	< 5 % changing compared with previous iteration	Listed in Table 3-6	

The maximum peeling stress was listed in Table A- 22 and plotted in Figure A- 10. There are two trends that can be learned from the simulation results. The first trend is that a larger step length will result in less stress, which agrees well with the previous simulations and tests. The second trend is that when the step height is close to half of the copper thickness, the peeling stress is minimized.

Table A- 22 Simulation Results List of Group N Study

Maximum stress (MPa)		Step length (mm)									
		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Step length (mm)	0.1	51.015	50.03	48.87	47.71	46.9	46.09	45.455	44.82	44.91	45
	0.2	49.93	47.86	45.44	43.02	41.3	39.58	38.21	36.84	36.92	37
	0.3	49.465	46.93	43.97	41.01	38.9	36.79	35.105	33.42	32.71	32
	0.4	49	46	42.5	39	36.5	34	32	30	28.5	27
	0.5	50.05	48.1	45.825	43.55	41.925	40.3	39	37.7	35.1	32.5
	0.6	51.1	50.2	49.15	48.1	47.35	46.6	46	45.4	41.7	38
	0.7	51.55	51.1	50.575	50.05	49.675	49.3	49	48.7	46.85	45
	0.8	52	52	52	52	52	52	52	52	52	52

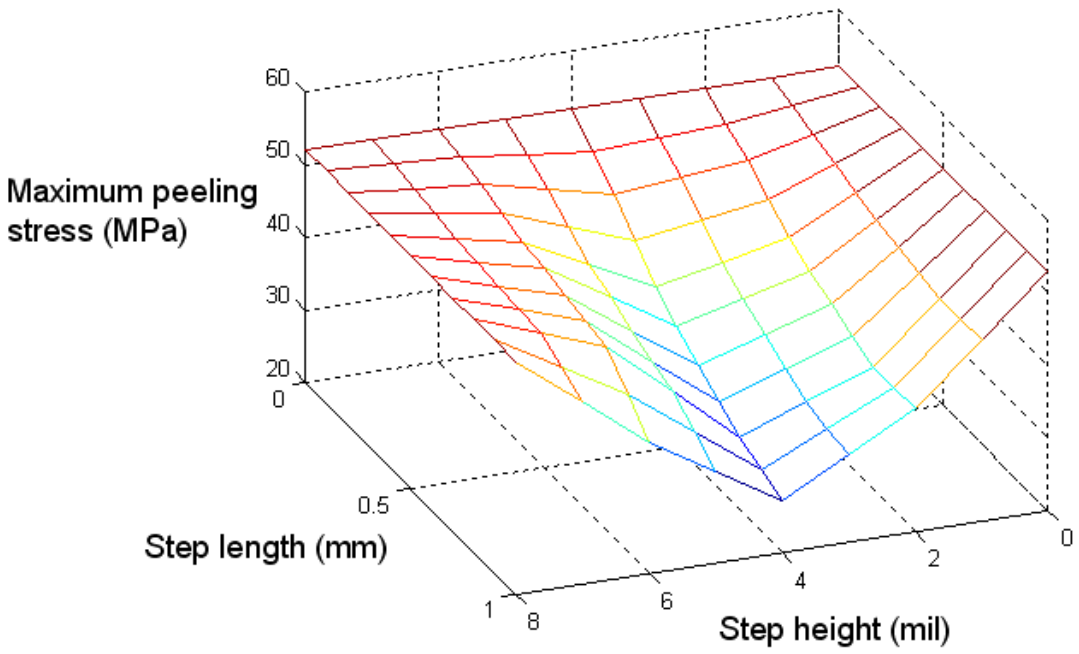


Figure A- 10. Simulation results plot of group N study.

There is good agreement between the calculation results and the simulation results listed above. Although the FEA software is limited to trend prediction, it is still an effective tool to study stress distribution, and can verify the experimental results. The peeling stress analysis by FEA simulation tools could be a major step in improving the overall performance of high-temperature power modules.