Modeling of Power Electronics Distribution Systems with Low-frequency, Large-signal (LFLS) Models

Sara Ahmed

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Dushan Boroyevich
Douglas K. Lindner
Fei Wang
Paolo Mattavelli
Saad A. Ragab

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ABSTRACT

This work presents a modeling methodology that uses new types of models called low-frequency, large-signal models in a circuit simulator (Saber) to model a complex hybrid ac/dc power electronics system. The new achievement in this work is being able to model the different components as circuit-based models and to capture some of the large-signal phenomena, for example, real transient behavior of the system such as startup, inrush current and power flow directionality. In addition, models are capable of predicting most low frequency harmonics only seen in real switching detailed models. Therefore the new models system can be used to predict steady state performance, harmonics, stability and transients. This work discusses the modeling issues faced based on the author recent experiences both on component level and system level. In addition, it recommends proper solutions to these issues verified with simulations.

This work also presents one of the new models in detail, a voltage source inverter (VSI), and explains how the model can be modified to capture low frequency harmonics that are usually phenomena modeled only with switching models. The process of implementing these different phenomena is discussed and the model is then validated by comparing the results of the proposed low frequency large signal (LFLS) model to a complete detailed switching model. In addition, experimental results are also obtained

with a 2 kW voltage source inverter prototype to validate the proposed improved average model (LFLS model).

In addition, a complete Verification, Validation, and Uncertainty Quantification (VV&UQ) procedures is applied to a two-level boost rectifier. The goal of this validation process is the improvement of the modeling procedure for power electronics systems, and the full assessment of the boost rectifier model predictive capabilities.

Finally, the performance of the new models system is compared with the detailed switching models system. The LFLS models result in huge cut in simulation time (about 10 times difference) and also the ability to use large time step with the LFLS system and still capture all the information needed. Even though this low frequency large signal (LFLS) models system has wider capabilities than ideal average models system, it still can't predict all switching phenomena. Therefore, another benefit of this modeling approach is the ability to mix different types of models (low frequency large signal (LFLS) and detailed switching) based on the application study they are used for.

To the people I love the most,

my parents, Nadia & Mohamed,

my fiancée, Mostafa

and sisters, Noha & Marwa.

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Chapter 1 INTRODUCTION

1.1. Motivation

Most of today's power systems are moving towards being electronic because it offers a high potential for life-cycle cost savings, a great improvement in system efficiency, high density, voltage regulation, reliability, smaller size and lighter weight with continuous growth of system complexity [1]-[2]. This research is concerned with modeling these power electronics systems. Fig. 1-1 shows the generic architecture of a power electronics system used in this study. The first stage is the power source, which can be a battery or a high voltage storage system as in electric and hybrid-electric vehicles. It can also be photovoltaic arrays for a space station power system, or a generator as in an aircraft power system. There can be several generators in the system, but in standard operation mode a single generator provides energy to different loads [3]. The energy is transferred to the loads through different types of power electronic converters. One of the main loads in these types of systems is the motor drive, which usually consumes a large percentage of the total generated power. In the case of aircrafts, this corresponds to air blowers for cabin pressurization [4], in a ship the integrated power system corresponds to the propulsion motors [5], and in electric hybrid terrestrial vehicles it corresponds to the driving motor [6]. Moreover, in some vehicular applications, it is common to use a variable frequency constant voltage ac source because of its reduced maintenance costs [7].

Due to the size and complexity of most of these power systems, a good way to analyze them is through simulation. Simulation illustrates how the system performs based on the interaction between the different components in the system. It also provides a means for validating and verifying the models designed [8]. In addition, simulation

models minimize cost by avoiding repetitive hardware development, and minimize the concept-to-production time lag by improving the system reliability [9].

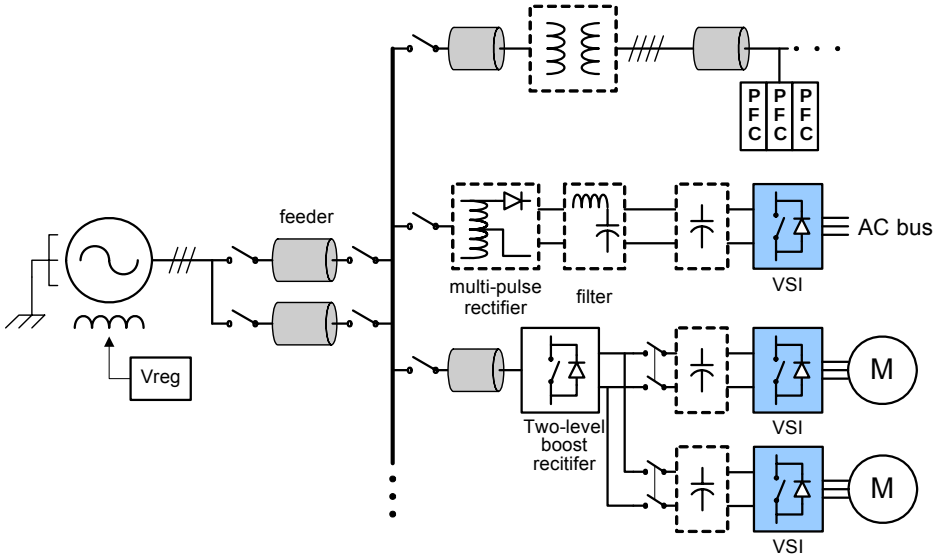


Fig. 1-1 Power electronics system.

There is always a demand for the development of accurate models that can correctly predict system performance. Switching models with detailed controllers are usually good candidates for accurate models since they can predict the switching ripple, model distortion and detailed transient information [10]. However, when implementing a large system using switching models, the system will reach a complication level that is difficult to implement in simulation. Moreover, in most application simulations, it is not necessary to represent detailed individual components, but what usually needs to be simulated are the terminal characteristics of a power electronic subsystem and how it interfaces with the connected systems [11]. In addition, detailed switching can compromise the numerical convergence of the solution. The other main drawback of using switching models is the long simulation time [12]. Therefore, it is useful to look at literature that uses switching models in small systems or individual component modeling as in [13] where a variable-speed cage machine wind generation system is modeled, simulated and validated experimentally. Although, this system consists of only four models, generator,

PWM rectifier, PWM inverter and a load, the author claimed the complexity of the system if represented with the full model. Hence, it is necessary to develop new accurate, time-efficient models that precisely reflect the performance of the system and that can be made more detailed or simplified depending on the application and type of study for which the system is used.

One simplification for switching models is in the case of switching function modeling of converters, which may help to improve the convergence and also speed up the simulations. Switching function implementation for a three phase voltage source inverter is described in [14]-[15]. The other type of model known in literature is the average model, which is a low-frequency, large-signal approximation of the real switching model. The average model is a good compromise between complexity, computing time and acceptable accuracy. However, these average models lose the large-signal phenomena as transients, distortions and harmonics. Fig. 1-2 shows a waveform representing the current waveform of an inverter in different cases as an example for the analysis. The figure shows the difference between the experimental prototype with and without an EMI filter. It can be seen that the EMI filter takes out all the high frequency harmonics. Practically, the EMI filter is part of the converter so it is the clean filtered waveform (pink) that we see on the bus when studying the system. Therefore, one should be concerned with the waveform with EMI filter. It can also be seen that the waveform with EMI filter contains some low harmonics and distortions and is not purely sinusoidal which means it represents more information than that retrieved by the ideal average model. This raises a question of whether the ideal average model satisfies the definition of being low-frequency, large-signal approximation of the real switching model and whether it is good enough for system representations or not. To answer this question the experimental result without the EMI filter is then averaged per-cycle and compared with the conventional ideal average model presented in the

literature depicting a pure sine wave that loses all harmonics of the model. It can be seen that the classical average model do not satisfy the definition of the average models being a low-frequency approximation, since it just represents fundamental frequency. A valid question in this case is why this conventional ideal average model could not be modified to predict these harmonics and distortions. Therefore, it is important to develop a new model that can capture these harmonics that are really affecting system interaction.

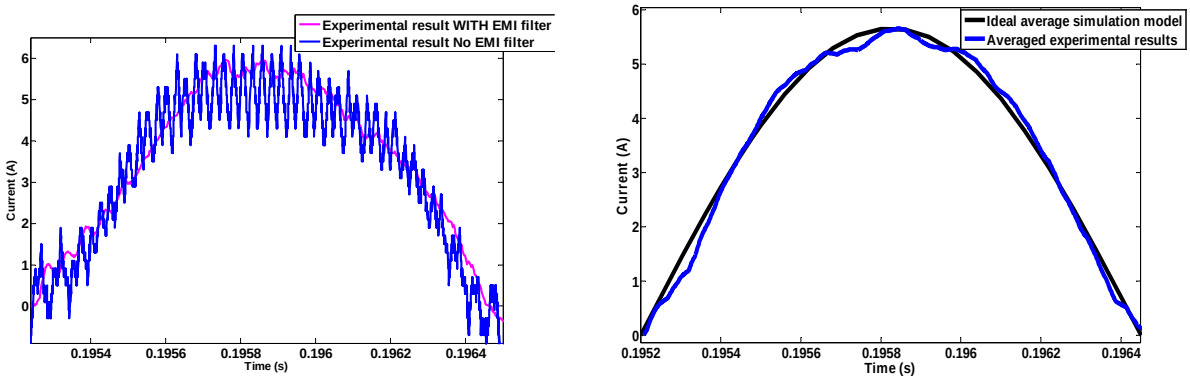


Fig. 1-2 Comparison between experimental prototype and switching simulation model for output phase current of an inverter, and per cycle averaged results with ideal average model.

1.2. Literature Survey

1.2.1. Modeling of Power Electronics Systems

System Modeling

The modeling of power electronic converters has generally followed two paths. One of these paths is through modeling the individual components where the converter model is derived from a detailed analysis of the operation that combines the component models. A different approach that avoids this complexity focuses on the relationships among the input/output magnitudes, producing models that are simpler, yet represent the original system under a limited set of circumstances [16]. In this way, a wide variety of models has been proposed, each one applicable for a particular study. Therefore, it is useful to be familiar with the models proposed in addition to the phenomena they describe and their range of validity [17]. Most of power electronics research is focused on analyzing each

converter individually in its stand-alone operation, rather than the reaction of this model in a complete system due to sophistication of most of these power systems [18]. In [19], a power electronics simulation blockset library is implemented in Matlab/Simulink that includes dc-dc converters, power-factor-correction rectifiers, electric drives, induction machines, dc machines, synchronous machines and more complete systems. These components are constructed in such a way where each component block has independent variables for inputs and delivers outputs which act as independent inputs to subsequent blocks.

There were some work on the system level modeling, but was concerned with large dc-dc systems where multiple dc-dc converters are used to supply needed power levels at different voltage levels. For example, many papers in the 90's were on the simulation of space station electric power system including multiple levels of switching dc-dc converters providing different electrical loads [20]. Another example for the large dc-dc systems modeling and simulation presented in literature is for a distributed power system and is shown in [10]. [21] presents the modeling and simulation of a large marine container ship power systems and [22] illustrates the dynamic performance of a 20-kHz spacecraft power system using computer simulation.

Recently, the power electronics systems are turning towards being ac/dc hybrid systems as mentioned in [1] and [23] for the different vehicular applications.

Most literature uses the state-space average modeling techniques in designing the large systems used in different applications. In [23] and [25] the modular modeling approach based on the generalized state space averaging method was used to model an additional multi-converter electric ship. In addition, in [26] the same approach was used to model active filter systems, where a linear set of state equations was derived from the non-linear equations of the system to obtain a quick approximation of the system and in more electric aircraft power systems in [27]. The same modular concept is also used in

spacecraft power systems modeling in literature, where the signal-block diagram based modeling is used [18],[20], and [28].

Modeling Software

There are several simulation programs available nowadays, however, the selection is based on the application of the system. The saber simulation program is software that is widely used since it allows for functional modeling using the MAST modeling language, SPICE-type model construction, and combined digital and analog capabilities. It is a robust simulator that allows for almost any size model, and has a large component library [29]-[32]. [33] gave an overview of modeling power semiconductor switches and models that are developed and given specifically for the SABER simulator. In addition, Saber is usually used in most multilevel simulations because it is capable of circuit partitioning and decoupling which allows for significant speed improvement when compared to modeling the whole power system as one block. In addition, it allows the user to reduce the large system into many small sub-systems [2]. For power electronic systems, most literature used the Matlab/Simulink for average modeling [34]-[35], and the spacecraft power systems used the EASY5 program, which is a software program developed by Boeing Computer Service [18],[20], and [28]. In [36] the authors used the SimPowerSystems tool in Simulink to develop a viable and effective integrated power system architecture for future naval platforms and claimed the tool to be inadequate in terms of parameter control and execution time. In [37] on the computer-aided analysis of the power converter systems, emphasis was laid on the global and sequential methods of analysis of power electronic converters, and converter-fed electrical machine drives using a dedicated power electronic system simulator called ATOSECS. The same author in [38] gives an update on the new simulation tools that are currently available with special emphasis on the analysis and design of power electronic converters that are used for power supplies. In addition, there was one power electronics toolbox that was discussed

in literature [39] in which the SimuPec was used with the Matlab/Simulink from the MathWorks Inc. The main features of this toolbox are the ability to model nonlinear components and circuit partioning and decoupling. Finally, [40] presents a complete survey on the different simulation tools available and its benefits depending on the different types of modeling and simulation tasks.

Multi-level Modeling

The type of models used in a system depends on the focus of the study. For example, if the user is interested in stability studies at one terminal, then average models can be used. However, if, for example, harmonic distortion is of interest, a detailed switching model that can capture this phenomenon would be more applicable. Literature discussed this point in [41]-[42] and concluded that when the focus of the study was the interaction between models and system stability, the average models were used. However, in [43]-[46] detailed switching models were needed for fault studies. A system that contains both average and detailed switching models can give a more broad choice of analysis; however, literature lacks this type of modeling.

1.2.2. Development of Low Frequency Large Signal (LFLS) Models

Types of Average models

Average models are a good compromise between complexity, computing time and acceptable accuracy. There are several kinds of average models that were discussed in the literature: the large signal average model that transforms an exact model into an average one, the small signal average model which is a linearized model around an operating point of the static converter, and the generalized average model [47]. The large signal model can include static parasitics such as capacitor ESR and a diode forward voltage drop [48]. The reason behind developing these average models is to answer these questions and others: 1) How to predict the dynamic behavior of a converter? 2) How to

design a controller? and 3) how to apply the linear control theory for analytical analysis? In order to apply linear control theory, we must first get a linear transfer function and a linear model. Literature first investigated open loop dc-dc converter, then closed loop ones and finally three phase converters. An ideal switching power converter usually consists of linear components like capacitors, inductors, transformers, voltage and current sources and nonlinear components which are the single pole multiple-throw switches. These switches are what need to be modeled in order to have a linear model that can be used to analyze the converter or to design controllers [49].

Averaging Techniques

In order to develop these types of average models, different techniques were used. The averaging techniques provide the analytical foundation for most power electronic design procedures at the system level. The three most popular approaches in dc-dc converters are the state space averaging method, the circuit averaging method and the injected-absorbed-current method. The state space averaging method was developed by Middlebrook [50] and its fundamental step is in replacement of the state-space descriptions of the two switched networks by their average over the single switching period, which results in a single continuous state-space equation designated by the basic averaged state-space model. The second averaging approach, the circuit averaging method, replaces each circuit element, whose terminal characteristics are given as instantaneous current and voltage relations, with a corresponding averaged circuit element. The averaged circuit element captures the relationship between the one-cycle average values of terminal quantities [51]. The third averaging approach, the injected-absorbed-current method, is based on the one-cycle average of instantaneous quantities. The relation between averaged terminal quantities of a switching cell is assumed to exist and is linearized. The most popular method of these mentioned above is the state-space averaging approach, which is due largely to its clear justification, simple

methodology, and demonstrated practical utility. However, there were some questions raised that led to the development of more advanced averaging techniques. Some of these questions include how far is the system approximated with average models, how can one quantify the errors incurred by that approximation, are the stability properties identical to real and average approximated model and what is the lower limit on the switching speed in order for averaging to be valid. All these questions are worth investigating, which is why literature is progressing in this area.

One modification to the average models was the ripple correction function. These functions can be found so that the behavior of a given converter can be estimated to obtain a larger degree of accuracy from the behavior of the averaged model. The ripple calculation is important for component selection and loss calculation [52]. Another correction of the average model can be made to the initial condition to improve its tracking of the actual system behavior when large transients appear [53]. In [51] a new averaging procedure is developed based on formal mathematical methods for periodic differential equations. This averaged model incorporates switching frequency effects and solves some of the limitations that existed in older averaged models. One of the limitations in the conventional averaged model was the steady-state dc offset error, which decreases as the switching frequency increases. It can often be compensated for by including an integrator in the control loop for variables of interest. Another limitation is the switching frequency effect on closed loop stability. The averaging approximation is based on the assumption that the switching frequency is "fast enough". While it is not known precisely how fast is "fast enough," designers typically take a rule-of-thumb to define linearized loop gain crossover frequency on the order of ¼ to 1/10 of the switching frequency. As a result of this, the transient performance is sometimes sacrificed. There are also other papers discussing the same issues and even extending the averaging theory to include feedback controlled converters [54]-[56]. A more general averaging procedure

is presented in [57] that is applicable to a much broader class of circuits than the state-space averaging as resonant type converters. This approach refines the theory of state-space averaging permitting a framework for analysis and design when small ripple conditions don't hold.

The theory is extended to three phase converters where in [58] a simple method of computing average and RMS currents is presented. These values are required to be able to select the right components. It was derived that the average and rms inverter currents are simple functions of a single factor equal to the product of the power factor and modulation index. There were different progresses in implementing average and small-signal models for three-phase PWM rectifiers. A reduced-order small-signal model for a three-phase power factor correction circuit is presented in [59]. This reduced-order model uses rearrangement of a PWM scheme to be viewed as two dc-dc converters for any 60 degrees interval. The PWM switch model of the dc-dc converters is then applied to these converters and a quasi-steady state model can be obtained. This slowly changing time-variant model is then "frozen" at an "average" operating point, which is defined by the rms value of the active line voltage in the 60 degrees interval. Since the two equivalent dc-dc converters have an identical "average" operating point, they are combined into one equivalent dc-dc converter, which is the reduced order model proposed. This way the three phase converter is modeled as a simple second-order system, which significantly simplifies control design and system analysis. This work continues in literature as in [60], where a systematic approach to small-signal modeling, and control design of three-phase PWM converters is presented.

A trial for the extension of the state space averaging method to the dc-ac converters is found in [61], where the time-varying nature of the switching systems is eliminated by equational *D-Q* transformation. The equational approach is limited to low-order systems having fewer than four reactive elements since manipulating matrices with an order

higher than four is very difficult. Following that, a new circuit D-Q transformation technique is identified in [62]. This is a simple and useful method in the analysis of ac converters and is used quit frequently in literature. The development of average models continues to be an interesting subject. As of 2009, [63] redefined a new-formed average model for three phase boost rectifiers that has less assumptions than those found in other literature. For example, the new model is suitable for any input/output voltage waveforms, regardless of whether they are sinusoidal or non-sinusoidal, balanced or unbalanced.

Control Strategies

Averaging also provides a framework for evaluation of the different control strategies for various types of converters. From the different control strategies for dc-dc converters is the peak current-mode control [64] where only the switch current is sensed, compared with the control voltage derived from the voltage loop and no compensation exists in the current loop. The modification to that is the average current-mode control where the inductor current is averaged and compensated by a compensation network. The output of the compensator is compared with a sawtooth ramp to generate PWM control [65]. The other type is the PWM conductance control proposed in [66] senses the inductor current and compares it with a triangular ramp to generate PWM control. Adding an integral-lead network to the current loop makes PWM conductance control similar to average current-mode control [67]. One concern about the current-mode control is the subharmonic oscillations at half the switching frequency. [68] presents a method based on switching function principles to represent any high-performance switch modules by an ideal switch in combination with basic logic elements. This method depends on the terminal behavior, not on the overall circuit behavior. It helps to show the forward voltage drops in diodes that contribute to waveform distortion and losses in many applications. As with the averaging techniques, the control strategies expand on three-phase PWM rectifiers. In [69], an average current control is presented with three

linear analog compensators (so both plant and compensator are in the rotating plane) and six-step PWM. It is a simple design; however, the closed-loop performance is based significantly on the compensator design. In addition, in [70] the application of average current model control to a three phase boost rectifier applied to small wind turbines is presented. This way reduces the input current total harmonic distortion (THD) and increase the PF in the rectifier. In [71] a review of the different current controllers for VSI-PWM inverters is presented. It shows that the hysteresis controller with three independent controls is the simplest to implement. The predictive controllers are the most complex and require knowledge of the load and extensive hardware which may limit the dynamic response of the controller. The ramp comparison controller has the advantage of limiting the maximum inverter switching frequency and producing well defined harmonics, but the controller requires a large gain and compensation to reduce the current error and generally has a lower bandwidth than hysteresis controllers. A combination of a ramp comparison controller for low-speed operation and a simple hysteresis controller for high-speed operation may provide a good overall solution.

1.2.3. Causes of low-frequency distortions

The previous two sections discussed the progress of research in the average modeling area starting from dc-dc converters and going into three phase dc-ac and ac-dc converters. From this we can conclude that the average models (small-signal models in particular) are good for control purposes or for steady state system analysis, however these average models miss the large-signal phenomena representations such as distortions, harmonics, and transients. This section will go through some of the causes for these distortions and how literature handles it.

Among these phenomena are various types of modulation schemes [72]-[73]. The earliest modulation types were widely used for carrier-based PWM and were sinusoidal modulation signals [74]. Following that the use of an injected zero-sequence signal for a

three-phase inverter [75] initiated the research on a non-sinusoidal carrier-based PWM [76]-[80]. Different zero-sequence signals lead to different non-sinusoidal PWM modulators. Research then developed another PWM method, which is the space vector modulation method for three-phase converters [81]-[88]. This method uses the space-vector (SVM) concept to compute the duty cycle of the switches. There are two types, continuous and discontinuous SVM. The discontinuous SVM reduces the switching losses; however, it introduces harmonics around $\frac{1}{2T_s}$ [72].

There are other phenomena that cause waveform distortion like the dead time that is inevitable to prevent the shoot-through phenomenon [89]-[93]. The dead time is the necessary blanking time that guarantees that both switches in an inverter leg never conduct simultaneously. These delays are added to the device turn on and turn off times and introduce a load dependent magnitude and phase error in the output voltage [94]-[98]. Since this delay occurs in every PWM cycle, the magnitude of the error grows in proportional to the switching frequency, introducing a serious waveform distortion and fundamental voltage drop [91]. This distortion introduces harmonic components that if not compensated for, may cause instabilities as well as losses in the converter. In addition to that, another cause of voltage distortion is due to the inherent characteristics of the switching devices as the voltage drops during the on-state [98], and the turn on/off time of the switches [107].

Previous literature concentrates on developing compensation methods for these types of phenomena in a switching model but none actually implements them in an average model. In most cases, the compensation techniques are based on an average value theory; the lost volt-seconds are averaged over an entire cycle and added to the commanded voltage [100]-[106]. An important issue that is seen in these dead time compensation techniques is that they are all based on the polarity of the current. This will cause a problem around the zero-crossings and therefore, an accurate measurement of the

currents is needed to correctly compensate for the dead time [100]. In [105], Itkonen described how dead-time effects can be taken into account in the switching-function-based model. The proposed method makes it possible to study how the dead-time effects affect the behavior of the system without using the detailed device models. There were some attempts to model average dc-dc power converters including semiconductor device non-linearities. The algorithm used is based on the bond graph technique and the causality analysis [108]. The purpose of this is to estimate the dissipated power in the different circuit devices [109].

The last phenomenon that was considered is the minimum pulse-width constraint [110]-[112]. This phenomenon is seen because of the slow switching properties of thyristors, which will cause a limitation on the maximum and minimum pulse-widths that can be achieved [113]. This was largely forgotten with the usage of fast switching insulated gate bipolar transistors (IGBT) but it is still occasionally an issue. The technique that is widely used in literature is to drop the pulse if its width is smaller than a defined one.

1.2.4. Model Verification and Validation

The problem as stated in previous sections is that simulation models are used for analysis and design of complex integrated systems. There are many decisions that are made based on results obtained from these computer models, however, there is no confidence these results are right. This is due to the lack of knowledge of how accurate these models are, and what assumptions they have. Therefore, it is really important to incorporate formal verification and validation methods during the development process of these simulation models. Literature discussed the general definitions for verification and validation and some rules to follow in the process; however, little was applied to power electronics models and systems.

Verification is the process of determining that a model implementation accurately represents the developer's conceptual description of the model and the solution to the model. Verification is commonly divided into two types: code verification and solution verifications. The code verification part is when the activities are directed toward finding and removing mistakes in the source code, finding and removing errors in numerical algorithms and improving software using software quality assurance practices. The solution verification activities are directed toward assuring the accuracy of input data for the problem of interest, estimating the numerical solution error and assuring the accuracy of output data for the problem of interest.

Validation is the process of determining the degree to which a model is an accurate representation of the real world from the perspective of the intended uses of the model. The main goal of validation is to characterize and minimize the uncertainties and errors in the computational model as well as in the experimental data. It increases confidence in the quantitative predictive capability of the computational model. Validation procedure does not imply that the experimental data is always correct because the experimental uncertainty estimates may be very large or unknown bias errors can exist in the experimental data. Therefore, the validation experiments can be conducted at different levels in a hierarchy of complexity and various system response quantities can each be used in a validation metric [114]-[116].

1.2.5. Power Electronics Systems Stability

Many efforts have been devoted to the research of power electronics system stability. There are three types of stability analyses: steady state, small-signal and large signal analysis [117]. Steady state analysis is the first step to approach a system stability study that provides useful understanding of the system behavior. The next step in a system stability study is the small-signal analysis. The small-signal analysis uses

linearized averaged models around the equilibrium point of interest. This allows using different analytical tools that can help in the study as Bode, Nyquist and root loci plots. The small signal system stability analysis is usually done following Middlebrook's work [118] based on the impedance criterion, which ensures stability by preventing the loop gain Z_o/Z_i from circling (-1,0) point in the s-plane by ensuring this condition $\left|\frac{Z_o}{Z_i}\right| < 1$ is satisfied. This design criterion is quite conservative as much of the forbidden region in Nyquist plane has little influence on stability. Therefore, different criteria were developed like the opposing component criterion and gain and phase margin criterion (GMPM) that are considered less artificially conservative [119]-[122]. Following that, a new stability criterion was proposed in the form of a forbidden region for the locus of the return ratio $Z_{source}(s) / Z_{load}(s)$ on which the stability of the dc interface depended [123]. This new criterion was extensively used in very large scale dc distributed power systems (DPS), like the International Space Station, by redefining the forbidden region for cascaded parallel loads [124]-[125].

It was not until Hiti's work in the early 1990's that the equivalent impedance based approach was developed for ac power systems [126]-[127]. In perfect dualism of Middlebrook's approach, Hiti et al. proposed the study of the synchronous *d-q* frame return ratio matrix $\mathbf{Z}_{sdq}(s) \cdot \mathbf{Y}_{Ldq}(s)$ to study the stability of three-phase ac power system interfaces, using conventional multivariable linear control theory to limit the source and load impedance magnitudes. This method though conservative was used as the main criterion for the design of three-phase EMI filters for three-phase AFE converters [128]-[130]. A later improvement of this method was proposed in [131]-[132] using the multivariable Nyquist diagram instead to evaluate the stability of the *d-q* frame return ratio matrix $\mathbf{Z}_{sdq}(s) \cdot \mathbf{Y}_{Ldq}(s)$. A significant, yet unnoticed contribution aiding in the reduction of the conservative nature of all ac stability criteria developed, was presented

by Mao et al. in 1996 [133]-[134]. While developing a reduced order model for AFE converters, Mao showed the direct association between the power transfer channel (in the *d-q* frame) and the constant power load dynamic of these converters, showing that the conventional Nyquist criterion could be used to study the stability of the converter using the reduced order model developed.

A key breakthrough was accomplished by Belkhayat who in 1997 proposed a further improvement over Hiti's work by employing the generalized Nyquist stability criterion (GNC) to assess the stability of ac interfaces in the *d-q* frame [135]-[136]. The GNC developed by MacFarlane and Postlethwaite in the 1970's [137]-[140], consolidated the frequency-response control methods developed for multivariable linear systems [141]-[144], and provided the complete dual development of the classical single-input single-output control theory [145]-[149] for multivariable systems [150]-[163]. Although the approach was not used finally for the control of multivariable systems [163], its stability analysis capabilities have proven to be extremely valuable for ac distributed power systems. The stability assessment based on the GNC has become the main practical approach used for the design and synthesis of ac power systems, where the *d-q* frame source and load impedance specifications can be applied mirroring Middlebrook's method for dc distributed power systems [164]-[165]. The GNC-based method has matured to the point where multiple practical *d-q* frame impedance measurement tools have been developed [166]-[170]; however the high mathematical intricateness of the approach has severely limited the usage of this stability criterion. Furthermore, the veiled relationship between the source and load *d-q* frame impedances and the characteristic loci of the return-ratio matrix $\mathbf{Z}_{sdq}(s) \cdot \mathbf{Y}_{Ldq}(s)$ has made its usage even more restricted.

Small-signal analysis does not always ensure stability in the large-signal sense, therefore the stability margins based on the small signal study are often quite conservative and the large signal stability study is necessary. The large signal stability

analysis is usually performed using computer simulations. It is examined through the response of the system to different types of transient changes and its ability to withstand or recover from these large perturbations [23]. These transients can be a large change in the system parameters, which can correspond to a load step; or could be a change in the system's structure, as when faults appear in the system and a branch is disconnected. There are different faults to be studied; for example, short circuit, open circuit and switch failures. The time domain computer simulation approach is not considered an efficient way in terms of use of the computational resources. However, it still continues to be the most used practice, especially when detailed models are required and it can produce accurate results based on the correctness of the models developed. Therefore, some literature has been devoted to the modeling and implementation of stability studies in computers and the use of time domain simulations as a basis for the stability analysis [171]-[173]. The literature known criteria and ways of analysis discussed above will be used to validate the low frequency large signal (LFLS) models developed in this research. The performance of these models will be compared to the detailed switching models under similar scenarios.

1.3. Objectives

The main objective of this research is to model ac/dc hybrid power systems with large number of power converters, which can be used for a variety of applications like automotive, ship spacecraft or aircraft. The main challenge is to have the complete system with proper types of models, perform well without migrating into simulation problems (either numerical or long simulation time). In order to achieve this goal, this research focused on developing new type of models named low frequency large signal (LFLS) models that are some type of average models that are simplified, fast, have minimal convergence and numerical errors but can capture many of the large-signal phenomena that are only seen by the switching models. The models are to be

implemented in a circuit simulator as electrical circuit based models. After developing these models, the challenge is to be able to use them to model a large system and to be able to capture the real transient behavior of the system, such as the startup, inrush current and power flow directionality, in addition to some low-frequency harmonic distortion phenomena. Another benefit and challenge of these models, is to be able to combine them with switching models in one system and mix them depending on the application of the system. Saber will be used as the simulation tool for this modeling research task due to its many capabilities described in the literature review. However, the same modeling approach can be applied with any simulation tool.

With this type of models in hand, we need to predict how accurate they are, and what assumptions they have therefore a validation procedure will be developed and applied to one power electronics converter (two-level boost rectifier) as an example. The models are then validated on the system level. The system will be used for different types of analysis like stability, harmonics and fault analysis.

1.4. Dissertation Outline and Summary of Contributions

Chapter 2 of this report will discuss the development of the low frequency large signal (LFLS) models that can capture the low frequency harmonics just seen by the switching models. The development process will be applied to a voltage source inverter (VSI) as an example. It will start with the ideal average model proposed in literature and then discuss the different low frequency phenomena modeled like modulation control methods, which is usually in average models represented by the sinusoidal duty cycles part only. However, in this research different zero-sequence signals were implemented and added to the sinusoidal modulation signals to generate a more realistic model. Other phenomenon modeled is the dead time and non-linearities due to turn on/turn off and voltage drop on switching devices. It will also discuss the effect of the passive

components of the model, for example, the inductor and its current ripple. These low frequency large signal (LFLS) average models will be capable of predicting some of the switching current ripples and with that a better current polarity judgment can take place around zero crossings. These models will also have the capability of computing the losses of the converters, which is one concern that was discussed thoroughly in the literature. All these phenomena were discussed in the switching model literature and as mentioned, the literature proposed different compensation methods for these distortions. However, in this research, some of the methods developed in the literature are used in a reverse way to introduce the harmonics into the classical average model to become more realistic and accurate as the switching model. This chapter will also capture and compare the performance of the detailed switching model with the new low frequency large signal (LFLS) model. It will also present the experimental prototype for the voltage source inverter model developed and will discuss some model validation. The validation done is power quality validation where the normal steady state performance in time domain is analyzed and also the frequency characteristics. In addition, some transient and voltage regulation under load steps is also studied. The model is also validated for small-signal stability and impedance measurements. Another example that will also be presented in this chapter is the two level boost rectifier applying the same types of distortions to it.

Chapter 3 will present an analytical small-signal model for the voltage source inverter (VSI) considering the effect of dead time and different types of space vector modulation used. It presented a time-invariant model that could be easily converted into the synchronous *d-q* frame and used for control and stability analysis. The model is compared to a detailed switching model, low frequency large signal model and to a 2kW experimental prototype.

Chapter 4 will introduce a verification, validation and uncertainty quantification procedure that can be applied to any power electronics converter. The chapter will show

the analysis of the procedure using a two-level boost rectifier. It will discuss the general approach following these steps: 1) modeling and simulation approach, 2) planning and prioritization, 3) code and solution verification, 4) model validation and finally 5) uncertainty quantification and predictive capability.

Chapter 5 will discuss the modeling aspects of the new LFLS studied power electronics system. It will give enough details on the individual equipment modeling with special concern on the practical considerations for system modeling and the issues faced while modeling this power electronics system. The main issues are how the models can capture transients, the subsystem connections and the system grounding issues. It will also focus on one branch of the large system presented and show it can be used for different studies as regeneration for example.

Chapter 6 will summarize all the work done and discuss the future work that can be done.

Chapter 2 LOW FREQUENCY LARGE SIGNAL (LFLS) VOLTAGE SOURCE INVERTER (VSI) MODEL PREDICTING LOW FREQUENCY HARMONICS

2.1. Introduction

This chapter presents a low frequency large signal model of a voltage source inverter (VSI) that can accurately predict some of the low frequency phenomena only seen by the switching models. These phenomena include the dead time, voltage drop across switching devices (switch & diode), different modulation techniques and minimum pulse width effect. In addition, the effect of the inductor current ripple is analyzed, enhancing the accuracy near the zero crossings. Simulation and experimental results with a 2 kW prototype are used for validation purposes. The low frequency large signal (LFLS) model simulation showed very good matching with the simulation switching model, less than 0.5% difference in time domain and frequency domain analysis.

2.2. Proposed Voltage Source Inverter Average (LFLS) Model

Fig. 2-1 shows the circuit schematic of the VSI model considered in this study, which is comprised of a power stage, controller, modulation and passive elements. The power stage is modeled as an ideal average model with Eqn 5-1 in the *abc*-coordinates as shown in Fig. 2-2. The controller is in the *dq*-frame.

The inverter parameters are as follows, it is a 2 kW prototype implemented in Saber running at about 1.5kW, the dc link voltage v_{dc}=300 V, the output phase rms voltage is 60 V, rms phase current is 4 A and the load resistor is 15 Ω. Fig. 2-3 shows the simulation results for the ideal VSI average model defined here, output rms voltage, current and duty cycle of the three phases respectively.

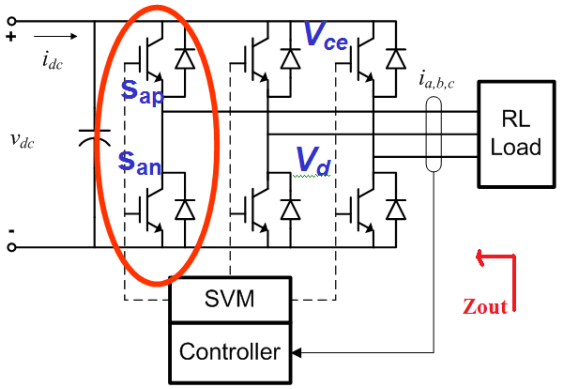


Fig. 2-1 VSI switching model schematic

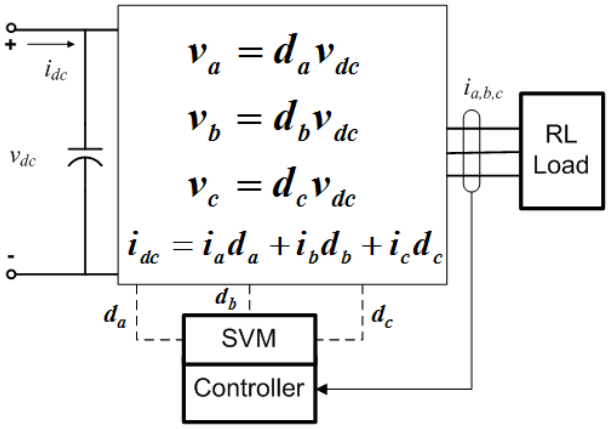


Fig. 2-2 Diagram of the VSI average model considered in this study

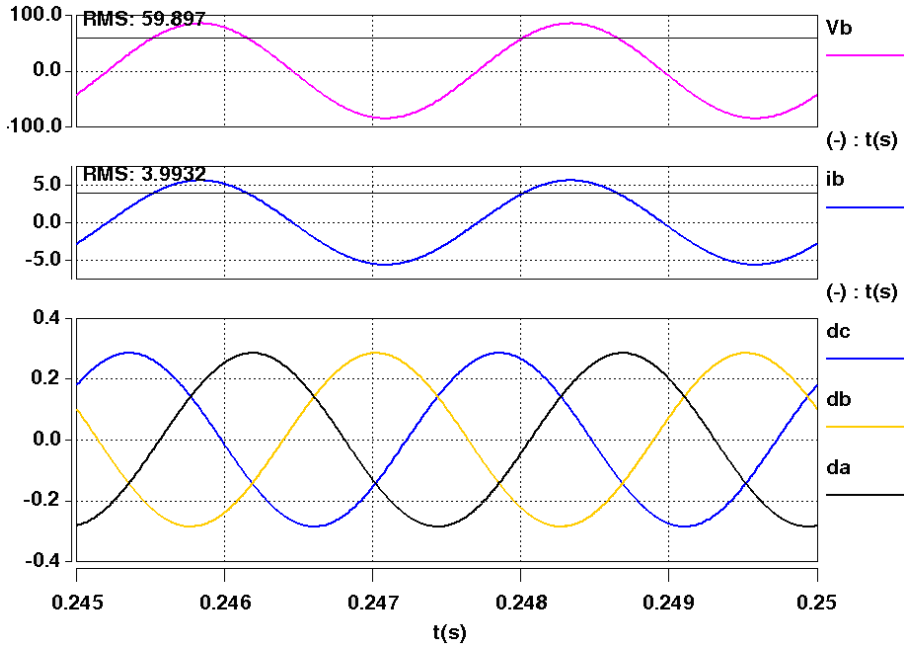


Fig. 2-3 Simulation results for ideal VSI average model proposed.

2.3. Different Low Frequency Phenomena Modeled

2.3.1. Modulation Control Methods

The ideal inverter simulation in the previous section shows pure sinusoidal PWM waveforms where it just represents the fundamental signals with no injected harmonics. The first modification for the model to be more realistic is to include the zero-sequence into the PWM waveforms. This signal depends on the distribution of the zero vector and

the type of modulation control used [71]. In [71] a unified representation for the zero-sequence signal $e_i(t)$ is given in Eqn 2-1:

$$e_i(t) = k_o(1 - u_{max}(t)) + (1 - k_o)(-1 - u_{min}(t)), \qquad 0 \le k_o \le 1 \qquad \text{Eqn 2-1}$$

and $u_i(t)$ is the fundamental sinusoidal waveforms, $u_{min}(t)$ and $u_{max}(t)$ is the minimum and maximum of the three phases respectively. For continuous symmetrical PWM (SYPWM), $k_o = 0.5$ and this means the two zero vectors are equally distributed. Fig. 2-4 shows the vector distribution in sector 1 and Fig. 2-5 shows the modulation signals for one phase, with the injected zero sequence. This modulation scheme has six commutations per switching cycle but since it is symmetric then it has lower total harmonic distortion.

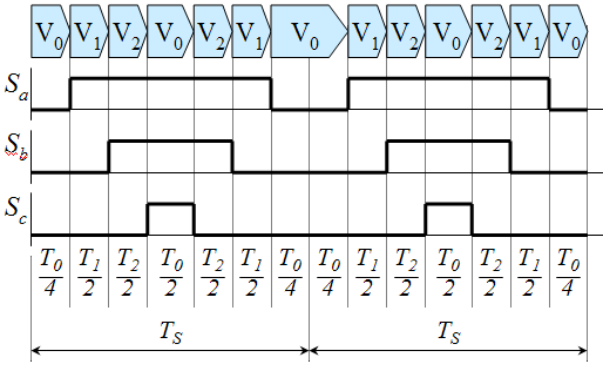


Fig. 2-4 Continuous symmetrical PWM vectors in sector 1.

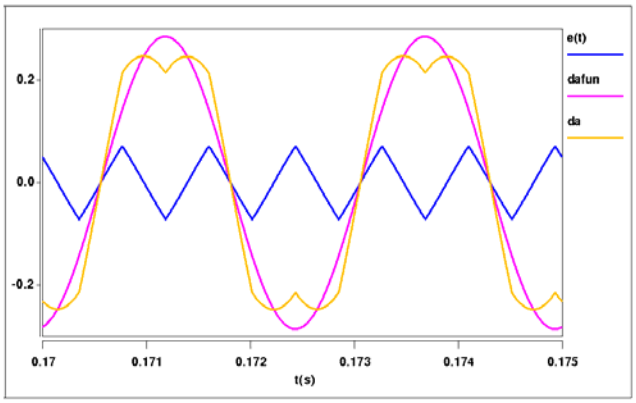


Fig. 2-5 Modulation signals for continuous symmetrical PWM.

For discontinuous PWM, there are different types of modulation schemes implemented as the two extremes, the DPWMMAX where the zero vector (111) is used for the six sectors and the DPWMMIN where the zero vector (000) is used, in this case for the six vectors. In addition to those two, there are many different modulation schemes that can be constructed; an example of which is the 2-phase right aligned (2-Φ RA) SVM, which is presented in Fig. 2-6. This modulation method has only four commutations

which will reduce the switching losses, however it will introduce harmonics at around $\frac{1}{2T_s}$. For each of these modulation schemes the zero vector can be constructed using Eqn 2-2 and added to the sinusoidal PWM to get the modulation signals needed.

$$e_i(t)=\frac{1}{3}(u_a(t)+u_b(t)+u_c(t)) \qquad \text{Eqn 2-2}$$

where $u_a(t),u_b(t),u_c(t)$ is the fundamental sinusoidal waveforms for phase a, b, and c respectively. Table 2-1 shows the zero-sequence representations and space voltage vectors used for all six sectors to achieve this discontinuous 2-Φ RA. Fig. 2-7 shows the resulted modulation signals for the discontinuous 2-Φ RA modulation scheme.

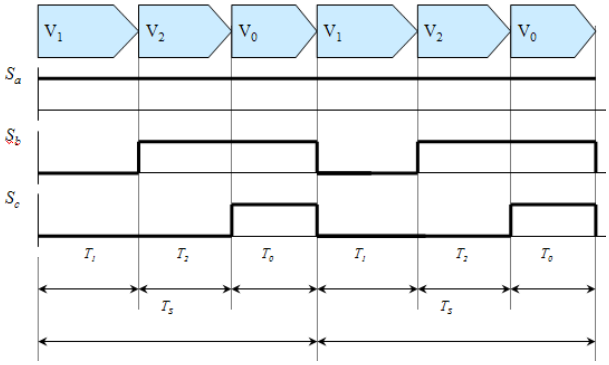


Fig. 2-6 Discontinuous 2-Φ RA modulation vectors in sector 1.

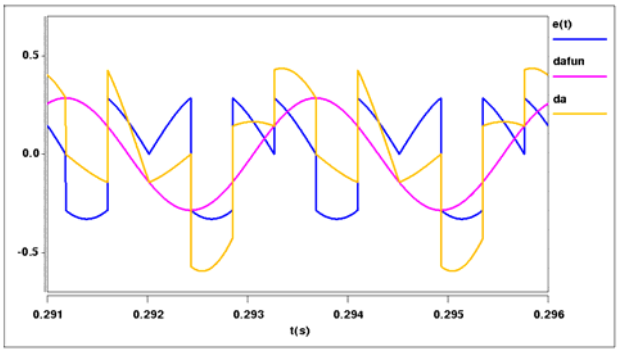


Fig. 2-7 Modulation signals for discontinuous 2-Φ RA modulation PWM.

Table 2-1The Zero Sequence calculated for each sector for 2-Φ RA modulation

Sector NO.	Space voltage vectors	Zero sequence $e_i(t)$
I	T_s=T_1 (100)+T_2 (110)+T_0 (111)	$e_i(t)=\frac{T_0}{Ts}+\frac{1}{3}\frac{T_2}{Ts}-\frac{1}{3}\frac{T_1}{Ts}$
II	T_s= T_1 (110)+T_2 (010)+T_0 (000)	$e_i(t)=\frac{-T_0}{Ts}-\frac{1}{3}\frac{T_2}{Ts}+\frac{1}{3}\frac{T_1}{Ts}$
III	T_s= T_1 (010)+ T_2 (011)+T_0 (111)	$e_i(t)=\frac{T_0}{Ts}+\frac{1}{3}\frac{T_2}{Ts}-\frac{1}{3}\frac{T_1}{Ts}$
IV	T_s= T_1 (011)+ T_2 (001)+ T_0 (000)	$e_i(t)=\frac{-T_0}{Ts}-\frac{1}{3}\frac{T_2}{Ts}+\frac{1}{3}\frac{T_1}{Ts}$

V	$T_s = T_1(001) + T_2(101) + T_0(111)$	$e_i(t) = \frac{T_0}{Ts} + \frac{1}{3}\frac{T_2}{Ts} - \frac{1}{3}\frac{T_1}{Ts}$
VI	$T_s = T_1(101) + T_2(100) + T_0(000)$	$e_i(t) = \frac{-T_0}{Ts} - \frac{1}{3}\frac{T_2}{Ts} + \frac{1}{3}\frac{T_1}{Ts}$

2.3.2. Sampling Effects

The effects caused by the sample and hold functions of the modulator could also be modeled by adding a clock to the modulator block with a sampling frequency equal to the switching frequency of the converter. The calculated duty cycles are updated only at the beginning of each new switching cycle. Fig. 2-8 compares the continuous and discrete sampling effect on the phase A current. It shows the duty cycle for phase A without and with the effect of sampling respectively.

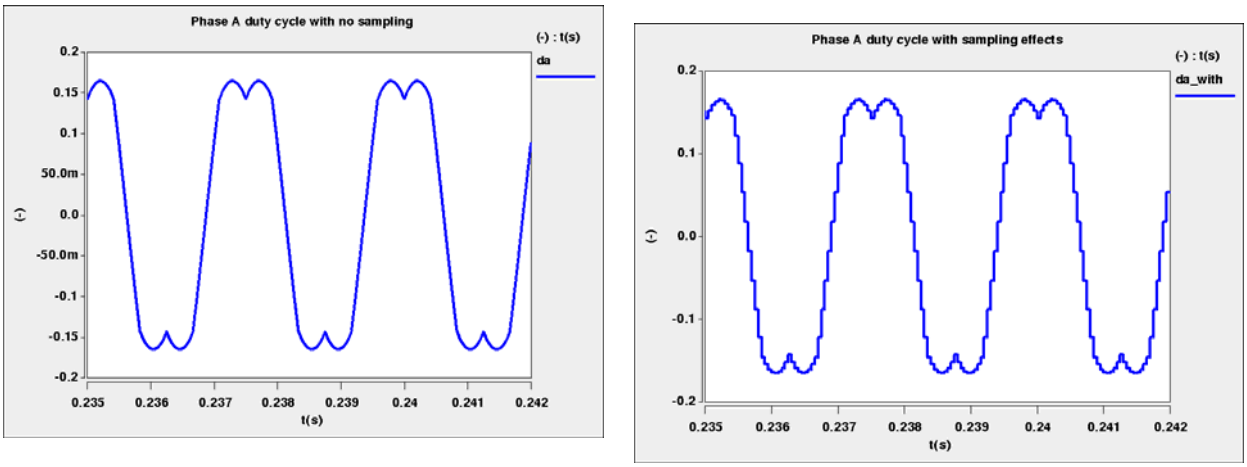


Fig. 2-8 Modulation signal for phase A without sampling (left) and with discrete sampling of 20kHz (right).

Fig. 2-9 shows the effect of sampling on the output current waveform for phase A. It can be seen that the current has these bumps which equals to the switching frequency. For this case, it is equal to 20 kHz as shown from the zoomed part in Fig. 2-9.

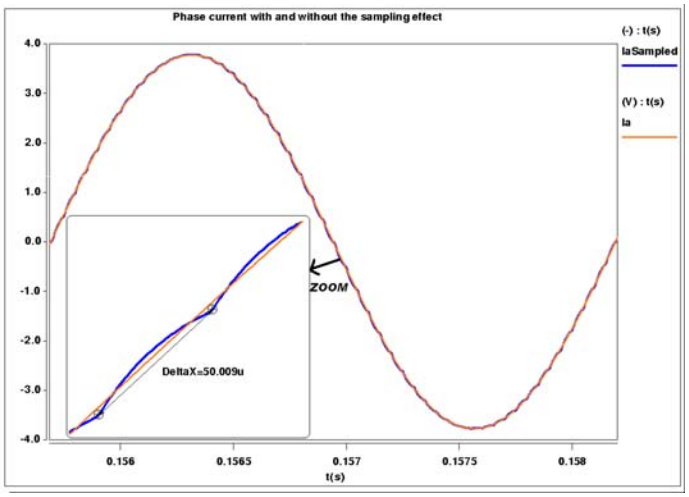


Fig. 2-9 Effect of sampling on output current for phase A.

2.3.3. Dead time and Non-linearities due to Turn On/off and Voltage Drop on Switching Devices

The third important phenomenon implemented is the dead time. The dead time is a blanking time to avoid the so-called shoot-through of the dc link. This time guarantee that both switches in an inverter leg never conduct simultaneously [89]. For switching model, dead time is generated by delaying the switching time as shown in the third and fourth waveforms (sapwithDT, sanwithDT) in Fig. 2-10. From Fig. 2-10, it can be seen that time error in the on time duration resulting from dead time is given by Eqn 2-3.

$$T_{err} = \left[-\frac{T_{off}}{2} + \frac{T_{on}}{2} + T_d \right] \text{sign}(i) \qquad \& \qquad \text{sign}(i) = \begin{bmatrix} 1 : when\ i > 0 \\ -1 : when\ i < 0 \end{bmatrix} \qquad \text{Eqn 2-3}$$

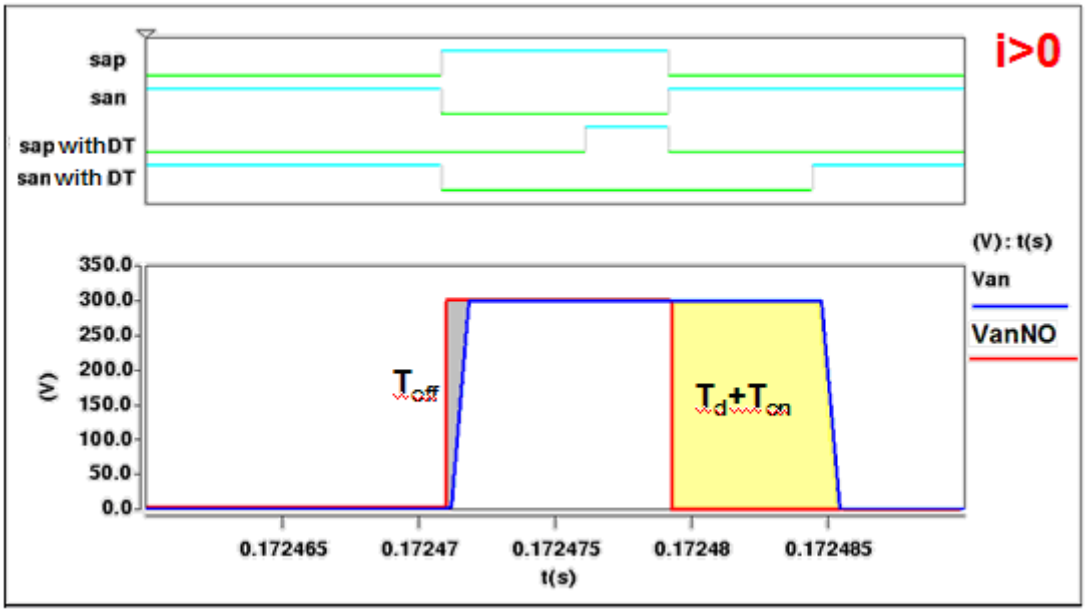


Fig. 2-10 From top to bottom – Switching signals for phase leg A top and bottom switches without (sap, san) and with deadtime (sapwithDT, sanwithDT) and phase A voltage to neutral without (VanNO) and with deadtime (Van)

For the ideal average model, the error time is added to the commanded time duration T_{com} so that the effective time duration T_{eff} is the summation of both as given in Eqn 2-4:

$$\boldsymbol{T_{eff} = T_{com} + \left[\left(-\frac{T_{off}}{2} + \frac{T_{on}}{2} + T_d\right)\right] sign\,(i)} \qquad \text{Eqn 2-4}$$

In addition to the effect of the dead time and the turn on and off time of the switches, there are some non-linearities caused by the voltage drop across the switch (V_{ce}) & on the voltage of the diode (V_d) as shown in Fig. 2-1. This can be realized in the model by adding the error caused by the voltage drop to the error time in Eqn 2-3 giving the new effective duty cycle as in Eqn 2-5:

$$\boldsymbol{d_{eff} = d_{com} + \left[\left(-\frac{d_{off}}{2} + \frac{d_{on}}{2} + d_d\right) + d_{com}(V_{ce}/V_{dc}) + (1 - d_{com})(V_d/V_{dc})\right] sign\,(i)} \qquad \text{Eqn 2-5}$$

Fig. 2-11 shows the phase A current comparison in the ideal case with no distortion and with the effect of dead time of 5μs and non-linearities due to turn on/off of 1μs and voltage drop on switching devices of 0.7V on the diode and 1.2V on the switch with and without the sampling effect.

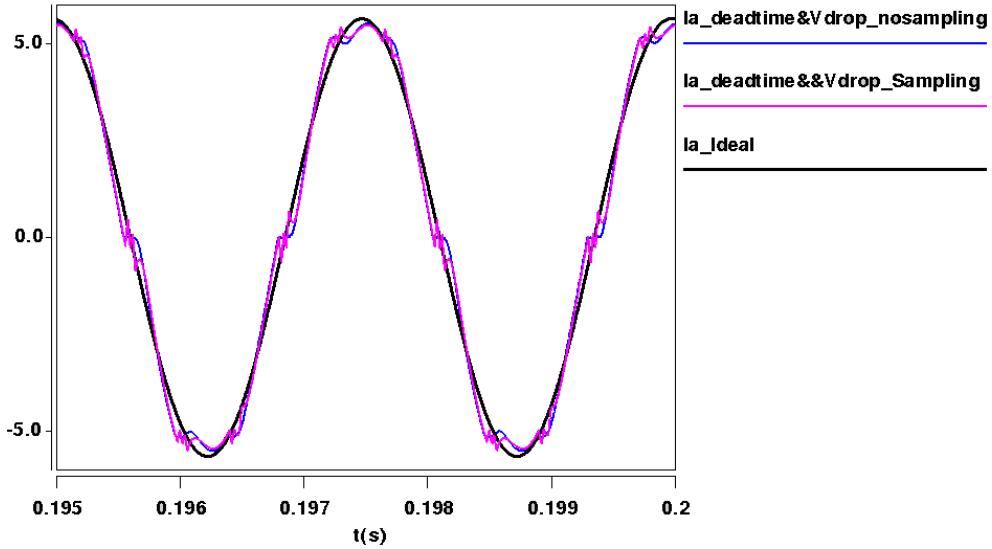


Fig. 2-11 Phase A current for proposed model with and without the effect of zero sequence signal and dead time.

This section showed how the dead time effect was implemented in the enhanced average model (LFLS model). However, as mentioned the method of implementation was taken by reversing the literature known. Old research was concerned with developing new methods for compensating this dead time effect in the switching models and it was here used to distort the average models. Therefore it is important to study the performance of the LFLS model with this compensation and to compare it to both switching and experimental prototype when the compensation is added. This comparison was done to prove the validity of the LFLS model, although the main task was to develop models that can predict the distortions.

2.3.4. Minimum Pulse-width

Another important source of distortion is the minimum pulse-width (MPW) limitations that result when small on-time duration of the switches cannot be achieved. Such limitations may have to be enforced to prevent damage of the semiconductors switches as this MPW can be smaller than the on and off time of the switch [111]. In a switching model, this can be easily implemented by comparing the width of the pulse of the gating signal to the minimum pulse allowed duration and if it is smaller then it gets deleted. However, in the proposed LFLS model, a limit is enforced on the duty cycle achievable. The minimum allowed duty cycle is given in Eqn 2-6 and if the duty cycle is smaller then it is deleted.

$$d_{min} = \left(\frac{T_{deadtime} + T_{MPW}}{T_s} \right) \qquad \text{Eqn 2-6}$$

Fig. 2-12 depicts the difference between the phase A current with all discussed distortion phenomena added except the MPW and with the MPW phenomenon added to the model.

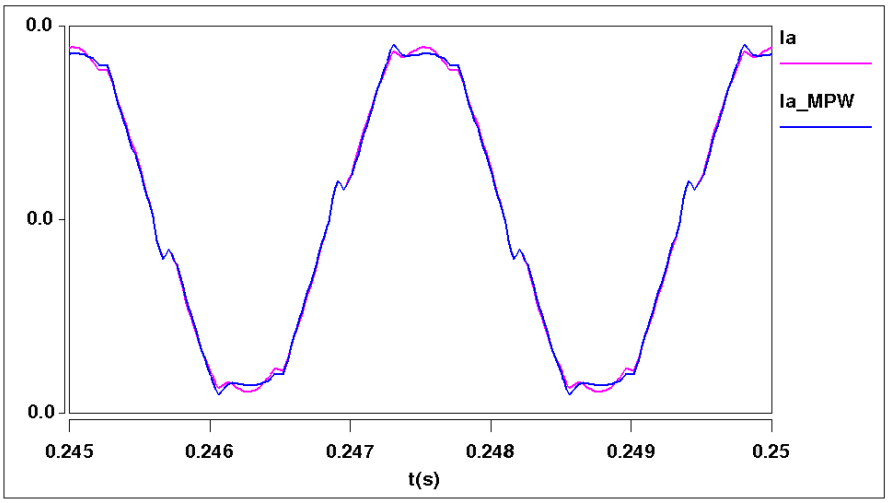


Fig. 2-12 Phase A current for proposed model with distortion but without MPW effect and with MPW effect respectively.

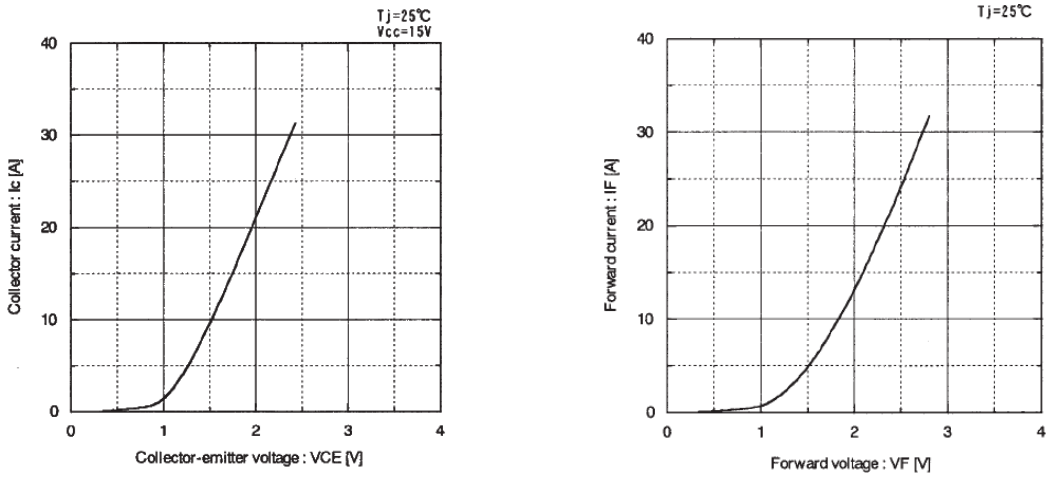
2.4. Loss Calculation for Switching and Low Frequency Large Signal Model (LFLS)

For this study, the 6-pack IGBT IPMs from Fuji (6MBP20RH060) (600V, 20A) that is used in the experimental prototype, is the one used for the loss calculation. The datasheet of Fuji (6MBP20RH060) is used to provide the data of the IGBT and diode which could be used in loss calculation as shown in Table 2-2 and Fig. 2-13. For the LFLS model, the losses are calculated using the equation below, however, for the switching model, the losses can be measured directly from the simulation. This section will show both the calculation and the measurement and compare the results.

Table 2-2 Data needed for loss calculation from datasheet of Fuji (6MBP20RH060)

Collector-Emitter saturation voltage	$V_{CE\ (sat)}$	Ic=20A	2.7	V
Forward voltage of FWD	V_F	–Ic=20A	3.5	V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Switching time (IGBT) See Fig. 3	ton	Ic=20A, VDC=300V	0.5	–	–	μs
	toff	Inductive-Load	–	–	3.5	μs
Switching time (FWD)	trr		–	–	0.5	μs



$$R_{CE} = \frac{2.4 - 1.5}{30 - 10} = 0.045\Omega \qquad R_{diode} = \frac{2.3 - 1.5}{30 - 5} = 0.032\Omega$$

Fig. 2-13 Output characteristics of IGBT (left) and diode (right).

2.4.1. Switching Losses

Turn on losses:

It is the sum of 1) the switch-on energy without taking the reverse recovery process into account , 2)switch-on energy caused by the reverse-recovery of the diode. Eqn 2-7 shows the turn on losses:

$$E_{turn\_on} = E_{turn\_on0}\frac{vi}{V_o I_o} + E_{rr}\frac{vi}{V_o I_o} = (1.5m + 0.2m)\frac{300 \cdot i}{600 \cdot 20} + (0.2m)\frac{3.5 \cdot i}{600 \cdot 20} \qquad \text{Eqn 2-7}$$

$E_{turn\_on0}, V_o, I_o, E_{rr}$ can be found from the data sheets as shown in Fig. 2-14.

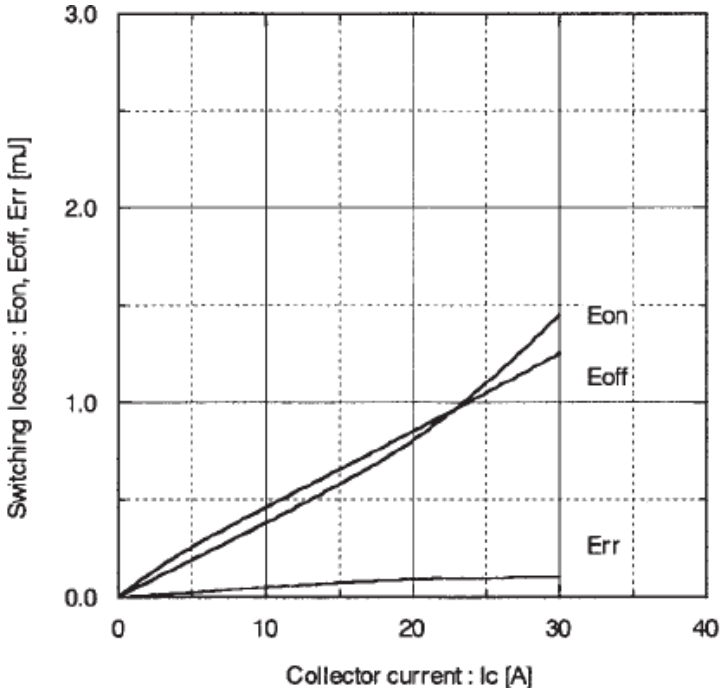


Fig. 2-14 Collector current Ic versus switching losses.

Turn off losses:

Eqn 2-8 shows the turn off losses of the IGBT:

$$\boldsymbol{E_{turn\_off}} = \boldsymbol{E_{turn\_off\,0}} \frac{\boldsymbol{vi}}{\boldsymbol{V_o I_o}} = (1.2\boldsymbol{m}) \frac{300 \cdot \boldsymbol{i}}{600 \cdot 20} \qquad \text{Eqn 2-8}$$

where $E_{turn\_off\,0}, V_o, I_o$ are all found from the data sheets as shown in Fig. 2-14.

The average current is found by integrating across the sine wave, since for this case, the DPWM modulation is used, which means for a 60 degrees period, one of the phases is clamped, the average current is given as,

$$i = I_{average} = I_B \frac{\left(\int_0^{78.8^\circ} \sin\theta \, d\theta + \int_{138.18^\circ}^{180^\circ} \sin\theta \, d\theta \right)}{\pi} = 1.8943 \text{ A} \qquad \text{Eqn 2-9}$$

Plugging the current in the energy equations Eqn 2.7 and Eqn 2.8 above,

$\boldsymbol{E_{turn\_on}} = 8.050758 \times 10^{-5} \boldsymbol{J}$

$\boldsymbol{E_{turn\_off}} = 5.68288 \times 10^{-5} \boldsymbol{J}$

So the switching power loss for each phase leg is given as,

Turn on losses:

$$\boldsymbol{P_{turn\_on}} = \boldsymbol{E_{turn\_on}}(\boldsymbol{f_s}) = 1.6101516\boldsymbol{W}$$

Turn off losses:

$$\boldsymbol{P_{turn\_off}} = \boldsymbol{E_{turn\_off}}(\boldsymbol{f_s}) = 1.1365776\boldsymbol{W}$$

Where f_s=20kHz

Total switching losses for each IGBT:

$$\boldsymbol{P_{T\_sw}} = \frac{(\boldsymbol{E_{turn\_on}} + \boldsymbol{E_{turn\_off}})(\boldsymbol{f_s})}{2} = \frac{2.74673\boldsymbol{W}}{2} = 1.3733646\boldsymbol{W}$$

For switching model, Eqn 2-7 and 2-8 are used for the losses calculation, but the current and voltage are measured directly from the simulation model. Fig. 2-17 shows the comparison between the turn on and turn off losses for the switching and LFLS model.

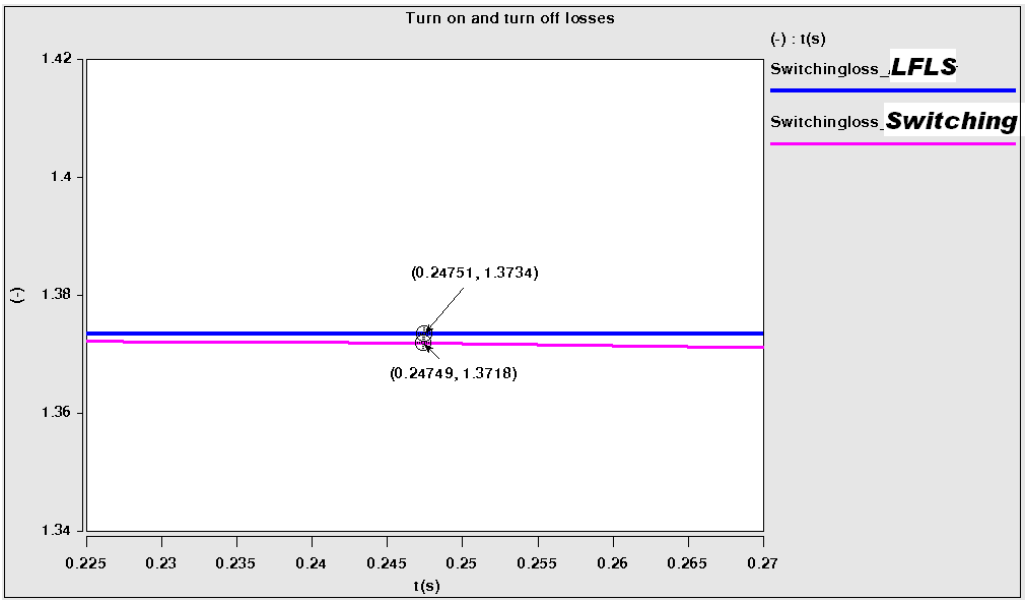


Fig. 2-15 Switching turn on and turn off losses comparison.

2.4.2. Conduction Losses:

The conduction losses equations for DSVM are derived as,

The energy for conduction losses of one phase of the IGBT is,

$$E_{IGBT\_conduction} = \begin{cases} d \cdot (V_{CE} + R_{igbt} I) \cdot I & (I > 0) \\ (1-d) \cdot (V_{CE} + R_{igbt} I) \cdot I & (I < 0) \end{cases} \qquad \text{Eqn 2-10}$$

The energy for conduction losses of one phase of the diode is,

$$E_{diode\_conduction} = \begin{cases} (1-d) \cdot (V_{diode} + R_{diode} I) & (I > 0) \\ d \cdot (V_{diode} + R_{diode} I) \cdot I & (I < 0) \end{cases} \qquad \text{Eqn 2-11}$$

From the data sheet, the on voltage and resistance can be calculated as shown in Table 2-2 and Fig. 2-13. The energy E is then calculated per phase by measuring the current and

duty cycle for each phase, summing them for the three phases and then dividing by six to get the result for each IGBT. The same procedure is applied to the switching model, however for this case, the energy for conduction losses is as follows:

The energy for conduction losses of one phase of the IGBT is,

$$E_{IGBT\_conduction} = \begin{cases} (V_{CE} + R_{igbt} I_{igbt}) \cdot I_{igbt} \\ 0 \end{cases} \qquad \text{Eqn 2-12}$$

And the energy for conduction losses of one phase of the diode is,

$$E_{diode\_conduction} = \begin{cases} (V_{diode} + R_{diode} I_{diode}) I_{diode} \\ 0 \end{cases} \qquad \text{Eqn 2-13}$$

Finally, the conduction loss for one IGBT can be calculated as,

$$P_{IGBT\_con} = E_{IGBT\_con} / T$$

And the conduction loss for one diode is,

$$P_{diode\_con} = E_{IGBT\_con} / T$$

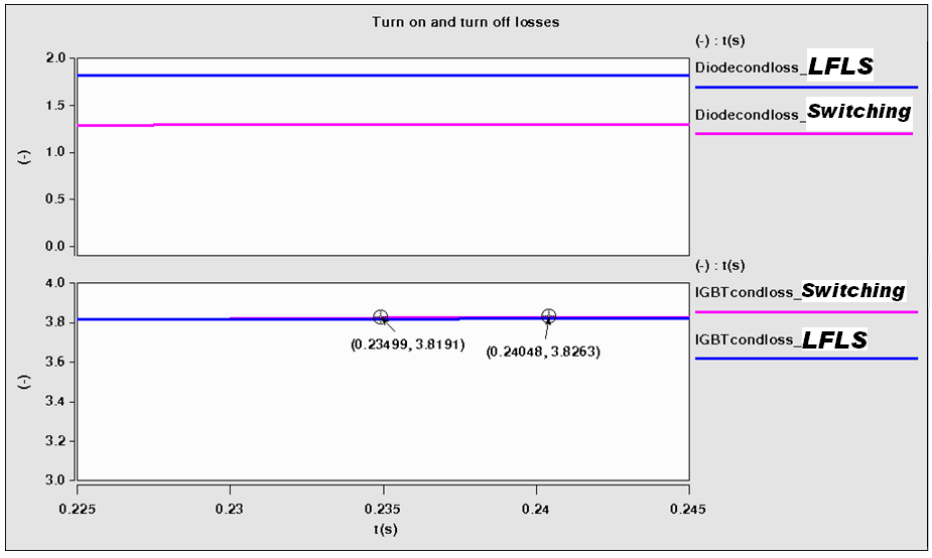


Fig. 2-16 Conduction losses comparison for LFLS and switching model.

2.5. Comparing the Performance of Switching and LFLS Model

The average model proposed (LFLS) in the previous section with all the different low frequency harmonics phenomena discussed is compared to a switching model with the same exact parameters and the results are compared in this section. Fig. 2-17 shows the comparison between the real switching and LFLS model when no distortion is enforced. It compares the phase B current. Fig. 2-18 shows the same current with the distortion added: 5μs dead time, on and off time of 1μs, voltage drop across the switch of 1.2V, diode on voltage of 0.7V and 1μs minimum pulse width.

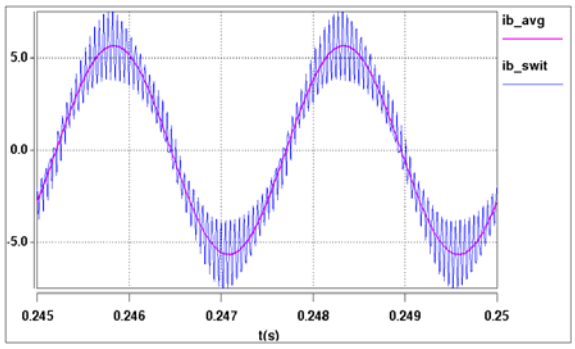


Fig. 2-17 Low frequency large signal model and switching model comparison without distortion.

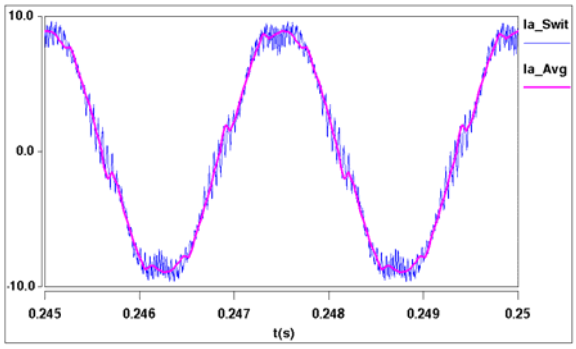


Fig. 2-18 Low frequency large signal model & switching model comparison with distortion.

It is hard to compare the switching and low frequency large signal model due to the switching ripple shown in Fig. 2-17 and Fig. 2-18. Since this analysis is concerned with the low frequency harmonics and not the switching frequency ones, the switching current waveform is averaged over one switching cycle and compared to the low frequency large signal model in Fig. 2-19. From looking at the time domain waveform, it can be seen that the two waveforms match very well. However, a more accurate way of verifying the results is to calculate the deviation percentage between both waveforms. This percentage is calculated using Eqn 2-14,

$$Deviation = \frac{1}{X_{RMS}} \sqrt{\frac{1}{N} \sum_{i=1}^{N} \left(x_{i\,swi} - x_{i\,avg} \right)^2} \qquad \text{Eqn 2-14}$$

Using the above equation, each point is subtracted from the corresponding one and the relative error is calculated and normalized using RMS current. The percentage error between the two models is 2.32%.

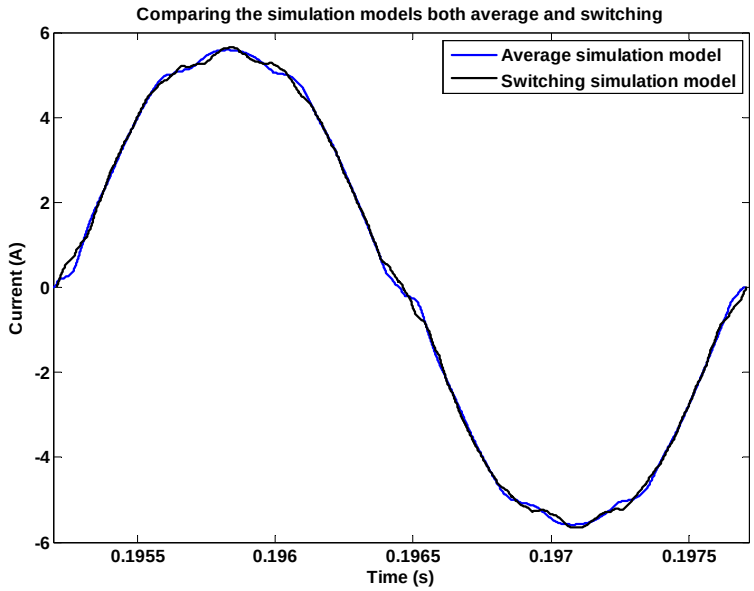


Fig. 2-19 Low frequency large signal model and averaged switching model comparison with distortion.

2.6. Low Frequency Large Signal (LFLS) Model Improvement

It can be seen from the previous section results that most of the 2.32% discrepancies between the switching and low frequency large signal model center on the zero crossing areas. This is reflected on the top and bottom of the waveform due to the two other phases zero crossings. It can be seen from Eqn 2-5 that the error in the duty cycle depends on the direction of the current (whether positive or negative). In addition, the low frequency large signal model doesn't model the switching ripple therefore the judgment for the current direction will not be correct near the zero crossings areas. Therefore, in order to improve the performance of the LFLS model, the current switching ripple has to be taken into consideration. The current ripple can be calculated as in Eqn 2-15:

$$\Delta I = \frac{V_L}{L}\Delta T \qquad \text{Eqn 2-15}$$

Where L is the output inductor of the VSI, V_L is the voltage across the inductor, and ΔT is the time change. The ripple is calculated for each sector. It is then added to the average (LFLS) currents and this total current is the one used for sign*(i)* judgment in duty cycle error calculation. Fig. 2-20 shows the switching current waveform averaged over one switching cycle and compared to the low frequency large signal model current waveform taking current ripple into consideration. The percentage error between the two models is recalculated using Eqn 2-14 and it is now reduced to 0.41%.

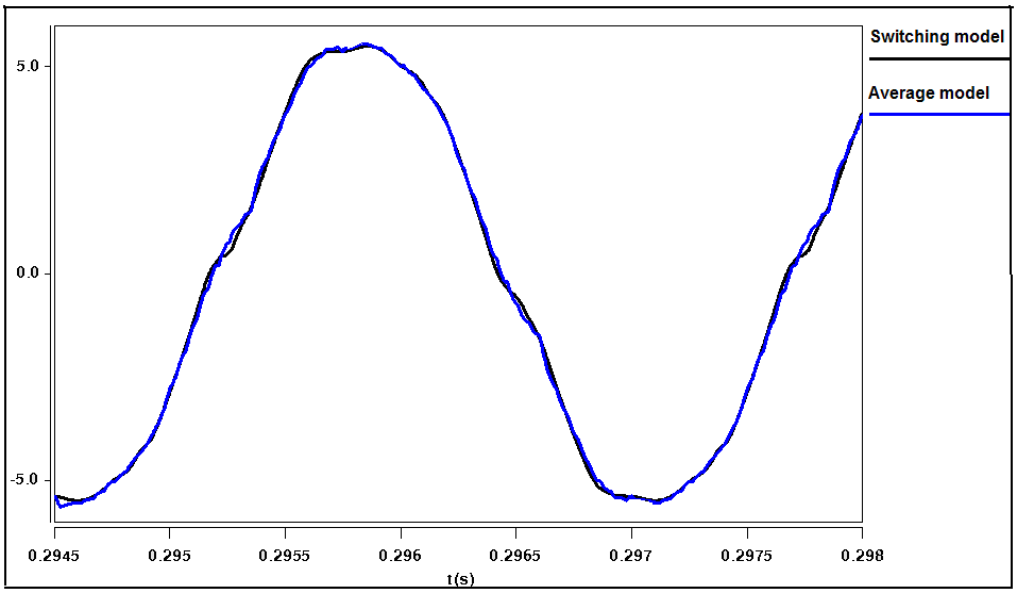


Fig. 2-20 Low frequency large signal model and averaged switching model comparison with ripple calculation improvement.

2.7. Simulation Time Comparison

In addition to the comparison above, the models simulation time was compared for a 0.2s simulation time window. The ideal average model with no distortion has the least simulation time (1.7 min) followed by the new low frequency large signal (LFLS) model with distortion (2.38 min) and finally the switching model almost 4 times more than the

low frequency large signal (LFLS) model time (8.1 min). So although there is a penalty paid when using the low frequency large signal (LFLS) models on the simulation time, the benefit of low frequency modeling is more significant than the time in this case. This is because the low frequency large signal (LFLS) model still has a much lower simulation time than the switching model; almost four times shorter time, and is a very good predictor of the performance (low frequency) as shown.

2.8. Experimental Validation for Low Frequency Large Signal Voltage Source Inverter Model

To validate the proposed low frequency large signal (LFLS) voltage source inverter model, a 2kW prototype setup is built. Fig. 2-21 shows the construction. A 6-pack IGBT IPMs from Fuji (6MBP20RH060) (600V, 20A) is used. The output inductance per phase is 600μH. The control board is DSP-FPGA digital controller.

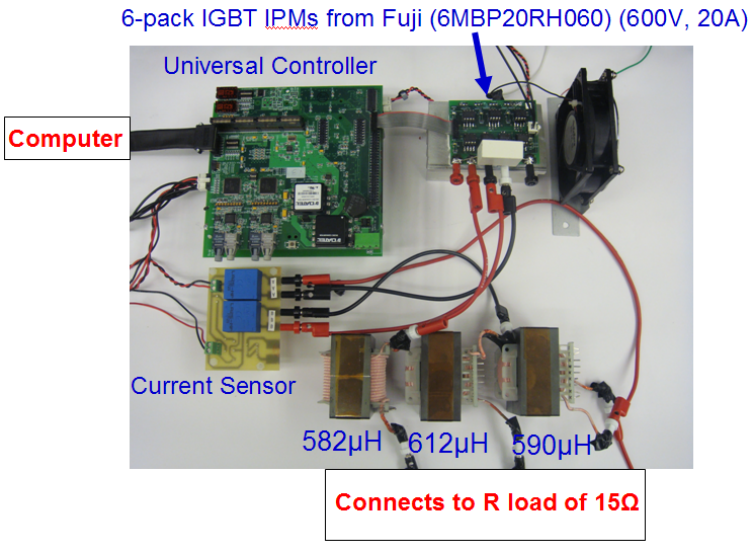


Fig. 2-21 Experimental Setup

In order to have a good validated model, many things needed to be taken into consideration during the prototype implementation process. From these issues, is the accurate measurement of all passives and for that all the parasitics are measured accurately and added to the simulation models for fair comparison. In addition, the effect

of filters, delays of the A/D and D/A boards and sensor gains are all added to the models too. Another important quantity that affects the model is the controller parameters. Controller affect transients and system response greatly and therefore it is an important point in validation. Finally, the effect of the sources and loads can be huge on the model design. For example, for this model working as an active rectifier, the experimental prototype was tested under two different sources and it was seen that the output impedance of the two sources is so different and this difference is affecting the rectified current and its harmonics. Fig. 2-22 shows the phase current using two different ac power supplies.

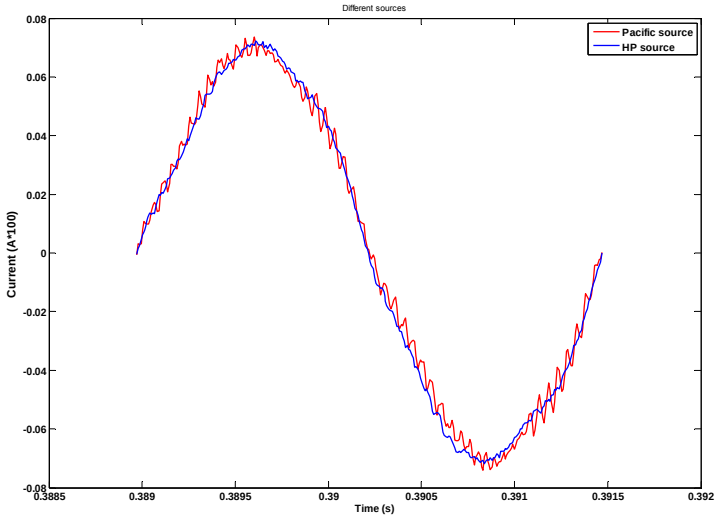


Fig. 2-22 Phase current under the effect of two different ac power supplies. (Pacific ac power source: Model 390-G, Hp source: Model:6834B rated: 300Vrms, 4500VA 1Φ-3Φ)

2.8.1. Time domain steady state validation

The validation process is divided into two sets, power quality validation, and impedance measurement validation. The power quality validation will be divided into normal steady state validation that will include time domain and frequency domain and transients and voltage regulation under load steps. However, this section will concentrate on the time domain validation part. For this part, the ac output current waveforms are measured and

compared versus the LFLS simulation model as done in the previous section comparing the detailed switching model instead. The error percentage is again calculated the same way using Eqn 2-14 where now the waveforms compared are the averaged experimental versus the low frequency large signal (LFLS) simulation model.

Fig. 2-23 compares both the experimental phase B current averaged over one cycle with the LFLS simulation model current without ripple taken into consideration. The percentage error is given as 8.74% calculated with Eqn 2-14 and mostly the differences are around the zero crossing.

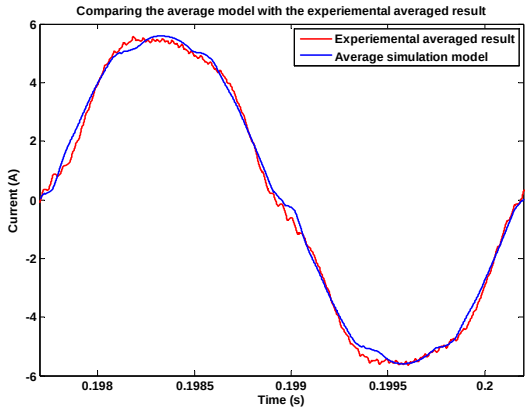


Fig. 2-23 LFLS and experimental model performance comparison for phase A current with distortions

Fig. 2-24 shows the result when the ripple calculated is added. Fig. 2-24 compares the experimental prototype to the ideal average model and the LFLS model. It can be seen that the percentage error between the averaged experimental result and the LFLS model decreased to 2.37% from 8.74% with considering the ripple effect. It can also be seen that the deviation percentage between the experimental prototype and the ideal average model is 19.94% which means the LFLS is 10 times better than the ideal average model in harmonics prediction.

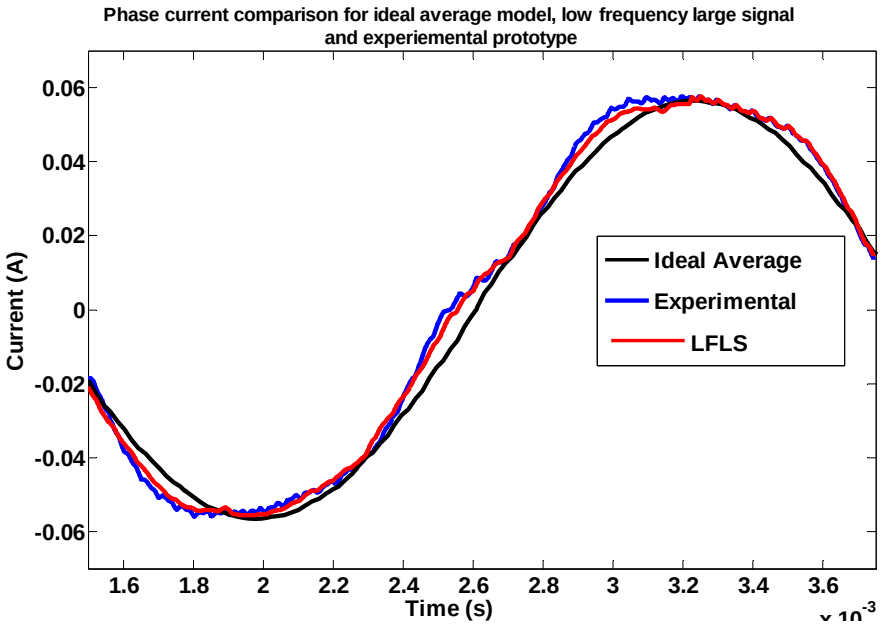


Fig. 2-24 LFLS, ideal average and experimental model performance comparison for phase A current with distortions

2.8.2. Frequency domain steady state validation

This section is a continuation of the power quality validation looking at the frequency characteristics. Fig. 2-25 compares the harmonic spectrum of phase A current for the three models (real switching model, low frequency large signal (LFLS) model and experimental prototype). The fundamental harmonic is about 5.72A (magnitude) and the figure zooms on the sub harmonics that are high enough to be investigated, therefore, it concentrates from the 5^{th} harmonic till half the switching frequency (10kHz) which is around the 23^{rd} harmonic. It can be seen that the simulation models (LFLS and switching) matches very well in most points while the experimental is little higher. Calculating the percentage of deviation or error using Eqn 2-14 and over the region given in Fig. 2-25, it is found to be 0.85% between the experimental prototype and the low frequency large signal (LFLS) model and 0.28% between the real switching simulation model and the LFLS model. The total harmonic distortion for the three models is around 4.2%.

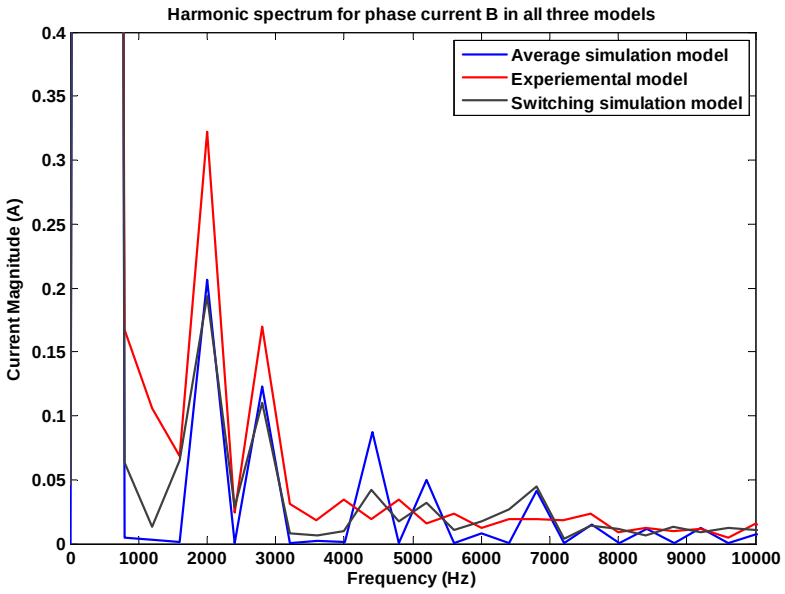


Fig. 2-25 Harmonic spectrum comparison for LFLS, switching simulation models and experimental model for phase A current with distortions and ripple consideration

2.8.3. Impedance measurement validation

The low frequency large signal (LFLS) model proposed here is also capable of predicting the right impedance of the converter. For this validation test an open loop VSI model is used because the impedance can be easily derived analytically using the conventional small-signal model known in literature. The low frequency large signal (LFLS) model was then used to measure the impedance (Z_{out}) looking into the converter as shown in Fig. 2-1 and compared to the real experiment measurement found with the help of an impedance measurement tool developed in [180], the detailed switching model and the derived analytical result.

The results showed a good match between the experimental results, detailed switching model and the low frequency large signal (LFLS) model proposed. However, the derived analytical result showed an inductor as the impedance representation which when compared to the real prototype results in a new missing damping factor in VSI in the d-q axis. This damping factor was predicted to be due to the nonlinearities of the model like

the dead time, losses and the modulation schemes that was modeled in this dissertation and that is why the low frequency large signal (LFLS) model was capable of predicting them. Fig. 2-26 shows the comparison results between the detailed switching model, the low frequency large signal (LFLS) model and the experimental prototype with the two types of modulation discussed (continuous and discontinuous SVM) and under 1us dead time. It can be seen that the results match very good within +2, 3 dB and 6 degrees which is within the error limit of the equipment used, till the high frequencies when it starts to divert. This can also be predicted since the measurement equipment used is only valid till this range and not for higher frequencies. It can also be seen from Fig. 2-26 that the discontinuous space vector modulation type (DSVM) has lower damping in the Z_{dd} axes than the continuous space vector modulation type (CSVM). This can be explained since for DSVM, there is one phase that is clamped for 60 degrees and only two phases switching as shown in Fig. 2-6 which means there is only four commutations, however for CSVM, all three phases are switching which means there is six commutations and this would cause more losses that can be seen on the direct active axes $Z_{dd.}$

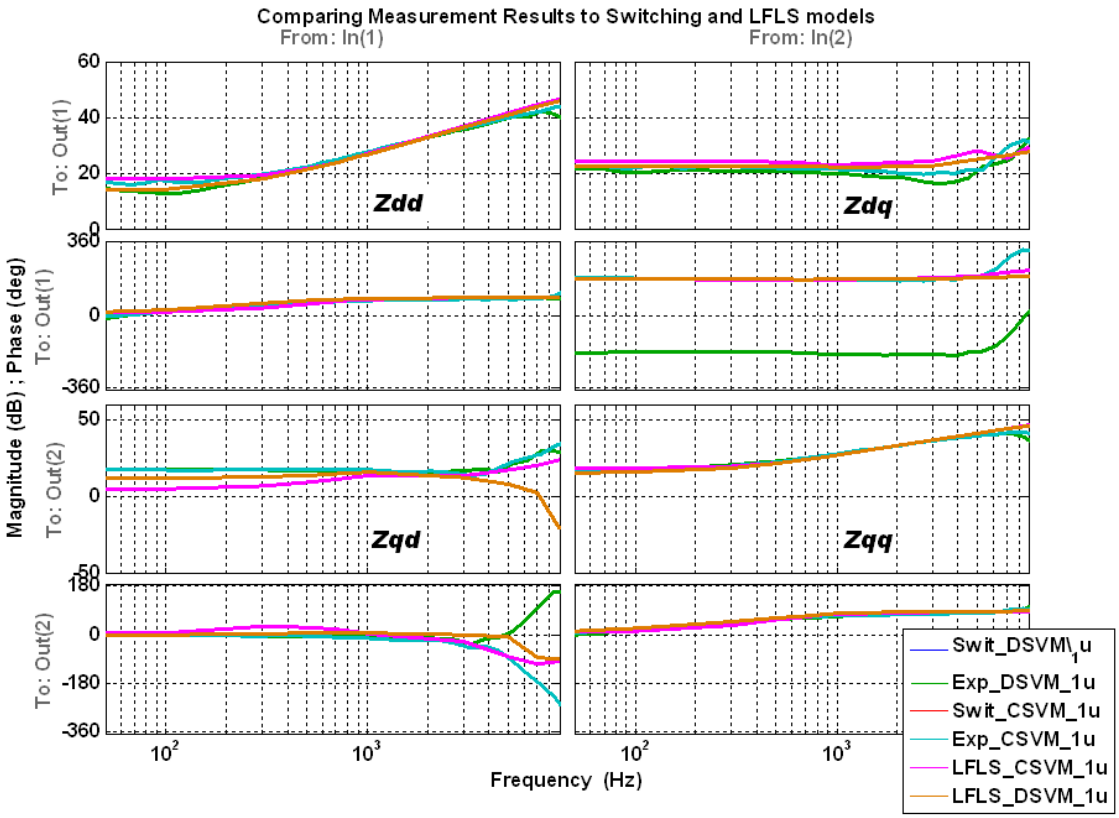


Fig. 2-26 Switching, LFLS model and experimental impedance measurement comparison for both types of modulation and 1μs dead time.

2.9. Low Frequency Large Signal (LFLS) Model of a Voltage Source Inverter Operating as a Boost Rectifier

In order to validate the model proposed, different topologies are modeled. This section modifies the two-level three-phase active rectifier defined in Fig. 5-3. The model parameters are as follows: a 25kW model implemented in Saber, the output dc link voltage v_{dc}=650 V, the input phase rms voltage is 230 V. The controller consists of two dq current loops and an output voltage loop to regulate the dc link voltage. Fig. 2-27 compares phase A input current for both switching and low frequency large signal (LFLS) models with continuous space vector modulation method under the same distortion of a dead time of 5μs, on and off time of the switch of 1μs, a voltage drop on the switch of 1.2V and a diode on voltage of 0.7V.

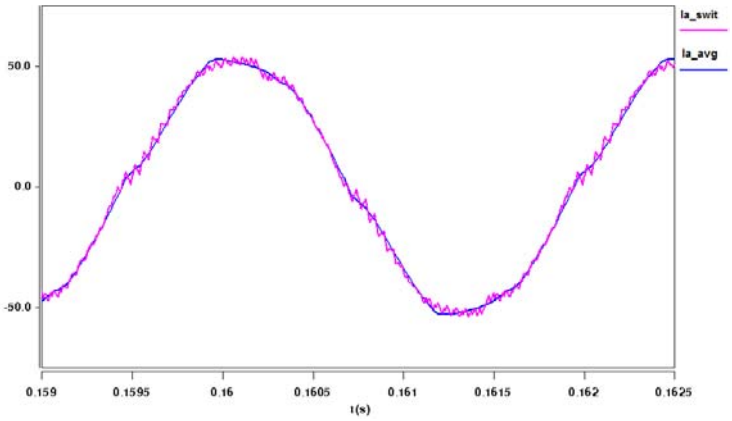


Fig. 2-27 LFLS model and switching model comparison for phase A input current of rectifier with continuous SVM and distortions

Fig. 2-28 compares the total harmonic distortion (THD) for both switching and low frequency large signal (LFLS) model of the rectifier depicting 5.316% for the switching model and 4.956% for the LFLS one.

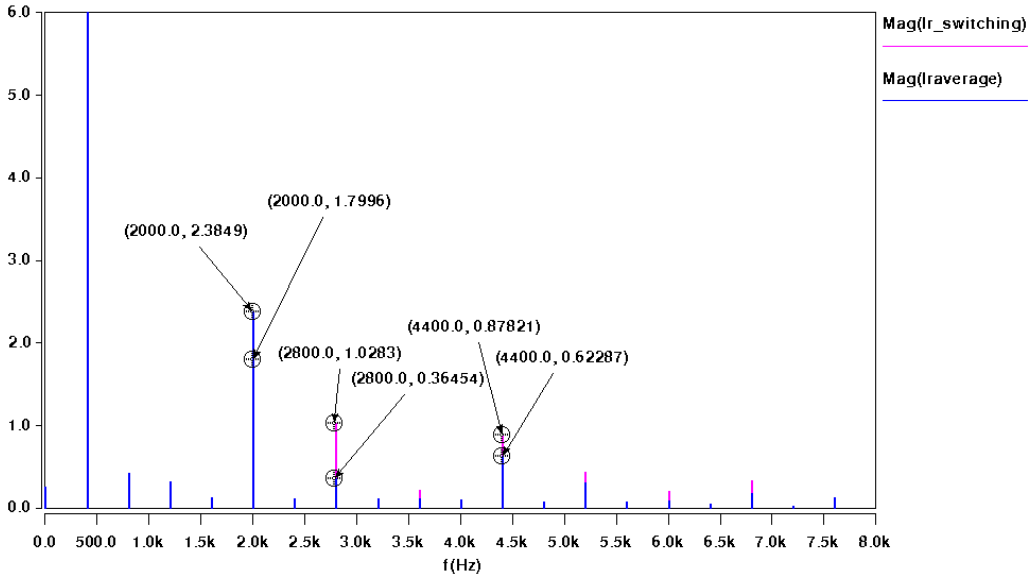


Fig. 2-28 THD comparison for low frequency large signal model and switching model phase A input current of rectifier

And Fig. 2-29 compares the time domain waveform for phase A current for the switching and low frequency large signal model with distortions but with discontinuous – right aligned SVM.

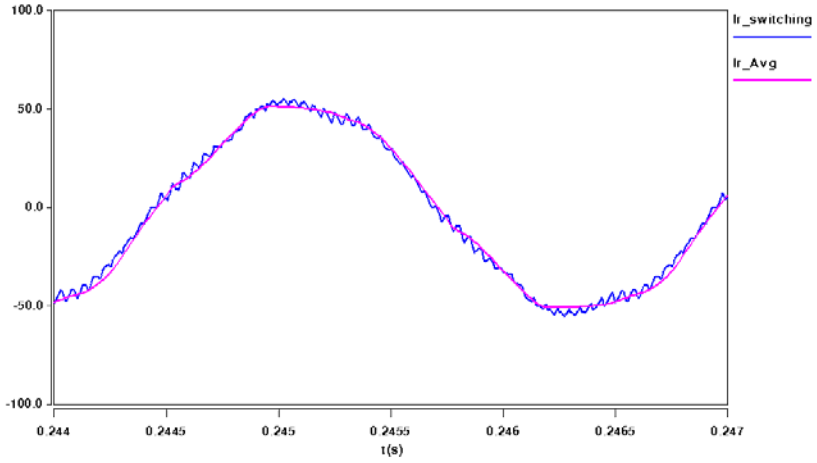


Fig. 2-29 Low frequency large signal model and switching model comparison for phase A input current of rectifier with discontinuous-RA SVM and distortions

Chapter 3 SMALL-SIGNAL MODEL OF A VOLTAGE SOURCE INVERTER (VSI) CONSIDERING THE DEAD-TIME EFFECT AND SPACE VECTOR MODULATION TYPES

3.1. Introduction

This chapter presents a modified small-signal model of a voltage source inverter (VSI) that captures model nonlinearities such as dead time and modulation effects that were not presented in the literature. Small-signal models are low-frequency approximations of the real switching model and are usually used for control and stability studies. Stability analysis is important because most power electronics converters behave as constant power loads that have negative impedance characteristics and can cause instabilities [181], [172] and [135]. For ac converters, a key breakthrough was accomplished by Belkhayat who employed the generalized Nyquist stability criterion (GNC) to assess the stability of ac interfaces in the *d-q* frame [135]-[136]. This work was used in this research along with an impedance measurement tool developed in [180] for stability assessment of the VSI. The impedances were also derived analytically using the conventional small-signal model known in literature showing a new missing damping factor in VSI in the d-q axis. This damping factor was predicted to be due to the nonlinearities of the model like the various types of modulation [72]-[73], the dead time that is inevitable to prevent the shoot-through phenomenon [89]-[91], and the inherent characteristics of the switching devices as the voltage drops, and the turn on/off time of the switches. This chapter presents a modified small-signal model that captures these model nonlinearities that were not presented in the literature. Previous research has concentrated on developing compensation methods for these types of phenomena in a switching model, but none actually derived an analytical model that can predict them. In this chapter, the small-signal model of the VSI in literature is used, and the different

phenomena are then incorporated into the model to get a complete model. In addition, the output impedance of the VSI is derived with the modified small-signal model, compared to the conventional one and validated with switching model and experimental results.

3.2. Proposed Voltage Source Inverter Average Model

Fig. 3-1 shows the circuit schematic of the voltage source inverter (VSI) model considered in this study. It is fed from a dc voltage source of 170V and feeding a RL load.

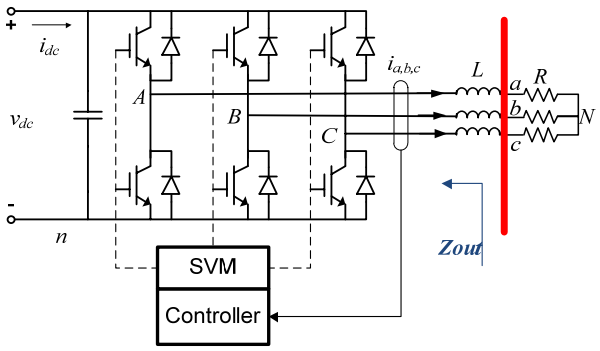


Fig. 3-1 Circuit schematic of VSI topology considered

The converter phase-leg operation has been modeled up to now by the following set of equations:

$$L\frac{di_{ph}}{dt} + i_{ph}R = v_{ph} - v_N \qquad \text{Eqn 3-1}$$

where $i_{ph}(i_a, i_b, i_c)$ and $v_{ph}(v_A, v_B, v_C)$ is the phase current and voltage respectively and $v_{ph} = s_{ph}v_{dc}$, where s_{ph} (for $ph = A, B, C$) is the state of the ac switches (s_{ph} = {+1, 0}), and v_N is represented by:

$$v_N = \frac{1}{3}(v_a + v_b + v_c) = \frac{1}{3}[1,1,1]\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{3}[1,1,1]\vec{v}_{ph} = \frac{1}{3}[1,1,1]\vec{s}_{ph}v_{dc} \qquad \text{Eqn 3-2}$$

By substituting Eqn 3-2 in Eqn 3-1, one can get the analytical representation for the switching ideal VSI in *abc*-coordinates as:

$$\frac{d\vec{i}_{ph}}{dt} = \frac{1}{L}(I - \frac{1}{3}\begin{bmatrix} 1,1,1 \\ 1,1,1 \\ 1,1,1 \end{bmatrix})\vec{s}_{ph}v_{dc} - \frac{R}{L}\vec{i}_{ph} \qquad \text{Eqn 3-3}$$

Applying the moving average operator at the switching cycle period, the average model of the VSI is obtained as:

$$\frac{d\bar{\vec{i}}_{ph}}{dt} = \frac{1}{L}(I - \frac{1}{3}\begin{bmatrix} 1,1,1 \\ 1,1,1 \\ 1,1,1 \end{bmatrix})\vec{d}_{ph}\bar{v}_{dc} - \frac{R}{L}\bar{\vec{i}}_{ph} \qquad \text{Eqn 3-4}$$

Eqn 3-4 needs to be modified so that it takes the effect of dead time into consideration. The dead time is as introduced in the previous chapter, a blanking time used to avoid the so-called shoot-through of the dc link. This time guarantees that both switches in an inverter leg never conduct simultaneously. Having the dead time effect will result in new duty ratios for each phase conducting and depend on current direction. In addition, dead time takes effect at the turn-on and turn-off of the switches therefore it will change depending on the modulation scheme. For example, when running with continuous space vector modulation (SVM), the three phases are affected, but if using discontinuous SVM, then only two of the three phases are changed. The following sections derive the small-signal model for both cases and compare them.

3.2.1. Continuous Space Vector Modulation (CSVM)

Fig. 2-10 shows the effect of dead time on phase A which is the same for phase B and C since we are using continuous SVM for this case. The effect is shown for positive current and the exact reverse occurs for negative current. Therefore, it can be represented by a duty cycle error, as shown below:

$$\vec{d}_{ph} = \vec{d}_{phREF} - \frac{T_{dead}}{T_s} sign(i_{ph}) \qquad \text{Eqn 3-5}$$

Thus the state space model in Eqn 3-4 is modified to,

$$\frac{d\vec{\vec{i}}_{ph}}{dt} = \frac{1}{L}(I - \frac{1}{3}\begin{bmatrix}1,1,1\\1,1,1\\1,1,1\end{bmatrix})\left[d_{phREF} - \frac{T_{dead}}{T_s} sign(\vec{\vec{i}}_{ph}) \right]\bar{v}_{dc} - \frac{R}{L}\vec{\vec{i}}_{ph} \qquad \text{Eqn 3-6}$$

Transforming the model into the d-q stationary frame by substituting $T^{-1}X_{dq0}$ for X_{abc}, we obtain:

$$\begin{aligned}\frac{d\bar{\bar{i}}_{dq0}}{dt} = {} & \frac{1}{L}\begin{bmatrix}1&0&0\\0&1&0\\0&0&0\end{bmatrix} d_{dq0}\bar{v}_{dc} - \frac{R}{L}\bar{i}_{dq0} - \begin{bmatrix}0&-\omega&0\\\omega&0&0\\0&0&0\end{bmatrix}\cdot\bar{\bar{i}}_{dq0} \\ & -\frac{1}{L}\frac{T_{dead}}{T_s}\sqrt{\frac{2}{3}}\begin{bmatrix}\cos\omega t & \cos(\omega t-\frac{2}{3}\pi) & \cos(\omega t+\frac{2}{3}\pi)\\ -\sin\omega t & -\sin(\omega t-\frac{2}{3}\pi) & -\sin(\omega t+\frac{2}{3}\pi)\\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}\end{bmatrix}\times\begin{bmatrix}\frac{2}{3}&\frac{-1}{3}&\frac{-1}{3}\\ \frac{-1}{3}&\frac{2}{3}&\frac{-1}{3}\\ \frac{-1}{3}&\frac{-1}{3}&\frac{2}{3}\end{bmatrix} \\ & \times sign\left(\sqrt{\frac{2}{3}}\begin{bmatrix}\cos\omega t & -\sin\omega t & \frac{1}{\sqrt{2}}\\ \cos(\omega t-\frac{2}{3}\pi) & -\sin(\omega t-\frac{2}{3}\pi) & \frac{1}{\sqrt{2}}\\ \cos(\omega t+\frac{2}{3}\pi) & -\sin(\omega t+\frac{2}{3}\pi) & \frac{1}{\sqrt{2}}\end{bmatrix}\bar{i}_{dq0}\right)\bar{v}_{dc}\end{aligned} \qquad \text{Eqn 3-7}$$

where $T^{-1} = \sqrt{\frac{2}{3}}\begin{bmatrix}\cos\omega t & -\sin\omega t & \frac{1}{\sqrt{2}}\\ \cos(\omega t-\frac{2}{3}\pi) & -\sin(\omega t-\frac{2}{3}\pi) & \frac{1}{\sqrt{2}}\\ \cos(\omega t+\frac{2}{3}\pi) & -\sin(\omega t+\frac{2}{3}\pi) & \frac{1}{\sqrt{2}}\end{bmatrix}$.

This model is observed as time-variant, and cannot be converted directly to the *d-q* frame due to the use of the *sign*( ) function; therefore, in this analysis the sign function is approximated with its fundamental as:

$$
\begin{aligned}
& sign\left(\sqrt{\frac{2}{3}}\begin{bmatrix} \cos\omega t & -\sin\omega t & \frac{1}{\sqrt{2}} \\ \cos(\omega t-\frac{2}{3}\pi) & -\sin(\omega t-\frac{2}{3}\pi) & \frac{1}{\sqrt{2}} \\ \cos(\omega t+\frac{2}{3}\pi) & -\sin(\omega t+\frac{2}{3}\pi) & \frac{1}{\sqrt{2}} \end{bmatrix}\bar{i}_{dq0}\right) \\
& = sign\left(\begin{bmatrix} \bar{i}_d\cos\omega t-\bar{i}_q\sin\omega t \\ \bar{i}_d\cos(\omega t-\frac{2}{3}\pi)-\bar{i}_q\sin(\omega t-\frac{2}{3}\pi) \\ \bar{i}_d\cos(\omega t+\frac{2}{3}\pi)-\bar{i}_q\sin(\omega t+\frac{2}{3}\pi) \end{bmatrix}\right) \\
& = sign\left(\begin{bmatrix} \cos(\omega t+\theta) \\ \cos(\omega t-\frac{2}{3}\pi+\theta) \\ \cos(\omega t+\frac{2}{3}\pi+\theta) \end{bmatrix}\right) \\
& \approx \frac{4}{\pi}\left(\begin{bmatrix} \cos(\omega t+\theta) \\ \cos(\omega t-\frac{2}{3}\pi+\theta) \\ \cos(\omega t+\frac{2}{3}\pi+\theta) \end{bmatrix}\right) where\ \sin\theta=\frac{\bar{i}_q}{\sqrt{\bar{i}_d^2+\bar{i}_q^2}}, \cos\theta=\frac{\bar{i}_d}{\sqrt{\bar{i}_d^2+\bar{i}_q^2}}
\end{aligned}
$$

Eqn 3-8

Substituting this back into Eqn 3-7, the average model in d-q frame is given as follows:

$$
\frac{d\bar{\bar{i}}_{dq0}}{dt}=\frac{1}{L}\begin{bmatrix}1&0&0\\0&1&0\\0&0&0\end{bmatrix}d_{dq0}\bar{v}_{dc}-\frac{R}{L}\bar{i}_{dq0}-\begin{bmatrix}0&-\omega&0\\\omega&0&0\\0&0&0\end{bmatrix}\cdot\bar{\bar{i}}_{dq0}-\frac{1}{L}\frac{T_{dead}}{T_s}\frac{2\sqrt{6}}{\pi}\begin{bmatrix}\frac{\bar{i}_d}{\sqrt{\bar{i}_d^2+\bar{i}_q^2}}\\ \frac{\bar{i}_q}{\sqrt{\bar{i}_d^2+\bar{i}_q^2}}\\ 0\end{bmatrix}\bar{v}_{dc}
$$

Eqn 3-9

By linearizing Eqn 3-9 around an operating point, the small-signal phase model with the dead time effect equivalent circuit is shown in Fig. 3-2. The previous derivation was as mentioned for the phase-to-neutral model of the VSI; however, the same procedure can

be followed to get the line-to-line model of the modified VSI, and the equivalent circuit is shown in Fig. 3-3.

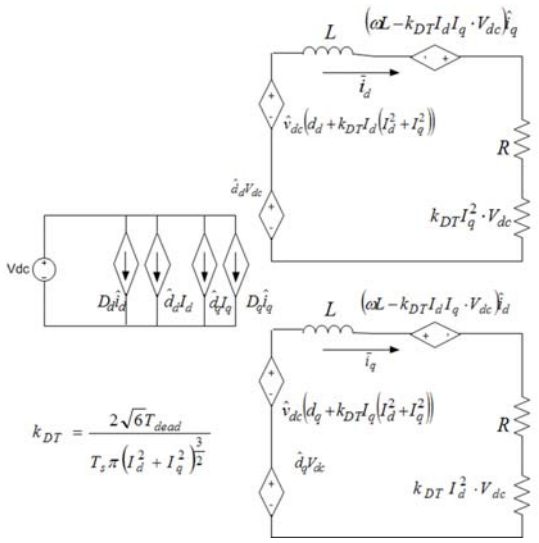


Fig. 3-2 Small-signal model with phase to neutral derivation, dead time and continuous SVM

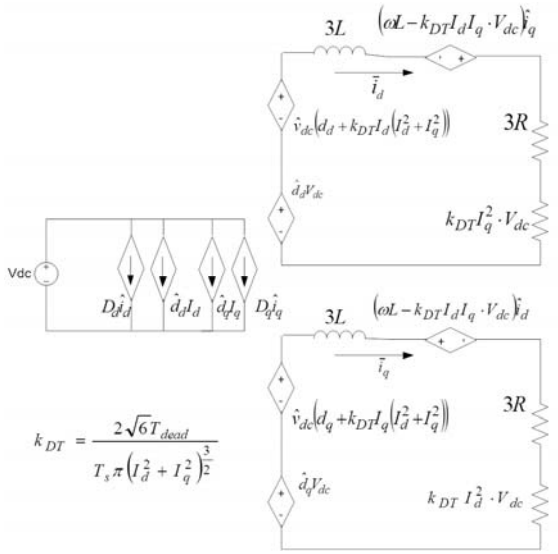


Fig. 3-3 Small-signal model with line to line derivation, dead time and continuous SVM.

3.2.2. Discontinuous Space Vector Modulation (DSVM)

For the discontinuous SVM, only two phases conduct in each sector. Fig. 2-6 shows one example of a discontinuous SVM scheme, and Fig. 3-4 shows the sector divisions with the current direction for each phase, which can be used to calculate the duty cycle error due to dead time as shown in Table 3-1.

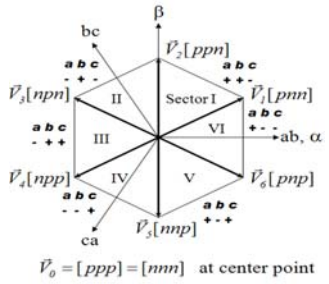


Fig. 3-4 Sectors and current directions.

Table 3-1 Duty cycle errors due to dead time in each sector

Sector Number	Duty cycle error
I	$\Delta d_a = 0, \quad \Delta d_b = -\frac{T_{dead}}{T_s} sign(i_b), \quad \Delta d_c = -\frac{T_{dead}}{T_s} sign(i_c)$
II	$\Delta d_a = -\frac{T_{dead}}{T_s} sign(i_a), \quad \Delta d_b = -\frac{T_{dead}}{T_s} sign(i_b), \quad \Delta d_c = 0$
III	$\Delta d_a = -\frac{T_{dead}}{T_s} sign(i_a), \quad \Delta d_b = 0, \quad \Delta d_c = -\frac{T_{dead}}{T_s} sign(i_c)$
IV	$\Delta d_a = 0, \Delta d_b = -\frac{T_{dead}}{T_s} sign(i_b), \Delta d_c = -\frac{T_{dead}}{T_s} sign(i_c)$
V	$\Delta d_a = -\frac{T_{dead}}{T_s} sign(i_a), \quad \Delta d_b = -\frac{T_{dead}}{T_s} sign(i_b), \quad \Delta d_c = 0$
VI	$\Delta d_a = -\frac{T_{dead}}{T_s} sign(i_a), \quad \Delta d_b = 0, \quad \Delta d_c = -\frac{T_{dead}}{T_s} sign(i_c)$

Using Table 3-1, Eqn 3-10 can represent the VSI phase-to-neutral model with the effect of dead time under discontinuous SVM:

$$\frac{d\bar{\bar{i}}_{ph}}{dt} = \frac{1}{L}\left(I - \frac{1}{3}\begin{bmatrix}1,1,1\\1,1,1\\1,1,1\end{bmatrix}\right)\left[d_{phREF} - \frac{1}{2}\cdot\frac{T_{dead}}{T_s}\left[sign\begin{pmatrix}i_a\\i_b\\i_c\end{pmatrix} - sign\begin{pmatrix}i_b\\i_c\\i_a\end{pmatrix}\right]\right]\bar{v}_{dc} - \frac{R}{L}\bar{\bar{i}}_{ph} \qquad \text{Eqn 3-10}$$

Using the same type of analysis as in the continuous SVM and approximating the sign () to its fundamental, the d-q frame model with DSVM (phase-to-neutral model) can be given as in Eqn 3-11 which when linearized gives the equivalent small-signal model in Fig. 3-5.

$$\begin{aligned}\frac{d\bar{\bar{i}}_{dq0}}{dt} &= \frac{1}{L}\begin{bmatrix}1&0&0\\0&1&0\\0&0&0\end{bmatrix}d_{dq0}\bar{v}_{dc} - \frac{R}{L}\bar{i}_{dq0}\\ &-\begin{bmatrix}0&-\omega&0\\\omega&0&0\\0&0&0\end{bmatrix}\cdot\bar{\bar{i}}_{dq0} - \frac{1}{L}\cdot\frac{T_{dead}}{T_s}\cdot\frac{3}{2\pi\sqrt{i_d^2+i_q^2}}\begin{bmatrix}\sqrt{6}i_d - \sqrt{2}i_q\\\sqrt{6}i_q + \sqrt{2}i_d\\0\end{bmatrix}\bar{v}_{dc}\end{aligned} \qquad \text{Eqn 3-11}$$

The same procedure can be followed to get the line-to-line model of the modified VSI with the effect of dead time and under discontinuous SVM. Eqn 3-12 shows the equation representing the d-q frame model:

$$\begin{aligned}\frac{d\bar{\bar{i}}_{dq0}}{dt} &= \frac{1}{3L}d_{dq0}\bar{v}_{dc} - \frac{R}{L}\bar{i}_{dq0} - \begin{bmatrix}0&-\omega&0\\\omega&0&0\\0&0&0\end{bmatrix}\cdot\bar{\bar{i}}_{dq0}\\ &-\frac{1}{3L}\frac{1}{2}\frac{4}{\pi}\sqrt{\frac{2}{3}}\begin{bmatrix}\dfrac{\bar{i}_d - \sqrt{3}\bar{i}_q}{\sqrt{\bar{i}_d^2+\bar{i}_q^2}}\\\dfrac{\bar{i}_q + \sqrt{3}\bar{i}_d}{\sqrt{\bar{i}_d^2+\bar{i}_q^2}}\\0\end{bmatrix}\bar{v}_{dc}\end{aligned} \qquad \text{Eqn 3-12}$$

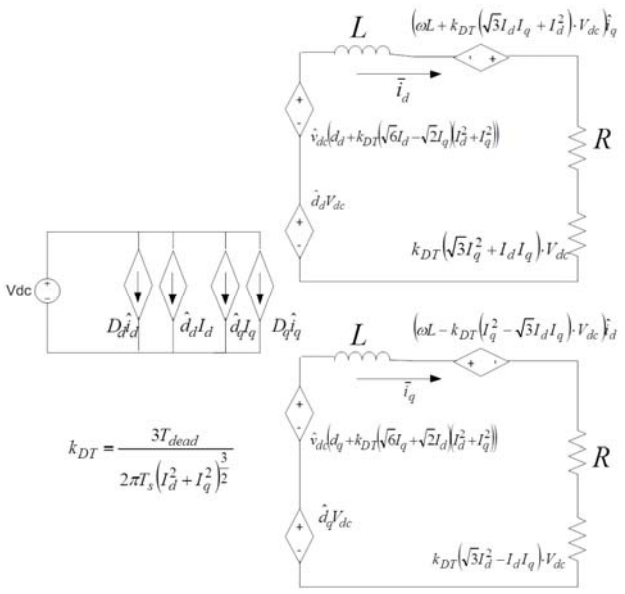


Fig. 3-5 Small-signal model phase to neutral derivation, dead time and discontinuous SVM.

3.3. Switching Model Results Comparison with Analytical Derivation

3.3.1. Open loop VSI

To verify the proposed small-signal model, the line-to-line ac output impedance of the open-loop VSI is calculated analytically in Eqn 3-13 and Eqn 3-14 for continuous and discontinuous SVM, respectively.

$$Z_{dq0}(s) = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = \begin{bmatrix} 3sL + k_{dT}\overline{V}_{dc}\bar{I}_q^2 & -3\omega L - k_{dT}\overline{V}_{dc}\bar{I}_d\bar{I}_q \\ 3\omega L - k_{dT}\overline{V}_{dc}\bar{I}_d\bar{I}_q & 3sL + k_{dT}\overline{V}_{dc}\bar{I}_d^2 \end{bmatrix} \qquad \text{Eqn 3-13}$$

$$\begin{aligned} Z_{dq0}(s) &= \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} \\ &= \begin{bmatrix} 3sL + k_{dT}\overline{V}_{dc}\left(\bar{I}_q^2 + \sqrt{3}\bar{I}_d\bar{I}_q\right) & -3\omega L - k_{dT}\overline{V}_{dc}\left(\sqrt{3}\bar{I}_d^2 + \bar{I}_d\bar{I}_q\right) \\ 3\omega L - k_{dT}\overline{V}_{dc}\left(\bar{I}_d\bar{I}_q - \sqrt{3}\bar{I}_q^2\right) & 3sL + k_{dT}\overline{V}_{dc}\left(\bar{I}_d^2 - \sqrt{3}\bar{I}_d\bar{I}_q\right) \end{bmatrix} \end{aligned} \qquad \text{Eqn 3-14}$$

These results are compared to the simulated switching model as shown in Fig. 3-6 and Fig. 3-7, showing a good matching with a small error that can be due to approximating the sign () with its fundamental sine and also due to the losses across the switches and diodes. The results are also compared to the conventional small-signal model which doesn't consider the effect of dead time or modulation. The conventional small-signal model displays the characteristic of only the filter inductor in d-q frame. However, in the switching model and the proposed small-signal model, we can see the impedance Z_{qq} has a significant magnitude increase at low frequency and is more resistive. Z_{dd} also becomes resistive at low frequency, but much less than Z_{qq} does.

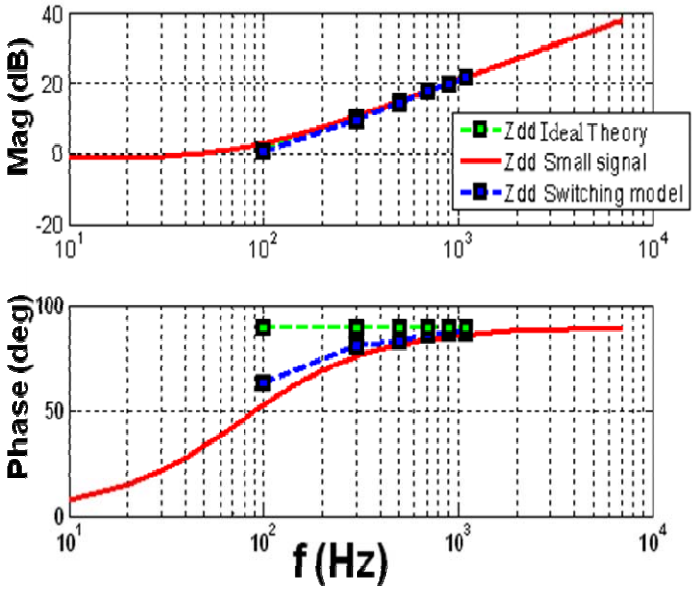


Fig. 3-6 Output impedance of the VSI for the d-d channel.

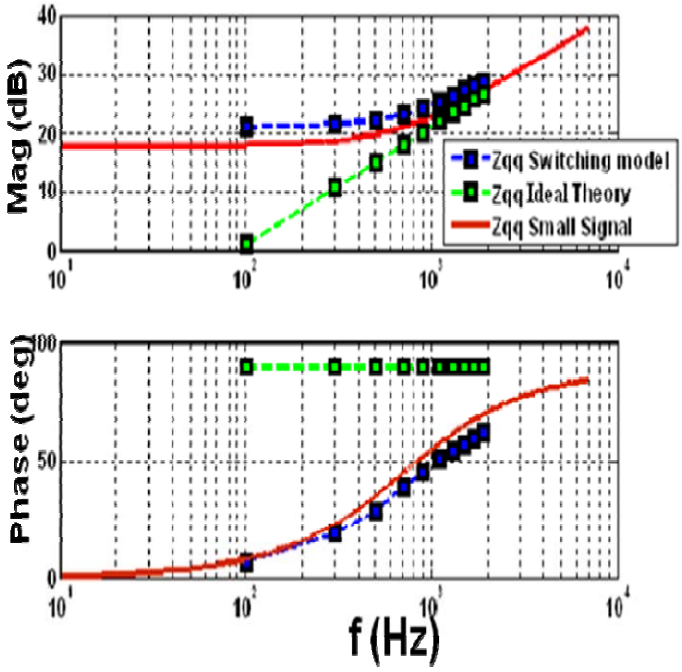


Fig. 3-7 Output impedance of the VSI for the q-q channel.

Impedance Extraction Technique

Several techniques are developed to measure the system impedances in d-q coordinates [165]. The main idea is to inject a perturbation into the system and measure the voltage and current response at the interface where the impedance is interesting. Then the response data is post processed to extract the impedance at the interface. For this research, the impedances are extracted from the simulation using the injection of shunt current disturbances technique [182]. A sinusoidal perturbation current reference is generated in d-q frame and then transferred into abc frame. The current reference is passed to power amplifiers which inject current into the system between source and load. The system voltage and both source and load sides currents waveform are recorded then transferred into d-q frame. The same frequency as the perturbation reference are filtered out and used to calculate system impedance at the perturbation frequency point. A frequency sweep is used to get the impedance curve. The impedances at the injection frequency are calculated by Eqn. 3-15 using the response data.

$$Z_s\left(j\omega_{inj}\right)=\begin{bmatrix} Z_{sdd}\left(j\omega_{inj}\right) & Z_{sdq}\left(j\omega_{inj}\right) \\ Z_{sqd}\left(j\omega_{inj}\right) & Z_{sqq}\left(j\omega_{inj}\right) \end{bmatrix}=\begin{bmatrix} v_{d1}\left(j\omega_{inj}\right) & v_{d2}\left(j\omega_{inj}\right) \\ v_{q1}\left(j\omega_{inj}\right) & v_{q2}\left(j\omega_{inj}\right) \end{bmatrix}\begin{bmatrix} i_{sd1}\left(j\omega_{inj}\right) & i_{sd2}\left(j\omega_{inj}\right) \\ i_{sq1}\left(j\omega_{inj}\right) & i_{sq2}\left(j\omega_{inj}\right) \end{bmatrix}^{-1} \quad \text{Eqn 3-15}$$

3.4. Experimental Results

3.4.1. Setup

The same 2 kW prototype experiment used for the low frequency large signal model validation is conducted here to verify the performance of the new developed model. Fig. 2-21 shows the construction. A 6-pack IGBT IPMs from Fuji (6MBP20RH060) (600V, 20A) is used. The output inductance per phase is 600μH. The control board is DSP-FPGA digital controller. The impedance analyzer is injected in-between the source and load (between output inductance of the source and the resistive load) and used to measure the output impedance of the source and the input impedance of the load.

3.4.2. Validation

Fig. 3-8 shows the effect of dead time on the output impedance on the d and q channels. The dead time is changed from 1µs to 5µs with the same modulation scheme (DSVM for this case), and the results show an increase in the q channel, as seen in the simulation results. For this case, the converter I_q is equal to zero which means converter is aligned to d-axis and therefore, we only see the damping effect on the Z_{qq} axis. However, this is not true if the dq frame is aligned differently. Fig. 3-9 shows the effect of modulation scheme by comparing the d and q channel output impedances with 5µs dead time; once with CSVM and other with DSVM. The results show the q-q channel to have nearly the same impedance in both modulation cases however, the d-d impedance is lower for the DSVM. This result is because of the lower switching losses in the DSVM due to being only four commutations instead of six in the CSVM case as explained in the previous chapter.

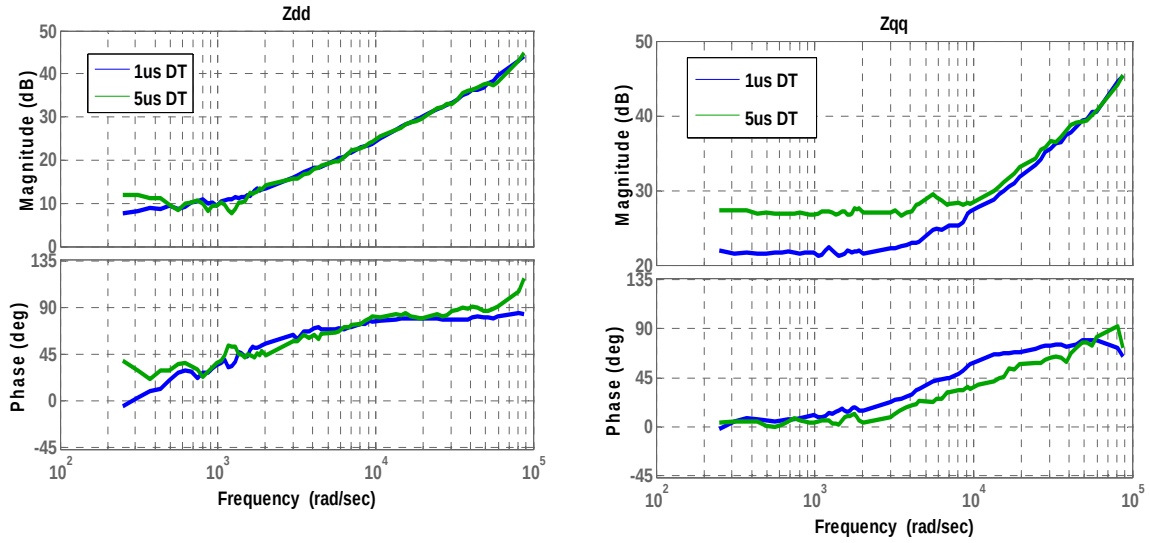


Fig. 3-8 Effect of dead time on the output impedance of the VSI for the DSVM case (with 1us and 5us) on d-d (left) and q-q channel (right).

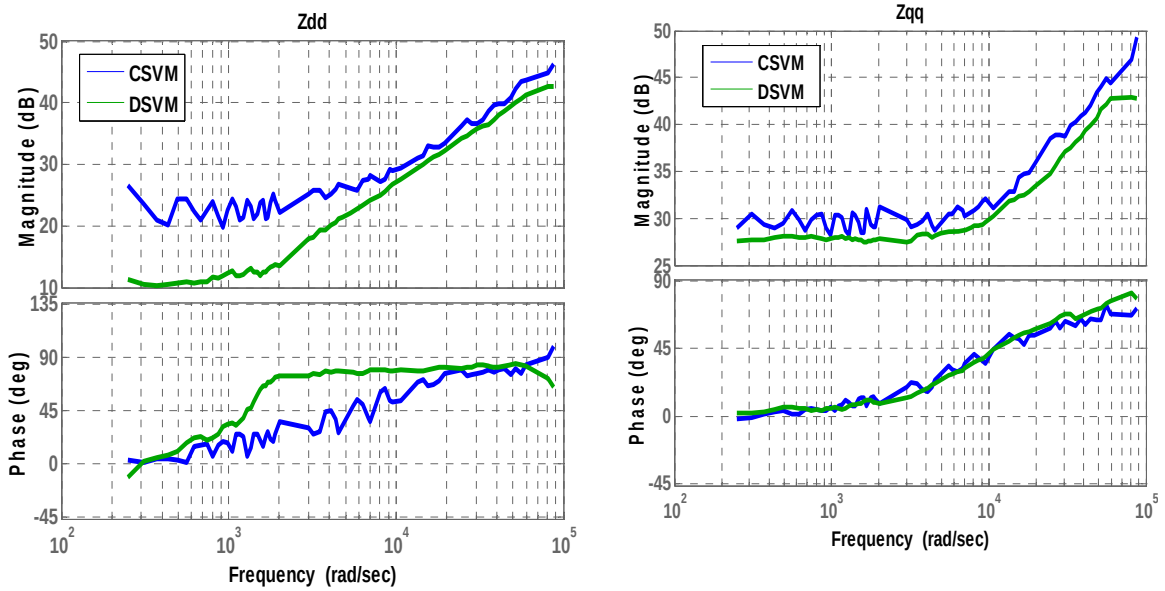


Fig. 3-9 Effect of modulation scheme on the output impedance of VSI.

Fig. 3-10 compares the results of the experimental measurement versus the analytical small-signal model derived in this chapter and the low frequency large signal model introduced in this work for the discontinuous space vector modulation (DSVM) type. It can be seen that the error is in-between 2,3 dB and 6 degrees which is within the accuracy measure of the equipment used to measure the impedance. As known the impedance in

the dq frame will differ based on the alignment of the axes. It can be seen from the results and the small-signal model derivation that when I_q is zero which means the system is aligned with the d-axis, there will be no damping on the d-axis and the impedance Z_{dd} for this case will be just the inductor and any resistive damping will come from the losses. The small-signal model derived doesn't include the losses and therefore it shouldn't predict any damping in the d-axis in this case. However, if I_q is not equal to zero which means the d and q axes are aligned differently, this will result in some reactive power and its effect will be seen on all four impedances. For the results in Fig. 3-10 and Fig. 3-11, there is some I_q current and converter d-axis is aligned to the line to line voltage (V_{ab}), therefore there is damping seen on both axes as predicted by the derived small-signal model.

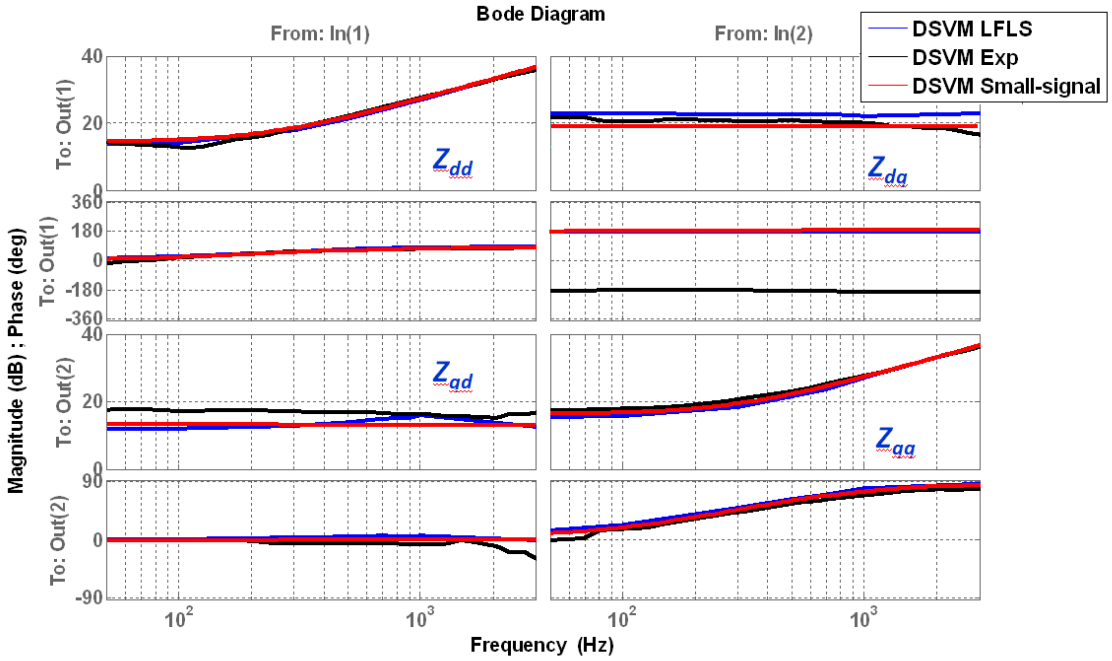


Fig. 3-10 Output impedance of the VSI for the DSVM case comparison between LFLS model, analytical small-signal and experimental result.

Fig. 3-11 again compares the results of the experimental measurement versus the analytical small-signal model derived in this chapter and the low frequency large signal model introduced in this work but for the CSVM case.

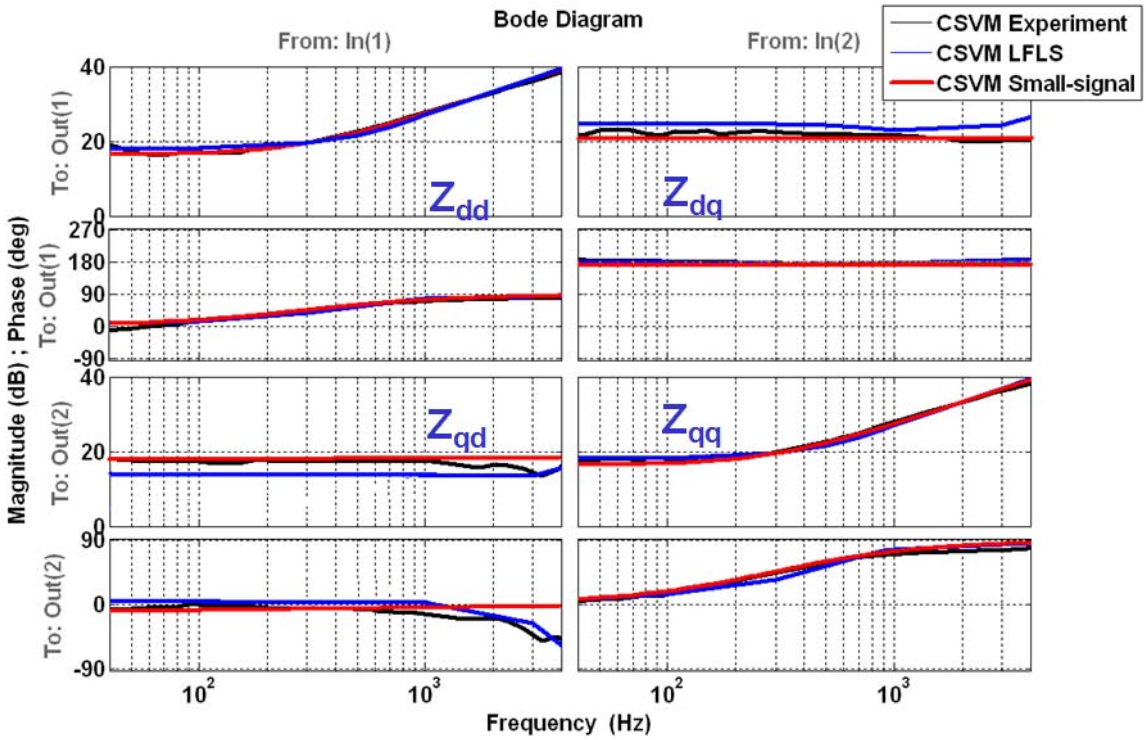


Fig. 3-11 Output impedance of the VSI for the CSVM case comparison between LFLS model, analytical small-signal and experimental result.

3.4.3. Effect of controller

The previous section discussed the effect of the dead time and modulation type on the open-loop VSI. However, it is important to see how these phenomena will influence the inverter when a controller is added. This section shows the influence of these phenomena on the inverter with current and voltage regulators added to the prototype. Fig. 3-12 and Fig. 3-13 show the experimental measurement results for the output impedance of the voltage source inverter with current regulator and with both current and voltage regulators respectively. The dead time is changed from 1μs to 3μs to see its influence on

the impedance measurement. The result shows the effect of dead time can still be seen as in the open loop case in the increase of the Z_{qq} impedance and since for this case, the Iq is not zero (not unity power factor), the effect of dead time can also be seen on the Z_{dd} axes. However, in Fig. 3-13 when the voltage regulator is added, the influence of the dead time is decreased dramatically. There is a much smaller change in the impedance than the previous two cases. This can be explained as the dead time causes an output voltage error so when voltage regulator is added, this can help in removing the effect of dead time.

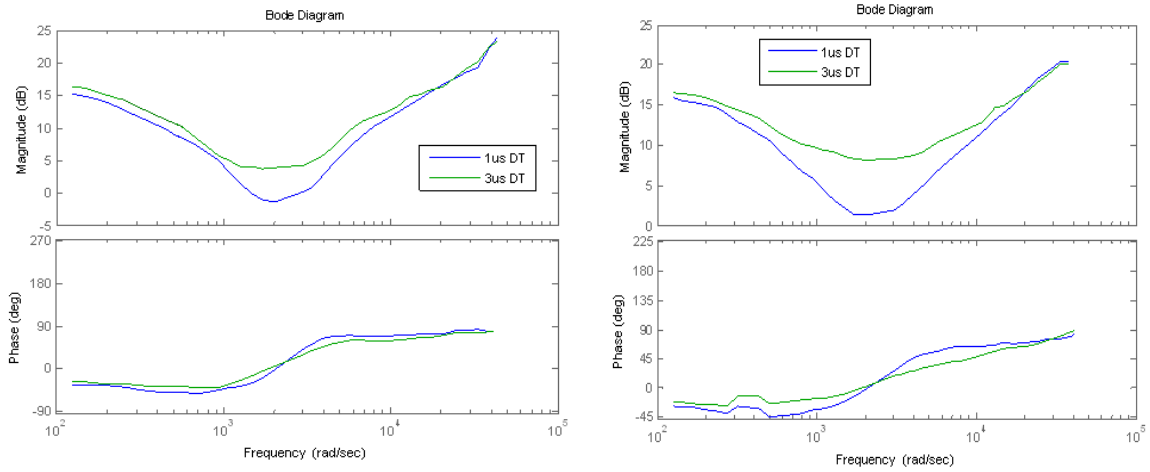


Fig. 3-12 Measured experimental output impedance of the VSI converter with current regulators and different dead times (Z_{dd} left and Z_{qq} right).

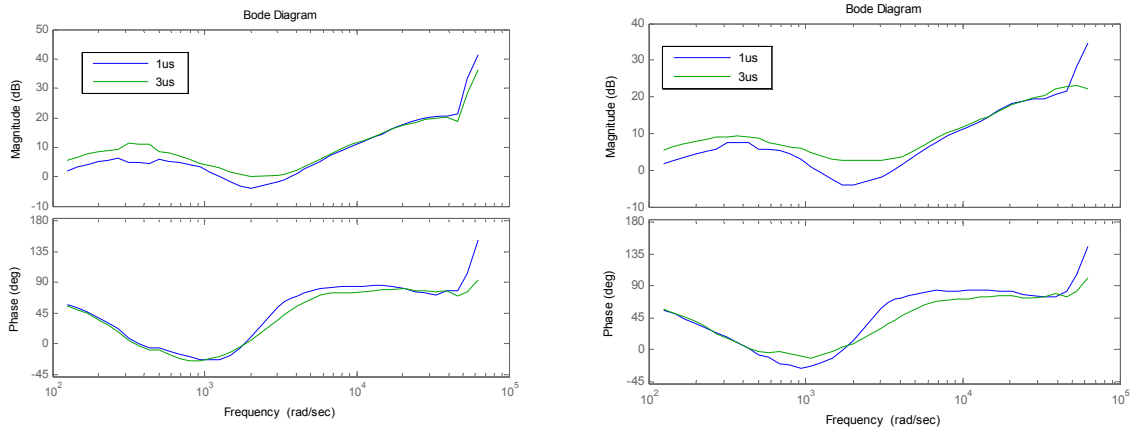


Fig. 3-13 Measured experimental output impedance of the VSI converter with both current and voltage regulators and different dead times(Z_{dd} left and Z_{qq} right).

3.5. Conclusions

This chapter has presented a new small-signal model for voltage source inverters that considers the effect of the dead time and the modulation scheme. It presented a time-invariant model that could be easily converted into the synchronous *d-q* frame and used for control and stability analysis. The model is compared to a detailed switching model and to a 2kW experimental prototype.

Chapter 4 MODELING VERIFICATION, VALIDATION, AND UNCERTAINTY QUANTIFICATION FOR A TWO-LEVEL THREE-PHASE BOOST RECTIFIER

4.1. Introduction

VV&UQ are a formal set of procedures for assessing the predictive capability of models in the computational sciences and engineering [183]. Verification assesses the mathematical accuracy of a numerical solution to a given set of governing equations and generally addresses sources of numerical error such as coding mistakes, round-off error, and discretization error. Validation addresses the physical adequacy of the underlying governing equations to describe the phenomenon of interest and must incorporate comparisons to real-world observations (i.e., experimental data). Uncertainty quantification estimates the effects of uncertainties in the system components (e.g., resistors, capacitors, inductors) and the system environment on the System Response Quantities (SRQs, i.e., the system behavior one would like to predict).

The VV&UQ process thus provides a prediction of the SRQ along with an estimate of the uncertainty in that prediction. At this point, an assessment can be made as to whether or not the model is adequate for the intended use. When models are found to be inadequate for the intended use, the VV&UQ process provides guidance as to how the model prediction can be improved. For example, if the largest uncertainties are found in the experimental data, then additional (possibly more sophisticated) experiments should be conducted; however, if the largest uncertainties occur due to inherent uncertainties in the system components or environment, then more stringent restrictions may be required (e.g., specifying that all inductors used in the component meet tighter uncertainty tolerances).

An overview of the VV&UQ process is presented in Fig. 4-1 . This figure shows the definition of the system of interest and the prioritization of the VV&UQ activities (steps 1 and 2), the verification process (steps 3 and 5), the validation process (steps 4 and 6),

and the uncertainty quantification process (step 7). It concludes with a decision on the adequacy of model for the given application and documentation (steps 8 and 9). The goal of this chapter is to apply this VV&UQ procedure to a number of different applications for a boost rectifier. A brief discussion of these various steps follows.

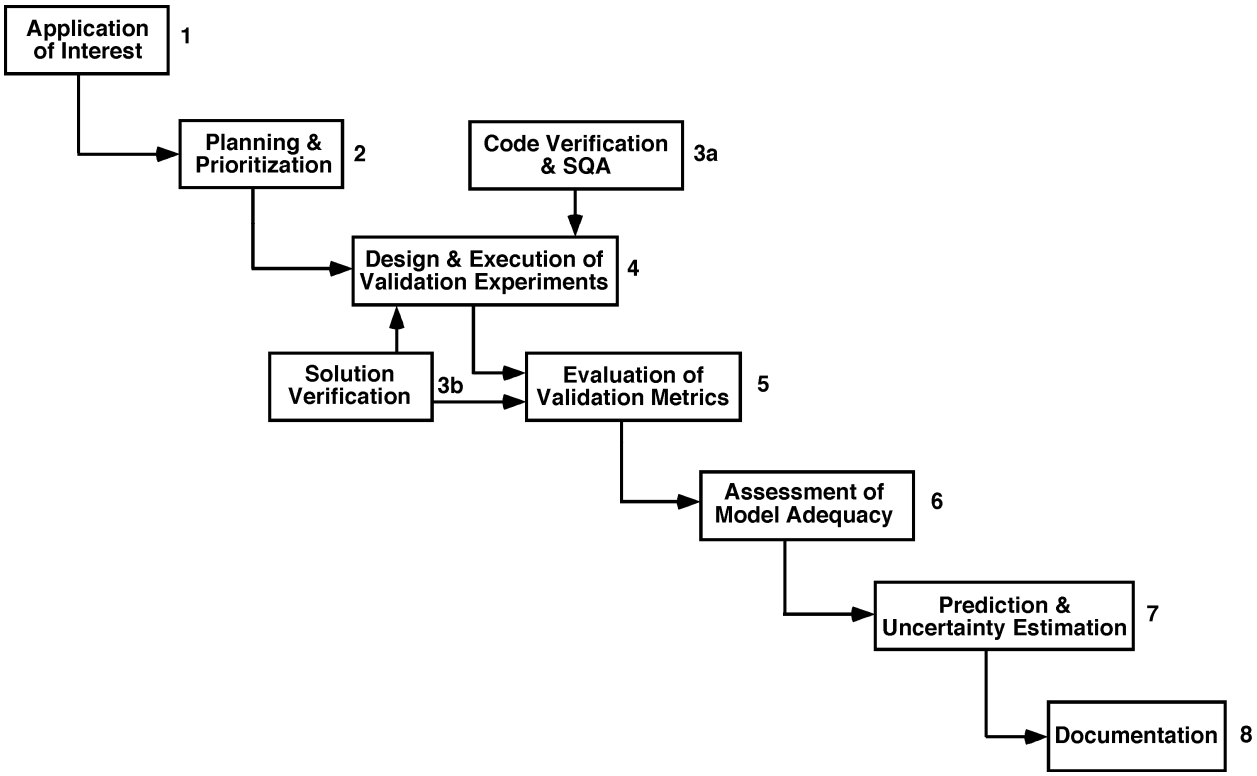


Fig. 4-1 Integrated view of the VV&UQ elements (adapted from [184]).

Fig. 4-2 shows the relationship between validation, calibration and prediction. Calibration is the process of adjusting numerical or physical modeling parameters in the computational model for the purpose of improving agreement with real-world data. It is also known as: parameter estimation, model tuning or model updating. Calibration is commonly conducted before validation activities. Prediction refers to a simulation result for a specific case of interest that is different from cases that have been validated. Therefore, computationally replicating a point in the validation database is not a prediction. Validation should be viewed as a reproducible evidence of measurable

agreement between computational and experimental results. Validation doesn't directly make a claim about the accuracy of a prediction.

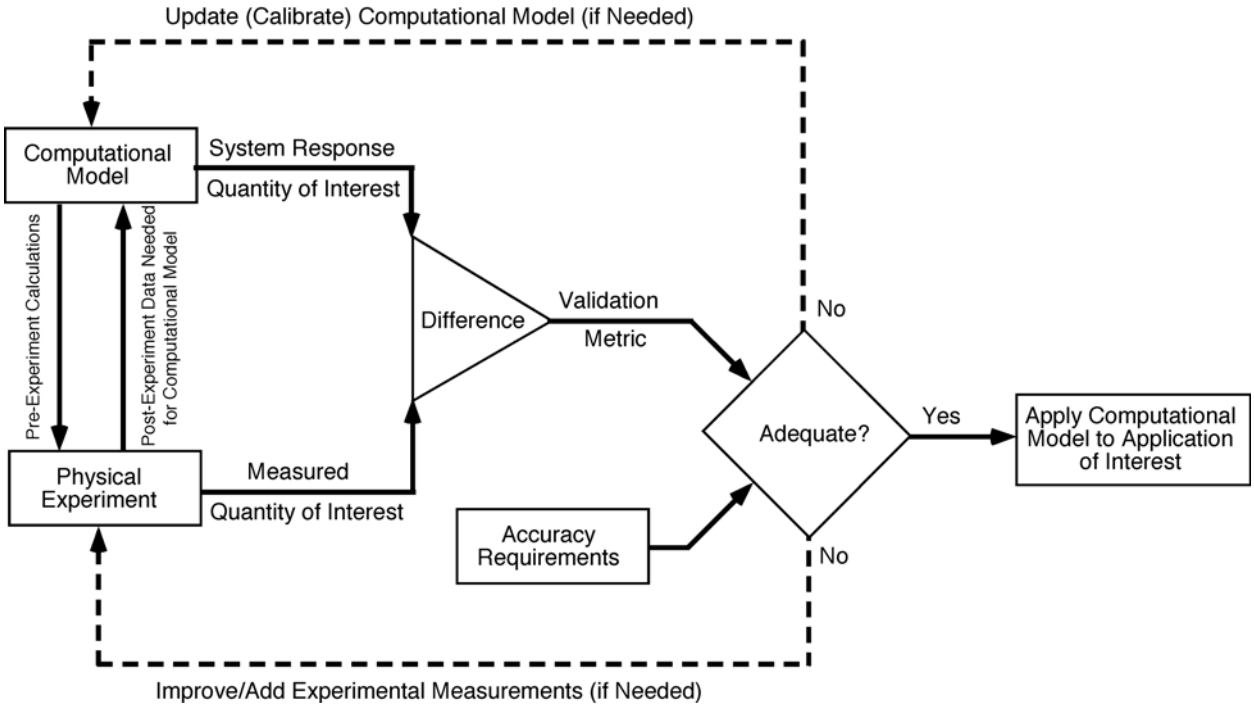


Fig. 4-2 Relationship between validation, calibration and prediction (adapted from [184]).

This chapter discusses applying rigorous Verification, Validation, and Uncertainty Quantification (VV&UQ) procedures to the modeling of a 2 kW two-level three-phase boost rectifier shown in Fig. 4-3 operating under normal environment conditions; specifically, 57.5 V ac, line frequency of 400 Hz, and ambient temperature of 25 °C. Different system response quantities (SRQs) shall be predicted under these conditions, namely the input current RMS value and THD (total harmonic distortion), the dc link voltage average value and ripple, and the converter input and output impedances, Z_{dqin} and Z_{dcout} respectively. The expected outcome is the improvement of the modeling procedure for power electronics systems, and the full assessment of the boost rectifier model predictive capabilities.

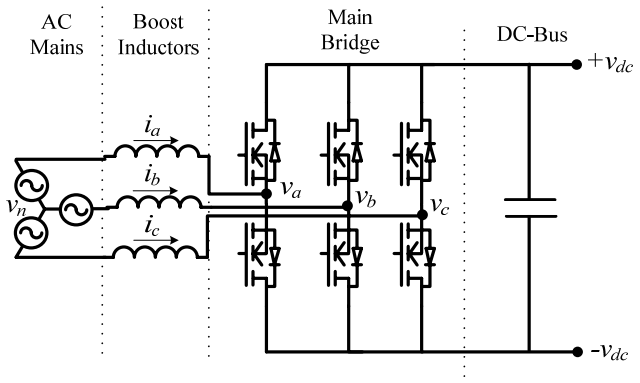


Fig. 4-3 Circuit schematic of the two-level boost rectifier under consideration.

4.2. General Approach

4.2.1. Modeling and Simulation Approach

For the physical modeling of the boost rectifier (see Fig. 4-3), three types of models are used: an ideal average model, a nonlinear average model developed in this work (the so-called low frequency large signal model) and the switching model which is a more detailed one. The circuit simulator Saber from Synopsys is used for model implementation.

4.2.2. Planning and Prioritization

One of the key issues in conducting the VV&UQ effort is how to prioritize the activities for a given application. One approach for establishing priorities is the Phenomenon Identification and Ranking Tables (PIRT) which is frequently used in the nuclear power generation industry. To generate a PIRT one must first establish the system of interest, the environment of interest, the various scenarios that could be encountered, the SRQs that one wishes to predict with the simulation tool, and the different physical phenomena that must be simulated (see Fig. 4-4). For our example, we will take the boost rectifier as the system, normal operating conditions as the environment, and scenarios of interest will be operating at normal and abnormal steady state conditions,

and operating under normal and abnormal transient conditions. For a given scenario, one then constructs a table with SRQs as the columns and pertinent physical phenomena as the rows.

Table 4-1 and Table 4-2 shows the PIRT tables for the normal steady state and transient scenarios defined above. The tables has different SRQs defined like THD (total input current harmonic distortion), V ripple (the dc bus voltage ripple), V average (the dc bus average voltage), and the converter input and output impedances, Z_{dqin} and Z_{dcout} respectively and the physical phenomena that would have to be simulated, namely the steady state voltages and currents, the small-signal transfer functions, and time domain transients. As observed, in each case, a ranking is assigned depending on how important each physical phenomenon is to the prediction of each SRQ. When viewed as a whole, these PIRTs provide guidance as to which physical phenomena are the most important in predicting the system behavior in the scenario of interest; however, they do not address the adequacy of the simulation code.

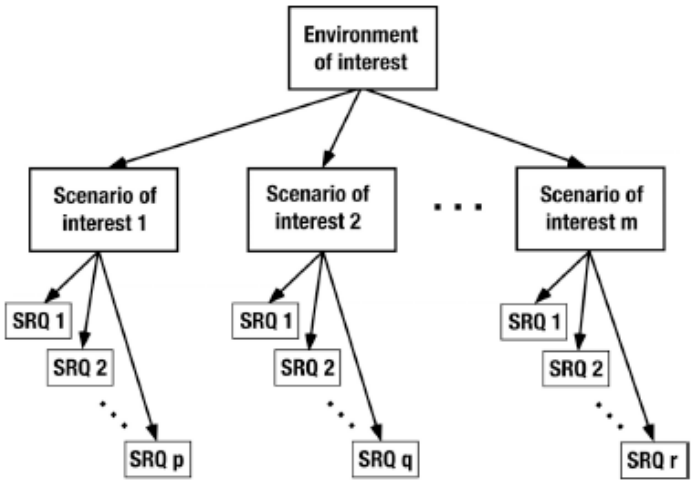


Fig. 4-4 Diagram showing the relationship between system environments, system scenarios, and system response quantities (SRQs) (from [183]).

Table 4-1 Phenomenon Identification and Ranking Table (PIRT) for the Boost Rectifier in a Normal Steady State Operating Environment

Physical Phenomenon	SRQ 1: THD of input current	SRQ 2: Spectrum of individual harmonics (Input current)	SRQ 3: Input current rms value	SRQ 4: Vdc (dc link average value)	SRQ 5: Vdc (pk-pk ripple)	SRQ 6: Spectrum of individual harmonics (Vdc)	SRQ 7: Zo	SRQ8: Zin	SRQ 9: Measure EMI standard	SRQ 10: Converter total weight
Steady state voltages and currents										
Small-signal transfer function										
Time domain transients										
EMI										
Weight estimation										

High Importance

Moderate Importance

Low Importance

Table 4-2 Phenomenon Identification and Ranking Table (PIRT) for the boost rectifier in a normal transient operating environment.

Physical Phenomenon	SRQ 1: Dc link voltage time domain	SRQ 2: Input current time domain
Steady state voltages and currents		
Small-signal transfer functions		
Time domain transients		
EMI		
Weight estimation		

High Importance

Moderate Importance

Low Importance

Once the physical phenomena have been ranked according to their importance to a given SRQ, a gap analysis is used to determine the VV&UQ status of the computational simulation code for each of the physical phenomena. Only the highest one or two levels of importance from the PIRT are used to generate a gap analysis table for a given SRQ for each computational simulation code to be used. For example, the gap analysis tables for the most important SRQ's are shown in Table 4-3 till 0. The gap analysis for the boost rectifier is done using three different models: a) the switching model, b) the ideal average model and c) the low frequency large signal (LFLS) model. Table 4-3 depicts the gap analysis for the total input current harmonic distortion (THD) SRQ 1 and the spectrum of individual harmonics (of input current) SRQ 2 respectively. Note that the ideal average model does not contain the proper physics to predict the harmonic currents, while all

models require additional validation assessments. This simple example provides an indication of how the process can be used to prioritize the VV&UQ efforts.

Table 4-3 Gap Analysis Applied to the Total Input Current Harmonic Distortion (THD) SRQ 1and to the Spectrum of Individual Harmonics (of input current) SRQ 2 for the Boost Rectifier in a normal steady state operating environment.

a) Switching Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Steady state voltages and currents				

b) Ideal Average Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Steady state voltages and currents				

c) Low Frequency Large Signal (LFLS) Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Steady state voltages and currents				

Inadequate
Unknown
Adequate

Table 4-4 shows the gap analysis for the dc link voltage average value SRQ 4 and the dc link pk-pk ripple SRQ 5 respectively. The three models compared are able to predict both SRQ's using the physics known but require additional validation assessments.

Table 4-4 Gap Analysis Applied to the Dc Link Voltage Average Value SRQ 4 and the Dc Link Pk-pk Ripple SRQ 5 for the Boost Rectifier in a Normal Steady State Operating Environment.

a) Switching Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Steady state voltages and currents				

b) Ideal Average Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Steady state voltages and currents				

c) Low Frequency Large Signal (LFLS) Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Steady state voltages and currents				

Inadequate
Unknown
Adequate

Table 4-5 and Table 4-6 show the gap analysis applied to the final important SRQ's, the output and input impedance SRQ 7 and 8 respectively. For this case of the boost rectifier, the output impedance is just a dc impedance, obtained using the tdsa block in Saber and therefore the code verification is unknown because we are not familiar with the inside of the block. However, the input impedance for this case is the ac impedance which is represented by the matrix of four impedances and is obtained using a developed method. For that, the code verification for this case is adequate.

Table 4-5 Gap Analysis Applied to the Output Impedance (Z_o) SRQ 7 for the Boost Rectifier in a Normal Steady State Operating Environment.

a) Switching Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Small-signal transfer function				

d) Ideal Average Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Small-signal transfer function				

e) Low Frequency Large Signal (LFLS) Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Small-signal transfer function				

Inadequate
Unknown
Adequate

Table 4-6 Gap Analysis Applied to the Input Impedance (Z_{in}) SRQ 8 for the Boost Rectifier in a Normal Steady State Operating Environment.

a) Switching Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Small-signal transfer function				

f) Ideal Average Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Small-signal transfer function				

g) Low Frequency Large Signal (LFLS) Model

Physical Phenomenon	Physics Modeling (Switching Model)	Code Verification	Model Validation	Uncertainty Quantification
Small-signal transfer function				

Inadequate
Unknown
Adequate

4.2.3. Code and Solution Verification

Verification addresses the mathematical accuracy of a given simulation relative to the exact solution to the model, which is generally unknown. It is decomposed into two distinct areas: code verification—ensuring that there are no mistakes (bugs) in the computer code or inconsistencies in the numerical algorithm, and solution verification—assessing the numerical errors that occur in every computational simulation. Since the commercial simulation code SABER is used in this work, only limited code

verification efforts can be conducted. The MAST language of SABER is used for most of the model coding and is assumed to be similar for all models studied. For simulation of power electronics systems, the two types of numerical errors that must be estimated are roundoff errors—the errors due to the fact that only a finite number of significant figures can be stored in memory, and discretization errors due to the replacement of temporal derivatives with finite difference or finite element approximations. In this proposed work, these numerical errors are considered small relative to the other sources of uncertainty in the system.

However, the verification process will be addressed in a different manner for this study. The author considered the switching model as the benchmark so it's a verified and a validated model and then the verification process can be applied to the low frequency large signal model (LFLS) against the per cycle averaged switching model. Fig. 4-5 compares the input current for phase A for both switching and low frequency large signal model for one line period. The left figure compares both models with a 1μs dead time and the right figure with a 4μs dead time. It can be seen that the LFLS model is capable of predicting the harmonics distortion due to the dead time effect. The deviation percentage between both waveforms is called based on the accuracy measure defined in Eqn. 2.7. As mentioned previously this accuracy measure calculates the difference between both models based on a point by point comparison and defines the error for one line cycle. For this case in Fig. 4-5, the deviation between the switching and LFLS model is calculated as $\sigma = 0.02$ for the 1μs dead time curve and $\sigma = 0.045$ for the 4μs dead time curve.

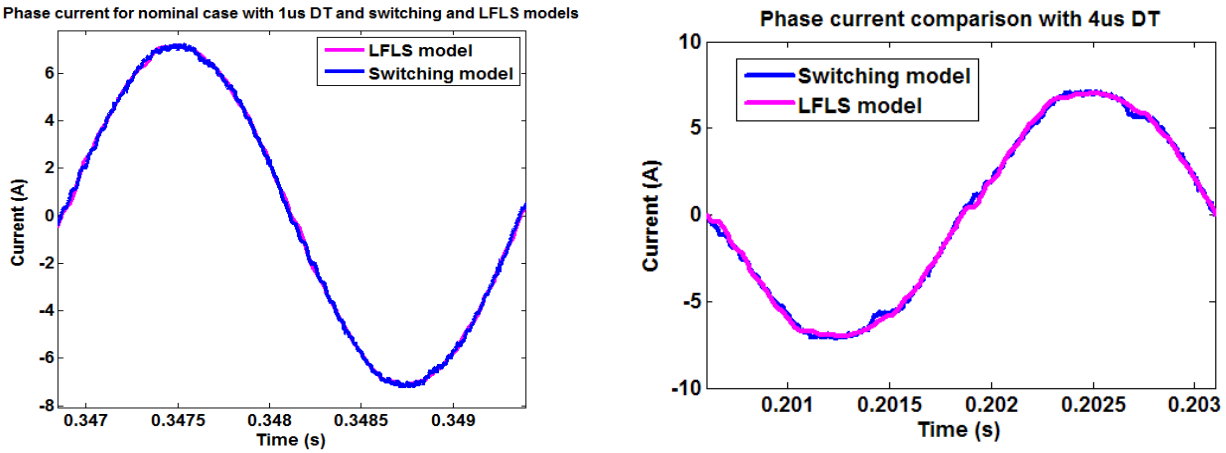


Fig. 4-5 Comparison between the switching and LFLS model input phase current for nominal case

4.2.4. Model Validation

Model validation entails a quantitative comparison between the simulation predictions and experimental data. Ideally, the experimental data will come directly from an experiment conducted for the purpose of validating the model, i.e., a validation experiment. Validation experiments can be conducted at varying levels of system complexity as shown in Fig. 4-6. At the complete system level, the actual working system is employed; however, due to the complexity of the system only a few SRQs can be measured and the uncertainties in these measurements are not well characterized. In addition, complete system level experiments often do not provide accurate measurements of the system environment which are needed to run the simulations. Conversely, unit problems are relatively simple problems involving a single physical phenomenon in which both the SRQs and the system environment can be extremely well characterized. Once the validation data has been obtained, simulations should be conducted in such a manner that only the inputs to the model are known, thus allowing the SRQs to be true predictions (i.e., a blind comparison) as shown in the validation chart in Fig. 4-7. The ultimate goal of the model validation step is to estimate the uncertainty due to the choice of the model, or the model form uncertainty.

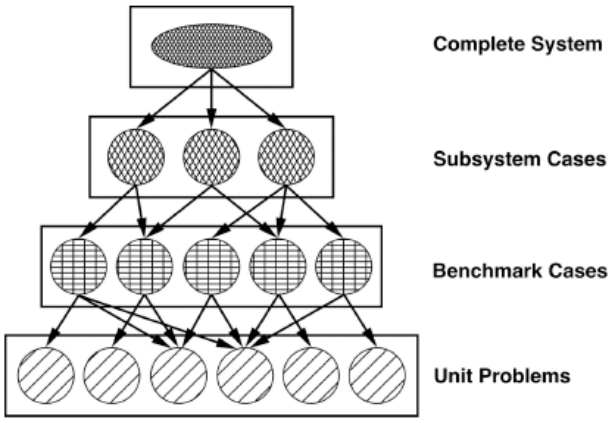


Fig. 4-6 Schematic of the validation hierarchy (from [185]).

Since the boost rectifier is actually a component of the full aircraft electrical power system, experiments using the boost rectifier can be considered to be at the subsystem level. Accordingly, the validation experiments planned in support of the boost rectifier will occur at the subsystem, benchmark, and unit problem levels. The selection of these experiments is guided by the planning and prioritization work discussed earlier. As a way to illustrate this process, the following discussion presents the prospective tests to be conducted with the boost rectifier.

Subsystem level: at this level the boost rectifier is treated as a standalone unit, with access to its input and output terminals only. The tests that can be conducted are thus limited, yet fully characterize the impact of the converter at the system level. A prospective list of tests is:

- Total input current harmonic distortion (THD)
- Input current harmonic spectrum
- Regulation under unbalanced voltage supply
- Synchronous d-q frame input impedance
- Dc voltage peak-to-peak ripple
- Dc voltage harmonic spectrum
- Output impedance

- Dc voltage and current regulation under voltage supply changes
- Dc voltage and current regulation under line frequency changes

Benchmark level: at this level the boost rectifier can be analyzed in terms of its subsystems allowing for a more complete and easier characterization of its operation. The tests in consequence can be set up using better instrumentation taking advantage of a better accessibility. A prospective list of subsystems and their corresponding tests is:

- Input filter: conducted differential- and common-mode noise, coupling between the differential- and common-mode paths, insertion impedance, temperature rise, etc.
- Power stage: input current THD and harmonic spectrum, bare differential- and common-mode noise measurement, current unbalance under unbalance supply conditions, dc voltage regulation, output impedance, synchronous frame input impedance, etc.

Unit problem level: This is the piece-wise level where detailed measurements and experiments with complete instrumentation are possible in order to model the different unit-components of the boost rectifier. A prospective list of units and their corresponding tests is:

- Inductors: measurement of equivalent series resistances (ESR), measurement of parasitic inter-winding capacitances, measurement and quantification of parameter variation under different operating temperature, etc.
- Capacitors: measurement of capacitance, measurement of ESR, measurement of leakage currents, measurements of equivalent series inductance (ESL), measurement and quantification of parameter variation under different operating temperature, etc.
- Power stage: measurement and characterization of the converter printed circuit board (PCB) under double-pulse test conditions, determining per converter

phase-leg the turn-on and turn-off times of the active switches (MOSFETs), current overshoot and ringing and voltage overshoot and ringing during turn-on and turn-off commutations, measurement of parasitic inductance, capacitance and resistance of the converter PCB, measurement and characterization of the parasitic capacitances of the semiconductor devices, measurement of the parasitic inductance of semiconductor packages (TO-220), etc.

- Gate drive: measurement of voltage and current transients of the gate-source loop of the gate drive in case physics-based semiconductors models are used instead of ideal switches to model the boost rectifier.
- Control system: characterization and measurement of current sensors and corresponding analog-to-digital (A/D) converters, characterization and measurement of voltage sensors and corresponding analog-to-digital (A/D) converters, measurement of the digital delay introduced by the digital control system, etc.

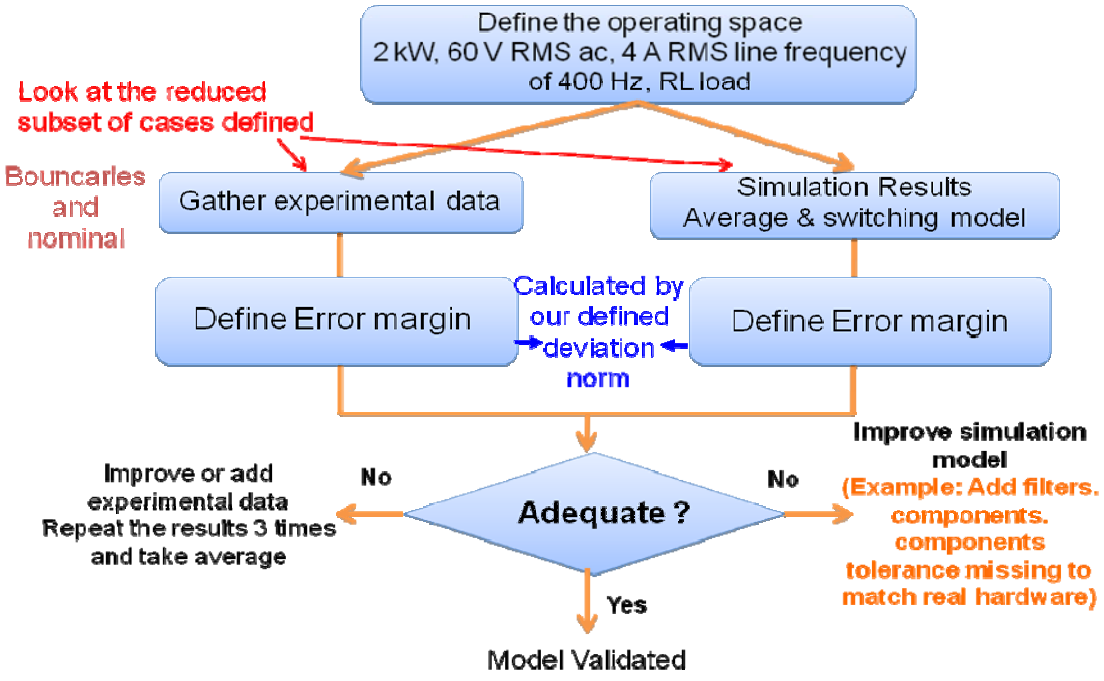


Fig. 4-7 Validation Flow Chart

Uncertainty Quantification

In addition to the uncertainties associated with the different physical parameters of a power converter—the tolerance of components expressed in percentages, there are also uncertainties associated with the measurements, the model structure, and numerical errors. There are additionally inherent uncertainties of the system that must be taken into consideration, for instance, the frequency of the electrical network, its voltage regulation range, its level of unbalance between phases, of dc offset, the load demand (active power consumption), the ambient temperature, etc. The effects of all these uncertainties on the SRQs are generally estimated by propagating them through the simulation model.

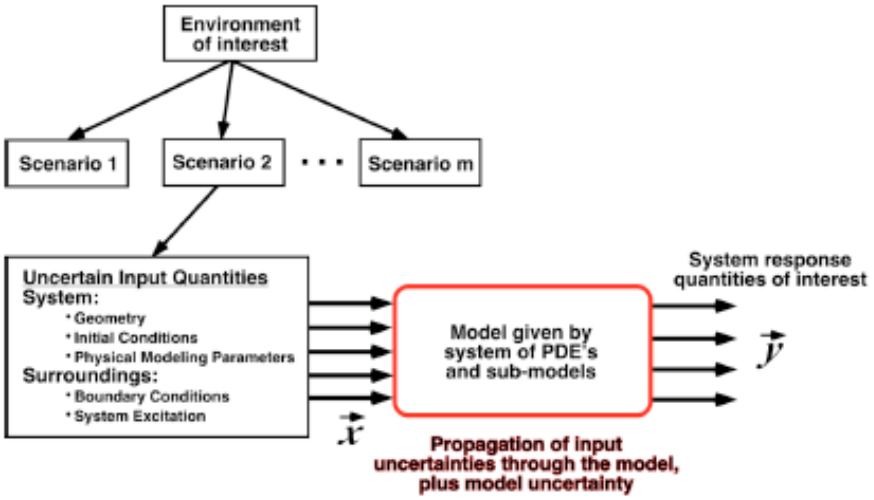


Fig. 4-8 Approach for propagating uncertainty through a simulation tool (from [183]).

Predictive Capability

Assessment of the predictive capability of a given model should account for all of the possible sources of uncertainty in the simulation prediction discussed above. In addition, the uncertainty in the prediction must necessarily increase when the model is applied outside of the validation domain. While many contributors to uncertainty follow a normal distribution, an important exception is the model form uncertainty, where the uncertainty is due to a lack of knowledge (i.e., epistemic uncertainty). The presence of both random

errors and epistemic uncertainty generally requires the use of Monte Carlo sampling, as depicted in Fig. 4-8.

4.2.5. Model Validation Tests Examples and Results

Subsystem Level Tests: Nominal case and predicting the different SRQ's

As mentioned in the previous section, at this level the boost rectifier is treated as a standalone unit, with access to its input and output terminals only. From the list of tests defined previously, the ones chosen to study for this case are:

- Total input current harmonic distortion (THD)
- Input current harmonic spectrum
- Synchronous d-q frame input impedance
- Dc voltage peak-to-peak ripple
- Output impedance
- Dc voltage and current regulation under voltage supply changes

This section will discuss the different validation cases applied to the two-level boost rectifier in order to predict the system SRQ's defined during the PIRT process. For the subsystem level tests, the boost rectifier is tested running under normal conditions: At 57.5V rms input ac voltage and regulating the dc bus to 270V dc with 400Hz line frequency and 20kHz switching frequency and under transient operation. These different environments are defined based on the power quality (PQ) and DO-160 standards. These standards are requirements defined by the industry (for this case aircraft manufactures) for the hardware delivered to them to meet. For purpose of validation, we propose the models need to also meet these requirements and if it failed then the hardware prototype has to fail also. Under these tests and requirements, the different SRQ's will be measured and the procedure defined in previous section will be followed.

a) Normal steady state operation environment:

Fig. 4-9 and Fig. 4-10 shows the results for the time domain analysis and frequency characteristics of the input phase current respectively. The figure compares the switching model, LFLS model to the experimental prototype. From these two figures, two of the SRQ's can be predicted, the input current harmonics (SRQ1: THD) and SRQ 2 which is the individual harmonics spectrum. The total harmonic distortion (THD) is calculated till half the switching frequency for each model and given as shown on Fig. 4-9 where the results shows less than 0.5% error between the models.

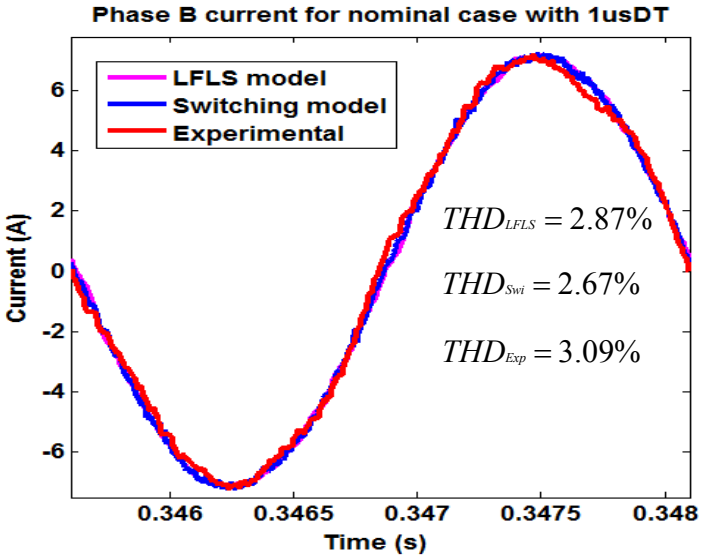


Fig. 4-9 Phase B input ac current for nominal case for switching model, LFLS model and the experimental prototype.

For the SRQ 2: individual harmonics spectrum, the limit for which the harmonics can't exceed is defined from the power quality standards as shown in Fig. 4-11. Table 4-7 shows the actual values for each harmonic for the different models and experimental prototype that are also presented by the black lines in Fig. 4-10. It can be seen that on the low even harmonics (2^{nd}, 4^{th} and 6^{th}), both models and experimental prototype violate the standards which is a good sign for validation since when the model is bad, the prototype

is also bad. In order to quantify the error more, the deviation accuracy measure defined in Eqn. 2.7 is used to calculate the error based on the 5th harmonic which for this case has the largest difference. The deviation between the experimental prototype and the switching model is given as: $\sigma_{\exp\ swi} = 0.416$ and the deviation between the experimental prototype and the LFLS model is given as: $\sigma_{\exp\ LFLS} = 0.645$. This shows that the converter model needs more improvement from that aspect. There are some explanations for this mismatch; however, more investigation needs to be done for this point. From these reasons is the effect of the source and how good is it. The model used ideal voltage source and didn't consider the output impedance of the source, however as we saw from Fig. 2-22, by using different ac sources, we can get very different currents and harmonics. Another reason can be the uncertainty in the dead time. There can be some delays that are missing in the models and would cause these distortions.

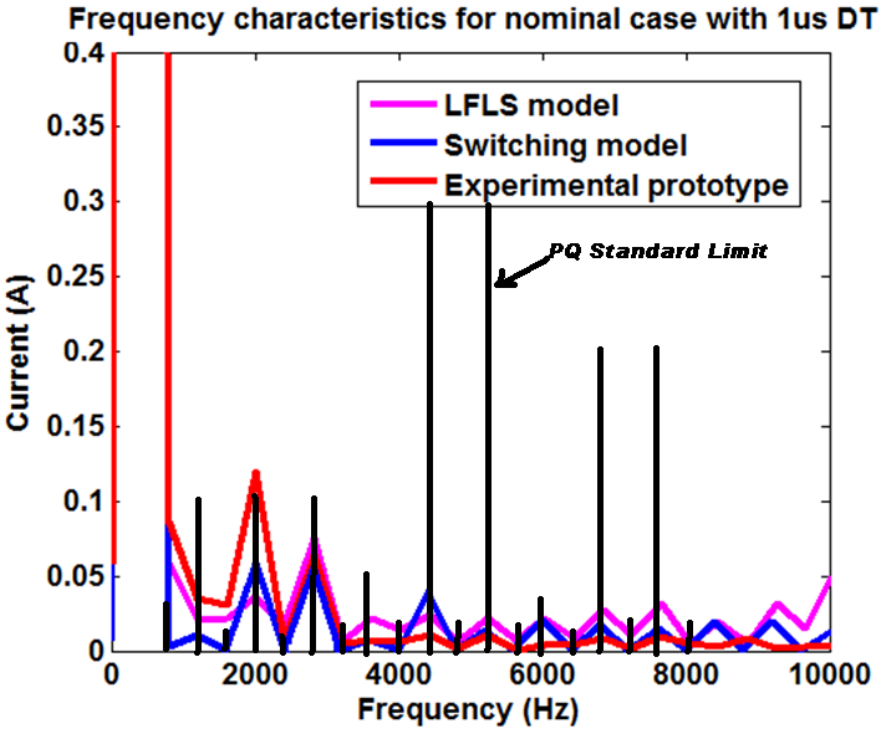


Fig. 4-10 The frequency characteristics of the phase input current for nominal case for switching model, LFLS model and the experimental prototype.

Harmonic Order	Limits
3^{rd}, 5^{th}, 7^{th}	$I_h = 0.02\ I_1$
Odd Triplen Harmonics (h = 9, 15, 21, ..., 39)	$I_h = 0.1\ I_1 / h$
11^{th}	$0.1\ I_1$
13^{th}	$0.08\ I_1$
Odd Non Triplen Harmonics 17, 19	$0.04\ I_1$
Odd Non Triplen Harmonics 23, 25	$0.03\ I_1$
Odd Non Triplen Harmonics 29, 31, 35, 37	$I_h = 0.3\ I_1 / h$
Even Harmonics 2 and 4	$I_h = 0.01\ I_1 / h$
Even Harmonics > 4 (h = 6, 8, 10, ..., 40)	$I_h = 0.0025\ I_1$

Fig. 4-11 Limits for the current harmonics from PQ standards.

Table 4-7 Complete Harmonic Analysis for Switching, LFLS Models and Experimental Prototype.

Harmonic Number	PQ Limit	Experimental Prototype	Switching Model	LFLS Model
2 (800 Hz)	0.02518	0.08671	0.06985	0.05996
3 (1200 Hz)	0.10072	0.03541	0.01097	0.02037
4 (1600 Hz)	0.01259	0.03071	0.0009803	0.02191
5 (2000 Hz)	0.10072	0.10092	0.05901	0.03597
6 (2400 Hz)	0.01259	0.006024	0.05995	0.07541
7 (2800 Hz)	0.10072	0.06448	0.05995	0.07541
8 (3200 Hz)	0.01259	0.004538	0.0005542	0.006605
9 (3600 Hz)	0.0559	0.007445	0.007382	0.02228
10 (4000 Hz)	0.01259	0.005846	0.0001872	0.004102
11 (4400 Hz)	0.5036	0.01054	0.03925	0.02398
12 (4800 Hz)	0.01259	0.001166	0.0002367	0.006566
13 (5200 Hz)	0.40288	0.01093	0.01378	0.02222
14 (5600 Hz)	0.01259	0.0004962	0.0004123	0.00676
15 (6000 Hz)	0.03357	0.004216	0.02065	0.02196
16 (6400 Hz)	0.01259	0.004178	0.000328	0.007864

17 (6800 Hz)	**0.20144**	**0.007894**	**0.0178**	**0.02734**
18 (7200 Hz)	**0.01259**	**0.00165**	**0.0001584**	**0.01036**
19 (7600 Hz)	**0.20144**	**0.008948**	**0.01484**	**0.03143**
20 (8000 Hz)	**0.01259**	**0.004572**	**0.0032**	**0.004572**

The other important system response quantities (SRQ's) that was discussed earlier in the PIRT stage are SRQ 4: dc link voltage average value and SRQ 5:Pk-pk differential dc link voltage ripple. Fig. 4-12 shows the results for comparing the dc link voltage for the switching and LFLS model versus the experimental prototype. As can be seen from Fig. 4-12, the average dc link voltage value is 269.92V for the LFLS model, 269.91V for the switching model and 269.9V for the experimental prototype. Therefore if calculated the error for this SRQ, it can be seen that the error between the experimental and switching model is $Error_{ExpSw}$=0.0037% and the error between the experimental prototype and the LFLS model is $Error_{ExpLFLS}$=0.0074%.

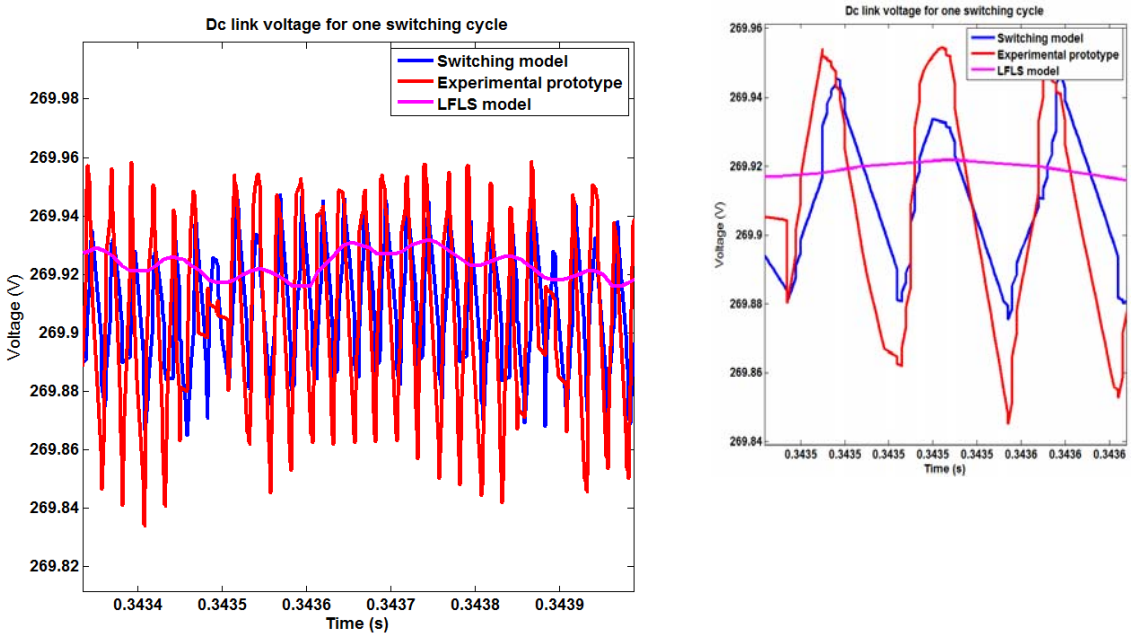


Fig. 4-12 Dc link voltage comparison for nominal case and the zoomed version.

For the differential voltage ripple system response quantity (SRQ 5), the LFLS model ripple voltage is found to be 0.015V, the switching model is 0.065V and the experimental prototype is 0.12V which means the model can't predict this SRQ accurately since the error between the experimental prototype and the switching model is about 45.8% and between the experimental prototype and the low frequency large signal model (LFLS) is 87.5%. This can be due to the different sampling in the oscilloscope versus the model, the time step of the simulation and the amount of data points saved.

Finally, the last two SRQ's studied for the normal steady state operating conditions are the input and output impedance. For this case (two-level boost rectifier), Fig. 4-13 shows the experimental setup and where the impedance analyzer that is used to measure the ac impedance is injected. For the dc impedance, the tool is injected the same way but on the dc side.

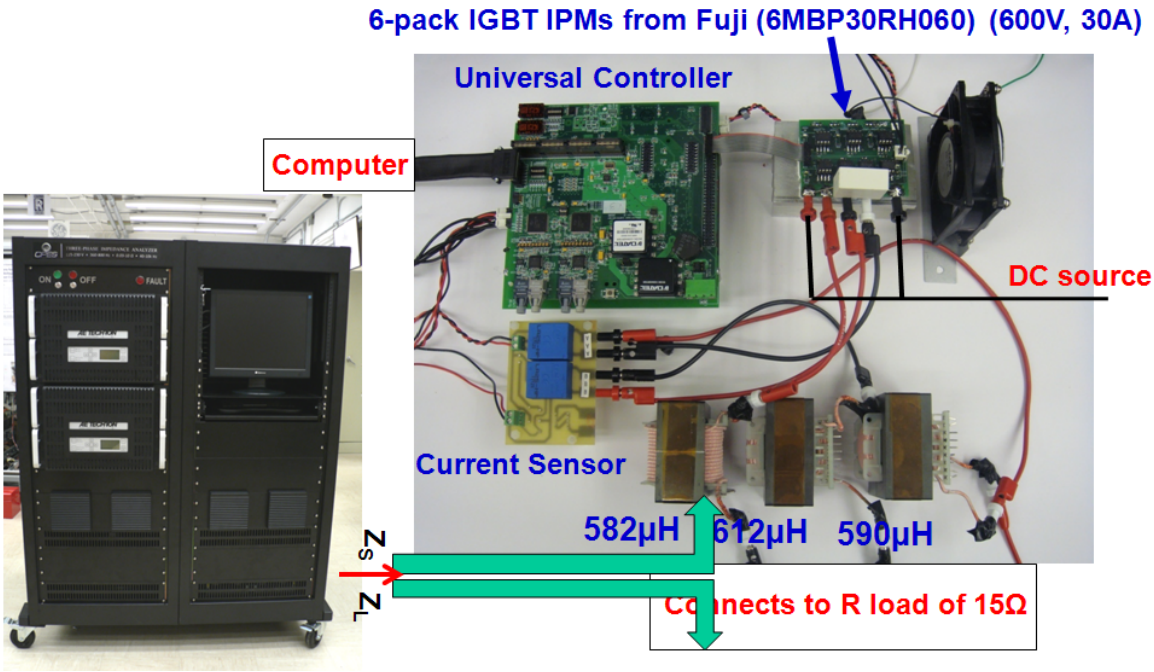


Fig. 4-13 Experimental setup for impedance measurement

The output impedance of the boost rectifier is dc impedance and Fig. 4-14 shows the comparison between the measurement results and the two models. It can be seen that the

low frequencies can be predicted well and for this case it is representing the dc output capacitor of the system which is equal to 520µF. However, there are some mismatches at the high frequencies which are not shown in Fig. 4-14 and this is because of using wires in the real experiment which are not modeled in the simulation. It is seen from the experimental result that the wires are equal to around 15µH.

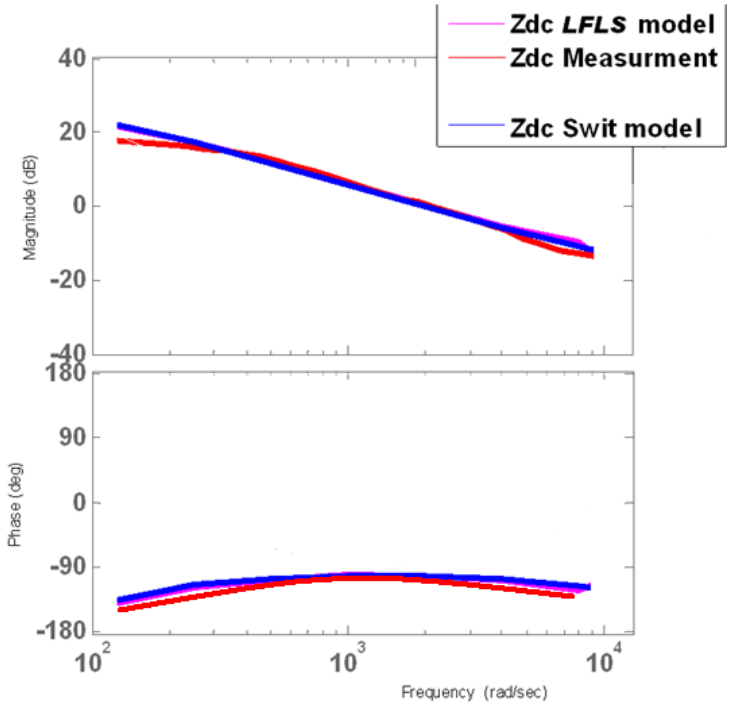


Fig. 4-14 Output impedance of the two-level boost rectifier comparison

The input impedance of the two-level boost rectifier is ac impedance as discussed in chapter 3 and is represented in the dq frame by a matrix as follows: $[Z]_{dq} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix}$.

Fig. 4-15 shows the input impedance for the switching, LFLS model and for the experimental prototype. It can be seen that the error is in 2-3dB which is within the equipment measurement error. If we analyzed the results, it can be seen that the beginning is the effect of the voltage loop where the phase is going to -180 degrees then the effect of the current controller till 500Hz which is the bandwidth of the controller and finally the resonance is due to the EMI filter with the boost inductance. Fig. 4-16

compares the full model impedance measurement with the impedance simulated if there is no EMI filter. This is to prove that the resonance in Fig. 4-15 is coming from the EMI filter resonating with the boost inductor.

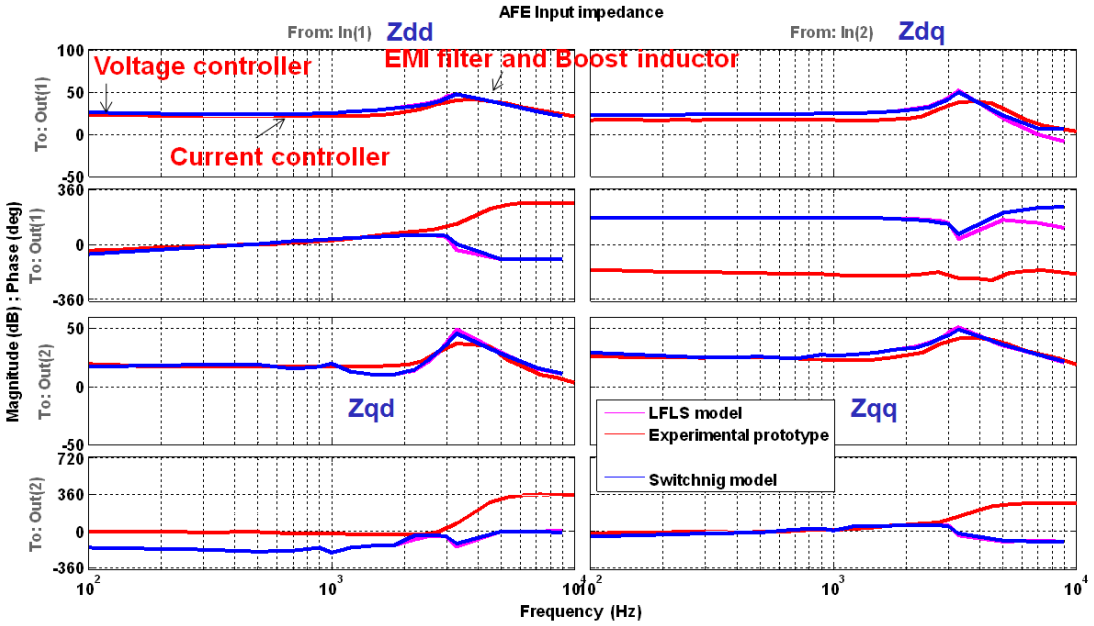


Fig. 4-15 Input impedance of the two-level boost rectifier comparison

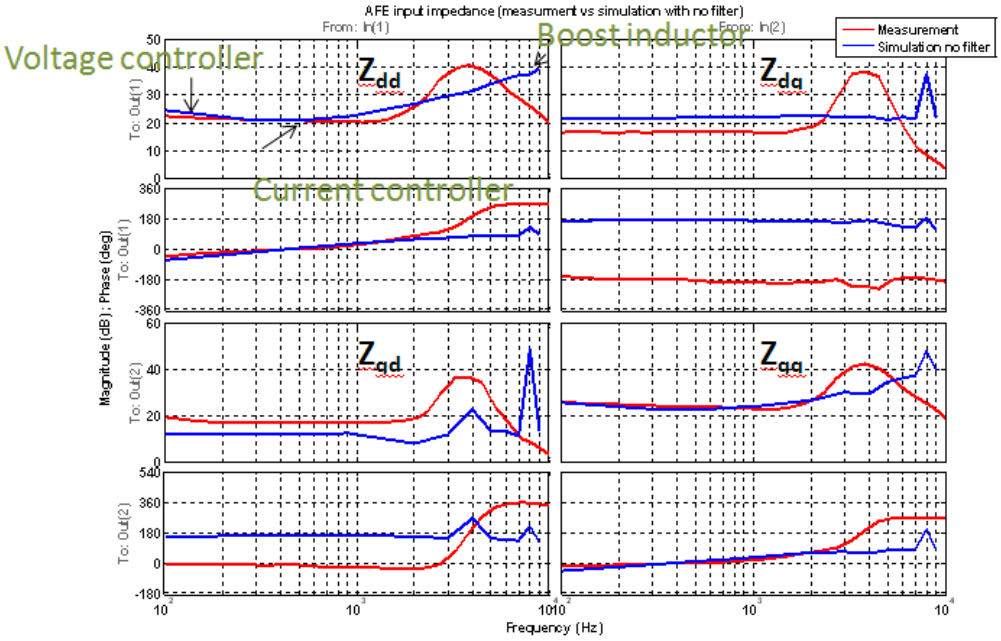


Fig. 4-16 Input impedance of the two-level boost rectifier comparing the full measurement with the simulation with no EMI filter.

The capacitance and inductance value can also be calculated from the slopes and it is found to be 1μF which is equal to the differential capacitor in the filter. Fig. 4-17 compares the effect of the current bandwidth and it can be seen that when the current loop bandwidth is increased from 500 Hz to 1300 Hz, the impedance is also higher.

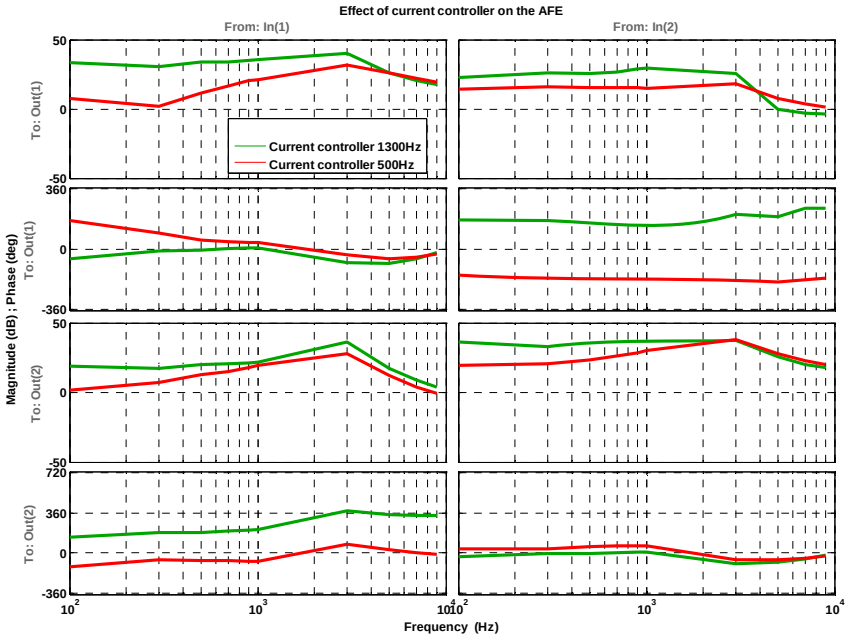


Fig. 4-17 Input impedance of the two-level boost rectifier comparing two current loop bandwidth

a) Normal transient operation environment:

Following the PIRT approach, there are two environments defined, the normal and abnormal steady state operation and normal and abnormal transient operation. This section will discuss the validation tests that were applied to the boost rectifier under the transient environment. From Table 4-2, it can be seen that the important physical phenomenon is the time domain transient and the 2 SRQ's are dc link voltage and input current time domain performance. There are different transient's tests that are defined using the PQ standards like voltage transients, frequency transients and load transients.

Voltage transient:

Fig. 4-18 shows an example from the transient validation cases. For this case, the boost rectifier is operated for five minutes with an ac input voltage of 57.5 V rms at equipment terminals, then the voltage is cycled three times as follows: the voltage is increased to 75V rms, in less than 1ms, and the rectifier is operated for 30ms. Then the voltage is returned to 57.5V rms, in less than 1ms, and operated under normal conditions for five seconds. The voltage is then decreased to 35V rms, in less than 1ms, and operated for 30ms. Finally, the voltage is returned to 57.5 V rms, in less than 1ms, and operated under normal conditions for five seconds.

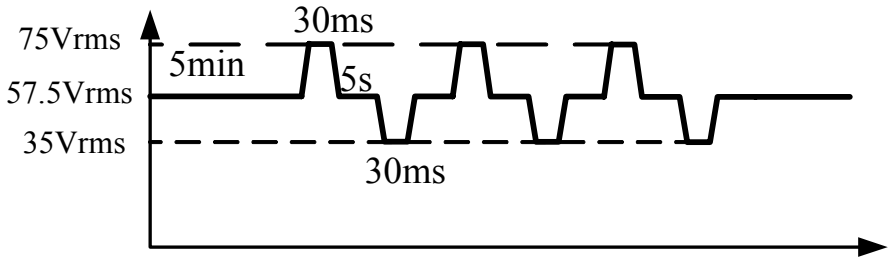


Fig. 4-18 Normal voltage transient from the PQ quality standards

Fig. 4-19 shows phase A voltage when the voltage transient pattern defined in Fig. 4-18 is applied to it. As a consequence of applying this voltage transient, the ac input current is changed as seen in Fig. 4-20 till it regulated back to its nominal value. Fig. 4-20 shows the response of both switching and LFLS models in addition to the experimental prototype. It can be seen from the time domain analysis that the models can predict the transient response as close to the experimental one. However, it is hard to predict the error percentage from looking at the waveform in Fig. 4-20. Therefore, in order to have a more accurate measurement, the moving rms of the phase current is calculated for both models and experimental prototype and compared. It can be seen from Fig. 4-21 that all of them can meet the power quality standards defined by the black curve. The power

quality standards states that when the voltage step is applied the current cannot exceed 150% of the nominal value and have to be able to go back to 125% of the nominal value after 100μs from the start of the transient. The system can then stay at 125% of the nominal value for 1.5s then has to go back to the normal operation. The percentage error is calculated based on the maximum deviated point and this is found at time is equal to 0.416s. The error between the experimental prototype and the models at this point is around 9%.

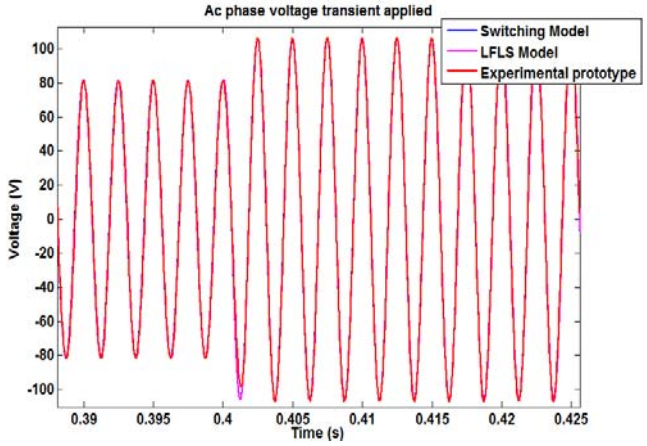


Fig. 4-19 Ac voltage with the step up voltage transient from 57.5V rms to 75 V rms

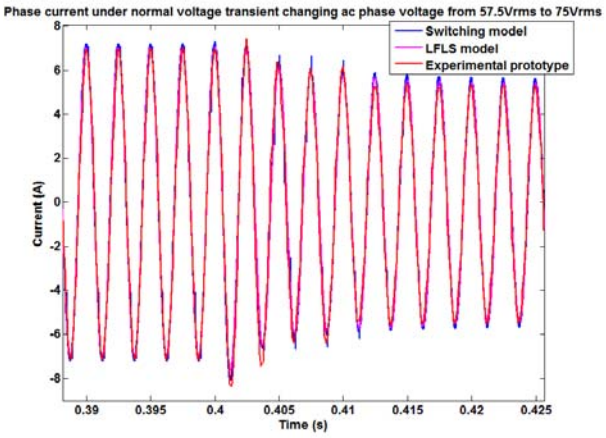


Fig. 4-20 Resultant phase current to the step up voltage transient from 57.5V rms to 75 V rms

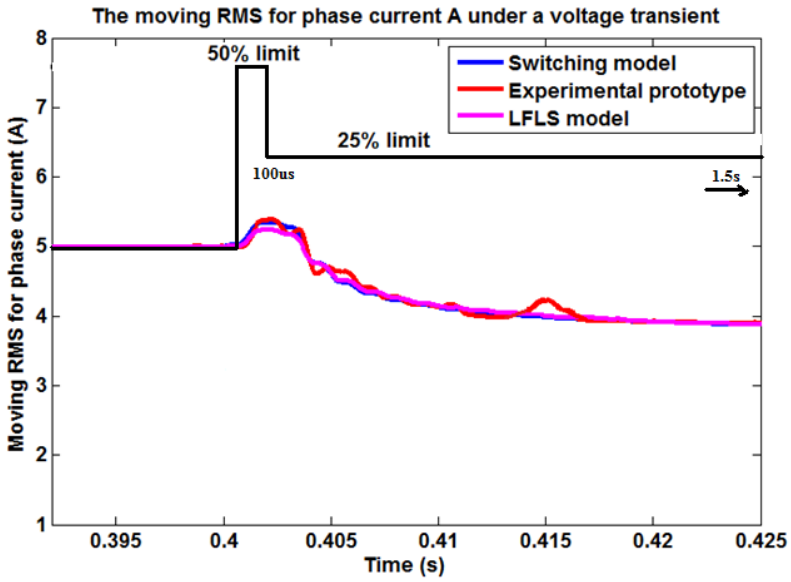


Fig. 4-21 Moving RMS for phase current under the step up voltage transient from 57.5V rms to 75 V rms

Fig. 4-22 shows the other part of the transient pattern shown in Fig. 4-18 where the voltage changes from 35 V rms to 57.5V rms. It can be seen that the resultant phase current doesn't go to steady state which means the settling time is much longer than the 30ms duration of the transient. However, for validation purposes, this is a good case

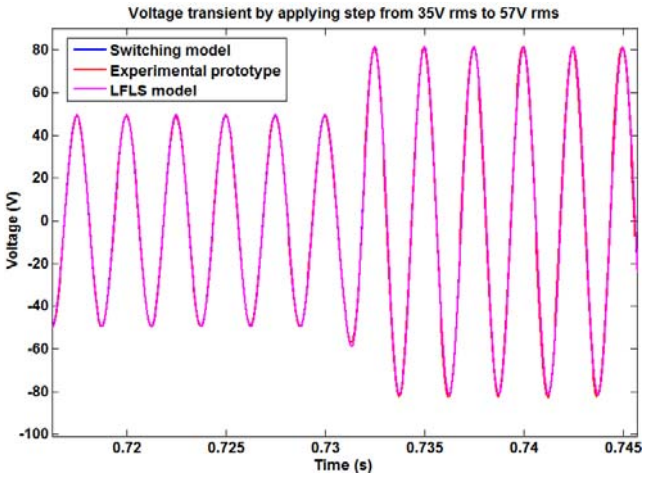


Fig. 4-22 Ac voltage with the step from 35 V rms to 57.5V rms

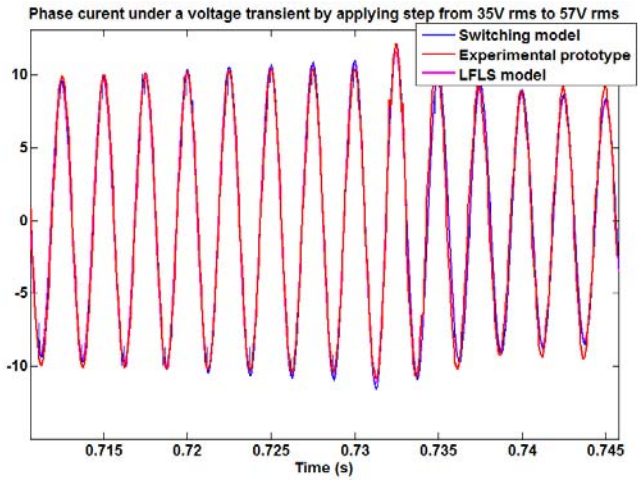


Fig. 4-23 Resultant phase current to the step in voltage from 35 V rms to 57.5V rms

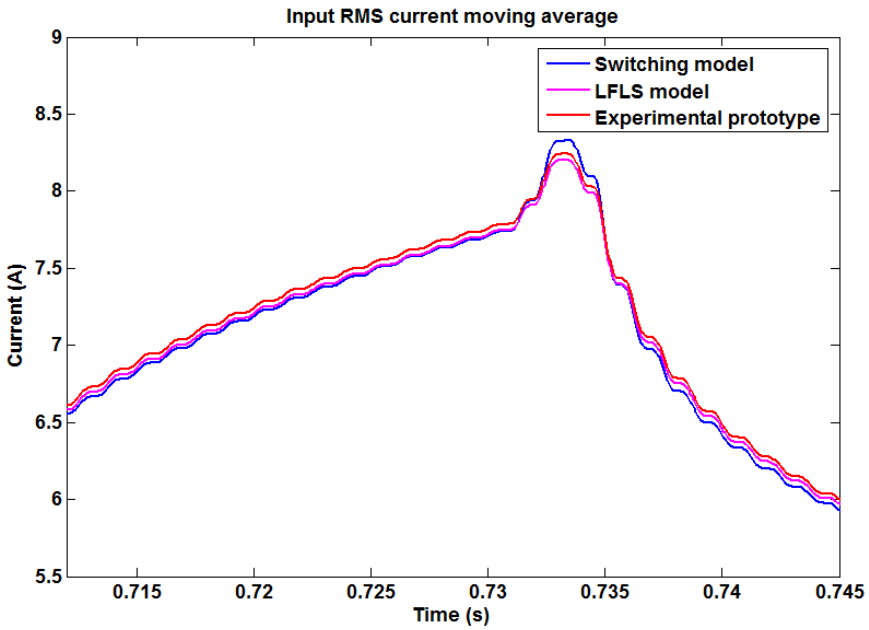


Fig. 4-24 Moving RMS for phase current under a voltage step from 35 V rms to 57.5V rms

where it shows that the experimental prototype settling time and that of the models is the same which shows that the controller performance in both models and experiment is close. The percentage error is again calculated based on the maximum deviated point and this is found at time is equal to 0.733s which is the point where the voltage is stepped. The error between the experimental prototype and the models at this point is around 2%.

The second important SRQ during transient is the dc link voltage time domain performance. Fig. 4-25 shows the dc link voltage response under normal operation voltage transient. The power quality limit is defined by the two black lines where it can be seen that the dc link voltage meets the requirements during the step up of the voltage but violates the standard during the step down and this is the same conclusion that was found from the current waveform which is not settled. This shows the performance of the controller and how it is slow and it also shows how the model predicts well the correct performance. Fig. 4-26 and Fig. 4-27 shows the zoomed version of the dc link voltage under the step up and down voltage transient respectively. It can be seen that models and prototype matches pretty well and that the error doesn't exceed 0.5%.

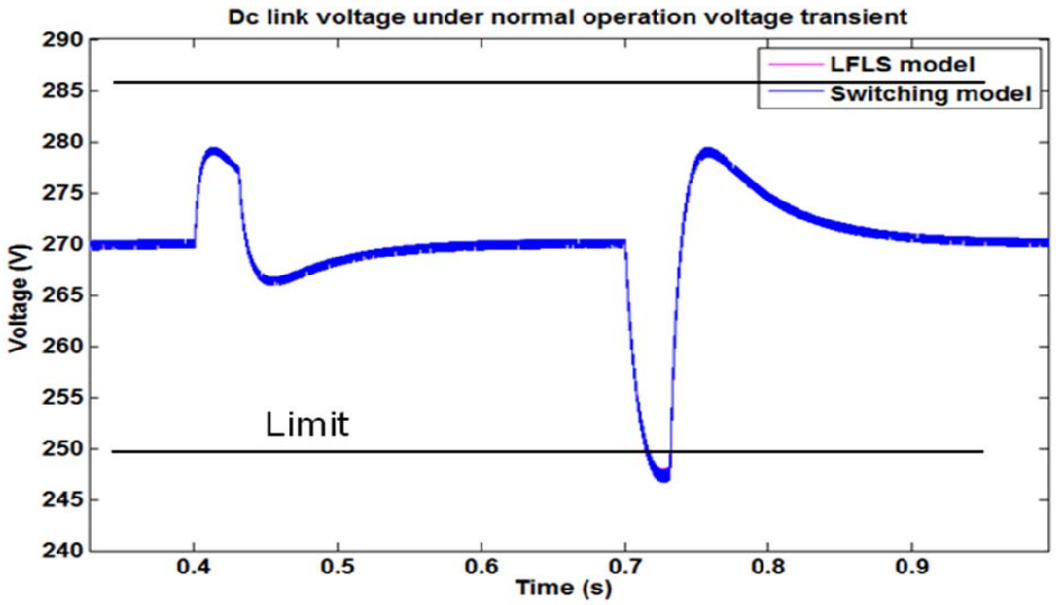


Fig. 4-25 Dc Link voltage response during the ac voltage transient

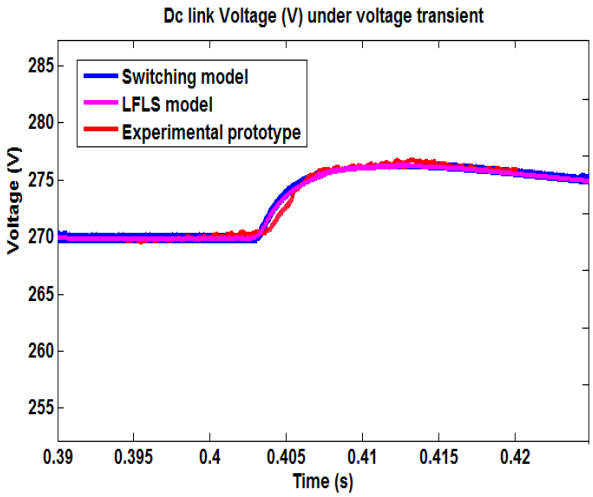


Fig. 4-26 Dc link voltage with the step from 35 V rms to 57.5V rms

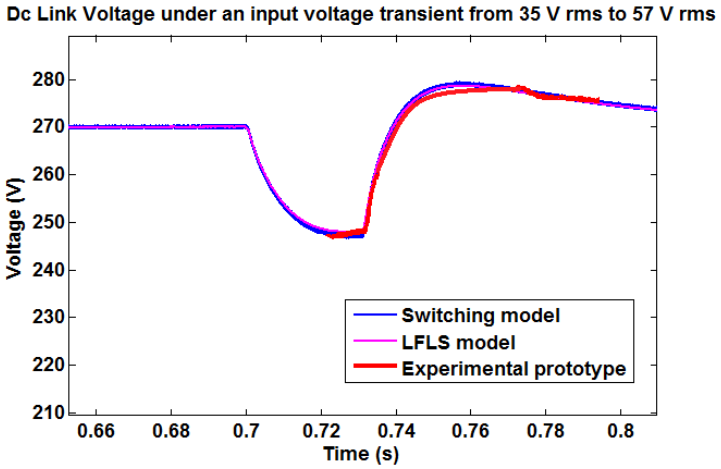


Fig. 4-27 Dc link voltage to the step in voltage from 35 V rms to 57.5V rms

Boundaries and Uncertainty Quantification Cases:

As mentioned in the previous section, for each environment and scenarios there are some uncertain input quantities that need to be considered for a complete validation process.

These uncertainties as discussed come from either physical parameters of the power converter or from the surroundings as the operating conditions and the boundaries of the system operation. This section will give different case examples for the converter surroundings and how the models are validated.

Case 1: Converter operating at maximum allowed input voltage (61Vrms)

This case shows the model ability to work under the full range of input voltages defined by the power quality standards. From the PQ standards, the nominal voltage applied to the converter should be increased to the maximum allowed voltage which for this case is 61 Vrms. The converter is then required to regulate the input current and the dc voltage and perform normally under these conditions. Therefore, the operating conditions are compared for the different models and experimental prototype and validated against the power quality standard requirements.

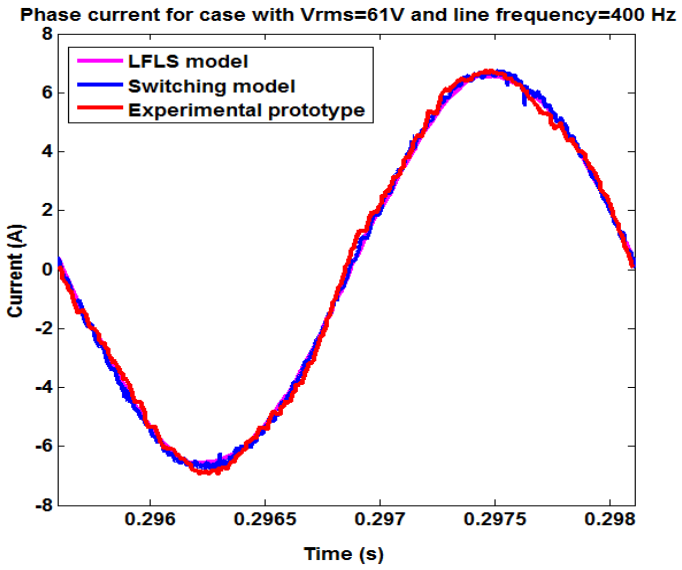


Fig. 4-28 Phase current with 61Vrms ac voltage applied and line frequency = 400Hz

Fig. 4-28 shows the input current response to the increase in the input voltage. It can be seen that the converter is able to regulate the current to its nominal value. As a comparison point between the different models and experimental prototype, the input

current rms value is calculated for each of them and a percentage error is found. It can be seen that the input current rms value for the LFLS model is 4.631 A rms, switching model is 4.7489 A rms and the experimental prototype is 4.79349 A rms. The percentage error calculated based on these value shows an error of 3.38% between the experimental prototype and the LFLS model and 0.93% between the switching model and the experimental prototype. The other system response quantity to look at is the regulated dc link voltage. Fig. 4-29 shows the dc bus voltage regulated to 270 V. The average dc link voltage is calculated as the measurement performance measure. According to the power quality standards, the dc link voltage is required to stay between 250 V and 320 V and the peak to peak ripple shouldn't exceed 16 V. For this case, it can be seen that the average dc link voltage for the LFLS model is 269.575V, for the switching model is 269.58V and for the experimental prototype is 269.56V. Therefore, if the percentage error is calculated, we can find an error of 0.0056% between the experimental prototype and LFLS model and 0.0074% error between the switching model and the experimental prototype. For the peak to peak differential voltage ripple, it is found to be 0.004V for the LFLS model, 0.05V for the switching model and 0.09V for the experimental prototype. It can be seen that both models can hardly predict the exact voltage ripple as there is a 94% error between the experimental result and LFLS model and 44.4% error with the switching model.

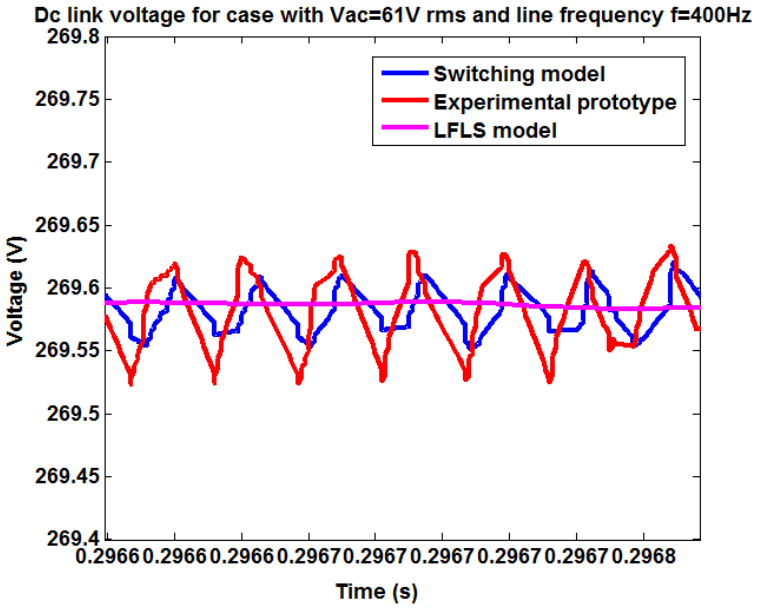


Fig. 4-29 Dc link voltage with 61Vrms ac voltage applied and line frequency = 400Hz

Case 2: Converter operating at different line frequency (f=800 Hz)

Another uncertain quantity of the boundary conditions is the frequency of the system. The converter studied is capable of working under all line frequencies in the range of 360Hz to 800Hz. This case discusses the performance of the boost rectifier under the maximum line frequency (800 Hz). The same analysis is done as the previous case where both the input current rms value and the average dc link voltage SRQ's are predicted. Fig. 4-30 shows the input current response to the change in frequency. It can be seen that the converter is able to regulate the current to its nominal value. As a comparison point between the different models and experimental prototype, the input current rms value is calculated for each of them and a percentage error is found. It can be seen that the input current rms value for the LFLS model is 4.8571 A rms, switching model is 4.858 A rms and the experimental prototype is 4.7913 A rms. The percentage error calculated based on these value shows an error of 1.373% between the experimental prototype and the LFLS model and 1.37% between the switching model and the experimental prototype.

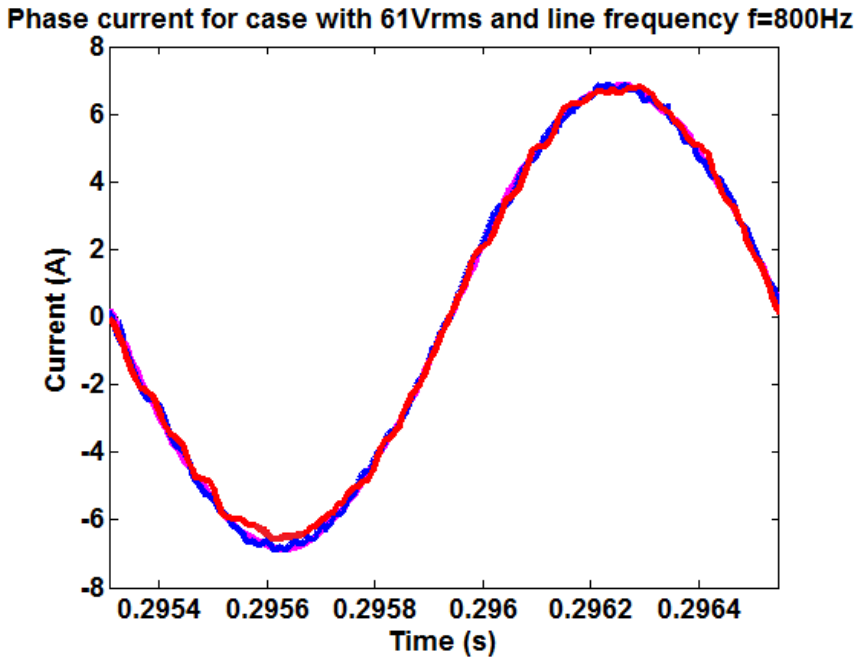


Fig. 4-30 Phase current with 61Vrms ac voltage applied and line frequency = 800Hz

The other system response quantity to investigate is the regulated dc link voltage. Fig. 4-31 shows the dc bus voltage regulated to 270 V. The average dc link voltage is calculated as the measurement performance measure. According to the power quality standards as mentioned in the previous case, the dc link voltage is required to stay between 250 V and 320 V and the peak to peak ripple shouldn't exceed 16 V. For this case, it can be seen that the average dc link voltage for the LFLS model is 269.55V, for the switching model is 269.54V and for the experimental prototype is 269.535V. Therefore, if the percentage error is calculated, we can find an error of 0.0055% between the experimental prototype and LFLS model and 0.0018% error between the switching model and the experimental prototype. For the peak to peak differential voltage ripple, it is found to be 0.02V for the LFLS model, 0.06V for the switching model and 0.09V for the experimental prototype. It can be seen that both models can hardly predict the exact voltage ripple as there is a 77.7% error between the experimental result and LFLS model and 33% error with the switching model.

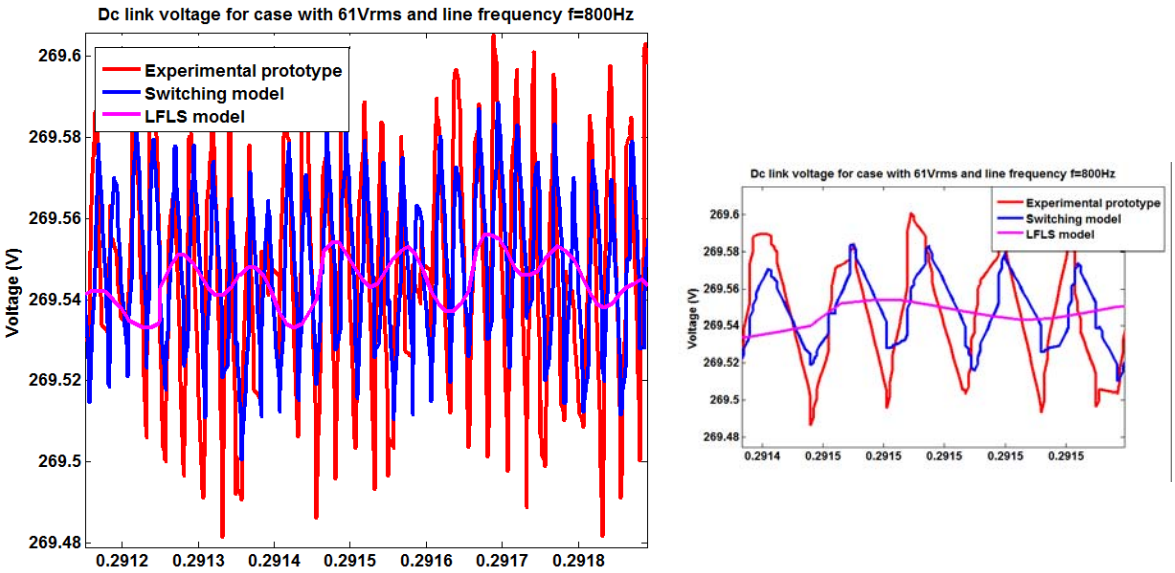


Fig. 4-31 Dc link voltage with 61Vrms ac voltage applied and line frequency = 800Hz

Case 3: Converter operating under normal operating conditions with 4μs dead time:

One of the main features of the low frequency large signal (LFLS) model as described in the previous chapters is that it can predict the low frequency harmonics due to dead time and non-linearities in the system. Therefore, it is important to study this case as part of the validation tests. For this case, the converter is operating under normal conditions with a 4μs dead time. Fig. 4-32 depicts the phase current for the three different models, the ideal average model that is not capable of predicting any harmonics (just the fundamental frequency), the LFLS and switching models with harmonics and the experimental prototype. The first SRQ to predict is the input current rms value and for this case, the rms value for the tdeal average model is 5.035A rms, for the LFLS model is 5.026 A rms, for the switching model is 5.045 A rms and the experimental prototype is 5.0346 A rms. The percentage error calculated based on these value shows an error of 0.206% between the experimental prototype and the switching model, 0.17% between the LFLS model and the experimental prototype and 0.079% between the experimental

prototype and the ideal average model. One can conclude from that the ability of all types of models to predict the rms value.

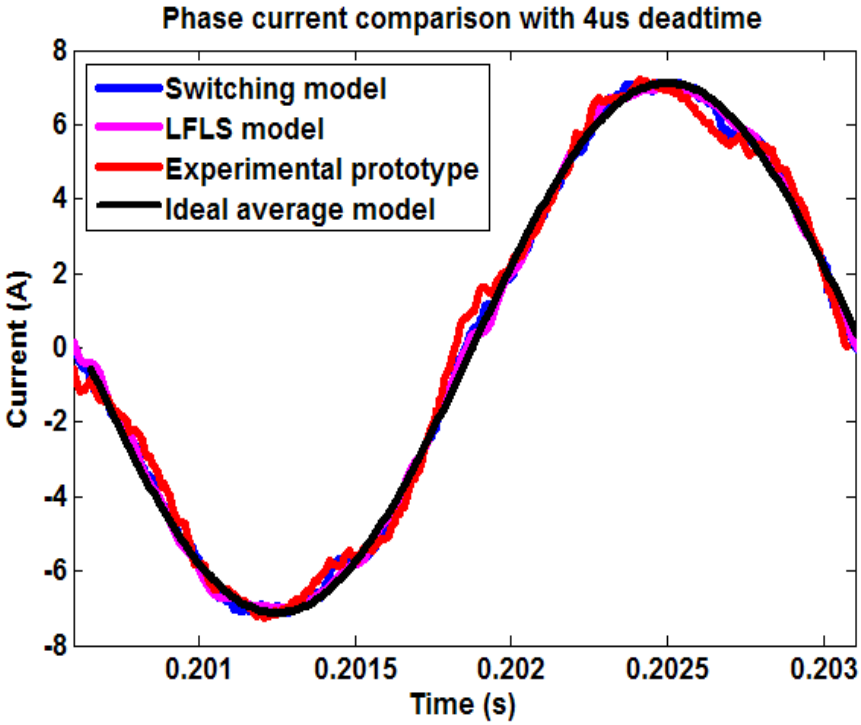


Fig. 4-32 Phase current for nominal condition with 4μs dead time

The other SRQ that is important to predict especially for this case is the total harmonic distortion. The harmonics analysis is done till half the switching frequency and each harmonic is compared to the power quality limit defined in Fig. 4-11. The total harmonic distortion for the low frequency large signal model is calculated as, $THD_{LFLS} = 4.91\%$, for the switching model as, $THD_{Swi} = 5.1\%$ and for the experimental prototype to be $THD_{Exp} = 5.6\%$. It can be seen that the THD increased around 2% by adding the dead time of 4μs and that both models could predict the correct harmonics like the experiment. Fig. 4-33 depicts the frequency spectrum for phase current with the 4μs dead time. It can be seen that the largest discrepancies is in the 5^{th}, 7^{th} and 11^{th} harmonics. The deviation accuracy measure defined in Eqn. 2.7 is calculated for the 5^{th} harmonic for both models and experimental prototype and it is found to be around $\sigma_{\exp swi} = 0.089$ between the

experimental and the switching model and around $\sigma_{\exp LFLS} = 0.087$ between the experimental and low frequency large signal model.

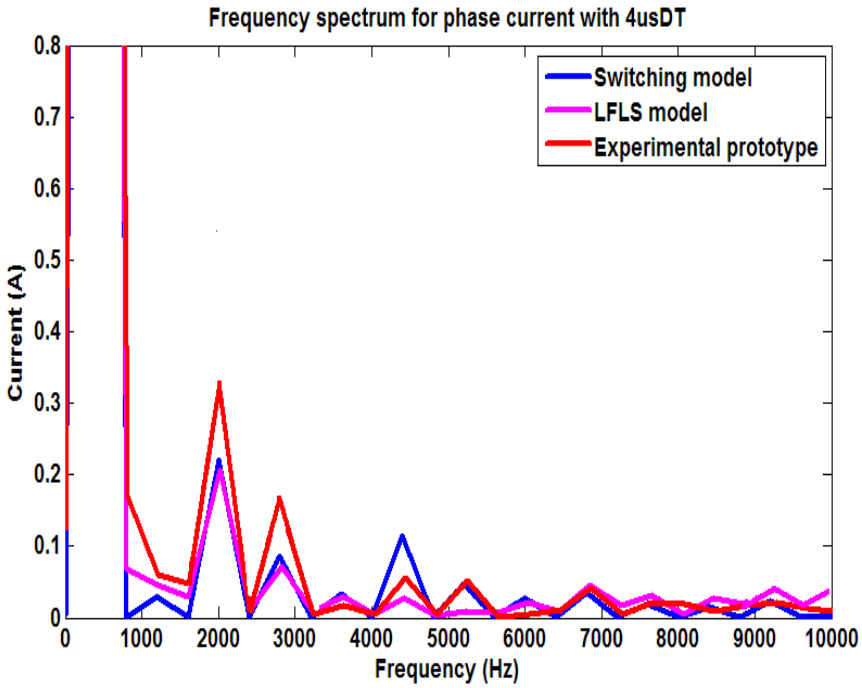


Fig. 4-33 Phase current frequency spectrum for nominal condition with 4μs dead time

The other system response quantity to investigate is the regulated dc link voltage. Fig. 4-34 shows the dc bus voltage regulated to 270 V. The average dc link voltage is calculated as the measurement performance measure. According to the power quality standards as mentioned in the previous cases, the dc link voltage is required to stay between 250 V and 320 V and the peak to peak ripple shouldn't exceed 16 V. For this case, it can be seen that the average dc link voltage for the LFLS model is 269.48V, for the switching model is 269.5V and for the experimental prototype is 269.49V. Therefore, if the percentage error is calculated, we can find an error of 0.00371% between the experimental prototype and LFLS model and 0.003% error between the switching model and the experimental prototype. For the peak to peak differential voltage ripple, it is found to be 0.02V for the LFLS model, 0.055V for the switching model and 0.1V for the experimental prototype. It can be seen that both models can hardly predict the exact

voltage ripple as there is a 80% error between the experimental result and LFLS model and 45% error with the switching model.

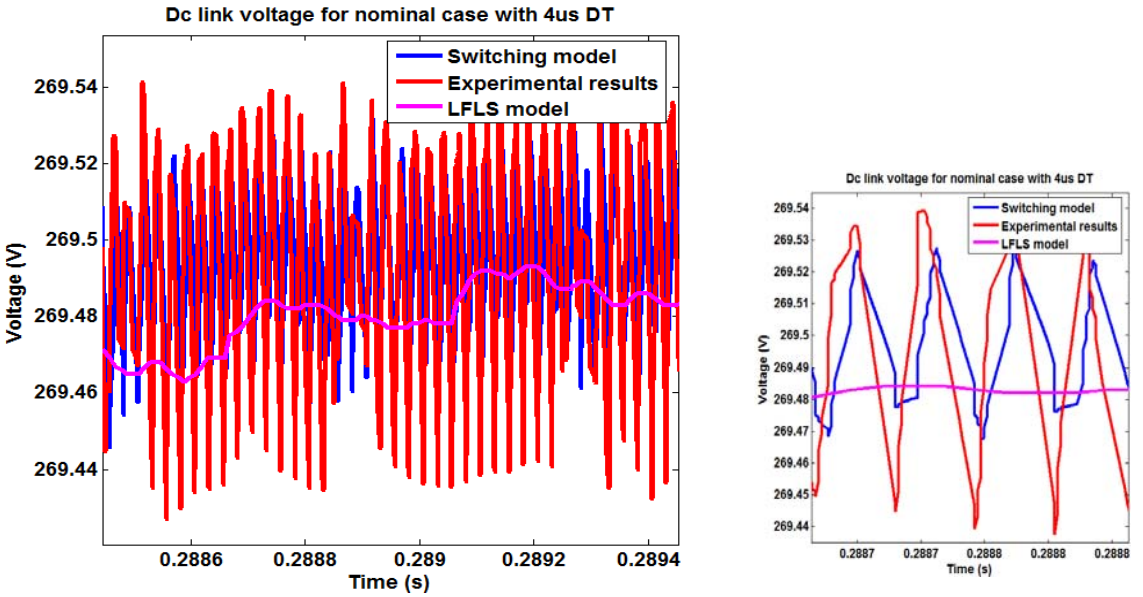


Fig. 4-34 Dc link voltage for nominal condition with 4μs dead time

4.3. Conclusion

This chapter gave a complete validation process applied to a power electronics converter. It first presented a literature review on the VV&UQ processes both within the power electronics area and in related disciplines, e.g., mechanical engineering and aerospace engineering. A two-level boost rectifier was taken as an example to apply the VV&UQ processes on. The rectifier was modeled in Saber, where switching, average and LFLS model are developed. Then an experimental prototype, including power stage, input filter, power supply and load is developed. The planning and prioritization task came next where the phenomenon identification and ranking tables (PIRT) and gap analysis tables are developed for the different environments and scenarios. The different models were then verified against each other then experiments were conducted to provide validation data for the simulation tool. These experiments include simple unit-level experiments as well as the full

rectifier system. In addition, the validation space is designed so as to capture in the best possible way the intrinsic operation of the converter subsystems, e.g., input voltage level, ac supply frequency, load level, controls bandwidth etc. With all these steps completed, the validation process should be done.

Chapter 5 SYSTEM MODELING AND PERFORMANCE EVALUATION

5.1. Introduction – System Description

The power system under study combines different types of components. The different components are modeled in the stand-alone operation and then interconnected to study the interaction of the different models together. The object of this chapter is to present the power system and provide a description of the models of the main components. It will then propose a different modeling methodology where it combines switching model with low frequency large signal (LFLS) models and describe the main modeling requirements. Fig. 5-1 shows the circuit schematic of the system under analysis with all the power ratings of the components.

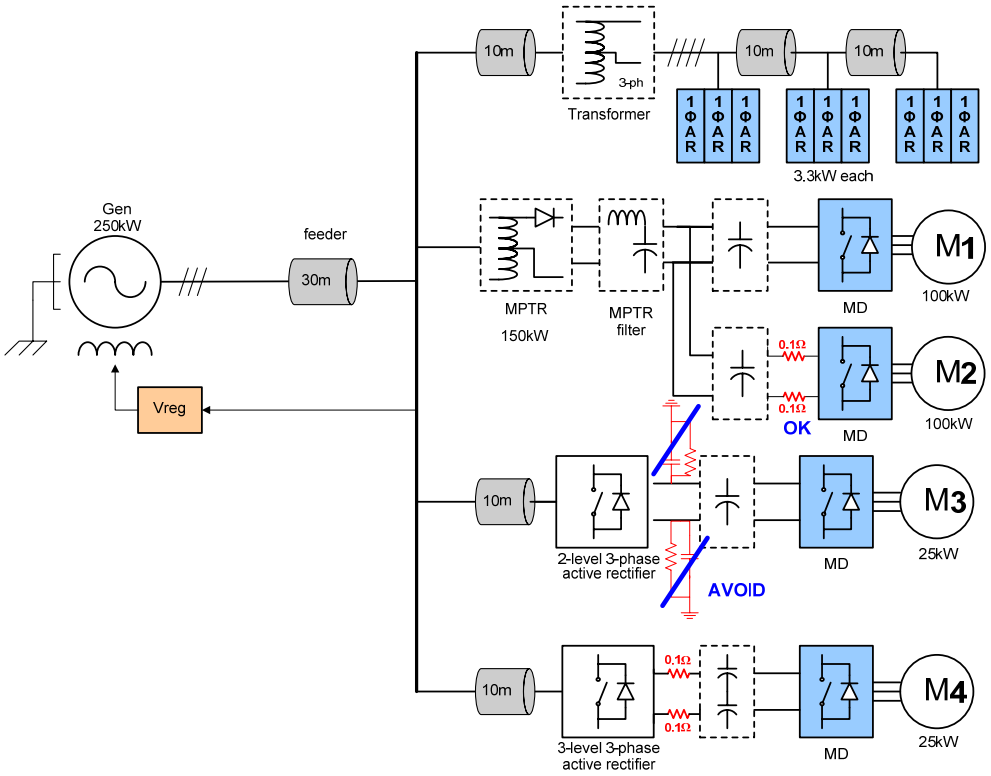


Fig. 5-1 Schematic of a hybrid ac/dc power system used for the study.

The system consists of a three-phase, synchronous machine generator power source with variable speed and remote regulation. It consists of a single machine that is

represented in the *d-q-0* synchronous reference [174]-[176]. This source is feeding multiple ac-dc and ac-to-ac power electronic loads. The main loads that will be discussed in this chapter are the multi-pulse transformer rectifier (MPTR) [177], comprised of a transformer and directly paralleled three-phase diode bridges as shown in the left of Fig. 5-2, three phase active rectifier (3ΦAR) in Fig. 5-3, and single-phase active rectifiers (1ΦAR).

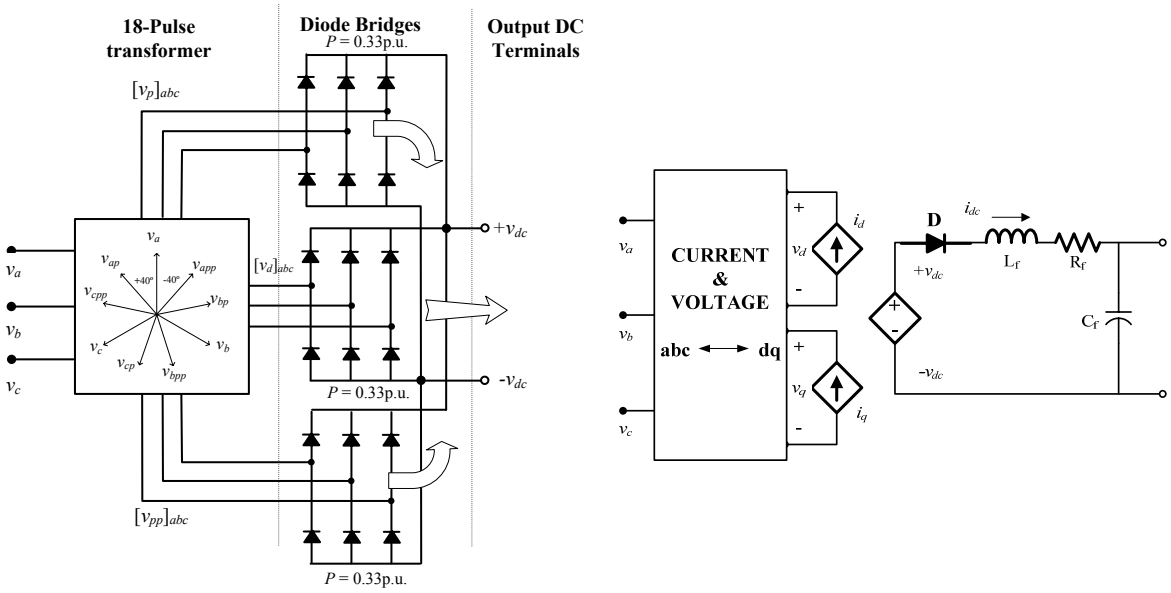


Fig. 5-2 MPTR real model schematic (left) and average model (right).

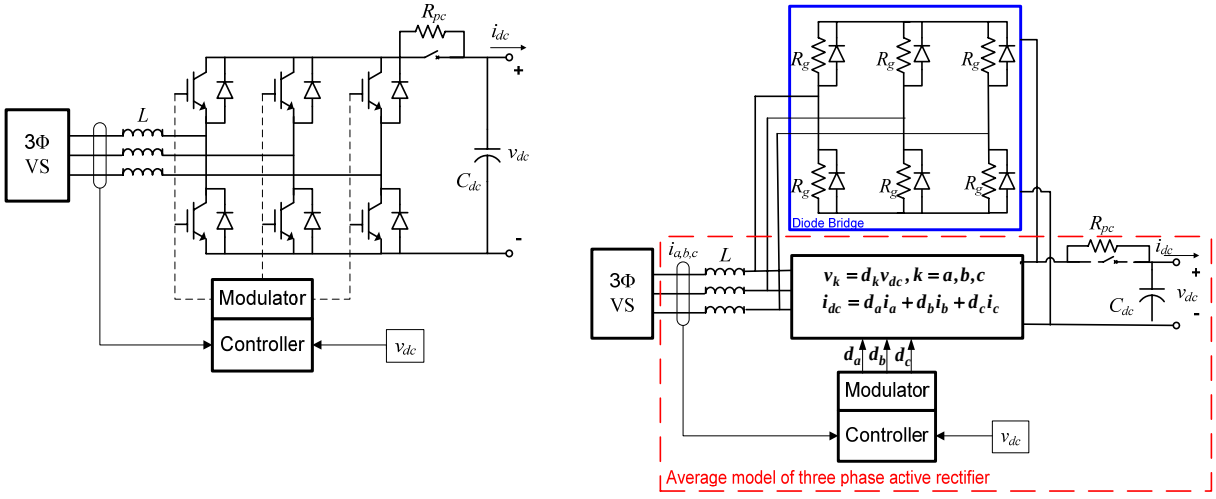


Fig. 5-3 Three phase AR real (left) and new average model (right).

5.2. Proposed Modeling Methodology

The power system under study combines different types of components which can make the system complicated and very hard to simulate and analyze. Therefore we had to come up with a different methodology that would allow us to study the system but with much simplified but accurate models. The different components of the new system are average and low frequency large signal circuit-based models modeled in the stand-alone operation and then interconnected in the circuit simulator (Saber) to analyze the system performance and to study the interaction of the different models together. The terminal characteristics of the models reflect the real detailed model. However, the inside of the model can be a simplified version, with or without detailed control or a sophisticated one depending on the application the system will be used in.

Connecting the subsystems can become an issue especially when the model terminal and inside characteristics are different and transformations are required. For example, some models are designed in dq coordinates, however, the outside terminals are in abc coordinates and this would require measuring the voltages and current fed into the model in line-line order to avoid any ground connections, which usually creates numerical convergence problems afterwards. In addition to the outside connections, the inside of the models are implemented in a non-ideal way that can capture the performance more accurately. These phenomena are discussed in detail in the next section. Since these are stand alone models with realistic terminal characteristics, a mixed system of the new average and LFLS models and the detailed switching models can be designed and used depending on the system application as discussed in the objectives section in the last chapter. For example, if the user is interested in stability studies at one terminal, then average models can be used for that. However, if for example, harmonic distortion is of interest, a detailed switching model that can capture this phenomenon would be more applicable.

5.3. *Practical Considerations for System Modeling*

There are issues faced while modeling the studied average power electronics system. These issues are based on our recent experiences but are worth mentioning because they can be seen in all types of models.

5.3.1. Modeling that captures transients

Power flow directionality

When the average model is designed using the mathematical functions of the models and not the real circuit components, the current direction can be a problem. The average model will not realize the real characteristics of the model and therefore the actual model characteristics have to be integrated by the model developer. For example, some converters, like the multi-pulse transformer rectifier, don't allow current to flow back into the converter (negative current), however, the mathematical function model will limit the current i_{dc} so in order to accommodate that, a diode (D) is required at the output to provide unidirectional current, as shown in the right figure of Fig. 5-2. Fig. 5-4 shows the dc link current being negative at the transient without a diode and when the diode is added, the negative current is eliminated.

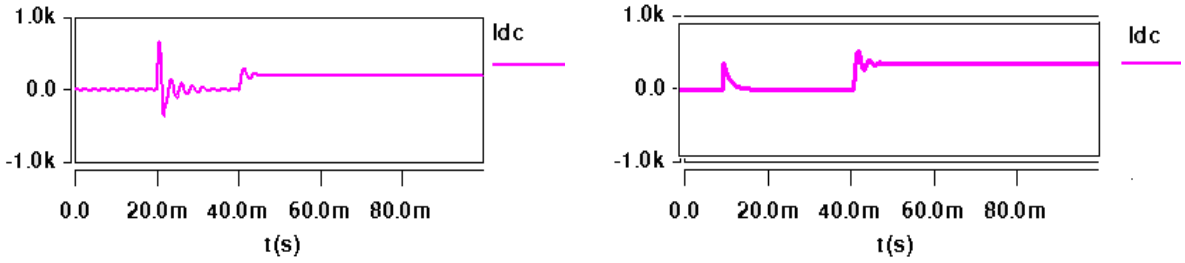


Fig. 5-4 Dc link current at output of MPTR without (left) and with diode (right).

Another example of this phenomenon is seen in the generator model (GEN in Fig. 5-1), a diode is also needed in the controller loop to provide a unidirectional excitation current. In all practical applications, the synchronous generator is limited in its excitation circuit to only excitation currents in one direction [178].

Inrush current

Another phenomenon that is usually not modeled in average models is inrush current. The inrush current is a form of over current (large transient current) that can be large enough to saturate the inductors or even fail the model components. For example, the boost rectifier in Fig. 5-3, has the advantage of a continuous inductor current in the ac line that can be controlled to obtain a unity power factor. However, there is an inherent disadvantage—the existence of uncontrollable range when the output voltage is below the peak value of the source voltage [179]. This results in the start-up inrush current. The ideal average model cannot capture this phenomenon therefore, the model developer will also need to add an extra part to model inrush. For the sample system studied here, there are two examples of these converters, the two-level boost rectifier (3ΦAR) and single-phase active rectifiers (1ΦAR). The average boost rectifier power stage in abc coordinates can be realized using Eqn 5-1. However, a diode bridge has to be added in parallel as shown in Fig. 5-3 (right) to generate the inrush current. Fig. 5-5 left shows the current waveform having a huge inrush current of 2kA, which has to be eliminated by adding a precharge circuit. The precharge circuit consists of a resistor (R_{pc}) in parallel to an ideal switch at the dc link as shown in Fig. 5-3. Fig. 5-5 right shows resultant current with the precharge circuit added.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc} \qquad \& \qquad i_{dc} = i_a d_a + i_b d_b + i_c d_c \qquad \text{Eqn 5-1}$$

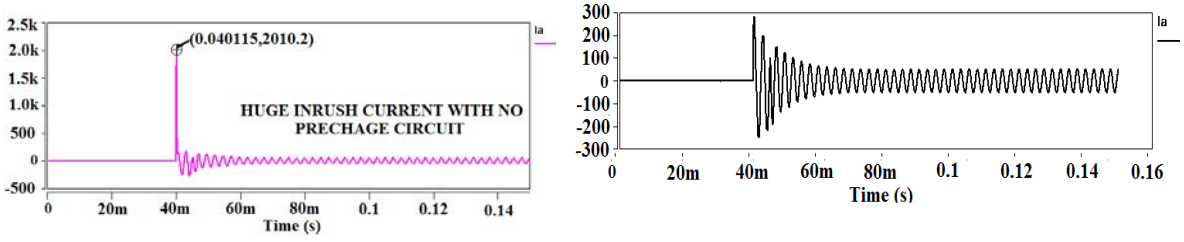


Fig. 5-5 Phase A current with inrush (left) & with precharge circuit (right).

Operating in a no load condition

Another transient phenomenon that is not related to the type of model (whether average or switching model) but needs to be considered is the operation of the model in a no load case. Most converters are followed with an LC filter and when there is no load, there would be a huge overvoltage that is stored in the capacitor and could destroy it. Therefore, a precharge circuit is required to avoid any overvoltage. An example of that in this system is in the multi-pulse transformer rectifier model where the dc link voltage in the no load case with no precharge circuit has an overvoltage of 200V. While with the precharge circuit added, this overvoltage disappears as shown in Fig. 5-6.

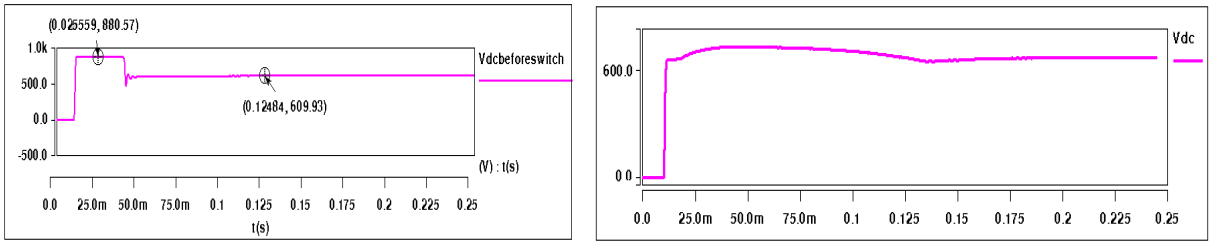


Fig. 5-6 DC link voltage without a precharge circuit and with one respectively.

In addition to this transient behavior, the average models used can capture some low frequency harmonics that are only seen in switching models. From these low frequency harmonics phenomena are the dead time effect, the distortion due to the inherent characteristics of the switching devices such as the voltage drop, the output voltage transition slope and the turn on/off time and finally due to the minimum pulse width. The details of these new results are explained in Chapter 3.

5.3.2. Subsystem connections

There are some issues that could arise when different subsystems are connected together. Some of these issues are system problems and don't rely on the type of models used. From these issues is the sharp change in one parameter or instant connection of a

subsystem. This phenomenon is seen clearly in this type of system studied because of the combination of the different models. For example, in the multi-pulse transformer rectifier model since it is a mathematical function model, many functions like square root, trigonometric functions are used. These functions result in the abrupt change that usually leads to a system crash. Therefore, a valid solution is to add a filter with a high bandwidth to smooth the change without affecting the system characteristics.

In addition when different models with various characteristics are connected together, they may interact or reflect on each other. For example, in this system distortions arose on the ac bus due to the switching converters. This required adding filters in the GEN in Fig. 5-1 to clean those unnecessary distortions. This phenomenon is a physical system one, since the generator control unit (GUC) will not work properly if low pass filters weren't added in the regulation loop (V_{gen} in Fig. 5-1). Fig. 5-7 shows the waveforms for the output voltage of the generator with and without the filter.

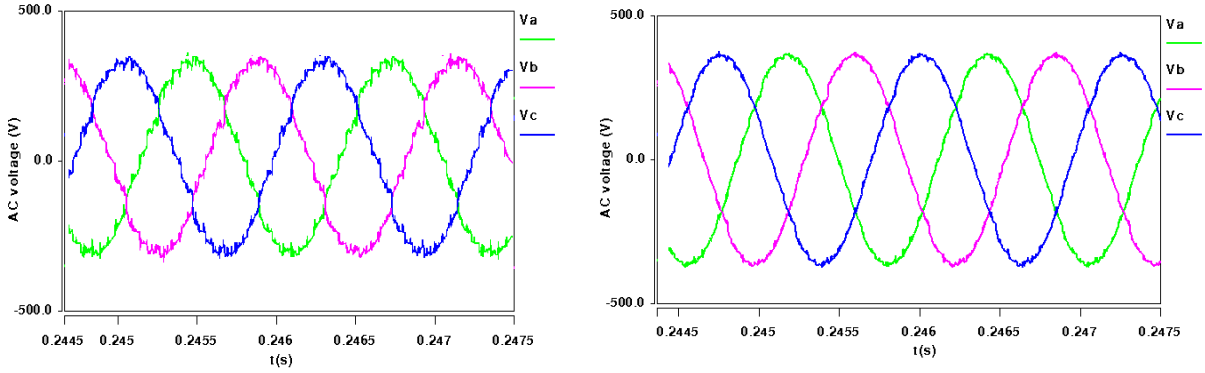


Fig. 5-7 Generator output voltage without and with filter respectively.

5.3.3. System grounding

For any simulator to run the system it has to have a ground node, however, for some models the realistic operation should actually be floating. Therefore, in order to solve this problem, literature usually uses high impedances to ground. This is not always a good solution especially inside the models because it can create a different path through the ground, which may be incorrect. An example of this was seen in this system for the boost

rectifier, where an RC high impedance network was added to ground on the dc link as shown in Fig. 5-1 with "avoid". This high impedance caused resonance, which doesn't actually reflect the real performance of the model as shown in Fig. 5-8.

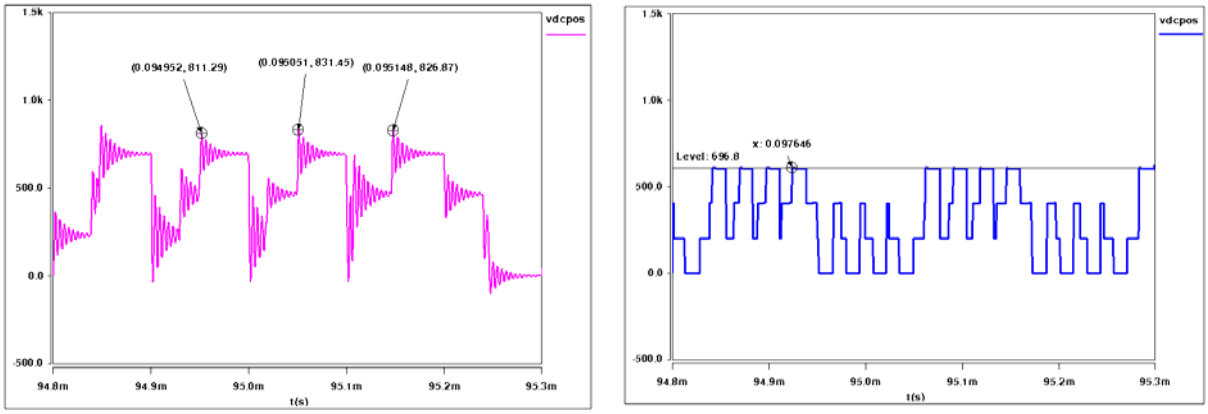


Fig. 5-8 Positive dc link voltage to ground at the output of the two level boost rectifier.

However, for the model to run, there must be a connection between the output and the input. For the 3ΦAR case, this was implemented using the resistors R_g where each ideal diode has a resistor in parallel to it of the magnitude of mega ohms to represent the physical real system as shown in Fig. 5-3. The high impedance problem is also common on the system level modeling since sometimes a user adds high impedance grounding on the buses to avoid numerical convergence. It might help but can cause unrealistic scenarios in the system. A solution for this issue is to add a small series resistance in the wires to provide the needed damping but not affect the system itself as shown in Fig. 5-1.

5.4. Switching Versus Low Frequency Large Signal Models System

Fig. 5-9 shows the block diagram for the system used in comparing the performance of the switching models system to the low frequency large signal models system. The system as shown in the figure below consists of a synchronous generator that is regulated from the ac bus and feeds different loads. There are three main branches fed by the generator. The first is a multi-pulse transformer rectifier (MPTR) that converts the

generator ac voltage to dc voltage and feeds two 100 kW motor controllers. The second branch is a 25 kW two-level boost rectifier feeding a small motor controller and finally the last branch is a three phase step down transformer that is feeding small 3.3kW power factor correction circuits. Both systems are simulated in Saber and their performance is compared. It is found that the LFLS models system takes 4.83min versus the switching models system that takes 115 min to simulate 0.2s simulation time. This means the LFLS system is around 23 times faster than the switching system. In addition, there are several simulation parameters that need to be adjusted in Saber in order to ensure a robust simulation process, namely the time step that is chosen 100 times less than the converters switching frequency, the number of target iterations and the truncation error which are chosen from the algorithm selection and calibration parts respectively. The latter ones has an effect of reduction of the time steps as its value increases [186], while the former will affect the overall numerical convergence. Since the LFLS models system is an improved average, and is not concerned with the high switching frequency, the time step of the simulation can be increased and for this case it is 20μs versus 1μs in the switching system due to the switching frequencies of the converters. And regarding the target iterations, the LFLS system worked with 55 but the switching model needed 400 which means the LFLS system is more robust.

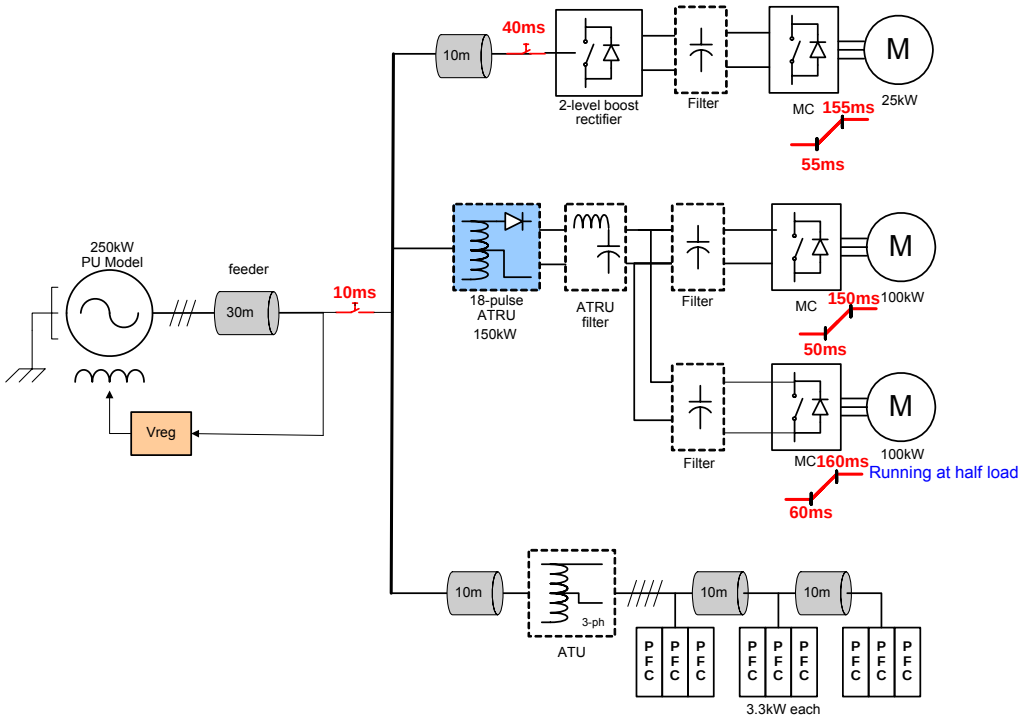


Fig. 5-9 Block diagram for the system used for comparison.

The other benefit of this modeling methodology as mentioned before is being models in a circuit simulator which means there is capability to mix different types of models and see the system performance so switching or average models can be used together depending on the study. The same system in Fig. 5-9 is used to prove this capability. The LFLS model is simulated with changing only the multi-pulse transformer rectifier shown in the blue box to switching model and both systems performance is compared. It can be seen that by changing the MPTR to a switching model, the simulation type is increased to 10.37 min which means its doubled from the pure LFLS system. However, this increase is not bad if compared to the whole switching system so with this capability, one can predict a particular study without the necessity of simulating a large complicated system. Fig. 5-10 shows the three phase input current and the harmonics for each of them and it is found to be around 3%.

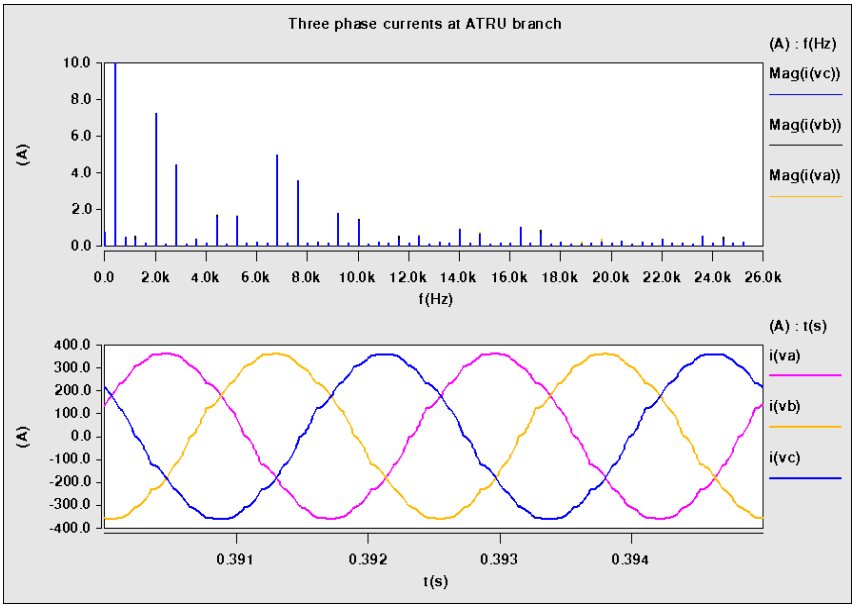


Fig. 5-10 MPTR input current harmonics.

5.5. Regeneration Study

The low frequency large signal (LFLS) models will be used for a regeneration study to validate their correct operation. One of the characteristics of this inverter is being bidirectional which means it has the capability to handle power flow in both directions (source to the load and the opposite). The regenerative mode is a typical mode of operation for flight control actuators. A system is defined in Fig. 5-11 for the bidirectional power flow analysis. The analysis will show the effect of regenerative power flow on the overall system performance characteristics such as dc bus power quality and system efficiency.

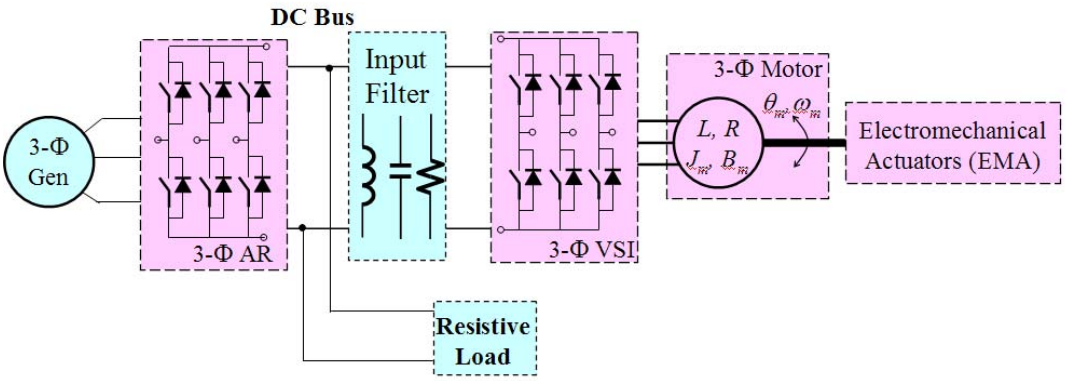


Fig. 5-11 System configuration for bidirectional power flow analysis.

The problem here comes from the fact that the energy coming from a regenerating subsystem tends to raise the dc bus voltage unless this energy is utilized by certain means. When no other load with sufficient power consumption is present at the moment of regeneration, and no measures are taken to utilize that regenerative energy, the dc bus voltage can easily rise beyond allowable power quality limits. This phenomenon may affect normal operation of the system and cause damage to the equipment connected to the bus. There are several possible ways to deal with regenerative energy in the system proposed in literature. From these solutions is:

1. to dissipate it in resistors connected to the bus at the time of regeneration,
2. let it go back to the engine by using the generator and three-phase-to-dc power converter in regenerative mode,
3. use large capacitors in order to store the regenerative energy either in the dc bus, or in the regenerating subsystem,
4. use a DC bus conditioner (a power converter that stores the extra energy from the bus in a large capacitor and returns the energy to the bus when loads are available).

This next section will explain the modified models for the regeneration study and the results.

5.5.1. New models for regeneration study

Electromechanical Actuator

The electromechanical actuator consists of a gearbox and a ball screw mechanism, which transmits motion from the motor to the flight control surface of an aircraft. Fig. 5-12 shows the block diagram representing the model and

Table 5-1 presents the parameters of the model and its description.

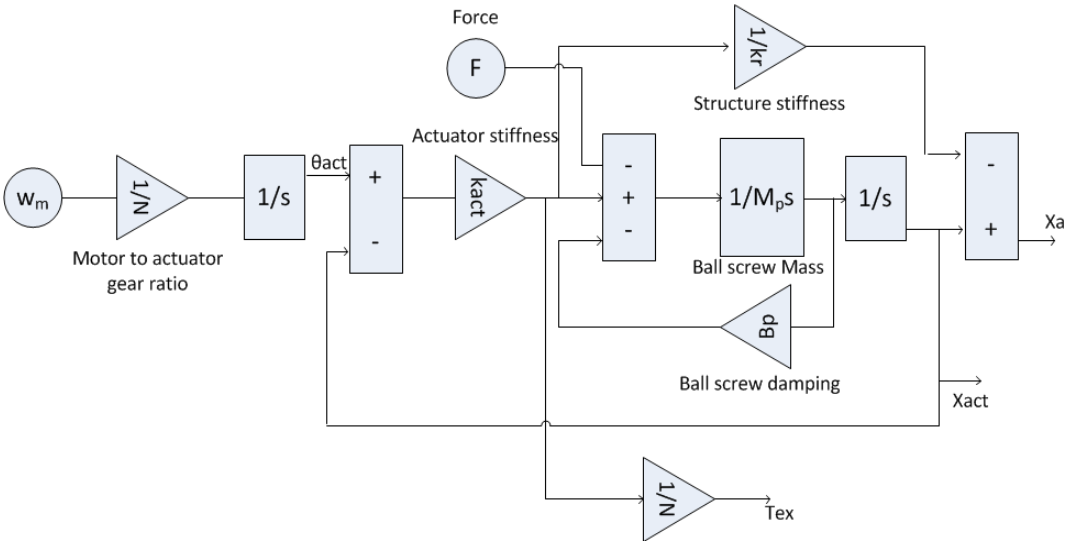


Fig. 5-12 Electromechanical actuator block diagram.

Table 5-1 Electromechanical Actuator Parameters and Description.

Parameters	Description
Force (F)	Load force applied to the actuator from the surface (N)
ω_m	Angular velocity of the motor shaft (rad/s)
T_{ex}	External torque applied to the motor shaft (N.m)
X_a	Effective ball screw displacement (m)
X_{act}	Ball screw position (m)
N	Motor-to-actuator gear ratio
k_{act}	Actuator stiffness (N/m)
k_r	Structure stiffness (kg.m)
Mp	Ball screw mass(kg)
Bp	Ball screw damping(N.s/m)

Surface Dynamics

Surface dynamics is model of aircraft surface displacement mechanism. Fig. 5-13 shows the block diagram representing the model and

Table 5-2 presents the parameters of the model and its description.

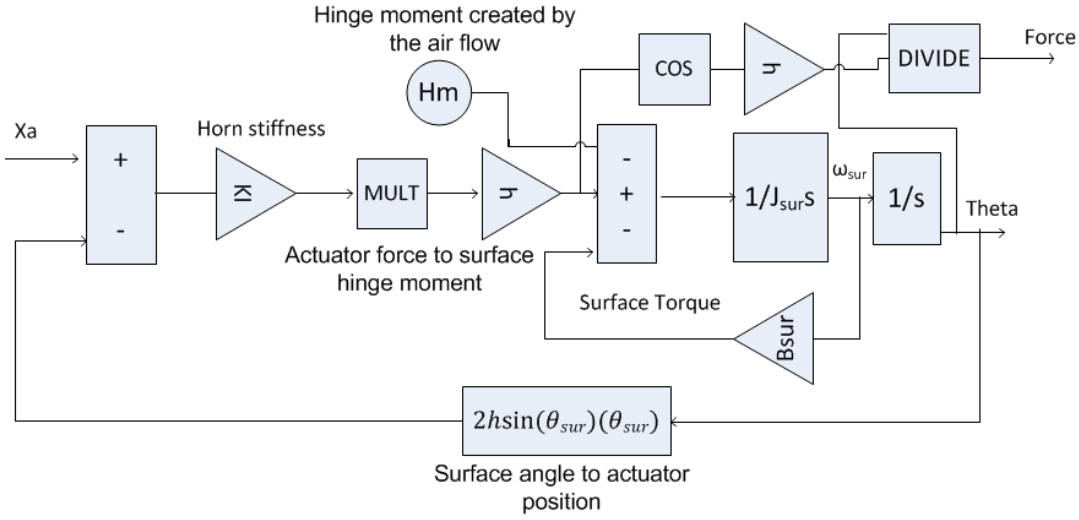


Fig. 5-13 Surface dynamics block diagram.

Table 5-2 Surface Dynamics Parameters and Description.

Parameter	Description
$\mathbf{H_m}$	Hinge moment created by the air flow (N.m)
$\mathbf{X_a}$	Effective actuator displacement (m)
Theta (θ)	Surface position angle (rad)
KI	Horn stiffness(m.kg)
$\mathbf{J_{sur}}$	Surface inertia(m.kg.s^2)
$\mathbf{B_{sur}}$	Surface damping (m.kg.s)
h	Horn radius (m)

5.5.2. Case Study and Results

Fig. 5-14 shows the Saber schematic for the simplified system used for the regeneration study. The system consists of a synchronous generator feeding an active front end (two-level boost rectifier). The electromechanical actuator (EMA) is driven by a three-phase permanent magnet synchronous motor drive. A three-phase DC-AC inverter (motor controller) converts the 650V DC available on the DC bus to the three phase AC voltages required by the motor drive. The control objective is to drive the surface in response to a deflection command θ_{ref} in the presence of a wind load disturbance. The origin of regenerative power is explained in the following.

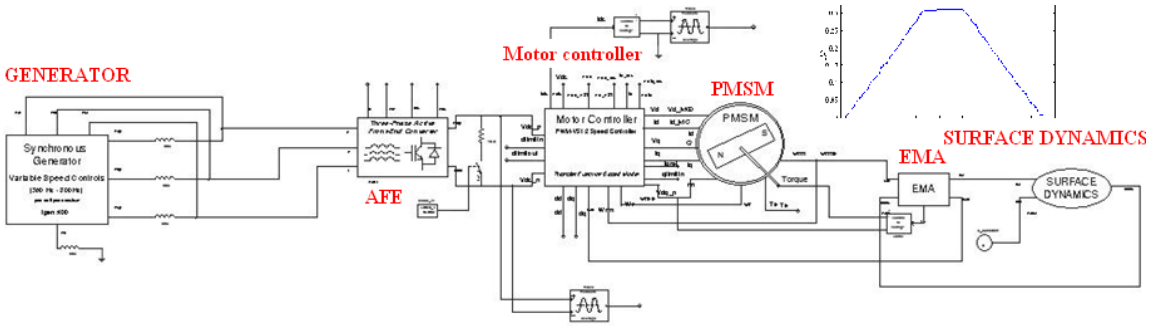


Fig. 5-14 System configuration for regeneration study in Saber.

The simulation results for the above system are shown in Fig. 5-15. A surface deflection command to drive the surface from zero to a given reference position is issued. In response to this command, the motor drive accelerates the control surface to drive θ_s toward θ_{ref}. During the acceleration, the motor draws large power which is for this case around 18 kW. The motor speed steadies at its maximum allowable as the deflection increases linearly in the presence of the wind load. For this simulation results, the wind load is in the same direction as the motor torque. Hence, in order to maintain the linear surface deflection profile, the EMA controller makes the motor acts as a generator, absorb the energy from the wind load and put it back to the DC bus. This is represented by the large negative power which is the regeneration. The same sequence of events is repeated when the surface is commanded to return to its original position.

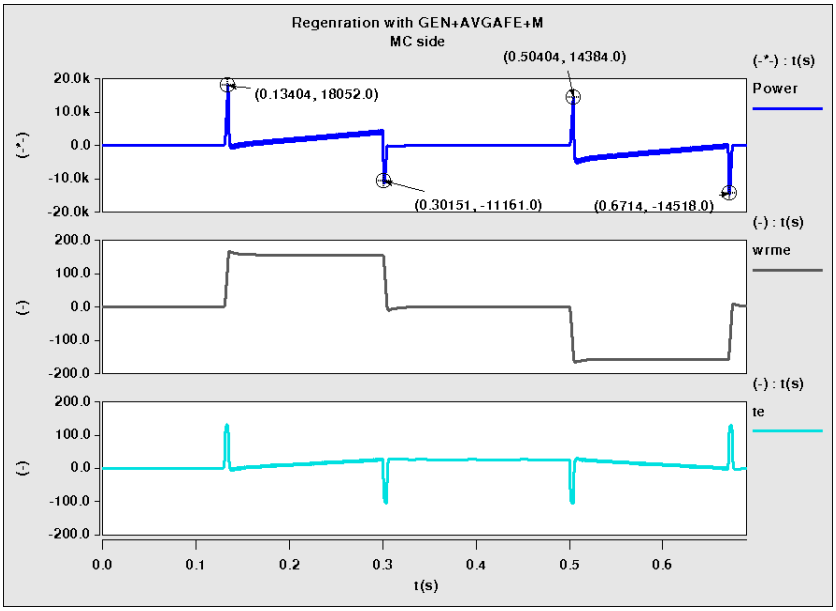


Fig. 5-15 Results on the motor controller side (from top: Power, speed, and electrical torque).

Fig. 5-16 shows the results for the case study on the AFE dc side. It can be seen that when regeneration happens, the dc link voltage increases from 650V to 680V which is around 30V increase. Fig. 5-17 shows the results for the case study on the generator side where one can conclude there is a very small change on the ac bus. This can be because the power of the load is just 10% (25kW) compared to the generator power (250kW). It

can be concluded from this section that the LFLS models are also capable of predicting the regeneration phenomena and can be used for these types of studies.

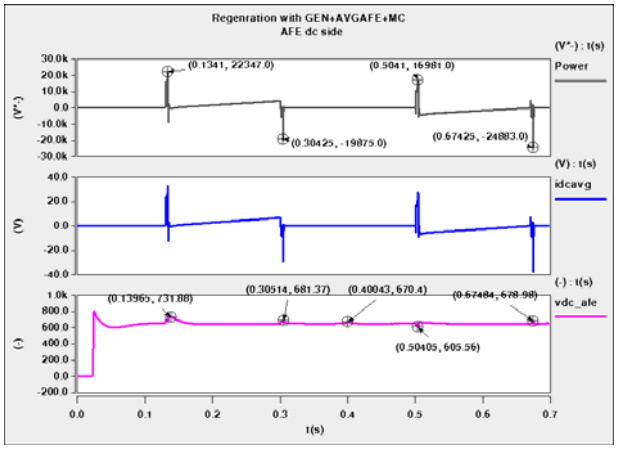


Fig. 5-16 Results on the AFE dc side (from top: Power, dc current, and dc link voltage).

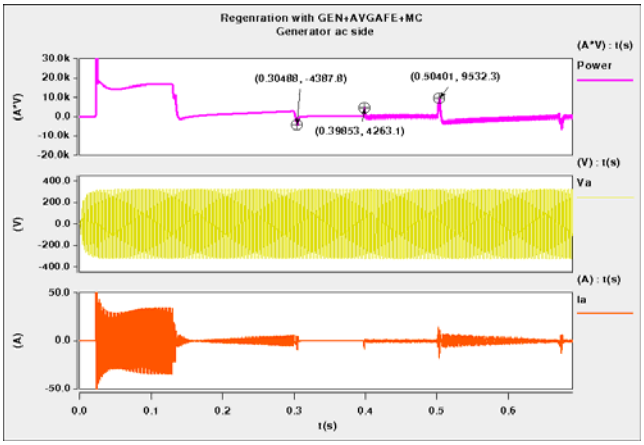


Fig. 5-17 Results on the generator side (from top: Power, phase voltage, and phase current).

Chapter 6 SUMMARY AND FUTURE WORK

This chapter presents the conclusions obtained from this work and also discusses the future work that can be done.

6.1. Summary

This work focused on modeling ac/dc hybrid power systems with large number of power converters, which can be used for a variety of applications like automotive, ship spacecraft or aircraft to be used for stability and power quality analysis. The work examined the different types of models know in literature and emphasized the benefits and drawbacks of each type in regards to the studies needed. This analysis raised a big challenge of developing new types of models that are more accurate, faster and carry enough information needed for these types of studies. These new models are called low frequency large signal (LFLS) models and they are some type of average models that can capture many of the large-signal phenomena that are only seen by the switching models. This work presented one of these LFLS models in detail, a voltage source inverter (VSI), and explained how the model can be modified to capture low frequency harmonics that are usually phenomena modeled only with switching models. The models are implemented in a circuit simulator as electrical circuit based models to be able to combine them with switching models in one system and mix them depending on the application of the system. The system is capable of capturing the real transient behavior of the system, such as the startup, inrush current and power flow directionality, in addition to some low-frequency harmonic distortion phenomena.

After these models were implemented, they had to be evaluated to understand how accurate they are, and what assumptions they undergo, therefore a validation

procedure was developed and applied to one power electronics converter (two-level boost rectifier) of the system as an example.

6.2. Future Work

Some possible ideas for future work continuing the development presented here are discussed in the following paragraphs.

First, more evaluation needs to be done to the frequency characteristics analysis in concern with some of the harmonics (like the 5^{th} harmonic) to get better matching results. There are different things that need to be taken into consideration as mentioned in the dissertation, like the effect of the impedance of the sources and loads. In addition, the small uncertainties in the dead time, passives tolerances which may be causing these discrepancies.

Second, the low frequency large signal (LFLS) model concept can be applied to different topologies for validation; in this dissertation a voltage source inverter working as an inverter and a rectifier was tested but the same concept can be applied to multi-level converters although the type of non-linear phenomena to be added might be different depending on the topology.

Third, more stability analysis and impedance measurement validation can be done, one example is connecting the two converters back to back and studying the interaction both on dc and ac sides.

Fourth, the study can be expanded by adding these low frequency large signal (LFLS) models to a larger system and evaluate the system behavior in comparison with the detailed switching models system.

REFERENCES

[1] A. Emadi and M. Ehsani, "Multi-converter power electronic systems: definitions and applications," in *Proceed. IEEE PESC '01*, vol. 2, pp. 1230−1236, June 2001.

[2] G. Franz, G. Ludwig and R. Steigerwald, "Modeling and simulation of distributed power systems," in *Proceed. IEEE PESC '90*, pp. 606−610, June 1990.

[3] C. C. Chan, "An overview of electric vehicle technology," Proc. of the IEEE, No.81, No.9, pp. 1202-1213, Sep. 1993.

[4] A. Emadi, M. Ehsani, J. M. Miller, *Vehicular electric power systems: land, sea, air, and space vehicles*, Marcel Dekker, 1994.

[5] S. Cutts, "A collaborative approach to the more electric aircraft," in *Proceed. IEE PEMD'02*, pp. 223−228, Apr. 2002.

[6] D. H. Clayton, S. D. Sudhoff, "Electric ship drive and power system," Conf. Record of the 24th International Power Modulator Symposium, pp. 85 - 88, June 2000.

[7] C. C. Chan, K. T. Chau, "An overview of power electronics in electric vehicles," IEEE Trans. On Industrial Electronics, Vol. 44, No. 1, pp. 3-13.

[8] Y. Hu, J. Tatler, and Z. Chen, "Modeling and Simulation of a Power Electronic Conversion System Using SIMULINK," *Proc. of UPEC'04,* pp. 289–293, 2004.

[9] V. Thottuvelil, and E. Lee, "On some practical aspects of power electronics simulation," in *Proceed. IEEE Computers in Power Electronics*, pp. 157−163, Aug 1994.

[10] P. Duijsen, "Multi-level modeling and simulation of power electronics systems," in *IEEE Trans. on Pow. Elec.*, vol. 4, pp. 347−352, Brighton, UK, Sept. 1993.

[11] A. Gole, A. Keri, et al, “Guidelines for modeling power electronics in electric power engineering application,” *in IEEE Tran. On Power Delivery,* vol. 12, no.1 pp. 505–514, Jan. 1997.

[12] N. Mohan, W. P. Robbins, T. M. Undeland, R. Nilssen, and O. Mo, “Simulation of Power Electronic and Motion Control Systems-An Overview,” *Proc. of 1994 IEEE*, pp.1287–1301, 1994.

[13] H. Li, D. Zhang, M. Steuer, K. Shi, S. Woodruf, "Modeling, simulation and experimental test of a variable-speed cage machine wind generation system," *Computers in Power Electronics, 2004. Proceedings. 2004 IEEE Workshop on* , vol., no., pp. 173- 177, 15-18 Aug. 2004.

[14] B. Lee, and M. Ehsani, “A simplified functional simulation model three-phase voltage-source inverter using switching function concept,” *IEEE Trans. on Ind. Elec.*, vol. 48, no. 2, pp. 309–321, Apr. 2001.

[15] P. Ziogas, E. Wiechmann and V. Stefanovic “A computer aided analysis and design approach for static voltage source inverters,” *IEEE Trans. on Ind. Applicat.*, vol. 21, no. 5, pp. 1234–1241, Sept. 1985.

[16] S. Rosado, R. Burgos, S. Ahmed, F. Wang, and D. Boroyevich, “Modeling of power electronics for simulation-based stability analysis of power systems,” in *Conf. SCS SCSC 2007*, San Diego, CA, July 2007.

[17] D. Maksimovic, A.M. Stankovic, V.J. Thottuvelil, G.C. Verhese, “Modeling and Simulation of Power Electronic Converters,” Proceedings IEEE, Vol. 89, No. 6, June 2001.

[18] B. Cho, F. Lee, “Modeling and analysis of spacecraft power systems,” *IEEE Trans. on Pow. Elec.*, vol. 3, no.1, pp. 44–54, Jan. 1988.

[19] D. Logue, P.T. Krein, "Simulation of electric machinery and power electronics interfacing using MATLAB/SIMULINK," *Computers in Power Electronics, 2000. COMPEL 2000. The 7th Workshop on* , vol., no., pp.34-39, 2000.

[20] K. Karimi, A. Booker, and A. Mong, "Modeling, simulation and verification of large dc power electronics systems," in *Proceed. IEEE PESC '96*, vol. 2, pp. 1731–1737, June 1996.

[21] W. Shi, T. Tang, J. Yang, "Simulation of a large marine container ship power system," *SICE 2004 Annual Conference* , vol.1, no., pp. 39- 44 vol. 1, 4-6 Aug. 2004.

[22] R. Nelms, B. Evans, and L. Grigsby, "Simulation of ac spacecraft power systems," *IEEE Trans. on Ind. Elec.*, vol. 36, no. 3, pp. 398–402, Aug. 1989.

[23] A. Emadi, M .Ehsani, "Aircraft power systems: technology, state of the art, and future trends," *Aerospace and Electronic Systems Magazine, IEEE* , vol.15, no.1, pp.28-32, Jan 2000.

[24] M. Jalla, A. Emadi, G. Williamson, and B. Fahimi, "Modeling of multi-converter more electric ship power systems using the generalized state space averaging method," *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE* , vol.2, no., pp. 1514- 1519 Vol. 2, 2-6 Nov. 2004.

[25] M. Jalla, A. Emadi, G. Williamson, and B. Fahimi, "Real time state estimation of multi-converter more electric ship power systems using the generalized state space averaging method," *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE* , vol.2, no., pp. 1514- 1519 Vol. 2, 2-6 Nov. 2004.

[26] A. Nasiri, and A. Emadi, "Modeling, simulation, and analysis of active filter systems using generalized state space averaging method," *Industrial Electronics*

Society, 2003. IECON '03. The 29th Annual Conference of the IEEE , vol.3, no., pp. 1999- 2004 Vol.3, 2-6 Nov. 2003.

[27] T. Skvarenina, S. Pekarek, O. Wasynczuk, P. Krause, R. Thibodeaux, J. Weimer, "Simulation of a More-Electric Aircraft power system using an automated state model approach," *Energy Conversion Engineering Conference, 1996. IECEC 96. Proceedings of the 31st Intersociety* , vol.1, no., pp.133-136 vol.1, 11-16 Aug 1996

[28] J. Lee, B. Cho, S. Kim, and F. Lee, "Modeling and simulation of spacecraft power systems," *Aerospace and Electronic Systems, IEEE Transactions on* , vol.24, no.3, pp.295-304, May 1988.

[29] V. Thottuvelil, and E. Lee, "On some practical aspects of power electronics simulation," in *Proceed. IEEE Computers in Power Electronics*, pp. 157–163, Aug 1994.

[30] A. Beuret, Fk. Bordry, and H. Seran, "Power converter simulation – power and control domain," in *IEEE Fifth European Conf.,* vol. 2, pp. 77–82, Sept. 1993.

[31] B. Needham, P. Eckerling, and K. Siri, "Simulation of large distributed dc power systems using averaged modeling techniques and the saber simulator," in Proceed. *IEEE APEC'94*, vol. 2, pp. 801–807, Orlando, FL, Feb. 1994.

[32] K. J. Karimi, S. J. Fu, "Modeling and Simulation of Space Station Laboratory Module Electric Power System," in *Conf. AIAA'94*, 1994.

[33] A. Hefner, "Modeling power semiconductor devices for realistic simulation," *Computers in Power Electronics, 1994., IEEE 4th Workshop on* , vol., no., pp.11-44, 7-10 Aug 1994.

[34] Y. Hu, J. Tatler, and Z. Chen, “Modeling and Simulation of a Power Electronic Conversion System Using SIMULINK,” *Proc. of Universities Power Engineering Conference* p. 289–293, 2004.

[35] A. Ba-Razzouk, A. Pittet, A. Cheriti, V. Rajagopalan, "SIMULINK based simulations of power electronic systems," *Computers in Power Electronics, 1994., IEEE 4th Workshop on* , vol., no., pp.105-108, 7-10 Aug 1994

[36] A. Ouroua, L. Domaschk, and J. Beno, "Electric ship power system integration analyses through modeling and simulation," *Electric Ship Technologies Symposium, 2005 IEEE* , vol., no., pp. 70- 74, 25-27 July 2005.

[37] V. Rajagopalan, "Computer-Aided Analysis of Power Electronic Systems," *Industrial Electronics Society, 1988. IECON '88. Proceedings., 14 Annual Conference of* , vol.3, no., pp.528-533, 24-28 Oct 1988.

[38] V. Rajagopalan, "Modeling and simulation of power electronic converters for power supplies," *Industrial Electronics, Control, and Instrumentation, 1995., Proceedings of the 1995 IEEE IECON 21st International Conference on* , vol.1, no., pp.27-32 vol.1, 6-10 Nov 1995.

[39] S. Salama, "Simulation of power electronics systems using "SimuPec": the new power electronics toolbox for "Simulink/Matlab"," *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* , vol.5, no., pp. 3409- 3413 Vol.5, 20-25 June 2004.

[40] Y. Kang, and J. Lavers, "Power electronics simulation: current progress and future development," *Computers in Power Electronics, 1994., IEEE 4th Workshop on* , vol., no., pp.169-174, 7-10 Aug 1994.

[41] S. Rosado, “Voltage stability and control in autonomous electric power systems with variable frequency”, PhD. Dissertation, Virginia Tech, 2007.

[42] A. Emadi, "Modeling of power electronic loads in AC distribution systems using the generalized State-space averaging method," *Industrial Electronics, IEEE Transactions on* , vol.51, no.5, pp. 992- 1000, Oct. 2004.

[43] R. Spee and A. K. Wallace, "Remedial strategies for brushless dc drive failures," *IEEE* Trans. on Industry *Applic*., 26(2):259-266, March/April 1990.

[44] R.L.A. Ribeiro, E.R.C. da Silva, and etal, "Fault Detection in Voltage-Fed PWM Motor Drive Systems" *Elec. Machines and Sys. For MEA*, IEE Colloquium, pp. 1/1−1/4, Nov. 1999.

[45] Hang-Seok Choi and D.Y Huh, "Protection Schemes for Various Fault Conditions for Off-line Flyback Converters," *IEEE PESC*, pp. 4355−4359, 2004.

[46] E.A. Ebrahim and N. Hammad, "Fault analysis of current-controlled PWM-inverter fed induction-motor drives," *Proc. of the 7th International Conference on Properties and Applications of Dielectric Materials*, pp. 1065-1070, Nagoya, June 2003.

[47] A. Merdassi, L. Gerbaud, S. Bacha, "A new automatic average modeling tool for power electronics systems," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp.3425-3431, 15-19 June 2008

[48] R. Bass, P. Krein, "Large signal design alternatives for switching power converter control," *Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE* , vol., no., pp.882-887, 24-27 Jun 1991.

[49] F. Lee, "Power converter modeling and control," Class notes, Virginia Tech, 2006.

[50] R. Middlcbrook and S. Cuk. “A general unified approach to modeling switching-converter power stages.” In *IEEE Power Electronics Specialists conf. Rec* .. 1976. pp. 18-34.

[51] B. Lehman, R. Bass, "Switching frequency dependent averaged models for PWM DC-DC converters," *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE* , vol.1, no., pp.636-642 vol.1, 18-22 Jun 1995.

[52] P. Krein, R. Bass, "A new approach to fast simulation of periodically switching power converters," *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE* , vol., no., pp.1185-1189 vol.2, 7-12 Oct 1990.

[53] P. Krein, J. Bentsman, R. Bass, B. Lesieutre, "On the use of averaging for the analysis of power electronic systems," *Power Electronics, IEEE Transactions on*, vol.5, no.2, pp.182-190, Apr 1990.

[54] B. Lehman, R. Bass, "Recently developed averaging theory applied to power electronic systems," *American Control Conference, 1994* , vol.2, no., pp. 1563-1567 vol.2, 29 June-1 July 1994.

[55] B. Lehman, R. Bass, "Extensions of averaging theory for power electronic systems," *Power Electronics, IEEE Transactions on* , vol.11, no.4, pp.542-553, Jul 1996.

[56] B. Lehman, R. Bass, "Recent advances in averaging theory for PWM DC-DC converters," *Decision and Control, 1996., Proceedings of the 35th IEEE* , vol.4, no., pp.4467-4471 vol.4, 11-13 Dec 1996.

[57] S. Sanders, J. Noworolski, X. Liu, and G. Verghese, "Generalized averaging method for power conversion circuits," *Power Electronics, IEEE Transactions on* , vol.6, no.2, pp.251-259, Apr 1991.

[58] R. Thurston, S. Legowski, "A simple and accurate method of computing average and RMS currents in a three-phase PWM inverter," *Power Electronics, IEEE Transactions on* , vol.8, no.2, pp.192-199, Apr 1993.

[59] M. Hengchun, D. Boroyevich, F. Lee, "Novel reduced-order small-signal model of three-phase PWM rectifiers and its application in control design and system analysis," *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE* , vol.1, no., pp.556-562 vol.1, 23-27 Jun 1996.

[60] S. Hiti, D. Boroyevich, and C. Cuadros, "Small-signal modeling and control of three-phase PWM converters," *Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE* , vol., no., pp.1143-1150 vol.2, 2-6 Oct 1994.

[61] K. D. T. Ngo, "Low frequency characterization of PWM converters," *IEEE Trans. Power Electron*.," vol. PE-1, 1986. pp. 223-230.

[62] C. Rim, D. Hu, G. Cho, "Transformers as equivalent circuits for switches: general proofs and D-Q transformation-based analyses," *Industry Applications, IEEE Transactions on* , vol.26, no.4, pp.777-785, Jul/Aug 1990.

[63] R. Wang, and J. Liu, "Redefining a New-Formed Average Model for Three-Phase Boost Rectifiers/Voltage Source Inverters," *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE* , vol., no., pp.1680-1686, 15-19 Feb. 2009.

[64] R. Ridley, "A new small-signal model for current-mode control," PhD. Dissertation, Virginia Tech, Nov. 1990.

[65] W. Tang, F. Lee, R. Ridley, "Small-signal modeling of average current-mode control," *Power Electronics, IEEE Transactions on* , vol.8, no.2, pp.112-119, Apr 1993.

[66] D. O'Sullivan, H. Spruyt, A. Crausaz, "PWM conductance control," *Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE* , vol., no., pp.351-359 vol.1, 11-14 April 1988.

[67] P. Krein, R. Bass, "Autonomous control technique for high-performance switches," *Industrial Electronics, IEEE Transactions on* , vol.39, no.3, pp.215-222, Jun 1992.

[68] A. Kislovski, "Small-signal, low-frequency analysis of a buck type PWM conductance controller," *Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE* , vol., no., pp.88-95, 11-14 Jun 1990.

[69] S. Hiti, S., D. Borojevic, R. Ambatipudi, R. Zhang, J. Yimin, "Average current control of three-phase PWM boost rectifier," *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE* , vol.1, no., pp.131-137 vol.1, 18-22 Jun 1995.

[70] O. Castillo, E. Amoros, G. Sanfeliu, and L. Morales, "Average Current Mode Control of Three-Phase Boost Rectifiers with Low Harmonic Distortion Applied to Small Wind Turbines," *Electronics, Robotics and Automotive Mechanics Conference, 2009. CERMA '09.* , vol., no., pp.446-451, 22-25 Sept. 2009

[71] D. Brod, and D. Novotny, "Current Control of VSI-PWM Inverters," *Industry Applications, IEEE Transactions on* , vol.IA-21, no.3, pp.562-570, May 1985

[72] K. Zhou, and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis [three-phase inverters]," *IEEE Trans on Indus Elect*, vol.49, no.1, pp.186–196, Feb 2002.

[73] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans on Indus Appl.,* vol.33, no.3, pp.756–764, May/Jun 1997.

[74] S. R. Bowes, “New sinusoidal pulsewidth modulated inverter,” *Proc. Inst. Elect. Eng.*, vol. 122, pp. 1279–1285, 1975.

[75] J. A. Houldsworth and D. A. Grant, “The use of harmonic distortion to increase the output voltage of a three-phasePWMinverter,” *IEEE Trans. Ind. Applicat.*, vol. 20, pp. 1224–1228, Sept./Oct. 1984.

[76] J. Holtz, “Pulsewidth modulation for electronic power conversion,” *Proc. IEEE*, vol. 82, pp. 1194–1214, Aug. 1994.

[77] V. G. Agelidis, P. D. Ziogas, and G. Joos, “’Dead-band’ PWM switching patterns,” *IEEE Trans. Power Electron.*, vol. 11, pp. 523–531, July 1996.

[78] A. Trzynadlowski and S. Legowski, “Minimum-loss vector PWM strategy for three-phase inverter,” *IEEE Trans. Power Electron.*, vol. 9, pp. 26–34, Jan. 1994.

[79] M. A. Boost and P. D. Ziogas, “State-of-the-art carrier PWM techniques: A critical evaluation,” *IEEE Trans. Ind. Applicat.*, vol. 24, pp. 271–280, Mar./Apr. 1988.

[80] P. D. Ziogas, L. Moran, G. Joos, and D. Vincenti, “A refined PWM scheme for voltage and current source converter,” in *Proc. IEEE PESC’90*, 1990, pp. 977–983.

[81] H. W. v. d. Brocker, H. C. Skudenly, and G. Stanke, “Analysis and realization of a pulse width modulator based on the voltage space vectors,” in *Conf. Rec. IEEE-IAS Annu. Meeting*, Denver, CO, 1986, pp. 244–251.

[82] O. Ogasawara, H. Akagi, and A. Nabel, “A novel PWM scheme of voltage source inverters based on space vector theory,” in *Proc. EPE European Conf. Power Electronics and Applications*, 1989, pp. 1197–1202.

[83] M. Depenbrock, “Pulsewidth control of a 3-phase inverter with nonsinusoidal phase voltages,” in *Proc. IEEE-IAS Int. Semiconductor Power Conversion Conf.*, Orlando, FL, 1975, pp. 389–398.

[84] J. Holtz, “Pulsewidth modulation—A survey,” in *Proc. IEEE PESC’92*, 1992, pp. 11–18.

[85] J. Holtz, W. Lotzkat, and A. Khambadkone, “On continuous control of PWM inverters in the overmodulation range including the six-step mode,” in *Proc. IEEE IECON’92*, 1992, pp. 307–312.

[86] B. K. Bose and H. A. Sutherland, “A high performance pulsewidth modulator for an inverter-fed drive system using a microcomputer,” *IEEE Trans. Ind. Applicat.*, vol. 19, pp. 235–243, Mar./Apr. 1983.

[87] A. M. Hava, R. Kerkman, and T. A. Lipo, “Carrier-based PWM-VSI overmodulation strategies: Analysis, comparison, and design,” *IEEE Trans. Power Electron.*, vol. 13, pp. 674–689, July 1998.

[88] D. W. Chung, J. S. Kim, and S. K. Sul, “Unified voltage modulation technique for real-time three-phase power conversion,” *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 374–380, Mar./Apr. 1998.

[89] A. Munoz-Garcia, and T.A. Lipo, "On-line dead time compensation technique for open-loop PWM-VSI drives," *IEEE APE '98,* vol.1,pp.95−100 vol.1, 15−19 Feb 1998.

[90] J. Choi; S. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Trans. On Pow Elect* , vol.11, no.2, pp.221–227, Mar 1996.

[91] J. Choi; S. Sul, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Trans on Indus Appl.*, vol.31, no.5, pp.1001–1008, Sep/Oct 1995.

[92] C. Attaianese, V. Nardi, and G. Tomasso, "A novel SVM strategy for VSI dead-time-effect reduction," *IEEE Trans on Indus Appl.*, vol.41, no.6, pp. 1667–1674, Nov.-Dec. 2005.

[93] C. Attaianese, D. Capraro, and G. Tomasso, "Hardware dead time compensation for VSI based electrical drives," *IEEE ISIE 2001.*, vol.2, pp.759–764 vol.2, 2001.

[94] Y. Murai, T. Watanabe and H. Iwasaki, "Waveform distortion and correction circuit for PWM inverters with switching lagtimes", IEEE Trans. on Ind. Appl., Vol. 23, No. 5, September-October 1987, pp. 881-886.

[95] F. Blaabjerg and J. K. Pedersen, "Ideal PWM-VSI inverter using only one current sensor in the DC-link", IEE, 5th Power Electronics and Variable-Speed Drives Conference, 1994, pp. 45 8 -464.

[96] Power Electronics and Variable Frequency Drives (book), edited by Bimal K. Bose, IEEE Press, 1996.

[97] R. *Sepe* and J. Lang, "Inverter nonlinearities and discrete-time vector current control", IEEE Trans. on Ind. Appl., Vol. 30, No. 1, January-February 1994, pp. 62-70.

[98] Z. Wu; J. Ying, "A novel dead time compensation method for PWM inverter," *Power Electronics and Drive Systems, 2003. PEDS 2003. The Fifth International Conference on* , vol.2, no., pp. 1258- 1263 Vol.2, 17-20 Nov. 2003.

[99] J. W. Choi and **S.** K. Sul, "Inverter output voltage synthesis using novel dead time compensation", IEEE Trans. on Power Electronics, Vol. 11, No. 2, March 1996, pp. 221-227.

[100] D. Leggate and R. Kerkman, "Pulse based time compensator for PWM voltage inverters", IEEE IECON 1995 Conference, 1995, pp. 474-481.

[101] T. Sukegawa, K. Kamiyama, K. Mizuno, T. Matsui and T. Okuyama, "Fully digital, vector-controlled PWM VSI fed ac drives with an inverter dead-time compensation strategy", IEEE Trans. on Ind. Appl., Vol. 27, No. 3, MaylJune 1991, pp. 552-559.

[102] H. Kubota and K. Matsuse, "The improvement of performance at low speed by offset compensation of stator voltage in sensorless vector controlled induction machines". IEEE IAS 1996 annual meeting, Oct. 1996, pp. 257-261.

[103] J. Seung-Gi, L. Bang-Sup, K. Kyung-Seo, and P. Min-Ho, “The analysis and compensaition of dead time effects,” in *IEEE IECON Con5 Rec.,* 1988, pp. 667--671.

[104] S. J. Jang, S. W. Cho, and S. K. Sul, “Current waveform improvement of PWM inverter,” in *Int. Symp. Power Electron.,* Seoul, 1989, pp. 51-55.

[105] T. Itkonen, and J. Luukko, "Switching-function-based simulation model for three-phase voltage source inverter taking dead-time effects into account," *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE* , vol., no., pp.992-997, 10-13 Nov. 2008.

[106] R. P. Joshi and B. K. Bose, “Base/gate drive suppression of inactive power devices of a voltage-fed inverter and precision synthesis of AC voltage and DC link current waves,” in *IEEE IECON Con5 Rec.,* 1990, pp. 1034-1040.

[107] A. Weschta and W. Weberskirch, “Nonlinear behavior of voltage source inverters with power transistors,” in *EPE Con5 Rec.,* 1989, pp. 533-537.

[108] B. Allard, H. Morel, A. Ammous, and S. Ghedira, "Averaged modeling of power converters including semiconductor device nonlinearities," *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE* , vol.1, no., pp.647-653 vol.1, 17-22 May 1998.

[109] A. Ammous, K. Ammous, M. Ayedi, Y. Ounajjar, and F. Sellami, "An advanced PWM-switch model including semiconductor device nonlinearities," *Power Electronics, IEEE Transactions on* , vol.18, no.5, pp. 1230- 1237, Sept. 2003.

[110] B.A. Welchko, S.E. Schulz, S. Hiti, "Effects and Compensation of Dead-Time and Minimum Pulse-Width Limitations in Two-Level PWM Voltage Source Inverters," *IEEE IAS’06* , vol.2, pp.889–896, 8–12 Oct. 2006.

[111] D.A. Grant, "Technique for pulse dropping in pulse-width modulated inverters," *IEEE Proceed. Elect Power Appl.* , vol.128, no.1, pp.67–72, January 1981.

[112] D. Grant, R. Seidner, "Technique for pulse elimination in pulsewidth-modulation inverters with no waveform discontinuity," *IEEE Proceed. Elect Power Appl.*, vol.129, no.4, pp.205–210, July 1982.

[113] G. Kliman and A. Plunkett, “Development of a modulation strategy for a PWM inverter drive,” in *Conf. Rec. IEEE IAS Annual Meeting, 1975*, pp.915-921.

[114] AIAA (1998), "Guide for the verification and validation of computational fluid dynamics simulations," American Institute of Aeronautics and Astronautics, AIAA-G-077-1998, Reston, VA.

[115] W. Oberkampf, and T. Trucano (2002), "Verification and validation in computational fluid dynamics," *Progress in Aerospace Sciences*, Vol. 38, No. 3, 209-272.

[116] W. Oberkampf, "Verification and validation in computational simulation," *2004 Transport Task Force Meeting*, Salt Lake City, Utah, April 29, 2004.

[117] S. Horowitz, A. Phadke, *Power System Relaying*, 2nd ed., Research Studies Press Ltd., 1995

[118] I. Lazbin, "Analysis of the stability margins of the Space Station Freedom electrical power system," in Proceed. *IEEE PESC'93*, pp. 839–845, June 1993.

[119] R. D. Middlebrook, "Design techniques for preventing input-filter oscillations in switched-mode regulators," in *Proceed. Powercon 5*, pp. A 3.1–A 3.16, May 1978.

[120] F. Lee, Y. Yu, and J. Triner, "Modeling switching regulator power stages with and without zero-inductor-current dwell time," in Proceed. *IEEE PESC'76*, pp. 62–72, June 1976.

[121] F. Lee, R. Iwens, Y. Yu, and J. Triner, "Generalized computer-aided discrete tome modeling and analysis of dc-dc converters," *IEEE Trans. Indust. Elec. Contr. Instrum.*, vol. 26, pp. 58–69, May 1979.

[122] B. Cho, and B. Choi, "Analysis and design of multi-stage distributed power systems," in Proceed. *IEEE INTELEC'91*, pp. 220–226, Nov. 1991.

[123] C. Wildrick, F. Lee, B. Cho, and B. Choi, "A method of defining the load impedance specification for a stable distributed power system," *IEEE Trans. on Pow. Elec.*, vol. 10, no. 3, pp. 280–285, May 1995.

[124] E. Gholdson, K. Karimi, F. Lee, J. Rajagopalan, Y. Panov, and B. Manners, "Stability of large dc power systems using switching converters, with application to the international space station," in Proceed. *Intersociety IECEC'96*, vol. 1, pp. 166–171, Aug. 1996.

[125] K. Karimi, A. Booker, A. Mong, , and B. Manners, "Verification of space station secondary power system stability using design experiment," in Proceed. *Intersociety IECEC'97*, vol. 1, pp. 526–531, July 1997.

[126] S. Hiti, V. Vlatokovic, D. Boroyevich, and F. Lee, "A new control algorithm for three-phase PWM buck rectifier with input displacement factor compensation," *IEEE Trans. on Pow. Elec.*, vol. 2, no. 2, pp. 173–180, Mar. 1994.

[127] S. Hiti, "Modeling and control of three-phase PWM converters," Ph.D. Dissertation, Virginia Tech, July 1995.

[128] V. Vlatkovic, D. Boroyevich, and F. Lee, "Input filter design for power factor correction circuits," *IEEE Trans. on Pow. Elec.*, vol. 11, no. 1, pp. 199–205, Jan. 1996.

[129] H. Mao, D. Boroyevich, A. Ravindra, and F. Lee, "Analysis and design of high frequency three-phase boost rectifiers," in Proceed. *IEEE APEC'96*, vol. 2, pp. 538–544, Mar. 1996.

[130] H. Mao, F. Lee, D. Boroyevich, and S. Hiti, "Review of high-performance three-phase power factor correction circuits," *IEEE Trans. on Ind. Elec.*, vol. 44, no. 4, pp. 437–446, Aug. 1997.

[131] S. Chandrasekaran, D. Boroyevich, and D. Lindner, "Input filter interactions in three phase ac-dc converters," in Proceed. *IEEE PESC'99*, vol. 2, pp. 987–992, June 1999.

[132] S. Chandrasekaran, "Subsystem design in aircraft power distribution systems using optimization," Ph.D. Dissertation, Virginia Tech, http://scholar.lib.vt.edu/theses/, May 2000.

[133] H. Mao, D. Boroyevich, and F. Lee, "Novel reduced-order small-signal model of three-phase PWM rectifier and its application in control design and system analysis," in *Proceed. IEEE PESC '96*, vol. 1, pp. 556–562, June 1996.

[134] H. Mao, D. Boroyevich, and F. Lee, "Novel reduced-order small-signal model of a three-phase PWM rectifier and its application in control design and system analysis," *IEEE Trans. on Pow. Elec.*, vol. 13, no. 3, pp. 511–521, May 1998

[135] M. Belkhayat. *Stability Criteria for AC Power Systems with Regulated Loads*. Ph.D. thesis, Purdue University, Dec. 1997.

[136] M. Belkhayat, O. Wasynczuk, "Stability analysis of ac power systems with regulated electronic loads," in Proceed. *SAE Aerospc. Pow. Sys. Conf.*, doc. no. 981265, Apr. 1998.

[137] A. MacFarlane and I. Postlethwaite, "The generalized Nyquist stability criterion and multivariable root loci," in *Int. Jour. of Control*, vol. 25, pp. 81-127, Jan. 1977.

[138] A. MacFarlane, *Frequency-Response Methods in Control Systems*. IEEE Press, Inc., New York 1979.

[139] I. Postlethwaite and A. MacFarlane, "A complex variable approach to the analysis of linear multivariable feedback systems," in A.V. Balakrishnan and M. Thoma, *Lecture Notes in Control and Information Sciences*, no.12, Springer-Verlag, Berlin 1979.

[140] A. MacFarlane, *Complex Variable Methods for Linear Multivariable Feedback Systems*. Taylor & Francis Ltd., London 1980.

[141] A. MacFarlane, "Return-difference and return-ratio matrices and their use in analysis and design of multivariable feedback control systems," in *Proc. IEE*, no. 117, pp.2037-2049, 1970.

[142] A. MacFarlane and J. Belletrutti, "The characteristic locus design method," in *Automatica*, no. 9, pp. 575-588, 1973.

[143] H. Rosenbrock, *Computer-Aided Control System Design*. Academic Press Inc, New York 1974.

[144] J. Layton, *Multivariable Control Theory*. Peter Peregrinus Ltd., England 1976.

[145] H. Nyquist, "Regeneration theory," *Bell Syst. Tech. Journ.*, vol. 11, pp. 126–147, Jan. 1932.

[146] W. Evans, "Control system synthesis by root locus method," AIEE Trans., vol. 69, pp. 66–69, 1950.

[147] M. Stojic, and D. Siljak, "Generalization of Hurwitz, Nyquist and Mikhailov stability criteria," *IEEE Trans. on Aut. Control*, vol. 10, no. 3, pp. 250–254, July 1965.

[148] W. Brockett, and J. Willems, "Frequency domain stability criteria—Part I," *IEEE Trans. on Aut. Control*, vol. 10, no. 3, pp. 255–261, July 1965.

[149] W. Brockett, and J. Willems, "Frequency domain stability criteria—Part II," *IEEE Trans. on Aut. Control*, vol. 10, no. 4, pp. 407–413, Oct. 1965.

[150] N. Munro, *Modern Approaches to Control System Design*. Peter Peregrinus Ltd. & IEE, New York and London 1979.

[151] M. Safonov, *Stability and Robustness of Multivariable Feedback Systems*. The MIT Press, MA 1980.

[152] I. Postlethwaite, J. Edmunds, and A. MacFarlane, "Principal gains and principal phases in the analysis of linear multivariable feedback systems," *IEEE Trans. on Aut. Control*, vol. 26, no. 1, pp. 32–46, Feb. 1981.

[153] M. Smith, "Matrix fractions and strict system equivalence," *Int. Jour. of Control*, vol. 34, no. 5, pp. 869–883,1981.

[154] M. Smith, "On the generalized Nyquist stability criterion," *Int. Jour. of Control*, vol. 34, no. 5, pp. 885–920,1981.

[155] M. Smith, "Multivariable root-locus behaviour and the relationship to transfer-function pole-zero structure," *Int. Jour. of Control*, vol. 34, no. 5, pp. 885–920,1981.

[156] R. Patel and N. Munro, *Multivariable System Theory and Design*. Pergamon Press, New York 1982.

[157] D. Bell, P. Cook, and N. Munro, *Design of Modern Control Systems*. Peter Peregrinus Ltd., New York 1982.

[158] Y. Hung and A. MacFarlane, "Multivariable Feedback: A Quasi-Classical Approach," in A.V. Balakrishnan and M. Thoma, *Lecture Notes in Control and Information Sciences*, no. 40, Springer-Verlag, Berlin 1982.

[159] G. Pang and A. MacFarlane, "An Expert Systems Approach to Computer-Aided Design of Multivariable Control Systems," in A.V. Balakrishnan and M. Thoma, *Lecture Notes in Control and Information Sciences*, no. 89, Springer-Verlag, Berlin 1987.

[160] J. Maciejoski, *Multivariable Feedback Design*. Addison-Wesley Publishuing Company, Inc., U.K. 1989.

[161] G. Bryant and L. Yeung, *Multivariable Control System Design Techniques: Dominance and Direct Methods*. John Wiley & Sons LTd., England 1996.

[162] K. Morris, *Introduction to Feedback Control.* Academic Press, 2002.

[163] S. Skogestad, and I. Postlethwaite, *Multivariable Feedback Control, Analysis and Design, 2nd Ed*. John Wiley & Sons Ltd., West Sussex, England 2005.

[164] Y Familiant, K. Corzine, J. Huang, and M. Belkhayat, "Ac impedance measurement techniques," in Proceed. *IEEE IEMDC'05*, pp. 1850–857, May 2005.

[165] Y. Familiant. *Ac Impedance Measurement Techniques in Power Systems*. Ph.D. Thesis, University of Wisconsin-Milwaukee, May 2006.

[166] J. Huang, and K. Corzine, "Ac impedance measurement by line-to-line injected current," in Proceed. *IEEE IAS'06*, vol. 1, pp. 300–306, Oct. 2006.

[167] P. Xiao, G. Venayagamoorthy, and K. Corzine, "Impedance identification of integrated power system components using recurrent neural networks," in Proceed. *IEEE ESTS'07*, pp. 48 – 52, May 2007.

[168] J. Huang, K. Corzine, and M. Belkhayat, "Single-phase ac impedance modeling for stability of integrated power systems," in Proceed. *IEEE ESTS'07*, pp. 483–489, May 2007.

[169] P. Xiao, G. Venayagamoorthy, and K. Corzine, "Combined training of recurrent neural networks with particle swarm optimization and backpropagation algorithms for impedance identification," in Proceed. *IEEE SIS'07*, pp. 9–15, Apr. 2007.

[170] P. Xiao, G. Venayagamoorthy, and K. Corzine, "A novel impedance measurement technique for power electronics systems," in Proceed. *IEEE PESC'07*, pp. 955–960, June 2007.

[171] T. Esaka, Y. Kataoka, T. Ohtaka and S. Iwamoto, "Voltage Stability Preventive Control Using a New Voltage Stability Index", *IEEE PowerCon '04*, vol. 1, pp. 344–349, Nov. 2004.

[172] M. Belkhayat, R. Cooley, A. Witulski, "Large signal stability criteria for distributed systems with constant power loads," n *Proceed. IEEE PESC '95*, vol. 2, pp. 1333–8, June 1995.

[173] J.V. Milanovic, T.A. David, "Stability of distribution networks with embedded generators and induction motors," *IEEE Power Engineering Society Winter Meeting*, 2002, vol. 2, pp 1023–1028, Jan. 2002.

[174] S. Rosado, X. Ma, C. Han, F. Wang, and D. Boroyevich, "Model-based digital controller for a variable frequency synchronous generator with brushless exciter," in *Proc. IEEE PESC '05*, pp. 90–95, June 2005.

[175] S. Rosado, "Voltage stability and control in autonomous electric power systems with variable frequency", PhD. Dissertation, Virginia Tech, 2007.

[176] S. Ahmed, "Computer Modeling and Simulation of Power Electronics Systems for Stability Analysis," MS. Thesis, Virginia Tech, 2007.

[177] S. Rosado, R. Burgos, F. Wang, and D. Boroyevich, "Large- and small-signal evaluation of average models for multi-pulse diode rectifiers," in *Conf. IEEE COMPEL'06*, pp. 89−94, Troy, NY, July 2006.

[178] P. M. Anderson, A. A. Fouad, *Power System Control and Stability*, 2nd ed., *IEEE-Press*, Piscataway, NJ, 2003.

[179] G. Moon, and M, Youn, “Start-up inrush current elimination control of new push-pull quantum series resonant rectifier,” in *IEEE Trans. on Pow. Elec.*, vol. 13, no.6, pp. 995–1004, Nov. 1998.

[180] G. Francis, “An Algorithm and System for Measuring Impedance in D-Q Coordinates,” PhD. Dissertation, Virginia Tech, 2010.

[181] M. Belkhayat, R. Cooley, and E. H. Abed, "Stability and dynamics of power systems with regulated converters," 1995 IEEE International Symposium on Circuits and Systems, Vols 1-3, pp.143-145, 1995.

[182] M. Belkhayat, J. Huang, and K. Corzine, “Impedance Measurement Using Line-to-Line Current Injection,” 2008 US patent, 20080084219 http://www.freepatentsonline.com/y2008/0084219.html.

[183] Oberkampf, W. L. and Roy, C. J., *Verification and Validation in Computational Simulation*, to be published by Cambridge University Press, New York, 2009.

[184] Trucano, T. G., Pilch, M., and Oberkampf, W. L., “General Concepts for Experimental Validation of ASCI Code Applications,” SAND2002-0341, Sandia National Laboratories, Albuquerque, NM, 2002.

[185] AIAA, “Guide for the Verification and Validation of Computational Fluid Dynamics Simulations,” AIAA-G-077-1998, American Institute of Aeronautics and Astronautics, Reston, VA, 1998.

[186] L. Goldgeisser, E. Christen, M. Vlach, and J. Langenwalter, “Open ended dynamic ramping simulation of multi-discipline systems,” in *Proceed. IEEE ISCAS’01*, vol. 5, pp. 307–310, 2001.