DYNAMICS AND CONTROL OF SWITCHMODE POWER CONVERSIONS IN DISTRIBUTED POWER SYSTEMS

by

Byungcho Choi

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APPROVED:

Bo H. Cho, Chairman

Fred C. Lee

Dušan Borojević

Milan M. Jovanović

Werner E. Kohler

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Blacksburg, Virginia

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Committee Chairman : Bo H. Cho
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(ABSTRACT)

Comprehensive analysis, modeling, and design techniques are developed for distributed power systems. Dynamic interactions caused by paralleling, stacking, and cascading converter modules are analyzed. Incorporating the effects of all subsystem interactions, systematic design procedures are established in order to optimize the dynamic performance of large-scale distributed power systems.

An advanced three-loop control scheme is developed to optimize the dynamics of multi-module converters. A design-oriented model reduction technique is employed to design power supplies utilizing a stacked configuration of multi-module converters. An unterminated modeling and design approach is proposed to optimize the dynamics of cascaded converter stages, while ensuring the stability and compatibility of the integrated system. Systematic design procedures for intermediate filters are developed.

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CHAPTER 1

INTRODUCTION

It is the purpose of this work to develop comprehensive analysis, modeling, and design techniques for distributed power conversion systems. The results of this study can be used to optimize dynamic performance of large-scale power systems, employing a distributed architecture using multi-module converters.

1.1 BACKGROUND

With rapid advance of VLSI technologies, power supplies for large-scale information processing systems need to meet severe requirements. Modern semiconductor technologies allow information processing systems to implement more functions in less space, resulting in an extremely high integration density. This ever increasing integration density results in a dramatic increase in power consumption, while supply voltages for high-speed VLSI circuitry have been continually reduced [B1]. As a result, many information processing systems require power systems which must provide hundreds or thousands of amps of current at voltages of five volts or less, with stringent dc regulation specifications. Furthermore, as the functional density of an information processing system expands, the reliability of the power system becomes more critical. For mainframe computers and telecommunication equipment, interruptions of the system operation due to the failure of their power supplies are no longer acceptable.

A conventional centralized power system architecture, featuring a single high-current low-voltage power supply connected to its loads through long distribution cables, is no longer practical for modern VLSI applications. A centralized power system suffers from low conversion efficiency, poor dc regulation, low power density, and excessive losses in distribution cables. More significantly, in a centralized architecture, system failure is often caused by excessive current stress on its switching devices. Even with conservative designs, power line anomalies may cause device failures, resulting in the shut-down of an entire power system.

As a viable solution to demanding power requirements, power supplies for large-scale VLSI applications employ multi-module converters [A1-A10] along with a distributed power system architecture [B1-B10,B20]. The use of multi-module converters allows efficient processing of high current and built-in redundancy. With current-mode control [D1-D2,D7,D8], the output current of a multi-module converter is equally distributed among parallel modules, thereby improving reliability and reducing current stress on switching devices [A8-A10]. Furthermore, the parallel processing of the load current provides fault-tolerance for the system against the failure of a single module.

The use of a distributed power system architecture, featuring cascaded stages of converters distributed throughout the power system, offers high conversion efficiency at low voltages, tight dc regulation, high power density, and improved dynamic performance [B1-B10,B20]. For low voltage applications, a distributed architecture significantly improves the overall conversion efficiency by using a relatively high voltage for the distribution bus. Also, the proximity of the converters to their loads offers good dc

regulation. Lastly, breaking the power processing down into several smaller conversion stages allows the use of high-frequency converters, improving the power density and dynamic performance.

A more advanced architecture is necessary for mainframe computer power systems to meet extreme demands [B20,C1-C4]. In an innovative power system developed for the IBM390 mainframe computer, the system employs a stacked configuration of three multi-module converters to produce five ultra low-voltage ($0.7 \sim 3.6\,V$) and ultra high-current ($2000 \sim 3000\,A$) outputs for high-density emitter coupled logic circuits [C2,C4]. This stacked power system architecture offers improvement of overall efficiency and production of five ultra low-voltage outputs using only three single-output converters.

The ever increasing size and complexity of power systems presents many new analysis and design challenges in order to ensure the system stability and to optimize the dynamic performance of the system. Even though the dynamics of individual converter module are well understood [D1-D11], a comprehensive system level analysis is essential to understand the overall system behavior and to design the system properly.

The dynamics of a converter operating as a subsystem of a large-scale power system are markedly different from those of a stand-alone converter. The parallel operation of converter modules introduces various interactions between converter modules [A11-A13]. The series operation of stages of converters causes significant impacts on the dynamics of each converter stage [B11-B19]. Furthermore, the stacked configuration of converters introduces complicated interaction between stacked converters and their associated loads. These numerous subsystem interactions must be systematically character-

ized and properly incorporated in designing converter modules. Otherwise, even though each converter module might be properly designed for its stand-alone operation, the entire system could result in an unacceptable performance or even instability [B17-B19].

1.2 MOTIVATION AND OBJECTIVE OF STUDY

Recently, remarkable advances have been made in the modeling, analysis, and control of switchmode power converters [D1-D11]. However, much of the current research found in the literature is focused on the dynamics and control of a single stand-alone converter. A successful adaptation of these existing techniques to complex distributed power systems requires two prerequisites. The first is the characterization of subsystem interactions and incorporation of their impacts into the design of each converter module. The second is the development of a reduced order model, which makes the design problem tractable while retaining all prominent features of the system. Any design attempt not furnished with these prerequisites would result in a power system with unacceptably poor dynamics or even instability problem.

The objective of this study is to develop comprehensive modeling, analysis, and design techniques for distributed switchmode power conversion systems. The results of this study can be used to optimize dynamic performance of large-scale power systems, employing a distributed architecture using multi-module converters. Throughout this study, emphases are placed on analysis of subsystem interactions, reduced order modeling, and development of advanced control schemes: all together are indispensable for the design optimization of complex distributed power systems. It is also intended to maximize the utilization of existing analysis and design techniques for stand-alone converters, by properly incorporating the effects of dynamic interactions caused by paralleling, stacking, and cascading converter modules.

1.3 OUTLINE OF DISSERTATION

To achieve the objective of this study, research efforts are centered on three areas: modeling and design of multi-module converters, analysis and design of stacked power supplies, and modeling and design of cascaded converters. The results of these studies can be individually used to optimize the dynamics of multi-module converters, stacked power supplies, and cascaded converters. However, more significantly, they can be collectively used to optimize the dynamics of large-scale power systems employing a distributed architecture using multi-module converters.

Chapter 2 covers modeling and design issues involved with paralleling several converter modules. Guidelines to select a proper scheme of paralleling converter modules are established. A general modeling and design methodology is developed for multi-module converters.

A reduced-order model is developed to simplify the analysis and design of multi-module converters. The reduced-order model has the structure of a conventional single-module converter, while preserving the dynamics of the original multi-module converter. Using this model, any control scheme developed for a single-module converter can be directly adapted to a multi-module converter. Furthermore, multi-module converters operating as subsystems of a large-scale power system can be replaced with the reduced-order models without compromising any analysis accuracy.

A three-loop control scheme is developed to overcome the limitations of the two-loop current-mode control for multi-module converters with a secondary LC filter. In addition to output voltage and inductor current feedback, the control scheme employs

feedback from the output capacitor of each module (the summing point where all modules are merged) to improve the transient response in the event of failure of a module, by compensating for the undesirable effects of the secondary LC filter.

Chapter 3 deals with analysis and design issues involved with stacking several converters to power multiple loads. Based on a comprehensive system level analysis, this chapter presents systematic design procedures for staked power systems, which naturally incorporate all subsystem interactions and optimize the overall performance of the entire system.

First, an effective load impedance of each converter is identified, incorporating all subsystem interactions. Second, using the effective load impedances, the system is decomposed into individual converters. Third, the effective load impedance of the decoupled converter is simplified to a resistive value (equivalent resistive load). Finally, the control design of each decoupled converter is designed individually using its equivalent resistive load. It is shown that this design procedure offers an optimal dynamic performance for the entire system.

Chapter 4 addresses modeling and design issues involved with cascading several stages of converters and intermediate filters. A methodology of analyzing the system stability and degree of interactions between two cascaded subsystems is discussed. An unterminated modeling and design approach is proposed to optimize the dynamics of the cascaded converter stage independently from its load dynamics, while ensuring the stability and compatibility of the integrated system.

This chapter also covers design considerations for intermediate filters employed between two cascaded converter stages. A design strategy to minimize interactions at both sides of the filter is presented. The design strategy is substantiated by step-by-step design procedures for both single-stage and two-stage filters.

Chapter 5 presents the conclusions of this dissertation. This chapter also briefly discusses the use of this dissertation to optimize the dynamics of various distributed power systems.

CHAPTER 2

MULTI-MODULE CONVERTER SYSTEMS

2.1 INTRODUCTION

Multi-module converters play an essential role in modern switchmode power conversion systems. Many large-scale distributed power systems utilize multi-module converters as integral subsystems to process high currents efficiently and reliably [B1,B3,B6,B10-B22]. Also, multi-module converters are widely used in various open-ended architectures for high-current applications due to their distinctive advantages over conventional single-module converters [A1-A10].

While the benefits and dc characteristics of multi-module converters are well understood, there are several issues to be addressed in the modeling and design of multi-module converters. The converter paralleling scheme must be selected taking the complexity, modularity, and redundancy of the system into consideration. Various interactions among converter modules must be incorporated into the control design to ensure the stability and a good dynamic performance. It is necessary to develop a reduced order model for multi-module converters, in order to simplify the control design and to facilitate the analysis of large-scale power systems employing multi-module converters as subsystems.

This chapter presents modeling, analysis, and design techniques for multi-module converters. Section 2.2 discusses several different schemes of paralleling converter mod-

ules. Section 2.3 addresses issues related to the current distribution among non-identical converter modules. Section 2.4 presents a reduced order modeling for multi-module converters which greatly simplifies the analysis and design. This section also presents control design procedures for multi-module converters using the reduced order model. Section 2.5 discusses the limitations of the two-loop current-mode control for multi-module converters with a multi-stage output filter, and it proposes an advanced three-loop control scheme to overcome the limitations of current-mode control.

2.2 PARALLELING SCHEMES OF CONVERTER MODULES

There are many different ways to parallel converter modules, with respective advantages and limitations. Figure 2.1 shows three different configurations for a two-module boost converter, each with two current-mode controlled boost modules in parallel.

Figure 2.1(a) shows the simplest configuration, where each module contains a converter power stage (without the output capacitor), a pulse width modulation (PWM) block, and a current sensing network (CSN) for current-mode control. Two identical modules are combined with the common output capacitor and voltage feedback circuit, forming a complete two-module regulator. This configuration is not suitable for open-ended applications that require flexible number of modules to accommodate the output power variation. As discussed in [A12,B12], the performance of this configuration is sensitive to the number of modules. Although the converter can be properly designed for a fixed number of modules, the closed-loop performance of the system becomes worse as the number of modules increases. Also, the addition of an extra output capacitor by user (necessary for high current applications using this configuration) requires a redesign of the control. The control optimized for a relatively small output capacitor could experience a severe performance degradation with an increased output capacitor. As demonstrated in [B21], both crossover frequency and phase margin of the loop gain can be significantly reduced with a larger output capacitor. In this case, it will be necessary to redesign the control loop, and major benefits of the modular approach will be lost.

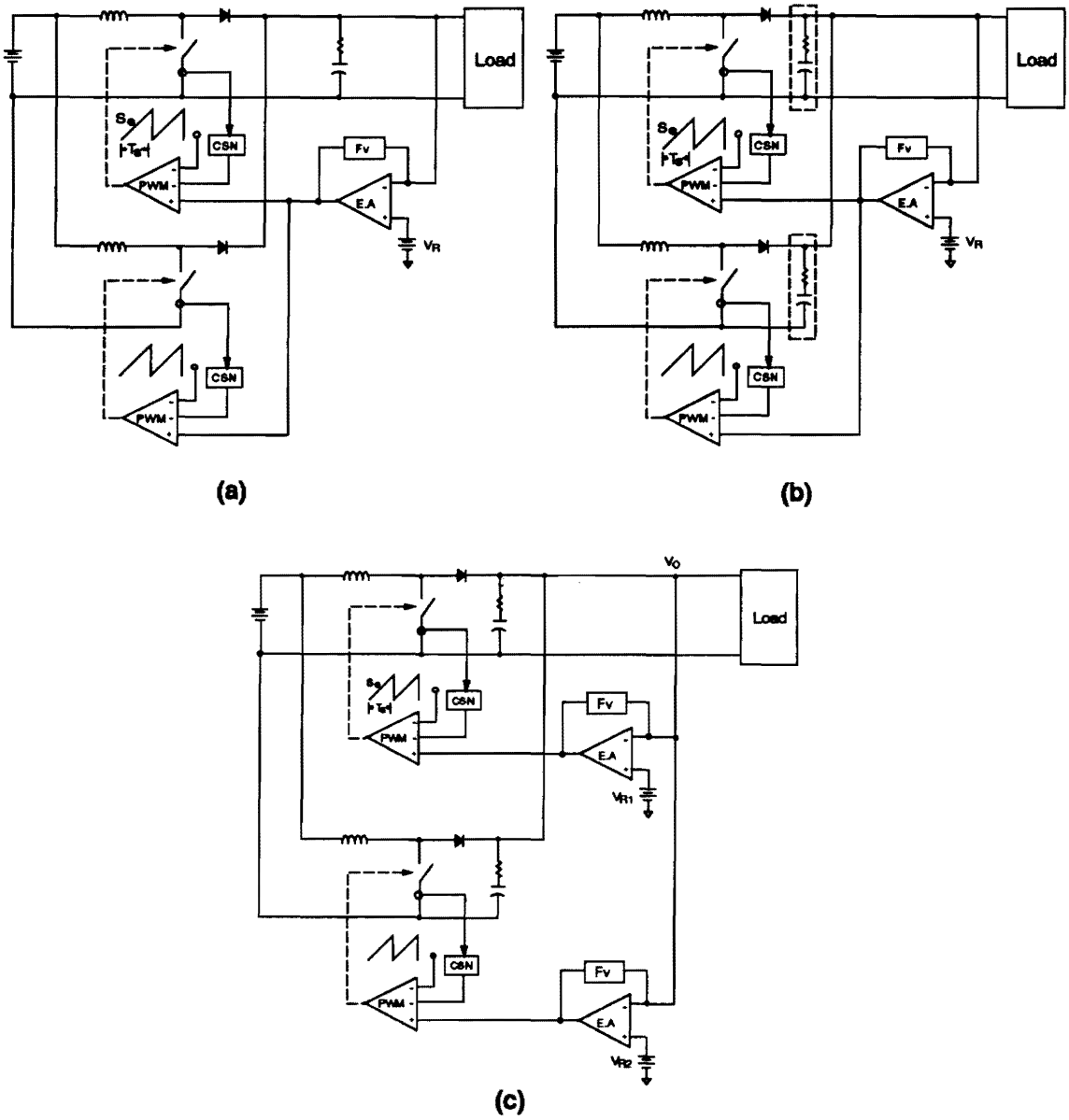


Fig. 2.1. Three different paralleling schemes for two-module boost converter: Each scheme employs current-mode controlled boost modules. PWM represents the pulse width modulation block, and CSN is the current sensing network. T_S represents the switching period, and S_e is the slope of the ramp function.

Figure 2.1(b) shows a multi-module configuration with an individual output capacitor for each module. Unlike the previous case, the closed-loop performance of the system is independent of the number of modules [B12]. Once control design is optimized for a given number of modules, the system can add or subtract an arbitrary number of modules as necessary without compromising any performance criteria. This configuration does not require an extra capacitor when the number of parallel modules increases. This configuration is well suited for high-power open-ended architectures with n+1 redundancy.

For some applications, it is desirable for each module to have the full features of a complete regulator for standardization of manufacturing and flexibility in system configuration. Figure 2.1(c) shows a two-module converter, where each module has an individual voltage feedback circuit, including its own voltage reference, V_R. This paralleling scheme readily realizes the fault-tolerance against the failure of any single component, and each module can operates as an individual converter.

The use of converter modules with an independent individual feedback controller, however, imposes an additional constraint on the voltage feedback compensation, F_V. If the voltage feedback compensation contains an integrator, the infinite dc gain of the integrator sufficiently amplifies any finite mismatch between voltage references of converter modules (unavoidable in practice) to cause a severe imbalance in current level of converter modules. To avoid such a problem, the voltage feedback compensation must have a finite dc gain. However, the finite dc gain of F_V results in a finite steady-state error in the output voltage. Thus the dc gain must be selected with a careful trade-off between current sharing and steady-state errors.

Figure 2.2(a) shows the modulator waveforms of a current-mode controlled module. The output of the voltage feedback circuit, V_C, is subtract by the output of CSN, to yield the total control signal, V_T. The total control signal is then compared with a ramp function, V_{RAMP}, to turn off the power switch when V_T intersects with the ramp function. The relationship between the dc gain of F_V and the current distribution among modules can be derived from the modulator waveform of Fig. 2.2(a). For an n-module converter, it can be assumed that the first module has the largest voltage reference of V_{R1} and the last module has the smallest voltage reference of V_{Rn}. Figure 2.2(b) shows the modulator waveforms of the first and last modules. From this figure, it can be easily seen that:

$$\Delta V_C = K_V(V_{R1} - V_O) - K_V(V_{Rn} - V_O) = K_V(V_{R1} - V_{Rn}) = (I_{1\max} - I_{n\max})R_i \qquad (2.1)$$

where K_V is the dc gain of F_V, V_O is the output voltage, $I_{k\max}$ $(k = 1, n)$ is the peak value of the switch current of each module, and R_i is the dc gain of CSN. Equation (2.1) can be rearranged as:

$$I_{1\max} - I_{n\max} = \frac{K_V(V_{R1} - V_{Rn})}{R_i} \qquad (2.2)$$

to yield an expression for the maximum deviation in switch currents of an n-module converter.

Figure 2.3 shows the current distribution of a three-module boost converter employing the paralleling scheme of Fig. 2.1(c). The converter has mismatched voltage references, and it undergoes a step load response. The maximum current deviation (between the first and the third modules) is given by a 6.7 A from Eq. (2.2). As shown in this

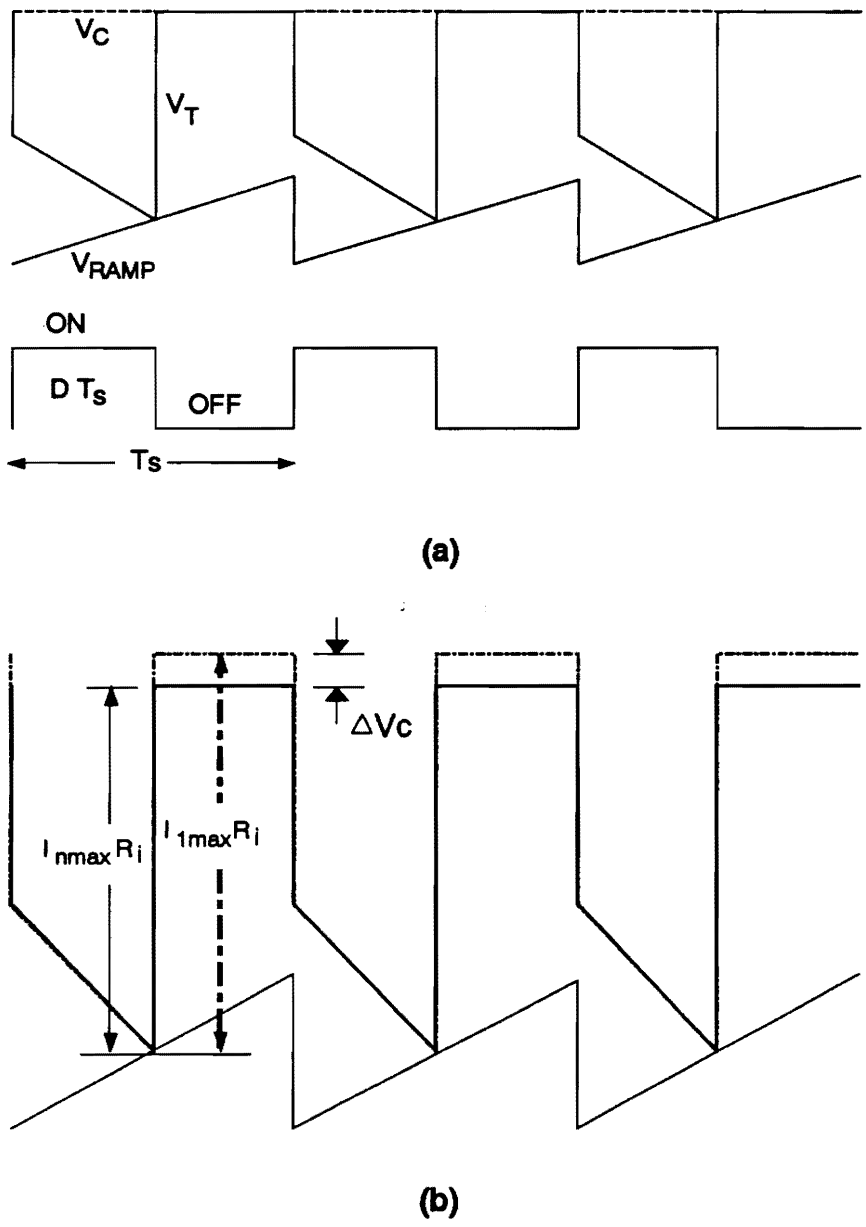


Fig. 2.2. Modulator waveforms of the current-mode controlled converter module: (a) Modulator waveforms of each module: The switch is turned ON at the beginning of the ramp function and turned OFF when V_T intersects with V_{RAMP}. **(b) Modulator waveforms of converter modules with non-identical voltage references.**

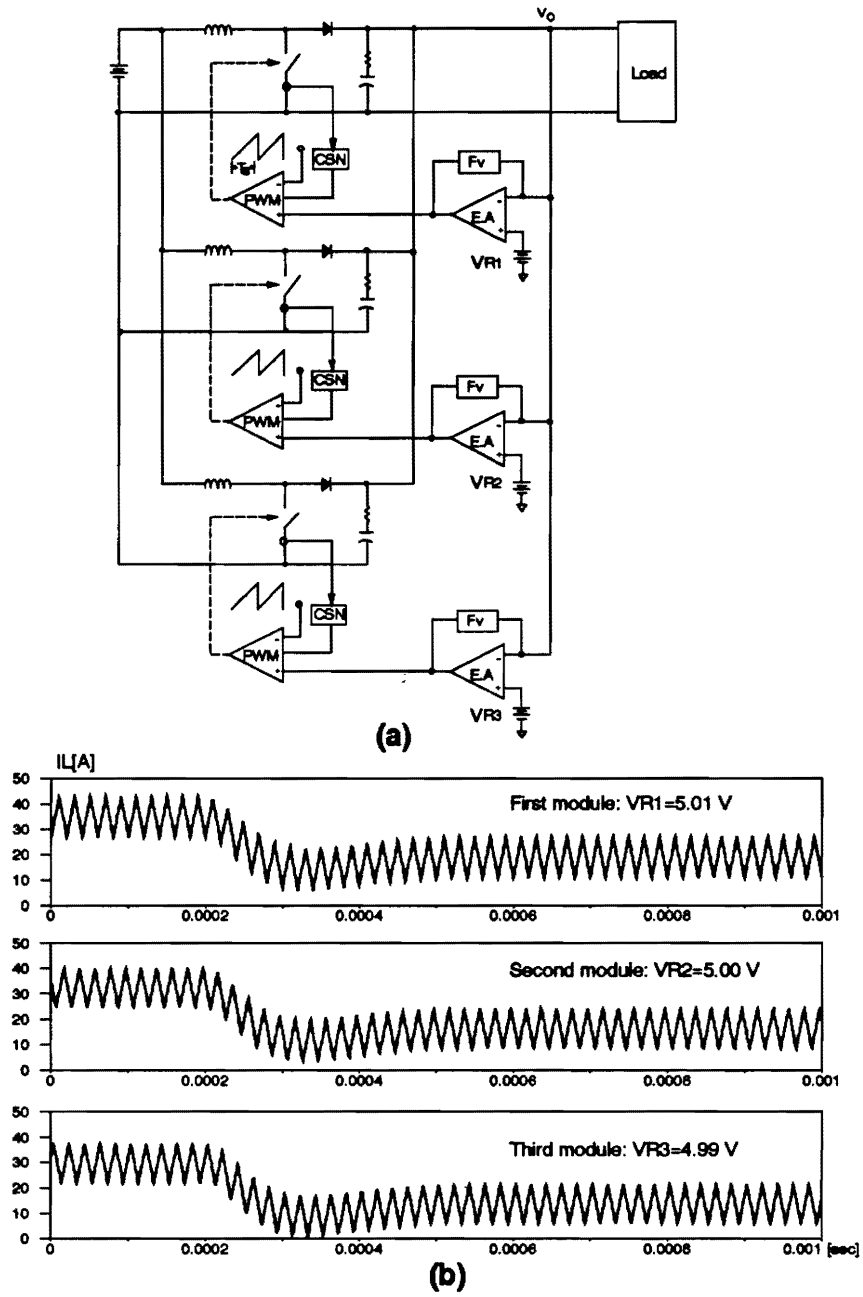


Fig. 2.3. Current distribution of a three-module boost converter during a step load response: (a) Block diagram. (b) Inductor currents of modules: $K_V = 50$, $R_i = 0.15$.

example, the current sharing can be adequately controlled by using a current-mode control with a finite voltage compensation gain. A high precision voltage reference may be used to further improve the current sharing. As will be discussed in section 2.3, a properly designed current-mode control provides a good current sharing in most practical applications.

The steady-state error of the output voltage in an n-module converter due to the step load change of ΔI_{step} is given by:

$$e_{load} = \lim_{s \to 0} sZ_O(s)\frac{\Delta I_{step}}{s} \tag{2.3}$$

where $Z_O(s)$ is the output impedance of converter. Using Eq. (2.3), the steady-state error can be easily derived as a function of K_V. For an n-module boost converter with a resistive load, the steady-state error is given by:

$$e_{load} = \frac{RV_G F_M R_i}{nD'^3 R + 2V_G F_M R_i + nD'RV_G F_M K_V}\Delta I_{step} \tag{2.4}$$

where R is the load resistor, V_G is the input voltage, F_M is the modulator gain of the PWM block, and $D' = 1 - D$ where D is the duty cycle. Similarly, using the audio-susceptibility, $A_U(s)$, the steady-state error due to the step line change of ΔV_{step} can be derived as:

$$e_{line} = \lim_{s \to 0} sA_U(s)\frac{\Delta V_{step}}{s} = \frac{nD'^3 R + V_G F_M R_i}{D'(nD'^3 R + 2V_G F_M R_i + nD'RV_G F_M K_V)}\Delta V_{step} \tag{2.5}$$

As shown in Eqs. (2.2), (2.4), and (2.5), a larger K_V offers smaller steady-state errors, but it causes a larger current imbalance. Thus K_V should be determined with a careful trade-off between these two conflicting factors. The steady-state errors for n-module buck and buck-boost converters can be derived in the same way, and they are summarized in Table 2.1.

Table 2.1: Steady-state error of n-module converters with a finite dc gain of voltage feedback compensation

	Steady-state error due to ΔI_{step}	Steady-state error due to ΔV_{step}
Buck	$\frac{RV_G F_M R_i \Delta I_{step}}{nR + V_G F_M R_i + nRV_G F_M K_V}$	$\frac{nD\Delta V_{step}}{nR + V_G F_M R_i + nRV_G F_M K_V}$
Boost	$\frac{RV_G F_M R_i \Delta I_{step}}{nD'^3 R + 2V_G F_M R_i + nD'RV_G F_M K_V}$	$\frac{(nD'^3 R + V_G F_M R_i)\Delta V_{step}}{D'(nD'^3 R + 2V_G F_M R_i + nD'RV_G F_M K_V)}$
Buck-boost	$\frac{RV_G F_M R_i \Delta I_{step}}{nD'^3 R + (1+D)V_G F_M R_i + nD'RV_G F_M K_V}$	$\frac{D(nD'^3 R + V_G F_M R_i)\Delta V_{step}}{D'(nD'^3 R + (1+D)V_G F_M R_i + nD'RV_G F_M K_V)}$

2.3 CURRENT DISTRIBUTION BETWEEN NON-IDENTICAL MODULES

One practical consideration for multi-module converters is the current distribution among parallel modules. Parallel modules are usually non-identical due to finite tolerances in power stage and control parameters. If no special provision is made to control the current level, one specific module might deliver an excessive load current, eliminating the major advantage of the modular approach.

Many approaches have been proposed [A7-A10] to achieve a good current sharing among non-identical converter modules, some employ a master-slave concept, and the others utilize an additional control loop which requires interconnections between converter modules. These control schemes, however, often degrade the reliability and modularity of the system. In the master-slave approach, where slave modules are forced to follow the current level of the master module, the failure of the master module results in the shut-down of the whole system. Also, the control methods relying on interconnections between converter modules degrade the modularity of the system.

The current mode control, widely used in high performance dc-to-dc converters, provides an excellent current sharing among non-identical modules without compromising the reliability and modularity of the system. There is no apparent need for any control scheme other than current-mode control in most practical applications.

The current-mode control, which uses the peak current to issue the switch off command, forces mismatched converter modules to have a good current sharing. The current

distribution between mismatched current mode-controlled modules can be easily derived from the modulator waveforms of Fig. 2.2(a). As an example, Fig. 2.4 shows the modulator waveforms of two boost modules whose ramp functions have two different slopes of S_{e1} and S_{e2}. From Fig. 2.4, the following relationship can be easily seen:

$$I_{2\max}R_i = I_{1\max}R_i + (S_{e1} - S_{e2})DT_S \tag{2.6}$$

which can be rearranged as:

$$I_{2\max} - I_{1\max} = \frac{(S_{e1} - S_{e2})DT_S}{R_i} \tag{2.7}$$

to give the expression for the current distribution.

Figure 2.5(a) shows the current distribution of a three-module boost converter, whose worst case current deviation (between the first and third modules) is predicted as a 2.04 A from Eq. (2.7). As shown this figure, Eq. (2.7) accurately predicts the current distribution among mismatched converter modules both in steady state and in step load transition.

The effects of mismatch in other power stage and control parameters can be derived in a similar way, and they are summarized in Table 2.2. As shown in this table, the mismatch in power stage parameters does not cause any imbalance in the peak current of the modules. The mismatch in control parameters also does not cause any significant imbalance for most practical applications.

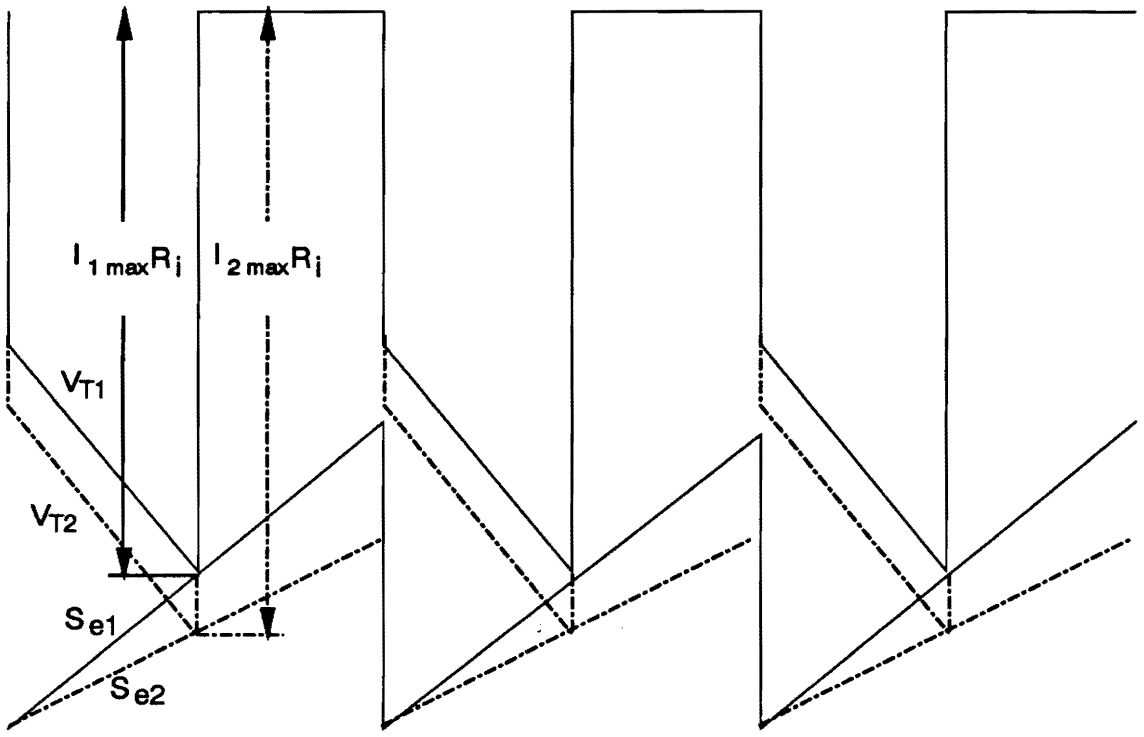


Fig. 2.4. Modulator waveforms of converter modules with non-identical ramp functions: The ramp functions have two different slopes of S_{e1}, and S_{e2}.

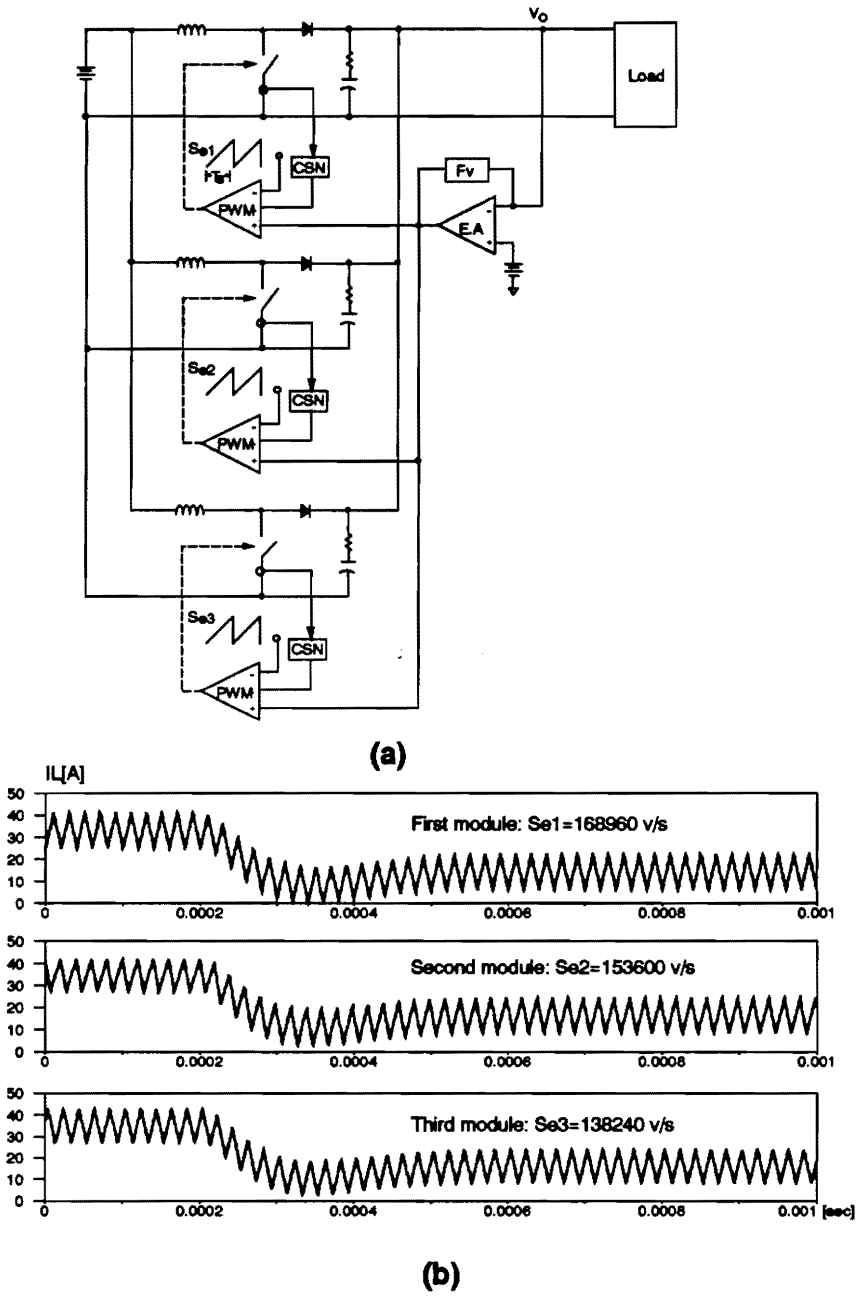


Fig. 2.5. Current distribution of a three-module boost converter during a step load response: (a) Block diagram. (b) Inductor currents of modules: $R_i = 0.15$, $D = 0.5$, $T_S = 20\,\mu$Sec.

Table 2.2: Current sharing between mismatched converter modules

Mismatched parameter	Current distribution
Inductor, L	$I_{2\max} = I_{1\max}$ $I_{2\min} - I_{1\min} = DT_S V_G \frac{L_2 - L_1}{L_1 L_2}$ *for boost*, or *buck/boost* $I_{2\min} - I_{1\min} = DT_S V_G (1-D) \frac{L_2 - L_1}{L_1 L_2}$ *for buck*
Capacitor, C	$I_{2\max} = I_{1\max}$ $I_{2\min} = I_{1\min}$
CSN gain, R_i	$\frac{I_{2\max}}{I_{1\max}} = \frac{I_{2\min}}{I_{1\min}} = \frac{R_{i1}}{R_{i2}}$
Slope of ramp function, S_e	$I_{2\max} - I_{1\max} = I_{2\min} - I_{1\min} = \frac{DT_S}{R_i}(S_{e1} - S_{s2})$

2.4 EQUIVALENT SINGLE-MODULE MODEL

The dynamic performance of a multi-module converter includes stability margins, audio-susceptibility, output impedance, and transient responses due to line and load variations. The ultimate goal of the control design is to optimize these performance criteria for given operating conditions and power stage parameters.

While a multi-module converter has a complex structure, it can be greatly simplified as far as the control design is concerned. The simplified model, referred to as an equivalent single-module model, has the structure of a conventional single-module converter, while preserving the dynamics of the original multi-module converter. Using the equivalent single-module model, any control scheme developed for a single-module converter can be directly adapted to a multi-module converter. The control design optimized using the equivalent single-module model offers a multi-module converter which matches its closed-loop performance by the equivalent single-module model. Also, multi-module converters operating as subsystems of a large-scale power system can be replaced with their equivalent single-module models without compromising any analysis accuracy. The benefits of the equivalent single-module model to the analysis and design of large-scale power systems will be demonstrated in Chapters 3 and 4.

An earlier work [A11] showed that a multi-module buck converter with a common output capacitor can be reduced to an equivalent single-module model. The approach taken in [A11] is based on the state space analysis which needs to include dynamics all reactive components of the power stage. This approach was successfully adapted to a

buck converter with separate output capacitors [B15] and a boost converter [A4]. However, this approach becomes very involved when the number of reactive components of power stage increases, and is difficult to adapt to other topologies.

This section presents a new approach to deriving the equivalent single-module model, which can be readily adapted to higher order multi-module systems. The new approach combines the concept of PWM switch model [D4] with standard circuit analysis techniques and does not require any complex analytical manipulations. Once the derivation steps are fully understood, the equivalent single-module model can be obtained, in many cases, by an inspection. The new approach can be generalized to ZVS-FB-PWM converters [D9] and quasi-resonant converters using an equivalent switch model [D3].

Detailed steps of deriving the equivalent single-module model are demonstrated using a three-module boost converter. Control design procedures for a multi-module converter using the equivalent single-module model are presented. The equivalence between the original multi-module converter and the equivalent single-module model is verified by both frequency- and time-domain simulations.

2.4.1 Model Derivation

Figure 2.6 shows the schematic diagram of a three-module boost converter. The converter consists of three current-mode controlled boost modules, a common voltage feedback compensation, F_V, and a load. Figure 2.7 shows the small-signal model of Fig. 2.6, obtained by replacing an active-passive switch pair with the PWM switch model

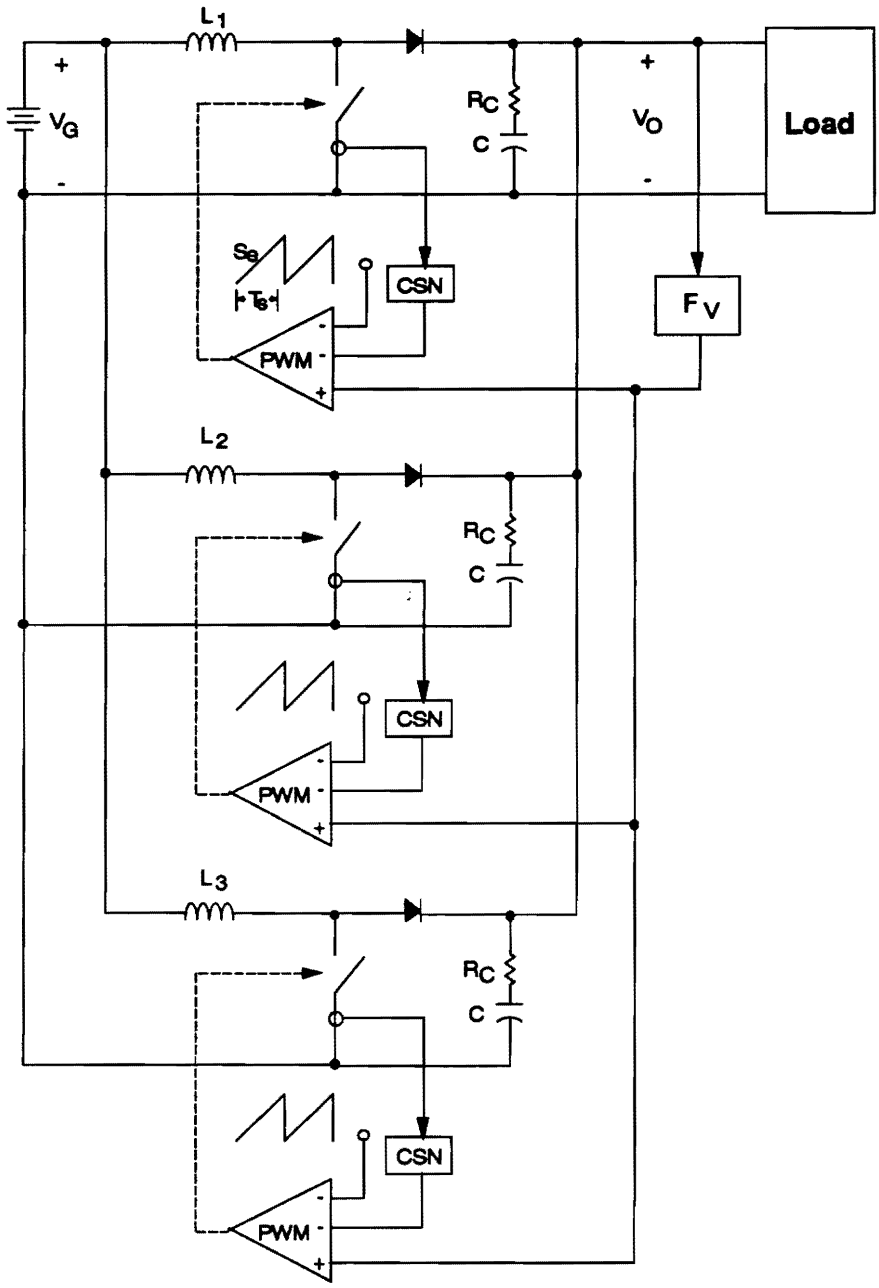


Fig. 2.6. Three-module boost converter: Power stage and control parameters are assumed to be identical for all three modules ($L_1 = L_2 = L_3 = L$).

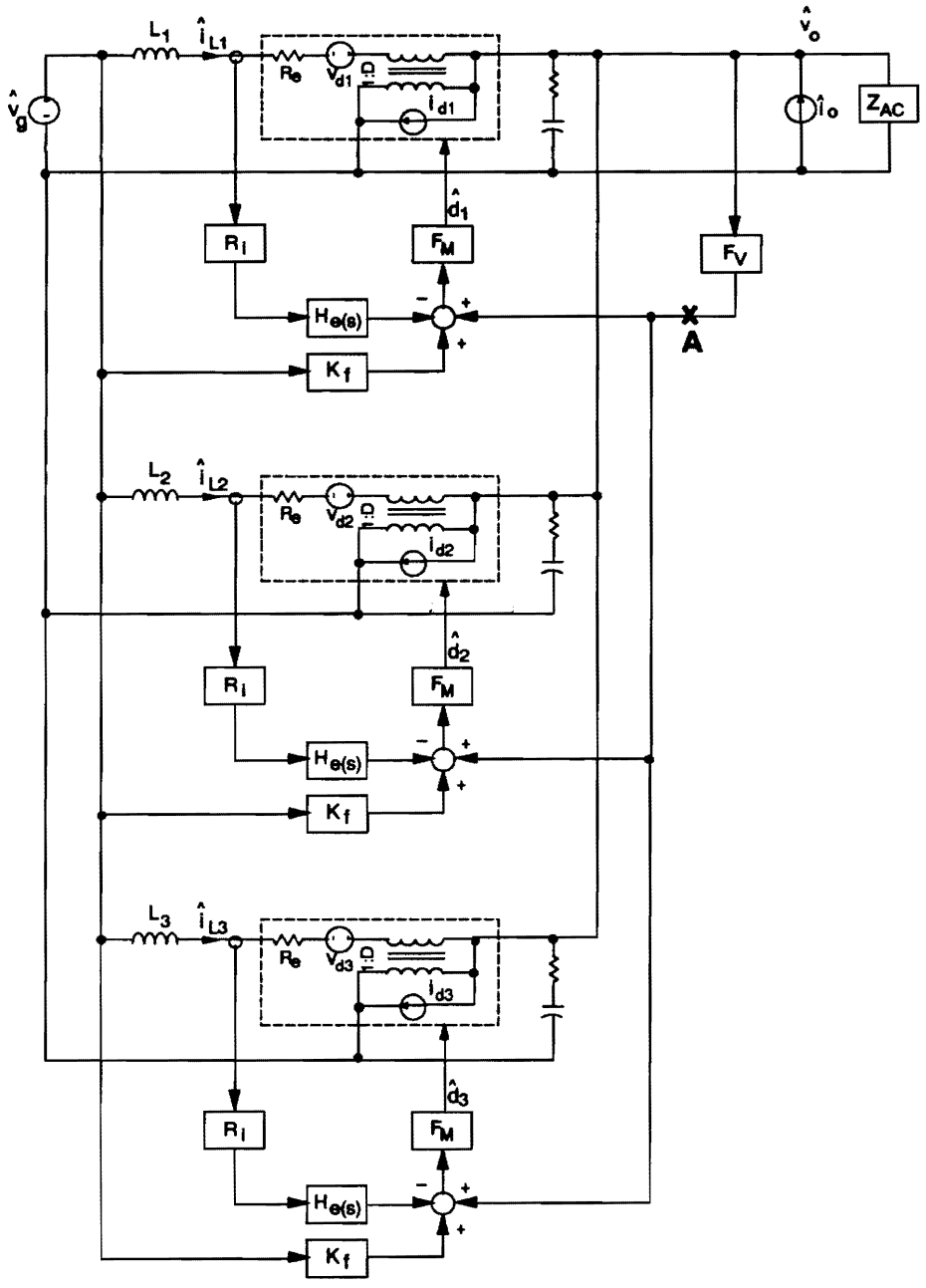


Fig. 2.7. Small-signal model of the system: F_M represents the modulator gain of the PWM block, and R_i is dc gain of the CSN [D8]. $H_e(s)$ represents the sampling gain of the CSN, and k_f is the feedforward gain created by the CSN.

[D3,D4], replacing the PWM and CSN blocks with their small signal models [D7,D8], and replacing the load with its input impedance, Z_{AC}. The parameters for the PWM switch model and definitions of the gain blocks are given in Table 2.3.

The small-signal model of Fig. 2.7 is successively simplified to yield an equivalent single-module model, keeping following performance criteria unchanged:

- audio-susceptibility $A_U \equiv \hat{v}_O/\hat{v}_g$;
- output impedance $Z_O \equiv \hat{v}_O/\hat{i}_O$; and
- loop gain measured at "A."

Figure 2.8(a) shows the power stage model of the system, where the ideal transformer is replaced with a pair of current and voltage sources, i_{Tk} and v_{Tk} $(k = 1,2,3)$. This model simplifies to Fig. 2.8(b) by combining the current sources, i_{Tk} and i_{ck} $(k = 1,2,3)$, and the output capacitors. Three identical voltage sources in Fig. 2.8(b), v_{T1}, v_{T2}, and v_{T3} are combined, and subsequently v_{T2} and v_{T3} are removed to yield Fig. 2.9(a). Figure 2.9(b) is the simplified system model, obtained by adapting Fig. 2.9(a) and replacing v_{T1} and i_{Te} with an ideal transformer.

Since the closed-loop performance of a multi-module converter is determined by the small-signal sources, $\hat{v}_g$, $\hat{i}_o$, and the injection signal at "A" for the loop gain measurement (refer to Fig. 2.7 for definitions of these small-signal sources), the only considerations in deriving a reduced model are the system response due to these small-signal disturbance sources. In deriving a reduced-order model which preserves the closed-loop performance of the multi-module system, $\hat{d}_1$, $\hat{d}_2$, and $\hat{d}_3$ (the small-signal averaged value

Table 2.3: Summary of parameters in Fig. 2.7

	Parameters
PWM switch	$R_e = R_C DD'$ $v_{dk} = (V_O + I_{Lk}(D - D')R_C)\hat{d}_k \quad (k = 1,2,3)$ $i_{dk} = I_{Lk}\hat{d}_k$ D:duty cycle $D' = 1 - D$ I_{Lk}: inductor current of k^{th} module
Modulator gain of PWM	$F_M = \frac{1}{(S_n + S_e)T_s}$ S_e: slope ramp function S_n: on-time slope of sensed switch current
Dc gain of CSN	R_i (constant)
Sampling gain of CSN	$H_e(s) = 1 + \frac{s}{\omega_n Q_n} + \frac{s^2}{\omega_n^2}$ $Q_n = -\frac{2}{\pi}, \qquad \omega_n = \frac{\pi}{T_s}$
Feedforward gain of CSN	$k_f = -\frac{T_S R_i}{2L}$

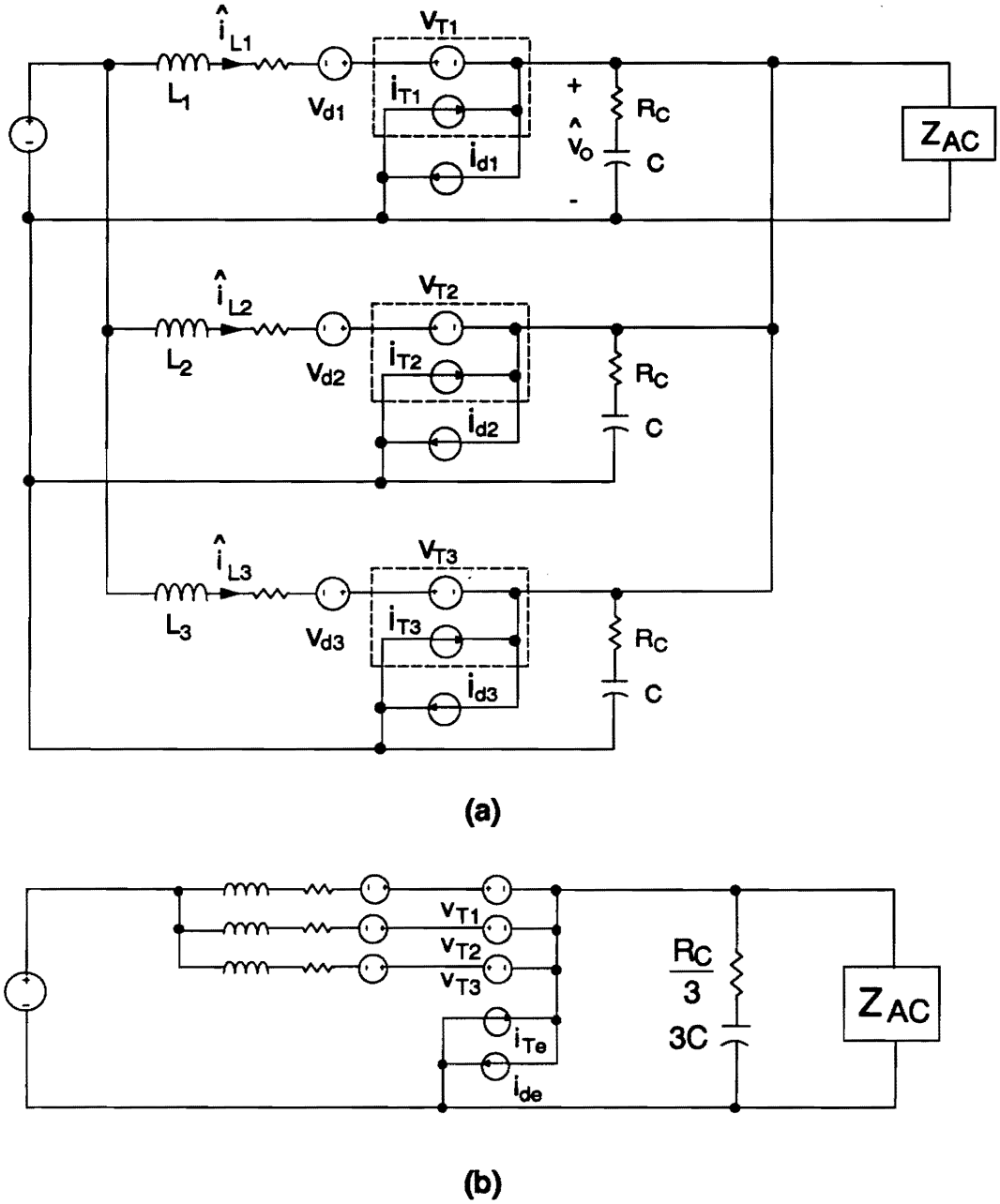


Fig. 2.8. Simplification of power stage model: (a) Modified power stage model: $i_{Tk} = -D\hat{i}_{Lk}\,(k = 1,2,3)$, $v_{Tk} = -D\hat{v}_O$; (b) Simplified power stage model: $i_{Te} = i_{T1} + i_{T2} + i_{T3} = -D(\hat{i}_{L1} + \hat{i}_{L2} + \hat{i}_{L3})$, $i_{de} = i_{d1} + i_{d2} + i_{d3} = I_{L1}\hat{d}_1 + I_{L2}\hat{d}_2 + I_{L3}\hat{d}_3$.

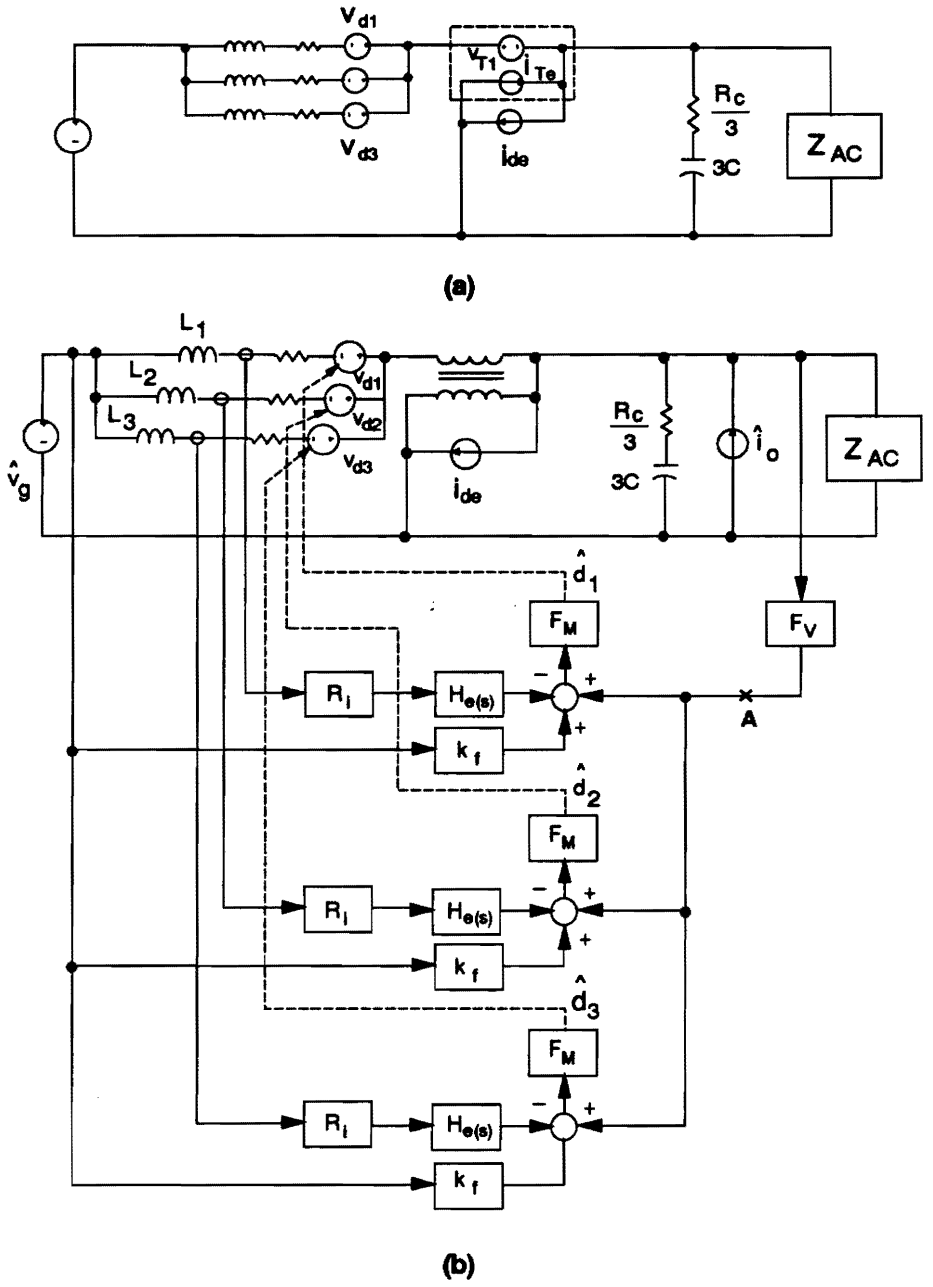


Fig. 2.9. Simplified small-signal model of the system: (a) Further simplification of power stage is achieved by eliminating v_{T2} and v_{T3}. (b) Simplified system model: $i_{de} = I_{L1}\hat{d}_1 + I_{L2}\hat{d}_2 + I_{L3}\hat{d}_3$, $v_{dk} = (V_O + I_{Lk}(D - D')R_c)\hat{d}_k$ $(k = 1,2,3)$.

of the change in duty cycle of each switch) can be considered identical due to the symmetry of the system. As a result, three dependent voltage sources, v_{d1}, v_{d2}, and v_{d3} are the same, and the inductors/resistors of the converter modules can be combined to yield a simplified model of Fig. 2.10(a). In Fig. 2.9(b), the output of the CSN of each module is given by:

$$V_{CSN} = \frac{R_i}{L_k} \int v_{Lk} dt \,. \tag{2.8}$$

Since the inductor is divided by three in Fig. 2.10(a), R_i should also be divided by three to produce the same output voltage as Eq. (2.8). With this scaling of CSN gain, F_M and k_f remain the same in Figs. 2.9(b) and 2.10(a).

As the last step, the redundant voltage sources, v_{d2} and v_{d3}, together with their associated feedback controller, are removed, resulting in the equivalent single-module model of Fig. 2.10(b).

2.4.2 Control Design Procedure

The equivalent single-module model allows design of the control loop of a multi-module converter to be same as for a conventional single-module converter:

1. Design R_{ie} using the equivalent single-module model. The switch current of the single-module model is the sum of switch currents of individual modules. Multiply

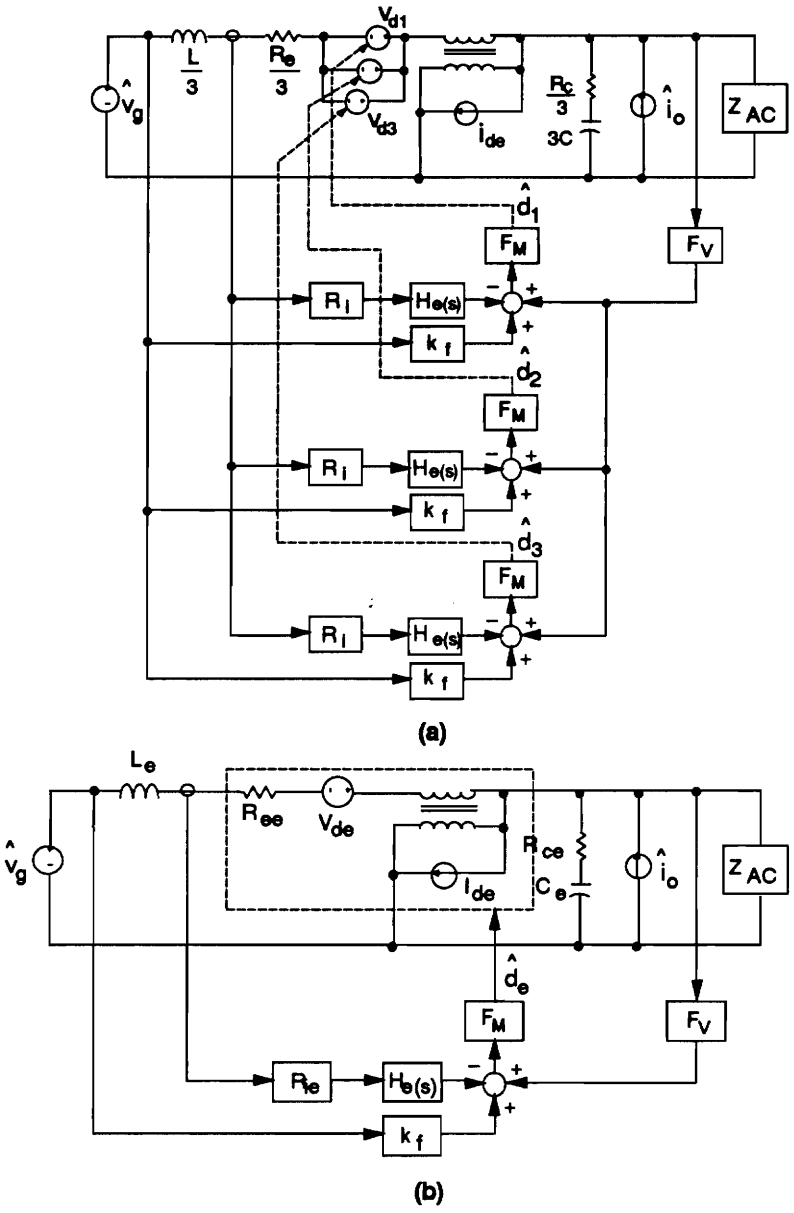


Fig. 2.10. Equivalent single-module model: (a) Further simplification using $\hat{d}_1 = \hat{d}_2 = \hat{d}_3$. (b) Equivalent single-module model: $L_e = L/3$, $R_{ce} = R_c/3$, $C_e = 3C$, $R_{ee} = R_e/3$, $v_{de} = (V_O + I_{Le}(D - D')R_{ce})\hat{d}_e$, $I_{Le} = I_{L1} + I_{L2} + I_{L3}$, $i_{de} = I_{Le}\hat{d}_e$, $R_{ie} = R_i/3$.

the resulting gain by the number of modules to obtain R_i for individual module. This CSN gain scaling compensates for the difference of switch currents between the equivalent single-module model and the original multi-module system.

2. Select the slope of the external ramp for a desired modulator gain [D8], using the single-module model. The result is directly applicable to the multi-module converter.

3. Design the voltage feedback compensation, F_V, using the single-module model. The standard design techniques developed for single-module converters [D1,D2] can be used to optimize the closed-loop performance. The result is also directly applicable to the multi-module converter.

This design procedure produces a multi-module converter which matches its closed-loop performance by the equivalent single-module model. Figure 2.11 shows the performance of the three-module converter in comparison with that of the equivalent single-module model. The exact agreement in the transfer functions verifies the modeling results and design procedures. The power stage and control parameters of the three-module converter are summarized in Table 2.4.

Figure 2.12 shows the time-domain counterpart of the equivalent single-module model of Fig. 2.10(b). This model produces the same transient responses as the three-module converter. Figure 2.13 compares the step load response of the three-module converter and that of the (time-domain) equivalent single-module model of Fig. 2.12. The

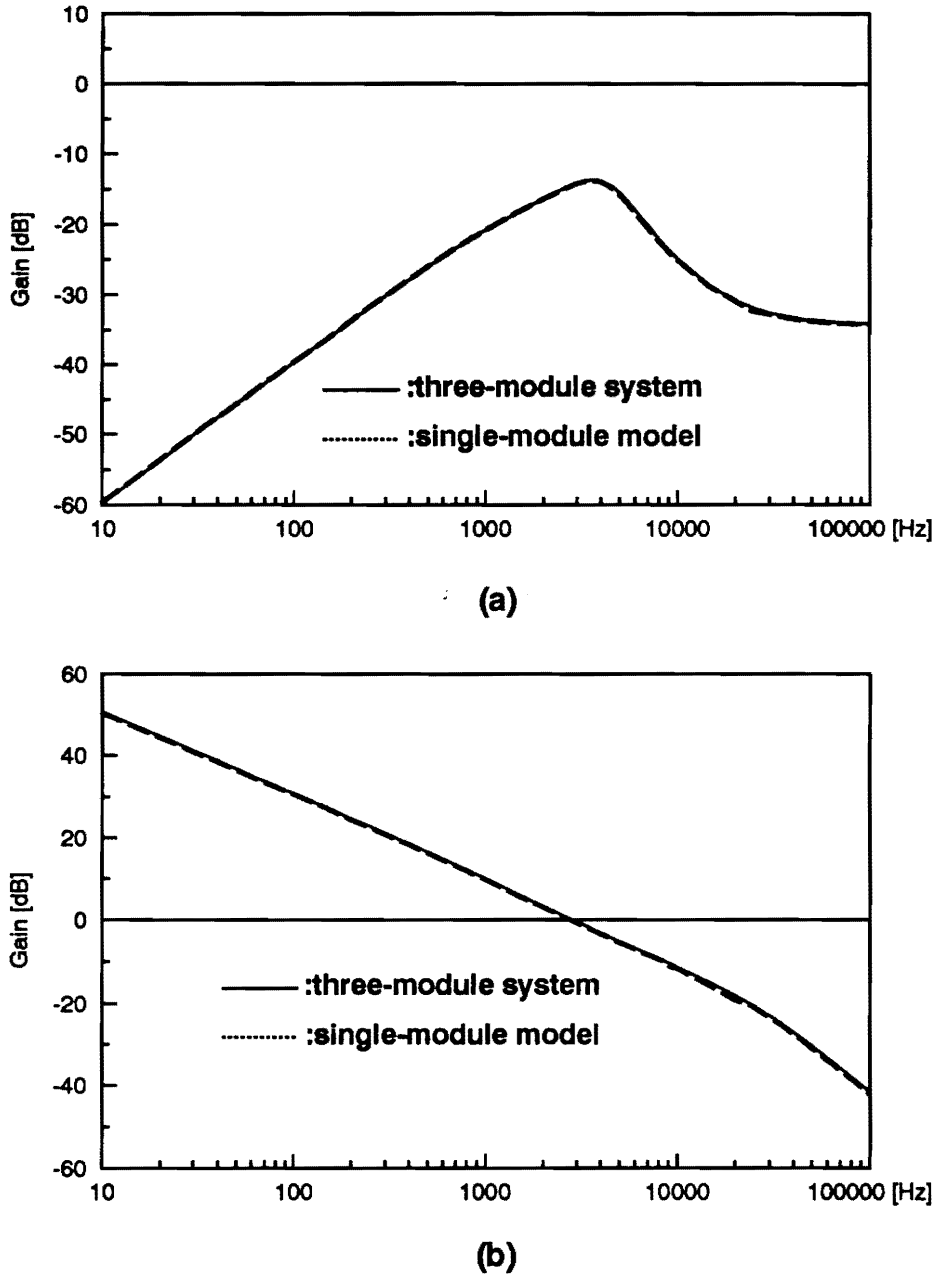


Fig. 2.11. Small-signal performance of the three-module system: (a) Output impedance. (b) Loop gain: The exact agreement in the transfer functions verifies the modeling results and design procedures.

Table 2.4: Parameters of the three-module boost converter

Parameters	Values
Power stage parameters	$V_G = 24V$, $V_O = 48V$ $L = 15\,\mu F$ $C = 133\,\mu F$, $R_C = 60\,m\Omega$
Load	Resistive load of 1 Ω
Control parameters	$T_S = 20\,\mu s$, $S_e = 153600$, $R_i = 0.15$ $F_V = \frac{6300(1 + s/8944)}{s(1 + s/50000)}$

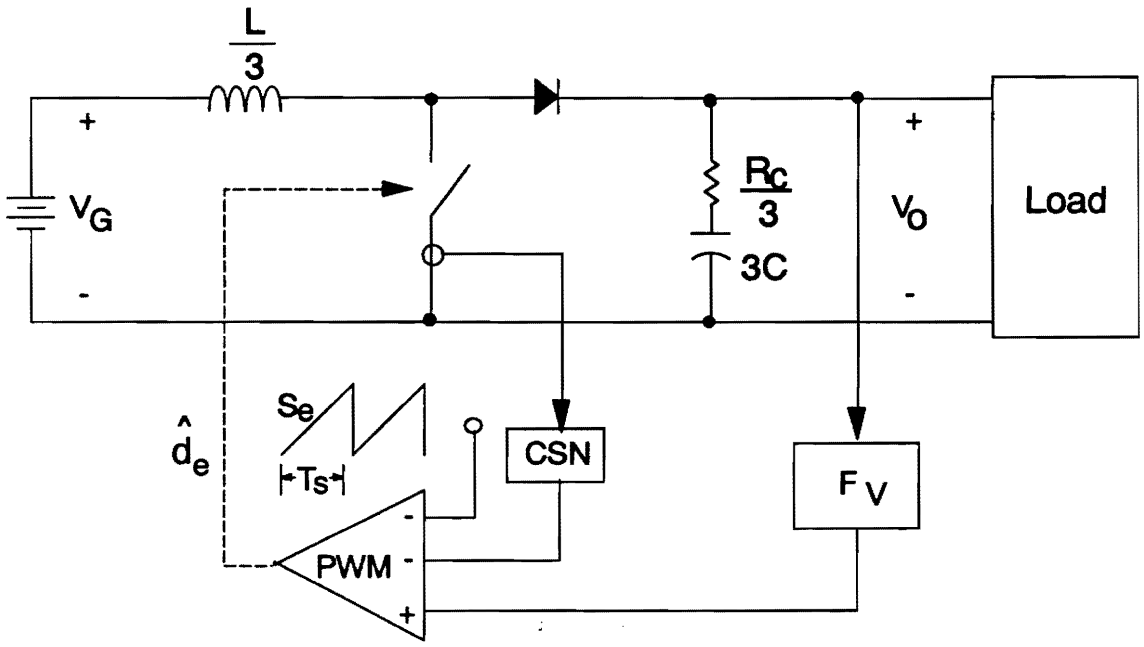


Fig. 2.12. Equivalent single-module model: This model generates the same transient response as the three-module converter. The dc gain of CSN is one-third of CSN gain of the three-module converter.

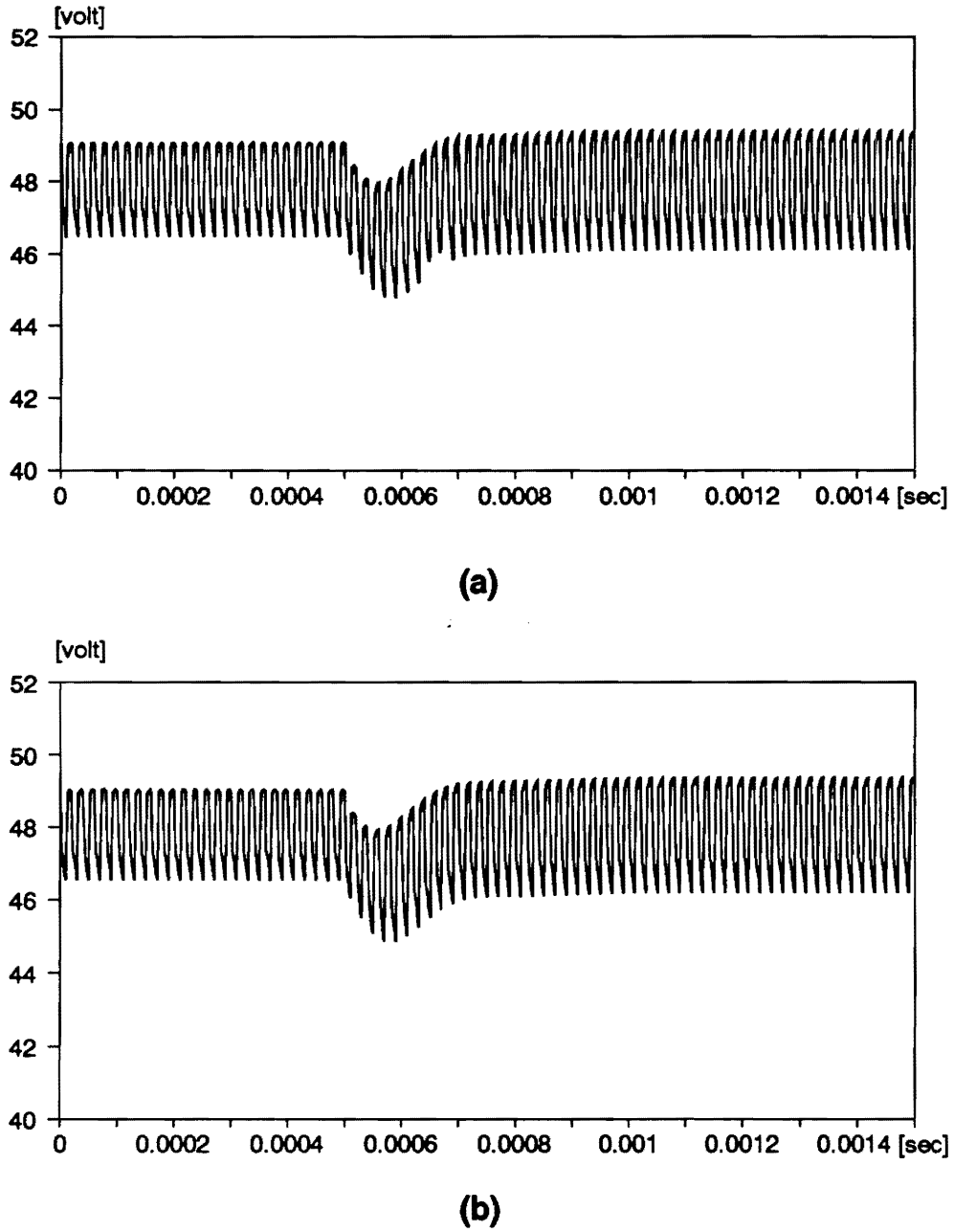


Fig. 2.13. Transient response of the output voltage due to the step load change from 48 A to 60 A: (a) Three-module system. (b) Equivalent single-module model: Transient response confirms that the equivalent single-module model preserves time-domain characteristics as well.

exact agreement in transient response of the output voltage confirms that the equivalent single-module model preserves both frequency- and time-domain performance of the multi-module converter.

2.4.3 Model Sensitivity

Parallel modules are usually non-identical due to finite tolerances of components. Thus it is necessary to investigate the sensitivity of the equivalent single-module model to the variation of power stage parameters and operating conditions of parallel modules.

Figures 2.14 and 2.15 show the closed-loop performance of four different three-module boost converters. While Converter 1 has identical modules, Converters 2, 3, and 4 have mismatched modules. Power stage parameters and inductor currents of these converters are summarized in Table 2.5. For Converter 1, the equivalent single-module model of Fig. 2.10(b) is used for frequency-domain simulations. For Converters 2, 3, and 4, the original multi-module model of Fig. 2.7 is used for computer simulations.

As shown in Figs. 2.14 and 2.15, the converters do not show any significant difference in closed-loop performance even though the power stage parameters and operating conditions are mismatched up to 20 %. The equivalent single-module model is highly robust against the mismatch of modules, and it provides a high accuracy for most practical applications.

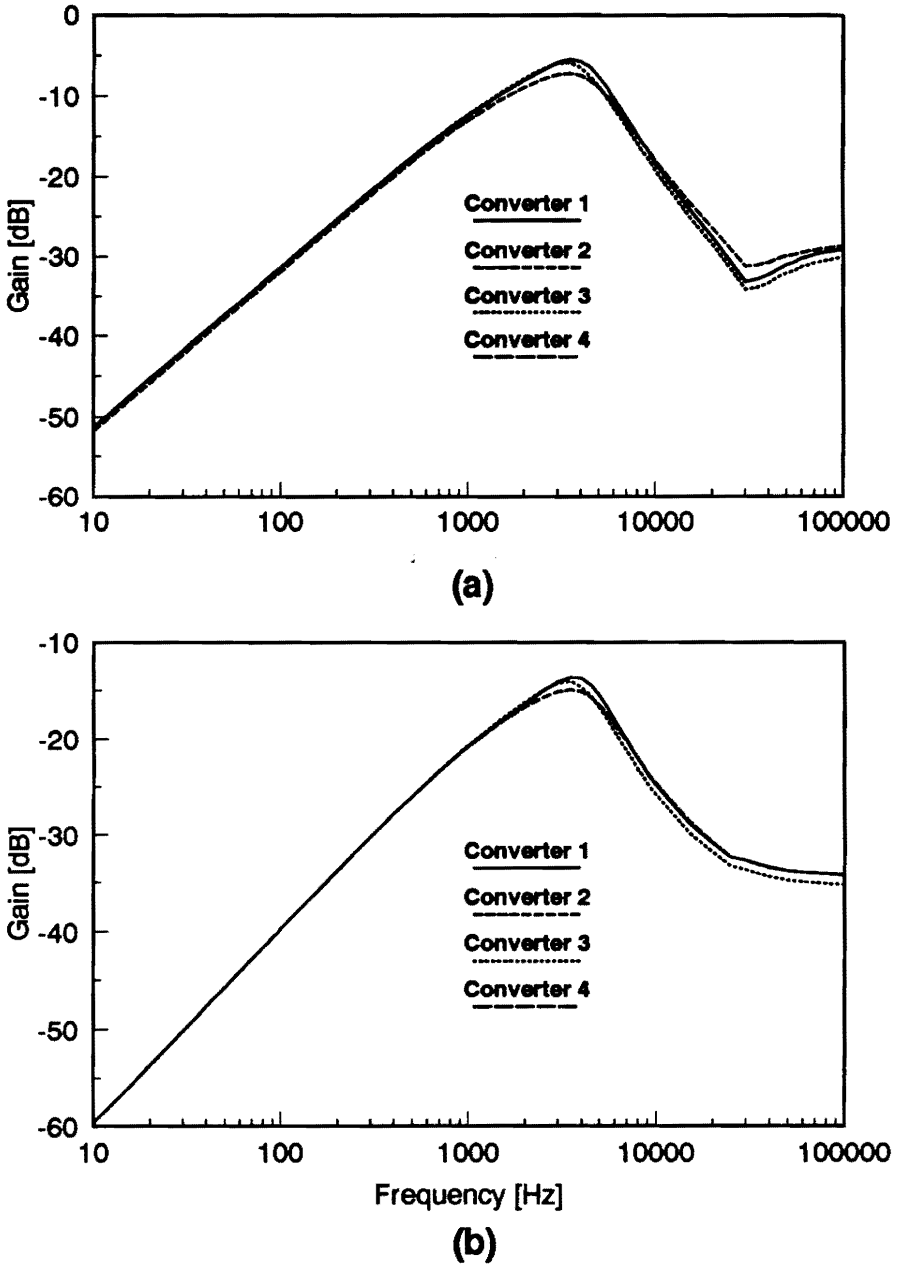


Fig. 2.14. Closed-loop performance of four different three-module boost converters: (a) Audio-susceptibility. (b) Output impedance.

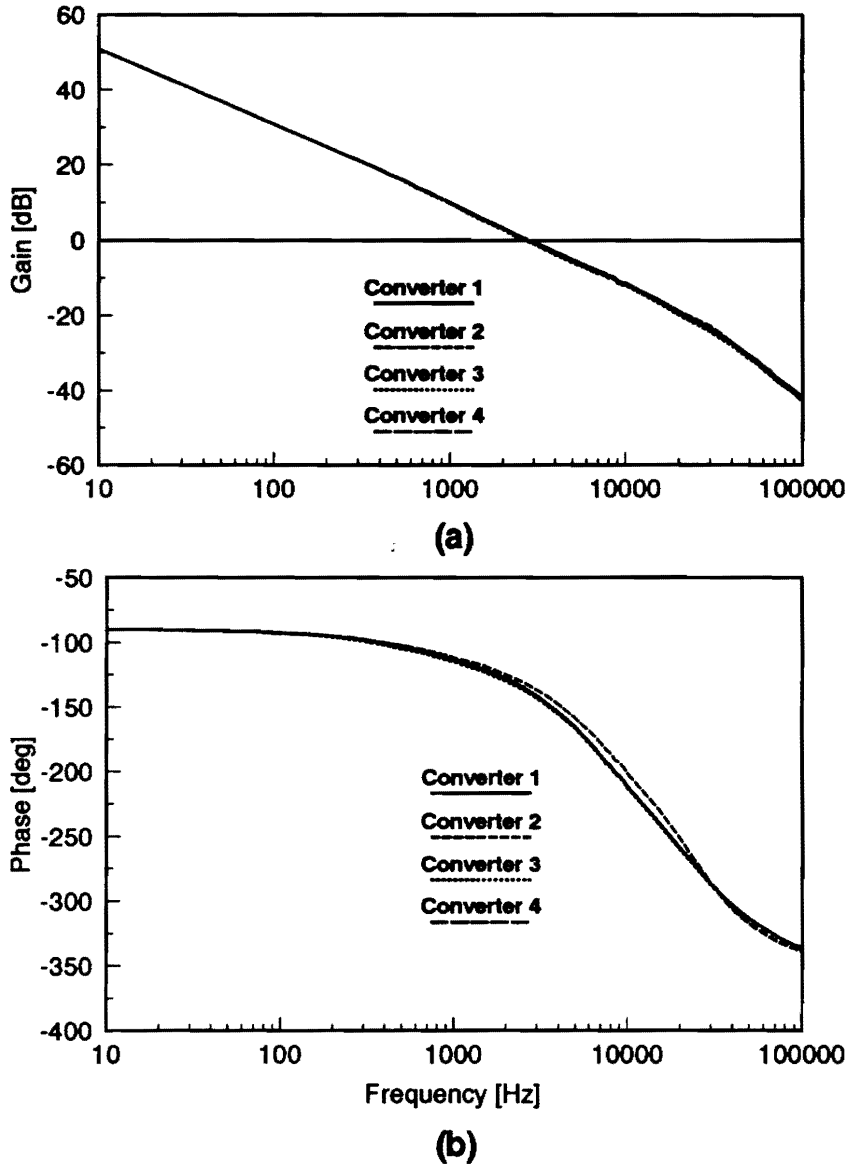


Fig. 2.15. Loop gain of four different three-module boost converters: (a) Gain. (b) Phase.

Table 2.5: Parameters of the three-module boost converters used in Figs. 2.14 and 2.15

Converter 1	$L = 15\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 16A$ for all modules
Converter 2	Module 1: $L = 15\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 16A$ Module 2: $L = 12\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 16A$ Module 3: $L = 12\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 16A$
Converter 3	Module 1: $L = 15\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 16A$ Module 2: $L = 15\,\mu H \quad C = 151\,\mu F \quad R_C = 0.05\,\Omega \quad I_L = 16A$ Module 3: $L = 15\,\mu H \quad C = 151\,\mu F \quad R_C = 0.05\,\Omega \quad I_L = 16A$
Converter 4	Module 1: $L = 15\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 19.2A$ Module 2: $L = 15\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 14.4A$ Module 3: $L = 15\,\mu H \quad C = 133\,\mu F \quad R_C = 0.06\,\Omega \quad I_L = 14.4A$

2.5 THREE-LOOP CONTROL

Many multi-module converters have applications that require very low output-voltage ripple and high-frequency noise. The high-speed VLSI circuitry often requires a supply voltage of 1 ~ 2 V, with less than 5 mV of switching ripple and noise. Since a single-stage filter is impractical to meet these requirements, a secondary LC filter is often employed between the output of converter modules and the load. Reference [E5] has provided guidelines to design an efficient secondary LC filter.

Unfortunately, a secondary LC filter introduces an additional resonance which could result in instability problem. The conventional two-loop current-mode control does not offer any means of controlling the secondary filter resonance. To ensure the stability at the presence of the secondary LC filter, a two-loop controlled system must sacrifice the closed-loop performance. The limitations of a two-loop controlled system are most pronounced in the transient response in the event of failure of a converter module (referred to as the module-failure response), which is a critical performance criterion for multi-module redundant system. To obtain the full benefits of the redundant modular approach, it is necessary to compensate for detrimental effects of the secondary filter resonance with an appropriate control scheme. Otherwise, the failure of a module might cause an excessive undershoot/overshoot in the output voltage, resulting in interruptions of the equipment downstream.

This section proposes a three-loop control scheme for multi-module converters with a secondary LC filter. In addition to output voltage and inductor current feedback, the control scheme employs feedback from the output capacitor of each module (referred to

as the local voltage feedback signal) to compensate for the detrimental effects of the secondary filter resonance. As will be discussed in Section 2.5.2, the local voltage feedback signal carries all information about the secondary filter resonance. The three-loop control uses the local voltage feedback as an integral part of the controller to eliminate any design constraints imposed by the secondary LC filter. As a result, the three-loop control minimizes the complexity and does not require exact knowledge of the secondary filter resonant frequency, while providing a much enhanced performance.

2.5.1 Limitations of Two-Loop Current-Mode Controls

Before proceeding with discussion of a three-loop control scheme, it is useful to examine the limitations of the conventional two-loop current-mode control. Figure 2.16 shows a schematic diagram of a three-module buck converter with two-loop control. The system consists of three current-mode controlled buck modules, a common secondary LC filter (L_2 and C_2), and an output voltage feedback circuit, F_R. Each module consists of a buck power stage operating at 100 kHz, a PWM block, and a CSN for the inductor current (on-time switch current) feedback.

Figure 2.17 shows the equivalent single-module model for Fig. 2.16, obtained by following the procedures established in Section 2.4.1. In this small-signal model, an additional current source, $\hat{i}_f$, is included to define a new performance criterion to characterize the module-failure response. The disturbance in the output current due to the failure of a converter module is represented by a current source at the summing junction. A

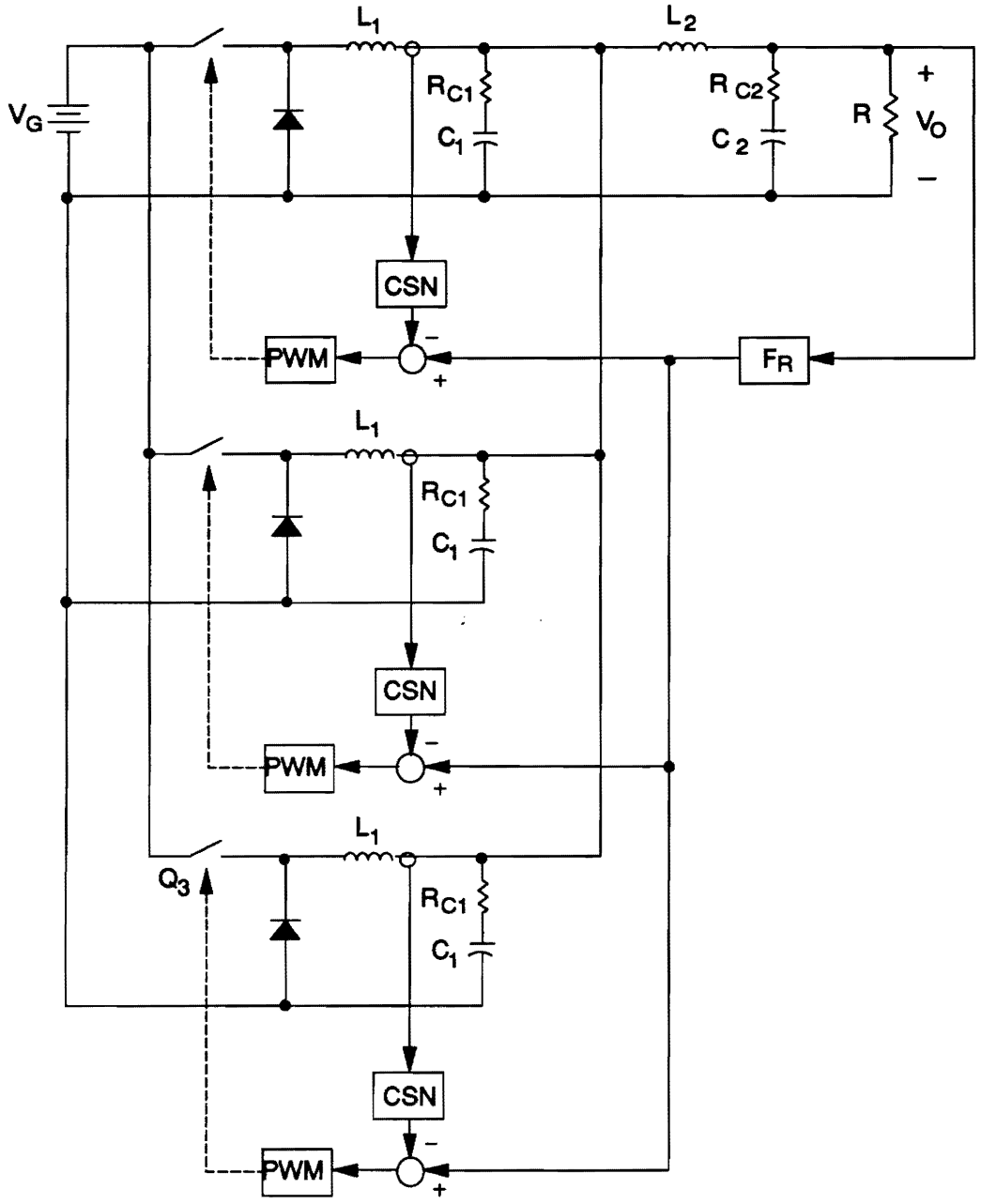


Fig. 2.16. Three-module buck converter with two-loop current-mode control: $L_1 = 24\,\mu H$, $L_2 = 1\,\mu H$, $C_1 = 867\,\mu F$, $C_2 = 12000\,\mu F$, $R_{C1} = 21\,m\Omega$, $R_{C2} = 6\,m\Omega$, $R = 0.05\,\Omega$, $V_G = 12\,V$, $V_O = 5\,V$.

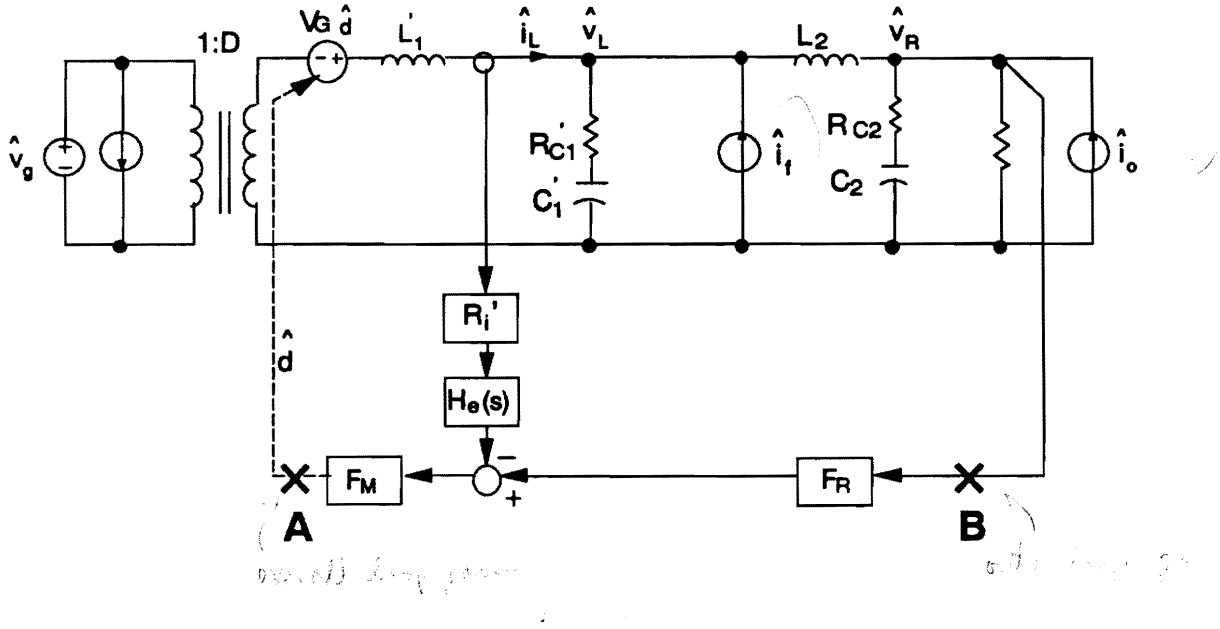


Fig. 2.17. Equivalent single-module model for Fig. 2.16: $L'_1 = L_1/3$, $R'_{C1} = R_{C1}/3$, $C'_1 = 3C_1$, $R'_i = R_i/3$.

transfer function called trans-impedance, defined as $Z_T = \hat{v}_R/\hat{i}_f$, represents the output voltage response due to the current disturbance at the summing junction. The trans-impedance is a useful tool for characterizing and improving module-failure response. The other performance criteria include audio-susceptibility, $A_U = \hat{v}_R/\hat{v}_g$, output impedance, $Z_O = \hat{v}_R/\hat{i}_O$, loop gain measured at "A" (overall loop gain), and loop gain measured at "B" (outer loop gain).

Reference [E5] provided design procedures for two-loop current-mode control for a single-module converter with a secondary LC filter. These procedures can be directly adapted to the multi-module converter using the equivalent single-module model of Fig. 2.17. However, as will be shown in this section, the two-loop control scheme does not offer any means of controlling the secondary filter resonance, and the system must compromise the closed-loop performance to achieve adequate stability margins.

Overall Loop Gain

The limitations of a two-loop control can be best demonstrated using the overall loop gain. The overall loop gain, T_1, is given by a vector sum of two individual feedback loops [D2]:

$$T_1 = T_I + T_R$$

where T_I is the feedback path created by the inductor current feedback and T_R is the feedback path created by the output voltage feedback.

Figure 2.18(a) shows the asymptotic plot of the overall loop gain of a two-loop controlled system. T_I has a -90° phase lag at high frequencies, and T_R experiences a rapid phase change from -180° to -360° around the resonant frequency of the secondary LC filter, f_{o3} in Fig. 2.18(a). Thus at f_{o3}, the phases of T_I and T_R are -180° apart and the overall loop gain shows a dip, as illustrated in Fig. 2.18(b).

The dip in the overall loop gain produces a high-frequency peaking in closed-loop transfer functions of the system, as will be discussed in Section 2.5.2. If T_R is increased to improve the system performance, the dip becomes deeper resulting in a severe peaking. When T_R is further increased until its magnitude at f_{o3} is the same as that of T_I, the dip is infinite and the system becomes unstable. To avoid an excessive dip or instability, the frequency where $|T_I| = |T_R|$ (denoted as f_c in Fig 2.18 (a)) must occur well below the secondary filter resonance. This is a demanding constraint on control design and prevents a further improvement of the system performance.

Outer Loop Gain

The limitations of the two-loop control can also be explained using the outer loop gain. The outer loop gain, T_2, is given by a ratio of two individual feedback loops [D2]:

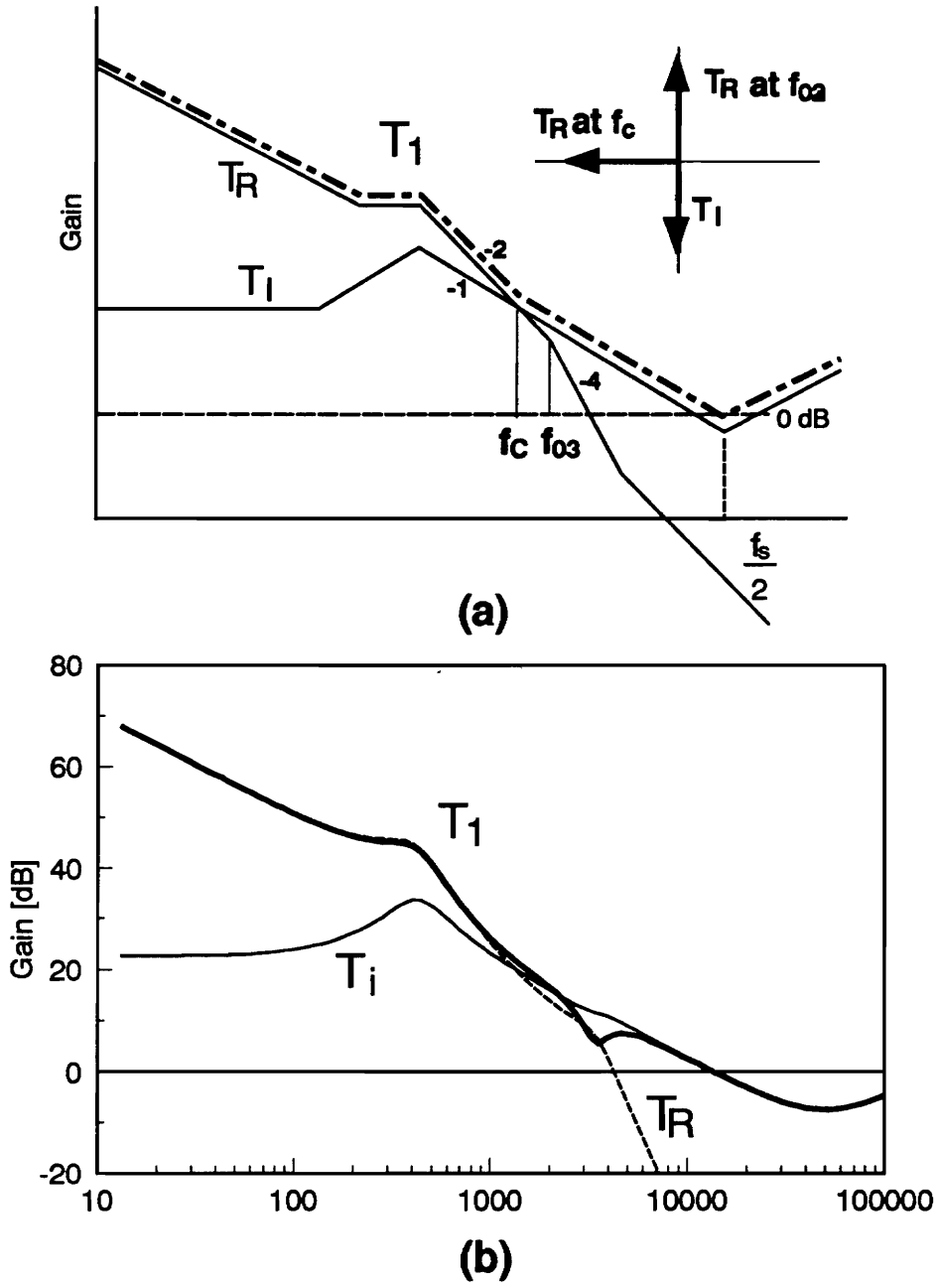


Fig. 2.18. Overall loop gain of two-loop controlled system: (a) Asymptotic plot. (b) Actual loop gain: A dip occurs at the second filter resonance.

$$T_2 = \frac{T_R}{1 + T_I}$$

Figure 2.19 shows the outer loop gain of the system. The resonance between L_2 and C_1 (f_{o3} in Figs. 2.18(a) and 2.19(a)) is apparent in the loop gain, imposing direct constraints on the control loop design. Since this resonance causes an additional phase delay of 180°, the zero dB crossover of the loop gain, f_c, should occur well before the resonant frequency to ensure an adequate phase margin. Any further increase in the feedback gains to improve the closed-loop performance pushes the crossover frequency toward the resonant frequency and rapidly reduces the phase margin. This is consistent with the results of the overall loop gain analysis. Since the crossover frequency of T_2 occurs the frequency where $|T_I| = |T_R|$, the stability criterion of $f_c >> f_{o3}$ applies for both T_2 and T_1.

Instability Due to the Secondary Filter Resonance

Figure 2.20 shows the loop gains of a two-loop controlled system whose voltage feedback gain is large enough to violate the condition for stability: $f_c > f_{o3}$ for this case. As shown in Fig. 2.20, both the overall loop gain and the outer loop gain apparently reveal instability. If there is no secondary LC filter, however, this design would provide a high performance without any instability problem. This clearly shows the need for a new control scheme which could provide both high performance and stability at the presence of the secondary LC filter.

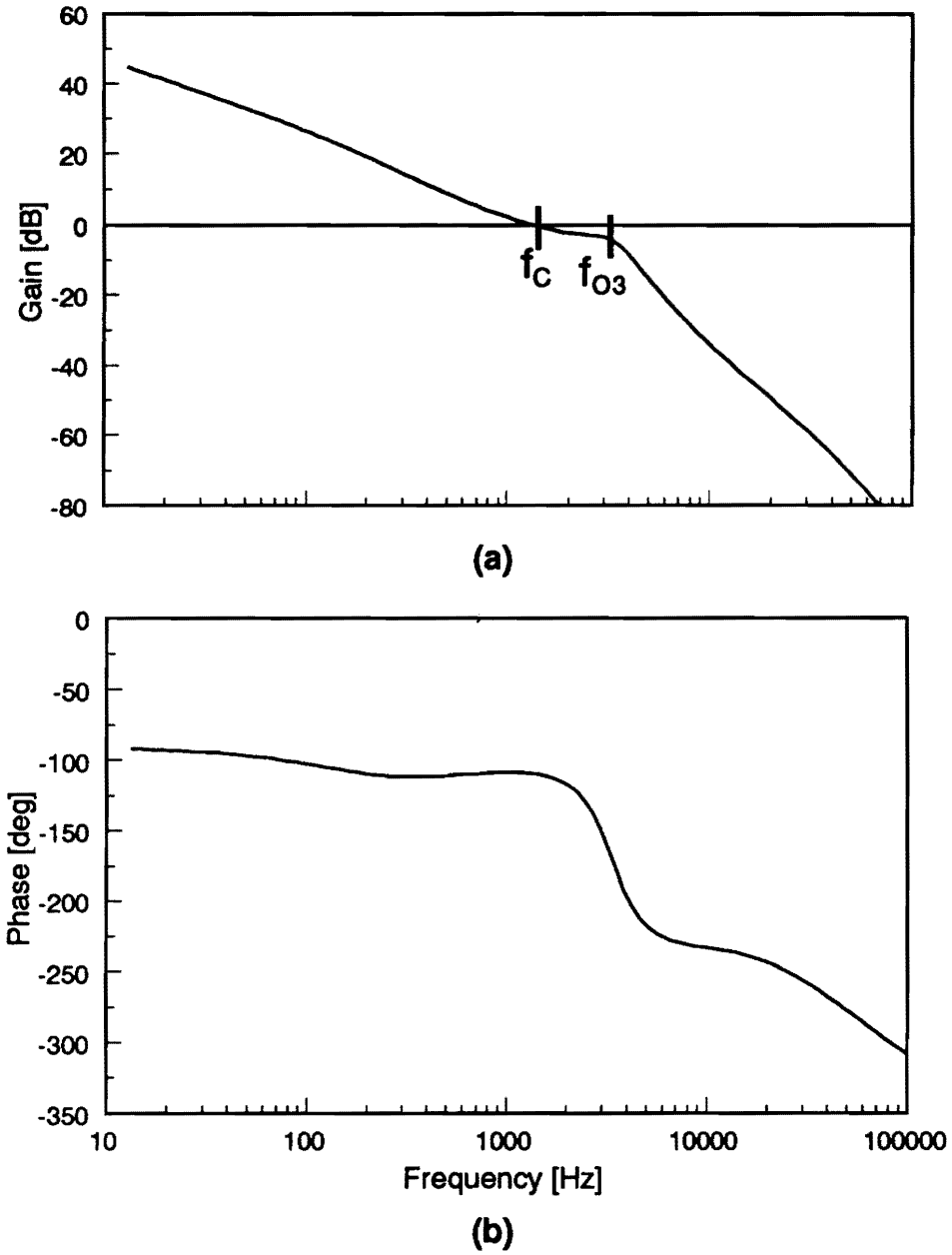


Fig. 2.19. Outer loop gain of two-loop controlled system: (a) Gain. (b) Phase: The resonance between L_2 and C'_1 is apparent in the loop gain. For stability, the crossover should occur well before the resonant frequency.

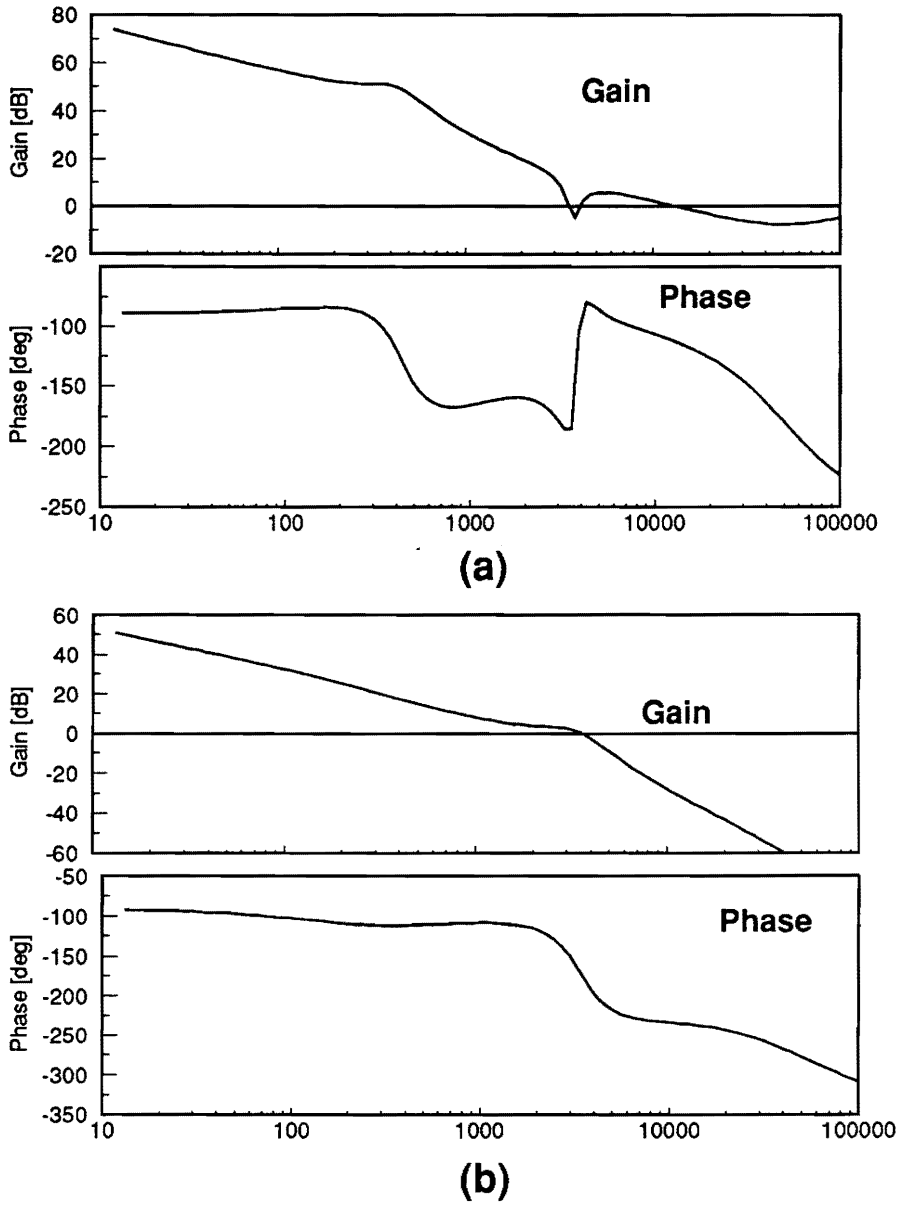


Fig. 2.20. Instability due to the secondary LC filter: (a) Overall loop gain. (b) Outer loop gain.

Audio-Susceptibility, Trans-Impedance, and Module-Failure Response

Figure 2.21 shows closed-loop transfer functions of a properly designed two-loop controlled system. The audio-susceptibility (Fig. 2.21(a)) and trans-impedance (Fig. 2.21(b)) exhibit a peaking at high frequencies. This peaking is a result of the dip in the overall loop gain due to the secondary filter resonance, and it is inherent in two-loop control. The peaking in the audio-susceptibility degrades the input-to-output noise rejection characteristics. The peaking in the trans-impedance degrades the module-failure response of the system. The peak value of the trans-impedance is directly related to the maximum undershoot of the output voltage.

To evaluate the module-failure response of the converter, time-domain simulations are performed assuming the switch of the third module (Q_3 in Fig. 2.16) is stuck in the open circuit position at 0.2 mSec, and the failed module remains in the system with its switch open. Figure 2.22 shows the transient responses of the inductor currents of parallel modules and the output voltage. The inductor current of the failed module (Fig. 2.22(a)) decreases linearly until blocked by the freewheeling diode. The inductor currents of the operational modules (Fig. 2.22(b)) increase to supplement the load current of the failed module. Figure 2.22(c) shows the transient response of the output voltage. The output voltage exhibits an oscillatory behavior with a relatively large maximum undershoot of 0.33 V, due to the high-frequency peaking observed in the trans-impedance of Fig. 2.21(b).

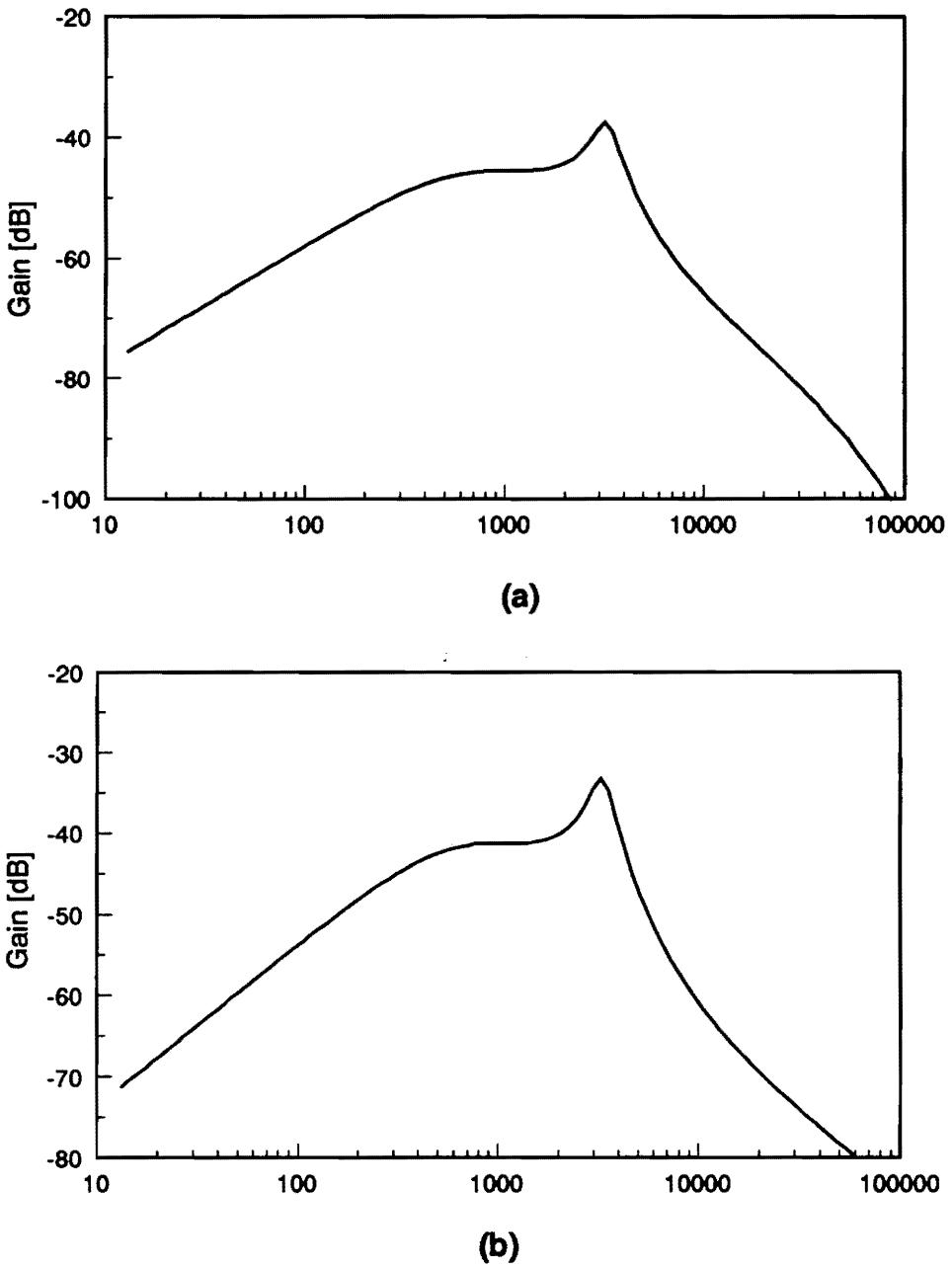


Fig. 2.21. Performance of two-loop controlled system: (a) Audio-susceptibility. (b) Trans-impedance: A peaking is apparent due to the resonance between converter modules and the secondary LC filter.

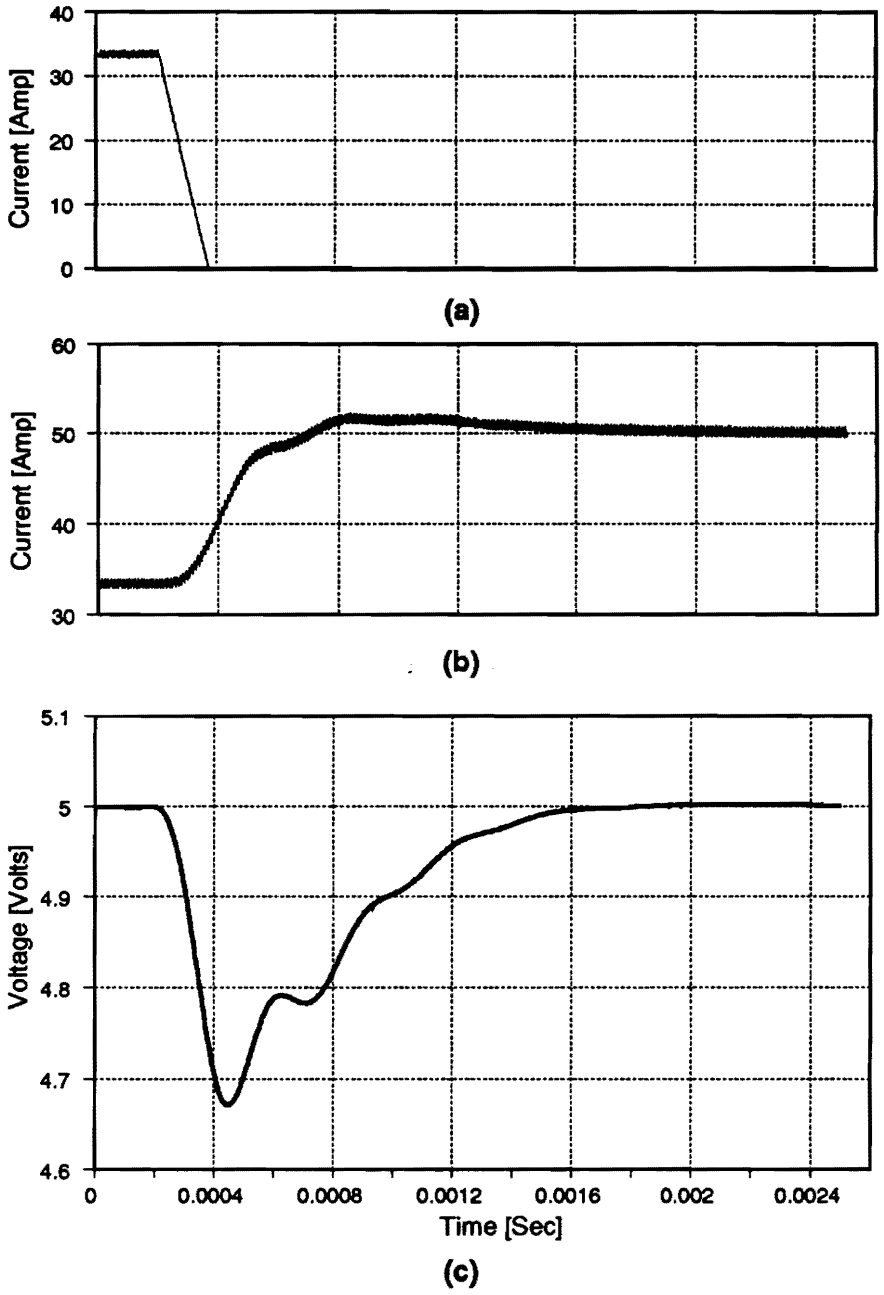


Fig. 2.22. Module-failure response of the two-loop controlled system: (a) Inductor current of failed module. (b) Inductor current of operational modules. (c) Output voltage: The output voltage shows a relatively large undershoot and an oscillatory behavior, reflecting the effects of the peaking in the trans-impedance.

2.5.2 Principles of Three-Loop Control

The three loop control scheme minimizes the detrimental effects of the secondary LC filter by employing an additional feedback from the output capacitor of each module. Figure 2.23 shows a three-module buck converter with the proposed three-loop control. In addition to CSN, each module has F_L for the voltage feedback from its output capacitor. The inner feedback from the output capacitor of each module is defined as the local voltage feedback, and the outer feedback from the output voltage of the converter is defined as the remote voltage feedback. Figure 2.24 shows the equivalent single-module model for Fig. 2.23. Using this model, the principles of the three-loop control are discussed with the emphasis on the use of local voltage feedback to improve closed-loop performance.

Open-Loop Analysis

To develop a three-loop control scheme, it is necessary to investigate the open-loop characteristics of the power stage. Transfer functions from the control variable, $\hat{d}$, to various feedback signals can be derived from the equivalent single-module model of Fig. 2.24:

$$F_4 \equiv \frac{\hat{v}_R}{\hat{d}} \sim \frac{V_G[1+sC'_1R'_{C1}][1+sC_2R_{C2}]}{[1+s(C_2R_{C2}+L'_1/R)+s^2L'_1C_2][1+sC'_1(R'_{C1}+R_{C2})+s^2L_2C'_1]}, \quad (2.9)$$

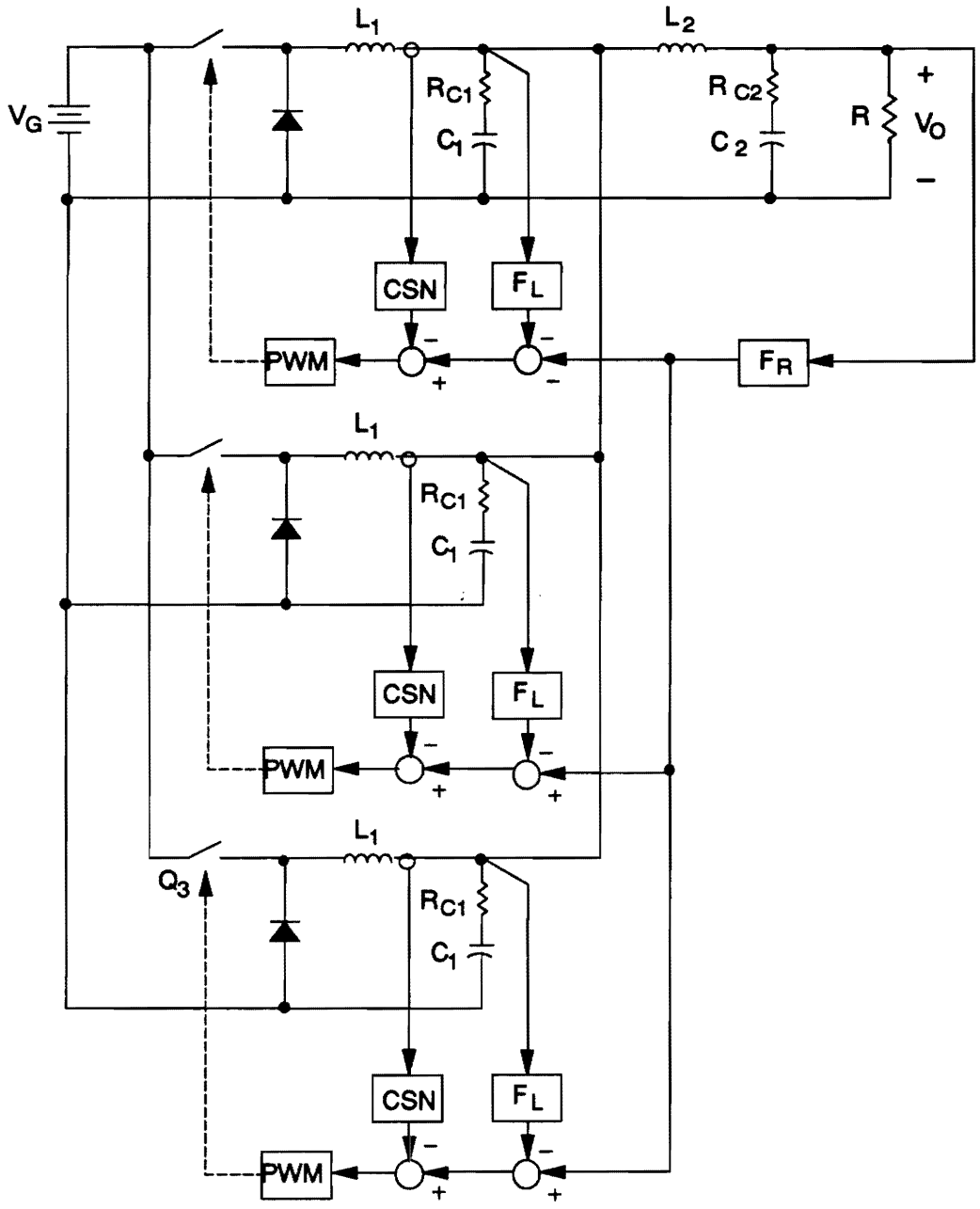


Fig. 2.23. Three-module buck converter with proposed three-loop control: Power stage parameters are identical to those of Fig. 2.16.

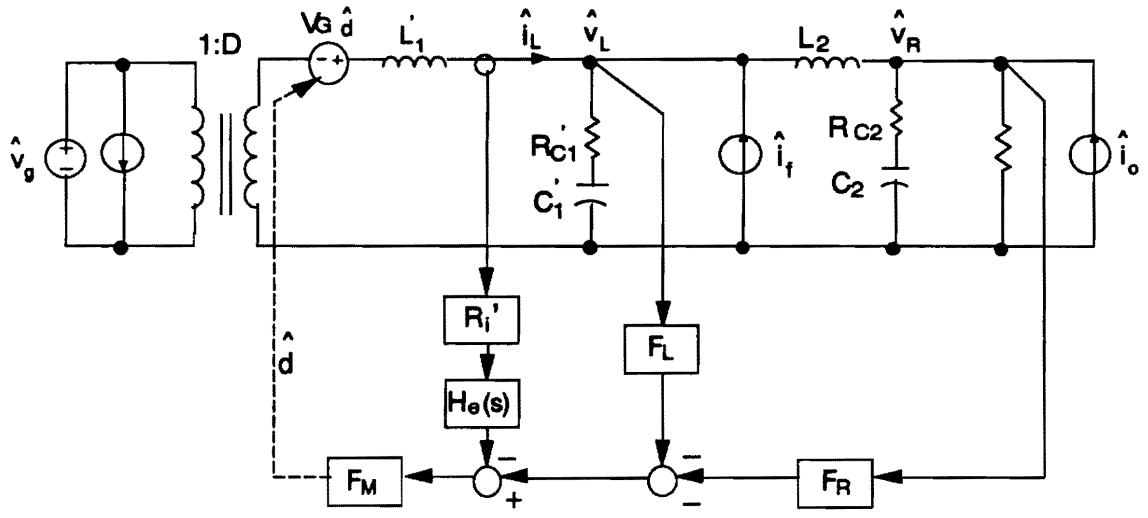


Fig. 2.24. Equivalent single-module model for Fig. 2.23: $L'_1 = L_1/3$, $R'_{C1} = R_{C1}/3$, $C'_1 = 3C_1$, $R'_i = R_i/3$.

$$F_8 \equiv \frac{\hat{v}_L}{\hat{d}} \sim \frac{V_G[1+sC'_1R'_{C1}][1+s(L_2/R+C_2R_{C2})+s^2L_2C_2]}{[1+s(C_2R_{C2}+L'_1/R)+s^2L'_1C_2][1+sC'_1(R'_{C1}+R_{C2})+s^2L_2C'_1]}, \quad (2.10)$$

$$F_{12} \equiv \frac{\hat{i}_L}{\hat{d}} \sim \frac{V_G[1+sC_2R]}{R[1+s(C_2R_{C2}+L'_1/R)+s^2L'_1C_2]}, \quad (2.11)$$

with assumptions that $L'_1 \gg L_2$, $C_2 \gg C'_1$, and $R \gg R'_{C1}$, R_{C2}. The conditions of $L'_1 \gg L_2$, $C_2 \gg C'_1$ not only make the analysis tractable but also are a good design practice. Being a combination of output filter inductor of converter module, L_1' is considerably larger than L_2 for most practical designs. The condition of $L_1' \gg L_2$ ensures an acceptable current ripple at the summing junction, and it allows the control-to-inductor current transfer function to be reduced to a second order. With $C_2 \gg C'_1$, the system maintains adequate stability margins with capacitive loadings [E5].

Figure 2.25(a) shows the asymptotic plots of the power stage transfer functions. The control-to-inductor current transfer function, $\hat{i}_L/\hat{d}$, is the same as that of the converter with a single-stage output filter of L'_1 and C_2. The control-to-remote voltage transfer function, $\hat{v}_R/\hat{d}$, has two resonances: the first between L'_1 and C_2 (f_{o1}), and the second between L_2 and C'_1 (f_{o3}). In the control-to-local voltage transfer function, $\hat{v}_L/\hat{d}$, there are the additional complex zeros determined by L_2 and C_2 (f_{o2}) besides the two resonances found previously. Due to these complex zeros, the transfer function has larger mid-band gain, and it can be used to overcome the drawbacks found in the two-loop controlled system.

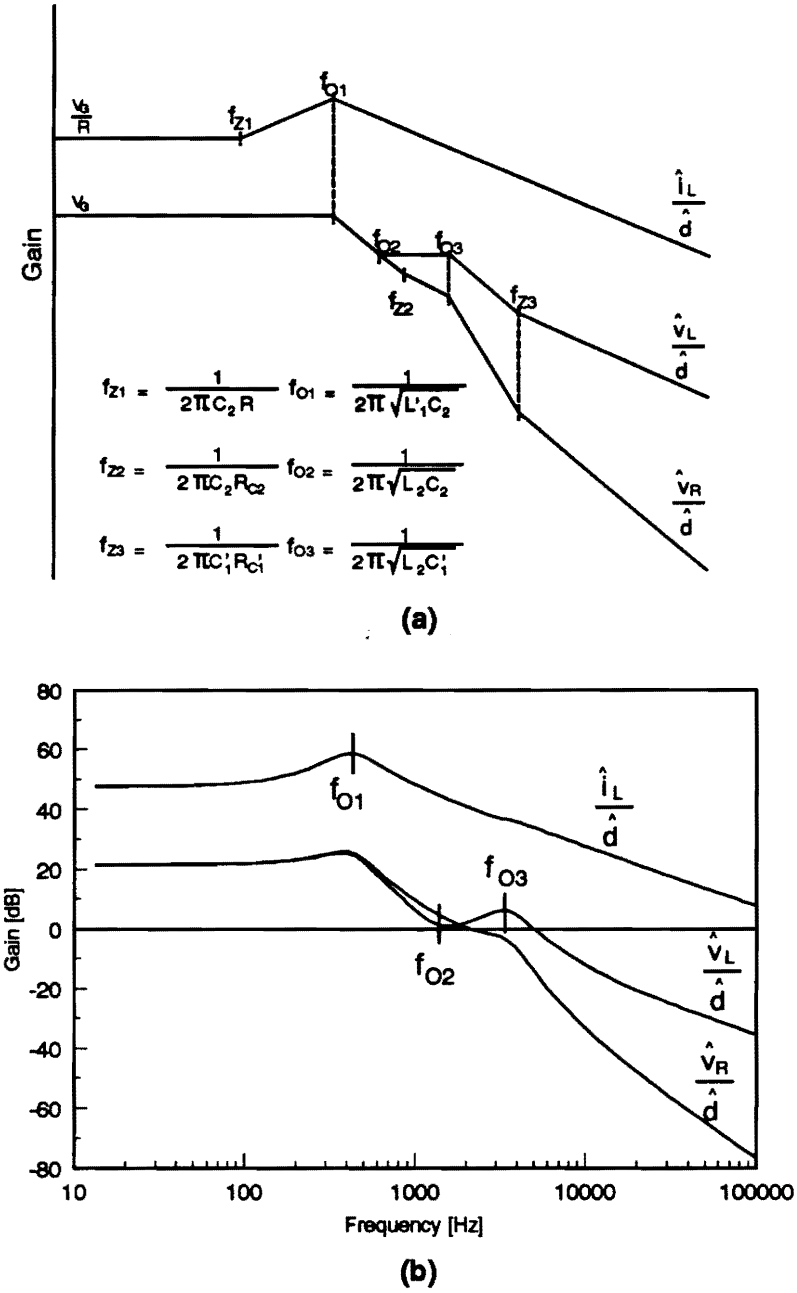


Fig. 2.25. Transfer functions from the duty cycle to various feedback signals: (a) Asymptotic plots. (b) Simulation results using the equivalent single-module model of Fig. 2.24.

Figure 2.25(b) shows the power stage transfer functions, obtained from computer simulations using the equivalent single-module model of Fig 2.24. The general shape and corner frequencies of the transfer functions are in good agreement with analytical predictions of Eqs. (2.9), (2.10), and (2.11).

Analysis of Three-Loop Control

Figure 2.26 shows the block diagram representation of the equivalent single-module model of Fig. 2.24. Gain blocks F_1 through F_{12} represent various open-loop transfer functions of the power stage. Figure 2.27 illustrates the principle of the three-loop control in comparison with a two-loop control. The current loop, T_I, local loop, T_L, and remote loop, T_R, represent the individual feedback loops associated with feedback signals:

$$T_I = F_M F_{12} R'_i H_e(s) \tag{2.12}$$

$$T_L = F_M F_8 F_L \tag{2.13}$$

$$T_R = F_M F_4 F_R \tag{2.14}$$

For the two-loop control, the remote loop is designed to be dominant at low frequencies for a good dc regulation, and the current loop is designed to be dominant at high frequencies to obtain the full benefits of current-mode control [D2]. The increase in current loop gain beyond half the switching frequency is the result of the sampling action

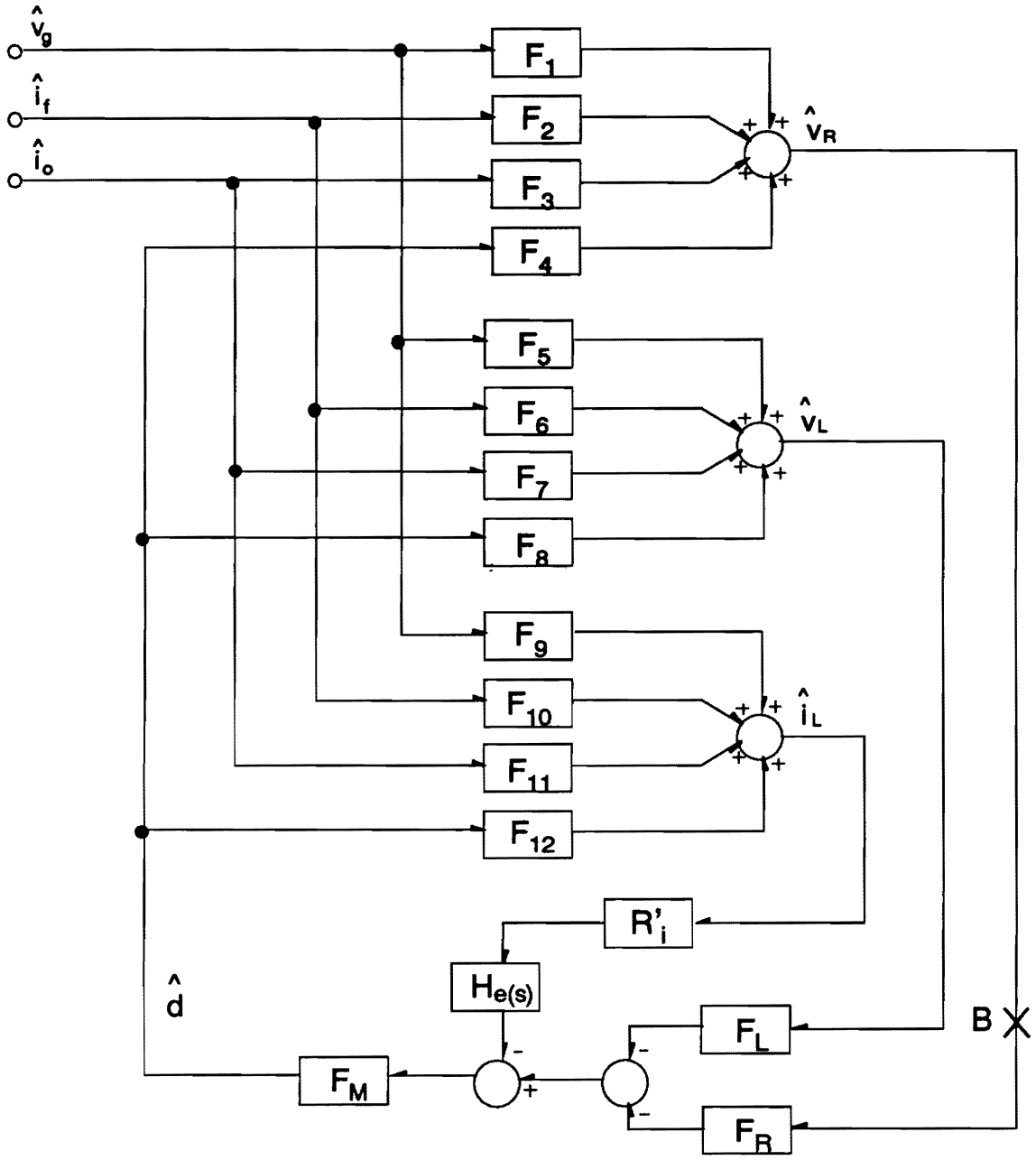


Fig. 2.26. Block diagram representation of the equivalent single-module model of Fig. 2.24: Gain blocks F_1 through F_{12} represent various open-loop transfer functions of the power stage, and the other blocks are feedback compensations and small-signal models of the controller.

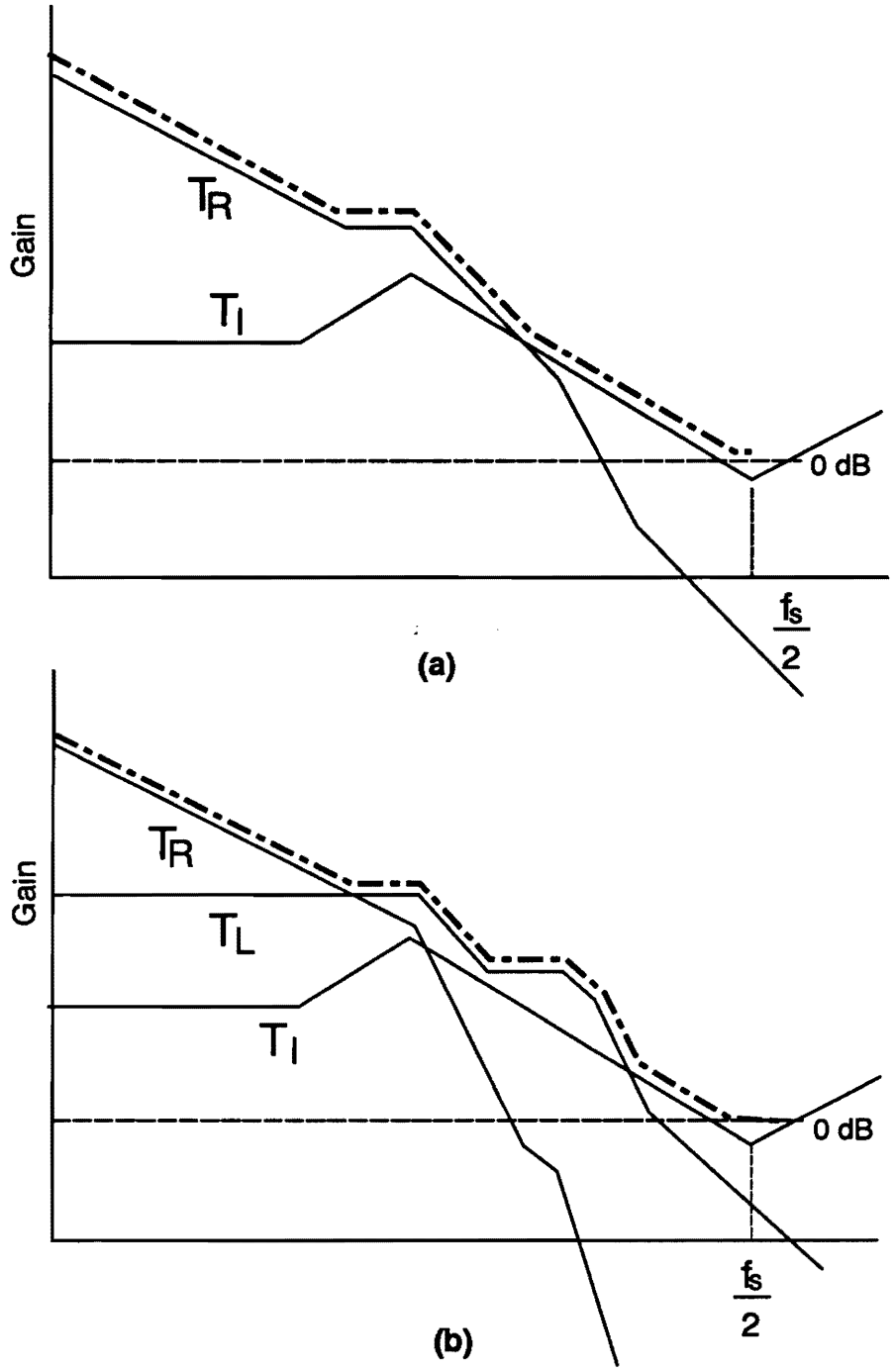


Fig. 2.27. Principles of three-loop control: (a) Two-loop control. (b) Three-loop control.

of the current-mode control [D7].

For the three-loop control, the remote loop is designed to be dominant at low frequencies, and the current loop is designed to be dominant at high frequencies, as is the case for two-loop control. In the mid-frequency band, however, the local loop is designed to prevail over the remote and current loops in order to nullify the detrimental effects of the resonance between L_2 and C'_1. The benefits of the local loop will be detailed in the next section.

Effects of Local Voltage Feedback

From the small-signal block diagram of Fig. 2.26, the audio-susceptibility, the trans-impedance, and the output impedance of the three-loop controlled system can be derived as:

$$A_U = \frac{F_1 + T_I\left(F_1 - \frac{F_9F_4}{F_{12}}\right) + T_L\left(F_1 - \frac{F_5F_4}{F_8}\right)}{1 + T_I + T_L + T_R}, \tag{2.15}$$

$$Z_T = \frac{F_2 + T_I\left(F_2 - \frac{F_{10}F_4}{F_{12}}\right) + T_L\left(F_2 - \frac{F_6F_4}{F_8}\right)}{1 + T_I + T_L + T_R}, \tag{2.16}$$

$$Z_O = \frac{F_3 + T_I\left(F_3 - \frac{F_{11}F_4}{F_{12}}\right) + T_L\left(F_3 - \frac{F_7F_4}{F_8}\right)}{1 + T_I + T_L + T_R}. \tag{2.17}$$

From the buck power stage model of Fig 2.24, it can be shown:

$$\frac{F_1}{F_4}=\frac{F_5}{F_8}=\frac{F_9}{F_{12}}=\frac{D}{V_G}, \qquad \frac{F_6}{F_8}=\frac{F_2}{F_4}=\frac{sL'_1}{V_G}, \tag{2.18}$$

which reduces Eqs. (2.15) and (2.16) to:

$$A_U=\frac{F_1}{1+T_I+T_L+T_R}, \tag{2.19}$$

$$Z_T=\frac{F_2+T_I\left(F_2-\frac{F_{10}F_4}{F_{12}}\right)}{1+T_I+T_L+T_R}. \tag{2.20}$$

The benefits of the local voltage feedback can be easily seen from Eqs. (2.19) and (2.20). The local loop directly improves the audio-susceptibility and trans-impedance, since T_L appears only in the denominators. However, in the output impedance of Eq. (2.17), T_L appears in both numerator and denominator. Thus its effect is not as significant as in the previous cases. The performance criteria of a two-loop controlled system can be directly derived from Eqs. (2.17), (2.19), and (2.20) by ignoring T_L.

The effects of the local loop on the trans-impedance, given by Eq. (2.20), are illustrated in Fig. 2.28. The numerator of the trans-impedance has two resonances: the first between L'_1 and C_2, and the second between L_2 and C'_1 (the middle curve in Figs. 2.28(a) and 2.28(b)). For the two-loop control case, the denominator of the trans-impedance (the upper curve in Fig. 2.28(a) which corresponds to the dotted line in Fig 2.27(a)) contains only the first resonance. Thus while the first resonance does not appear

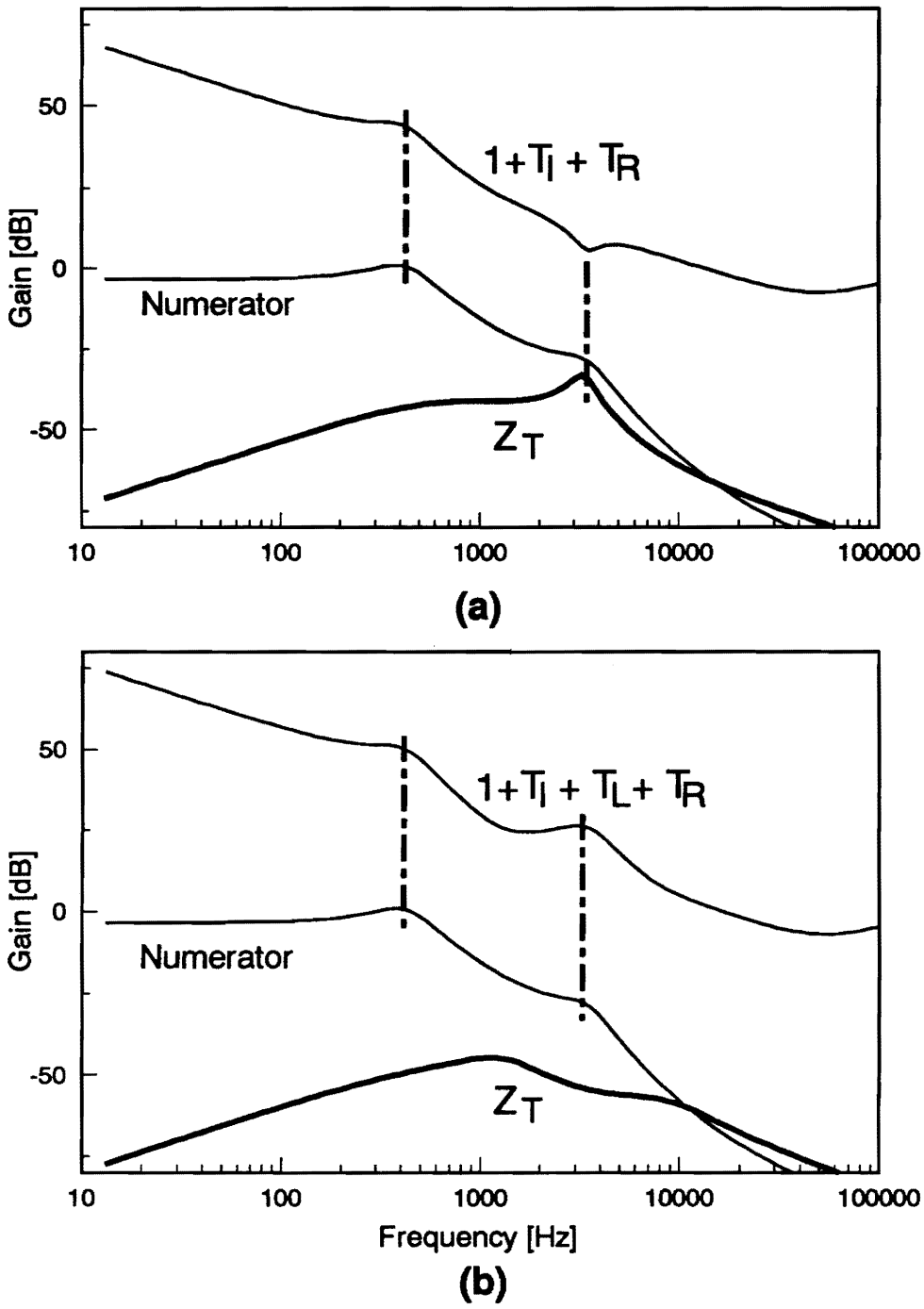


Fig. 2.28. Effects of local voltage feedback on the trans-impedance: (a) Two-loop control. (b) Three-loop control: Unlike the two-loop control, the three-loop control eliminates both low- and high-frequency resonances.

in the trans-impedance due to the cancelling between the numerator and denominator, the second resonance is still apparent. Furthermore, the dip in the denominator further amplifies the resonant peak, resulting in a high-frequency peaking.

On the other hand, for the three-loop control case, the denominator of the trans-impedance (the upper curve in Fig. 2.28(b) which corresponds to the dotted line in Fig. 2.27(b)) contains both the first and the second resonances. Consequently, both the first and the second resonances are cancelled, resulting in a much improved trans-impedance. The enhanced trans-impedance significantly improves the module-failure response, as will be demonstrated in Section 2.5.3.

The benefits of the local loop on the audio-susceptibility can be explained in a way similar to the case of the trans-impedance, and they are illustrated in Fig. 2.29.

Figure 2.30 shows the effects of the local loop on the outer loop gain. The outer loop gain measured at "B" in Fig. 2.26 can be derived as:

$$T_2 = \frac{T_R}{1 + T_I + T_L} \tag{2.21}$$

As in the case of the trans-impedance and audio-susceptibility, the numerator of the loop gain (the dotted line in Figs 2.30(a) and (b)) contains two resonances. For two-loop control (Fig. 2.30(a)), the denominator of the loop gain (the middle curve in Fig. 2.30(a)) contains only the first resonance. Consequently, the first resonance does not appear in the loop gain, but the second resonance is apparent in the loop gain. Since this resonance causes a -180° phase delay, the crossover of the loop gain should occur well

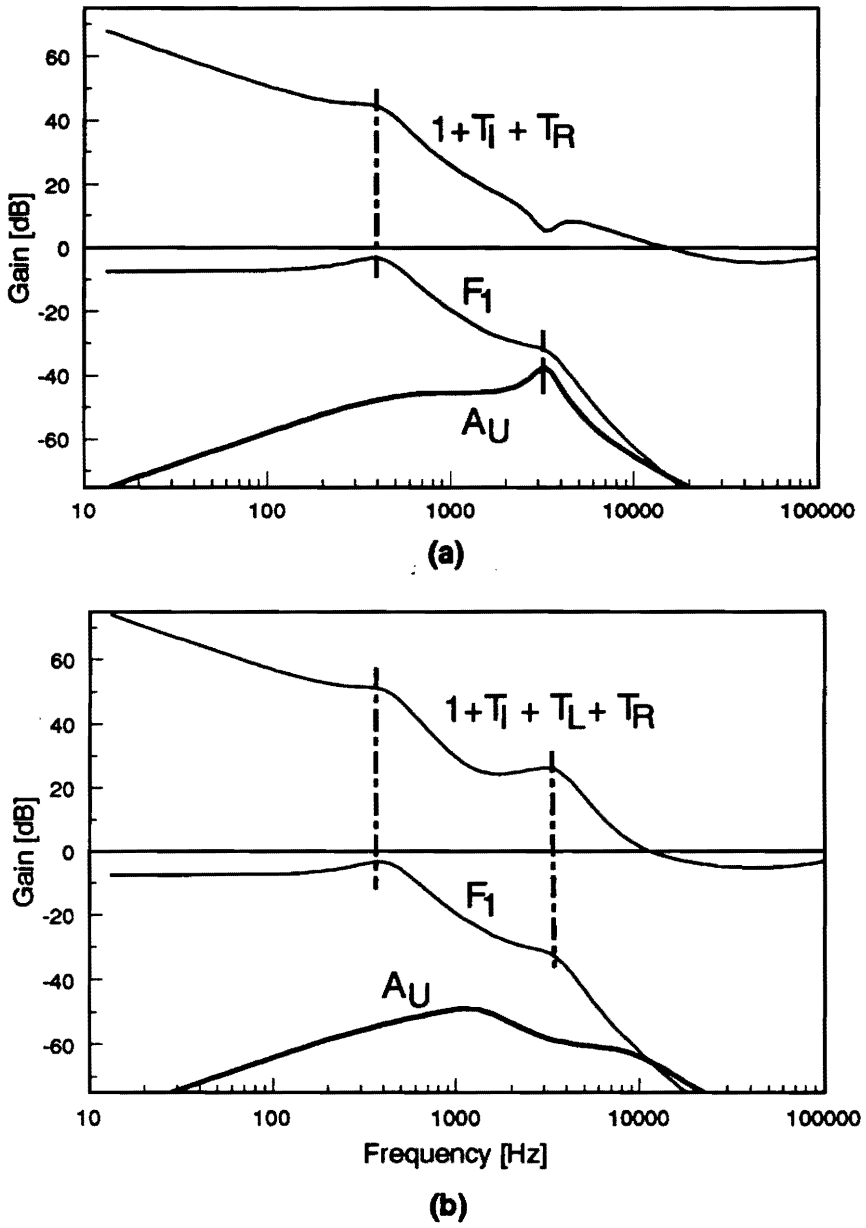


Fig. 2.29. Effects of local voltage feedback on the audio-susceptibility: (a) Two-loop control. (b) Three-loop control: Unlike the two-loop control, the three-loop control eliminates both low- and high-frequency resonances, resulting in a much improved audio-susceptibility.

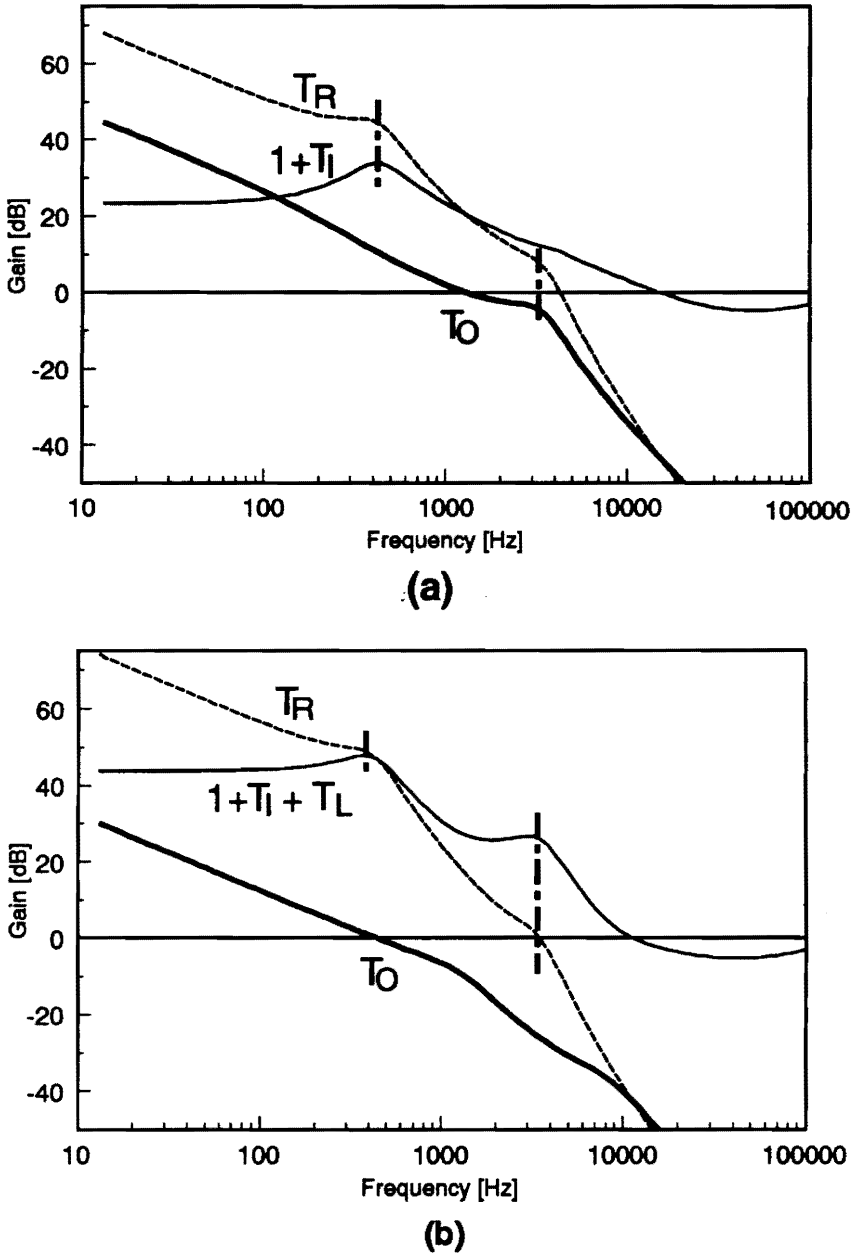


Fig. 2.30. Effects of local voltage feedback on the outer loop gain: (a) Two-loop control. (b) Three-loop control: The three-loop control minimizes any detrimental effects of the secondary LC filter on the loop gain.

before the second resonant frequency. On the other hand, for three-loop control (Fig. 2.30(b)), the denominator of the loop gain (the middle curve in Fig. 2.30(b)) contains both the first and the second resonance. In this case, both the first and the second resonances do not appear in the loop gain, and the secondary LC filter does not impose any direct constraint on the control design.

Depending on the control scheme, the crossover frequency of the outer loop gain has different implications. The crossover frequency of the two-loop control occurs when $|T_I| = |T_R|$ and the crossover frequency of the three loop control occurs when $|T_I + T_L| = |T_R|$. Thus although the three-loop controlled system offers a much enhanced closed-loop performance, it shows a much reduced crossover frequency of the outer loop gain.

Figure 2.31 shows the loop gains of the three-loop controlled system in comparison with those of a two-loop controlled system. Note that the compensations for two-loop control is tailored to offer the same overall loop gain characteristics as those of the three-loop control at both low and high frequencies. While the three-loop control offers both high feedback gain and stability, the two-loop controlled system reveals instability in both overall loop gain and outer loop gain. This demonstrates the benefits of the local voltage feedback and the superiority of the three-loop control.

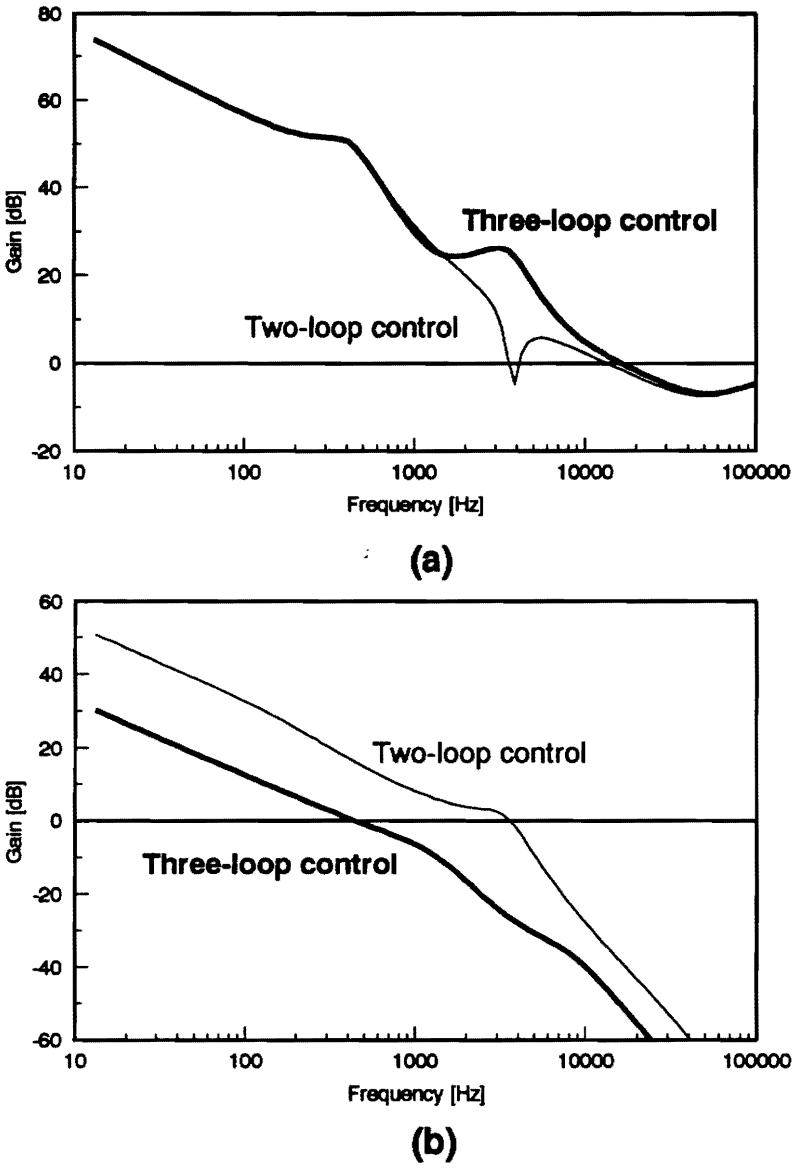


Fig. 2.31. Comparison with two-loop control: (a) Overall loop gain. (b) Outer loop gain.

Feedback Compensation for Three-Loop Control

The feedback compensation for a three loop control, together with design guidelines using the equivalent single-module model, is given as follows:

Current sensing network gain, R'_i, and *modulator gain*, F_M.

For the full benefits of current mode control, R'_i and F_M should be selected to provide a sufficiently high crossover frequency for T_I. Since the control-to-inductor current transfer function is the same as that of the converter with a single-stage output filter, T_I can be optimized independently from the high frequency resonance. The equivalent current sensing network gain for the k-module system is $R_i = k R'_i$.

Local voltage feedback compensation: $F_L = \dfrac{K_L}{(1 + s/\omega_p)}$.

K_L should be selected to provide sufficient mid-frequency gain of T_L, while maintaining the dominance of the current loop at high frequencies. A pole, ω_p, is placed after the resonance between L_2 and C'_1 to reduce the high-frequency gain.

Remote voltage feedback compensation: $F_R = \frac{K_R}{s}$.

An integrator is employed to provide good dc regulation of the output voltage. The integrator gain, K_R, determines the low-frequency attenuation of the closed-loop transfer functions.

2.5.3 Performance of Three-Loop Controlled Systems

Figures 2.32 through 2.35 show various performance criteria of the three-loop controlled system in comparison with those of a two-loop controlled system. The compensation parameters for three-loop control are given in Table 2.5.

The three-loop control provides significant improvements in the system performance. The peaking in audio-susceptibility (Fig. 2.32(a)) and trans-impedance (Fig. 2.32(b)) is eliminated, and the low- and mid-frequency gains of the transfer functions are reduced. In particular, for the case of the module failure (Fig. 2.33(b)), the maximum undershoot of the output voltage is reduced to 0.16 V. By comparing Figs. 2.33(a) and 2.33(b), the effects of the local voltage feedback on the module-failure response can be best understood. By eliminating the peaking in trans-impedance, the three-loop control offers a much smaller undershoot and a faster response.

As shown in Fig. 2.34, the outer loop gain of the three-loop controlled system is not affected by the resonance between L_2 and C'_1, and it maintains the phase delay of

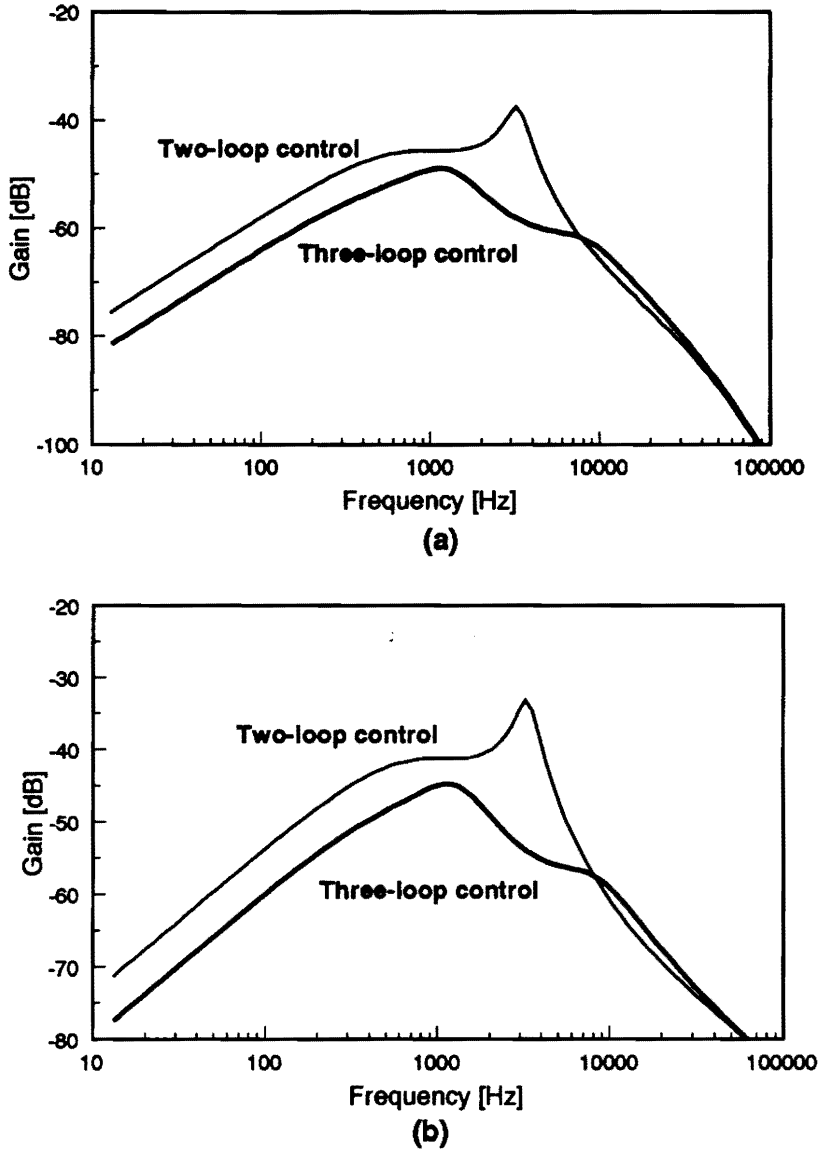


Fig. 2.32. Performance of the three-loop controlled converter: (a) Audio-susceptibility. (b) Trans-impedance.

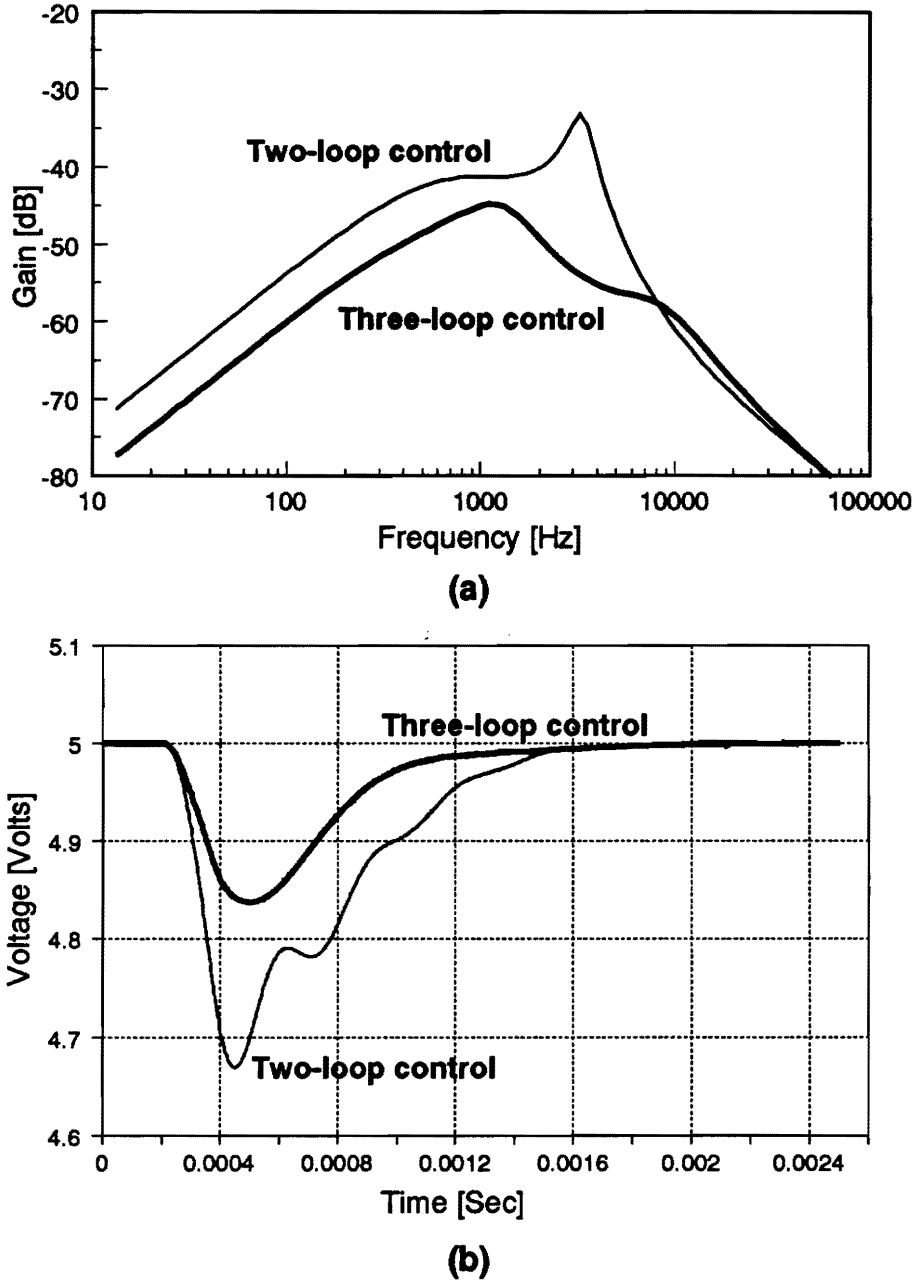


Fig. 2.33. Performance of the three-loop controlled system: (a) Trans-impedance. (b) Module-failure response: By eliminating the peaking in the trans-impedance, the three-loop control offers a much improved module-failure response.

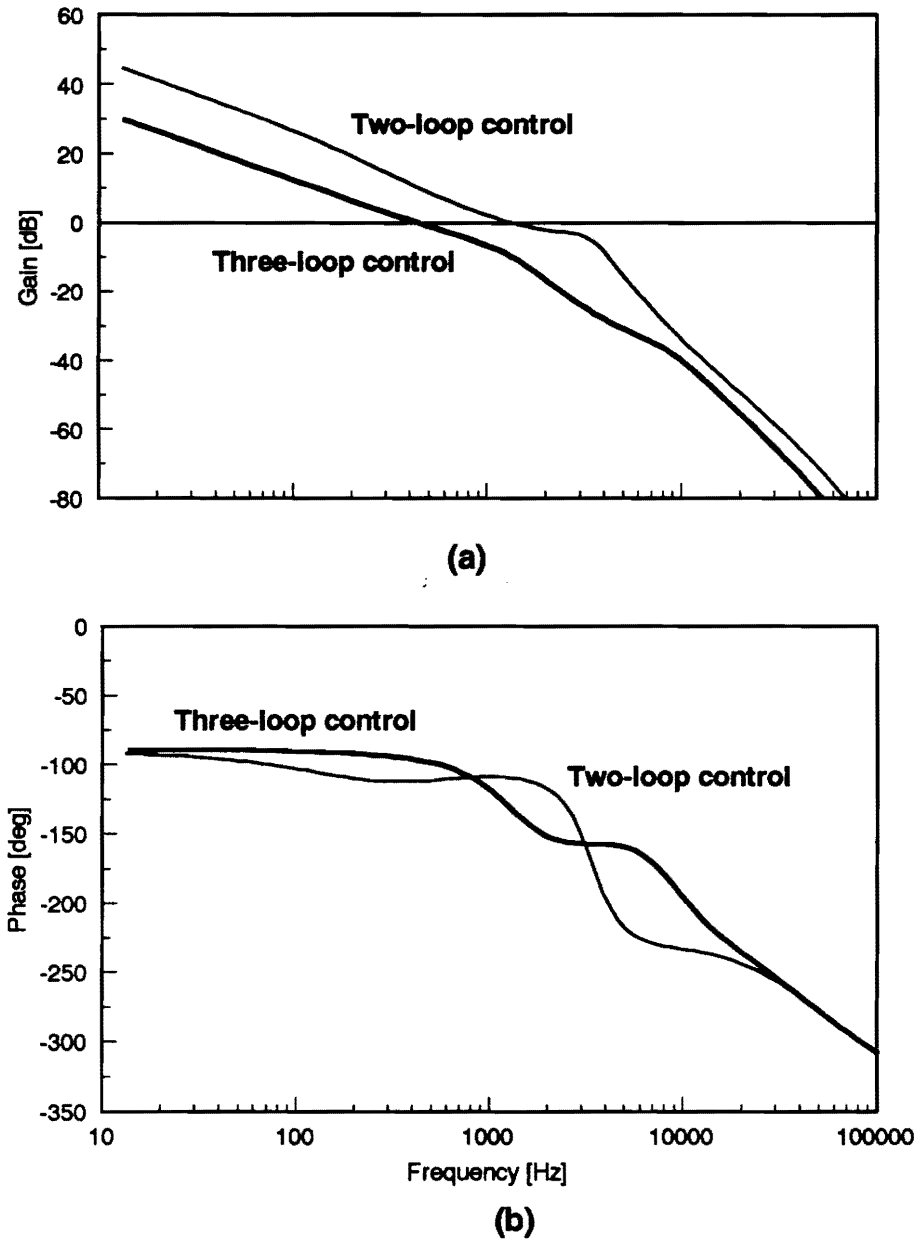


Fig. 2.34. Outer loop gain of the three-loop controlled system: (a) Gain. (b) Phase.

$-90°$ up to the crossover frequency. This allows a significant improvement in the closed-loop performance, maintaining a larger phase margin than for two-loop control. Finally, Fig. 2.35(a) compares the output impedances of the two systems. While the local voltage feedback does not significantly affect the output impedance at high frequencies, it improves the low- frequency characteristics. Figure 2.35(b) compares the transient response of the output voltage due to the step load change from 100 A to 67 A. As predicted from Fig. 2.35(a), the three-loop controlled system shows a much faster response with the higher corner frequency of the output impedance.

To summarize this section, comparisons between two-loop control and three-loop control schemes are given in Table 2.5.

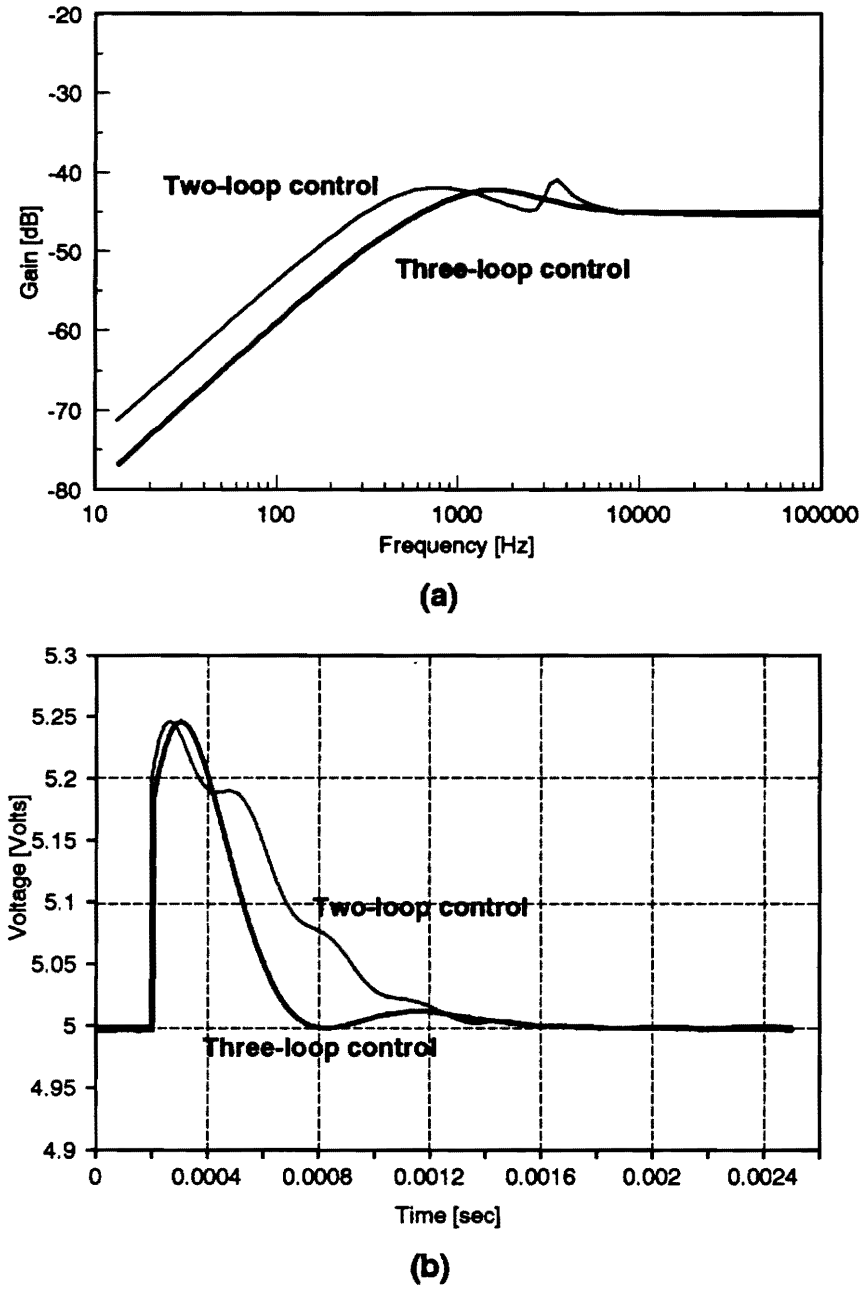


Fig. 2.35. Performance of the three-loop controlled system: (a) Output impedance. (b) Transient response of the output voltage due to the step load change 100 A to 67 A.

Table 2.5 : Summary of two control schemes

	Individual loop gains	Compensation parameters	Closed-loop performance
Two-loop control	$T_I = F_M F_{12} R'_i H_e(s)$ $T_L = 0$ $T_R = F_M F_4 F_R$	$R_i = 0.548$ $F_L = 0$ $F_R = \frac{58182(1+s/2753)}{s(1+s/13900)}$	$A_U = \frac{F_1}{1+T_I+T_R}$ $Z_T = \frac{F_2 + T_I\left(F_2 - \frac{F_{10}F_4}{F_{12}}\right)}{1+T_I+T_R}$ $Z_O = \frac{F_3 + T_I\left(F_3 - \frac{F_{11}F_4}{F_{12}}\right)}{1+T_I+T_R}$
Three-loop control	$T_I = F_M F_{12} R'_i H_e(s)$ $T_L = F_M F_8 F_L$ $T_R = F_M F_4 F_R$	$R_i = 0.548$ $F_L = \frac{40}{(1+s/23900)}$ $F_R = \frac{116400}{s}$	$A_U = \frac{F_1}{1+T_I+T_L+T_R}$ $Z_T = \frac{F_2 + T_I\left(F_2 - \frac{F_{10}F_4}{F_{12}}\right)}{1+T_I+T_L+T_R}$ $Z_O = \frac{F_3 + T_I\left(F_3 - \frac{F_{11}F_4}{F_{12}}\right) + T_L\left(F_3 - \frac{F_7F_4}{F_8}\right)}{1+T_I+T_L+T_R}$
For both two-loop and three loop controls: $F_M = 0.293, \quad H_e(s) = 1 + \frac{s}{\omega Q} + \frac{s^2}{\omega^2}, \quad Q = -2/\pi, \quad \omega = \pi \times 10^5$			

2.6 SUMMARY

This chapter established two major modeling and control techniques for multi-module converter systems: a new procedure to obtain an equivalent single-module model, and an advanced three-loop control scheme. The results of this chapter constitute underlying bases for the analysis and design of more complex power systems covered in Chapters 3 and 4.

The new approach to deriving an equivalent single-module model relies on the concept of PWM switch model and standard circuit analysis techniques. The approach can be readily adapted to a wide class of multi-module converters including resonant converters, and does not require any complex analytical manipulation. Once the derivation steps are fully understood, the equivalent single-module model can be obtained, in many cases, by an inspection.

It is not surprising that the equivalent single-module model produces the exactly same performance as the original multi-module system. A multi-module converter is a non-minimal order system due to the symmetry in its structure. A non-minimal system can be reduced to a minimal order system, the equivalent single-module model, keeping all input-to-output characteristics unchanged. The performance criteria of a converter, such as audio-susceptibility, output impedance, and transient responses due to line and load variations, are the input-to-output characteristics. Thus the equivalent single-module model retains all dynamics necessary to design the controller and produces the same performance criteria as the multi-module system.

The secondary LC filter, widely used in low-voltage applications, introduces an additional resonance, which adversely affects the closed-loop performance of a multi-module converter. A two-loop current-mode control does not offer any means of controlling this resonance, and the result could be poor module-failure response and small-signal performance. To overcome the limitations of the two-loop control, a three-loop control scheme is proposed for multi-module converters with a secondary LC filter. The basic idea of the three-loop control is to compensate for the detrimental effects of the secondary filter using the local voltage feedback signal which carries all information about the secondary filter resonance. The three-loop control offers significant improvements in module-failure response and other performance criteria without compromising any stability criteria. The structure of and the design procedures for three-loop compensation are no more complicated than those of a two-loop control, while providing a much enhanced performance.

CHAPTER 3

STACKED POWER SYSTEMS

3.1 INTRODUCTION

Stacked power systems denote a class of power conditioning architectures which employ a stacked configuration of several single-output converters to power multiple loads. To illustrate the concept of the stacked power system, Fig. 3.1 compares two different approaches to the same multiple-output application. In Fig. 3.1(a), the power conversion is performed by two stand-alone converters. In Fig. 3.1(b), Converter 1 and Converter 2 are stacked together and collectively meet the same requirements. In this stacked power system, R_1 receives the load current from both Converter 1 and Converter 2, and R_2 utilizes the voltage difference between the output of Converter 2 and the output of Converter 1 to obtain an output voltage of 0.7 V.

The stacked power architecture offers two major advantages in low-voltage high-current applications. The first is a significant improvement in the overall efficiency. In Fig. 3.1(a), Converter 1 delivers 400 A of current at the output voltage of 1.4 V, and Converter 2 delivers 200 A of current at the output voltage of 0.7 V. In this case, the loss associated with the internal voltage drop in the output diode (0.4 V for a Schottky diode) and the load current of two converters (600 A) is 240 W. In the stacked architecture of Fig. 3.1(b), each converter delivers 200 A of current for the same load requirements. The loss associated with the voltage drop in the diode (0.4 V) and the load current of two converters (400 A) is 160 W, only 67 % of the power loss of the previous case.

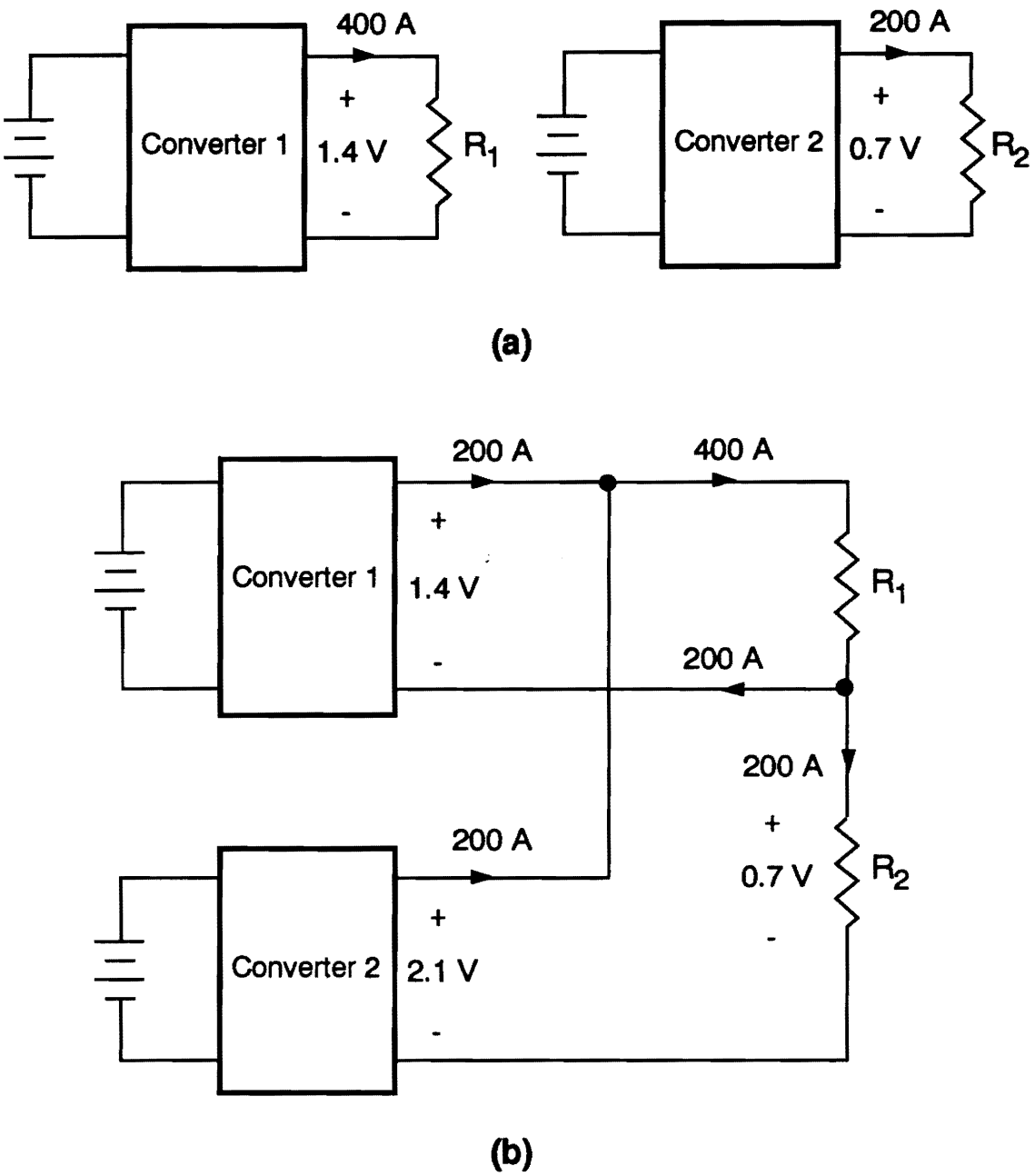


Fig. 3.1. Two different approaches to the same application: (a) Two stand-alone converters. (b) Stacked power system.

The second benefit of stacked architecture is the generation of an arbitrary low-voltage output using the voltage difference between outputs of two converters. Recently, the stacked architecture has been successfully adapted to mainframe computer power systems [C2,C4], which must provide several ultra low-voltage outputs at ultra high-current levels.

The primary concern in designing a stacked power system is to characterize various dynamic interactions among stacked converters and to incorporate their impacts into the control. Any design attempt not furnished with this prerequisite would result in a system with unacceptable dynamics. Based on a comprehensive system level analysis, this chapter presents systematic design procedures for stacked power systems which naturally incorporate all subsystem interactions and optimize the overall performance of the entire system.

Section 3.2 discusses structural considerations for stacked power systems. Constraints on the system architecture are explained in terms of voltage and current requirements of the loads. A general approach to constructing a stacked configuration for a given load profile is presented. Section 3.3 addresses load characteristics of a converter in a stacked power system, focusing on their impacts on the control design. The concept of ac load and dc load is established to allow a stacked power system to be decomposed into individual converters. A design strategy to optimize the overall performance of the entire system is developed. Section 3.4 presents the analysis and design of the stacked power system developed for the IBM390 mainframe computer. This section details all analysis and design issues necessary to optimize the dynamic performance of a practical stacked power system.

3.2 CONSTRUCTION OF STACKED POWER SYSTEMS

To construct a feasible stacked power architecture for a given load profile, both voltage and current distributions among loads must be considered simultaneously. KVL applied to load voltages determines the lower limit of the number of converters to be stacked, and the current distribution among loads determines the structure of the system.

Figure 3.2 shows the current and voltage distributions in a three-stage stacked power system. Assuming $V_3 > V_2 > V_1$, KVL requires the conditions:

$$V_{BC} = V_{AC} - V_{AB} \tag{3.1}$$

$$V_{BD} = V_{AD} - V_{AB} \tag{3.2}$$

$$V_{CD} = V_{AD} - V_{AC} \tag{3.3}$$

Also, the condition of a unidirectional power processing in each converter requires:

$$I_{AB} > I_{BC} + I_{BD} \tag{3.4}$$

$$I_{BC} + I_{AC} > I_{CD} \tag{3.5}$$

If the voltage and current profile of six loads satisfies Eqs. (3.1) through (3.5), only three converters are necessary to form a stacked configuration. Otherwise, a larger number of converters (> 3) are necessary to form a feasible configuration. The observations made in this example can be generalized as follows, in order to determine the lower limit of the number of converters:

$$N_C = N_L - N_D \tag{3.6}$$

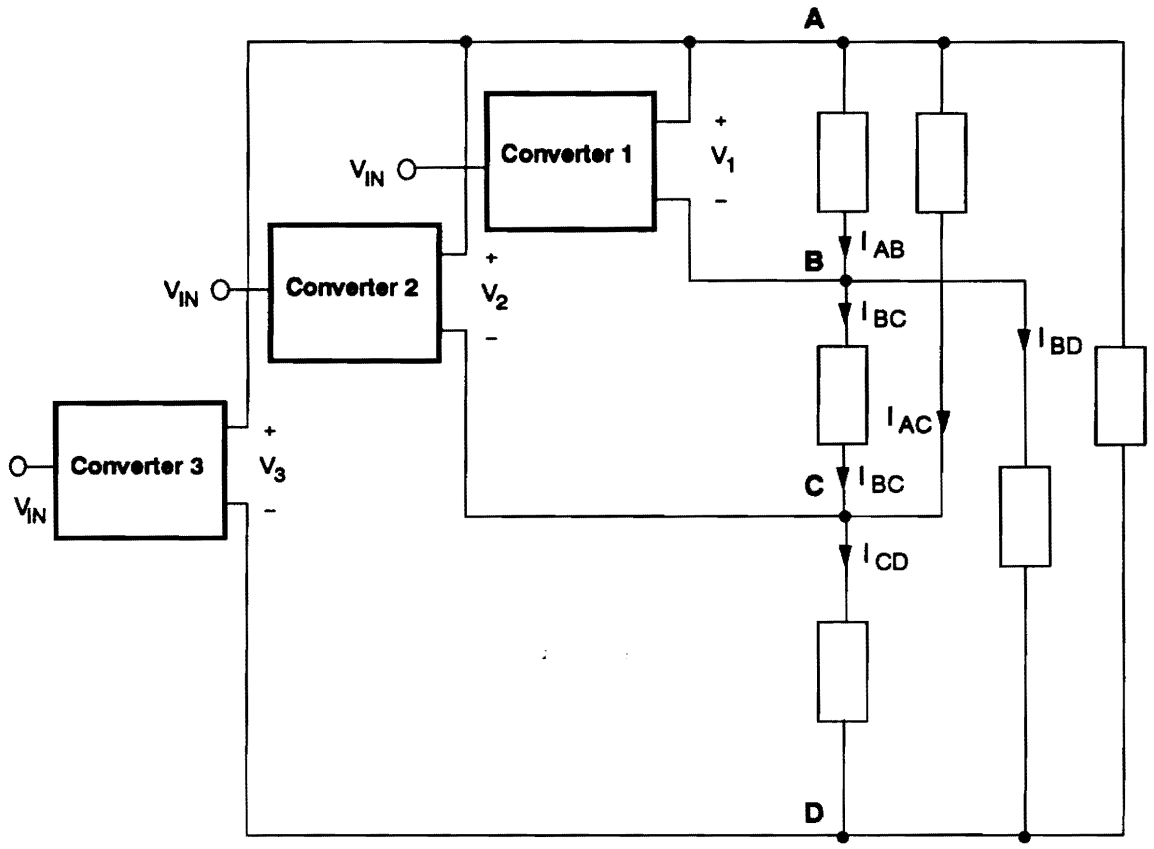


Fig. 3.2. Three-stage stacked power system: KVL requires $V_{BC} = V_{AC} - V_{AB}$, $V_{BD} = V_{AD} - V_{AB}$, and $V_{CD} = V_{AD} - V_{AC}$. The unidirectional power processing requires $I_{AB} > I_{BC} + I_{BD}$ and $I_{BC} + I_{AC} > I_{CD}$.

where

N_C: minimum number of converters,

N_L: number of loads, and

N_D: number of loads whose voltages can be obtained subtracting voltages of other two loads.

Equation (3.6) can be combined with the condition of unidirectional power processing to construct a feasible stacked configuration.

Example 1:

Load profile:

load 1 : 100 A of current at 1.0 V output,

load 2 : 250 A of current at 2.0 V output,

load 3 : 300 A of current at 3.0 V output,

load 4 : 400 A of current at 4.0 V output, and

load 5 : 500 A of current at 5.0 V output.

By applying Eq. (3.6) to the given load profile, the minimum number of converters is found to be three. Figure 3.3(a) shows a stacked configuration using three converters. However, this configuration is not feasible since Converter 1 violates the condition of unidirectional power processing; the current of Converter 1 is flowing in the opposite direction. Figure 3.3(b) shows a feasible configuration using the minimum number of converters for the given load profile.

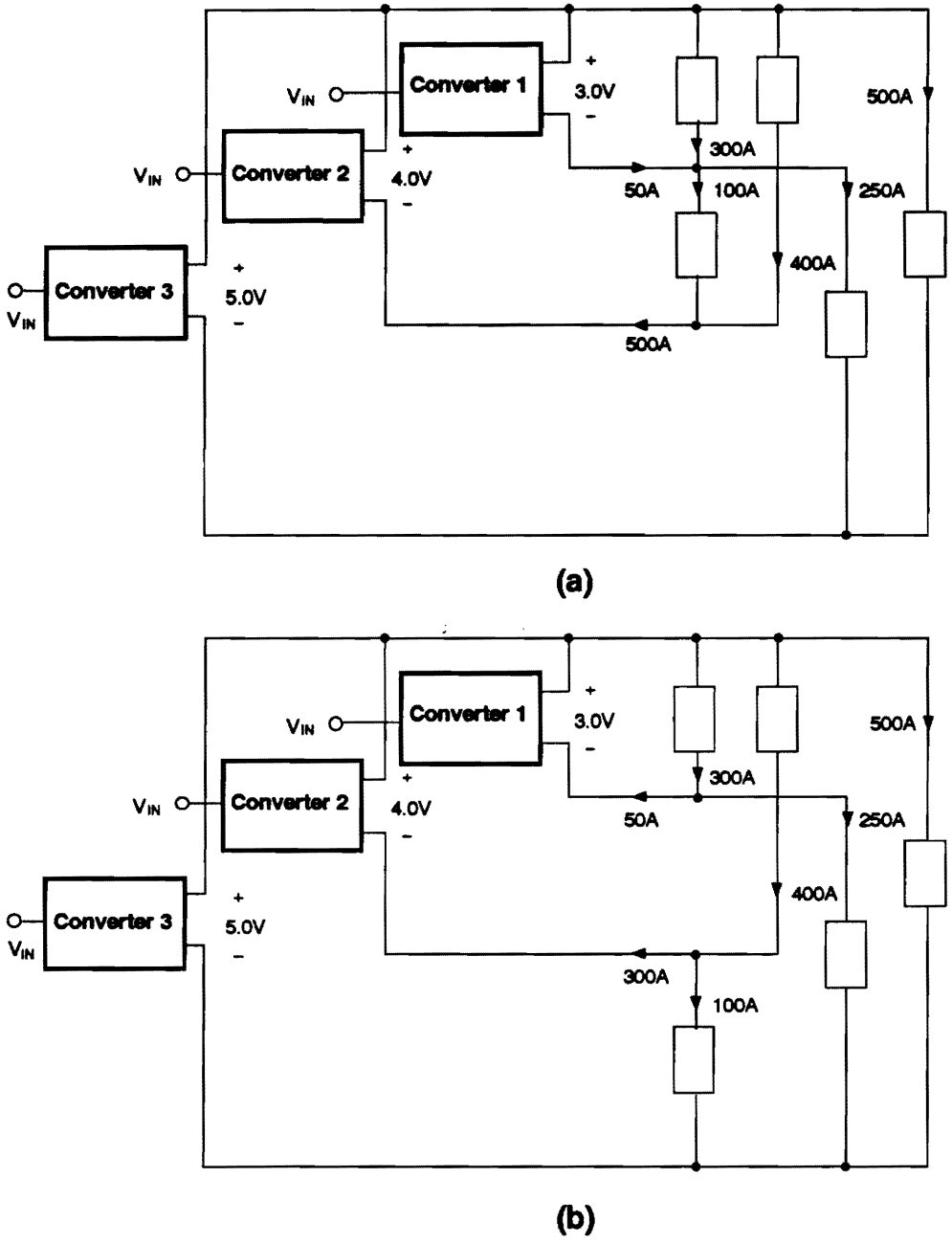


Fig. 3.3. Feasible and non-feasible stacked configurations: (a) Non-feasible configuration: Converter 1 violates the condition of unidirectional power processing since its current is flowing in the opposite direction. **(b) Feasible configuration:** The system provides five outputs using three converters.

Example 2:

Load profile:

load 1 : 300 A of current at 1.3 V output,

load 2 : 200 A of current at 2.2 V output, and

load 3 : 100 A of current at 3.1 V output.

Figure 3.4(a) shows a stacked configuration using three converters. This configuration significantly improves the overall efficiency, as discussed in Section 3.1.

Example 3:

Load profile:

load 1 : 100 A of current at 1.3 V output,

load 2 : 200 A of current at 2.2 V output, and

load 3 : 300 A of current at 3.1 V output.

Figure 3.4(b) shows the only feasible configuration for the given load profile. However, this configuration does not realize any benefits of the stacked system architecture.

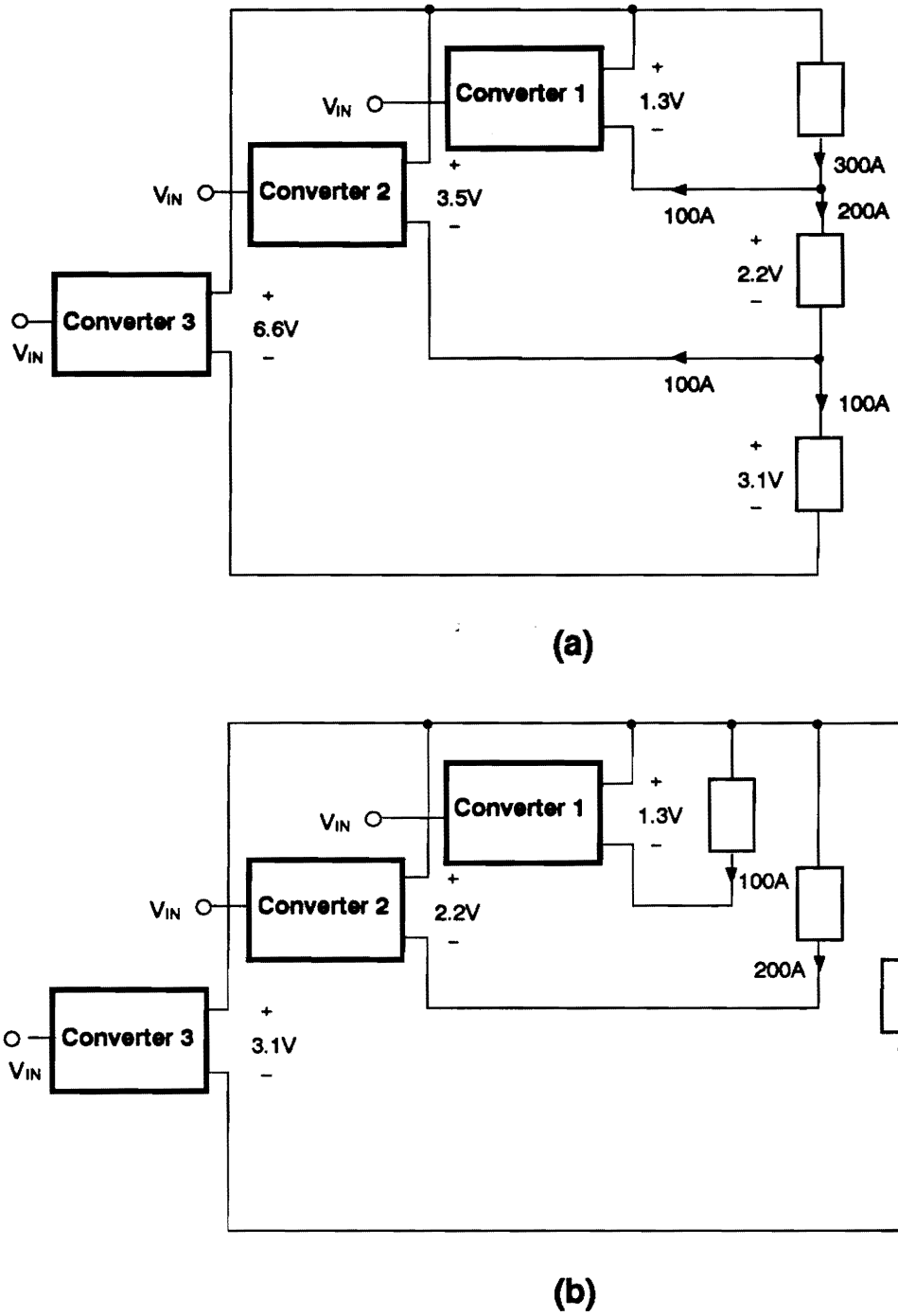


Fig. 3.4. Feasible stacked configurations.

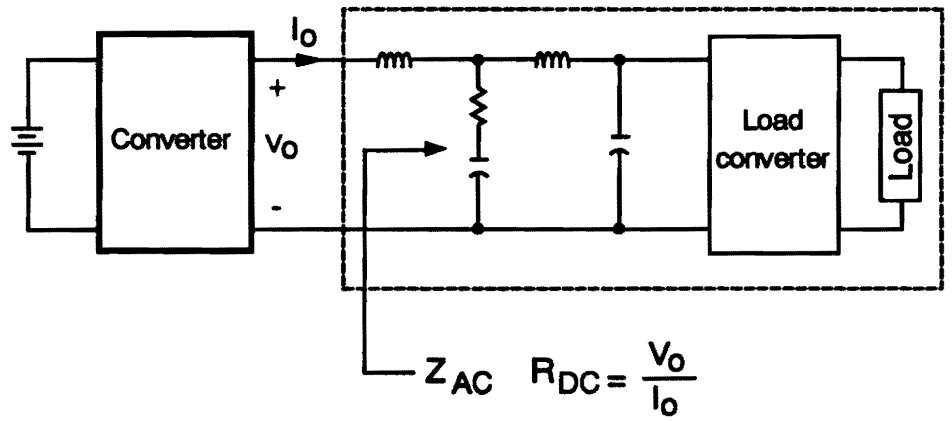
3.3 LOAD DYNAMICS AND DESIGN STRATEGY

A converter operating as a subsystem of a stacked power system has unique load characteristics which keenly contrast with those of a stand-alone converter. This section addresses these unique load characteristics, focusing on their impacts on the analysis and design of stacked power systems.

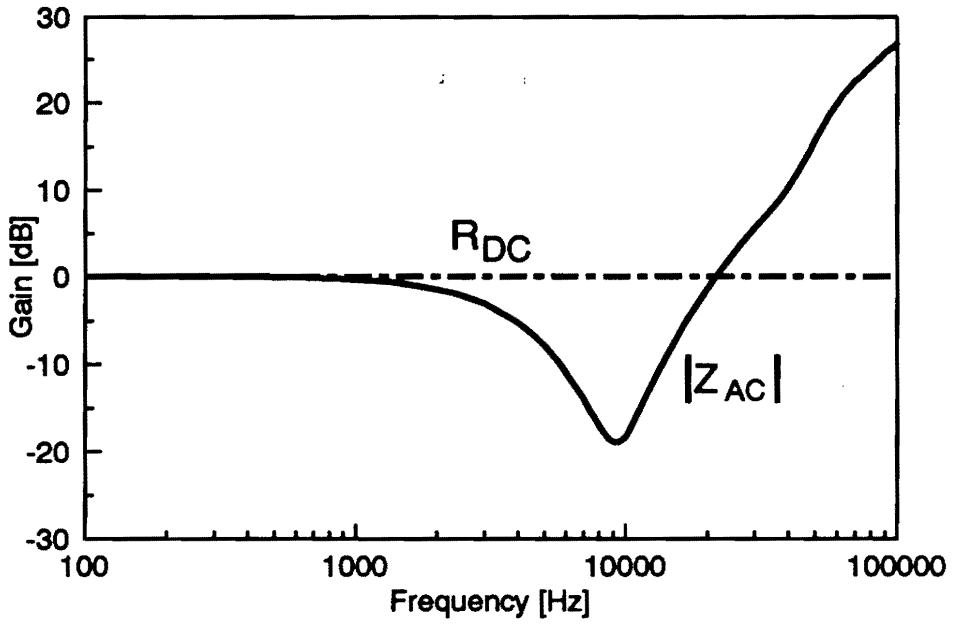
3.3.1 Concept of ac Load and dc Load

The load of a converter is characterized by two different quantities. The first is the load impedance seen by the output of the converter, denoted as ac load, Z_{AC}. The second is the ratio of the dc output voltage of the converter and the dc current drawn from the converter, denoted as dc load, R_{DC}. These two load parameters, along with power stage parameters, fully characterize the small-signal dynamics of a converter and provide all information necessary to design the feedback controller [B12,B19].

With the exception of a single converter with a purely resistive load, Z_{AC} and R_{DC} should be considered separately. For a conventional converter, however, R_{DC} is identical to the magnitude of Z_{AC} evaluated at zero frequency ($|Z_{AC}|_{dc}$), since the power drawn from the converter should be the same as the power consumed at the load. Figure 3.5 compares $|Z_{AC}|$ and R_{DC} of a converter driving another converter through an intermediate filter stage. While $|Z_{AC}|$ and R_{DC} are quite different at mid- and high-frequencies, two curves converge at low-frequencies.



(a)



(b)

Fig. 3.5. Comparison between $|Z_{AC}|$ and R_{DC}: (a) Converter driving another converter through an intermediate filter. (b) Comparison between $|Z_{AC}|$ and R_{DC}: $|Z_{AC}|$ and R_{DC} converge at low frequencies since the power drawn from the converter should be the same as the power consumed at the load.

In a stacked power system, a converter sees a complex load consisting not only of load resistors but also of the other converters in the system. In Fig. 3.6(a), the multiple-sourced power system of Fig. 3.1(b) is rearranged to illustrate the load characteristics of Converter 1. Since the load of Converter 1 contains Converter 2 as well as load resistors, the power drawn from Converter 1 is not the same as the power consumed at its effective load. Thus R_{DC} of the converter is not directly related with $|Z_{AC}|_{dc}$. Figure 3.6(b) compares the dc load of Converter 1, $R_{DC} = 1.4/200 = 7\,m\Omega$, with its ac load Z_{AC}:

$$Z_{AC} = R_1 \parallel (R_2 + Z_{OU2}) \tag{3.7}$$

where Z_{OU2} represents the output impedance of Converter 2 (detailed discussions about the output impedance of a converter will be given in Section 3.4). In contrast to the previous case, $|Z_{AC}|$ of Converter 1 is entirely different from R_{DC} for all frequencies. Due to this unique feature, a clear distinction between R_{DC} and Z_{AC} is essential in the analysis and design of a stacked power system.

3.3.2 System Decomposition Using ac Load and dc Load

In many practical applications, the size and complexity of a stacked power system do not allow the system to be designed as a whole. To make the design problem more tractable, it is essential to decompose the system into several smaller subsystems. An obvious approach to decomposing the system is to divide the system into individual converters. This reduces the design problem of a complex stacked power system to that of

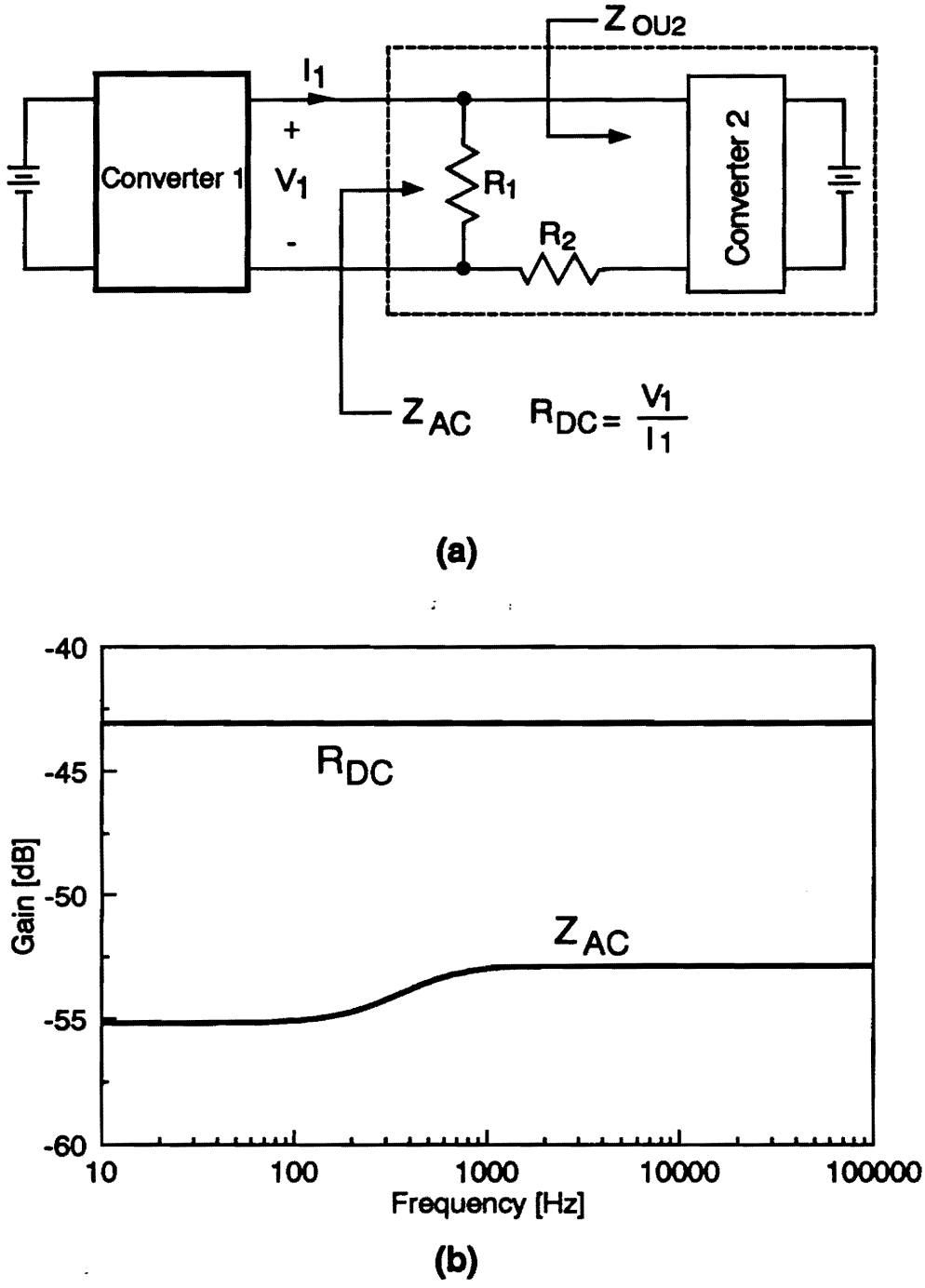


Fig. 3.6. Comparison between Z_{AC} and R_{DC}: (a) Converter 1 in the stacked architecture of Fig. 3.1(b). (b) Comparison between $|Z_{AC}|$ and R_{DC}: Unlike the previous case, $|Z_{AC}|$ is entirely different from R_{DC} for all frequencies.

individual converters. In this decomposition process, interactions among converters must be incorporated. Otherwise, even though each converter might be properly designed for stand-alone operation, the overall performance of the entire system could be very poor when converters are stacked together.

The role of Z_{AC} and R_{DC} in the decomposition of a stacked power system is self-evident. Z_{AC} reflects all interactions among system components and fully characterizes the dynamics of the effective load. R_{DC} is an integral part of the power stage parameters [D3,D4] and determines the open-loop dynamics of the power stage. Thus once Z_{AC} and R_{DC} of each converter are identified, a stacked power system can be decoupled into individual converters. Figure 3.7 shows the stacked power system of Fig. 3.1(b) decomposed into two individual converters using Z_{AC} and R_{DC} of each converter.

3.3.3 Design Approach

Once the system is decomposed into individual converters, the control of decoupled converters can be optimized using their respective Z_{AC} and R_{DC}. This approach automatically incorporates all subsystem interactions and optimizes the closed-loop performance of the integrated system.

Z_{AC} of the decoupled converter is a complex frequency-dependent quantity. Thus a systematic analysis of Z_{AC} is necessary to adapt the standard design techniques to the

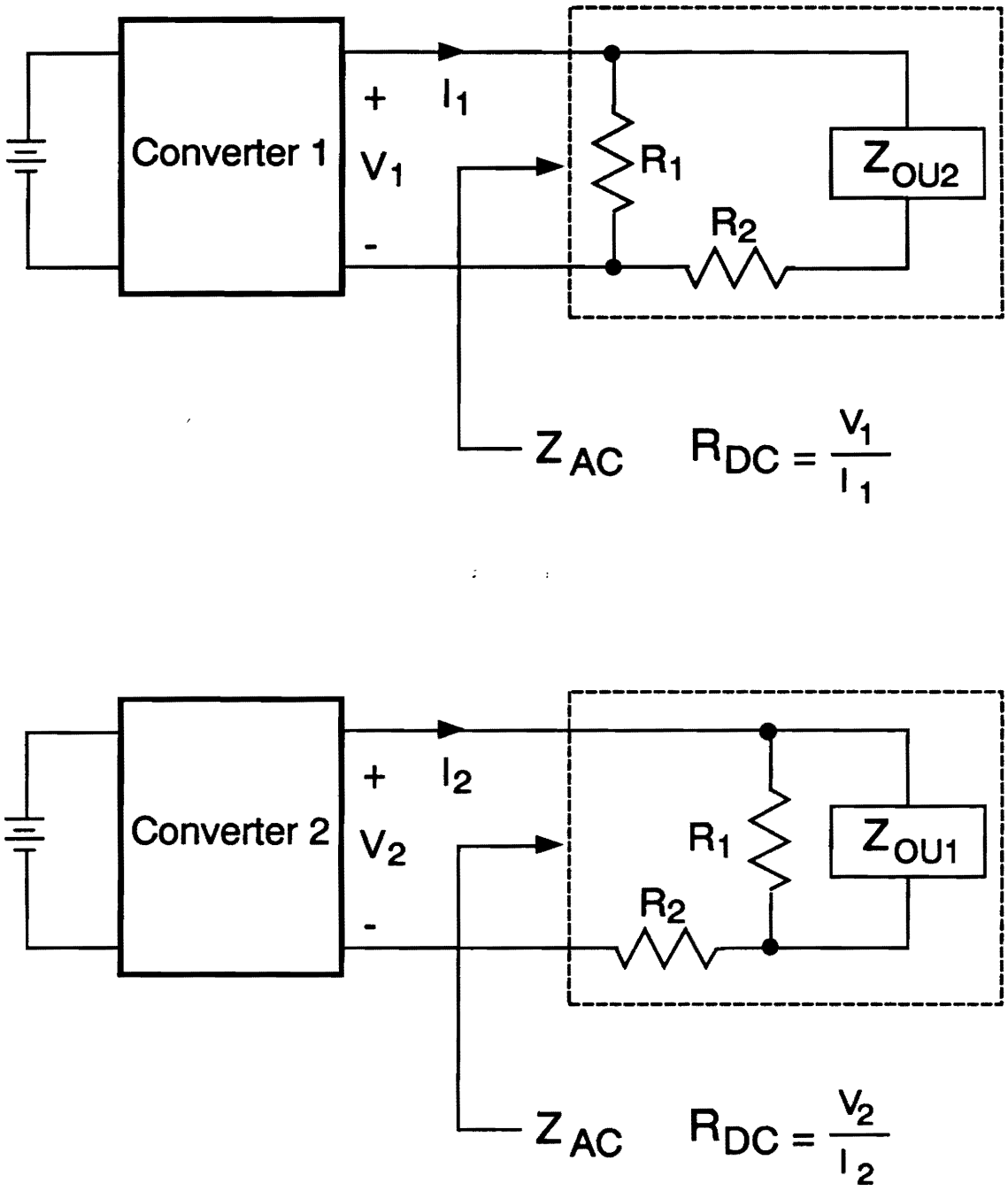


Fig. 3.7. Decomposition of the stacked power system of Fig. 3.1(b) into two individual converters: Z_{OU1} is the output impedance of Converter 1, and Z_{OU2} is the output impedance of Converter 2.

decoupled converters. Detailed discussions about Z_{AC} and design of the decoupled converters will be presented in the next section, which covers the analysis and design of a stacked power system developed for the IBM390 mainframe computer.

3.4 ANALYSIS AND DESIGN OF A THREE-STAGE STACKED POWER SYSTEM

This section presents the analysis and design of a three-stage stacked power system developed for the IBM390 mainframe computer system. In addition to the confirmation of the design approach discussed in Section 3.3, this section presents a comprehensive system level analysis and detailed design procedures which can be readily extended to stacked power systems in general.

3.4.1 System Description

Figure 3.8 shows the schematic diagram of the system. The system consists of three multi-module converters stacked together to provide five low-voltage high-current outputs for the high-density emitter coupled logic circuits (represented by the five resistors in Fig. 3.8). V_{AB} (1.4 V) is regulated by Converter 1. V_{AC} (2.1 V) is regulated by Converter 2, and V_{AD} (3.6 V) is regulated by Converter 3. These three outputs are directly connected to R_{AB}, R_{AC}, and R_{AD}, respectively. The other two loads, R_{BC} and R_{BD}, utilize voltage differences between the outputs of two converters. R_{BC} utilizes the voltage difference between the output of Converter 2 (V_{AC}= 2.1 V) and the output of Converter 1 (V_{AB}=1.4 V) to obtain an ultra low output voltage of 0.7 V. R_{BD} utilizes the voltage difference between the output of Converter 3 (V_{AD}= 3.6 V) and the output of Converter 1 (V_{AB}=1.4 V) to obtain an output voltage of 2.2 V. While each converter has its own output capacitor, an additional load capacitor (C_{BC}) is employed across R_{BC} in

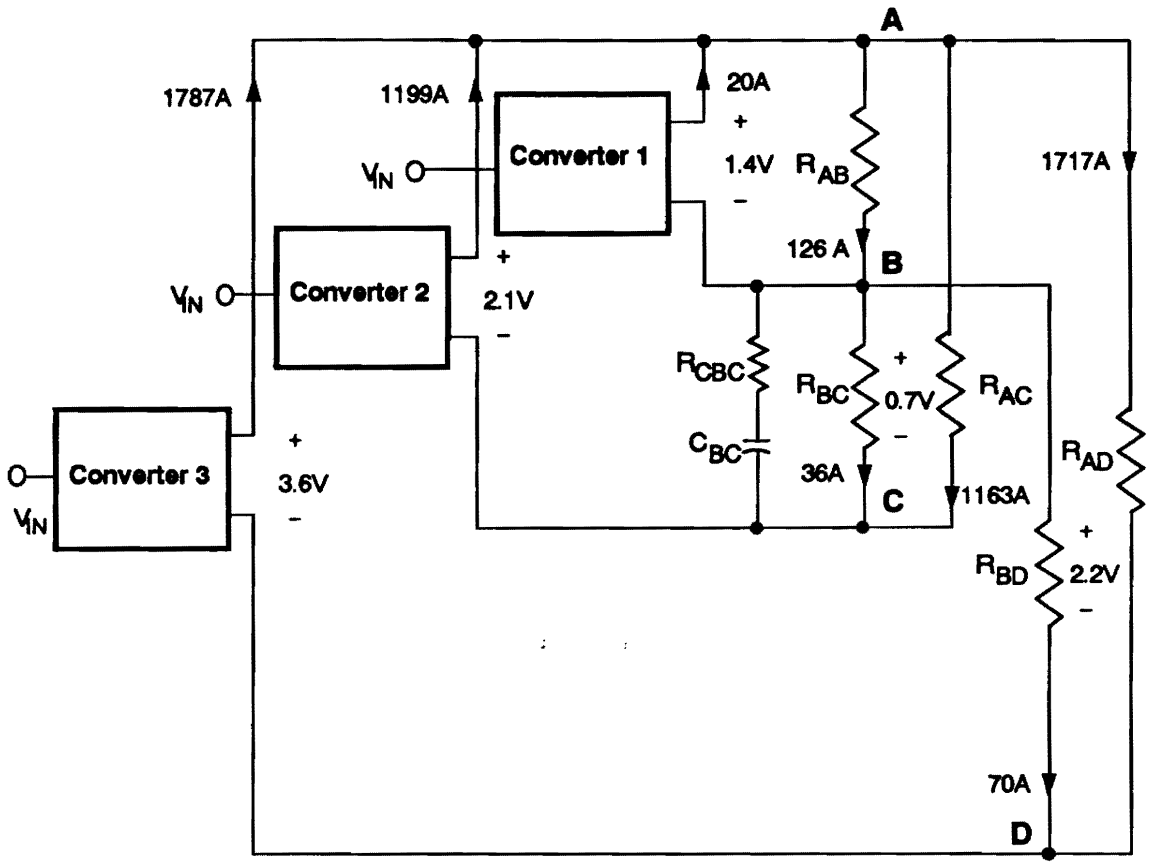


Fig. 3.8. Stacked power system: The system employs a stacked configuration of three multi-module converters to power five high-density emitter coupled logic circuits: $V_{IN} = 297\ V$, $C_{BC} = 2720\ \mu F$, and $R_{CBC} = 2.9\ m\Omega$.

order to further reduce the switching ripple on this particular output.

Three converters collectively deliver the high current to the loads. Converter 3 delivers 1787 A of current, Converter 2 delivers 1199 A, and Converter 1 delivers 20 A. The total current drawn from three converters (3006 A) is supplied to three load resistors directly connected to the outputs of the converters: 126 A to R_{AB}, 1163 A to R_{AC}, and 1717 A to R_{AD}. The current through R_{AB} (126 A) is further divided into three portions: 20 A back to Converter 1, 36 A to the load resistor R_{BC}, and 70 A to the load resistor, R_{BD}. Each converter employs a number of converter modules in parallel in order to deliver the high current efficiently and to realize a built-in redundancy. Converter 1 has two modules in parallel, Converter 2 has four modules, and Converter 3 has six modules.

Figure 3.9 shows the schematic diagram of Converter 1 (Converter 2 and 3 have the same structure as Converter 1 other than the number of modules). The converter consists of two full-bridge PWM modules, a secondary LC filter, and an output voltage feedback compensation circuit, F_R. The secondary LC filter is used to efficiently meet the specifications for ripple and high frequency noise. Each module consists of a power stage operating at 100 kHz ripple frequency, a PWM block, and two inner feedback circuits, CSN and F_L. Section 2.5 showed that the local voltage feedback, F_L, offers significant improvements in the closed-loop performance of the converter, particularly the transient response in the event of failure of a module. In addition, each module contains an input filter stage to prevent the pulsating switch current from being reflected to the input bus.

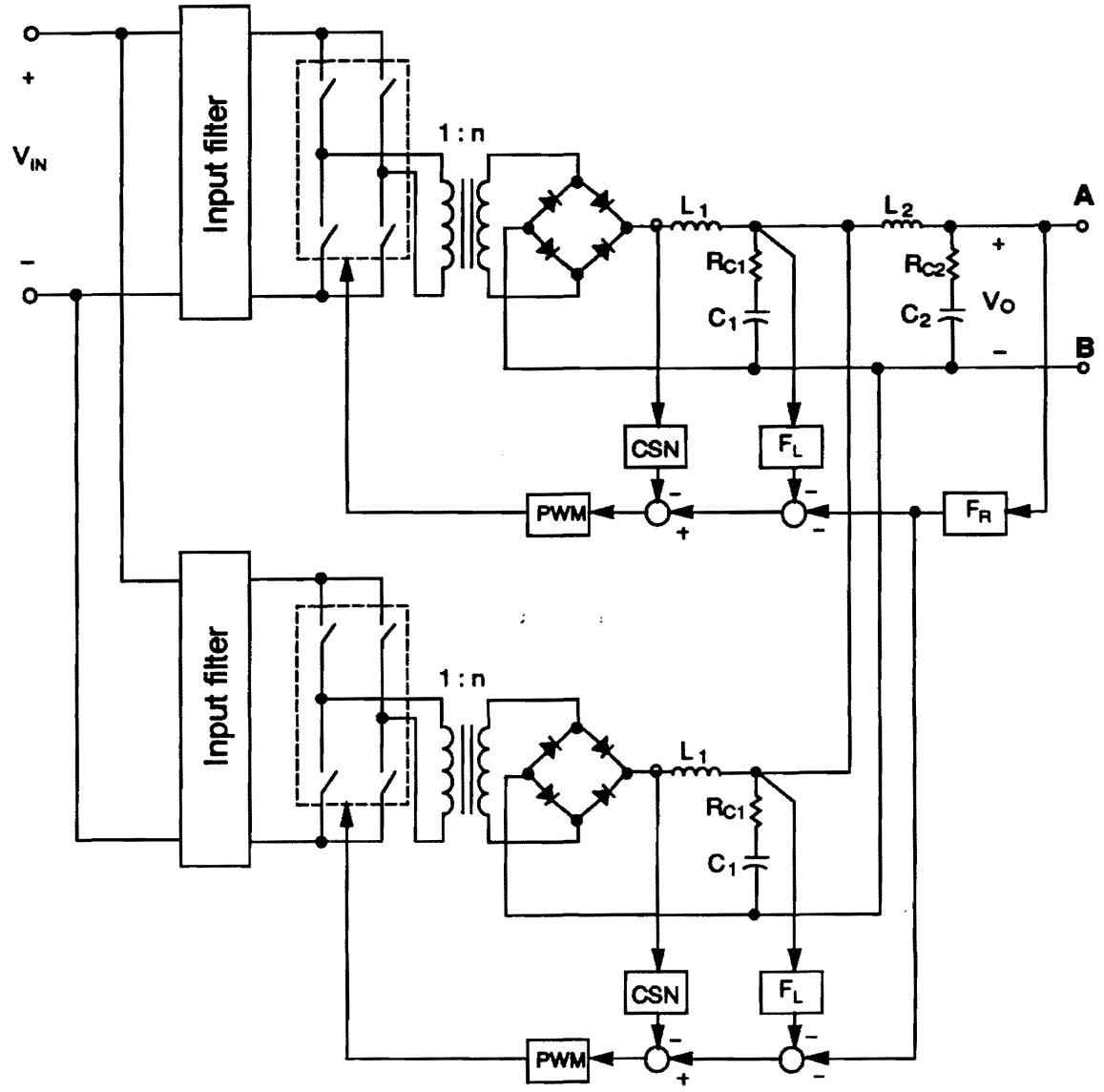


Fig. 3.9. Converter 1: The converter employs the three-loop control scheme to improve the module-failure response and the other performance criteria: $V_{IN} = 297\ V$, $V_O = 1.4\ V$, $n = 1/48$, $L_1 = 0.82\ \mu H$, $L_2 = 0.15\ \mu H$, $C_1 = 6000\ \mu F$, $C_2 = 0.052\ F$, $R_{C1} = 5\ m\Omega$, and $R_{C2} = 2\ m\Omega$.

3.4.2 Design-Oriented Model Reduction

It is impractical to design such a complex system as a whole. To make the design problem more tangible, this section presents a sequence of system level analyses which successively simplify the system but retain all prominent dynamics.

System Decomposition

Figure 3.10 shows the system decomposed into three individual converters by identifying the ac load and dc load of each converter. $Z_{OUk}\,(k = 1,2,3)$ represents the output impedance of each converter. The dc load can be determined from the dc operating point of each converter and is not shown in Fig. 3.10. With this decomposition, the design problem of the stacked power system is reduced to that of three individual multi-module converters.

The use of ac and dc load in designing the decoupled multi-module converters is closely related to the design strategy for a multi-module converter. For a complex multi-module converter, it is advantageous to design the control loop and the input filter separately. After designing the control loop assuming an ideal voltage source as the input of the converter, an input filter can be added whose output impedance is sufficiently lower than the closed-loop input impedance of the power stage. This approach simplifies the design and minimizes undesirable interactions between the input filter and control loop. Detailed discussions on this subject will be given in Chapter 4.

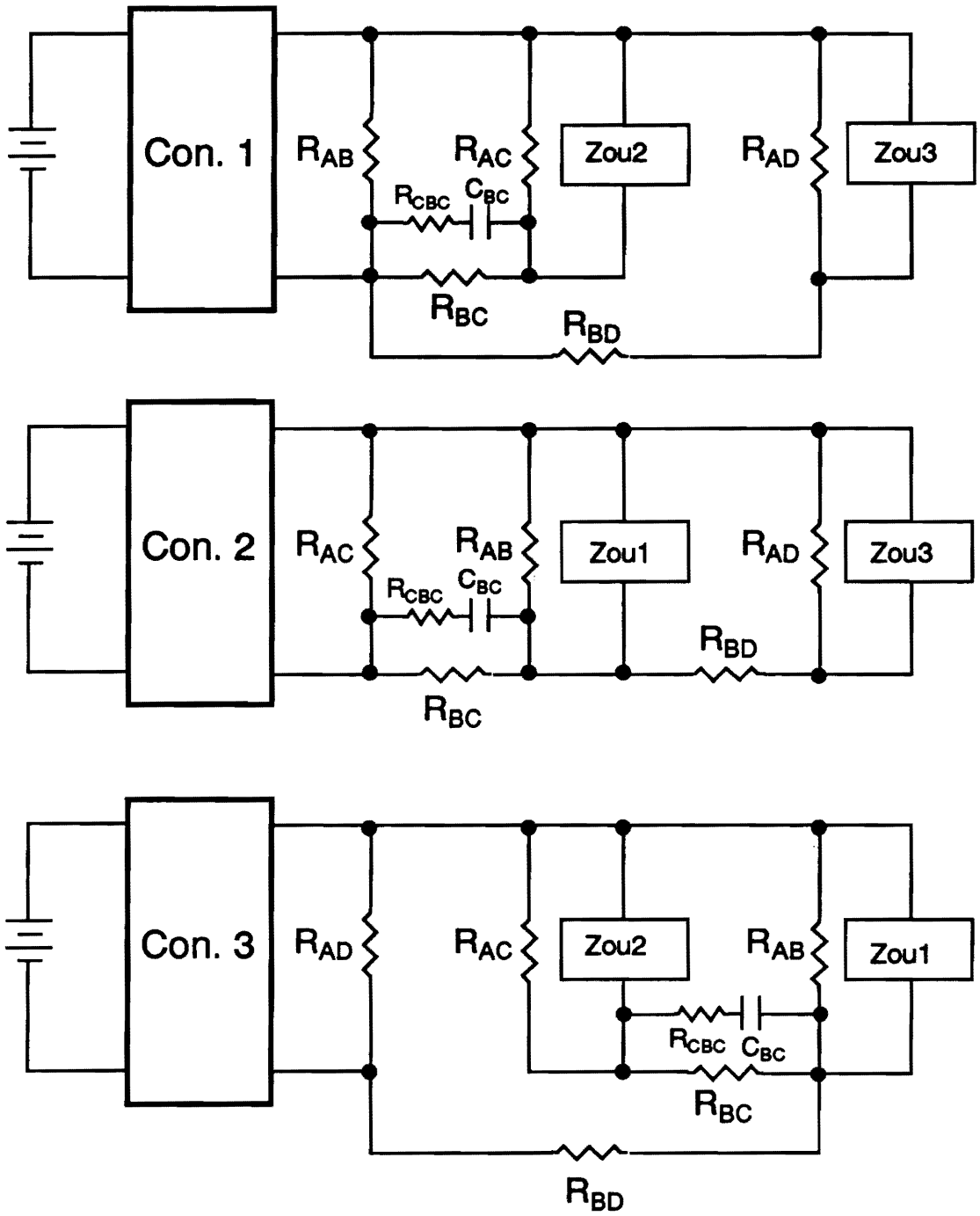


Fig. 3.10. Decomposition of the stacked power system into three individual converters: Z_{OUk} (k=1,2,3) represents the output impedance of each converter.

Figure 3.11 shows the equivalent single-module model of Converter 1 with an ideal voltage source. It can be easily seen from Fig. 3.11 that the dependent current source, I_d , the only parameter depending on R_{DC}, has no effect on transfer functions from the duty cycle to various feedback signals. In deriving these transfer functions, $\hat{v}_{in}$ is assumed to be zero and absorbs I_d. Thus the only load parameter which affects the control loop design is the ac load, Z_{AC}. (This is true only for buck-derived converters. For boost-derived topologies, both Z_{AC} and R_{DC} must be considered in the control loop design.)

On the other hand, R_{DC} directly affects the input filter design. As will be illustrated in Section 3.4.4, R_{DC} can be used to estimate the minimum magnitude of the closed-loop input impedance of the power stage. This information is critical in designing an input filter which minimizes interactions with the control loop of the power stage.

Load Impedance Analysis

The load impedance of the decoupled converter is a complex combination of the load resistors/capacitor and the output impedance of the other converters. Thus a systematic analysis of the load impedance is necessary to understand the dynamics of the decoupled converters and to establish design strategies.

To understand the dynamics of the load impedance of decoupled converters, the output impedance of a converter should be characterized first. Figure 3.12 shows the simplified small-signal model of a converter (Fig. 3.12(a)) and its corresponding block

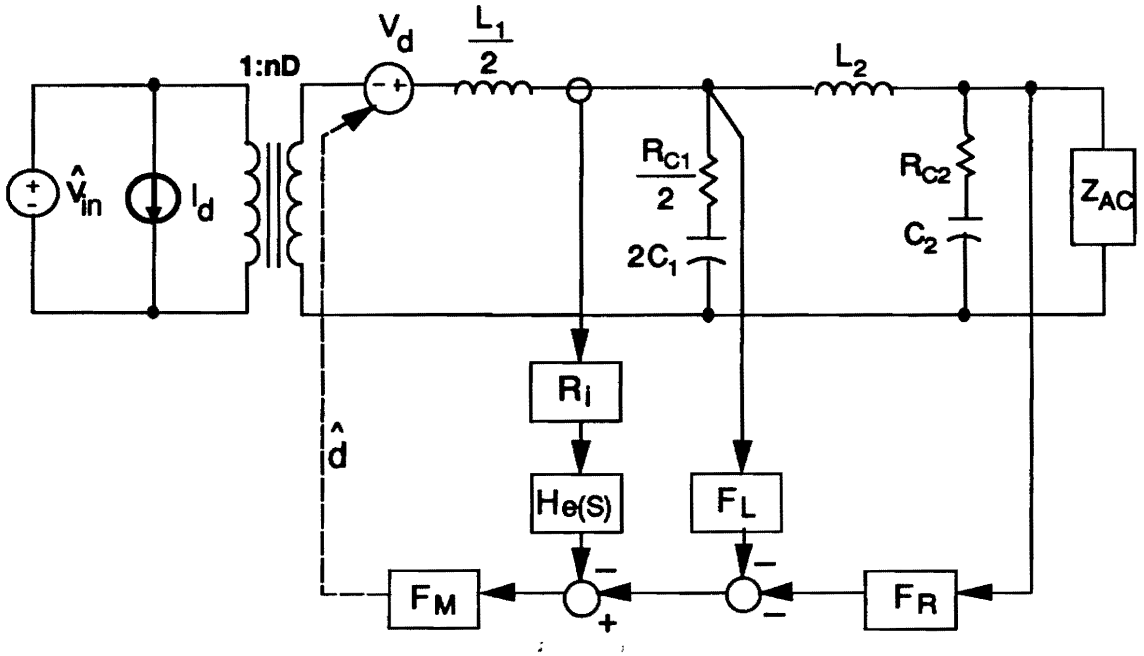


Fig. 3.11. Equivalent single-module model of Converter 1 with Z_{AC} and R_{DC}: $I_d = \frac{n^2 D V_{IN}}{R_{DC}} \hat{d}$ $V_d = n V_{IN} \hat{d}$ where D is the duty cycle of each switch with respect to the ripple frequency. The dependent current source, I_d, has no effect on transfer functions from the duty cycle to various feedback signals.

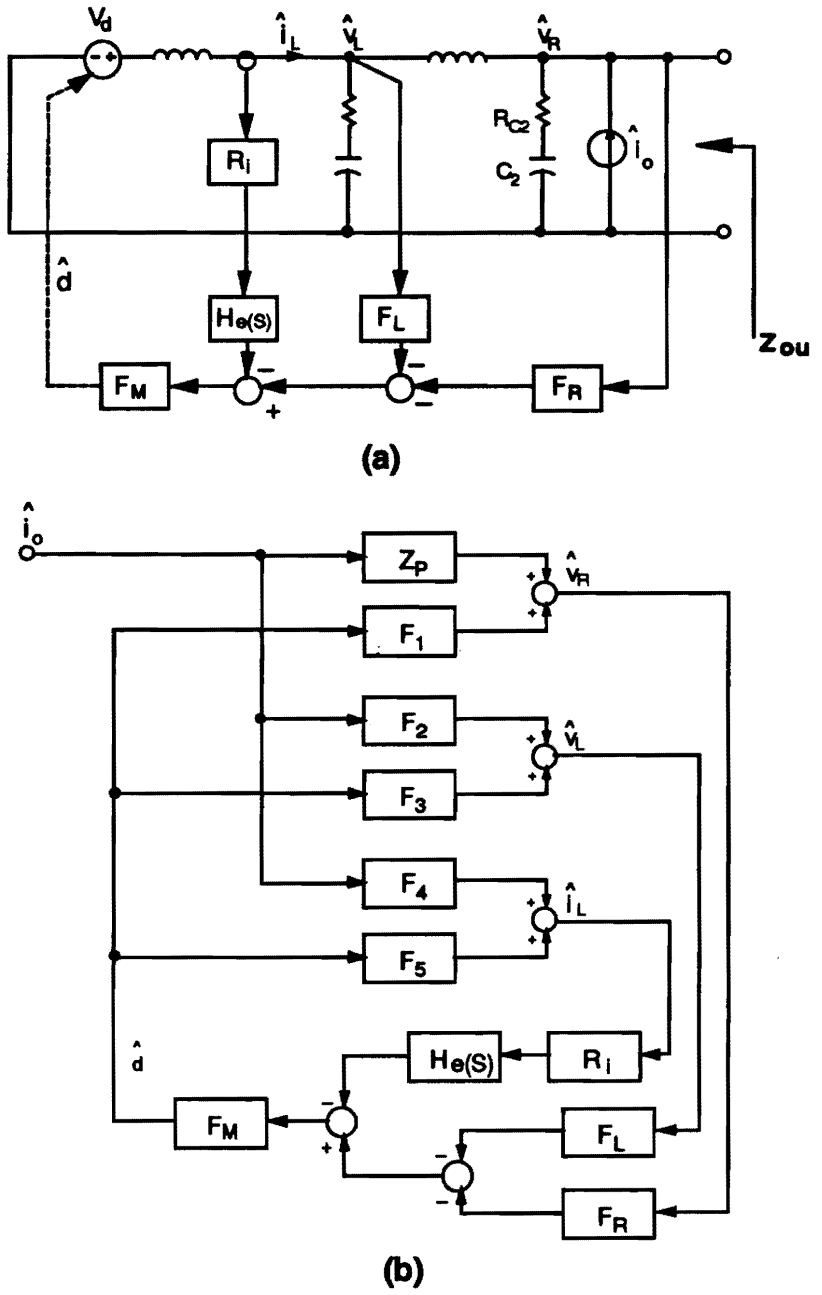


Fig. 3.12. Simplified small-signal model of the decoupled converter: (a) Circuit model. (b) Block diagram: Gain blocks Z_P and F_1 through F_5 represent various open-loop transfer functions of the power stage. The other blocks are feedback compensations and small-signal models of the controller.

diagram (Fig. 3.12(b)). In deriving the output impedance, $\hat{v}_{in}$ in Fig. 3.11 is assumed to be zero, so $\hat{v}_{in}$, I_d, and the ideal transformer are not included in Fig. 3.12(a). From Fig. 3.12(b), the output impedance can be derived as:

$$Z_{OU} = \frac{\hat{v}_R}{\hat{i}_O} = \frac{Z_P + T_I\left(Z_P - \frac{F_4F_1}{F_5}\right) + T_L\left(Z_P - \frac{F_2F_1}{F_3}\right)}{1 + T_I + T_L + T_R}, \tag{3.8}$$

where Z_P is the open-loop output impedance, and T_I, T_L, T_R are given by:

$$T_I = F_M F_5 R_i H_e(s), \tag{3.9}$$

$$T_L = F_M F_3 F_L, \tag{3.10}$$

$$T_R = F_M F_1 F_R . \tag{3.11}$$

The equations can be used to derive an analytical expression for the load impedance of the decoupled converter. However, such a complex derivation is neither practical nor necessary. For analysis and design purposes, it is sufficient to extract the prominent features of the load impedance from the simplified analysis of the output impedance of the converter.

While the output impedance of the converter is a rather complicated frequency-dependent quantity, its asymptotic behavior can be easily deduced. At low frequencies, T_R approaches infinity due to the integrator contained in F_R; this consequently reduces Z_{OU} to zero, regardless of the numerator of Eq. (3.8). At high frequencies, T_I, T_L, and

T_R reduce to zero, and Z_P approaches the equivalent series resistor (ESR) of the secondary filter capacitor (R_{C2} in Fig. 3.12(a)). Thus Z_{OU} approaches ESR of the secondary filter capacitor at high frequencies. Figure 3.13 shows the output impedance of Converter 1. The output impedance decreases monotically at low frequencies and is limited by ESR of the secondary filter capacitor ($2m\Omega = -54dB$) at high frequencies.

Based on the previous analysis, two resistors can be identified which approximate the asymptotic behavior of the load impedance of the converter:

- $R_{eq}(low)$: low frequency approximation of Z_{AC} obtained by replacing the output impedance of each converter with a short circuit and replacing the load capacitor with an open circuit.
- $R_{eq}(high)$: high frequency approximation of Z_{AC} obtained by replacing the output impedance of each converter with the ESR of the secondary filter capacitor and replacing the load capacitor with its ESR.

Using these definitions, $R_{eq}(low)$ and $R_{eq}(high)$ of three converters are calculated as follows:

Converter 1: $R_{eq}(low) = 5.77\,m\Omega\,(-44.8\,dB\Omega)$, $R_{eq}(high) = 2.29\,m\Omega\,(-52.8\,dB\Omega)$;

Converter 2: $R_{eq}(low) = 1.65\,m\Omega\,(-55.65\,dB\Omega)$, $R_{eq}(high) = 1.26\,m\Omega\,(-57.99\,dB\Omega)$;

Converter 3: $R_{eq}(low) = 1.967\,m\Omega\,(-54.13\,dB\Omega)$, $R_{eq}(high) = 1.972\,m\Omega\,(-54.10\,dB\Omega)$.

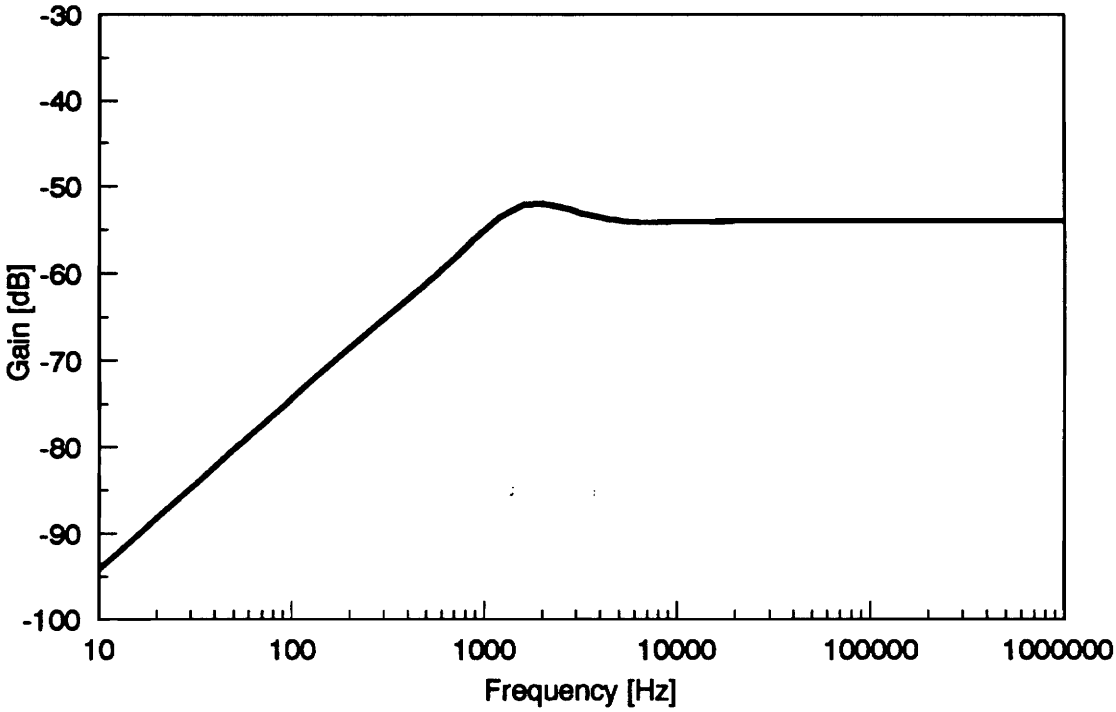


Fig. 3.13. Output impedance of Converter 1: The output impedance decreases monotically at low frequencies and approaches the ESR of the secondary filter capacitor ($2\ m\Omega = -54\ dB$) at high frequencies.

Figure 3.14 shows the actual load impedances of three converters in the stacked power system. The low and high frequency asymptotes of the load impedances are in good agreement with the respective values of $R_{eq}(low)$ and $R_{eq}(high)$. For Converter 3, $R_{eq}(low)$ and $R_{eq}(high)$ are almost identical, and its load impedance is effectively a resistor.

Open-Loop Dynamics of the Decoupled Converter

The open-loop dynamics of the decoupled converter can be characterized by $R_{eq}(low)$ and $R_{eq}(high)$. Figure 3.15 shows the control-to-output transfer function of Converter 1 with three different loading conditions. The solid line is the transfer function with the actual load impedance, Z_{AC}. The dashed line is the transfer function with a load resistor of $R_{eq}(low)$, and the dotted line is the transfer function with $R_{eq}(high)$. As shown in Fig. 3.15, $R_{eq}(low)$ predicts the low-frequency behavior of Converter 1, and $R_{eq}(high)$ predicts the high-frequency behavior of Converter 1. Note that the dc gain of the transfer function is independent of the load impedance.

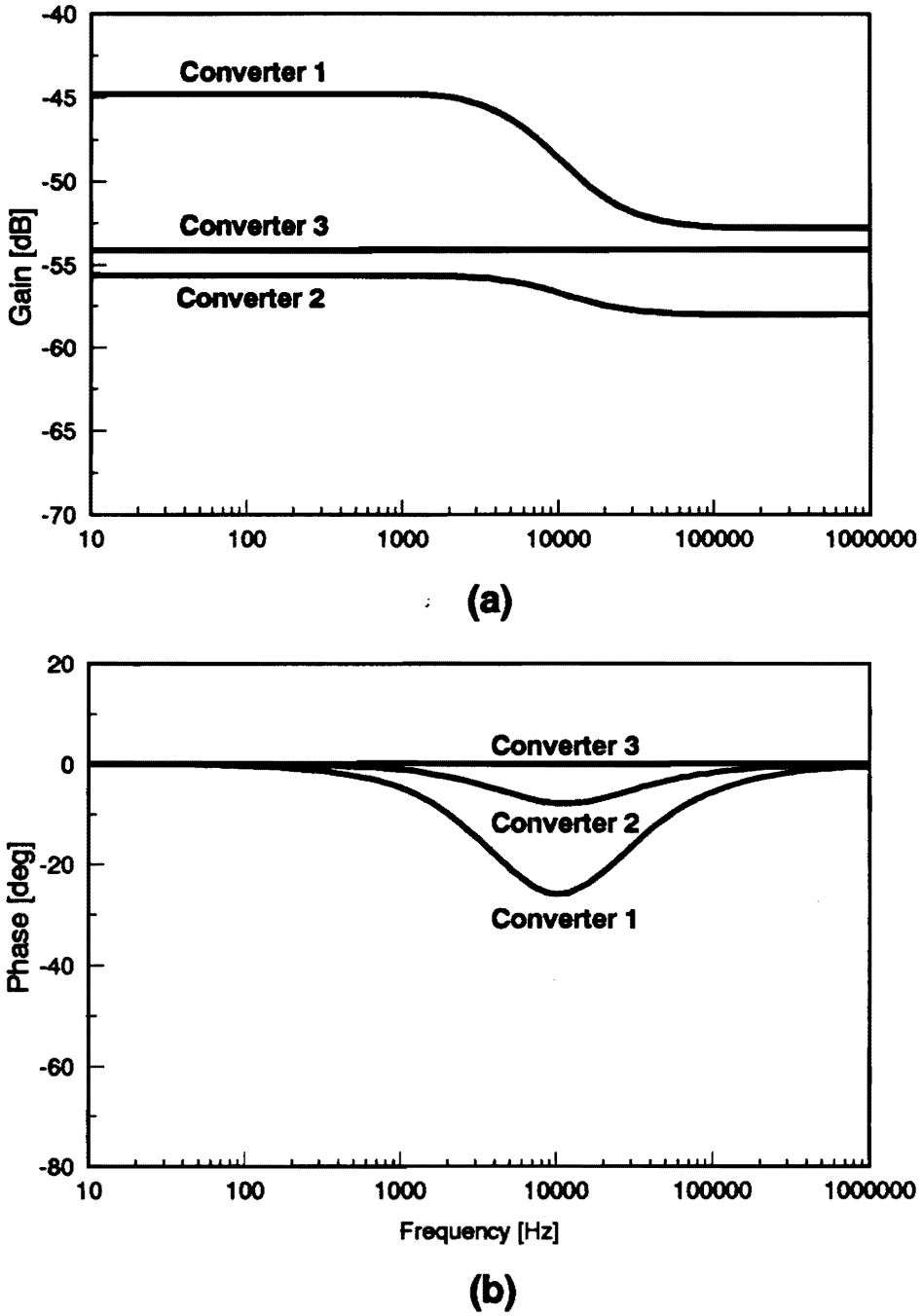


Fig. 3.14. Load impedance of converters: (a) Gain. (b) Phase: The close agreement between the asymptotes of load impedances and analytical predictions verifies theoretical discussions.

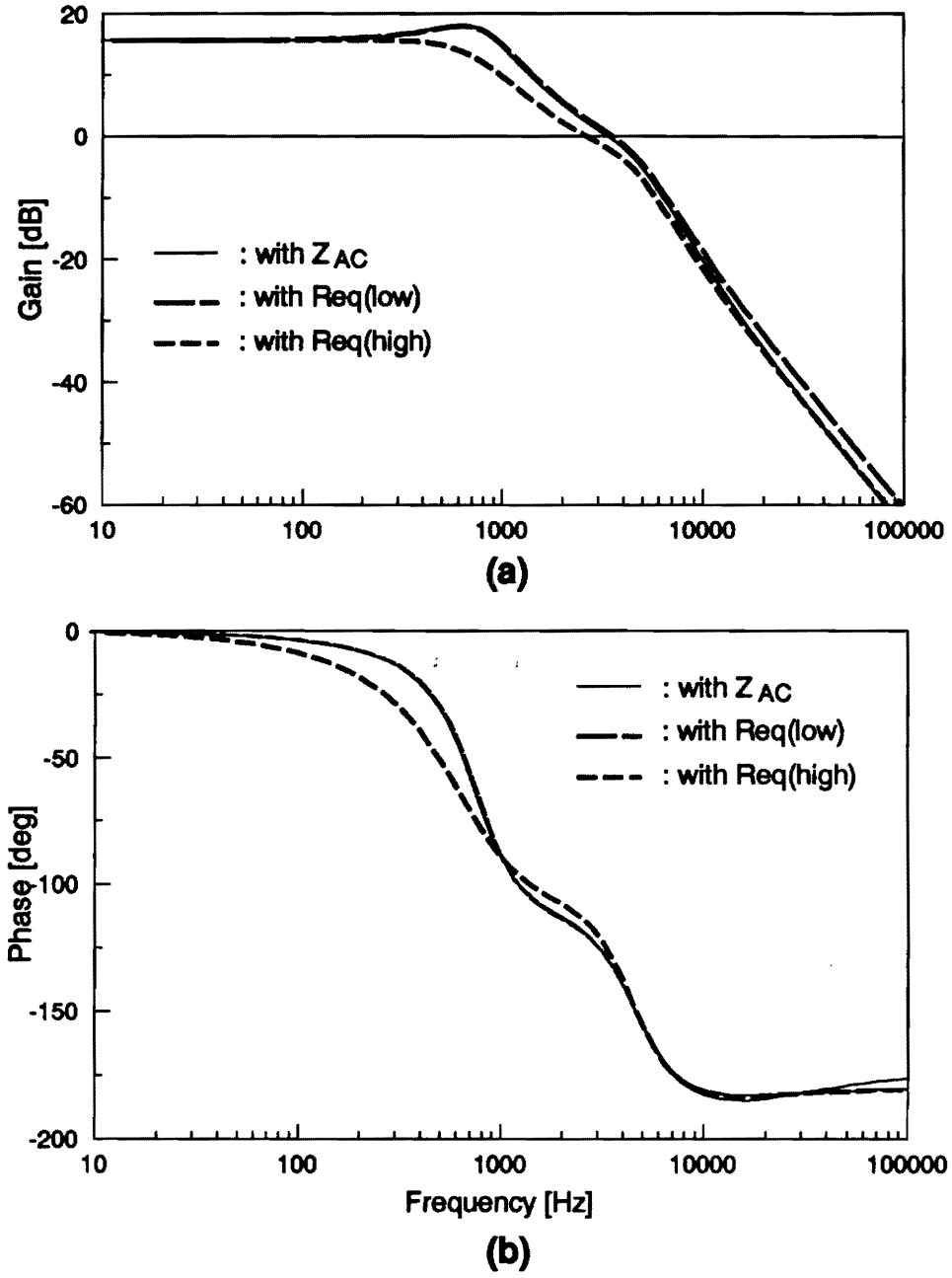


Fig. 3.15. Control-to-output transfer function of Converter 1 with three different loading conditions: (a) Gain. (b) Phase: $R_{eq}(low)$ predicts the low-frequency behavior, and $R_{eq}(high)$ predicts the high-frequency behavior of the decoupled converter.

3.4.3 Control Loop Design

Based on the results of the previous section, this section presents the control design for the decoupled converters. The design optimizes the control loop of each decoupled converter, providing an optimal performance for the entire system.

Design Strategy

In general, the closed-loop performance of a converter is evaluated by stability margins of the loop gain, the peak value of audio-susceptibility and output impedance. Since these performance criteria are determined practically by high-frequency characteristics of a converter, $R_{eq}(high)$ (which predicts the high-frequency behavior of the decoupled converter) can be used as an equivalent resistive load for control design purposes. Feedback compensations optimized for $R_{eq}(high)$ offer an optimal closed-loop performance of the converter in the stacked power system. Furthermore, the optimal design of three individual converters using their respective $R_{eq}(high)$ would result in the best possible performance of the entire system. Thus once the $R_{eq}(high)$ of each converter is identified, the design problem of the stacked power system simplifies to that of three individual multi-module converters with a resistive load.

Design procedures for a multi-module converter with a resistive load were given in Chapter 2. Following those procedures, the control loop of three converters are designed, individually, using their equivalent resistive load, $R_{eq}(high)$.

Design Verification

To confirm the validity of using $R_{eq}(high)$ for the control loop design, Fig. 3.16 shows the loop gain of Converter 1 with two different loading conditions: one with the actual load impedance, Z_{AC}, and the other with the load resistor of $R_{eq}(high)$. The loop gain is measured at the output of PWM block [D2], using the equivalent single-module of Fig. 3.11. The converter shows very similar loop gain characteristics except the discrepancy around the first resonance of the power stage, where Z_{AC} behaves like $R_{eq}(low)$. Figure 3.17 compares the performance of Converter 2 with Z_{AC} and $R_{eq}(high)$. Figure. 3.17(a) compares the loop gain, and Fig. 3.17(b) compares the output impedance of the converter. The converter shows almost identical closed-loop performance with two different loading conditions. Figure 3.18 compares the closed-loop performance of Converter 3 with Z_{AC} and $R_{eq}(high)$. The transfer functions are indistinguishable. This is consistent with the fact that the load impedance of Converter 3 is practically a resistor.

3.4.4 Input Filter Design

This section addresses the use of R_{DC} in designing an input filter for each converter module. Detailed discussions about the input filter design will be given in Chapter 4.

For each module, an input filter must be employed to prevent the pulsating switch current from being reflected to the input bus. Figure 3.19(a) shows the simplified block diagram of Converter 1 with input filters. To avoid undesirable interactions between

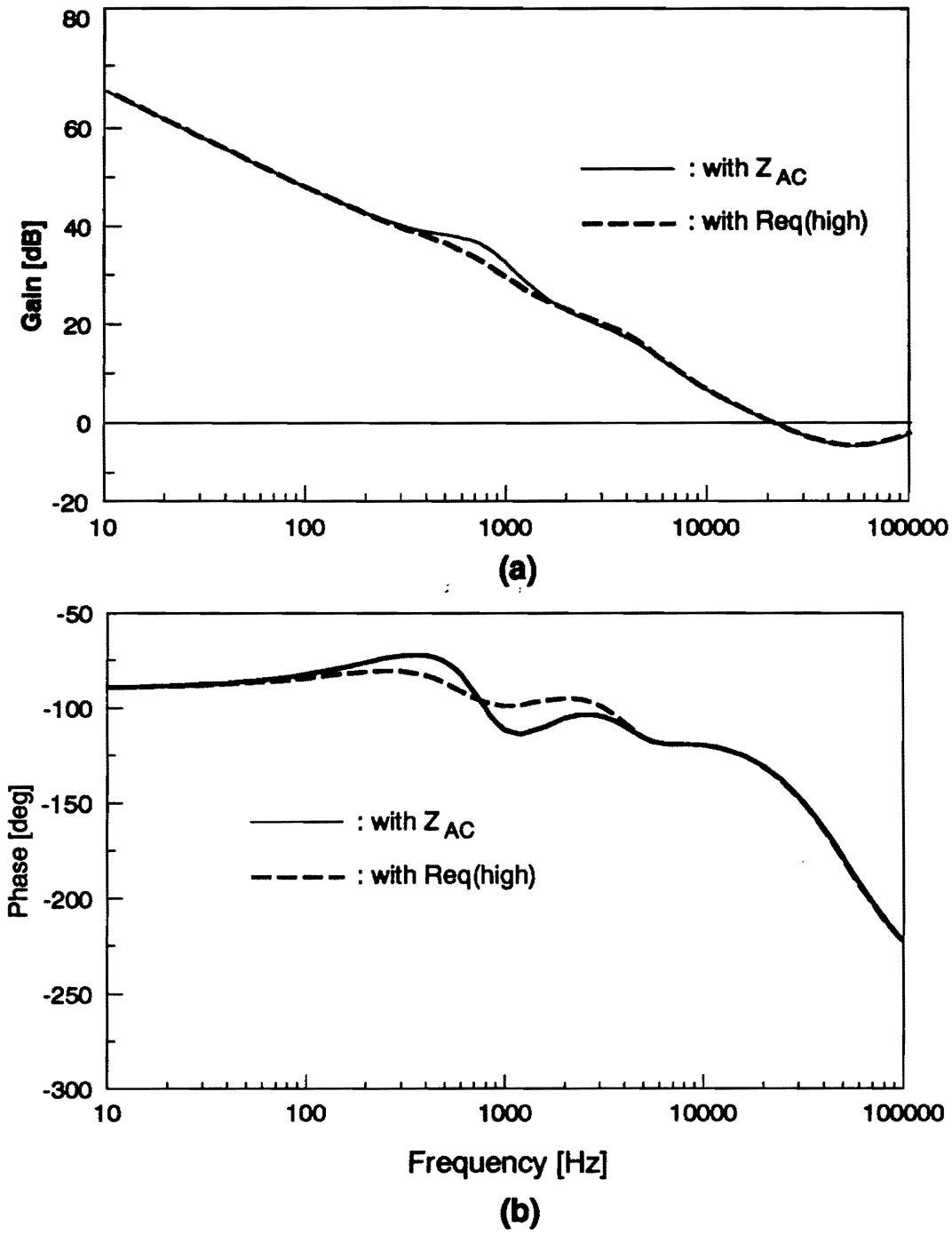


Fig. 3.16. Loop gain of Converter 1 with two different loading conditions: (a) Gain. (b) Phase: The converter shows similar loop gain characteristics.

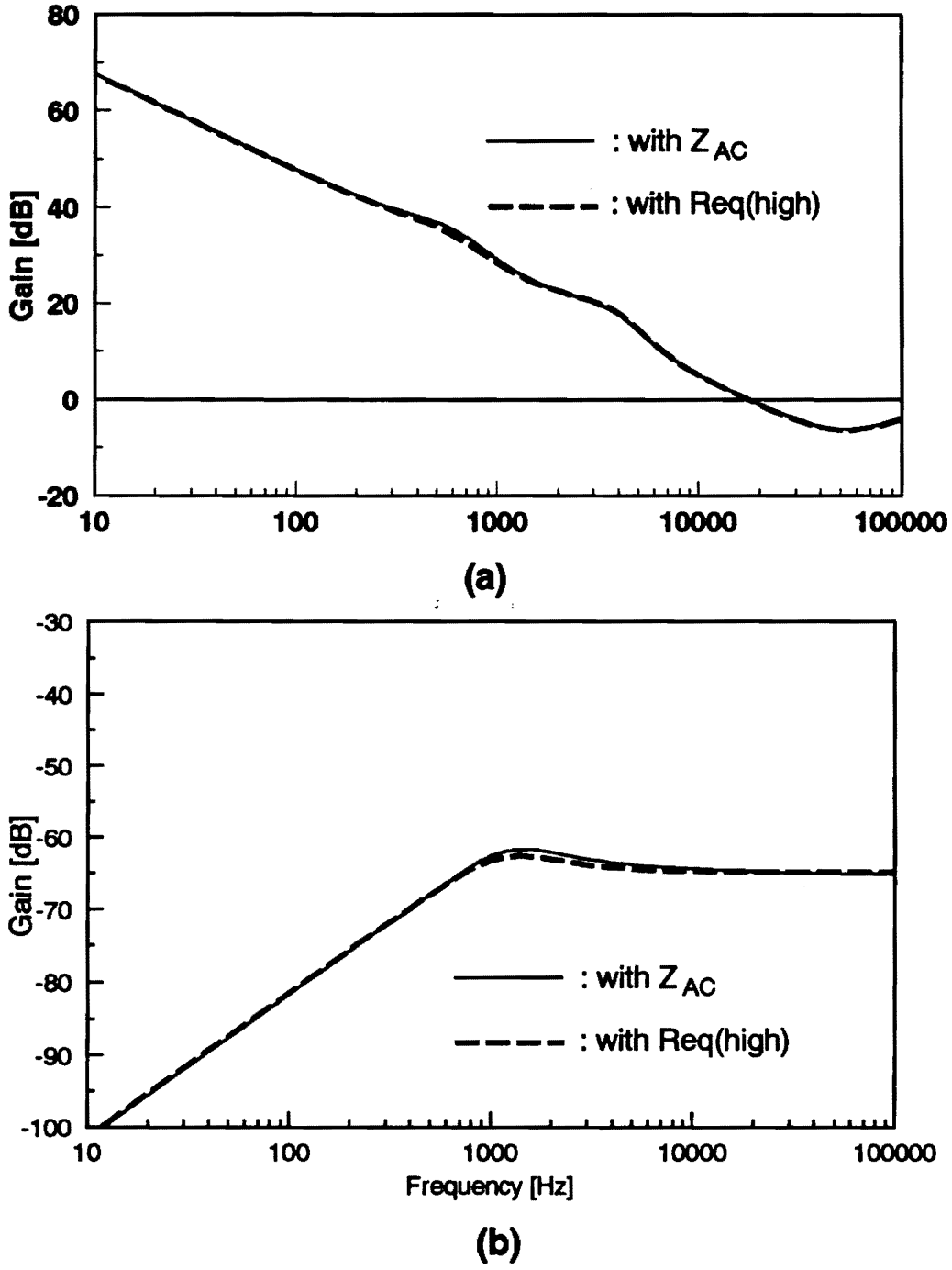


Fig. 3.17. Closed-loop performance of Converter 2 with two different loading conditions: (a) Loop gain. (b) Output impedance: The converter shows almost identical closed-loop performance.

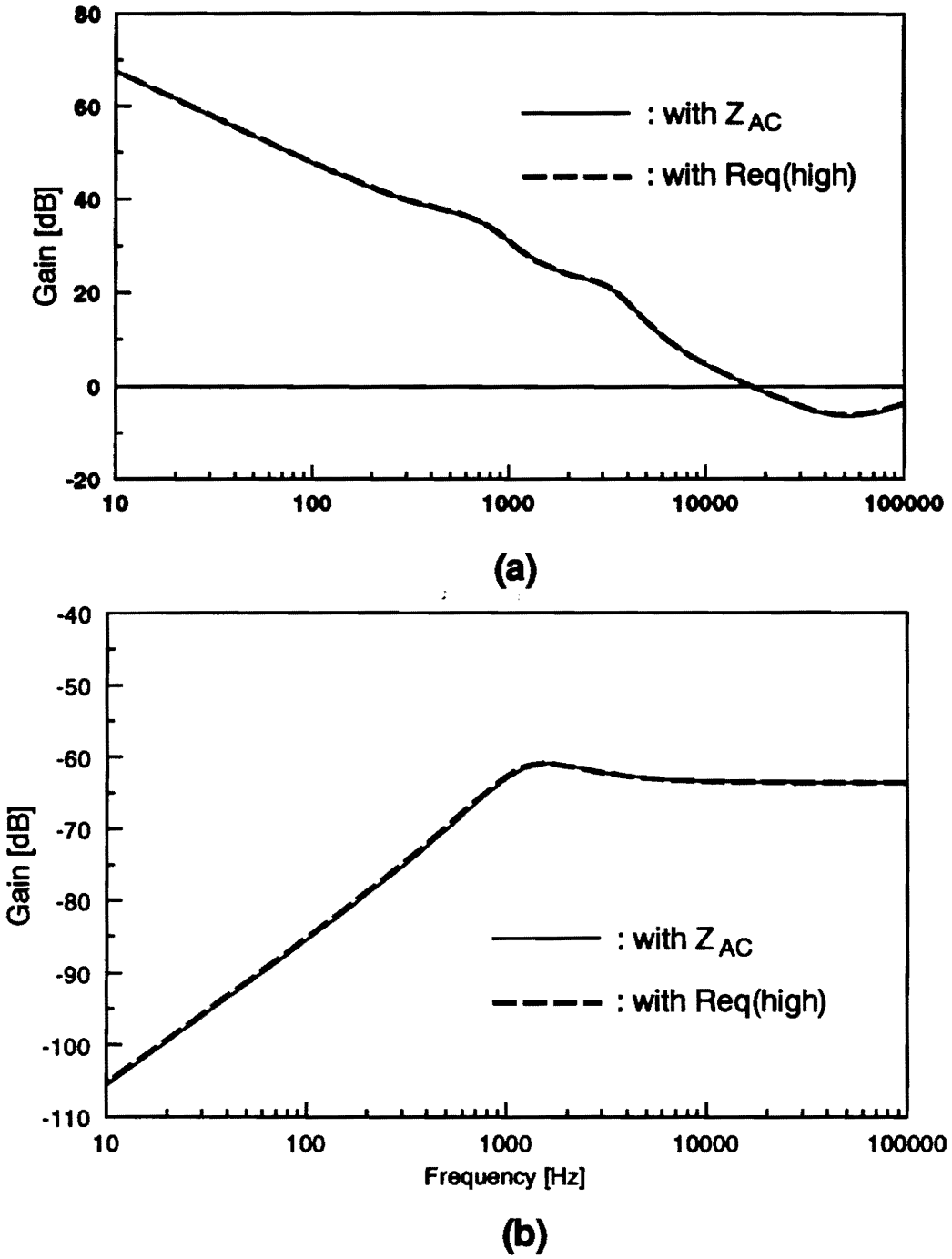
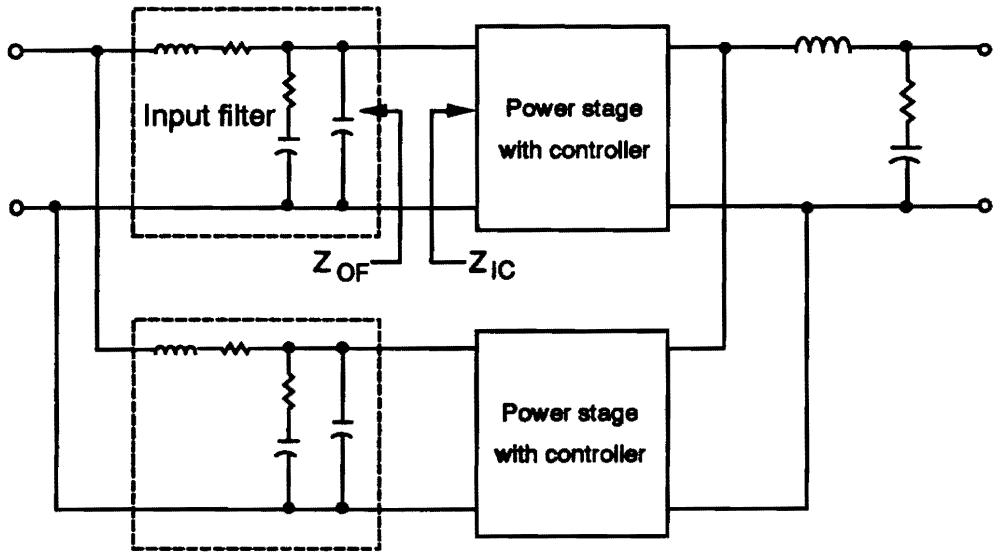
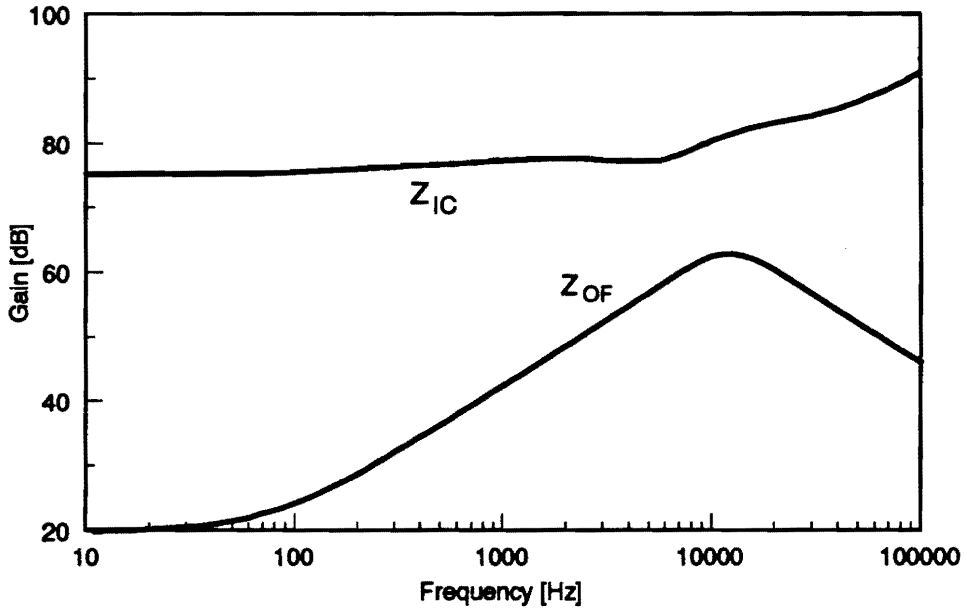


Fig. 3.18. Closed-loop performance of Converter 3 with two different loading conditions: (a) Loop gain. (b) Output impedance: The converter shows indistinguishable closed-loop performance.



(a)



(b)

Fig. 3.19. Converter 1 with input filters: (a) Block diagram. (b) Impedance comparison: To minimize the detrimental effects on the converter performance, the input filter is designed so that $|Z_{OF}| << |Z_{IC}|$ for all frequencies.

input filter and power stage, the output impedance of the input filter (Z_{OF} in Fig. 3.19(a)) must be sufficiently lower than the closed-loop input impedance of the power stage (Z_{IC} in Fig. 3.19(a)) for all frequencies, as will be discussed in Chapter 4.

For a converter with a high loop-gain crossover frequency, the minimum magnitude of the closed-loop input impedance of the power stage is determined by its dc value [E1,E2]:

$$|Z_{IC}|_{\min} \approx |Z_{IC}|_{dc} \tag{3.12}$$

If a regulated converter is assumed to be 100 % efficient, then its input power must equal its output power. This forces a converter to draw a constant amount power for the given load condition. If the input voltage of a converter (V_S) increases, the input current (I_S) must decrease to maintain the fixed power level of $P_S = V_S I_S$. This causes the input impedance of a converter to have a negative dynamic resistance characteristic at dc:

$$|Z_I|_{dc} = \frac{dV_S}{dI_S} = \frac{d}{dI_S}\frac{P_S}{I_S} = -\frac{P_S}{I_S^2} = -\frac{V_S}{I_S} = -\frac{1}{\mu^2}\frac{V_O}{I_O} \tag{3.13}$$

where V_O is the dc output voltage, I_O is the dc current drawn from the converter, and μ is the forward voltage gain of the converter. For an isolated multi-module full-bridge PWM converter, Eqs. (3.12) and (3.13) can be combined as:

$$|Z_I|_{\min} \approx |Z_I|_{dc} = k\frac{R_{DC}}{n^2 D^2} \tag{3.14}$$

where

k: number of modules,

n: turns ratio of the power transformer (1:n),

R_{DC}: dc load of the (multi-module) converter, and

D: duty cycle of each switch with respect to the ripple frequency.

Once $|Z_{IC}|_{\min}$ is determined from Eq. (3.14), an input filter can be designed to offer a sufficient gap between $|Z_{IC}|_{\min}$ and the maximum magnitude of its output impedance ($|Z_{OF}|_{\max}$). This guarantees a wide separation between the output impedance of the filter and the input impedance of the power stage for all frequencies. Figure 3.19(b) shows the input impedance of the first module of Converter 1 and the output impedance of the filter. The upper curve is the input impedance of the power stage, whose minimum magnitude is calculated as 76 dB from Eq. (3.14). The lower curve is the output impedance of the filter, designed to offer a 13 dB gap between $|Z_{OF}|_{\max}$ and $|Z_{IC}|_{\min}$.

3.4.5 Transient Response of System

Time-domain simulations were performed to verify the small-signal analysis and to investigate the large-signal dynamics of the system. Figure 3.20 illustrates the transient response of five outputs of the system, due to a step change in the load current through R_{AC} (step size, I_{step}=117 A). The maximum undershoot ($V_{\min}$) and settling time (t_s) of

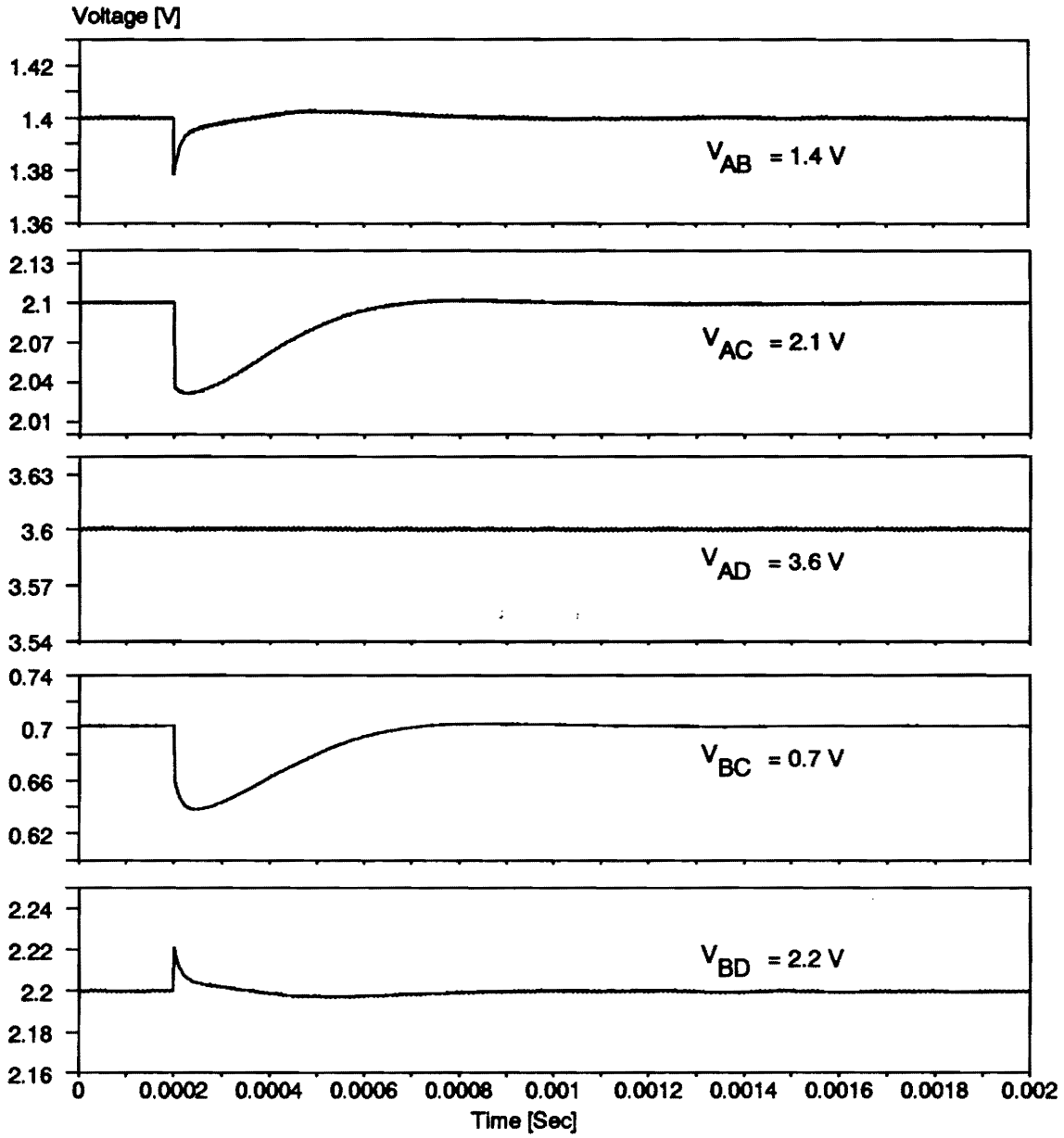


Fig. 3.20. Transient response of the outputs due to the step load change: V_{AC} can be closely predicted from the output impedance of Converter 2 shown in Fig. 3.17(b).

V_{AC} (output of Converter 2) can be predicted from the peak value ($|Z_{OC}|_{max}$) and the corner frequency (ω_p) of the output impedance of Converter 2 shown in Fig. 3.17(b) [D1]:

$$V_{min} = 2.1 - I_{step} \times |Z_{OC}|_{max} = 2.034\,V, \tag{3.15}$$

$$t_s = \frac{3}{\omega_p} = 0.48\,mS. \tag{3.16}$$

To avoid the shut-down of the entire power system due to a single point failure, each converter employs a number of modules in parallel, providing a built-in redundancy for the system. Also, to ensure the continuous operation of the computer system down-stream, each converter employs a feedback from the output capacitor of each module, minimizing the disturbance in the system outputs when one module fails. Figures 3.21 and 3.22 illustrate the transient response of the system, due to the switch-open failure (switches are stuck in the open circuit positions at 0.2 mS) of the fourth module of Converter 2. Figure 3.21 shows the transient response of inductor currents of three converters in the system. The inductor current of the failed module of Converter 2 (the second curve) decreases linearly until blocked by freewheeling diodes. The inductor current of the operational module of Converter 2 (the third curve) increases to supplement the load current of the failed module. Figure 3.22 shows the transient responses of five outputs of the system. V_{AC}, the output of Converter 2, experiences the maximum undershoot of 0.12 V. V_{BC}, the differential voltage between the outputs of Converter 2 and Converter 1, is directly affected by the failure of Converter 2, and exhibits essentially the same disturbance as V_{AC}.

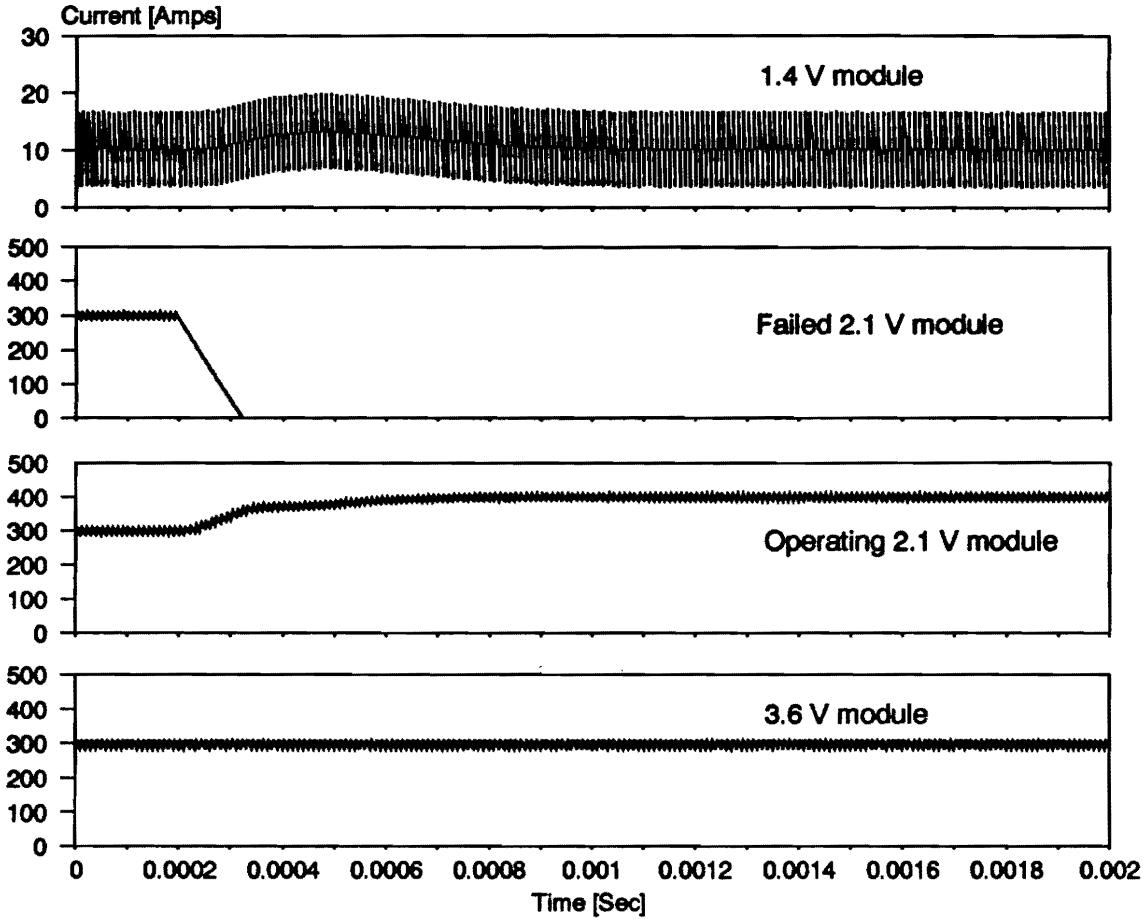


Fig. 3.21. Transient response of the inductor currents due to the switch-open failure of the fourth module of Converter 2.

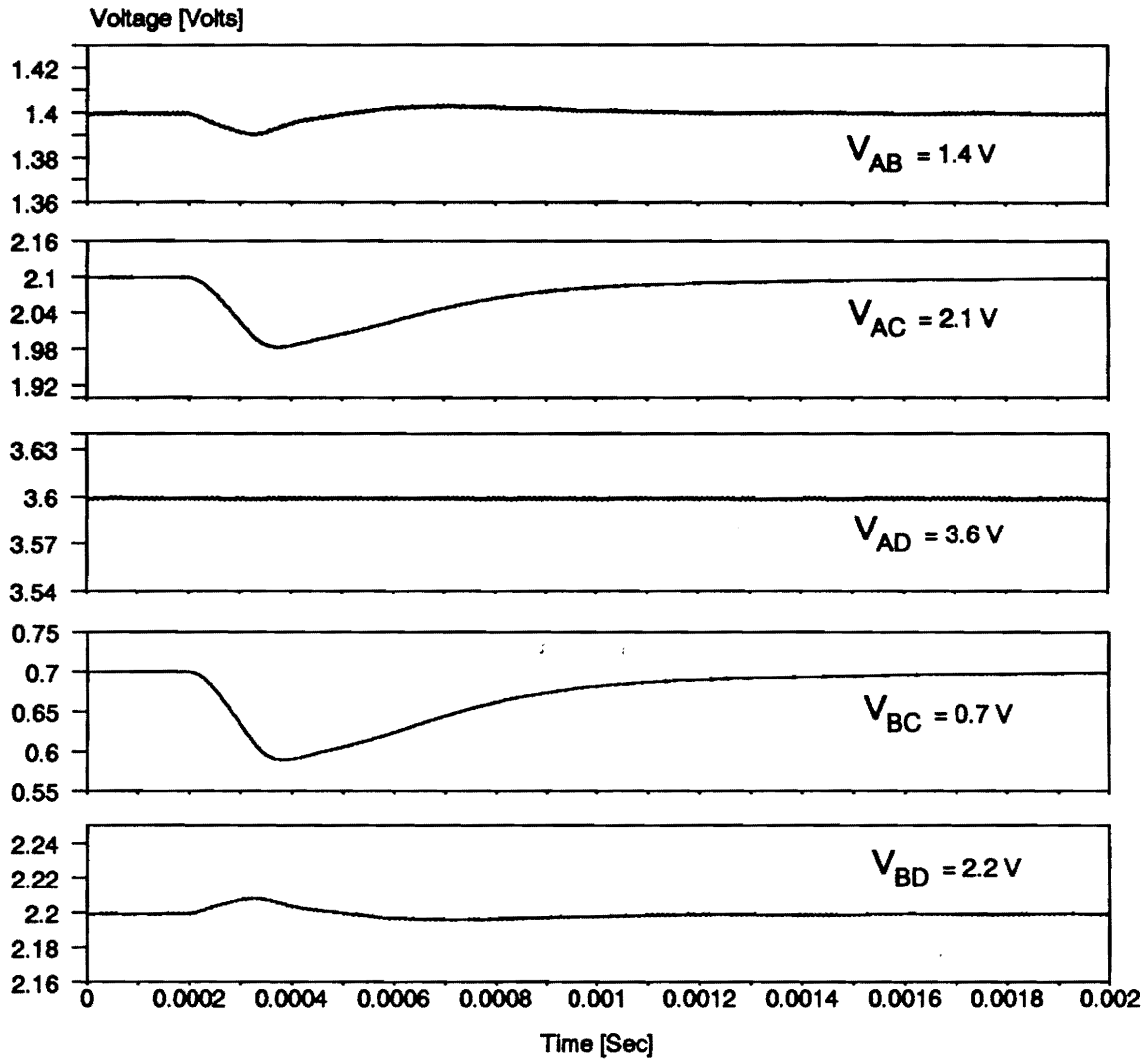


Fig. 3.22. Transient response of the outputs due to the switch-open failure of the fourth module of Converter 2.

3.5 SUMMARY

This chapter presented the analysis and design of stacked power systems. Based on a comprehensive system level analysis, systematic design procedures are established, which can be adapted to stacked power systems in general.

Step 1: System Decomposition

- Identify the load impedance (ac load) of each converter as a combination of the load resistors and the output impedances of the other converters.
- Determine the dc operating point of each converter (dc load).
- Decompose the system into individual converters using the ac load and dc load of each converter. With this decomposition, the design problem of the multiple-sourced power system is reduced to that of decoupled converters.

Step 2: Control Design of Each Converter Using ac Load

- Derive an equivalent resistive load from the load impedance by replacing the output impedances of the other converters with ESRs of their output capacitors.
- Optimize the control loop using its respective equivalent resistive load. The results of Chapter 2 can be used for multi-module converters with three-loop control.

Step 3: Input Filter Design of Each Converter Using dc Load

- Estimate the minimum magnitude of the input impedance of the power stage from dc load using Eq. (3.14).
- Design an input filter whose output impedance is sufficiently lower than the input impedance of the power stage for all frequencies. Detailed design procedures for input filters will be given in Section 4.4.

These design procedures naturally incorporate all subsystem interactions and optimize the overall performance of the entire system. The proposed design procedures are successfully adapted to the design of the three-stage stacked power system for the IBM390 mainframe computer. The validity of the design is confirmed by both small-signal analysis and time-domain simulations.

CHAPTER 4

MULTI-STAGE DISTRIBUTED POWER SYSTEMS

4.1 INTRODUCTION

The central feature of multi-stage distributed power systems is the use of cascaded stages of converters to improve conversion efficiency, load regulation, power density, and dynamic response [B1,B3,B10-B22]. However, together with its associated benefits, cascading stages of converters presents an important design consideration as well. When two converter stages are cascaded, the first converter stage (line conditioner) sees the input impedance of the second converter stage (load converter) as its load impedance. Due to the non-resistive nature of the load impedance, the dynamics of a line conditioner differ markedly from those of a conventional converter and require a control design correctly reflecting these effects. As demonstrated in [B19], a line conditioner designed for a resistive load could experience a severe performance degradation or even instability when combined with the load converter.

For most practical applications, an intermediate filter stage must be employed between two cascaded converters, in order to prevent the pulsating input current of the load converter from being reflected to the line conditioner. It is well known that a filter stage could adversely interact with the switching regulator, resulting in a performance degradation or even instability of the integrated system. The intermediate filter employed between two cascaded converters sees a switching regulator as a load subsystem, and at the same time it sees another switching regulator as a source subsystem. Thus when

designing an intermediate filter, interactions must be avoided not only with the load converter bus also with the line conditioner in order to ensure the stability of the entire system. As will be shown in Section 4.4, the design goals of avoiding interactions at both sides of the filter are conflicting, and a systematic design strategy is necessary to meet the design goals. Moreover, when the line conditioner feeds several load converters through a common distribution bus, the intermediate filter must be designed considering the parallel interactions among load converters as well.

This chapter presents the modeling and design issues involved with cascading stages of converters and intermediate filters. Section 4.2 reviews the results of subsystem interaction analysis and addresses a criterion to determine the system stability and the degree of interactions between two cascaded subsystems. Section 4.3 discusses design considerations for cascaded converters and presents an unterminated modeling and design approach which allows the design optimization of the cascaded converter independently from its load impedance. Section 4.4 discusses the design of intermediate filters. A design strategy to avoid interactions at both sides of the filter is presented. The design strategy is substantiated by developing step-by-step design procedures for both single-stage and two-stage filters. This section also discusses additional design constraints imposed by parallel interactions between load converters connected to a common distribution bus. Section 4.5 presents the design of a two-module zero-voltage-switched full-bridge (ZVS-FB) PWM [D9] line conditioner for a three-stage distributed power application. This section demonstrates how the results of this chapter can be integrated to design the line conditioner and its input filter, ensuring the stability and compatibility of the integrated system.

4.2 SUBSYSTEM INTERACTION ANALYSIS

This section reviews general results of the subsystem interaction analysis. Detailed discussions on this subject can be found in [E1,F1].

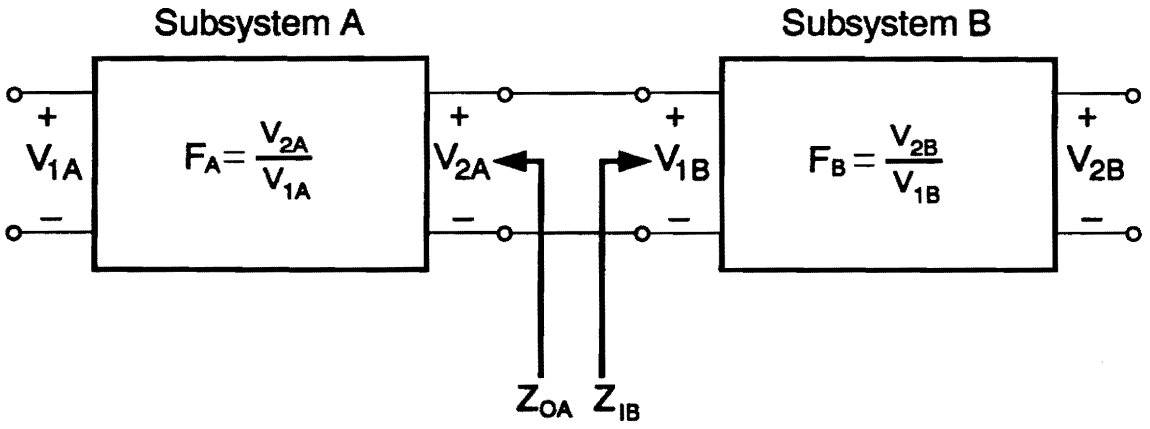
Figure 4.1 shows two subsystems connected in series. Initially, it is assumed that each subsystem is stable and well designed for its stand-alone operation. Subsystem A has an input-to-output transfer function of F_A, and Subsystem B has an input-to-output transfer function of F_B. The overall input-to-output transfer function of the integrated system is given by [F1]:

$$F_{AB} = \frac{V_{2B}}{V_{1A}} = \frac{F_A F_B}{1 + Z_{OA}/Z_{IB}} \tag{4.1}$$

where Z_{OA} is the output impedance of Subsystem A, and Z_{IB} is the input impedance of Subsystem B. It has been shown in the literature [B17,B18,F1] that the denominator of Eq. (4.1) contains all information necessary to analyze the system stability and subsystem interactions. The stability of the integrated system can be determined by applying the Nyquist stability criterion [F3] to Z_{OA}/Z_{IB}, and the degree of interactions is determined by the relative magnitude of $|Z_{OA}|$ and $|Z_{IB}|$.

Case 1. $|Z_{OA}| << |Z_{IB}|$ for all frequencies (minimal interactions):

Two subsystems are essentially decoupled. The overall input-to-output transfer function of the integrated system is the product of the transfer functions of individual subsystems. The overall system is stable, and interactions are negligible.



$$\frac{V_{2B}}{V_{1A}} = \frac{F_A F_B}{1 + \frac{Z_{OA}}{Z_{IB}}}$$

Fig. 4.1. Two cascaded subsystems: The condition $|Z_{OA}| << |Z_{IB}|$ ensures minimal subsystem interactions and the stability of the integrated system.

Case 2. $|Z_{OA}| < |Z_{IB}|$ for all frequencies (non-minimal interactions):

There are certain degree of interactions. However, the integrated system is stable as long as subsystems are individually stable.

Case 3. $|Z_{OA}| > |Z_{IB}|$ for some frequencies (strong interactions):

Relatively strong interactions occur. The integrated system could become unstable, although the subsystems are individually stable. The Nyquist criterion must be applied to Z_{OA}/Z_{IB} to determine the stability of the integrated system.

For both stability and minimal interactions, it is essential to minimize the output impedance of Subsystem A and to maximize the input impedance of Subsystem B. A wide separation of these two impedances minimizes subsystem interactions and guarantees the stability of the integrated system. Throughout this chapter, this criterion will be used as the theoretical basis of design strategies for multi-stage distributed power systems.

4.3 UNTERMINATED MODELING AND DESIGN OF CASCADED CONVERTERS

A line conditioner driving a load converter downstream sees the input impedance of a switching regulator, Z_{IC}, as its load impedance. The input impedance of a switching regulator is a complex frequency-dependent quantity, and often complicates the analysis and design of a line conditioner. An approach to eluding such a complication is to use a simple approximation for Z_{IC}. As demonstrated in [B12], Z_{IC} behaves like a negative resistance up to the crossover frequency of the loop gain. Thus for analysis and design purposes, the load impedance of the line conditioner may be replaced with a negative resistance $-R$, the ratio of the input voltage and the input current of the load converter. However, such a simple approach may not be valid when an input filter is added to the load converter. As an example, Fig. 4.2 compares the input impedance of a buck converter without input filter, the $-R$ approximation, and the input impedance of the converter with input filter. While the $-R$ closely approximates the low- and mid-frequency behavior of the input impedance without input filter, it apparently fails to predict the input impedance with the presence of the input filter.

Ideally, it is desirable to consider the actual load impedance in designing a line conditioner. However, in many practical applications, the load dynamics of a line conditioner are highly complex or not available in advance. To deal with this problem, the line conditioner can be modeled as an unterminated stand-alone regulator without considering the load impedance. Based on dynamics of the unterminated line conditioner, the control can be designed to minimize the undesirable interactions with the load

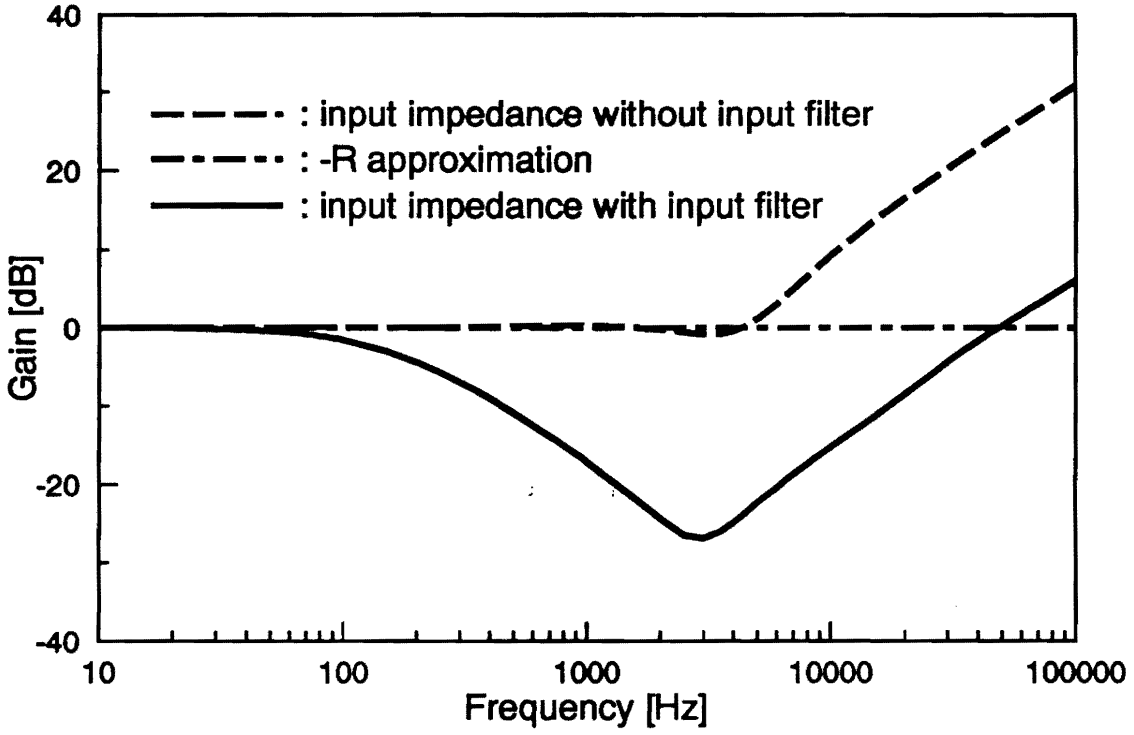


Fig. 4.2. Comparison of input impedance of load subsystem with -R approximation.

subsystem while providing a good performance for the line conditioner. This approach is particularly useful when dynamic characteristics of the load are not available in advance. Also, the design results can be readily verified using a constant current sink load.

Figure 4.3 shows the unterminated model of a current-mode controlled line conditioner. The current sink at the output port represents the dc current drawn from the power stage, and indicates that the line conditioner is unterminated in the small-signal sense. From Fig. 4.3, the open-loop transfer functions can be derived in terms of output voltage and output current. After designing the current loop based on the open-loop characteristics and large-signal constraints, the control-to-output transfer function, $\hat{v}_o/\hat{v}_c$, can be derived. Using the control-to-output transfer function with the current-loop closed, the voltage feedback compensation can be designed similar to that of the load-terminated case. By shaping the loop gain, T, in Fig. 4.3, the stability and dynamic performance of the unterminated line conditioner can be optimized. It is particularly important to minimize the output impedance of the unterminated line conditioner, in order to ensure the stability after integration and minimal interactions with the load subsystem.

Once the control design is optimized for the unterminated line conditioner, the compatibility between line conditioner and load subsystem can be assessed using impedances at the interface of two subsystems, as discussed in the previous section. Complete details about the unterminated modeling and design of the line conditioner will be provided in Section 4.5, which covers the design of a two-module ZVS-FB-PWM line conditioner.

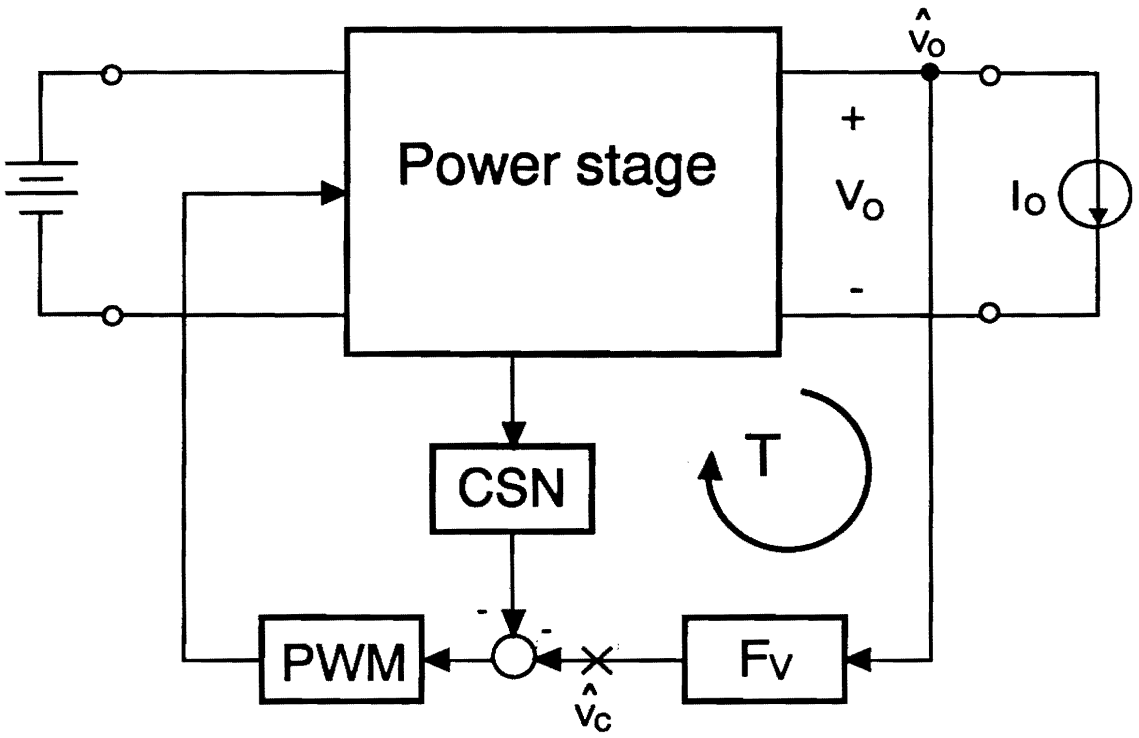


Fig. 4.3. Unterminated model of line conditioner: The current sink at the output port indicates that the line conditioner is unterminated in the small-signal sense.

4.4 DESIGN CONSIDERATIONS FOR INTERMEDIATE FILTERS

This section presents design considerations for intermediate filters. After establishing a general design strategy, step-by-step design procedures for both single-stage and two-stage filters are presented. This section also addresses the additional design considerations for intermediate filters employed between the line conditioner and several load converters connected through a common distribution bus.

4.4.1 Design Strategy

Figure 4.4 shows a simple distributed power system consisting of a line conditioner, an intermediate filter, and a load converter. As discussed in Section 4.1, the intermediate filter must avoid interactions with converters at both sides of the filter, while providing a desired current attenuation. These requirements can be itemized as follows:

- a specified current attenuation, A_{IF}, to smooth out the pulsating input current of the load converter,
- the highest possible input impedance, Z_{IF}, to minimize interactions with the line conditioner, and
- the lowest possible output impedance, Z_{OF}, to minimize interactions with the load converter.

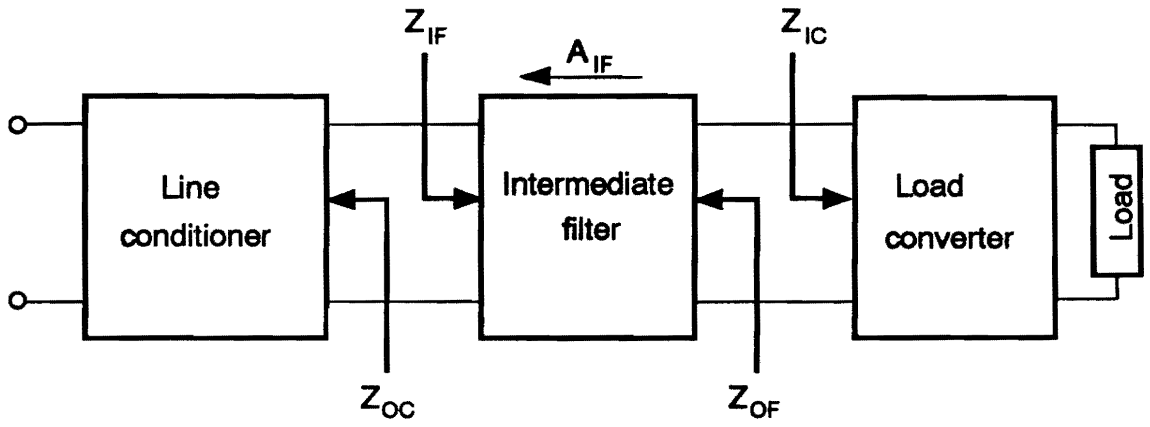


Fig. 4.4. Intermediate filter between two cascaded converter stages: In order to avoid interactions at both interfaces, the filter should be designed so that $|Z_{OC}| \ll |Z_{IF}|$ and $|Z_{OF}| \ll |Z_{IC}|$ for all frequencies.

It is important to note that the design goals of large input impedance and low output impedance are conflicting. Since both the input impedance and the output impedance of a filter are proportional to its characteristic resistance [E2], the filter designed for a large input impedance produces a large output impedance as well. Thus a careful design trade-off should be made to compromise these conflicting requirements for intermediate filters. One design strategy, offering both minimal interactions and desired current attenuation, is given as follows:

1. determine the current attenuation desired at the switching frequency.

2. estimate the maximum magnitude of the output impedance ($|Z_{OC}|_{max}$) of the line conditioner.

3. estimate the minimum magnitude of the input impedance ($|Z_{IC}|_{min}$) of the load converter.

4. design the filter so that:

$$|Z_{IF}|_{min} = |Z_{OF}|_{max} = \frac{|Z_{IC}|_{min} + |Z_{OC}|_{max}}{2k} \quad (1 \le k), \tag{4.2}$$

while providing the desired current attenuation.

This design strategy is graphically illustrated in Fig. 4.5, assuming $|Z_{OC}| \ll |Z_{IC}|$ (true for most practical applications). When k is selected as 1, the design guarantees an impedance gap of:

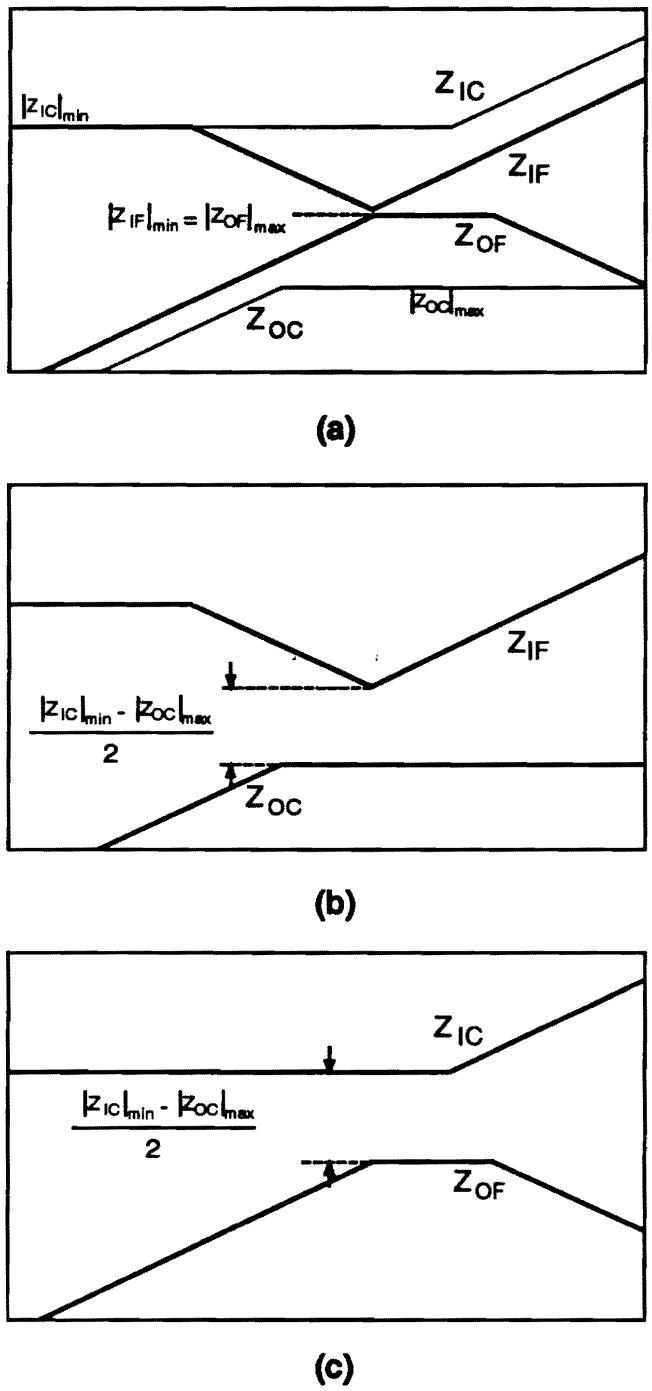


Fig. 4.5. Intermediate filter design: (a) Design strategy. (b) Impedance comparison at front interface. (c) Impedance comparison at rear interface: The design offers the same impedance gap at both sides of the filter.

$$|Z|_{gap} = \frac{|Z_{IC}|_{min} - |Z_{OC}|_{max}}{2} \tag{4.3}$$

at both ends of the intermediate filter, as shown in Figs. 4.5(b) and (c). If $|Z_{IC}|_{min}$ is at least 20 dB larger than $|Z_{OC}|_{max}$, the intermediate filter offers a 10 dB impedance gap at both sides, which would prevent any significant interactions with the converter.

In Eq. (4.2), k provides a design trade-off in determining impedance gaps at both side of the filter. The larger k offers a wider impedance gap between $|Z_{OF}|_{max}$ and $|Z_{IC}|_{min}$ at the expense of a narrower gap between $|Z_{OC}|_{max}$ and $|Z_{IF}|_{min}$. If the condition $|Z_{OC}| \ll |Z_{IC}|$ is not satisfied, a larger $k (\geq 1)$ is necessary, since the interaction at the rear interface is more detrimental than that at the front interface. The input impedance of the load converter has a -180° phase characteristic up to the crossover frequency of its loop gain. This could cause a severe degradation in the performance of the load converter if the condition $|Z_{OF}| \ll |Z_{IC}|$ is violated. Also, while the condition $|Z_{OC}| > |Z_{IF}|$ does not necessary cause instability, the condition $|Z_{OF}| > |Z_{IC}|$ is highly susceptible to instability.

The implementation of this design strategy needs two prerequisites. The first is the prior knowledge of $|Z_{OC}|_{max}$ and $|Z_{IC}|_{min}$. While $|Z_{OC}|_{max}$ can be obtained from either measurement or small-signal analysis, $|Z_{IC}|_{min}$ can be closely predicted from the dc operating point of the load converter, as discussed in Section 3.4.4. The second is systematic design procedures for intermediate filters, which simultaneously meet specifications for input impedance, output impedance, and current attenuation. In the next sections, design procedures for several useful filter topologies are presented.

4.4.2 Single-Stage Filter with Damping Branch

Figure 4.6(a) shows a single-stage filter with a damping branch, which has been widely used for low- and medium-current applications [E1,E2]. The current attenuation, A_{IF}, the input impedance, Z_{IF}, and the output impedance, Z_{OF}, of the filter can be approximated as:

$$A_{IF} \approx \frac{1}{1 + s/Q\omega_o + s^2/\omega_o^2} \tag{4.4}$$

$$Z_{IF} \approx \frac{(1 + sC_BR_d)(1 + s/Q\omega_o + s^2/\omega_o^2)}{s(C + C_B)\left(1 + s\frac{C_BC}{C_B + C}R_d\right)} \tag{4.5}$$

$$Z_{OF} \approx \frac{sL}{1 + s/Q\omega_o + s^2/\omega_o^2} \tag{4.6}$$

where

$$Q = R_d\sqrt{\frac{C}{L}}, \quad \omega_o = \frac{1}{\sqrt{LC}}$$

with assumptions $C_B \gg C$, $C_BR_d \gg L/R_d$. These assumptions simplify the analysis and also are desirable in practice. Since the sole function of C_B is to block dc current from the damping resistor R_d, C_B should be considerably larger than C to avoid any excessive loss.

Figure 4.6(b) shows the asymptotic plots of the transfer functions given by Eqs. (4.4) through (4.6). The current attenuation has a -40 dB/dec slope at high frequencies.

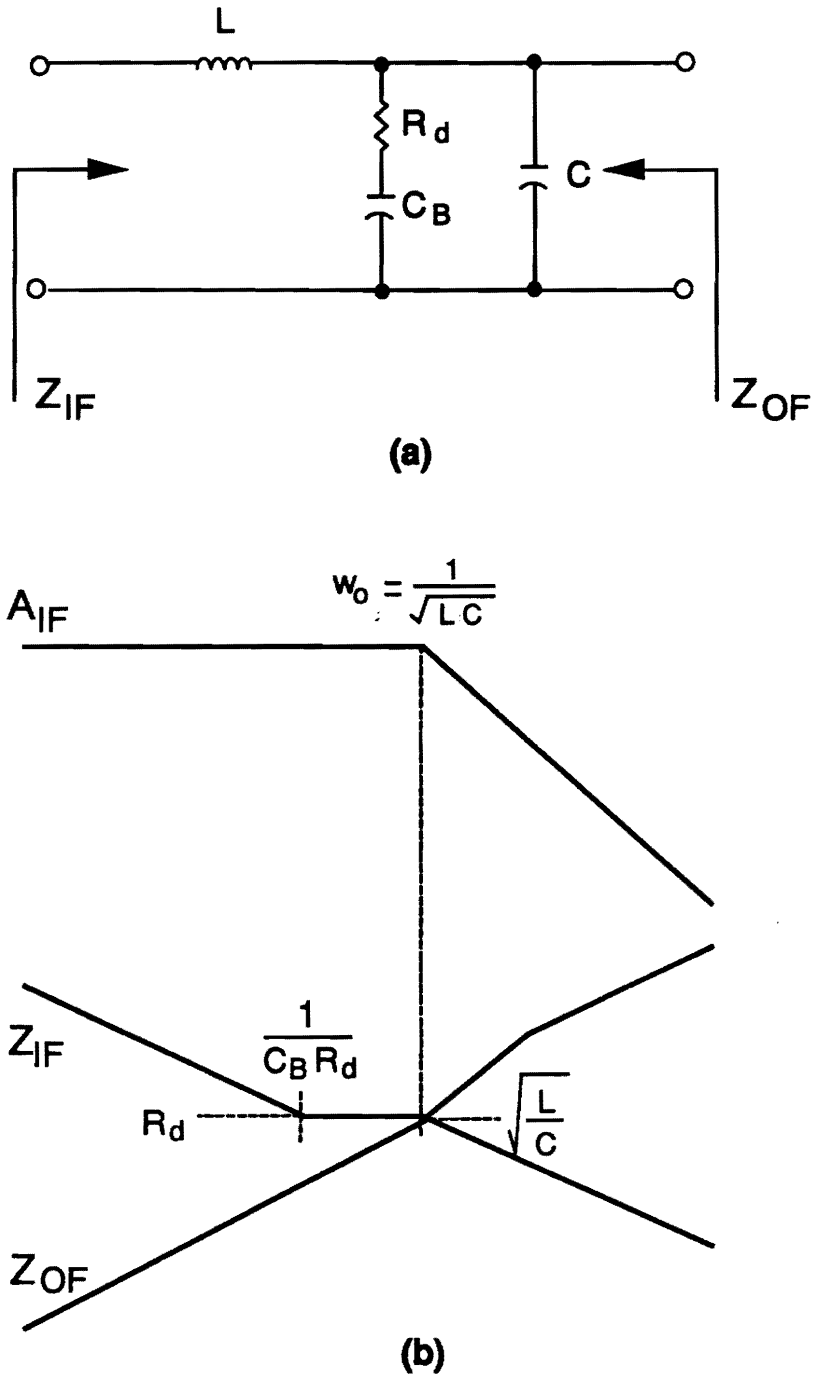


Fig. 4.6. Single-stage filter with damping branch: (a) Filter parameters. (b) Transfer functions: The RC branch provides a lossless damping without compromising any filtering properties [E2].

The input impedance has a flat gain between the corner frequency of $1/C_B R_d$ and the resonant frequency. This flat gain determines the minimum magnitude and can be approximated as:

$$|Z_{IF}|_{\min} \approx \left.\frac{1+sC_B R_d}{s(C+C_B)}\right|_{s\to\infty} \approx R_d \tag{4.7}$$

The output impedance has a peak at the resonant frequency, which can be approximated as:

$$|Z_{OF}|_{\max} \approx sL\,|_{s=\frac{1}{\sqrt{LC}}} = \sqrt{\frac{L}{C}} \tag{4.8}$$

assuming a sufficient damping for the resonance.

To achieve the design goal of $|Z_{IF}|_{\min} \approx |Z_{OF}|_{\max}$, it can be assumed that:

$$Q = R_d\sqrt{\frac{C}{L}} = 1 \tag{4.9}$$

which implies $|Z_{IF}|_{\min} = |Z_{OF}|_{\max} = R_d$. The condition of $Q = 1$ also ensures a sufficient damping for the resonance, which was assumed in Eqs. (4.7) and (4.8).

Based on the above analysis, design procedures can be formulated to realize the design strategy discussed in Section 4.4.1. A design example is given to illustrate the design procedures.

Design Example

Assumptions:

- maximum magnitude of the output impedance of line conditioner: $|Z_{OC}|_{\max} = -10 \quad dB$.
- minimum magnitude of the input impedance of load converter: $|Z_{IC}|_{\min} = 20 \quad dB$.
- input current of the load converter: 100 kHz pulse train with a peak of 7.5 A.

Filter Specification:

- 35 dB current attenuation at 100 kHz for 0.13 A current ripple at the output of the line conditioner.
- $|Z_{OF}|_{\max} = |Z_{IF}|_{\min} = 5 \quad dB$ to offer a 15 dB margin at both sides of the filter.
- $C_B = 10 \times C$.

Design Procedures

1. Calculate the LC product from the current attenuation specification:

$$-40\log\frac{f_s}{f_o} = -35, \qquad f_o = \frac{1}{2\pi\sqrt{LC}} \quad \Rightarrow LC = 1.426 \times 10^{-10}.$$

2. Determine R_d using:

$$|Z_{OF}|_{\max} = |Z_{IF}|_{\min} = 20\log R_d = 5dB \qquad \Rightarrow \quad R_d = 10^{5/20} = 1.78\Omega.$$

3. Calculate L, C, and C_B using:

$$Q = R_d\sqrt{\frac{C}{L}} = 1, \quad LC = 1.426\times 10^{-10}, \quad C_B = 10\times C \quad \Rightarrow \quad L = 21.3\mu H, \quad C = 6.7\mu F, \quad C_B = 67\mu F.$$

It can be easily shown that this design procedures automatically satisfy the assumption $C_B R_d \gg L/R_d$. Figure 4.7 shows the transfer functions of the resulting filter. The filter offers the desired impedance margin of 15 dB at both sides, and a 35 dB current attenuation at 100 kHz.

4.4.3 Two-Stage Filter

Figure 4.8(a) shows a two-stage filter which has been widely used for high-current applications [E1,E2,E4]. The current attenuation, the input impedance, and the output impedance of the filter can be approximated as:

$$A_{IF} \approx \frac{(1+s/\omega_{z1})}{(1+s/Q_1\omega_{o1}+s^2/\omega_{o1}^2)(1+s/Q_2\omega_{o2}+s^2/\omega_{o2}^2)} \tag{4.10}$$

$$Z_{IF} \approx \frac{(1+s/Q_1\omega_{o1}+s^2/\omega_{o1}^2)}{sC_1} \tag{4.11}$$

$$Z_{OF} \approx \frac{sL_1(1+s/\omega_{z1})(1+s/\omega_{z2})}{(1+s/Q_1\omega_{o1}+s^2/\omega_{o1}^2)(1+s/Q_2\omega_{o2}+s^2/\omega_{o2}^2)} \tag{4.12}$$

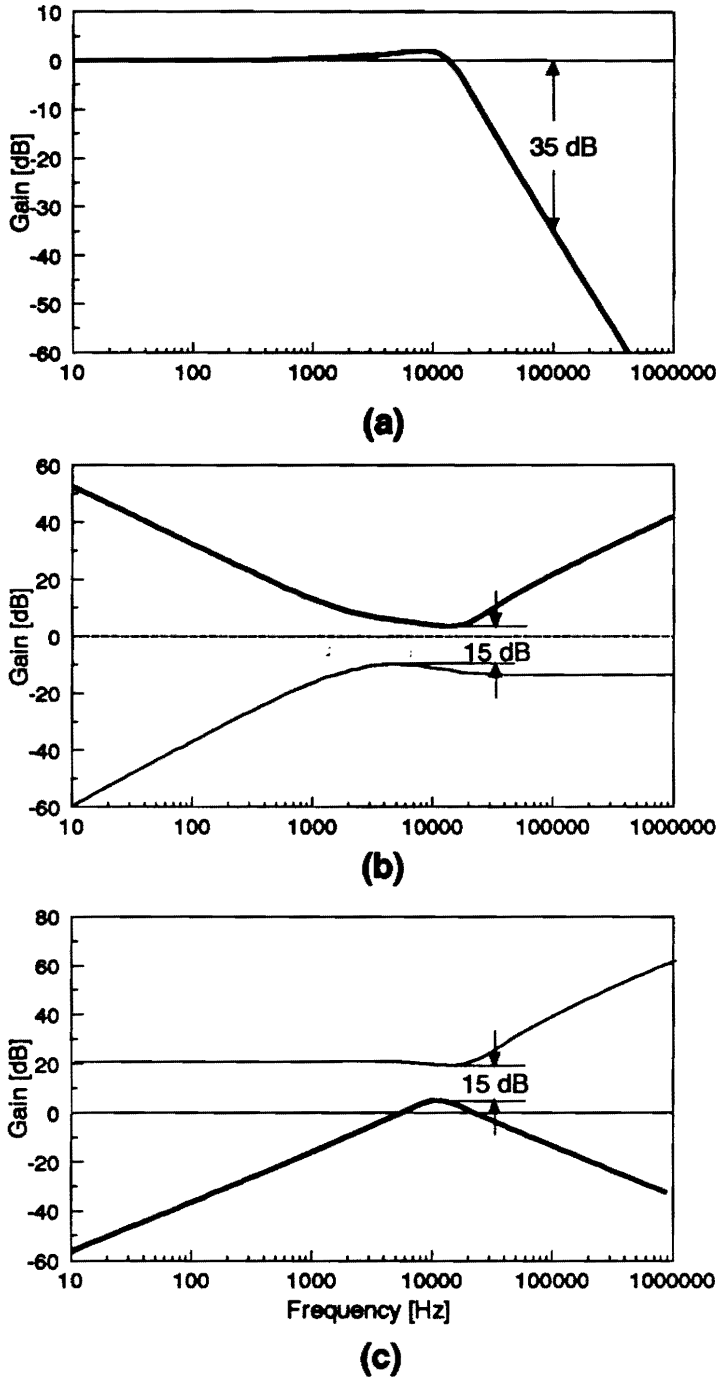


Fig. 4.7. Transfer functions of single-stage filter: (a) Current attenuation. (b) Input impedance. (c) Output impedance.

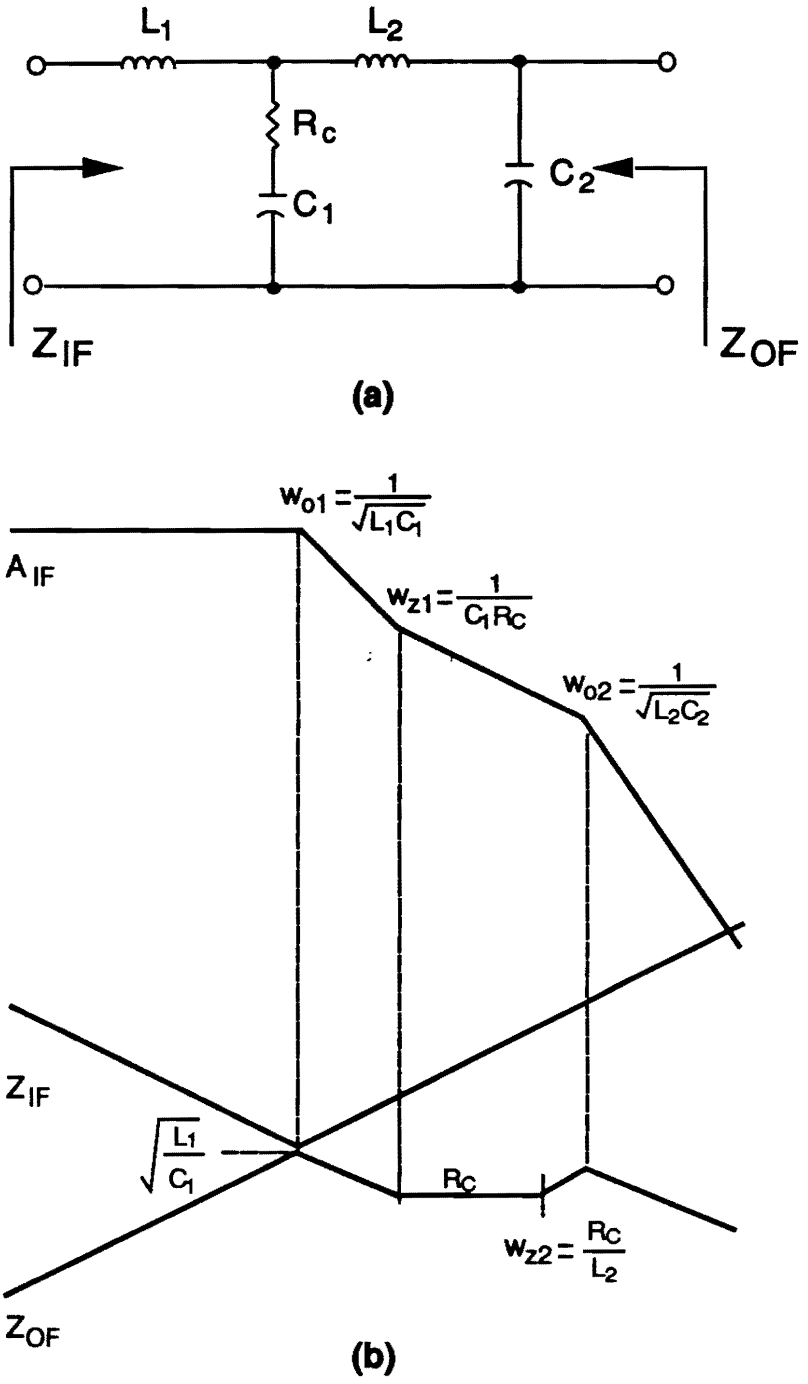


Fig. 4.8. Two-stage filter: (a) Filter parameters. (b) Transfer functions: The damping resistor R_C provides a damping for both low- and high-frequency resonances.

where

$$Q_1 = \frac{1}{R_C}\sqrt{\frac{L_1}{C_1}} \qquad \omega_{o1} = \frac{1}{\sqrt{L_1 C_1}}$$

$$Q_2 = \frac{1}{R_C}\sqrt{\frac{L_2}{C_2}} \qquad \omega_{o2} = \frac{1}{\sqrt{L_2 C_2}}$$

$$\omega_{z1} = \frac{1}{C_1 R_C} \qquad \omega_{z2} = \frac{R_C}{L_2}$$

with assumptions $L_1 >> L_2$, $C_1 >> C_2$, $L_1 >> R_C^2 C_2$, and $C_1 >> L_2/R_C^2$. These assumptions make the analysis tractable and are a good design practice. These conditions ensure a wide separation of the two resonant frequencies, allowing the filter to have a smaller output impedance and a larger input impedance when compared with a filter not satisfying these conditions [E1].

Figure 4.8(b) shows asymptotic plots of the transfer functions given by Eqs. (4.10) through (4.12). The current attenuation, A_{IF}, has one zero and four poles, giving a high frequency slope of -60 dB/sec. The input impedance, Z_{IF}, has one resonance, and its minimum value can be approximated as:

$$|Z_{IF}|_{\min} \approx \left.\frac{1}{sC_1}\right|_{s=1/\sqrt{L_1 C_1}} = \sqrt{\frac{L_1}{C_1}} \tag{4.13}$$

The output impedance, Z_{OF}, has a flat gain between two resonant frequencies of ω_{o1} and ω_{o2}. The flat gain in the mid band can be approximated as:

$$|Z_{OF}|_{mid} \approx \frac{sL_1(1+s/\omega_{z1})}{(1+s/Q_1\omega_{o1}+s^2/\omega_{o1}^2)}\bigg|_{s=\infty} = R_C \tag{4.14}$$

If $|\omega_{o1}-\omega_{z1}| > |\omega_{o2}-\omega_{z2}|$ and two resonances are well damped, the peak value of the output impedance occurs at the first resonance:

$$|Z_{OF}|_{\max} \approx sL_1|_{s=1/\sqrt{L_1C_1}} = \sqrt{\frac{L_1}{C_1}} \tag{4.15}$$

From Eqs. (4.13) and (4.15), it follows:

$$|Z_{IF}|_{\min} \approx |Z_{OF}|_{\max} \approx \sqrt{\frac{L_1}{C_1}} \tag{4.16}$$

To further simplify the design and to ensure a sufficient damping, it can be assumed that $Q_1 = Q_2 = 1$. It can be easily shown that this condition is equivalent to following three conditions:

$$\frac{1}{\sqrt{L_1C_1}} = \frac{1}{R_CC_1} \tag{4.17}$$

$$\frac{1}{\sqrt{L_2C_2}} = \frac{R_C}{L_2} \tag{4.18}$$

$$|Z_{IF}|_{\min} = |Z_{OF}|_{\max} = \sqrt{\frac{L_1}{C_1}} = R_C \tag{4.19}$$

Note that Eqs. (4.17) and (4.18) are identical to conditions $\omega_{o1} = \omega_{z1}$ and $\omega_{o2} = \omega_{z2}$. Figure 4.9 shows asymptotic plots of the transfer functions of a filter with $Q_1 = Q_2 = 1$. In addition to the simplicity in design, the condition of $Q_1 = Q_2 = 1$ is a good design trade-off between the small output impedance and the large input impedance.

Based on the above analysis, design procedures can be formulated in a way similar to that presented in the previous section.

Design Example

Assumptions:

- $|Z_{OC}|_{\max} = 8 \quad dB$, and $|Z_{IC}|_{\min} = 38 \quad dB$.
- input current of the load converter: 100 kHz pulse train with a peak of 18.2 A.

Filter Specifications:

- -43 dB current attenuation at $f_S = 100\,kHz$ for 0.13 A current ripple at the output of the line conditioner.
- $|Z_{IF}|_{\min} = |Z_{OF}|_{\max} = 23 \quad dB$ to offer a 15 dB gap at both sides of the filter.
- one decade separation between the first and second resonant frequencies, f_{O1} and f_{O2}.

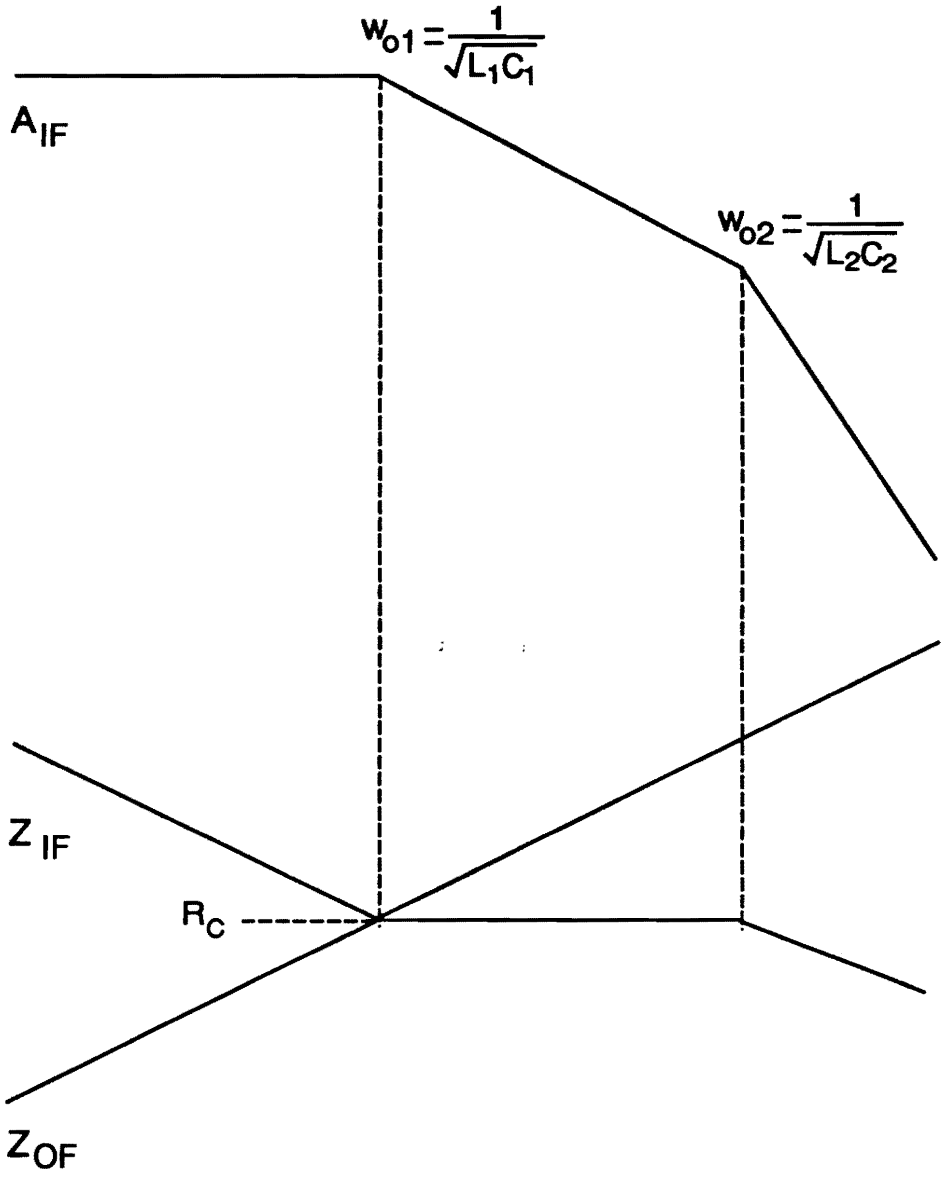


Fig. 4.9. Transfer functions of two-stage filter with $Q_1 = Q_2 = 1$: The condition $Q_1 = Q_2 = 1$ is identical to conditions $\omega_{o1} = \omega_{z1}$ and $\omega_{o2} = \omega_{z2}$.

Design Procedures:

1. Calculate the L_2C_2 product from the current attenuation specification:

$$-60\log\frac{f_s}{f_{o2}} - 20 = -43, \quad f_{o2} = \frac{1}{2\pi\sqrt{L_2C_2}} \quad \Rightarrow L_2C_2 = 1.16\times10^{-12}$$

2. Determine R_C using:

$$|Z_{OF}|_{\max} = |Z_{IF}|_{\min} = 20\log R_C = 23dB \quad \Rightarrow \quad R_C = 10^{23/20} = 14\Omega$$

3. Calculate L_2 and C_2 using:

$$Q_2 = \frac{1}{R_c}\sqrt{\frac{L_2}{C_2}} = 1, \quad L_2C_2 = 1.16\times10^{-12} \quad \Rightarrow L_2 = 54.3\mu H, \quad C_2 = 0.27\mu F$$

4. Calculate L_1 and C_1 using:

$$\frac{f_{o2}}{f_{o1}} = 10, \quad Q_1 = \frac{1}{R_c}\sqrt{\frac{L_1}{C_1}} = 1 \quad \Rightarrow L_1 = 543\mu H \quad C_1 = 2.7\mu F$$

It can be easily shown that this design procedures automatically satisfy the assumptions $L_1 \gg R_C^2C_2$ and $C_1 \gg L_2/R_C^2$. Figure 4.10 shows the transfer functions of the resulting intermediate filter. The filter satisfies all design specifications, including the current attenuation and the desired impedance gap at both sides of the filter.

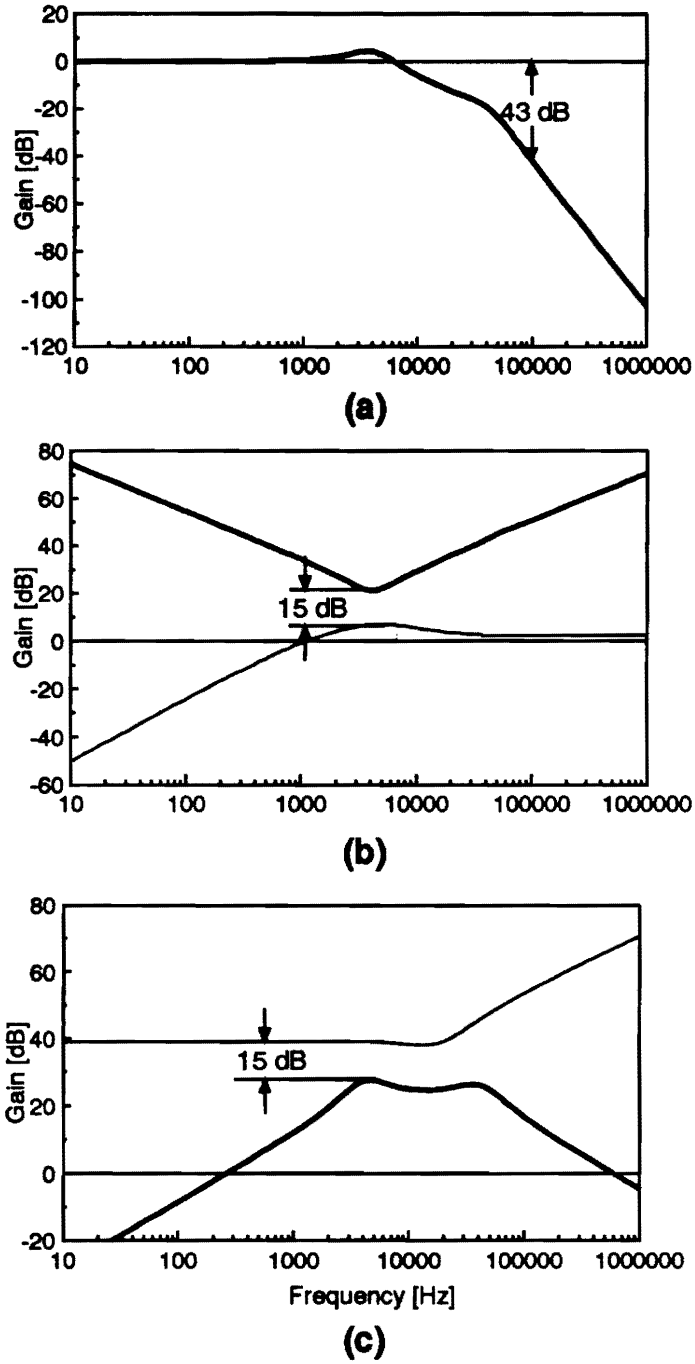


Fig. 4.10. Transfer function of two-stage filter: (a) Current attenuation. (b) Input impedance. (c) Output impedance.

4.4.4 Two-Stage Distributed Filter

In many distributed power applications, the line conditioner feeds several load converters through a common distribution bus [B11,B12,B17]. In this case, it is advantageous to use a two-stage distributed filter, with the first stage common to all, and a second stage at the input of each load converter, as shown in Fig. 4.11. The second stage is necessary to attenuate the pulsating input current of each load converter to an acceptable level at the distribution bus. The first stage is essential to further attenuate the current ripple to a specified level at the output of the line conditioner.

The two-stage filter discussed in the previous section can be adapted to Fig. 4.11 by distributing various components of the second stage. Figure 4.12(a) shows a distributed filter, obtained by distributing only the capacitor of the secondary filter stage. While this approach needs the minimum number of components, problems occur when load converters are not synchronized with a common clock. As demonstrated in [B13,B18], the phase-shifted operation of load converters develops a potential difference across each distributed capacitor, C_2, causing a large current to circulate between load converters.

Figure 4.12(b) shows a distributed filter, obtained by distributing the inductor and capacitor of the secondary filter stage. Although this topology is free from the problem of a large circulating current, it has a potential instability problem originating from parallel interactions among load converters. The damping resistor, R_C, originally intended to damp both the first and second resonances, fails to damp the second resonance due to parallel interactions among load converters [B14,B17]. As a result, a severe peaking

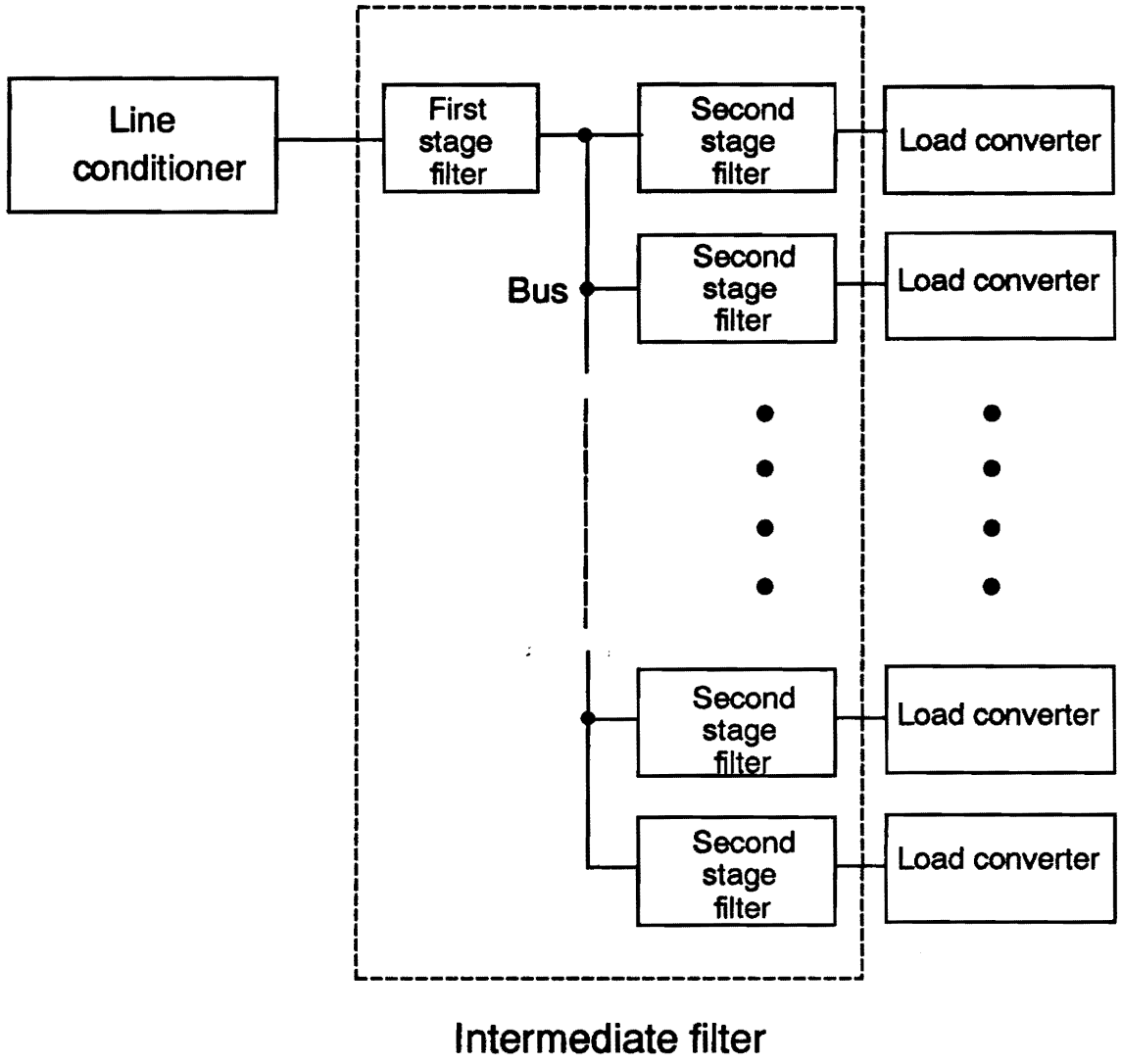


Fig. 4.11. Two-stage distributed filter: The first stage is located before the distribution bus, and the second stage is located at the input of each load converter.

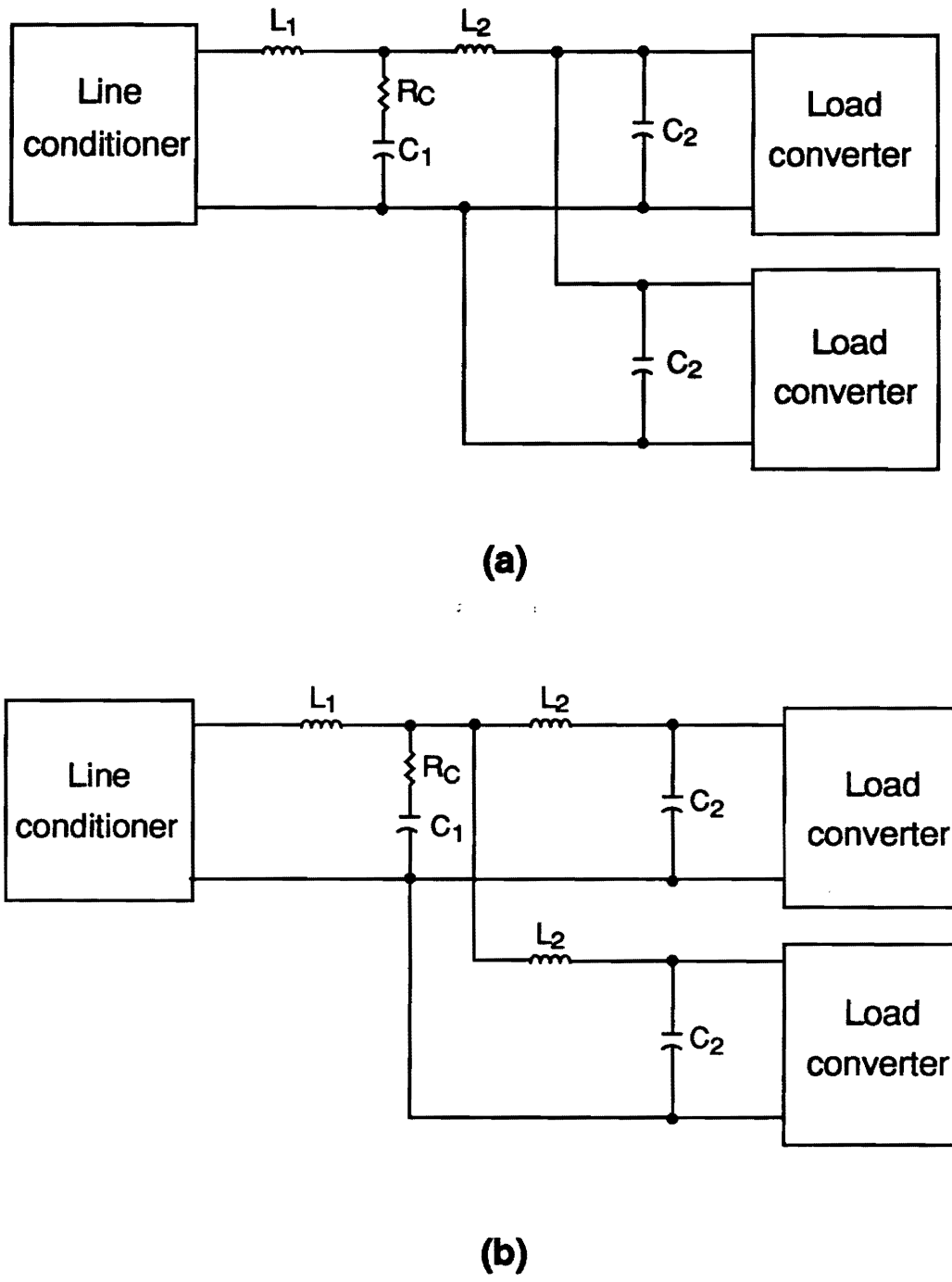


Fig. 4.12. Two-stage distributed filters: (a) Filter 1. (b) Filter 2: Filter 1 could cause a large circulating current, and Filter 2 could cause an instability.

occurs in the output impedance of the filter. This peaking could cause the output impedance of the filter to exceed the input impedance of the load converter, resulting in instability.

As the final modification, a damping branch, R_d and C_B, is added across the second stage capacitor, resulting in an improved topology of Fig. 4.13(a). The damping branch provides the necessary damping for the second resonance and minimizes the detrimental effects of parallel interactions. Figure 4.13(b) shows the effects of the damping branch on the output impedance of the filter seen by the input of each load converter.

To summarize this section, design procedures are formulated for the two-stage distributed filter.

1. Determine the current attenuation required for each load converter.

2. Determine the desired values of $|Z_{IF}|_{\min}$ and $|Z_{OF}|_{\max}$.

3. Design a two-stage filter to meet design specifications, using the procedures discussed in Section 4.4.3.

4. Place the first stage of the resulting filter before the summing junction, and place the indictor and capacitor of the secondary filter stage in the front of each load converter.

5. Add an RC damping branch to the second stage filter capacitor. The following inequalities are recommended to select the value for R_d and C_B:

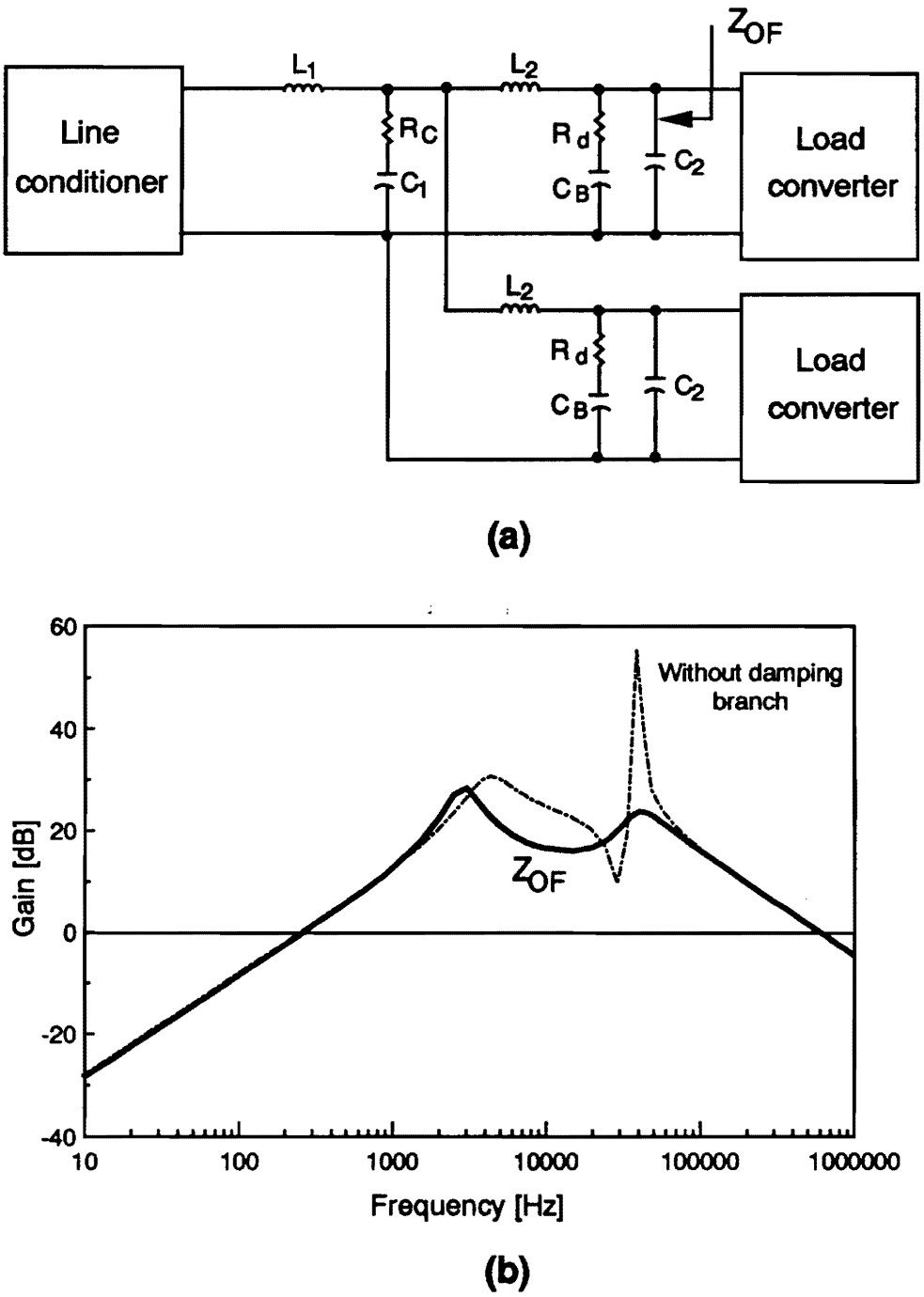


Fig. 4.13. Two-stage distributed filter: (a) Filter parameters. (b) Output impedance of the filter seen by the input of each load converter.

$$C_1 >> C_B >> C_2 \qquad R_d > R_C$$

These conditions minimize the effects of the damping branch on the current attenuation and the input impedance of the filter.

4.5 DESIGN OF TWO-MODULE A ZVS-FB-PWM LINE CONDITIONER

This section demonstrates how the results of this chapter can be integrated to design a multi-module line conditioner for a practical distributed power system. Figure 4.14 shows the block diagram of a three-stage distributed power system developed for mainframe computers. The front end is a three-phase ac-to-dc preregulator operating under the principles of six-step PWM [D10,D11]. The preregulator receives the input from three-phase utility and provides the high-voltage dc output to the line conditioner. The line conditioner employs two ZVS-FB-PWM converter modules in parallel and produces an intermediate voltage to the stacked load converter subsystem discussed in Section 3.3.

The unterminated modeling and design method is combined with the reduced-order modeling technique to optimize the control design while ensuring the stability and compatibility of the entire system. The filter design techniques developed in the previous section is adapted to the design of the input filter for line conditioner modules.

4.5.1 Control Design

Figure 4.15 shows the schematic diagram of the unterminated two-module ZVS-FB-PWM line conditioner. The system consists of two current-mode controlled ZVS-FB-PWM modules, a common output capacitor, and an output voltage feedback circuit.

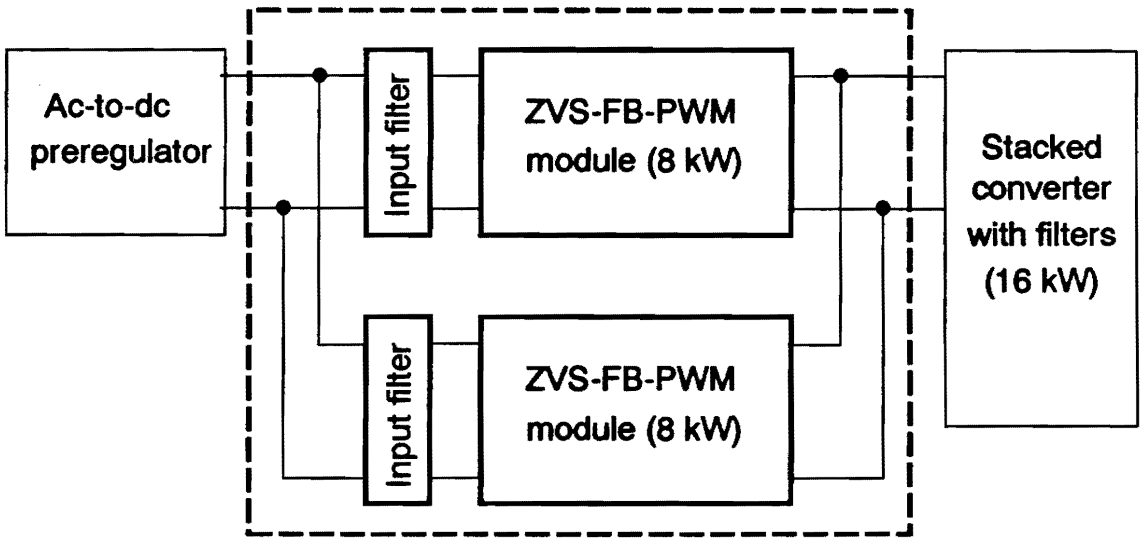


Fig. 4.14. Block diagram of three-stage distributed power system for mainframe computers: The two-module ZVS-FB-PWM line conditioner converts the output of the preregulator to an intermediate voltage for stacked load converters.

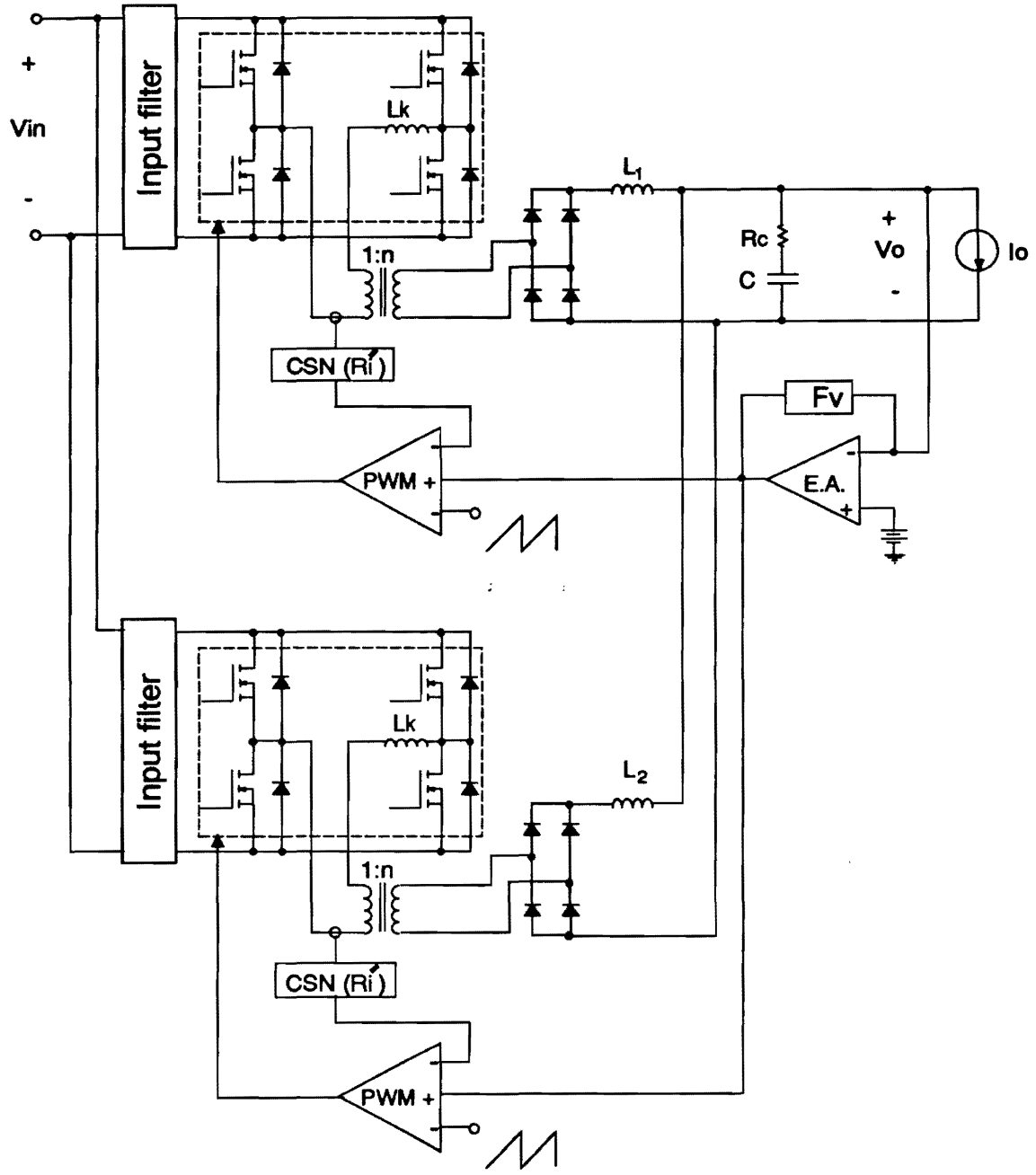


Fig. 4.15. Two-module ZVS-FB-PWM line conditioner: $V_{in} = 400\,V$, $V_O = 360\,V$, $I_O = 45\,A$, $R_i' = 0.048$, $n = 1.8$, $L_k = 4\,\mu H$, $L_1 = L_2 = 90\,\mu H$, $C = 10\,\mu F$, $R_C = 5\,m\Omega$.

Each module contains a power stage operating at 100 kHz and an input filter. The current sink at the output port emphasizes that the line conditioner is considered as an unterminated regulator.

Reduced-Order Modeling

Figure 4.16 shows the small-signal model of the unterminated line conditioner, obtained by replacing the power stage with its small-signal model [D9], and replacing the PWM and CSN blocks with their small-signal models [D7]. For control design purposes, the input of the line conditioner is considered as an ideal voltage source. The parameters for the power stage model and definitions of gain blocks are given in Table 4.1.

By taking the steps similar to those of Section 2.4.1, the small-signal model of Fig. 4.16 can be simplified to an equivalent single-module model of Fig. 4.17(a). Figure 4.17(b) is the time-domain counter part of Fig. 4.17(a). As discussed in Section 2.4.1, this model produces the same transient response as the original two-module system. The parameter for the equivalent single-module model are summarized in Table 4.2.

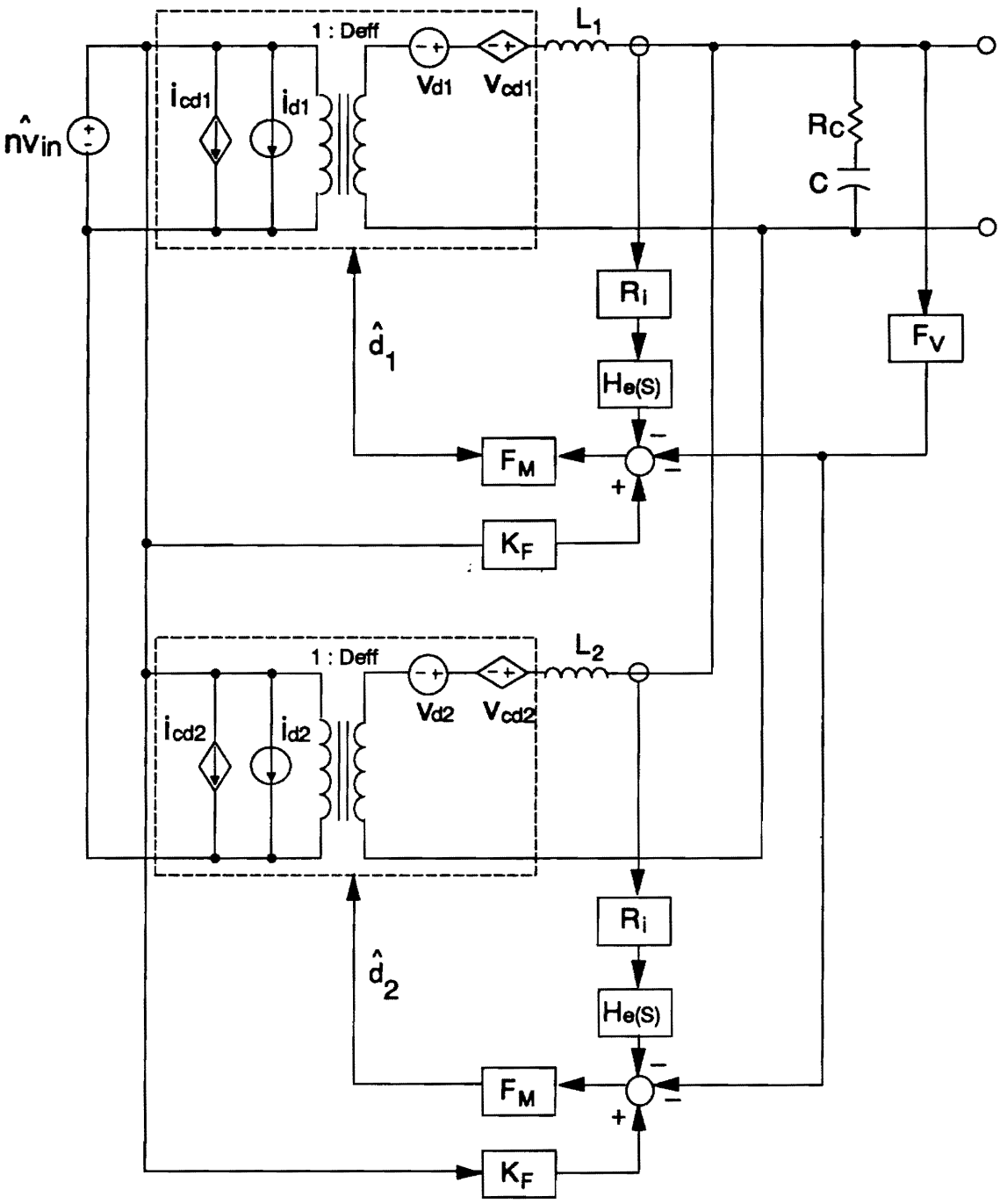


Fig. 4.16. Small-signal model of line conditioner: The model contains only dc information about load, and represents dynamics of the system unterminated in the small-signal sense.

Table 4.1: Summary of parameters in Fig. 4.16

Power stage	$D_{eff} = \dfrac{V_O}{nV_{in}}$ $i_{dk} = I_{Lk}\hat{d}_k \quad (k = 1,2)$ $i_{cdk} = I_{Lk}(\hat{d}_{ik} + \hat{d}_{vk})$ $v_{dk} = nV_{in}\hat{d}_k$ $v_{cdk} = nV_{in}(\hat{d}_{ik} + \hat{d}_{vk})$ $\hat{d}_{ik} = \dfrac{-2nL_k f_r}{V_{in}}\hat{i}_{Lk}$ $\hat{d}_{vk} = \dfrac{2nL_k f_r I_{Lk}}{V_{in}^2}\hat{v}_{in}$ f_r: ripple frequency
Modulator gain of PWM	$F_M = \dfrac{1}{(S_n + S_e)T_s}$ $T_s = \dfrac{1}{f_r}$ S_e: slope of external ramp S_n: on-time slope of sensed inductor current
Dc gain of CSN	R_i (constant)
Sampling gain of CSN	$H_e(s) = 1 + \dfrac{s}{\omega_n Q_n} + \dfrac{s^2}{\omega_n^2}$ $Q_n = -\dfrac{2}{\pi}, \qquad \omega_n = \dfrac{\pi}{T_s}$
Feedforward gain of CSN	$k_F = -\dfrac{D_{eff}T_s R_i}{L}\left(1 - \dfrac{D_{eff}}{2}\right)$

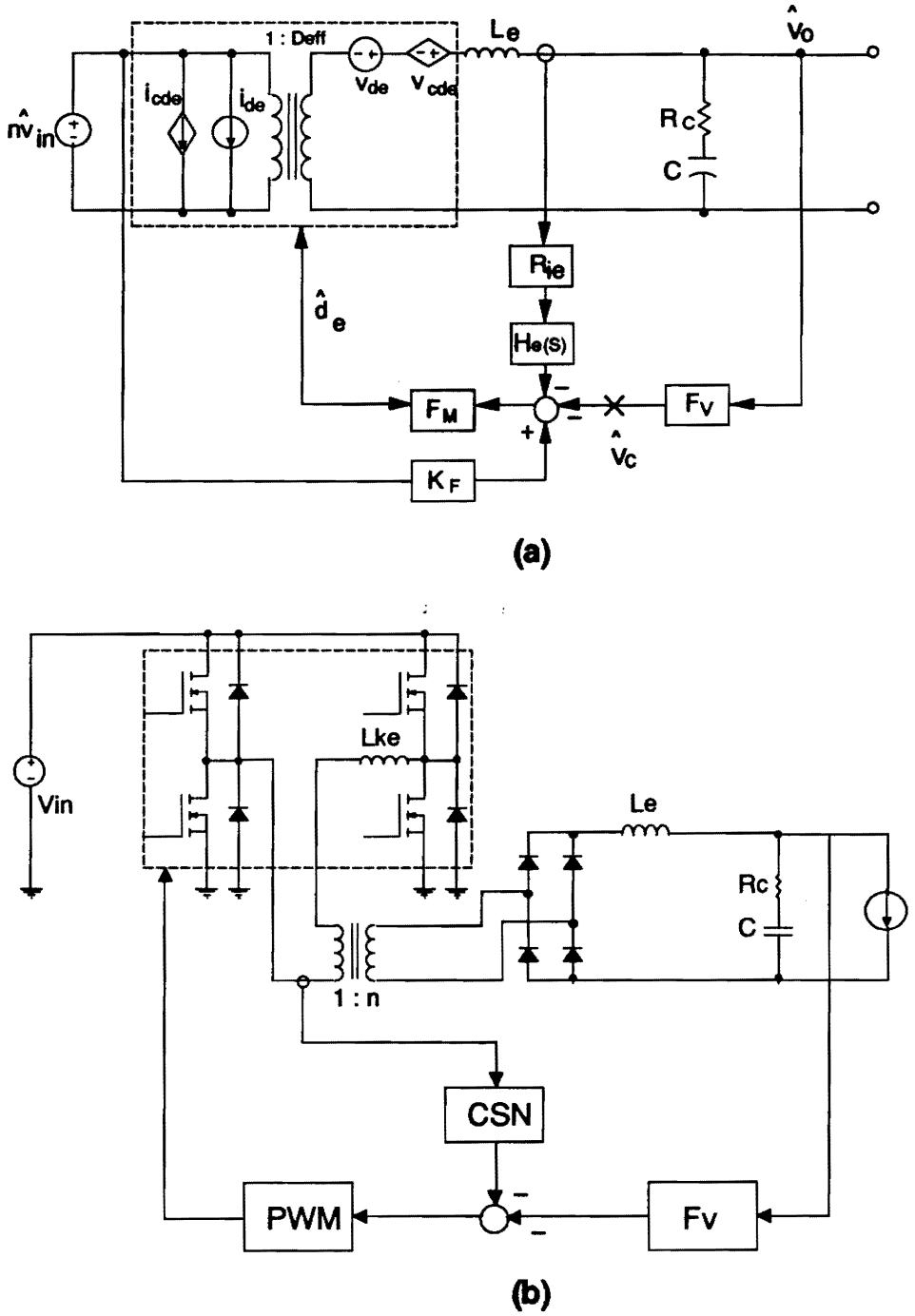


Fig. 4.17. Equivalent single-module model: (a) Frequency-domain model. (b) Time-domain model.

Table 4.2: Parameters of equivalent single-module model of Fig. 4.17

Leakage inductor	$L_{ke} = \frac{L_k}{2}$
Filter inductor	$L_e = \frac{L}{2}$
CSN gain	$R_{ie} = \frac{R_i}{2}$
Dc current of filter inductor	$I_{Le} = I_{L1} + I_{L2}$
Small-signal parameters	$\hat{d}_e = \hat{d}_1 = \hat{d}_2$ $i_{de} = I_{Le}\hat{d}_e$ $v_{de} = nV_{in}\hat{d}_e$ $i_{cde} = I_{Le}(\hat{d}_{ie} + \hat{d}_{ve})$ $v_{cde} = nV_{in}(\hat{d}_{ie} + \hat{d}_{ve})$ $\hat{d}_{ie} = \frac{-2nL_{ke}f_r}{V_{in}}\hat{i}_{Le}$ $\hat{d}_{ve} = \frac{2nL_{ke}f_rI_{Le}}{V_{in}^2}\hat{v}_{in}$

Voltage Compensation Design

Once the current loop is designed considering the large-signal constraints and the sampling effects of CSN [D7], the approximated control-to-output transfer function with current-loop closed can be derived from Fig. 4.17 (a):

$$G_{vc} = \frac{\hat{v}_O}{\hat{v}_c} = \frac{K_C(1 + sCR_c)}{(1 + s/\omega_{pL})(1 + s/\omega_H Q_H + s^2/\omega_H^2)}, \tag{4.20}$$

where

$$K_C = \frac{L_e f_r}{R_{ie}(m_C D_{eff}' - 0.5)}, \tag{4.21}$$

$$\omega_{pL} = \frac{m_C D_{eff}' - 0.5}{L_e C f_r}, \tag{4.22}$$

$$Q_H = \frac{1}{\pi(m_C D_{eff}' - 0.5)}, \tag{4.23}$$

$$\omega_H = \pi f_r, \tag{4.24}$$

with

$$D_{eff}' = 1 - D_{eff} \quad , \qquad m_c = 1 + \frac{S_e}{S_n}.$$

Using Eqs. (4.20) through (4.24), the voltage compensation can be designed to optimize the closed-loop performance of the unterminated line conditioner. For both stability and high performance, a two-pole one-zero compensation can be used:

$$F_V = \frac{K_V(1 + s/\omega_Z)}{s(1 + s/\omega_P)}. \tag{4.25}$$

For given power stage parameters, the voltage feedback compensation is designed as follows:

- ω_Z is placed at 46700 r/s to give settling time of 64 μSec in step load response;
- ω_P is placed at half the ripple frequency to minimize the detrimental effects of the sampling effects of CSN [D7]; and
- K_V is selected as 2600 r/s to minimize the output impedance, while maintaining a good phase margin of 53°.

Figure 4.18 shows the loop gain of the resulting design in comparison with the control-to-output transfer function with current-loop closed.

Compatibility with Stacked Load Converter Subsystem

As discussed in Section 4.2, the compatibility between the line conditioner and the stacked load converter subsystem can be assessed using impedances at the interface of two subsystems. Figure 4.19(b) compares the output impedance of the line conditioner with the input impedance of the stacked load converter subsystem. The condition $|Z_{OC}| \ll |Z_{IF}|$ guarantees the stability and compatibility of the integrated system.

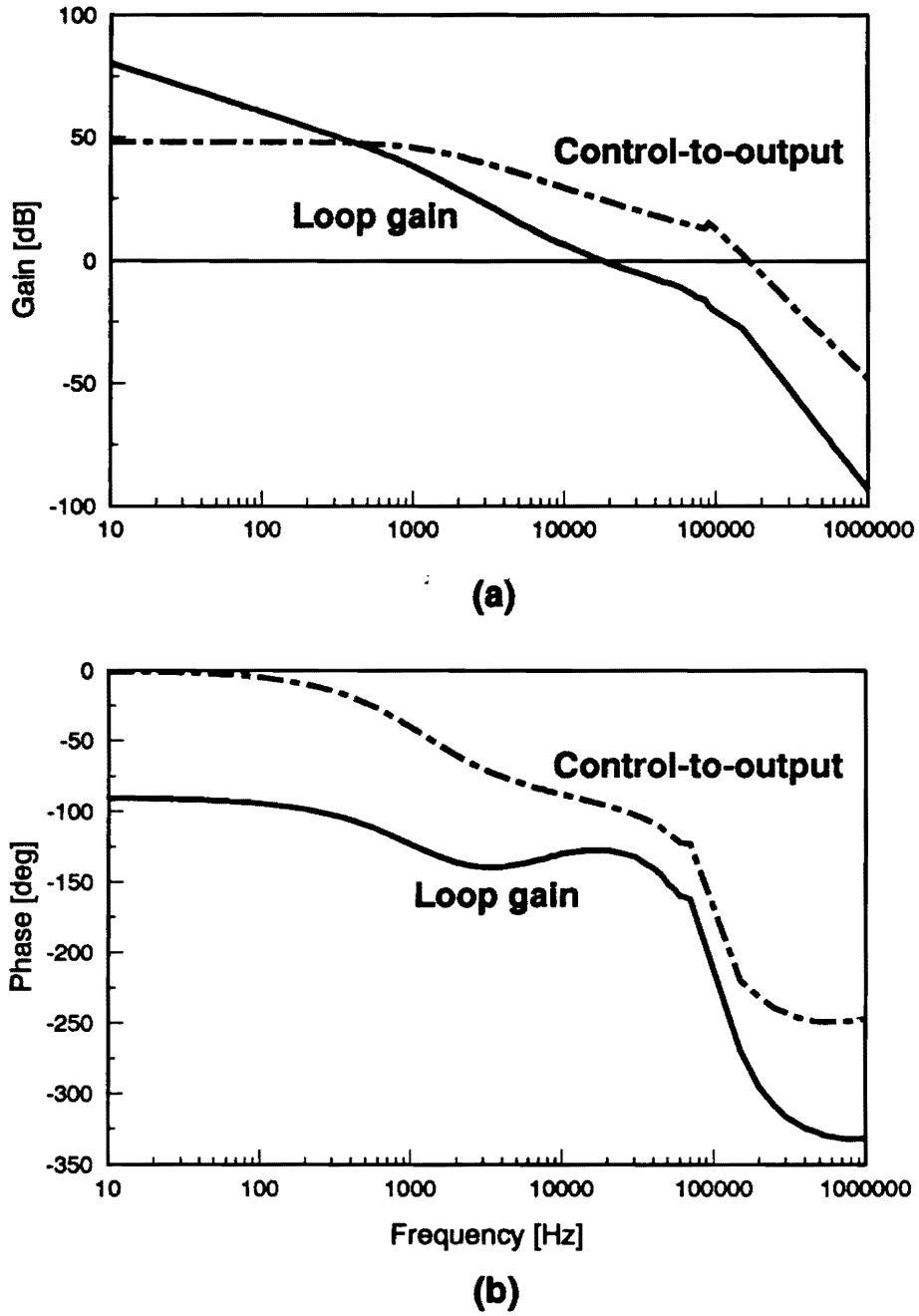


Fig. 4.18. Loop gain and control-to-output transfer function: (a) Gain. (b) Phase: The voltage feedback compensation is designed to offer a 53° phase margin of the loop gain.

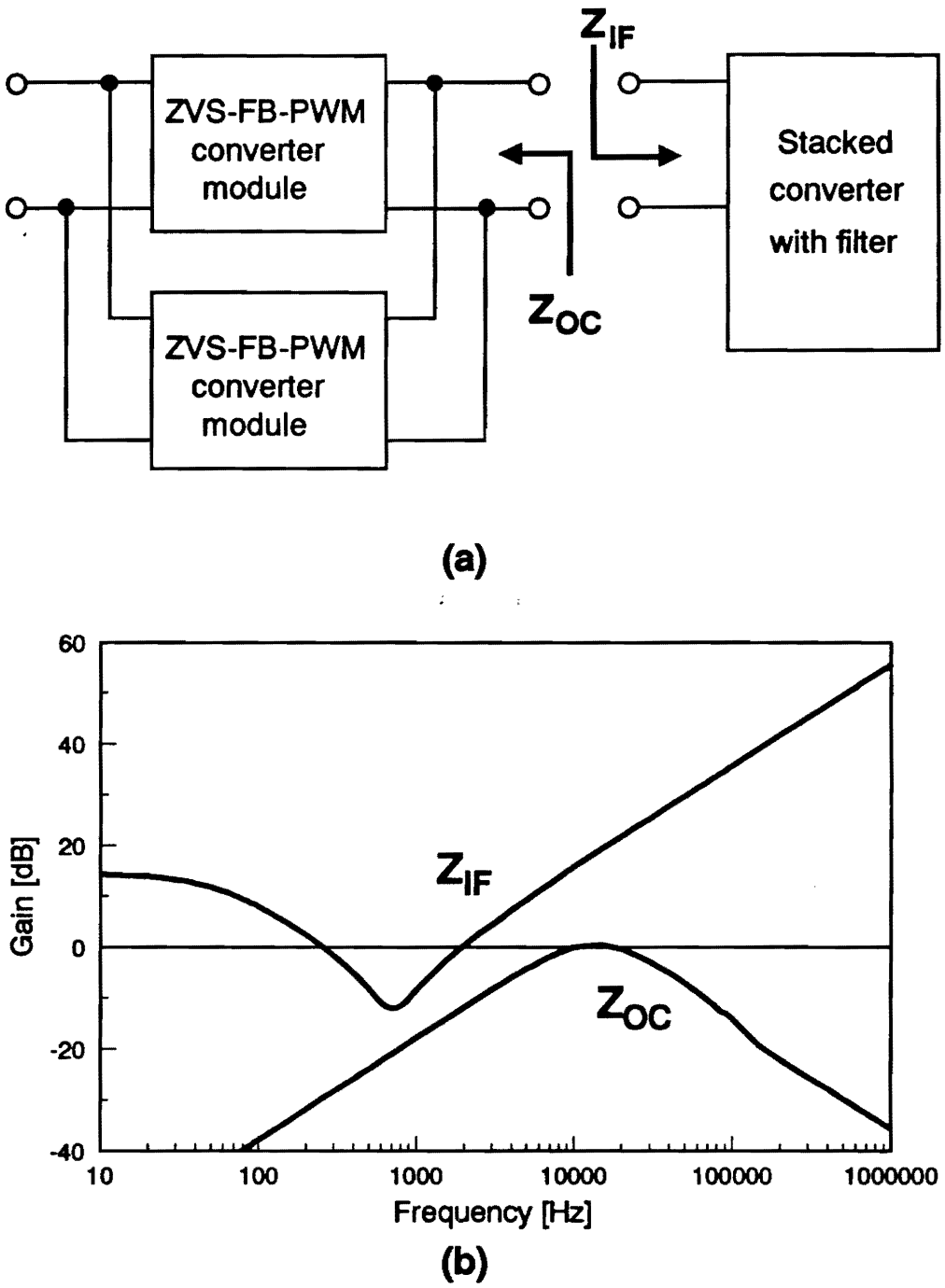


Fig. 4.19. Interaction analysis between line conditioner and stacked load converter subsystem: (a) Block diagram. (b) Impedance comparison: The condition $|Z_{OC}| \ll |Z_{IF}|$ guarantees the stability and compatibility of the integrated system.

4.5.2 Input Filter Design

Filter Specifications

Form the dc analysis, the peak value of the input current of each ZVS-FB-PWM module is determined to be 43 Amps. To achieve 2.1 Amps ripple at the output of ac-to-dc preregulator, a current attenuation of 26 dB at 200 kHz is required. The single-stage filter discussed in Section 4.4.2 is found to be sufficient to provide the necessary current attenuation. Figure 4.20 (a) shows the overall configuration of the single-stage distributed filter.

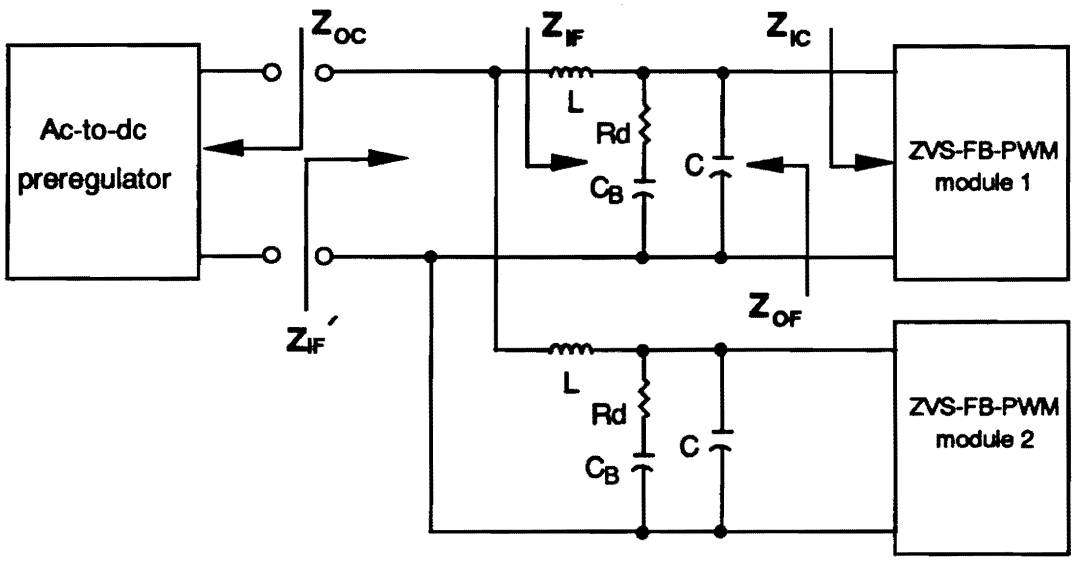
The minimum value of the input impedance of each ZVS-FB-PWM module can be found as 26 dB from following equation:

$$|Z_{IC}|_{\min} \approx |Z_{IC}|_{DC} = \frac{2V_O}{n^2 D_{eff}^2 I_O} = 26\,dB \tag{4.26}$$

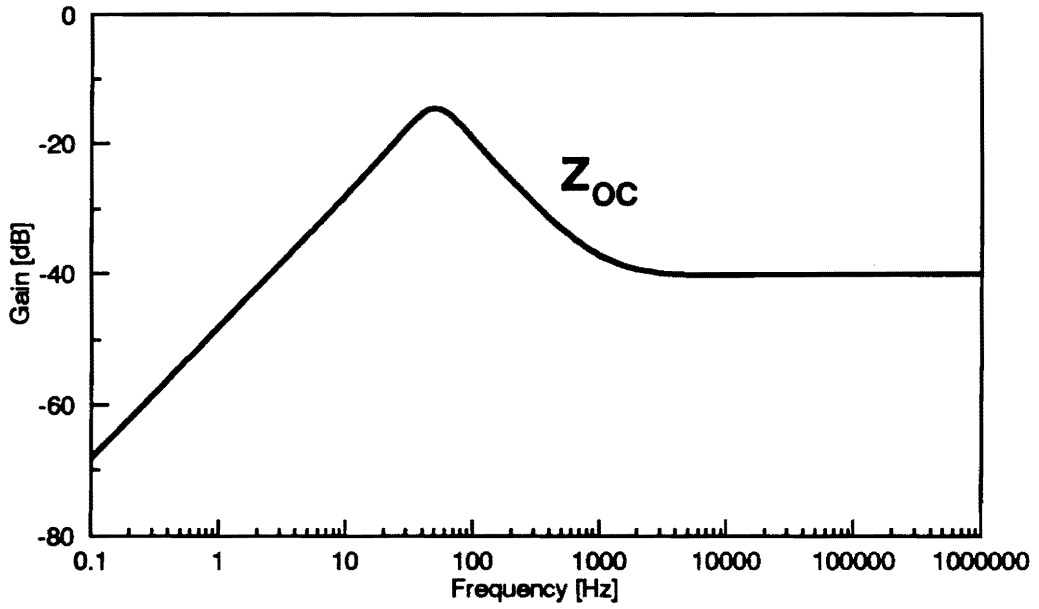
Figure 4.20(b) shows the output impedance of the ac-to-dc preregulator [D11], whose high-frequency value is - 40 dB. From Fig. 4.20(b) and Eq. (4.26), it can be concluded that the filter having

$$|Z_{IF}|_{\min} \approx |Z_{OF}|_{\max} \approx \frac{|Z_{IC}|_{\min} + |Z_{OC}|_{\max} + 6\,dB}{2} = -4\,dB \tag{4.27}$$

offers a 30 dB gap between $|Z_{OF}|$ and $|Z_{IC}|$, and also provides a 30 dB gap between $|Z_{OC}|$ and $|Z_{IF}'|$.



(a)



(b)

Fig. 4.20. Single-stage distributed input filter: (a) Overall configuration. (b) Output impedance of ac-to-dc preregulator.

Design Results

Using the design procedures established in Section 4.4.2, the filter parameters are determined as follows

$$L = 2.85\,\mu H, \qquad C = 4.6\,\mu F, \qquad R_d = 0.63\,\Omega, \qquad C_B = 46\,\mu F.$$

Figure 4.21 shows the transfer functions of the resulting single-stage distributed filter. The filter satisfies all design specifications including the current attenuation and the desired impedance gap at both sides of the filter.

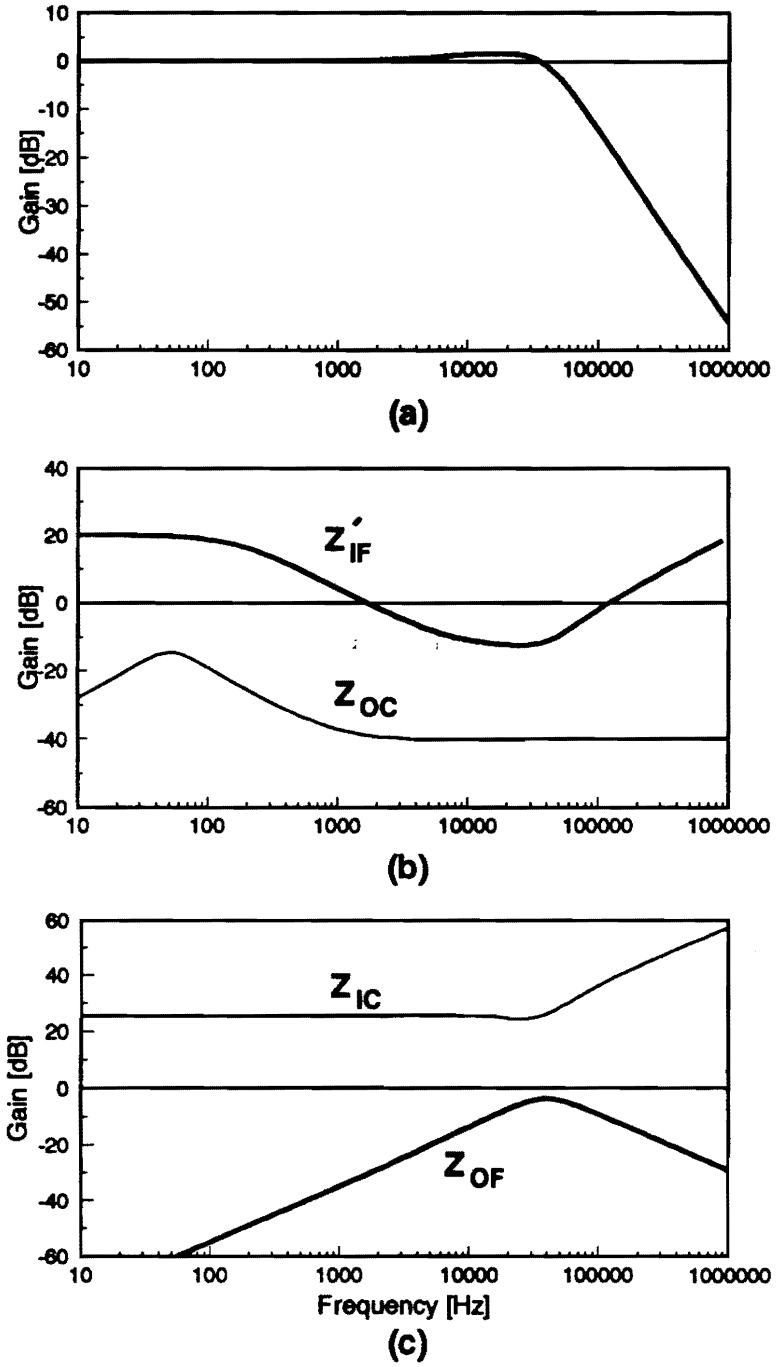


Fig. 4.21. Transfer functions of single-stage distributed filter: (a) Current attenuation. (b) Input impedance. (c) Output impedance.

4.6 SUMMARY

This chapter established two useful design techniques for multi-stage distributed power systems: 1) unterminated modeling and design method of converter stages, and 2) design guidelines for intermediate filters. The use of these techniques was fully demonstrated in Section 4.5, which covered the design of a two-module ZVS-FB-PWM line conditioner.

The primary concern in designing converters for distributed power applications is the complexity or the uncertainty of the load dynamics. To resolve this problem, the unterminated modeling and design method is developed. This approach initially considers the converter as an unterminated stand-alone regulator and does not need any prior information about the dynamic characteristics of the load subsystem. For the given dc power level and output voltage, the control is designed to optimize the dynamic performance of the unterminated converter, and at the same time, to minimize undesirable interactions with the load subsystem.

Once the control design is optimized, the compatibility with the load subsystem can be investigated using the output impedance of the converter and the input impedance of the load subsystem. If the input impedance of the load subsystem is lager than the output impedance of the converter for all frequencies, the entire system is stable as long as subsystems are individually stable. Otherwise, Nyquist analysis is necessary to evaluate the system stability.

Intermediate filters employed between the line conditioner and the load converter must avoid interactions with the converters at both sides of the filter. This requirement implies following two conditions:

- a sufficient gap between the output impedance of the line conditioner (Z_{OC}) and the input impedance of the filter, and
- a sufficient gap between the output impedance the filter and the input impedance of the load converter (Z_{IC}).

This chapter presented design guidelines for both single-stage and two-stage filters, which offer an impedance gap of

$$|Z|_{gap} = \frac{|Z_{IC}|_{\min} - |Z_{OC}|_{\max}}{2k} \quad (1 \le k)$$

at both sides of the filter, while providing the desired current attenuation. If $|Z_{IC}|_{\min}$ is at least 20 dB larger than $|Z_{OC}|_{\max}$ (which is true for most practical applications), k can be selected as 1 to realize a 10 dB impedance gap at both sides. This would prevent any major interactions with both the line conditioner and the load converter.

CHAPTER 5

CONCLUSIONS

Comprehensive modeling, analysis, and design techniques have been developed for large-scale distributed power systems. Dynamic interactions caused by paralleling, stacking, and cascading converter modules are fully characterized and properly incorporated into the control design in order to optimize dynamics of the entire system. The results of this dissertation, coupled with the existing techniques, would constitute extensive analytic archives which can be used to optimize the dynamic performance of a wide class of distributed power systems.

A circuit oriented procedure to obtain a reduced-order model for multi-module converters is developed. As demonstrated in Chapter 2, the reduced-order model preserves both frequency- and time-domain performance of the original multi-module converter. The derivation steps automatically incorporate all interactions among parallel modules; the steps are general enough to be directly extended to a large class of multi-module converters. The resulting reduced-order model has the structure of a conventional single-module converter, while preserving the dynamics of the original system. Using this model, any control scheme developed for a single-module converter can be directly adapted to a multi-module system. Furthermore, multi-module converters operating as subsystems of a large-scale power system can be replaced with reduced-order models without compromising any analysis accuracy.

It is shown that the secondary LC filter, widely used in multi-module converters for low-voltage applications, could degrade the system performance when the conventional

two-loop current-mode control is used. The detrimental effects of the secondary LC filter are most pronounced in the transient response in the event of failure of a converter module, which is a critical performance criterion for multi-module redundant systems.

To overcome the limitations of two-loop control, a three-loop control scheme is proposed for multi-module converters with a secondary LC filter. Using an additional feedback from the output capacitor of each module, the three-loop control minimizes the detrimental effect of the secondary LC filter, and offers several advantages over the conventional two-loop current-mode control, including a significant improvement in the module-failure response.

Guidelines to selecting the three-loop feedback compensation are presented. The structure of and the design procedures for three-loop compensation are no more complicated than those of a two-loop control. The superiority of the three-loop control over the two-loop control is verified by both the frequency- and time-domain simulations.

Systematic design procedures are established for power supplies employing a stacked configuration of converters for low voltage and high current applications in mainframe computer power system. The converter in the stacked power supply has dc load determined by its dc operating point, but it also has ac load determined by the load impedance seen by the output of the converter. These two load parameters are entirely different and play two distinctive roles in designing the converter. The dc load governs the input filter design, and the ac load governs the control design.

Interactions between stacked converters are reduced to a simple loading effect, by identifying the ac load of each converter as a combination of load resistors and output impedances of the other converters. An equivalent resistive load of each converter is

obtained from its ac load by replacing the output impedance of the other converters with the ESR of their output filter capacitor. Using the equivalent resistive load, the control loop of each converter is designed as for a single conventional converter. This design procedure naturally incorporates all subsystem interactions, and optimizes the system performance using standard design techniques.

As discussed in Chapter 4, in a distributed power system, the primary concern in designing a converter driving other converters through an intermediate filter is the complexity or uncertainty of its load dynamics. To deal with this problem, an ac unterminated modeling and design method is proposed for the cascaded converter stages. In this approach, the converter is considered as an ac unterminated stand-alone regulator without considering the load dynamics. For given dc power level and output voltage, the control is designed to optimize the dynamic performance of the unterminated converter stage. It is particularly important to minimize the output impedance of the unterminated converter, in order to ensure the stability after integration and minimal interactions with the load subsystem.

Once the control design is optimized for the unterminated converter stage, the stability and compatibility of the integrated system can be analyzed using the impedances at the interface of two subsystems. A system loop gain is defined to which Nyquist criterion can be applied to assess stability and compatibility of the integrated system.

Design considerations for intermediate filters employed between two cascaded converters are addressed. A design strategy to minimize undesirable interactions at both sides of the filter is presented. The design strategy is substantiated by detailed design procedures for both single-stage and two-stage filters.

The results of this dissertation can be used in various ways to assist the design of distributed power systems. While the results of Chapter 2 can be individually used to design multi-module converters, they can be combined with the results of Chapter 3 to design power supplies employing a stacked configuration of multi-module converters. Similarly, the results of Chapters 2 and 4 can be collectively used to design a multi-stage distributed power system using multi-module converters. Finally, the results of Chapters 2, 3, and 4 can be integrated to optimize the dynamic performance of complex power systems, employing a combination of paralleling, stacking, and cascading converter modules.

REFERENCES

MULTI-MODULE CONVERTER SYSTEMS

[A1] P. Koetsch, "Connecting power supplies in parallel," Machine Design, September 10, 1981.

[A2] J. Reed, and N. Sharma, "Large parallel UPS system utilizing PWM technology," IEEE Power Electronics Specialists' Conference, 1984 Record, pp. 282-289.

[A3] T. Kawabata, and S. Higashino, "Parallel operation of voltage source inverters," IEEE Transactions on Industry Applications, Vol. 24, No. 2, Mar./Apr. 1988, pp.281-287.

[A4] D.M. Sable, and R.B. Ridley, "A high-frequency multi-module, Spacecraft boost regulator", VPEC Power Electronics Seminar, 1988 Record, pp. 178-186.

[A5] D.M. Sable, S. Deuty, F.C. Lee, and B.H. Cho, "Experimental verification of space platform battery discharger design optimization," Intersociety Energy Conversion Engineering Conference, 1991 Record.

[A6] C.E. Mullett, "A user's guide to applying power-conversion modules," Electronic Design, January 1991, pp.75-81.

[A7] F. Petruzziello, P.D. Ziogas, and G. Joos, "A novel approach to paralleling of power converter units with true redundancy," IEEE Power Electronics Specialists' Conference, 1990 Record, pp. 808-813.

[A8] K. Siri, and C.Q. Lee, "Current distribution control of converters connected in parallel," IEEE IAS Annual Meeting, 1990 Record, pp. 1274-1280.

[A9] C.Q. Lee, K. Siri, and T.F. Wu, "Dynamic current distribution controls of a parallel connected converter system," IEEE Power Electronics Specialists' Conference, 1991 Record, pp. 875-881.

[A10] T.F. Wu, K. Siri, C.Q. Lee, and J.R. Burns, "A fault-tolerant parallel connected power system," Intersociety Energy Conversion Engineering Conference, 1991 Record.

[A11] R.B. Ridley, "Small-signal analysis of parallel power converters," Master's Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, March 1986.

[A12] R.B. Ridley, "Analysis and design of paralleled power converter modules," VPEC Power Electronics Seminar, 1986 Record, pp. 160-168.

[A13] B. Choi, B.H. Cho, R.B. Ridley, and F.C. Lee, "Control strategy for multi-module parallel converter systems," IEEE Power Electronics Specialists' Conference, 1990 Record, pp 225-234.

DISTRIBUTED POWER SYSTEMS

[B1] B. Carsten, "VLSI and VHSIC power system design considerations," Power Conversion International Conference, 1986 Record, pp.1-15.

[B2] W.T. Rutledge, "Distributed power 'time for a second look'," International Telecommunications Energy Conference, 1986 Record, pp.369-375.

[B3] B. Carsten, "Distributed power systems of the future utilizing high frequency converters," High Frequency Power Conversion Conference, 1987 Record, pp. 1-14.

[B4] C.C. Heath, "The market for distributed power systems," IEEE Applied Power Electronics Conference, 1991 Record, pp. 225-229.

[B5] L. Thorsell, "Will distributed on-board dc/dc converters become economically beneficial in telecom switching equipment?," International Telecommunications Energy Conference, 1990 Record, pp. 63-69.

[B6] B. Carpenter, R. Lewis, B. Choi, B.H. Cho, F.C. Lee, "A distributed power system for military VLSI applications," High Frequency Power Conversion Conference, 1988 Record, pp.430-441.

[B7] M.M. Walters, and W.M. Polivka, "A high-density power processor for distributed military power systems," IEEE Applied Power Electronics Conference, 1989 Record, pp. 403-412.

[B8] C.S. Leu, M. Tullis, L. Keller, F.C. Lee, "A high frequency ac bus distributed power system," VPEC Power Electronics Seminar, 1990 Record pp. 98-107.

[B9] C.E. Mullett, "Practical design of small distributed power systems," Power Conversion and Intelligent Motion, Jan. 1991, pp. 21-27.

[B10] W.A. Tabisz, M.M. Jovanovic, and F.C. Lee, "Benefits and challenges of distributed power systems," Government Microcircuit Applications Conference, 1991 Record, pp.71-74.

[B11] B. Choi, R. Lewis, B.H. Cho, and F.C. Lee, "Distributed power system analysis," Final Report of Phase I for IBM-Manassas, VPI&SU, Jan. 1988.

[B12] L.R. Lewis, B.H. Cho, F.C. Lee, and B.A. Carpenter, "Modeling, analysis and design of distributed power systems," IEEE Power Electronic Specialists' Conference, 1989 Record, pp. 152-159.

[B13] S. Schulz, J. Liu, B.H. Cho, F.C. Lee, "Large-signal modeling and simulation of distributed power systems," VPEC Power Electronics Seminar, 1989 Record, pp. 139-144.

[B14] S. Schulz, B.H. Cho, and F.C. Lee, "Integrating a series of high-density converters," Powertechnics Magazine, January 1990, pp. 32-37.

[B15] L.R. Lewis, "Small-signal analysis and design of a distributed power system," Master's Thesis, Virginia Polytechnic Institute and State University, February 1990.

[B16] G.A. Franz, G.W. Ludwig, and R.L. Steigerwald, "Modeling and simulation of distributed power systems," IEEE Power Electronics Specialists' Conference, 1990 Record, pp. 606-610.

[B17] S. Schulz, B.H. Cho, and F.C. Lee, "Design considerations for a distributed power system," IEEE Power Electronic Specialists' Conference, 1990 Record, pp. 611-617.

[B18] S. Schulz, "System interactions and design considerations for distributed power systems," Master's Thesis, Virginia Polytechnic Institute and State University, January 1991.

[B19] B.H. Cho, and B. Choi, "Analysis and design of multi-stage distributed power systems," International Telecommunications Energy Conference, 1991 Record, pp.220-226.

[B20] W.A. Tabizs, M.M. Jovanovic, and F.C. Lee, "Present and future of distributed power systems," IEEE Applied Power Electronics Conference, 1992 Record, pp.11-18.

[B21] B.H. Cho, and R.B. Ridley, "Distributed power systems," High Frequency Power Conversion Conference, 1992 Record.

[B22] B. Choi, E.X. Yang, C. Wildrick, B.H. Cho, and F.C. Lee, "Dynamics and control of multi-module series/parallel resonant preregulator for distributed power applications," VPEC Power Electronics Seminar, 1992 Record.

COMPUTER POWER SYSTEMS

[C1] H.N. Chandra, V.J. Thouttuvelil, "Modeling and analysis of computer power systems," IEEE Power Electronics Specialists' Conference, 1989 Record, pp.144-151.

[C2] B. Choi, B.H. Cho, R.B. Ridley, and F.C. Lee, "Analysis and design of stacked power system," VPEC Power Electronic Seminar, 1990 Record, pp. 118-126.

[C3] C.D. Smith, "Distributed power systems via ASICs using SMT," Surface Mount Technology, Oct. 1990, pp. 29-32.

[C4] B. Choi, B.H. Cho, R.B. Ridley, and F.C. Lee, "The stacked power system: A new power conditioning architecture for mainframe computer systems," IEEE Power Electronics Specialists' Conference, 1991 Record, pp. 867-874.

POWER CONVERTER MODELING

[D1] F.C Lee, Y. Yu, and M.F. Mahmoud, "A unified analysis and design procedure for a standardized control module for dc-dc switching regulators," IEEE Power Electronic Specialists' Conference, 1979 Record, pp.284-301.

[D2] R.B. Ridley, B.H. Cho, and F.C. Lee, "Analysis and interpretation of loop gains of multi-loop-controlled switching regulator," IEEE Transactions on Power Electronics, Vol. 3, No. 4, pp. 489-498, October 1988.

[D3] V. Vorperian, R. Tymerski, and F.C. Lee, "Equivalent circuit model for resonant and PWM switches," IEEE Transactions on Power Electronics, Vol. 4, No. 2, pp. 205-214, April 1989.

[D4] V. Vorperian, "Simplified analysis of PWM converters using the model of PWM switch: Part I and II," IEEE Transactions on Aerospace and Electronic Systems, Vol.26, No.3, pp.490-505, May 1990.

[D5] S.R. Sanders, J.M. Noworolski, X.Z. Liu, and G.C. Verghese, "Generalized averaging method for power conversion circuits," IEEE Power Electronics Specialists' Conference, 1990 Record, pp. 333-340.

[D6] C.T. Rim, D.Y. Hu, and G.H. Cho, "Transformers as equivalent circuits for switches: general proofs and D-Q transformation-based analysis," IEEE Transactions on Industry Applications, Vol.26, No.4, July/August 1990.

[D7] R.B. Ridley, "A new, continuous-time model for current-mode control," IEEE Transactions on Power Electronics, Vol. 6, No. 2, pp.271-280, April 1991.

[D8] R.B. Ridley, "A new, small-signal model for current-mode control," Ph.D. dissertation, Virginia Polytechnic Institute and State University, Blacksburg, Nov. 1990.

[D9] V. Vlatkovic, J.A. Sabate, R.B. Ridley, F.C. Lee, and B.H. Cho, "Small-signal analysis of the phase-shifted PWM converter," IEEE Transactions on Power Electronics, Vol.7, No. 1, pp.128-135, January 1992.

[D10] K.D.T. Ngo, "Topology and analysis in PWM inversion, rectification, and cycloconversion," Ph.D. dissertation, California Institute of Technology, Pasadena, May 1984.

[D11] S. Hiti, D. Borojevic, F.C. Lee, B. Choi, and S. Lee, "Small-signal modeling of three-phase PWM buck rectifier with input filter," VPEC Power Electronics Serminar, 1991 Record, pp.229-237.

INPUT FILTER DESIGN

[E1] R.D. Middlebrook, "Input filter considerations in design and application of switching regulators," IEEE Industry Applications Society Annual Meeting, 1976 Record, pp. 366-382.

[E2] R.D. Middlebrook, "Design techniques for preventing input filter oscillations in switched-mode regulators," National Solid-State Power Conversion Conference, 1978 Record, pp.A3-A16.

[E3] R.D. Middlebrook, "Power filter damping," Power Electronics Design Conference, 1985 Record.

[E4] T.K. Phelps, and W.S. Tate, "Optimizing passive input filter design," National Solid-State Power Conversion Conference, 1979 Record, pp.G1.1-G1.10.

[E5] R.B. Ridley, "Secondary LC filter analysis and design techniques for current-mode-controlled converters," IEEE Transactions on Power Electronics, Vol. 3, No. 4, pp.499-507, October 1988.

[E6] H.D. Venable, "Minimizing input filter requirements in military power supply design," Power Conversion and Intelligent Motion, May 1987, pp.26-38.

[E7] S.Y. Erich, and W.M. Polivka, "Input filter design criteria for current-programmed regulators," IEEE Transactions on Power Electronics, Vol. 7, No. 1, pp.143-151, January 1992.

GENERAL

[F1] B.H. Cho, "Modeling and Analysis of spacecraft power systems," Ph.D Dissertation, Virginia Polytechnic Institute and State University, October 1985.

[F2] C.T. Chen, "Liner system theory and design," CBS College Publishing, 1984.

[F3] G.F. Franklin, J.D. Powell, and A. Emami-Naeini, "Feedback control of dynamic systems," Addison Wesley, 1986.

[F4] J.G. Kassakian, M.F. Schlecht, and G.C. Verghese, "Principles of power electronics," Addison Wesley, 1991.

Vita

Byungcho Choi was born in Korea in 1957. He received a B.S. degree in electronic engineering from Hanyang University, Seoul, Korea, in 1980. From 1980 to 1985, he was employed as a research engineer in the Agency for Defense Development, Korea, where he was involved in the development of switchmode power supplies for pulsed laser applications.

He began studying at Virginia Polytechnic Institute and State University in 1985 and received an M.S. degree in electrical engineering in 1988, concentrating on the time-domain analysis of switchmode power converters. Since 1988, he has been a Graduate Project Assistant at Virginia Power Electronics Center. He is actively involved in the research on modeling, analysis, and design of large-scale switchmode power conversion systems such as computer power systems, distributed power systems, space power systems, and multi-module converter systems.