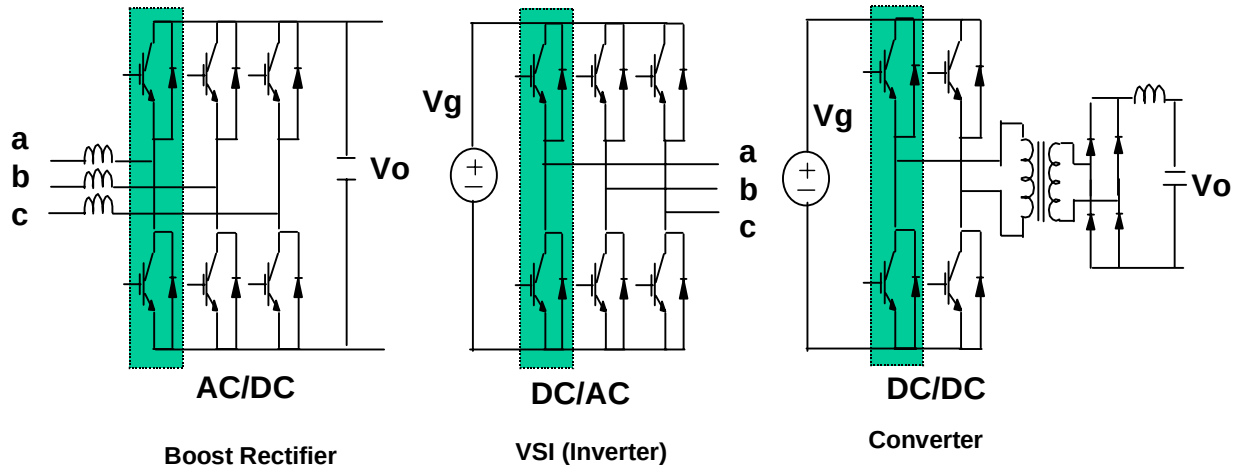
2. Power Electronics Building Blocks

2.1 Definition of PEBB

PEBB research starts with the identification of PEBB structure. There are several desired features for PEBB application. The essential feature is its commonality. Even though it is impossible to find one or more switching topologies that can cover all applications, it is feasible that they should cover most applications. Figure 2.1 shows some of the common switching topologies which can be used in ac/dc, dc/dc, and dc/ac conversion. Figure 2.1(a) is the most widely used half bridge leg structure, which consists of two active switches in a totem pole arrangement and two diodes in anti-parallel with them. It can be used in voltage source converters. In this type of structure, the voltage is unidirectional and the current is bi-directional. Figure 2.1(b) shows a common structure for current source converters. Example systems include an ac/dc rectifier and a dc/ac inverter. In this case the voltage can be applied bi-directionally, and the current flows only in one direction [A5-6]. The discussion in this chapter will concentrate on the voltage source switching leg in Figure 2.1(a).

2.1.1 The Selection of Power Semiconductor Devices

The selection of the power semiconductor device for PEBB application depends on power ratings. The performance of the power semiconductor devices can be characterized by the current carrying capability, voltage blocking capability, dv/dt, di/dt, and gating requirements. Depending on the device's physical structure, the trade-offs already have been exhibited by the existing switches. To date, MOSFETs typically are used for low power high frequency applications. The IGBT is gaining widespread favor for power systems up to 1000KVA, with devices now available up to 2,3 kV and 1,200A. It is now the workhorse of the power electronics industry. GTOs commonly are used for switches above that power level. Although MCTs do have a good forward voltage drop, they are presently not superior in switching as are IGBT [A3]. Other emerging power devices include IGCT, MTO, ETO [A10], which have shown or are showing their competitiveness in high power applications.



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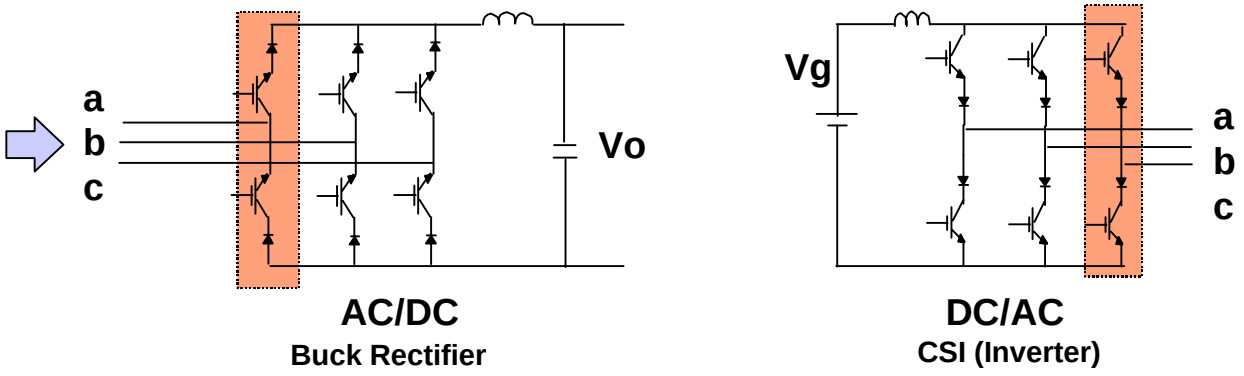


(b)

Figure 2.1 Common switching structures for PEBB

2.1.2 Considerations of Gate Driver and Standard Interface

The second desired feature of the PEBB switching cell is the integrated intelligence. This is an issue of where to partition the system so that each part can contain a certain level of intelligence and the integration can be done separately [A4]. The answer to this question is not definite. But at this stage, it is feasible to integrate the driver circuit associated with each IGBT and the relevant protection and diagnosis functions into one package. A driver circuit generally performs (1) power amplification and level shift; (2) isolation; (3) protection such as short circuit detection, under voltage lockout, and dead time control; and (4) diagnostics functions to provide status information to supervisory control. Other desired features on the driver circuit include (1) a single power supply for both low and high side devices, (2) a transformerless isolation for easy monolithic integration, and (3) a high slew rate and low impedance of gating signal. Although sensors inside the PEBB switching cell would be a good feature, problems may arise such as size, integration, and disruption of the circuit. Given the above hardware structure and functionality, the interface for the phase leg module would include at least the power supply input for the gating power, on and off control signals for the top and bottom active switches, and a fault diagnosis output signal. In order to provide isolated floating power supply, the integration of an on-board power converter for each IGBT is one of the key problems when there is only one power input at the interface. The boost-strap on-board power supply [A10] is a good concept for monolithic integration because no magnetics is needed. However, because of the increased component count and circuit complexity, it may be a good solution for low power applications. The second choice of providing the gating power is to use an isolated dc/dc converter locally for each IGBT. This method has been proved feasible in hardware development. The drawback is that it is relatively expensive to use commercial dc/dc converters. The third choice is to use the square-wave ac distribution bus as the input of the gate power supply. Each IGBT driver will transform the ac voltage into dc using an isolated transformer and diode rectifier. This method needs to develop a square-wave ac source outside the package, and the high degree of integration is somehow loose. There are several ways to provide isolation of logic level signals. One is to use the optical coupler, which requires a strict specification of common-mode noise attenuation. The other is to use optic fiber for gate and fault signal transmission, which is relatively expensive.

Figure 2.2 illustrates the circuit diagram of the auxiliary charge-pump driver circuit for the high side IGBT. The bottom IGBT uses the dc voltage Vs directly for its own driver IC, which is not shown in the circuit for clarity. The high side driver chip uses the voltage on capacitor C1 as its power supply. There are two charge pumps in the circuit. The first one is composed of d1, d2, C1, and Sn. When the bottom switching Sn is on, the capacitor C1 will be charged to around Vs through d1 and d2. The second charge pump is composed of d1, d2, C1, C2, San, and Sap. The square waveform generator generates complementary square waveforms for San and Sap. When San is on, capacitor C2 is charged approximately to Vs through d1 and San. When Sap is on, the pre-charged C2 will charge C1 through d2 and Sap. The driver chip for Sap is powered by the voltage on C2. The second auxiliary charge pump ensures the operation of the high side IGBT even without operation of the first charge-pump. There is no magnetic transformer involved for isolation. d1, d2, Sap, and San are high voltage semiconductor devices. This circuit has been tested in 400 V dc bus applications.

Even though much research work is in the packaging area to achieve highly compact PEBB modules, the current power electronic system still can be constructed using commercial IGBT modules or discrete devices. A conceptual PEBB module is shown in Figure 2.2(a), where discrete IGBT devices are used to build the phase leg structure. The driver circuit implements the charge-pump power supply concept with an optical coupler interface. Figure 2.2(b) is the structure diagram of this module. For high power applications, the half-bridge phase leg modules are used.

2.1.3 PEBB Module Switching Characteristics

The PEBB module can be treated as a multi-terminal device. Its switching characteristics will determine the performance of the integrated system as the IC chips in the digital circuit. In order to study the switching behavior of the integrated PEBB module, the module was modeled and experimented based on its design and layout.

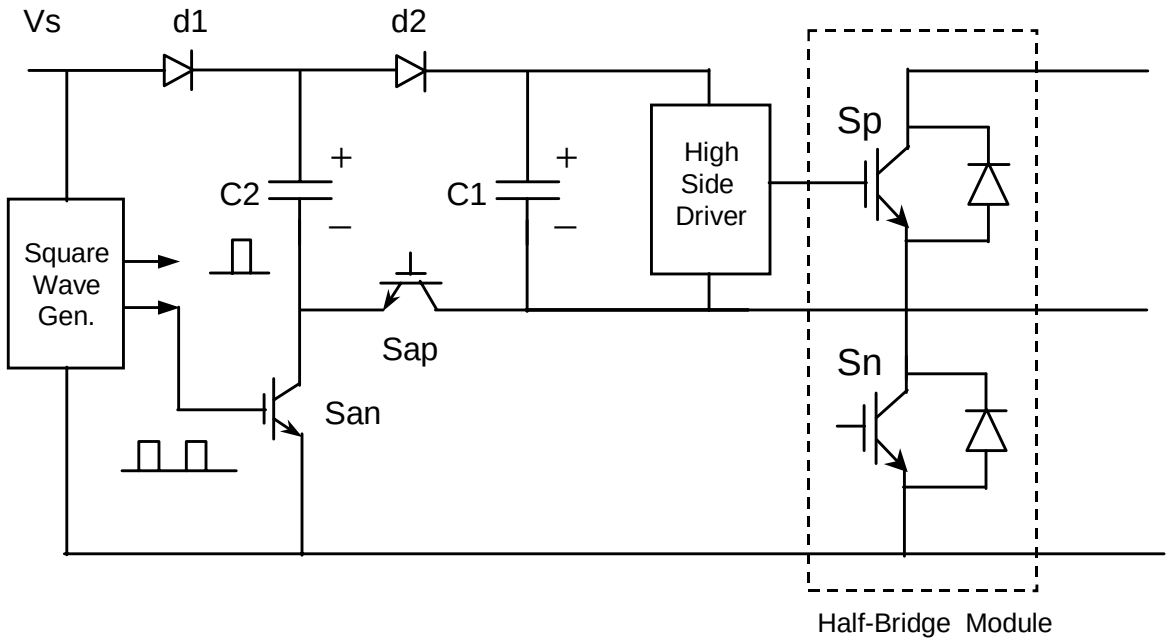
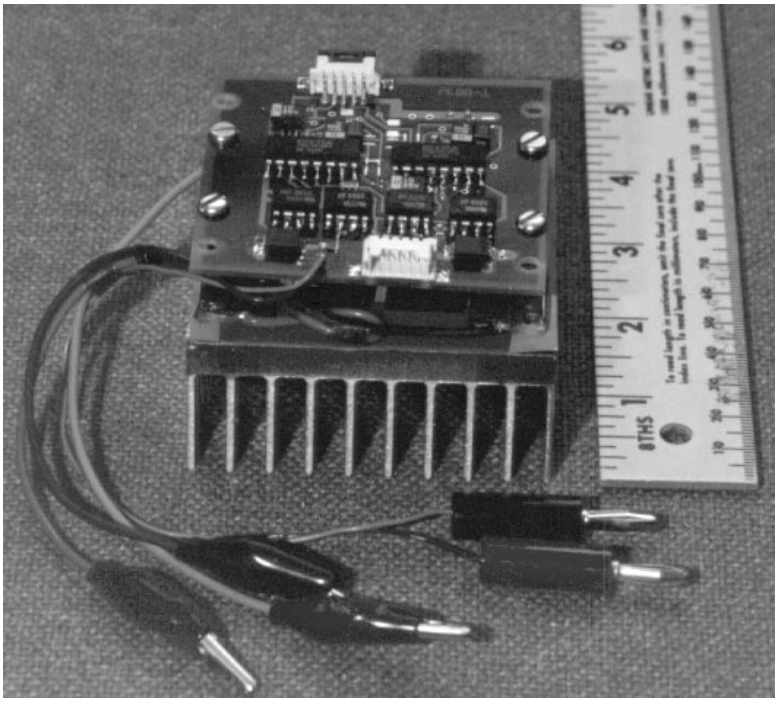


Figure 2.2 The circuit diagram for the auxiliary charge-pump driver circuit



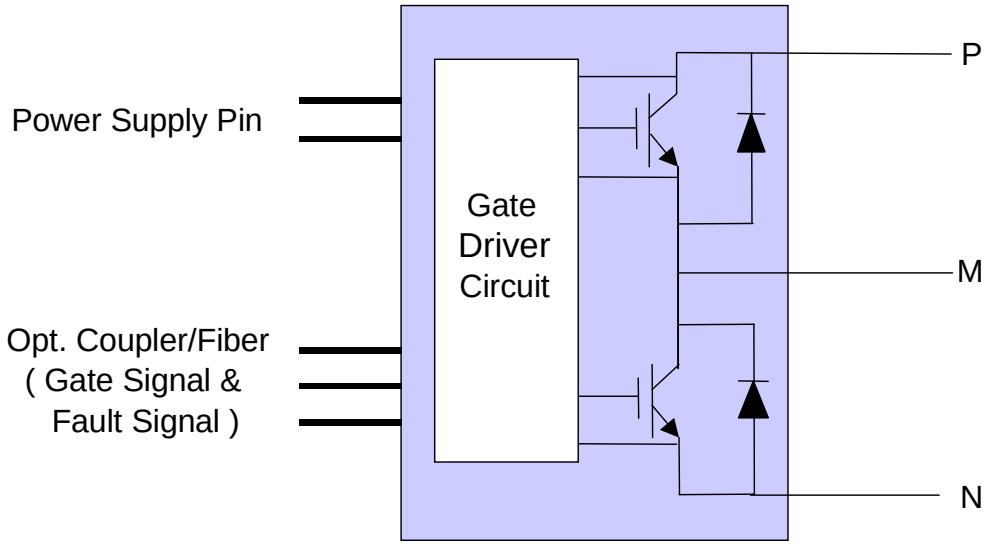
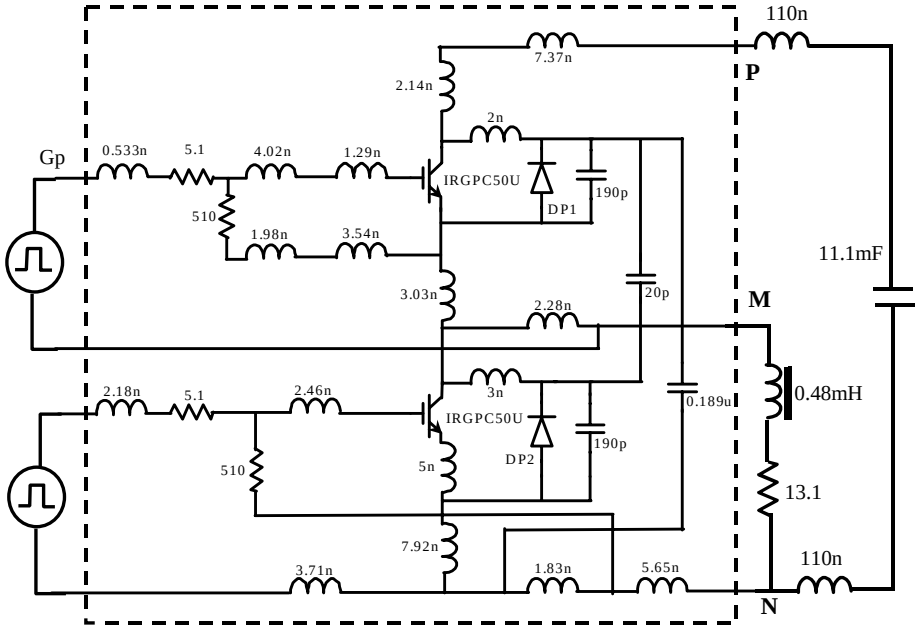


Figure 2.3 The conceptual PEBB switching cell

Figure 2.4(a) shows the simplified equivalent circuit of the PEBB module with the considerations of the layout parasitics. The mutual inductance between the parasitic inductors are not shown in the circuit. This circuit is connected to a 400 V dc bus and an inductive load. The inductors outside the dashed box are the inductance contributed by the terminal bus connection. The gate signal is applied only to the top IGBT, and the bottom IGBT is held off. When the top IGBT is on, the current will flow from the capacitor through the IGBT and load and go back to the source. When the switch is off, the bottom diode will freewheel the load current as a normal buck converter. Based on this model, a simulation is performed using Saber. Figure 2.4(b) and (c) show the switching waveforms of the module, with (b) the voltage waveform between the middle and the positive point and (c) the current going into the module through the dc bus. As shown in the current waveform, the switching frequency current is expected, the high frequency ringing, however, is a severe problem. The resonance is formed in the process of device turn-on and turn-off. For example, when the top IGBT is turned off, the parasitic energy stored in the parasitic inductance will be released through the clamping capacitor. The resonant loop has very little damping, and, therefore, a sustained oscillation is formed. The modeling and simulation is verified with the hardware test of this module, as shown in Figure 2.4(b).

Figure 2.5(a) shows a three-phase inverter composed of three such modules with distributed parasitic inductance on a 400 V dc bus. The middle points of the module are connected to a three-phase inductive load. The space vector modulation (SVM) is used as the control with switching frequency of 20 kHz and modulation frequency 500 Hz. The three-phase current and the current going out of the voltage source are shown in Figure 2.5(b). In addition to the switching frequency ripple, there is another peak representing the parasitic resonant frequency spectrum. This resonant current can cause the overheating of the dc bus capacitor. In general, the parasitic energy is detrimental to a system because it has to be released in the form of power loss, over voltage, ringing current or all of them. This simulation shows only one of the scenarios of parasitic resonance in a simple system structure. The large system requires the integration of a series of PEBB modules with different power levels and complicated layout. The research of the PEBB packaging and structure is to pre-shape the switching waveform of the module so that it is not sensitive to the system integration.



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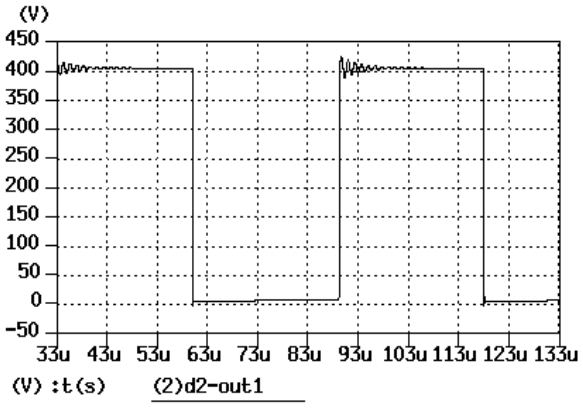

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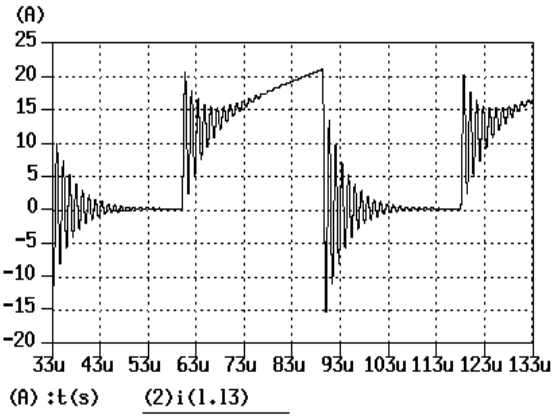

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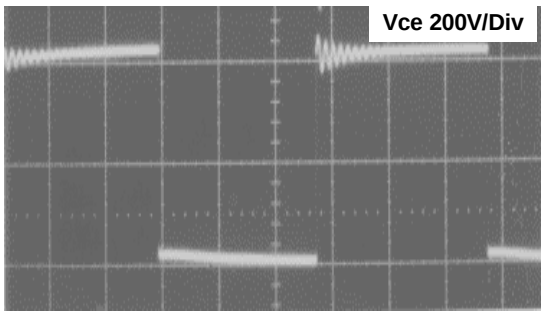

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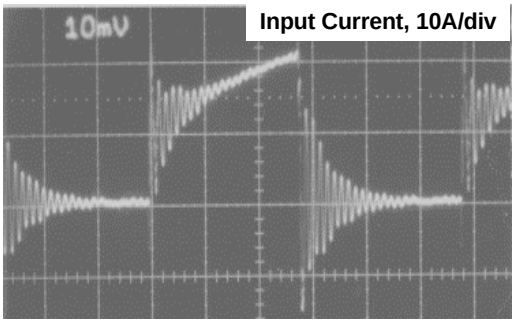
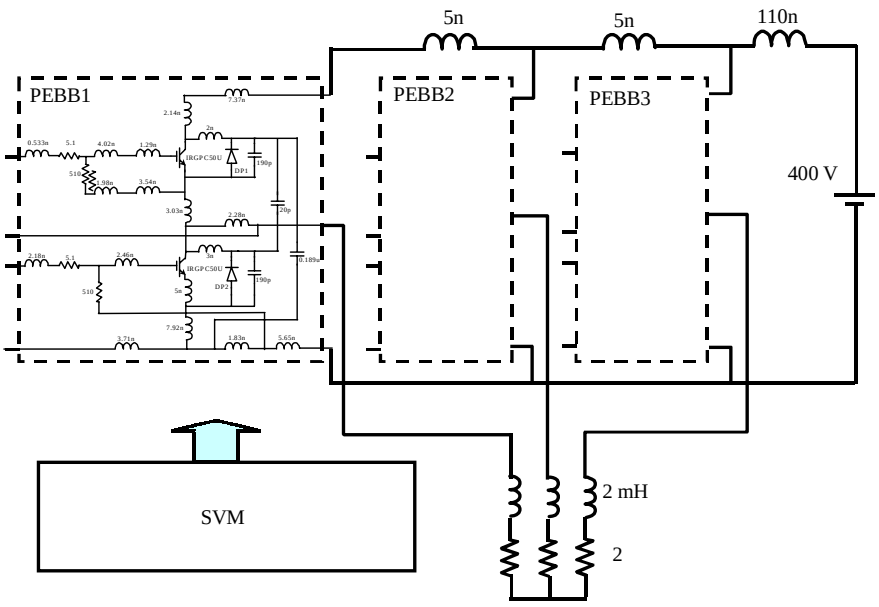


(e)

Figure 2.4 PEBB module and switching waveforms, (a) The equivalent circuit with parasitics, (b) and (c) the simulation waveform of the terminal voltage and current, and (c) and (d) the experimented terminal waveforms



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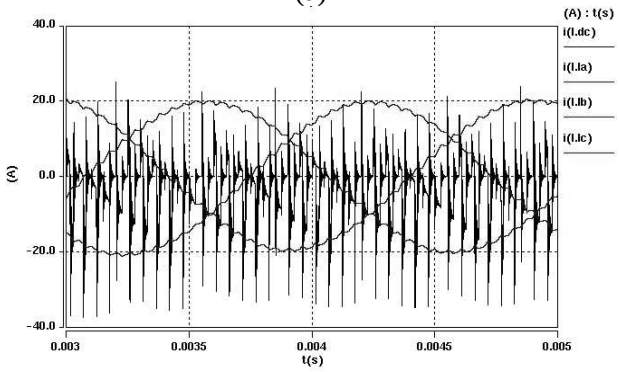

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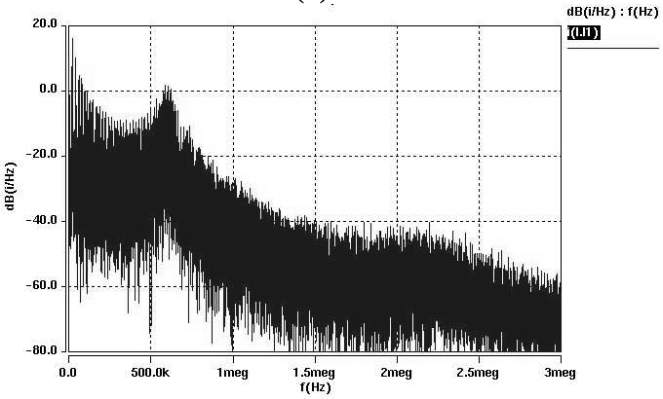


(c)

Figure 2.5 Three-phase inverter and switching waveforms (a) the three-phase inverter, (b) the three-phase current and dc bus current, and (c) the frequency spectrum of the dc bus current

2.2 Extraction of Parasitics within Wire-bond IGBT Modules

Developing advanced packaging techniques for the PEBB module is one of the solutions to reduce the parasitic effect. The power semiconductor devices are fabricated with silicon chips. The packaging process is to make power connections from the silicon chip to the outside. The parasitic inductance exists from the IGBT chip collector and emitter to their terminal connections, no matter what kind of package is used. The parasitic inductance stores energy whenever the current flows through the interconnections when the IGBT is on. When it turns off, the energy is released directly as a voltage spike if there is no external snubber capacitor in the current loop. The spike is a function of inductance and di/dt rate. Even with careful layout of the power stage, a snubber capacitor usually is needed to absorb this energy. If the snubber loop ESR is small, a high oscillatory current is produced. If the ESR is large, the current waveform is improved, but at the expense of circuit loss and heating. Although the IGBT is designed to remove the conventional heavy-duty snubbers, such as RCD, it cannot survive without some form of snubber circuit in most applications. How to deal with the parasitic effect will ultimately affect the EMI, efficiency, and performance of a circuit.

Before the new packaging techniques were investigated, the parasitic effect associated with the commercial wire-bond IGBT module was studied. For the IGBT module, there are three trade-offs: (1) saturation voltage drop and turn-off fall time; (2) forward oscillation and current peaking during commutation and turn-on loss; and (3) turn-off voltage spikes and turn-off time [B1]. The third generation IGBT and soft-recovery power diode attempt to solve the problems related to these devices. On the other hand, some of the trade-offs are basically packaging- and application-related. For example, voltage spikes during turn-off are proportional to the total loop inductance. At the packaging point of view, high thermal conductivity and good dielectric property materials, like AlN (Aluminum Nitride) ceramic substrate [B2] and other new substrates, [B3] have been introduced to improve the packaging thermal management as well as the ratio between chip area and module footprint. This, in turn, reduces the packaging inductance. There are also other packaging techniques emerging to reduce the electrode inductance [B4]. Nonetheless, current commercial IGBT power modules still are based on wire-bond technology. The device manufacturer usually recommends three or more soft wires of 20 mil in diameter to handle a current higher than 40 amps in a die area of 60 mm^2. The inductance

associated with a wire-bond IGBT module is still a major concern in the power device packaging and application.

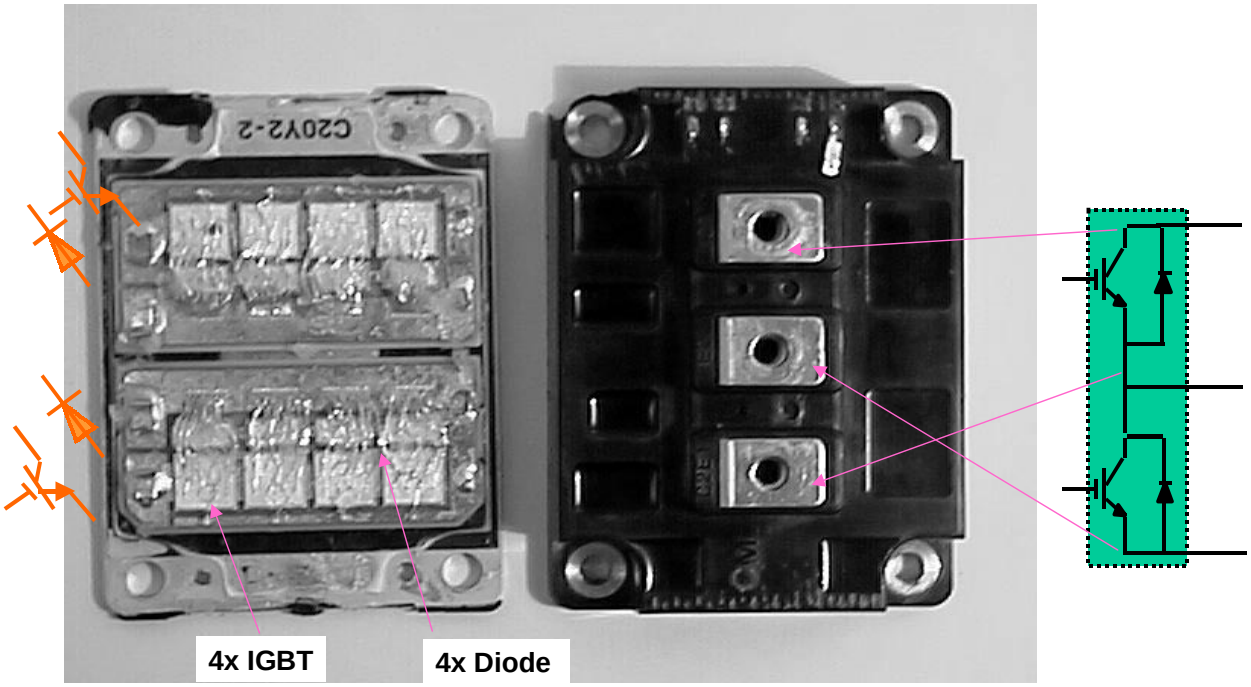
2.2.1 Structure of the IGBT Module

In order to achieve high current capability, silicon chips are connected in parallel with aluminum bonding wires in the commercial plastic modules. This kind of package has been widely used in applications such as motor drives and power conversion. A commercial 300 A/1200 V IGBT module was used in this study. The layout of the package substrate and the plastic chamber is shown in Fig. 2.6 (a). This module is the phase leg as used for the PEBB switching cell in the circuit diagram, which includes a totem pole arrangement of IGBTs and the anti-paralleled diodes. Each IGBT and diode in the circuit actually has four IGBT chips and four diode chips inside the package. The emitter and the gate of the IGBT and the anode of the diode are located on the top of the die. The back is the IGBT collector and diode cathode, respectively. The cross-sectional structure of such a module together with the heat-sink is illustrated in Fig. 2.6(b). The direct-bond-copper (DBC) substrate is etched with the desired pattern such that the attachment of the IGBT and diode chips will make the collector-to-cathode connection in the bottom. Bonding wires are used to solder the IGBT and the diode chips to a conductor pad so that the emitter-to-anode connection can be made. The terminal leads, including power leads and gate control leads, are soldered on the required pad and introduced to the outside screw-mounting holes and the gate control connectors.

2.2.2 Extraction of the Packaging Parasitics Using INCA

Because the module is symmetrical, only half of the module is modeled. As can be seen from Fig. 2.7 (a), which is the input file for the INCA* software, each IGBT has 12 wires connecting the silicon top surface to the conductor pad. The gate connection uses one wire.

* INCA, Inductance Calculator, is provided by Laboratorie d'Electrontechnique de Grenoble CNRS URA 355.



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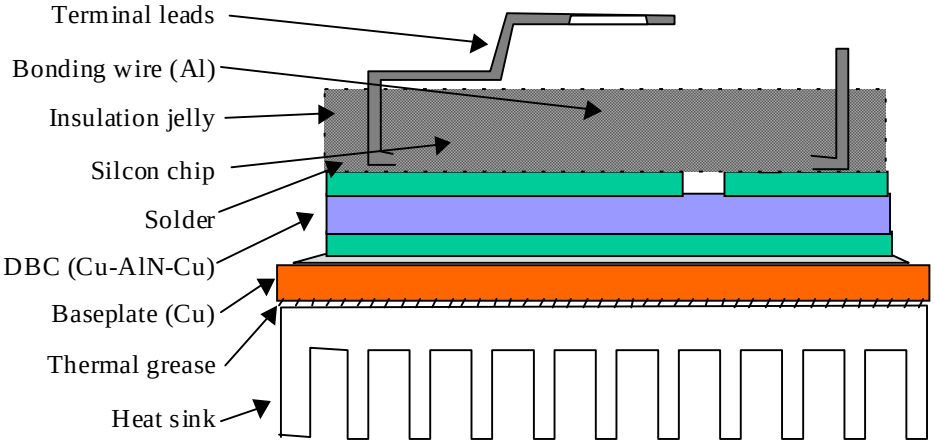


(b)

Figure 2.6 (a) Cut-away of commercial IGBT module (b) The cross-sectional view of the IGBT module on a heatsink

Three factors must be considered when extracting the parasitic inductance. (1) When the switch performs the on and off actions, the circuit structure and the current path change accordingly. The total loop inductance in each operation mode is not a fixed value. Each conductor trace will contribute its own inductance to the circuit. The total loop inductance can be obtained with the partial inductance concept by breaking the loop into pre-defined current paths. (2) In order to account for the skin effect, each small conductor is divided again into subdivisions in the calculation. (3) The mutual coupling between the conductor traces and the ground plane effect have to be taken into consideration.

The parasitic inductance of the IGBT module is calculated at 20 kHz. A ground plane was defined to be the bottom layer of the DBC, which is 25 mil away from the top traces. The calculation results have a resistance and an inductance matrix. The resistance matrix has only diagonal components, which are the conductor resistance at 20 kHz. The inductance matrix has a dimension of 60×60. The diagonal elements are the self-inductance of the conductor traces. The off-diagonal elements are the mutual inductance between conductors. After extracting the significant components in the inductance matrix, an equivalent circuit is obtained, which is shown in Fig. 4(b). There is actually a resistance related to each inductor and numerous mutual inductances between the inductors which are not shown in this diagram for clarity.

The terminal lead inductance also is calculated using this method. The typical value of the lead inductance is about 30 nH, which actually dominates the package inductance. The equivalent capacitance in the layout is estimated using the formula:

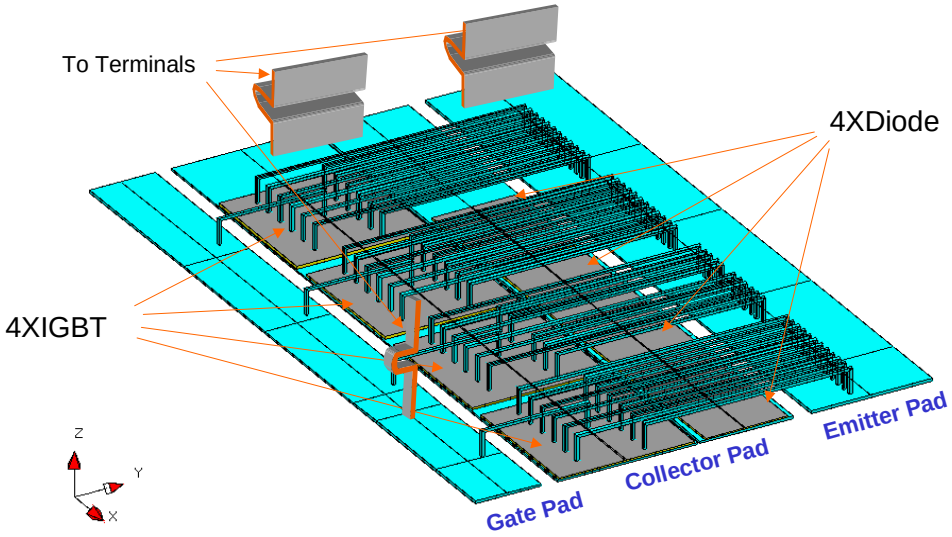
$$c = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{2-1}$$

where ε_0 is the air dielectric constant, ε_r is the relative dielectric constant of the substrate material, A is the equivalent area, and d is the distance between the top copper conductors and the DBC bottom copper layer.

2.3 The Parasitic Effects Related to Wire-bond

2.3.1 Uneven Current Distribution between Bonding Wires

Because the IGBT performs a periodic switching action, the collector current of the IGBT can be expressed in a Fourier series:



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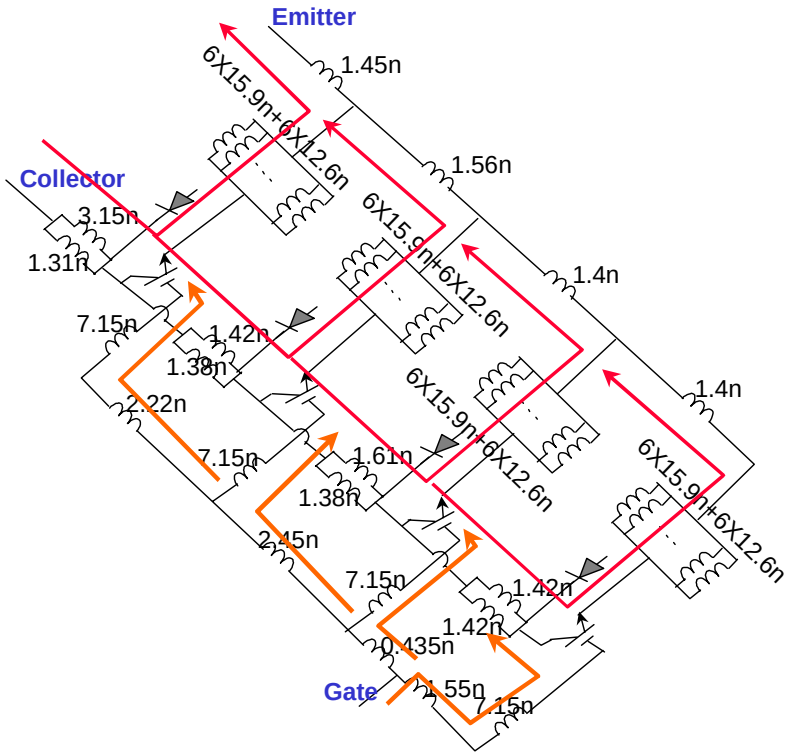


(b)

Figure 2.7 Extraction of parasitics in a IGBT layout, (a) INCA input layout file, (b) Equivalent circuit

$$Ic = \sum_{i=0}^{\infty} I_i \cos(i\omega + \theta_i) \qquad (2\text{-}2)$$

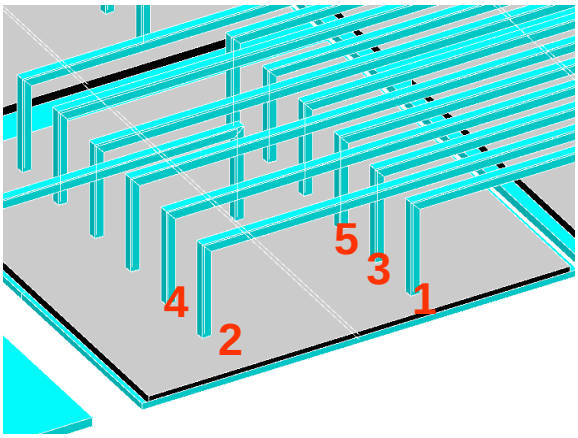
$$i = 1,3,5,\ldots.,$$

where ω is the switching angular frequency and I_i is the magnitude of harmonics of the current. Inside the IGBT module, the current has to go through the bonding wires to the outside connectors. Theoretically, the current in the coupled wires can be calculated based on circuit theory using equation (2-3), where ω_i and I_i are the harmonic angular frequency and magnitude, and m_{ij} is the mutual inductance between wires. R_i and L_i are the self-resistance and inductance.

$$\begin{bmatrix} R_1+j\omega_1 L_1 & j\omega_1 m_{12} & j\omega_1 m_{13} & \ldots & j\omega_1 m_{1n} & -1 \\ j\omega_1 m_{21} & R_2+j\omega_1 L_2 & j\omega_1 m_{23} & \ldots & j\omega_1 m_{2n} & -1 \\ j\omega_1 m_{31} & jw_1 m_{32} & R_3+j\omega_1 L_3 & \ldots & j\omega_1 m_{3n} & -1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & -1 \\ j\omega_1 m_{n1} & j\omega_1 m_{n2} & j\omega_1 m_{n3} & \cdots & R_n+j\omega_1 L_n & -1 \\ 1 & 1 & 1 & \cdots & 1 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ \\ i_n \\ v \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ Ii \end{bmatrix} \qquad (2\text{-}3)$$

The harmonic contents of a current will be different under different circuit operating conditions. The total current in a particular wire is the sum of the fundamental component and all the harmonics going through it. Each harmonic current will contribute its own amplitude and phase angle. Total current can be calculated based on the linear superposition theory by adding all harmonic currents. This process requires a complicated matrix manipulation. In this paper, a simulation was performed using a circuit simulator. The commonly used clamped inductive load circuit is used as the example, where the IGBT and diode are carrying current alternately. From the simulated current waveform, the following phenomena were observed.

In the transients where the current rises and falls quickly, the high frequency contents are concentrated. As the current starts to increase or decrease, the mutual coupling terms in the equation become so significant that the wires in the edge appear as a low impedance path compared to the middle wires. Those wires carry more current than the others. Meanwhile, because of the non-uniform bonding wires on the chip, the steady state current distribution is affected. This can possibly load the IGBT cells inside the silicon differently. Figure 2.8(a) shows the wire connections on the first chip of the module. Figure 2.8(b) shows the current distribution between those wires.



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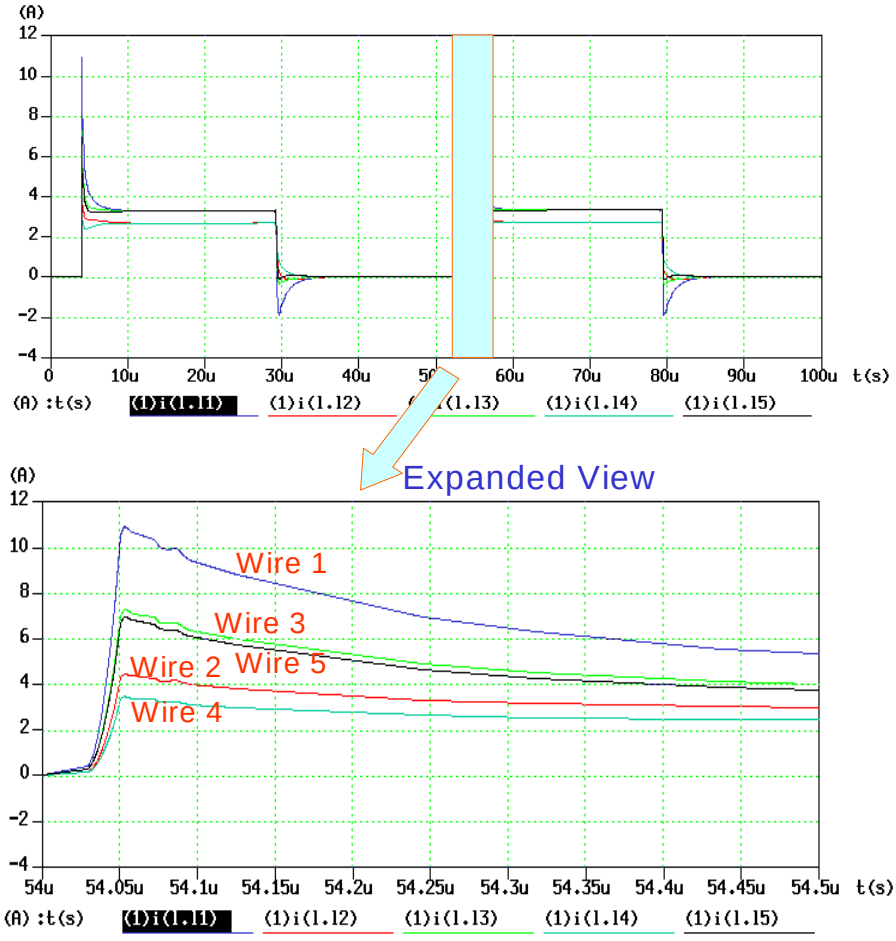


(b)

Figure 2.8 Current distribution in wires, (a) Expanded view of bonding wires on IGBT chip 1, (b) Current waveforms

2.3.2 Nonuniform Current in Paralleled Chips

Because of the planar layout of the package and relatively large total-chip-area of the high power module, the parasitics are a distributed parameter. Even though the chips are carefully selected to be in parallel, there are still discrepancies in circuit parameters imposed by the parasitics, which exist in the high current loop as well as the gating signal loop. These differences together with the proximity effect result in a nonuniform current distribution between the chips. This is shown in Fig. 2.9, where the four chips provide equal current in steady state, but the transient currents are different. The chip in the edge and close to the applied gate signal has the highest di/dt rate. This actually prevents the paralleled IGBTs from being identical. This effect will result in an uneven power loss of the paralleled chips. And finally, it behaves as an uneven thermal distribution problem.

2.3.3 Mechanical Stress on Bonding Wires

It is known that a magnetic force will be generated on a conductor carrying current when it is exposed to a magnetic field. The force generated on a particular wire can be regarded as:

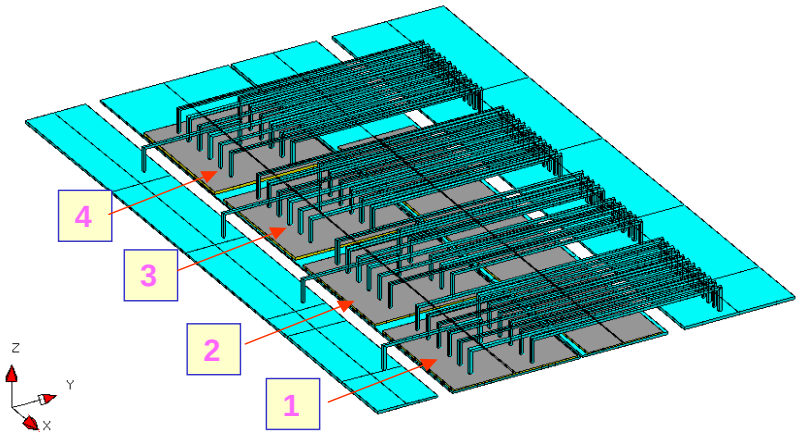
$$f_i = Bi_i l_i , \tag{2-4}$$

where, i_i and l_i are the current and the length of the *ith* wire, and *B* is the magnetic flux density at that position

The magnetic flux density is the sum of the flux density generated by all the other bonding wires, if we assume that the wires are perfectly in parallel, and their length is much longer compared to their distance. The flux density contributed by wire *k* to *i* can be written as:

$$B_{i,k} = \frac{i_k \mu_0}{2\pi\delta_{i,k}}, \tag{2-5}$$

where $\delta_{i,k}$ is the distance between the two wires, and i_k is the current magnitude in wire *k*.



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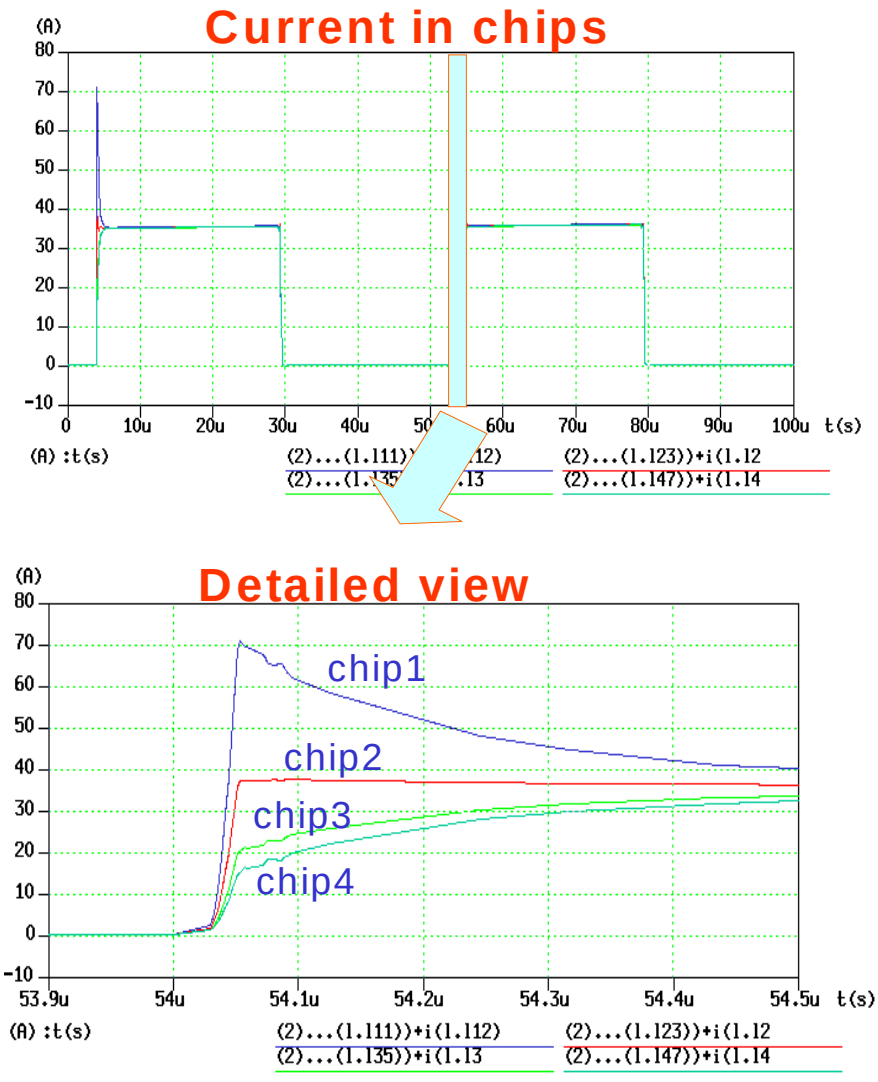
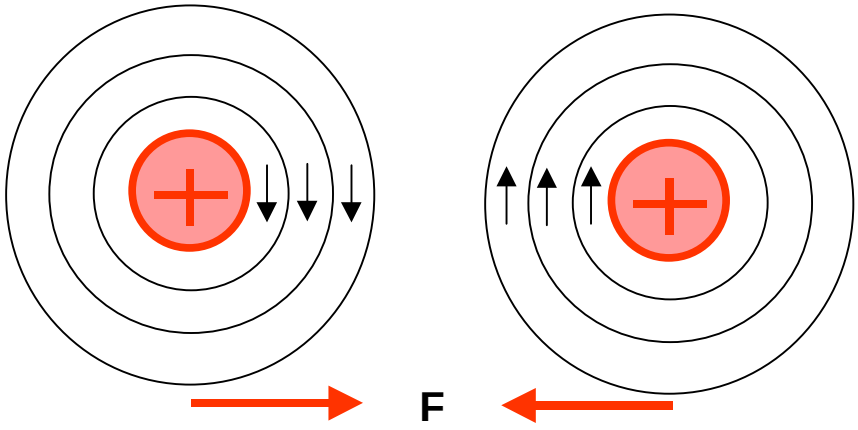


(b)

Figure 2.9 Current distribution in chips: (a) IGBT chips in the layout, (b) Current waveforms



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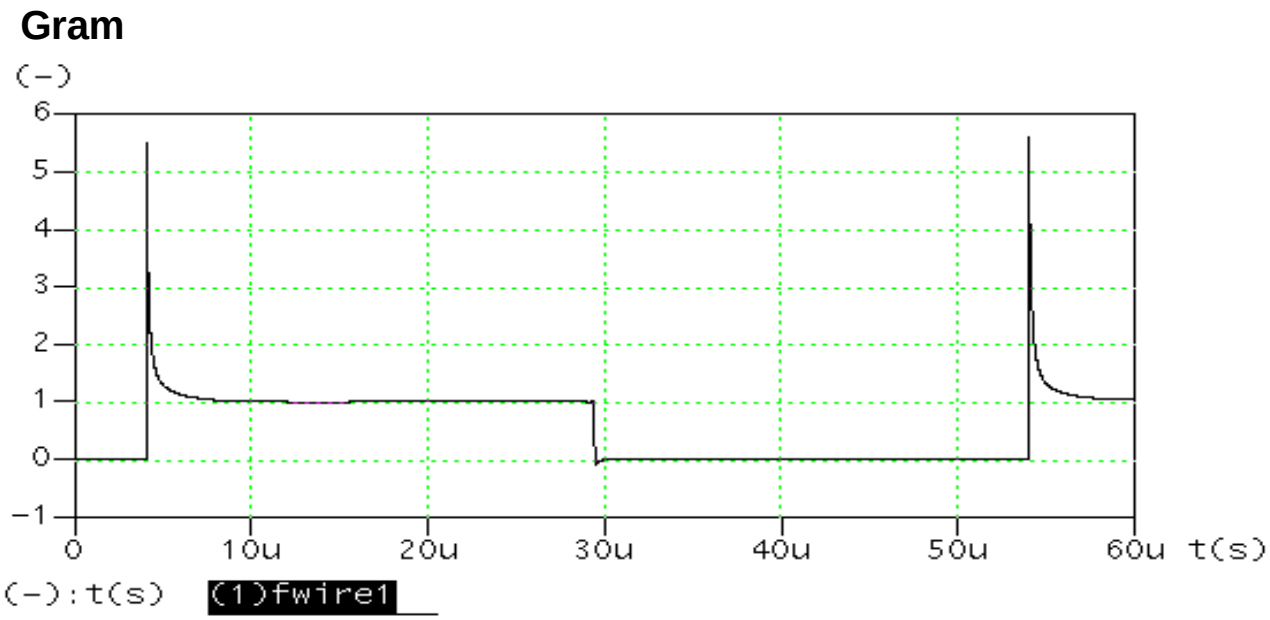


(b)

Figure 2.10 Contraction force generated on wire 1

With this simplified model, the magnetic force generated on the bonding wires can be simulated. Figure 2.10 shows the force generated on the first wire (with its adjacent 24 wires considered). This explains why the wire-bond modules are more fragile under large repetitive transient current. Under thermal and power cycling, with the deviation of device characteristics, the bonding joint fatigue mechanism becomes more complicated with the thermal, electrical, magnetic and mechanical interactions. [B5] reported a similar phenomena: the aluminum layer under the solder joint is likely to de-bond under power cycling, which increases the on-voltage drop and power loss.

2.3.4 Design Considerations of the Packaging Layout

High reliability and long-term stability are essential in high power applications. According to [B6,7], a 30-year lifetime, 338,000 long-term cycles, and 12 million short-term temperature changes are required for traction applications. But the reliability of IGBT modules has been questioned for such applications. Several scenarios have been used to explain the IGBT failure. The first involves the temperature dependence of the forward characteristics of the IGBT devices. Negative temperature coefficient of resistance is detrimental for current sharing. The second involves the TCE mismatch between the silicon and copper base-plate in the thermal cycling. The third involves the packaging parasitics. Both IGBT turn-off and turn-on dv/dt spikes have a detrimental effect in causing the shoot-through failures. With a certain circuit layout, it can only be controlled effectively by the gate resistance at the cost of high switching loss. In many applications, it can be found easily that one or two bonding wires were opened, or that the chip surface at the bonding joints is cracked when an IGBT failed. First of all, the conductor trace on a packaging substrate has to accommodate the required current rating of the device. The maximum current through a conductor can be determined by the relationship:

$$I_{max} = J_D W t \qquad (2\text{-}6)$$

Where W is the conductor width,

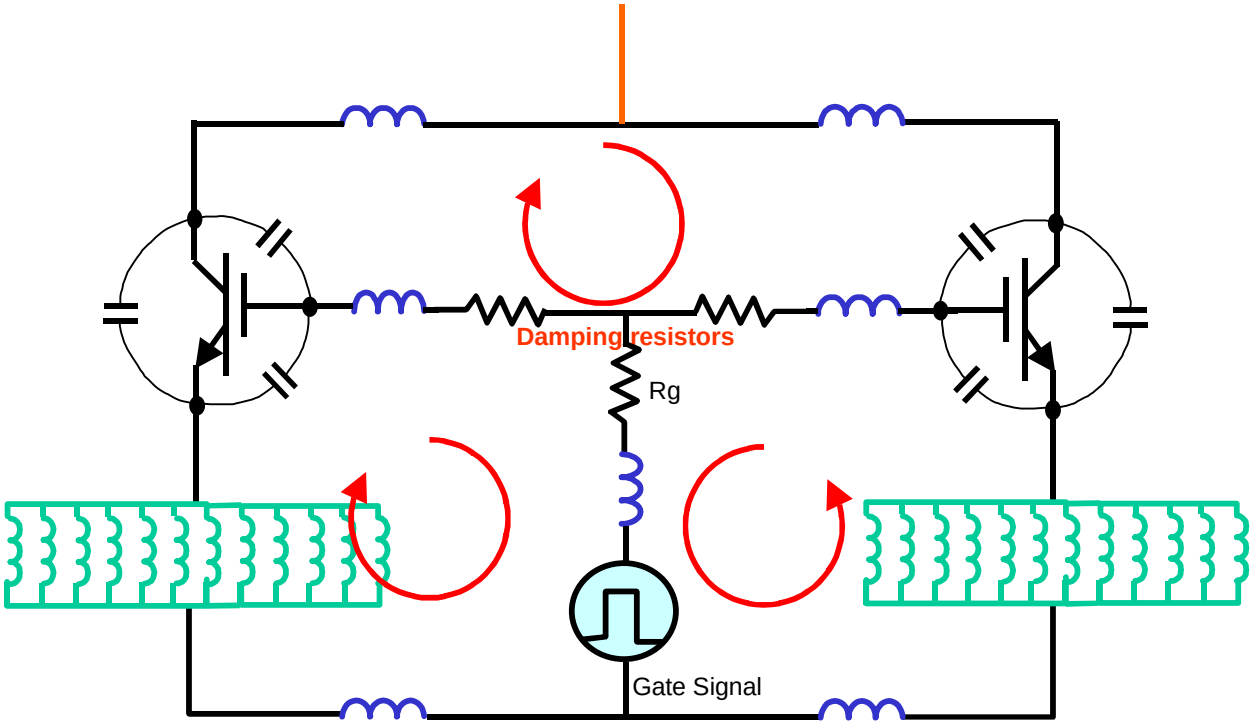
t is the conductor thickness.

J_D is the current density, $J_D \approx 3\text{x}10^4$ A/cm^2 (~$2\text{x}10^5$ A/in^2) for pure copper conductors

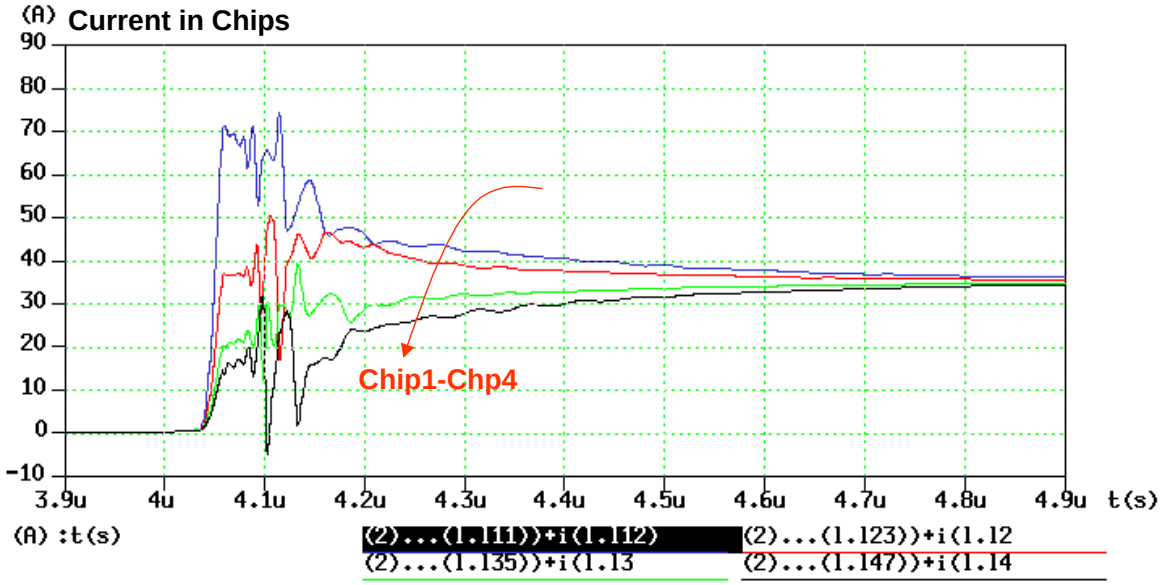
The process of parasitic extraction reveals the piece-to-piece layout-to-circuit relationship. Therefore, the dominant parasitics can be identified, and design improvements can be made. The parasitic inductance of a module can be defined as several categories from their origin: (1) the

parasitics caused by the wire-bond or top surface connection, (2) the packaging substrate inductance related to device attachment and thermal management, (3) the electrode inductance, and (4) parasitics outside the package, most importantly, the dc bus inductance. According to the extracted inductance matrix, the bonding wire is about 24 mm long with a diameter of 10 mil. The self-inductance is between 10-20 nH. With 12 such branches in parallel, the equivalent inductance will not exceed several nano-henrys. The substrate conductor trace inductance is also within a range of a few nH. However, the copper strips used for the terminal leads from the substrate to the mounting joints have about 30 nH inductance. The middle terminal of the half-bridge module normally is connected to an inductor. Therefore, the parasitic inductance in series is not a concern. By examining the commercial IGBT modules, one finds that there is still a place to reduce the parasitic inductance related to the terminal connection and the packaging substrate: to utilize the laminated structures as power terminal leads.

In high power IGBT modules, the chips are required to parallel for high current capability. In the actual package process, multi-resonant loops can be formed between the packaging inductance and the IGBT capacitance as shown in Figure 2.11(a). The incurred oscillation at the turn-on process is shown in Figure 2.11(b). Therefore, a damping resistor individually connected to each gate of the IGBT chips is absolutely necessary. This has been recognized and implemented in most of the high power modules. But the gate connection terminal still suffers from a parasitics inductance as large as that in the power terminals. The impedance exhibited by long terminal leads can be extremely high under the high dv/dt slew rate. The dv/dt coupled by the miller capacitance between the collector and gate can trigger the IGBT falsely. Because the physical measurement points always are located outside the module, the real electrical signal on the IGBT chip is not observable. It is, therefore, desirable to use the laminated structure or twisted insulating wires for the gate terminals. Very closed gate protection components such as gate zenors and a close-to-chip clamping capacitor inside the module will benefit the device for reliable operation.



(a)



(b)

Figure 2.11 The multi-loop oscillation between paralleled chips

2.4 Reduction of Parasitic Effect Using Advance Packaging Techniques

2.4.1 Component Selection for the PEBB Module

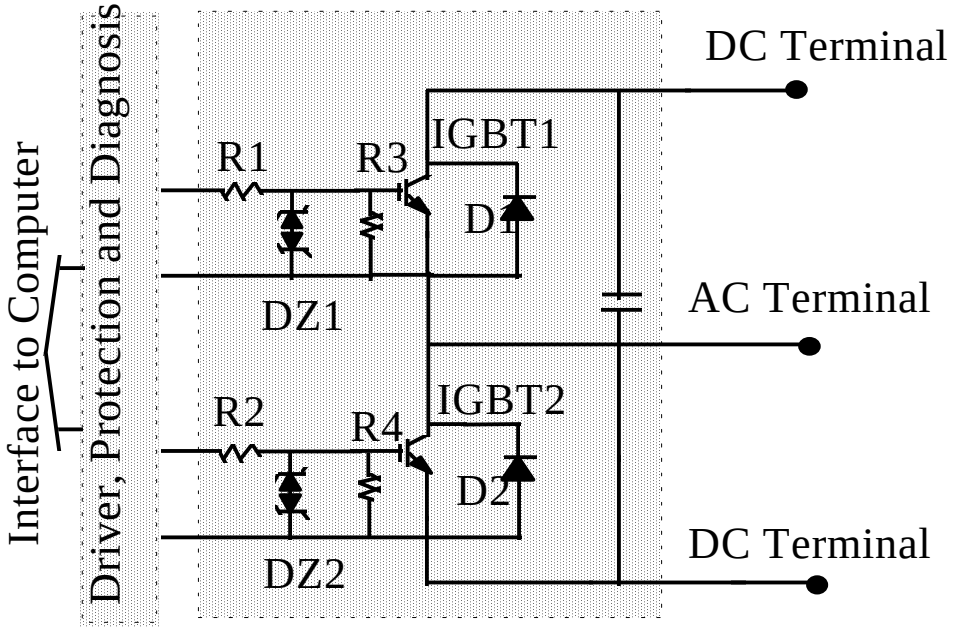
PEBB packaging is one of the key technologies in PEBB research [B8-9]. Based on the identified PEBB structure, the circuit shown in Figure 2.12 was used to test the packaging concepts. The power semiconductor devices are the same as a common phase leg, and several other components are added. A snubber capacitor is connected between dc terminals, which is very close to the IGBT chip so that it will clamp the voltage right on the chip. Several integrated gate components, including the gate resistor and zener diodes, will provide better protection for the IGBTs. Another purpose of putting passive components into the power stage is to verify the package process for hybrid integration. A PCB gate driver is used as the other layer of the package. The parts used in the power stage are listed in Table 2.1. The IGBT top view and diode cross-section view are shown in Figure 2.12 [B11]

Table 2.1 Parts List for Figure 2.2

Device	Rating	Part	Packaging Form
IGBT	600V/40A	IXGD40N60A	Die Form
Diode	600V/50A	C-DWEP55-06A	Die Form
DZ	18V	Harris transient suppressor	SMD
R1, 2	8 Ù 1/4W	Surface mount resistor	SMD
R3, 4	1.5 K 1/4W	Surface mount resistor	SMD
Cap	600V, 0.2ì *F*	NOVA Cap multi-layer ceramic, 0.1uF/600V	SMD

Based on the selected power device, the performance goals for the PEBB package are listed below:

DC Bus	400 V
Three-phase system power processing capability	10 kW
Switching Frequency	20 kHz



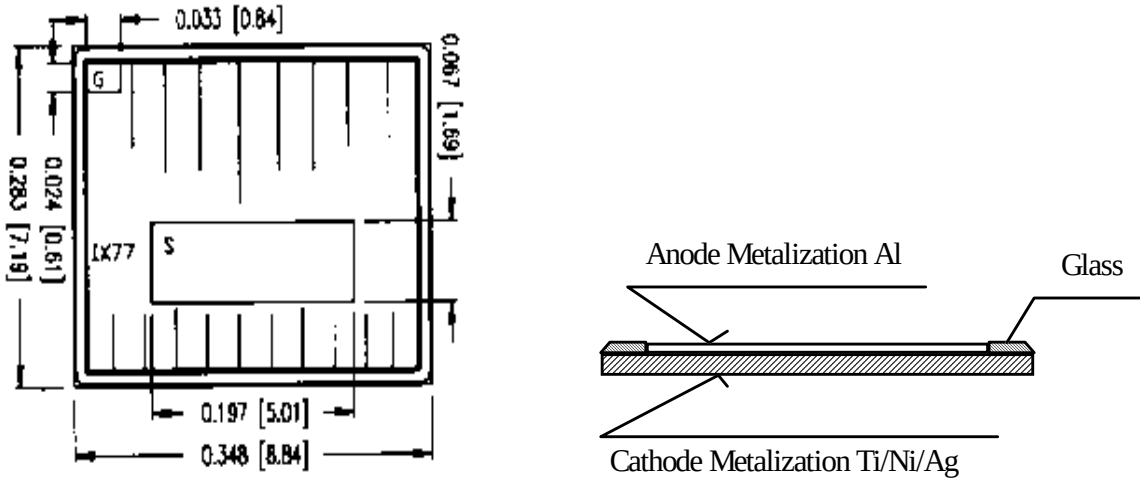
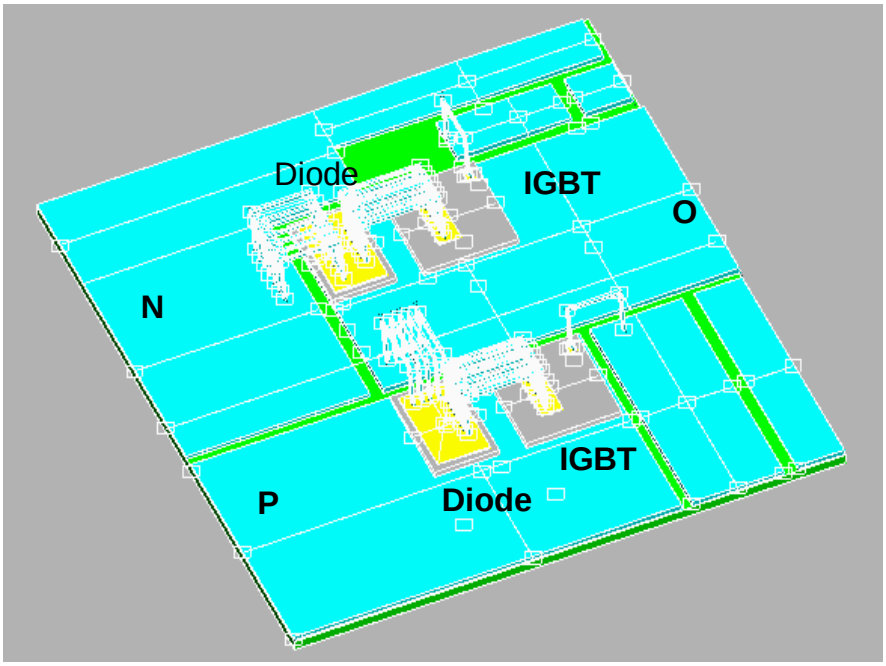
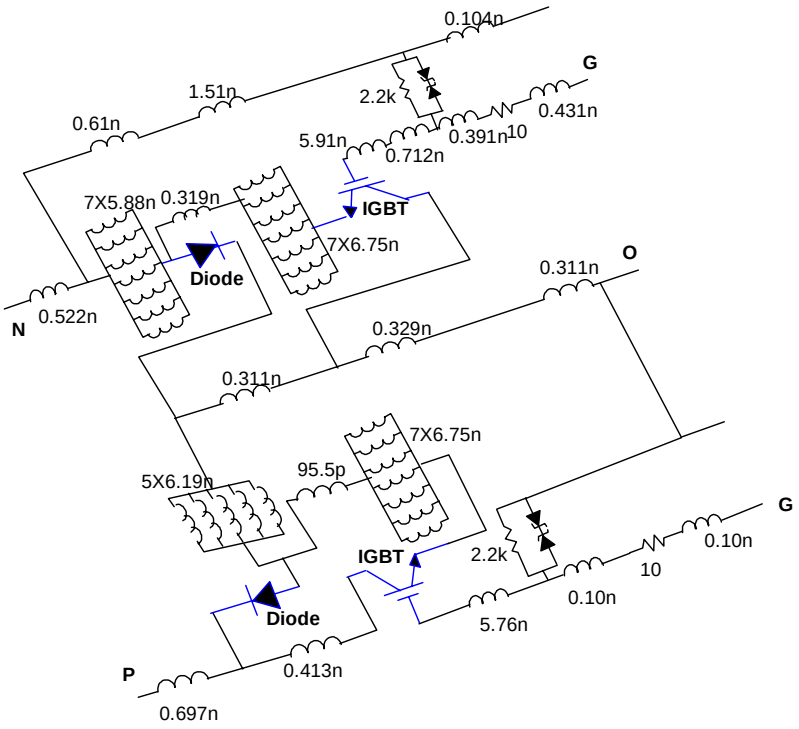


Figure 2.12 Device physical view



(a)



(b)

Figure 2.13 The wire-bond PEBB module, (a) Packaging layout (2) The equivalent circuit with parasitic inductance (mutual inductance and the self-resistance are not shown)

2.4.2 Wire-bond Benchmark module

The wire-bond PEBB module was built as the benchmark in the research. The 2 ×n 2 inch^2 substrate is ALN DBC. The top copper side was itched first into a desired pattern. The IGBT and diode are attached to the DBC copper, which connects the IGBT collector and diode cathode. The connections of the emitter and the anode are made through aluminum wires. The passive components in the circuit diagram are also put on the patterned coppers in the layout. The layout of the wirebond PEBB module and the equivalent circuit with the extracted parameters are shown in Figure 2.13.

2.4.3 Multi-Layer Packaging

As an initial concept, only a two-layer structure was designed and constructed in order to explore the issues involved in the fabrication of these modules as well as to prove the concept. The driver circuit was built outside the module. Figure 2.14 illustrates the design concept. DBC on ceramic is used as the base substrate layer, and is bonded to a metallic heat spreader. The back side, facing the heat sink, of the DBC substrate is full face 12 mil thick copper metallization, while the front side is etched to define the first metal layer. All of the copper layers are nickel-plated to prevent oxidation and to permit bonding and attachment. The next layer above the DBC consists of a ceramic isolation layer which is the same thickness as the power devices used in the circuit. This layer has a number of cutouts or recessed areas contained within it to accommodate the positioning of the power devices, as well as vias to transmit power signals to the top metal layer. The ceramic layer, the heat spreader, and the DBC substrate are fabricated separately and bonded together to form one unit or module, with recessed cavities for the power devices. The power devices are then bonded into the cavities and a dielectric layer is applied on top of the whole assembly. Vias are opened up into the dielectric layer and a second metal layer is applied and patterned to create the second power conductor [A10].

Using the INCA software, the parasitic inductance is extracted from the multi-layer design, as shown in Figure 2.15. In the circuit diagram, the inductance of terminal leads is included, which is at the magnitude of 8 nH.

2.4.4 Comparison of Switching Performance between Different Packaging Approaches

From the circuit point of view, the major differences between the multi-layer and the wire-bond design is the termination inductance. The terminal inductance for the wire-bond module is around 30 nH, whereas the multi-layer modules only has 8 nH terminal inductance. This is because the power leads of the wire-bond module are placed in the same layer; it is difficult to make the lamination structure. Compared to the terminal inductance, other circuit parasitics are relatively small. Figure 2.16 shows the circuit operation waveform of these two modules. The simulation conditions are:

Ideal 400 DC bus, inductive load switching, load current 40 A,

Wire-bond and multilayer layout for PEBB packaging,

Rg=12 Ohm,

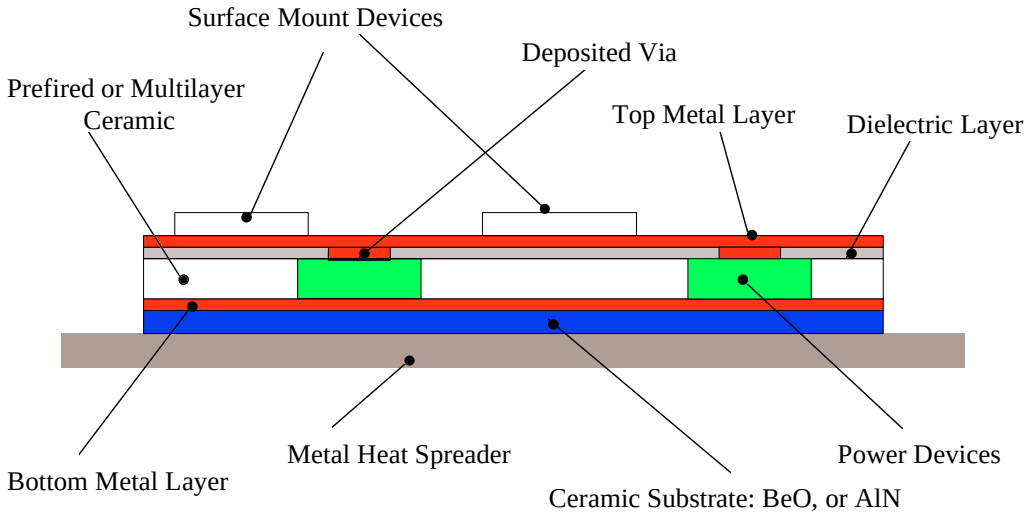
Terminal inductance 30nH for wire-bond design and 8nH for multilayer design respectively,

No snubber capacitors are used in order to see the voltage overshoot.

Saber IGBT models and the diode model in [B10] were used in the simulation.

It can be seen in the waveform that the mutlilayer module has a small switching voltage overshoot, which is reduced by two factors: (1) the parasitic energy storage is reduced with less inductance when the current goes to the conductors and (2) the less the inductance, the higher the oscillation frequency, which can be damped easily by controlling the turn-on speed of the IGBT (gate resistance). Meanwhile, in real circuit operations, a conductor always has a higher resistance at higher frequency because of the skin effect.

A number of other benefits of multi-layer packaging approach include a very short thermal path between the power devices and the heat sink, easier inclusion of driver circuits, and improved mechanical strength of the compact module.



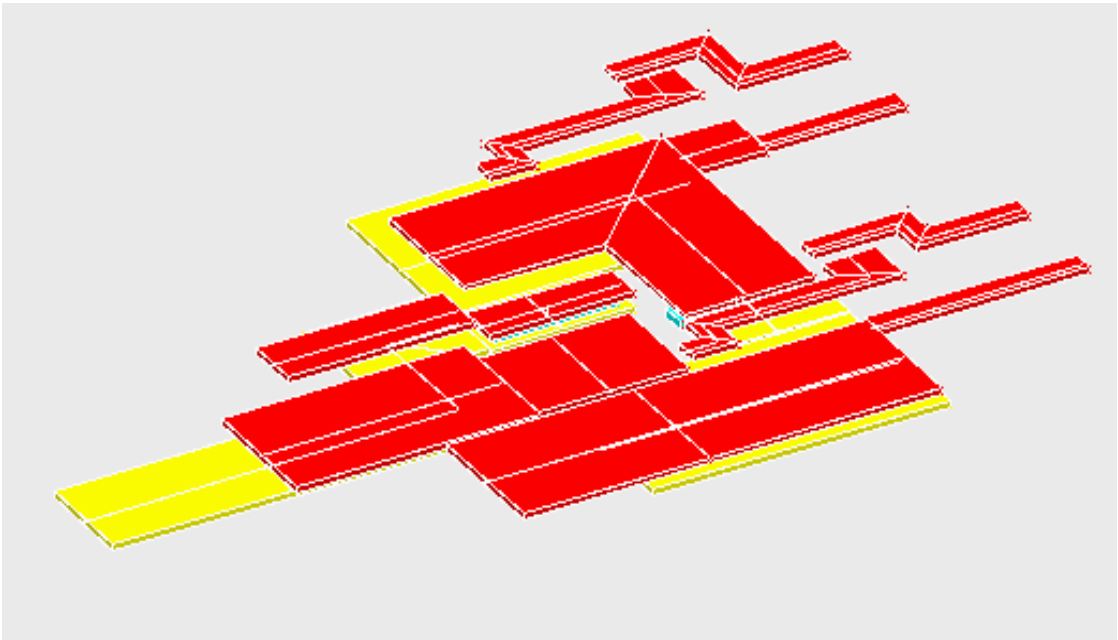


Figure 2.14 A Multilayer packaging technique: (a) Cross section view of the package (b) INCA input file of the design

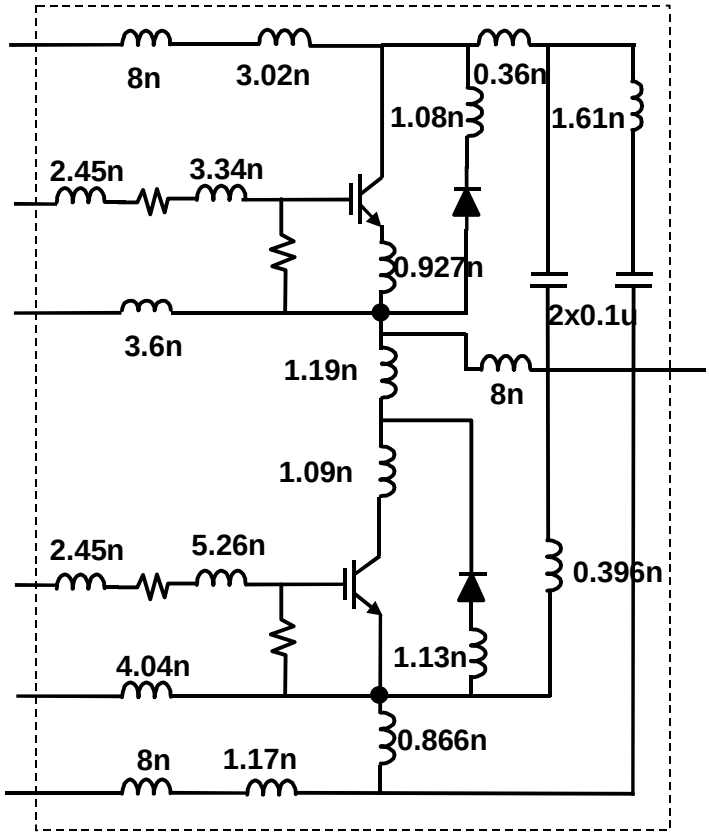


Figure 2.15 The equivalent circuit of the multi-layer design

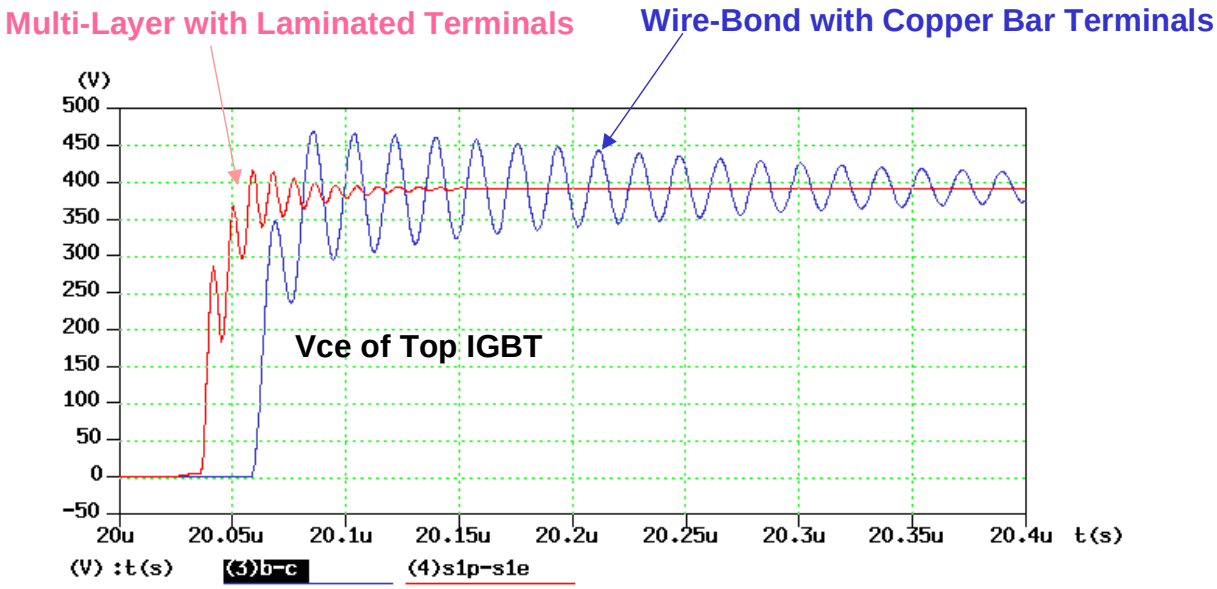


Figure 2.16 The diode turn-off dv/dt (bottom IGBT turn-on) waveform with different packaging designs

2.5 Reduction of Parasitic Effects Using Soft Switching Techniques

A PEBB module can be treated as a multi-terminal box. The desired input current and output voltage waveform would have soft rising and falling edges for easier system integration. There are many soft-switching techniques [C1-C4]. The soft-switching topologies that can be incorporated with the PEBB module are considered the candidates for PEBB application.

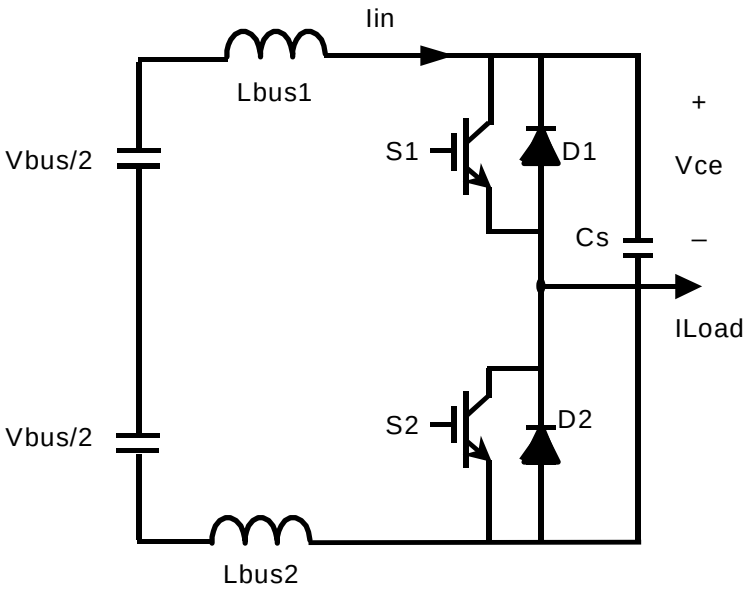
2.5.1 Auxiliary Resonant Commutated Pole Converter (ARCP)

The ARCP is believed to be the most viable approach for high power applications. Figure 2.18(a) shows a PEBB module integrated with the ARCP, which is inside the dashed box. Lr and Cr are the resonant tank inductor and capacitors. Split capacitors are used for the soft-switching commutation.

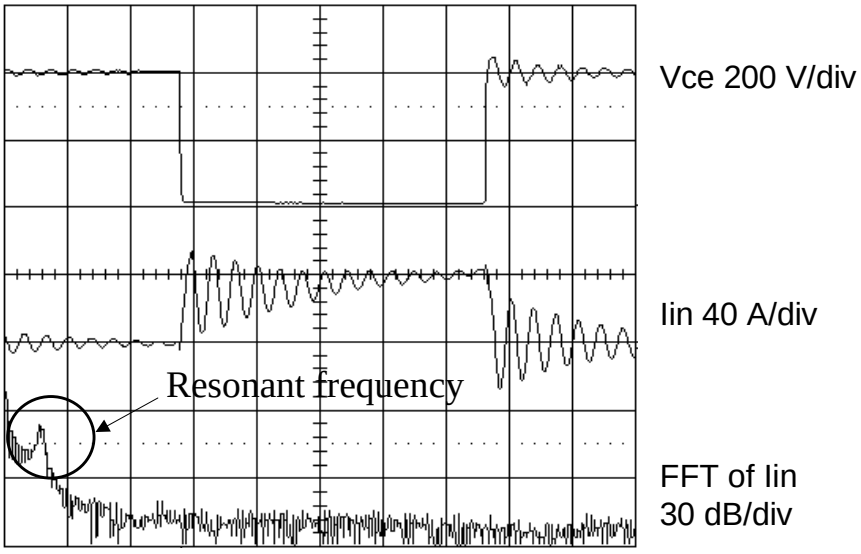
The discussion is focused on the commutation between D2 and S1. The load current is assumed to be going out of the middle point as shown in this Figure.

In the hard switching conditions, Lbus2 stores the parasitic energy when the D2 is carrying the load current. And Lbus2 is charged with the energy after the current is commutated from D2 to S1. The current shift between D2 and S1 is completed in turn-off and -on process, but parasitic energy is released in the resonant loop formed by the dc bus capacitors, bus inductors, and the clamping capacitor Cs, which incurs a high frequency oscillation. The commutation from S1 to D2 is the similar to the above process. Therefore, the two commutation waveform edges are contaminated with high frequency ringings, as shown in Figure 2.17.

In ARCP operation, before S1 is turned on, the S4 is turned on first. The diode current in D2 is decreased linearly by the bottom capacitor. Before the D2 diode current falls to zero, S2 is turned on under zero voltage conditions, and S2 keeps conduction to let the inductor Lr overcharged with extra current. When S2 is turned off, the extra inductor current charges the Cr2 and discharges Cr1. After Cr1 is completely discharged to zero, D1 conducts, which introduces the ZVS condition for S1. The current in Lbus2 is effectively controlled by the resonant inductor and the bus capacitor. When the S2 is turned off, however, the commutation process is almost the same as the hard switching except that Cr1 and Cr2 will also participate in the parasitic ringing. Therefore, only one of the commutation edges is clean as shown in Figure 2.19 (a).

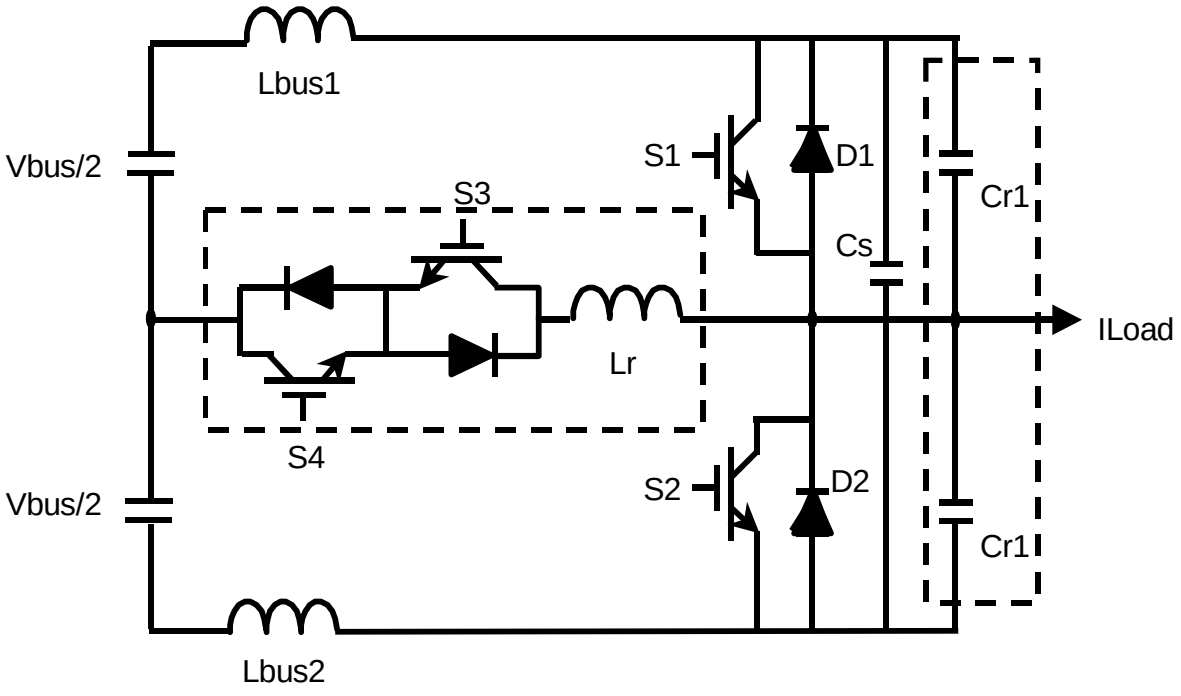


(a)



(b)

Figure 2.17 Hard switching PEBB and switching waveforms and frequency spectrum



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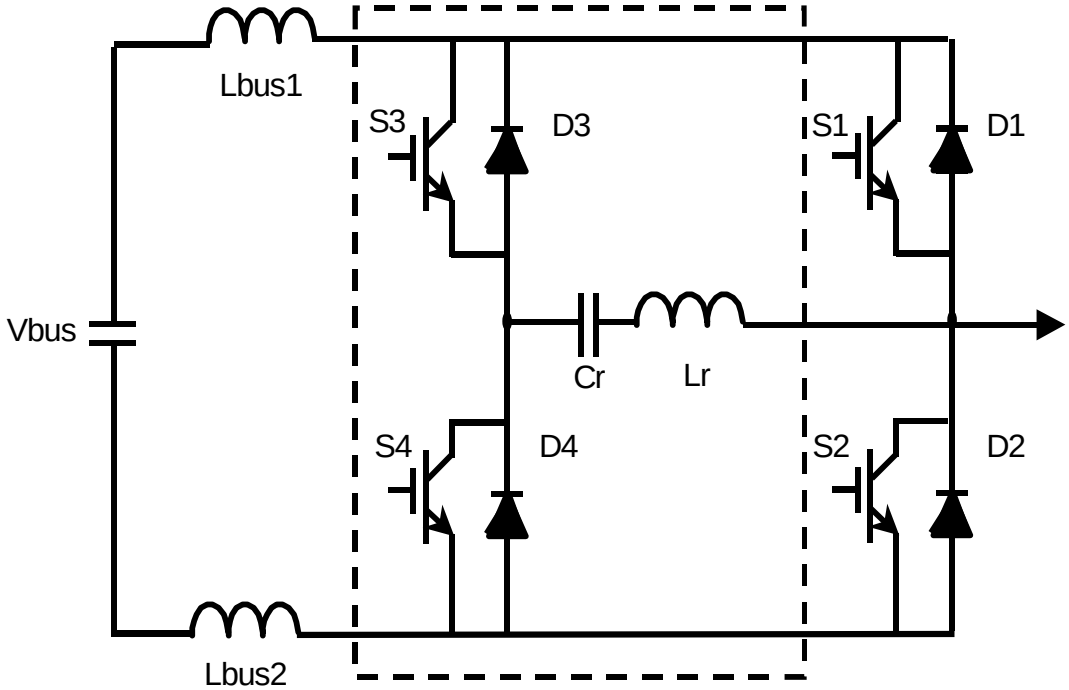
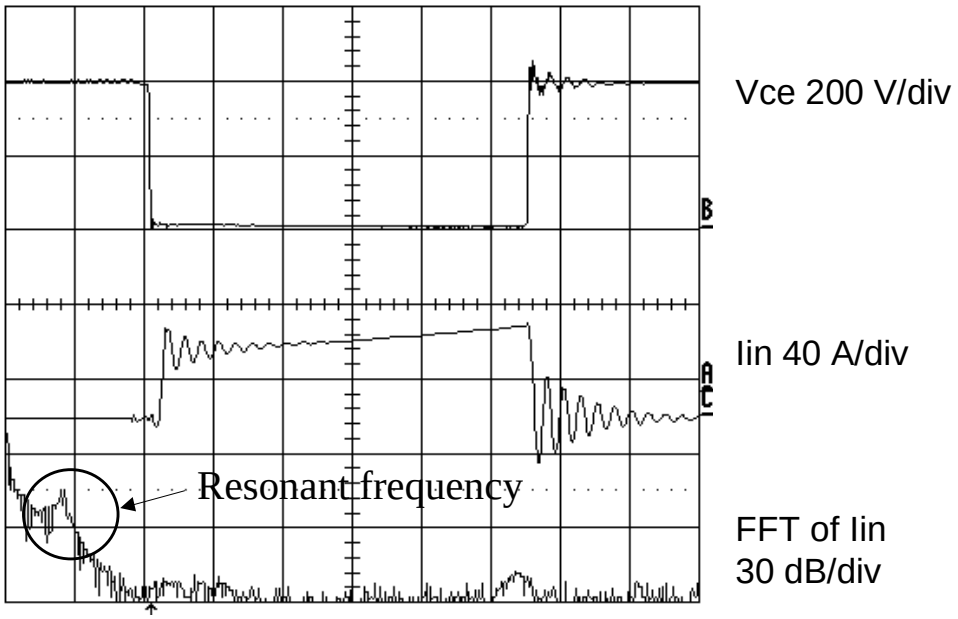
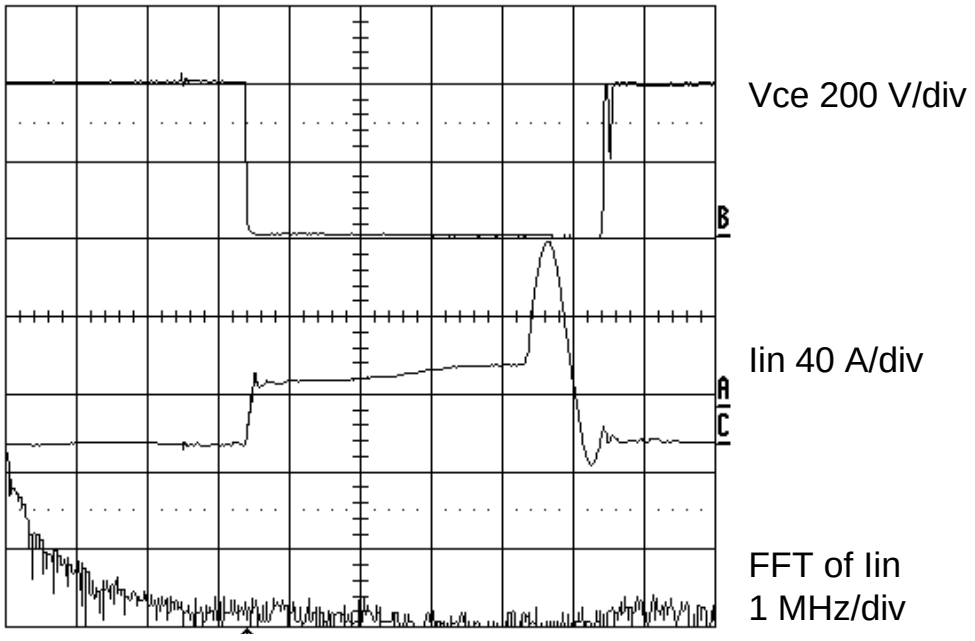


(b)

Figure 2.18 PEBB with ARCP and ZCT soft-switching techniques, (a) ARCP, (b) ZCT



(a)



(b)

Figure 2.19 Comparison of ARCP (a) and ZCT (b) soft-switching waveforms and frequency spectrum

2.5.2 ZCT Soft-Switching Technique

Intuitively, the parasitic energy stored in the power current flowing path is the problem of the current ringing and voltage overshoot. If the energy could be released smoothly in the device turn-on and turn-off process, there would be no such concerns. The improved ZCT technique was proposed by Mao [C3]. It is one of the best soft-switching techniques to reduce the switching losses. With improved control scheme, the main switch can achieve zero current turn off. The auxiliary switches are soft-switched. The main diode reverse recovery is alleviated. The major advantage of the ZCT technique for PEBB application is that the parasitic energy associated with parasitic inductance in the main switch can be absorbed into the soft-switching resonant loop. Therefore, the falling edge of the current is controlled. There is no voltage spike or current ringing caused by the parasitic energy at turn on and off. Figure 2.16 shows the ZCT PEBB configuration. Figure 2.18 shows the switching waveforms and the frequency spectrums of the ARCP and ZCT. When the top switch turns off, the current in the dc bus parasitic inductance naturally rings back to zero, as shown in the switching waveform. There is no high frequency ringing at the turn-on and turn-off edges. Therefore, the frequency spectrum of the current has no peaking associated with the ringing frequency. The resonant frequency of the soft-switching network is at the low frequency range.

Generally speaking, the soft-switching techniques can improve the switching waveforms of PEBB module. Because the concerned the waveforms for PEBB application are at the terminals, the soft-switching techniques, which are good for power semiconductor devices, may not be good as well for PEBBs. The ZCT soft-switching technique reduces the switching losses and improves the switching waveforms.