

# Ac-dc Bus-interface Bi-directional Converters in Renewable Energy Systems

Dong Dong

Dissertation submitted to the Faculty of the Virginia  
Polytechnic Institute and State University in partial fulfillment of  
the requirements for the degree of

Doctor of Philosophy  
in  
Electrical Engineering

Dushan Boroyevich

Fred C. Lee

Paolo Mattavelli

Jaime De La Ree Lopez

John J. Lesko

July 25, 2012

Blacksburg, Virginia

Keywords: grid-interface power converter, residential dc distribution  
systems, passive filters, grid-synchronization, islanding detection

# Ac-dc Bus-interface Bi-directional Converters in Renewable Energy Systems

Dong Dong

## Abstract

This dissertation covers several issues related to the ac-dc bus-interface bi-directional converters in renewable energy systems.

The dissertation explores a dc-electronic distribution system for residential and commercial applications with a focus on the design of an ac-dc bi-directional converter for such application. This converter is named as the “Energy Control Center” due to its unique role in the system. First, the impact of the unbalanced power from the ac grid, especially the single-phase grid, on the dc system operation is analyzed. Then, a simple ac-dc two-stage topology and an advanced digital control system is proposed with a detailed design procedure. The proposed converter system significantly reduces the dc-link capacitor volume and achieves a dynamics-decoupling operation between the interfaced systems. The total volume of the two-stage topology can be reduced by upto three times compared with the typical design of a full-bridge converter. In addition, film capacitors can be used instead of electrolytic capacitors in the system, and thus the whole system reliability is improved.

A set of ac passive plus active filter solutions is proposed for the ac-dc bus-interface converter which significantly reduces the total power filter volume but still eliminate the total leakage current and the common-mode conducted EMI noises by more than 90%. The dc-side low-frequency CM voltage ripple generated by the unbalanced ac voltages can be eliminated as well. The proposed solution features a high reliability and fits three types of the prevalent low-voltage ac distribution systems.

Grid synchronization, a critical interface control in ac-dc bus-interface converters, is discussed in detail. First, a novel single-phase grid synchronization solution is proposed to achieve the rejection of multiple noises as well as the capability to track the ac voltage

amplitude. Then, a comprehensive modeling methodology of the grid synchronization for three-phase system is proposed to explain the output frequency behaviors of grid-interface power converters at the weak grid, at the islanded condition, and at the multi-converter condition. The proposed models provide a strong tool to predict the grid synchronization instabilities raised from industries under many operating conditions, which is critical in future more-distributed-generation power systems.

Islanding detection issues in ac-dc bus-interface converters are discussed in detail. More than five frequency-based islanding detection algorithms are proposed. These solutions achieve different performances and are suitable for different applications, which are advantageous over existing solutions. More importantly, the detailed modeling, trade-off analysis, and design procedures are given to help completely understand the principles. In the end, the effectiveness of the proposed solutions in a multiple-converter system are analyzed. The results drawn from the discussion can help engineers to evaluate other existing solutions as well.

## Acknowledgements

I would like to express my sincere gratitude to my advisor Dr. Dushan Boroyevich, who gave me this great opportunity to do research and guided me to the field of power electronics. It is hardly to imagine that I didn't know Buck and Boost when I first started my master program five years ago. His profound knowledge, masterly creative thinking, and encouragement have been the source of inspiration through the course of the work and will be consistently inspiring me in the pursuit of my future career.

I wish to thank my professor Dr. Fred C. Lee for his inspiring guidance and encouragement through the project I had and Dr. Paolo Mattavelli for his instructions in many aspects and the creative ideas. I would like to also thank my committee members, Dr. De La Ree, who provided valuable comments and knowledge in power system, and Dr. John Lesko, who gave me lots of support and encouragement during my both master and doctorate study here.

I would like to also thank Dr. Rolando Burgos for giving me help and guidance in my toughest time, and Dr. Fred Wang for giving the support and encouragement in my early study in Blacksburg.

I would like to thank all of my fellows in CPES. Their help, mentorship, and friendship provided a base for the accomplishment of this work. I must mention some of those who made valuable input to my work. They are Dr. Tim Thacker, Dr. Rixin Lai, Dr. Di Zhang, Dr. Puqi Ning, Dr. Carson Baisden, Dr. Sara Ahmed, Dr. Jerry Francis, Dr. Fang Luo, Dr. Jin Li, Dr. Dong Jiang, Dr. Ruxi Wang, Mr. Igor Cvetkovic, Mr. Bo Wen, Mr. Zhiyu Shen, Mr. Zheng Chen, Mr. Xuning Zhang, Mr. Jing Xue, Mr. Wei Zhang, Mr. Jiang Li, Mr. Marko Jaksic, Mr. Milisav Danilovic, and Mr. Hemant Bishnoi.

I would like to thank all the other CPES students who made me enjoying the life here. Although it is not a complete list, I would like to mention: Dr. Luis Arnedo, Dr. Pengju Kong, Dr. Qiang Li, Dr. Xiao Cao, Dr. David Reusch, Dr. Dianbo Fu, Dr. Jian Li, Mr. Zijian Wang, Mr. Pengjie Lai, Mr. Qian Li, Mr. Daocheng Huang, Mr. Feng Yu, Mr. Haoran Wu, Ms. Zhuxian Xu, Mr. Mingkai Mu, Mr. Weiyi Feng, Mr. Yang Jiao, Mr. Shuilin Tian, Ms. Ying Lu, Mr. Chanwit Prasantanakorn, Mr. Zheyuan Tan, Mr. Yingyi

Yan, Mr. Shu Ji, Mr. Yipeng Su, Mr. Zhemin Zhang, Mr. Bo Zhou, and Mr. Lingxiao Xue. I cherish the wonderful time together and the great friendship.

I would like to thank the administrative staff members, Ms. Marianne Hawthorne, Ms. Teresa Shaw, Ms. Trish Rose, Ms. Linda Long, Ms. Linda Gallagher, Mr. Douglas Sterk, and Mr. David Gilham for their support and help over the past five years.

With much love and gratitude, I want to thank my parents for their endless love, encouragement, and support throughout twenty years of school. Thank you for educating me since a very early stage of my life to be a person with a brave heart and a determined mind that help me through all the tough times. I am so proud of being your son!

Finally and most importantly, I must thank my wife Yi Li, whom I love deeply. Thank you for being with me in Blacksburg, sharing laughter and sadness with me. You are my external source of inspiration in every aspect and every moment of my life.

I am sure I have missed my appreciation to many other people. To you all, thank you so much!

All photos in this dissertation are taken by author

# Table of Contents

Chapter 1. Introduction	1
1.1. Background	1
1.1.1. Electrical Energy	1
1.1.2. Electric Power System	2
1.1.3. Technology Trend in EPS	3
1.2. Dissertation Motivations and Objective	6
1.2.1. Challenges to Electric Power System	6
1.2.2. Challenges of Bi-directional Power Electronic Converters in Power Distribution System	7
1.2.3. Challenges in the System Interface Design	8
1.3. Literature Review	9
1.3.1. Residential Dc Distribution System	9
1.3.2. Bus-interface Bi-directional Converter	11
1.3.3. Power Filter Design for System-interface	13
1.3.4. Grid Synchronization and its Stability	13
1.3.5. Islanding Detection	14
1.4. Research Scope and Outline	17
Chapter 2. Single-phase Energy Control Center Converters	19
2.1. Nano-grid, Energy Control Center	19
2.2. ECC Converter Topology	25
2.3. ECC Converter for Single-phase Utility and Dc Nano-grid	29
2.3.1. Impact of Ripple Power on Dc Nano-grid	29
2.3.2. High-density ECC Converter for Single-phase Ac-Dc Bus-interface	33

2.3.3. Bi-directional Control System	40
2.3.4. Volume Comparison and Hardware Development	47
2.3.5. Experimental Evaluation	49
2.3.6. Conclusion	52
Chapter 3. Design and Optimization of Power Filters for Ac-dc Bus-interface Converters	54
3.1. Power Quality issue and Current Technologies	54
3.1.1. Power Quality and its Standard	54
3.1.2. Ac Low-voltage Distribution Practice	57
3.2. High-frequency Leakage Current Reduction using Passive Filter	59
3.2.1. Leakage Current Issue in Single-phase System	59
3.2.2. High-frequency Leakage Current Analysis in Split-phase Single-phase Systems	62
3.2.3. Proposed Modified Ac L-C-L Passive Filter Solution	68
3.2.4. High-frequency Leakage Current Reduction in Asymmetrical Single-phase Systems	76
3.2.5. High-frequency Leakage Current Reduction in Three-phase Systems	78
3.2.6. Conclusion	83
3.3. Low-frequency Dc-side CM Voltage Ripple Reduction using Active Control	83
3.3.1. Active Control System Analysis in Split-phase Single-phase Systems	83
3.3.2. Low-frequency Dc-side CM Voltage Ripple Reduction in Three-phase Systems	93
3.3.3. Low-frequency Dc-side CM Voltage Ripple Reduction in Asymmetrical Single-phase Systems	95
3.3.4. Conclusion	96
3.4. EMI Attenuation in Bus-interface Bi-directional Converter System	96

---

3.4.1. Introduction	96
3.4.2. Grounding Capacitor Impact in EMI Filter Design on Both-sides	98
3.4.3. Floating Filter in Bi-directional Converter System	100
3.4.4. EMI Filter Implementation and the Noise Measurement	106
3.4.5. Conclusion	115
Chapter 4. Modeling of Grid Synchronization in Ac-dc Bus-interface Converters	116
4.1. Single-Phase Phase Locked Loop System	116
4.1.1. Introduction	116
4.1.2. Proposed PLL System and Analysis	121
4.1.3. PLL Modeling and Design	124
4.1.4. Dc-offset and Input Harmonics Noise Rejection	128
4.1.5. Experimental Evaluation	132
4.1.6. Conclusion	134
4.2. Grid Synchronization Behavior and its Stability	135
4.2.1. Introduction	135
4.2.2. Modeling of Grid Synchronization in General Conditions	137
4.2.3. Modeling of Grid Synchronization at Islanded Conditions	153
4.2.4. Low-frequency Small-signal Analysis of Grid Synchronization	167
4.3. Grid Synchronization Modeling for Multi-Converter Condition	177
4.3.1. Introduction	177
4.3.2. Multiple-converter System at Islanded Conditions	177
4.3.3. Multiple-converter System at Weak Grid Conditions	186
4.3.4. Conclusion	194
Chapter 5. Islanding Detection Algorithms in Ac-dc Bus-interface Converters	196
5.1. Introduction	196



---

5.2. Islanding Detection based on Large-signal Stability	199
5.2.1. First PLL-based islanding Detection Method	199
5.2.2. Second PLL-based Islanding Detection Method	206
5.2.3. Experimental Evaluation	208
5.2.4. Conclusion	209
5.3. Islanding Detection based on Small-signal Stability	210
5.3.1. Third PLL-based Islanding-detection Method	210
5.3.2. Fourth and Fifth PLL-based Islanding-detection Methods	218
5.3.3. Experimental Evaluation	221
5.3.4. Conclusion	222
5.4. Evaluation for Multi-converter conditions	223
5.4.1. Introduction	223
5.4.2. Islanding Detection Performance Evaluation	223
5.4.3. Conclusion	227
Chapter 6. Conclusions and Future Work	228
6.1. Summary	228
6.2. Conclusions	230
6.3. Future Work	231
Appendix	232
A.1 Controller Parameters	232
A.2 Derivation of Volt-second	232
A.3 Simulation for Grid-synchronization Study	233
List of References	235

## List of Figures

Fig. 1.1: Illustration of electric power system .....	2
Fig. 1.2: Configurations of energy storage devices: a) directly tied to dc-bus, b) tied to intermediate dc-link, c) tied to dc-bus via charger. ....	10
Fig. 1.3: Illustration of NDZ.....	15
Fig. 2.1: Concept of “smart-grid” .....	20
Fig. 2.2: Inter-grid and ECC Converters .....	22
Fig. 2.3: Structure of dc nano-grid in home.....	24
Fig. 2.4: Two-level VSC .....	26
Fig. 2.5: Three-level boost rectifier .....	26
Fig. 2.6: Three-level neutral point clamp (NPC) converter .....	26
Fig. 2.7: Three-level active neutral point clamp (ANPC) Converter.....	26
Fig. 2.8: Cascaded modular multi-level converter (MMC) .....	27
Fig. 2.9: Cascaded modular multi-level converter.....	27
Fig. 2.10: Ac-ac transformerless ECC.....	27
Fig. 2.11: Dc-ac transformerless ECC.....	27
Fig. 2.12: Bi-directional buck converter.....	28
Fig. 2.13: Three-phase interleaved buck converter.....	28
Fig. 2.14: Two-level full-bridge dc-dc converter .....	28
Fig. 2.15: Example of dc source converters with droop control .....	29
Fig. 2.16: ECC converter dc-side output V-I operation curve.....	30
Fig. 2.17: Single-phase full-bridge converter .....	30
Fig. 2.18: Bi-directional charger (BDC) regulates dc-bus voltage and ECC operates in current limiting mode.....	33
Fig. 2.19: Ripple current [1 A/DIV] flowing to battery charger due to ripple power.....	33
Fig. 2.20: Two-stage bi-directional single-phase PWM converter .....	34
Fig. 2.21: Average current $i_c$ flowing to $C_{dc}$ under different $C_{dc}$ .....	37
Fig. 2.22: Average current flowing to $C_{dc}$ under different $V_{av}$ .....	37
Fig. 2.23: Input impedance of 2 <sup>nd</sup> stage $Z_{in}$ and impedance of $C_{dc}$ under 1.1 mF and 200 uF cases. ....	38
Fig. 2.24: Routes of ac-side high-frequency noise $i_{hs}$ .....	38
Fig. 2.25: $v_{dc\_max}$ and $v_{dc\_min}$ in relationship with $C_{dc}$ and $V_{av}$ .....	39
Fig. 2.26: Minimum point of the dc-link capacitor $C_{dc}$ .....	39
Fig. 2.27: Proposed bi-directional control structure .....	40
Fig. 2.28: Transfer-function block diagram of ECC control system .....	41
Fig. 2.29: Control-to-output small-signal model for 2 <sup>nd</sup> stage.....	43
Fig. 2.30: Output voltage without a resonant controller $R$ .....	44
Fig. 2.31: Output voltage with a resonant controller $R$ .....	44

Fig. 2.32: Ac current without a notch filter .....	45
Fig. 2.33: Ac current with a notch filter .....	45
Fig. 2.34: Simplified ac current loop .....	46
Fig. 2.35: Simplified ac current loop with disturbance rejection .....	46
Fig. 2.36: Simulation system setup .....	46
Fig. 2.37: Simulation of mode transition .....	47
Fig. 2.38: 10 kW ECC converter prototype .....	49
Fig. 2.39: System test setup .....	49
Fig. 2.40: Dc nano-grid testbed setup .....	50
Fig. 2.41: 9 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [200V/DIV] .....	51
Fig. 2.42: 9 kW regenerative mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [200V/DIV] .....	51
Fig. 2.43: 6 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [5V/DIV] .....	51
Fig. 2.44: 9 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [10A/DIV], $V_{dc}$ (purple) [20V/DIV], $V_o$ (orange) [20V/DIV] .....	51
Fig. 2.45: 6 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [5V/DIV] .....	51
Fig. 2.46: 6 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [5V/DIV] .....	51
Fig. 2.47: 6 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [5V/DIV] .....	52
Fig. 2.48: 6 kW rectifier mode test. $V_{ac}$ (green) [200V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [200V/DIV], $V_o$ (orange) [5V/DIV] .....	52
Fig. 2.49: 3 kW rectifier mode test. $V_{ac}$ [500V/DIV], $I_{ac}$ (blue) [50A/DIV], $V_{dc}$ (purple) [100V/DIV], $V_o$ (orange) [20V/DIV] .....	52
Fig. 3.1: Some utility voltage waveforms related to the power quality .....	55
Fig. 3.2: Low-voltage distribution system in North America .....	58
Fig. 3.3: Low-voltage distribution system in Europe and China .....	58
Fig. 3.4: Split-phase single-phase system .....	58
Fig. 3.5: Asymmetrical single-phase system .....	58
Fig. 3.6: Three-phase system .....	58
Fig. 3.7: H5 inverter .....	61
Fig. 3.8: HERIC inverter .....	61
Fig. 3.9: FB-DCBP inverter .....	61
Fig. 3.10: FB-ZVR inverter .....	61

Fig. 3.11: Full-bridge inverter interconnected with grid.....	62
Fig. 3.12: Terminal voltage of each phase-leg, DM and CM voltage.....	63
Fig. 3.13: Spectrum of DM noise .....	64
Fig. 3.14: Spectrum of CM noise .....	64
Fig. 3.15: Equivalent circuit of full-bridge converter .....	65
Fig. 3.16: Simplified equivalent circuit of full-bridge converter.....	65
Fig. 3.17: Equivalent circuit of full-bridge inverter.....	66
Fig. 3.18: CM equivalent circuit of full-bridge converter .....	66
Fig. 3.19: CM voltage of negative dc-rail $v_{dc\_N}$ in simulation using an asymmetrical L-C-L harmonic filter.....	67
Fig. 3.20: CM voltage of negative dc-rail $v_{dc\_N}$ in simulation using a symmetrical L-C-L harmonics filter.....	67
Fig. 3.21: Proposed full-bridge inverter .....	68
Fig. 3.22: Equivalent circuit of the modified full-bridge converter.....	69
Fig. 3.23: Simplified equivalent circuit of the modified full-bridge converter.....	69
Fig. 3.24: CM equivalent circuit of the modified full-bridge converter .....	69
Fig. 3.25: CM voltage of negative dc-rail $v_{dc\_N}$ in simulation by using the proposed full-bridge topology.....	72
Fig. 3.26: Leakage current level by using the typical LCL filter (upper waveform, [5A/DIV]) and the modified filter (lower waveform, [5mA/DIV]) .....	73
Fig. 3.27: AC CM choke and AC DM capacitors.....	74
Fig. 3.28: $v_{dc\_N}$ [100V/DIV] without the proposed ac filter .....	74
Fig. 3.29: $v_{dc\_N}$ [100V/DIV] with the proposed ac filter .....	74
Fig. 3.30: $I_c$ that flows through the split dc-link capacitors. $I_c$ (blue) [2A/DIV], $V_{ac}$ (green) [500V/DIV].....	75
Fig. 3.31: Spectrum of $v_{dc\_N}$ with (red) and without (blue) the proposed ac filter structure. ....	75
Fig. 3.32: Full-bridge inverter connected to single-phase system with asymmetrical grounding scheme.....	76
Fig. 3.33: CM voltage of negative dc-rail $v_{dc\_N}$ in simulation using the proposed full-bridge topology under asymmetrical ac ground scheme.....	77
Fig. 3.34: Proposed ac filter for dc leakage current reduction without split dc-link capacitor. ....	77
Fig. 3.35: CM voltage of negative dc-rail $v_{dc\_N}$ (purple) [100V/DIV] and ac current $I_{ac}$ (blue) [50A/DIV] using the proposed full-bridge topology under asymmetrical ac ground scheme.....	78
Fig. 3.36: Two-level three-phase voltage source converter.....	78
Fig. 3.37: CM equivalent circuit of the three-phase ECC.....	78
Fig. 3.38: Continuous SVM (SVPWM) .....	79
Fig. 3.39: Discontinuous SVM (DPWM).....	79
Fig. 3.40: Negative dc-rail CM voltage $v_{dc\_N}$ of three-phase ECC converter.....	80
Fig. 3.41: Three-phase ECC Converter with the proposed filter structure. ....	80
Fig. 3.42: CM equivalent circuit with the modified ac filter. ....	81
Fig. 3.43: Negative dc-rail CM voltage $v_{dc\_N}$ [250V/DIV] with the modified ac filter structure using DPWM modulation.....	82

Fig. 3.44: Negative dc-rail CM voltage $v_{dc\_N}$ [250V/DIV] with the modified ac filter structure using carrier-based without CM injection modulation.....	82
Fig. 3.45: Proposed low-frequency dc CM voltage modulation scheme and controller .....	84
Fig. 3.46: State feedback control block diagram .....	86
Fig. 3.47: Transient period simulation waveform of $v_{dc\_N}$ when the CM controller is initiated, $v_{dc\_N}$ (orange) [25V/DIV], $d_{CM}$ (blue) [50m/DIV].....	87
Fig. 3.48: $v_{dc\_N}$ (magenta) [25V/DIV] without the proposed controller.....	87
Fig. 3.49: $v_{dc\_N}$ (magenta) [25V/DIV] with the proposed controller.....	87
Fig. 3.50: Volt-second generated by CM terminal voltage.....	87
Fig. 3.51: $V_{CM}$ when ac current is zero-crossing.....	89
Fig. 3.52: $V_{CM}$ when dc-link voltage reaches the peak value.....	89
Fig. 3.53: Designed CM choke with air gap.....	90
Fig. 3.54: Impedance measurement of fabricated $L_{CM}$ .....	91
Fig. 3.55: Grid-connected ac power regulation without the proposed CM voltage control. Negative dc-rail CM voltage $v_{dc\_N}$ (green) [50V/DIV], Grid voltage $V_{ac}$ (orange) [500V/DIV], Ac current $I_{ac}$ (blue) [50A/DIV].....	92
Fig. 3.56: Grid-connected ac power regulation with the proposed CM voltage control. Negative dc-rail CM voltage $v_{dc\_N}$ (green) [50V/DIV], Grid voltage $V_{ac}$ (orange) [500V/DIV], Ac current $I_{ac}$ (blue) [50A/DIV].	92
Fig. 3.57: Positive and Negative dc-rail CM voltage of 380 V dc-bus [100V/DIV] without the proposed active controller.....	92
Fig. 3.58: Positive and Negative dc-rail CM voltage of 380 V dc-bus [100V/DIV] with the proposed active controller .....	92
Fig. 3.59: Current flowing into the mid-point of dc-link $i_c$ (blue) [2A/DIV], Grid voltage $V_{ac}$ (green) [500V/DIV].....	93
Fig. 3.60: Negative dc-rail CM voltage under balanced input condition. Top waveforms show three-phase inductor current (upper waveform) [20A/DIV], and bottom waveform shows the negative dc-rail CM voltage $v_{dc\_N}$ [10V/DIV] .....	94
Fig. 3.61: Negative dc-rail CM voltage under unbalanced input condition. Top waveforms show three-phase input voltage (upper waveform) [100V/DIV], and bottom waveform shows the negative dc-rail CM voltage $v_{dc\_N}$ [25V/DIV] .....	94
Fig. 3.62: Open-loop PQ control with proposed CM voltage control.....	94
Fig. 3.63: Negative dc-rail CM voltage under balanced input condition with proposed control. Top waveforms show three-phase inductor current (upper waveform) [20A/DIV], and bottom waveform shows the negative dc-rail CM voltage $v_{dc\_N}$ [10V/DIV].....	95
Fig. 3.64: Negative dc-rail CM voltage under balanced input condition with proposed control. Top waveforms show three-phase input voltage (upper waveform) [100V/DIV], and bottom waveform shows the negative dc-rail CM voltage $v_{dc\_N}$ [25V/DIV].....	95

Fig. 3.65: Two-stage approach with both ac, dc CM decoupled operation; the first-stage can be either single or three-phase VSC.....	96
Fig. 3.66: A system with power electronics .....	96
Fig. 3.67: Ac-side EMI measurement in PFC system.....	97
Fig. 3.68: Dc-side EMI measurement in dc-fed motor drives .....	97
Fig. 3.69: Dc-side EMI measurement using one LISN in bus-interface bi-directional converter .....	98
Fig. 3.70: Dc-side EMI measurement using two LISNs in bus-interface bi-directional converter.....	98
Fig. 3.71: EMI filter in single-phase ECC converter.....	99
Fig. 3.72: CM equivalent circuit of voltage-source converter system .....	99
Fig. 3.73: CM equivalent circuit with DC and AC CM filter .....	99
Fig. 3.74: CM equivalent with a normal ac filter.....	101
Fig. 3.75: CM equivalent with a floating filter .....	101
Fig. 3.76: CM equivalent circuit with major components parasites .....	102
Fig. 3.77: Simulation results of in-circuit attenuation ( $i_{CM1}/v_{CM}$ ): purple waveform is $i_{CM1}/v_{CM}$ ; blue waveform is $i_{CM2}/v_{CM}$ .....	103
Fig. 3.78: Insertion gain ( $i_{CM1}/i_{CM2}$ ) achieved by the floating filter .....	103
Fig. 3.79: CM equivalent circuit by considering the stray capacitor between device and ground.....	103
Fig. 3.80: Simplified CM equivalent circuit by considering the stray capacitor between device and ground .....	104
Fig. 3.81: In-circuit attenuation of $i_{CM}$ : maroon color is result without $Z_s$ ; purple and blue plots are the results with (50 pF $Z_s$ 1 nF $Z_{dc_s}$ ) and (50 pF $Z_s$ 2 nF $Z_{dc_s}$ ), respectively .....	104
Fig. 3.82: Attenuation improvement by floating filter: maroon color is result without $Z_s$ ; purple and blue plots are the results with (50 pF $Z_s$ 1 nF $Z_{dc_s}$ ) and (50 pF $Z_s$ 2 nF $Z_{dc_s}$ ), respectively .....	104
Fig. 3.83: CM equivalent circuit for dc-side CM noise measurement.....	105
Fig. 3.84: In-circuit attenuation of CM noise ( $i_{CM}/v_{CM}$ ) with (purple) and without (blue) the floating filter .....	106
Fig. 3.85: EMI measurement setup.....	106
Fig. 3.86: Ac-side CM noise measurement with (red) and without (blue) the floating filter when heatsink is floated.....	107
Fig. 3.87: Ac-side CM noise measurement with (red) and without (blue) the floating filter when heatsink is grounded.....	107
Fig. 3.88: Ac-side CM noise measurement results with floating filter (grey) and result by adding additional 1.5 nF grounding capacitor on dc-link (black) .....	108
Fig. 3.89: AC-side converter filter structure.....	108
Fig. 3.90: AC-side total EMI noise measurement .....	109
Fig. 3.91: Dc-side converter filter structure.....	110
Fig. 3.92: Terminal voltage noise of the second-stage converter, $V_{oDM}$ .....	111

Fig. 3.93: Converter output impedance with (purple) and without (blue) the damping resistor.....	111
Fig. 3.94: Dc-side CM EMI noise with (black) and without (grey) the floating filter.....	112
Fig. 3.95: Dc-side total EMI noise measurement result.....	112
Fig. 3.96: Ac-dc bus-interface bi-directional converter system.....	113
Fig. 3.97: Physical layout and the major components of the converter.....	113
Fig. 3.98: Complete diagram of a single-phase ac-dc bus-interface bi-directional converter system.....	114
Fig. 4.1: Typical PLL structure.....	117
Fig. 4.2: ZCD Time Delay.....	118
Fig. 4.3: Generic structure of single-phase DQ frame PLL.....	119
Fig. 4.4: Typical mixer PD type single-phase PLL (T-PD PLL).....	119
Fig. 4.5: Output of T-PD PLL when input voltage drops from 240 Vrms to 120 Vrms.....	120
Fig. 4.6: Modified mixer PD type single-phase PLL (M-PD PLL).....	120
Fig. 4.7: Output of M-PD PLL when input voltage drops from 240 V rms to 120 V rms.....	121
Fig. 4.8: Proposed single-phase PLL with peak voltage detection.....	122
Fig. 4.9: Normalization of the proposed single-phase PLL.....	123
Fig. 4.10: Output of proposed PLL when input voltage drops from 240 Vrms to 120 Vrms.....	124
Fig. 4.11: Phase feedback model for PLL system.....	125
Fig. 4.12: Frequency feedback model for PLL system.....	125
Fig. 4.13: State-feedback model for peak voltage detection loop.....	126
Fig. 4.14: Bode-plot of compensated voltage loop open-loop gain.....	127
Fig. 4.15: One rad phase jump response of the proposed PLL (grey) and the mathematics model (black).....	128
Fig. 4.16: 1 Hz step response of the proposed PLL (grey) and the mathematics model (black).....	128
Fig. 4.17: 240 V rms to 120 V rms step response of the peak voltage detection loop (black) and the closed-loop model (grey).....	128
Fig. 4.18: Proposed PLL with dc-offset rejection.....	129
Fig. 4.19: PLL comparison between proposed PLL with (black), and without (grey) dc-offset rejection with 1% dc-offset.....	130
Fig. 4.20: Output of M-PD PLL (grey) and P-PD PLL (black) under the 5% third harmonics injection.....	131
Fig. 4.21: P-PD PLL peak voltage $V_{pk}$ with the 5% third harmonics injection.....	131
Fig. 4.22: Full-bridge converter with ac current control and PLL.....	132
Fig. 4.23: Proposed PLL frequency output $\omega_C$ [3Hz/DIV] and peak voltage output $V_{pk}$ [150V/DIV] with 50% input voltage $V_{grid}$ sag [500V/DIV].....	133
Fig. 4.24: Proposed PLL and M-PD PLL frequency output $\omega_C$ with 50% input voltage $V_{grid}$ sag [200V/DIV].....	133
Fig. 4.25: Proposed PLL and T-PD PLL frequency output $\omega_C$ with 50% input voltage $V_{grid}$ sag [200V/DIV].....	133

Fig. 4.26: 1 Hz step response of the proposed PLL output frequency $\omega_c$ [1.5Hz/DIV] and the input voltage $V_{grid}$ [500V/DIV] .....	134
Fig. 4.27: One rad phase jump response of the proposed PLL output frequency $\omega_c$ [3Hz/DIV] and the input voltage $V_{grid}$ [500V/DIV] .....	134
Fig. 4.28: Output ripple of T-PD PLL [1.5Hz/DIV] and M-PD PLL [1.5Hz/DIV] under 70% clipped sinusoid input $V_{grid}$ [500V/DIV] .....	134
Fig. 4.29: Output ripple of M-PD PLL [1.5Hz/DIV] and the proposed PLL [1.5Hz/DIV] under 70% clipped sinusoid input $V_{grid}$ [500V/DIV] .....	134
Fig. 4.30: Three-phase grid-interface converter system with PLL .....	137
Fig. 4.31: Positive sequence detection (PSD) block .....	137
Fig. 4.32: Synchronous reference frame PLL .....	138
Fig. 4.33: Linearized PLL model .....	138
Fig. 4.34: One-line circuit of the converter system .....	139
Fig. 4.35: System when only grid is considered .....	140
Fig. 4.36: System when only converter is considered .....	140
Fig. 4.37: System when effects of the grid and converter are considered .....	140
Fig. 4.38: PLL system by considering system operation .....	141
Fig. 4.39: Proposed quasi-static PLL model .....	142
Fig. 4.40: Trigonometric PD output .....	144
Fig. 4.41: Switching converter simulation results $\omega_c$ (purple) [5 Hz/DIV], one phase current $i_a$ (blue) [25A/DIV], and proposed PLL model output $\omega_c$ (dark blue) .....	145
Fig. 4.42: Switching converter simulation results $\omega_c$ (purple) [5 Hz/DIV], one phase current $i_a$ (blue) [25A/DIV], and proposed PLL model output $\omega_c$ (dark blue) .....	145
Fig. 4.43: One-line circuit with multiple shunt and series impedance .....	146
Fig. 4.44: One-line circuit with only the equivalent grid-input impedance .....	146
Fig. 4.45: Simplified PLL model considering converter interaction with utility .....	146
Fig. 4.46: Open circuit .....	147
Fig. 4.47: Circuit with resistor 1 .....	147
Fig. 4.48: Circuit with resistor 2 .....	147
Fig. 4.49: Two-level three-phase voltage source converter system .....	148
Fig. 4.50: PLL behavior under the capacitive local-load condition: $\omega_c/2\pi$ (purple) [6 Hz/DIV], one-phase voltage $v_{ga}$ (green) [100V/DIV] .....	150
Fig. 4.51: Simulation of PLL output behavior when grid steps from stiff to weak condition under capacitive load in simulation. $\omega_c/2\pi$ (purple) [5 Hz/DIV], one phase-voltage $v_{ga}$ (green) [50/DIV] .....	150
Fig. 4.52: PLL behavior under inductive local load condition: $\omega_c/2\pi$ (green) [5 Hz/DIV], one-phase voltage $v_{ga}$ (purple) [100V/DIV] .....	151



Fig. 4.53: Simulation of PLL output behavior when grid steps from stiff to weak condition under inductive load in simulation. $\omega_c/2\pi$ (green) [5 Hz/DIV], one phase-voltage $v_{ga}$ (purple) [50/DIV] .....	151
Fig. 4.54: PLL output behavior when grid steps from stiff to weak condition under inductive load. $\omega_c$ (purple) [2.5 Hz/DIV], one phase-voltage $v_{ga}$ (brown) [100/DIV] .....	152
Fig. 4.55: PLL behavior under resistive local load condition. $\omega_c/2\pi$ (purple) [5 Hz/DIV], one-phase voltage $v_{ga}$ (orange) [100V/DIV] .....	152
Fig. 4.56: PLL model under stiff grid-connected condition .....	154
Fig. 4.57: PLL model under islanded condition .....	155
Fig. 4.58: $R_L, C_L, L_L$ in parallel as the local load .....	155
Fig. 4.59: 3-D figure of $K_2$ in terms of $\omega_c$ and $Q$ .....	157
Fig. 4.60: 2-D figure of $K_2$ in terms of $\omega_c$ and $Q$ .....	157
Fig. 4.61: 3-D figure of $\varphi_2$ in terms of $\omega_c$ and $Q$ .....	158
Fig. 4.62: 2-D figure of $\varphi_2$ in terms of $\omega_c$ and $Q$ .....	158
Fig. 4.63: PLL output under islanded condition with $//R_L C_L$ load. One phase voltage and current, $v_{Ca}$ (maroon) [50V/DIV], $i_a$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (magenta) [1Hz/DIV] .....	159
Fig. 4.64: PLL output under islanded condition with $//R_L L_L$ load. One phase voltage and current, $v_{Ca}$ (maroon) [50V/DIV], $i_a$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (magenta) [5Hz/DIV] .....	160
Fig. 4.65: PLL output under islanded condition with $//R_L L_L C_L$ load. One phase voltage and current, $v_{Ca}$ (maroon) [50V/DIV], $i_a$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (magenta) [0.5Hz/DIV] .....	160
Fig. 4.66: PLL when considering the delay effect .....	161
Fig. 4.67: Average model simulation results of PLL output with digital delay under $//R_L C_L L_L$ load with 60 Hz resonant frequency. $\omega_c$ (blue) [0.5 Hz/DIV] without delay, $\omega_c$ (green) [0.5 Hz/DIV] with 25 $\mu$ s delay, $\omega_c$ (red) [0.5 Hz/DIV] with 50 $\mu$ s delay .....	162
Fig. 4.68: PLL model under purely resistive load at islanded condition .....	163
Fig. 4.69: 5 kW three-phase PWM converter test bed .....	164
Fig. 4.70: Three-phase loads for test .....	164
Fig. 4.71: Three-phase relay used as the PCC switch .....	164
Fig. 4.72: PLL output under $//R_L C_L$ load condition: phase voltage: $v_{Ca}$ (maroon) [100V/DIV], $\omega_c$ (purple) [2.5Hz/DIV] .....	165
Fig. 4.73: PLL output under $//R_L C_L$ load condition in simulation: phase voltage $v_{Ca}$ (green) [100V/DIV], $\omega_c$ (purple) [5Hz/DIV] .....	165
Fig. 4.74: PLL output under $//R_L L_L$ load condition: phase voltage: $v_{Ca}$ (purple) [100V/DIV], $\omega_c$ (green) [5Hz/DIV] .....	166
Fig. 4.75: PLL output under $//R_L L_L$ load condition in simulation: phase voltage: $v_{Ca}$ (purple) [100V/DIV], $\omega_c$ (green) [5Hz/DIV] .....	166
Fig. 4.76: PLL output under $//R_L C_L L_L$ load condition: phase voltage: $v_a$ (maroon) [100V/DIV], $\omega_c$ (purple) [5Hz/DIV] .....	167

Fig. 4.77: Small-signal PLL model under pure resistor load at islanded condition.....	168
Fig. 4.78: Small-signal gain of the sinusoidal function .....	169
Fig. 4.79: Proposed low-frequency small-signal PLL model .....	169
Fig. 4.80: Simulation verification of grid synchronization small-signal model at weak grid.....	170
Fig. 4.81: Steady-state operation of converter at weak grid .....	171
Fig. 4.82: Comparison between the measurement result (blue) and the model (red) .....	172
Fig. 4.83: Low-frequency small-signal PLL model at the islanded condition.....	173
Fig. 4.84: Illustration of mall-signal measurement.....	174
Fig. 4.85: Comparison between the measurement result (blue) and the model (red) .....	174
Fig. 4.86: Impedance of a $//RLC$ linear-load .....	175
Fig. 4.87: Impedance of a series $RLC$ load.....	175
Fig. 4.88: Impedance of a pure resistor load.....	176
Fig. 4.89: Impedance of a pure capacitor load.....	176
Fig. 4.90: Impedance of a pure inductor load.....	176
Fig. 4.91: Two bi-directional ac-dc bus-interface converters in system.....	178
Fig. 4.92: Two PLLs' unstable output with two bus-interface converters: $\omega_{C1}/2\pi$ (green), $\omega_{C2}/2\pi$ (magenta) [2 Hz/DIV], $I_{Ca1}$ (green), $I_{Ca2}$ (magenta) [100 A/DIV] .....	179
Fig. 4.93: Two PLLs are fully coupled together at a purely resistive load islanded condition.....	179
Fig. 4.94: Two PLLs are fully coupled together under $//RLC$ load islanded condition .....	180
Fig. 4.95: Simplified PLL loop under $//RLC$ load islanded condition .....	180
Fig. 4.96: Illustration of mall-signal measurement at two-converter case with $//RLC$ load at the islanded condition.....	182
Fig. 4.97: Comparison between the measurement result (blue) and the model (red). .....	182
Fig. 4.98: PLL output for case 1 .....	183
Fig. 4.99: PLL output for case 2.....	183
Fig. 4.100: PLL output for case 3 .....	183
Fig. 4.101: PLL output for case 4.....	183
Fig. 4.102: PLL1 loop for a three-converter case.....	184
Fig. 4.103: Simplified PLL1 loop for a three-converter case .....	184
Fig. 4.104: Signal-flow-graph (SFG) representation of PLL1 loop.....	184
Fig. 4.105: SFG representation of PLL loop in three-converter case .....	185
Fig. 4.106: SFG representation of PLL loop in four-converter case.....	185
Fig. 4.107: An example of future local distribution generation system.....	187
Fig. 4.108: Two converters' unstable output frequency at the weak grid condition.....	188
Fig. 4.109: Small-signal model of PLL in two-converter case at the weak grid condition.....	189
Fig. 4.110: SFG representation of PLL loops in two-converter at the weak grid condition .....	190
Fig. 4.111: Illustration of mall-signal measurement at two-converter case with $//RC$ load.....	191

Fig. 4.112: Comparison between the measurement result (blue) and the model (red) .....	191
Fig. 4.113: SFG representation of PLL loops in a three-converter system at the weak grid condition .....	192
Fig. 4.114: SFG representation of PLL loops in a four-converter system at the weak grid condition.....	192
Fig. 4.115: PLL1 output for case 1 .....	193
Fig. 4.116: PLL output for case 2 .....	193
Fig. 4.117: The future local distribution generation system with ECC .....	194
Fig. 5.1: The first proposed PLL for anti-islanding detection .....	200
Fig. 5.2: Model of the first proposed PLL .....	200
Fig. 5.3: Model of the first proposed PLL under islanded condition.....	201
Fig. 5.4: The first proposed PLL output behavior when the islanding condition occurs: $k_{fb}$ (green), $\omega_c$ (red) .....	201
Fig. 5.5: Simulation results of the first proposed PLL output when islanding occurs: signal $k_{fb} * \omega_c$ (orange) [0.1 rad/DIV], $\omega_c/2\pi$ (magenta) [2 Hz/DIV].....	202
Fig. 5.6: Low-voltage ride-through (LVRT) test principle.....	203
Fig. 5.7: One-line circuit to generate a low voltage.....	203
Fig. 5.8: PLL output under low-voltage conditions.....	204
Fig. 5.9: The first proposed PLL model under the stiff-grid-connected condition .....	205
Fig. 5.10: Normalized natural frequency $\omega_{nM}/\omega_n$ of the proposed PLL.....	205
Fig. 5.11: Normalized damping factor $\zeta_M/\zeta$ of the proposed PLL .....	205
Fig. 5.12: 2 Hz step response of the first proposed PLL (grey) [0.5 Hz/DIV] and the typical PLL (red) [0.5 Hz/DIV].....	206
Fig. 5.13: The second proposed PLL for islanding detection .....	206
Fig. 5.14: Model of the second proposed PLL at the stiff-grid-tied condition .....	207
Fig. 5.15: Model of the second proposed PLL at the islanded condition .....	207
Fig. 5.16: Second proposed PLL output behavior at the islanded condition by using variable delay block.....	207
Fig. 5.17: Proposed PLL steady-state output under the grid-tied mode .....	208
Fig. 5.18: The typical PLL output under $//RLC$ load with 60 Hz resonant frequency when islanding occurs: $\omega_c/2\pi$ (purple) [5Hz/DIV], $v_{Ca}$ (orange) [100V/DIV] .....	209
Fig. 5.19: The first proposed PLL output under $//RLC$ load with 60 Hz resonant frequency when islanding occurs: $\omega_c/2\pi$ (purple) [5Hz/DIV], $v_{Ca}$ (orange) [100V/DIV].....	209
Fig. 5.20: The third proposed PLL for islanding detection.....	211
Fig. 5.21: Small-signal model of the third proposed PLL for islanding detection.....	211
Fig. 5.22: The third PLL output under the islanded condition when the initial condition is positive.....	212
Fig. 5.23: The third PLL output under the islanded condition when the initial condition is negative .....	212
Fig. 5.24: Small-signal model of the third proposed PLL at the stiff-grid-tied mode .....	213
Fig. 5.25: Normalized natural frequency $\omega_{nM}/\omega_n$ of the third proposed PLL .....	214
Fig. 5.26: Pole location of the third proposed PLL in terms of $N$ at the stiff-grid-tied mode.....	214

Fig. 5.27: The third proposed PLL steady-state results under two different $N$ values: $\omega_c/2\pi$ with $N = 0$ (red) [1 Hz/DIV], $\omega_c/2\pi$ with $N > 1/K_p$ (green) [1 Hz/DIV] .....	215
Fig. 5.28: The third proposed PLL dynamics response under 2 Hz input step with 1% 600 Hz grid voltage harmonics: $\omega_c/2\pi$ with $N = 0$ (red) [1 Hz/DIV], $\omega_c/2\pi$ with $N = 0.01$ (green) [1 Hz/DIV] .....	215
Fig. 5.29: Typical PLL output when islanding condition occurs with $//R_L L_L C_L$ load. One phase voltage and current, $v_{ga}$ (orange) [100V/DIV], $i_{Ca}$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (green) [1Hz/DIV] .....	216
Fig. 5.30: Third proposed PLL output when islanding condition occurs with $//R_L L_L C_L$ load. One phase voltage and current, $v_{ga}$ (orange) [50V/DIV], $i_{Ca}$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (green) [1Hz/DIV] .....	216
Fig. 5.31: Typical PLL output when islanding condition occurs with $R_L$ load. One phase voltage and current, $v_{ga}$ (orange) [50V/DIV], $i_{Ca}$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (green) [1Hz/DIV].....	217
Fig. 5.32: Proposed third PLL output when islanding condition occurs with $R_L$ load. One phase voltage and current, $v_{ga}$ (orange) [50V/DIV], $i_{Ca}$ (blue) [50A/DIV], PLL output $\omega_c/2\pi$ (green) [1Hz/DIV] .....	217
Fig. 5.33: The fourth proposed PLL system for islanding detection .....	218
Fig. 5.34: Two Hz step responses of the fourth proposed PLL $\omega_c/2\pi$ (red) [1 Hz/DIV] and the typical PLL $\omega_c/2\pi$ (blue) [1 Hz/DIV] .....	219
Fig. 5.35: The fifth proposed (mixed-type) PLL system .....	219
Fig. 5.36: Comparison of the fourth PLL $\omega_c/2\pi$ (blue) [1 Hz/DIV] and the mixed-type PLL $\omega_c/2\pi$ (red) [1 Hz/DIV].....	220
Fig. 5.37: The typical PLL output when the islanding event occurs: $v_{Ca}$ (purple) [100 V/DIV], $i_{Ca}$ (blue) [20 A/DIV], $\omega_c$ (green) [6 Hz/DIV] .....	222
Fig. 5.38: Modified PLL output when the islanding event occurs: $v_{Ca}$ (purple) [100 V/DIV], $i_{Ca}$ (blue) [20 A/DIV], $\omega_c$ (green) [6 Hz/DIV] .....	222
Fig. 5.39: Two bus-interface converters implemented with anti-islanding protection are tied to ac grid....	224
Fig. 5.40: The fastest RPH pole of PLLs with two converters .....	225
Fig. 5.41: Comparison of No. 1 PLL output for islanding detection between single converter $\omega_c$ (blue) [0.1 Hz/DIV] and two converters conditions $\omega_c$ (green) [0.1 Hz/DIV].....	226
Fig. 5.42: The fastest RPH pole of PLLs at two converter condition .....	227
Fig. A.1: Dc-link voltage and delivered ac power waveform.....	233
Fig. A.2: Inverter block used in system simulation to study the frequency behavior .....	234
Fig. A.3: Inside of the inverter block.....	234
Fig. A.4: Inside of the current source block .....	234

## List of Tables

Table 1.1: Organizations that work on dc system standards.....	11
Table 2.1: Operations specifications for the full-bridge topology for the dc nano-grid .....	32
Table 2.2: Main volume comparison between two-stage topology and full-bridge where $f_s = 20$ kHz .....	48
Table 3.1: Maximum harmonic current distortion in percent of current .....	56
Table 3.2: Full-bridge converter system specifications .....	71
Table 3.3: Designed ac filter values .....	72
Table 3.4: Leakage current comparison.....	75
Table 3.5: Filter value for three-phase first-stage ECC converter .....	81
Table 3.6: Filter value for three-phase first-stage ECC converter .....	82
Table 3.7: Lumped components in simulation.....	102
Table 3.8: Ac passive filter value .....	108
Table 3.9: Dc passive filter value .....	110
Table 4.1: PLL parameters .....	127
Table 4.2: System parameters.....	132
Table 4.3: Parameters used for simulation .....	144
Table 4.4: Parameters used in experiments.....	149
Table 4.5: Parameters in simulation .....	159
Table 4.6: Comparison between simulation and prediction of $\Delta\omega_C$ .....	161
Table 4.7: Parameters in simulation .....	162
Table 4.8: Parameters for Test (per phase).....	163
Table 4.9: Simulation Parameters for two bus-interface converters.....	178
Table 4.10: Simulation parameters for two bus-interface converters with $//RLC$ load.....	181
Table 4.11: Four examples for two-converters under $//RLC$ islanded condition .....	182
Table 4.12: Simulation parameters for two bus-interface converters .....	187
Table 4.13: Two examples for two-converters at the weak grid condition.....	193
Table 5.1: Interconnection system response to abnormal voltages.....	197
Table 5.2: Interconnection system response to abnormal frequencies.....	197
Table 5.3: Simulation parameters for islanding detection .....	202
Table 5.4: Parameters in simulation .....	215
Table 5.5: Comparison of different islanding-detection methods .....	220
Table 5.6: Parameters for islanding-detection test.....	221
Table 5.7: Simulation parameters for two-converter condition .....	224
Table 5.8: RHP pole locations for two converters.....	224
Table A.1: Controller parameters .....	232

## **Chapter 1. INTRODUCTION**

This chapter presents the motivations and objectives of this work. It describes the state of the art of electric power systems, advances in dc distribution/transmission systems and smart grids, and the roles and challenges of power electronics in this field. A review of the power converter system in the electric power system is provided, with a special attention paid to the residential low-voltage distribution systems. Challenges in the field and a literature review are also provided, followed by the dissertation outline and the scope of research.

### **1.1. BACKGROUND**

#### **1.1.1. ELECTRICAL ENERGY**

A continuous growing energy demand all over the globe along with the economic growth requires human society's great effort to address enormous challenges in energy areas.

Fossil fuels, such as coal, natural gas, and petroleum, are still the dominant energy resource, which, however, are not a simple and cheap way to use directly. Thus, it is necessary to find a clean and efficient solution to convert these prime energies so that the emerging concerns over the issues of climate change, carbon dioxide emissions, and environmental pollution are also handled. Though not the best option in terms of energy density, electrical energy is a much cleaner, more cost-effective and safer form to transmit and consume. It is becoming a conventional wisdom to expect that massively increased utilization of electricity in the energy production, transfer, and consumption will provide the necessary means for a sustainable future.

As of 2009, more than 40.7% of energy was delivered in the form of electricity, and most of it is consumed in residential/commercial applications. As the electricity cost per watt is decreasing and the performance of electrical/electronic equipment is improving, it becomes a consensus that more energy are and will be consumed in the electric form almost everywhere, including in the industrial and transportation fields.

### 1.1.2. ELECTRIC POWER SYSTEM

An electric power system (EPS) is a network of electrical components used to supply, transmit and use electric power, which can be divided into the categories of power generation, power transmission, power distribution, and power consumption, as illustrated in Fig. 1.1. Small-scale power systems are also found in transportations, where their structure mainly consists of power generation and power distribution.

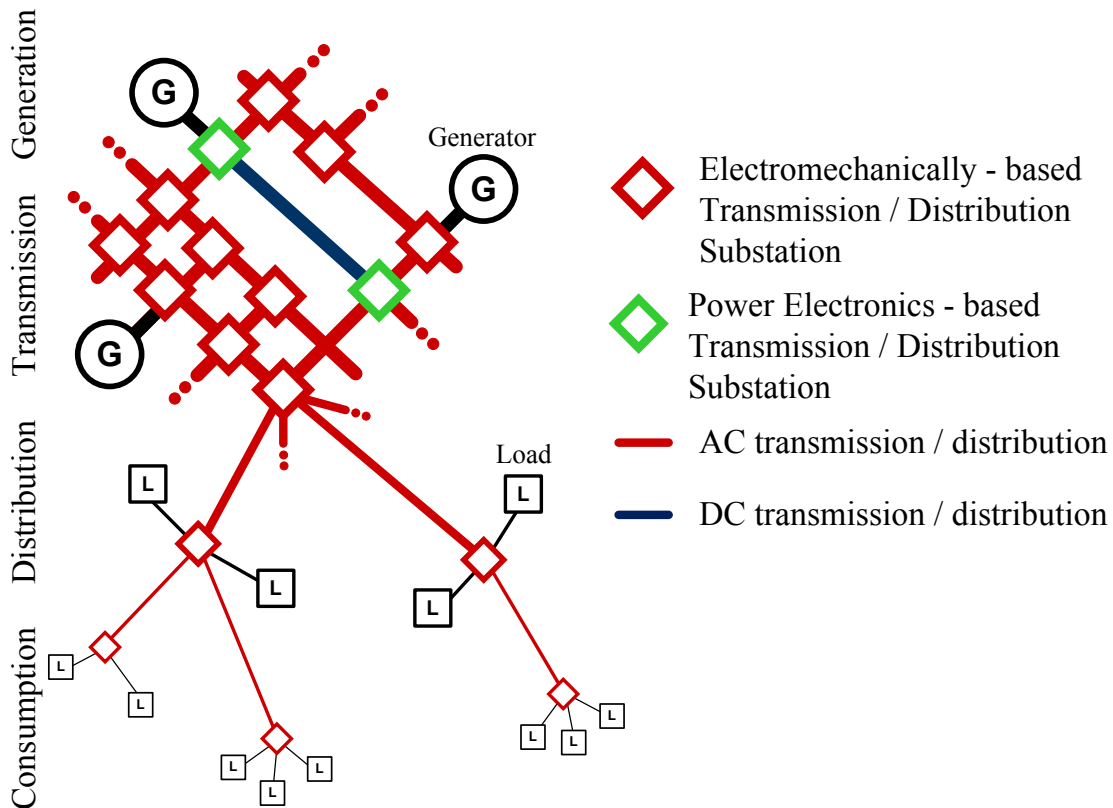


Fig. 1.1: Illustration of electric power system

The large-region EPS is the most sophisticated system ever built by humankind, and involves hundreds of different components and pieces of equipment during operation. The major components in a conventional EPS are described below.

The majority of electric power still comes from rotating power generators, which are driven by steam/gas turbines, or combustion/jet engines in transportation EPSs. All generators in a single system rotate synchronously and will target a set frequency using frequency droop control.

Power systems deliver energy to loads that perform a function. These loads range from household appliances to industrial machinery. Most loads expect a certain voltage and, for alternating current devices, a certain frequency and number of phases. At any time, the net amount of power consumed by the loads on a power system equals the net amount of power produced by the supplies minus the power lost in transmission.

Power systems contain protective devices to prevent injury or damage during failures. In modern systems, miniature circuit breakers and protective relays are typically used, which can detect a fault and initiate a trip. Switchgear in substations is another main component to interrupt short-circuit and overload fault currents while maintaining service to unaffected circuits. Switchgears provide isolation of circuits from power supplies, and are also used to enhance system availability by allowing more than one source to feed a load.

In large electric power systems, supervisory control and data acquisition (SCADA) is used for tasks such as switching on generators, controlling generator output, and switching in or out system elements, such as switchgears, for maintenance. SCADA systems are much more sophisticated than previous forms of system control.

### **1.1.3. TECHNOLOGY TREND IN EPS**

#### **1.1.3.1. More Distributed Power Generation**

In recent years, leaders in industry, government, and academia have recognized the need and importance for an energy market that consists of a diversity of power generation sources and efficient delivery mechanisms. Just as diversified generation helps to ensure the security and independence of the American energy supply, diversified transmission technology helps to ensure the optimal, safe, and reliable delivery of electric power to end users. Renewable energy, a major contributor to the distributed generation, has become a significant presence in the energy market. Renewable energy comes from natural resources such as sunlight, wind, rain, tides, and geothermal heat, just to name a few.

In 2008, about 19% of global final energy consumption came from renewables, with 13% coming from traditional biomass and 3.2% from hydroelectricity [1]. New renewables, such as solar, wind, geothermal, and biofuel, accounted for another 2.7% and



are growing rapidly [2]. The share of renewable sources in electricity generation is around 18%, with 3% coming from new renewables [2]. In the U.S., renewable sources provided about 8% of total energy in 2010. Between 2009 and 2010, renewable energy consumption rose by 6 % [3].

Photovoltaic (PV) cells convert sunlight directly into electricity, and they are the fastest growing type of renewable energy, increasing at 50 percent a year [4]. At the end of 2009, cumulative global photovoltaic (PV) installations surpassed 21 gigawatts (GW) [5].

Most modern wind power is generated in the form of electricity by converting the rotation of turbine blades into electrical currents by means of an electrical generator. Wind power is growing at a rate of 30% annually, with a worldwide installed capacity of 197 GW in 2010, and is widely deployed in Europe, Asia, and the United States [6]. Several countries have achieved relatively high levels of wind power penetration, such as Denmark's 21% of stationary electricity production [6].

#### **1.1.3.2. More Electronic Controlled Equipment**

Power electronics is growing rapidly in residential and commercial areas. Most contemporary appliances are electronic loads. The lighting, heating and cooling sector will follow the same trend and will be controlled more and more by power converters [7].

Power electronics are penetrating rapidly in the industry/automation and transportation sectors dominated by traditional mechanical-controlled equipment [8-10].

On the other side, more energy will be supplied by electronic sources. Most renewable energies and energy storages, such as batteries and superconducting magnetic energy storage (SMES), are managed by power electronics equipment in the way that EPS and energy storage devices prefer [9, 10].

Lots of electronic equipment are deployed to help power transmission for better power quality and reliability. Many examples can be found in the development of flexible alternative current transmission system (FACTS) and high-voltage direct current (HVDC) transmission systems [11].

It is seen that more high-efficiency and high-reliability power electronics equipment will take on more roles throughout the chain of the electric power system and shape the way we control electrical energies.

### **1.1.3.3. More Dc-based Power System**

Dc transmission is a favorable way of increasing transmission efficiency, improving controllability, and reducing footprint and cost over long-distance. High-voltage dc transmission (HVDC) technologies have demonstrated their advantages in many countries. HVDC can provide fast voltage support, fast power flow control, reactive power compensation, and dynamic congestion management [12].

Dc distribution is also believed to be a promising and simple solution to integrate distribution generation and energy storage devices as well as manage the power consumption and utilization among multiples electronic loads [13, 14]; thereby eliminating redundant components and improving the system efficiency. Compared to its ac counterpart, stability criteria in the dc system is clearer, and the dc-dc converter is more reliable and efficient than the ac-dc converter.

The fast growing of dc power technology recalls the historical debate between Thomas Edison and Nicola Tesla about the “AC vs. DC”. Most likely both of their opinions are right. The future grid is envisioned to be a mixed-type grid infrastructure with both dc and ac power systems [15].

### **1.1.3.4. Smart Grid**

A smart grid is a type of electrical grid which attempts to predict and intelligently respond to the behavior and actions of all electric power users connected to it - suppliers, consumers and those that do both – in order to efficiently deliver reliable, economic, and sustainable electricity services [16].

A smart grid is a very generic concept, and different people have different perspectives on it. In a broad sense, a smart grid is conceived of as employing products and services together with intelligent monitoring, control, communication, and self-healing technologies to eventually maintain a reliable and secure electricity infrastructure that can meet future demand growth and achieve each of the listed functions: 1. self-

healing; 2. consumer participation; 3. resist attack; 4. high-quality power; 5. accommodate generation options; 6. enable an electricity market; 7. optimize assets; 8. enable high penetration of intermittent generation sources.

In a narrow sense, smart grid literally implies using the state-of-art information technology to implement an on-time two-way data processing and communication layers on top of the power grid so that people are capable of accessing on-time data for better system control and energy utilizations.

## **1.2. DISSERTATION MOTIVATIONS AND OBJECTIVE**

### **1.2.1. CHALLENGES TO ELECTRIC POWER SYSTEM**

The Department of Energy's 2009 annual energy outlook highlights the expected energy growth in the U.S. By 2030, these projections estimate that domestic demand for electricity will increase by 26% [17]. The traditional power system is aging and inescapably facing not only an update of its infrastructure, but more likely a complete reconstruction in future. The statistics show an increase in grid outages and blackouts in the last 30 years. In addition, the grid's infrastructure is a global concern, since the majority of installed transmission and distribution equipment has experienced service duty in excess of 30 years. In the deregulated power system market environment, they operate close to their power transfer capabilities, significantly influencing stability.

Although the EPS involves many considerations other than technical problems; such as aspects of society, environment, and policy; it is expected to undergo a paradigm shift in system infrastructure to increase capacity, reliability and efficiency in near future. The following challenges would be part of the reason.

The EPS is inherently slow due to the fact that it is mechanically controlled. It cannot deal with the fast dynamics that renewable energy brings [15, 18]. The intermittent problem of distributed generation results in the variations in the voltage and power, such as voltage instability and flicker [5], which quickly cause the system to become unstable. When wind turbines are involved, this can also result in undesirable changes in operating frequencies and rotational speeds. The reactive power compensation increases in proportion to wind speed, which has a notable effect on voltage level. All of these variations have the potential to damage the quality and safety of the power being

transmitted to end users. For example, a transmission system fault may result in the loss of a power line, leading to tripping of wind turbine generators. The sudden loss in generation can be the start of a major cascading outage event propagating through the entire system network.

Moreover, the variable nature of renewable energy forms will require accurate forecasting of resource availability and intelligent decision-making of renewable energy dispatch for both operation and investment.

### **1.2.2. CHALLENGES OF BI-DIRECTIONAL POWER ELECTRONIC CONVERTERS IN POWER DISTRIBUTION SYSTEM**

The EPS still deploys the unidirectional transmission and distribution infrastructure—like a “star” — to feed the energy to end-users. With the growing penetration of distributed generation and energy storage, energy flows could be “bi-directional” on a bus feeder [15]. Future power systems will have more bi-directional systems interlinked to each other, which poses many challenges to the power flow control and estimation, planning of future generations, protection strategies, and transmission/distribution equipment [20].

A bus-interface bi-directional converter is required to process the bi-directional energy flow. It's been developed in emerging applications, such as the EV charger and utility-scale energy-storage, and the future trend is that more such converters will penetrate into various voltage/power rating power distribution system. Traditionally, the power electronics engineers focus more on the design for a specific load or source rather than considering the system requirement. The bus-interface bi-directional converter system however requires the power electronics engineers to step out of their familiar zone and embrace more challenges in the whole energy and system sector.

Therefore, many technology challenges lie in a highly reliable and efficient converter topology design and the advanced control architecture capable of adjusting the terminal characteristics and responding to diverse system dynamics as well. High-performance power filter and EMI filter solutions have to be designed together to reduce the switching actions' impact on the interconnected system. A cost-effective hierarchical design

methodology from the component level up to the system level is required to adapt to the continuous changes in energy sector.

### **1.2.3. CHALLENGES IN THE SYSTEM INTERFACE DESIGN**

A well-designed power converter doesn't ensure the reliable and safe operation with the existing ac grid and future dc grid. The power electronics operations have to fulfill lots of the dc and ac grid interface requirements, such as power quality and various grid codes.

In the ac system interface, over/under voltage and over/under frequency protections, harmonics level and islanding-detection are required for distribution level (< 10 MW) interface. However, low/high voltage and zero-voltage ride-through, fault ride-through, and frequency ride-through are mostly required in transmission level interface. Future grid codes will include flicker mitigation, unbalance compensation, voltage regulation, black-start, and various ancillary functions [21].

Specifically, the grid synchronization-one of the interface requirements-involves the secure operation of a power converter with the ac electric grid. Many of the existing system stability issues, such as reactive power oscillations [22], require the clear understanding of the power converter grid synchronization performance and its potential impact on the power system stability. In future more distributed generation smart grid, this issue would be more critical as lots of bus-interface converters operate together in the system and the frequency synchronization unit of each converter will "cross-talk" to each other.

All of these system interface requirements mean that power electronics engineers have to understand the power system operation principles and their needs. On the other hand, power system engineers have to know the operation functions of the power converters and be aware of the "the inside" in order to design and tackle the future system problems.

Therefore, the equipment suppliers and the system integrators must work closely together to define the future grid codes and provide proper solutions. There are many challenges in the power electronics fields to determine how to make the power

electronics equipment better fit its role in an EPS, and how to integrate the power electronics equipment into the EPS, or even reshape the grid.

This dissertation is focused on the bus-interface bi-directional power converter to address many of the above challenges. All research in this dissertation is based on the development of a dc/ac electronic distribution system interfaced by multiple renewable energy resources and energy storage devices in low-voltage distribution power system. Residential buildings and houses are the direct applications of this research, but the results and conclusions can be extended to a more generic condition for many grid-interface converters. The major research efforts include:

1. Investigation of power electronics-based distribution system architecture and its basic operation for residential applications.
2. Study of the design procedure and methodology of the ac-dc bus-interface power electronics converter.
3. Exploration of the power filter and the EMI filter design methodology to address system level interface for power quality consideration.
4. Modeling of grid synchronization behaviors to address frequency stability issue in the distributed system with multiple distributed generation units.
5. Investigation of islanding-detection algorithms suitable for the existing and future grid conditions.

### **1.3. LITERATURE REVIEW**

#### **1.3.1. RESIDENTIAL DC DISTRIBUTION SYSTEM**

There has been a broad range of discussion on the potential utilization of a dc distribution system in electric power systems in transportation, data centers, and residential buildings.

Much research [16, 17, 23-50] has been conducted on the dc distribution and ac/dc hybrid distribution system in residential and commercial areas. Basically, the system architectures are gaining consensus among researchers: one common dc bus connected by multiple power converters.

One of the major differences among the existing publications is the type of components which connect to the bus. Aside from the PV sub-system, energy storage, and loads, Reference [23] connects a permanent magnetic synchronous wind generator; Reference [25] includes a diesel generator on the ac side; Reference [25] has a flywheel on the bus; and Reference [47] ties a super capacitor on the dc-bus. The different components on the bus yield different system behaviors and operation strategies, which results in a lack of a generic system operation approach.

The dc bus voltage also differs greatly between existing publications, and includes 48V [18, 26], 240 V [34], 380V [18, 26, 29, 47], +170V [35], 318V [29], 400 V [48], 800 V [30], and 3500 V [23]. The voltage level is obtained based on different considerations or is randomly chosen. More recently, 380 V has become a well-accepted voltage-level in data center applications, and the use of 380 V is spreading out quickly in residential applications.

Another deviation among existing systems is how the energy storage device is connected to the system. References [27, 34, 39, 43] directly tie the battery to the dc-bus to sustain the dc-bus voltage and ensure the system stability. However, the bus-voltage changes with the state of the charge of the batteries, and the charging current quality cannot be well-regulated. A proper battery management and cell-equalization are hard to achieve as well. References [18, 26, 29, 47] tie the battery directly to the bus via a bi-directional charger/discharge to decouple the dynamics between the dc-bus and the battery. Various modes of operation can be applied to battery system while the dc system stability highly relies on a proper design. Reference [37] ties the battery system onto the intermediate dc-link between the ac/dc front-end converter and the voltage regulator to fulfill a dual-mode. However, the flexibility of the control strategy suffers.

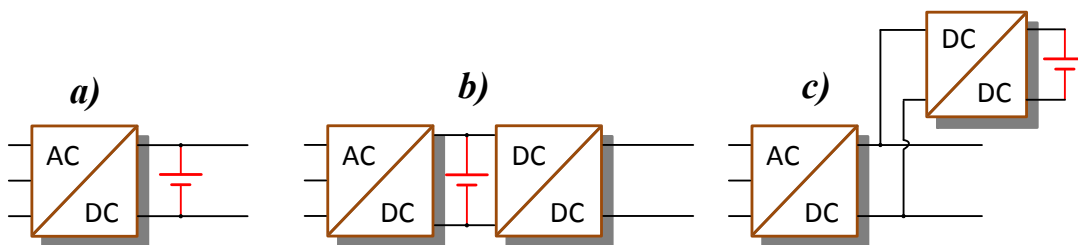


Fig. 1.2: Configurations of energy storage devices: a) directly tied to dc-bus, b) tied to intermediate dc-link, c) tied to dc-bus via charger.

A utility-interface converter is one of the key components in the system. It can be categorized into the unidirectional and bi-directional type. References [18 and 44] use a single-phase diode-bridge PFC circuit; references [47] uses a single-phase full-bridge in a single-phase ac/dc distribution system; reference [18 and 47] use a two-level three-phase voltage-source converter (VSC); references [30 and 35] use a three-level neutral-point-clamped topology; and references [17 and 44] use a three-phase VSC plus a buck converter to fulfill the control requirement.

Besides the system operation and architecture, much research is about efficiency comparison, protection, system grounding, and stability. Reference [28] compares the dc and ac appliances in term of power quality and efficiency, and concludes that the dc system is advantageous over the ac system. Protection designs are presented by using fuses [45], circuit-breakers [43], different self-configured protection devices [42], converters [49], and a combination of these [43]. A great deal of stability studies have been done on electronic dc distribution system over the past decades. However, few of them could systematically apply and verify the stability theorem to the whole system design, e.g., the design of converters and their components, cables, and locations. Up to now, few of these studies and solutions in publications have been accepted broadly.

Scholars and industry partners realize the need for standards to design such new dc systems. Thus, many organizations [51], as shown in Table 1.1, are working to accelerate the standardization process.

Table 1.1: Organizations that work on dc system standards

IEC	ATIS	Starlin3	EPRI
Emersion	Emerge Alliance	PSMA	Starline

In short, a generic system specification, definition of components, and function clarification are still not clear. And a dc distribution system design guideline is still missing from the literature. Thus, a generic dc distribution test-bed has to be built for the exploration of system operation, control strategy, bus-voltage level, protection, stability, etc., which can fit most of the residential/commercial applications.

### 1.3.2. BUS-INTERFACE BI-DIRECTIONAL CONVERTER



In the ac/dc distribution system, a bi-directional bus-interface converter is the crucial component in the system. There are many publications on power converter topologies in PV and wind systems, power factor correction (PFC) applications, and hundreds of topologies exist with the potential application for the bus-interface [52-59]. However, many of them are not suitable for bi-directional operation. Single-phase converter systems are mostly seen in PV applications. References [60 and 61] summarize different topologies. Many topologies, such as dual-bridge with resonant tank [62, 63] and dual-bridge without resonant tank [64-69], are proposed for isolated topologies. However, the isolated topologies still suffer from low efficiency and low reliability. Therefore, transformerless topologies [70-72] have become more attractive for bus-interface power converters. Soft-switching techniques are studied in grid-tied inverter application [73, 74], but they suffer from the additional cost and the limit of uni-directional operation. In single-phase applications, bulky dc-link capacitors pose a major problem, leading to more cost and lower power density, and many papers [75-77] propose different solutions to address the use of capacitors, such as using an active filter on the ac or dc side, multi-stage converters, and bus-conditioning.

For the high power applications, topologies would be more limited and don't have as many topologies as single-phase topologies. Two-level and three-level voltage-source converters, which are extensively used in three-phase motor drive applications, are demonstrated to be suitable for utility-interface applications. The group of four-leg converters [78] is seen in three-phase, four-wire systems to deal with unbalance condition. Many papers present a trade-off comparison between two-level converters and three-level converters in terms of efficiency, cost, reliability, etc. [79]. There have also been several soft-switched ac-dc converters [80] with potential for use in bi-directional applications presented over the past few decades.

However, a summarization of bi-directional converters from a system perspective has not been provided; the requirements are not quite clear to power electronics engineers for the application of an ac/dc distribution system where both sides of the converter are actually systems. Particularly in the single-phase system application, the impact of ripple power issues on the dc system is not quite understood. The bi-directional control system design in dc distribution systems is not well presented in existing literature.

### **1.3.3. POWER FILTER DESIGN FOR SYSTEM-INTERFACE**

In addition to low-order harmonics components, high-frequency noises also have a huge impact on system operation. In transformerless-based bus-interface converter systems, the dc-side bears large high-frequency CM voltage noises, which could easily induce a large leakage current, damage the equipment, and threaten human safety [81]. Many modified topologies [81-86] are found in the single-phase solar system application, using additional blocking or bypass active switches on the dc-rail or ac side. Reference [71] proposes to use NPC topology and a four-wire system in three-phase applications to deal with the leakage current issue. Some modified PWM schemes [87-90] are proposed to reduce the CM noises. However, the existing methods require large passive filter components, additional active devices, or the design of complicated control schemes. Also, none of the previous papers have noticed the dc-side low-frequency CM voltage ripple due to the ripple power and unbalanced ac-input. This CM voltage ripple however has to be considered due to the power quality requirement on dc-side.

EMI issues have gained more attention recently in commercial/residential applications [91-94]. For the converter system where both sides are bus systems, the EMI mitigation and filter design poses challenges for achieving high-density filters [95]. One of the reasons is that the existing EMI standard and measurement setup cannot be directly applied to a bi-directional converter system as either-side could be a source or load. Although the discussion of EMI measurement on both dc and ac-side can be found in existing publications [96-99], the application under discussion is only uni-directional-oriented.

Another issue is that some of the research publications [95, 100] show that the typical EMI filter structure and design procedure doesn't necessarily give an optimal result of CM conducted EMI noises attenuation due the coupling issues.

In short, both the power filter and EMI filter design trade-off and their optimizations are still desired in the bus-interface bi-directional converter system.

### **1.3.4. GRID SYNCHRONIZATION AND ITS STABILITY**

Ac grid frequency synchronization is vital to a converter to deliver power to the grid. Many papers on single-phase and three-phase PLL techniques have been published over

the past decades [101-108]. The issue in a single-phase system is that more design and implementation efforts are required. Because the orthogonal signal generation method must be used in single-phase D-Q frame PLLs, the stationary frame PLLs are widely used in both the digital and analog realms, but it suffers from the noises issue. Many papers propose different solutions in the stationary-frame PLL [109, 110], such as using an additional feedback term, a low-pass filter, etc. However, none of the solutions could effectively reduce the single-phase PLL output noise under different conditions.

There are piles of papers about the PLL design for better performance such as the synchronization speed, steady-state under various grid conditions. However, few of them consider the impact of their design, e.g. pushing up the bandwidth of PLL, on the converter operation and overall power system stability. On the other hand, there are also numerous papers [111, 112] working on the system interaction small-signal stability and use the terminal characteristics, mostly the impedance, to predict the converter stability. However, most of the paper did not notice the grid-synchronization low-frequency dynamic behaviors; thus many potential instability issues are not considered.

As a matter of fact, the grid synchronization instability issue is not new and the corresponding low-frequency power oscillations between synchronous generators are found in the electric power systems [113].

The frequency behavior in power converters has not been well-understood, especially the behavior during weak grid and islanded conditions. Although frequency instability has been reported under a weak grid with a large penetration of distributed generation systems [114, 115], lots of papers [116-119] presents the converter control systems for weak grid and islanded conditions, where they ignore the PLL's potential instability issues and simply assume that the PLL can operate well enough to give precise phase estimation. Insightful analyses on this issue, e.g., what parameters will affect the frequency behavior, are not provided.

### **1.3.5. ISLANDING DETECTION**

An attractive feature of a micro-grid system is that it can operate in a stand-alone mode, independent of the grid. How to determine when the micro-grid should enter such a mode of operation, and not remain connected to the grid, is an important task for the

control to perform. This is the functionality that islanding detection leads to the control system; sensed parameters from the system are used to determine when an islanding event has occurred [120-122]. There are two basic types of detection schemes: passive and active methods.

Passive islanding detection schemes passively search for disturbances upon the grid through sensed and calculated system parameters (voltage, current, frequency, etc.). Such passive schemes use the tolerance ranges of the voltage (88% - 110% of the nominal voltage) and frequency (59.3Hz-60.5Hz) [123, 124] as absolute ratings (for interconnections at the distribution level), but can also be modified to use additional factors such as rate of change in voltage and/or frequency [125, 126] and change in THD levels [74, 75] as well. The main issue with passive detection schemes is the large non-detection zones (NDZs) [127, 128]. This is most commonly the case when a converter is operating at near load-matching conditions, in which the current delivered to/from the grid is virtually zero. The NDZ can be characterized as a region shown in Fig. 1.3.  $\Delta P$  and  $\Delta Q$  are the active and reactive power delivered from the grid.

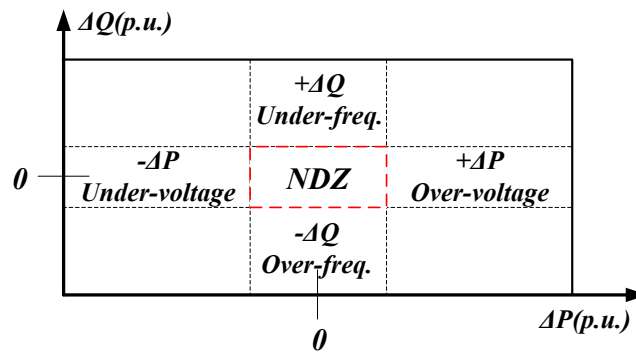


Fig. 1.3: Illustration of NDZ

Active detection schemes [120, 129-153] are incorporated into the system level control loops of a converter system. Active schemes can drive the system voltage and/or frequency away from the normal value and out of NDZs. References [132, 133, 135, 136] use the active frequency drift (AFD) method to distort the current waveform, presenting a zero current segment to drift up the frequency. However, the frequencies in all of these methods are obtained by the zero-crossing method, which cannot work if the system has a phase-locked-loop (PLL) for grid-synchronization. And the methods are valid only under the unity-power factor condition. Reference [135] uses the Sandia voltage shift method to

monitor voltage amplitude to detect islanding condition; however, it may damage the loads. References [138-148] inject the perturbation current, e.g., square waveform, pulse, and random noises, into the system and measures the voltage response or change rate of current/frequency to detect islanding. References [149, 150] use the bus-signal technique that all distributed generation units measure the voltage response generated by a central signal injection unit in the system. However, this group of methods degrades the performance under the polluted system condition, and needs to perturb the system with strong signals.

Reference [151] injects a frequency phase-shift term and measures the drift of frequency to detect the islanding condition, which however needs to modify the control system. Reference [153] directly injects a pulse signal into PLL, which is beyond the PLL loop bandwidth, making the difference of the frequency behaviors under the grid-tide condition and the islanded condition very small. Reference [152] injects a perturbation signal into  $d$ - and  $q$ - channel current to change the converter system frequency and voltage to detect islanding condition, which, however, requires lots of design and tuning effort and may potentially destabilize the converter operation itself.

Most of the active schemes [135, 138-152] have to inject a strong perturbation current into the system for an accurate enough measurement due to the unavailable model for design. It reduces the converter power quality and their continuous perturbations may cause the system-wide instability or damage the equipment. Modification has to be made onto the control systems, such as the current loop, complicating the design and implementation. Some of the active methods [132, 135, 136, 138-152] couldn't be applied to the system where PLL is involved, or may violate other grid-codes, such as the low-voltage-ride-through requirement.

It can be seen that frequency-based active islanding detection methods are very popular in publications. However, these frequency-based methods are still not well-understood. Therefore, the design guideline of the existing frequency-stability-based islanding detection algorithms are missing and a large perturbation has to be implemented resulting in a performance degradation and a damage of other equipment.

Several publications are found on the assessment of the islanding detections at the multi-inverter condition. For example, references [218-220] present the evaluation of several frequency-based islanding detections at the multi-inverter and reveals the degradation of the performance. However, the evaluations didn't give any quantitative results for any number of inverters. Thus, a detailed analysis and modeling methodology is desired to study the islanding-detection at the multi-inverter condition.

#### **1.4. RESEARCH SCOPE AND OUTLINE**

Taking into account the issues mentioned in the review of the existing literature on the ac/dc distribution system and the bi-directional utility-interface converter, several issues will be addressed in this dissertation, and the outline is shown below.

Chapter 1 includes:

1. Research background, research motivation, and literature review.

Chapter 2 includes:

2. Dc-distributing system architecture, system definitions and operations among multiple-converters.

3. Ac-dc bus-interface bi-directional converter topology and the control system design, especially in the single-phase system which has a ripple power issue.

Chapter 3 includes:

4. Power harmonic filter design to mitigate the leakage current reduction in the ac-dc bus-interface converter system.

5. Active control to reduce CM voltage noise and EMI filter investigation of bi-directional converter system.

Chapter 4 includes:

6. Single-phase grid-synchronization solution to reduce the multiple noises.
7. Frequency synchronization modeling and stability study under different grid conditions, including weak grid and islanded conditions.

Chapter 5 includes:

8. Islanding detection algorithm study for three-phase converter system

Chapter 6 includes:

9. Summary and future work.

## **Chapter 2. SINGLE-PHASE ENERGY CONTROL CENTER CONVERTERS**

This chapter presents the concepts of “inter-grid” and energy control center (ECC) converter. In particular, this chapter describes the dc nano-grid, a small-scale sub-system of the “inter-grid”, and how its main operation functions can be used in future commercial/residential distribution systems. The ECC converter, namely the ac-dc bus-interface bi-directional power converter, not only accomplishes ac-dc power conversion, but also decouples the systems’ dynamics and interactions. Embedded with the fast current-interrupt protection, the data-acquisition and communication functions, the multi-functional ECC realizes a more controllable, more reliable, and smarter nano-grid.

### **2.1. NANO-GRID, ENERGY CONTROL CENTER**

In conventional electric power systems, generation and consumption are fully coupled through the overwhelmingly slow dynamics of the electromechanically anchored constant frequency of the rotating masses, assuring transient and static stability [154]. Guaranteed delivery of energy to the consumers is only ensured through redundancy, over-design, and electromechanically controlled system reconfigurations, which, added to the fact that grid infrastructure is aging, inevitably leads to the conclusion that existing power system can be considered to be inherently slow, inefficient, and increasingly unreliable.

Power generation, transmission and distribution facilities cannot easily respond to the variable dynamics of the distributed-generation-sources (DGS), fast load changes, and high-frequency oscillations, thus degrading the reliability and stability of the power system [15, 155]. Additionally, the maintenance cost for power distribution facilities is constantly increasing since the mechanical equipment tends to wear out more quickly than the static electronic devices, greatly influencing overall system efficiency [11, 15]. Moreover, in the way it is built today, the traditional radial architecture and unidirectional feeder protection devices cannot easily accept a high penetration of DGS and renewable-energy-sources (RES) without significant changes.



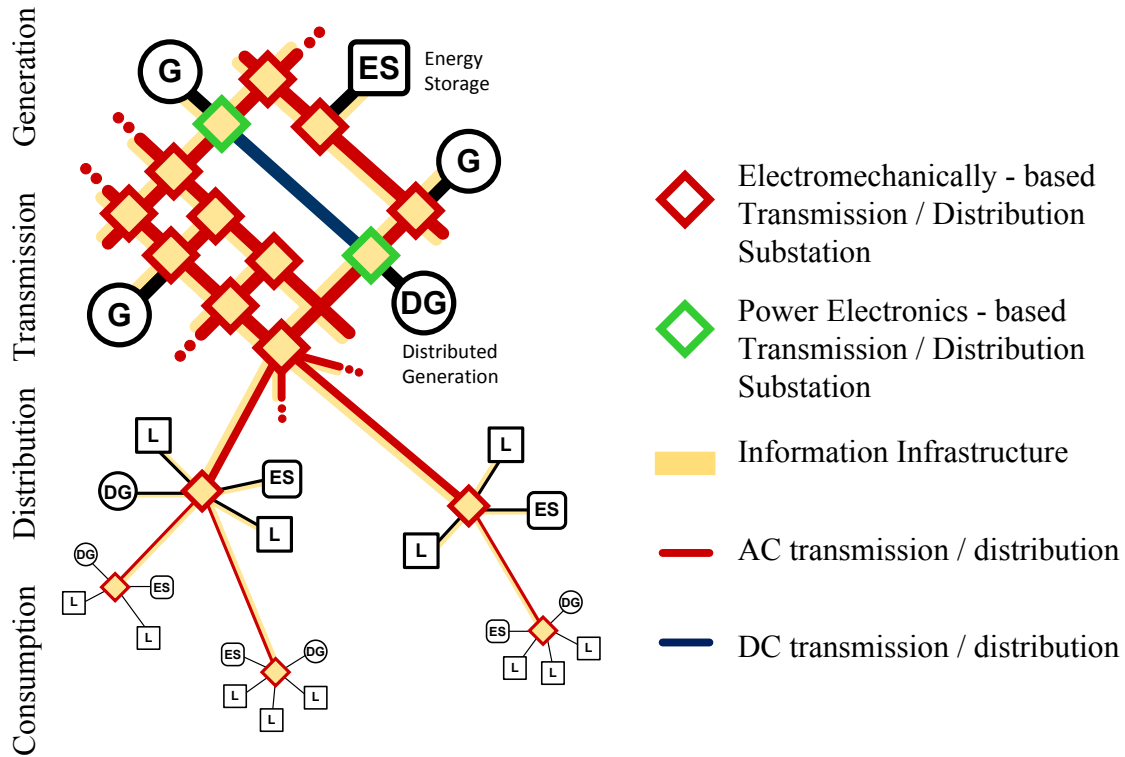


Fig. 2.1: Concept of "smart-grid"

The concept of the "smart grid" has become a widespread initiative in both developed and developing societies, and is gaining significant investment and research interests across different industries. Although the "smart grid" is defined differently by diverse perspectives, the basic idea behind it is to implement an information and communication infrastructure on the top of the existing power grid [158], as shown in Fig. 2.1, to provide increased reliability at, perhaps, a lower installation and operation cost. A "smart grid" would be capable of monitoring and reporting the on-line data of most of the involved components and equipment to the utility in order to assist the optimal-decision making algorithm. In addition, smart-meters with two-way communications capabilities, smart appliances, and demand-response features are some examples of "smart grid" elements that could substantially increase energy efficiency and controllability as well as reduce the cost of energy utilization. However, due to the fact that "smart grid" is still an electro-mechanically controlled system and involves people in the grid control decision-making chain, it might not be capable of addressing some of the technical challenges that will be put to it in the future. Energy demand is growing are tremendously, the number of renewable energy sources and constant power loads (CPL) are increasing rapidly, and

dynamics interactions within the system could easily occur due to the inherent nature of constant power loads to be seen by the grid as a “negative incremental resistance”.

The higher engagement of power electronics converters with the embedded advanced control into the power system transmission and distribution infrastructure offers encouraging solutions to many of the issues mentioned above [7, 9, 19, 15, 154, 155]. The intermittent dynamics of the RES can now be decoupled by power electronics to avoid transient stability problems [15, 19] and to provide the control of active/reactive power for the system voltage support and frequency stabilization. Power-electronics-based HVDC systems significantly reduce the power lost during transmission over long distances with a lower capital cost. Multi-port electronically controlled transmission systems provide a promising solution to interface unsynchronized regional power systems, dramatically improving the system operation reliability and stability.

At the distribution level, in a similar manner, it may be possible that the backbone of future electric power transmission and distribution systems will be based on power electronic converters taking the role of energy control centers (ECC), like an “energy router,” used to interconnect several sub-systems, such as the micro-, mini- and nano-grid [14, 15].

This envisioned future EPS, interconnected by bi-directional ECCs, is named the “inter-grid” system, as shown in Fig. 2.2. The “inter-grid” is composed of ac or dc sub-systems. Each sub-system, containing distributed generation, consumption and energy storage, forms a self-sustained system which could operate under islanded conditions. The energy can then be traded freely in a bi-directional manner between sub-systems via ECCs.

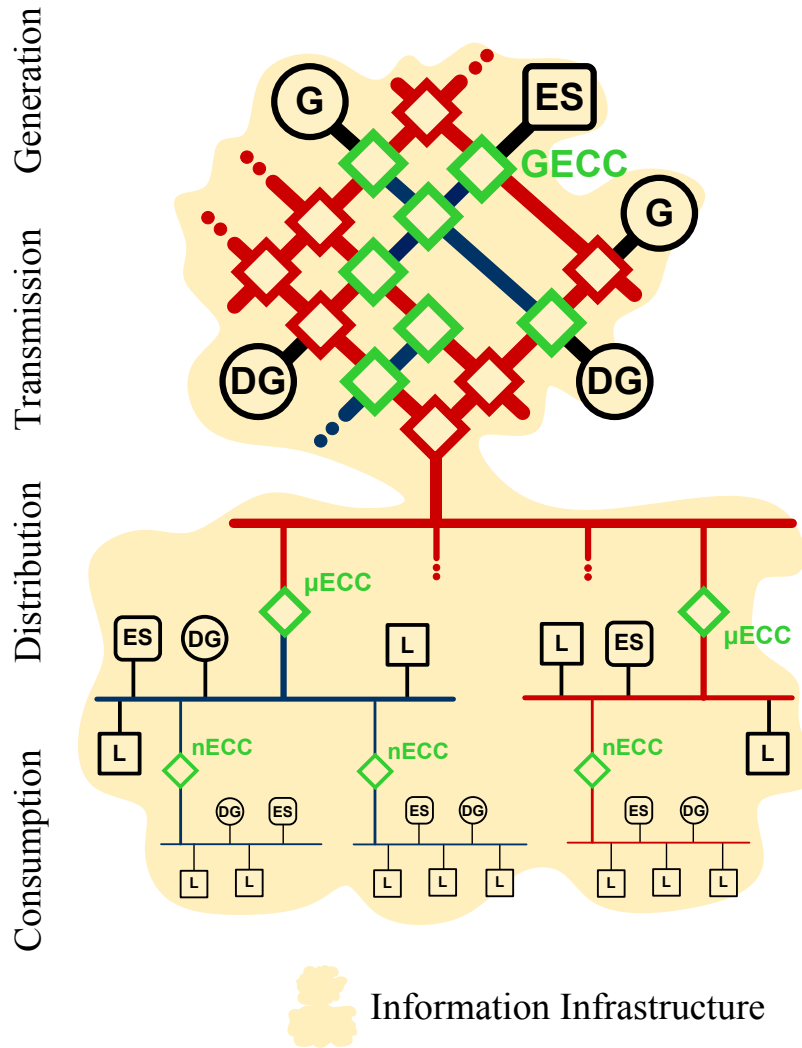


Fig. 2.2: Inter-grid and ECC Converters

As a result, the dynamic interactions and faults of interconnected systems, such as synchronizations, outages and blackouts, will be decoupled and isolated from each other, effectively preventing a cascading system failure. In addition, the complexity of the overall system can be reduced, due in large part to the decoupling of operation, which reduces the effort needed for system-level design and integration. In addition, ECCs inherently provide smart metering [15] by instantaneously recording the system states and parameters, and provide fast fault detection and protection, thereby possibly significantly reducing the need for mechanical breakers [7, 15, 155]. The whole system will be more controllable and autonomous; likewise, it will also be smarter.

Neither a source nor a load converter, an ECC serves as a bus-interface converter interconnecting different systems, and the general requirement of ECCs would be:

1. Bi-directional power flow operation,
2. Fast regulation capability and independent operation based on different interface requirements and conditions,
3. Fast bi-directional fault current interrupt capability,
4. Power metering, data acquisition, and communications,
5. High reliability, high efficiency, and low cost.

The nano-grids in residential houses and buildings could be part of inter-grid sub-systems. Because the ECC converter decouples the dynamics, the nano-grids can be either ac-based or dc-based. Fig. 2.3 shows the interfacing of a single-phase distribution system and a dc-based distribution system through an ECC converter at the residential power level. Dc power provides a straightforward and simple way to integrate multiple sources and loads, such as PV cells, energy storage devices, and variable-speed motor drives, as there are neither ac losses, reactive power issues, nor frequency synchronization issues. Since most household appliances are currently electronic loads, the dc system also helps eliminate the power-factor-correction (PFC) stages.

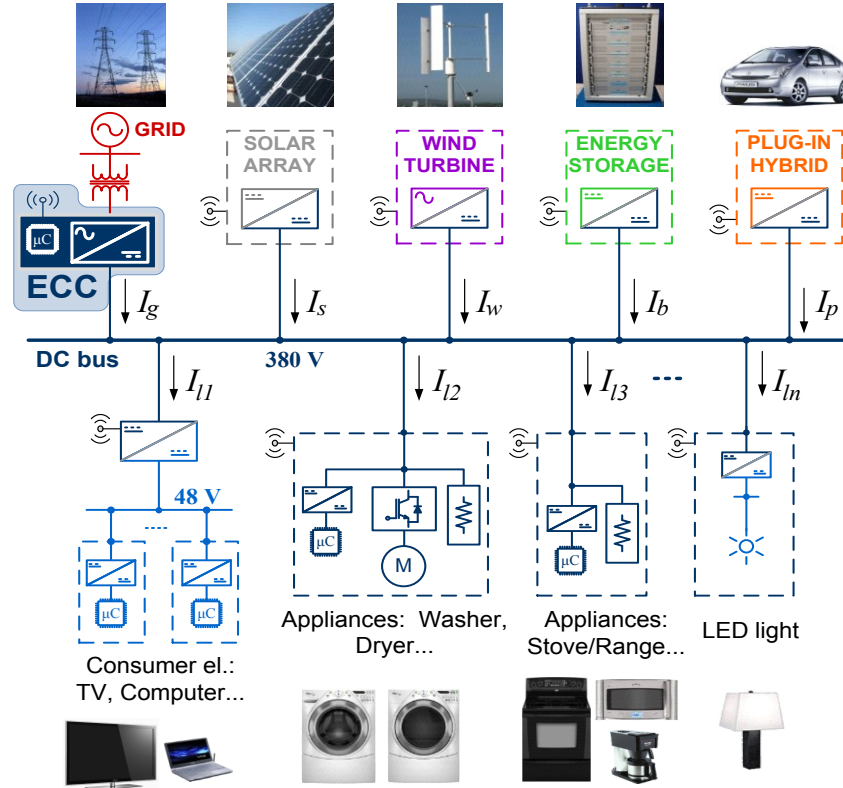


Fig. 2.3: Structure of dc nano-grid in home

In this dc distribution system, multiple distributed renewable energy resources, energy storage elements and loads are connected to a 380 V dc bus via various power converters, as illustrated in the Fig. 2.3. Another low-voltage 48 V dc bus is for the consumer electronic devices and portable equipment. A 380 V bus voltage level is considered economical and efficient enough to apply to the system and be compatible with most products in use today. Currently, 380 V is being adopted as the standard voltage in dc data centers. 48 V is used by consumer devices simply because it has been in use for years in telecommunication applications and is accessible directly by 48 V batteries. This system can be regarded as an “electronic-based” dc nano-grid, which is fully dynamically decoupled from the grid by the grid-interface, bi-directional ac-dc ECC converter. Regardless of the presence of grid, the dc nano-grid is self-sustainable by its own dc sources, and a zero net-energy consumption by a house is possible. Current-limit protection functions are built into every converter, achieving mechanical breakerless system architecture. This proposed dc nano-grid is unlike the current dc distribution system solution in data centers, in which the battery is directly tied to the dc bus for voltage regulation purposes [16].

The ECC converter allows the power demand/response operation with the utility, and, aside from ac current regulation, regulates the dc system bus voltage (around 380V) with fast dynamics and a small ripple. Based on the general requirements of ECC, several major characteristics of this ECC converter include but are not limited to:

1. Stiff and fast regulation of the high-voltage (around 380V) dc bus with droop characteristics [4, 31]: enables the ECC to ride through the transient dynamics that occur on both ac and dc side, achieving decoupled operation. The droop characteristics help attain current sharing between multiple sources; thus the dc system can operate even under islanded conditions.
2. Taut regulation of ac injection current: It is used to comply with the utility-interface codes; thus the whole dc system behaves like a simple ac load/source. As such, the dc dynamics will be transparent to the utility side.
3. Bi-directional-oriented topology: It provides the dc system the opportunity to regenerate the power back to the utility; thus the ECC is more like an energy router, giving more change to residents for power management.
4. Bi-directional current interrupting capability: The current limit protection is integrated into the power converter itself, eliminating the need on both sides for a bulky and costly mechanical protection device, e.g., circuit breaker.
5. Small-stored static energy on the dc-side: It can reduce the transient energy spike under shot-circuit conditions, thus improving the safety to human.
6. High power density, high efficiency, and low cost.

## **2.2. ECC CONVERTER TOPOLOGY**

There are probably countless power converter topologies in the world; however, only a few of them are prevalent and commercialized. Voltage-source-converter (VSC) is a quite successful group of topologies that are under mass production and used in diverse applications thanks to the continuous advancement of self-commutated devices, such as insulated-gate bi-polar transistors (IGBTs), integrated gate-commutated thyristors (IGCTs), and gate turn-off thyristors (GTOs). VSCs are suitable to be ECCs by means of their bi-directional-oriented topologies and the interruption of fault current in one

direction. The dc-link capacitor helps decouple the low- to intermediate-frequency dynamics between the dc side and the ac side. Some of the well-accepted bi-directional VSC topologies used in three-phase case are shown in Fig. 2.4 to Fig. 2.7, including a two-level VSC [53, 54], a three-level boost rectifier [54], a three-level neutral point clamp (NPC) converter [53-55], and a three-level active neutral point clamp (ANPC) converter [54, 55]. The selection of topology among these candidates relies on multi-faceted trades-offs and the specific power/voltage conditions. Many of them are being used in applications such as medium-voltage drives, wind power converter, and FACTS equipment.

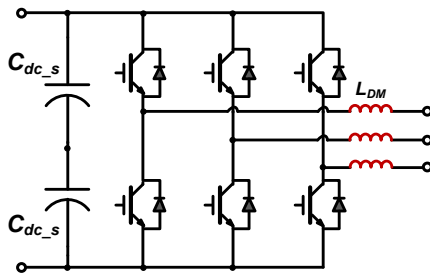


Fig. 2.4: Two-level VSC

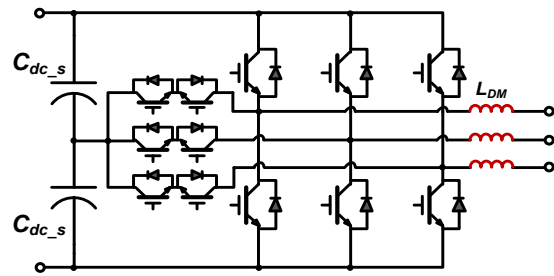


Fig. 2.5: Three-level boost rectifier

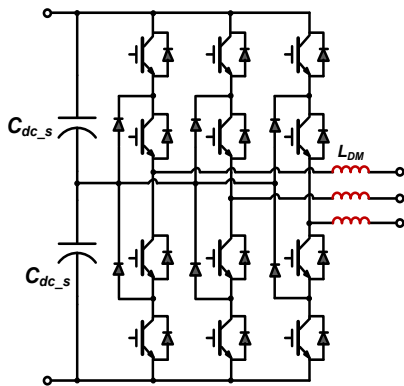


Fig. 2.6: Three-level neutral point clamp (NPC) converter

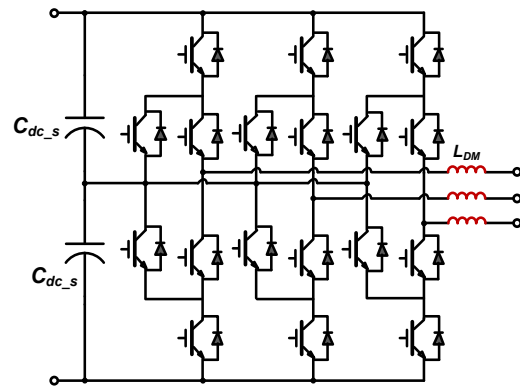


Fig. 2.7: Three-level active neutral point clamp (ANPC) Converter

For applications with higher voltage or higher power, the same topologies can be employed by using devices with higher ratings or using multiple devices in series or in parallel. Multilevel (more than three levels) or cascaded converters [54, 158] make up a large group of topologies that have been studied extensively over the past decade. For example, Fig. 2.8 shows a modular multilevel converter (MCC) used in high-voltage-direct-current (HVDC) systems, and Fig. 2.9 shows a five-level ANPC converter used in

motor drives. These can be also regarded as possible ECC ac-dc topologies in medium to high-voltage distribution systems.

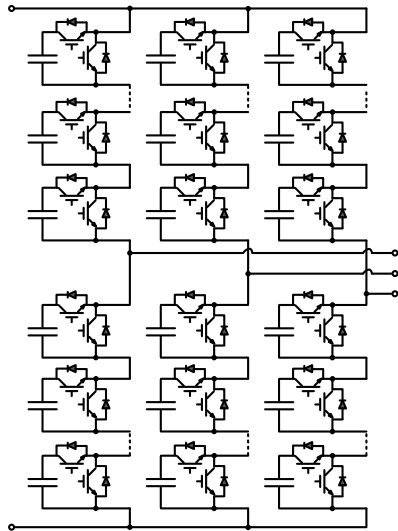


Fig. 2.8: Cascaded modular multi-level converter (MMC)

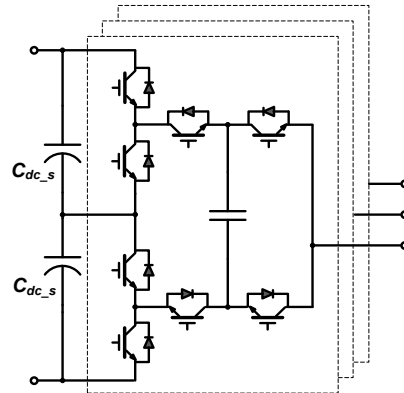


Fig. 2.9: Cascaded modular multi-level converter

All of the topologies discussed above could serve as the basic cell of an ac-dc converter. However, one stage is not enough for a bridge-type ac-dc ECC as the dynamic interactions still exist. The dc-side dynamics, e.g., the dc voltage dynamics, are largely determined by the dc-link capacitor value and variations on the ac-side, such as the low-frequency harmonics and the unbalanced ac input. Moreover, the protection function cannot be achieved to interrupt the dc-side fault current. Therefore, one of the possible ECC converter topologies would have two stages: each stage processes the energy and deals with the interface requirement for each side. Fig. 2.10 and Fig. 2.11 show the two-stage topology for an ac-ac ECC and dc-ac ECC, respectively.

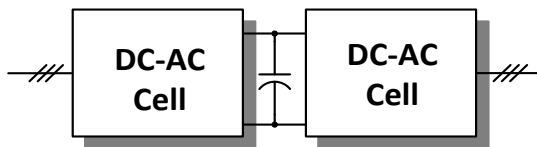


Fig. 2.10: Ac-ac transformerless ECC

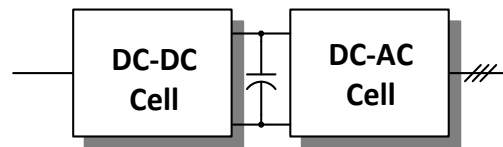


Fig. 2.11: Dc-ac transformerless ECC

For a bi-directional dc-dc converter cell, in contrast, there are not as many publications on high-voltage/power dc-dc converter as there are on their ac-dc counterparts. The simple topologies would be the bi-directional buck converter (Fig. 2.12)



and its interleaved topology; e.g., the three-phase interleaved converter in Fig. 2.13. Multi-stage or multi-level topologies might be chosen if the voltage ratio is high.

The two phase legs of these converters can also be used as a bi-directional dc-dc converter in which both the positive and negative dc output rails can be controlled in respect to the dc-link. Fig. 2.14 is an example of two-level full-bridge VSC topology as the dc-dc cell.

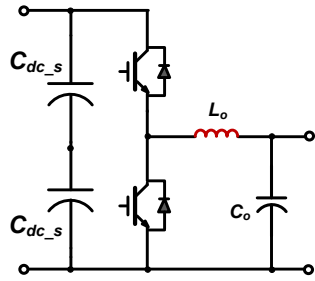


Fig. 2.12: Bi-directional buck converter

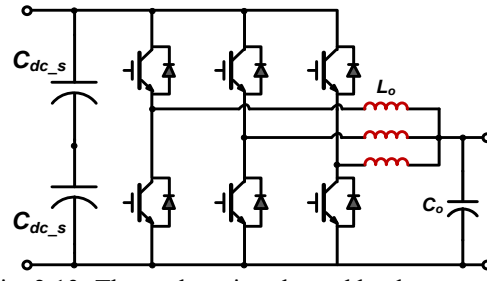


Fig. 2.13: Three-phase interleaved buck converter

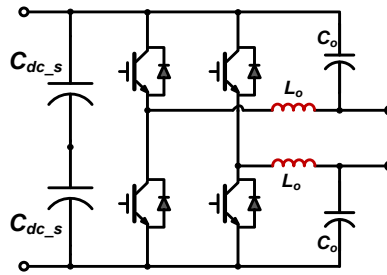


Fig. 2.14: Two-level full-bridge dc-dc converter

There are also some research activities focused on the integration of the ECC converter with the transformer. The purpose of employing a transformer is to provide galvanic isolation and/or to step up/down the voltage level. Using either high-frequency or low-frequency isolation converter cells provides more converter topologies. Many high-frequency transformers have a dual-bridge topology without a resonant tank; such as single-phase or three-phase dual active bridge, or a full-bridge or half-bridge isolated topology. A resonant dual-bridge can be chosen for low switching loss, such as a PRC, SRC, LLC, or CLL. Most isolated topologies operate under low-voltage and low-power conditions, and currently their application in high-voltage, high-power applications still suffer from reliability and efficiency issues. Emerging wide band-gap devices, such as SiC and GaN devices, are believed to solve many of these issues.

There are many ECC converter topologies made possible just by choosing different cell combinations. Engineers can design the ECC converters based on different applications and requirements. The following discussion presents an example of ECC converter design for a single-phase utility system.

## 2.3. ECC CONVERTER FOR SINGLE-PHASE UTILITY AND DC NANO-GRID

### 2.3.1. IMPACT OF RIPPLE POWER ON DC NANO-GRID

The bus-signaling technique [15, 157, 159, 160] using the droop control accomplishes the current sharing independent of communication among multiple source converters on the dc side. As shown in Fig. 2.15, the source converters on the dc side with droop control can be illustrated by voltage sources with different output droop resistors.

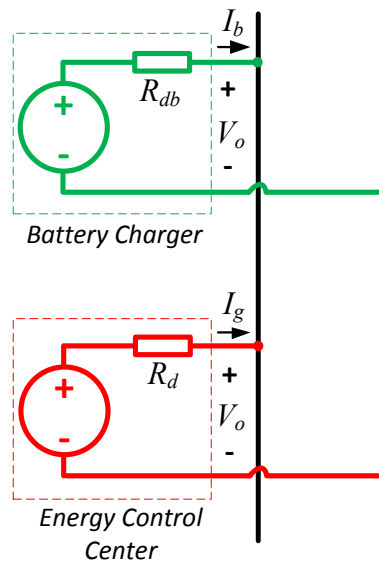


Fig. 2.15: Example of dc source converters with droop control

The nominal voltage of the dc-bus is 380 V, but the operating voltage of the dc bus is chosen to be in a range, e.g., between 360 V and 400 V, to allow for power sharing and voltage regulation using droop control. The static V-I curve of ECC is shown in Fig. 2.16 [15] where  $R_d$  represents the droop value. In the first quadrant of the V-I plane, ECC takes energy from the grid when the dc output current  $I_g$  is positive, while in the second quadrant it is sourcing energy back to the grid.

If the ECC output is overloaded or even shorted in the first quadrant, the ECC limits the output current to  $I_{gD}$  in Fig. 2.16. If the operator of the utility to which the nano-grid

is connected requests from the ECC a specific amount of power that is less than the converter rating, the converter can reprogram its V-I characteristic in the second quadrant to limit the current to a value that corresponds to the demanded power, as represented by the dotted line. Under these two conditions, the battery on the dc-side can take charge of the dc-bus voltage regulation via the bi-directional charger (BDC) [161].

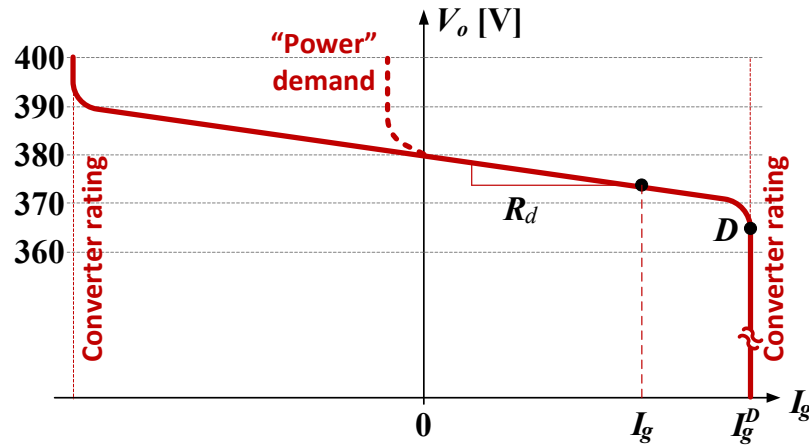


Fig. 2.16: ECC converter dc-side output V-I operation curve.

The H-bridge topology, as shown in Fig. 2.17, is widely used as a grid-interfaced converter to deliver energy between the ac grid and dc renewable energy sources [11, 52, 162]. Specifically, compared with the single-phase boost PFC topology [5], the H-bridge converter processes the energy either in rectification mode, meaning that the power goes from the ac grid to the dc side, or in regeneration mode, from the dc energy resources to deliver power from the dc-side to the ac grid. Examples for this are seen in many solar, energy-storage systems, and electric vehicle (EV) applications.

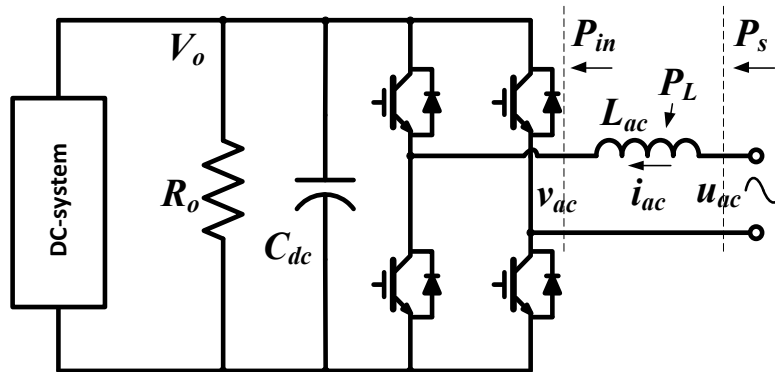


Fig. 2.17: Single-phase full-bridge converter

The grid current and voltage in Fig. 2.17 are defined below in (1) and (2), in which the power factor (PF) angle is  $\varphi$ .

$$i_{ac} = I_s \sin(\omega_o t - \varphi) \quad (1)$$

$$u_{ac} = U_s \sin(\omega_o t) \quad (2)$$

The power ( $P_{in}$ ) that flows through the full-bridge topology will be the full-bridge terminal voltage  $v_{ab}$  multiplied by input current  $i_{ac}$ , as shown in (3). The voltage difference between  $v_{ab}$  and input voltage  $u_{ac}$  is the voltage across the ac inductor  $L_{ac}$ , as shown in (4).

$$P_{in} = v_{ab} \cdot i_{ac} \quad (3)$$

$$v_{ab} = U_s \sin(\omega_o t) - \omega_o L_{ac} I_s \cos(\omega_o t - \varphi) \quad (4)$$

$P_{in}$  consists of two parts: the dc average power  $P_{av}$  in (5), and the second-order ripple power  $P_r$  in (6).

$$P_{av} = \frac{U_s I_s}{2} \cos \varphi \quad (5)$$

$$\begin{aligned} P_r &= -\frac{U_s I_s}{2} \cos(2\omega_o t - \varphi) - \frac{\omega_o L_{ac} I_s^2}{2} \sin(2\omega_o t - 2\varphi) \\ &= \sqrt{P_{av}^2 + \left( \frac{\omega_o L_{ac} I_s^2}{2} - P_{av} \frac{\sin \varphi}{\cos \varphi} \right)^2} \sin(2\omega_o t - 2\varphi + \psi), \psi = \arctan \frac{P_{av}}{\frac{\omega_o L_{ac} I_s^2}{2} - P_{av} \frac{\sin \varphi}{\cos \varphi}} \\ &= A \sin(2\omega_o t - 2\varphi + \psi), \psi = \arctan \frac{P_{av}}{\frac{\omega_o L_{ac} I_s^2}{2} - P_{av} \frac{\sin \varphi}{\cos \varphi}} \end{aligned} \quad (6)$$

If the full-bridge topology directly feeds to the dc system, as shown in Fig. 2.17, which includes a resistor load  $R_o$ ;  $P_s$  is the net power delivered by other dc sources. The resistor load consumes all the active power under  $V_o = 380$  V, as shown in (7). Then (8) is obtained.

$$R_o = \frac{V_o^2}{P_{av} + P_s} \quad (7)$$

$$\frac{v_o^2}{R_o} + v_o \cdot C \frac{dv_o}{dt} = A \sin(2\omega_o t - 2\varphi + \psi) + P_{av} + P_s \quad (8)$$

This differential equation has only one steady-state solution obtained as (9).

$$v_o = \sqrt{V_o^2 + \frac{A}{\sqrt{\left(\frac{P_{av} + P_s}{V_o^2}\right)^2 + (\omega_o C_{dc})^2}} \sin(2\omega_o t - 2\varphi + \psi + \lambda), \lambda = -\arctan\left(\frac{C_{dc} V_o^2}{P_{av} + P_s}\right)} \quad (9)$$

Then the dc-link voltage ripple can be obtained as shown in (10).

$$\Delta v_{o\_pp} = v_{o\_max} - v_{o\_min} = \frac{A}{\frac{(v_{o\_max} + v_{o\_min})}{2} \sqrt{\left(\frac{P_{av} + P_s}{V_o^2}\right)^2 + (\omega_o C_{dc})^2}} \quad (10)$$

It is seen that the maximum dc-bus voltage ripple under the same ac input condition occurs when  $P_s = 0$ . If the approximation of the average dc-bus voltage is obtained in (11), (10) can be simplified as (12).

$$V_{o\_av} = \frac{1}{T} \int_t^{t+T} v_o \cdot dt \approx \frac{v_{o\_min} + v_{o\_max}}{2} \quad (11)$$

$$\Delta v_{o\_pp} = \frac{A}{V_{o\_av} \sqrt{\left(\frac{P_{av} + P_s}{V_o^2}\right)^2 + (\omega_o C_{dc})^2}} \quad (12)$$

Due to the droop operation range, it is desired to have a small dc-bus voltage ripple. Specifically, the dc-link capacitors  $C_{dc}$  must be 6.9 mF based on the specifications in Table I.

Table 2.1: Operations specifications for the full-bridge topology for the dc nano-grid

Parameter	$V_{av}$	$P_{av}$	$L_{ac}$	$\Delta V_{o\_pp}$	$\omega_o$	$\varphi$	$C_{dc}$
Value	380 V	10 kW	300 $\mu$ H	10 V pk-pk	$2\pi 60$ rad/s	$0^\circ$	6.9 mF

Many electrolytic capacitors have to be employed as the dc-link capacitor  $C_{dc}$  for single-phase power conversion [52, 162] in the wake of stabilizing the dc-bus voltage. However, the impact of ripple power on the dc nano-grid still presents a challenge. When the ECC converter operates as a current source or in current limiting mode and the battery regulates the dc-bus voltage via BDC, the output impedance of the BDC is determined by the droop resistance, which could be much smaller than the impedance of the dc-bus capacitor at 120 Hz. Thus, as shown in Fig. 2.18, lots of ripple power  $P_r$  will circulate between the battery and grid, degrading the battery life and resulting in more losses. Fig. 2.19 shows the battery current in an experiment when the battery charger

changes from current mode to droop mode ( $0.5 \Omega$ ). It is clear that there is circulating current under the droop mode. Moreover, the life-time and power-density of the full-bridge are degraded dramatically due to the bulky electrolytic capacitors, and there is a safety issue because of the large static energy stored in the dc-link capacitors. In addition, the full-bridge topology suffers from a shortage of internal active current-limit protection on dc-side. Therefore, a single-stage topology, such as a full-bridge topology, is unable to fulfill the decoupled operation requirement of the ECC.

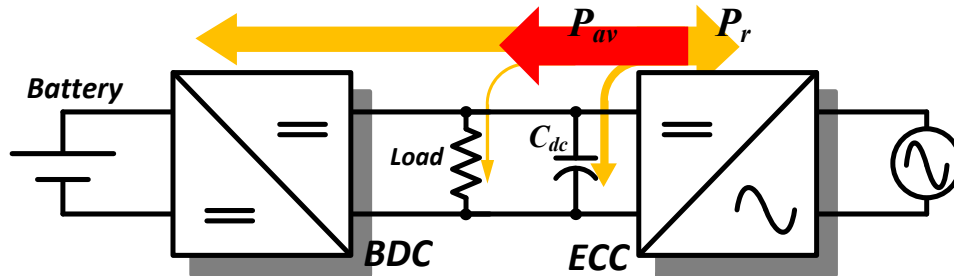


Fig. 2.18: Bi-directional charger (BDC) regulates dc-bus voltage and ECC operates in current limiting mode.

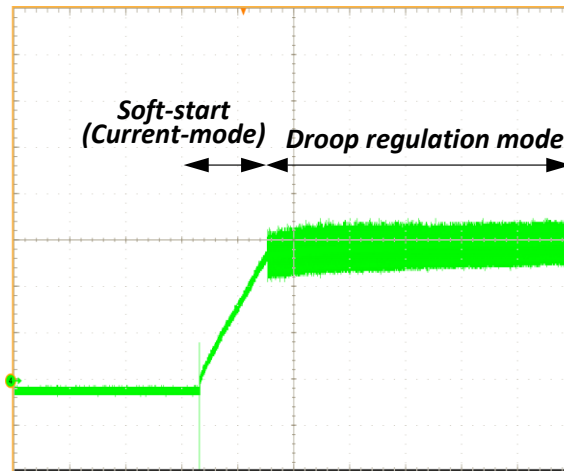


Fig. 2.19: Ripple current [1 A/DIV] flowing to battery charger due to ripple power

### 2.3.2. HIGH-DENSITY ECC CONVERTER FOR SINGLE-PHASE AC-DC BUS-INTERFACE

In this chapter, a two-stage single-phase PWM converter, as shown in Fig. 2.20, is investigated as a high power-density ECC converter for a dc nano-grid application. Two phase legs are used as the full-bridge to interface with the grid. The other phase leg is used as a bi-directional SR dc-dc converter to regulate the dc-bus voltage with a small voltage ripple and with a fast dynamic response. Short-circuit protection can be readily attained in either direction by turning off the second-stage or full-bridge switches. The

black-start is simple due to the “buck” topology on both sides. Moreover, in terms of dc system-level design and study of dc-bus converters’ interactions, the second-stage dc-dc converter is deemed advantageous over the dc-link of the full-bridge to interface to the dc system, as the complicated quasi-static analysis approach [163] must be used for terminal characterization of the full-bridge topology. To improve the power density and eliminate the electrolytic capacitors, it is desirable to explore ways to shrink the size of dc-link capacitor  $C_{dc}$ .

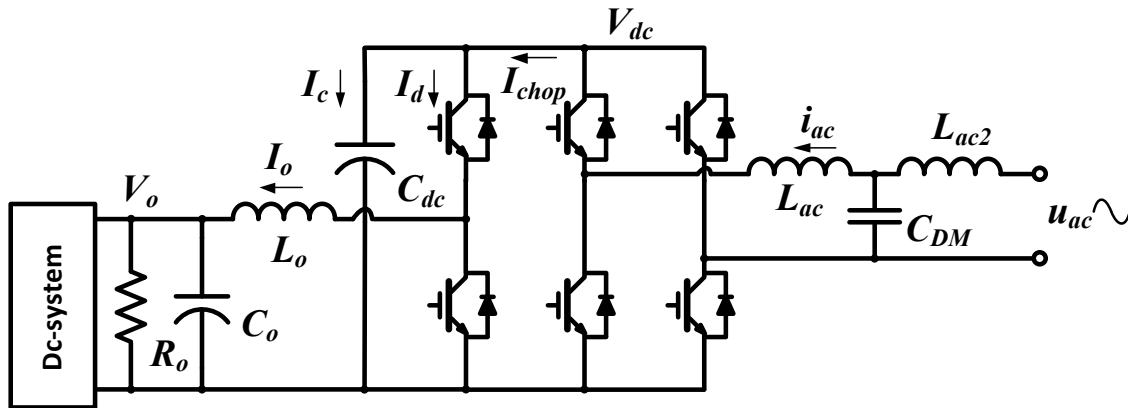


Fig. 2.20: Two-stage bi-directional single-phase PWM converter

Information on single-phase ac-dc converters with reduced dc-link capacitor volume, which leads to high power density, can be found in [73-75, 164-167]. References [73, 74] use an additional paralleled phase-leg and an inductor as an auxiliary circuit to reduce the dc-link voltage ripple. Alternatively, references [164, 165] use a similar structure but with an ac capacitor as the energy storage element, while [75] uses a dc capacitor to absorb the ripple energy. It is proposed that an additional ripple energy storage circuit be put on the ac line in [164] and in parallel with the PFC circuit in [167] to reduce the dc-side capacitor value. The drawbacks of the above approaches are the difficulty of designing linear-type controls and the sensitivity to system parameters. Bi-directional controls and the seamless bi-directional mode transition for those topologies have not been well-documented. References [168] and [169] propose a topology that uses dc-dc converter plus silicon-controlled rectifier (SCR), in which the SCR is switched at the line-frequency, thus leading to low switching loss. All of these solutions require additional phase-legs or significant change of topology as well as a sophisticated controller, which dramatically reduce the system reliability and efficiency. Thus, the

following analysis intends to address the possibility of and the corresponding design issues with significantly reducing the dc-link capacitor using a two-stage ECC converter without modification.

As shown in Fig. 2.20, the reduction of the dc-link capacitor  $C_{dc}$  will naturally yield a large dc-link voltage variation. For the converter to operate using the specifications in Table I, two requirements must be fulfilled. Firstly, if the dc-bus voltage  $V_o$  is regulated with a very small ripple, the input power  $P_{in}$  should be fully-controlled so that all the dc average power  $P_{av}$  flows through the second-stage dc-dc converter and the ripple power  $P_r$  goes to the small dc-link capacitor  $C_{dc}$ . Secondly, the input current for this case can still be well-controlled as a sinusoidal waveform at PF angle  $\varphi$ .

If neglecting the instantaneous power  $P_L$  that is dissipated on the boost inductor  $L_{ac}$ , the first requirement can be expressed in (10), which allows that the instantaneous power  $P_{cap}$  in the dc-link capacitor is the same as the input ripple power, which is  $P_r$  on the right-hand side in (13).

$$\begin{aligned} P_{cap} &= v_{dc} \cdot i_c = -\frac{U_s I_s}{2} \cos(2\omega t - \varphi) \\ \Leftrightarrow C_{dc} \frac{dv_{dc}}{dt} \cdot v_{dc} &= -\frac{U_s I_s}{2} \cos(2\omega t - \varphi) \end{aligned} \quad (13)$$

By solving the differential equation of (13), the dc-link voltage  $v_{dc}$  can be resolved as in (14); the maximum and minimum dc-link voltages are also shown below in (15). The constant value  $K_{c\_const}$  represents the energy stored in the dc-link capacitor.

$$v_{dc} = \sqrt{K_{c\_const} - \frac{U_s I_s}{2C_{dc}\omega_o} \sin(2\omega t - \varphi)} \quad (14)$$

$$v_{dc\_min} = \sqrt{K_{c\_const} - \frac{U_s I_s}{2C_{dc}\omega_o}}, \quad v_{dc\_max} = \sqrt{K_{c\_const} + \frac{U_s I_s}{2C_{dc}\omega_o}} \quad (15)$$

The definition of average dc-link voltage  $V_{av}$  is shown in (16). The relationship between  $K_{c\_const}$  and the average dc-link voltage  $V_{av}$  is established below in (17).

$$V_{av} = \frac{1}{T} \int_t^{t+T} v_{dc} \cdot dt \approx \frac{v_{dc\_min} + v_{dc\_max}}{2} \quad (16)$$



$$K_{c\_const} = V_{av}^2 + \left( \frac{U_s I_s}{4V_{av} C_{dc} \omega_o} \right)^2 \quad (17)$$

The dc-link voltage  $v_{dc}$  thereby can be reformed as shown in (18).

$$v_{dc} = \sqrt{\left( V_{av} + \frac{U_s I_s}{4V_{av} C_{dc} \omega} \right)^2 - \frac{U_s I_s}{2C_{dc} \omega} [1 + \sin(2\omega t - \varphi)]} \quad (18)$$

For any  $C_{dc}$  value, the expression under the radical sign in (18) is larger than zero, offering the possibility to reduce  $C_{dc}$ . Based on (18), the averaged dc-link capacitor current  $i_c$  and the averaged current flowing to the dc-dc converter  $i_d$  can be derived as:

$$i_c = \frac{-\frac{U_s I_s}{2} \cos(2\omega_o t - \varphi)}{\sqrt{\left( V_{av} + \frac{U_s I_s}{4V_{av} C_{dc} \omega_o} \right)^2 - \frac{U_s I_s}{2C_{dc} \omega_o} [1 + \sin(2\omega_o t - \varphi)]}} \quad (19)$$

$$i_d = \frac{\frac{U_s I_s}{2} \cos \varphi}{\sqrt{\left( V_{av} + \frac{U_s I_s}{4V_{av} C_{dc} \omega_o} \right)^2 - \frac{U_s I_s}{2C_{dc} \omega_o} [1 + \sin(2\omega_o t - \varphi)]}} \quad (20)$$

Using a value of 550 V for the dc-link average voltage and a value of 10 kW for the average power,  $i_c$  is shown in Fig. 2.21 under different dc-link capacitor values. These figures show that the reduction of dc-link capacitor  $C_{dc}$  doesn't increase the dc-link capacitor average current rating. Fig. 2.22 shows the value of  $i_c$  with different dc-link average voltage levels  $V_{av}$  with 300  $\mu\text{F}$   $C_{dc}$ . They show that the reduction of  $V_{av}$  results in a bigger  $i_c$ . It is quite evident from Fig. 2.21 and Fig. 2.22 that the average dc-link voltage level has more impact on the current rating of the dc-link capacitor than the value of the dc-link capacitor does.

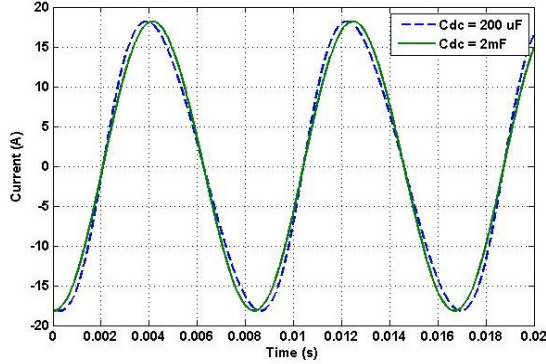


Fig. 2.21: Average current  $i_c$  flowing to  $C_{dc}$  under different  $C_{dc}$ .

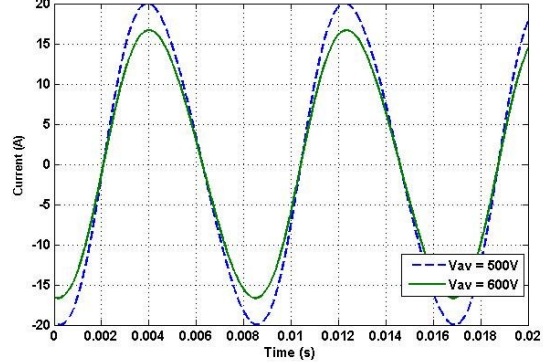


Fig. 2.22: Average current flowing to  $C_{dc}$  under different  $V_{av}$ .

For the ac current regulation requirement, it should be noted that the dc-link current  $i_{chop}$  is the switching current with the rectified sinusoidal profile. The average value of  $i_{chop}$  should be confined within the profile of ac current  $i_{ac}$  such that the second requirement can be written as (21). Substituting (19) and (20) into (21) gives (22).

$$|i_d + i_c| = |i_{chop}| < |I_s \sin(\omega_o t - \varphi)| \quad (21)$$

$$U_s < V_{dc} \quad (22)$$

Equation (21) indicates that as long as the input grid peak voltage  $U_s$  is smaller than the dc-link voltage  $v_{dc}$ , ac current can be regulated as the sinusoidal waveform regardless of the dc-link capacitor value. Thus, the low-frequency average and ripple power can be decoupled with a small  $C_{dc}$  as long as a well-designed controller is implemented.

The high-frequency interactions between the ac side and dc-side with a small  $C_{dc}$  can be investigated by comparing the input impedance of the second-stage  $Z_{in}$  and the impedance of dc-link capacitor  $Z_{Cdc}$ .  $Z_{in}$  at high-frequency can be derived as (23), where  $D$  is the duty-cycle of the second-stage. The impact of the dc-system impedance is ignored as it is decoupled by the large capacitance  $C_o$ , and the  $Z_{in}$  is dominated by  $L_o$ .

$$Z_{in} = \frac{1}{D^2} \frac{s^2 L_o R_o C_o + s L_o + R_o}{1 + s R_o C_o} \quad (23)$$

Fig. 2.23 shows the impedances in the high-frequency range ( $>1$  kHz) under different values of  $C_{dc}$ , which shows that the  $Z_{in}$  (using component values from Table 2.2) is always higher than  $Z_{Cdc}$ . As such, all of the high-frequency noise  $i_{hs}$  from the grid are routed to  $C_{dc}$ , though very small, decoupling the high-frequency dynamics between the dc side and ac-side, as shown in Fig. 2.24.

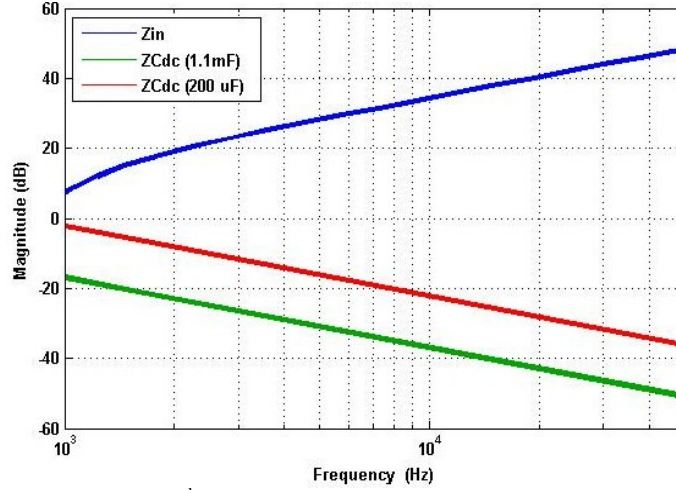


Fig. 2.23: Input impedance of 2<sup>nd</sup> stage  $Z_{in}$  and impedance of  $C_{dc}$  under 1.1 mF and 200 uF cases.

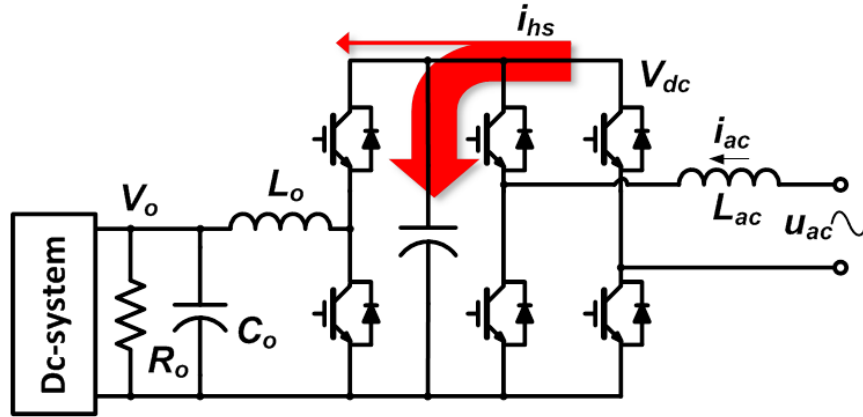


Fig. 2.24: Routes of ac-side high-frequency noise  $i_{hs}$ .

Thus, it is appropriate to use the dc-dc converter regulating the dc bus voltage  $V_o$  with a small ripple plus the H-bridge regulating ac current with a small dc-link capacitor  $C_{dc}$ . For this case, the design of this small  $C_{dc}$  lies in the trade-off between the power level  $P_{av}$ , the average dc-link voltage  $V_{av}$ , and the dc-link voltage variation range. Fig. 2.25 shows the relationship between the dc-link maximum and minimum values ( $v_{dc\_max}$ ,  $v_{dc\_min}$ ), the dc-link voltage average value  $V_{av}$ , and the dc-link capacitor value  $C_{dc}$  for a 10 kW average power level.

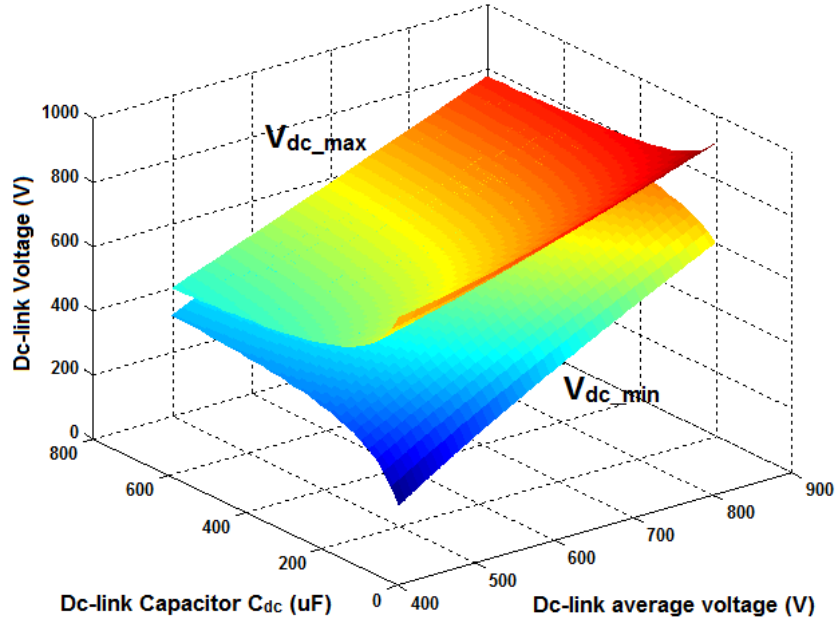


Fig. 2.25:  $v_{dc\_max}$  and  $v_{dc\_min}$  in relationship with  $C_{dc}$  and  $V_{av}$

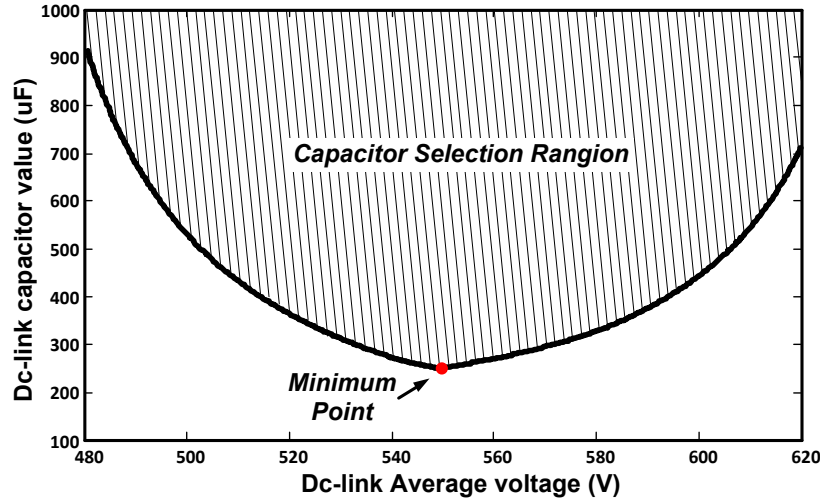


Fig. 2.26: Minimum point of the dc-link capacitor  $C_{dc}$

To find the minimum dc-link capacitor, the minimum dc-link voltage  $V_{min}$  value is set as 450 V as the output voltage  $V_o$  (dc-bus voltage) is controlled at 380 V, and the maximum dc-link voltage value  $V_{max}$  is set as 650 V. Using (14) - (18), the boundary of the dc-link capacitor is obtained as follows:

$$C_{dc} \geq \frac{U_s I_s}{4(V_{av} - V_{min})V_{av}\omega_o} \quad (24)$$

$$C_{dc} \leq \frac{U_s I_s}{4(V_{max} - V_{av})V_{av}\omega_o} \quad (25)$$

The dc-link capacitor selection range based on (24) and (25) can be readily found in Fig. 2.26, where the minimum capacitor value can be directly found. The minimum dc-link capacitor value is derived as in (26).

$$C_{dc\_min} = \frac{U_s I_s}{(V_{max}^2 - V_{min}^2) \omega_o} \quad (26)$$

As a result, the minimum capacitor value is observed to be 241  $\mu$ F. For the real system, to leave a margin, the value is chosen as 360  $\mu$ F. Compared to 6.9 mF, this is a huge reduction in the dc-link capacitor. The reduction of dc-link capacitor  $C_{dc}$  in turn poses challenges to designing the controller to separate the ripple power and dc average power, which is examined in the following section.

### 2.3.3. BI-DIRECTIONAL CONTROL SYSTEM

The proposed bi-directional digital control structure consists of two independent controllers illustrated in Fig. 2.27, where other dc renewable energy resources are simply modeled as the current sources.

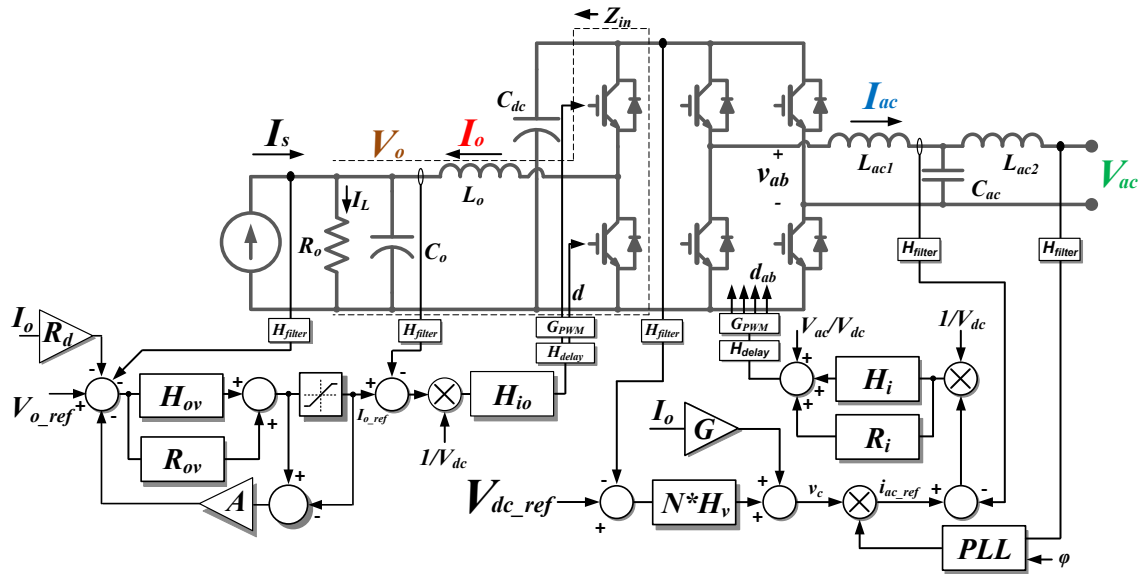


Fig. 2.27: Proposed bi-directional control structure

Essentially, one controller is used to control the dc bus voltage  $V_o$  by operating the dc-dc converter in SR buck mode or SR boost mode, relying on the power flow direction. The carefully designed PID ( $H$ ) plus the resonant controller ( $R$ ) are used to accomplish high bandwidth and high loop-gain, especially at double-line frequency (120Hz), to handle a large input ( $V_{dc}$ ) variation as well as to regulate the output voltage  $V_o$ .  $H_{io}$  is used

to regulate the dc inductor current and to damp the resonance formed by the output LC filter. The other double-loop controller controls the H-bridge topology. The outer-loop controls the dc-link average voltage  $V_{dc}$  in conjunction with an additional load current feedback term ( $G$ ); while the inner-loop regulates the power from the grid. The outer-loop controller has a notch-filter ( $N$ ) in series with PID ( $H_v$ ) to correct the control-signal, achieving a low THD of the ac current regulation.

The control delay due to the sensor filter and digital computation must be modeled. Each sensor filter is assumed to be a second-order low-pass-filter  $H_{filter}$ .  $H_{delay}$  is the total delay from the digital controller, which consists of a one switching-cycle ( $T_s$ ) delay, due to the digital, A/D conversion process, and digital PWM modulator. The modulator gain is assumed to be unity.

It is necessary to establish the small-signal models in order to design the controller for  $H_{io}$ ,  $H_{iv}$ ,  $R_{ov}$ ,  $H_v$ ,  $N$ ,  $H_i$ , and  $G$ . The ECC frequency response and the controller can be represented by the small-signal-based transfer function block diagram in Fig. 2.28.

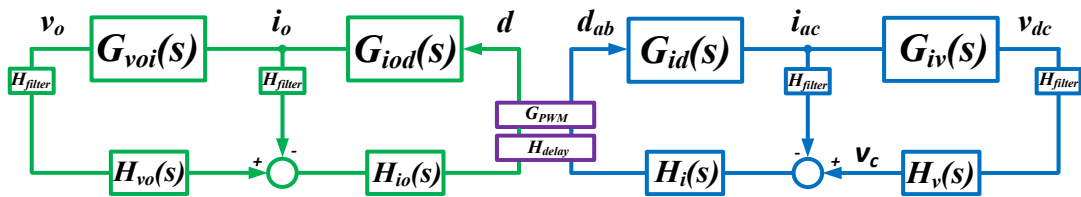


Fig. 2.28: Transfer-function block diagram of ECC control system

During every half-line cycle, the sub-modes of the full-bridge are the same as the single-phase PFC circuit due to the nature of the boost converter. So, the quasi-static modeling approach [163, 170], due to the varying line voltage, can be applied to model the current loop behavior in the high-frequency range.

The small-signal control-to-current transfer function of the full-bridge in the high-frequency range is obtained in (27) [163, 170], in which  $d_{ab}$  (between -1 and 1) is the average duty-cycle signal of the full-bridge. The input impedance of the second-stage converter  $Z_{in}$  will be the loading impedance of the first stage.

Normally, the control bandwidth of  $V_o$  is lower than that of the ac current loop. Thus in the high-frequency range near the cross-over frequency of the ac current loop,  $Z_{in}$ , as shown in (23), would be the unregulated input impedance of the second-stage converter.

As such,  $H_i$  can be designed to compensate  $G_{id}$  to achieve high bandwidth and the desired phase-margin based on (27).

It is also seen that the ac current loop dynamics after the resonant frequency ( $L_{ac}$ ,  $C_{dc}$ ) will be mostly dominated by the ac boost inductor  $L_{ac}$ , and (27) can be simplified, as shown in (28).

$$G_{id} = \frac{\tilde{i}_{ac}}{\tilde{d}_{ab}} = V_{dc} \frac{2 + sZ_{in}C_{dc}}{d_{ab}^2 Z_{in} + sL_{ac} + s^2 Z_{in}L_{ac}C_{dc}} \quad (27)$$

$$G_{id}' = \frac{\tilde{i}_{ac}}{\tilde{d}_{ab}} = V_{dc} \frac{1}{sL_{ac}} \quad (28)$$

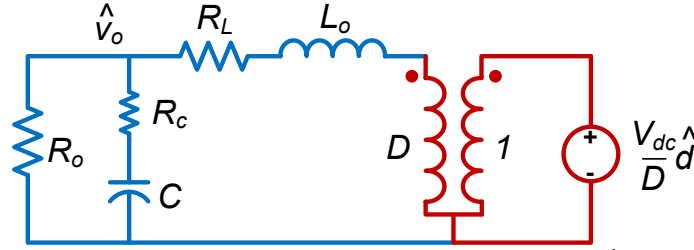
Since the designed bandwidth of the dc-link voltage loop is not beyond the double line-frequency (120Hz), the inner high-bandwidth ac current loop can be assumed to be ideal to design the voltage compensator  $H_v$  and the second-stage is regarded as a constant power load (CPL). Then the current-to-dc-link-voltage small-signal model in the low-frequency range is obtained in (29) [163, 171].  $h$  is the scaling factor of the PLL.

$$G_{iv} = \frac{\tilde{v}_{dc}}{\tilde{v}_c} = \frac{V_{acRMS}^2}{hV_{dc}} \frac{1}{sC_{dc}} \quad (29)$$

The variable  $G$  shown in (30) is applied to balance the power between the dc load and the ac grid, and also to improve the dc-link voltage regulation transient response speed especially during the load-step period. The variable  $V_{acRMS}$  denotes the grid voltage RMS value,  $V_{dc\_ref}$  is the dc-link voltage reference, and  $H_{LPF}$  is a low-pass-filer used to reduce the sensitivity to high-frequency noise.

$$G(s) = \frac{\sqrt{2}V_{dc\_ref}}{V_{acRMS}} \cdot H_{LPF}(s) \quad (30)$$

To design the second-stage voltage loop controller, the small-signal models of the second-stage converter in buck mode (rectification mode) and boost mode (regeneration mode) can be derived. In fact, it can be derived that the buck mode and the boost mode of the second-stage both have the same control-to-output small-signal model as shown in Fig. 2.29.

Fig. 2.29: Control-to-output small-signal model for 2<sup>nd</sup> stage

The dc loading impedance as well as the small-signal transfer functions vary with the dc-bus operation. However, in order to design a fixed compensator, the small-signal model under light resistor load  $R_o$  can be used as the worst case.

The control-to-output inductor current transfer function in (31) is used to design current compensator  $H_{io}$ , and the inductor-to-output voltage transfer function in (32) is used to design the output voltage compensator  $H_{vo}$ .

$$G_{iod} = \frac{\tilde{i}_o}{\tilde{d}} = V_{dc} \frac{1 + sR_o C_o}{R_o + sL_o + s^2 L_o C_o R_o} \quad (31)$$

$$G_{voi} = \frac{\tilde{v}_o}{\tilde{i}_o} = \frac{R_o}{1 + sC_o R_o} \quad (32)$$

The droop resistance  $R_d$  is included in the dc bus voltage loop to change the ECC converter static dc output impedance. The gain “ $A$ ” in Fig. 2.27 is anti-windup feedback to prevent the voltage-loop controller from saturation when ECC operates in current limit mode. A detailed compensator design procedure can be found in [172].

Several more control techniques must be implemented to effectively separate the dc average power and ripple power into two paths with a small dc-link capacitor. The dc-link voltage will bear a big 120 Hz ripple variation during full load conditions. This input variation will affect the output voltage  $V_o$  through the closed-loop audio susceptibility transfer function due to the finite loop-gain at 120 Hz. Fig. 2.30 shows that  $V_o$  has a 30 V voltage ripple at 120 Hz under 10 kW condition.

To suppress this voltage ripple, an additional gain is added to the control loop by implementing a resonant controller described below.

$$R(s) = k \frac{s}{s^2 + (2\omega_o)^2} \quad (33)$$



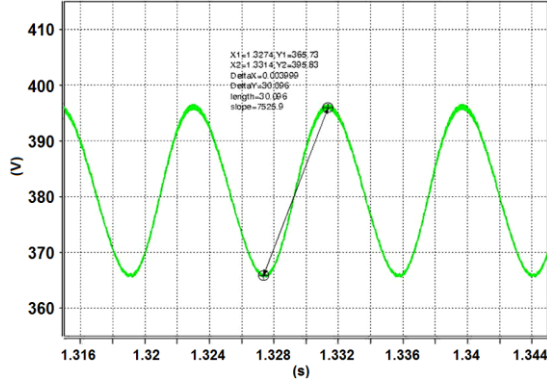


Fig. 2.30: Output voltage without a resonant controller  $R$

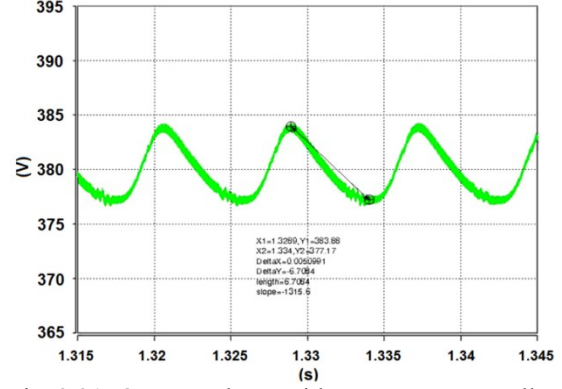


Fig. 2.31: Output voltage with a resonant controller  $R$

When  $\omega_o=2\pi 60 \text{ rad/s}$ , the resonant controller almost achieves infinite gain at 120 Hz. As such, the voltage ripple can be greatly reduced, as shown in Fig. 2.31, with only 7 V under full-load conditions.

In addition, the loop-gain at 120Hz provided by the dc-link voltage controller  $H_v$  is not very small. Hence, relatively large 120 Hz components are still included in the output of the dc-link voltage controller  $v_c$ , which is also the ac current magnitude reference as seen in Fig. 2.27, thus affecting the ac current regulation performance. As (34) shows, the PLL line-frequency signal will modulate with this double-line-frequency component in  $v_c$ , yielding third-order current harmonics.  $K_{Vdc}$  and  $K_{V120}$  are the dc-link voltage loop-gains at dc and 120 Hz, respectively; and  $\Delta v_{dc}$  and  $\Delta v_r$  are the dc and 120 Hz errors, respectively.

$$\begin{aligned} i_{ac\_ref} &= h \sin(\omega_o t + \varphi) \cdot v_c \\ &= h \sin(\omega_o t + \varphi) \cdot \left[ K_{Vdc} \cdot \Delta v_{dc} + K_{V120} \cdot \Delta v_r \sin\left(2\omega_o t + \varphi - \frac{\pi}{2}\right) \right] \end{aligned} \quad (34)$$

As shown in Fig. 2.32, the ac current has a considerable third-order harmonic component due in large part to this effect.

The notch filter in (35) can be used here to block the 120 Hz component in the voltage loop. The current loop can benefit from implementing this filter by reducing the 120 Hz component from  $v_c$ :

$$N(s) = \frac{\left(\frac{s}{2\omega_o}\right)^2 + 1}{\left(\frac{s}{2\omega_o}\right)^2 + s\frac{1}{2\omega_o Q_o} + 1} \quad (35)$$

In Fig. 2.33, the ac current presents almost the ideal case with the notch filter, and low THD of the ac current regulation can be readily attained.

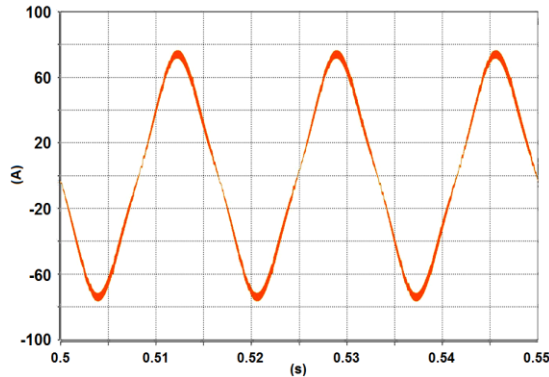


Fig. 2.32: Ac current without a notch filter

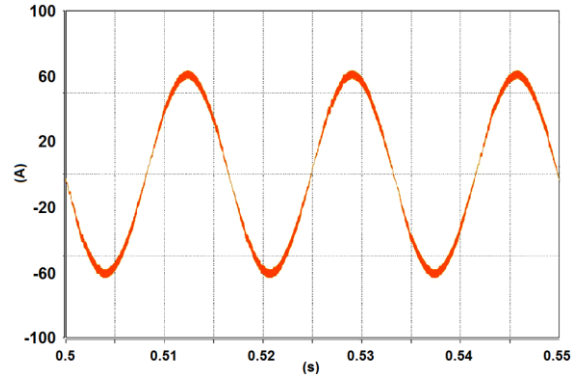


Fig. 2.33: Ac current with a notch filter

The dc-link voltage decoupling terms are applied in both controllers' current loops as depicted in Fig. 2.27, to reduce the loop-gain variation due to the low-frequency dynamics of dc-link voltage (120 Hz) in (27) and (31).

Perturbation of the ac grid should be also considered, especially during the weak grid application when the high-frequency dynamics of the grid cannot be ignored. Based on (28), an additional small-signal perturbation from the grid,  $v_{ac}$ , is added into the current loop, as shown in Fig. 2.34.  $v_{ab}$  is the full-bridge terminal voltage. The perturbation can be thereby canceled by the disturbance rejection term ( $v_{ac}/v_{dc}$ ) in the controller, as shown in Fig. 2.35.

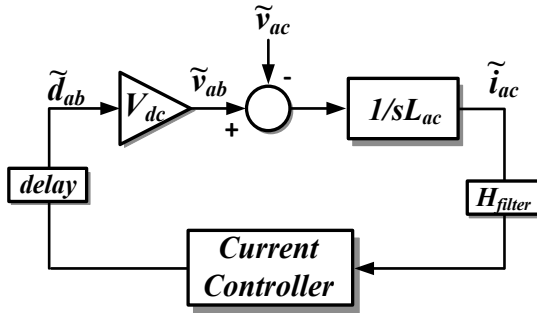


Fig. 2.34: Simplified ac current loop

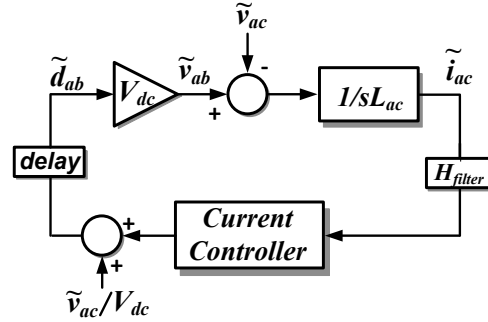


Fig. 2.35: Simplified ac current loop with disturbance rejection

All of the aforementioned small-signal transfer functions are used to design the multi-pole/zero linear controllers with the desired control bandwidth and phase/gain margins. The designed controllers will then be transferred to the discrete form via a continuous-to-discrete transformation, such as the Tustin transformation.

One key simulation case is shown in Fig. 2.36 and its result is shown in Fig. 2.37. In the simulation, the ECC first provides power to the dc load, and then the dc source starts pumping out the power. Eventually, the additional power is dispatched back to the ac grid via ECC. The ECC converter parameters can be found in Chapter 3.

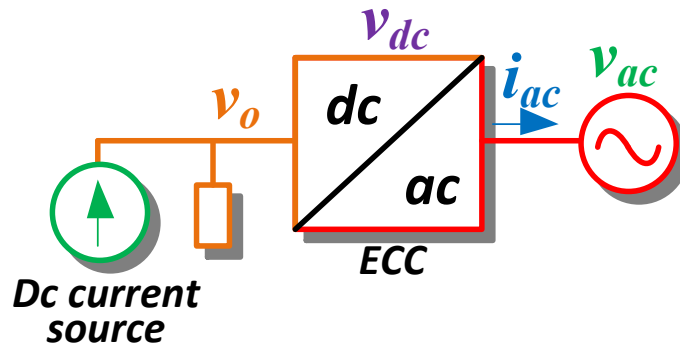


Fig. 2.36: Simulation system setup

Fig. 2.37 shows the mode transition from rectification mode to regeneration mode. The dc-link voltage ripple drops then increases. The ac current is initially converted from ac to dc and finally from ac to dc. The dc-bus voltage increases due to a 0.2 Ω droop resistor.

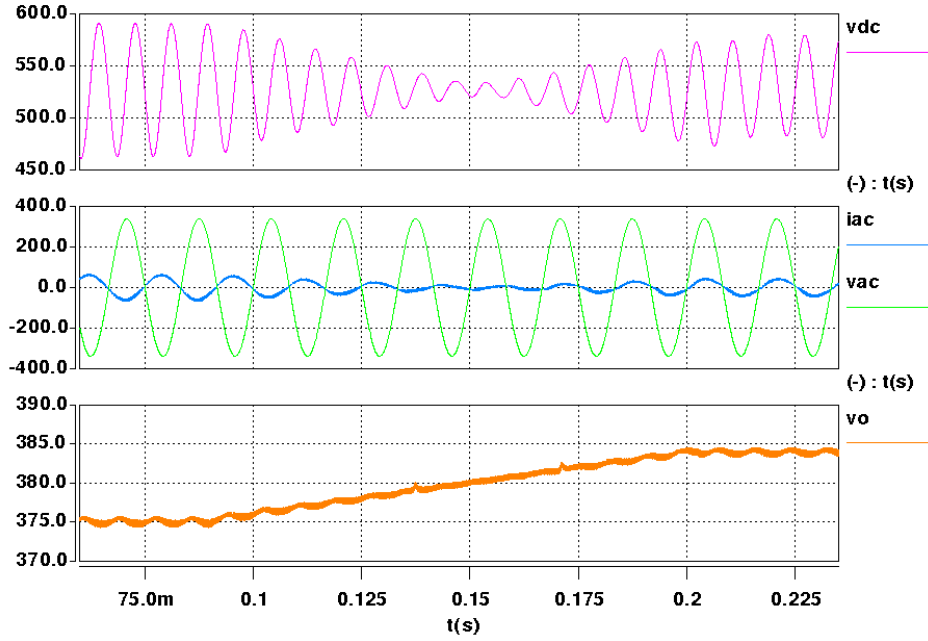


Fig. 2.37: Simulation of mode transition

### 2.3.4. VOLUME COMPARISON AND HARDWARE DEVELOPMENT

An extra dc LC filter ( $L_o$ ,  $C_o$ ) is required for the second-stage converter to produce a constant dc-bus voltage. The small dc-link capacitor will have an impact on the size of the dc-side filter, and should be considered when evaluating the total volume.

The design of dc inductor  $L_o$  and capacitor  $C_o$  are based on the current ripple  $\Delta i_o$  and capacitor voltage ripple  $\Delta v_o$ , as shown below in (37) and (38).

$$L_o = T_s \frac{(1-d)V_o}{2\Delta i_o} = \frac{T_s}{2\Delta i_o} \left( V_o - \frac{V_o^2}{V_{dc}} \right) \quad (35)$$

$$C_o = T_s \frac{\Delta i_o}{8\Delta v_o} \quad (36)$$

The physical design of  $L_o$  should consider the maximum value of  $I_o$  when  $v_{dc}$  reaches the maximum value, as shown in (37), to avoid core saturation.

$$I_{o\_max} = \frac{P_{av}}{V_o} + \frac{V_o T_s}{2L_o} \left( 1 - \frac{V_o}{V_{av} + \frac{P_{av}}{2V_{av} C_{dc} \omega_o}} \right) \quad (37)$$

The design of the ac filter  $L_{ac}$ ,  $C_{DM}$ ,  $L_{ac2}$  is presented in Chapter 3.

The system theoretical design parameters and volume of the passive and active components by using unipolar modulation at 20 kHz switching frequency are shown in Table II. The dc-link capacitor volume is calculated based on film-type capacitors (450 V rating for  $C_o$ , 800 V rating for  $C_{dc}$ ) available on the market. The inductor volume is calculated using the amorphous alloy CC type magnetic core, chosen due to its high saturation flux-density as well as low high-frequency core loss.

The results show that, for the dc nano-grid application, a large improvement in power-density is accomplished by the two-stage topology with a reduced dc-link capacitor, in addition to fulfilling ECC requirements.

Table 2.2: Main volume comparison between two-stage topology and full-bridge where  $f_s = 20$  kHz

Topology	Full-bridge	Two-stage
$V_{av}$	$V_{av} = V_o = 380$ V	$V_{av} = 550$ V
Dc bus voltage Vo ripple	10 V pp	
$C_{dc}$	6.9 mF (10.54 Liter)	360 $\mu$ F (1.14 Liter)
$L_{ac1}$	180 $\mu$ H (0.23 Liter)	260 $\mu$ H (0.3 Liter)
$L_{ac2}$	24.8 $\mu$ H (0.04 Liter)	24.5 $\mu$ H (0.04 Liter)
$C_{DM}$	10 $\mu$ F (0.03 Liter)	10 $\mu$ F (0.03 Liter)
$C_o$	0 $\mu$ F (0 Liter)	100 $\mu$ F (0.1 Liter)
$L_o$	0 $\mu$ H (0 Liter)	200 $\mu$ H (0.15 Liter)
Heatsink and Fan	0.41 + 0.2 Liter	0.75 + 0.3 Liter
Device	0.16 Liter	0.2 Liter
Efficiency	95.2%	93.0%
Total Volume	11.64 Liter	3.16 Liter

A 10 kW high-power-density bi-directional PWM converter was developed and shown in Fig. 2.38. A fifth-generation 1200V/150A three-phase intelligent power module (IPM) and a pin-type heatsink with fans are used as the active component and cooling device in the system, respectively. Besides the main components, dc-side and ac-side EMI filters are also implemented in the system. A more detailed discussion on the ac and dc-side interface solutions is presented in Chapter 3.

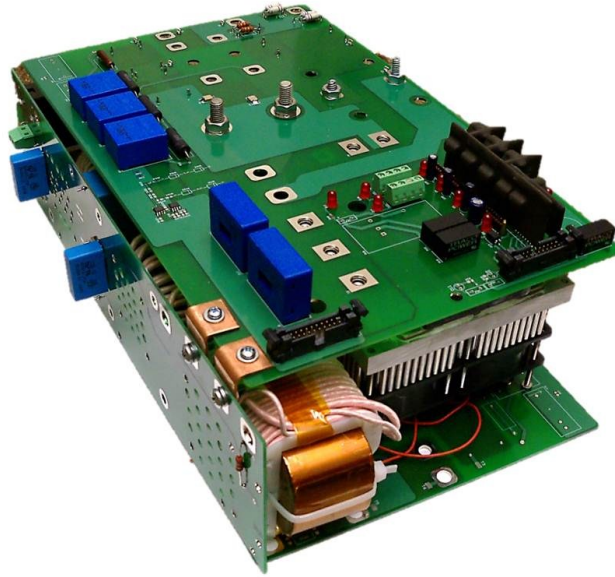


Fig. 2.38: 10 kW ECC converter prototype

### 2.3.5. EXPERIMENTAL EVALUATION

The ac/dc system test setup is shown in Fig. 2.39 and Fig. 2.40, which includes one 25 kVA split-phase single-phase transformer to supply the 240 V rms ac bus, the ECC converter, the BDC, and one ac power supply. It should be noted that the BDC is a discontinuous-current-mode (DCM) three-phase interleaved dc-dc converter [161], and the battery is a 330V lithium-ion battery pack manufactured by Saft. An ac power supply emulates the grid, and the BDC injects power to the dc system. There are loads on both the ac and dc sides. If the injected dc power is less than that required by the dc load, the converter will regenerate the power from the dc-side to ac-side.

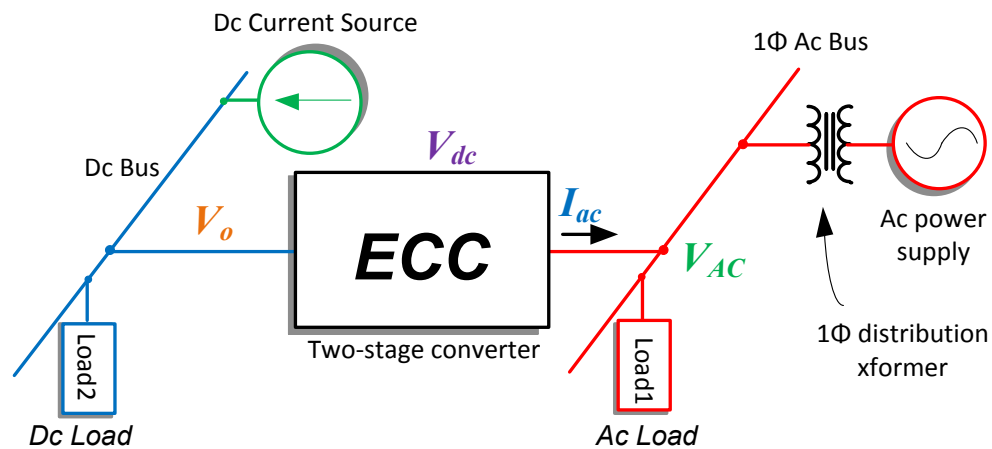


Fig. 2.39: System test setup

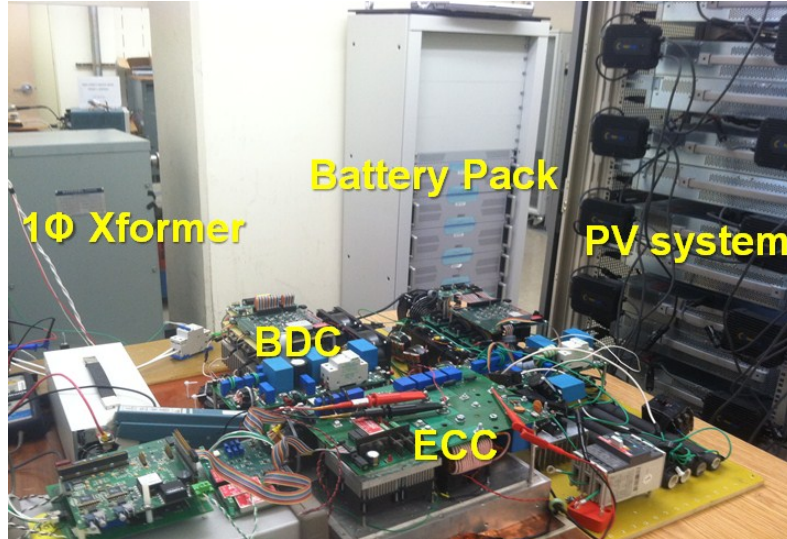


Fig. 2.40: Dc nano-grid testbed setup

Bi-directional power tests under rectification mode (ac to dc) and regeneration mode (dc to ac) are shown in Fig. 2.41 and Fig. 2.42, respectively. For the regeneration mode test, total of 5.9 kW power is generated by other dc sources. 1.5 kW loads are placed on the dc side, while 4.4 kW power is dispatched to the grid. Fig. 2.43 shows the results under a 5 kW condition, and shows that the advanced control regulates the dc nano-grid bus  $V_o$  at 380 V with a small voltage ripple ( $<2 V_{pp}$ ); even the ripple of dc-link voltage  $V_{dc}$  is relatively large (120 V<sub>pp</sub>) due to the reduction of the dc-link capacitor  $C_{dc}$ . The seamless transition from the rectification mode to the regeneration mode is shown in Fig. 2.44. This shows that the energy flows freely in either direction between the ac and dc sides without affecting the dc-bus voltage  $V_o$ .

Fig. 2.45 and Fig. 2.46 show how the notch filter improves the ac current regulation performance as discussed above. It is seen that, in comparison with Fig. 2.46, the ac current in Fig. 2.45 bears relatively large third-order current harmonics without the notch filter. The ac current waveform under regeneration mode is shown without and with the grid voltage perturbation cancellation terms in Fig. 2.47 and Fig. 2.48, respectively. The THD of the current is also improved by adding this additional term to the controller. Finally, Fig. 2.49 shows the 3 kW load-step transient response when the dc current source pumps the dc current. The converter changes from rectification mode to regeneration mode, while a dc-link voltage spike of only 30 V is observed during this transient due to the fast response of the dc-link voltage.

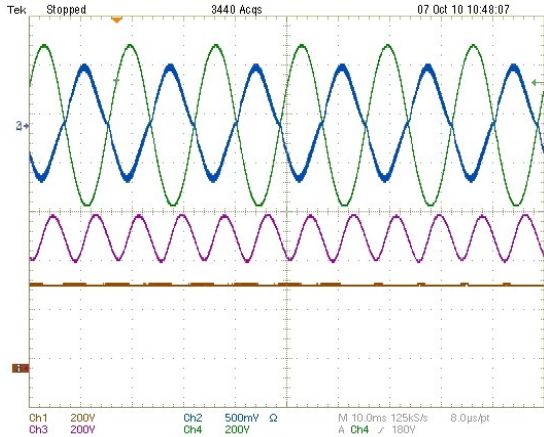


Fig. 2.41: 9 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [200V/DIV]

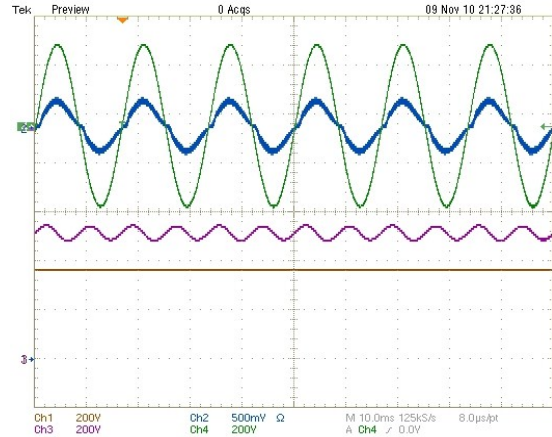


Fig. 2.42: 9 kW regenerative mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [200V/DIV]

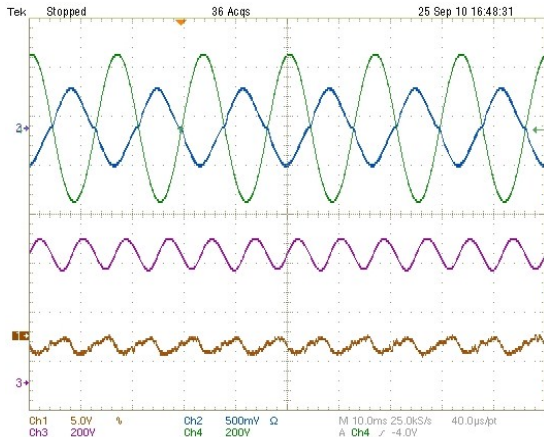


Fig. 2.43: 6 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [5V/DIV]

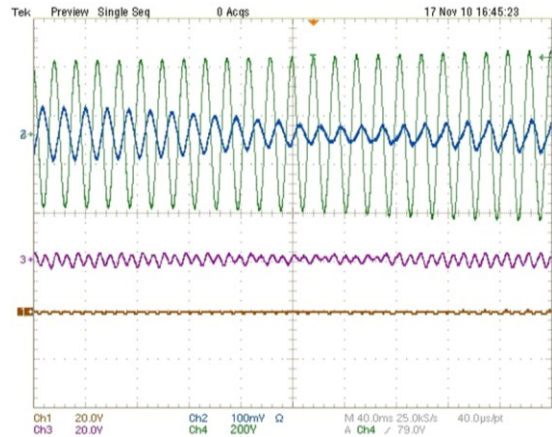


Fig. 2.44: 9 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [10A/DIV],  $V_{dc}$  (purple) [20V/DIV],  $V_o$  (orange) [20V/DIV]

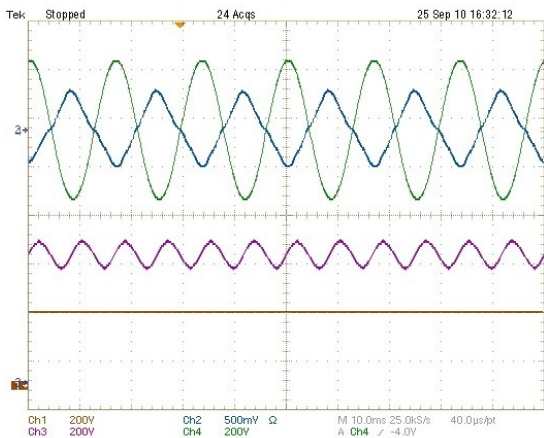


Fig. 2.45: 6 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [5V/DIV]

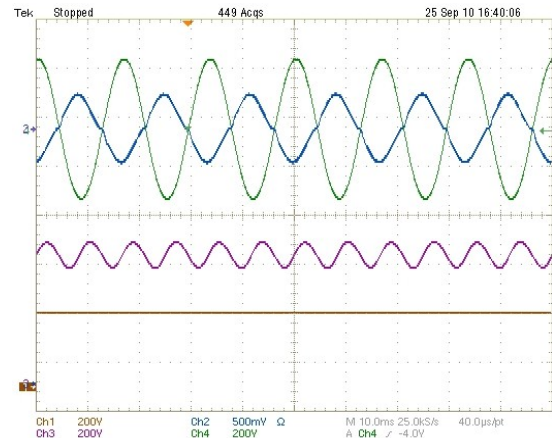


Fig. 2.46: 6 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [5V/DIV]



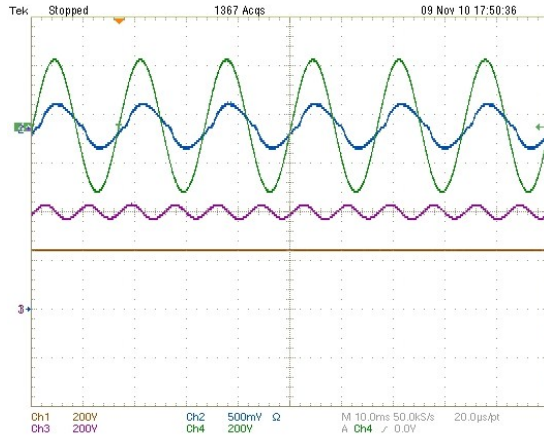


Fig. 2.47: 6 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [5V/DIV]

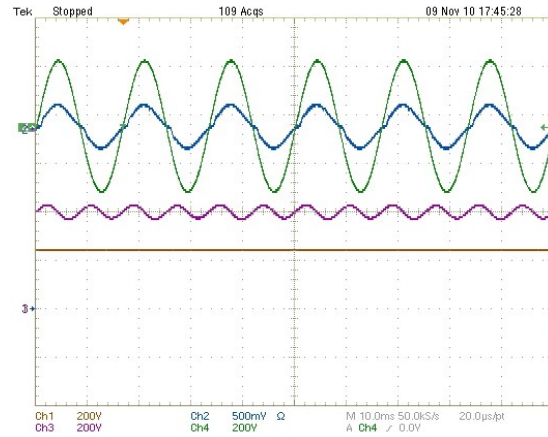


Fig. 2.48: 6 kW rectifier mode test.  $V_{ac}$  (green) [200V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [200V/DIV],  $V_o$  (orange) [5V/DIV]

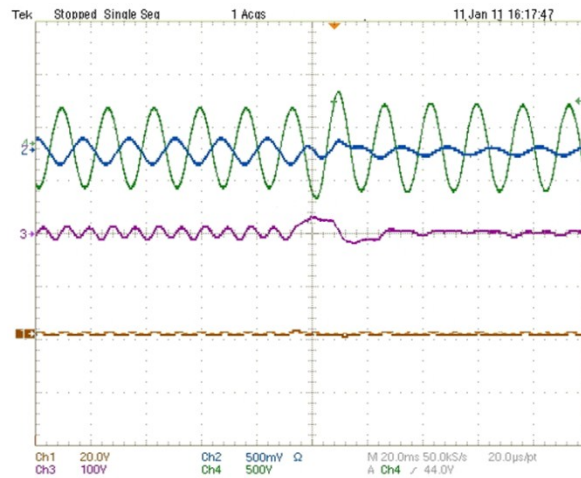


Fig. 2.49: 3 kW rectifier mode test.  $V_{ac}$  [500V/DIV],  $I_{ac}$  (blue) [50A/DIV],  $V_{dc}$  (purple) [100V/DIV],  $V_o$  (orange) [20V/DIV]

### 2.3.6. CONCLUSION

This chapter describes the components of a dc electronic distribution system in residential buildings as a future distribution system solution to integrate multiple renewable energy sources, energy storage devices, and electronic loads. A two-stage high power density single-phase bi-directional PWM converter is investigated for use in a dc renewable energy system for residential power applications. This converter can operate as a single power module with a very small dc-link capacitor, which is proven to be possible by a power-based analysis. With the goal of realizing this converter, small-signal models with a bi-directional control structure and control design procedure are presented, and experiment shows they work well. Besides the dc nano-grid, this converter is also

applicable as a high power-density bi-directional charger for plug-in hybrid electric vehicle (PHEV) applications.

## **Chapter 3. DESIGN AND OPTIMIZATION OF POWER FILTERS FOR AC-DC BUS-INTERFACE CONVERTERS**

In this chapter, the focus is on the filter design of the bi-directional converter system for ac-dc bus-interface.

The major power quality requirement, EMI regulations, grid codes, and relevant issues are first presented. The high-frequency CM noises and the associated leakage current issue in grid-interface converter system are discussed in detail, and a solution using a modified ac filter is provided to mitigate such issues. An active filter solution is then proposed to decouple the low-frequency CM interactions between ac and dc side. The EMI filter trade-off design on both dc and ac-side for such bi-directional converter applications are presented lastly.

### **3.1. POWER QUALITY ISSUE AND CURRENT TECHNOLOGIES**

#### **3.1.1. POWER QUALITY AND ITS STANDARD**

Power quality and the corresponding environmental-impact are gaining more attention in the chain of the electric power processing and delivery. Bad quality of the electric power wears out the system equipment quickly, increases the cost of maintenance, results in system failure or nuisance shut down, and poses strong negative influence to environments [173, 174]. Power electronics not only reshapes the electric properties, such as voltage and current, but also needs to convert the electric power into a more clean and reliable form [175].

Power quality (PQ) is the set of limits of electrical properties that allows electrical systems to function in their intended manner without significant loss of performance or life. About 70% to 80% of all PQ related problems can be attributed to faulty connections and/or wiring [173]. Power frequency disturbances, electromagnetic interference, transients, harmonics and low power factor are the other problems that are related to the source of supply and types of load [174].

As an example, Fig. 3.1 shows several utility voltages waveform related to the power quality, and many reasons can affect the voltage power quality.

Some of the distortions may come from power electronics. The EMI emission mostly comes from the high-speed  $dv/dt$  and  $di/dt$  events during the high-frequency switching commutations, the voltage surge/dip may come from the start period of motor drive. Intermediate frequency interaction between constant power load and system could result in the voltage swell or oscillation. The diode-rectifier can easily yield the low-frequency harmonics.

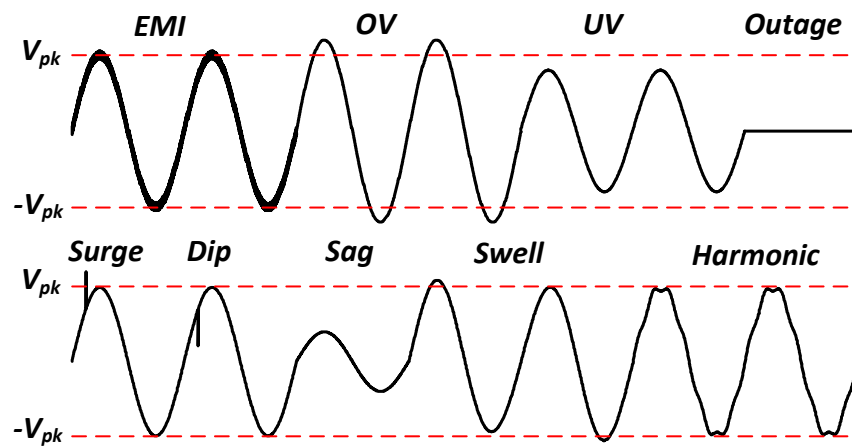


Fig. 3.1: Some utility voltage waveforms related to the power quality

Lots of regulation standards specify the interconnection requirement [123, 124, 176, 177] of distributed generation (DG) units in electric power system, especially in low-voltage distribution networks. Also, many standards define the interconnection requirement for electric loads [178-180], such as appliances, variable-speed motor drives. Due to the dynamic decoupling and the bi-directional operation achieved by the ECC converter, the whole dc system will be either like a single DG unit when the power is dispatched to the grid or like a load when the power is delivered to the dc-side [15]. Thus, both standards for DGs and electric loads have to be applied to the design of ECC converter to interface the ac low-voltage distribution system from the dc system.

As the ECC converter delivers the power to the ac grid, behaving like a current source, the ac current PQ requirement, as shown in Table 3.1, defined by IEEE 1547 has to be applied.

Table 3.1: Maximum harmonic current distortion in percent of current

Individual harmonic order $h$ (odd harmonics)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 < h$	Total demand distortion (TDD)
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

Even harmonics are limited to 25% of the odd harmonic limits above

The current harmonics in low-frequency range ( $h < 17$ ) are closely related to the converter interaction with the system and loads, which require the converter control to address them. Some of the control issues are given in the previous chapter.

On the other hand, when the ECC converter behaves as an ac load, the mitigation of high-frequency (150 kHz to 30 MHz) electromagnetic interference (EMI) noise emission to the ac grid is a consideration to reduce the pollution and to minimize the interference to the adjacent devices. Recently, the EMI standards with the similar regulation requirement are also applied to the ac source converters, such as PV inverter. In addition, many other utility-interface requirements are valid to the bus-interface bi-directional converter, e.g., anti-islanding protection, low-voltage ride-through (LVRT), and ancillary functions, which, however, are more related to control-design and will not be discussed in this chapter. Other than aforementioned regulation requirements, lots of PQ standards are applied in every engineering phase of the commercial production.

In terms of the dc-side, currently there are several organizations, e.g., EPRI, IEC, and Emerge Alliance, developing different dc system standards; however, there is no public and uniform standard for such residential dc system now. Currently, power quality and EMI can still be used as the design consideration similarly as the ac-side. Mostly, ECC behaves as a voltage source on dc-side, thus the power quality of output voltage is a design aspect. The dc-side conductive EMI noises should be minimized, though no specific standards, especially when relative long dc-cables are deployed. There are several publications on the dc-side EMI study in residential PV systems [91-94]. Some other standards on dc-system in different applications, e.g., the dc distribution system in aircraft power system can be a reference. According to [181], the power quality of differential-mode (DM) and common-mode (CM) dc-bus voltage are required to be maintained within a small voltage ripple. If in future there are more specific standards

available, the dc-side interface requirement may change the design of filter and/or power-stage topology.

### **3.1.2. AC LOW-VOLTAGE DISTRIBUTION PRACTICE**

System grounding schemes and type of ac distribution systems that the ECC interfaces to are also the factors to consider in the design of the converter system.

The typical low-voltage (LV) ( $<2400$  V) distribution system in North America is shown in Fig. 3.2, while the LV distribution system in most European countries and China is shown in Fig. 3.3. It is seen that, a split-phase step down distribution transformer is used in North America to feed the end-users. On the secondary side of the transformer is the split-phase 240V rms single-phase system. The utility converter can be tied to it. In Europe, by contrast, they feed a three-phase system into the end users, and the load can be connected between one of three hot wires and the neutral wire. So, a three-phase or single-phase converter system can be tied. In Europe, single-phase system, as seen in Fig. 3.3, normally is used to supply users in the rural areas.

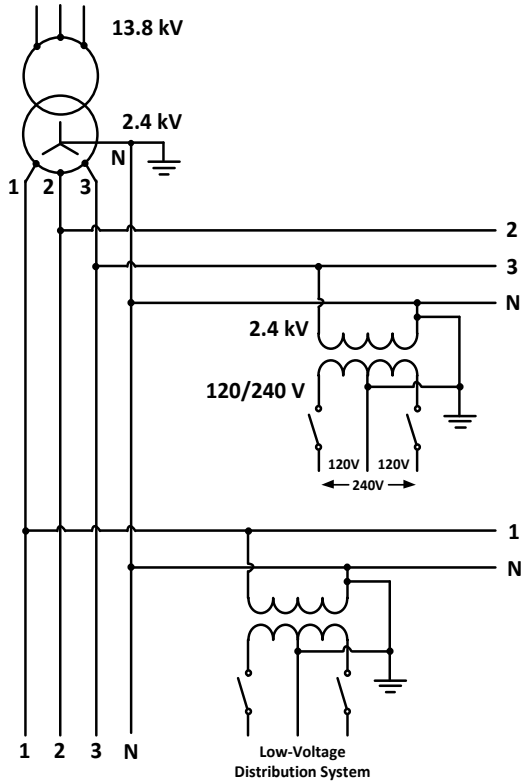


Fig. 3.2: Low-voltage distribution system in North America

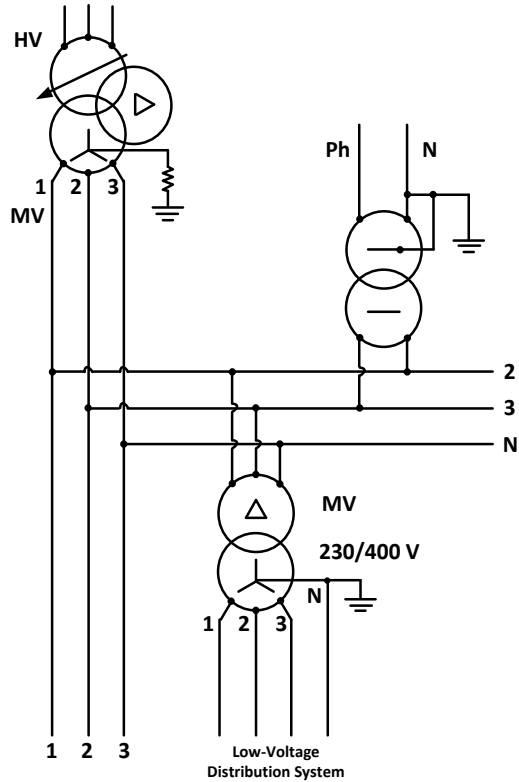


Fig. 3.3: Low-voltage distribution system in Europe and China

It is seen that there would be three types of utility in low-voltage distribution system for converter system to connect. Fig. 3.4 is the single-phase split-phase system. The voltage across line to neutral is 120 V rms, and the voltage across line to line is 240 V rms. Fig. 3.5 shows the asymmetrical single-phase system, whole voltage is 240 V rms. Fig. 3.6 shows the three-phase grid where the phase to neutral voltage is around 230 V rms. All aforementioned value varies in different countries.

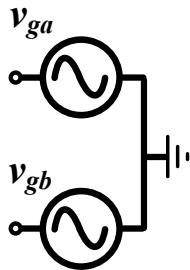


Fig. 3.4: Split-phase single-phase system

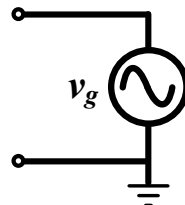


Fig. 3.5: Asymmetrical single-phase system

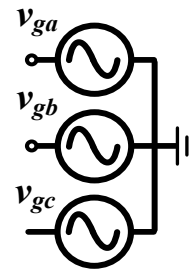


Fig. 3.6: Three-phase system

Notice that the corresponding CM voltage of these three types of utilities can be defined from (1) to (3), respectively.

$$v_{CM} = \frac{1}{2}(v_{ga} + v_{gb}) = 0 \quad (1)$$

$$v_{CM} = \frac{1}{2}(v_g + 0) = \frac{1}{2}v_g \quad (2)$$

$$v_{CM} = \frac{1}{3}(v_{ga} + v_{gb} + v_{gc}) = 0 \quad (3)$$

### 3.2. HIGH-FREQUENCY LEAKAGE CURRENT REDUCTION USING PASSIVE FILTER

The discussion covers the ECC converter interface to three types of the low-voltage distribution system mentioned above. The detailed design is presented in single-phase case as shown below.

#### 3.2.1. LEAKAGE CURRENT ISSUE IN SINGLE-PHASE SYSTEM

Leakage current issue exists in various industrial equipment and facilities, especially in the switching mode converters. For instance, leakage current wears out the bearing quickly in industrial motor systems; many of human electric shock incidences are also due to leakage current. In bus-interface converters, leakage current presents even more severe issues which potentially could damage lots of involved equipment. PV inverter, a bus-interface source converter, suffers the leakage current issue due to a large stray capacitance between ground and PV panel.

At the distribution level, most of the solar systems are single-phase installations [60, 61, 70, 72]. The photovoltaic (PV) panels are tied in a series/parallel form, and connected to the grid via a central PV inverter. Alternatively, an individual PV panel is directly tied to the grid through a small microinverter to avoid the partial shading problem due to the series and parallel connections. There are also some three-phase solar power systems [71, 89] either in the higher distribution voltage levels or in some countries where the three-phase low-voltage distributions systems are employed.

Many topologies for PV systems had a galvanic transformer that isolates the PV panels from the grid [52, 55, 183]. Not only does the isolation ensure safety, but also it reduces the EMI noise and steps up or step down dc voltage levels. However, the line-frequency transformer suffers from large weight and size [71, 89]. In addition the high-



frequency transformer requires more switching devices and conversion stages, significantly reducing the overall system efficiency, performance and reliability.

The transformerless topology has gotten attention recently, both in industry and academia, due to its simple topology, high efficiency, and reliability, especially in up-to-10 kW power rating applications. Example is seen in solar systems, of which the isolation is not required in many countries. The full-bridge converter, as discussed in previous chapter, is a well-accepted topology in single-phase power conversion applications. Besides the PV application, it is also used as the rectifier to deliver the ac power to dc loads or batteries [52], and in the bi-directional operation. Such applications can be found in electric vehicle (EV) charger [182, 183] and residential ac/dc hybrid distribution systems [15].

The unipolar PWM modulation, which is known as the three-level modulation, employs two sinusoidal references with the opposite signs to modulate each phase-leg. It is normally applied onto the full-bridge topology due to the small differential-mode (DM) switching noise, which leads to a smaller ac passive filter size. However, the unipolar modulation generates a large dc-side high-frequency leakage current flowing to the ground in the transformerless topologies [186], which has a profound impact, such as aging effect, on dc-side source/load and human safety [184, 185]. To ensure the safety of equipment and personnel, the leakage current must be suppressed to a certain level [185].

Over the past few years, there have been many research publications [70, 82, 186] and industrial practices [83-86] established to tackle these issues. Several modified full-bridge topologies are proposed in Fig. 3.7 to Fig. 3.10.

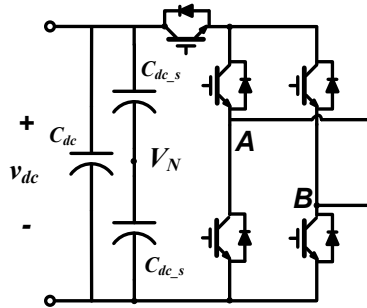


Fig. 3.7: H5 inverter

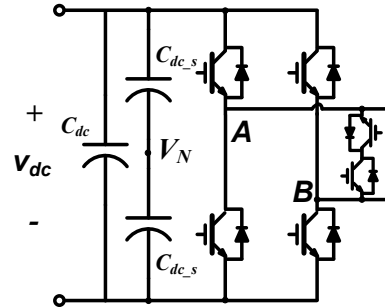


Fig. 3.8: HERIC inverter

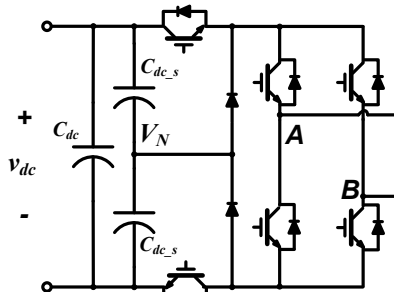


Fig. 3.9: FB-DCBP inverter

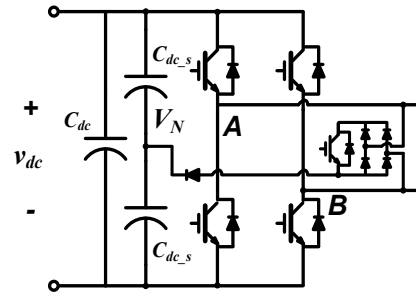


Fig. 3.10: FB-ZVR inverter

The common feature in the above modified full-bridge topologies is that the extra dc or ac switches provide isolation or there is a bypass loop to avoid the direct CM loop between the dc source and ac grid during the “zero voltage state,” when terminals A and B are both clamped to the positive or negative dc-rail.

The modified bridgeless PFC topology and Karschny topology are discussed in [186]. These topologies eliminate the leakage current because of a direct connection between the output neutral and the negative terminal of the PV array.

However, these topologies have some major drawbacks. They experience the additional power loss and cost due to more switches. The sequences of the control signal for the additional switches will be more complicated if the dead-time is considered. Their reliability and lifetime also degrade at a rate inversely proportional to the switch-counts. Moreover, bi-directional operation is not well-documented.

Reference [188] also proposes to use additional CM capacitors connected between the mid-point of dc-link and ground to compensate the effects on leakage current by considering the phase-leg parasitic parameters. However, the CM capacitance is limited by safety standards, and is also sensitive to system setup. Reference [71] proposes to use

the multi-level neutral-point-clamp topology in three-phase applications. However, it requires a four-wire system and the selection of PWM modulation strategy is limited.

This paper analyzes and addresses the dc-leakage current issues and their characteristics at the inverter or rectifier operation of the full-bridge topology. A high-density ac passive filter structure is proposed for use with the full-bridge topology to reduce the dc-side leakage current level without introducing extra components. Aside from the dc-side leakage current reduction, it also provides additional ac-side EMI CM noise mitigation, thereby reducing the ac EMI filter size and design effort. The impact of the ac grid grounding scheme on the leakage current level is also discussed.

### 3.2.2. HIGH-FREQUENCY LEAKAGE CURRENT ANALYSIS IN SPLIT-PHASE SINGLE-PHASE SYSTEMS

Fig. 3.11 shows the full-bridge inverter with an ac harmonic filter. The full-bridge is connected to the split-phase (120 V rms/ 240 V rms) single-phase grid, which is normally seen in North America low-voltage residential distribution systems.  $v_{ga}$  and  $v_{gb}$  have the same voltage level (120 V rms) but opposite phases. The mid-point is grounded as shown in Fig. 3.11. The L-C-L type ac filter ( $L_{ac1}$ ,  $C_{DM}$ ,  $L_{ac2}$ ) is the most accepted type of harmonic filter to comply with the grid-interface power quality requirement in IEEE 1547.

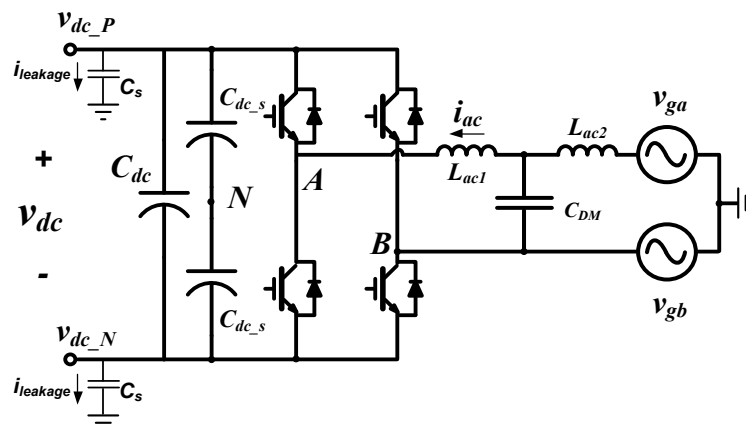


Fig. 3.11: Full-bridge inverter interconnected with grid

The unipolar PWM modulation employs two sinusoidal references with the opposite signs to modulate each phase-leg. For the bipolar PWM modulation, two diagonal switches share the same PWM signal. The “hybrid” modulation (discontinuous PWM modulation) modulates the phase-legs using high-frequency PWM during half line-cycle

and clamps the phase-leg terminal voltage at either positive or negative dc-rail during another half cycle.

The effects of different PWM schemes can be evaluated by exploring the generated differential-mode (DM) and common-mode (CM) terminal voltages, which are defined in (4) and (5).  $V_{AN}$  and  $V_{BN}$  are the terminal voltages of two phase-legs with respect to the mid-point of dc-link  $N$ , as labeled in Fig. 3.11.

$$v_{DM}(\omega) = \frac{1}{2}[v_{AN}(\omega) - v_{BN}(\omega)] \quad (4)$$

$$v_{CM}(\omega) = \frac{1}{2}[v_{AN}(\omega) + v_{BN}(\omega)] \quad (5)$$

Fig. 3.12 shows the unipolar modulation scheme and its corresponding DM and CM terminal in two switching periods. Since each of the split dc-link capacitors  $C_{dc_s}$  shares half of the dc-link voltage  $v_{dc}$ , the terminal voltages  $V_{AN}$ ,  $V_{BN}$  step up/down between  $0.5v_{dc}$  and  $-0.5v_{dc}$ . The terminal noise spectrums of  $V_{AN}$  and  $V_{BN}$  can be obtained as shown in (3) and (4) by applying the Double-Fourier analysis. Notice that  $J_n$  in (3) and (4) is the Bessel type I function [25], and  $\omega_o$  and  $\omega_s$  are the line-frequency and switching-frequency respectively.

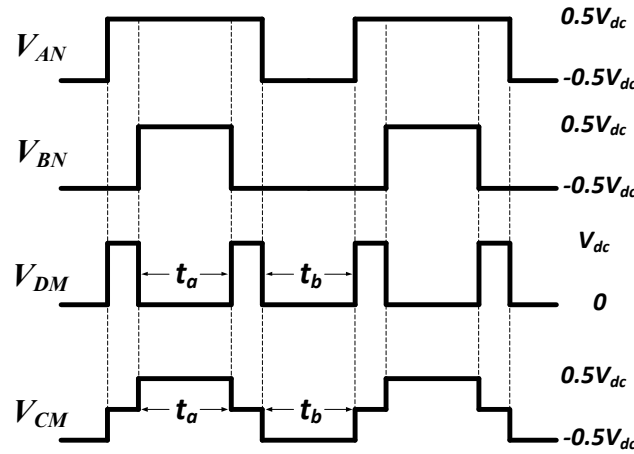


Fig. 3.12: Terminal voltage of each phase-leg, DM and CM voltage

$$V_{AN} = \frac{1}{2}V_{dc}M \cos(\omega_o t) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2V_{dc}}{\pi m} J_n\left(m \frac{\pi}{2} M\right) \sin\left([m+n]\frac{\pi}{2}\right) \cos(m\omega_s t + n\omega_o t) \quad (6)$$

$$V_{BN} = \frac{1}{2}V_{dc}M \cos(\omega_o t - \pi) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2V_{dc}}{\pi mn} J_n\left(m\frac{\pi}{2}M\right) \sin\left([m+n]\frac{\pi}{2}\right) \cos(m\omega_s t + n[\omega_o t - \pi]) \quad (7)$$

The spectrums of the DM and CM noise of unipolar modulation scheme are shown in Fig. 13 and Fig. 14, respectively. The average value of dc-link voltage is assumed to be 600 V, the switching frequency is 20 kHz, and the line frequency is 60 Hz. The value of modulation index  $M$  is shown in (8).

$$M = \frac{V_{ac-pk}}{V_{dc}} = \frac{240\sqrt{2}}{600} = 0.5656 \quad (8)$$

In Fig. 3.13, the first switching harmonics appear at two times of the switching frequency, rendering a small DM switching noise. As such, the unipolar modulation scheme yields a smaller ac harmonic filter, i.e., four-times smaller than the bipolar modulation scheme [189]. In addition, unipolar modulation features a smaller magnetic core loss than bipolar modulation due to a small flux swing. Although the CM noise of the bipolar modulation is theoretically zero, high-frequency CM noises still exists in practices due to non-ideal conditions. The 40 kHz “hybrid” modulation features the same DM noise spectrum distribution as the 20 kHz unipolar modulation.

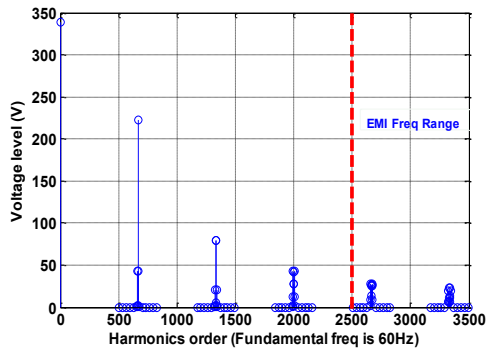


Fig. 3.13: Spectrum of DM noise

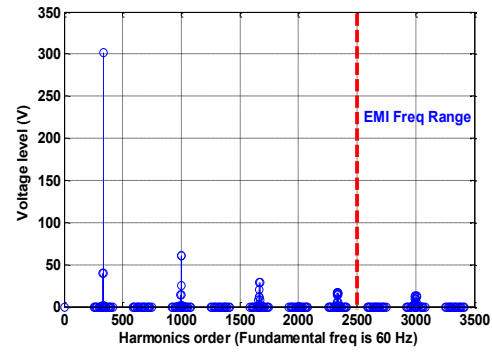


Fig. 3.14: Spectrum of CM noise

Fig. 3.13 indicates that the unipolar modulation generates significant CM noise, and the first switching-harmonics (20 kHz) contribute most of the CM noise. The “hybrid” modulation generates both line-frequency and switching-frequency CM noises. As shown in Fig. 3.13 and Fig. 3.14, both DM and CM switching noise that is higher than 150 kHz should be attenuated by the ac EMI filter.

Due to the low-impedance grounding scheme of the ac grid, the generated CM noise will appear on both positive and negative dc-rails. The leakage current  $i_{leakge}$  is induced flowing into the ground through the stray capacitors  $C_s$ . The leakage current can be estimated by (9), where  $C_s$  is the equivalent stray capacitance of each dc-rail and  $v_{dc\_N\_RMS}(\omega)$  is the RMS value of the negative dc-rail CM voltage at  $\omega$ . The term “2” in (9) means both the positive and negative dc-rail contributes equally to the dc-side CM leakage current due to the symmetrical topology and PWM scheme.

$$i_{leakage} \approx \sqrt{\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [2(m\omega_s + n\omega_o) \cdot C_s \cdot v_{dc\_N\_RMS}(m\omega_s + n\omega_o)]^2} \quad (9)$$

This leakage current issue can also be explored clearly by investigating the CM equivalent circuit, which is valid up to several times of switching-frequency. Fig. 3.15 can be obtained by modeling each phase leg as an ideal voltage source with respect to the negative dc-rail. If the interested frequency is not high, e.g., lower than a few hundred kHz, the impedances of the equivalent voltage sources can be ignored. Then these two voltage sources can be reformed as the DM and CM voltage sources, as shown in Fig. 3.16.

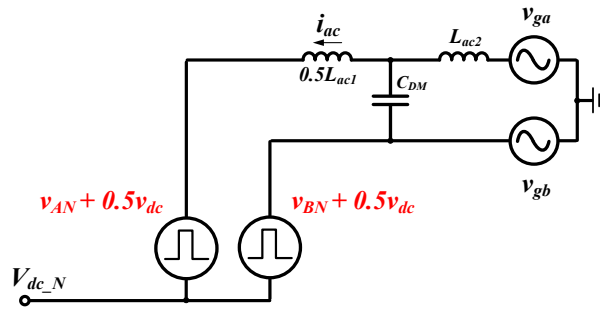


Fig. 3.15: Equivalent circuit of full-bridge converter

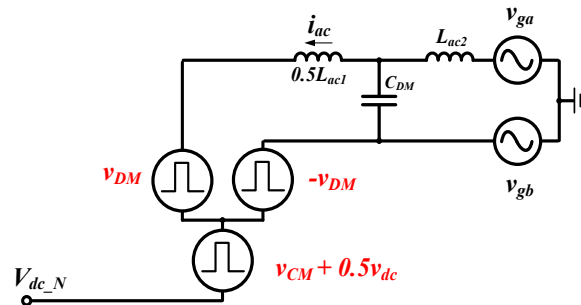


Fig. 3.16: Simplified equivalent circuit of full-bridge converter

In Fig. 3.16, the dc-link voltage  $v_{dc}$  in (10) consists of two components: dc average value  $V_{dc}$  and the low-frequency ripple  $v_{ripple}$ . If the full-bridge operates as an inverter,  $v_{ripple}$  is the low-frequency ripple from dc source. If the full-bridge operates as a rectifier,  $v_{ripple}$  is the 120 Hz component due to ripple power delivered by the single-phase grid.

$$v_{dc} = V_{dc} + v_{ripple} \quad (10)$$

It can be derived that the  $v_{dc\_N}$  will be in (11)

$$\begin{aligned} v_{dc\_N} &= -v_{BN} - 0.5v_{dc} + v_{gb} \\ &= -v_{CM} - 0.5V_{dc} - 0.5v_{ripple} + 0.5v_{DM} + v_{gb} \end{aligned} \quad (11)$$

It is seen that, besides the CM voltage source  $v_{CM}$ , the DM voltage source  $v_{DM}$  also becomes the contributor to the dc-side CM voltage, mostly due to the asymmetrical ac passive filter configuration. However, if a symmetrical ac L-C-L harmonic filter is implemented, the equivalent circuit would be shown in Fig. 3.17. Hence, the CM equivalent circuit is obtained in Fig. 3.18 by considering only the CM components due to the symmetrical configuration.

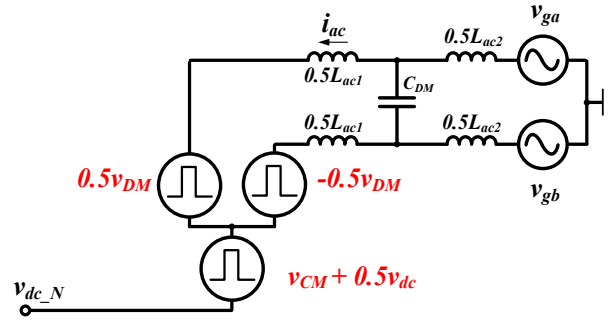


Fig. 3.17: Equivalent circuit of full-bridge inverter

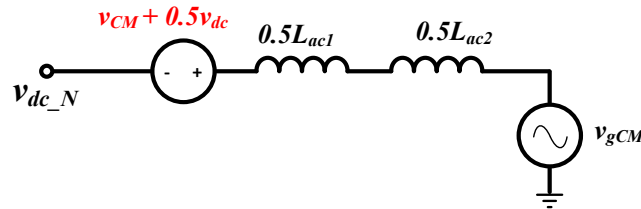


Fig. 3.18: CM equivalent circuit of full-bridge converter

In Fig. 3.18,  $v_{gCM}$  is the CM voltage of the utility grid, which is defined in (12).

$$v_{gCM} = \frac{1}{2}(v_{ga} + v_{gb}) \quad (12)$$

The CM voltage of the negative dc-rail  $v_{dc\_N}$ , can be determined from Fig. 3.18, as shown in (13).

$$\begin{aligned} v_{dc\_N} &= -v_{CM} - 0.5v_{dc} + v_{gCM} \\ &= -v_{CM} - 0.5V_{dc} - 0.5v_{ripple} + v_{gCM} \end{aligned} \quad (13)$$

It is seen that  $v_{dc\_N}$  mainly consists of four frequency components: the 60 Hz component from  $v_{gCM}$ , the dc value from  $V_{dc}$ , the low-frequency ripple, e.g., 120 Hz, from  $v_{ripple}$ , and the switching harmonics component (mainly 20 kHz) from  $v_{CM}$ .  $v_{CM}$  is the major contributor to the leakage current issue, which will be more severe when the switching frequency is higher. Fig. 3.19 and Fig. 3.20 show the time-domain simulation waveforms of the CM voltage  $v_{dc\_N}$  under the rectifier operation using an asymmetrical ac filter and a symmetrical ac filter, respectively. The dc-link voltage is 600 V, the power level is 10 kW, the switching frequency is 20 kHz, the ac grid voltage is the 240 V rms split-phase systems, and the dc-link capacitor is 360  $\mu$ F. The 60 Hz low-frequency profile in Fig. 3.19 is due to the  $v_{gb}$  term in (8), which is, however, mostly canceled by the 60 Hz component of  $0.5v_{DM}$ .

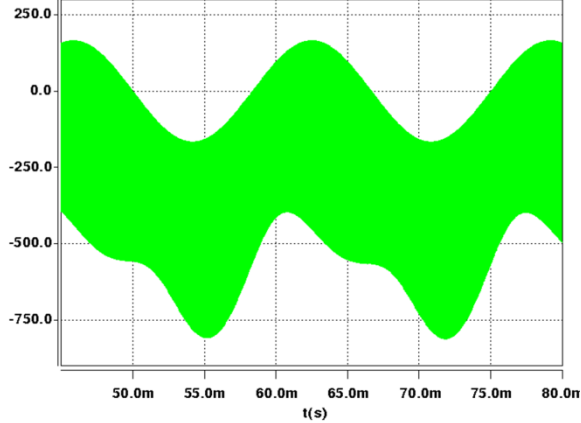


Fig. 3.19: CM voltage of negative dc-rail  $v_{dc\_N}$  in simulation using an asymmetrical L-C-L harmonic filter

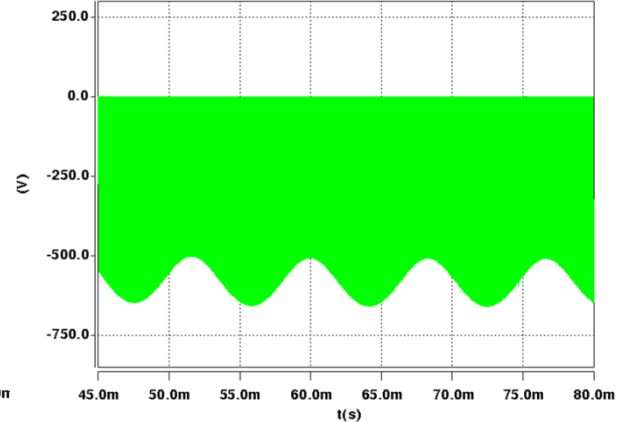


Fig. 3.20: CM voltage of negative dc-rail  $v_{dc\_N}$  in simulation using a symmetrical L-C-L harmonics filter

The analysis and simulation are based on the assumption that the impedance of  $C_s$  ( $Z_s$ ) is much bigger than the ac CM impedance, which is normally the case. However, if the ac-side is cascaded with an EMI filter, which gives a large ac CM impedance, e.g.:  $Z_{acCM}$ , the dc-side CM voltage will have a distortion due to the voltage divider formed by  $Z_s$  and  $Z_{acCM}$ , especially at the resonant frequency formed by  $(2Z_s, Z_{acCM})$ .



Although the symmetrical ac filter configuration helps reduce the dc-side CM voltage noise, the big switching-frequency CM noise still needs to be eliminated.

### 3.2.3. PROPOSED MODIFIED AC L-C-L PASSIVE FILTER SOLUTION

#### 3.2.3.1. Analysis of the Modified Ac Filter Solution

Since the full-bridge inverter is tied to the residential distribution system, the EMI filter normally should be cascaded with the L-C-L harmonic filter to comply with the regulation standard, such as [178], which offers the opportunity to reduce the dc-side leakage current. In this paper, a passive filter structure is proposed to utilize the ac passive L-C-L harmonic filter and one CM choke from the ac EMI filter to reduce the high-frequency dc-side leakage current.  $C_{DM\_P}$  and two split capacitors  $C_{DM\_S}$ , are used as the first-stage DM capacitor  $C_{DM}$ . The CM choke  $L_{CM}$ , normally one part of the EMI filter, is connected between the first-stage DM inductor (boost inductor),  $L_{ac1}$ , and the split capacitors  $C_{DM\_S}$ , as shown in Fig. 3.21. Then, the mid-point of the dc-link and the mid-point of the split capacitor  $C_{DM\_S}$  are connected electrically to each other. The modulation scheme for this full-bridge topology is the unipolar modulation. Similar ac filter structure can be found in bridge-less PFC circuit [190] with a different design target.

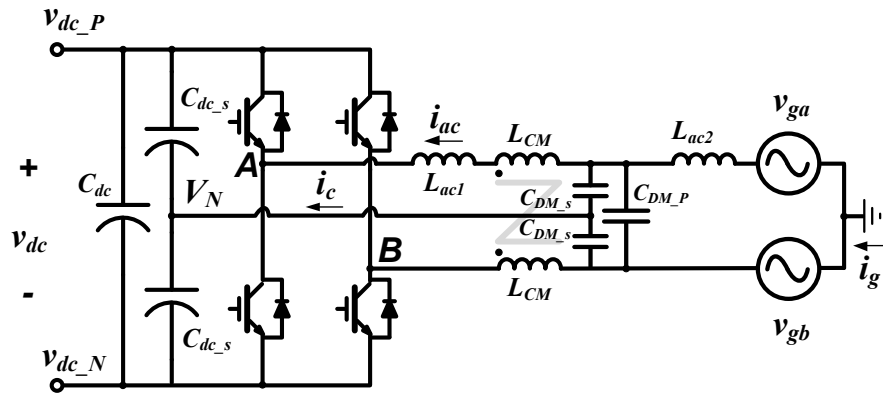


Fig. 3.21: Proposed full-bridge inverter

The proposed inverter structure doesn't introduce any extra components, but rather reconfigures the ac passive components. Thus, the inverter operation reliability is guaranteed compared to other solutions. It doesn't require control for extra switches, and no extra cost or loss is introduced in the proposed solution.

To better understand the dc leakage current reduction performance, the equivalent CM circuit is obtained, as shown in Fig. 3.22 to Fig. 3.24. It shows that the split DM capacitors  $C_{DM\_S}$  and the split dc-link capacitors  $C_{dc\_s}$  are included in the circuit. It is seen that a LC low-pass passive filter is introduced in the CM circuit. The split dc-link capacitor  $C_{dc\_s}$  is in series with the split ac DM capacitor  $C_{DM\_S}$ . Thus a large split dc-link capacitor is preferred for better attenuation.

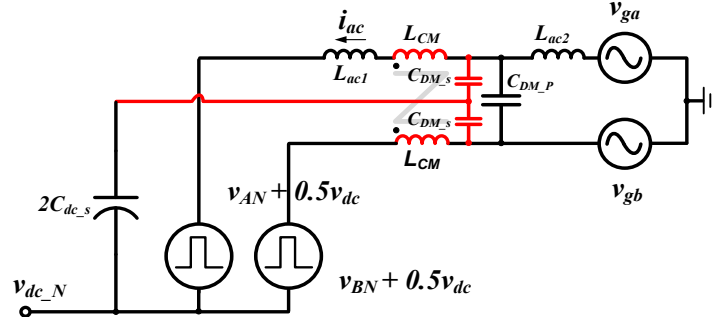


Fig. 3.22: Equivalent circuit of the modified full-bridge converter

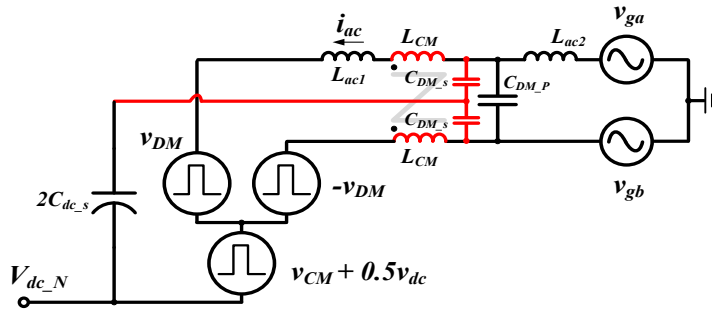


Fig. 3.23: Simplified equivalent circuit of the modified full-bridge converter

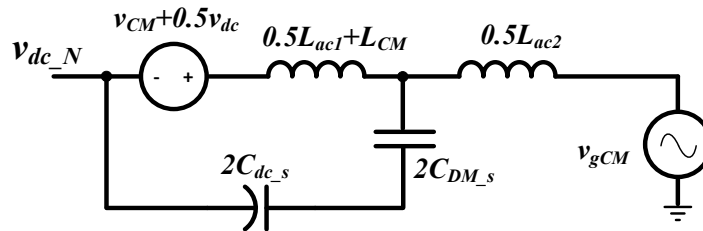


Fig. 3.24: CM equivalent circuit of the modified full-bridge converter

Based on Fig. 3.24, the CM voltage level of the mid-point of dc-link  $v_{dc\_N}$  can be determined. The CM negative dc-rail voltage is obtained in turn as shown in (14).  $\omega_r$  is the resonant frequency of the LC components:  $(0.5L_{ac1}+L_{CM}), (2C_{DM\_S}/2C_{dc\_s})$ . Normally, the  $\omega_r$  is much higher than 120 Hz, thus (14) can be simplified as shown in (15). Smaller  $\omega_r$  leads to a higher attenuation of  $v_{CM}$ .

$$\begin{aligned}
v_{dc\_N} &= -\frac{v_{CM}(\omega) + 0.5v_{dc}}{1 - \omega^2(0.5L_{ac1} + L_{CM}) \cdot (2C_{DM\_s} // 2C_{dc\_s})} + v_{gCM} \\
&= -\frac{v_{CM}(\omega) + 0.5v_{dc}}{1 - \frac{\omega^2}{\omega_r^2}} + v_{gCM}
\end{aligned} \tag{14}$$

$$v_{dc\_N} \approx -\frac{v_{CM}(\omega)}{1 - \frac{\omega^2}{\omega_r^2}} - 0.5V_{dc} - 0.5v_{ripple} + v_{gCM} \tag{15}$$

These equations show that an extra attenuation term has been applied on the  $v_{CM}$ , and the attenuation gain can be predicted by this CM circuit, as shown in (16).

$$Atten(\omega) = 20 \log_{10} \left( \left| 1 - \frac{\omega^2}{\omega_r^2} \right| \right) \tag{16}$$

Due to the CM propagation path formed by the proposed ac filter, additional CM noise current  $i_c$  is generated circulating in the loop as shown in Fig. 3.21. Based on Fig. 3.24, this CM current  $i_c$  can be calculated as shown in (17). It shows that  $i_c$  mainly consists of two frequency components: switching frequency components and low-frequency (120 Hz) component.

$$\begin{aligned}
i_c &= v_{CM}(\omega) \cdot k(\omega) + 0.5v_{ripple} \cdot k(2\pi \cdot 120) \\
k(\omega) &= \frac{\omega}{1 - \frac{\omega^2}{\omega_r^2}} (2C_{DM\_s} // 2C_{dc\_s})
\end{aligned} \tag{17}$$

Since the resonant frequency  $\omega_r$  is much smaller than the switching frequency, almost all the high-frequency noise is applied onto  $L_{CM}$  rather than  $(2C_{DM\_s} // 2C_{dc\_s})$ , the current in the return path  $i_c$  is very small, so the filter doesn't require a damping resistor.

### 3.2.3.2. Ac Filter Design

In order to investigate the performance, an ac passive filter design procedure is proposed. The full-bridge converter system specifications are shown in Table 3.2.

Table 3.2: Full-bridge converter system specifications

Symbol	Value
$P_{rate}$	10 kW
$f_s$	20 kHz
$\omega_o$	$2\pi 60$ rad/s
$V_{ac}$	240 V rms
$V_{dc}$	600 V
$C_{dc}$	360 $\mu$ F

The first-stage inductor  $L_{ac1}$  is chosen to limit the switching ripple (*pk-pk* value) of the ac current  $I_{ac}$ , e.g., within 25% of the rated peak current in (18), due in large part to the light-load efficiency consideration. The left side in (18) is determined by the mechanism of unipolar modulation [191].

$$\frac{\sqrt{2}V_{dc}}{16f_sL_{ac1}} = \Delta i_{pp\_max} < 25\% \frac{P_{rate}}{240} \quad (18)$$

The first-stage DM capacitor  $C_{DM}$  is limited by the reactive power level. For this 10 kW converter, 2.5% reactive power is chosen in (19). The value of split capacitors  $C_{DM\_S}$  and  $C_{DM\_P}$  in turn is determined as shown in (20).

$$C_{DM} < 2.5\% \frac{P_{rate}}{2\pi f_o V_{ac}^2} \quad (19)$$

$$0.5C_{DM\_S} + C_{DM\_P} = C_{DM} \quad (20)$$

The second-stage DM inductor  $L_{ac2}$  is designed to meet the current harmonics injection level [123], as shown in (21).

$$\frac{-v_{DM}(\omega)}{\sqrt{2}\omega(-\omega^2L_{ac1}L_{ac2}C_{DM} + L_{ac} + L_{ac2})} = I_G(\omega) < I_R \quad (21)$$

The selection of  $C_{DM\_S}$  and  $L_{CM}$  can be chosen by tuning the value of  $\omega_r$  based on the attenuation requirement in (13). The value varies with the switching frequency, power level, stray capacitance, and the standards. Typically,  $\omega_r$  can be chosen to be smaller than one tenth of the switching frequency to limit the  $i_c$  and avoid the damping resistor. In order to achieve a better impedance mismatch, the  $C_{DM\_S}$  is around several  $\mu$ F.

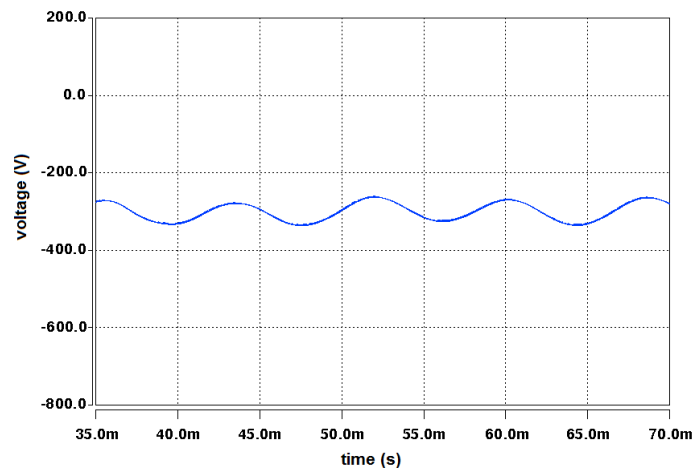
In this 10 kW power rating converter, the resonant frequency  $\omega_r$  is chosen as 800 Hz, and the  $C_{DM\_S}$  is chosen 5.6  $\mu$ F. Then the minimum value of  $L_{CM}$  has to be 3.5 mH.

A set of ac passive filters whose design is based on the above discussions are shown in Table 3.3. The 50  $\mu\text{F}$ , 450 V rated film capacitor is chosen as the split dc-link capacitors  $C_{dc\_s}$ .

Table 3.3: Designed ac filter values

Symbol	Value
$L_{ac1}$	360 $\mu\text{H}$
$C_{DM\_S}$	5.6 $\mu\text{F}$
$C_{DM\_P}$	6.6 $\mu\text{F}$
$L_{ac2}$	25 $\mu\text{F}$
$L_{CM}$	3.5 mF

Fig. 3.25 shows the time-domain simulation waveforms of  $v_{dc\_N}$  under 7 kW after applying the proposed ac passive filter structure. It shows that the dc-side switching-frequency CM voltage noise is significantly reduced, leaving only the low-frequency component. Therefore, the dc-side high-frequency leakage current is almost eliminated.

Fig. 3.25: CM voltage of negative dc-rail  $v_{dc\_N}$  in simulation by using the proposed full-bridge topology

The simulation is conducted by using the full-bridge inverter as shown in Fig. 3.11. A typical LCL filter and the modified ac filter are used and the system parameters are shown in Table 3.2 and Table 3.3. 5 nF stray capacitors without any damping resistors are assumed on both positive and negative dc-rails. As shown in Fig. 3.26, the total leakage current is obtained by measuring the current flowing into the ac earth wire  $i_g$ , as labeled in Fig. 3.21.

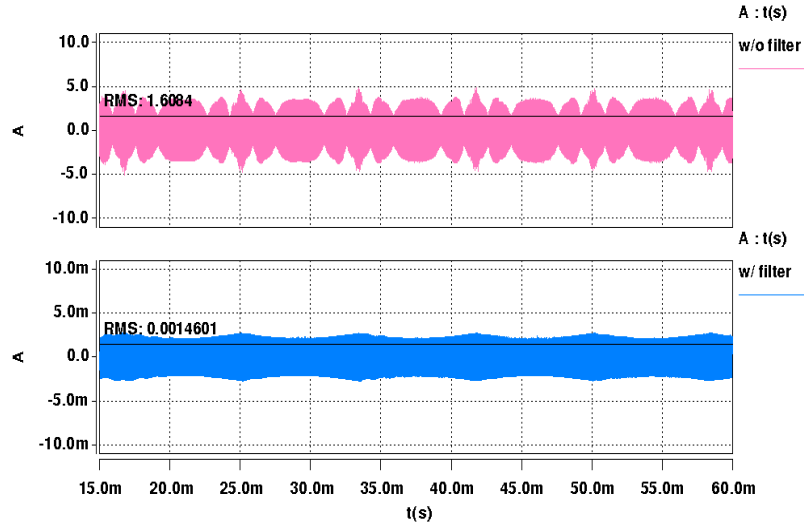


Fig. 3.26: Leakage current level by using the typical LCL filter (upper waveform, [5A/DIV]) and the modified filter (lower waveform, [5mA/DIV])

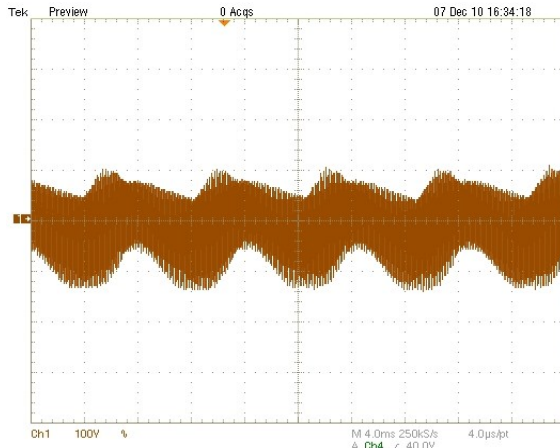
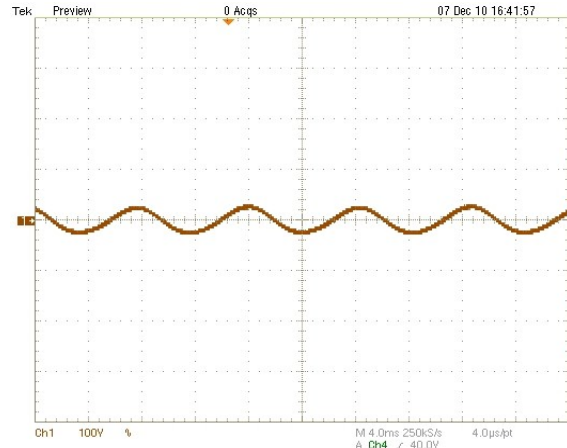
It is seen that the leakage current has been attenuated from 1.6 A to 1.46 mA, achieving about attenuation of 60 dB. And this attenuation level matches with the estimated value from (13) at the switching frequency.

### 3.2.3.3. Experimental Verification for Single-phase Case

A 10 kW single-phase full-bridge converter is built to demonstrate the performance of the proposed ac filter structure. The 240 V rms split-phase single-phase grid is connected. As shown in Fig. 3.27, the CM choke is built with nanocrystalline magnetic materials. The experiments are conducted under the rectifier operation using the specifications in Table II. The value of the split DM capacitors is chosen from Table II. The time-domain experimental waveforms of the negative dc-link voltage with respect to the ground  $v_{dc\_N}$  with and without the proposed ac filter structure are shown in Fig. 3.28 and Fig. 3.29, respectively. They show a significant reduction of the switching frequency CM noise on the dc-link.



Fig. 3.27: AC CM choke and AC DM capacitors

Fig. 3.28:  $v_{dc\_N}$  [100V/DIV] without the proposed ac filterFig. 3.29:  $v_{dc\_N}$  [100V/DIV] with the proposed ac filter

In order to investigate the additional power loss due to the proposed ac filter structure, it is necessary to measure the CM current  $i_c$  flowing back into the mid-point of the dc-link, as labeled in Fig. 3.21. The time-domain waveform of  $i_c$  is shown in Fig. 30 under 7 kW conditions. The ac grid voltage waveform is also shown in Fig. 3.30. As discussed in (17),  $i_c$  consists of the switching-frequency component and the 120 Hz low-frequency component. The rms value of  $i_c$  in Fig. 3.30 is less than 0.7 A. Thus, the additional power loss due to this ac filter structure is almost negligible.

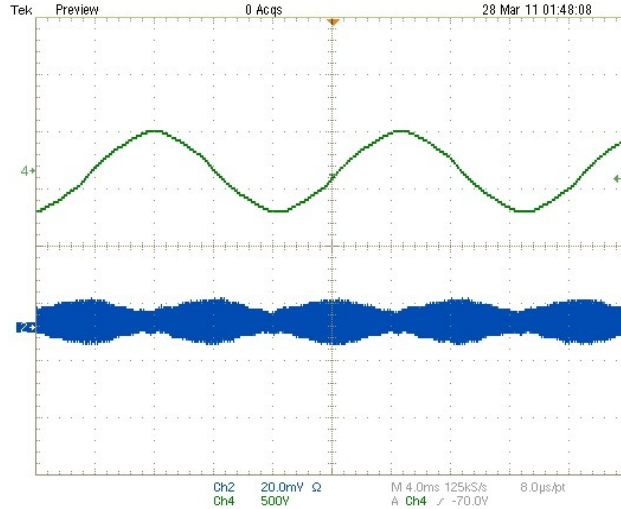


Fig. 3.30:  $I_c$  that flows through the split dc-link capacitors.  $I_c$  (blue) [2A/DIV],  $V_{ac}$  (green) [500V/DIV]

Fig. 3.31 shows the measured spectrum of  $v_{dc\_N}$  with and without the proposed ac filter structure. A reduction of about 50 dBV is achieved at the 20 kHz switching component, which agrees with the predicted value obtained by (12).

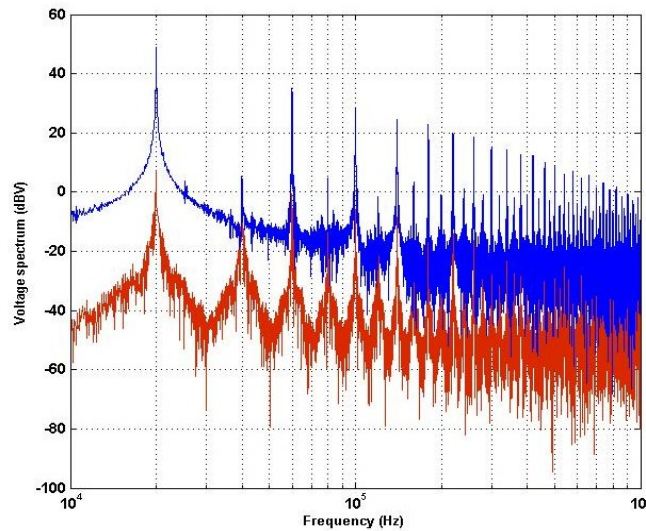


Fig. 3.31: Spectrum of  $v_{dc\_N}$  with (red) and without (blue) the proposed ac filter structure.

The leakage current comparison between the normal LCL filter and the proposed ac filter is shown below in Table 3.4. The proposed filter significantly eliminates the leakage current by more than 98%.

Filter structure	Leakage current (mA)
LCL ac filter	5.6
Proposed ac filter	0.1



### 3.2.4. HIGH-FREQUENCY LEAKAGE CURRENT REDUCTION IN ASYMMETRICAL SINGLE-PHASE SYSTEMS

The previous analysis is based on the North American split-phase single-phase system. In Europe or elsewhere, the residential LV distribution feeder is from the three-phase, four-wire distribution transformers, and the full-bridge inverter is normally interfaced between one of the three-phase lines and the neutral wire. The neutral wire is connected to the earth ground at the terminal of the distribution transformer. The equivalent circuit is shown in Fig. 3.32. For this type of ac system, the analysis and the CM equivalent circuit in Fig. 3.18 and Fig. 3.24 are still valid. The major difference is that the CM voltage  $v_{gCM}$  will be half of the line voltage, as shown in (22), while  $v_{gCM}$  is almost equal to zero in the split-phase system. The negative dc-rail CM voltage  $v_{dc\_N}$  is shown in (23).

$$v_{gCM} = \frac{1}{2}(0 + v_g) = 0.5v_g \quad (22)$$

$$v_{dc\_N} = -\frac{v_{CM}(\omega)}{1 - \frac{\omega^2}{\omega_r^2}} - 0.5V_{dc} - 0.5v_{ripple} + 0.5v_g \quad (23)$$

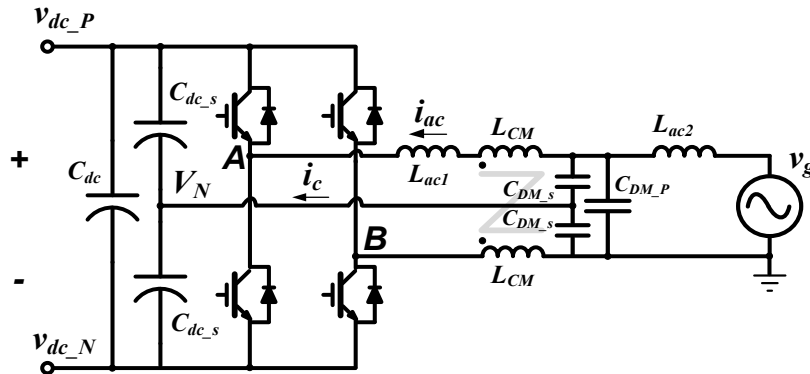


Fig. 3.32: Full-bridge inverter connected to single-phase system with asymmetrical grounding scheme

Thus, the proposed ac filter structure can be used to attenuate the high-frequency leakage current as well, leaving a relatively large 60 Hz line CM voltage ripple on the dc-side according to (23). As shown in Fig. 3.33, the simulation results of  $v_{dc\_N}$  with respect to ground show half of the line-frequency voltage ripple, but the high-frequency CM voltage noise is still eliminated.

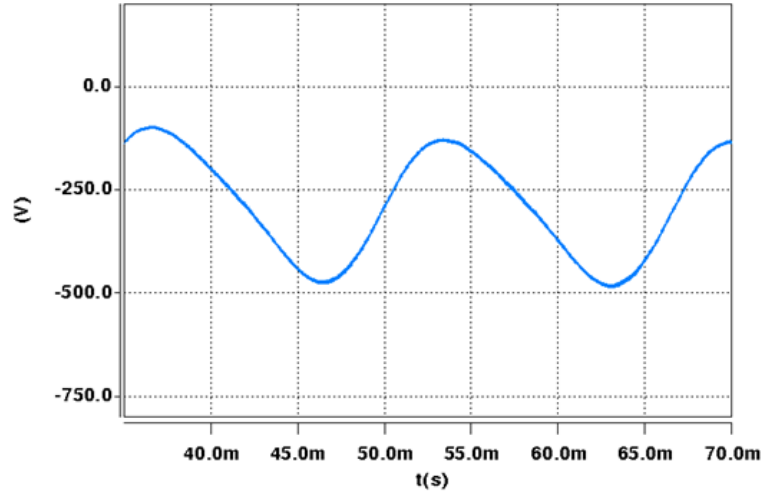


Fig. 3.33: CM voltage of negative dc-rail  $v_{dc\_N}$  in simulation using the proposed full-bridge topology under asymmetrical ac ground scheme

Thus, the asymmetrical single-phase system generate a large ling-frequency CM voltage ripple on the dc-side, resulting in lots of issues, such as insulation, safety, and low-frequency leakage current issue.

There are also different configurations of the proposed ac filter structure. As shown below in Fig. 3.34, the system gives the same high-frequency leakage current reduction without using the split dc-link capacitors. The trade-off is the ac capacitor will bear half of the dc-link voltage plus half of the ac voltage, which increases the voltage rating.

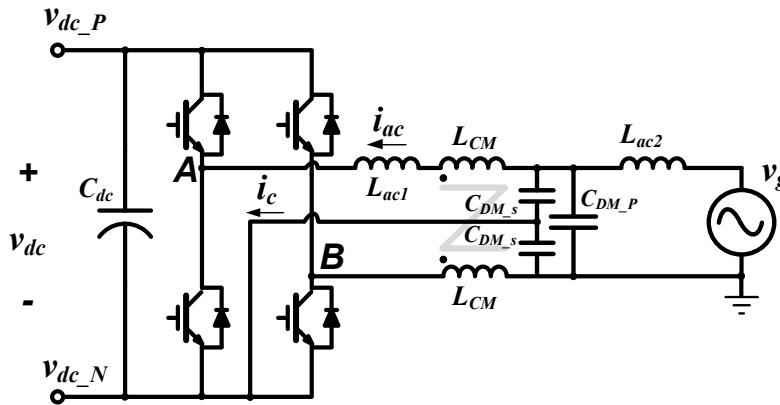


Fig. 3.34: Proposed ac filter for dc leakage current reduction without split dc-link capacitor.

An experimental evaluation is also conducted for asymmetrical single-phase system. The grounding connection point of the transformer is moved from the mid-point to one-side of the output wire. As such, the equivalent grid would be a 240V rms asymmetrical grid. As shown in Fig. 3.35, the change of grounding point doesn't affect the ac current

regulation performance, but change the dc-side CM voltage as analyzed before. However, the high-frequency CM noises are still eliminated.

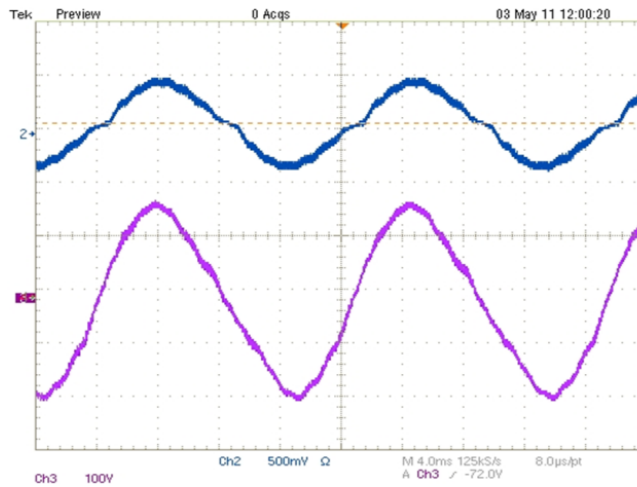


Fig. 3.35: CM voltage of negative dc-rail  $v_{dc\_N}$  (purple) [100V/DIV] and ac current  $I_{ac}$  (blue) [50A/DIV] using the proposed full-bridge topology under asymmetrical ac ground scheme

### 3.2.5. HIGH-FREQUENCY LEAKAGE CURRENT REDUCTION IN THREE-PHASE SYSTEMS

As discussed before, three-phase interface is also popular in the low-voltage distribution system. For the first-stage of three-phase ECC converter, two-level voltage-source-converter (VSC), as shown in Fig. 3.36, is used as an example for discussion. A three-phase L-C-L harmonic filter ( $L_{ac1}$ - $C_{DM}$ - $L_{ac2}$ ) is used for the grid interface [192]. The same modeling process gives the CM equivalent circuit as shown in Fig. 3.37.

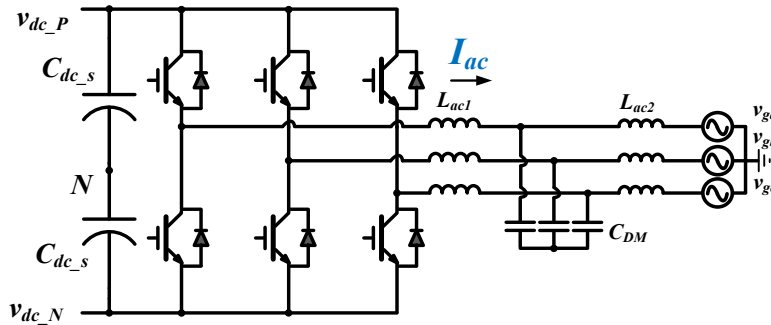


Fig. 3.36: Two-level three-phase voltage source converter

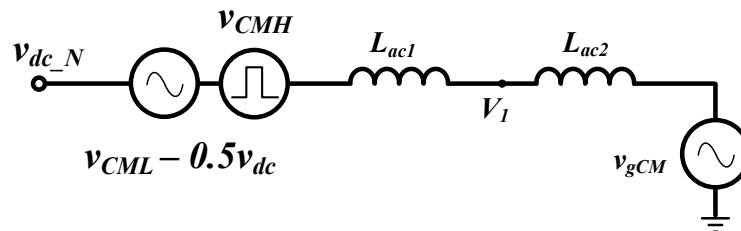


Fig. 3.37: CM equivalent circuit of the three-phase ECC

Due to the space vector modulation (SVM) methods, the CM voltage sources include two major frequency components, the high-frequency switching noise, and the low-frequency noise (mostly the third-order harmonics). As such, the negative dc-rail CM voltage would be in (24).  $v_{gCM}$  is the grid CM voltage defined in (25).

$$V_{dc\_N} = V_{CML} + V_{CMH} - 0.5v_{dc} + v_{gCM} \tag{24}$$

$$v_{gCM} = \frac{1}{3}(v_{ga} + v_{gb} + v_{gc}) \tag{25}$$

Different modulation methods and different modulation indices give different characteristics of  $V_{CML}$  and  $V_{CMH}$ . Two popular SVM methods and their CM voltages in two switching cycles are shown in Fig. 4.38 and Fig. 4.39.

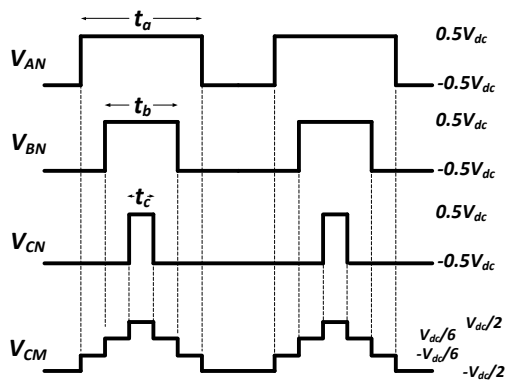


Fig. 3.38: Continuous SVM (SVPWM)

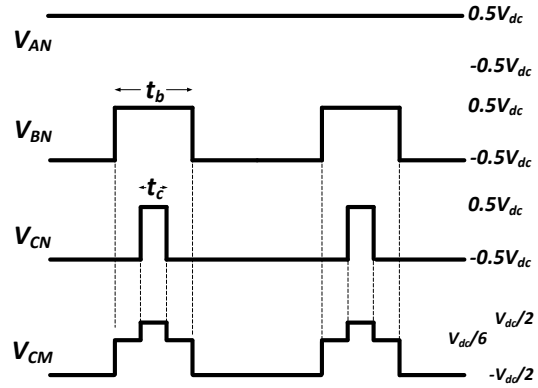


Fig. 3.39: Discontinuous SVM (DPWM)

The CM voltage jumps at the switching frequency, leading to a large high-frequency leakage current. A simulation result of the negative dc-rail CM voltage  $v_{dc\_N}$  is shown in Fig. 3.40 with 20 kHz switching frequency, 600 V dc-link voltages, and DPWM method.

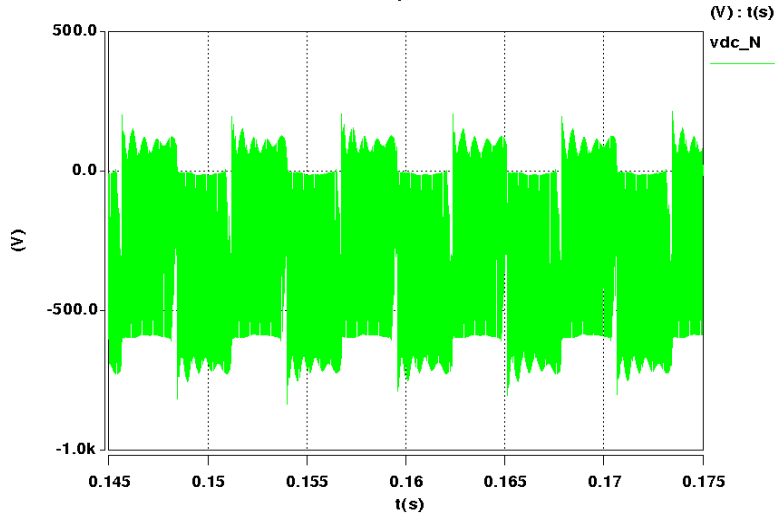


Fig. 3.40: Negative dc-rail CM voltage  $v_{dc\_N}$  of three-phase ECC converter.

Lots of publications focus on the PWM modulation solution, e.g., near-state PWM, to eliminate the CM noises in transformerless inverter [85-90]. However, the existing solutions pose more additional switching loss, large DM noises, and more magnetic core loss. Using the modified ac passive filter, all the aforementioned discussions and results in this paper can be also applied to the three-phase ECC converter, as shown below in Fig. 3.41. This filter is similar as the so-called “ $dv/dt$ ” filter [99] normally seen in three-phase motor drive applications. The major difference is that here a CM inductor is required to put inside the loop, reducing the damping resistor value and loss. Thus, the practical implementation is much easier than  $dv/dt$  filter.

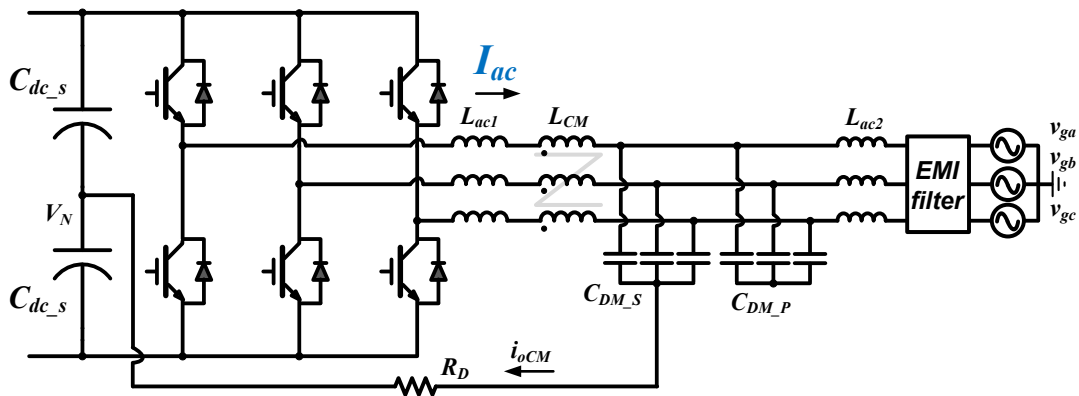


Fig. 3.41: Three-phase ECC Converter with the proposed filter structure.

The same modeling process can give the CM equivalent circuit as shown in Fig. 3.42.

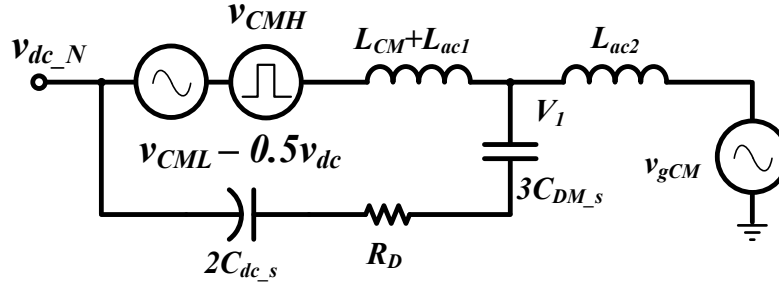


Fig. 3.42: CM equivalent circuit with the modified ac filter.

The filter design would be different than the single-phase case, simply due to the low-frequency voltage-source  $V_{CML}$ . In the single-phase case discussed before, a large  $C_{DM_s}$  is chosen for a lower resonant frequency  $\omega_r$  and a better attenuation performance. However, in three-phase case, large value of  $C_{DM_s}$  results in more low-frequency voltage-second from  $V_{CML}$  applied onto  $L_{CM}$ , leading to a bigger volume to avoid saturation. Therefore the selection of  $C_{DM_s}$  should be small to limit the volt-second on  $L_{CM}$ . For this case, the damping resistor has to be bigger. The detailed design relies on the application requirement, e.g.: CM noises attenuation requirement, PWM modulation method, and operation condition. A simulation result is shown as a design case. The parameters are shown in Table 3.5, and the negative dc-rail CM voltage is shown in Fig. 3.43.

Table 3.5: Filter value for three-phase first-stage ECC converter

$f_s$	$V_{dc}$	$P_{rate}$	$C_{DM_s}$	$R_D$	$L_{CM}$
20 kHz	600 V	5 kW	0.5 $\mu$ F	80 $\Omega$	5 mH

The simulation results show that most of the high-frequency CM noises have been eliminated, though not totally, leaving only the low-frequency CM voltage ripple contributed by the  $V_{CML}$ . This performance is applicable in many applications, such as PV system.

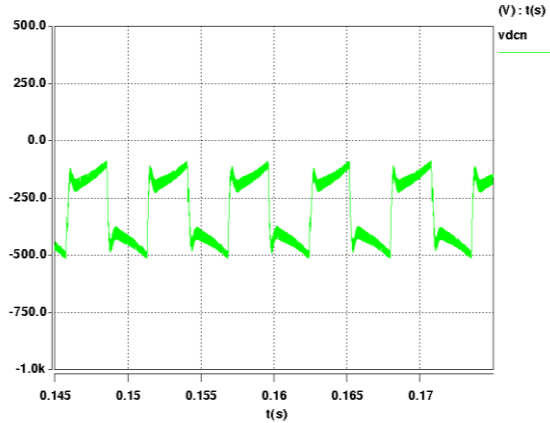


Fig. 3.43: Negative dc-rail CM voltage  $v_{dc\_N}$  [250V/DIV] with the modified ac filter structure using DPWM modulation.

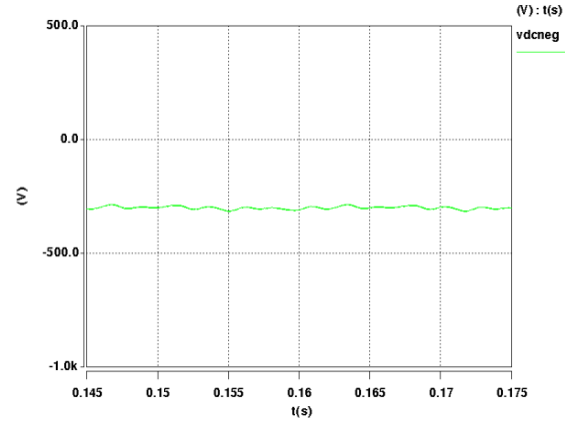


Fig. 3.44: Negative dc-rail CM voltage  $v_{dc\_N}$  [250V/DIV] with the modified ac filter structure using carrier-based without CM injection modulation.

However in the dc distribution system, the low frequency voltage ripple needs to be eliminated. Thus, it is preferable to get rid of the  $V_{CML}$ , which also helps reduce the saturation requirement of CM choke. The carrier-based PWM without CM injection can be used instead of SVM. As such, the CM equivalent circuit would be as Fig. 3.42 but no  $V_{CML}$ , similar as the single-phase case. The above discussion also explains why the unipolar PWM modulation is chosen rather than the discontinuous PWM (hybrid) modulation [193, 194] in single-phase case simply because the hybrid modulation methods generate a low-frequency CM voltage shown on the dc-side.

As shown in Fig. 3.44, a simulation is conducted by using the carrier-based PWM without CM injection modulation method, and the parameters are shown in Table 3.6.

Table 3.6: Filter value for three-phase first-stage ECC converter

$f_s$	$V_{dc}$	$P_{rate}$	$C_{DM\_s}$	$R_D$	$L_{CM}$
20 kHz	600 V	5 kW	10 $\mu$ F	1 $\Omega$	5 mH

It is seen that the negative dc-rail CM voltage is almost a pure dc value around -300 V, all the high-frequency CM voltage noises have been totally eliminated, which reduce the whole dc system leakage current level.

The advantage of using the carrier-based PWM without CM injection is the almost zero low-frequency CM voltage ripple. However, the trade-off would be more switching loss. Reference [195] systemically compared the converter efficiency using different modulation methods. The DPWM accomplish 0.5 to 1% more efficiency compared with

the carrier-based PWM without CM injection. Moreover, the carrier-based PWM without CM injection requires 15.5 % more dc-link voltage compared with the space vector modulation method.

For dc distribution system application, it is still desirable to use the carrier-based PWM without CM injection to benefit the overall system operation and reliability. The loss issue can be resolved by reducing the switching frequency.

The detailed filter design and consideration is omitted here since most considerations have been discussed in the single-phase case.

### **3.2.6. CONCLUSION**

In this section, a novel full-bridge converter topology is proposed using the proposed ac passive filter structure to reduce the dc-side leakage current by more than 90%. Unlike existing solutions, the proposed method doesn't introduce any extra switches, thus reducing the cost, improving the reliability and eliminating extra power loss. The proposed filter structure is suitable for different ac grounding schemes, as well as bi-directional power flow conditions. The overall ac passive filter volume is also reduced due to the attenuation of ac conducted CM noise.

The proposed solution can be applied onto both split-phase single-phase system, asymmetrical single-phase system, and three-phase system.

## **3.3. LOW-FREQUENCY DC-SIDE CM VOLTAGE RIPPLE REDUCTION USING ACTIVE CONTROL**

### **3.3.1. ACTIVE CONTROL SYSTEM ANALYSIS IN SPLIT-PHASE SINGLE-PHASE SYSTEMS**

#### **3.3.1.1. Analysis of the Active Control Method**

The modified ac passive filter solution can dramatically reduce the high-frequency CM noise, leaving the low-frequency part. From the dc-side power quality point of view, the low-frequency CM voltage ripple still needs to be maintained in a small value. For example, the CM voltage ripple below 1 kHz of dc system in aircraft power system should be less than 5% [181]. From the leakage current regulation point of view, even low-frequency CM voltage results in a leakage current due to lots of CM capacitors in every dc-dc converters on dc-side.



The low-frequency CM voltage ripple in split-phase single-phase system, as shown in Fig. 3.25, is mainly from  $v_{gCM}$  and  $v_{ripple}$ , which can be attenuated by imposing dc CM filters. However, due to the limited value of dc CM capacitors, the total size of the CM choke will be extremely big, therefore reducing the total power density of the converter system.

Another approach to addressing the low-frequency CM voltage ripple, proposed in this paper, is to generate the corresponding low-frequency CM voltage by full-bridge. As depicted in Fig. 3.12, it shows the terminal switching schemes of each phase-leg and the CM voltage  $v_{CM}$ . Since  $t_a$  equals  $t_b$  for unipolar modulation, the average value of the CM voltage equals zero all the time. The low-frequency  $v_{CM}$ , however, can be modulated by the CM duty-cycle  $d_{CM}$  to slightly change the ratio between  $t_a$  and  $t_b$ . As such, the modified unipolar modulation scheme and the associated feedback controller are proposed in Fig. 3.45.  $R_L$  is a small resistor with only several  $\Omega$ .

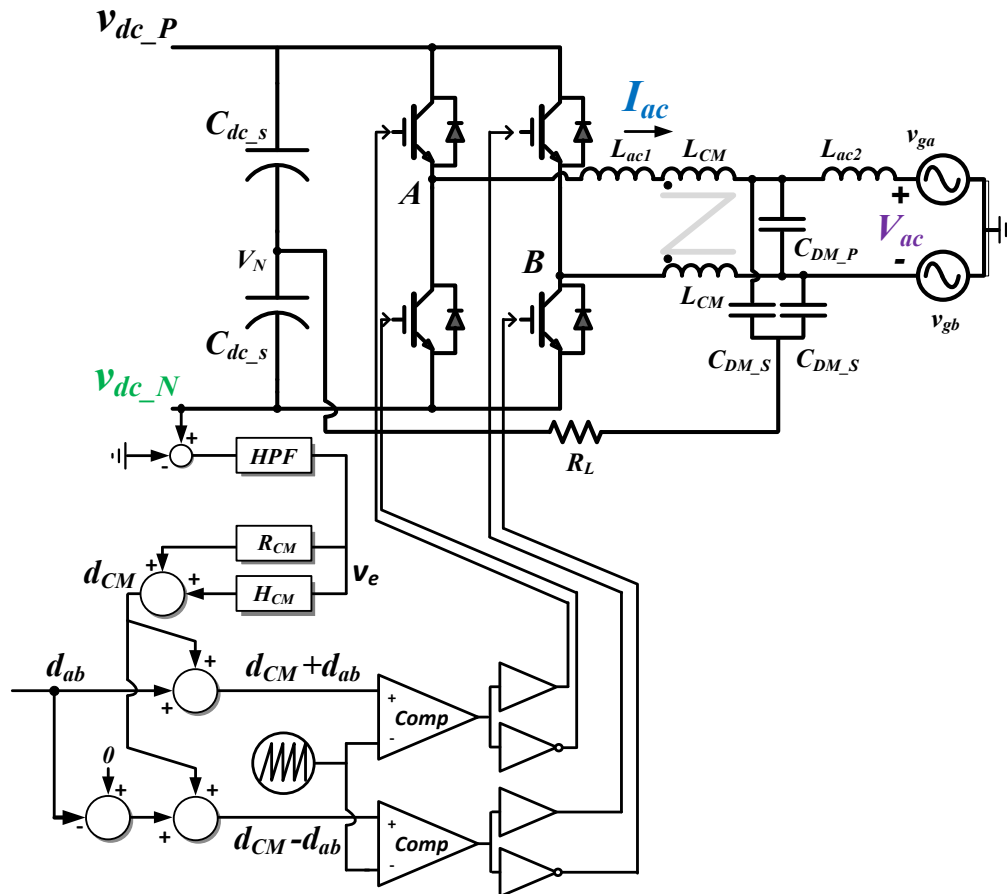


Fig. 3.45: Proposed low-frequency dc CM voltage modulation scheme and controller

The negative dc-rail CM voltage  $v_{dc\_N}$  is measured and filtered by the high-pass-filer HPF to eliminate the dc component leaving only the low-frequency ripple information. A CM duty cycle  $d_{CM}$  is generated by the compensator  $H_{CM}$  plus the resonant controller  $R_{CM}$ , and is injected into the unipolar modulator. The form of  $H_{CM}$  and  $R_{CM}$  are shown in (26) and (27).

$$H_{CM}(s) = K \frac{(s + \omega_{z1})(s + \omega_{z2})}{s(s + \omega_{p1})(s + \omega_{p1})}, \quad (26)$$

$$R_{CM}(s) = 2k \frac{s}{s^2 + (2\omega_o)^2}, \quad \omega_o = 2\pi 60 \text{ rad/s} \quad (27)$$

In (26), two zeros are placed around the resonant frequency ( $L_{CM}, 2C_{DM\_s}$ ) for desired phase-margin; two poles are placed after the crossover frequency to attenuate the high-frequency noises.  $R_{CM}$  is to achieve the high loop-gain at 120 Hz for better control performance. The corresponding low-frequency CM voltage in the full-bridge output terminals is shown in (28).

$$\begin{aligned} v_{CM} &= \frac{1}{2} [V_{AN} + V_{BN}] \\ &= \frac{1}{2} \left[ \frac{1}{2} v_{dc} (d_{CM} + d_{ab}) + \frac{1}{2} v_{dc} (d_{CM} - d_{ab}) \right] \\ &= \frac{v_{dc}}{2} d_{CM} \end{aligned} \quad (28)$$

The state feedback control block diagram is shown in Fig. 3.46. The control objective is to force the measured  $v_{dc\_N}$  as a constant dc value, namely eliminating the low-frequency ripple. In order to design the controller, the control-to-output small-signal model  $G_{vd}(s)$  is obtained in (29) by applying the quasi-static modeling process.  $H_{delay}$  represents the one switching-cycle digital computation delay.

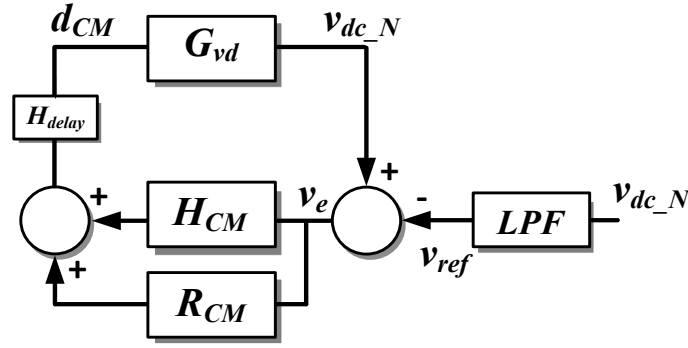


Fig. 3.46: State feedback control block diagram

$$\begin{aligned}
 G_{vd}(s) &= \frac{\tilde{v}_{dc\_N}}{\tilde{d}_{CM}} \\
 &= -\frac{v_{dc}}{2} \frac{sR_L \cdot 2C_{DM\_s} + 1}{s^2 L_{CM} \cdot 2C_{DM\_s} + sR_L \cdot 2C_{DM\_s} + 1}
 \end{aligned} \tag{29}$$

The control voltage reference  $v_{ref}$  is the dc component of the  $v_{dc\_N}$ , generated by a low-pass-filter (LPF). Similarly, as shown in Fig. 3.45, a HPF is used instead to generate the error signal  $v_e$ .

The transient simulation result, as seen in Fig. 3.47, shows that the low-frequency dc CM voltage ripple is being regulated and reduced when the CM voltage controller starts generating the CM duty-cycle  $d_{CM}$ . Fig. 3.48 and Fig. 3.49 also show the steady-state negative dc-rail CM voltage level  $v_{dc\_N}$  (under around 10 kW power condition) with and without the proposed CM voltage controller. The voltage ripple is reduced by 80%, likewise the reduction of corresponding dc low-frequency leakage current.

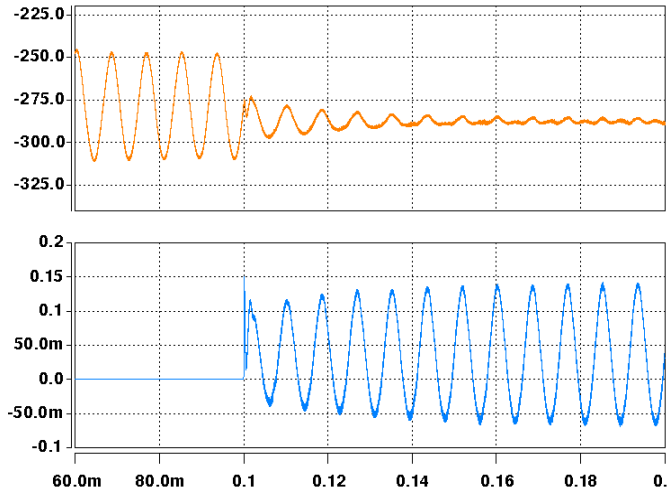


Fig. 3.47: Transient period simulation waveform of  $v_{dc\_N}$  when the CM controller is initiated,  $v_{dc\_N}$  (orange) [25V/DIV],  $d_{CM}$  (blue) [50m/DIV].

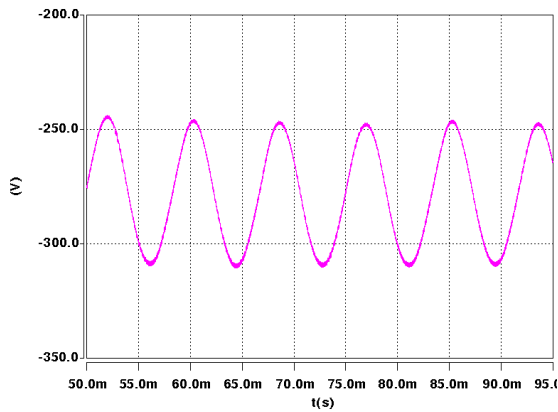


Fig. 3.48:  $v_{dc\_N}$  (magenta) [25V/DIV] without the proposed controller.

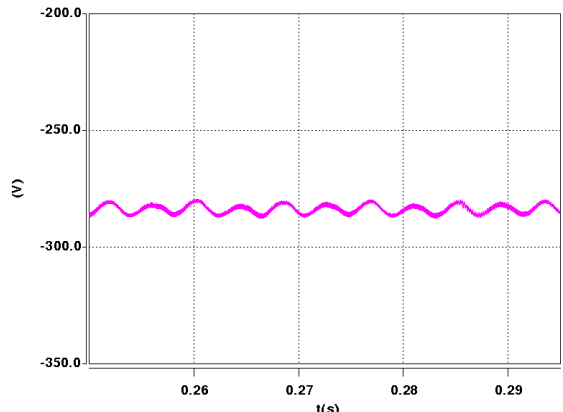


Fig. 3.49:  $v_{dc\_N}$  (magenta) [25V/DIV] with the proposed controller

### 3.3.1.2. CM Inductor Design

The basic modeling of single-phase CM choke and its design can be found in [196]. The design of  $L_{CM}$  should take the saturation issue into account in the proposed ac filter structure. Besides the leakage inductance of the CM choke [197], the major contributor to the saturation of the  $L_{CM}$  is the switching-frequency volt-second excitation VS generated by the PWM switching function [198], as labeled in Fig. 3.50.

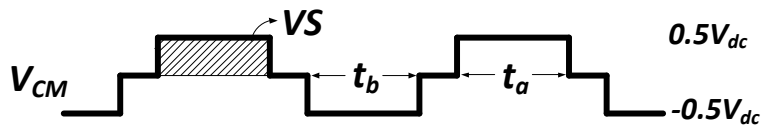


Fig. 3.50: Volt-second generated by CM terminal voltage

The CM volt-second applied on the CM choke  $L_{CM}$  is shown in (30).

$$VS = \int v_{CMC} dt \quad (30)$$

$V_{CMC}$  is the volt-second excitation applied on the CM choke  $L_{CM}$ . Based on Fig. 3.16,  $V_{CMC}$  is derived as shown in (31).

$$\begin{aligned} v_{CMC} &= v_{CM}(\omega) \frac{-\omega^2(0.5L_{DM} + L_{CM}) \cdot (2C_{DM\_s} // 2C_{dc\_s})}{1 - \omega^2(0.5L_{DM} + L_{CM}) \cdot (2C_{DM\_s} // 2C_{dc\_s})} \\ &= v_{CM} \frac{\omega^2}{\omega^2 - \omega_r^2} \end{aligned} \quad (31)$$

There are two frequency volt-second components: switching frequency volt-second and low-frequency volt-second. The switching-frequency volt-second is due to the PWM switching.

Since  $\omega_r$  is much lower than the switching frequency, most of the high-frequency CM voltage will be applied onto the CM choke  $L_{CM}$ . Thus, (31) can be simplified, as shown in (32).

$$v_{CMC} \approx v_{CM} \quad (32)$$

There are two possible switching-frequency maximum volt-second points. One occurs when the ac current  $I_{ac}$  is zero-crossing. At this instant, the CM duty-cycle reaches the peak value (close to 0.5). Another one occurs when the dc-link voltage reaches the peak value  $V_{dc} + |v_{ripple}|$ .

These two possible switching-frequency maximum points are shown below in (33) and (34), respectively.

$$VS_{H1} = V_{CMC} t_{CM} = \frac{1}{2} V_{dc} t_{CM\_max} \quad (33)$$

$$VS_{H2} = V_{CMC} t_{CM} = \frac{1}{2} V_{dc\_max} t_{CM} \quad (34)$$

If the full-bridge operates as the inverter, the dc-link voltage and its ripple level are determined by the dc-source, such as PV panels. The maximum volt-second point can be determined by comparing these two possible maximum points.

$$VS_{\max\_H} = \max\{VS_{H1}, VS_{H2}\} \quad (35)$$

If the full-bridge operates as the rectifier, these two possible maximum points can be represented by Fig. 3.51 and Fig. 3.52. It can be derived that when CM duty cycle reaches 0.5, the dc-link voltage  $v_{dc}$  stays at the average value.

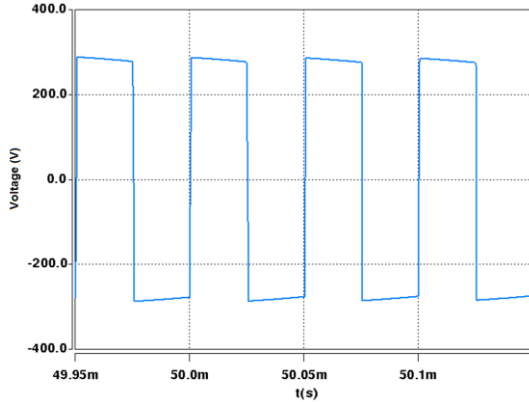


Fig. 3.51:  $V_{CM}$  when ac current is zero-crossing

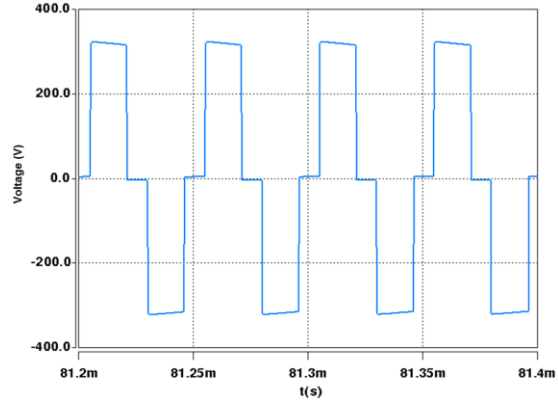


Fig. 3.52:  $V_{CM}$  when dc-link voltage reaches the peak value

The volt-second is shown in (36). When the dc-link voltage reaches the peak value  $V_{dc} + |v_{ripple}|$ , the volt-second is derived in (37), where  $M$  is the full-bridge modulation index.

$$VS_{H1} = \frac{1}{2} V_{dc} \frac{1}{2} T_s \quad (36)$$

$$VS_{H2} = \frac{1}{2} (V_{dc} + |v_{ripple}|) \frac{1}{2} \left(1 - \frac{M}{\sqrt{2}}\right) T_s \quad (37)$$

The maximum switching-frequency volt-second can be calculated by solving (36) and (37) and choosing whichever value is the largest. In a practical case, under unity power factor conditions, the volt-second in (36) is the maximum point.

$$VS_{\max\_H} = VS_{H1} \quad (38)$$

The low-frequency (mainly 120 Hz) volt-second is due to the CM voltage generated by  $d_{CM}$ , and the corresponding volt-second is shown in (39).

$$VS_L = \int \frac{1}{2} v_{dc} d_{CM} \quad (39)$$

$VS_L$  in (39) reaches the peak value  $VS_{L\max}$  every half cycle (120 Hz). If  $d_{CM}$  is expressed in (40), the generated maximum low-frequency volt-second  $VS_{L\max}$  is derived in (41).

$$d_{CM} = M_{CM} \sin(2\omega_o t), \omega_o = 2\pi 60 \text{ rad/s} \quad (40)$$

$$VS_{L_{\max}} = \frac{1}{2} V_{dc} \frac{M_{CM}}{\omega_o} \quad (41)$$

As such, the maximum low-frequency volt-second applied on the CM choke  $L_{CM}$  is derived as:

$$VS_{\max\_L} \approx \frac{(2\omega_o)^2}{(2\omega_o)^2 - \omega_r^2} VS_{L_{\max}} \quad (42)$$

The total maximum volt-second applied on  $L_{CM}$  is shown in (43), which determines the design of  $L_{CM}$ . In order to avoid the saturation of  $L_{CM}$ , the number of turns  $N_c$  and the core cross-sections  $A_c$  have to fulfill the requirement in (44).

$$VS_{total\_max} = VS_{\max\_L} + VS_{\max\_H} \quad (43)$$

$$N_c \cdot A_c > \frac{VS_{total\_max}}{B_{\max}} \quad (44)$$

As seen in (44), it determines the value of  $N_c$  and  $A_c$ , thus determining the  $L_{CM}$  value. A magnetics material with proper permeability has to be chosen for the optimal design.

In this paper, in order to freely tune the value of  $L_{CM}$ , an air-gap is designed and implemented. The design procedure of this CM choke  $L_{CM}$  and  $C_{DM\_s}$  capacitor are proposed simply as follows. Firstly, design the core size and number of turns based on (44). Then, design the  $L_{CM}$  value by designing the air-gap value. Finally, based on (16), design the  $C_{DM\_s}$  to obtain the resonant frequency  $\omega_r$  for a desired CM noise attenuation.

A nanocrystalline toroid core with air-gap is designed as shown in Fig. 3.53. The core is over-designed leaving 40% saturation margin. The air-gap is 0.1 mm and the number of turns is 25.

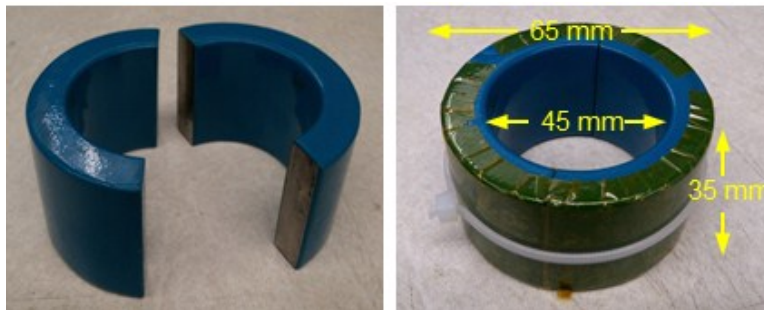


Fig. 3.53: Designed CM choke with air gap

As shown in Fig. 3.54, the measured CM inductance in the interested frequency range is about 3.5 mH. The resonant frequency  $\omega_c$  is chosen around 0.9 kHz, and the corresponding  $C_{DM\_s}$  is 5.6  $\mu\text{F}$ .  $C_{DM\_P}$  is 6.6  $\mu\text{F}$  ( $C_{DM} = 10 \mu\text{F}$ ).

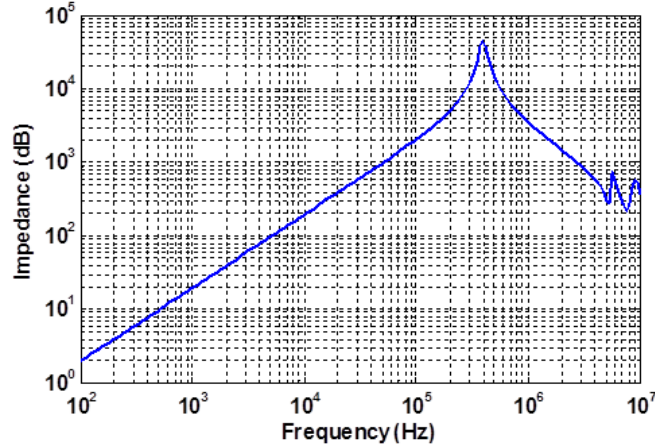


Fig. 3.54: Impedance measurement of fabricated  $L_{CM}$

### 3.3.1.3. Experimental Evaluation

The experimental evaluation is conducted under a 10 kW single-phase grid-connected PWM converter prototype with a DSP-FPGA digital control platform. The converter parameters are shown in Table 2.1. The HPF implemented in DSP is a three-order Chebyshev type I filter. As shown in Fig. 55, about 50 V of the low-frequency dc CM voltage ripple (measured between negative dc-rail and ground) appears without the proposed controller under 5 kW power condition. The input ac voltage is 240 V rms, and the dc-link voltage is regulated at 500 V. The proposed CM voltage controller regulates the ripple within 2 V, as seen in Fig. 56, reducing the low-frequency dc leakage current accordingly by more than 90%.



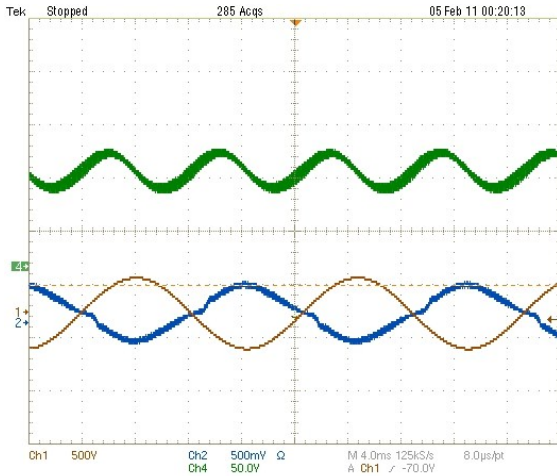


Fig. 3.55: Grid-connected ac power regulation without the proposed CM voltage control. Negative dc-rail CM voltage  $v_{dc\_N}$  (green) [50V/DIV], Grid voltage  $V_{ac}$  (orange) [500V/DIV], Ac current  $I_{ac}$  (blue) [50A/DIV]

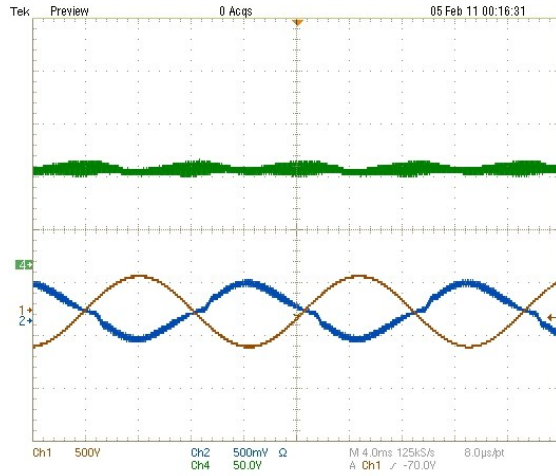


Fig. 3.56: Grid-connected ac power regulation with the proposed CM voltage control. Negative dc-rail CM voltage  $v_{dc\_N}$  (green) [50V/DIV], Grid voltage  $V_{ac}$  (orange) [500V/DIV], Ac current  $I_{ac}$  (blue) [50A/DIV]

Fig. 3.57 shows the measured CM voltages of 380 V dc-bus voltages under 7.5 kW condition. Without the proposed active controller, the low-frequency CM voltage ripple reaches around 70 V. Fig. 3.58 shows the same variables with the proposed controller under the same test condition. The CM voltage ripple is reduced lower than 5V.

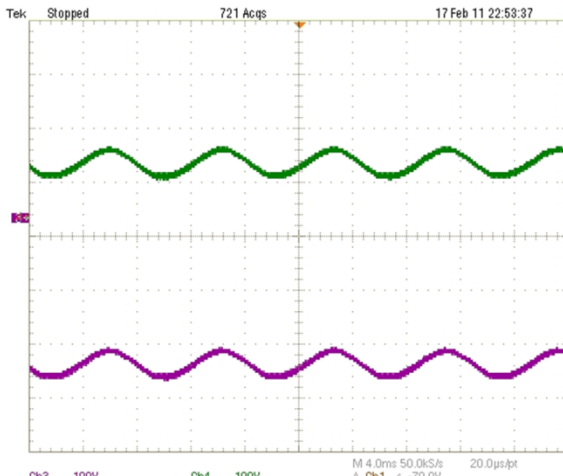


Fig. 3.57: Positive and Negative dc-rail CM voltage of 380 V dc-bus [100V/DIV] without the proposed active controller

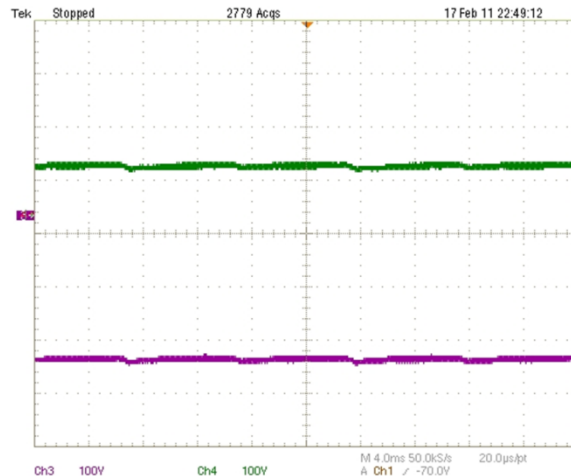


Fig. 3.58: Positive and Negative dc-rail CM voltage of 380 V dc-bus [100V/DIV] with the proposed active controller

Fig. 3.59 shows the current  $i_c$  flowing into the mid-point of dc-link, as labeled in Fig. 3.21. Only 0.6 rms A current is observed, showing a very small power loss caused by the modified filter structure and the proposed controller.

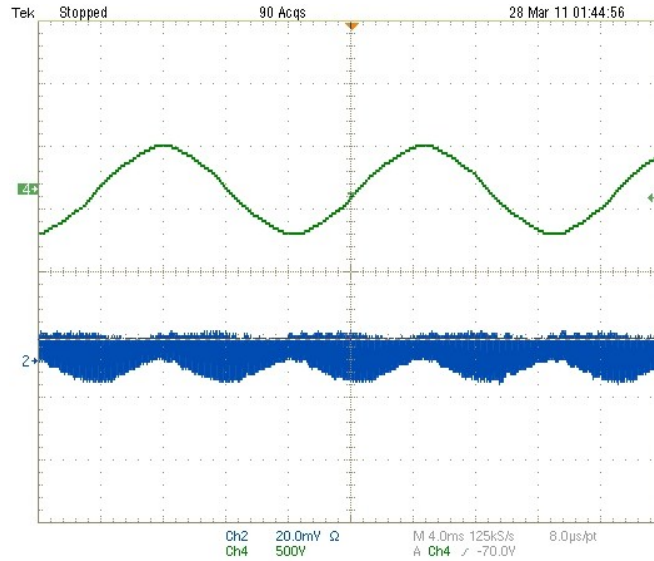


Fig. 3.59: Current flowing into the mid-point of dc-link  $i_c$  (blue) [2A/DIV], Grid voltage  $V_{ac}$  (green) [500V/DIV]

### 3.3.2. LOW-FREQUENCY DC-SIDE CM VOLTAGE RIPPLE REDUCTION IN THREE-PHASE SYSTEMS

Although the low-frequency CM voltage source has been eliminated by using the carrier-based PWM modulation method, the dc-side low-voltage CM voltage ripple still exists due to multiple reasons, such as asymmetrical phase-legs, dead time, non-identical components, unbalanced input voltage, and input harmonics. Fig. 3.60 and Fig. 3.61 show the two simulation conditions under the balanced input and the unbalanced input conditions, respectively. Both conditions reveal the dc-side low-frequency CM voltage ripple, which is more severe under the unbalanced input condition.

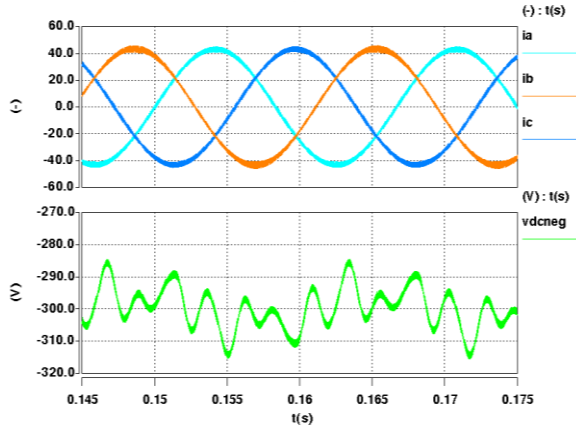


Fig. 3.60: Negative dc-rail CM voltage under balanced input condition. Top waveforms show three-phase inductor current (upper waveform) [20A/DIV], and bottom waveform shows the negative dc-rail CM voltage  $v_{dc\_N}$  [10V/DIV]

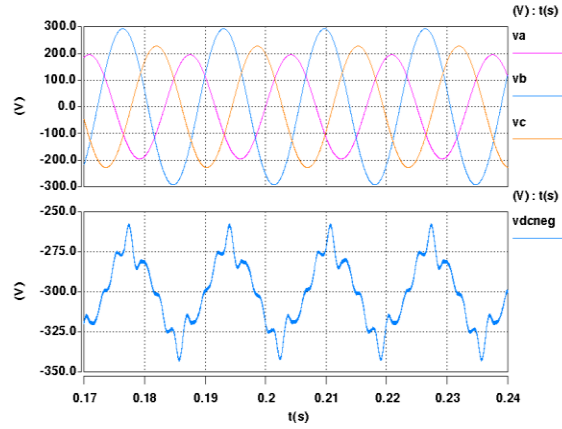


Fig. 3.61: Negative dc-rail CM voltage under unbalanced input condition. Top waveforms show three-phase input voltage (upper waveform) [100V/DIV], and bottom waveform shows the negative dc-rail CM voltage  $v_{dc\_N}$  [25V/DIV]

The proposed solution, similar as the single-phase case, is to use the active filter method. Using the open-loop PQ control as an example, as shown in Fig. 3.62, the negative dc-rail CM voltage is measured to generate a CM duty cycle  $d_{CM}$ , and the current-loop control is accomplished in the  $d$ - $q$  frame.

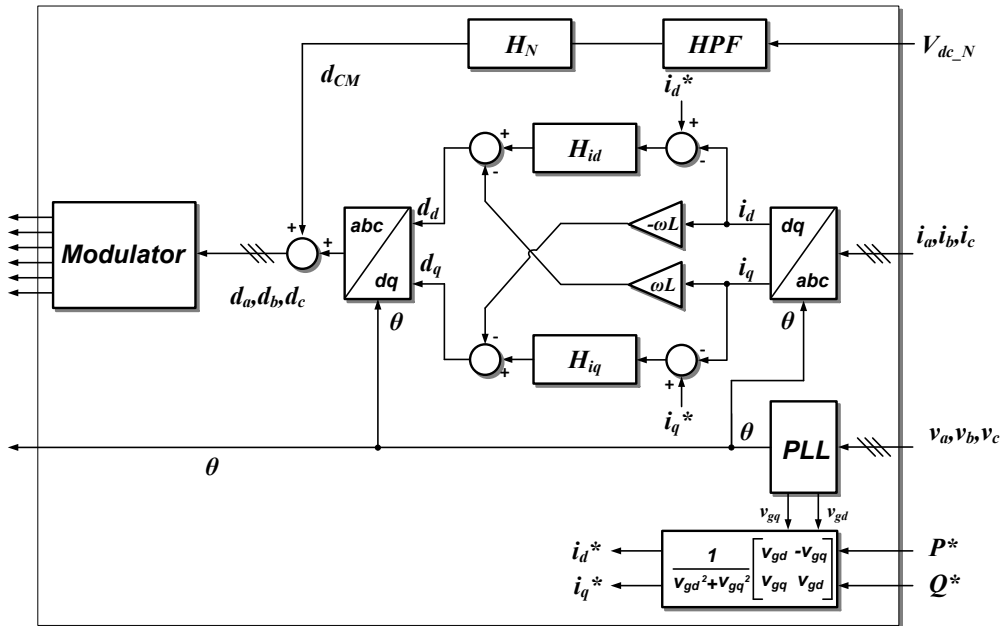


Fig. 3.62: Open-loop PQ control with proposed CM voltage control

The control design consideration and procedure are exactly the same as the single-phase case. By using the proposed CM voltage control, the CM voltage ripple can be

reduced by more than 80% under both balanced and unbalanced input conditions, which are shown in Fig. 3.63 and Fig. 3.64, respectively.

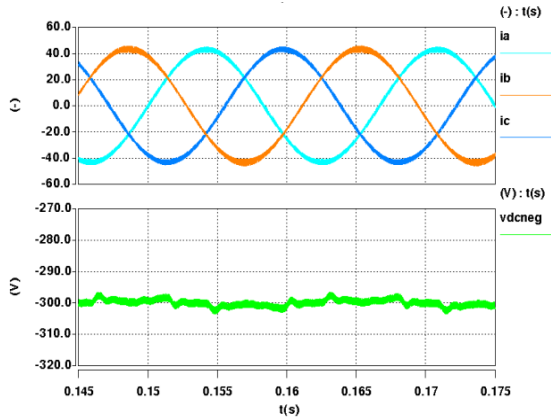


Fig. 3.63: Negative dc-rail CM voltage under balanced input condition with proposed control. Top waveforms show three-phase inductor current (upper waveform) [20A/DIV], and bottom waveform shows the negative dc-rail CM voltage  $v_{dc\_N}$  [10V/DIV]

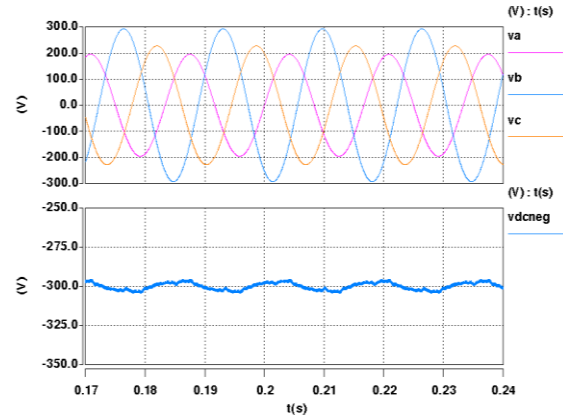


Fig. 3.64: Negative dc-rail CM voltage under balanced input condition with proposed control. Top waveforms show three-phase input voltage (upper waveform) [100V/DIV], and bottom waveform shows the negative dc-rail CM voltage  $v_{dc\_N}$  [25V/DIV]

### 3.3.3. LOW-FREQUENCY DC-SIDE CM VOLTAGE RIPPLE REDUCTION IN ASYMMETRICAL SINGLE-PHASE SYSTEMS

The previous proposed active filter method can be applied to reduce the low-frequency CM voltage ripple. But it generates a large CM duty-cycle, which needs either to lower the modulation index or to increase the dc-link voltage level. Thus, for the interface between asymmetrical single-phase and dc system, the most straightforward solution is to have an additional isolation stage.

Another solution which can decouple the dynamics between ac and dc-side on both DM and CM properties is to use the symmetrical two-stage topology, as shown in Fig. 3.65. The second-stage achieves more controllability of the dc-side common-mode voltage level at any value (between  $-0.5V_{dc}$  and  $0.5V_{dc}$ ), which is also a topology solution if the future dc standards have a strict requirement of dc CM voltage level. This topology also provides both short-circuit and ground-fault protections by turning off the switches.

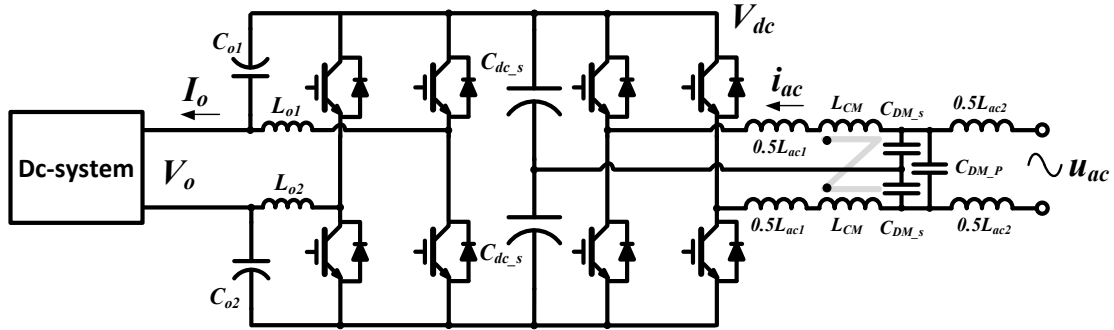


Fig. 3.65: Two-stage approach with both ac, dc CM decoupled operation; the first-stage can be either single or three-phase VSC

### 3.3.4. CONCLUSION

A low-frequency dc CM voltage active controller and a modified modulation scheme are proposed for a single-phase grid-connected full-bridge PWM converter system. The controller is based on a modified ac passive filter structure to effectively reduce both the high-frequency and the low-frequency dc CM voltage noise and the associated dc leakage current. The volt-second issue for the ac CM choke design is also discussed.

## 3.4. EMI ATTENUATION IN BUS-INTERFACE BI-DIRECTIONAL CONVERTER SYSTEM

### 3.4.1. INTRODUCTION

The high-frequency switching of the current and voltage in power electronics can easily generate the fast  $di/dt$  and  $dv/dt$  noises, namely the EMI noises. The EMI noises which propagate in the system can potentially harm the neighbor component and deteriorate the system operation. Typically, an electrical system, as shown in Fig. 3.66, with power electronics converters can be categorized, in terms of EMI study, into the EMI noise source and victim, which normally are the power electronics converters and the system that ties to the converters, e.g., grid, respectively.

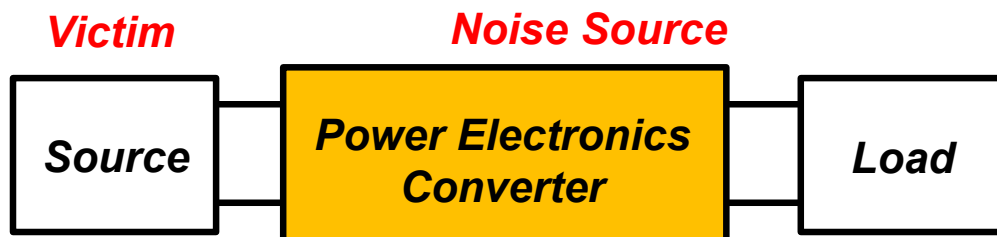


Fig. 3.66: A system with power electronics

The total EMI noises produced in a system can be categorized into conducted and radiated EMI noises. The range of conducted EMI is determined by the application of the product. Most residential and commercial applications regulate the conducted region between 150 kHz and 30 MHz. Some military or sensitive applications go as far down at 10 kHz while above 10-30 MHz is usually considered radiated noise. Radiated EMI is typically for the frequencies above the conducted region; it will not be considered here since it has fundamental differences from the focus of this study. As shown in Fig. 3.67, there have been extensive researches on the EMI mitigation in the power converters in appliances and IT equipment. Several EMI standards prevail for measurement between ac load and ac source by using the EMI measurement tool: LISN which provides the DM and CM impedance as required. The reason of using LISN is to decouple the impact of the various sources on measurement system.

The growing adoption of dc distribution system and long dc cable require the consideration of the dc-side EMI noise mitigation. Some of the standards, e.g., FCC Part 15, are being used for low-power dc-dc converters in the distributed power system in telecoms applications, and a set of standards [93] define the dc-side EMI limit in the dc-fed motor drives as seen in Fig. 3.68. However, in a generic distribution system, the dc-side EMI measurements are still in question and waiting for standards. For example, several studies [88, 89, 91] on dc-side EMI measurement in the PV grid-interface system, since no standards, directly use the measurement setup for ac-side. Reference [90] presents a LISN whose CM impedance is  $150\ \Omega$  for the RF measurement on the dc side.

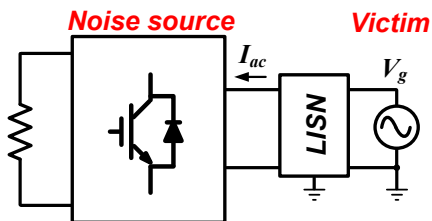


Fig. 3.67: Ac-side EMI measurement in PFC system

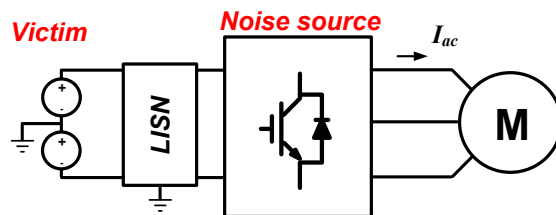


Fig. 3.68: Dc-side EMI measurement in dc-fed motor drives

Many applications require both the ac and dc side EMI noise to be attenuated. Examples are seen in battery-charger systems in EV, bus-interface bi-directional converter in ac/dc distribution system, large-scale PV systems. The common characteristic of these systems is that both-side of the converter are actually “distribution

buses” tied with many other components. Although, the dc-fed motor drives need the mitigation of both ac and dc-side EMI. However, only dc-side can still be regarded as the bus-interface and need a LISN.

Notice that LISN is to isolate between power source and power converters. Thus, for those bi-directional converter systems, LISN has to be used on both sides for isolation and measurement, which eventually leads to the dilemma. If LISN is put on the dc-side for noise measurement, the ac system will be included in the measurement system, vice versa. As shown in Fig. 3.69, the ac system grounding scheme influence the dc-side noise measurement. If two LISN are put on both ac and dc-side to isolate both ac and dc bus impact, as shown in Fig. 3.70, an additional CM propagation path forms due to the LISNs which dramatically change the EMI propagation characteristics.

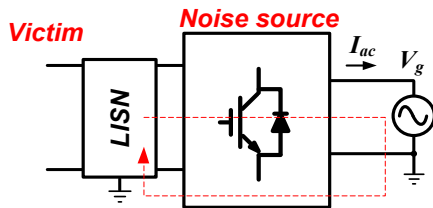


Fig. 3.69: Dc-side EMI measurement using one LISN in bus-interface bi-directional converter

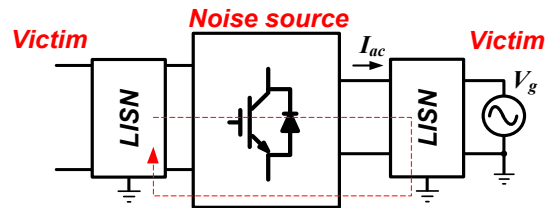


Fig. 3.70: Dc-side EMI measurement using two LISNs in bus-interface bi-directional converter

The tentative EMI measurement of bi-directional converter in this chapter is to use one LISN and follow the typical EMI measurement setup and procedure. However, this EMI measurement issue needs further standardization of EMI measurement in bi-directional bus-interface converter system.

The following discussion presents one specific EMI filter design issue in this bus-interface bi-directional converter system, showing how dc and ac-side CM noises are strongly coupled and eventually influences the filter design. Ac-dc single-phase bus-interface system is used for analysis.

### 3.4.2. GROUNDING CAPACITOR IMPACT IN EMI FILTER DESIGN ON BOTH-SIDES

The basic EMI filter structure in the utility bi-directional converter system can be found in Fig. 3.71. The objective of EMI filter design is to attenuate the EMI noise on both-side.

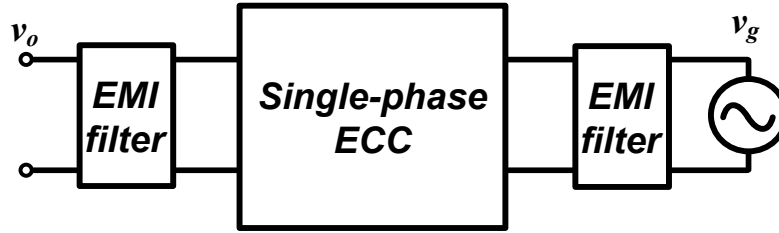


Fig. 3.71: EMI filter in single-phase ECC converter

Ac and dc-side differential-mode (DM) noises are decoupled due to the relatively large dc-link capacitor inside the ECC converter [95]. Therefore, the DM filter can be designed independently by identifying the ac and dc-side DM source/loop impedances as well as the attenuation requirement; the typical EMI filter design procedure can be used to attenuate the DM noises level. The dc and ac-side CM noises, however, are fully coupled via the ground plane, which is illustrated by a typical CM equivalent circuit (Fig. 3.72) where  $V_{CM}$  is the equivalent CM noise source due to the PWM switching.

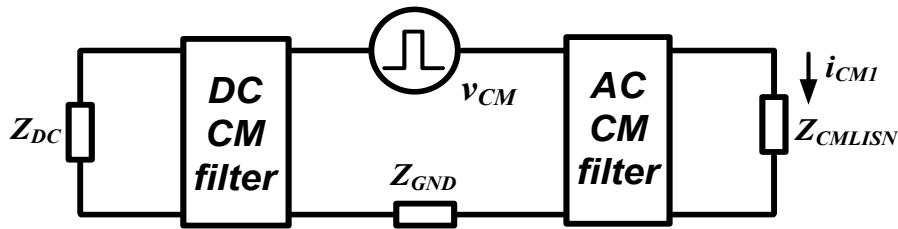


Fig. 3.72: CM equivalent circuit of voltage-source converter system

The CM filter design in turn becomes much more complicated. The dc-side CM EMI filter, for example, will change the CM propagation path impedance [95, 96], thereby requiring redesign of the ac-side CM filter and vice versa. CM capacitors are commonly used in switching power electronics for CM noise reduction. As shown in Fig. 3.73, the typical ac and dc CM filters are implemented.

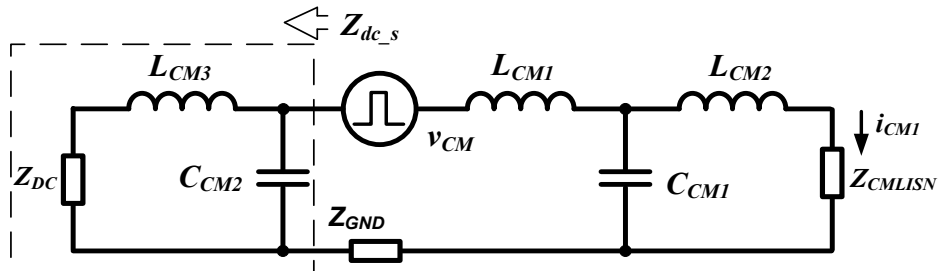


Fig. 3.73: CM equivalent circuit with DC and AC CM filter



The grounding capacitor ( $C_{CM2}$ ) bypasses the CM noise, thus reducing the dc-side CM noise; however, more noises will be measured on the ac-side [95]. This can be also explained from an impedance perspective. As shown in Fig. 3.73, the dc-side component can be simply modeled as a source impedance  $Z_{dc\_s}$  for ac-side filter design, and large  $C_{CM2}$  reduces this source impedance. Without  $C_{CM2}$ , the  $Z_{dc\_s1}$  in (45) is mainly determined by a dc stray capacitance whose impedance  $Z_{DC}$  is much higher than  $Z_{dc\_s2}$  in (46) with  $C_{CM2}$ . Thus the total CM prorogation path impedance with  $C_{CM2}$  is much smaller, leading to higher ac-side noise. The ac-side grounding capacitors will have the same effect to the dc-side CM noise level.

$$Z_{dc\_s1} = Z_{DC} + Z_{LCM3} \approx Z_{DC} \quad (45)$$

$$Z_{dc\_s2} = (Z_{DC} + Z_{LCM3}) // Z_{CCM2} \approx Z_{CCM2} \quad (46)$$

Therefore, the EMI filter design in bi-directional converter system has to pay more attention to the CM grounding capacitors. It's better to reduce the grounding capacitors value or use some approach to decouple the grounding capacitor impact to both ac and dc-side CM EMI filter design.

### 3.4.3. FLOATING FILTER IN BI-DIRECTIONAL CONVERTER SYSTEM

As discussed in previous chapters, a modified ac filter structure is introduced to reduce the dc-side leakage current level. As a matter of fact, the proposed ac filter has a strong performance improvement on the ac-side CM noise level. And this filter is renamed as a floating filter. So firstly, the ac-side CM noise attenuation can be compared between the normal ac filter and the floating filter.

In order to simplify the discussion, the heatsink is considered to be floated firstly, without any ground connection on it. Then, the stray capacitance between the device and ground, which would be the stray capacitance between device and heatsink in series with the stray capacitance between heatsink and ground, can be ignored due to the small value.

The EMI noise attenuation improvement is obtained by comparing the CM noise currents measured by the ac LISN between the circuit in normal ac filter in Fig. 3.74, and with the floating filter in Fig. 3.75.  $Z_1$  and  $Z_2$  are the impedance of equivalent CM choke;  $Z_{dc\_s}$  is the impedance of the dc-side equivalent CM components;  $Z_{GND}$  is the impedance

of the copper ground plane;  $Z_{CMLISN}$  is the CM impedance of the ac LISN.  $Z_3$  in Fig. 3.75 is the impedance of the floating filter return path.

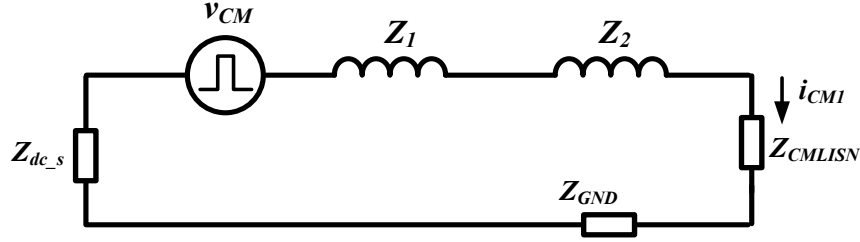


Fig. 3.74: CM equivalent with a normal ac filter

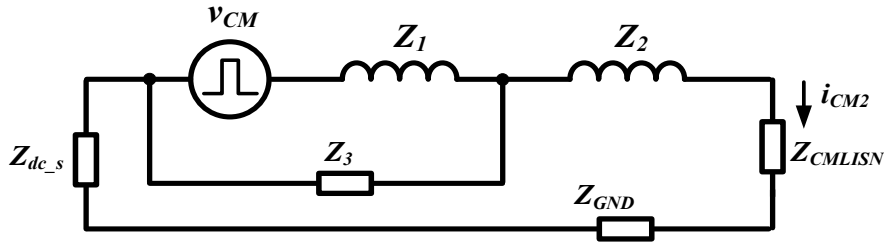


Fig. 3.75: CM equivalent with a floating filter

The CM current measured by ac LISN in both circuits are shown in (47).  $i_{CM1}$  is obtained by the assumption that  $Z_3 \ll Z_2$ .

$$\begin{cases} i_{CM1} \approx v_{CM} \frac{Z_3}{Z_3 + Z_1} \frac{1}{Z_2 + Z_s + Z_{GND} + Z_{CMLISN}} \\ i_{CM2} = v_{CM} \frac{1}{Z_1 + Z_2 + Z_s + Z_{GND} + Z_{CMLISN}} \end{cases} \quad (47)$$

The insertion gain ( $i_{CM1}/i_{CM2}$ ) is shown below.

$$\begin{aligned} H_{insertion} &\approx 20 \log_{10} \left( \left| 1 + \frac{Z_1}{Z_3} \frac{1}{\frac{Z_1}{Z_2 + Z_s + Z_{GND} + Z_{CMLISN}} + 1} \right| \right) \\ &= 20 \log_{10} \left( \left| 1 + \frac{Z_1}{Z_3} \right| \right) + 20 \log_{10} \left( \left| \frac{1}{\frac{Z_1}{Z_2 + Z_{dc_s} + Z_{GND} + Z_{CMLISN}} + 1} \right| \right) \end{aligned} \quad (48)$$

The two terms determines the attenuation improvement. Due to the lumped component of  $Z_1$  and  $Z_3$ , the attenuation improvement throughout the frequency range is

mainly due to the first term. However, the second-terms will change the improvement in high frequency range, especially around the resonant frequency of  $(Z_2, Z_{dc\_s})$ . Since  $Z_1 \gg Z_3$ , large attenuation improvement can be accomplished.

A simulation circuit is built to identify the analysis. The first simulation is conducted under the circuit model as shown in Fig. 3.76. All the components in simulation are shown in Table 3.7.

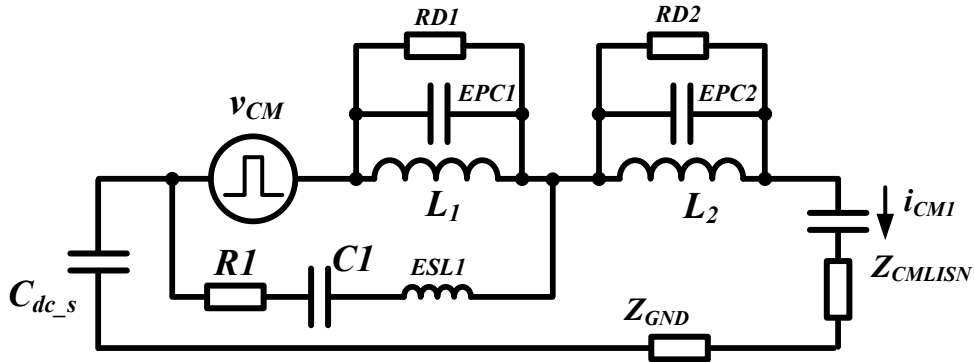


Fig. 3.76: CM equivalent circuit with major components parasites

Table 3.7: Lumped components in simulation

$L_1$	$L_2$	$Z_{dc\_s}$	$R_1$	$C_1$	$Z_{CMLISN}$
3 mH	2 mH	1 nF	2	11 uF	0.2 uF + 25 $\Omega$
$Z_{GND}$	$ESL1$	$EPC1$	$EPC2$	$RD1$	$RD2$
0	10 nH	20 pF	10 pF	100 k $\Omega$	150

The in-circuit attenuation results  $(i_{CM}/v_{CM})$  are shown in Fig. 3.77, where the blue color and purple color waveforms are the result for Fig. 3.74 and Fig. 3.75, respectively. It is clearly seen that the floating filter provides a large CM noise attenuation improvement. The insertion gain  $H_{insertion}$  is shown in Fig. 3.78.

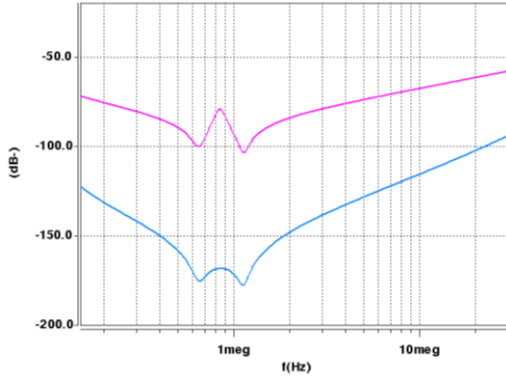


Fig. 3.77: Simulation results of in-circuit attenuation ( $i_{CM1}/v_{CM}$ ): purple waveform is  $i_{CM1}/v_{CM}$ ; blue waveform is  $i_{CM2}/v_{CM}$

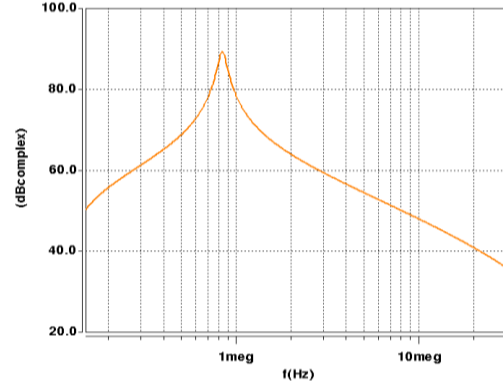


Fig. 3.78: Insertion gain ( $i_{CM1}/i_{CM2}$ ) achieved by the floating filter

However, if the converter heatsink is grounded, the stray capacitance ( $\sim 50$  pF) between device and ground cannot be ignored. Then the CM equivalent circuit with the floating filter would be shown in Fig. 3.79.  $Z_s$  is the CM impedance of the stray capacitance between devices and ground.

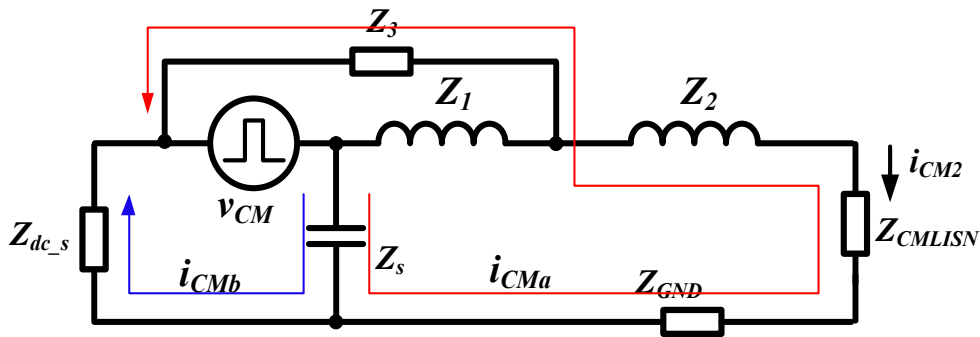


Fig. 3.79: CM equivalent circuit by considering the stray capacitor between device and ground

It is seen that two additional CM propagation paths forms as shown in the red and blue color. The red-color CM current flow through the LISN, so that the CM noise actually increases due to this, whereas this CM noise doesn't exist in normal ac filter structure. Therefore, the CM noise attenuation improvement by using floating filter when the heatsink is grounded would not as big as the one when the heatsink is floated.

Firstly the  $Z_s$  and  $Z_{dc_s}$  form as a voltage divider, and the  $Z_{dc_s}$  is in parallel with the impedance in the red path. A simplified circuit which only considers the two additional CM current paths ( $i_{CMa}$ ,  $i_{CMb}$ ) is shown in Fig. 3.80. Smaller voltage applied on  $Z_{dc_s}$  will

results in smaller  $i_{CMa}$ . Therefore, the additional current following into LISN is proportional to  $Z_{dc\_s}/(Z_s+Z_{dc\_s})$ .

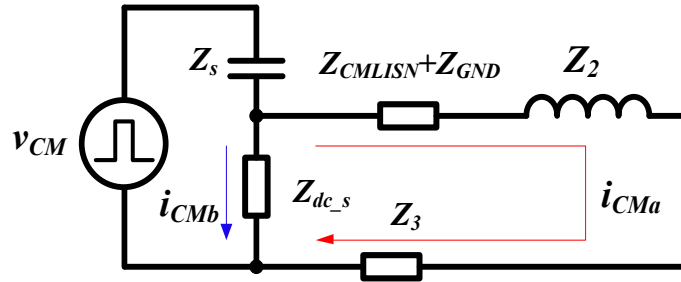


Fig. 3.80: Simplified CM equivalent circuit by considering the stray capacitor between device and ground

The simulation is conducted by considering the  $Z_s$ , which is 50 pF. The in-circuit attenuation ( $i_{CM}/v_{CM}$ ) are shown in Fig. 3.81. The orange waveform is the result without  $Z_s$ . The purple waveform is the result with 50 pF  $Z_s$  and 1 nF  $Z_{dc\_s}$ , while the blue waveform is the result with 50 pF  $Z_s$  and 2 nF  $Z_{dc\_s}$ . It is clearly seen that the attenuation achieved by the floating filter is increased by adding more dc grounding capacitor.

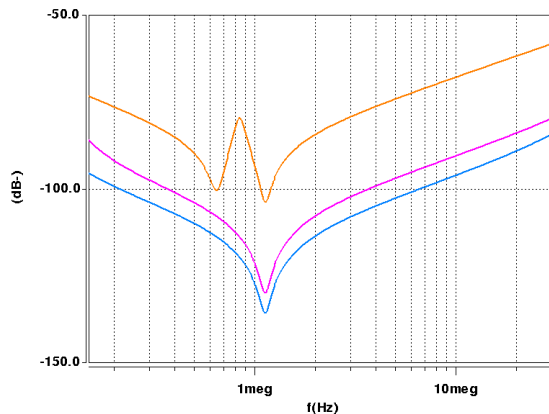


Fig. 3.81: In-circuit attenuation of  $i_{CM}$ : maroon color is result without  $Z_s$ ; purple and blue plots are the results with (50 pF  $Z_s$  1 nF  $Z_{dc\_s}$ ) and (50 pF  $Z_s$  2 nF  $Z_{dc\_s}$ ), respectively

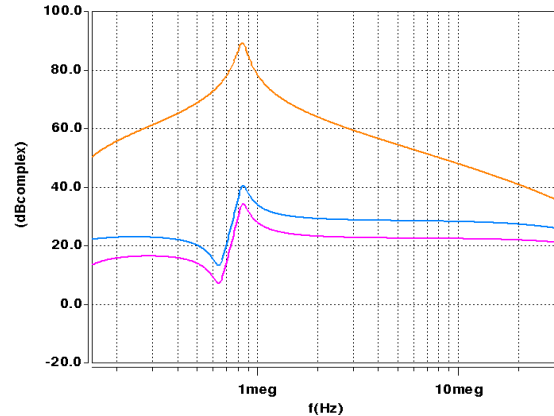


Fig. 3.82: Attenuation improvement by floating filter: maroon color is result without  $Z_s$ ; purple and blue plots are the results with (50 pF  $Z_s$  1 nF  $Z_{dc\_s}$ ) and (50 pF  $Z_s$  2 nF  $Z_{dc\_s}$ ), respectively

It is seen that bigger  $Z_{dc\_s}$  helps reduce the ac-side CM noise after the resonant frequency ( $Z_{dc\_s}, Z_2$ ) with the floating filter structure. Therefore, the floating filter reduces the ac CM noise but also decouple the impact of  $Z_{dc\_s}$  to the ac-side.

As mentioned before, the dc-side EMI measurement is not clear so far. On the dc-side, the utility-interface bi-directional converter is also tied to the bus, so a LISN is needed for measurement. Tentatively, the standard in aircraft [181] is used to design and measure the

dc-side EMI. However, the placement of LISN will change the real operation, due to additional ground loops. In order to isolate the ground loop, the transformer is connected on the ac-side. A CM equivalent circuit for dc-side EMI measurement is shown below in Fig. 66. Additional CM choke  $L_3$  (2 mH) is put for dc-side CM noise attenuation.  $C_{ac\_s}$  (e.g., 10 nF) is the ac-side grounding capacitor. There are two CM noises paths which are measured by dc-side LISN, as shown in Fig. 3.83.  $Z_s$  and  $Z_{dc\_s}$  form a voltage divider, and the noise is proportional to the  $Z_{dc\_s}/(Z_s+Z_{dc\_s})$ , which become a major contributor to the noise. It can be seen that after the resonant frequency of ( $C_{dc\_s}$ , and  $L_3$ ), the noise in red path is bypassed by  $C_{dc\_s}$ , and after the after the resonant frequency ( $C_s$ ,  $L_1+L_2$ ), the noise in red path is also bypassed by  $C_s$ . Since the floating filter only reduces the CM noise in red path, the floating filter gives a limited improvement of the attenuation on the dc-side CM noise, especially in the high-frequency range.

As shown in the simulation results in Fig. 3.84, the dc-side CM noise is mostly determined by the noise in the blue path. So the in-circuit attenuation results of CM noise ( $i_{CM}/v_{CM}$ ) with and without the floating filter are very close.

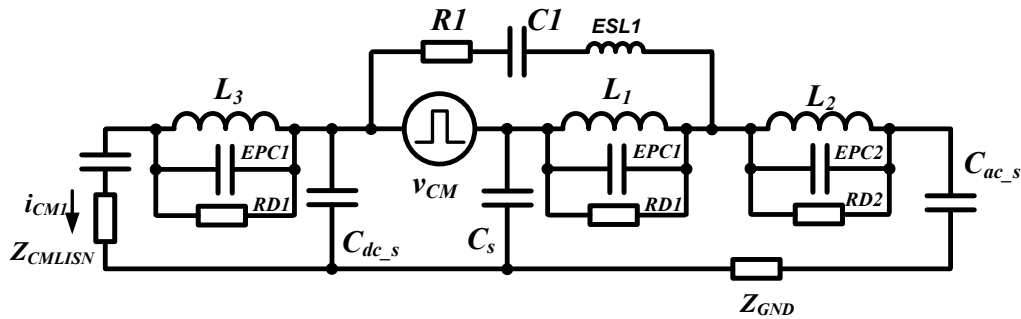


Fig. 3.83: CM equivalent circuit for dc-side CM noise measurement

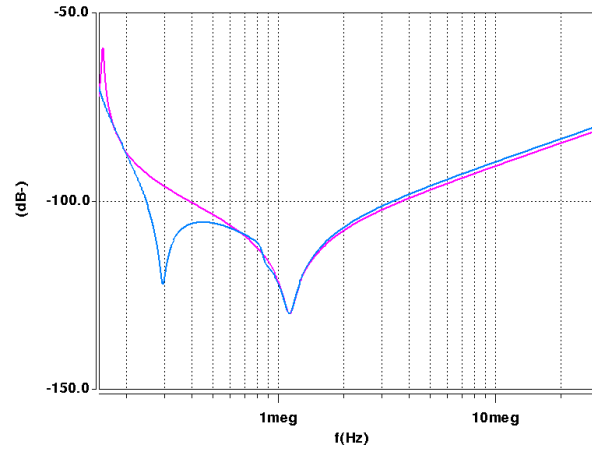


Fig. 3.84: In-circuit attenuation of CM noise ( $i_{CM}/v_{CM}$ ) with (purple) and without (blue) the floating filter

#### 3.4.4. EMI FILTER IMPLEMENTATION AND THE NOISE MEASUREMENT

The experiments, as shown in Fig. 3.85, are conducted to measure the EMI noise level on both dc and ac-side of the utility-interface converter system. Using the same filter structure in Fig. 3.21, the floating filter CM noise attenuations are measured. When the heatsink is floated, the CM EMI noises with and without the floating filter (disconnect the return path) are shown below in Fig. 3.86. It is seen that a large attenuation is achieved by the floating filter.



Fig. 3.85: EMI measurement setup

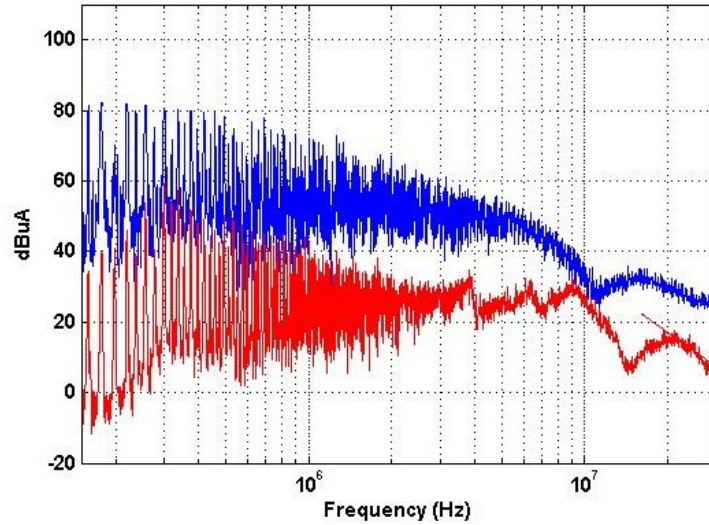


Fig. 3.86: Ac-side CM noise measurement with (red) and without (blue) the floating filter when heatsink is floated

The measured ac-side CM noises with and without the floating filter, when the heatsink are grounded, are shown in Fig. 3.87. Due to the stray capacitance between devices and ground, the attenuation improvement is not as much as of the ungrounded heatsink condition.

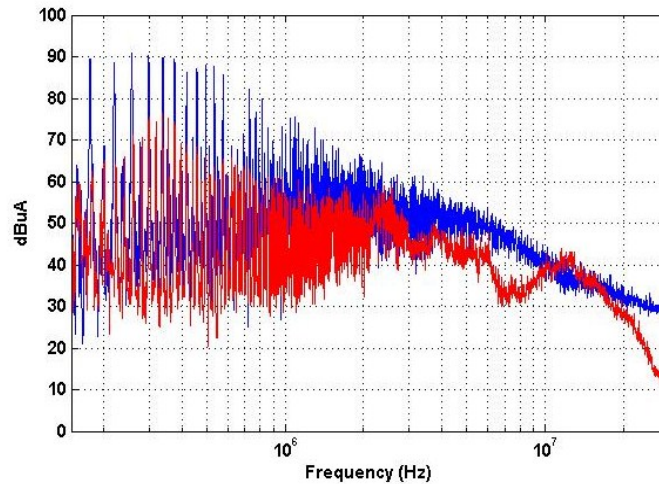


Fig. 3.87: Ac-side CM noise measurement with (red) and without (blue) the floating filter when heatsink is grounded

If a 1.5 nF grounding capacitors are added on the dc-link, the CM noise measurement results is shown in Fig. 3.88. About 10 dB more attenuation is achieved by the floating filter, simply because lower  $Z_{dc\_s}$  help reduces the CM noise  $i_{CMa}$  in Fig. 3.79, so the performance of floating filter approaches the ungrounded heatsink case.



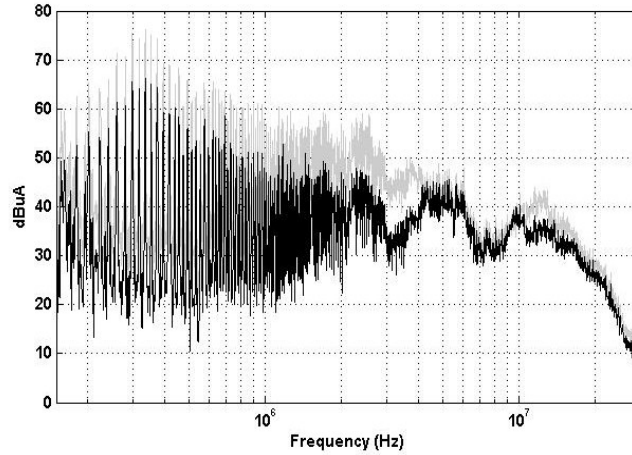


Fig. 3.88: Ac-side CM noise measurement results with floating filter (grey) and result by adding additional 1.5 nF grounding capacitor on dc-link (black)

The ac-side filter structure is shown in Fig. 3.89 with a multi-stage EMI filter. The parameters are shown in Table 3.8, and the total EMI noise measurement is shown in Fig. 3.90. The DM filter has two stages:  $L_{ac1}$ ,  $(C_{DM\_P}+0.5C_{DM\_S})$ ,  $L_{ac2}$ ,  $C_{DM2}$ . As discussed before,  $L_{ac1}$ ,  $(C_{DM\_P}+0.5C_{DM\_S})$ ,  $L_{ac2}$  also forms as a LCL harmonic filter, so the  $C_{DM2}$  is designed and tuned simply to meet the EMI specification according to the terminal DM EMI spectrum in Fig. 3.13.

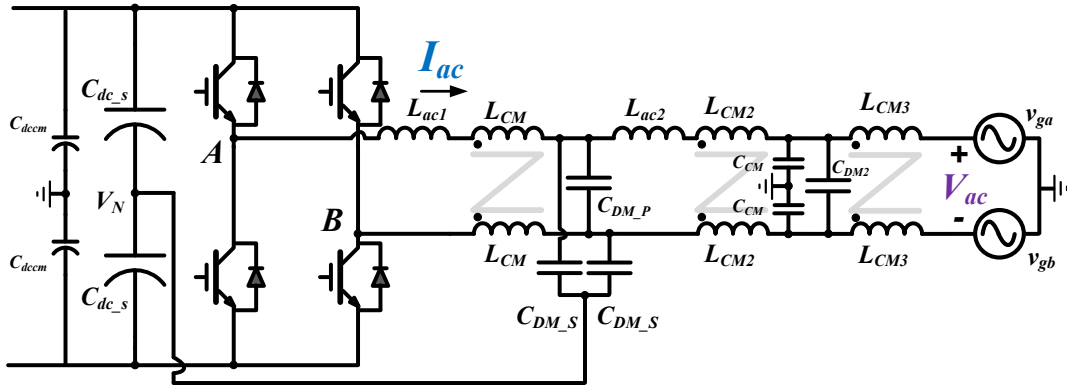


Fig. 3.89: AC-side converter filter structure

Table 3.8: Ac passive filter value

Symbol	Value	Symbol	Value
$L_{ac1}$	260 $\mu$ H	$C_{dcm}$	1.5 nF
$C_{DM\_S}$	5.6 $\mu$ F	$L_{CM3}$	2 mF
$C_{DM\_P}$	6.6 $\mu$ F	$C_{CM}$	3 nF
$L_{ac2}$	25 $\mu$ F	$C_{DM2}$	1.5 $\mu$ F
$L_{CM}$	3.5 mF	$C_{dc\_s}$	50 $\mu$ F
$L_{CM2}$	2 mF		

The CM filter includes a floating filter and additional two-stage T type EMI filter:  $L_{CM2}$ ,  $C_{CM}$ , and  $L_{CM3}$ . The design criterion is the impedance mismatch.  $L_{CM3}$  is used due to the small CM LISN impedance ( $\sim 25 \Omega$ ).  $L_{CM2}$  is for impedance mismatch with  $C_{DM_s}$ , fully utilizing the floating filter. The design is based on the terminal CM noise spectrum in Fig. 3.14. Due to  $C_{dcm}$ , which dominates the dc-side CM impedance, the CM propagation path impedance can be roughly estimated. Several iterations according to test are needed after the initial design.

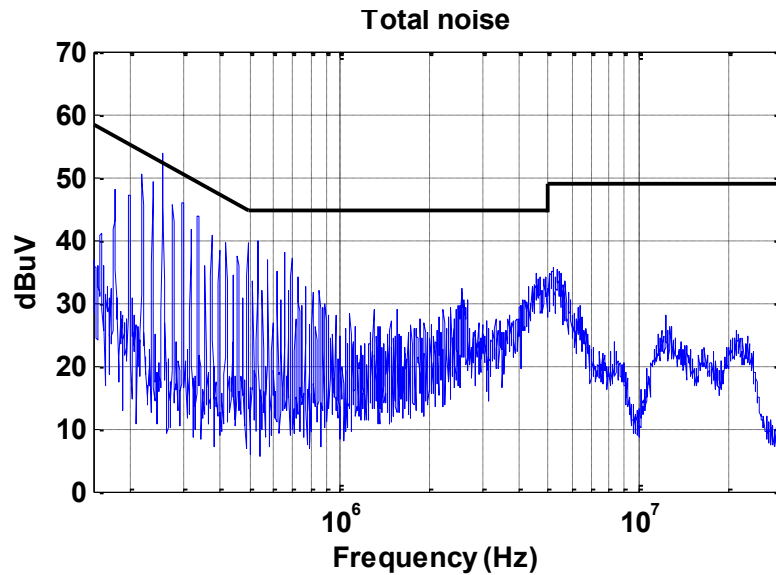


Fig. 3.90: AC-side total EMI noise measurement

Fig. 3.91 shows the dc-side filter structure, and the parameters are shown in Table 3.9.

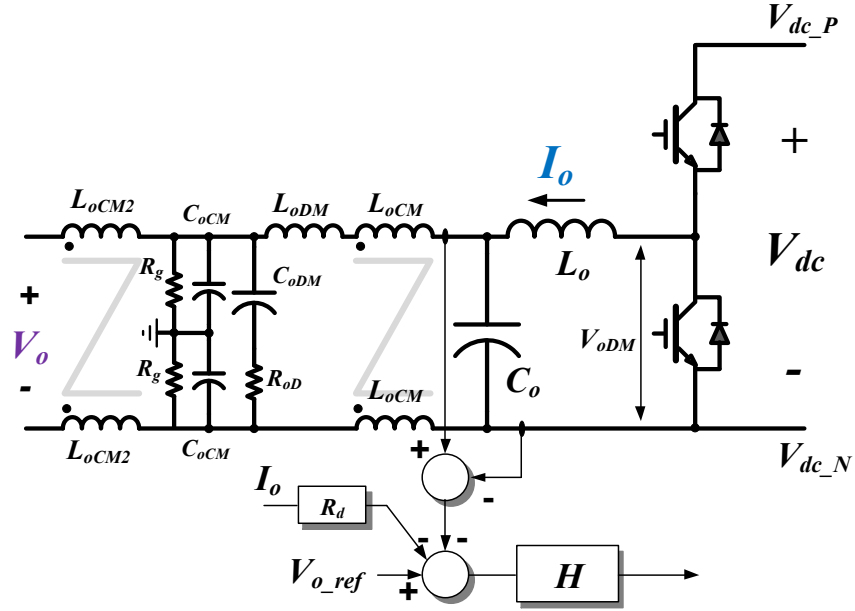


Fig. 3.91: Dc-side converter filter structure

Table 3.9: Dc passive filter value

Symbol	Value	Symbol	Value
$L_o$	380 $\mu$ H	$C_{oCM}$	5 nF
$C_o$	110 $\mu$ F	$R_g$	100 k $\Omega$
$L_{oCM}$	15 mF	$L_{oCM2}$	2 mH
$L_{oDM}$	5 $\mu$ F	$C_{oDM}$	25 $\mu$ F
$R_{oD}$	0.5 $\Omega$		

A two-stage DM filter,  $L_o$ ,  $C_o$ ,  $L_{oDM}$ ,  $C_{oDM}$ , is used for DM noise attenuation. The design is based on the simulated terminal DM noise  $V_{oDM}$  with the closed-loop control, as shown in Fig. 3.92, or can be estimated roughly by equation (48) with open-loop constant duty-cycle. However, (48) will give some error due to the neglect of the duty-cycle ripple.

$$V_{oDM}(n\omega_s) = \frac{2}{n} \frac{V_{dc}}{\pi} \sin(n\pi D) \quad (48)$$

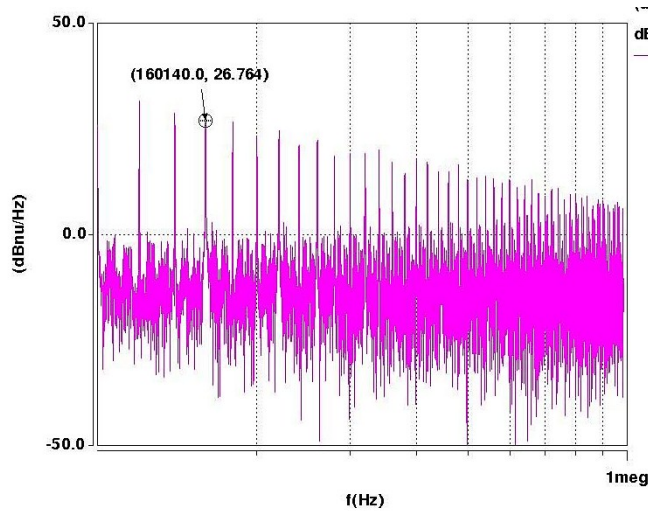


Fig. 3.92: Terminal voltage noise of the second-stage converter,  $V_{oDM}$

$L_o$  and  $C_o$  are already design based on ripple current and voltage requirement.  $L_{oDM}$  and  $C_{oDM}$  are design and tuned to meet the EMI requirement. Since the second-stage filter is outside of the control loop, a damping resistor has to be implemented to attenuate the resonant peak point of the output impedance to avoid potential system stability issue. The damping resistor is simply chosen the same as the droop resistor  $R_d$  in control system, as shown in (49), so the converter high-frequency output impedance will be the same as the low-frequency range.

$$R_{oD} = R_d \quad (49)$$

As shown in Fig. 3.93, the damping resistor  $R_{oD}$  effectively reduces the output impedance resonant peak point, and the high frequency output impedance is same as the low-frequency range, which is determined by the droop resistor.

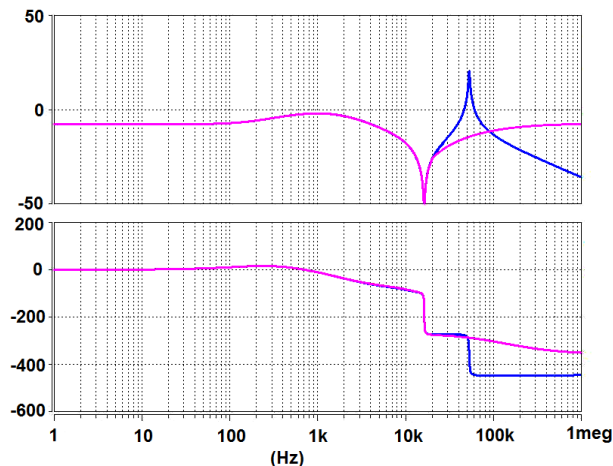


Fig. 3.93: Converter output impedance with (purple) and without (blue) the damping resistor

The grounding resistance  $R_g$  is used to clamp the dc-bus CM voltage when the dc distribution system goes into the stand-alone mode. The CM voltage will shift from (-300 V, 80 V) CM voltage to (-190 V, 190 V) due to  $R_g$ .

Two-stage CM filter is used for the CM noise attenuation. As discussed before, the dc-side CM noise is highly related to the  $C_s$ , and thus the filter needs several iterations. The  $L_{oCM2}$  is also used to block the CM noises propagated from other converters tied on the dc-bus. As shown in Fig. 3.94, the dc-side CM noise measurement results with and without the floating filter. The results show that the floating filter doesn't achieve much additional EMI noise attenuation, especially in the high-frequency range. The total EMI noise result is shown in Fig. 3.95. It is seen that the DM noise dominates the total noise. The CM filter is a little overdesigned to attenuate CM noise, simply because in the operation, lots of dc grounding capacitors contributes CM noise flowing through utility-interface converter. There are several dc-bus capacitors, so the DM noise is not as critical as CM noise.

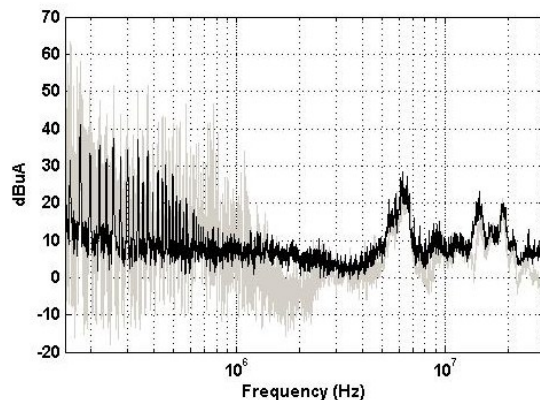


Fig. 3.94: Dc-side CM EMI noise with (black) and without (grey) the floating filter

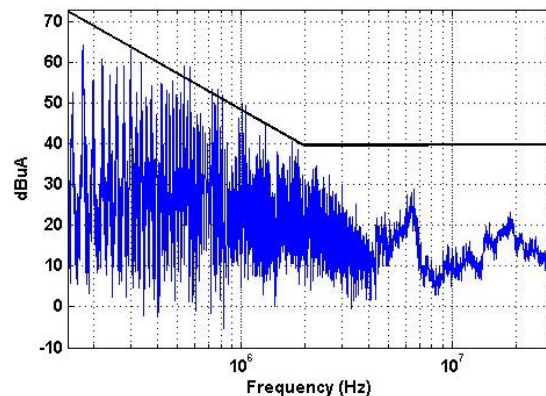


Fig. 3.95: Dc-side total EMI noise measurement result

The final circuit diagram and control system is shown below in Fig. 3.96, the physical layout and the major components are labeled in Fig. 3.97, and the complete utility-interface bi-directional converter as well as the control system is shown in Fig. 3.98.

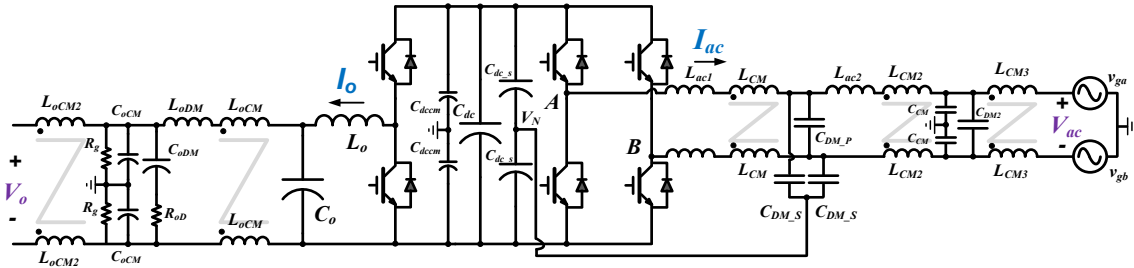


Fig. 3.96: Ac-dc bus-interface bi-directional converter system

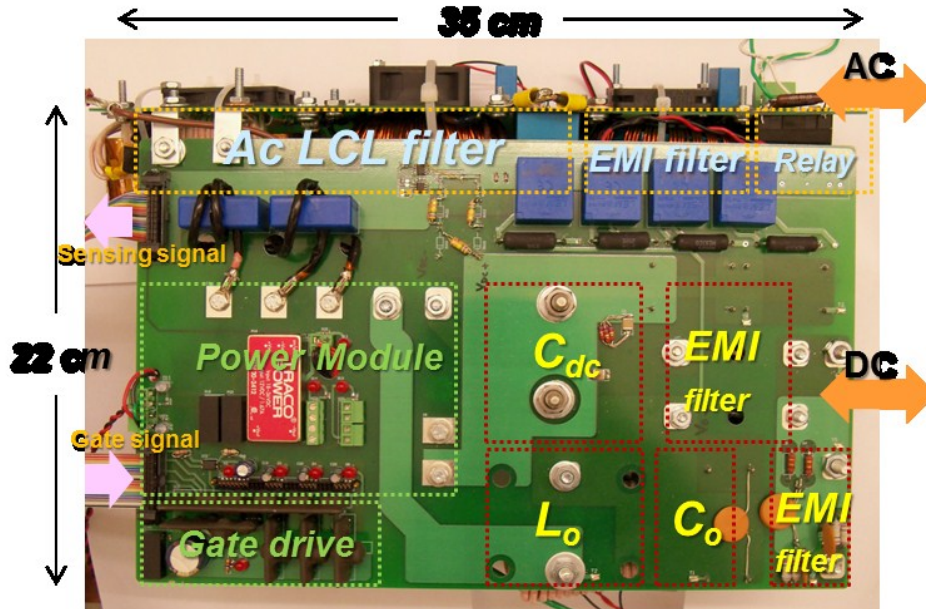


Fig. 3.97: Physical layout and the major components of the converter

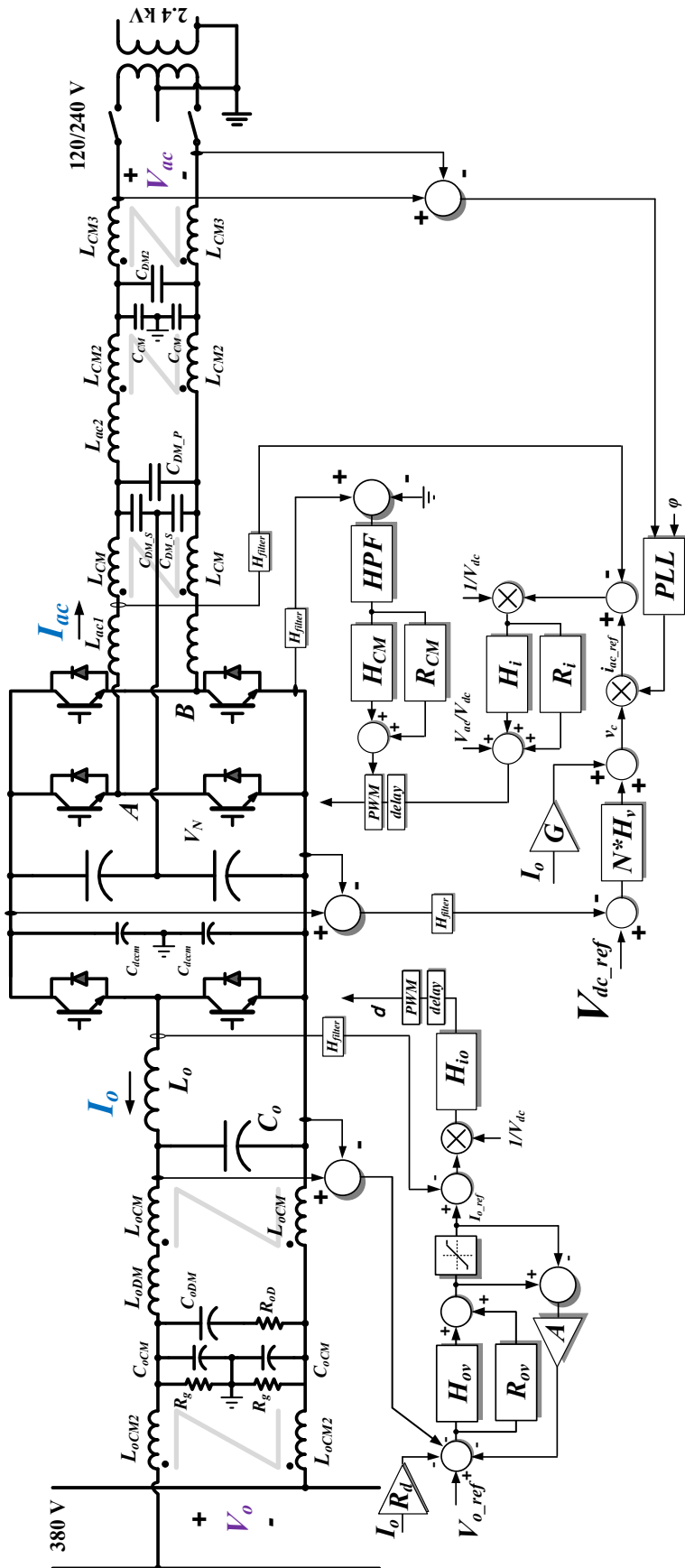


Fig. 3.98: Complete diagram of a single-phase ac-dc bus-interface bi-directional converter system

Based on the discussion in chapter two and chapter three, it is found that finding a “optimal design” in terms of both cost and volume is almost impossible. For example, dc-link capacitor reduction reduces the cost of capacitor and volume, but requires more control cost and higher rated devices. Increase of switching frequency reduces the high frequency energy-storage filter, especially the DM filter volume and cost, but increases the cooling system cost and volume; CM filter may be bigger as well.

#### **3.4.5. CONCLUSION**

The passive filter including the EMI filter structure is presented for single-phase utility-interface bi-directional converter system. The EMI filter design and consideration is presented for the system which both dc and ac-side EMI and power quality have to be considered. The floating filter not only reduces the dc-side leakage current level, but also gives a large ac-side EMI CM noise attenuation performance. Some of the filter design considerations, such as damping, saturations.



## **Chapter 4. MODELING OF GRID SYNCHRONIZATION IN AC-DC BUS-INTERFACE CONVERTERS**

This chapter presents grid synchronization, which is a major grid interface issue. First, a novel single-phase phase-locked loop (PLL) is presented to reduce the output frequency noises caused by multiple sources, and a comprehensive explanation of the modeling of PLL is given during the discussion.

Then, the discussion focuses on the converter output frequency behavior at weak grid and islanded conditions. A generic quasi-static PLL model is proposed to predict the PLL behaviors, such as the nonlinear oscillations and the frequency drifting. Many results can be directly drawn from the model to understand many grid synchronization stability issues reported from industry.

### **4.1. SINGLE-PHASE PHASE LOCKED LOOP SYSTEM**

#### **4.1.1. INTRODUCTION**

A crucial component of the single-phase ( $1\Phi$ ) power conversion system is the phase-locked-loop (PLL) that tracks the grid voltage's frequency and phase angle [101-104]. The PLL can be used not only for control and signal generation, through synthesis and transformation, but also in protection schemes to detect when the system should shut down or disconnect from the grid and enter an islanded mode of operation.

Distortions and transients often occur in the grid, such as harmonics, voltage and frequency variations, and phase shifts. A PLL must be able to phase-lock quickly and accurately, and provide low distortion outputs to the control system under all possible grid conditions. Otherwise, inaccurate and potentially harmful control of the system can arise, such as false tripping and potentially the destabilization of the grid [105-108].

Therefore, accurate, fast-responding PLLs with clean output for control and protection purposes are required to provide these measurements. This is especially

important for bus-interface bi-directional power converter systems where the power/current is regenerated back to the utility grid with a specific power factor.

As illustrated in Fig. 4.1, a typical digital PLL system is composed of a phase-detector (PD), a loop-filter (LF), and a digital-controlled oscillator (DCO) [101, 102]. The PLL synchronization speed is determined by the characteristics of the LF as well as the PD gain, and the noise in the output of the PLL  $\theta_C$  is due to the PLL loop-gain, and the input signals. Generally, the PLL structures available in the literature mainly differentiate each other by the implementation of the phase detector.

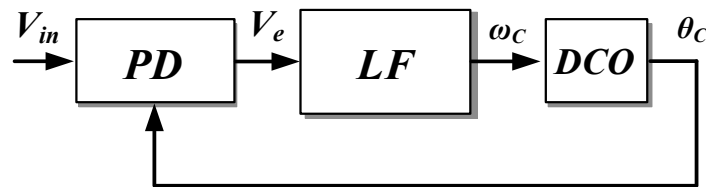


Fig. 4.1: Typical PLL structure

The most commonly used PD types are: zero-crossing detection (ZCD), vector products, and sinusoidal multipliers; all of these methods are limited in their response times, accuracy, and/or application.

The ZCDs work by sensing the zero crossing of the AC voltage and comparing two crossing instances to calculate the time (and thus the frequency) between crossing events. Because of this, ZCD PDs suffer from angle estimation inaccuracies and have slow response times to disturbances due to the inherent half line-cycle delays in the measurements needed for the frequency calculation. The inaccuracies of this method come from the fact that the system can only calculate information about  $\omega$  and  $\theta$  twice per line-cycle, as shown in Fig. 4.2, and cannot determine system information between these times. The LF in this case, is a simple passive low pass filter (LPF). The filter is needed to reject the jitter effects of multiple zero crossings that can occur in a real system due to harmonics, switching ripple, sensor noise, etc.; and is used to smooth the discrete jumps in the estimated frequency by averaging. The system transient response and tracking times are therefore severely increased, and as such the ZCD method is rarely used in systems that require detailed information on the sub-cycle level for control purposes; it is more commonly used as a supplement to other forms of phase detection.

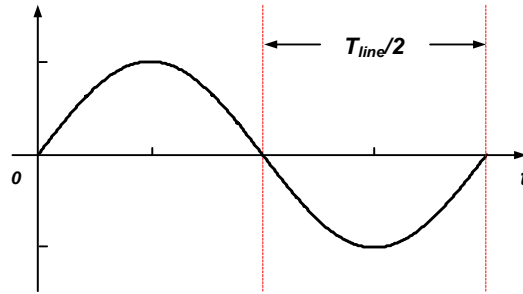


Fig. 4.2: ZCD Time Delay

Vector-product PDs require multiple, independent input variables, which increases the system complexity and the number of sensed parameters that are required; vector-product PDs are common in three-phase ( $3\Phi$ ) systems where multiple, independent voltage variables are easily obtained. This usually comes about in the form of Park's transformation, converting the system from the  $3\Phi$  stationary (ABC) frame to the DQ coordinate frame.

Compared with the three-phase systems, the single-phase PLL poses more challenges, especially in the presence of different grid conditions due to the reduced number of input signals. A profound drawback of the vector-product PLLs in the  $1\Phi$  system is that there is only one signal to synchronize with; an orthogonal signal must therefore be created to transform the system from the stationary frame to the DQ synchronous frame. For this reason, as shown in Fig. 4.3, the orthogonal-signal-generation-method (OGM) is required. Some of the existing measures include: delay filters [199-202], Kalman filter [203], Hilbert transformation (HT) [204], all-pass-filters (APF) [109], second-order generalized integrator (SOGI) [199], inverse Park transformation [201, 205], and other methods, such as p-q theory [206].

In some of these methods, an additional delay is introduced into the PLL loop, lowering the dynamics response [110, 200-202]. Some methods require the selection of internal parameters, which tend to become unstable [200, 201, 203, 205]. Although all OGMs generate an orthogonal signal at the line frequency, they have different dynamics responses throughout the other frequency ranges. These dynamics responses at the harmonic frequencies as well as the digital precision of OGMs have a direct impact on the PLL output performance. In addition, all of the OGMs require additional digital implementation effort and greater computation cost.

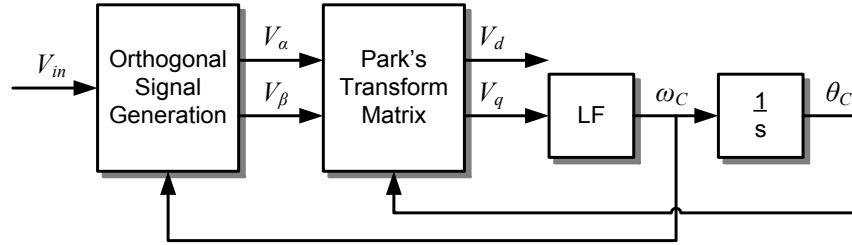


Fig. 4.3: Generic structure of single-phase DQ frame PLL

Sinusoidal multiplier-based PDs, namely the stationary-frame PLLs, are useful due to the lack of multiple line signals for synchronization, as well as their ease of implementation compared with other DQ PLLs in both analog and digital applications. Moreover, the stationary frame PLL presents a simple and distinct loop modeling and design procedure in order to optimize PLL performance. As shown in Fig. 4.4, the typical system (T-PD PLL), commonly known as the mixer system [98, 204], employs the sinusoidal multiplier phase detector (PD), which generates error voltage  $V_e$ , for the loop filter (LF), which in turn generates  $\omega_C$ .

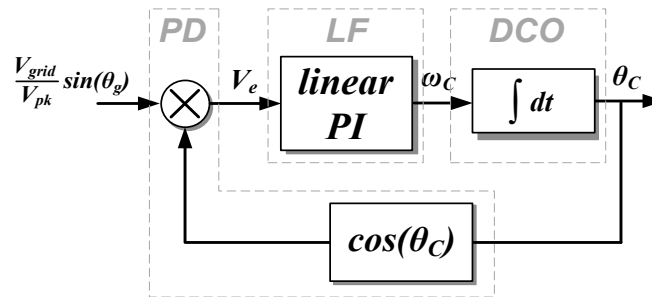


Fig. 4.4: Typical mixer PD type single-phase PLL (T-PD PLL)

One problem with this type of PD is that it inherently creates a  $2\omega$  ripple in  $V_e$  that in turn propagates through the LF and finally appears in  $\omega_C$  [208-210].

Aside from the LF gain at  $2\omega$ , this  $2\omega$  ripple level also changes with the different input line-voltage amplitudes. Fig. 4.5 shows the output frequency in terms of the different input voltages (from 240V rms to 120 V rms at 2.5 sec). The figure shows that the ripple level is proportional to the input voltage amplitude.

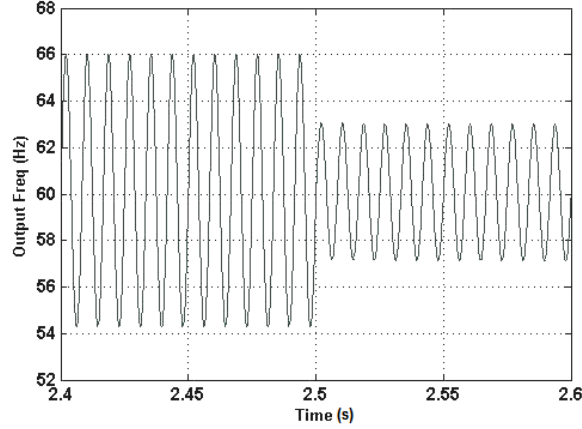


Fig. 4.5: Output of T-PD PLL when input voltage drops from 240 Vrms to 120 Vrms

This fictitious noise is a by-product of the PD's multiplication function, and should be removed prior to the LF. Previous methods to minimize this ripple effect have focused on adding filters, before and/or after the LF, which attenuate the  $2\omega$  ripple [109, 200, 201, 205, 207]. These solutions generally cause the LF bandwidth and/or the phase margin to decrease resulting in slower overall synchronization speeds.

As illustrated in Fig. 4.6, a modified solution, referred to as the M-PD PLL, is proposed in [107] to modify the T-PD PLL.

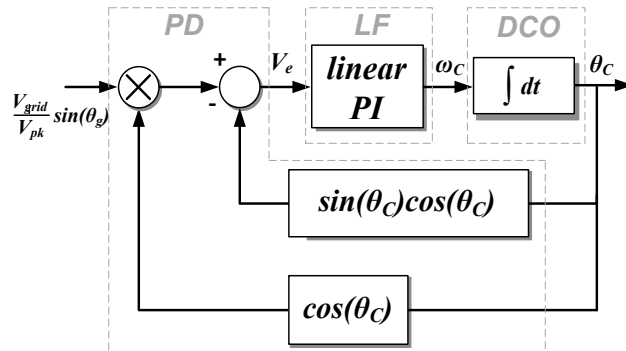


Fig. 4.6: Modified mixer PD type single-phase PLL (M-PD PLL)

This solution simply adds another trigonometric term in the PD to reduce the output steady-state ripple.

$$V_e = \frac{V_{grid}}{2V_{pk}} \sin(\theta_g - \theta_c) + \frac{1}{2} \sin(2\theta_g + \chi) \sqrt{\left(\frac{V_{grid}}{V_{pk}}\right)^2 + 1 - 2\frac{V_{grid}}{V_{pk}} \cos(\theta_g - \theta_c)}, \quad (1)$$

$$\chi = \tan^{-1}\left(\frac{V_{grid} \sin(\theta_g - \theta_c)}{V_{grid} \cos(\theta_g - \theta_c) - V_{pk}}\right)$$

If the pre-set value  $V_{pk}$  equals the input voltage amplitude  $V_{grid}$ , (1) can be simplified as

$$V_e = \frac{1}{2} \sin(\theta_g - \theta_C) + \sin(2\theta_g + \chi) \sin\left(\frac{\theta_g - \theta_C}{2}\right), \chi = \tan^{-1}\left(\frac{\sin(\theta_g - \theta_C)}{\cos(\theta_g - \theta_C) - 1}\right) \quad (2)$$

When the PLL output  $\theta_C$  is in lock with the input phase  $\theta_g$ , the second  $2\omega_C$  term automatically drops to zero and thereby achieves zero steady-state error. However, this PLL is vulnerable to a change of input voltage amplitude and requires the input to be of unity gain ( $V_{grid}/V_{pk} = 1$ ); otherwise the PLL still suffers the ripple issue, as explained by the second term of (1). This issue is more important during a low-voltage or zero-voltage transition [123].

Fig. 4.7 shows the simulation results when the  $2\omega$  ripple occurs as the input voltage amplitude drops by half at 2.5 seconds. As mentioned above, the LF bandwidth can be tuned to be much lower than the line-frequency to reduce this ripple; yet the dynamic responses, such as settling time and overshoot, are sacrificed accordingly.

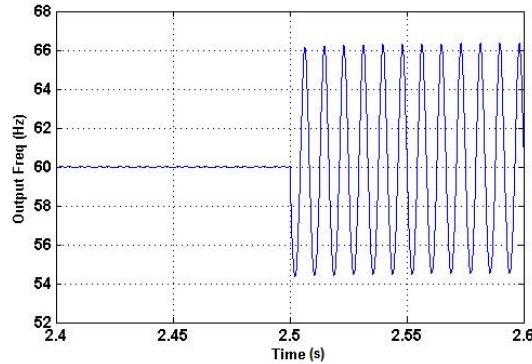


Fig. 4.7: Output of M-PD PLL when input voltage drops from 240 V rms to 120 V rms

#### 4.1.2. PROPOSED PLL SYSTEM AND ANALYSIS

Generally, in a DQ PLL, if an ac signal and its orthogonal counterpart pass through the  $\alpha\beta$ -dq transformation as,

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T \begin{bmatrix} V_e \sin(\theta_g) \\ -V_e \cos(\theta_g) \end{bmatrix} = \begin{bmatrix} \cos(\theta_C) & \sin(\theta_C) \\ -\sin(\theta_C) & \cos(\theta_C) \end{bmatrix} \begin{bmatrix} V_e \sin(\theta_g) \\ -V_e \cos(\theta_g) \end{bmatrix} = \begin{bmatrix} V_e \sin(\theta_g - \theta_C) \\ -V_e \cos(\theta_g - \theta_C) \end{bmatrix} \quad (3)$$

it will be converted to dc components in both the  $d$  and  $q$  channels.  $T$  denotes the  $\alpha\beta$ -dq transformation matrix. The  $d$ -channel is for the PD to regulate. During the steady-state, the  $d$ -channel will be zero, and the  $q$  channel will approach  $-V_e$ , reflecting the input signal

amplitude information. However, if forcing the orthogonal signal zero and applying the  $\alpha\beta$ - $dq$  transformation, the  $d$  and  $q$  channels generate double-line frequency components but still have the dc information to use, which is shown in (4).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T \begin{bmatrix} V_e \sin(\theta_C) \\ 0 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} V_e \sin(\theta_g - \theta_C) \\ -V_e \cos(\theta_g - \theta_C) \end{bmatrix} + \frac{1}{2} \begin{bmatrix} V_e \sin(\theta_g + \theta_C) \\ V_e \cos(\theta_g + \theta_C) \end{bmatrix} \quad (4)$$

Fig. 4.8 shows the proposed 1 $\Phi$  PLL system. The  $\alpha\beta$ - $dq$  transformation is applied to convert the error signal  $V_a$  to the  $d$  and  $q$  channels. The  $d$  channel signal  $V_d$ , which is the output of the PD, is used to generate the estimated phase angle  $\theta_C$ , thus forming the stationary-frame PLL feedback loop; the  $q$  channel signal propagates through a compensator  $H_v$  and then yields the voltage amplitude of the input signal  $V_{pk}$ . Afterwards, both feedback loops multiply together ( $V_{pk}\sin(\theta_C)$ ) and return back to physically close the loop.

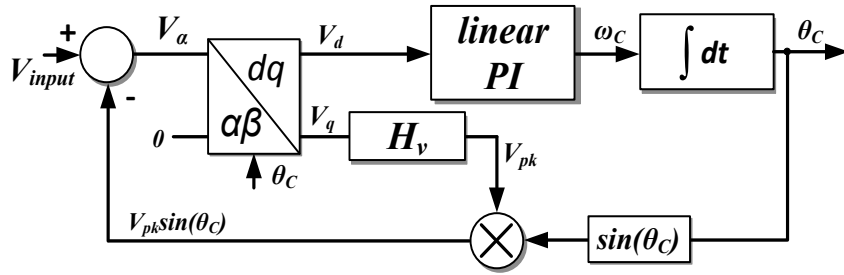


Fig. 4.8: Proposed single-phase PLL with peak voltage detection

The input signal is defined as

$$V_{input} = V_{grid} \sin(\theta_g) \quad (5)$$

Without the implementation effort of any OGMS, the  $\alpha\beta$ - $dq$  transformation is applied to generate the  $d$  and  $q$  channel signals by simply forcing the orthogonal input signal to zero. Thus, the  $d$  and  $q$  channels are comprised of two components, the dc and the double-line frequency components, which can be written as:

$$\begin{cases} V_d = \frac{1}{2} V_{grid} \sin(\theta_g - \theta_C) + \frac{1}{2} V_{grid} \sin(\theta_g + \theta_C) - \frac{1}{2} V_{pk} \sin(2\theta_C) \\ V_q = -\frac{1}{2} V_{grid} \cos(\theta_g - \theta_C) + \frac{1}{2} V_{pk} + \frac{1}{2} V_{grid} \cos(\theta_g + \theta_C) - \frac{1}{2} V_{pk} \cos(2\theta_C) \end{cases} \quad (6)$$

However, as shown in (6), the PD gain in the proposed PLL is proportional to the input voltage amplitude  $V_{grid}$  which is much higher than unity, thereby having a large

impact on the LF parameter design. Therefore, an improved PLL is shown in Fig. 4.9, in which the PD gain has been normalized by a factor  $V_N$ .

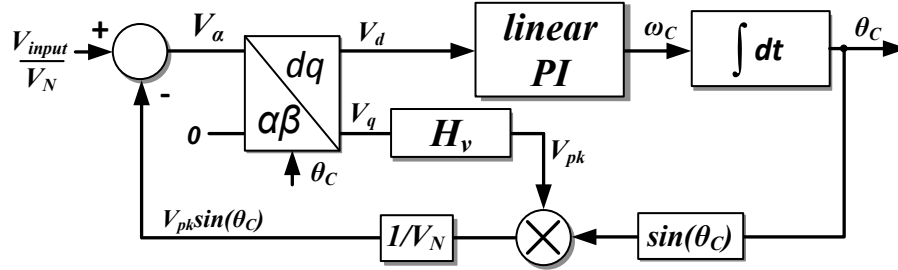


Fig. 4.9: Normalization of the proposed single-phase PLL

According to (6) and Fig. 4.9, the  $d$  and  $q$  channel signals can be rewritten as:

$$V_d = \frac{V_{grid}}{2V_N} \sin(\theta_g - \theta_C) + \frac{V_{pk}}{2V_N} \sin(2\theta_g + \chi) \sqrt{\left(\frac{V_{grid}}{V_{pk}}\right)^2 + 1} - 2 \frac{V_{grid}}{V_{pk}} \cos(\theta_g - \theta_C), \quad (7)$$

$$\chi = \tan^{-1} \left( \frac{V_{grid} \sin(\theta_g - \theta_C)}{V_{grid} \cos(\theta_g - \theta_C) - V_{pk}} \right)$$

$$V_q = \left[ \frac{V_{pk}}{2V_N} - \frac{V_{grid}}{2V_N} \cos(\theta_g - \theta_C) \right] + \frac{V_{pk}}{2V_N} \cos(2\theta_g + \chi) \sqrt{\left(\frac{V_{grid}}{V_{pk}}\right)^2 + 1} - 2 \frac{V_{grid}}{V_{pk}} \cos(\theta_g - \theta_C), \quad (8)$$

$$\chi = \tan^{-1} \left( \frac{V_{grid} \sin(\theta_g - \theta_C)}{V_{grid} \cos(\theta_g - \theta_C) - V_{pk}} \right)$$

As shown in (8), when the estimated phase angle  $\theta_C$  approaches the input phase  $\theta_g$ , the dc error in the  $q$  channel is

$$V_{q\_dc} = -\frac{1}{2V_N} (V_{grid} - V_{pk}) \quad (9)$$

Therefore, a compensator can force this dc error (the first term in (9)) to approach zero, which makes the estimated peak voltage  $V_{pk}$  equal the input voltage amplitude  $V_{grid}$ . The second term in the  $q$  channel in turn also goes to zero. Thus, the  $q$  channel simply becomes a peak voltage detection feedback loop. The compensator can be tuned to make the bandwidth of the  $q$ -channel loop up to 10 times higher than the line frequency to improve the peak voltage detection speed. When the  $V_{pk}$  equals  $V_{grid}$ , the  $d$  channel output signal  $\omega_C$  will have a zero steady-state error as the second term in (7) is eliminated. Although the lack of orthogonal signal leaves both channel signals with double-line frequency components. Both feedback and input ac signals propagate through the same



$\alpha\beta$ - $dq$  transformation, and both double-line frequency components in each channel are canceled under the steady-state.

The small-signal approximation can be applied to the dc signal in (7) to obtain the PD gain, which is expressed as:

$$\begin{aligned}\tilde{v}_d &= \frac{V_{grid}}{2V_N} \sin(\tilde{\theta}) \approx \frac{V_{grid}}{2V_N} \tilde{\theta} \\ \Rightarrow K_{PD} &= \frac{\tilde{v}_d}{\tilde{\theta}} = \frac{V_{grid}}{2V_N}\end{aligned}\quad (10)$$

The simulation results in Fig. 4.10 give the frequency output (60 Hz) of the proposed PLL with a 50% input voltage amplitude drop at 5 seconds. When the input amplitude changes, the proposed PLL maintains consistent output by achieving almost 90% ripple reduction. The overshoot and settling time of the proposed PLL is so small that it greatly benefits the grid-interfaced converter's power factor control.

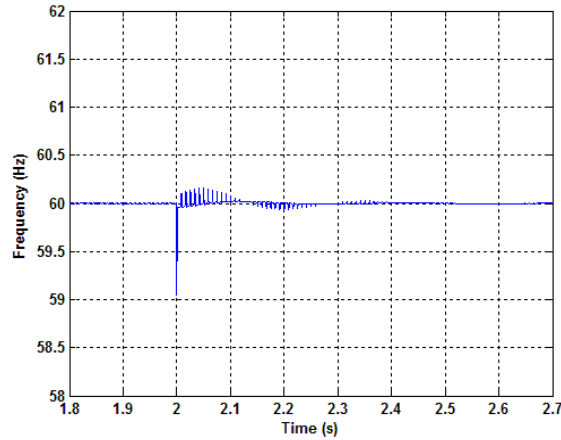


Fig. 4.10: Output of proposed PLL when input voltage drops from 240 Vrms to 120 Vrms

#### 4.1.3. PLL MODELING AND DESIGN

One of the advantages of the stationary-frame PLL is its clear modeling procedure for engineers to design PLLs for different applications. Under the phase-lock condition, the stationary frame PLL can be simply modeled as a classic SISO state-feedback control system [209, 210]. Fig. 4.11 and Fig. 4.12 show the model for estimated phase  $\theta_C$  and frequency  $\omega_C$ .

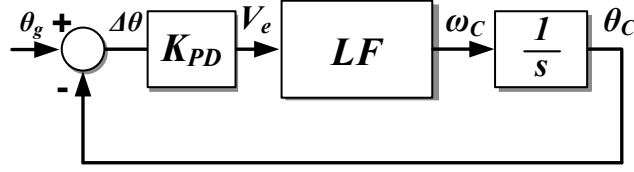


Fig. 4.11: Phase feedback model for PLL system

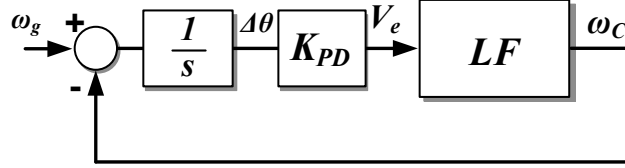


Fig. 4.12: Frequency feedback model for PLL system

In Fig. 4.11 and Fig. 4.12,  $K_{PD}$  is the gain of phase detector expressed in (10). The form of the LF is shown in (11); and the open-loop gain and closed-loop transfer function of the PLL are shown in (12) and (13), respectively.

$$LF(s) = k_p + k_i \cdot \frac{1}{s} \quad (11)$$

$$G(s) = K_{PD} \cdot LF(s) \cdot \frac{1}{s} \quad (12)$$

$$F_{close}(s) = \frac{G(s)}{1 + G(s)} \quad (13)$$

If the LF is a simple PI type filter in (11), the closed-loop response  $F_{close}(s)$  in (13) is a second-order linear type system. Substituting (12) into (13) gives,

$$F_{close}(s) = \frac{\omega_n^2 \left( 1 + \frac{s}{\omega_{zero}} \right)}{s^2 + 2\xi\omega_n s + \omega_n^2}, \quad (14)$$

$$\omega_{zero} = \frac{k_i}{k_p}, \omega_n = \sqrt{\frac{V_{grid} k_i}{2V_N}}, \xi = \frac{k_p}{2} \sqrt{\frac{V_{grid}}{2k_i V_N}}$$

where  $\zeta$  is the damping factor that affects the dynamics response. The design of the PLL LF parameters can be based on (14) to balance to the trade-off between the overshoot and the settling time in terms of the application requirements. For example,  $\zeta$  can be set as the under-damp state to optimize the trade-off between the overshoot and the settling time. The zero  $\omega_{zero}$  is placed around  $2\pi 6$  rad/s to attain a desired phase-margin around the line frequency.

For the peak voltage detection loop design, an equivalent state feedback loop is obtained under phase-lock condition as shown in Fig. 4.13.

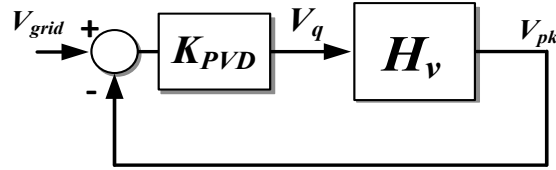


Fig. 4.13: State-feedback model for peak voltage detection loop

$K_{PVD}$  is the gain of the peak voltage detection block, and is defined as:

$$K_{PVD} = -\frac{1}{2V_N} \quad (15)$$

The second-order compensator  $H_v$  in (16) can be designed using (16).

$$H_v = -k_v \frac{s+p}{s(s+z)} \quad (16)$$

The design of the pole and zero in  $H_v$  can be based on the Bode plot of the compensated open-loop gain in (17).

$$P(s) = K_{PVD} \cdot H_v \quad (17)$$

As shown in Fig. 4.14, the zero location can be placed before the cross-over frequency for the desired phase margin; a pole can be placed after the crossover frequency to attenuate the high-frequency noise. The compensator gain  $k_v$  can be tuned to change the loop bandwidth, which is around 1 kHz in Fig. 4.14. A high control bandwidth yields a fast voltage regulation speed as well as input harmonic rejection, which is discussed in the following section.

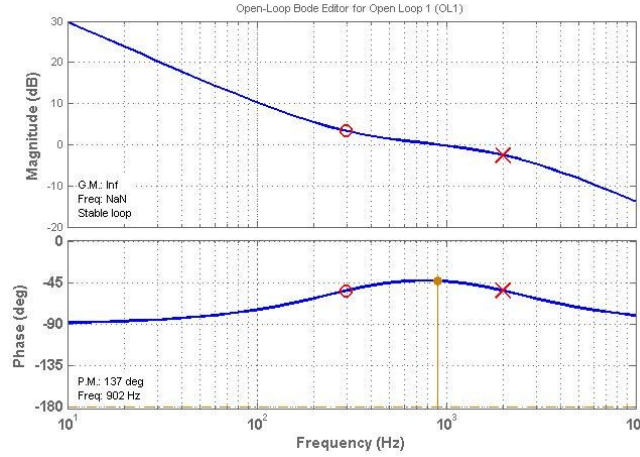


Fig. 4.14: Bode-plot of compensated voltage loop open-loop gain

Since the two-loops are formed together, their dynamics will be coupled together. During the phase tracking period, there is a feedforward gain right after the input  $V_{grid}$  as shown in (18),

$$F_g = \cos(\psi) \quad (18)$$

where  $\psi$  is the phase difference between input  $\theta_g$  and output  $\theta_C$ . If a phase jump occurs, the fast peak-voltage detection loop will behave according to (18) during the transient period until the PLL tracking loop returns to steady-state, i.e., until  $\psi$  goes back to zero.

One set of the PLL parameters, based on Fig. 4.9, is shown in Table 4.1, which shows the values used to simulate the PLL output in comparison with the PLL model.

Table 4.1: PLL parameters

Parameter	$k_p$	$k_i$	$V_N$	$k_v$	$z$	$p$
Value	49	$12\pi \times 49$	$240\sqrt{2}$	$8 \times 10^6$	$1.8 \times 10^3$	$1.25 \times 10^4$

The PLL behavior under the frequency change and phase change are the step response and impulse response of the frequency feedback second-order system, respectively. Fig. 4.15 shows the frequency step-response from 60 to 61 Hz of the proposed PLL along with the closed-loop model based on Fig. 4.12. The one radius phase jump response of the proposed PLL as well as the result from the impulse response of the closed-loop model is also shown in Fig. 4.16. The  $2\omega$  frequency ripple would appear during this transient period because of the non-zero second-term in (7).

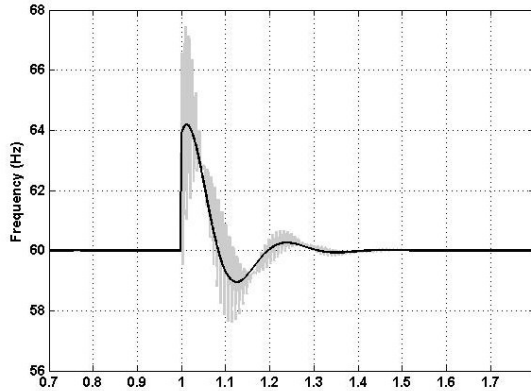


Fig. 4.15: One rad phase jump response of the proposed PLL (grey) and the mathematics model (black)

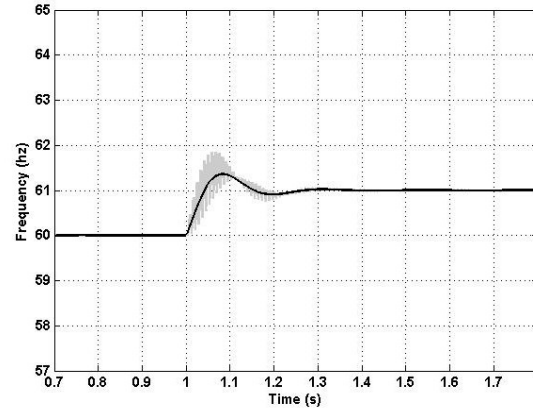


Fig. 4.16: 1 Hz step response of the proposed PLL (grey) and the mathematics model (black)

The line voltage step from 240 V rms to 120 V rms is shown in Fig. 4.17 along with the closed-loop model (Fig. 4.13). In order to explicitly show the transient period, the  $k_v$  in this simulation is chosen to be one tenth of the value in Table I to slow down the peak-voltage detection loop. The  $2\omega$  frequency ripple also appears during this transient period because of the non-zero second-term in (8). It is seen that both the PLL phase tracking loop and the peak-voltage detection loop can be modeled as linear second-order systems, which can be designed according to different application requirements.

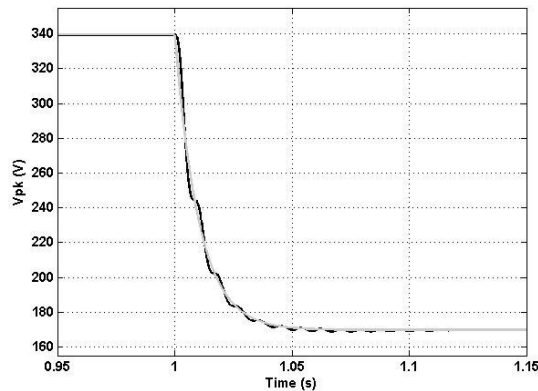


Fig. 4.17: 240 V rms to 120 V rms step response of the peak voltage detection loop (black) and the closed-loop model (grey)

#### 4.1.4. DC-OFFSET AND INPUT HARMONICS NOISE REJECTION

In addition to the  $2\omega$  frequency ripple generated by the PD and the change in the input voltage amplitude, there are another three major contributors to the PLL output noise: dc-offset, input low-frequency harmonics, and input high-frequency noise.

#### 4.1.4.1. Analysis of the Dc-offset

When considering the input dc-offset  $V_{off}$  that occurs due to a measurement or digital quantization/rounding error in (19),

$$V_{input} = V_{grid} \sin(\theta_g) + V_{off} \quad (19)$$

the  $d$  and  $q$  channels will have additional line-frequency ripple information in (20), which appears in the output through the LF, yielding a steady-state error.

$$\begin{cases} V_d = \frac{1}{2} \frac{V_{grid}}{V_N} \sin(\theta_g - \theta_C) + \frac{1}{2} \frac{V_{grid}}{V_N} \sin(\theta_g + \theta_C) - \frac{1}{2} \frac{V_{pk}}{V_N} \sin(2\theta_C) + \frac{V_{off}}{V_N} \cos(\theta_C) \\ V_q = -\frac{1}{2} \frac{V_{grid}}{V_N} \cos(\theta_g - \theta_C) + \frac{1}{2} \frac{V_{pk}}{V_N} + \frac{1}{2} \frac{V_{grid}}{V_N} \cos(\theta_g + \theta_C) - \frac{1}{2} \frac{V_{pk}}{V_N} \cos(2\theta_C) - \frac{V_{off}}{V_N} \sin(\theta_C) \end{cases} \quad (20)$$

A simple improvement for the proposed PLL is shown in Fig. 4.18. A high-order low-pass-filter (LPF) with a bandwidth much lower than the line frequency, e.g., a fifth-order type I Chebyshev filter, is used to get rid of the dc offset in error signal  $V_a$ . Fig. 4.19 shows the simulation results with and without this dc offset rejection with a 1% dc offset at 240 V rms ac voltage. The figure demonstrates how this simple dc offset rejection intensively reduces the output line-frequency ripple.

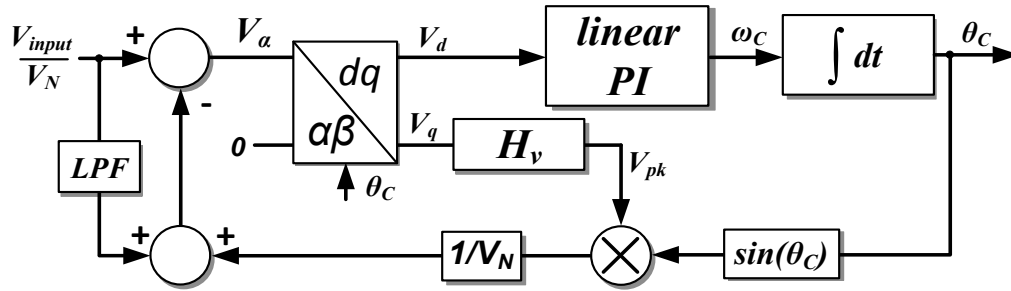


Fig. 4.18: Proposed PLL with dc-offset rejection

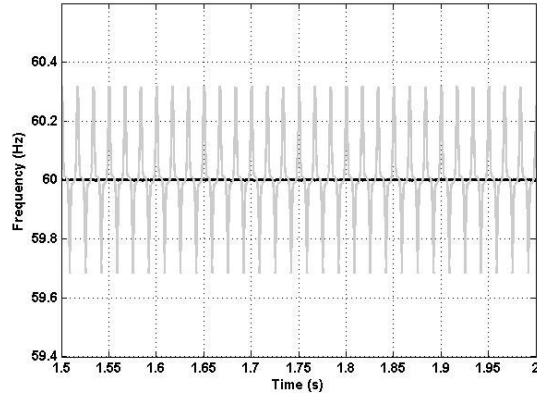


Fig. 4.19: PLL comparison between proposed PLL with (black), and without (grey) dc-offset rejection with 1% dc-offset

#### 4.1.4.2. Analysis of Harmonics Rejection

The high-frequency input harmonics and measurement noise normally can be directly attenuated by analog and/or digital filters in the sensor loop and by LF if the frequency is much higher than the PLL loop bandwidth. However, the attenuation of the low-order input harmonics is a big concern for designing the PLL in a 1 $\Phi$  converter system. Since the proposed PLL includes the  $\alpha\beta/dq$  transformation, the linear frequency response analysis cannot be directly used to evaluate the harmonics attenuation; however, the harmonics attenuation analysis under steady-state can be given. If we consider a  $h$ -order harmonics noise in the input signal, as shown in (21),

$$V_{input} = V_{grid} \sin(\theta_g) + V_h \sin(h\theta_g) \quad (21)$$

the  $q$ -channel signal will be defined in (22).

$$V_q = -\frac{\sin(\theta_C)}{V_N} [V_{grid} \sin(\theta_g) + V_h \sin(h\theta_g) - V_{pk} \sin(\theta_C)] \quad (22)$$

At the steady-state,  $\theta_C = \theta_g$ , and if the harmonics frequency is lower than the control bandwidth of the  $q$ -channel, the  $q$ -channel signal  $V_q$  will approach zero. The generated peak voltage in turn will be in (23).

$$V_{pk} = \begin{cases} V_{grid} + V_h \frac{\sin(h\theta_g)}{\sin(\theta_g)}, & \theta_g \notin n\pi, n \in N \\ V_{grid} + hV_h, & \theta_g \in n\pi, n \in N \end{cases} \quad (23)$$

Equation (23) shows that the low-order harmonics will appear during the peak voltage. Due to the regulation action in the  $q$ -channel, the harmonics component in  $V_{pk}$  will be fed

back, which eliminates the input low-order harmonics component in  $V_a$ , thus significantly reducing the harmonics noise in the output of the PLL without the need to reduce the LF bandwidth or implement any complex filter in the LF.

The 5% (12 V rms) third harmonics (180 Hz) noise, which is normally seen in single-phase grid, is injected into a 240 V rms ac voltage as the input signal for the PLL to synchronize with. Fig. 4.20 shows the outputs of the M-PD PLL and of the proposed PLL to evaluate the noise rejection performance, under the same LF parameters. It is clearly seen that, since the  $q$ -channel bandwidth is designed around 1 kHz, which is much higher than the harmonics frequency, the proposed PLL achieves better input harmonics rejection, providing a better estimated frequency and phase. In Fig. 4.21, due to the third harmonics input signal, the ripple component is superimposed on the dc peak-voltage signal.

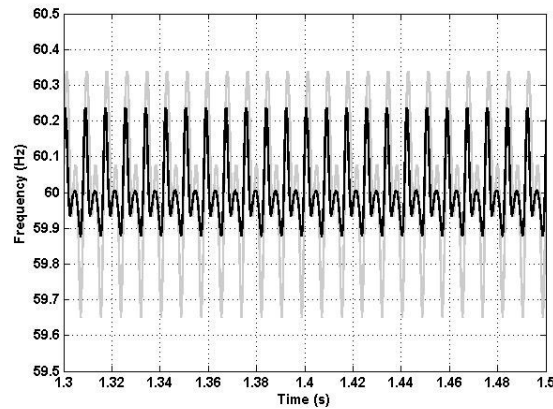


Fig. 4.20: Output of M-PD PLL (grey) and P-PD PLL (black) under the 5% third harmonics injection.

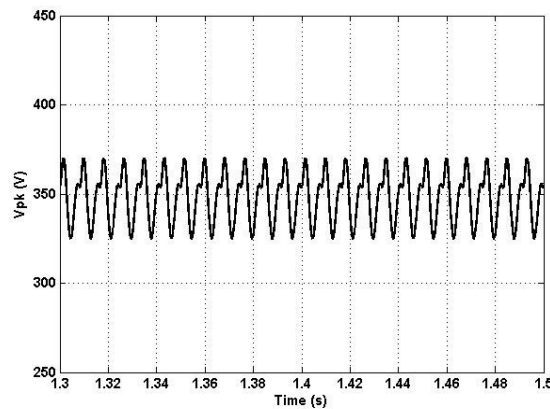


Fig. 4.21: P-PD PLL peak voltage  $V_{pk}$  with the 5% third harmonics injection



#### 4.1.5. EXPERIMENTAL EVALUATION

As shown in Fig. 4.22, the verification is carried on a 1 $\Phi$  ac-dc grid-interface PWM full-bridge converter system with a DSP-FPGA control platform. The implemented PLLs for comparison are shown in Fig. 4.4, Fig. 4.6, and Fig. 4.18. The above simulation results and the following experimental evaluations are conducted based on this system setup. The system parameters can be found in Table 4.2, where  $f_s$  and  $f_o$  are the switching frequency and line-frequency, respectively.

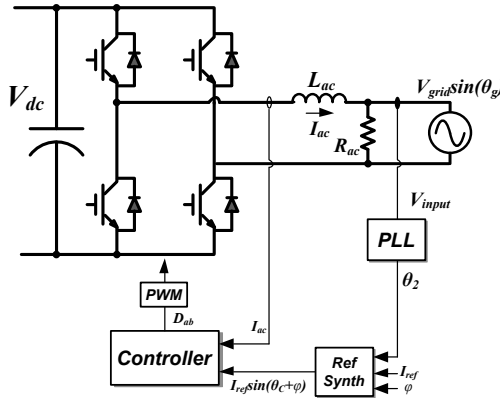


Fig. 4.22: Full-bridge converter with ac current control and PLL

Table 4.2: System parameters

Parameter	Value
$V_{grid}$	$240\sqrt{2}$
$f_o$	60 Hz
$f_s$	20 kHz
$L_{ac}$	400 $\mu$ H
$V_{dc}$	550 V
$S_{rate}$	10 kVA
$R_{ac}$	10 $\Omega$

The input ac voltage with 5% THD is generated by an HP6843A ac voltage source. The PLL output signal is from the D/A converter on the digital controller. The results are the transient responses when the input ac voltage has a magnitude jump from 240 V rms to 120V rms (50%). Fig. 4.23 shows the proposed PLL frequency output  $\omega_C$  and peak voltage output  $V_{pk}$ . It can be explicitly seen that the peak voltage detection loop fast tracks the input amplitude  $V_{grid}$ , and thus leads to a negligible transient response at the PLL output  $\omega_C$ .

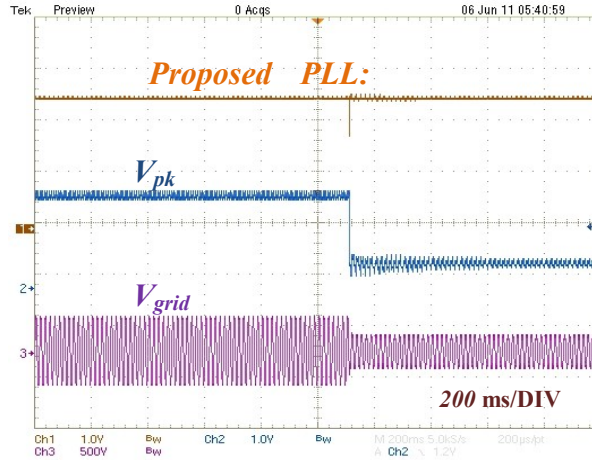


Fig. 4.23: Proposed PLL frequency output  $\omega_C$  [3Hz/DIV] and peak voltage output  $V_{pk}$  [150V/DIV] with 50% input voltage  $V_{grid}$  sag [500V/DIV]

Fig. 4.24 and Fig. 4.25 show the proposed PLL in comparison with M-PD PLL and T-PD PLL, respectively. These figures clearly show that the proposed PLL presents an output that is identical with the other PLLs, with much less ripple under the different input conditions. This set of comparisons matches with the simulation results and shows the PLL output noise reduction that the proposed PLL readily makes.

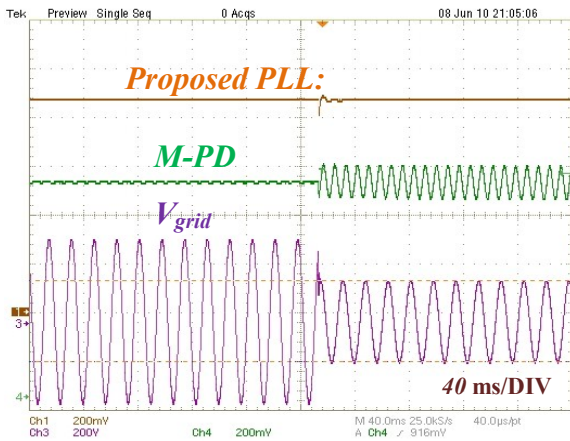


Fig. 4.24: Proposed PLL and M-PD PLL frequency output  $\omega_C$  with 50% input voltage  $V_{grid}$  sag [200V/DIV]

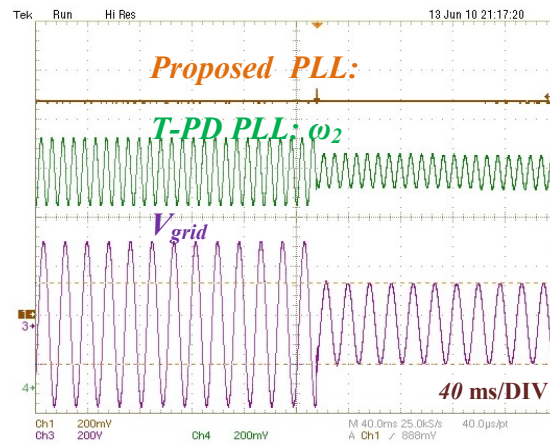


Fig. 4.25: Proposed PLL and T-PD PLL frequency output  $\omega_C$  with 50% input voltage  $V_{grid}$  sag [200V/DIV]

Fig. 4.26 and Fig. 4.27 show the transient response of the proposed PLL when the input frequency steps from 60 up to 61 Hz and the input phase jump with one radius, respectively, indicating the fast transient period as predicted by the analysis and the models.

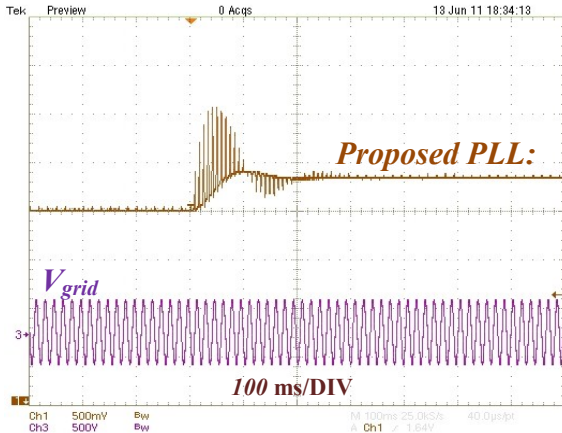


Fig. 4.26: 1 Hz step response of the proposed PLL output frequency  $\omega_C$  [1.5Hz/DIV] and the input voltage  $V_{grid}$  [500V/DIV]

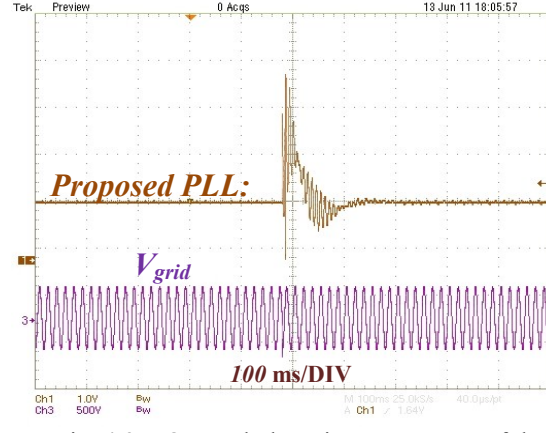


Fig. 4.27: One rad phase jump response of the proposed PLL output frequency  $\omega_C$  [3Hz/DIV] and the input voltage  $V_{grid}$  [500V/DIV]

The input harmonics rejection performances of the PLLs are compared using the same LF parameters. A 70% clipped sinusoid, 25% THD rich input signal was used, which is common in motor systems that produce trapezoidal back EMF. As shown in Fig. 4.28, the M-PD PLL (0.6 Hz ripple) shows a considerable improvement over the T-PD PLL (2 Hz ripple) via a ~50% reduction in the noise ripple generated. Fig. 4.29 shows a further output harmonics reduction (> 50%) is achieved by the proposed PLL (0.1 Hz ripple).

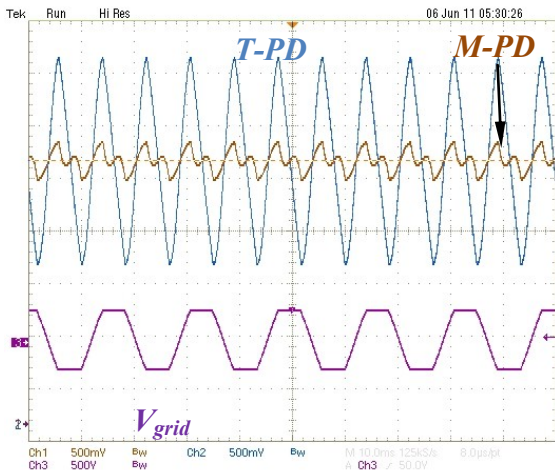


Fig. 4.28: Output ripple of T-PD PLL [1.5Hz/DIV] and M-PD PLL [1.5Hz/DIV] under 70% clipped sinusoid input  $V_{grid}$  [500V/DIV]

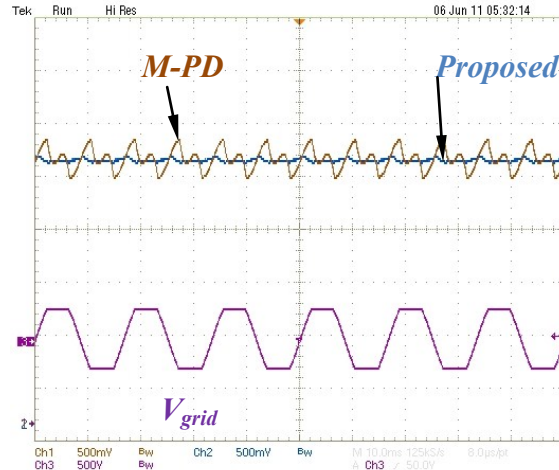


Fig. 4.29: Output ripple of M-PD PLL [1.5Hz/DIV] and the proposed PLL [1.5Hz/DIV] under 70% clipped sinusoid input  $V_{grid}$  [500V/DIV]

#### 4.1.6. CONCLUSION

The proposed feedback mechanism for stationary-frame single-phase PLL doesn't require any OGMs, thus reducing the digital implementation effort, and the PLL phase tracking and peak voltage detection models are clearly discussed. Three stationary-frame PLLs are compared both in simulation and experimental evaluation. Besides the ideal output, the fast peak voltage detection can be utilized to diagnose ac grid voltage faults, such as voltage sag and voltage flicker. The proposed PLL can be used in most  $1\Phi$  grid-interface converter systems, especially in weak-grid applications.

## **4.2. GRID SYNCHRONIZATION BEHAVIOR AND ITS STABILITY**

### **4.2.1. INTRODUCTION**

Because of the naturally different mechanisms, the characteristics of power electronics-based bus-interface converters e.g., PV and wind converters, are very different from rotating synchronization generators, resulting in different impacts on the grid static and dynamics operations. With the continuous growth of distributed generation resources, the behavior of the bus-interface converter and its potential impact on electric power system cannot be simply ignored. Utility operators have thus issued many of grid-codes for DG units to reduce the regulation difficulties for the grid. As mentioned above, one of the basic aspects to ensuring safe and reliable operation of a bus-interface converter is grid synchronization control. Thus, it is important to understand the frequency synchronization behaviors of a converter system under different operation conditions. This is especially critical when the penetration level of DG units are significantly increased, as is projected for the near future, as well as when the regional power distribution systems operate in an islanded mode.

The issue of converter grid-synchronization stability has been noticed by industry. General Electric [114, 115, 211] reported that the converter system may be destabilized under very weak grid conditions, especially when some so-called "positive-feedback techniques" are used in the control system. Reference [212-214] presents converter frequency stability under islanded conditions in an electric power system. However, none of the existing literature has ever fully studied frequency synchronization behaviors, but only present some "interesting results".

Additionally, many publications [211, 215, 216] use the so-called “positive feedback” or various non-linear control solutions in a control system to destabilize or perturb the converter synchronization loop to detect grid faults or islanding conditions, which is a very dangerous practices if the researcher is not aware of the side-effects.

There are several publications that propose many sophisticated PLL techniques and design procedures in pursuit of high-end performance, but most of them ignore the strong effect of PLLs on grid-interface operations.

Moreover, a so-called “zero net energy” concept has become popular recently, and its essential scenario is that the continuous growing energy requirement e.g., more loads, can be fully supplied by interfacing the local DG units, such as PV inverters, without upgrading the distribution power feeder as no more power is flowing between the local consumers and the remote distribution transformer. One of the unacknowledged problems with this concept is the grid synchronization behavior.

Therefore, a comprehensive understanding of the grid synchronization behavior of bus-interface converters (ECC converters) is strongly desired to address all of the above issues and questions.

In fact, the bus-interface converter grid synchronization behavior is closely related to the performance of the PLL. In order to generalize the results, a typical three-phase utility-interface converter system with a simplified current control system and PLL is used for this study, as shown in Fig. 4.30. Balanced loads are assumed here.

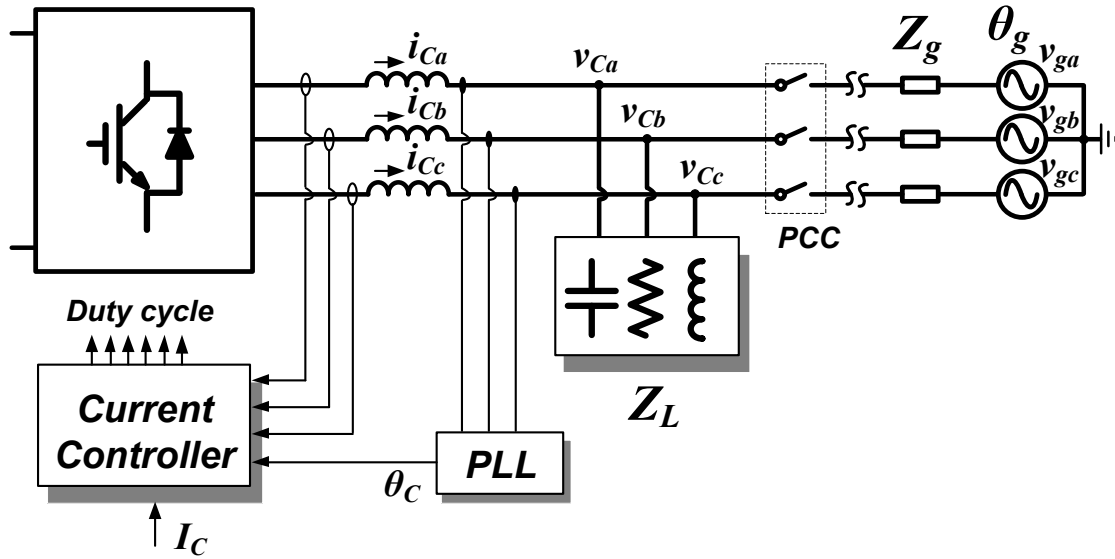


Fig. 4.30: Three-phase grid-interface converter system with PLL

As discussed above, the PLLs vary from each other because of the implementation of the phase detector. Most of the digital PLL PDs are based on trigonometric functions to obtain phase-error information, and only the PD gains vary with the different implementations. Hence, it is possible to use a simple and well-accepted PLL to study the synchronization behavior. For three-phase applications, many sophisticated PLLs are designed for the purpose of extracting the positive sequence component from the distorted voltages. Therefore, this study assumes a positive sequence extractor, as shown in Fig. 4.31, is implemented to obtain only the positive sequence component for the PLL to synchronize with.

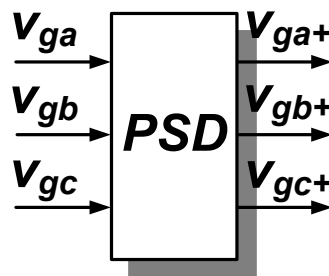


Fig. 4.31: Positive sequence detection (PSD) block

## 4.2.2. MODELING OF GRID SYNCHRONIZATION IN GENERAL CONDITIONS

### 4.2.2.1. Synchronous Reference Frame (SRF) PLL

A synchronous reference frame (SRF) PLL [102, 103], as illustrated in Fig. 4.32, is widely used in three-phase switching power converters to estimate the utility frequency and phase. A typical linear PLL model [102, 103, 207] is shown in Fig. 4.33.

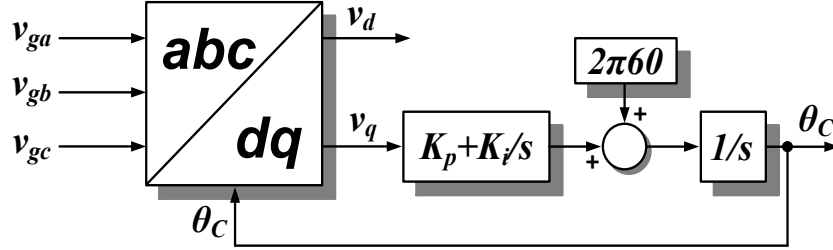


Fig. 4.32: Synchronous reference frame PLL

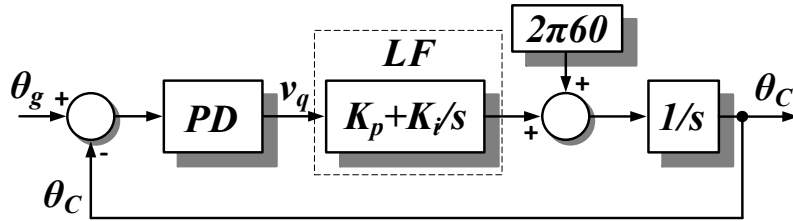


Fig. 4.33: Linearized PLL model

The SRF PLL uses the  $abc/dq$  transformation in (24) as the phase-detector (PD) to convert the measured utility phase voltages in (25) to the  $q$  channel signal.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_c) & \cos\left(\theta_c - \frac{2}{3}\pi\right) & \cos\left(\theta_c + \frac{2}{3}\pi\right) \\ -\sin(\theta_c) & -\sin\left(\theta_c - \frac{2}{3}\pi\right) & -\sin\left(\theta_c + \frac{2}{3}\pi\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (24)$$

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = \begin{bmatrix} V_m \sin(\theta_g) \\ V_m \sin\left(\theta_g - \frac{2}{3}\pi\right) \\ V_m \sin\left(\theta_g + \frac{2}{3}\pi\right) \end{bmatrix} \quad \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = \begin{bmatrix} V_m \sin(\theta_g) \\ V_m \sin\left(\theta_g - \frac{2}{3}\pi\right) \\ V_m \sin\left(\theta_g + \frac{2}{3}\pi\right) \end{bmatrix} \quad (25)$$

Thus,  $q$ -channel signal  $v_q$  is the phase-error signal, which is the output of the PD. The PD gain can be derived using (26).

$$PD = \frac{\tilde{v}_q}{\tilde{\theta}} = V_m \quad (26)$$

#### 4.2.2.2. Quasi-stationary PLL Modeling

Plainly stated, the current-loop bandwidth in PWM grid-interface converter systems is much higher than the line-frequency (60Hz), leading to accurate line-frequency current regulation. Therefore, the converter system can be simply modeled as a current source that precisely follows the current reference in (27).

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} I_C \sin(\theta_C) \\ I_C \sin\left(\theta_C - \frac{2}{3}\pi\right) \\ I_C \sin\left(\theta_C + \frac{2}{3}\pi\right) \end{bmatrix} \quad (27)$$

The three-phase grid-interface converter system can be simplified and represented using a one-line circuit as depicted in Fig. 4.34, where the bus-interface converter and the utility-grid are modeled as a current source and a voltage source, respectively.  $Z_g$  is the equivalent grid input-impedance;  $Z_L$  is the local load of the converter system. Notice that Fig. 4.34 is obtained under the assumption of a balanced condition or a three-phase four-wire configuration.

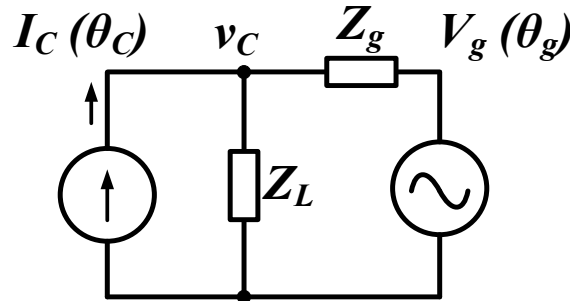


Fig. 4.34: One-line circuit of the converter system

The injected current flows into the system network, generating corresponding voltage response  $v_c$  at the terminal of the converter. Based on the separation principle, the impact of two independent sources on the system can be explored in Fig. 4.35 and Fig. 4.36 separately. The voltage measured by the PLL would be the combination of two voltage responses  $v_{c1}$ , and  $v_{c2}$ , which are contributed by the two sources individually, as shown in Fig. 4.37.



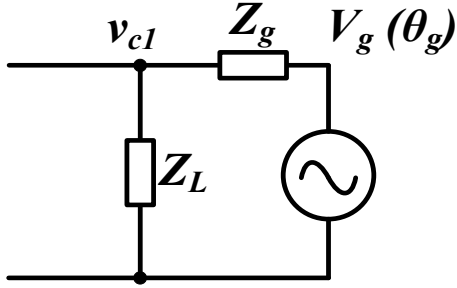


Fig. 4.35: System when only grid is considered

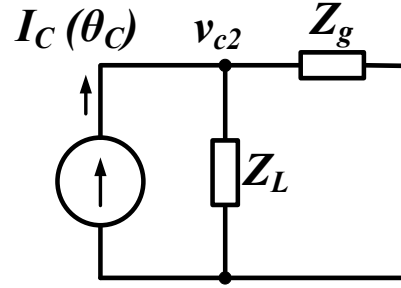


Fig. 4.36: System when only converter is considered

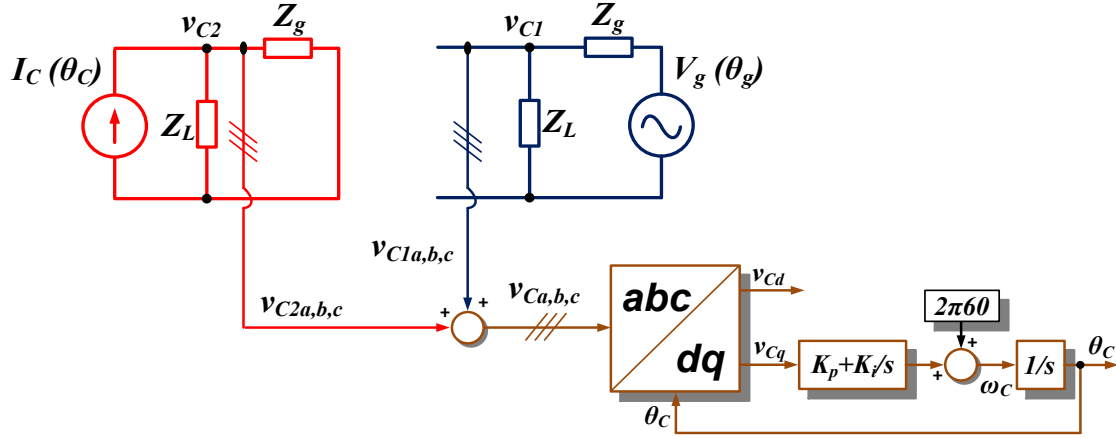


Fig. 4.37: System when effects of the grid and converter are considered

The voltage  $v_{C1}$  is the injection current flowing into the parallel impedance of  $Z_L$  and  $Z_g$ , and the voltage  $v_{C2}$  is the voltage due to the grid input voltage applied to the voltage divider formed by  $Z_L$  and  $Z_g$ . Thus, the terminal voltage  $v_C$  is shown in (28).

$$\begin{aligned} \vec{v}_C &= \frac{Z_L}{Z_L + Z_g} \cdot \vec{v}_g + \frac{Z_L Z_g}{Z_L + Z_g} \cdot \vec{i}_C \\ &= \left| \frac{Z_L}{Z_L + Z_g} \right| V_g e^{j(\theta_g + \varphi_1)} + \left| \frac{Z_L Z_g}{Z_L + Z_g} \right| I_C e^{j(\theta_C + \varphi_2)}, \end{aligned} \quad (28)$$

$$\varphi_1 = \text{phase} \left( \frac{Z_L}{Z_L + Z_g} \right), \varphi_2 = \text{phase} \left( \frac{Z_L Z_g}{Z_L + Z_g} \right)$$

where  $\varphi_1$  and  $\varphi_2$  are the phase-shift angles that occur at the line frequency due to the presence of the reactive components in  $Z_g$  and  $Z_L$ . The voltage response to the switching-frequency current ripple is ignored in (28) due to its small amplitude compared to the line frequency component. It should be noted that the PD in a PLL only tracks the line frequency's large-signal, while all the other harmonics, such as the switching-frequency harmonics, propagate through the PD and LF and appear in the output as ripple noise. It

is seen from (28) that two frequency components are measured for PLL to synchronize with:  $\theta_g$  from the utility and  $\theta_C$  from the self-injected current.

The modeling in equation (28) uses the dynamic phasor representation, which is accurate only for the steady-state (line-frequency) and slow dynamic behavior at frequencies lower than the line frequency. However this modeling process is sufficient enough, as the bandwidth of the PLL in a power system is much lower than the line-frequency, and the high-frequency non-linearity of the PLL is attenuated by the PLL LF.

Therefore, Fig. 4.38 shows the PLL structure when taking into account the converter interaction with the grid. Each phase voltage  $v_c$  is decoupled as  $v_{c1}$  and  $v_{c2}$ . The  $K_1$  and  $K_2$  in Fig. 4.38 are shown in (29).

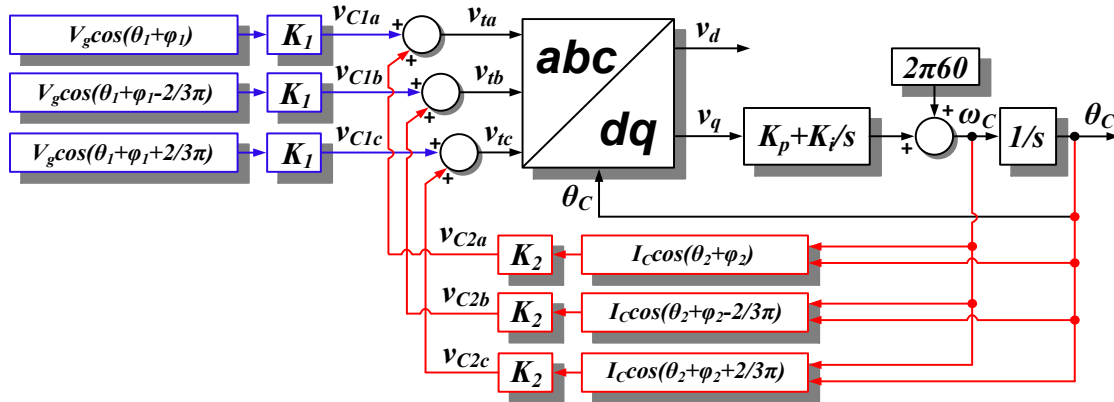


Fig. 4.38: PLL system by considering system operation

$$\begin{cases} K_1 = \left| \frac{Z_L}{Z_L + Z_g} \right| \\ K_2 = \left| \frac{Z_L Z_g}{Z_L + Z_g} \right| \end{cases} \quad (29)$$

Simply following the typical modeling process, Fig. 4.39 shows the proposed PLL model considering the converter system operation. In general, the non-linear characteristics of the PD are ignored in the typical PLL model, since the model is linearized around the equilibrium point which is close to zero; i.e.,  $\theta_g - \theta_C = 0$ . However, the non-linear term (sinusoidal function) has to be included in the proposed model here, since the steady-state may not necessarily be at zero.

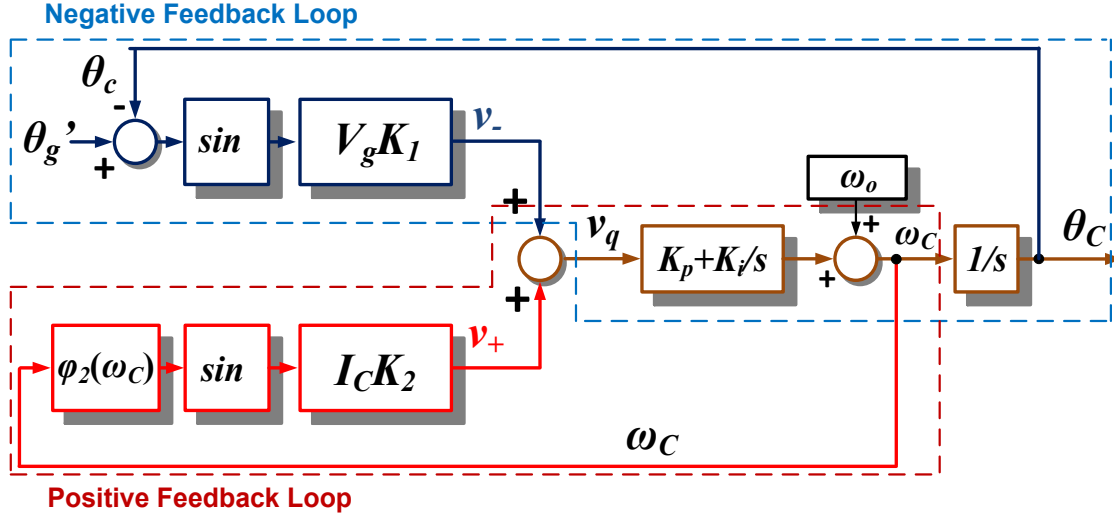


Fig. 4.39: Proposed quasi-static PLL model

The parameters in Fig. 4.39 are shown in (30) and (31).

$$\begin{cases} K_1 = \left| \frac{Z_L(\omega_g)}{Z_L(\omega_g) + Z_g(\omega_g)} \right| \\ K_2 = \left| \frac{Z_L(\omega_C) Z_g(\omega_C)}{Z_L(\omega_C) + Z_g(\omega_C)} \right| \end{cases} \quad (30)$$

$$\begin{cases} \theta_g' = \theta_g + \varphi_1(\omega_g) = \theta_g + \text{phase} \left( \frac{Z_L(\omega_g)}{Z_L(\omega_g) + Z_g(\omega_g)} \right) \\ \varphi_2(\omega_C) = \text{phase} \left( \frac{Z_L(\omega_C) Z_g(\omega_C)}{Z_L(\omega_C) + Z_g(\omega_C)} \right) \end{cases} \quad (31)$$

Besides the second order negative-feedback loop, another first order positive-feedback loop appears in the proposed model, representing the injection current effect. The output of the positive-feedback loop  $v_+$  in (32) is a disturbance to the PLL loop, which tends to drive the output of the PLL away from the utility input phase  $\theta_g$ . It should be noted that the  $\varphi_2$  in Fig. 4.39 is the phase-shift function in terms of input frequency  $\omega_C$ .

$$v_+ = I_C \cdot K_2 \cdot \sin(\varphi_2(\omega_C)) \quad (32)$$

It is seen that the effect of the positive feedback is determined by  $\varphi_2$ ,  $I_C$ , and  $K_2$ . Higher injection current, bigger grid input impedance (weak grid condition), and bigger reactive components (bigger  $\varphi_2$ ) give a bigger positive-feedback effect. Higher grid-input impedance and lower utility voltage give a smaller negative feedback. Due to the integrator inside of the LF ( $K_p + K_i/s$ ), the PLL is stable only when  $v_q = 0$ . The negative

feedback loop automatically tunes the error signal  $\theta_g' - \theta_C$  to correct the disturbance of  $v_+$  and to secure  $v_q = 0$ .

However, the non-linearity (sinusoidal function) of the PD limits its negative feedback output  $v_-$  in (33), which is determined by  $K_I$  and  $V_g$ .

$$-V_g K_I \leq v_- \leq V_g K_I \quad (33)$$

Therefore, the PLL may leave the stability region when  $v_+$  is bigger than the maximum output of  $v_-$ . The large-signal stability requirement can be derived in (34).

$$\begin{aligned} |v_+| &< |v_-| \\ \Rightarrow I_C &< \frac{V_g}{|\sin(\phi_2(\omega_C))Z_g|} \approx \frac{V_g}{|\phi_2(\omega_C)Z_g|} \end{aligned} \quad (34)$$

The results of (34) show that a higher utility voltage level, lower injection current, smaller grid input impedance and smaller reactive component result in a more stable operation of PLL. The results also reveal that a higher penetration of renewable distributed generation units or a weak grid may result in the frequency instability of the converter. Further derivation shows a conservative global large-signal stability requirement in (35) given any  $Z_L$  and system frequency  $\omega_C$ . This means if (35) is true, the frequency will be always stable.  $I_{C\_p.u.}$  and  $Z_{g\_p.u.}$  are the per unit values. Therefore, (35) can be used for systems with different ratings.

$$I_{C\_p.u.} \cdot |Z_{g\_p.u.}| < 1 \quad (35)$$

The instability of PLL can be also understood in another way.  $v_+$  simply shifts the operating point of the negative feedback loop away from zero. As shown in Fig. 4.40, as soon as the operating point moves out of the stable region, the PD gain will flip the sign. As such, the negative feedback loop will act like another positive feedback loop leading to instability. If there is a ripple component on top of  $\omega_C$ , it could increase the maximum value of  $v_+$ , which reduces the stability region of PLL. Thus, the PLL tends to be more unstable when the system is polluted or severely unbalanced.

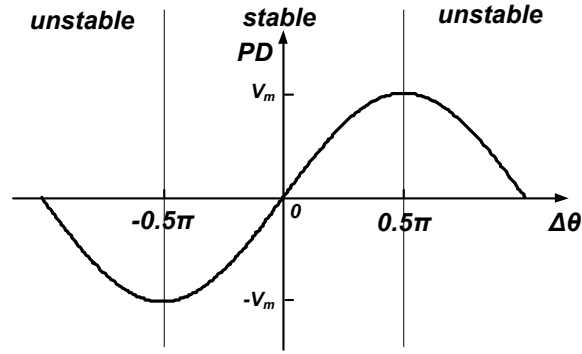


Fig. 4.40: Trigonometric PD output

The proposed PLL model also shows that the sign of  $\varphi_2$  determines the sign of the positive-feedback loop. When  $\varphi_2 > 0$  (inductive load), the positive-feedback loop tries to drive the frequency up to infinity; when  $\varphi_2 < 0$  (capacitive load), the positive-feedback loop tries to drive the frequency down to zero. When  $\varphi_2 = 0$ , the positive feedback loop disappears.

Fig. 4.41 and Fig. 4.42 show two instability PLL simulation results under capacitive and inductive local-load ( $Z_L$ ), respectively. Both results are obtained under weak grid conditions, and the parameters are shown in Table 4.3, where the switching frequency  $f_s$  is 20 kHz.

Table 4.3: Parameters used for simulation

$Z_L$ in Fig. 4.41	$3 \Omega + 50 \mu\text{F}$
$Z_L$ in Fig. 4.42	$3 \Omega + 60 \text{mF}$
$Z_g$	$90 \Omega$
$I_C$	50 A
$V_g$	150 V
$f_o$	60 Hz
$f_s$	20 kHz
$K_p, K_i$	5, 1

As shown in both figures, the unstable non-linear oscillations occur when the grid input-impedance steps from a stiff grid to a weak grid at 0.1 seconds, and the oscillation direction depends on the sign of  $\varphi_2$ . As shown in the figures, the proposed PLL model (blue curve) can accurately predict the non-linear frequency oscillation and matches the switching model simulation results.

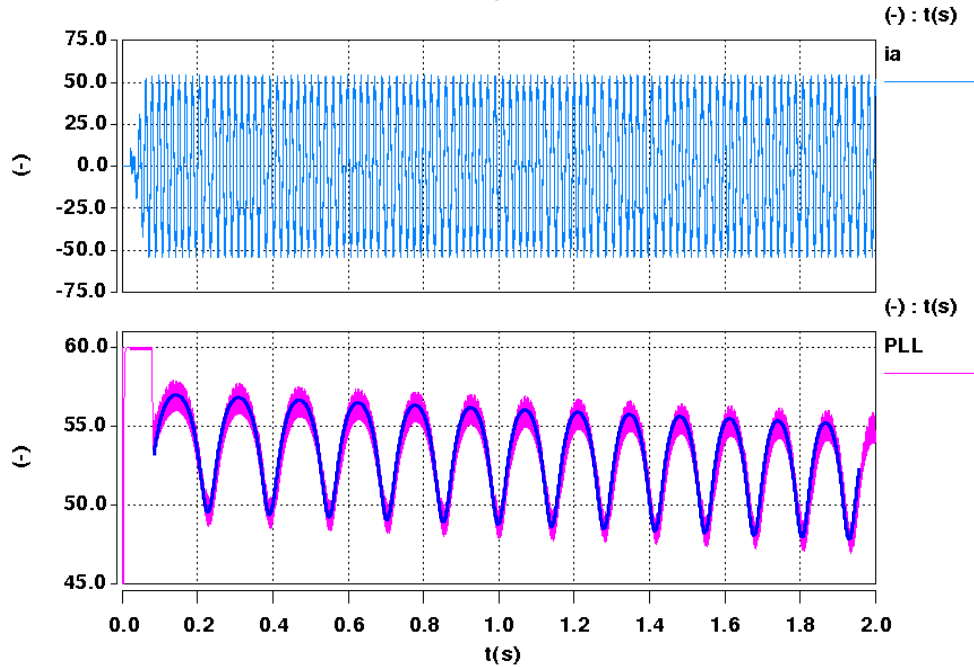


Fig. 4.41: Switching converter simulation results  $\omega_c$  (purple) [5 Hz/DIV], one phase current  $i_a$  (blue) [25A/DIV], and proposed PLL model output  $\omega_c$  (dark blue)

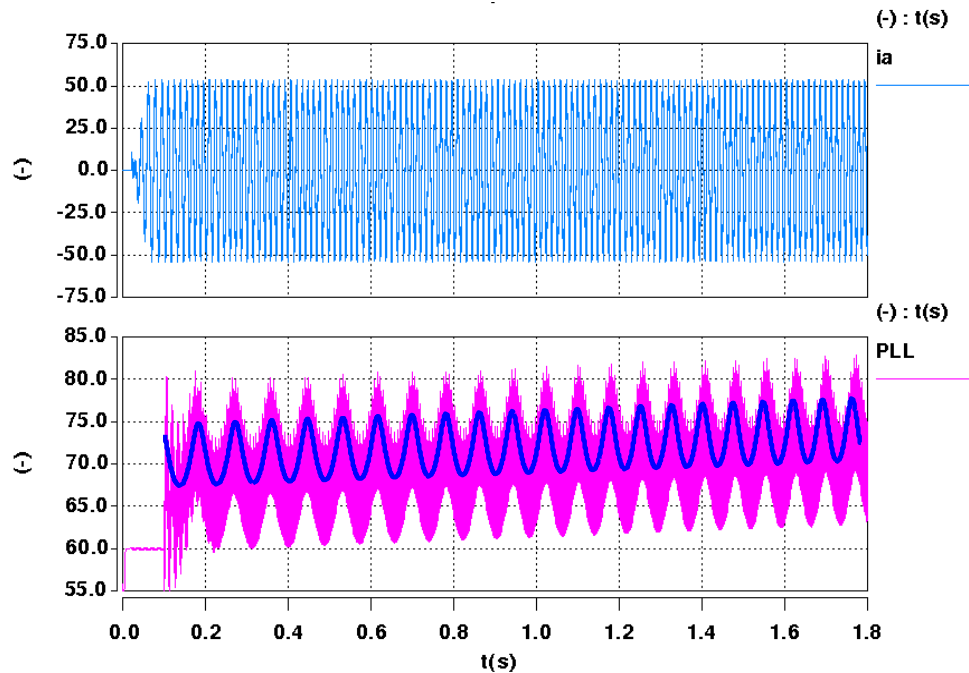


Fig. 4.42: Switching converter simulation results  $\omega_c$  (purple) [5 Hz/DIV], one phase current  $i_a$  (blue) [25A/DIV], and proposed PLL model output  $\omega_c$  (dark blue)

The above analysis can be readily applied to more complicated system configurations, like that Fig. 4.43, since the two-port network theorem can be easily used to simplify Fig. 4.43 as the equivalent circuit in Fig. 4.44.

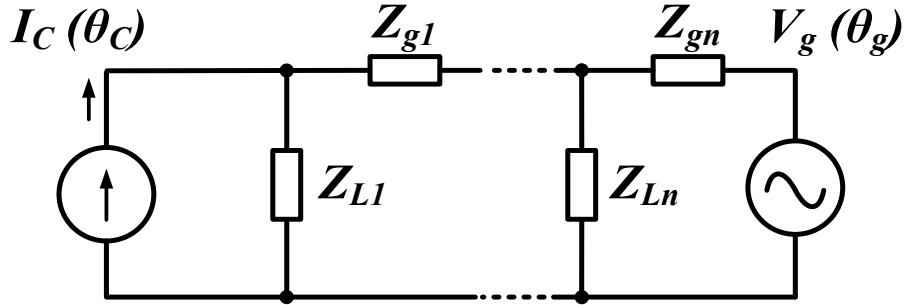


Fig. 4.43: One-line circuit with multiple shunt and series impedance

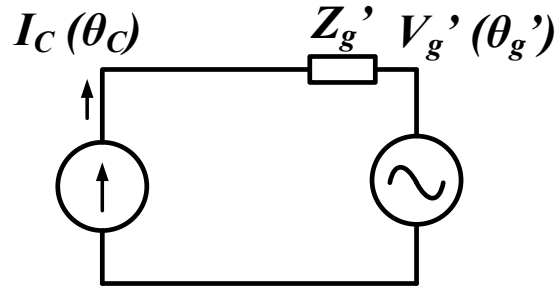


Fig. 4.44: One-line circuit with only the equivalent grid-input impedance

A simplified quasi-static PLL model based on Fig. 4.44 is readily obtained to predict the PLL frequency behavior as shown in Fig. 4.45. The parameters are shown in (36) and (37).

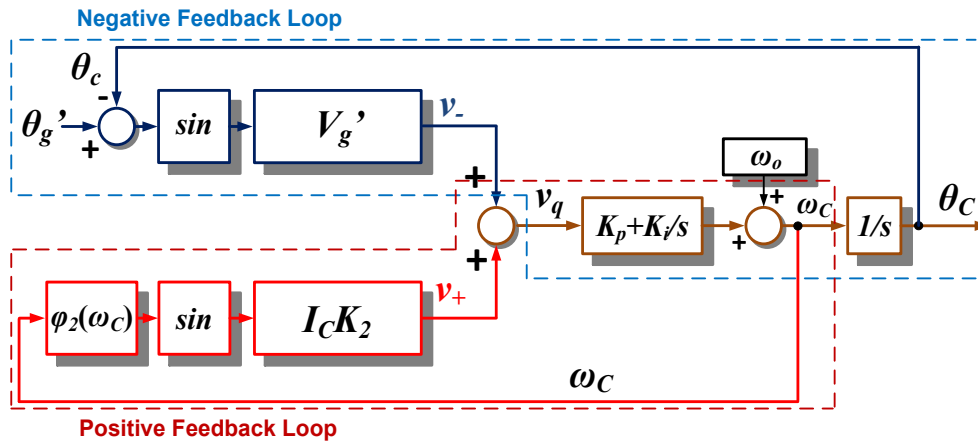


Fig. 4.45: Simplified PLL model considering converter interaction with utility

$$K_2 = \left| Z_g' \right| \tag{36}$$

$$\varphi_2 = \text{phase} \left( Z_g'(\omega_c) \right) \tag{37}$$

According to the model,  $V_g'$  and  $K_2$  must be obtained. To measure these values, the open circuit utility grid voltage amplitude  $V_g'$  can be measured in Fig. 4.46. The grid

input-impedance can be measured by placing the resistor loads  $R_1$  and  $R_2$ , as shown in Fig. 4.47 and Fig. 4.48, and measuring the terminal voltages two times.

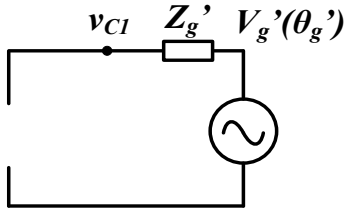


Fig. 4.46: Open circuit

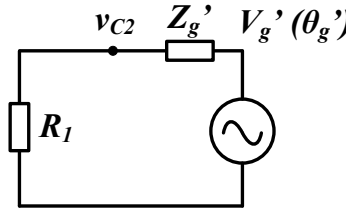


Fig. 4.47: Circuit with resistor 1

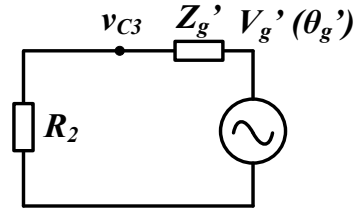


Fig. 4.48: Circuit with resistor 2

The amplitude of the terminal voltage  $v_{C1}$  measured in Fig. 4.46 is  $V_g'$ , and the voltage  $v_{C2}$ , and  $v_{C3}$  across the resistors  $R_1$  and  $R_2$ , as shown in (39), can be used to calculate the value of  $Z_g$  ( $R_g$  and  $X_g$ ), as shown in (40). Here the  $Z_g$  is assumed to be a passive component.

$$V_{C1} = V_g \quad (38)$$

$$\begin{cases} V_{C2} = \frac{R_1 V_{C1}}{\sqrt{(R_1 + R_g)^2 + (X_g)^2}} \\ V_{C3} = \frac{R_2 V_{C1}}{\sqrt{(R_2 + R_g)^2 + (X_g)^2}} \end{cases} \quad (39)$$

$$\begin{cases} R_g = \frac{v_{C1}^2}{2(R_1 - R_2)} \left( \frac{R_1^2}{V_{C2}^2} - \frac{R_2^2}{V_{C3}^2} \right) - \frac{R_1 + R_2}{2} \\ X_g = \sqrt{\frac{R_1^2 V_{C1}^2}{V_{C2}^2} - \left( \frac{V_{C1}^2}{2(R_1 - R_2)} \left( \frac{R_1^2}{V_{C2}^2} - \frac{R_2^2}{V_{C3}^2} \right) + \frac{R_1 - R_2}{2} \right)^2} \end{cases} \quad (40)$$

The above analysis is based on a unity power factor current-injection condition. If the phase of the injected current is intentionally shifted by a factor of  $\Delta$  to support a certain amount of reactive power, the injected current in Fig. 4.34 would be shown in (41). The corresponding  $\varphi_2$  term in the proposed model (Fig. 4.39) would be calculated in (42).

$$\begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} = \begin{bmatrix} I_C \cos(\theta_C + \Delta) \\ I_C \cos\left(\theta_C - \frac{2}{3}\pi + \Delta\right) \\ I_C \cos\left(\theta_C + \frac{2}{3}\pi + \Delta\right) \end{bmatrix} \quad (41)$$



$$\varphi_2(\omega_c) = \text{phase} \left( \frac{Z_L(\omega_c)Z_g(\omega_c)}{Z_L(\omega_c) + Z_g(\omega_c)} \right) + \Delta \quad (42)$$

The results of (42) show that the angle  $\Delta$  has a strong impact on the positive feedback term, and thus affects the PLL stability region. If the bus-interface converter supplies reactive power to support the local-load reactive power requirement, (43) can be obtained. In this case, the PLL would be more stable due to the smaller positive feedback effect.

$$\left| \text{phase} \left( \frac{Z_L Z_g}{Z_L + Z_g} \right) + \Delta \right| < \left| \text{phase} \left( \frac{Z_L Z_g}{Z_L + Z_g} \right) \right| \quad (43)$$

#### 4.2.2.3. Experimental Evaluation

The frequency behavior under the weak grid is verified in a 2 kW two-level three-phase PWM converter system with a DSP-FPGA digital control platform, as shown in Fig. 4.49.

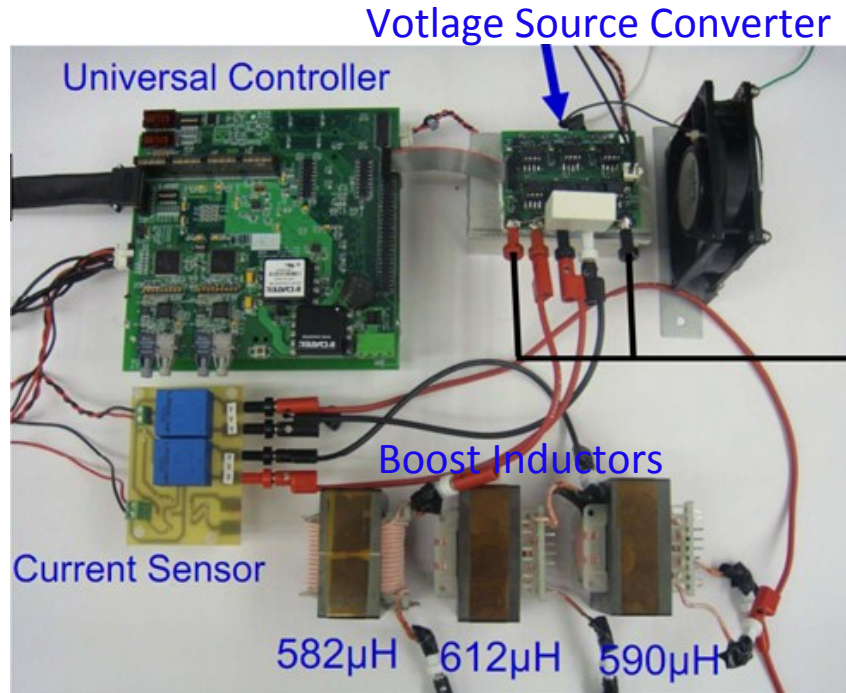


Fig. 4.49: Two-level three-phase voltage source converter system

The SRF PLL in Fig. 4.32 is used in the experiment. Different combinations of the three-phase resistor ( $R_L$ ), inductor ( $L_L$ ), and capacitor ( $C_L$ ) are used as the local-load  $Z_L$ , and a three-phase resistor is used as the grid input impedance  $Z_g$ . The system parameters in Table 4.4 are used in the test. When the grid impedance steps, the local-load voltage

doesn't change much, since most of the local-load power is supplied by the converter rather than the grid.

Table 4.4: Parameters used in experiments

$V_g$	$80 V_{pk}$
$I_C$	$10 A_{pk}$
$Z_g$	$160 \Omega$
$Z_L$ in Fig. 4.50 and Fig. 4.51	$10 \Omega R_L$ in parallel with $20 \mu F C_L$
$Z_L$ in Fig. 4.52 and Fig. 4.53	$10 \Omega R_L$ in parallel with $15 mH L_L$
$Z_L$ in Fig. 4.54 and Fig. 4.55	$10 \Omega R_L$
$f_o$	$60 \text{ Hz}$
$f_s$	$20 \text{ kHz}$

In the experimental results, a three-phase AC relay is used in parallel with  $R_g$  to switch between the stiff grid (0 p.u.  $Z_g$ ) and weak grid (20 p.u.  $Z_g$ ) conditions. The PLL output ( $\omega_C$ ) and one-phase voltage measured at the terminal of the local-load are shown under these three test conditions.

For the capacitive load condition ( $R_L//C_L$ ) ( $\varphi_2 < 0$ ) in Fig. 4.50, the PLL output drifts down to zero from 60 Hz as soon as the grid input-impedance steps. The PI parameters in the PLL are ( $K_p = 4.5$ ,  $K_i = 0.5$ ). Fig. 4.50 shows the oscillation due to the non-linearity of the PD. The PLL output drifts up under the inductive load condition ( $R_L//L_L$ ) ( $\varphi_2 > 0$ ), which is shown in Fig. 4.52. The PI parameters in PLL are ( $K_p = 0.5$ ,  $K_i = 1.5$ ). The simulation results under these two local-load conditions are also conducted and shown in Fig. 4.51 and Fig. 4.53, respectively. These figures clearly show that the experimental results match with the simulation results, and both can be explained and predicted by the proposed model.

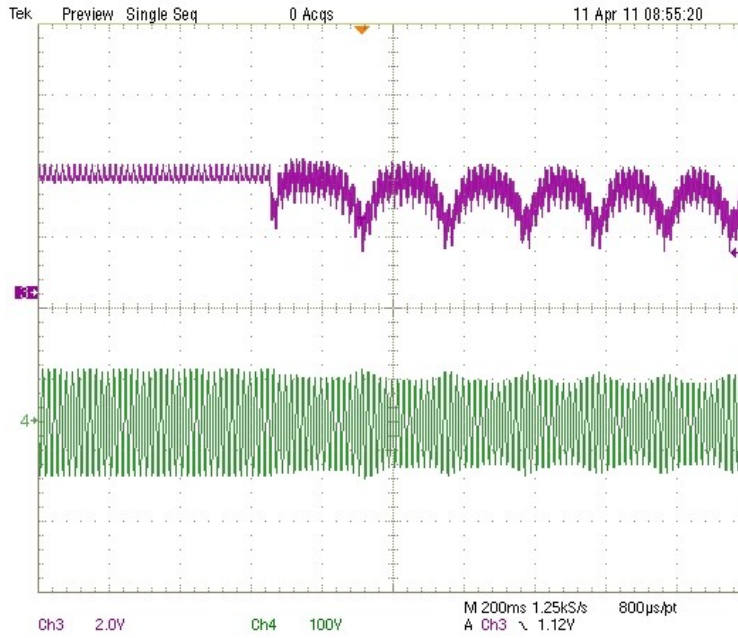


Fig. 4.50: PLL behavior under the capacitive local-load condition:  $\omega_c/2\pi$  (purple) [6 Hz/DIV], one-phase voltage  $v_{ga}$  (green) [100V/DIV]

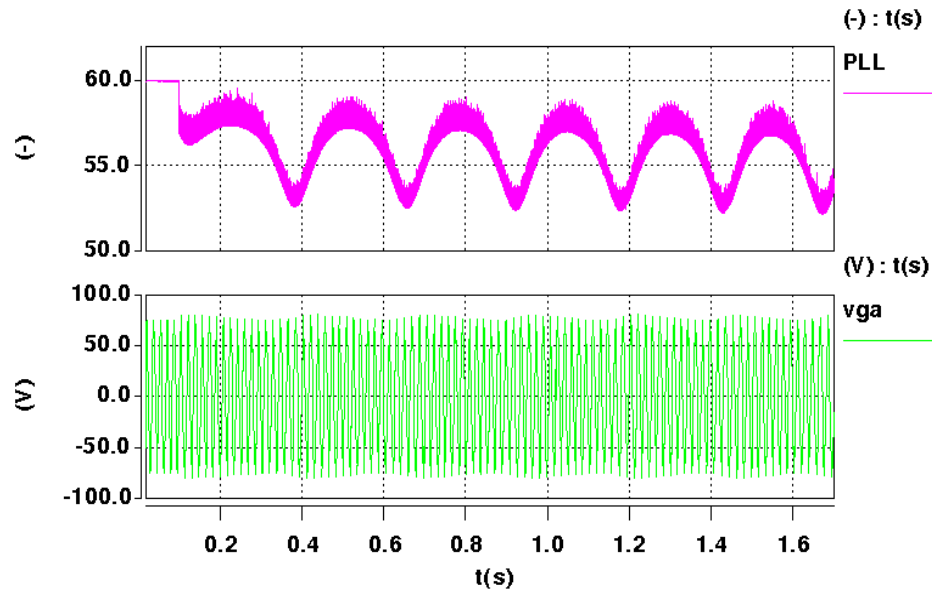


Fig. 4.51: Simulation of PLL output behavior when grid steps from stiff to weak condition under capacitive load in simulation.  $\omega_c/2\pi$  (purple) [5 Hz/DIV], one phase-voltage  $v_{ga}$  (green) [50/DIV]

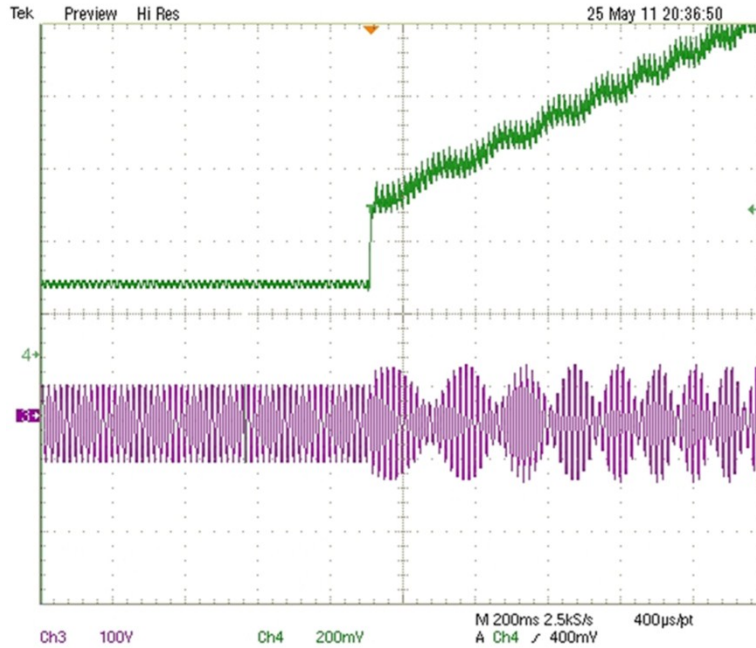


Fig. 4.52: PLL behavior under inductive local load condition:  $\omega_c/2\pi$  (green) [5 Hz/DIV], one-phase voltage  $v_{ga}$  (purple) [100V/DIV]

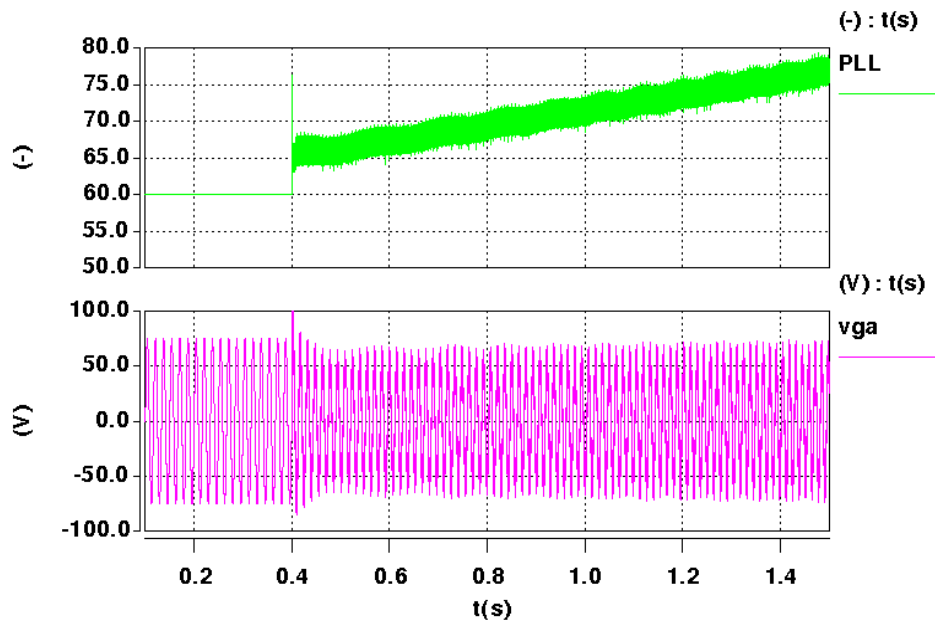


Fig. 4.53: Simulation of PLL output behavior when grid steps from stiff to weak condition under inductive load in simulation.  $\omega_c/2\pi$  (green) [5 Hz/DIV], one phase-voltage  $v_{ga}$  (purple) [50/DIV]

In Fig. 4.54, since the  $\varphi_2 = 0$ , the PLL output does not drift, but stays at the 60Hz under the resistor load condition eliminating the positive feedback effect. The PI parameters of PLL are ( $K_p = 4, K_i = 1$ ). Fig. 4.55 shows the simulation results matching with the experiment results.

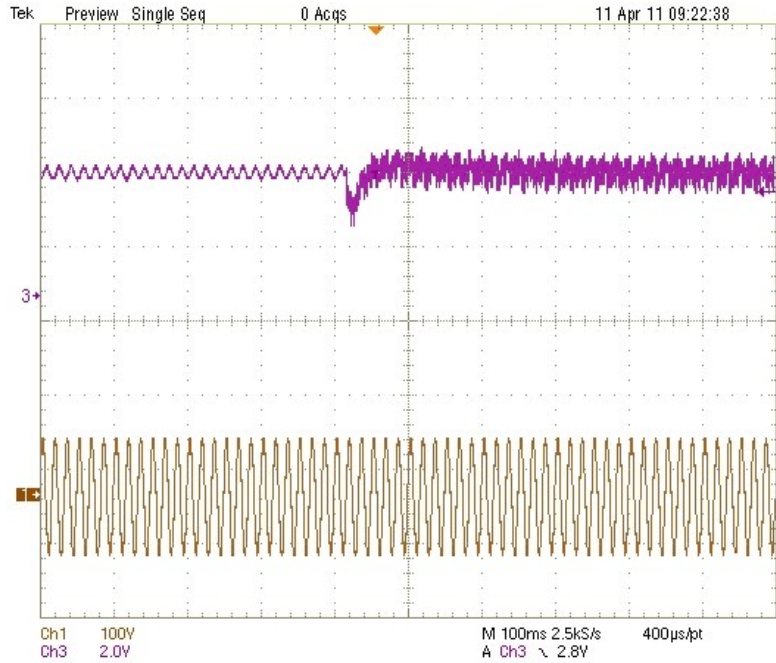


Fig. 4.54: PLL output behavior when grid steps from stiff to weak condition under inductive load.  $\omega_2$  (purple) [2.5 Hz/DIV], one phase-voltage  $v_{ga}$  (brown) [100/DIV]

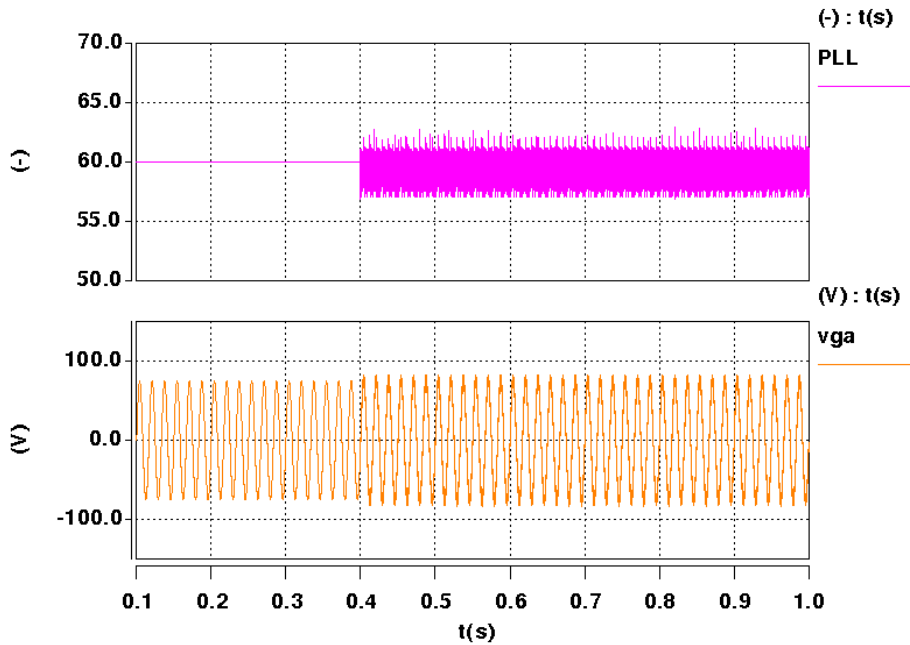


Fig. 4.55: PLL behavior under resistive local load condition.  $\omega_c/2\pi$  (purple) [5 Hz/DIV], one-phase voltage  $v_{ga}$  (orange) [100V/DIV]

#### 4.2.2.4. Conclusion

The first section in this chapter proposes a quasi-static PLL model by considering the converter system operation with utility grid and system impedances. A frequency

positive-feedback term is proposed, and its effect in regards to the grid input impedance, injection current (penetration level), and local-load characteristics is addressed.

Both simulation and experimental results validate the proposed model, which accounts for the frequency-stability and its non-linear behavior under the weak grid. The model can also explain many frequency-stability behaviors in converter system operating under islanded condition, and the modeling process can be applied to other  $1\Phi$  and  $3\Phi$  PLLs.

### **4.2.3. MODELING OF GRID SYNCHRONIZATION AT ISLANDED CONDITIONS**

#### **4.2.3.1. Introduction**

Ac micro-grid or nano-grid, which are pockets of distributed energy resources that can be isolated from the utility power grid, are considered by many in the industry to be the ultimate example of energy democracy since they diversify the ownership of the supply infrastructure. Micro-grids offer a compelling alternative to traditional energy generation and distribution, utilizing smart grid technologies to enable integrated control of distributed power generation assets either in parallel to or “islanded” from the utility power grid. Thus micro-grids have become more popular in the commercial, military and industrial sectors. The world micro-grid market reached 4 billion US dollars in 2010.

One of the prominent features of the ac micro-grid is that the local distribution system is able to operate under islanded conditions. The power generation and power consumption are balanced between the DG units, energy storage devices, and local loads. There are many challenges in controlling of the grid-interface converter in micro-grid applications in terms of achieving stable steady-state operation, predictable transient behavior, and seamless mode transition between the grid-connected mode and the islanded mode. Therefore, a clear understanding of the converter’s frequency transient behavior from the grid-tied mode to the islanded mode is required to avoid potential system failure, oscillation, or cascading failure propagating throughout the micro-grid system.

In addition, detailed insight into the grid synchronization behavior under islanded conditions is a useful tool to evaluate the existing frequency-stability-based islanding

detection methods. In turn, new islanding detections solutions and design procedures can be proposed.

#### 4.2.3.2. PLL Analysis

The PLL model proposed in previous section is very suitable for use in studying the converter system grid synchronization behavior at the islanded condition. If the system is only supported by a single DG unit, the islanded system frequency is solely determined by the converter itself, and the converter output frequency is the same as the system frequency.

In order to understand the frequency transient behavior from the grid-tied mode to islanded mode, two extreme operation conditions can be considered; i.e., a stiff-grid condition and islanded (off-grid) condition. The grid input impedance  $Z_g$  at these two conditions would be approaching to zero and infinite, respectively. As such, the parameters in Fig. 4.39 would be (44) at the stiff grid-tied condition.

$$\begin{cases} K_1 = 1 \\ K_2 = 0 \\ \varphi_1(\omega_g) = \varphi_2(\omega_c) = 0 \end{cases} \quad (44)$$

The PLL sub-model at the stiff-grid condition can be simplified by substituting the parameters in (44) into the proposed PLL model in Fig. 4.39. The PLL sub-model at the stiff-grid condition is shown in Fig. 4.56.

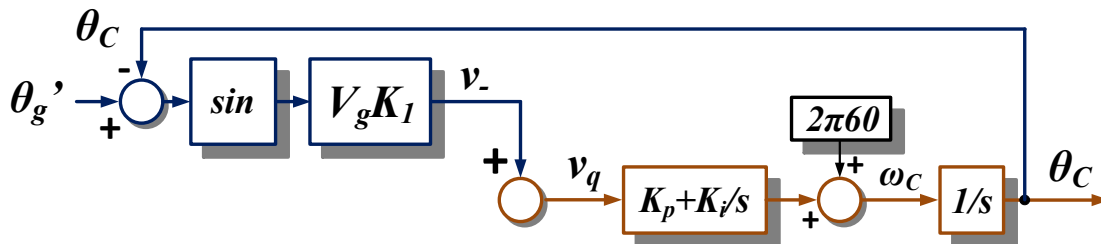


Fig. 4.56: PLL model under stiff grid-connected condition

Under the islanded condition, the  $K_1$ ,  $K_2$  and  $\varphi_2$  in Fig. 4.39 would be the values shown in (45).

$$\begin{cases} K_1 = 0 \\ K_2 = |Z_L| \\ \varphi_2(\omega_c) = \text{phase}(Z_L(\omega_c)) \end{cases} \quad (45)$$

The PLL sub-model at the islanded condition can be obtained as shown in Fig. 4.57.

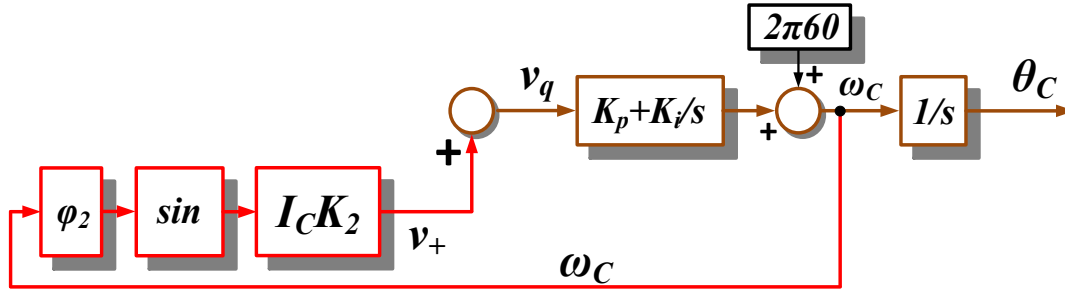


Fig. 4.57: PLL model under islanded condition

The PLL at the stiff grid would be the same as the typical second-order PLL model, and the PLL model under the islanded condition shows that only the first-order (only one integrator in the loop) positive feedback loop presents in PLL, which is inherently unstable. Due to the integrator in PI in PLL, the frequency may drift away from the steady-state. The following discussion focuses on the PLL model in Fig. 4.57 and addresses its characteristics.

If consider a *RLC* paralleled local-load according to [176], as shown in Fig. 4.58, the impedance of  $Z_L$  would be  $//R_L C_L L_L$ .

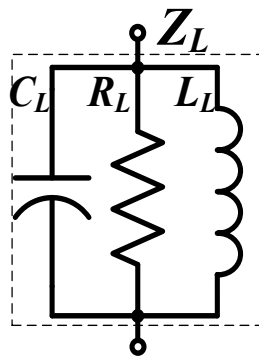


Fig. 4.58:  $R_L, C_L, L_L$  in parallel as the local load

The characteristics of  $K_2$  and  $\varphi_2$  can be simply derived as:



$$\left\{ \begin{array}{l} K_2(\omega_C) = \frac{R_L}{\sqrt{1 + Q^2 \left( \frac{\omega_C}{\omega_r} - \frac{\omega_r}{\omega_C} \right)^2}} \\ \varphi_2(\omega_C) = \arctan \left[ \frac{R_L \left( 1 - \frac{\omega_C^2}{\omega_r^2} \right)}{\omega_C L_L} \right] \end{array} \right. \quad (46)$$

$$\omega_r = \frac{1}{2\pi\sqrt{L_L C_L}}, Q = R_L \sqrt{\frac{C_L}{L_L}}$$

It is seen that the injection current level  $I_C$ , local-load quality-factor  $Q$ , and local-load resonant-frequency  $\omega_r$  largely determine the positive-feedback loop gain  $I_C K_2$ . For matched load condition, the following equation would be valid in (47), meaning simply that the positive loop gain is proportional to the system voltage level.

$$I_C K_2(\omega_C) = \frac{V_g}{\sqrt{1 + Q^2 \left( \frac{\omega_C}{\omega_r} - \frac{\omega_r}{\omega_C} \right)^2}} \quad (47)$$

The PLL model also shows that the sign of  $\varphi_2$  determines the sign of the positive-feedback loop. When  $\varphi_2 > 0$  (inductive load,  $\omega_r > \omega_C$ ), the positive-feedback loop tries to drive the frequency up; when  $\varphi_2 < 0$  (capacitive load,  $\omega_r < \omega_C$ ), the positive-feedback loop tries to drive the frequency down. When  $\varphi_2 = 0$  (resistive load or  $\omega_r = \omega_C$ ), the positive-feedback loop disappears. Hence, the PLL frequency will be driven by the PI in the PLL until the positive feedback loop disappears. The following conclusions can be drawn under the islanded condition:

1. The PLL frequency  $\omega_C$  will approach the local-load resonant frequency  $\omega_r$ . The drift rate is determined by integrator gain  $K_i$  in PI,  $\varphi_2$  and  $K_2$ . Therefore, a higher PLL bandwidth leads to higher drift rate. Due to the nature of the first-order system, the PLL frequency will never stay at  $\omega_r$ , and the drift rate will be slower when  $\omega_C$  is closer to  $\omega_r$ .

2. The PLL frequency won't drift if  $\omega_r$  is the same as the line-frequency, or under a purely resistive load condition.

As mentioned above,  $K_2$  and  $\varphi_2$  are related to the system frequency  $\omega_C$  and quality factor  $Q$ . A small  $Q$  makes  $K_2$  and  $\varphi_2$  insensitive to the system frequency. Fig. 4.59 and Fig. 4.60 show the normalized  $K_2$  in terms of system frequency and quality factor.  $K_2$  reaches its maximum value at the resonant frequency (in simulation, the resonant frequency is set at 60 Hz). Fig. 4.61 and Fig. 4.62 show  $\varphi_2$  in terms of system frequency and quality factor. The  $\varphi_2$  figure shows that the positive feedback will drive the frequency to the resonant frequency; the resonant frequency would be the stable equilibrium point.

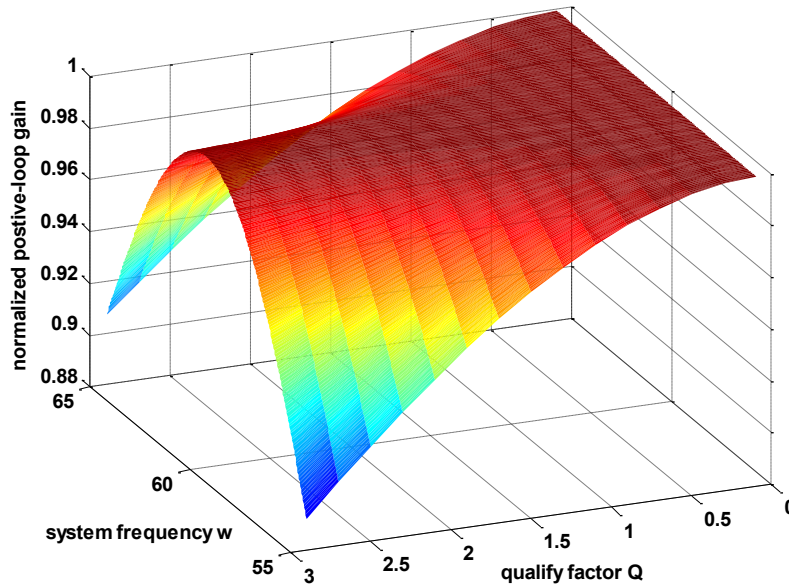


Fig. 4.59: 3-D figure of  $K_2$  in terms of  $\omega_C$  and  $Q$

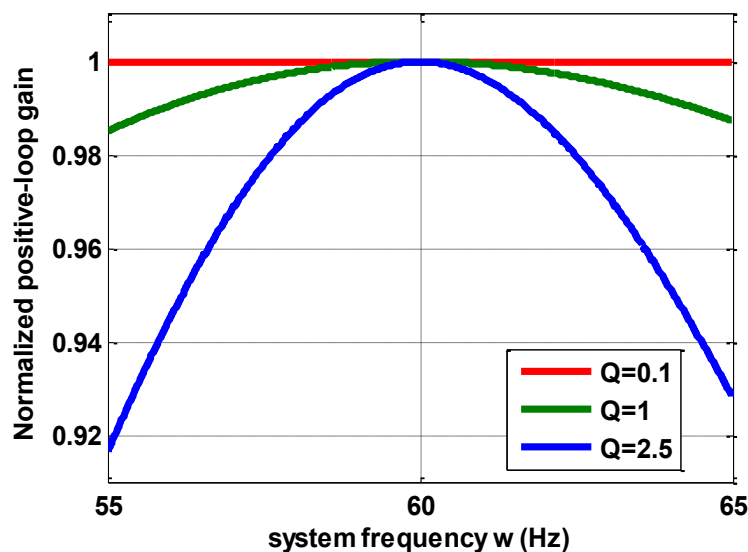


Fig. 4.60: 2-D figure of  $K_2$  in terms of  $\omega_C$  and  $Q$

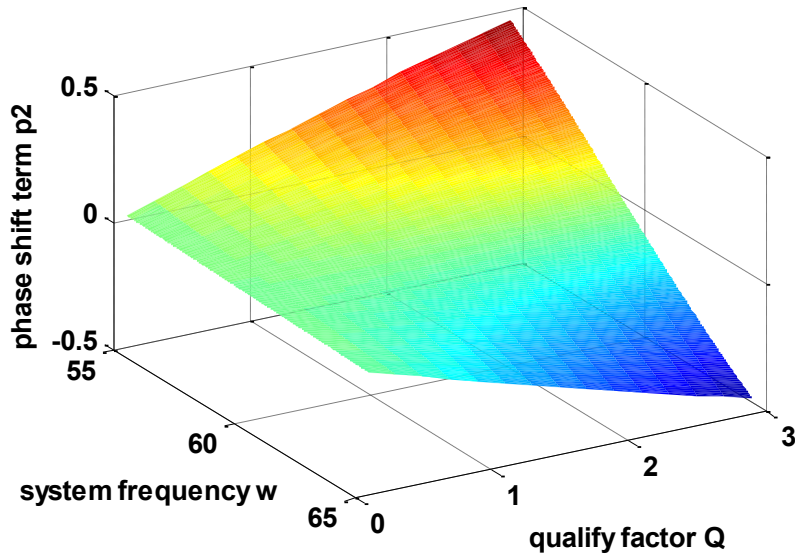


Fig. 4.61: 3-D figure of  $\varphi_2$  in terms of  $\omega_C$  and  $Q$

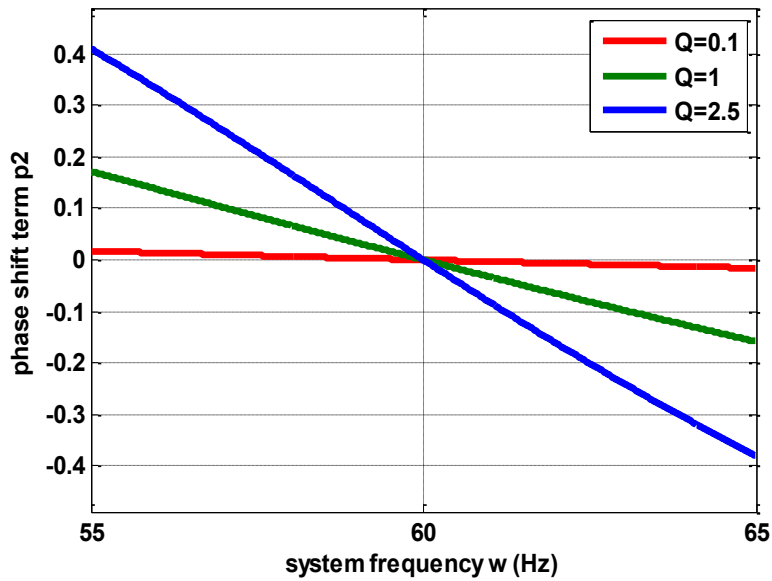


Fig. 4.62: 2-D figure of  $\varphi_2$  in terms of  $\omega_C$  and  $Q$

The switching model (2-level 3  $\Phi$  voltage-source converter) simulation is conducted to evaluate the above results. The parameters in the simulation are shown in Table 4.5 and the islanding condition occurs at 0.2 sec.  $//R_L C_L$  (equivalent  $\omega_r = 0$ ) and  $//R_L L_L$  (equivalent  $\omega_r = \infty$ ) local-loads are simulated in Fig. 4.63 and Fig. 4.64, respectively. The frequency will drift toward to the equivalent resonant frequency to 0 Hz or  $\infty$  Hz, and thus an over/under frequency measurement can easily detect the islanding event. Another

load  $//R_L L_L C_L$  ( $\omega_r = 60$  Hz) is simulated in Fig. 4.65, showing that the frequency won't drift due to  $\varphi_2 = 0$ , which requires a modification to detect.

Table 4.5: Parameters in simulation

$K_p, K_i$	3, 2
$//R_L C_L$	3 $\Omega$ // 20 $\mu$ F
$//R_L L_L$	3 $\Omega$ // 50 mH (0.1 $\Omega$ resistor is in series with LL for damping )
$//R_L L_L C_L$	3 $\Omega$ // 17.4 mH // 400 $\mu$ F (0.1 $\Omega$ resistor is in series with LL for damping )
$V_g$	150 V
$I_C$	50 A
$f_o$	60 Hz
$f_s$	20 kHz

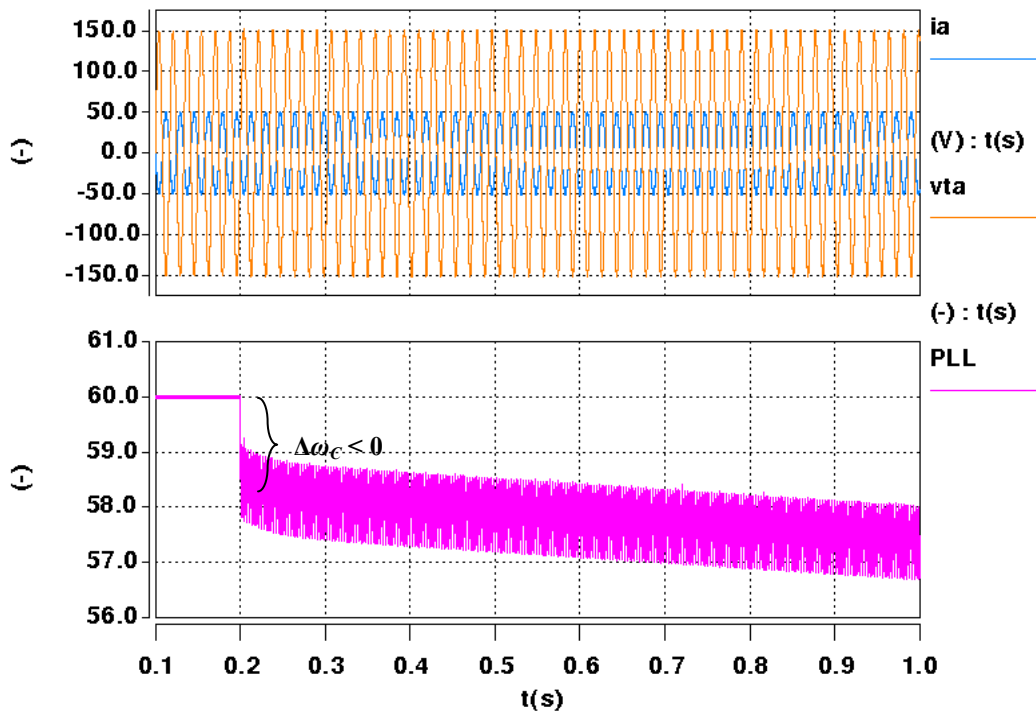


Fig. 4.63: PLL output under islanded condition with  $//R_L C_L$  load. One phase voltage and current,  $v_{Ca}$  (maroon) [50V/DIV],  $i_a$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (magenta) [1Hz/DIV]

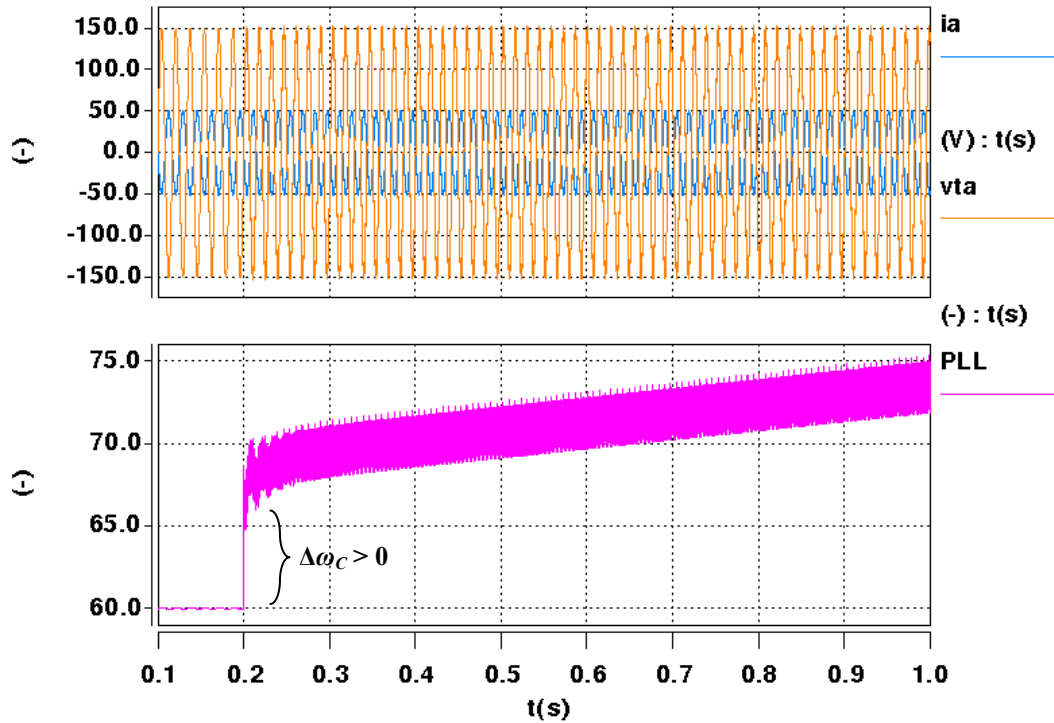


Fig. 4.64: PLL output under islaned condition with  $//R_L L_L$  load. One phase voltage and current,  $v_{Ca}$  (maroon) [50V/DIV],  $i_a$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (magenta) [5Hz/DIV]

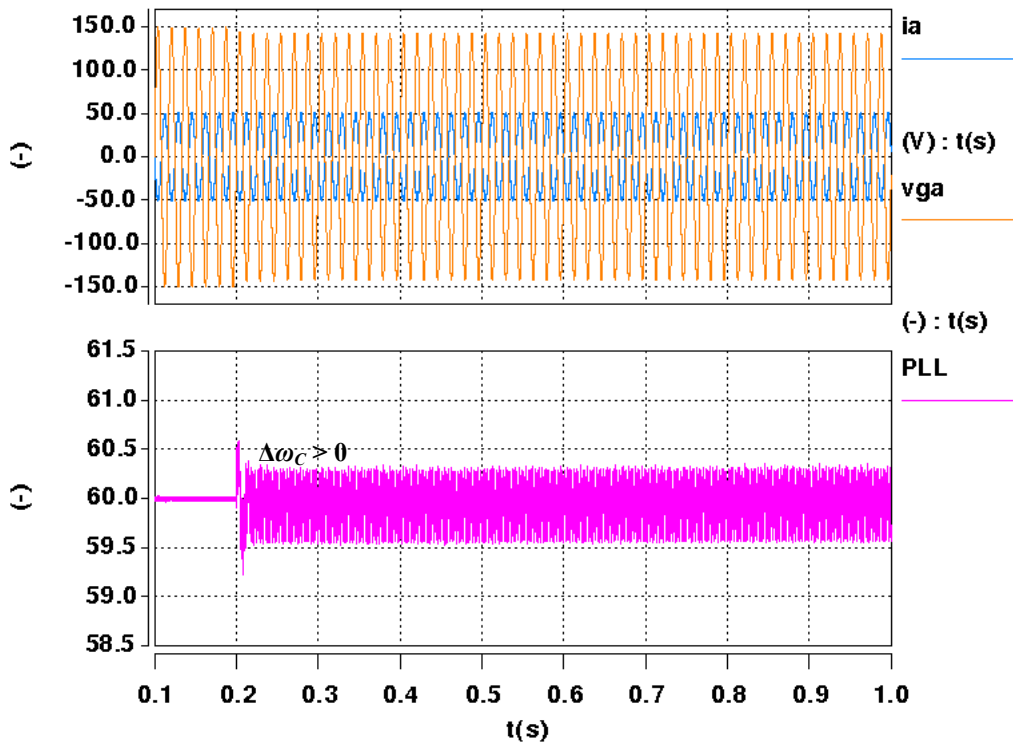


Fig. 4.65: PLL output under islaned condition with  $//R_L L_L C_L$  load. One phase voltage and current,  $v_{Ca}$  (maroon) [50V/DIV],  $i_a$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (magenta) [0.5Hz/DIV]

It is also interesting to observe the frequency step  $\Delta\omega_C$  when islanding occurs, which helps quickly detect the islanding event.  $\Delta\omega_C$  is due to the switch from the grid-tied sub-mode in Fig. 4.56 to the islanded sub-mode in Fig. 4.57.  $v_q$  equals zero before the islanding event. After the islanding event,  $v_q$  steps from zero to  $v_+$ , leading to a frequency step, as shown in (48).

$$\Delta\omega_C = K_p \cdot v_+ = K_p \cdot \varphi_2(\omega_C) \cdot I_C \cdot K_2 \quad (48)$$

Table 4.6 shows a comparison between the simulation results and the model prediction results of the frequency step  $\Delta\omega_C$ .

	Simulation	Prediction
// $R_L C_L$	$-1.6 \times 2\pi$ rad	$-1.6125 \times 2\pi$ rad
// $R_L L_L$	$+9.3 \times 2\pi$ rad	$+11.2 \times 2\pi$ rad
// $R_L L_L C_L$	0 rad	0 rad

Table 4.6 shows that the PLL can be used to detect most of the islanding event. Ideally, there is no obvious stability issue under the power-matched //RLC load with 60 Hz resonant frequency, and this load can be regarded as the worst load condition or non-detection zone (NDZ) point.

If the delay effect is considered, which is contributed largely by the sensor delay, the real worst loading case is NOT the //RLC load with 60 Hz resonant frequency. The following discussions explain this briefly.

If it is assumed that the total delay at 60 Hz is  $\Delta$  rad, the PLL system would be configured as shown in Fig. 4.66 with the consideration of this delay.

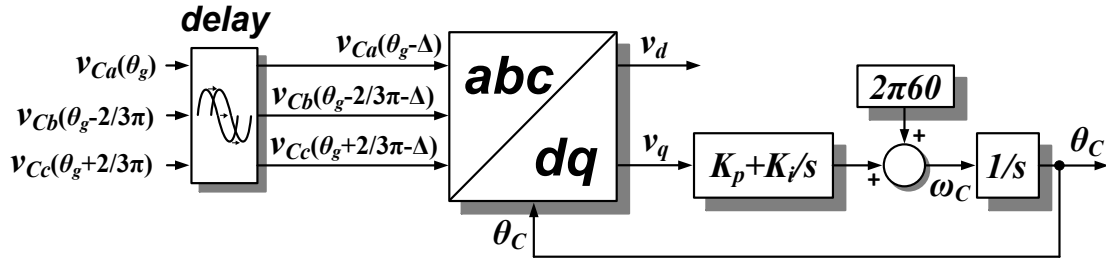


Fig. 4.66: PLL when considering the delay effect

Thus, the  $\varphi_2$  term in Fig. 4.57 would be (49).

$$\varphi_2(\omega_C) = \arctan \left[ Q \left( \frac{\omega_r^2 - \omega_C^2}{\omega_C \omega_r} \right) \right] - \Delta \quad (49)$$

The delay has a direct impact on the phase-shift term. If the local-load resonant frequency is 60 Hz, the  $\varphi_2$  term would be (50) when the islanding condition occurs.

$$\varphi_2(\omega_C) = -\Delta \quad (50)$$

Thus, the PLL output frequency is expected to have a negative frequency step, and the PLL will drift to a frequency when  $\varphi_2 = \Delta$ . The frequency step would be

$$\Delta\omega_C = K_p \cdot v_+ = -K_p \cdot I_C \cdot R_L \cdot \Delta \quad (51)$$

It can be seen that the negative frequency step would be in proportional to the delay time, and the frequency will drift down to a frequency smaller than 60 Hz, even though the local-load resonant frequency is 60 Hz. As shown in Fig. 4.67, if the delay at 60 Hz (exaggerated for clarity) is 25  $\mu\text{s}$  and 50  $\mu\text{s}$ , the average model simulation results show that the PLL will drift down. The simulation condition is shown in Table 4.7. Therefore, due in large part to the delay-effect, the islanding event under the 60 Hz resonant frequency local-load can still be detected.

Table 4.7: Parameters in simulation

$K_p, K_i$	3, 3
$R_L$	4 $\Omega$
$L_L$	50 mH (in series with 0.3 $\Omega$ damping resistor)
$C_L$	140.7 $\mu\text{F}$
$\omega_r$	$2\pi 60$ rad/s
$V_g$	100 V
$I_C$	25 A

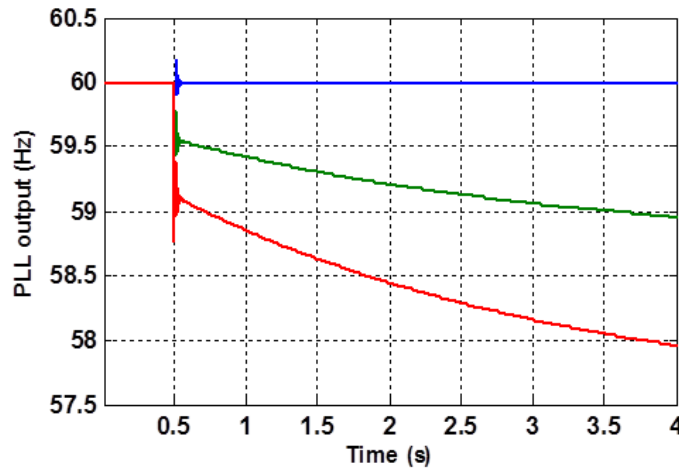


Fig. 4.67: Average model simulation results of PLL output with digital delay under  $//R_L C_L L_L$  load with 60 Hz resonant frequency.  $\omega_C$  (blue) [0.5 Hz/DIV] without delay,  $\omega_C$  (green) [0.5 Hz/DIV] with 25  $\mu\text{s}$  delay,  $\omega_C$  (red) [0.5 Hz/DIV] with 50  $\mu\text{s}$  delay

If the delay effect is considered, the real NDZ local-load would be the power-matched load with the resonant frequency in (52).

$$\arctan \left[ Q \left( \frac{\omega_r^2 - \omega_c^2}{\omega_c \omega_r} \right) \right] = \Delta \Rightarrow \omega_r = \left( \frac{k}{2} + \sqrt{\left( 1 + \frac{k}{4} \right)} \right) \omega_c, k = \frac{1}{Q} \tan \Delta \quad (52)$$

It is seen that the NDZ point resonant frequency, related to the load quality factor  $Q$  and the delay time, no longer stays at 60 Hz, but will be a little higher than 60 Hz. On the other hand, using PLL itself without any modification can directly comply with the AI test standard which defines using the  $RLC$  load with a 60 Hz resonant frequency, as long as a digital delay is present in the loop.

It should be noted that, if the local-load is a purely resistive load, the PLL model under the islanded condition by considering the delay effect is shown in Fig. 4.68. The PLL becomes an open-loop system as  $\varphi_2$  equals zero. As such, the delay propagates through the PLL and the output  $\omega_c$  drifts away. However, the sensor delay is so small at the line frequency that the drift rate is extremely slow.

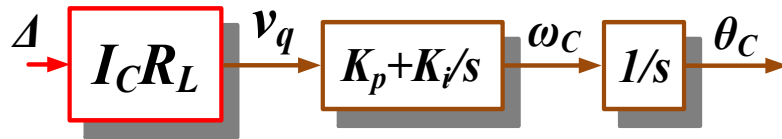


Fig. 4.68: PLL model under purely resistive load at islanded condition

#### 4.2.3.3. Experiments

The experimental setup is shown in Fig. 4.69. A three-phase two-level VSI is used as the grid-interface converter. The components used to conduct the experiment are shown in Fig. 4.70, including three-phase resistors, capacitors, and inductors. Fig. 4.71 shows the three-phase relays at the PCC switch. The test parameters are shown in Table 4.8.

Table 4.8: Parameters for Test (per phase)

System voltage $V_g$	// $R_L C_L$ load in Fig. 43	// $R_L L_L$ load in Fig. 45	// $R_L L_L C_L$ load in Fig. 47
80 V	$10\Omega + 20\mu\text{F}$	$10\Omega + 15\text{mH}$	$10\Omega + 600\mu\text{F} + 11.5\text{mH}$



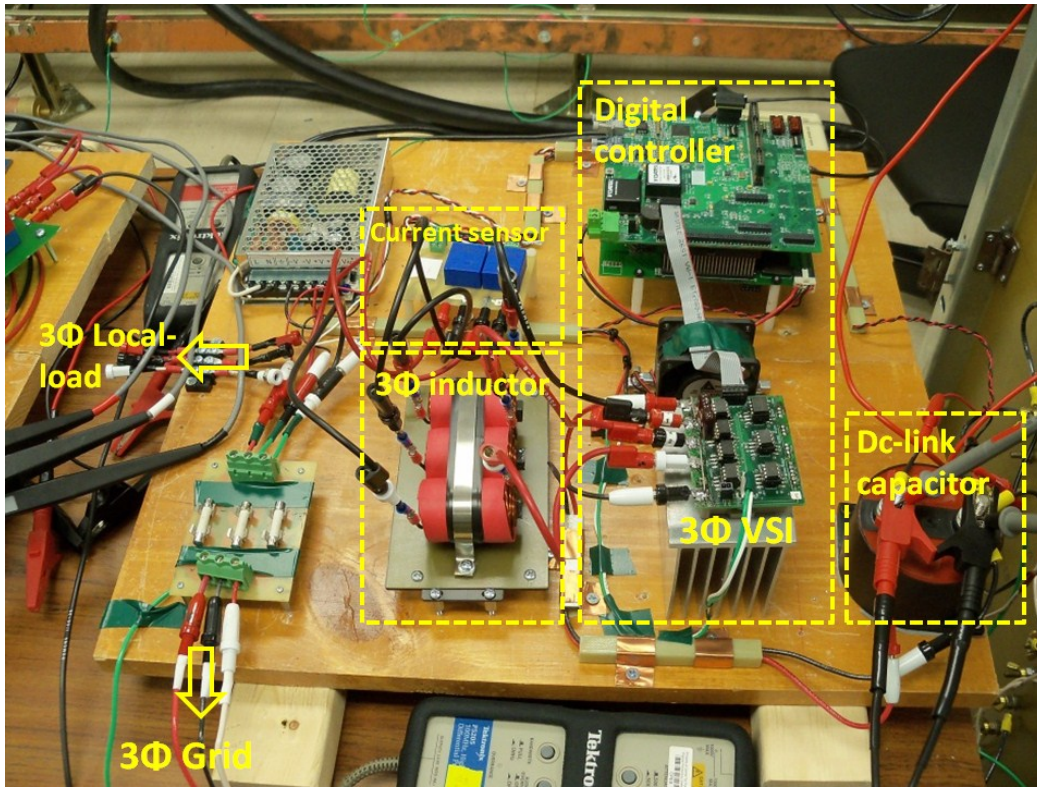


Fig. 4.69: 5 kW three-phase PWM converter test bed

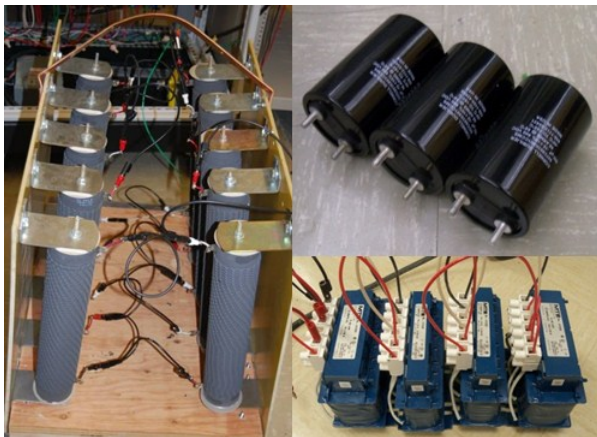


Fig. 4.70: Three-phase loads for test



Fig. 4.71: Three-phase relay used as the PCC switch

Fig. 4.72 and Fig. 4.73 show the PLL outputs with the capacitive load under the islanded condition in experiment and in simulation, respectively. In both of these cases, the output drifts down to zero.

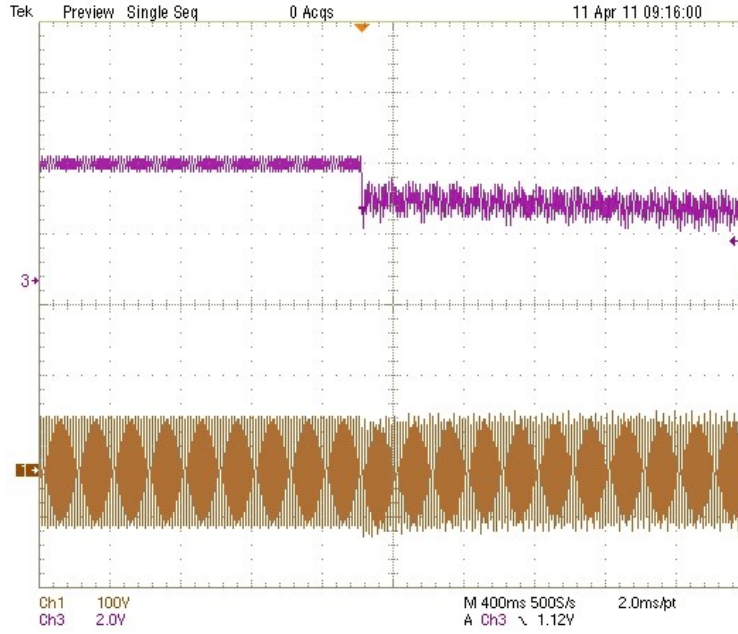


Fig. 4.72: PLL output under  $//R_L C_L$  load condition: phase voltage:  $v_{Ca}$  (maroon) [100V/DIV],  $\omega_C$  (purple) [2.5Hz/DIV]

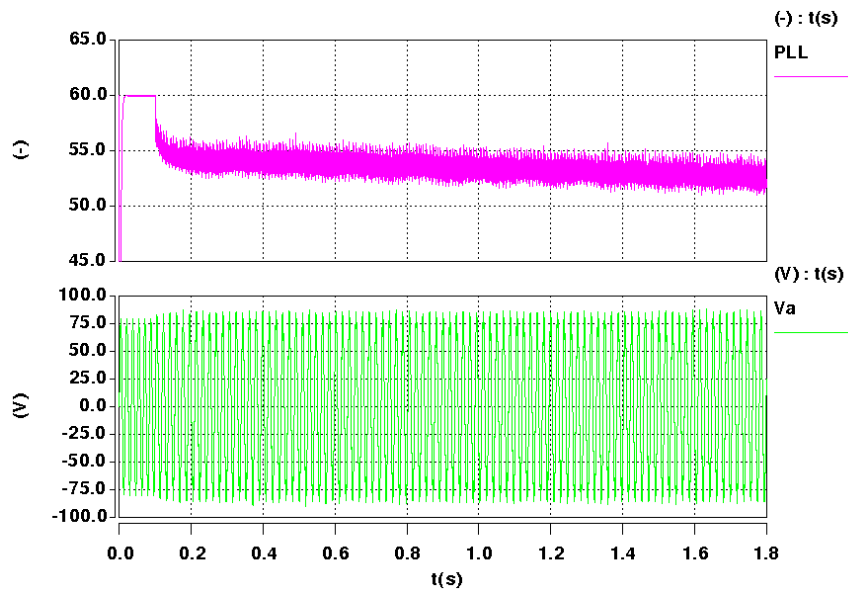


Fig. 4.73: PLL output under  $//R_L C_L$  load condition in simulation: phase voltage  $v_{Ca}$  (green) [100V/DIV],  $\omega_C$  (purple) [5Hz/DIV]

Fig. 4.74 and Fig. 4.75 show the PLL outputs with the inductive load under islanded conditions in experiment and simulation, respectively. In these cases, the output drifts up to infinity.

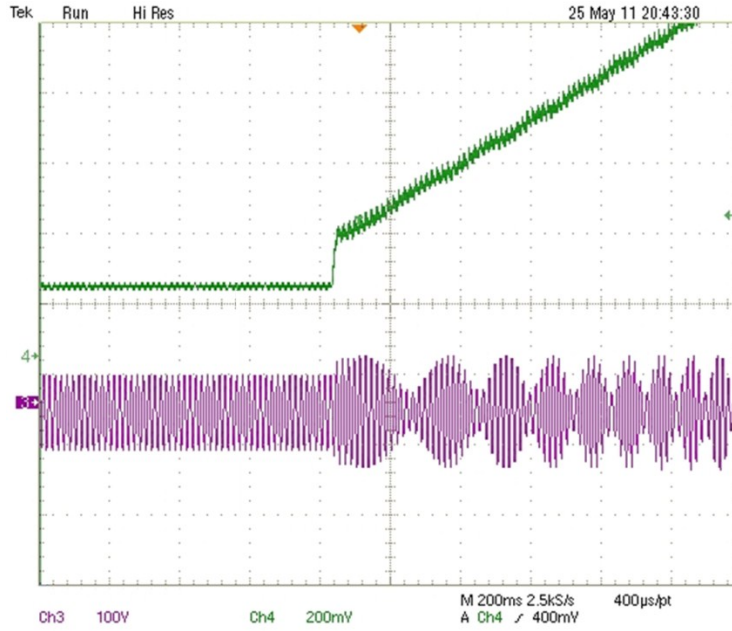


Fig. 4.74: PLL output under  $//R_L L_L$  load condition: phase voltage:  $v_{Ca}$  (purple) [100V/DIV],  $\omega_C$  (green) [5Hz/DIV]

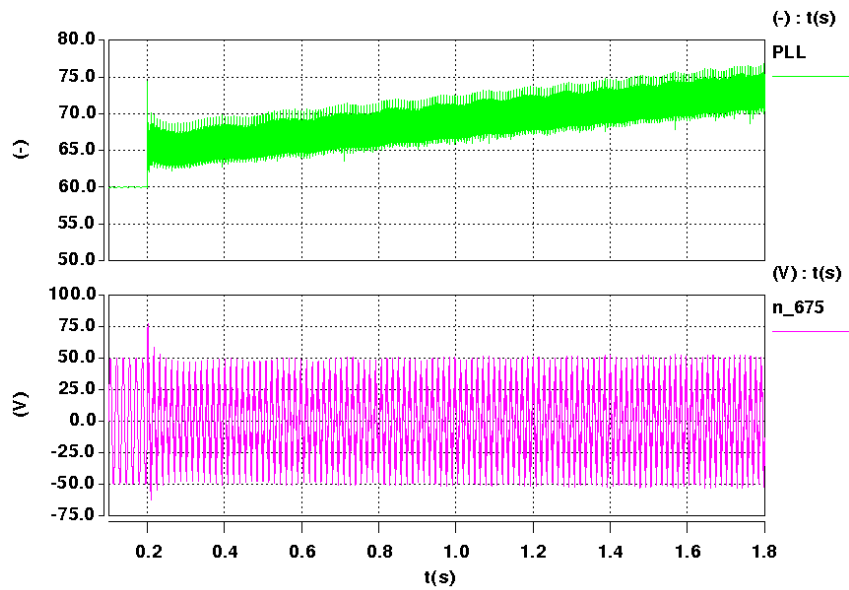


Fig. 4.75: PLL output under  $//R_L L_L$  load condition in simulation: phase voltage:  $v_{Ca}$  (purple) [100V/DIV],  $\omega_C$  (green) [5Hz/DIV]

Fig. 4.76 shows the PLL output with the  $//R_L L_L C_L$  load under the islanded conditions in the experiment.

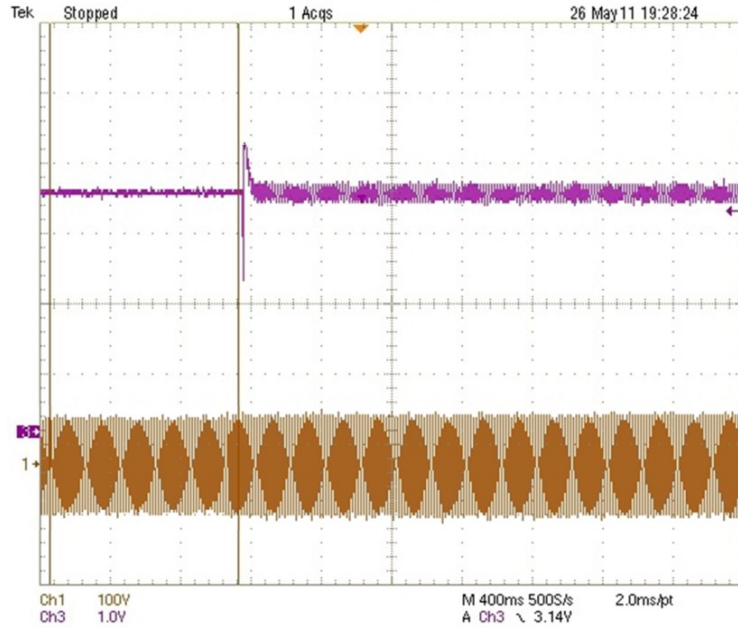


Fig. 4.76: PLL output under  $//R_L C_L L_L$  load condition: phase voltage:  $v_a$  (maroon) [100V/DIV],  $\omega_C$  (purple) [5Hz/DIV]

#### 4.2.3.4. Conclusion

This section comprehensively analyzed the grid-synchronization behavior at the islanded condition. It shows that different local-loads result in different behavior, and the  $//RLC$  load can stabilize the output frequency at the resonant frequency. All of these results can be used to study islanding detection in the next chapter.

### 4.2.4. LOW-FREQUENCY SMALL-SIGNAL ANALYSIS OF GRID SYNCHRONIZATION

#### 4.2.4.1. Introduction

The previous discussions analyzed the PLL behaviors at the weak grid and the islanded condition. However, some of questions still cannot be explained by the proposed non-linear quasi-static model. For example, the previous results showed that the PLL output tends to approach the local-load resonant frequency with a  $//RLC$  load at the islanded condition. How to demonstrate this conclusion mathematically? The previous analysis presented the converter system frequency behavior under the  $//RLC$  load condition, and extended the discussion to  $R, L, C$  conditions. How to extend the results to any passive load conditions?

The small-signal analysis at an equilibrium point is a useful tool to understand the dynamic behavior of a non-linear system. Many of the above questions actually can be

explained by such tool. Therefore, this section will focus on the small-signal analysis of the grid-synchronization in the ac-dc bus-interface converter system.

#### 4.2.4.2. Generic Small-signal Model

The small-signal PLL model under a purely resistive load at the islanded condition can be directly obtained as shown in Fig. 4.77 since it is a linear system. The transfer function from perturbation  $\theta_{pert}$  to output  $\omega_C$  is shown in (53). Due to the integrator, this reveals a marginal stable system which explains why the additional delay can drive away the PLL output.

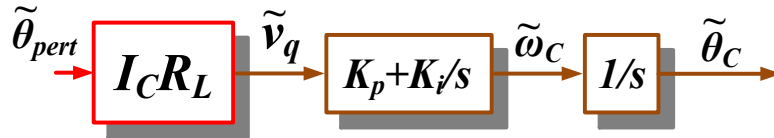


Fig. 4.77: Small-signal PLL model under pure resistor load at islanded condition

$$\frac{\tilde{\omega}_C}{\tilde{\theta}_{pert}} = I_C R_L \frac{K_p s + K_i}{s} \quad (53)$$

Generally, the proposed quasi-static PLL model shown in Fig. 4.39 can be linearized around an equilibrium operating point, e.g.,  $\omega_{op}$ .  $\tilde{\omega}_C$  is the small-signal frequency deviation at the equilibrium operating point. The large-signal positive feedback terms are linearized as shown in (54) and (55).

$$\begin{aligned} K_2(\omega_C) &= K_2(\omega_{op}) + k_z \times (\omega_C - \omega_{op}) \\ &= K_2(\omega_{op}) + k_z \times \tilde{\omega}_C \end{aligned} \quad (54)$$

$$\begin{aligned} \sin[\varphi_2(\omega_C)] &= \sin[\varphi_2(\omega_{op}) + k_\varphi \times (\omega_C - \omega_{op})] \\ &= \sin(\varphi_2(\omega_{op})) + \cos(\varphi_2(\omega_{op})) \times k_\varphi \times \tilde{\omega}_C \\ &\approx \varphi_2(\omega_{op}) + k_\varphi \times \tilde{\omega}_C \end{aligned} \quad (55)$$

$k_z$  and  $k_\varphi$  are the small-signal linearized gains at the operation point, as shown in (56) and (57).

$$k_z = \left. \frac{\partial K_2}{\partial \omega_C} \right|_{\omega_C = \omega_{op}} \quad (56)$$

$$k_\varphi = \left. \frac{\partial \varphi_2}{\partial \omega_C} \right|_{\omega_C = \omega_{op}} \quad (57)$$

The large-signal negative feedback terms in Fig. 4.39 can be linearized as well. The equation (58) is simplified by assuming the grid-frequency to be constant.

$$\begin{aligned}
 K_1(\omega_g) &= K_2(\omega_{op}) + k_g \times (\omega_g - \omega_{op}) \\
 &= K_2(\omega_{op}) + k_g \times \tilde{\omega}_g \\
 &= K_2(\omega_{op})
 \end{aligned}
 \tag{58}$$

The sinusoidal function small-signal gain  $k_{sin}$  in PD has to be considered as the operating point ( $\theta_g - \theta_C = \theta_\Delta$ ) may not stay at zero. As shown in Fig. 4.78, this gain is shown in (59).

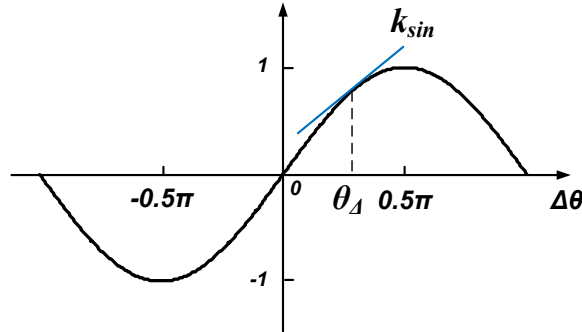


Fig. 4.78: Small-signal gain of the sinusoidal function

$$k_{sin} = \cos(\theta_\Delta) \tag{59}$$

If ignoring the product of small-signals, Fig. 4.79 shows the proposed small-signal PLL model around the operating point.

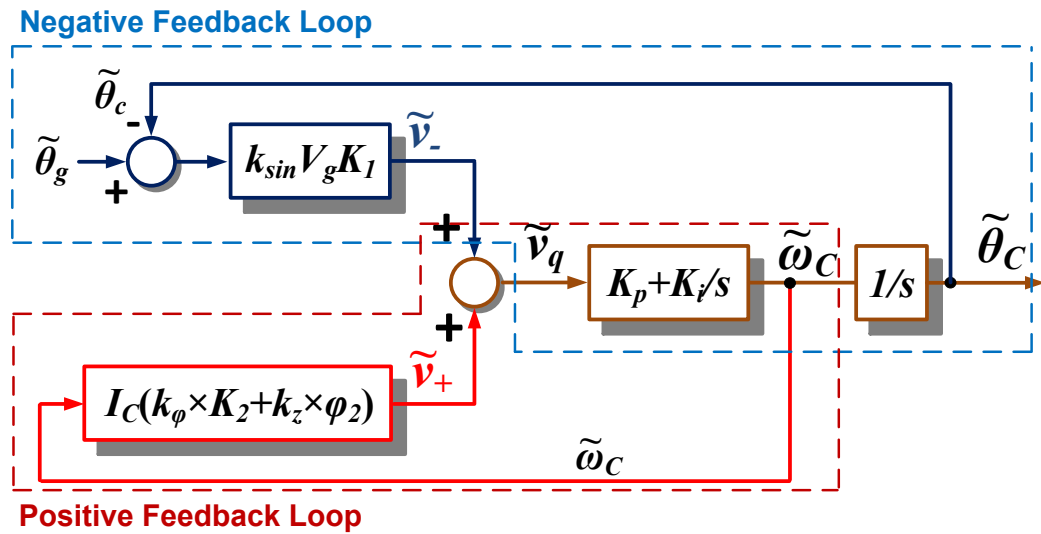


Fig. 4.79: Proposed low-frequency small-signal PLL model

As mentioned above, the phasor representation is valid at frequencies much lower than the line frequency, within the bandwidth of the PLL. Thus, the linearized gains of the phasor values are also valid only when the small-signal frequency deviation dynamics

are slow. This is essentially a low-frequency small-signal model which, however, is sufficient to help understand the characteristic of the operation point.

In order to verify this small-signal model, a measurement setup is performed in simulation, as shown in Fig. 4.80. The converter system supplies 50 A<sub>pk</sub> to a //RC (2 Ω//87.95μF) load under the grid-tied condition with a resistor  $R_g = 10 \Omega$  as the grid impedance, and the PLL PI values are  $K_p = 1.5$ ,  $K_i = 3$ .

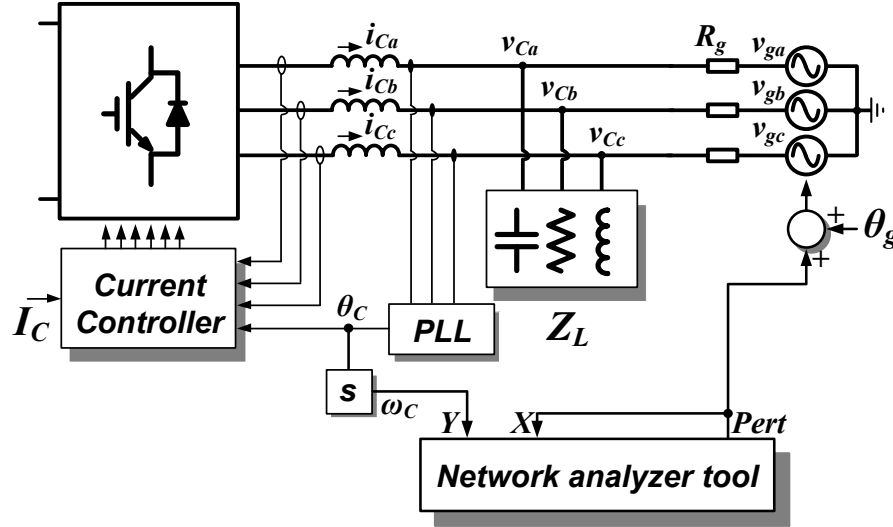


Fig. 4.80: Simulation verification of grid synchronization small-signal model at weak grid

The model gives the following parameters in (60) and (61).

$$\omega_{op} = 2\pi 60 \quad (60)$$

$$\left\{ \begin{array}{l} K_1 = \frac{R_L}{\sqrt{(R_L + R_g)^2 + (R_L R_g \omega_{op} C_L)^2}} \\ K_2 = \frac{R_{pp}}{\sqrt{1 + (\omega_{op} R_{pp} C_L)^2}} \\ \varphi_2 = -\arctan(\omega_{op} R_{pp} C_L) \\ k_\varphi = -\frac{R_{pp} C_L}{1 + (\omega_{op} R_{pp} C_L)^2} \\ k_z = -\frac{C_L^2 R_{pp}^3 \omega_{op}}{[(\omega_{op} R_{pp} C_L)^2 + 1]^{\frac{3}{2}}} \\ k_{\sin} = \cos(\theta_\Delta) \end{array} \right. , R_{pp} = \frac{R_L R_g}{R_L + R_g} \quad (61)$$

The operating point  $\theta_\Delta$  can be obtained by solving the power balance equations according to Fig. 4.81.

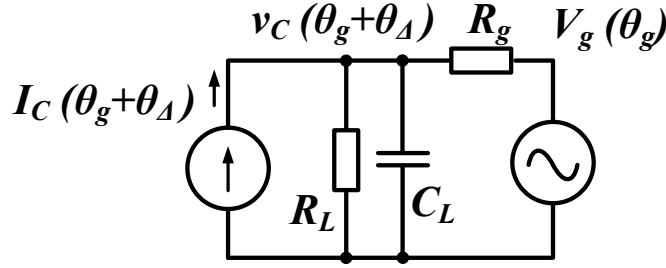


Fig. 4.81: Steady-state operation of converter at weak grid

$$\begin{cases} V_g \sin(\theta_\Delta) = \omega_{op} C_L V_C R_g \\ V_g \cos(\theta_\Delta) = V_C + R_g \left( \frac{V_C}{R_L} - I_C \right) \end{cases} \quad (62)$$

Upon obtaining all the parameters needed in Fig. 4.79, the small-signal transfer-function at  $\omega_C = \omega_{op}$  is obtained in (63).

$$\frac{\tilde{\omega}_C}{\tilde{\theta}_g} = \frac{k_{\sin} V_g K_1 G}{1 + k_{\sin} V_g K_1 G \frac{1}{s}}, \text{ where } G = \frac{K_p + K_i \frac{1}{s}}{1 - I_C (k_\phi Z_2 + k_z \varphi_2) \left( K_p + K_i \frac{1}{s} \right)} \quad (63)$$

As shown in Fig. 4.80, this model can be verified by using the developed injection and measurement tool in MATLAB to inject a perturbation signal into the phase of the grid-voltage and measure the signal of  $\omega_C$  from 0.01 Hz to 10 Hz.

In Fig. 4.82, the simulation measurement result ( $\omega_C/\theta_g$ ) is shown in the blue curve and the model gives the red curve. It reveals that the proposed small-signal model matches with the measurement result.



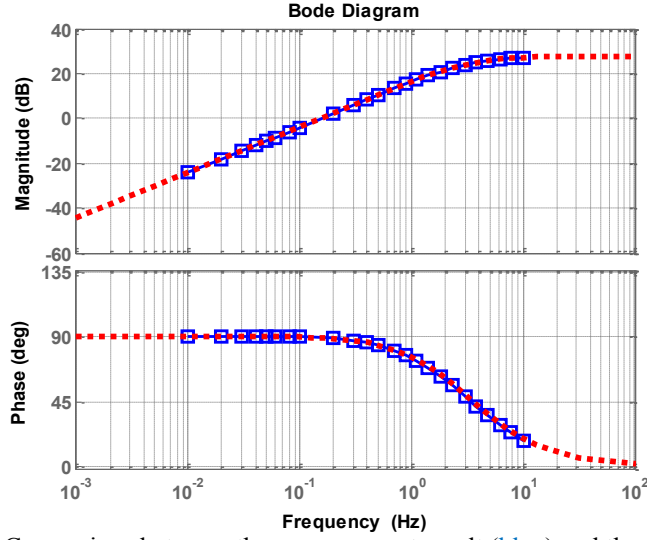


Fig. 4.82: Comparison between the measurement result (blue) and the model (red)

#### 4.2.4.3. Small-signal Model at Islanded Conditions

If the local-load  $Z_L$  is a  $//RLC$  load, the small-signal PLL model around the equilibrium operating point  $\omega_r$  can be obtained based on Fig. 4.57. As such, the following equations are obtained.

$$\omega_{op} = \omega_r \quad (64)$$

$$\left\{ \begin{array}{l} k_z = \frac{\partial}{\partial \omega_C} \left( \arctan \left[ Q \left( \frac{\omega_r^2 - \omega_C^2}{\omega_C \omega_r} \right) \right] \right) \Big|_{\omega_C = \omega_r} \\ k_\phi = \frac{\partial}{\partial \omega_C} \left( \frac{R_L}{\sqrt{1 + Q^2 \left( \frac{\omega_C - \omega_r}{\omega_r} \right)^2}} \right) \Big|_{\omega_C = \omega_r} \end{array} \right. \quad (65)$$

$$\left\{ \begin{array}{l} K_2(\omega_r) = R_L \\ \varphi_2(\omega_r) = 0 \end{array} \right. \quad (66)$$

Equation (65) can be further simplified as shown in (67).

$$\left\{ \begin{array}{l} k_z = 0 \\ k_\phi = -\frac{2Q}{\omega_r} \end{array} \right. \quad (67)$$

Then, the small-signal PLL model at the islanded condition can be further simplified as shown in Fig. 4.83.

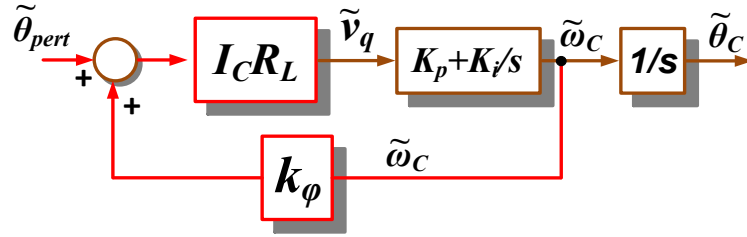


Fig. 4.83: Low-frequency small-signal PLL model at the islanded condition

The transfer function in (68) and the closed-loop pole in (69) can be easily drawn from this small-signal PLL model.

$$\frac{\tilde{\omega}_{out}}{\tilde{\theta}_{pert}} = \frac{I_C R_L}{1 - I_C R_L K_p k_\phi} \frac{s K_p + K_i}{\left( s - \frac{I_C R_L K_i k_\phi}{1 - I_C R_L K_p k_\phi} \right)} \quad (68)$$

$$\omega_{pole} = \frac{I_C R_L K_i k_\phi}{1 - I_C R_L K_p k_\phi} \quad (69)$$

This is a very low-frequency pole under a low  $Q$  condition, much lower than the bandwidth of PLL. Since  $k_\phi < 0$ , the PLL essentially only has one small-signal negative feedback loop, and this closed-loop pole always stays at the left-half-plane. So, the PLL is stable at this equilibrium point, which simply means that when an islanding condition occurs, the PLL output tends to approach  $\omega_r$ , and stay at  $\omega_r$  even with the perturbation due to the nature of negative feedback.

In order to verify this small-signal model, a measurement setup is performed in simulation, as shown in Fig. 4.84. The converter system supplies 50 A<sub>pk</sub> to a //RLC (2 Ω//80 mH// 87.95μF) load under the islanded condition, and the PLL PI values are  $K_p = 2$ ,  $K_i = 5$ . The developed injection and measurement tool in MATLAB injects a perturbation signal into  $v_q$  and measures the signal of  $\omega_c$  from 0.01 Hz to 10 Hz. In Fig. 4.85, the simulation measurement result ( $\omega_c/v_q$ ) matches with the model.

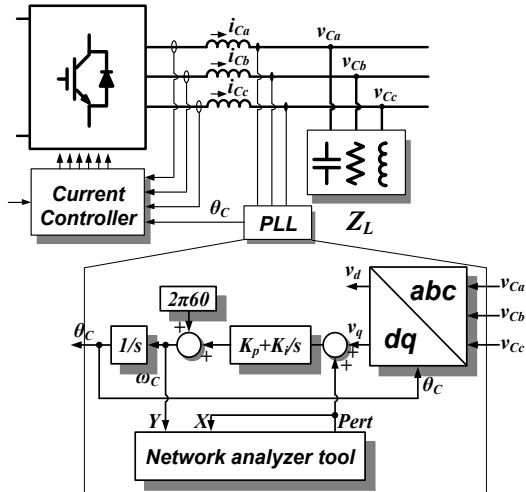


Fig. 4.84: Illustration of small-signal measurement

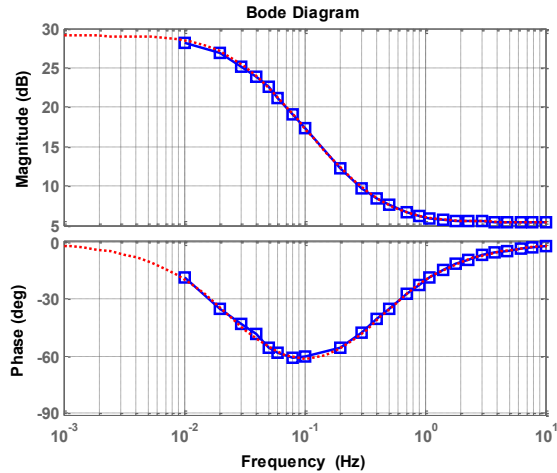


Fig. 4.85: Comparison between the measurement result (blue) and the model (red)

The above analysis shows that the small-signal phase shift term  $k_\varphi$  is critical for evaluating the characteristics of the PLL equilibrium point. The value of  $k_\varphi$  can also be obtained by checking the 2-D figure of  $\varphi_2$  in terms of  $\omega_C$ , which is shown above in Fig. 4.62. Similarly  $k_Z$  can be also obtained by checking the 2-D figure of  $K_2$  in terms of  $\omega_C$ , which is shown in Fig. 4.60.

Therefore, for any type of linear load, the PLL behavior can be directly evaluated by simply observing the off-line impedance. The two steps for evaluating PLL behavior are:

1. Find the equilibrium point: The PLL equilibrium point is the frequency at which phase of the impedance equals zero.
2. Find the sign of  $k_\varphi$ : Directly check the slope of the phase of the impedance around the equilibrium point. If  $k_\varphi$  is positive, it is an unstable equilibrium point, while if  $k_\varphi$  is negative, it is a stable equilibrium point.

For example, Fig. 4.86 shows an impedance measurement of a //RLC load. It is easily to find that there is one equilibrium point where the phase equals zero, which is exactly the resonant frequency. Also, the  $k_\varphi$  is a negative value, which can be obtained by checking the slope of the phase around the equilibrium point.

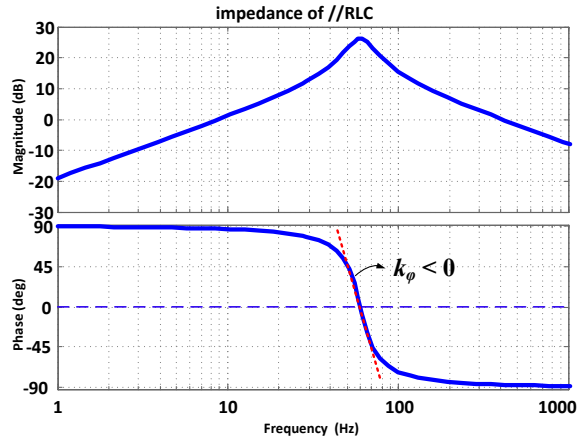


Fig. 4.86: Impedance of a //RLC linear-load

Another example shows an impedance measurement of a  $RLC$  load in series. It is seen from Fig. 4.87 that the resonant frequency is still an equilibrium point, and  $k_\phi$  is positive around the equilibrium point. This means that, for a series  $RLC$  load, the resonant frequency is an unstable equilibrium point, and the PLL output drifts out of the resonant frequency as soon as an islanding event occurs.

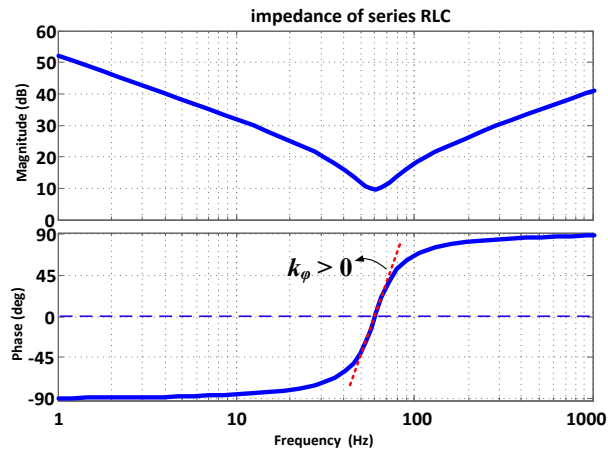
Fig. 4.87: Impedance of a series  $RLC$  load

Fig. 4.88 shows the impedance of a purely resistive load. It shows that the phase of the resistor is zero throughout the frequency. So, any frequency can be the critical equilibrium point.

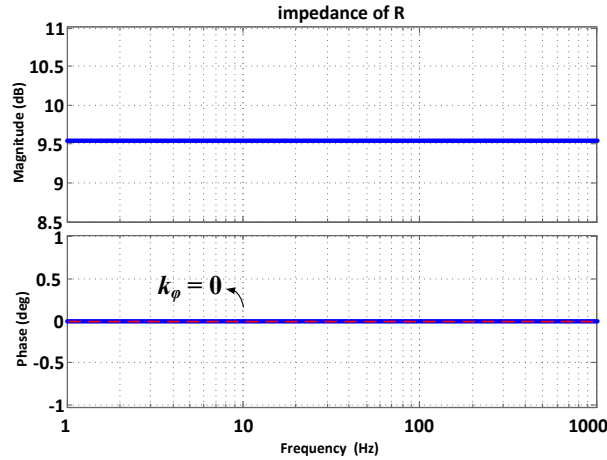


Fig. 4.88: Impedance of a pure resistor load

The capacitor and the inductor load, as shown in Fig. 4.89 and Fig. 4.90, don't have any equilibrium points, so the PLL output will drift to zero and infinity, respectively.

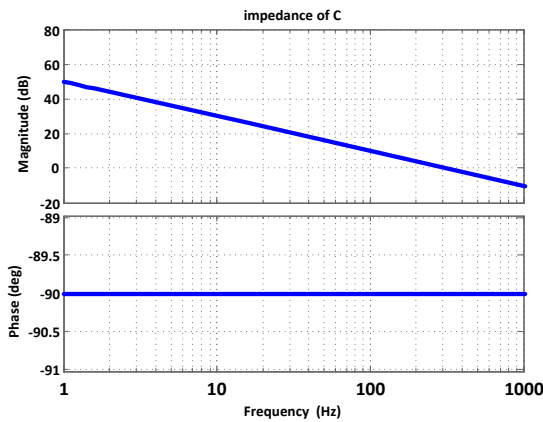


Fig. 4.89: Impedance of a pure capacitor load

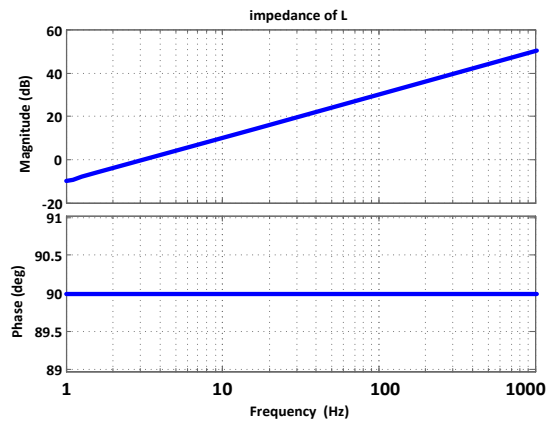


Fig. 4.90: Impedance of a pure inductor load

The above figures show that for the  $//RLC$  load defined in IEEE 1547, its resonant frequency is a stable equilibrium point for PLL. In other words, if the power drawn by  $//RLC$  load is exactly the same as delivered by the converter unit, when an islanding condition occurs, the whole system will still operate normally and both the output current, terminal voltage and frequency stay the same. In this case, the converter itself cannot detect whether the whole system operates in the islanded condition or in the grid-tied mode.

#### 4.2.4.4. Conclusion

The small-signal analysis of the grid synchronization at both the weak grid and the islanded condition are given. The modeling concept, procedure, and verification are given.

The small-signal model at the islanded condition helps determine the stability of operating point, and the PLL behavior and stability at any passive local-load can be obtained from the proposed small-signal model.

### **4.3. GRID SYNCHRONIZATION MODELING FOR MULTI-CONVERTER CONDITION**

#### **4.3.1. INTRODUCTION**

The previous section presents an extensive analysis of the single bus-interface converter output frequency behavior. A straightforward question would be: “what would be the results if there were two or more bus-interface converters connected in parallel with the grid.” Answering this question is critical to evaluate any grid synchronization strategies [222] and the related control methods [223, 224] in the ac micro-grid/nano-grid where lots of DG converters are tied to the grid.

Moreover, the answer to this question can further help us understand the potential small-signal interaction issues among PLLs at weak grid conditions and eventually help engineers develop the design rules for a multi-converter system. For example, in a future power system, hundreds of EVs could be connected to the grid in a very limited space, and their grid synchronization “talk” to each other, which might result in the instability of the system.

#### **4.3.2. MULTIPLE-CONVERTER SYSTEM AT ISLANDED CONDITIONS**

In order to simplify the study, this discussion begins with a islanded system connected by two converters that are close to each other, as shown in Fig. 4.91.

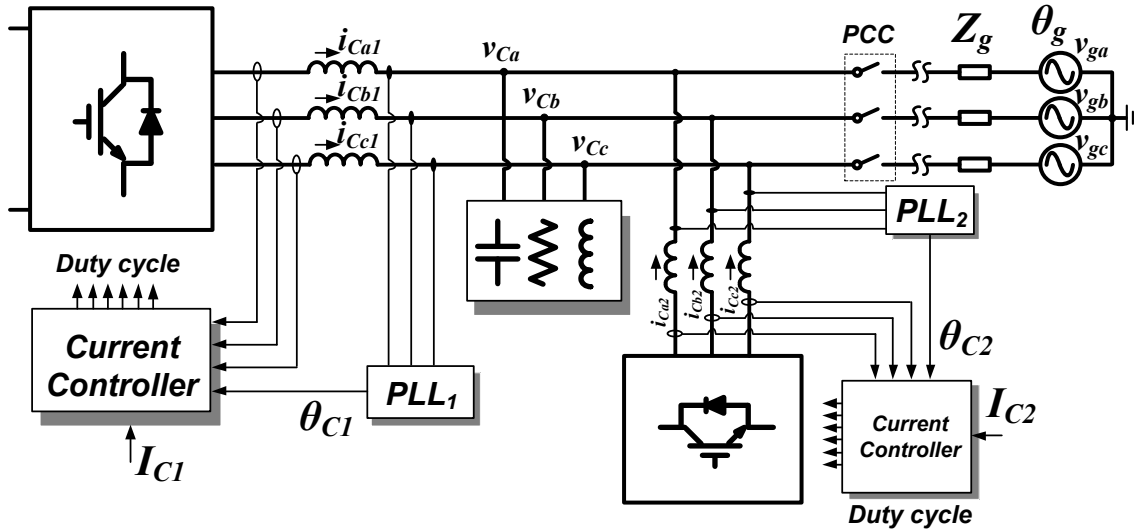


Fig. 4.91: Two bi-directional ac-dc bus-interface converters in system

A switching model simulation is conducted by using the parameters shown in Table 4.9.  $K_p$  and  $K_i$  are the proportional and integrator gains in two PLL LFs.  $I_{C2} = -50 \text{ A}_{pk}$  means converter 2 operates as the rectifier mode, or it can be regarded as a active front-end rectifier (AFE) load. As shown in Fig. 4.92, both converters' PLL output frequencies start drifting downward when an islanding condition occurs, indicating an unstable case which doesn't appear under single bus-interface converter conditions. This unique result indicates that the grid synchronization dynamics do change at the multi-converter condition.

Table 4.9: Simulation Parameters for two bus-interface converters

$f_o$	$f_s$	$I_{C1}$	$I_{C2}$	$Z_L$	$K_{p1}, K_{i1}$	$K_{p2}, K_{i2}$
60 Hz	20 kHz	100 $\text{A}_{pk}$	-50 $\text{A}_{pk}$	2 $\Omega$	1, 5	1, 1

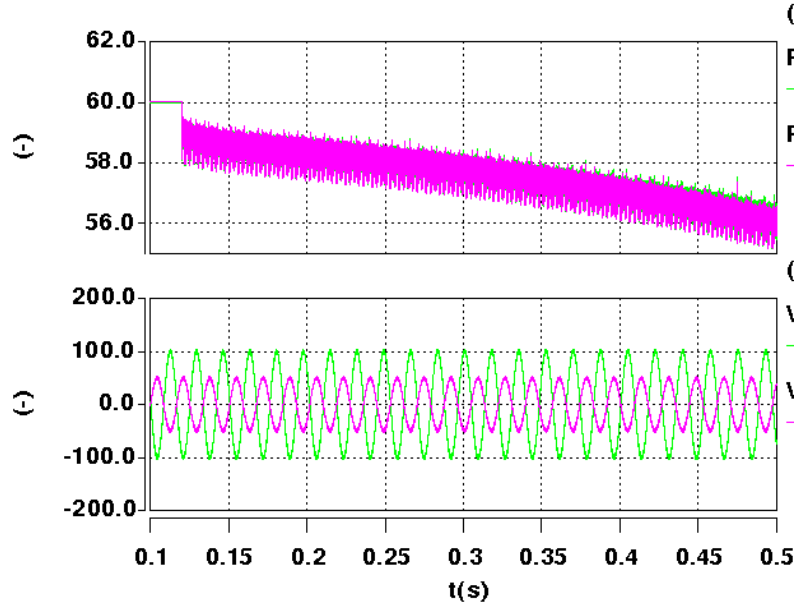


Fig. 4.92: Two PLLs' unstable output with two bus-interface converters:  $\omega_{C1}/2\pi$  (green),  $\omega_{C2}/2\pi$  (magenta) [2 Hz/DIV],  $I_{Ca1}$  (green),  $I_{Ca2}$  (magenta) [100 A/DIV]

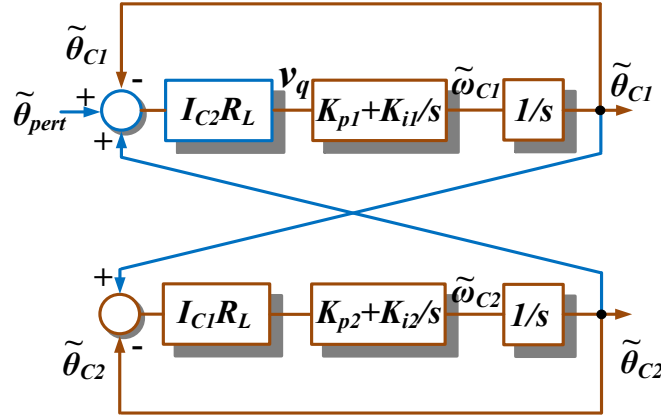


Fig. 4.93: Two PLLs are fully coupled together at a purely resistive load islanded condition

As shown in Fig. 4.93, the PLL model at the islanded condition can be used to study this simple case. This model is obtained by following the superposition principle. Each converter's phase output is a reference to the other's. The transfer function of the No.1 PLL is derived in (70), which shows two poles and one integrator.

$$\frac{\tilde{\omega}_{C1}}{\tilde{\theta}_{pert}} = \frac{s\tilde{\theta}_{C1}}{\tilde{\theta}_{pert}} = \frac{I_{c2}R_L(sK_{p1} + K_{i1})[s^2 + sI_{c1}R_LK_{p2} + I_{c1}R_LK_{i2}]}{s[s^2 + s(I_{c2}K_{p1} + I_{c1}K_{p2})R_L + (I_{c2}K_{i1} + I_{c1}K_{i2})]} = \frac{N(s)}{s(s - \omega_{p1})(s - \omega_{p2})} \quad (70)$$

$$\omega_{p1,2} = -\frac{R_L}{2} \left[ (I_2K_{p1} + I_1K_{p2}) \pm \sqrt{(I_2K_{p1} + I_1K_{p2})^2 - 4(I_2K_{i1} + I_1K_{i2})} \right] \quad (71)$$

The following conclusions can be inferred from (71):



If both converters deliver the power ( $I_{C1} > 0, I_{C2} > 0$ ), the two poles are located on the left-half-plane, and the PLL behavior is similar to the behavior in the single-converter case.

If both converters have the same PLL PI values, the two poles will be canceled by the two zeros in  $N(s)$ , and (71) will be reduced to (53). The two converters can be regarded as a single converter.

If the power directions of two converters are different, the poles in (71) might be located on the right-half-plane (RHP) at some PI values. If so, the PLL outputs are unstable at the islanded condition.

This discussion can then be extended to a two-converter system with the  $//RLC$  local-load at the islanded condition. As seen in Fig. 4.94, the two small-signal PLL loops (around  $\omega_r = 2\pi 60$  rad/s) are fully coupled to each other via the system impedance, and it is more complicated than the  $R$  case. Additional positive feedback loops, due to the resonance of the load, show up in each PLL loop. Since the two converters share the same system impedances,  $k_{\phi 1} = k_{\phi 2} = k_{\phi}$  at the same operating point. This system can be simplified as in Fig. 4.95, where  $G_1$  and  $G_2$  are shown in (72). The transfer function of PLL1 is shown in (73), and it is found that the denominator  $D(s)$  includes three poles.

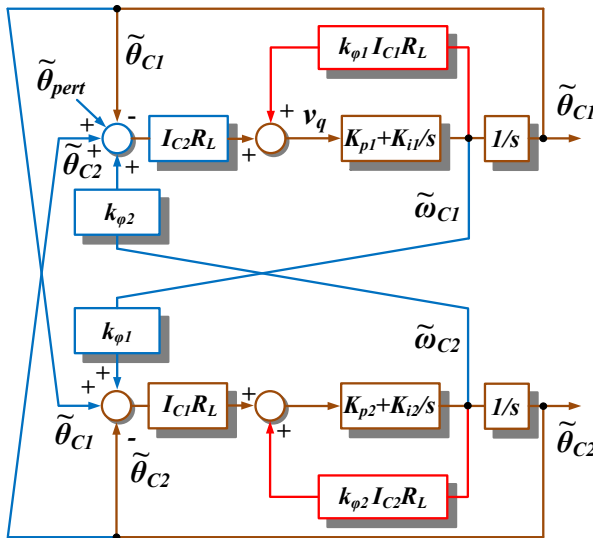


Fig. 4.94: Two PLLs are fully coupled together under  $//RLC$  load islanded condition

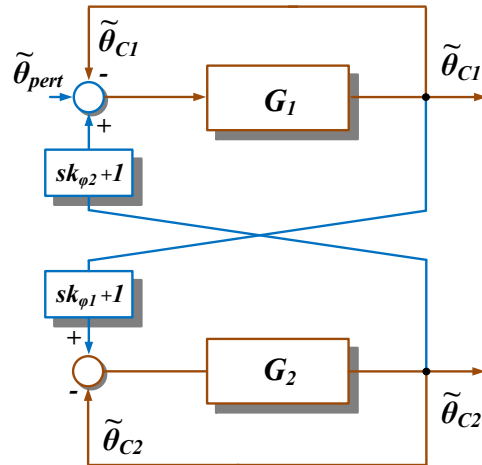


Fig. 4.95: Simplified PLL loop under  $//RLC$  load islanded condition

$$\left\{ \begin{array}{l} G_1 = \frac{1}{s} I_{C2} R_L \frac{K_{p1} + K_{i1} \frac{1}{s}}{1 - k_\phi I_{C1} R_L \left( K_{p1} + K_{i1} \frac{1}{s} \right)} \\ G_2 = \frac{1}{s} I_{C1} R_L \frac{K_{p2} + K_{i2} \frac{1}{s}}{1 - k_\phi I_{C2} R_L \left( K_{p2} + K_{i2} \frac{1}{s} \right)} \end{array} \right. \quad (72)$$

$$\frac{\tilde{\omega}_{C1}}{\tilde{\theta}_{pert}} = \frac{s \tilde{\theta}_{C1}}{\tilde{\theta}_{pert}} = \frac{s \frac{G_1}{1+G_1}}{1 - \frac{G_1}{1+G_1} \frac{G_2}{1+G_2} (s k_\phi + 1)^2} = \frac{N(s)}{D(s)} = \frac{N(s)}{(s - \omega_{p1})(s - \omega_{p2})(s - \omega_{p3})} \quad (73)$$

If three of the poles are located on left-half-plane, the PLL system is stable and its behavior is similar to that of a single converter case. The analytical expressions of three poles of this three-order system are extremely complicated, and the numerical method can be used.

In order to verify the model, a simulation in Fig. 4.96 is established by randomly picking up parameters shown in Table 4.10. The results from the small-signal measurement and the model are shown in Fig. 4.97. The results match to each other.

Table 4.10: Simulation parameters for two bus-interface converters with //RLC load

$f_o$	$I_{C1}$	$I_{C2}$	$Z_L$	$K_{p1}, K_{i1}$	$K_{p2}, K_{i2}$
60 Hz	70 A <sub>pk</sub>	-20 A <sub>pk</sub>	2 Ω//80 mH//87.95 μF	0.1, 1	1, 1

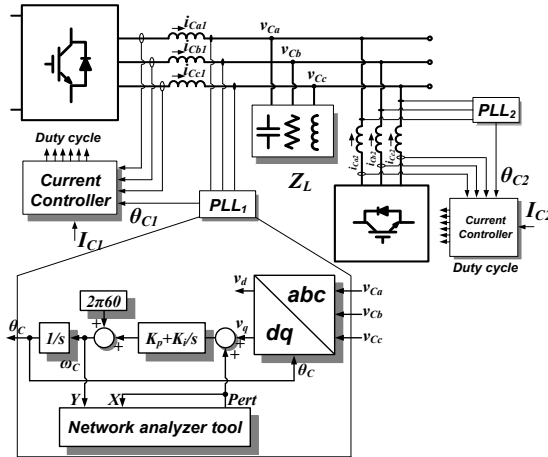


Fig. 4.96: Illustration of small-signal measurement at two-converter case with  $//RLC$  load at the islanded condition.

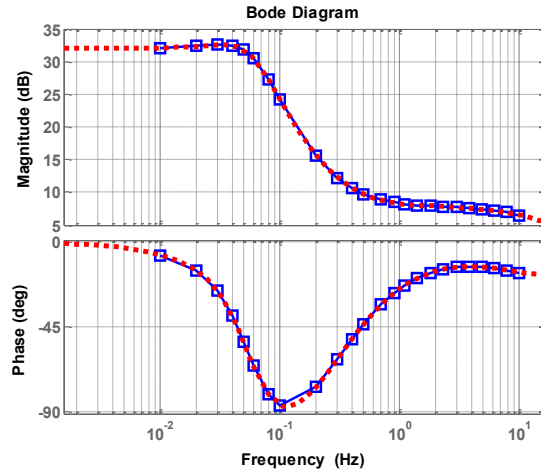


Fig. 4.97: Comparison between the measurement result (blue) and the model (red).

Another four examples using different parameters are shown in Table 4.11 to illustrate how the PLL stability can be predicted by the loci of the three poles.

The corresponding PLL output simulation results are shown in Fig. 4.98 to Fig. 4.101. The denominator in case 1 shows an unstable double-pole (0.227 rad/s), and the simulation result in Fig. 4.98 shows an unstable oscillation at 0.274 rad/s, which is close to the prediction. In case 2, the denominator shows a very fast single-pole (214.5 rad/s), and the simulation result in Fig. 4.99 shows a very fast unstable behavior. In case 3, the denominator shows two slow single-poles, and Fig. 4.100 shows a slow exponential drift behavior. Case 4 shows a stable case revealing a stable double-pole (0.7154 rad/s) matching with the damped oscillation behavior (0.737 rad/s) in the simulation in Fig. 4.101.

Table 4.11: Four examples for two-converters under  $//RLC$  islanded condition

	Simulation condition	Calculated Characteristics equation
Case 1	$//R_L L_L C_L = 2\Omega // 80\text{mH} // 87.95\mu\text{F}$ $K_{p1}=1, K_{i1}=2.5, K_{p2}=1, K_{i2}=1$ $I_{C1} = 100 \text{ A}_{pk}, I_{C2} = 50 \text{ A}_{pk}$	$D(s) = (s^2 - 0.3631s + 0.08454)(s + 100.5)$
Case 2	$//R_L L_L C_L = 2\Omega // 80\text{mH} // 87.95\mu\text{F}$ $K_{p1}=5, K_{i1}=2.5, K_{p2}=1, K_{i2}=1$ $I_{C1} = 100 \text{ A}_{pk}, I_{C2} = 50 \text{ A}_{pk}$	$D(s) = (s - 214.5)(s + 0.2231)(s - 0.1396)$
Case 3	$//R_L L_L C_L = 2\Omega // 10\text{mH} // 703.62\mu\text{F}$ $K_{p1}=1, K_{i1}=2.5, K_{p2}=1, K_{i2}=0.1$ $I_{C1} = 100 \text{ A}_{pk}, I_{C2} = 50 \text{ A}_{pk}$	$D(s) = (s + 102.3)(s - 1.15)(s - 0.04667)$
Case 4	$//R_L L_L C_L = 2\Omega // 80\text{mH} // 87.95\mu\text{F}$ $K_{p1}=1, K_{i1}=2.5, K_{p2}=1, K_{i2}=1$ $I_{C1} = 100 \text{ A}_{pk}, I_{C2} = 50 \text{ A}_{pk}$	$D(s) = (s^2 + 0.3712s + 0.5463)(s + 100.5)$

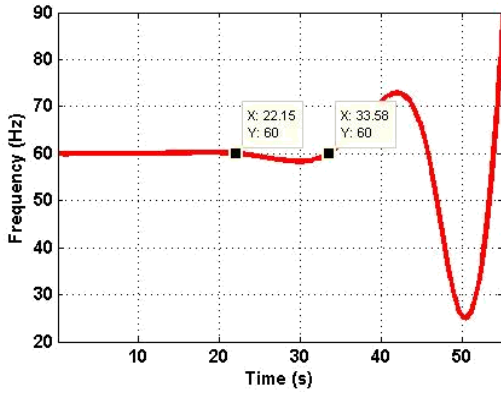


Fig. 4.98: PLL output for case 1

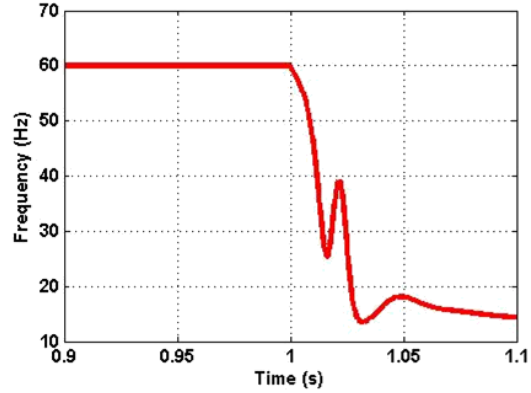


Fig. 4.99: PLL output for case 2

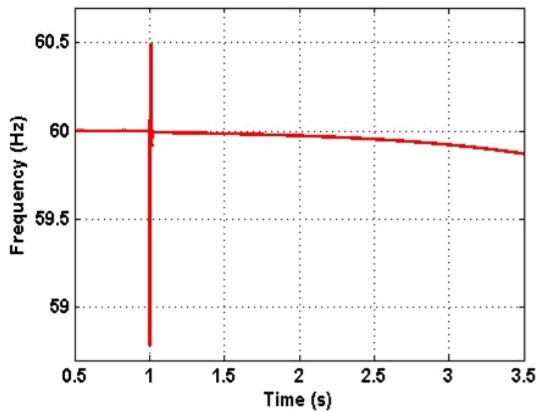


Fig. 4.100: PLL output for case 3

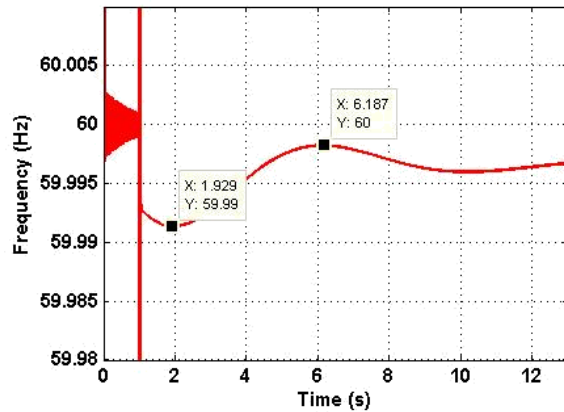


Fig. 4.101: PLL output for case 4

The results demonstrate that the PLL model helps predict the frequency behaviors of multiple-converter system at the islanded condition, which is a very useful tool for evaluating the performance of any frequency stability-based islanding detection methods, which will be discussed in Chapter 5.

Deriving the transfer function requires a tremendous effort and would be impossible for a large number of converters working together. Thus, a simple resolution is desired to generalize the result for any number of converters. Fig. 4.102 shows the No.1 PLL loop at a three-converter condition. The output phases of the other two converters  $\theta_{C2}$ ,  $\theta_{C3}$  are the input references. This block diagram can be simplified as Fig. 4.103, which uses the parameters shown in (74). Then, the signal-flow-graph (SFG) can be used as shown in Fig. 4.104 to represent the signals' relationship, where the dots and arrows indicate the signals and transfer functions, respectively.

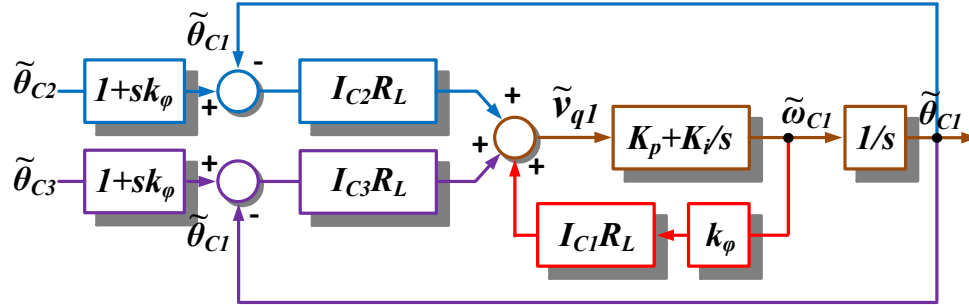


Fig. 4.102: PLL1 loop for a three-converter case

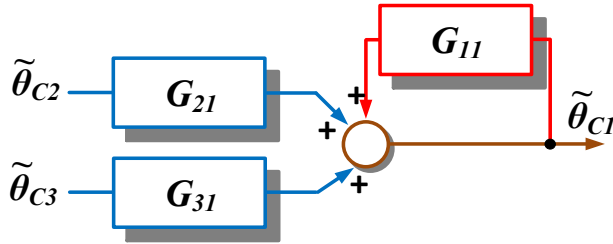


Fig. 4.103: Simplified PLL1 loop for a three-converter case

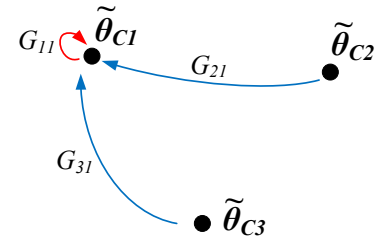


Fig. 4.104: Signal-flow-graph (SFG) representation of PLL1 loop

$$\left\{ \begin{aligned} G_{21} &= \left( \frac{1}{s} + k_\phi \right) I_{C2}R_L \frac{K_{p1} + K_{i1} \frac{1}{s}}{1 - k_\phi I_{C1}R_L \left( K_{p1} + K_{i1} \frac{1}{s} \right)} \\ G_{31} &= \left( \frac{1}{s} + k_\phi \right) I_{C3}R_L \frac{K_{p1} + K_{i1} \frac{1}{s}}{1 - k_\phi I_{C1}R_L \left( K_{p1} + K_{i1} \frac{1}{s} \right)} \\ G_{11} &= -\frac{G_{21} + G_{31}}{1 + sk_\phi} \end{aligned} \right. \quad (74)$$

As such, the transfer functions of the PLL loops in any number of converter case can be generalized in (75), where  $N$  is the total number of converters.

$$\begin{cases} G_{nm} = \left(\frac{1}{s} + k_\varphi\right) I_{Cn} R_L \frac{K_{pm} + K_{im} \frac{1}{s}}{1 - k_\varphi I_{Cn} R_L \left(K_{pm} + K_{im} \frac{1}{s}\right)}, n \neq m \\ G_{mm} = -\frac{1}{1 + sk_\varphi} \sum_{n=1}^N G_{nm} \end{cases} \quad (75)$$

The signals' relationship can be generalized as well by using the SFG. The number of signals depends on the number of converters. A three-converter case and a four-converter case are shown in Fig. 4.105 and Fig. 4.106, respectively.

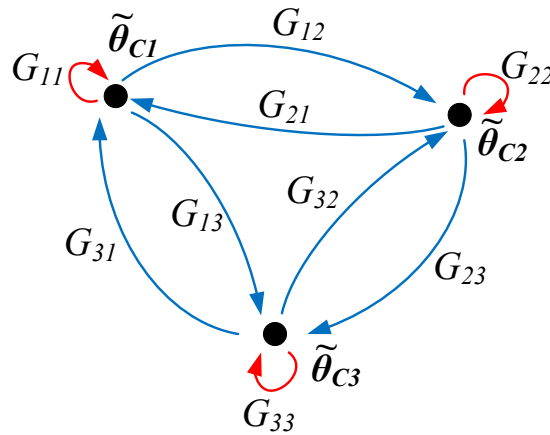


Fig. 4.105: SFG representation of PLL loop in three-converter case

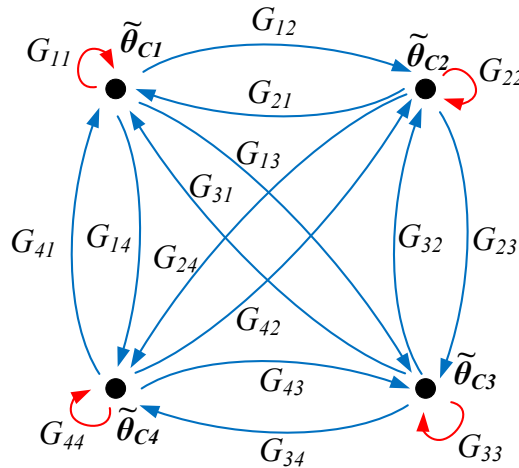


Fig. 4.106: SFG representation of PLL loop in four-converter case

Aside from its simplicity of showing the relationships between signals, SFG also provides a generic solution to derive the high-order system transfer function by following the Mason gain formula (MGF) as shown in (76).

$$G = \frac{y_{out}}{y_{in}} = \frac{\sum_{k=1}^N G_k \Delta_k}{\Delta} \quad (76)$$

$$\Delta = 1 - \sum L_i + \sum L_i L_j - \sum L_i L_j L_k + \dots + (-1)^m \sum \dots + \dots$$

where  $\Delta$  = the determinant of the graph.  $N$  = total number of forward paths between  $y_{in}$  and  $y_{out}$ .  $G_k$  = gain of the  $k^{\text{th}}$  forward path between  $y_{in}$  and  $y_{out}$ .  $L_i$  = loop gain of each closed loop in the system.  $L_i L_j$  = product of the loop gains of any two non-touching loops (no common nodes).  $L_i L_j L_k$  = product of the loop gains of any three pairwise non-touching loops.  $\Delta_k$  = the cofactor value of  $\Delta$  for the  $k^{\text{th}}$  forward path, with the loops touching the  $k_{\text{th}}$  forward path removed.

High-order system transfer functions thus can be obtained by using the computer-aided-system according to the rules of MGF. The PLL loop dynamics at the multi-converter condition can be used to study the frequency stability and also to evaluate the islanding detection methods.

### 4.3.3. MULTIPLE-CONVERTER SYSTEM AT WEAK GRID CONDITIONS

The next question is how the PLLs behave if a weak grid is present. Before answering the question, the following example shows a potential frequency stability issue at weak grid conditions, which has been ignored until now. As shown in Fig. 4.107, a manufacture factory located in a rural area is supplied by a 1 MW distribution transformer and a 1MW bus feeder from the distribution power grid. The factory owner needs more electricity energy due to the newly-installed 8 MW electric drives. To avoid bothering the utility to upgrade the grid distribution system, the owner thus installs PV panels, wind turbines, and energy storage and connects these to the factory via several power electronic inverters.

This example reflects the concept of the future distributed generation system or smart grid being promoted by governments. The basic idea is that the local energy consumption can be compensated by the local generation without massively upgrading the transmission/distribution infrastructure. The popular “zero net energy consumption” concept is also the immediate derivative of this idea. However, when the factory starts running all the loads, it is found that the output frequency of inverters starts oscillating and eventually the whole system collapses.

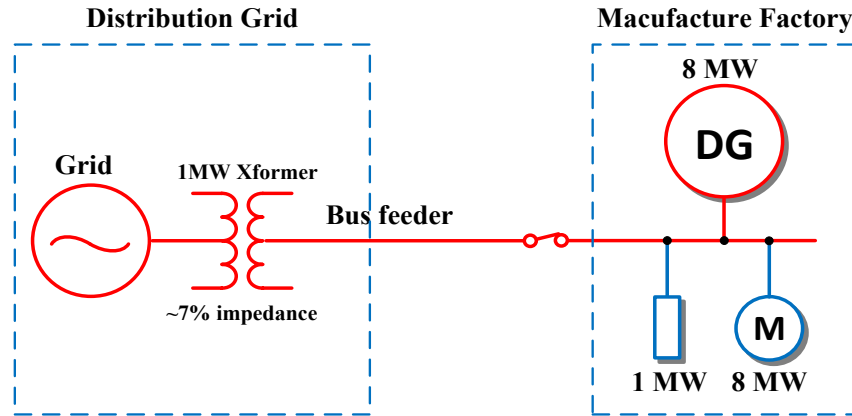


Fig. 4.107: An example of future local distribution generation system

This example can be simplified by using Fig. 4.91. Converter No. 1 represents all DG inverters, rated around 8 MW, the local-load  $Z_L$  are the original 1 MW load, and converter No. 2 represents the 8 MW electric drives with the active front-end rectifiers tied to the grid. The parameters used in this example are shown in Table 4.12. The three-phase grid impedance are around 7% of the base-impedance ( $10 \Omega$ ).

Table 4.12: Simulation parameters for two bus-interface converters

$f_o$	$V_g$	$I_{C1}$	$I_{C2}$	$Z_L$	$K_{p1}, K_{i1}$	$K_{p2}, K_{i2}$	$3\Phi Z_{xformer}$
60 Hz	100 V	85 A	-85 A	$10 \Omega // 87.95 \mu\text{F}$	0.1, 3.2	0.05, 0.5	$0.7 \Omega, 0.8 \Omega, 0.65 \Omega$

Fig. 4.108 shows both of the PLLs' unstable oscillation outputs when the grid impedances step from zero to the values in Table 4.12. The oscillation frequency is about 2 Hz, and a 120 Hz ripple is on top of it. This frequency instability issue should be considered by both power system and power electronics engineers. This instability issue will be even more severe under unbalanced load, harmonic polluted system conditions.



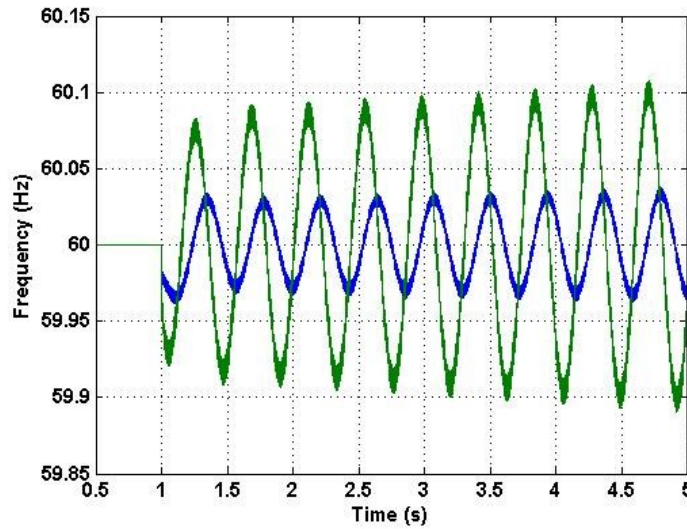


Fig. 4.108: Two converters' unstable output frequency at the weak grid condition

In order to predict this potential instability, the grid synchronization model in multi-converter case at the weak grid condition is needed. Last section has already showed the PLL small-signal model of single-converter at the weak grid condition. The information can be used here.

Similarly as the modeling of grid-synchronization in multi-converter case at the islanded condition, the small-signal model at the weak grid condition in two-converter case is shown in Fig. 4.109. Compared to the model of two-converter at the islanded condition, the loops contain the dynamics from the grid. The phase of grid is the input reference for both converters. In other words,  $v_q$  signal in each converter's PLL system consists of the contributions from itself (red), the other converter (blue), and the grid (purple).

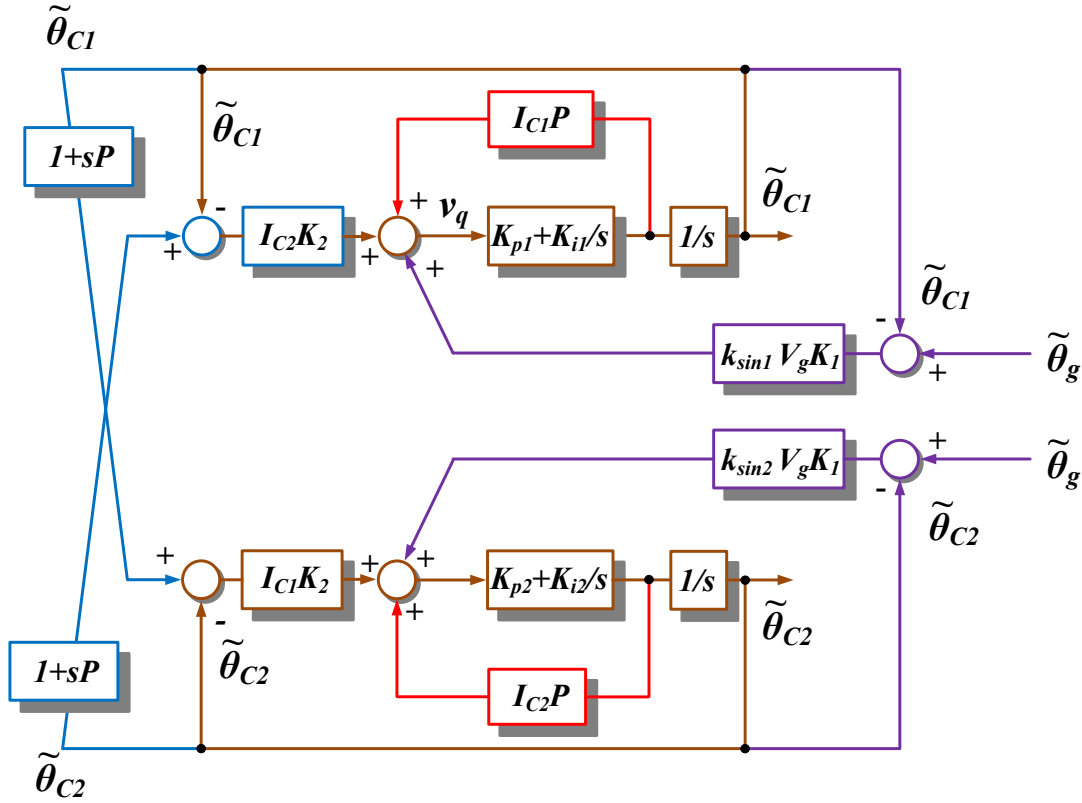


Fig. 4.109: Small-signal model of PLL in two-converter case at the weak grid condition

As a matter of fact, since both converters share the same system impedances,  $P_1 = P_2 = P$ ; since both converters synchronize the same connection point (there is no impedance between converters),  $\theta_g - \theta_{C1} = \theta_g - \theta_{C2} = \theta_\Delta$ . The parameters in this model are shown in (77).

$$\begin{cases} P_1 = P_2 = P = K_2 (\omega_{op}) k_\varphi + \varphi_2 (\omega_{op}) k_z \\ k_{\sin} = k_{\sin 1} = k_{\sin 2} = \cos(\theta_\Delta) \end{cases} \quad (77)$$

In this example,  $//R_L L_L$  and  $R_g$  are the local-load and grid impedance, which are the same condition as in Fig. 4.80. So, all parameters in Fig. 4.109 can be found in (61).

In order to find the steady-state operating point  $\theta_\Delta$ , this system can be simplified as Fig. 4.81, where  $I_C = I_{C1} + I_{C2}$ . Then, (62) can be also used here to find  $\theta_\Delta$ . The average value (0.716  $\Omega$ ) is picked up as  $R_g$ .

The signals' relationships can then be illustrated by SFG, as shown in Fig. 4.110, and the parameters are shown in (78). The transfer function of PLL1 can be obtained easily by following MGF, as shown in (79).

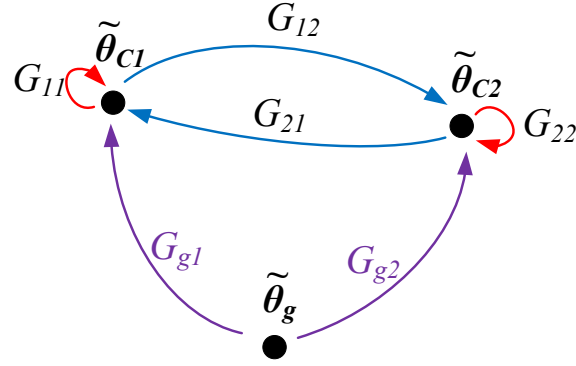


Fig. 4.110: SFG representation of PLL loops in two-converter at the weak grid condition

$$\left\{ \begin{array}{l} G_{21} = \left( \frac{1}{s} + P \right) I_{C2} K_2 \frac{K_{p1} + K_{i1} \frac{1}{s}}{1 - I_{C1} P \left( K_{p1} + K_{i1} \frac{1}{s} \right)} \\ G_{12} = \left( \frac{1}{s} + P \right) I_{C1} K_2 \frac{K_{p2} + K_{i2} \frac{1}{s}}{1 - I_{C2} P \left( K_{p2} + K_{i2} \frac{1}{s} \right)} \\ G_{g1} = k_{\sin} V_g K_1 \frac{K_{p1} + K_{i1} \frac{1}{s}}{1 - I_{C1} P \left( K_{p1} + K_{i1} \frac{1}{s} \right)} \frac{1}{s} \\ G_{g2} = k_{\sin} V_g K_1 \frac{K_{p2} + K_{i2} \frac{1}{s}}{1 - I_{C2} P \left( K_{p2} + K_{i2} \frac{1}{s} \right)} \frac{1}{s} \\ G_{11} = -\frac{G_{21}}{1 + sP} - G_{g1} \\ G_{22} = -\frac{G_{12}}{1 + sP} - G_{g2} \end{array} \right. \quad (78)$$

$$\frac{\tilde{\omega}_{C1}}{\tilde{\theta}_g} = \frac{s\tilde{\theta}_{C1}}{\tilde{\theta}_g} = s \frac{G_{g1}(1 - G_{22}) + G_{g2}G_{21}}{1 - (G_{12}G_{21} + G_{11} + G_{22}) + G_{11}G_{22}} = \frac{N(s)}{D(s)} \quad (79)$$

If plug the parameters from Table 4.12 into (79), the characteristics equation  $D(s)$  is found in (80).

$$D(s) = (s^2 + 12.06s + 88.05)(s^2 - 0.898s + 158.1) \quad (80)$$

An unstable double-pole can be found in (80), and the oscillation frequency can be calculated as 2.0 Hz. This result from the model matches with the time-domain simulation results.

Another simulation, as shown in Fig. 4.111, is conducted to verify the proposed model. The parameters are the same in Table 4.12 except that the PI in PLL2 are different:  $K_{p2} = K_{i2} = 0.5$ . As shown in Fig. 4.112, the transfer function  $\omega_{C1}/\theta_g$  is measured by the network analyzer tool and is compared with the result from the model. The predicted transfer function of the model matches very well with the measurement results.

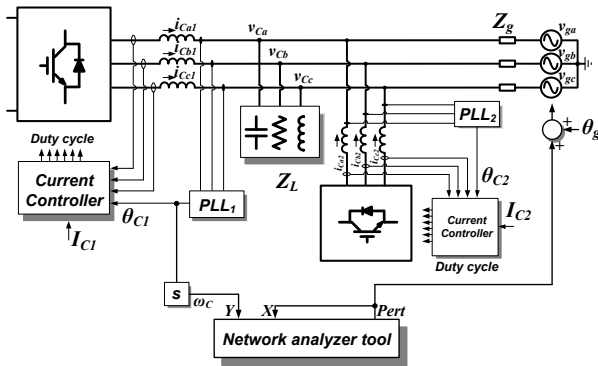


Fig. 4.111: Illustration of mall-signal measurement at two-converter case with //RC load

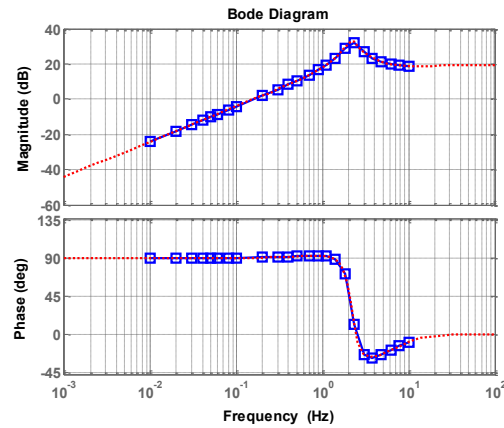


Fig. 4.112: Comparison between the measurement result (blue) and the model (red)

It can be seen that using the proposed small-signal model can predict the stability of grid-synchronization at the weak grid condition.

The generalization of any number of converters at the islanded condition can be obtained by SFG and MGF. For example, Fig. 4.113 and Fig. 4.114 show a three-converter system and a four-converter system at the weak grid condition, respectively. The transfer functions in SFG can be also generalized in (81).

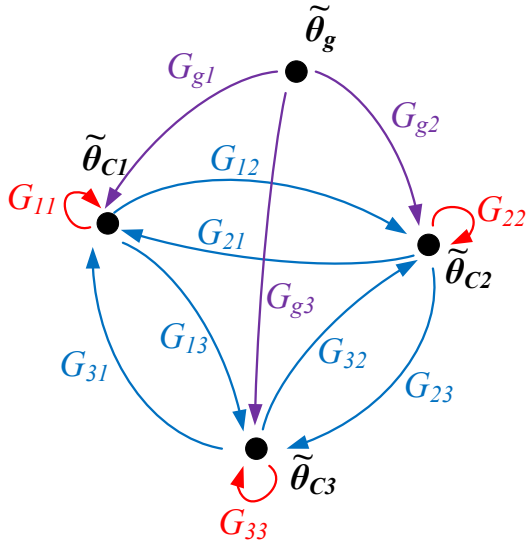


Fig. 4.113: SFG representation of PLL loops in a three-converter system at the weak grid condition

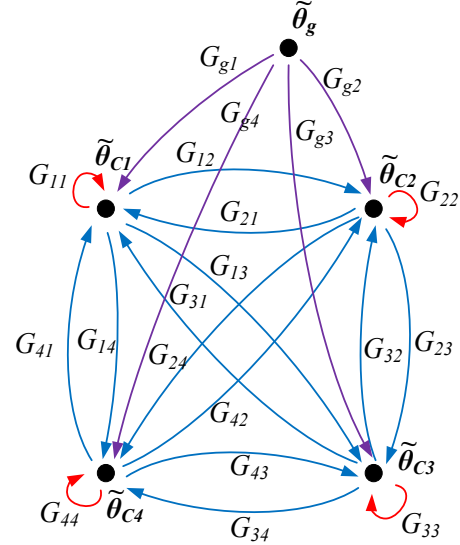


Fig. 4.114: SFG representation of PLL loops in a four-converter system at the weak grid condition

$$\left\{ \begin{array}{l} G_{nm} = \left( \frac{1}{s} + P_n \right) I_{Cn} K_{2m} \frac{K_{pm} + K_{im} \frac{1}{s}}{1 - I_{Cm} P_m \left( K_{pm} + K_{im} \frac{1}{s} \right)}, n \neq m \\ G_{gm} = k_{\sin_m} V_g K_{1m} \frac{K_{pm} + K_{im} \frac{1}{s}}{1 - I_{Cm} P_m \left( K_{pm} + K_{im} \frac{1}{s} \right)} \frac{1}{s} \\ G_{mm} = - \sum_{n=1}^N \frac{G_{nm}}{1 + sP_n} - G_{gm} \end{array} \right. \quad (81)$$

If ignoring the impedance between converters, the equation in (82) is valid.

$$\left\{ \begin{array}{l} P_1 = P_2 = \dots P_m = P = K_2 (\omega_{op}) k_\varphi + \varphi_2 (\omega_{op}) k_z \\ k_{\sin_1} = k_{\sin_2} = \dots k_{\sin_m} = k_{\sin} = \cos(\theta_\Delta) \\ K_{11} = K_{12} = \dots K_{1m} = K_1 = \left| \frac{Z_L}{Z_L + Z_g} \right| \\ K_{21} = K_{22} = \dots K_{2m} = K_2 = \left| \frac{Z_L Z_g}{Z_L + Z_g} \right| \end{array} \right. \quad (82)$$

Another two examples using different parameters are shown in Table 4.13 to explain how the grid synchronization behaviors can be predicted by the poles' locus from the model. The corresponding PLL1 output simulation results are shown in Fig. 4.115 and Fig. 4.116. The denominator in case 1 shows a stable double-pole (3.44 rad/s), and the simulation result in Fig. 4.115 shows a stable oscillation at 3.43 rad/s, matched with the prediction. In case 2, the denominator shows an unstable double-pole (22.7 rad/s), and the simulation result in Fig. 4.116 also shows an unstable oscillation behavior at 22.74 rad/s. These two examples show that the proposed model can precisely predict the grid synchronization behaviors.

Table 4.13: Two examples for two-converters at the weak grid condition

	Simulation condition	Calculated Characteristics equation
Case 1	$//R_L C_L = 2\Omega/87.95\mu\text{F}$ $K_{p1}=0.1, K_{i1}=1, K_{p2}=0.5, K_{i2}=1.1$ $V_g = 100 \text{ V}_{\text{pk}}, Z_g = 10 \Omega$ $I_{C1} = 80 \text{ A}_{\text{pk}}, I_{C2} = -30 \text{ A}_{\text{pk}}$ $\theta_A = 0.3347 \text{ rad}$	$D(s) = (s + 68.29)(s + 2.094)(s^2 + 0.7472s + 11.98)$
Case 2	$//R_L C_L = 10 \Omega/87.95\mu\text{F}$ $K_{p1}=0.01, K_{i1}=7, K_{p2}=0.3, K_{i2}=0.2$ $V_g = 100 \text{ V}, Z_g = 0.4 \Omega$ $I_{C1} = 70 \text{ A}_{\text{pk}}, I_{C2} = -70 \text{ A}_{\text{pk}}$ $\theta_A = 0.0127 \text{ rad}$	$D(s) = (s + 37.04)(s + 0.6781)(s^2 - 0.08923s + 515.3)$

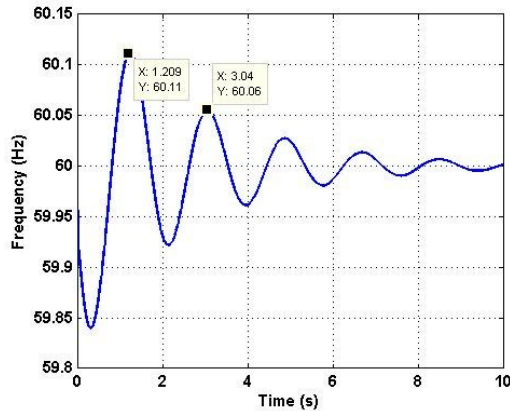


Fig. 4.115: PLL1 output for case 1

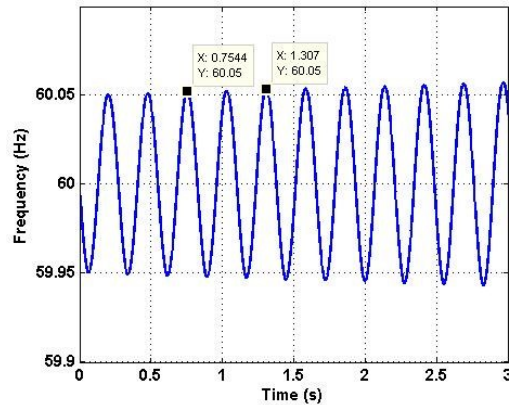


Fig. 4.116: PLL output for case 2

According to the above discussions, several conclusions are drawn here.

1. Grid synchronization might be unstable in the multi-converter case at the weak grid or islanded condition if PLLs PI values are not designed well.

2. The worst case happens when some of the converters operate at the inverter mode and some the converters operate at the rectification mode.

3. Electronic loads, e.g. AFE, may have interactions with DGs.

4. High penetration level of DG, high engagement of electronic load, weak grid, and more reactive power consumption result in higher chance of instability of grid synchronization among converters.

5. All frequency related control, such as islanding detections, will be highly affected due to the cross-talk among converters in the multi-converter case.

If we explore the solutions to the issue in the example mentioned at the beginning of this section, one of the solutions is to upgrade the distribution system bus feeder and transformer. However, in the rural area, the cost will be very high, and this solution poses no need to install the local distributed generation. Another solution is to apply the droop control for any of the distributed generation units, which, however, makes the design complicated since all the inverters are coupled together in the whole electric grid. The third solution is to use the ECC to interface the local distribution system with the outside; thus the local system is fully decoupled from the grid and any droop control in the manufacture factory is applicable. This example shows why ECC is required in future power grid architecture.

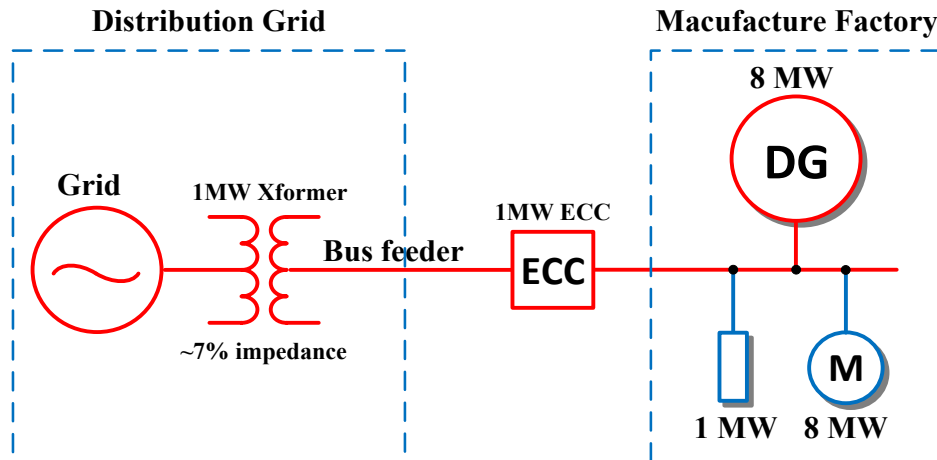


Fig. 4.117: The future local distribution generation system with ECC

#### 4.3.4. CONCLUSION

This section discussed the grid synchronization in the multi-converter case at islanded and weak grid conditions. The analysis shows that the PLL loops are fully coupled together among converters, which are determined by PLL PI values, system impedances, and stiffness of grid.

This coupling effect among converters is fully characterized by the proposed model, and this model can precisely predict the dynamic behaviors of any converter's PLL. The model can also help investigate the stability of grid synchronization at a very sophisticated electric power system employed with multiple converters. The proposed model helps power electronics engineers and power system integration engineers design and optimize the grid synchronization performance of ac-dc bus-interface converters.



## **Chapter 5. ISLANDING DETECTION ALGORITHMS IN AC-DC BUS-INTERFACE CONVERTERS**

This chapter presents a discussion of islanding detection algorithms for three-phase ( $3\Phi$ ) ac-dc bus-interface converters in distributed generation systems. Building on the discussion of grid synchronization in Chapter 4, this chapter proposes several modified PLLs to effectively detect an islanding event at the worst local-load conditions, ideally achieving a zero non-detection-zone (NDZ). The discussion on islanding-detection is then extended to the multi-converter condition, and the corresponding solutions are given. The discussions in this chapter aim to assist engineers in understanding the principles of the popular “frequency-stability-based islanding detection” and provide a set of design procedures.

All the ideas and solutions presented here can be also applied to the single-phase ac-dc converters.

### **5.1. INTRODUCTION**

IEEE 1547 [120] and its additions [124, 221] require that the distributed generation (DG) unit below 10 MW rating, such as a solar inverter, has to fulfill a set of interface codes, which consist of the detection of abnormal voltage and frequency conditions.

Table 5.1 and Table 5.2 outline the voltage and frequency thresholds and clearing times. These sets of interface codes are suitable for both grid-connected condition and islanded condition including both intentional and unintentional islanded conditions. For example, during the intentional islanded condition, a local area power system can keep operation supported by local DG units if both voltage and frequency stay in the normal range. As long as the voltage and frequency are beyond the limit, the DG units have to cease energizing the system within the clearing time in Table 5.1 and Table 5.2.

Table 5.1: Interconnection system response to abnormal voltages

Voltage Range (% of base voltage)	Clearing Time (second)
$V < 50\%$	0.16
$50\% \leq V < 88\%$	2.00
$110\% \leq V < 120\%$	1.00
$V \geq 120\%$	0.16

Table 5.2: Interconnection system response to abnormal frequencies

DR size	Frequency range (Hz)	Clearing times (second)
$\leq 30$ kW	$> 60.5$	0.16
	$< 59.3$	0.16
$> 30$ kW	$> 60.5$	0.16
	$< \{59.8 - 57.0\}$ (adjustable set point)	Adjustable 0.16 to 300
	$< 57.0$	0.16

Besides the detection of abnormal conditions, the standards also require that the DG unit has to detect the “unintentional islanding condition” and de-energizes the area’s electric power system (EPS) within two seconds. As such, an islanding detection algorithm is needed in any DG unit.

When the unintentional islanded condition occurs, the system voltage and frequency normally shift out of the normal range, and an over and under voltage (OUV) and frequency (OUF) protection based on Table 5.1 and Table 5.2 can be directly used to detect islanding event. However, the detection time sometimes might be longer than two seconds if the voltage or frequency shifts slowly. Therefore, a specific islanding detection algorithm has to be implemented to ensure the fulfillment of islanding detection requirement.

In addition to detecting faults on the grid, islanding detection algorithms play another key role in future ac micro-grid and nano-grid systems: through the detection of an islanding event, these methods allow the control system to decide on an appropriate operational mode.

Therefore, there have been many publications that explore an islanding detection algorithm. In general, islanding detection can be performed using either passive or active methods. As mentioned in Chapter I, passive methods are simple but susceptible to NDZs and incompatible to other grid standards, such as low-voltage (LV) and zero-voltage ride-through (RT) requirements.

Active methods involve continuous perturbations and/or distortion of the converter's output, such as current perturbation. The performance of this type of islanding detection method varies with the operating condition; thus normally large perturbations are performed, which can lead to problems with power quality as well as instability issues. The output-frequency-based islanding detection methods, belonging to the active methods, are gaining recent popularity as the method itself doesn't violate the LVRT requirement and doesn't require the perturbation of an injection current. Many publications [114, 122, 136, 211, 215-217] mention the generation of a "frequency positive feedback," which drives the converter system output frequency away from the steady-state and can detect an islanding event. However, the positive-feedback mechanism is not presented in detail, and thus the question of "how it determines the output frequency behaviors" has not been answered. Furthermore, these publications lack a detailed design procedure and over-design or simple trial-and-error methods are applied. The impact of these methods on the power converter operation and system stability are still unknown, as is the performance under more sophisticated conditions, e.g., in a multi-converter system.

The islanding-detection test procedure is described in [221], in which the local load is the *//RLC* load with 60 Hz resonant frequency.

This chapter is dedicated to comprehensively analyzing and summarizing frequency-based islanding detection using a typical PLL system. The design of PLL PI values in all the proposed methods in this chapter are based on the typical PLL. All the proposed methods will be compared to the typical PLL to determine any differences. The typical PLL closed-loop response is shown in (1), in which  $k_{PD}$  is the phase-detector gain.

$$F_{close}(s) = \frac{\omega_n^2 \left(1 + \frac{s}{\omega_{zero}}\right)}{s^2 + 2\xi\omega_n s + \omega_n^2}, \quad (1)$$

$$\omega_{zero} = \frac{K_i}{K_p}, \omega_n = \sqrt{k_{PD} K_i}, \xi = \frac{K_p}{2} \sqrt{\frac{k_{PD}}{K_i}}$$

For simplicity, the natural frequency  $\omega_n$  can be regarded as an indicator of the PLL bandwidth. As such, the PLL PI value shown in (2) can be based on the natural frequency  $\omega_n$  and the damping factor  $\zeta$ .

$$\begin{cases} K_i = \frac{\omega_n^2}{k_{PD}} \\ K_p = \frac{2\xi\omega_n}{k_{PD}} \end{cases} \quad (2)$$

## 5.2. ISLANDING DETECTION BASED ON LARGE-SIGNAL STABILITY

### 5.2.1. FIRST PLL-BASED ISLANDING DETECTION METHOD

Using the understanding of the PLL frequency behavior at the islanded conditions presented in Chapter 4, we know that most islanding events can be effectively detected by directly monitoring the PLL output. Only the worst local-load case of an  $//RLC$  load with a 60 Hz resonant frequency cannot be detected, which is the only NDZ point for the PLL. Therefore, in order to detect islanding for all local-load conditions, modifying the PLL is a requirement.

As discussed above, the transfer function of the PLL under the  $//RLC$  islanded condition is shown in (3).

$$\frac{\tilde{\omega}_{out}}{\tilde{\theta}_{pert}} = \frac{I_C R_L}{1 - I_C R_L K_p k_\phi} \frac{sK_p + K_i}{\left( s - \frac{I_C R_L K_i k_\phi}{1 - I_C R_L K_p k_\phi} \right)} \quad (3)$$

It can be inferred from this equation that the PLL keeps tracking to and staying at the equilibrium point. If the equilibrium point changes, the PLL output will automatically react to this change. The principle behind this is discussed below.

The proposed islanding detection is shown in Fig. 5.1.

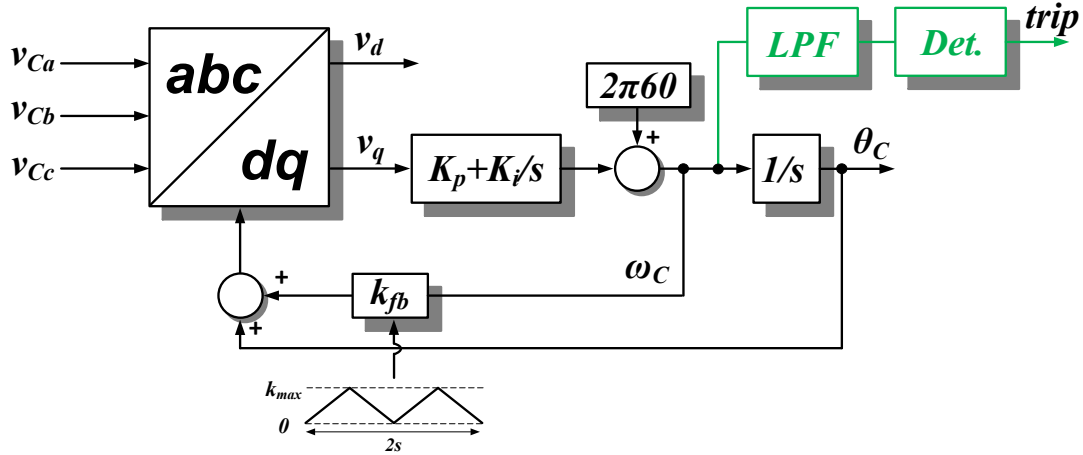


Fig. 5.1: The first proposed PLL for anti-islanding detection

An additional large-signal feedback loop is introduced multiplied by a gain  $k_{fb}$ , which is a 0.5 Hz or 1 Hz small triangular signal between 0 and  $k_{max}$ . This additional feedback loop constantly shifts the equilibrium point, that is, the equivalent resonant frequency. Thus, there will be no stable equilibrium point, and the PLL output frequency will change constantly all the time at the islanded condition.

Fig. 5.2 shows the model of the proposed PLL; Fig. 5.3 shows the corresponding PLL model under the islanded condition.

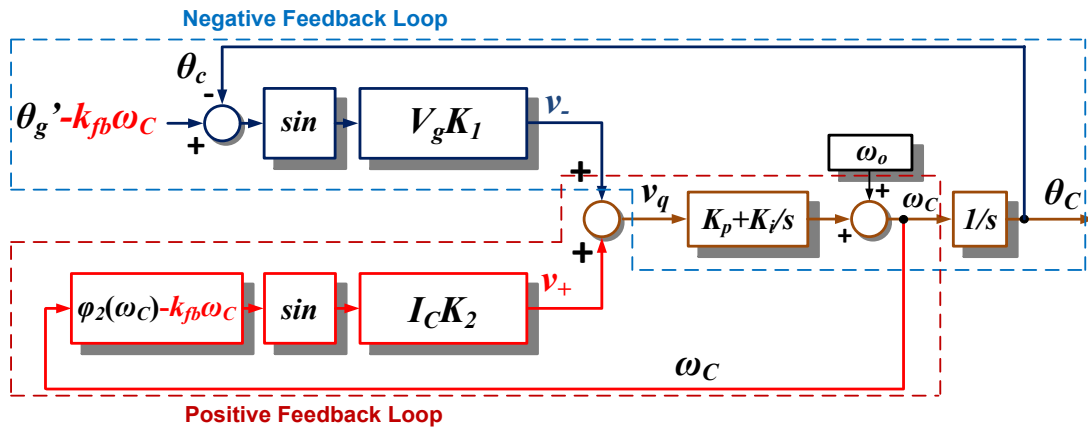


Fig. 5.2: Model of the first proposed PLL

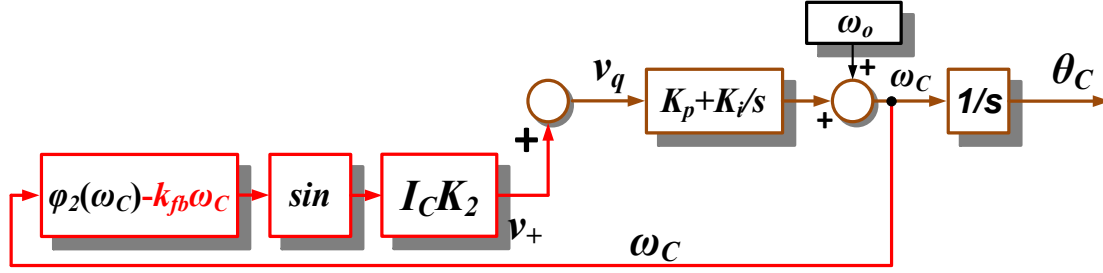
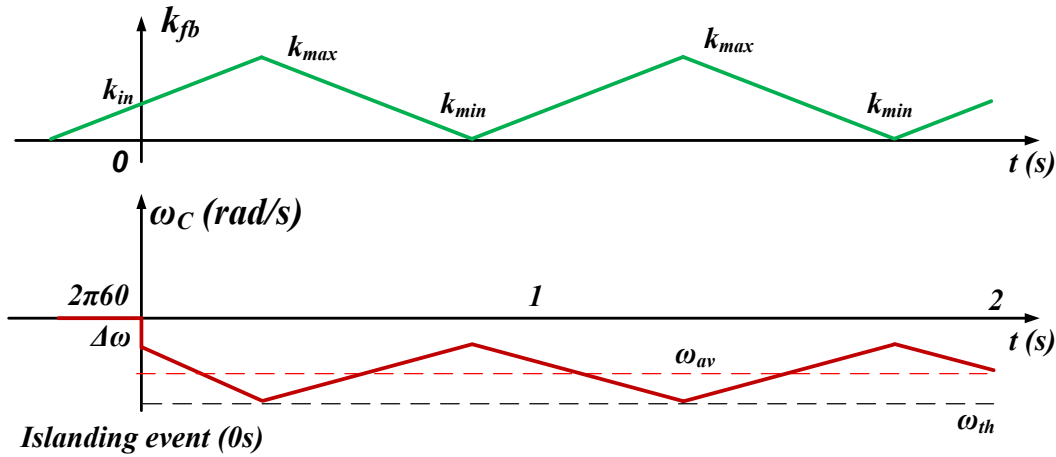


Fig. 5.3: Model of the first proposed PLL under islanded condition

The output frequency will follow the input injection signal  $k_{fb}$ , and is shown below in Fig. 5.4. Eventually, the average value  $\omega_{av}$  of the PLL output will stay lower than 60 Hz and its value can be determined by (4).

$$\varphi_2(\omega_{av}) = \frac{1}{2}(k_{\max} + k_{\min}) = \frac{1}{2}k_{\max} \quad (4)$$

Fig. 5.4: The first proposed PLL output behavior when the islanding condition occurs:  $k_{fb}$  (green),  $\omega_C$  (red)

It is also seen that there is a frequency jump  $\Delta\omega$  when the islanding event occurs. This frequency jump is due to the mode step from the grid-tied mode to the islanded mode, and the value can be estimated as in (5).

$$\Delta\omega = K_p k_{in} I_C R_L \quad (5)$$

According to Fig. 5.4, the PLL output  $\omega_C$  can be directly monitored to detect the islanding condition, and a low-pass-filter (LPF) is used to eliminate the high-frequency ringing. The detection algorithm is developed using the following method.

1. When  $k_{fb}$  reaches  $k_{max}$ ,  $\omega_C$  is compared with threshold frequency  $\omega_{th}$ . If  $\omega_C$  is lower than  $\omega_{th}$ , the anti-islanding protection signal is set.

2. When  $k_{fb}$  reaches  $k_{max}$ , compare  $\omega_C$  with the value when  $k_{fb}$  reaches 0. If the difference is bigger than the threshold, the anti-islanding protection signal is set.

Either of these two conditions will trip the protection signal. The only design parameter is  $k_{fb}$ . Since  $k_{fb}$  is a very low-frequency signal, much lower than the PLL bandwidth, the output of the PLL can be assumed to be at the steady-state all the time. Thus when  $k_{fb}$  reaches  $k_{max}$ ,  $\omega_C$  reaches  $\omega_{th}$ , as shown in (6).

$$\begin{aligned} \varphi_2(\omega_r) - k_{\max} \omega_r &= 0 \\ \Rightarrow k_{\max} &= \left( \frac{Q}{\omega_{th}} \right) \frac{\omega_r^2 - \omega_{th}^2}{\omega_r \omega_{th}} \end{aligned} \quad (6)$$

A simulation evaluation is conducted using the  $//R_L L_L C_L$  load described in Table 5.3. The frequency of  $k_{fb}$  is set as 1 Hz, and  $k_{max}$  can be calculated as 0.000421. Thus, the maximum injection angle ( $k_{fb} \times \omega_C$ ) is less than 0.11 rad. As shown in Fig. 5.5, the output of the PLL will follow the signal  $k_{fb}$ , and the islanding event can be easily detected.

Table 5.3: Simulation parameters for islanding detection

$f_o$	$f_s$	$I_C$	$V_g$	$//R_L L_L C_L$	$K_p, K_i$
60 Hz	20 kHz	8 A	80 V	10 $\Omega$ // 17.4 mH // 600 $\mu$ F (0.1 $\Omega$ resistor is in series with $L_L$ for damping )	3, 2

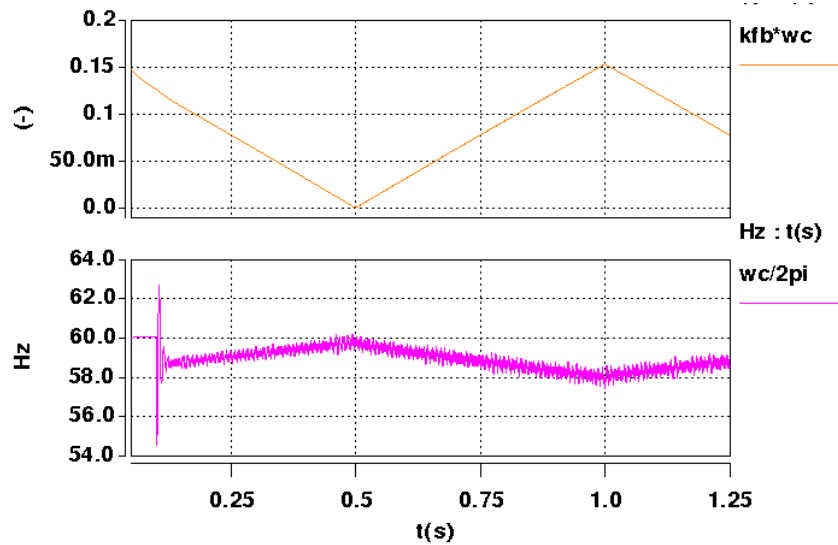


Fig. 5.5: Simulation results of the first proposed PLL output when islanding occurs: signal  $k_{fb} * \omega_C$  (orange) [0.1 rad/DIV],  $\omega_C / 2\pi$  (magenta) [2 Hz/DIV]

The islanding detection algorithm has to be tested at low-voltage conditions to determine whether it violates the requirement. During the low-voltage conditions, the anti-islanding protection should not be tripped. The low-voltage ride-through (LVRT) test circuit is defined in standard, as shown in Fig. 5.6. A small shunt-impedance  $Z_2$  is connected to generate a low voltage condition.

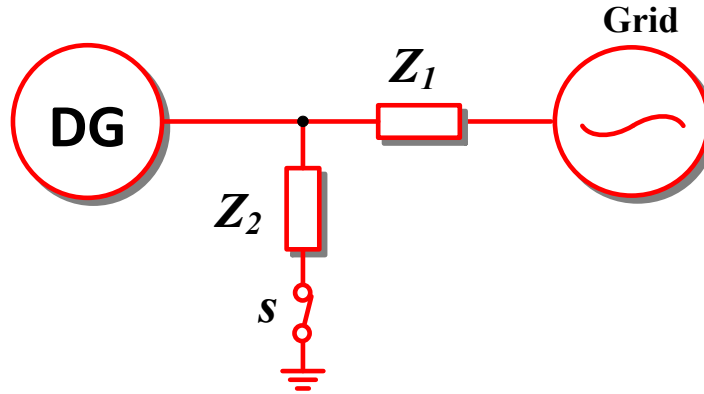


Fig. 5.6: Low-voltage ride-through (LVRT) test principle

The corresponding one-line circuit is shown in Fig. 5.7.

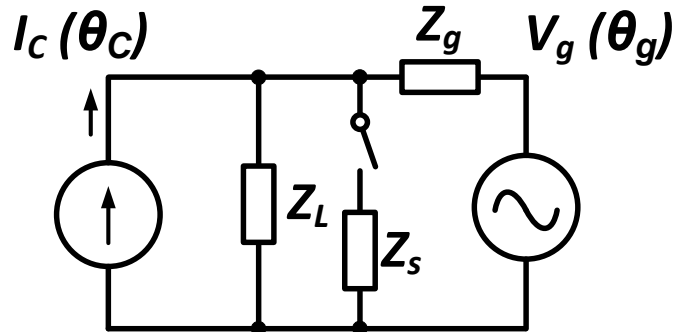


Fig. 5.7: One-line circuit to generate a low voltage

Based on the circuit, the parameters in the generic PLL model in Fig. 4.39 are shown in (7) and (8).

$$\begin{cases} K_1 = \left| \frac{Z_s // Z_L}{Z_s // Z_L + Z_g} \right| \\ K_2 = \left| \frac{(Z_s // Z_L)Z_g}{Z_s // Z_L + Z_g} \right| \end{cases} \quad (7)$$



$$\begin{cases} \varphi_1 = \text{phase} \left( \frac{Z_s // Z_L}{Z_s // Z_L + Z_g} \right) \\ \varphi_2 = \text{phase} \left[ \frac{(Z_s // Z_L) Z_g}{Z_s // Z_L + Z_g} \right] \end{cases} \quad (8)$$

These equations show that the ratio of  $K_1/K_2$  doesn't change when a low-voltage condition occurs, but instead changes when the phase-shift term  $\varphi_2$ . The PLL will be stable under low-voltage conditions unless it is connected to an extreme grid.

A simulation is conducted using the converter system in Table 5.3 to verify the PLL behavior under low-voltage conditions. Values for  $R_g$  and  $R_s$  are chosen to be  $5.6 \Omega$  (0.56 p.u.) and  $5.6 \Omega$  (0.056 p.u.)  $R_g$  is a relatively large value, representing a very weak grid condition. Fig. 5.8 shows that the PLL is stable during the low-voltage period from 1 to 1.3 sec.

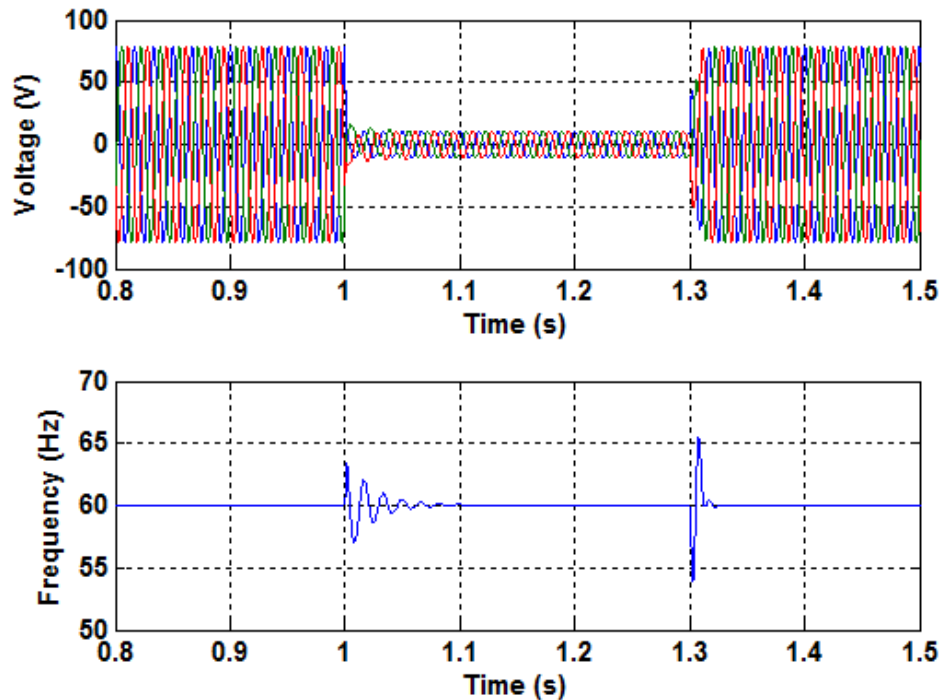


Fig. 5.8: PLL output under low-voltage conditions

The change in the grid synchronization performance due to the additional feedback loop can be investigated by exploring the model at the stiff-grid-tied mode, as shown in Fig. 5.9.

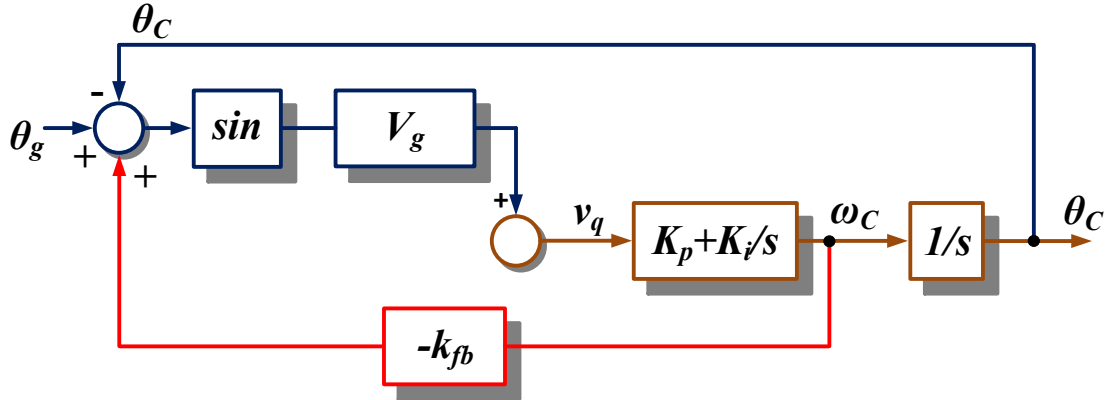


Fig. 5.9: The first proposed PLL model under the stiff-grid-connected condition

The consequent closed-loop transfer function can be derived as in (9) where  $\omega_{nM}$  and  $\zeta_M$  are the corresponding natural frequency and damping factor of the modified PLL, respectively.

$$F_{close}(s) = \frac{\omega_{nM}^2 \left(1 + \frac{s}{\omega_{zero}}\right)}{s^2 + 2\zeta_M \omega_{nM} s + \omega_{nM}^2}, \omega_{zero} = \frac{K_i}{K_p}, \tag{9}$$

$$\omega_{nM} = \frac{\sqrt{V_{grid} K_i}}{\sqrt{1 + k_{fb} V_{grid} K_p}}, \zeta_M = \frac{K_p + k_{fb} K_i}{2\sqrt{1 + k_{fb} V_{grid} K_p}} \sqrt{\frac{V_{grid}}{K_i}}$$

Both  $\omega_{nM}$  and  $\zeta_M$  of the proposed PLL change accordingly. If the PI values in (9) are designed by choosing  $\omega_n=2\pi 6$  rad/s and  $\zeta = 1$  based on (2),  $\omega_{nM}/\omega_n$  and  $\zeta_M/\zeta$  can be compared using the curves shown in Fig. 5.10 and Fig. 5.11, respectively.

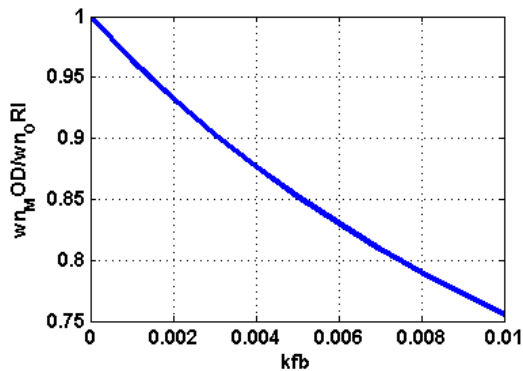


Fig. 5.10: Normalized natural frequency  $\omega_{nM}/\omega_n$  of the proposed PLL

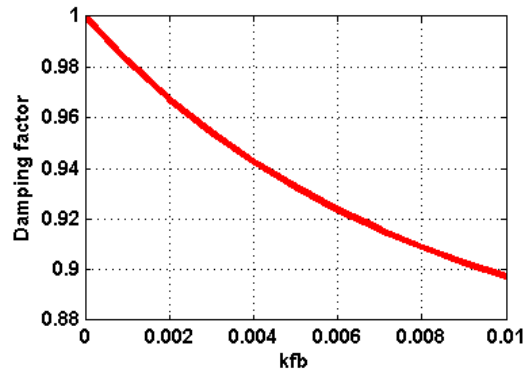


Fig. 5.11: Normalized damping factor  $\zeta_M/\zeta$  of the proposed PLL

It is easy to see that the change of the PLL performance is very limited in terms of both the damping factor and the natural frequency. The bandwidth of the proposed PLL

will be slightly lower than the typical PLL. Even when  $k_{fb}$  equals 0.01 (normally  $k_{fb}$  is smaller than 0.001), the decrement of the bandwidth is less than 30%. Fig. 5.12 shows the 2 Hz step responses of the typical PLL and the proposed PLL when  $k_{fb}$  is set as 0.01 and 1% 600 Hz grid voltage harmonics are present. The result shows the proposed PLL has a slower dynamic response than the typical PLL.

Thus, the grid synchronization performance of the proposed PLL can be treated the same as the original PLL.

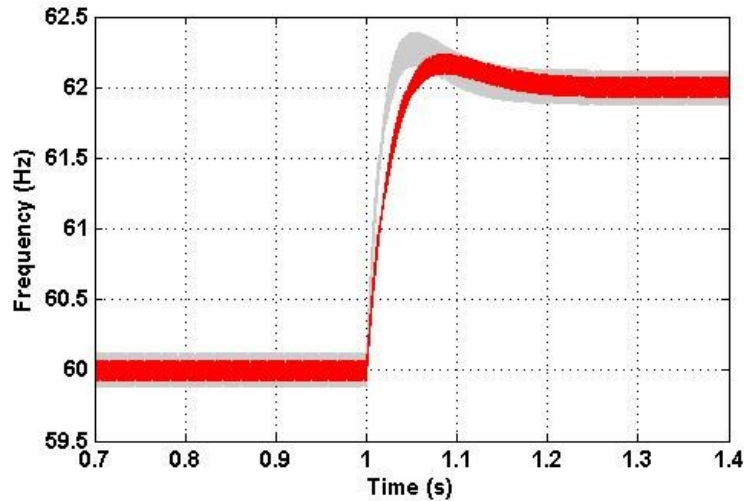


Fig. 5.12: 2 Hz step response of the first proposed PLL (grey) [0.5 Hz/DIV] and the typical PLL (red) [0.5 Hz/DIV]

### 5.2.2. SECOND PLL-BASED ISLANDING DETECTION METHOD

The second PLL-based islanding detection algorithm is shown in Fig. 5.13, and is based on the same principle as the first detection algorithm. The difference is that a delay block is introduced in this PLL, and the delay time  $\Delta$  is constantly shifted in a triangular shape.

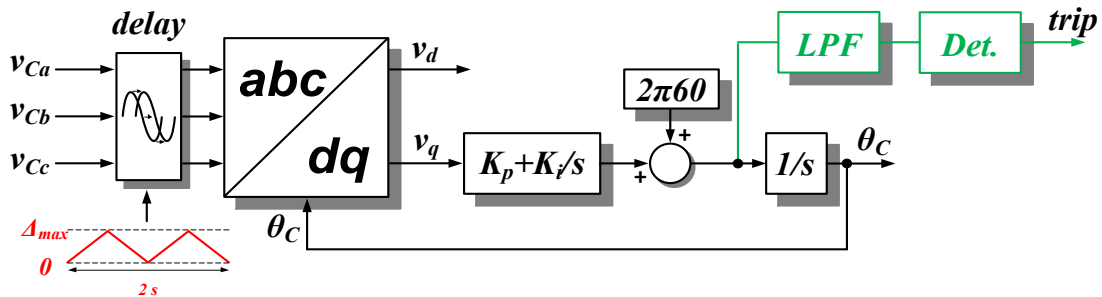


Fig. 5.13: The second proposed PLL for islanding detection

The corresponding PLL sub-models at the stiff-grid-tied and the islanded conditions are shown in Fig. 5.14 and Fig. 5.15, respectively.

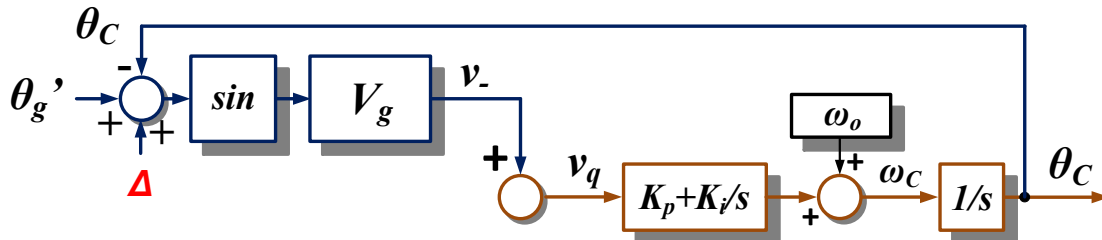


Fig. 5.14: Model of the second proposed PLL at the stiff-grid-tied condition

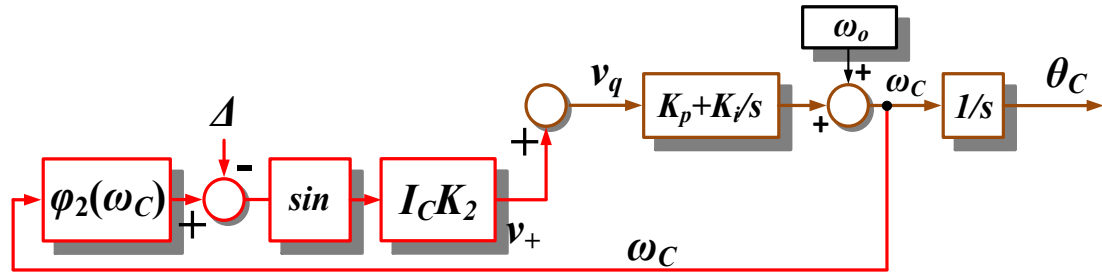


Fig. 5.15: Model of the second proposed PLL at the islanded condition

The figures show that the second proposed islanding detection algorithm behaves similarly to the first algorithm at the islanded condition. However, it doesn't introduce any additional feedback at the stiff grid-tied mode.

Using the parameters in Table 5.3, Fig. 5.16 shows the MATLAB simulation shows the output frequency behavior when using the variable time delay block in MATLAB. The maximum delay is set as 0.0005 sec.

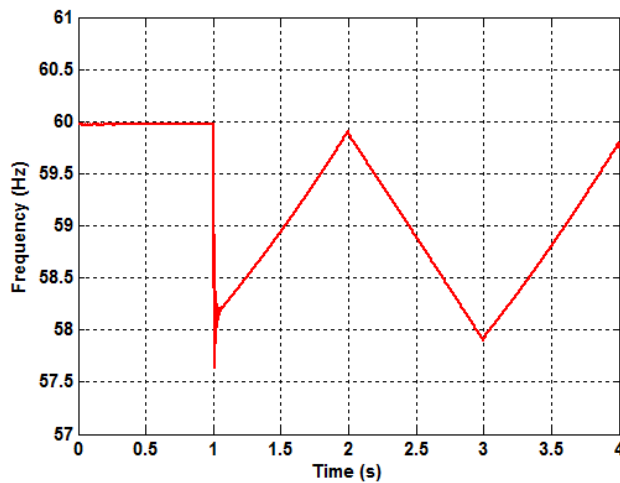


Fig. 5.16: Second proposed PLL output behavior at the islanded condition by using variable delay block

The down-side of islanding detections based on the large-signal stability of PLL is that a small frequency perturbation degrades the performance of the output power factor regulation at the grid-tied mode. As shown in Fig. 5.17, the PLL output performs a small step in the previous simulation (Table 5.3). However, it should be noted that this simulation is obtained under a local-load with a high  $Q$ , and the threshold frequency is set as 58 Hz, which exaggerates the design and the results. In practice, this step error will be diluted due to the unbalanced system voltage condition. In addition, the threshold can be set to only 59.5 Hz, leading to a very small perturbation in the practical design.

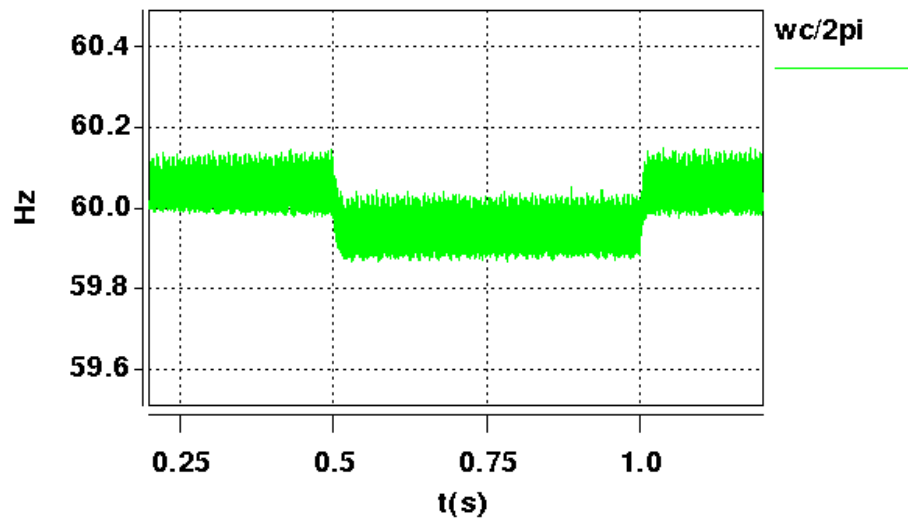


Fig. 5.17: Proposed PLL steady-state output under the grid-tied mode

Compared to other perturbation methods, using this method the perturbation in the proposed solutions is small enough to only destabilize the PLL. However, as with other perturbation methods, the proposed solutions still have a fundamental problem when used under the multi-converter condition as the perturbation signals talk to each other, which changes the performance dramatically.

### 5.2.3. EXPERIMENTAL EVALUATION

The islanding detection test is conducted in a lab prototype as shown in Fig. 4.69. An ac power supply is used as the grid. The test conditions are shown in Table 5.3. In order to obtain the NDZ, the frequency of the ac power supply is set slightly lower than 60 Hz.

As shown in Fig. 5.18, using the typical PLL, the frequency stays at 60 Hz and the voltage doesn't change due to the matched load condition. The converter system cannot

determine whether it operates at the islanded condition. Fig. 5.19 shows the first proposed PLL output performance when an islanding event occurs. It clearly shows a triangular waveform due to the additional feedback. The converter system can easily detect the islanding event by exploring such output waveforms.

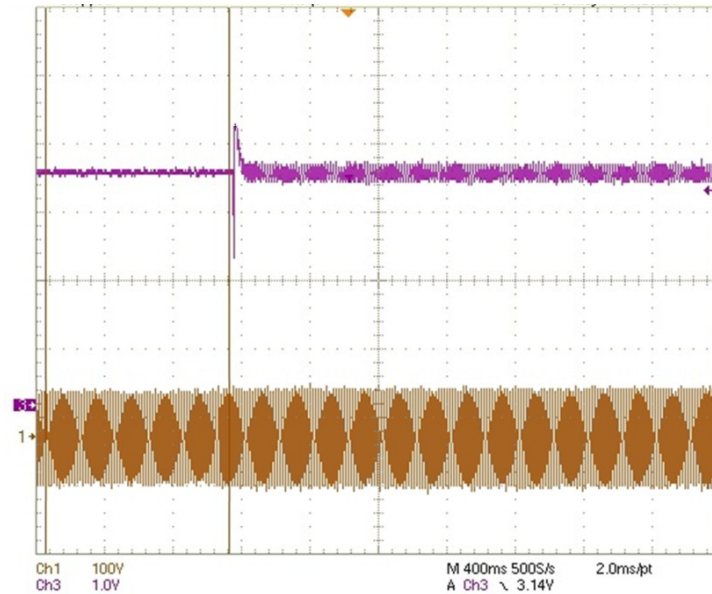


Fig. 5.18: The typical PLL output under  $//RLC$  load with 60 Hz resonant frequency when islanding occurs:  $\omega_c/2\pi$  (purple) [5Hz/DIV],  $v_{Ca}$  (orange) [100V/DIV]

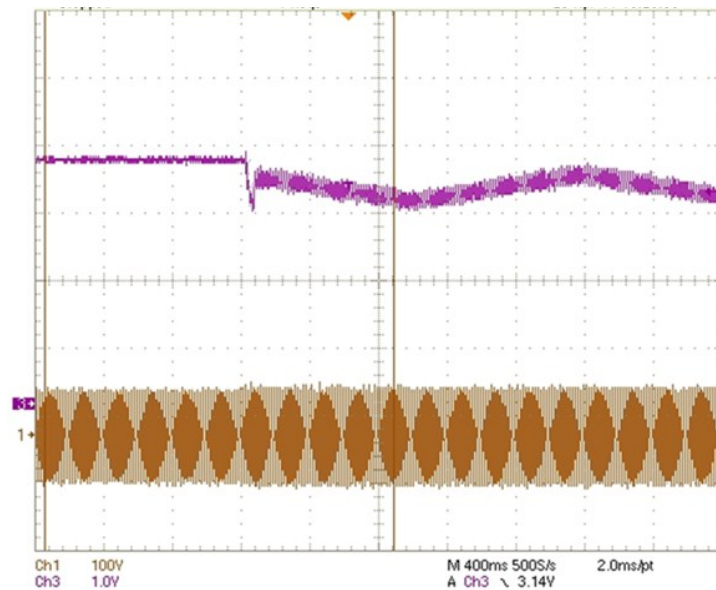


Fig. 5.19: The first proposed PLL output under  $//RLC$  load with 60 Hz resonant frequency when islanding occurs:  $\omega_c/2\pi$  (purple) [5Hz/DIV],  $v_{Ca}$  (orange) [100V/DIV]

#### 5.2.4. CONCLUSION

Frequency-based islanding detection algorithms are investigated using the large-signal stability of the PLL system. By introducing a small perturbation, the PLL equilibrium point can be moved constantly, leading to unstable PLL output at the islanded condition. Only one parameter needs to be designed, and its impact on the grid synchronization performance under normal operation is very small. The detailed design presented in this chapter can help the designer achieve the desired performance while avoiding over-design.

### **5.3. ISLANDING DETECTION BASED ON SMALL-SIGNAL STABILITY**

#### **5.3.1. THIRD PLL-BASED ISLANDING-DETECTION METHOD**

The previous PLL-based anti-islanding algorithms own a common drawback that a perturbation, though very small, is still required. Thus, during the grid-tied mode, the power quality of the converter output current still suffers from this small perturbation. Hence, the third proposed frequency-stability-based islanding detection method aims to eliminate any of the perturbation signals into the control system.

The idea of the third method comes from the small-signal PLL model, as shown in Fig. 4.83. The PLL cannot detect the  $//RLC$  load with 60 Hz resonant frequency because the equilibrium point of the PLL is a stable one.

Therefore, in order to detect the islanding condition under the  $//RLC$  load, the PLL has to be unstable at the equilibrium point. Besides moving the equilibrium point as proposed in the previous section, the equilibrium point itself can be modified to be unstable. If this is done, the PLL will always drift away at the islanded condition. Based on this idea, the PLL can be modified as shown in Fig. 5.20, which shows that an additional small-signal feedback term is introduced multiplied by a constant gain  $N$ .

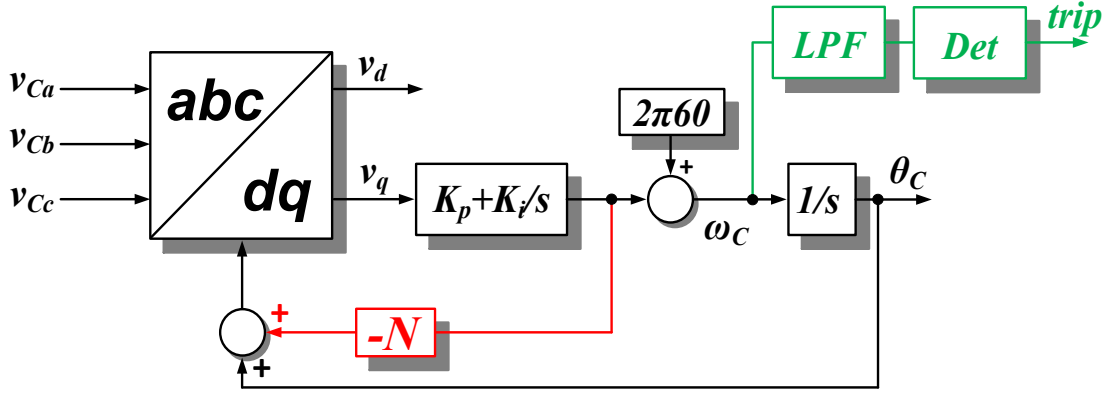


Fig. 5.20: The third proposed PLL for islanding detection

Fig. 5.21 shows the equivalent small-signal PLL model around the equilibrium point under islanded conditions.

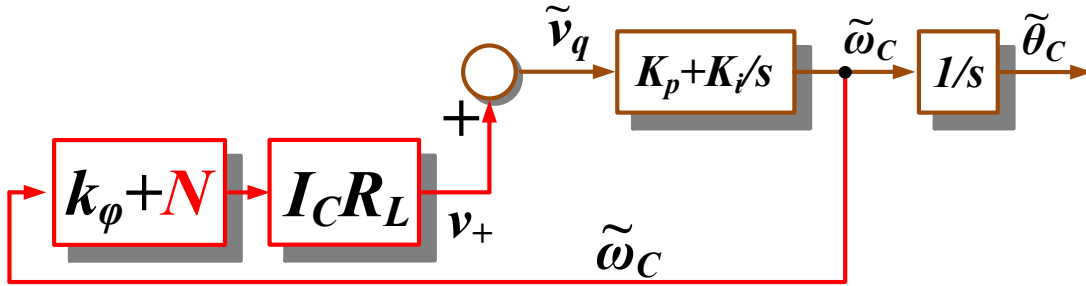


Fig. 5.21: Small-signal model of the third proposed PLL for islanding detection

Fig. 5.21 shows that the additional small-signal term  $N$  appears in the small-signal feedback loop, and the closed-loop pole is derived in (10).

$$\omega_{pole} = \frac{(k_\phi + N)I_C R_L K_i}{1 - (k_\phi + N)I_C R_L K_p} \quad (10)$$

The  $N$  can be designed as shown in (11).

$$k_\phi + N > 0 \Rightarrow k_\phi > \frac{2Q}{\omega_r} \quad (11)$$

Practically,  $k_\phi + N$  is designed to be a small number, and the PLL proportional gain  $K_p$  is not very big. Thus, the condition in (12) is valid.

$$K_p < \frac{1}{k_\phi + N} \quad (12)$$

As such, the closed-loop pole will be moved to the right half-plane (RHP) in the  $s$  domain thanks to the additional feedback, and the PLL is unstable at the equilibrium



point. Since this is a first-order system, the output of the unstable PLL will follow an exponential curve (monotonic instability), as shown in Fig. 5.22 and Fig. 5.23.

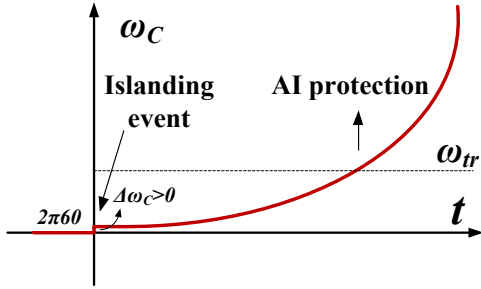


Fig. 5.22: The third PLL output under the islanded condition when the initial condition is positive

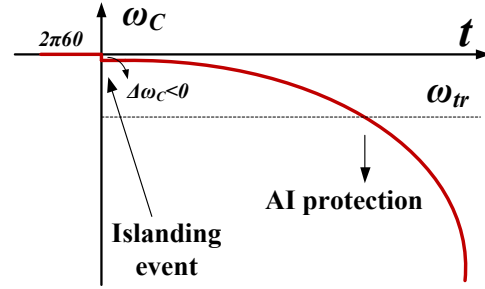


Fig. 5.23: The third PLL output under the islanded condition when the initial condition is negative

The frequency either drifts upwards or downwards depending on the initial condition  $\Delta\omega_C$  as in (13).

$$\Delta\omega_C = \omega_r - \omega_o \quad (13)$$

Besides the initial condition, the RPH pole location is also significant when determining the frequency drift speed. When considering the worst case, in which the converter terminal voltage doesn't change under the islanding event, the pole location can be further simplified as in (14), which indicates that the PLL dynamic performance solely determines the drift speed. From this angle, a higher PLL bandwidth is desired.

$$\omega_{pole} = \frac{(k_\varphi + N)I_C R_L K_i}{1 - (k_\varphi + N)I_C R_L K_p} = \frac{(k_\varphi + N)V_g K_i}{1 - (k_\varphi + N)V_g K_p} \quad (14)$$

The islanding detection algorithm in the *Det.* block is simple. A simple over/under frequency criteria can be used here. If the filtered PLL output frequency is outside of the threshold value, an anti-islanding protection signal is set.

The model of the proposed PLL is shown in Fig. 5.24 under the stiff-grid-tied mode to evaluate the PLL performance at the normal operation.

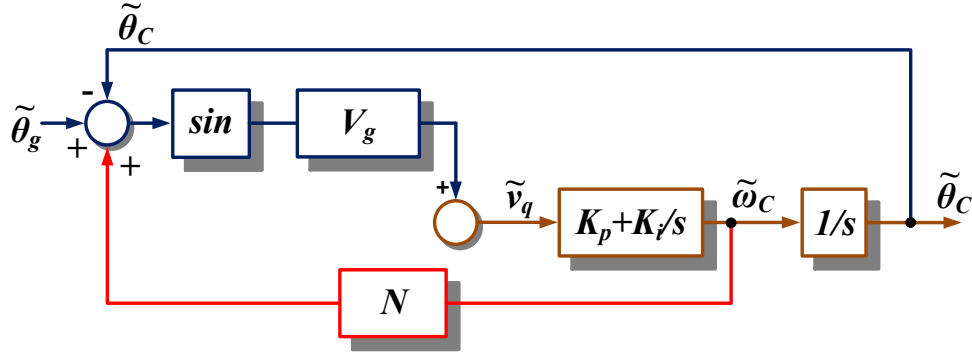


Fig. 5.24: Small-signal model of the third proposed PLL at the stiff-grid-tied mode

The closed-loop transfer function can be derived using (15).

$$F_{close}(s) = \frac{\omega_{nM}^2 \left( 1 + \frac{s}{\omega_{zero}} \right)}{s^2 + 2\zeta\omega_{nM}s + \omega_{nM}^2}, \quad \omega_{zero} = \frac{K_i}{K_p}, \quad (15)$$

$$\omega_{nM} = \frac{\sqrt{V_{grid}K_i}}{\sqrt{1 - NV_{grid}K_p}}, \quad \zeta_M = \frac{K_p - NK_i}{2\sqrt{1 - NV_{grid}K_p}} \sqrt{\frac{V_{grid}}{K_i}}$$

Both the natural frequency  $\omega_{nM}$  and the damping factor  $\zeta_M$  of the proposed PLL change accordingly.

If the PI values in (15) are designed by choosing  $\omega_n = 2\pi 6$  rad/s and  $\zeta = 1$  based on (2), the normalized natural frequency  $\omega_{nM}/\omega_n$  of the proposed PLL in terms of  $N$  is shown in Fig. 5.25. We can see that the proposed PLL has a faster response given a bigger  $N$ . When  $N$  approaches  $1/K_p$ , the natural frequency will increase dramatically to infinity, exhibiting an unstable behavior.

Fig. 5.26 shows the closed-loop pole location of the proposed PLL at the stiff-grid-tied mode in terms of  $N$ . When  $N$  equals zero, two poles are overlapped together on the real axis because  $\zeta = 1$ . When  $N$  increases, the two poles are split and moved apart. One of the poles will approach the zero axis, and eventually stay on the origin when  $N$  equals  $1/K_p$ .

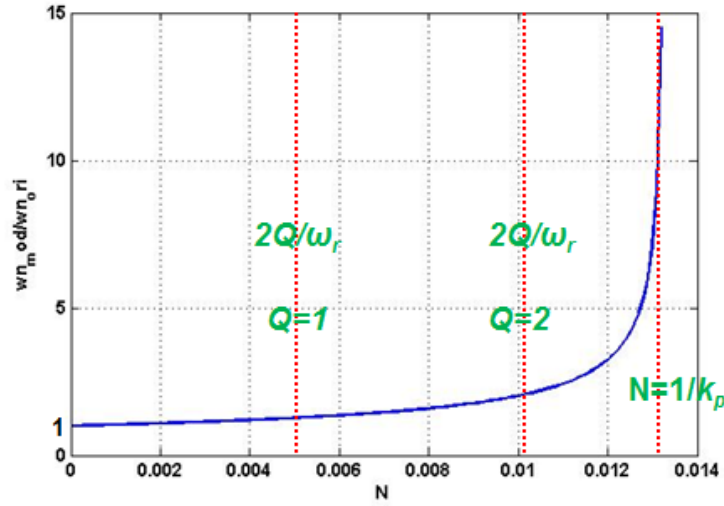


Fig. 5.25: Normalized natural frequency  $\omega_{nM}/\omega_n$  of the third proposed PLL

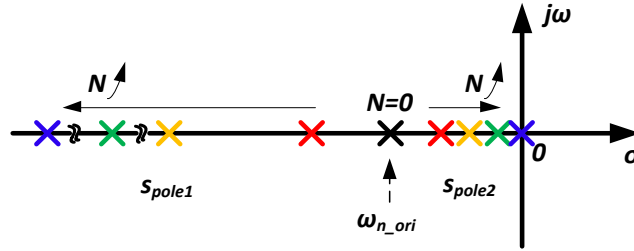


Fig. 5.26: Pole location of the third proposed PLL in terms of  $N$  at the stiff-grid-tied mode

This proposed PLL essentially has a limit on the design of  $N$ , as shown in (16), due to the stability problems of the grid-tied mode.

$$N < \frac{1}{K_p} \tag{16}$$

As shown in Fig. 5.25, under a high  $Q$  condition, the design region will be smaller. Thus this PLL may not work at the high  $Q$  load conditions, unless a low-bandwidth PLL (smaller  $K_p$ ) is implemented. This limit is shown in (17).

$$\begin{aligned} \frac{2Q}{\omega_r} < N < \frac{1}{K_p} \\ \Rightarrow Q < \frac{\omega_r}{2K_p} \end{aligned} \tag{17}$$

Fig. 5.27 shows the PLL output steady-state performance at the stiff-grid-tied mode by using different values for  $N$ . The figure illustrates the PLL's unstable oscillation when

$N$  is designed beyond the limit in (16). Fig. 5.28 reveals that the proposed PLL is faster than the typical PLL, and the high-frequency noise attenuation of the proposed PLL is in turn smaller.

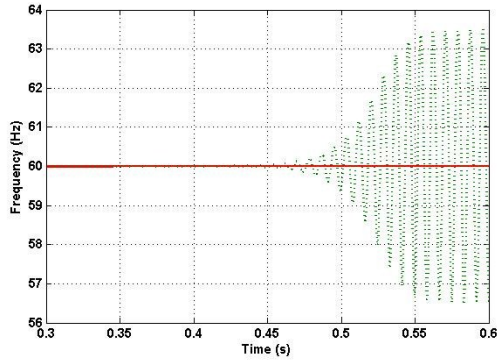


Fig. 5.27: The third proposed PLL steady-state results under two different  $N$  values:  $\omega_c/2\pi$  with  $N = 0$  (red) [1 Hz/DIV],  $\omega_c/2\pi$  with  $N > 1/K_p$  (green) [1 Hz/DIV]

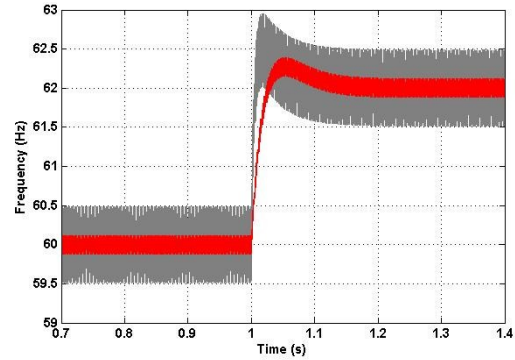


Fig. 5.28: The third proposed PLL dynamics response under 2 Hz input step with 1% 60 Hz grid voltage harmonics:  $\omega_c/2\pi$  with  $N = 0$  (red) [1 Hz/DIV],  $\omega_c/2\pi$  with  $N = 0.01$  (green) [1 Hz/DIV]

A switching model simulation is conducted to verify the effectiveness of the third proposed islanding detection algorithm. The simulation parameters are shown in Table 5.4.

Table 5.4: Parameters in simulation

$K_p, K_i$	3, 3
$R_L$	5 $\Omega$
$L_L$	35.18 mH (in series with 0.3 $\Omega$ damping resistor)
$C_L$	200 $\mu$ F
$\omega_r$	$2\pi 60$ rad/s
$V_g$	150 V
$I_C$	30 A
$f_o$	60 Hz
$f_s$	20 kHz

The islanding condition occurs at 0.3 sec. Without any modification, the typical PLL output result is shown in Fig. 5.29. It is seen that PLL output is stable around the line frequency.

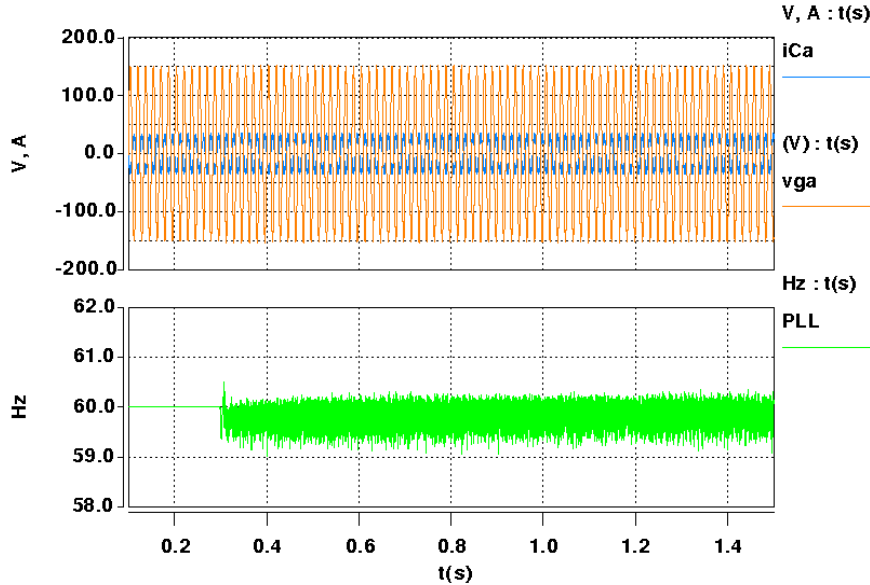


Fig. 5.29: Typical PLL output when islanding condition occurs with  $//R_L L_L C_L$  load. One phase voltage and current,  $v_{ga}$  (orange) [100V/DIV],  $i_{Ca}$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (green) [1Hz/DIV]

According to the load parameters shown in Table 5.4, the value of  $k_\phi$  can be calculated as -0.001. Thus, in the proposed PLL,  $N$  is chosen to be 0.002 accordingly to generate a small-signal positive feedback. Under the same load conditions, the results for the third PLL are shown in Fig. 5.30.

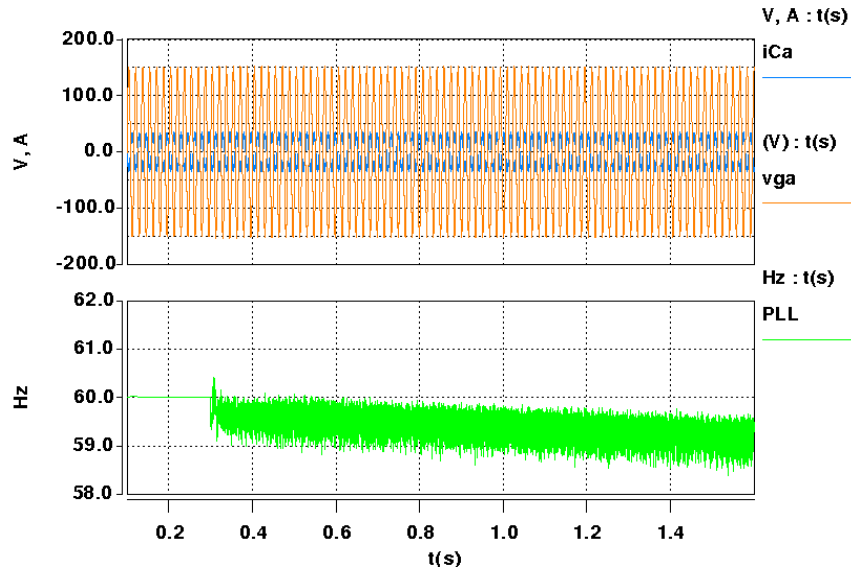


Fig. 5.30: Third proposed PLL output when islanding condition occurs with  $//R_L L_L C_L$  load. One phase voltage and current,  $v_{ga}$  (orange) [50V/DIV],  $i_{Ca}$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (green) [1Hz/DIV]

It is seen that the PLL output frequency drifts away from the line-frequency when the islanding condition occurs, which means that the frequency can be directly used to detect the islanding condition.

Another set of simulations are conducted at the purely resistant conditions. Fig. 5.31 and Fig. 5.32 show the results of the typical PLL output and the proposed PLL output, respectively. These figures show that the small-signal positive feedback loop can drive the frequency immediately away from the steady-state point. Since  $k_\phi$  equals zero, the positive feedback loop is stronger than that in the  $//RLC$  case; thus the PLL output can drift away even faster, and the islanding condition can be detected very early.

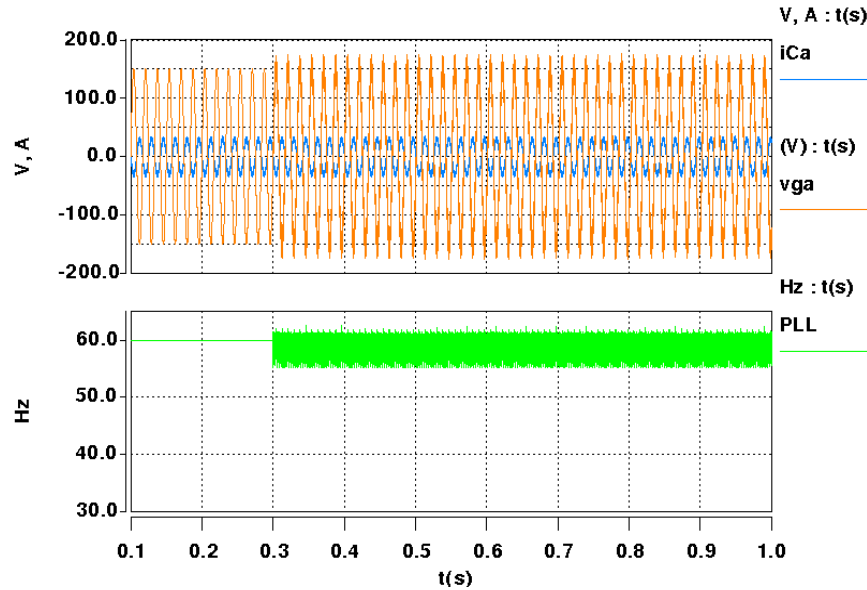


Fig. 5.31: Typical PLL output when islanding condition occurs with  $R_L$  load. One phase voltage and current,  $v_{ga}$  (orange) [50V/DIV],  $i_{Ca}$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (green) [1Hz/DIV]

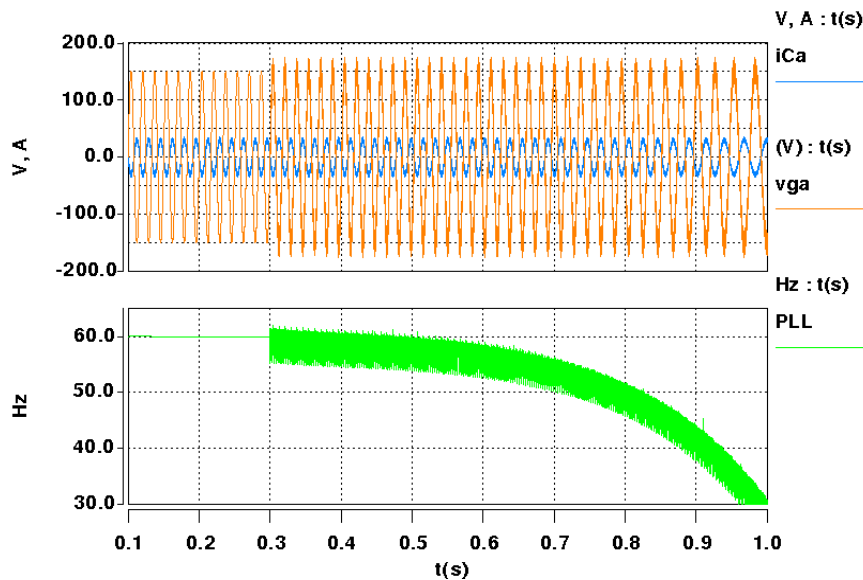


Fig. 5.32: Proposed third PLL output when islanding condition occurs with  $R_L$  load. One phase voltage and current,  $v_{ga}$  (orange) [50V/DIV],  $i_{Ca}$  (blue) [50A/DIV], PLL output  $\omega_c/2\pi$  (green) [1Hz/DIV]

### 5.3.2. FOURTH AND FIFTH PLL-BASED ISLANDING-DETECTION METHODS

According to the analysis above, the third PLL may have instability problems under the stiff-grid-tied mode, resulting in the design limit on the  $N$  value. Thus, the drift speed cannot be pushed too high. To tackle this shortcoming, the fourth PLL system, as shown in Fig. 5.33, is proposed.

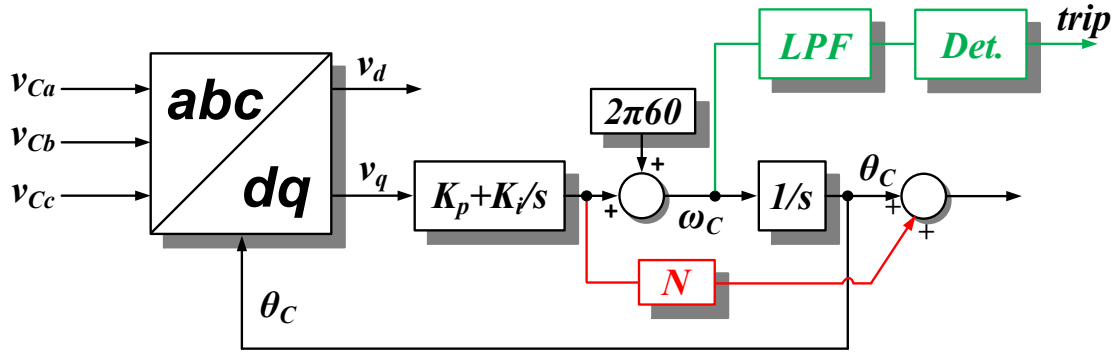


Fig. 5.33: The fourth proposed PLL system for islanding detection

Instead of introducing a small-signal feedback loop, this PLL uses an additional small-signal feedforward loop. This previously mentioned small-signal effect is still effective due to the voltage response caused by the injection current. As such, the equivalent small-signal model in Fig. 5.21 can also be used to represent this PLL behavior at the islanded condition. Therefore, the design criteria of  $N$  in (10) is still valid here, but (13) is not necessary.

In terms of the stiff-grid-tied condition, the small-signal effects from the injection current are decoupled by the grid voltage because there is zero grid impedance. However, at the weak grid, this additional feedforward loop still affects the system operation.

Fig. 5.34 shows the performances of the fourth proposed PLL and the typical PLL at the stiff-grid-tied condition. No obvious discrepancy is found between them.

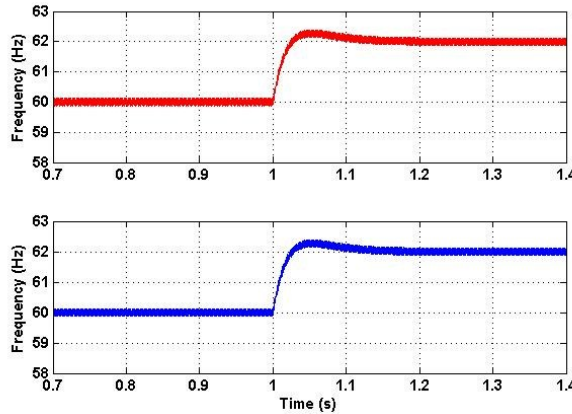


Fig. 5.34: Two Hz step responses of the fourth proposed PLL  $\omega_c/2\pi$  (red) [1 Hz/DIV] and the typical PLL  $\omega_c/2\pi$  (blue) [1 Hz/DIV]

The drift in output of both the third PLL and the fourth PLL in terms of direction and speed at the islanded condition cannot be predicted because the drift is strongly related to the value  $\Delta\omega$  at the initial condition. In an ideal case, the frequency drift speed might be extremely slow when the initial value is almost zero.

In order to generate an initial value  $\Delta\omega$ , a very small perturbation can be used to generate  $\Delta\omega$  which is big enough to quickly drive the output frequency away. Therefore, the two types of techniques discussed above can be combined together, and the corresponding mixed-type PLL is proposed in Fig. 5.35.

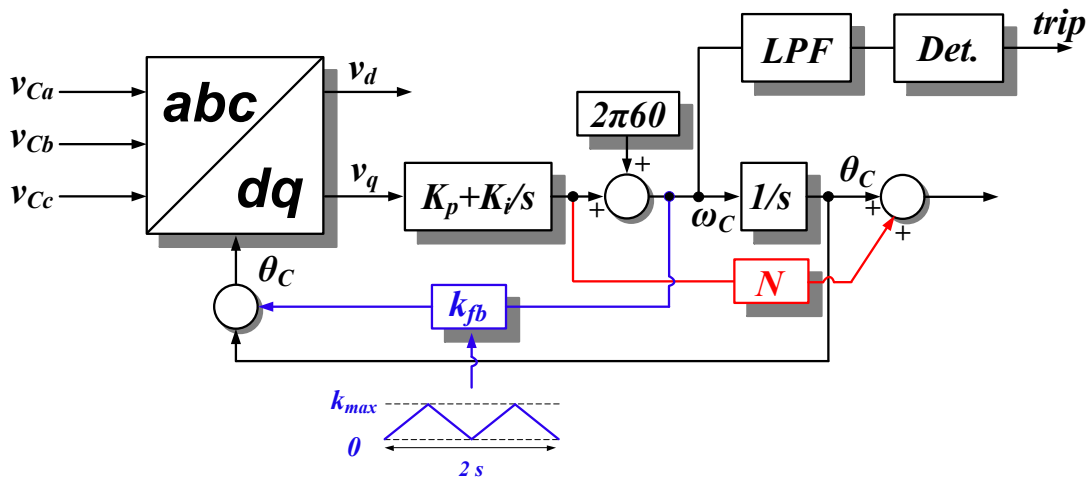


Fig. 5.35: The fifth proposed (mixed-type) PLL system

One of the benefits of the mixed-type PLL is that the large-signal feedback term  $k_{fb}$  can be much smaller to only generate an initial condition value whose impact on output



current power factor is negligible. The second benefit is that the drift speed is always fast enough to achieve anti-islanding protection even under the ideal case.

A simulation using the parameters in Table 5.3 is conducted to compare the fourth PLL and the mixed-type PLL. Both PLLs use  $N = 0.013$ , and the  $k_{max}$  of  $k_{fb}$  in the mixed-type PLL is set as 0.0001. The result shows that the mixed-type PLL presents a faster frequency drift behavior.

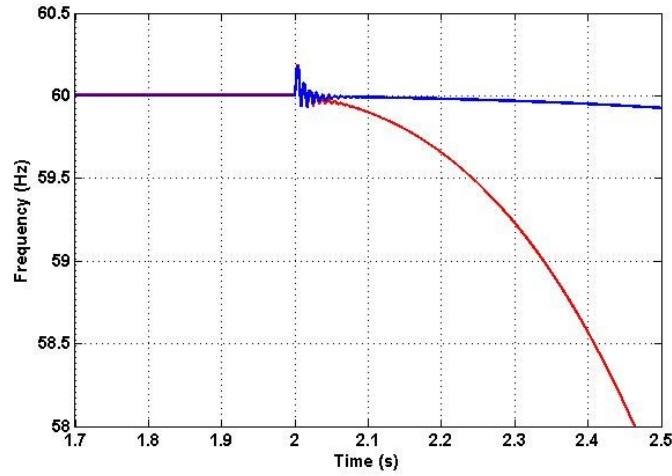


Fig. 5.36: Comparison of the fourth PLL  $\omega_c/2\pi$  (blue) [1 Hz/DIV] and the mixed-type PLL  $\omega_c/2\pi$  (red) [1 Hz/DIV]

The five different implementations of frequency-stability-based PLLs are compared in Table 5.5. The comparisons are based on the aspects of the need for perturbation, the impact on grid-synchronization operation, the detection speed, stability concerns at the grid-tied condition, the compatibility with other grid codes, and operation performance when used with multiple converters.

Table 5.5: Comparison of different islanding-detection methods

	Other methods	Based on large-signal stability		Based on small-signal stability		
		1 <sup>st</sup>	2 <sup>nd</sup>	3 <sup>rd</sup>	4 <sup>th</sup>	5 <sup>th</sup>
Perturbation	Large	Small	Small	No	No	Very small
Impact on PLL operation	Large	Small	Small	No	No	Very small
Detection speed	N/A	Fast	Fast	Fast or Slow	Fast or Slow	Very fast
Stability	N/A	Very small	No	Small	Very small	Very small
LVRT compatibility	N/A	Yes	Yes	Yes	Yes	Yes
Multi-DG	N/A	Not good	Not good	OK	OK	OK

### 5.3.3. EXPERIMENTAL EVALUATION

The small-signal-stability-based islanding-detection methods are tested using the system parameters shown in Table 5.6. According to the load parameters, the small-signal phase-shift term  $k_\phi$  can be calculated as -0.008, and the value for  $N$  is chosen as 0.009 for the test to move the closed-loop pole from the left-half-plane to the right-half-plane. The PI values are  $K_p=1$  and  $K_i=2$ .

Table 5.6: Parameters for islanding-detection test

Ac voltage $V_g$	// $R_L C_L$ load	Switching frequency $f_s$	3 $\Phi$ boost inductor	$k_\phi$	$N$
80 V	10 $\Omega$ +400 $\mu$ F+17.4mH	20 kHz	1.2 mH	-0.008	0.009

Fig. 5.37 shows the typical PLL output when the islanding condition occurs, and it shows that the PLL stays at its equilibrium point. Neither the voltage nor the current change due to the matched load condition, and the system cannot determine the operation condition.

Fig. 5.38 shows the proposed PLL, which introduces an additional small-signal feedback loop. It can be seen that the PLL output starts to drift and follow an exponential curve when the islanding condition occurs. In this test, the PLL drifts upwards, and over/under frequency protection can be triggered to detect the islanding condition.

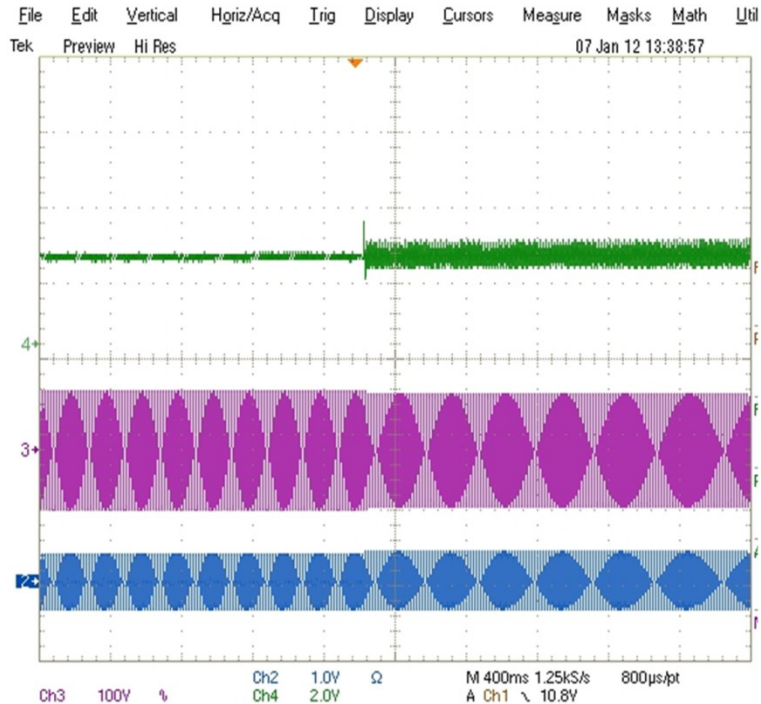


Fig. 5.37: The typical PLL output when the islanding event occurs:  $v_{Ca}$  (purple) [100 V/DIV],  $i_{Ca}$  (blue) [20 A/DIV],  $\omega_C$  (green) [6 Hz/DIV]

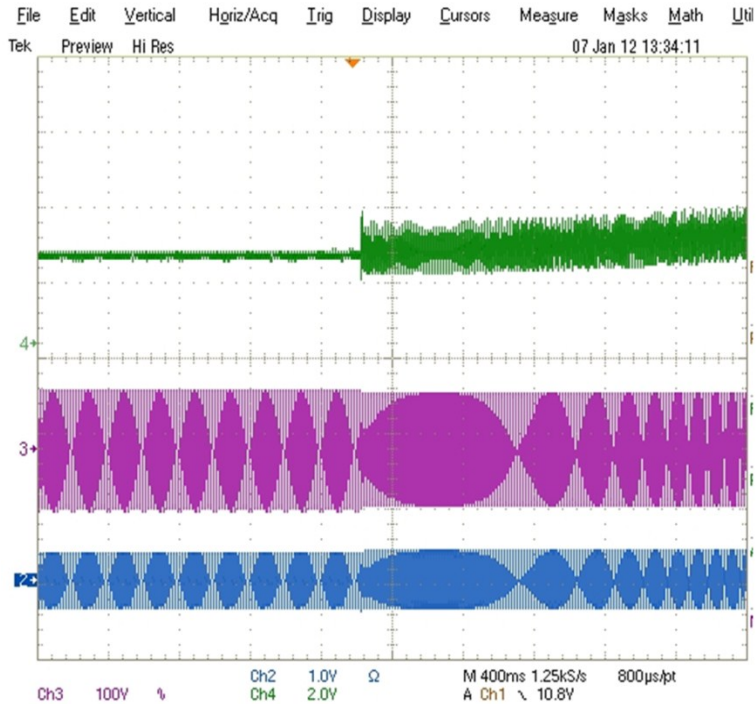


Fig. 5.38: Modified PLL output when the islanding event occurs:  $v_{Ca}$  (purple) [100 V/DIV],  $i_{Ca}$  (blue) [20 A/DIV],  $\omega_C$  (green) [6 Hz/DIV]

### 5.3.4. CONCLUSION

This section presents an islanding-detection algorithm based on the PLL small-signal stability. The small-signal model is used to design an additional feedback or a feedforward loop to move the closed-loop pole from the left-half-plane to the right-half-plane. The design procedure, the PLL performance, and the stability under the grid-connected condition are also discussed. The advantage of these PLL small-signal stability-based solutions over others is the zero perturbation injection, while the uncontrollable detection time presents to be the downside.

## **5.4. EVALUATION FOR MULTI-CONVERTER CONDITIONS**

### **5.4.1. INTRODUCTION**

In many applications, such as an EV charging station or an the ac micro-grid, islanding detection at a multi-converter condition is desired to help with the system-level design. One of the common features of such applications is that lots of ac-dc bus-interface converters and electronic loads are connected geographically close to each other. Thus, the control system of each converter will be coupled together.

One of the interactions would be the PLL loops, and thus the islanding detection will be affected. The first question of islanding-detection at a multi-converter condition is: if the islanding detection function of each inverter complies with the IEEE 1547 standard, does it necessarily mean the islanding detection still works if many of the inverters are tied together?

### **5.4.2. ISLANDING DETECTION PERFORMANCE EVALUATION**

This question can be answered by using the model proposed in the Chapter 4. Two bi-directional inverters in parallel are used as an example as illustrated in Fig. 5.39. Both converters are implemented with the same islanding-detection algorithm. The fourth proposed PLL is chosen and  $N$  is designed such that  $N + k_\varphi = 0.002$ .

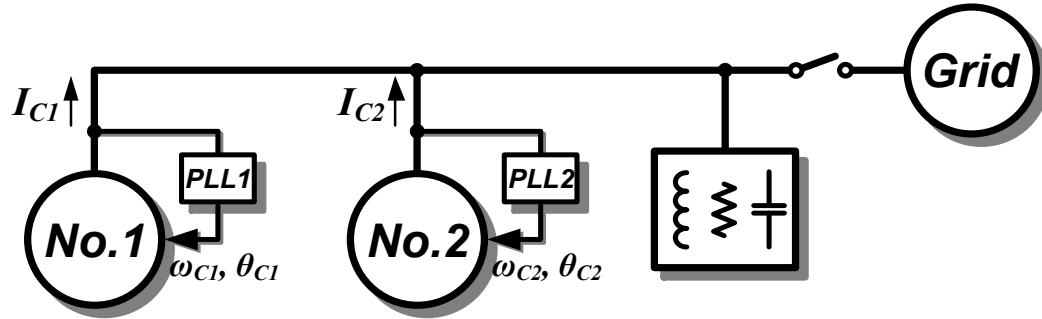


Fig. 5.39: Two bus-interface converters implemented with anti-islanding protection are tied to ac grid

Assuming the parameters in Table 5.7 are used in the system, converter 1 (“fast converter”) has a faster grid-synchronization speed than that of the converter 2 (“slow converter”).

Table 5.7: Simulation parameters for two-converter condition

$V_g$	$I_{C1}+I_{C2}$	$K_{p1}, K_{i1}$	$K_{p2}, K_{i2}$	//RLC	$N+k_\phi$
100 V	50 A	1, 2	0.5, 1	$2 \Omega // 440 \mu\text{F} // 16 \text{mH}$	0.002

As discussed previously, the frequency drift speed can be estimated by the RHP pole locations. If each converter is tested separately, the RHP pole is calculated as in Table 5.8.

Table 5.8: RHP pole locations for two converters

$\omega_{pole \text{ No1}}$	0.5 rad/s @ $I_{C1} = 50 \text{ A}$
$\omega_{pole \text{ No2}}$	0.222 rad/s @ $I_{C2} = 50 \text{ A}$

Chapter 4 shows that three poles determine the converter PLL output frequency dynamics at a two-converter condition. Due to the modification of the PLL, one or more poles will be located in the RHP. Fig. 5.40 shows the result of the fastest RHP pole among three poles under the different combinations of  $I_{C1}$  and  $I_{C2}$ .

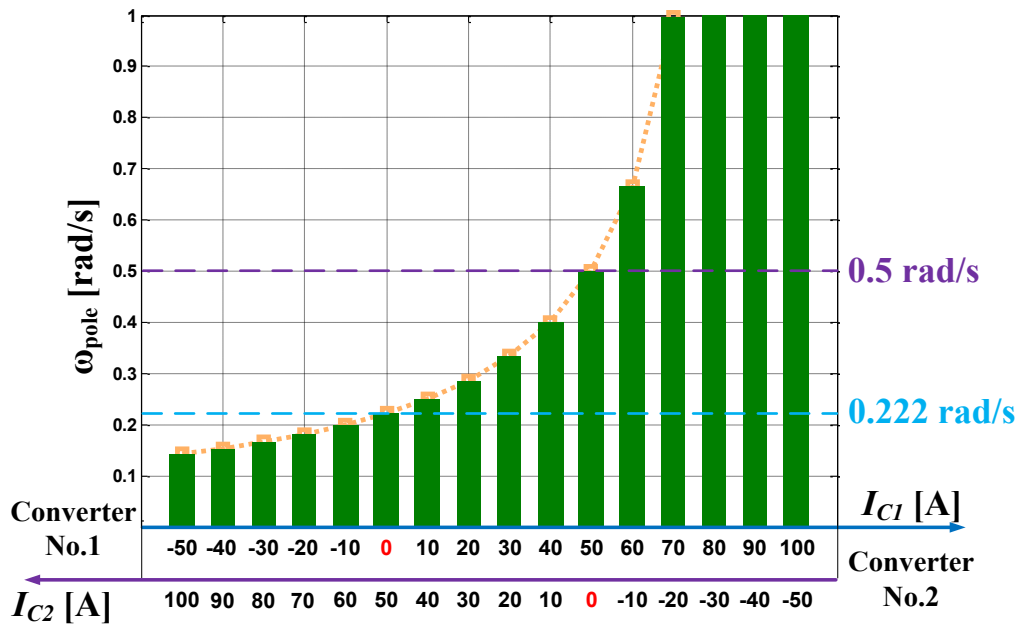


Fig. 5.40: The fastest RHP pole of PLLs with two converters

If both converters inject power to the system, the RHP pole location will be confined between the poles in Table 5.8. It implies that the frequency drift speed is always faster than that of the single converter 2. Thus, the converter 2 can detect the islanding condition within the required clearing time at the two-converter condition.

However, if converter 1 takes the power instead of pumping the power, the RHP pole will be slower. This simply means that the PLL drift rate is slower and the detection time is longer. Therefore, there could be a case when both islanding detections in two converters cannot trigger the protection signal within 2 s at the multi-converter condition.

Contrarily, if converter 2 takes power and converter 1 injects more power, the RHP pole would be even faster, leading to fast islanding detection.

This behavior can be vividly explained by the simulation result in Fig. 5.41. The single-inverter PLL drift speed is much faster than the two-converter condition when the “slow converter” injects the power and the “fast converter” takes the power. This could be a potential problem at a multi-converter condition.

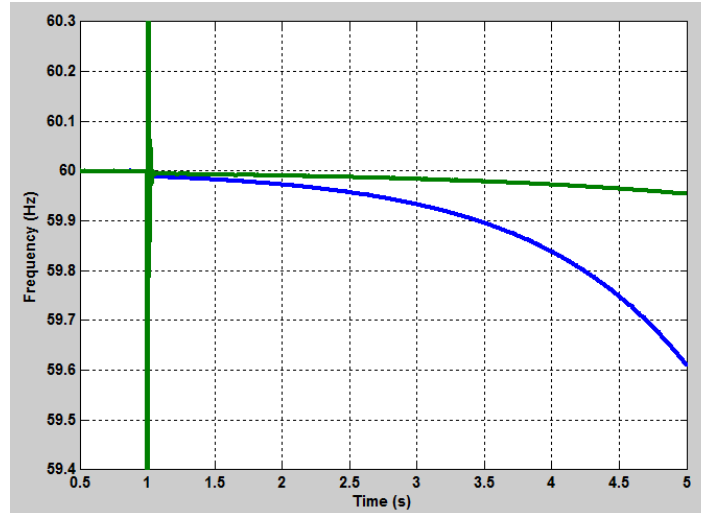


Fig. 5.41: Comparison of No. 1 PLL output for islanding detection between single converter  $\omega_C$  (blue) [0.1 Hz/DIV] and two converters conditions  $\omega_C$  (green) [0.1 Hz/DIV]

One of the ways, as suggested by author, to reduce this impact is to lower the PLL PI parameters or bandwidth, e.g., by half, if any of the converters operate at the rectification mode. The PLL bandwidths in any active front-end rectifier loads have to be lower than source converters’.

Using the conditions in Table 5.7, Fig. 5.42 shows the result when reducing the PI value by half if converter 1 or 2 operates in rectification mode. In this specific case, the RHP pole is guaranteed to be equal to at least 0.222 rad/s. As such, converter 2 is always able to detect the islanding event.

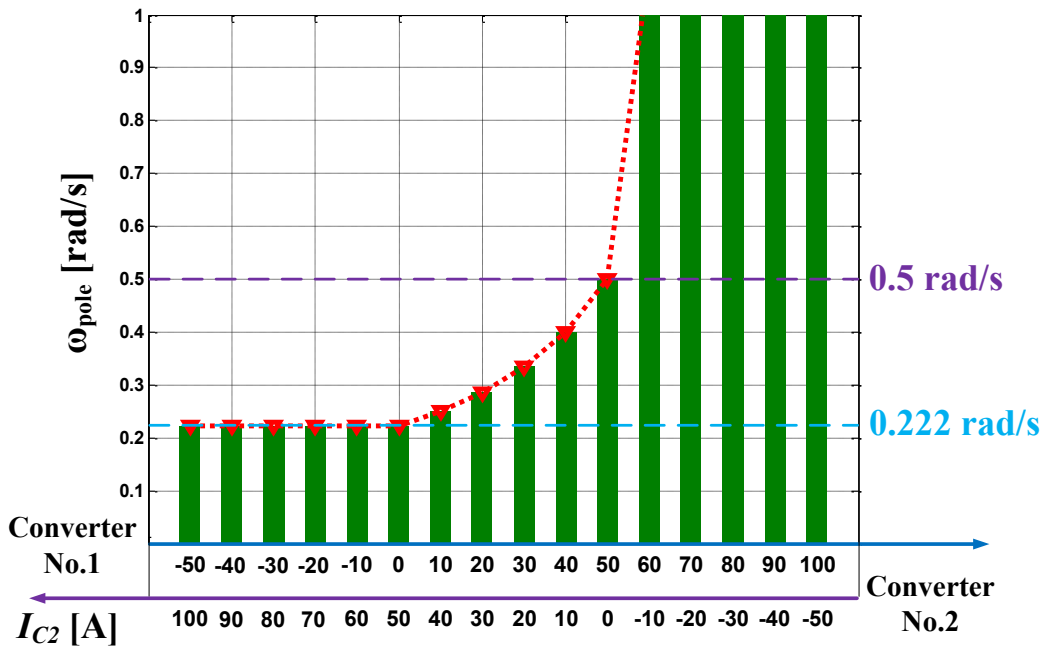


Fig. 5.42: The fastest RPH pole of PLLs at two converter condition

### 5.4.3. CONCLUSION

This section presents an evaluation of the island-detection performance under multiple-converter conditions. The analysis shows that the islanding detection doesn't necessarily fulfill the requirement at the multiple-converter case even if the converters are verified individually. The worst case happens when the "fast converters" take the power or the active front-end rectifier loads in system have a faster synchronization speed than that of the source converters.



## **Chapter 6. CONCLUSIONS AND FUTURE WORK**

This dissertation deals with the ac-dc bi-directional power converters for distributed generation systems and renewable energy systems.

The detailed analyses are presented from Chapter 2 to Chapter 5. This chapter will summarize the work and give the future work.

### **6.1. SUMMARY**

The dissertation first presented the design of an ac-dc bus-interface bi-directional converter system in a residential/commercial dc electronics distribution system. Related issues are addressed; corresponding standards are briefed; the power-stage design considerations are discussed and a digital control system design is given finally.

The dissertation then focuses on the grid synchronization in ac-dc bus-interface converter system. The unstable behaviors of the grid synchronization at the weak grid, islanded condition, and multi-converter condition are found and also explained.

Specifically speaking, the summary and the contributions of the dissertation are listed as follows.

1. The dissertation clearly discusses the impact of the unbalanced ripple power on the dc distributed system operation. The ripple power issue is more severe in the single-phase ac system. The dissertation then proposed a simple two-stage topology as the ac-dc bus-interface bi-directional power converter to effectively decouple the dynamics interactions between the interfaced systems, thereby eliminating the ripple power impact. The dissertation then proposed a design solution to significantly reduce the bulky dc-link capacitor, which improves the power density.

2. Using the single-phase ac-dc bus-interface converter as an example, a bi-directional control system modeling and design procedure are given in the dissertation. The droop control function and over-current protections are imbedded into the control systems as well. Several helpful high-performance control techniques are proposed to

improve the control dynamic response, reduce ac current THD level, and suppress the dc-side ripple level. The detailed control design procedure and considerations will help engineers to design their control system in the similar applications. The design demonstrates that the advanced digital control as well as the power-semiconductors-based converter helps benefit the whole system design, such as providing the fast current-interrupt protection, metering, and communications.

3. A passive plus active power filter solutions are proposed to reduce the leakage current level in the ac-dc bus-interface converters by more than 90%. Combined with the active filter, the proposed solution achieves a overall filter volume minimization. The design trade-off of the proposed filter solution and the physical filter design are given in detail. The proposed solution fits three different types of the ac systems. With the help of the proposed solution, the dc-side CM voltage power quality can be maintained under unbalanced polluted ac input conditions.

4. A novel single-phase grid synchronization solution is proposed in this dissertation to achieve a fast dynamics response, a strong immunity to the ac system voltage variation, and a rejection of multiple noises. The proposed solution is easy to implement in the digital platform and gives the capability to monitor the ac voltage amplitude for protection purposes as well. The detailed design is given for engineers to fully understand the trades-off of a grid synchronization system.

5. A comprehensive grid synchronization modeling methodology in the ac-dc power converter system is proposed in dissertation, which basically covers most of the issues raised in previous publications within the similar scope. The conclusions drawn from the proposed methodology helps fully characterize the converter grid synchronization behaviors under different operation conditions, including the weak grid, the islanded condition, the multi-converter condition, and even more-sophisticated conditions. The proposed methodology can explain the behaviors observed from industry. The proposed model provides a strong tool to predict the grid synchronization stability operation and helps engineers to design the grid synchronization system.

6. A complete study of the popular frequency-based islanding detections are given. More than five novel islanding detection algorithms are proposed in the dissertation for

different applications. More importantly, the detailed modeling, design procedure, and the stability discussion are given so that engineers can understand the knowledge of islanding detections clearly and don't need to apply the traditional cut-and-trail design process. This dissertation also covers the analysis and evaluation of islanding detection performance at the multi-converters condition. The related issues are presented and the suggested solutions are given to engineers in the design of the ac micro-grid and nano-grid system.

## 6.2. CONCLUSIONS

Based on the study in the dissertation, several conclusions and suggestions are given to engineers.

1. In the design of power converters for grid applications, such as the ac-dc bus-interface bi-directional converters, the electric distribution power system requirement and the system-level issues should be the primary design objective, which include the impedance shaping for stability consideration, power sharing, protections, multiple modes of operation, and the dynamics decoupling. Engineers cannot solely focus on the efficiency and density improvement of power converters.

2. The seamless bi-directional power flow regulation, fast and accurate fault protections, and the ancillary functions, such as reactive power compensation, active damping, and data acquisitions can be accomplished by the advanced digital control system to replace the expensive electro-mechanical devices and other equipment in the system.

4. Interface design of the converters has to deal with low-frequency to high frequency power quality requirements, such as the voltage ripple level and current THD level, high-frequency harmonics level, and high-frequency EMI compatibility. Power filter currently is still an effective and reliable way to fulfill such power quality requirements. Cost, volume, and the impedance interactions must be concerned and balanced.

5. In the ac electric power system, grid synchronization operation and its stability of the ac-bus interface converters is very critical to securing a reliable system. High penetration of power electronic converters in future grids will result in more instability of

the grid synchronization in converters. This should be of concern by engineers when integrating renewable energy resources.

6. Frequency-based islanding detections are popular nowadays. Any implementations of the frequency-based islanding detection will change the original operation performance, and sometimes may make the converter system more unstable during normal conditions. Engineers need to be aware of this and refer to the results in Chapter 5 when designing such methods.

### **6.3. FUTURE WORK**

Future research may concentrate on the following:

1. The dc electronic system power management strategies among multiple converters, dc stability study, cable design, short-circuit and ground fault protections design, and the grounding solution are all the future work in system-level study.

2. Power topology investigation can be explored based on the two-stage approach to further improve the density and efficiency. For example, the efficiency of both the first-stage and the second-stage converter can be improved by lots of techniques, such as soft-switching, interleaving technologies, and coupled-inductors.

3. The control system can be improved by using more advanced solutions to improve the performance, such as the adaptive digital control.

4. Research efforts can focus on EMI standardization and the EMI filter optimization design for the ac-dc bus-interface converters and future dc system. Integration of DM and CM power filters can be considered as future work to further improve filter density.

5. Grid synchronization analysis can be studied in a more complicated and realistic condition. For example, the governor control of power generations and the constant power regulation loop in converters could be considered. Simpler modeling approaches, such as the “black-box” terminal modeling, can be studied, which is more helpful to engineers when converter parameters are unknown.

6. Future work can also explore more effective and simpler islanding-detection solutions suitable for multi-converter conditions.

## APPENDIX

### A.1 CONTROLLER PARAMETERS

All the controllers in Fig. 3.98 in Chapter 3 are based on the plant's small-signal transfer functions. The designed controllers are shown in Table A.1.

Table A.1: Controller parameters

Controller	Expressions
$H_i$	$H_i = 5 \times 10^7 \frac{(s + 4.67 \times 10^3)(s + 2.67 \times 10^4)}{s(s + 1.2 \times 10^6)(s + 3.25 \times 10^5)}$
$R_i$	$R_i = 1500 \frac{s}{s^2 + 0.001s + (2\pi 60)^2}$
$H_v$	$H_v = 80 \frac{s + 90}{s(s + 300)}$
$H_{ov}$	$H_v = 3789.7 \frac{s + 2.6 \times 10^3}{s(s + 1.24 \times 10^4)}$
$R_{ov}$	$R_i = 100 \frac{s}{s^2 + 0.001s + (2\pi 120)^2}$
$H_{io}$	$H_i = 1.4736 \times 10^6 \frac{(s + 4.4 \times 10^3)(s + 9.65 \times 10^3)}{s(s + 6.37 \times 10^4)(s + 7.77 \times 10^4)}$
$H_{CM}$	$H_{CM} = 1410 \frac{(s + 38.6)(s + 2.65 \times 10^3)}{s(s + 1.9 \times 10^4)(s + 4.07 \times 10^4)}$
$R_{CM}$	$R_{CM} = 0.5 \frac{s}{s^2 + 0.5s + (2\pi 120)^2}$
$A$	$A = 10$
$N$	$N = \frac{s^2 + (2\pi 120)^2}{s^2 + 40s + (2\pi 120)^2}$

### A.2 DERIVATION OF VOLT-SECOND

The derivation of (28) and (29) in Chapter 3 is shown below. The ac-side voltage and current is defined in (1) and (2) under unity-power-factor conditions.

$$V_{ac} = U_s \sin(\omega_o t) \quad (1)$$

$$I_{ac} = I_s \sin(\omega_o t) \quad (2)$$

The delivery of the power consists of two parts: dc average power  $P_{av}$  in (3), and the ripple power  $P_r$  in (A4). Most of the  $P_{av}$  is delivered to the dc-side, and most of the  $P_r$  is absorbed by the dc-link capacitor.

$$P_{av} = \frac{U_s I_s}{2} \quad (3)$$

$$P_r = -\frac{U_s I_s}{2} \cos(2\omega_o t) \quad (4)$$

As shown in Fig. A.1, when the total power ( $P_{av} + P_r$ ) equals the average power ( $P_{av}$ ) as shown in (5), the dc-link voltage reaches the maximum or minimum value. The time when dc-link voltage reaches the maximum value can be obtained by (6).

$$P_{av} + P_r = P_{av} \quad (5)$$

$$\omega_o t = n\pi + \frac{3}{4}\pi, n \in Z \quad (6)$$

The duty-cycle of the full-bridge converter is defined below in (7). The corresponding CM equivalent duty-cycle is defined in (A8).  $M$  is the modulation index.

$$d_{ab} = M \sin(\omega_o t) \quad (7)$$

$$d_{CM} = 0.5(1 - d_{ab}) \quad (8)$$

The CM volt-second is shown in (A9).

$$VS_H = \frac{1}{2} v_{dc} d_{CM} T_s \quad (9)$$

When  $\omega_o t$  equals zero and the value shown in (6), (28) and (29) in Chapter 3 can be obtained, respectively.

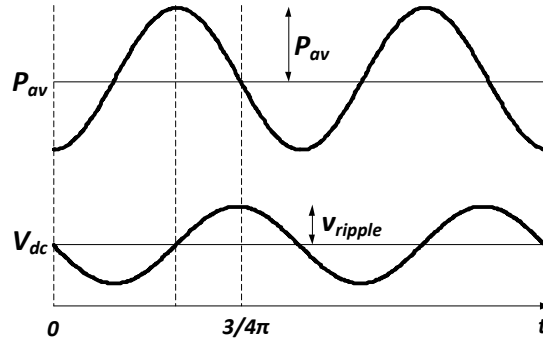


Fig. A.1: Dc-link voltage and delivered ac power waveform

### A.3 SIMULATION FOR GRID-SYNCHRONIZATION STUDY

Matlab Simulink simulation is used to study the frequency behavior in multi-converter condition. Following shows the converter used in the file. The inverter in simulation, as shown in Fig. A.2 has five signals. Three ( $TA$ ,  $TB$ ,  $TC$ ) of them are tied to the grid; another two signals are to monitor the frequency and phase.

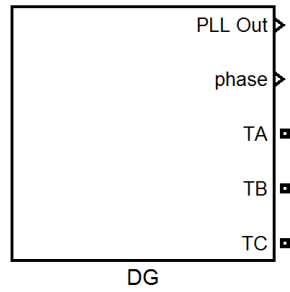


Fig. A.2: Inverter block used in system simulation to study the frequency behavior

Since the DG units behaves as a current source, as shown in Fig. A.3, the inside of the inverter block only includes a PLL loop and a controlled-current source block. The PLL output provides the phase information to the current source block. Also Fig. A.4 shows the inside of the current source. This simple simulation file can be used to study the grid synchronization behaviors without digging out the details of other controllers.

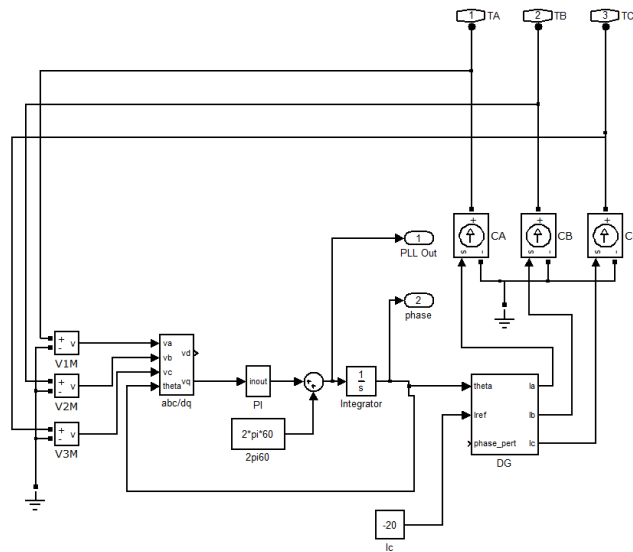


Fig. A.3: Inside of the inverter block

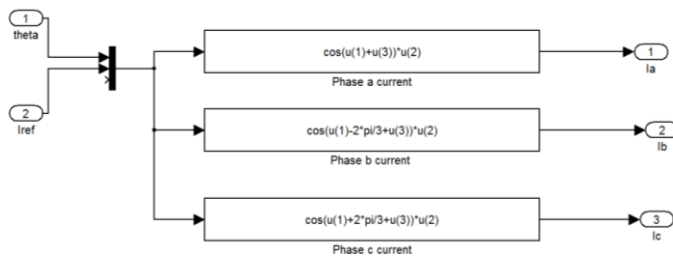


Fig. A.4: Inside of the current source block

## LIST OF REFERENCES

- [1] “Renewable 2010 Global Status Report,” from Renewable Energy Policy Network for the 21st Century (REN21).
- [2] “Renewable 2011 Global Status Report,” from Renewable Energy Policy Network for the 21st Century (REN21).
- [3] “Renewable Energy Consumption and Electricity Preliminary Statistics 2010,” from U.S. Energy Information Administration.
- [4] “The Power and the Glory,” from the Economist 21, June 2008:6.
- [5] “Renewable 2009 Global Status Report,” from Renewable Energy Policy Network for the 21st Century (REN21).
- [6] “World Wind Energy Report 2010,” from World Wind Energy Association, Feb. 2011.
- [7] F. Blaabjerg, A. Consoli, J. A. Ferreira, and J. D. van Wyk, "The Future of Electronic Power Processing and Conversion," IEEE Trans. Power Electronics, vol. 20, pp. 715-720, 2005.
- [8] P. K. Steimer, "Enabled by High Power Electronics - Energy Efficiency, Renewables and Smart Grids", in International Power Electronics Conference, 2010, pp. 11-15.
- [9] P. K. Steimer, "Power electronics, a Key Technology for Future More Electrical Energy Systems", in IEEE Energy Conversion Congress and Exposition, 2009, pp. 1161-1165.
- [10] K. J. Dyke, N. Schofield, and M. Barnes, "The Impact of Transport Electrification on Electrical Networks", IEEE Trans. Industrial Electronics, vol. 57, pp. 3917 - 3926, 2010.
- [11] N. G. Hingorani and L. Gyugyi: Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems. New York: IEEE Press, 2000.
- [12] X. P. Zhang, L. Yao, B. Chong, C. Sasse, and K. R. Godfrey, “FACTS and HVDC Technologies for the Development of Future Power Systems,” in International Conference on Future Power Systems, 2005, pp. 1-6.
- [13] M. E. Baran and N. R. Mahajan, “DC Distribution for Industrial Systems: Opportunities and Challenges,” IEEE Trans. Industry Applications, vol. 39, pp. 1596-1601, 2003.
- [14] D. Salomonsson and A. Sannino, “Low-Voltage DC Distribution System for Commercial Power Systems with Sensitive Electronic Loads,” IEEE Trans. Power Delivery, vol. 22, pp. 1620-1627, 2007.
- [15] D. Boroyevich, I. Cvetkovic, Dong Dong, et al., “Future Electronic Power Distribution Systems A contemplative review,” in 12th International Conference on Optimization of Electrical and Electronic Equipment, 2010, pp. 1-6.



- [16] S. M. Amin and B. F. Wollenberg, "Toward a Smart Grid: Power Delivery for the 21st Century," *IEEE Power and Energy Magazine*, vol. 3, pp. 34-41, 2005.
- [17] "Annual Energy Outlook 2009 with Projections to 2030," for US Department of Energy, Mar. 2009.
- [18] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power Electronics as Efficient Interface in Dispersed Power Generation Systems," *IEEE Trans. Power Electronics*, vol. 19, pp. 1184-1194, 2004.
- [19] G. F. Reed, B. M. Grainger, H. Bassi, E. Taylor, Z. H. Mao, and A. K. Jones, "Analysis of High Capacity Power Electronic Technologies for Integration of Green Energy Management," in *IEEE Transmission and Distribution Conference and Exposition*, 2010, pp. 1-10.
- [20] G. J. Schaeffer and P. Vaessen, "Future Power System Transition – Step into the Light," in *International Conference on Future Power Systems*, 2005, pp. 1-6.
- [21] Y. Xue, K. C. Divya, G. Griepentrog, M. Liviu, and S. Suresh, "Towards Next Generation Photovoltaic Inverters," in *IEEE Energy Conversion Congress and Exposition*, 2011, pp. 2467-2474.
- [22] Q. Wang, Y. Zhang, and Y. Min, "Study on Inter-area Oscillation Frequency of Power Systems," in *International Conference on Power System Technology*, 2006, pp. 914-921.
- [23] K. Kurohane, T. Senjyu, Y. Yonaha, A. Yona, T. Funabashi, and C. H. Kim, "A Distributed DC Power System in an Isolated System," in *IEEE International Symposium on Industrial Electronics*, 2009, pp. 1-6.
- [24] M. Sautreuil, N. Retiere, D. Riu, and O. Sename, "A Generic Method for Robust Performance Analysis of Aircraft DC Power Systems," in *IEEE Annual Conference of Industrial Electronics*, 2008, pp. 49-54.
- [25] X. Liu, P. Wang, and P. C. Loh, "A Hybrid Ac/Dc Microgrid and its Coordination Control," *IEEE Trans. Smart Grid*, vol. 2, pp. 278-286, 2011.
- [26] C. D. Xu and K. W. E Cheng, "A Survey of Distributed Power System – Ac Versus Dc Distributed Power System," in *International Conference on Power Electronics Systems and Applications*, 2011, pp. 1-12.
- [27] M. A. Masrur, D. S. Sitar, and V. A. Sankaran, "Can an AC (Alternating Current) Electrical System Replace the Present DC System in the Automobile? An Investigation Feasibility Study – Part I: System Architecture," *IEEE Trans. Vehicular Technology*, vol. 47, pp. 1072-1080, 1998.
- [28] K. Techakittiroj and V. Wongpaibool, "Co-existence Between AC-distribution and DC-distribution: in the view of Appliances," in *International Conference on Computer and Electrical Engineering*, 2009, pp. 421-425.
- [29] M. M. Amin, M. A. Elshaer, and O. A. Mohammed, "Dc Bus Voltage Control for PV Sources in a DC Distribution System Infrastructure," in *IEEE Power and Energy Society General Meeting*, 2010, pp. 1-5.

- [30] M. E. Baran and N. R. Mahajan, "DC Distribution for Industrial Systems: Opportunities and Challenges," *IEEE Trans. Industry Applications*, vol. 39, pp. 1596-1602, Nov. 2003.
- [31] J. Schonberger, R. Duke, and S. D. Round, "DC-Bus Signaling: A Distributed Control Strategy for a Hybrid Renewable Nanogrid," *IEEE Trans. Industrial Electronics*, vol. 53, pp. 1453-1460, 2006.
- [32] H. Zhang, F. Mollet, C. Saudemont, and B. Robyns, "Experimental Validation of Energy Storage System Management Strategies for a Local Dc Distribution System of More Electric Aircraft," *IEEE Trans. Industrial Electronics*, vol. 57, pp. 3905-3916, 2010.
- [33] Y. Pan, M. Steurer, and T. L. Baldwin, "Ground Fault Location Testing of a Noise-Pattern-Based Approach on an Ungrounded DC System," *IEEE Trans. Industry Applications*, vol. 47, pp. 996-1002, 2011.
- [34] L. A. S. Ribeiro, O. R. Saavedra, S. L. Lima, and J. G. Matos, "Isolated Microgrids with Renewable Hybrid Generation: The Case of Lencois Island," *IEEE Trans. Sustainable Energy*, vol. 2, pp. 1-11, 2011.
- [35] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage Bipolar-type DC Microgrid for Super High Quality Distribution," *IEEE Trans. Power Electronics*, vol. 25, pp. 3066-3075, 2010.
- [36] G. S. Seo, J. Baek, K. Choi, H. Bae, and B. Cho, "Modeling and Analysis of DC Distribution Systems," in *IEEE International Conference on Power Electronics and ECCE Asia*, 2011, pp. 223-227.
- [37] G. S. Thandi, R. Zhang, K. Xing, F. C. Lee, and D. Boroyevich, "Modeling, Control and Stability Analysis of a PEBB based DC DPS," *IEEE Trans. Power Delivery*, vol. 14, pp. 497-505, 1999.
- [38] H. Zhang, H. Fakham, C. Saudemont, and B. Robyns, "Power Management Strategies in a Local DC Power Distribution System of More Electric Aircraft with the Help of Hybrid Storage and Dissipation Systems," in *International Symposium on Advanced Electromechanical Motion Systems and Electric Drives*, 2009, pp. 1-7.
- [39] K. Yukita, K. Ban, Y. Goto, K. Ichyanagi, K. Hirose, T. Ushirokawa, Y. Okui, and H. Takabayashi, "Power Supply System of DC/AC Micro Grid System," in *IEEE International Conference on Power Electronics and ECCE Asia*, 2011, pp. 228-234.
- [40] L. Han, J. Wang, and D. Howe, "Stability Assessment of Distributed DC Power Systems for More-electric Aircraft," in *IET Conference on Power Electronics, Machines and Drives*, 2008, pp. 661-665.
- [42] K. N. Areerak, S. V. Bozhko, L. Lillo, G. M. Asher, D. W. P. Thomas, A. Watson, and T. Wu, "The Stability Analysis of AC-DC Systems Including Actuator Dynamics for Aircraft Power Systems," in *European Conference on Power Electronics and Applications*, 2009, pp. 1-10.
- [43] R. M. Cuzner and G. Venkataramanan, "The Status of DC Micro-Grid Protection," in *IEEE Industry Applications Society Annual Meeting*, 2008, pp. 1-8.

- [44] D. Salomonsson, L. Soder, and A. Sannino, "Protection of Low-voltage DC Microgrids," *IEEE Trans. Power Delivery*, vol. 24, pp. 1045-1053, 2009.
- [45] D. Salomonsson and A. Sannino, "Centralized ac/dc Power Conversion for Electronic Loads in a Low-voltage dc Power System," in *IEEE Power Electronics Specialists Conference*, 2006, pp. 1-7.
- [46] J. P. Brozek, "DC Overcurrent Protection – Where We Stand," *IEEE Trans. Industry Applications*, vol. 29, pp. 1029-1032, 1993.
- [47] A. Kwasinski, "Quantitative Evaluation of DC Microgrids Availability: Effects of System Architecture and Converter Topology Design Choices," *IEEE Trans. Power Electronics*, vol. 26, pp. 835-851, 2011.
- [48] T. F. Wu, Y. K. Chen, G. R. Yu, and Y. C. Chang, "Design and Development of DC-Distributed System with Grid Connection for Residential Applications," in *IEEE International Conference on Power Electronics and ECCE Asia*, 2011, pp. 235-241.
- [49] A. Q. Huang, M. L. Crow, G. T. Heydt, J. P. Zheng, and S. J. Dale, "The Future Renewable Electric Energy Delivery and Management (FREEDM) System: The Energy Internet," *Proceedings of the IEEE*, pp. 133-148, 2011.
- [50] P. Cairolì, I. Kondratiev, and R. Dougal, "Ground Fault Protection for DC Bus using Controlled Power Sequencing," in *IEEE Southeast Conference*, 2010, 234-237.
- [51] D. J. Becker, "Dc Microgrids in Buildings and Data Centers," in *IEEE Telecommunications Energy Conference*, 2011, pp. 1-7.
- [52] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single Phase Power Factor Correction: a Survey," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 749-755, 2003.
- [53] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM Regenerative Rectifiers: State of the Art," *IEEE Trans. Industrial Electronics*, vol. 52, pp. 5-22, 2005.
- [54] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Industrial Electronics*, vol. 57, pp. 2553-2580, 2010.
- [55] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Industrial Electronics*, vol. 54, pp. 2930-2945, 2007.
- [56] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. M. Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Trans. Industrial Electronics*, vol. 53, pp. 1002-1016, 2006.
- [57] Y. Zhang, Y. Tang, J. Li, J. Shi, and L. Ren, "Superconducting Magnet Based VSC Suitable for Interface of Renewable Power Sources," *IEEE Trans. Applied Superconductivity*, vol. 20, pp. 880-883, 2010.
- [58] S. Zhang, K. J. Tseng, D. M. Vilathgamuwa, T. D. Nguyen, and X. Y. Wang,

- “Design of a Robust Grid Interface System for PMSG-Based Wind Turbine Generators,” *IEEE Trans. Industrial Electronics*, vol. 58, pp. 316-328, 2011.
- [59] T. Bhattacharya, V. S. Giri, K. Mathew, and L. Umanand, “Multiphase Bidirectional Flyback Converter Topology for Hybrid Electric Vehicles,” *IEEE Trans. Industrial Electronics*, vol. 56, pp. 78-84, 2009.
- [60] Y. Xue, L. Chang, S. Kjaer, J. Bordonau, and T. Shimizu, “Topologies of Single-phase Inverters for Small Distributed Power Generators: An Overview,” in *IEEE Trans. Power Electronics*, vol. 19, pp. 1305-1314, 2004.
- [61] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A Review of Single-phase Grid-Connected Inverters for Photovoltaic Modules,” in *IEEE Trans. Industry Applications*, vol. 41, pp. 1292-1306, 2005.
- [62] J. Walter and R. W. De Doncker, “High-power Galvanically Isolated DC/DC Converter Topology for Future Automobiles,” in *IEEE Annual Power Electronics Specialist Conference*, 2003, pp. 27–32.
- [63] J. B. Klaassens, “Steady-state Analysis of a Series-resonant DC-DC Converter with a Bipolar Power Flow,” *IEEE Trans. Industrial Electronics*, vol. 36, pp. 48–55, Feb. 1989.
- [64] K. Wang, F. C. Lee, and J. Lai, “Operation Principles of Bi-directional Full-bridge DC/DC Converter with Unified Soft-switching Scheme and Soft-starting Capability,” in *IEEE Applied Power Electronics Conference and Exposition*, 2000, pp. 111–118.
- [65] L. Zhu, K. Wang, F. C. Lee, and J.-S. Lai, “New Start-up Schemes for Isolated Full-bridge Boost Converters,” *IEEE Trans. Power Electronics*, vol. 18, pp. 946–951, 2003.
- [66] H. Xiao and S. Xie, “A ZVS Bidirectional DC-DC Converter with Phase Shift Plus PWM Control Scheme,” *IEEE Trans. Power Electronics*, vol. 23, pp. 813–823, 2008.
- [67] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, “Performance Characterization of a High-power Dual Active Bridge DC-to-DC Converter,” *IEEE Trans. Industry Applications*, vol. 28, pp. 1294–1301, 1992.
- [68] S. Inoue and H. Akagi, “A Bidirectional DC-DC Converter for an Energy Storage System with Galvanic Isolation,” *IEEE Trans. Power Electronics*, vol. 22, pp. 2299–2306, 2007.
- [69] R. W. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, “A Three-phase Soft-switched High-power-density DC/DC Converter for High-power Applications,” *IEEE Trans. Industry Applications*, vol. 27, pp. 63–73, 1991.
- [70] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, “Transformerless Inverter for Single-phase Photovoltaic Systems,” *IEEE Trans. Power Electronics*, vol. 22, pp. 693–697, 2007.
- [71] T. Kerekes, M. Liserre, R. Teodorescu, C. Klumpner, and M. Summer, “Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies,” *IEEE*

Trans. Power Electronics, vol. 24, pp. 2202-2211, 2009.

[72] B. Chen, P. Sun, C. Liu, C. Chen, J. Lai, and W. Yu, "High Efficiency Transformerless Photovoltaic Inverter with Wide-range Power Factor Capability," in IEEE Applied Power Electronics Conference and Exposition, 2012, pp. 575-582.

[73] M. Chen, X. Lee, and Y. Tsutomu, "A Novel Soft-switching Grid-connected PV Inverter and Its Implementation," in IEEE Power Electronics and Drive Systems, 2011, pp. 373-378.

[74] D. Zhang, Q. Zhang, A. Grishina, A. Amirahmadi, H. Hu, J. Shen, and I. Batarseh, "A Comparison of Soft and Hard-switching Losses in Three-phase Micro-Inverters," in IEEE Energy Conversion Congress and Exposition, 2011, pp. 1076-1082.

[75] T. Shimizu, Y. Jin, and G. Kimura, "DC Ripple Current Reduction on a Single-Phase PWM Voltage-Source Rectifier," IEEE Trans. on Industrial Applications, vol. 36, pp. 1419-1428, 2000.

[76] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM Converter Power Density Barriers," in IEEE 2007 Power Conversion Conference, 2007, pp. 455-452.

[77] R. Wang, F. Wang, R. Lai, P. Ning, R. Burgos, and D. Boroyevich, "Study of Energy Storage Capacitor Reduction for Single Phase PWM Rectifier," in IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 1177-1183.

[78] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-Dimensional Space Vector Modulation for Four-Leg Voltage-Source Converters," IEEE Trans. Power Electronics, vol. 17, pp. 314-326, 2002.

[79] R. Teichmann and S. Bernet, "A Comparison of Three-Level Converters Versus Two-Level Converters for Low-Voltage Drives, Traction, and Utility Applications," IEEE Trans. Industry Applications, vol. 41, pp. 855-865, 2005.

[80] R. Zhang, S. Hiti, F. C. Lee, and D. Boroyevich, "A Three-phase ZVT Boost Rectifier with Improved Analog Controller," in IEEE Power Electronics Specialists Conference, 1996, pp. 469-474.

[81] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A Review of Single-phase Grid-connected Inverters for Photovoltaic Modules," IEEE Trans. Industry Applications, vol. 41, pp. 1292-1306, 2005.

[82] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A New High-Efficiency Single-Phase Transformerless PV Inverter Topology," IEEE Trans. Industrial Electronics, vol. 58, pp. 184-191, 2011.

[83] Victor, M. et al., US Patent Application, Publication Number US 2005/0286281 A1, 29 Dec. 2005.

[84] Schmid, H. et al., UP Patent 7046534, issued 16 May 2006.

[85] Hantschel, J., German Patent Application, Publication Number DE102006010694 A1, 20 Sept. 2007.

[86] Gonzalez, S. R. et al., International Patent Application, Publication Number

WO2008015298, 2 July 2007.

- [87] E. Un and A. H. Have, "A Near-State PWM Method With Reduced Switching Losses and Reduced Common-Mode Voltage for Three-phase Voltage Source Inverters," *IEEE Trans. Industry Applications*, vol. 45, pp. 782-793, 2009.
- [88] R. M. Tallam, R. J. Kerkman, D. Leggate, and R. A. Lukaszewski, "Common-Mode Voltage Reduction PWM Algorithm for AC Drives," *IEEE Trans. Industry Applications*, vol. 46, pp. 1959-1969, 2010.
- [89] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo, and F. C. Camboim, "Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-phase Photovoltaic Systems," *IEEE Trans. Industrial Electronics*, vol. 57, pp. 1360-1368, 2010.
- [90] A. M. Have and E. Un, "Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison with Standard PWM Methods for Three-phase Voltage-Source Inverters," *IEEE Trans. Power Electronics*, vol. 24, pp. 241-252, 2009.
- [91] D. Hamza and P. Jain, "Conducted EMI in Grid-tied PV System," in *International Telecommunications Energy Conference*, 2010, pp. 1-7.
- [92] M. C. Di Piazza, C. Serporta, G. Tine, and G. Vitale, "Electromagnetic Compatibility Characterization of the DC-side in a Low Power Photovoltaic Plant," in *IEEE International Conference on Industrial Technology*, 2004, pp. 672-677.
- [93] H. Uarberlin, "New DC-LISN for EMC Measurement on the DC side of PV Systems: Realisation and First Measurement at Inverters," in *European Photovoltaic Solar Energy Conference*, 2001.
- [94] R. Araneo, S. Lammens, G. Marco, and S. Bertone, "EMC Issues in High-Power Grid-Connected Photovoltaic Plants," *IEEE Trans. Electromagnetic Compatibility*, vol. 51, pp. 639-648, 2009.
- [95] Fang Luo, Xuning Zhang, D. Boroyevich, P. Mattavelli, J. Xue, "On discussion of AC and DC side EMI Filters Design for Conducted Noise Suppression in DC-fed Three Phase Motor Drive System," in *IEEE Applied Power Electronics Conference and Exposition*, 2011, pp. 667-672.
- [96] Y. Maillet, R. Lai, S. Wang, F. Burgos, and D. Boroyevich, "High-Density EMI Filter Design for Dc-Fed Motor Drives," *IEEE Trans. Power Electronics*, vol. 25, pp. 1163-1172, 2010.
- [97] H. Akagi and T. Shimizu, "Attenuation of Conducted EMI Emissions from an Inverter-Driven Motor," *IEEE Trans. Power Electronics*, vol. 23, pp. 282-290, 2008.
- [98] T. Wang, Z. Ye, S. Gautam, and X. Yuan, "Output Filter Design for a Grid-interconnected Three-phase Inverter," in *IEEE Power Electronics Specialists Conference*, 2003, pp. 779-784.
- [99] D. A. Rendusara and P. N. Enjeti, "An Improved Inverter Output Filter Configuration Reduces Common and Differential Modes dv/dt at the Motor Terminals in PWM Drive Systems," *IEEE Trans. Power Electronics*, vol. 13, pp. 1135-1143, 1998.

- [100] F. Luo, D. Boroyevich, P. Mattavelli, "Improving EMI Filter Design with in Circuit Impedance Mismatching," in IEEE Applied Power Electronics Conference and Exposition, 2012, pp. 1652-1658.
- [101] G. C. Hsieh and J. C. Hung, "Phase-Locked Loop Technique. A survey," IEEE Trans. Industrial Electronics, vol. 43, pp. 609-615, Dec. 1996.
- [102] Se-Kyo Chung, "A Phase Tracking System for Three Phase Utility Interface Inverters," IEEE Transactions on Power Electronics, vol. 15, pp. 431-438, 2000.
- [103] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," IEEE Trans. Industrial Electronics, vol. 53, pp. 1398-1409, 2006.
- [104] A. Timbus, R. Teodorescu, F. Blaabjerg, and M. Liserre, "Synchronization Methods for Three Phase Distributed Power Generation Systems, An Overview and Evaluation," in IEEE Power Electronics Specialists Conference, 2005, pp. 2474-2481.
- [105] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions," IEEE Trans. Industrial Electronics, vol. 58, pp. 127-138, 2011.
- [106] V. Kaura and V. Blasko, "Operation of a Phase Locked Loop System under Distorted Utility Conditions," IEEE Trans. Industry Applications, vol. 33, pp. 58-63, 1997.
- [107] J. Suonan, W. Shao, G. Song, and Z. Jiao., "A Novel Single-phase Adaptive Reclosure Scheme for Transmission Lines with Shunt Reactors," IEEE Trans. Power Delivery, vol. 24, pp. 545-551, 2009.
- [108] M. A. Perez, J. R. Espinoza, L. A. Moran, M. A. Torres, and E. A. Araya, "A Robust Phase-Locked Loop Algorithm to Synchronize Static-Power Converters with Polluted AC systems," IEEE Trans. Industrial Electronics, vol. 55, pp. 2185-2192, 2008.
- [109] T. Thacker, R. Wang, Dong Dong, R. Burgos, F. Wang, and D. Boroyevich, "Phase-Locked Loops using State Variable Feedback for Single-phase Converter Systems," in IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 864-870.
- [110] T. Thacker, D. Boroyevich, R. Burgos, and F. Wang, "Phase-Locked Loop Noise Reduction via Phase Detector Implementation for Single-phase Systems," IEEE Trans. Industrial Electronics, vol. 58, pp. 2482-2490, 2011.
- [111] J. Sun, "Impedance-Based Stability Criterion for Grid-Connected Inverters," IEEE Trans. Power Electronics, vol. 26, pp. 3075-3078, 2011.
- [112] B. Wen, D. Boroyevich, P. Mattavelli, Z. Shen, and R. Burgos, "Experimental Verification of the Generalized Nyquist Stability Criterion for Balanced Three-phase Ac Systems in the Presence of Constant Power Loads," in IEEE Energy Conversion Congress and Exposition, 2012.
- [113] M. A. Pai, D. P. Sen Gupta, and K. R. Padiyar, "Small-signal Analysis of Power Systems," Alpha Science International, 2004.

- [114] Z. Ye, R. Walling, L. Garces, R. Zhou, L. Li, and T. Wang, "Study and Development of Anti-islanding Control for Grid-Connected Inverters," NREL/SR-560-36243, 2004.
- [115] M. Cespedes and J. Sun, "Renewable Energy Systems Instability Involving Grid-Parallel Inverters," in IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 1971-1977.
- [116] J. C. Vasquez, J. M. Guerrero, A. Luna, and P. Rodriguez, "Adaptive Droop Control Applied to Voltage-Source Inverters Operating in Grid-Connected and Islanded Modes," IEEE Trans. Industrial Electronics, vol. 36, pp. 4088-4096, 2009.
- [117] H. H. Zeineldin, "A Q-f droop Curve for Facilitating Islanding Detection of Inverter-Based Distributed Generation," IEEE Trans. Power Electronics, vol. 24, pp. 665-673, 2009.
- [118] A. Seon-Ju, P. Jin-Woo, C. I-Yop, M. Seung-I, K. Sang-Hee, and N. Soon-Ryul, "Power-sharing Method of Multiple Distributed Generators Considering Control Modes and Configurations of a Microgrid," IEEE Trans. Power Delivery, vol. 25, pp. 2007-2016, 2010.
- [119] R. Majumder, B. Chaudhuri, A. Ghosh, R. Majumder, G. Ledwich and F. Zare, "Improvement of Stability and Load Sharing in an Autonomous Microgrid using Supplementary Droop Control Loop," IEEE Trans. Power Systems, vol. 25, pp. 796-808, 2010.
- [120] J. E. Kim and J. S. Hwang, "Islanding detection method of distributed generation units connected to power distribution system," in International Conference on Power System Technology, 2000, pp. 643-647.
- [121] K. A. Nigim and Y. G. Hegazy, "Intention islanding of distributed generation for reliability enhancement," in IEEE Power Engineering Society General Meeting, 2003, pp. 2446-2451.
- [122] T. Thacker, F. Wang, R. Burgos, and D. Boroyevich, "Implementation of control and detection algorithms for utility interfaced power conversion systems," in IEEE Applied Power Electronics Conference and Exposition, 2006, pp. 1745-1750.
- [123] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, IEEE Std. 1547-2003.
- [124] IEEE Application Guide for IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, IEEE Std. 1547.2-2008.
- [125] H. Zeineldin, E. F. El-Saadany, and M. M. A Salama, "Intentional Islanding of Distributed Generation," in IEEE Power Engineering Society General Meeting, 2005, pp. 1496-1502.
- [126] H. Zeineldin, E. F. El-Saadany, and M. M. A Salama, "Impact of DG interface control on islanding detection and nondetection zones," IEEE Trans. on Power Delivery, vol. 21, pp. 1515-1523, 2006.
- [127] S. I. Jang and K. H. Kim, "Development of a Logical Rule-based Islanding Detection Method for Distributed Resources," in IEEE Power Engineering Society



Winter Meeting, 2002, pp. 800-806.

[128] S. I. Jang and K. H. Kim, "An Islanding Detection Method for Distributed Generations using Voltage Unbalance and Total Harmonic Distortion of Current," *IEEE Trans. Power Delivery*, vol. 19, pp. 745-752, 2004.

[129] H. H. Zeineldin, E. F. El-Saadany, and M. M. A. Salama, "Islanding detection of inverter-based distributed generation," *IEE Proceedings of Generation, Transmission and Distribution*, vol. 153, pp. 644-652, 2006.

[130] T. Thacker, F. Wang, R. Burgos, and D. Boroyevich, "Implementation of control and detection algorithms for utility interfaced power conversion systems," in *Applied Power Electronics Conference and Exposition*, 2006.

[131] C. Jeraputra and P. N. Enjeti, "Development of a Robust Anti-islanding Algorithm for Utility Interconnection of Distributed Fuel Cell Powered Generation," *IEEE Trans. Power Electronics*, vol. 19, pp. 1163-1170, 2004.

[132] L. A. C. Lopes and H. Sun, "Performance assessment of active frequency drifting islanding detection methods," *IEEE Trans. Energy Conversion*, vol. 21, pp. 171-180, 2006.

[133] M. J. Ko, I. Choy, J. Choi, K. Lee, and G. Yu., "Simulation of Active Frequency Drift Adding Zero Current Method for Islanding Detection," in *Power Electronics Specialists Conference*, 2006, pp. 1-5.

[134] F. De Mango, M. Liserre, and A. Dell'Aquila, "Overview of Anti-islanding Algorithms for PV Systems. Part II: Active methods," in *12th International Power Electronics and Motion Conference*, 2006, pp. 1884-1889.

[135] W. Bower and M. Ropp, "Evaluation of Islanding Detection Methods for Utility-Interactive Inverters in Photovoltaic Systems," SANDIA Report SAND2002-3591.

[136] Y. Jung, J. Chio, B. Yu, J. So, and G. Yu, "A Novel Active Frequency Drift Method of Islanding Prevention for the Grid-Connected Photovoltaic Inverter," in *IEEE Power Electronics Specialists Conference*, 2005, pp. 1915-1921.

[137] M. Ciobotaru, V. Agelidis, and R. Teodorescu, "Accurate and Less-Distributing Active Anti-islanding Method Based on PLL for Grid-connected PV Inverters," in *IEEE Power Electronics Specialists Conference*, 2008, pp. 4569-4576.

[138] "Islanding Detection Method" US. Patent No. 2006/0146582 A1.

[139] "System and Method for Islanding Detection" US Patent No. 6850074 B2.

[140] "Islanding Detection and Protection Method" US Patent No. 7275002 B2.

[141] "Islanding Detection Apparatus for A Distributed Generation Power System and Detection Method" US Patent No. 7843082 B2.

[142] "Islanding Detection in an Electrical Power Delivery System" US Patent No. US 2010/0286838 A1.

[143] "Method for Detecting Islanding Operation of a Distributed Generator," US Patent No. US 2008/0204044 A1.

- [144] "Anti-islanding Device and Method for Grid Connected Inverters Using Random Noise Injection" US Patent No. 2003/0165036 A1.
- [145] "Anti-islanding Techniques for Distributed Power Generation" US Patent No. 7138728 B2.
- [146] "Inverter Anti-islanding Method" US. Patent No. 7432618 B2.
- [147] "System and Method for Anti-islanding, such as Anti-islanding for a Grid-connected Photovoltaic Inverter" US Patent No. 2008/0122293 A1.
- [148] "Method and Area Electric Power System Detection Islanding by Employing Controlled Reactive Power Injection by a Number of Inverters" US Patent No. 2011/0115301 A1.
- [149] "Power Signaling based Technique for Detecting Islanding Conditions in Electric Power Distribution Systems," US Patent No. 7304403 B2.
- [150] "Detection of Islanding in Power Grids" US Patent No. 7376491 B2.
- [151] "Device and Method for Detecting Islanding Operation of a Static Power Source" US Patent No. 2003/0147191 A1.
- [152] "Method and Apparatus for Anti-islanding Protection of Distributed Generations" US Patent No. 2006/0004531 A1
- [153] "Method and Apparatus for Anti-islanding of Distributed Power Generation Systems," US Patent No. 7899632 B2.
- [154] T. G. Wilson Sr., "The Evolution of Power Electronics," IEEE Trans. Power Electronics, vol. 15, pp. 439-446, 2000.
- [155] N. G. Hingorani, "Power Electronics in Electric Utilities: Role of Power Electronics in Future Power Systems," Proceedings of IEEE, vol. 76, pp. 481-482, 1988.
- [156] V. C. Gungor, D. Sahin, T. Kocak, S. Ergut, C. Buccella, C. Cecati, and G. P. Hancke, "Smart Grid Technologies: Communication Technologies and Standards," IEEE Trans. Industrial Informatics, vol. 7, pp. 529-539, 2011.
- [157] A. Fukui, T. Takeda, K. Hirose, and M. Yamasaki, "HVDC Power Distribution Systems for Telecom Sites and Data Centers," in IEEE International Power Electronics Conference, 2010, pp. 874-880.
- [158] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," IEEE Trans. Power Electronics, vol. 24, pp. 592-602, 2009.
- [159] J. Bryan, R. Duke, and S. Round, "Decentralized Generator Scheduling in a Nanogrid using DC Bus Signaling," in IEEE Power Engineering Society General Meeting, 2004, pp. 977-982.
- [160] P. Karlsson and J. Svensson, "DC Bus Voltage Control for a Distributed Power System," IEEE Trans. Power Electronics, vol. 18, pp. 1405-1412, 2003.
- [161] W. Zhang, D. Dong, I. Cvetkovic, F. C. Lee, and D. Boroyevich, "Lithium-based Energy Storage Management for Dc Distributed Renewable Energy System," in IEEE

Energy Conversion Congress and Exposition, 2011, pp. 3270-3277.

[162] X. Zhou, J. Li, Z. Liang, A. Huang, and S. Bhattacharya, "The Issue of Plug-in Hybrid Electric Vehicles' Grid Integration and Its Control Solution," in IEEE Energy Conversion Congress and Exposition, 2010, pp. 3596-3603.

[163] D. Dong, T. Thacker, R. Burgos, D. Boroyevich, F. Wang, and B. Giewont, "Control Design and Experimental Verification of a Multi-Function Single-Phase Bidirectional PWM Converter for Renewable Energy Systems," in European Conference on Power Electronics and Applications, 2009, pp.1-10.

[164] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, "A Unity Power Factor PWM Rectifier with DC Ripple Compensation," IEEE Trans. on Industrial Applications, vol. 44, pp. 447-455, 1997.

[165] J. P. Gegner, C. Y. Hung, and C. Q. Lee, "High Power Factor AC-to-DC Converter Using a Reactive Shunt Regulator," in IEEE Power Electronics Specialists Conference, 1994, pp. 349-355.

[166] H. Fujita, "A Single-Phase Active Filter Using an H-Bridge PWM Converter With a Sampling Frequency Quadruple of the Switching Frequency," IEEE Trans. on Power Electronics, vol. 24, pp. 2882-2888, 2009.

[167] T. Ninomiya, Jin Chun-feng, M. Shoyama, and T. Ohmae, "Line-harmonics Reduction Techniques for Consumer Electronics and Low-Power Electronic Equipment," in IEEE Annual Conference of the Industrial Electronics Society, 2000. pp. 766-770.

[168] A. Cid-Pastor, L. Martinez-Salamero, A. EI Aroudi, and D. Hernando-Ureta, "Analysis of a Modular One-phase PV Inverter," in IEEE International Multi-Conference on System, Signal and Devices, 2009, pp. 1-5.

[169] Z. Zhao, M. Xu, Q. Chen, J. Lai, Y. Cho, "Derivation of Boost-buck Converter Based High-efficiency Robust PV Inverter," in IEEE Energy Conversion Congress and Exposition, 2010, pp. 1479- 1484.

[170] C. Zhou and M. M. Jovanovic, "Design Trade-offs in Continuous Current-Mode Controlled Boost Power-Factor Correction Circuits," in Proc. 1992 Virginia Power Electronics Seminar, pp. 57-68.

[171] R. B. Ridley, "Average Small-Signal Analysis of the Boost Power Factor Correction Circuit," in Proc. VPEC Power Electronics Seminar, 1989, pp. 108-120.

[172] D. Dong, "Modeling and Control Design of a Bidirectional PWM Converter for Single-phase Energy Systems," Master Thesis, Virginia Tech, 2009.

[173] B. H. Chowdhury, "Power Quality," IEEE Potentials, vol. 20, pp. 5-11, 2001.

[174] M. M. Morcos and J. C. Gomez, "Electric Power Quality – The Strong Connection with Power Electronics," in IEEE Power and Energy Magazine, 2003, pp. 18-25, 2003.

[175] B. Kroposki, C. Pink, R. DeBlasio, H. Thomas, M. Simoes, and P. K. Sen, "Benefits of Power Electronics Interfaces for Distributed Energy Systems," IEEE Trans. Energy Conversion, vol. 25, pp. 901-908, 2010

- [176] “Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems,” IEEE Std. 1547.1-2005.
- [177] “Photovoltaic (PV) Systems – Characteristics of the Utility Interface,” IEC 61727 Ed. 2, 2004.
- [178] “CISPR 14-1 Electromagnetic Compatibility – Requirement for Household Appliances, Electric Tools and Similar Apparatus – Part 1: Emission,” IEC Std. 2009.
- [179] “Safety of Information Technology Equipment Including Electrical Business Equipment,” IEC Std. 950.
- [180] “Electromagnetic Compatibility (EMC) – Part 3-2: Limits – Limits for Harmonic Current Emissions (Equipment Input Current < 16 A per Phase),” IEC Std. 61000-3-2, 2005.
- [181] “Environmental Conditions and Test Procedures for Airborne Equipment,” RTCA DO-160E Std. 2004.
- [182] L. Shi, A. Meintz, and M. Ferdowsi, “Single-phase Bidirectional ac-dc Converters for Plug-in Hybrid Electric Vehicle Applications,” in IEEE Vehicle Power and Propulsion Conference, 2008, pp. 1-5.
- [183] I. Cvetkovic, T. Thacker, Dong Dong, and et al. “Future Home Uninterruptible Renewable Energy System with Vehicle-to-grid Technology,” in IEEE Energy Conversion Congress and Exposition, 2009, pp. 2675-2681.
- [184] O. Lopez, R. Teodorescu, F. Freijedo, and J. D. Gandoy, “Leakage Current Evaluation of a Single-phase Transformerless PV Inverter Connected to the Grid,” in IEEE Applied Power Electronics Conference, 2007, pp. 907-912.
- [185] “Safety of Power Converters for Use in Photovoltaic Power Systems—Part 1: General requirement,” IEC Std. 62109-1-2007.
- [186] S. M. Araujo, P. Zacharias, and R. Mallwitz, “Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems,” IEEE Trans. Industrial Electronics, vol. 57, pp. 3118-328, 2010.
- [187] J. M. A. Myrzik and M. Calais, “String and Module Integrated Inverters for Single-phase Grid Connected Photovoltaic Systems – A review,” in IEEE Power Tech Conference, 2003.
- [188] Huafeng Xiao, Shaojun Xie, “Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter,” IEEE Trans. Electromagnetic Compatibility, vol. 52, pp. 902-913, 2010.
- [189] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications and Design, 2<sup>nd</sup> edition, New York: Wiley, 1995.
- [190] W. Kolar, J. Biela, and J. Minibock, “Exploring the Pareto Front of Multi-objective Single-phase PFC Rectifier Design Optimization – 99.2% Efficiency vs. 7kW/din<sup>3</sup> Power Density,” in IEEE Power Electronics and Motion Control Conference, 2009, pp. 1-21.
- [191] H. Kim and K. H. Kim, "Filter Design for Grid Connected PV Inverters," in IEEE

International Conference on Sustainable Energy Technologies, 2008, pp.1070-1075.

[192] E. Twining and D. G. Holmes, "Grid Current Regulation of a Three-Phase Voltage Source Inverter With an LCL Input Filter," *IEEE Trans. Power Electronics*, vol. 18, pp. 888-895, 2003.

[193] D. G. Holmes, T. A. Lipo, "Pulse Width Modulation for Power Converters: Principles and Practice," Wiley-IEEE Press, 2003.

[194] R. S. Lai and K. D. T. Ngo, "A PWM Method for Reduction of Switching Loss in a Full-bridge Inverter," *IEEE Trans. Power Electronics*, vol. 10, pp. 326-332, 1995.

[195] Y. Wu, M. A. Shafi, A. M. Knight, and R. A. McMahon, "Comparison of the Effects of Continuous and Discontinuous PWM Schemes on Power Losses of Voltage-Sourced Inverters for induction Motor Drives," *IEEE Trans. Power Electronics*, vol. 26, pp. 182-191, 2011.

[196] M. J. Nave, "On Modeling the Common Mode Inductor," in *IEEE International Symposium on Electromagnetic Compatibility*, 1991, pp. 452-457.

[197] J. K. Steinke, "Use of an LC Filter to Achieve a Motor-friendly Performance of the PWM Voltage Source Inverter," *IEEE Trans. Energy Conversion*, vol. 14, pp. 649-654, 1999.

[198] Fang Luo, Shuo Wang, Fei Wang, and et al., "Analysis of CM Volt-second Influence on CM Inductor Saturation and Design for Input EMI Filters in Three-phase DC-Fed Motor Drive Systems," *IEEE Trans. Power Electronics*, vol. 25, pp. 1905-1914, 2010.

[199] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A New Single-phase PLL Structure Based on Second Order Generalized Integrator," in *IEEE Power Electronics Specialists Conference*, 2006, pp. 1-6.

[200] B. Y. Bae and H. Byung-Moon, "Novel 3-phase Phase-Locked Loop Composed of Adaptive Linear Combiner," in *European Conference on Power Electronics and Applications*, 2007, pp. 1-10.

[201] S. M. Silva, B. M. Lopes, B. J. C. Filho, and et al., "Performance Evaluation of PLL Algorithms for Single-phase Grid-connected Systems," in *IEEE Industry Applications Conference*, 2004, pp. 2259-2263.

[202] M. Cacciato, A. Consoli, R. Attanasio, and F. Gennaro, "Soft-Switching Converter with HF Transformer for Grid-Connected Photovoltaic Systems," *IEEE Trans. Industrial Electronics*, vol. 57, pp. 1678-1686, 2010.

[203] K. D. Brabandere, T. Loix, K. Engelen, B. Bolsens, J. Van den Keybus, J. Driesen, and R. Belmans, "Design and Operation of a Phase-Locked Loop with Kalman Estimator-based Filter for Single-phase Applications," in *IEEE Industrial Electronics Society Conference*, 2007, pp. 525-530.

[204] M. Saitou and T. Shimizu, "Generalized Theory of Instantaneous Active and Reactive Powers in Single-phase Circuits based on Hilbert Transform," in *IEEE Power Electronics Specialists Conference*, 2002, pp. 1419-1424.

- [205] R. M. Santos Filho, P. F. Sixas, P. C. Cortizo, L. A. Torres, and A. F. Souza, "Comparison of Three Single-phase PLL Algorithms for UPS Applications," *IEEE Trans. Industrial Electronics*, vol. 55, pp. 2923-2932, 2008.
- [206] L. G. Rolin, D. R. da Costa, and M. Aredes, "Analysis and Software Implementation of a Robust Synchronization PLL Circuit based on pq Theory," *IEEE Trans. Industrial Electronics*, vol. 53, pp. 1919-1926, 2006.
- [207] W. F. Egan, *Phase-Lock Basics*, 2<sup>nd</sup> ed.: WileyIEEE Press, 2007.
- [208] J. R. C. Piqueira, A. Z. Caligares, and L. H. A. Monteiro, "Considering Double Frequency Terms from Phase Detectors in Synchronous Master-slave Networks," in 38<sup>th</sup> Southeastern Symposium on System Theory, 2006, pp. 453-356.
- [209] R. E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, 6<sup>th</sup> ed.: McGraw Hill, 2007.
- [210] F. Gardner, *Phase Lock Technique*, 2<sup>nd</sup> ed.: Wiley-IEEE Press, 2007.
- [211] Z. Ye, A. Kolwalkar, Y. Zhang, P. Du, and R. Walling, "Evaluation of Anti-islanding Schemes based on Nondetection Zone Concept," *IEEE Trans. Power Electronics*, vol. 19, pp. 1171-1176.
- [212] T. Thacker, F. Wang, R. Burgos, and D. Boroyevich, "Islanding Detection Using a Coordinate Transformation Based Phase-Locked Loop," in *IEEE Power Electronics Specialists Conference*, 2007, pp. 1151-1156.
- [213] T. Thacker, R. Burgos, F. Wang, and D. Boroyevich, "Single-phase Islanding Detection Based on Phase-Locked Loop Stability," in *IEEE Energy Conversion Congress and Exposition*, 2009, pp. 3371-3377.
- [214] I. Y. Chung and S. I. Moon, "A New Islanding Detection Method using Phase-Locked Loop for Inverter-Interfaced Distributed Generators," *Journal of Electrical Engineering & Technology*, vol. 2, pp. 165-171, 2007.
- [215] X. Wang, W. Freitas, "Impact of Positive-Feedback Anti-Islanding Methods on Small-Signal Stability of Inverter-Based Distributed Generation," *IEEE Trans. Energy Conversion*, vol. 23, pp. 923-931, 2008.
- [216] P. Du, Z. Ye, E. Aponte, and et al., "Positive-Feedback-Based Active Anti-Islanding Schemes for Inverter-Based Distributed Generators: Basic Principle, Design Guideline and Performance Analysis," *IEEE Trans. Power Electronics*, vol. 25, pp. 2941-2948, 2010.
- [217] D. Velasco, C. Trujillo, G. Garcera, and E. Figueres, "An Active Anti-Islanding Method Based on Phase-PLL Perturbation," *IEEE Trans. Power Electronics*, vol. 26, pp. 1056-1066, 2011.
- [218] L. A. C. Lopes and Y. Zhang, "Islanding Detection Assessment of Multi-Inverter Systems with Active Frequency Drifting Methods," *IEEE Trans. Power Delivery*, vol. 23, pp. 480-486, 2008.
- [219] H. H. Zeineldin and S. Conti, "Sandia Frequency Shift Parameter Selection for Multi-inverter Systems to Eliminate Non-detection Zone," *IET Trans. Renewable Power*

Generation, vol. 5, pp. 1750183, 2011.

[220] W. Han, T. Zaheng, and X. Wang, "Investigation of Multi-inverter Distributed Generation Resident Sandia Frequency Shift Anti-islanding Method," in IEEE International Conference on Advanced Power System Automation and Protection, 2011, pp. 935-939.

[221] IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems, IEEE Std. 1547.1-2005.

[222] C. T. Lee, R. P. Jiang, and P. T. Cheng, "A Grid Synchronization Method for Droop Controlled Distributed Energy Resources Converters," in IEEE Energy Conversion Congress and Exposition, 2011, pp. 743-749.

[223] M. Cespedes, J. Sun, "Impedance Shaping of Three-phase Grid-parallel Voltage-source Converters," in IEEE Applied Power Electronics Conference and Exposition, 2012, pp. 754-760.

[224] C. L. Chen, Y. Wang, J. S. Lai, Y. S. Lee, and D. Martin, "Design of Parallel Inverters for Smooth Mode Transfer Microgrid Applications," IEEE Trans. Power Electronics, vol. 25, pp. 6-15, 2010.