ANALYSIS OF INDUCTOR-COUPLED ZERO-VOLTAGE-TRANSITION CONVERTERS

Jae-Young Choi

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Dushan Boroyevich, Chair

Fred C. Lee

Jason J. Lai

Jacobus D. Van Wyk

Douglas J. Nelson

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(ABSTRACT)

As is the case for DC-DC converters, multi-phase converters require both high-quality power control and high power-density. Although a higher switching frequency not only improves the quality of the converter output but also decreases the size of the converter, it increases switching losses and electromagnetic interference (EMI) noise. Since the soft-switching topologies reduce the switching losses of the converter main switches, the topologies make converters partially independent from the switching frequency. However, the conventional soft-switching topologies have already proposed most of the possible ways to improve converter performance. In addition, the trends of the newly generated power devices reduce the advantages of soft-switching topologies. This critical situation surrounding soft-switching topologies gives research motivations: What features of soft-switching topologies facilitate their practical applications? Given this motivation, the dissertation discusses two aspects – simplifying auxiliary circuits and accounting for the effects of soft-switching operations on the converter control.

Engineers working with medium- and high-power multi-phase converters require simplified soft-switching topologies that have the same level of performance as the conventional soft-switching topologies. This demand is the impetus behind one of the research objectives – simplifying the auxiliary circuits of Zero-Voltage-Transition (ZVT) inverters. Simplifying the auxiliary circuits results in both a smaller number of and lower cost for auxiliary components, without any negative impact on performance. This dissertation proposes two major concepts for the simplification – the Single-Switch Single-Leg (S^3L) ZVT cell and the Phase-Lock (PL) concept.

Throughout an effort to eliminate circulating currents of inductor-coupled (IC) ZVT converters, the S^3L ZVT cell is developed. The proposed cell allows a single auxiliary switch to achieve zero-voltage conditions for both the top and bottom main switches, and it achieves the same level of performance as the conventional ZVT cell, as well. This proposal makes IC ZVT topologies more attractive to multi-phase converter applications.

Because all of the top main switches generally have identical sequences for zero-voltage turn-on commutations, one auxiliary switch might handle the commutations of all of the top main switches. This possibility introduces the PL concept, which allows the two auxiliary switches to provide a zero-voltage condition for any main switch commutation. In order to compensate for restrictions of this concept, a modified space-vector modulation (SVM) scheme also is introduced.

A soft-switching topology changes the duty ratios of the converter, which affects the controllability of the converter. Therefore, this dissertation selects resolution of this issue as one of the research objectives. This dissertation derives the generalized timing equations of ZVT operations, and the generalized equations formulize the effect of ZVT operation on both duty ratios and DC current. Moreover, the effect of SVM schemes is also investigated. An average model of the ZVT converter is developed using both the timing analysis and the investigation of SVM schemes, and small-signal analysis using the average model predicts the steady-state characteristics of the converter.

To my wife and daughters

with my love

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Chapter 1. INTRODUCTION

One of the largest areas of Power Electronics, multi-phase converter applications can be largely classified to two groups: rectifiers and inverters. The inverters are used for two distinct applications: connecting to utility lines and controlling motors. As with DC-DC converter applications, all multi-phase converters require both high-quality power control and high power density. Among several factors that affect these requirements, the switching frequency of converters is one of the most effective ones. Higher switching frequency not only improves the quality of the converter output but also achieves the low profile of the converter, because it can reduce the size of passive components. Therefore, both the rectifiers and the inverters for utility applications have commonly used the highest possible switching frequency. However, the higher switching frequency has trade-offs in terms of increases in both switching losses and electromagnetic interference (EMI) noise. Particularly in medium- and high-power applications, the trade-offs become more critical, because the converters in the power ranges generally use IGBTs as main power devices.

Even inverters for motor control applications have begun to increase their switching frequencies. So far, inverters for motor control applications do not require high switching frequencies, due to the load motors' high inductances and large inertias. Recently, many applications, especially electric vehicle (EV) applications require high-torque motors. To properly control the load motors, the switching frequency of the inverters must increase. On the other hand, inverter-driven motors have more serious problems: motor losses and degradation. Traditionally, only the fundamental-frequency resistances of motor are considered as loss factors. However, several research papers have proposed high-frequency resistance terms of inverter-driven motors [F1-F4]. In general, inverters are connected to motors with long lead wires. High *dv/dt* generated by the inverter PWM controls creates high spike in side the motor, which damages the motor insulation [F5-F7]. This motor degradation can be improved by using lower *dv/dt*.

Soft-switching topologies have been hot issues since the first was disclosed to the Power Electronics engineering field. Quite a few research projects have developed new

soft-switching topologies to both improve the converter efficiency and to reduce the EMI and device stresses [A1-A10, B1-B16, C1-C39]. Not only for DC-DC converter applications, but also for multi-phase converter applications, a variety of soft-switching topologies have been proposed to improve performances [B1-B16, C1-C39]. Since the soft-switching topologies reduce the switching losses of the converter's main switches, the topologies render converters partially independent from switching frequencies. Soft-switching topologies are now one of the most viable solutions for increasing switching frequency. In addition, the *dv/dt* value reduced using soft-switching topologies improves the motor efficiency [D13] and insulation.

The soft-switching topologies of multi-phase converters can be divided into two large groups: DC-side soft-switching topologies [B1-B16] and AC-side soft-switching topologies [C1-C39]. The DC-side topologies are advantageous in the simplicity of their auxiliary circuits, which are comprised of only one or two auxiliary switches. The AC-side soft-switching topologies can be further divided into two groups: AC-side Zero-Voltage-Transition (ZVT) topologies [C2-C13, C15-C20, C22-C30, C32, C34-C35, C38] and AC-side Zero-Current-Transition (ZCT) topologies [A10, C1, C14, C21, C31, C33, C36-C37, C39]. Because the improved ZCT topologies [A10, C14, C31, C33] allow both the soft turn-on and the soft turn-off, their commutation characteristics are better than those of the other soft-switching topologies. The AC-side ZVT topologies have characteristics good enough to meet not only the demand for high efficiency and low EMI noise, but also those for load adaptability [D1-D18].

Even though all of the soft-switching topologies have strengths that could improve converter performance, they also have some weaknesses and restrictions. In particular, the AC-side soft-switching topologies have such complicated structures that their auxiliary circuits require high cost and large space. These disadvantages make engineers hesitant to apply these topologies, although there are great benefits [D17]. For three-phase converters, there have been several research projects aimed at developing AC-side soft-switching topologies with simplified auxiliary circuits [C5-C6, C10, C12-C13, C15]. These topologies make it possible to decrease the requirements of both cost and space. However, these topologies still have some restrictions, and even create several critical disadvantages that worsen the converter performances in some applications. Section 1.1

reviews the literature related to conventional soft-switching topologies, and briefly reveals the characteristics of the topologies.

Conventional soft-switching topologies have already suggested most of the possible ways to improve converter performance. In addition, the trends of newly generated power devices reduce the effects of soft-switching topologies. This critical situation surrounding soft-switching topologies offers the motivation for this research: What features of soft-switching topologies allow for their practical applications? Given this motivation, Section 1.2 discusses two research directions – simplifying auxiliary circuits and accounting for the effects of soft-switching operations on the converter control. Section 1.3 introduces the major proposals of this dissertation.

1.1 CONVENTIONAL THREE-PHASE SOFT-SWITCHING TOPOLOGIES

Conventional soft-switching topologies in three-phase converter applications can be grouped as follows: DC-side ZVT converters, AC-side ZVT converters, and AC-side ZCT converters. This section investigates those characteristics of the three groups, which motivate this research and proposes the research directions as well.

1.1.1 DC-Side ZVT Converters

Since the earliest version of this kind of topology was published [B1], many papers have proposed improved performances and control [B2-B16]. Even with their different power stages and control methods, all topologies have common characteristics: They periodically drop entire DC link voltage to zero, and all auxiliary components are connected only to the DC side. Unlike AC-side soft-switching topologies, the DC-side ZVT topologies generally have only one auxiliary switch and one resonant tank regardless of the number of phases. These simple structures make DC-side topologies very attractive in multi-phase converter applications. However, most of them require specialized modulation method and have a power factor restriction. The switching frequency of the specialized modulation is much higher than that of general pulse width modulation (PWM) schemes. The power factor restriction makes the topologies impossible to use in some motor drive applications. Three outstanding topologies are introduced as follows.

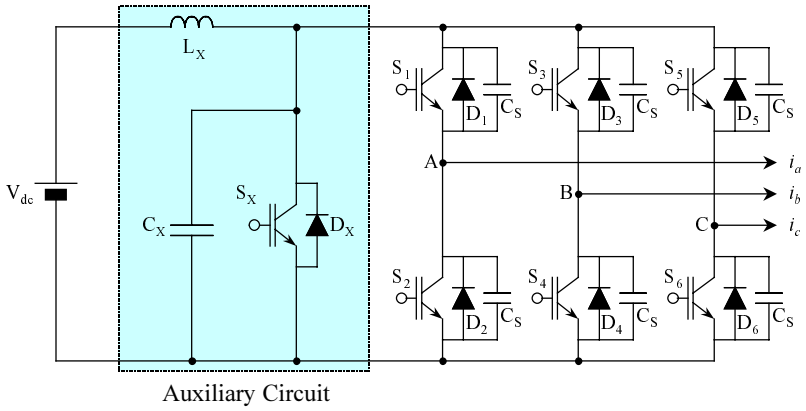
- **Resonant DC Link (RDCL) converter** [B1-B4]: This topology has been a basic concept for most other DC-side ZVT topologies. Figure 1.1 (a) shows the power stage of the topology, the auxiliary circuit of which consists of one auxiliary switch (S_X) and a resonant tank that includes one inductor (L_X) and one capacitor (C_X). L_X and C_X create resonance with the operation of S_X. Whenever the voltage across C_X drops to zero, the main switches can change their switching statuses with zero-voltage conditions. Because conventional SVM schemes cannot optimize this resonant operation, the RDCL converter uses a family of delta modulations called Sigma-Delta modulation [B2]. Since main switches suffer

from at least twice the DC input voltage, the Active-Clamped RDCL (ACRL) converter limits the high DC link voltage using an active-clamping circuit [B3-B4]. This topology generates significant harmonics of between a quarter and a half the DC link resonant frequency. Therefore, the DC link resonant frequency should be at least four times the switching frequency of conventional PWM schemes in order to achieve the same performance.

- **DC Notch Commutated PWM converter** [B7]: A DC notch commutated PWM converter uses an advanced active-clamping method. Figure 1.1 (b) shows its power stage. The clamped DC link voltage generally reaches 1.3 times the DC input voltage. Unlike the ACRL converter, this topology controls the pre-charging level so that the circulating energy can be minimized. Furthermore, this topology can work with a modified SVM scheme. However, the auxiliary switch turns on and off with hard-switching conditions. There are high-frequency harmonics at both the DC link voltage and the resonant inductor current.

- **Passive Clamped Quasi-Resonant Link (PCQRL) converter** [B11-B12]: This topology is one of the latest in DC-side ZVT topologies. Figure 1.1 (c) shows its power stage. Instead of an active-clamping circuit, a magnetic coupling between L_{X1} and L_{X3} provides clamped DC link voltage. This clamped voltage generally reaches 1.3 times the DC input voltage. L_{X1} and L_{X2} create a zero-voltage condition for the resonant capacitors across the main switches. In addition, the magnetizing coupling between L_{X1} and L_{X2} provides a zero-current condition for the turn-off of clamp switch S_X. However, the voltage stress of the clamping diode is twice the DC input voltage, and the power stage is more complicated than other DC-side ZVT converters.

Since the introduction of the first topology [B1], their performance has been improved tremendously. However, even the latest topology has several performance issues. First, the modified SVM scheme always has synchronized turn-on commutations just after a zero switching-state vector (SSV). However, some power factors require separate commutations in one switching cycle. Due to a wide range of power factors in motor drive applications, DC-side ZVT topologies cannot always achieve zero-voltage



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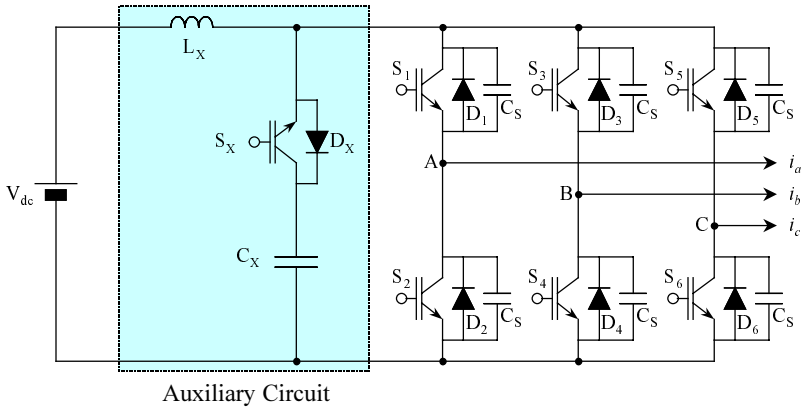

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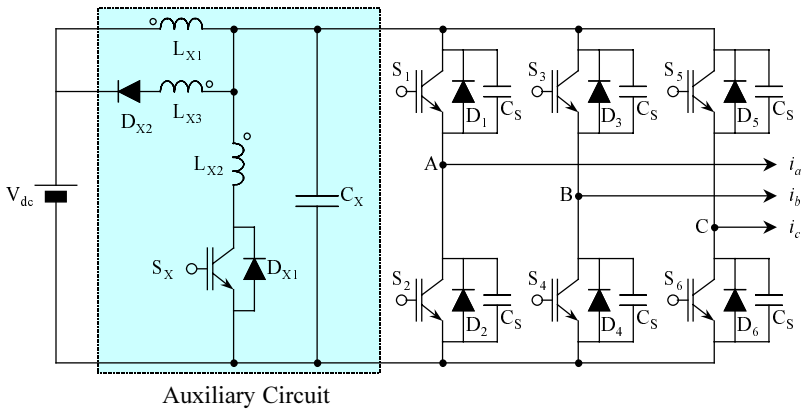


(c)

Figure 1.1 Power stages of DC-side ZVT converters:

(a) RDCL three-phase converter,

(b) DC Notch Commutated PWM three-phase converter, and

(c) PCQRL three-phase converter.

turn-on commutations. Second, auxiliary circuits of these topologies cannot assist the commutation from switch to diode when the load current is small. Therefore, a large snubber capacitance that reduces main switch turn-off losses is not acceptable. Third, any type of DC-side ZVT converters has an auxiliary resonant inductor between the DC power source and the main bridges, as shown in Figure 1.1. Since the inductor is in the main power path, it always generates conduction loss proportional to the load currents, which is not insignificant amount.

1.1.2 AC-Side ZVT Converters

AC-side ZVT topologies have characteristics good enough to meet not only the requirements for high efficiency and low device stresses, but also those for load adaptability. For three-phase converter applications, however, these topologies have such complicated structures that their auxiliary circuits are large and expensive. These disadvantages make engineers hesitant to apply ZVT topologies with six auxiliary switches, although there are great benefits [D17].

In order to reduce the cost and space of the auxiliary circuit, there have been several research projects aimed at developing ZVT topologies with simplified auxiliary circuits [C5-C6, C10, C12-C13, C15]. These topologies make it possible to decrease the requirements for both cost and space. Although their performances are as good as the ZVT topologies with six auxiliary switches in rectifier applications, the topologies create several critical disadvantages in the inverter applications.

A. AC-Side ZVT Converters with Six Auxiliary Switches

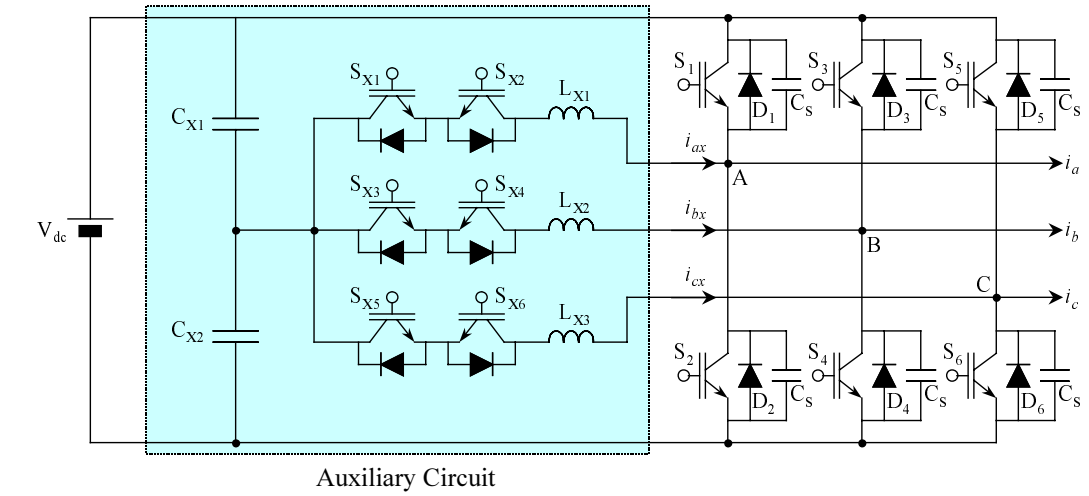
This kind of ZVT converter topology has been one of the main branches in soft-switching research [C2-C13, C15-C20, C22-C26, C28-C29]. Each topology has its benefits and appropriate power ranges. Because IGBTs are used as auxiliary switches in the motor drive converters for medium- and high-power applications, the ZVT topologies should minimize losses in the auxiliary circuits as well as minimize the turn-on losses of the main switches. Otherwise, the ZVT topologies may even decrease efficiency, and thus become useless. Based on these requirements, the next paragraphs investigate three groups of AC-side ZVT topologies.

- **Auxiliary Resonant Commutated Pole (ARCP) Converters** [B5, C2-C3, C7, C9, C11, C18-C19, C22, C28]: Figure 1.2 (a) shows the power stage of an ARCP three-phase converter. One auxiliary pole consists of two auxiliary switches and a resonant inductor. Using the midpoint of DC voltage allows this topology to achieve zero-current turn-off of the auxiliary switches as well as zero-voltage turn-on of the main switches. While this topology has excellent performance, there are several problems related to the midpoint of DC voltage. When the DC input voltage is not high, the resonant inductance cannot be large enough to provide proper charging and discharging times. The midpoint fluctuates with the auxiliary circuit operations. Since the original papers proposed the theoretical concept [C2-C3], there have been tremendous efforts to improve the performance and to realize this topology [C7, C9, C11, C18-C19, C22, C28]. However, only a few papers proposed ideas related to controlling the midpoint [C11]. There are three possible ways to control the midpoint: an additional control circuit, a modified switching pattern, or a huge DC capacitance. Even if the additional circuit can control the midpoint well, adding cost is counterproductive. Modifying the auxiliary switching pattern is an effective choice, in spite of the limitation of timing control. In an EV, huge DC capacitance is available by using the midpoint of a battery bank. Especially in high-voltage, high-power applications, many industrial engineers are making a concerted effort to realize this topology, which implies its reasonable potential.

- **Inductor-Coupled (IC) ZVT Converters** [A7-A8, C4, C20, C23-C25, C29]: A coupled inductor provides both a negative bias for discharging the auxiliary current and a resonant inductance. With the help of the coupled inductors, this topology achieves zero-current turn-off of the auxiliary switches and zero-voltage turn-on of the main switches. There are three ways to use the coupled inductors: Transformer-assisted ZVS pole converter [C23, C25, C29], True-PWM ZVS pole converter [C4, C23-C24], and ZVT converter with inductor feedback [C20, C24]. A Transformer-assisted ZVS pole converter uses two separate windings of coupled inductors. While this topology does not have any problems with resetting

the magnetizing current, full DC voltage cannot be used for the charging and discharging operations, similarly as in an ARCP converter. A True-PWM ZVS pole converter makes a common connection of coupled inductors at the DC input side. While only some part of the load current conducts through the auxiliary switches, this topology still has problems as far as not using full DC voltage for the charging and discharging operations, as in the Transformer-assisted ZVS pole converter. A ZVT converter with inductor feedback makes a common connection of coupled inductors at the load side, as shown in Figure 1.2 (b). The original concept of this topology was proposed for DC-DC converters to turn off the auxiliary switch with zero-current condition as well as to turn-on the main switch with zero-voltage condition [A7]. A three-phase converter application with this concept has all the benefits of the original DC-DC applications. If the turns-ratio of coupled inductors is 1:1, only half the load current conducts through the auxiliary switches. In addition, the charging and discharging operations use full DC voltage, so the resonant inductance can be larger than that of other topologies. This topology requires saturable inductors to reset the magnetizing current; otherwise, the magnetizing current cannot be reset and finally becomes too large to ignore. Despite this problem, this topology has the best characteristics of this group, including its full use of DC input voltage and that its auxiliary switches carry half the load current.

- **Resonant Snubber Converters (RSIs)** [C8, C12, C17]: This topology installs each auxiliary pole between two phases. Therefore, there are only three auxiliary poles in the AC side that are not connected to the DC side. Because all the operations use the potential difference between two phases, two phases should change their switching statuses at the same time. This means a modified SVM scheme (non-adjacent vector scheme) is necessary for this topology. Because the modified SVM scheme generates more switching than the Minimum-Loss SVM scheme, this topology is not a good candidate for the base model for this research.



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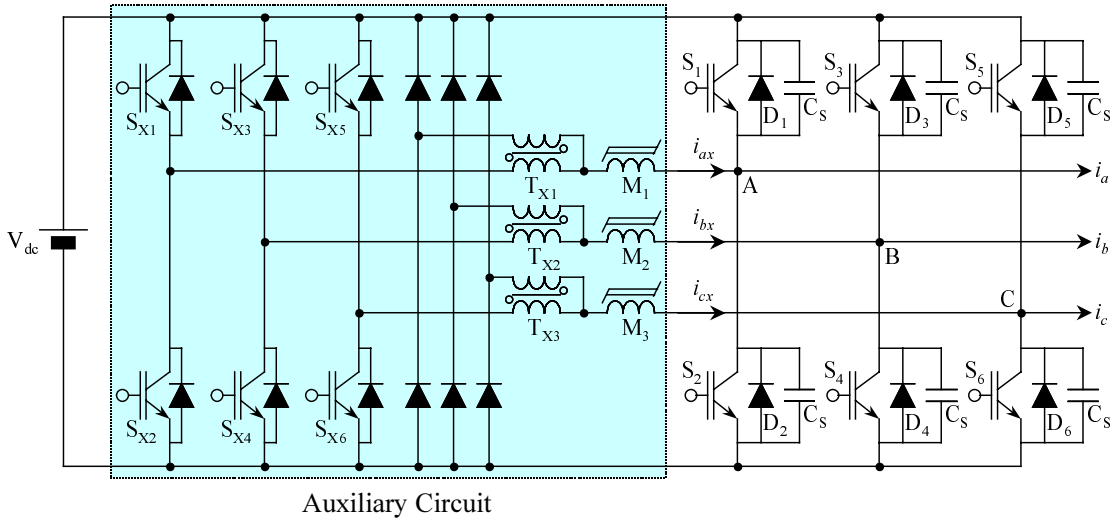


(b)

Figure 1.2 Power stage of three-phase ZVT converters:

(a) ARCP ZVT converter, and

(b) ZVT converter with inductor feedback.

B. AC-Side ZVT Converters with Simplified Auxiliary Circuits

There have been several research projects aimed at simplifying the auxiliary circuits [C5-C6, C10, C12-C13, C15] in order to decrease the cost and space. Although their performances are as good as the ZVT topologies with six auxiliary switches in rectifier applications, these topologies create several critical disadvantages in inverter applications: an additional commutation of the main switches [C5-C6, C10, C13, C15], excessive conduction losses in the auxiliary circuit [C5-C6], non-zero-voltage turn-ons of the main switches [C10, C13], and hard turn-offs of the auxiliary switches [C10]. These unfortunate characteristics make the ZVT topologies useless in inverter applications. This section describes two ZVT topologies as follows.

- **ZVT converter with single switch** [C5-C6]: Figure 1.3 (a) shows the power stage of this topology, which has only one auxiliary switch instead of the traditional six switches. This topology is a good example of the potential and direction of ZVT topologies with simple auxiliary structures. With the help of the auxiliary circuit, the main switches turn on with zero-voltage conditions. The auxiliary switch turns off with some current, the level of which is insignificant. However, in the inverter-mode operation, the main switch that carries the largest load current among three phases should turn off in order to generate the auxiliary inductor current at the beginning of commutation. Compared to the Minimum-Loss SVM scheme that does not change the switching status of the largest current phase, the switching pattern of this topology is completely unacceptable. In addition, because the level of every auxiliary inductor current should reach that of its corresponding load currents, there is redundant auxiliary current in some load current distribution. This redundant current causes more conduction losses in the auxiliary circuit than those of other ZVT topologoies.

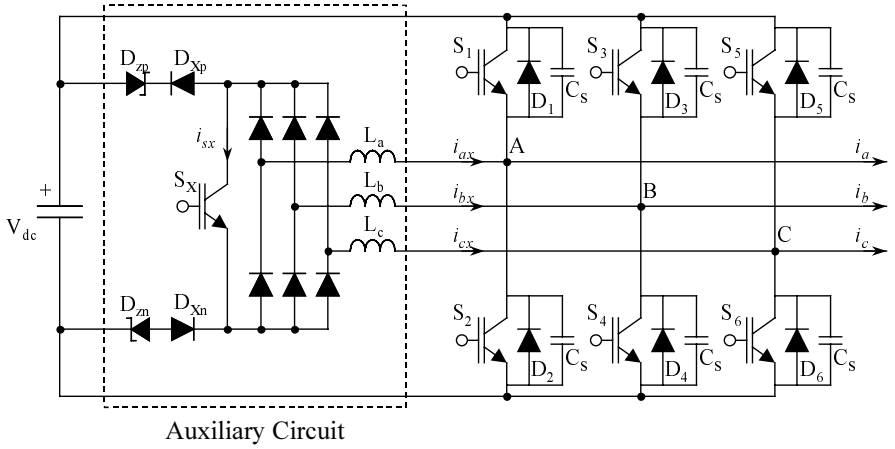
- **ZVT converter with single inductor** [C10]: This topology uses only one inductor and two switches in its auxiliary circuit, as shown in Figure 1.3 (b). By using a single inductor, this topology minimizes the possible trouble caused by passive components. The main switches turn on without reverse recovery currents. However, in converter applications, this topology has more problems than the

ZVT with single switch. An extra turn-off of the main switches at the beginning of a commutation is the same as that of the ZVT with single switch. Because there is no overlap between the main and auxiliary switches, the conduction losses of the auxiliary switch are small. Even if the reverse recovery current is removed, three node voltages stay at two-thirds of V_{dc} after the resonant period ends. Therefore, the main switches cannot turn on with zero-voltage conditions, which results in an inability to use the snubber capacitors that can reduce turn-off losses. In addition, the auxiliary switches turn off with the sum of load current and resonant peak current, because there is no way to decrease the auxiliary inductor current except by hard turn-off of the auxiliary switches. This topology is not at all appropriate for inverter applications.

1.1.3 AC-Side ZCT Converters

ZCT topologies are another branch of AC-side soft-switching topologies [A6, A10, C1, C14, C21, C31, C33, C36-C37, C39]. Since the first version of AC-side ZCT topologies was proposed, most of the ZCT topologies have used the same power stage, as shown in Figure 1.4 (a). While the first version only achieved the turn-off loss reduction for main switches [A6], the improved ZCT topologies allow both the soft turn-ons and the zero-current turn-offs of main switches [A10, C14, C31, C33]. Therefore, their commutation characteristics are better than those of the ZVT topologies. All AC-side ZCT topologies, however, have fixed resonant tanks large enough to allow soft-switching commutation at any load current. This characteristic worsens the load adaptability. Therefore, researchers hesitate to implement the ZCT topologies on any multi-phase converter with varying load conditions.

An AC-side ZCT converter with simplified auxiliary circuit was also proposed, as shown in Figure 1.4 (b) [C33]. This power stage meets the application engineers' demands for small, inexpensive auxiliary circuits. However, this ZCT converter must use different timing control methods according to the load current direction. The resonant current is larger than that of the conventional ZCT converter shown in Figure 1.4 (a), which increases the converter conduction losses.



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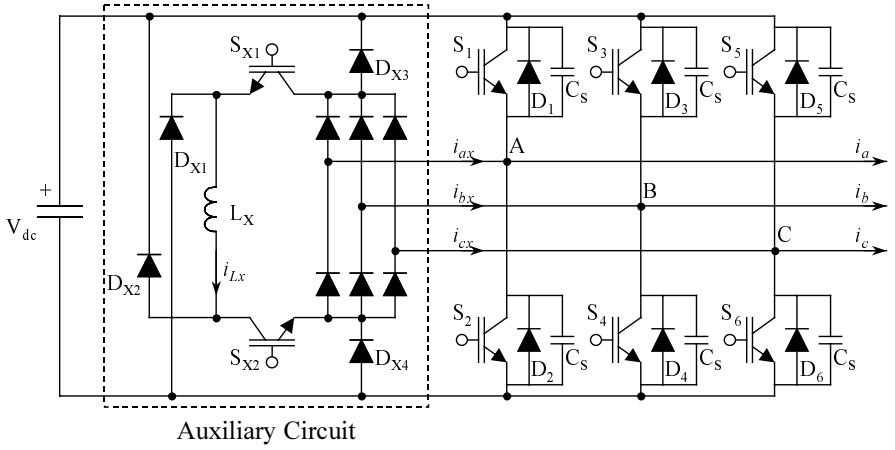
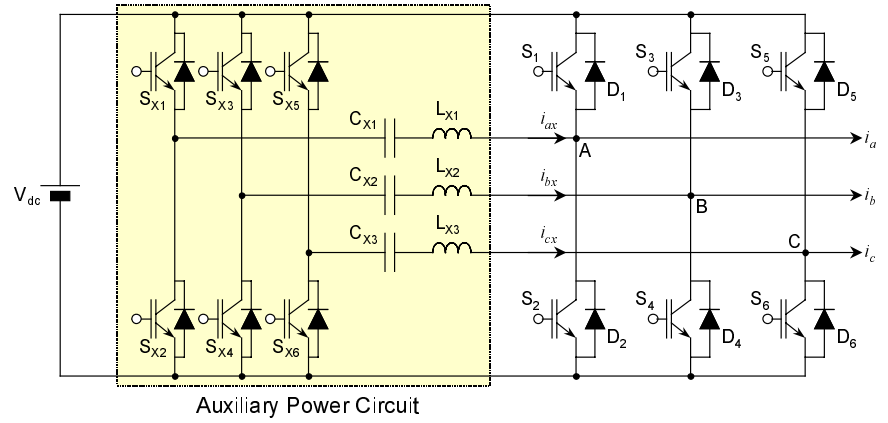


(b)

Figure 1.3 Three-phase ZVT converters with simplified auxiliary circuits:

(a) ZVT converter with single switch, and

(b) ZVT converter with single inductor.



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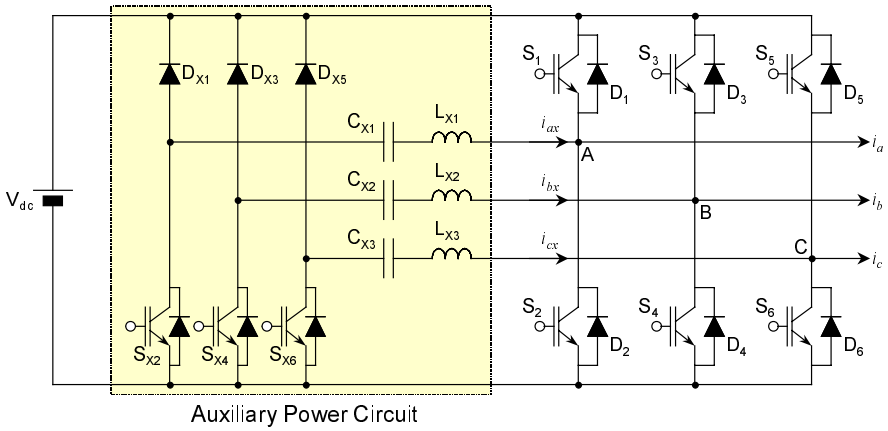


(b)

Figure 1.4 Power stages of three-phase ZCT converters:

(a) Commonly used power stage, and

(b) Simplified power stage using three auxiliary switches.

1.2 RESEARCH DIRECTION

Earlier sections discuss research motivations and related present technologies. While increasing the switching frequency improves the converter performance and controllability, it also increases the converter switching losses. There are soft-switching topologies that can resolve this trade-off.

How can we choose an appropriate soft-switching topology? It depends on the application and required features of the converter in terms of power range, switching frequency, size, cost, etc. Since this dissertation focuses on medium- and high-power applications, the converter needs not only soft switching of the main switches but also soft switching of the auxiliary switches. Even if AC-side ZVT topologies with simplified auxiliary circuits have simple power stages, they cannot be chosen due to the hard turn-offs of the auxiliary switches. For motor drive applications, the topology should be properly operated under any power factor condition. Otherwise, the topology cannot meet the required performance as a soft-switching topology. This requirement excludes DC-side ZVT topologies. Both AC-side ZVT and ZCT topologies can appropriately handle the converter losses in medium- and high-power applications. However, there is another point of performance evaluation – conducted EMI noise. While ZVT topologies can reduce the EMI noise by controlling *di/dt* and *dv/dt*, ZCT topologies cannot fully control them [D18]. Inductor-coupled ZVT topologies offer proper bias voltages for zero-voltage commutations regardless of DC voltage fluctuation, and the peak value of their auxiliary currents is just half the load currents. Therefore, in high-current and low-cost applications such as EV propulsion applications, the Inductor-coupled ZVT topologies are more advantageous than the ARCP ZVT topologies. This dissertation therefore chooses Inductor-coupled ZVT topologies as the base model for research.

Any soft-switching converter has two major issues: the complexity of power stage and controllability. Although soft-switching topologies achieve better performance than hard-switching topology, engineers working with medium- or high-power multi-phase converters still hesitate to use these topologies due to their complicated structures; they need simplified soft-switching topologies that have the same level of performance as the conventional soft-switching topologies. One research direction becomes clear –

investigation into the possibility of simplification and development of the inductor-coupled (IC) ZVT topologies with simplified auxiliary circuits for multi-phase applications. The investigation of conventional soft-switching topologies reveals the following required features of the future IC ZVT topologies.

- **Minimum-Loss SVM scheme**: The Minimum-Loss SVM scheme already achieves loss reduction by half that of the six-commutation SVM schemes. If a topology needs an additional commutation for its operation, then the topology becomes useless. In order to maximize the performance, operation of any ZVT topologies should match the Minimum-Loss SVM scheme.

- **Zero-voltage turn-on commutation of the main switches**: Eliminating the reverse recovery current is insufficient. A topology that is unable to achieve full zero-voltage conditions cannot use the snubber capacitors that are necessary for reduced turn-off losses of the main switches. The snubber capacitors make the proper resonant time with auxiliary inductors as well.

- **Zero-current turn-off commutation of the auxiliary switches**: Medium- and high-power converters use IGBTs as auxiliary switches. If the auxiliary switches turn off with near-load current, reducing the turn-on losses of the main switches becomes futile. For this reason, using the midpoint of DC voltage or the coupled inductor is an appropriate choice for any ZVT topologies.

- **Piggyback concept in the power stage**: If a component is inserted between any parts of the original main power stage, it causes unacceptable characteristics such as more losses, increased device voltage, or complicated control schemes. The piggyback concept in the power stage can minimize these kinds of problems.

Since a soft-switching topology changes the duty ratio of the converter, there are definitely control issues. For the practical implementation, the control issues are as important as the power stages of soft-switching converters. Some research has developed the average models of soft-switching converters [E3-E4, E9-E13, E15-E17]. The small-signal analysis could be used for closed-loop control design. The average models also help to easily find the output characteristics of soft-switching converters. While there

have been efforts to make the average models of DC-DC converters [E4, E11, E13, E17], there were few approaches relevant to multi-phase converters [E12, E15-E16] and only for the DC-side soft-switching topologies. The timing analysis of multi-phase converters is more complicated than that of DC-DC converters, and the average models generally use *dq* transformation. However, developing the average models of multi-phase soft-switching converters allows the control characteristics and output performance to be easily predicted regardless of the fundamental operating frequency.

1.3 MAJOR PROPOSALS OF DISSERTATION

The research direction has chosen the inductor-coupled ZVT topologies as a base model group. It has also defined two tasks: simplification of power stage and development of an average model. In order to accomplish these tasks, this dissertation analyzes the conventional inductor-coupled (IC) ZVT topologies and reveals research results. This section summarizes the next chapters, which contains the major proposals.

1.3.1 Analysis of Conventional Inductor-Coupled ZVT Converters

Chapter 2 analyzes several conventional IC ZVT topologies based on their research literature. This analysis compares their characteristics and performances, and eventually selects the ZVT converter with inductor feedback [A7, C20, D10] as a base model. Former analysis of this converter is not sufficiently clear to use in the development of the average model. Therefore, this chapter outlines the generalized timing equations for each operation period. These equations will be used in Chapter 5, in which an average model is derived.

1.3.2 Novel Inductor-Coupled ZVT Cells

Each phase of a conventional IC ZVT converter can be a ZVT cell. Even if an individual cell can accomplish zero-voltage commutation, it contains inherent circulating currents: freewheeling and residual magnetizing currents. These currents produce more losses and EMI noise, and can lead to the malfunction of the converter. Although the conventional ZVT cell employs a saturable inductor, the problems remain.

Chapter 3 proposes a novel ZVT cell that eliminates all the circulating currents [C38]. The proposed cell reduces the losses and EMI noise of converter, and its structure is simpler than that of the conventional cell. In addition, the ZVT cell leads intuitively to the simplification of the ZVT cell. Eventually, Chapter 3 proposes another novel ZVT cell with simplified auxiliary circuit – the single-switch single-leg (S^3L) ZVT cell [C35]. This simplified ZVT cell using one auxiliary switch can achieve the same performance as

the conventional ZVT cell. This proposal makes IC ZVT topologies more attractive for multi-phase converter applications.

1.3.3 Inductor-Coupled ZVT Converters with Phase-Lock (PL) Concept

In general, all the top main switches have identical sequences for zero-voltage turn-on commutations. This means that one auxiliary switch can handle the commutations of all the top main switches. The same concept can be applied to all the bottom main switches.

Chapter 4 introduces the Phase-Lock (PL) concept that allows the two auxiliary switches to provide zero-voltage condition for any main switch commutation [C26, C30, C32, C34]. In order to compensate for restrictions of this concept, a modified SVM scheme is also introduced [C27].

1.3.4 Average Modeling of Inductor-Coupled ZVT Converters

In order to make the average model of the three-phase ZVT converter with inductor feedback, the average model of a three-phase hard-switching converter is modified using the timing equations obtained in Chapter 2. Different from the hard-switching converter, the average model of the ZVT converter has another low-frequency term. Additionally, the ZVT converter needs double averaging for its average model.

Chapter 5 introduces the average model, and shows the results of small-signal analysis for verifying the stability of the converter. For an inverter case, the average model reveals the relationship between output voltage and other factors.

1.3.5 Conclusion and Suggestion for Future Research

Chapter 7 concludes this dissertation and suggests the direction of future research.

Chapter 2. ANALYSIS OF CONVENTIONAL INDUCTOR-COUPLED ZERO-VOLTAGE-TRANSITION CONVERTERS

This chapter reviews the literature written about inductor-coupled (IC) ZVT converters. According to the comparison of those ZVT converters, the ZVT converter with inductor feedback is chosen as a base model for analysis and simplification. In addition to discussing the operation principle of the converter, this chapter introduces the generalized timing analysis of the converter. This timing analysis shows the effects of both the amount of boost current and the turns-ratio of coupled inductors, and will be used to model the converter in Chapter 5.

2.1 REVIEW OF CONVENTIONAL IC ZVT CONVERTERS

Just as the ARCP ZVT converters [B5, C2-C3, C7, C9, C11, C18-C19, C22, C28] use the midpoint of DC voltage as a power source for the auxiliary circuit operations, the inductor-coupled ZVT converters [A7-A8, C4, C20, C23-C25, C29] use the coupling effect of two inductors. The coupling effect not only linearly charges the auxiliary inductor currents, but also discharges the currents by automatically biasing reverse voltage to the auxiliary inductors. In addition, some of the converters might carry half the load current through the auxiliary switches, so these are suitable for high-current applications, such as EV propulsion systems.

So far, several kinds of inductor-coupled ZVT converters have been proposed. The first proposal of the inductor-coupled ZVT topologies was a three-phase converter that allows both the zero-current turn-off of auxiliary switches and the zero-voltage turn-on of main switches [C4]. Another type of inductor-coupled ZVT concept was applied to a DC-DC converter [A7-A8]. The concept used in the DC-DC converter was expanded to a three-phase converter with the same switching characteristics [C20, C24, D10]. A technical paper proposed another coupling method, which involved the electrical separation of two inductors [C23, C25, C29]. The ZVT concept has been used even in multi-level converters [C23, C25, C28].

The proposed ZVT converters using the inductor coupling effect can be categorized into three predominant groups: the True-PWM ZVS pole converter [C4, C23-C24], the ZVT converter with inductor feedback [C20, C24, D10], and the Transformer-assisted ZVS pole converter [C23, C25, C29]. The operation of each phase of the converters is not only identical but also independent from each other. Therefore, each phase of the converters can be defined as a ZVT cell, which consists of two main switches and corresponding auxiliary circuit. Figure 2.1 shows the ZVT cells of three types of inductor-coupled ZVT converters. Although the topologies have common features, they have several differences, as described in the following.

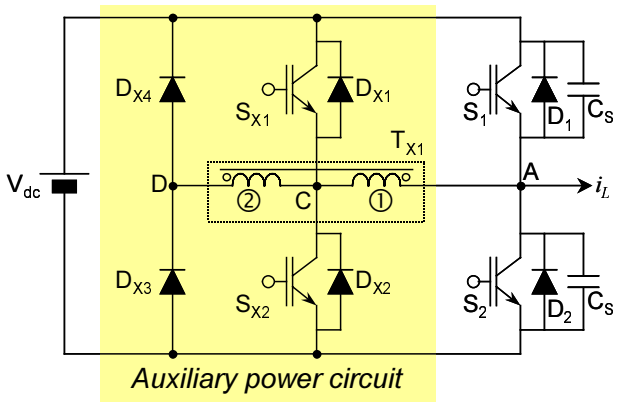
- *True-PWM ZVS pole converter*: Figure 2.1 (a) shows a cell using this topology. Winding ② (secondary winding) is in series with winding ①. Normally, winding

②'s number of turns is twice that of winding ①. Therefore, both winding ② and the auxiliary switch carry half the current of winding ①. Because only half the DC input voltage is applied to the auxiliary inductance (L_X) of winding ① in all commutation periods, the inductance should be only half those of the other ZVT topologies for the same *di/dt* value.

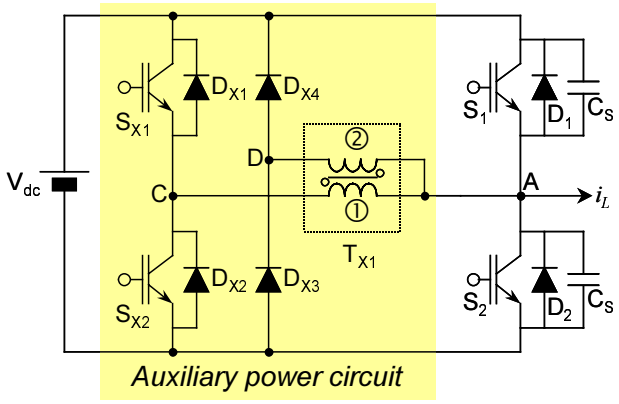
- *ZVT converter with inductor feedback*: Figure 2.1 (b) shows a cell using this topology. Winding ② is in parallel with winding ①. Since winding ②'s number of turns is normally the same as that of winding ①, each winding of coupled inductors carries the same amount of current. Therefore, the auxiliary switch becomes at most only half the load current. The auxiliary inductance (L_X) of winding ① is the same as those of the other ZVT topologies for the same *di/dt* value.

- *Transformer-assisted ZVS pole converter*: Figure 2.1 (c) shows a cell using this topology. Winding ② is isolated from winding ①. Because winding ②'s number of turns is normally twice that of winding ①, only half the DC input voltage is applied to the auxiliary inductance (L_X) of winding ① in all commutation periods. Therefore, the inductance should be only half those of the other ZVT topologies for the same *di/dt* value. Winding ② carries half the current of winding ①, which is the same as the auxiliary switch current.

Although both the True-PWM ZVS pole and the Transformer-assisted ZVS pole converters are attractive, the ZVT converter with inductor feedback has more advanced features: All of the auxiliary components carry only at most half the load current; the auxiliary inductance (L_X) is twice those of the other two topologies for the same *di/dt* value. These advanced features allow the ZVT converter with inductor feedback to have lower losses and to be easily implemented. These features become more effective in high-current medium-voltage applications, especially in EV propulsion systems. Section 2.2 reviews the operation principles of the topology in detail, in order to ascertain the target performances of novel simplified ZVT converters.



(a)



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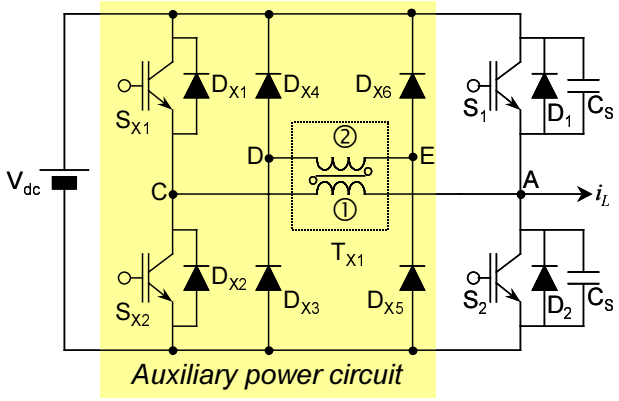


(c)

Figure 2.1 ZVT cells of conventional three-phase inductor-coupled ZVT converters:

(a) True-PWM ZVS pole converter,

(b) ZVT converter with inductor feedback, and

(c) Transformer-assisted ZVS pole converter.

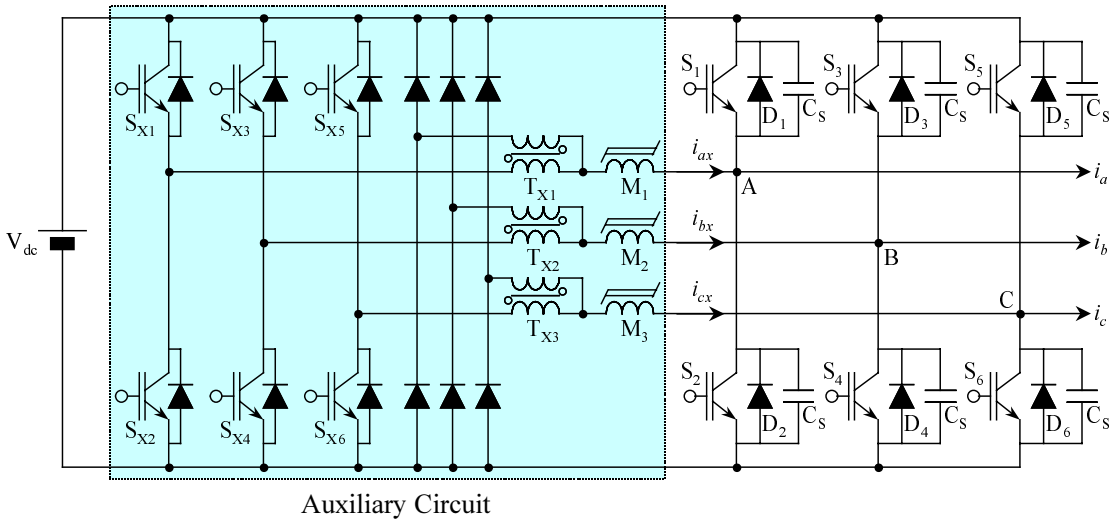
2.2 REVIEW OF ZVT CONVERTER WITH INDUCTOR FEEDBACK

Originally, this kind of coupling method was proposed for a DC-DC converter [A7]. Later, this inductor coupling method was expanded to a three-phase converter application [C20, D10]. The three-phase ZVT converter had an issue related to the residual magnetizing current, and the research proposed the solution of the issue using saturable inductors. Although the issue and the solution are definitely important for implementing the topology, these do not affect the analysis of switching cycle operations. Therefore, for detail analysis, this section uses the original power structure of this topology without the saturable inductors. Later, Chapter 3 will discuss the issues surrounding the residual magnetizing current and propose a solution.

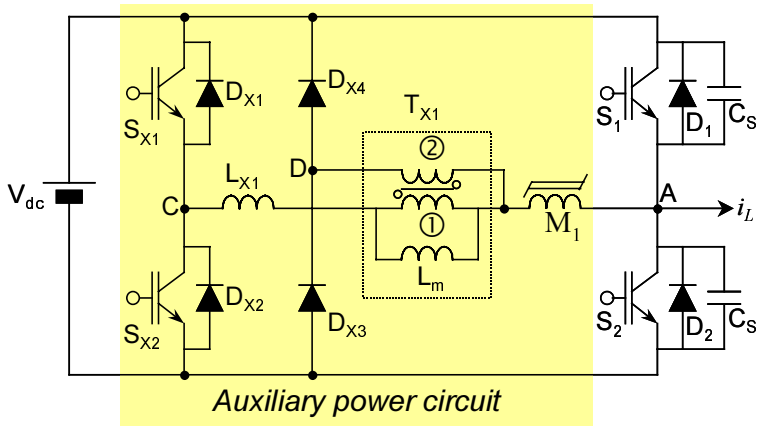
2.2.1 Power Stage

Figure 2.2 (a) shows the power stage of a three-phase ZVT converter with inductor feedback [C20]. The auxiliary circuit of this power stage consists of six auxiliary switches (S_{X1}~S_{X6}), three coupled inductors (T_{X1}~T_{X3}), three saturable inductors (M_1~M_3), and several diodes. The saturable inductors help reset the residual magnetizing current. Because the leakage inductance of the coupled inductor is used as a resonant inductor, there is no additional auxiliary inductor. In addition, six snubber capacitors are attached across the main switches, which not only reduces the turn-off losses of the main switches but also acts as part of the resonant tank.

For analyzing the ZVT topology, Figure 2.2 (b) separately shows both the magnetizing inductance and the leakage inductance of the coupled inductors. The saturable inductors are necessary only to reset the magnetizing inductance. Because the inductances are related to operation principles, they should appear in the ZVT cell for clear analysis. The following sections will use this ZVT cell for explaining the operation principles.



(a)



(b)

Figure 2.2 Power stage of ZVT converter with inductor feedback:

(a) Three-phase ZVT converter, and

(b) A ZVT cell for one phase.

2.2.2 Operation Principles

Since commutation waveforms are a major deciding factor in the performance evaluation of a ZVT converter, the commutation sequences should be analyzed in detail. In addition, the SVM scheme should be defined since it is also responsible for switching performances. Auxiliary circuit operations for zero-voltage turn-on commutation should be available at any switching pattern. If necessary, the SVM scheme is modified to match the circuit operations. The SVM modification is meaningless, however, if it causes more commutations in the main switches. The best solution is to use the Minimum-loss (ML) SVM scheme that achieves minimized converter losses [E1-E2, E5-E8, E14]. This ZVT converter and SVM scheme are compatible. The following sections explain the ML SVM scheme as well as the commutation sequences.

A. Space Vector Modulation (SVM) Scheme

The SVM schemes select some switching-state vectors (SSVs) out of eight SSVs in order to generate the voltage reference vector V_{ref} on the vector space shown in Figure 2.2 [E2, E5-E8, E14]. In general, two non-zero SSVs adjacent to V_{ref} are chosen to generate this voltage vector. For example, when V_{ref} is in either sector I or II, both V_1 (*pnn*) and V_2 (*ppn*) are adjacent to the voltage vector, as shown in Figure 2.3 (a). These SSVs generate the voltage vector with the duty ratios of d_1 and d_2. The sum of d_1T_s and d_2T_s is generally less than a switching cycle time T_s. Zero SSVs occupy this remaining time in a switching cycle. There are several methods for selecting the zero SSVs. Choosing the appropriate zero SSVs can reduce the switching losses or harmonics [E14].

The ML SVM scheme chooses a zero SSV, based on the location of current vector i_{Load}, in order to minimize the switching losses [E7, E14]. The main strategy of this modulation scheme is not to commutate the phase that has the largest current among three phases. The measured three-phase currents (i_a, i_b and i_c) comprise the current vector, as shown in Equation (2.1):

$$i_{Load} = \frac{2}{3} \cdot \left(i_a + i_b \cdot e^{j\gamma} + i_c \cdot e^{j2\gamma} \right) \qquad (2.1)$$

$$\text{where} \quad \gamma = \frac{2}{3} \cdot \pi .$$

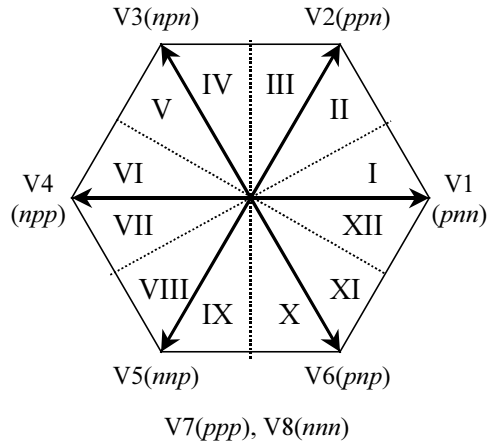
The current vector can be at any sector in the vector space with the phase difference θ from the voltage vector V_{ref}, as shown in Figure 2.3 (a). In this example, the current vector is in sector I, which implies that phase A has the largest current. The switching status of phase A is *p* (turn-on of the top switch) in both V_1 and V_2. Therefore, choosing V_7 (*ppp*) as a zero SSV results in no commutation in phase A, as expected. Figure 2.3 (b) shows the SSV sequences and corresponding phase signals. In the same manner, the appropriate zero SSV can be selected for any case. Table 2.1 shows the selection of the proper zero SSV when the voltage vector is in either sector I or II. If the switching status of the largest current phase is both *p* and *n* (turn-on of the bottom switch) in one switching cycle, this scheme chooses a zero SSV that will not change the switching status of the phase with the second largest current.

This scheme always causes four commutations in two phases. Because the switching losses are proportional to the current magnitude, this scheme tries to not commutate the largest current phase. This strategy decreases the switching losses to at most half the switching losses of the SVM schemes with six commutations [E14].

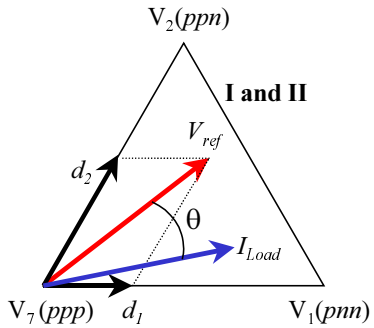
Table 2.1

SELECTION OF THE PROPER ZERO VECTOR WHEN V_{REF} IS IN SECTOR I OR II

Locations of Current Vector	Proper Zero Vector
XI, XII or I	*ppp*
II, III or IV	*nnn*
V, VI or VII	*ppp*
VIII, IX or X	*nnn*



(a)



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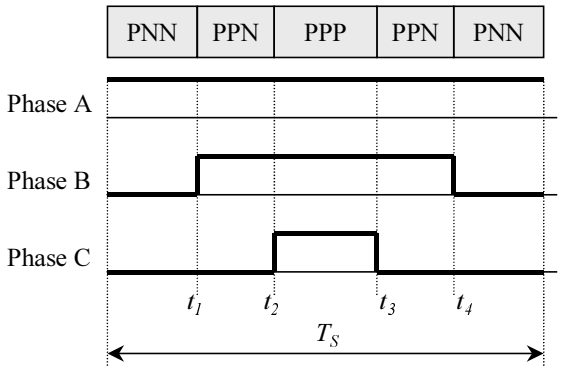


(c)

Figure 2.3 Minimum-loss SVM scheme when V_{ref} and I_{Load} are in either sector I or II:

(a) Vector space with switching space vectors,

(b) Decomposition of V_{ref}, and

(c) Center-based switching vector sequence.

B. Zero-Voltage Turn-On Commutations

In general, a commutation from diode to switch requires the auxiliary circuit operation to achieve zero-voltage condition for the switch. A commutation from switch to diode, however, cannot be accomplished within an acceptable length of time when the load current is too small to discharge a snubber capacitor. In this case, the auxiliary circuit assists this commutation by boosting the discharging current of a snubber capacitor. Otherwise, the snubber capacitance cannot be large enough to reduce turn-off losses.

The auxiliary circuit of this ZVT converter can provide the operations necessary for both commutations. Figure 2.4 shows several waveforms of corresponding devices during the zero-voltage turn-on commutations of both cases: from diodes to switch and from switch to diode with low load current. This figure clearly shows the zero-voltage turn-on of the main switches and the zero-current turn-off of the auxiliary switches in both cases.

Figure 2.4 (a) shows the commutation waveforms of phase A when the load current i_a is positive. At this moment, the load current conduction is changed from a main diode D_2 to a main switch S_1 with the operation of an auxiliary switch S_{X1}. Figure 2.5 shows the current conduction statuses of all commutation periods.

- *Before commutation* [before t_0] : Due to the load current direction, D_2 carries the load current. The conduction voltage drop of diode D_2 allows the current conduction through D_{X2} and D_{X4} and the coupled inductor T_{X1}.

- *Charging period* [$t_0 \sim t_1$] : When S_{X1} turns on at t_0, the winding ② of the coupled inductor T_{X1} does not have any voltage drop, because the potential of node A is the same as that of the negative DC rail. Therefore, the DC input voltage V_{dc} is applied to the leakage inductor L_{X1} of T_{X1}. This applied voltage generates a charging current through S_{X1} and L_{X1}. This auxiliary switch current i_{SX1} increases linearly and reaches half the load current i_a at t_1. The winding ② carries the same amount of current as i_{SX1} through D_{X4}. Due to these auxiliary currents, the main diode current i_{D2} decreases linearly and reaches zero at t_1. Therefore, the anti-parallel diode D_2 can turn off with zero-current condition.

- *Boost period* [$t_1 \sim t_2$] : After i_{SX1} reaches half the load current i_a at t_1, both S_2 and S_{X1} stay in on-states in order to add the boost current I_{boost} to the auxiliary switch current. The auxiliary switch current i_{SX1} reaches the sum of I_{boost} and half the load current at t_2.

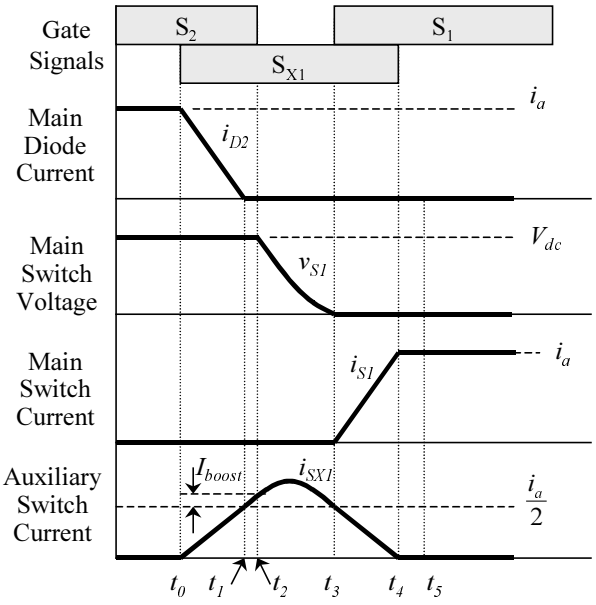
- *Resonant period* [$t_2 \sim t_3$] : When S_2 turns off at t_2, the leakage inductor L_{X1} of T_{X1} starts to resonate with the capacitors across both S_1 and S_2. This resonant operation charges the capacitor across S_2 and discharges the capacitor across S_1. When the voltage across the main switch S_1 reaches zero at t_3, this main switch turns on with zero-voltage condition.

- *Discharging period* [$t_3 \sim t_4$] : Since S_1 turns on with zero-voltage condition at t_3, node A stays connected to the positive DC rail. This potential applies V_{dc} to the winding ② and L_{X1} as a reverse bias of the auxiliary inductor current. Due to this reverse bias, i_{SX1} decreases and i_{S1} increases linearly. When i_{SX1} reaches the very small magnetizing current of T_X, S_{X1} turns off with a quasi-zero-current condition at t_4. At the same time, S_1 carries all load current i_a.

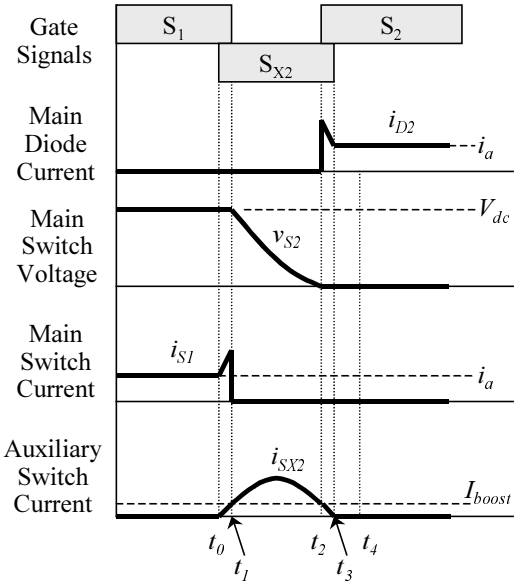
- *Reset period* [$t_4 \sim t_5$] : When S_{X1} turns off with a quasi-zero-current condition at t_4, the coupled inductor T_{X1} carries only the magnetizing energy. Because the saturable inductor M_1 blocks the current path from node A to T_X, D_{X2} and D_{X3} provide a current path for the magnetizing current. During this conduction period, each winding of T_X holds half the DC input voltage as reverse bias to the magnetizing current. Therefore, this energy is totally reset at t_5.

- *After commutation* [$t_5 \sim$] : After the commutation is completed at t_5, the load current flows only through S_1, and there is no energy in the auxiliary circuit.

As a second example of the zero-voltage turn-on of the main switches, Figure 2.4 (b) shows the commutation waveforms of phase A when the load current i_a is positive. At this moment, the load current conduction is changed from a main switch S_1 to a main diode D_2 with the operation of an auxiliary switch S_{X2}.



(a)



(b)

Figure 2.4 Zero-voltage turn-on commutation waveforms:

(a) Commutation from diode to switch, and

(b) Commutation from switch to diode with low load current.

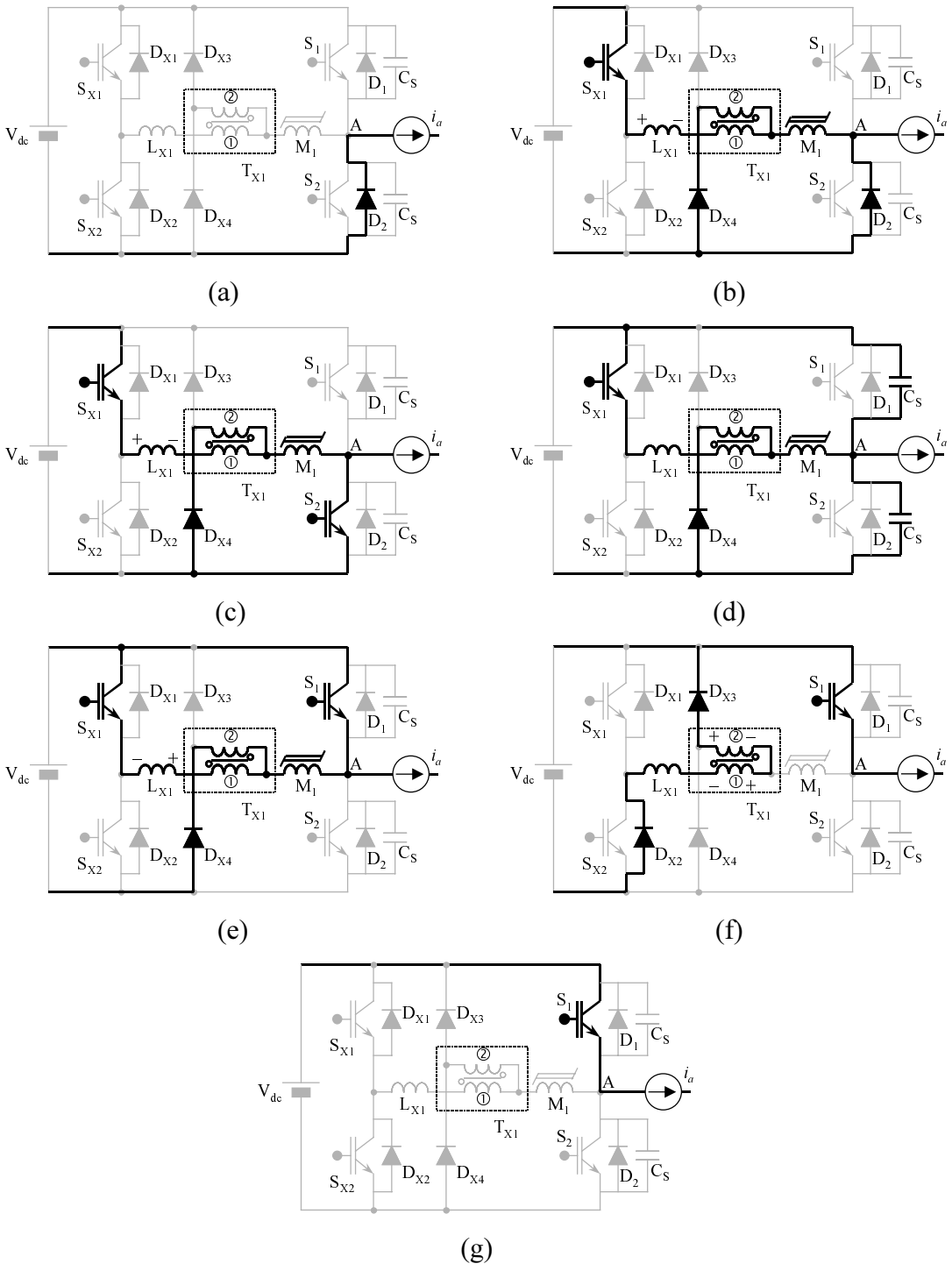


Figure 2.5 Commutation description of sequential periods from diode to switch: (a) Before commutation, (b) Charging period, (c) Boost period, (d) Resonant period, (e) Discharging period, (f) Reset period, and (g) After commutation.

- *Boost period* [$t_0 \sim t_1$] : When S_{X2} turns on at t_0, the DC input voltage V_{dc} is applied to the leakage inductor L_{X1} of the coupled inductor T_{X1}, because the potential of node A is the same as that of the positive DC rail. This applied voltage generates a boost current through S_{X2} and L_{X1}. This auxiliary switch current i_{SX2} increases linearly and finally reaches the required boost current I_{boost} at t_1. The winding ② carries the same amount of current as i_{SX2} through D_{X3}.

- *Resonant period* [$t_1 \sim t_2$] : When S_1 turns off at t_1, the leakage inductor L_{X1} of T_{X1} starts to resonate with the capacitors across both S_1 and S_2. This resonant operation charges the capacitor across S_1 and discharges the capacitor across S_2. When the voltage across the main switch S_2 reaches zero at t_2, this main switch turns on with a zero-voltage condition.

- *Discharging period* [$t_2 \sim t_3$] : Since S_2 turns on with a zero-voltage condition at t_2, node A stays connected to the negative DC rail. This potential applies V_{dc} to winding ② and L_{X1} as a reverse bias of the auxiliary inductor current. This reverse bias decreases i_{SX2} linearly. When i_{SX2} reaches the very small magnetizing current of T_X, S_{X2} turns off with a quasi-zero-current condition at t_3. At the same time, D_2 carries all load current i_a.

- *Reset period* [$t_3 \sim t_4$] : When S_{X2} turns off with a quasi-zero-current condition at t_3, the coupled inductor T_{X1} carries only the magnetizing energy. Because the saturable inductor M_1 blocks the current path from T_X to node A, D_{X1} and D_{X4} provide a current path for the magnetizing current. During this conduction period, each winding of T_X holds half the DC input voltage as reverse bias to the magnetizing current. Therefore, this energy is totally reset at t_4.

- *After commutation* [$t_4 \sim$] : After the commutation is completed at t_4, the load current flows only through D_2, and there is no energy in the auxiliary circuit.

2.3 TIMING ANALYSIS OF ZVT CONVERTER WITH INDUCTOR FEEDBACK

The first paper written about the ZVT with inductor feedback described the timing control scheme with the unity turns-ratio of the coupled inductors, as explained in Section 2.2.3 [C20]. Therefore, the timing equations cannot be used for other turns-ratios. Although the paper does not explain why the converter uses a unity turns-ratio, the two most attractive features of this ratio are its effect on losses and timing. The conduction losses of auxiliary switches are smaller than those of any other turns-ratios, and the charging time is the same as the discharging time. Recently, several papers have proposed the non-unity turns-ratio for the coupled inductors toward the goal of advanced timing control methods [C23, C24, C40-C41]. This trend requires generalized timing equations. For both the True-PWM ZVS Pole converter and the ZVT converter with inductor feedback, some papers already investigated the influence of the turns-ratios. Although some papers have shown the effects of the turns-ratio in the ZVT with inductor feedback, the developed timing equations were not generalized for modeling [C40-C41]. This section will reveal the generalized timing equations of the ZVT converter with inductor feedback, which are used for accurate timing analysis and future modeling of the converter.

2.3.1 Conventional Timing Control Scheme using Unity Turns-Ratio

A snubber capacitor (C_S) is chosen to maximize the turn-off loss of the main switch. However, the large snubber capacitor produces a large resonant peak current and long commutation time, as shown in Equations (2.2) and (2.3):

Peak resonant current $$I_{res} = \frac{V_{dc}}{Z_{res}} = \frac{V_{dc}}{\sqrt{\frac{L_X}{C_S}}} \tag{2.2}$$

Commutation time $$T_{comm} = \pi \cdot \sqrt{L_X \cdot C_S} \tag{2.3}$$

where V_{dc} : DC input voltage

Even if the proper resonant inductance (L_X) that limits *di/dt* can reduce the resonant peak current, it increases the commutation time. Therefore, after the initial values of the

snubber capacitance and resonant inductance are determined by turn-off loss and *di/dt*, these values should be adjusted to minimize the resonant peak current in the appropriate commutation time. A coupled inductor is designed to maximize the magnetizing inductance, and its leakage inductance is controlled by a coupling factor that matches the resonant inductance.

Once C_S and L_X are determined, the operation time of all periods are estimated using the load current and boost current, as shown in Equations (2.4)–(2.7):

Charging time [t_0, t_1] $$T_{ch} = \frac{L_X \cdot i_L}{V_{dc}} \tag{2.4}$$

Boost time [t_1, t_2] $$T_b = \frac{L_X \cdot I_{boost}}{V_{dc}} \tag{2.5}$$

Resonant time [t_2, t_3] $$T_{res} = \pi \cdot \sqrt{L_X \cdot C_S} \tag{2.6}$$

Discharging time [t_3, t_4] $$T_{dis} = \frac{L_X \cdot i_L}{V_{dc}} \tag{2.7}$$

where V_{dc} : DC input voltage

i_L : instantaneous load current

I_{boost} : designed boost current

The charging time (T_{ch}) and discharging time (T_{dis}) are proportional to the load current, while the boost time (T_b) and resonant time (T_{res}) are not related to the load current. The variable-timing control method adjusts both T_{ch} and T_{dis} using the load current value. Although the boost time T_b should be adjusted to be proportional to the load current that is related to the resonant losses, in practical applications, it is fixed to a value that can guarantee zero-voltage condition for any load current value.

2.3.2 Generalized Timing Equations

Figure 2.7 (a) shows the original power stage of one phase of the ZVT converter with inductor feedback. L_p represents the leakage inductance of winding ①, L_s represents that of winding ②, and C_S represents a snubber capacitance. The number of turns of winding ② is *n*-times that of winding ①, which means the turns-ratio is 1:*n*.

If the leakage inductance of winding ② is transferred to winding ①, then it is connected in series with L_p, and its value is changed to $\frac{L_s}{n^2}$. Therefore, the equivalent inductance (L_{eq}) is defined as:

$$L_{eq} = L_p + \frac{L_s}{n^2}. \tag{2.8}$$

Figure 2.7 (b) shows the equivalent power stage with L_{eq} as well as the definition of each current. The sum of primary current (i_p) and secondary current (i_s) is the same as i_x:

$$i_p = \frac{n}{n+1} \cdot i_x \tag{2.9}$$

$$i_s = \frac{1}{n+1} \cdot i_x \tag{2.10}$$

As shown in Figure 2.7 (b), assume that the load current (i_L) both flows from load to the converter and is constant during the commutation. Therefore, the bottom main switch (S_2) requires the operation of the auxiliary circuit for its zero-voltage turn-on commutation. The following descriptions are based on this assumption, and a timing chart is shown in Figure 2.4 (a).

A. Charging and Boost Periods

Before S_{X2} turns on, i_L flows through the anti-parallel diode (D_1) of S_1. Therefore, the potential of point A is the same as that of point P (V_{dc}). When S_{X2} turns on, the potential difference between points A and N, V_{dc}, is applied to winding ①, and hence:

$$L_{eq} \cdot \frac{d}{dt}\left(i_p\right) = V_{dc} \tag{2.11}$$

Since i_x is equal to i_L at the end of charging period, the charging time (T_{ch}) is derived using Equations (2.9) and (2.11) as:

$$T_{ch} = \frac{n}{n+1} \cdot L_{eq} \cdot \frac{i_L}{V_{dc}} \tag{2.12}$$

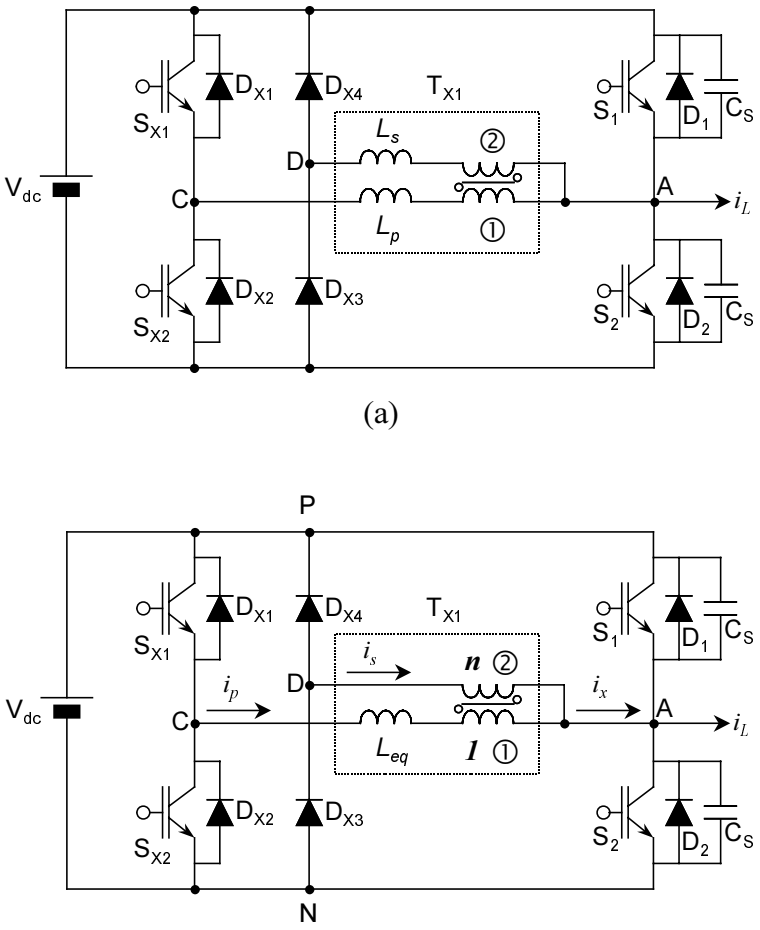


Figure 2.6 Power stages for timing analysis:

(a) Original power stage, and

(b) Equivalent power stage using L_{eq}.

Assume I_b is assigned as the value of the boost current. Because I_b flows through the same path as i_x, the boost time (T_b) can be easily derived from Equation (2.12) by replacing i_L with I_b, as:

$$T_b = \frac{n}{n+1} \cdot L_{eq} \cdot \frac{I_b}{V_{dc}} \tag{2.13}$$

If the turns-ratio is 1 (n=1), then L_p and L_s become identical. Therefore, L_{eq} equals twice the value of L_p. Assigning n=1 and L_{eq}= L_p into Equations (2.12) and (2.13) results in the equations of charging and boost times for a unity turns-ratio, which are the same as Equations (2.4) and (2.5), respectively.

B. Resonant Period

When i_x reaches the sum of i_L and I_b, S_1 turns off to begin the resonance between C_s and L_{eq}. During the resonant period, the voltage of winding ② changes, due to the changing potential of point A. This voltage is reflected to winding ①, which results in the resonant equation:

$$L_{eq} \cdot \frac{d}{dt}\left(i_p\right) - \frac{1}{C_S} \cdot \int i_{S2} dt = -\frac{1}{n} \cdot \left(V_{dc} - \frac{1}{C_S} \cdot \int i_{S2} dt \right) \tag{2.14}$$

When the resonant current (i_r) is defined as $i_r = i_x - i_L$, from Equation (2.9):

$$i_p = \frac{n}{n+1} \cdot i_x = \frac{n}{n+1} \cdot i_r + \frac{n}{n+1} \cdot i_L , \tag{2.15}$$

and because i_L is assumed constant:

$$\frac{d}{dt}\left(i_p\right) = \frac{n}{n+1} \cdot \frac{d}{dt}\left(i_r\right). \tag{2.16}$$

The charging current of a snubber capacitor across S_1 (i_{S1}) is equal to the discharging current of a snubber capacitor across S_2 ($-i_{S2}$). Therefore, their values are the same as half the resonant current (i_r):

$$i_{S1} = -i_{S2} = \frac{i_r}{2} \tag{2.17}$$

Using Equations (2.16) and (2.17), Equation (2.14) can be rewritten as:

$$L_{eq}\cdot\frac{d}{dt}(i_r)-\frac{1}{C_S}\cdot\int\left(-\frac{i_r}{2}\right)dt=-\frac{1}{n}\cdot\left[V_{dc}-\frac{1}{C_S}\cdot\int\left(-\frac{i_r}{2}\right)dt\right]. \tag{2.18}$$

Rearranging the terms of Equation (2.18) results in:

$$L_{eq}\cdot\frac{2n^2}{n+1}\cdot\frac{d}{dt}\left(\frac{i_r}{2}\right)-\frac{n+1}{C_S}\cdot\int\left(\frac{i_r}{2}\right)dt=-V_{dc}. \tag{2.19}$$

When the resonant period starts, i_x is equal to the sum of i_L and I_b. Therefore, the initial condition of i_r becomes I_b. The second-order differential equation, Equation (2.19), then has a solution:

$$\begin{aligned} i_r &= 2\cdot\omega_0\cdot\left[\frac{I_b}{2\cdot\omega_0}\cdot\cos(\omega_0 t)+\frac{n}{n+1}\cdot C_S\cdot V_{dc}\cdot\sin(\omega_0 t)\right] \\ &= I_b\cdot\cos(\omega_0 t)+\frac{2n}{n+1}\cdot C_S\cdot V_{dc}\cdot\omega_0\cdot\sin(\omega_0 t) \\ &\text{where } \omega_0=\frac{n+1}{n}\cdot\sqrt{\frac{1}{2\cdot L_{eq}\cdot C_S}}. \end{aligned} \tag{2.20}$$

In addition, the primary current and the voltage of a discharged snubber capacitor (v_C) can be derived from Equation (2.20):

$$\begin{aligned} i_p &= \frac{n}{n+1}\cdot i_r \\ &= \frac{n}{n+1}\cdot I_b\cdot\cos(\omega_0 t)+2\cdot\left(\frac{n}{n+1}\right)^2\cdot C_S\cdot V_{dc}\cdot\omega_0\cdot\sin(\omega_0 t) \end{aligned} \tag{2.21}$$

$$v_C=\frac{V_{dc}}{n+1}\left[1+n\cdot\cos(\omega_0 t)\right]-\frac{I_b}{2\cdot C_S\cdot\omega_0}\cdot\sin(\omega_0 t) \tag{2.22}$$

Because the voltage of a discharged snubber capacitor reaches zero at the end of resonant period, the equation of resonant time can be derived by using $v_C = 0$ in Equation (2.22). To get the equation of resonant time, assume two cases: either $n = 1$ or $I_b = 0$.

(a) If n = 1, and I_b varies:

This method has been generally used in this topology.

Using $n = 1$ changes Equation (2.22) to:

$$v_C = \frac{V_{dc}}{2}\left[1+\cos(\omega_0 t)\right] - \frac{I_b}{2\cdot C_S \cdot \omega_0}\cdot \sin(\omega_0 t) \tag{2.23}$$

Using $v_C = 0$ and $t = T_{res}$ in Equation (2.23) derives the equation of resonant time as:

$$0 = \frac{V_{dc}}{2}\left[1+\cos(\omega_0 \cdot T_{res})\right] - \frac{I_b}{2\cdot C_S \cdot \omega_0}\cdot \sin(\omega_0 \cdot T_{res}) \tag{2.24}$$

$$\begin{aligned}\frac{V_{dc}\cdot C_S \cdot \omega_0}{I_b} &= \frac{\sin(\omega_0 \cdot T_{res})}{1+\cos(\omega_0 \cdot T_{res})} \\ &= \tan\left(\frac{\omega_0 \cdot T_{res}}{2}\right)\end{aligned} \tag{2.25}$$

$$T_{res} = \frac{2}{\omega_0}\cdot \arctan\left(\frac{V_{dc}\cdot C_S \cdot \omega_0}{I_b}\right) \tag{2.26}$$

With $n = 1,\ \omega_0 = \dfrac{1}{\sqrt{L_p \cdot C_S}}$, which changes Equation (2.26) to:

$$\begin{aligned}T_{res} &= 2\sqrt{L_p \cdot C_S}\cdot \arctan\left(\frac{V_{dc}}{I_b}\cdot\sqrt{\frac{C_S}{L_p}}\right) \\ &= 2\sqrt{L_p \cdot C_S}\cdot \arctan\left(\frac{V_{dc}}{I_b \cdot Z_{eq}}\right) \\ &= 2\sqrt{L_p \cdot C_S}\cdot \arctan\left(\frac{I_{eq}}{I_b}\right)\end{aligned} \tag{2.27}$$

$$\text{where } Z_{eq} = \sqrt{\frac{L_p}{C_S}} \text{ and } I_{eq} = \frac{V_{dc}}{Z_{eq}}$$

If $I_b = 0$, then Equation (2.27) becomes $T_{res} = \pi\sqrt{L_p \cdot C_S}$, which is the same as Equation (2.6). This result verifies that the original timing equation does not consider the effect of boost current.

(b) If $I_b = 0$, and n varies:

This method has been recently proposed for improving control performance. Using $I_b = 0$ changes Equation (2.22) to:

$$v_C = \frac{V_{dc}}{n+1}\left[1 + n \cdot \cos(\omega_0 t)\right] \tag{2.28}$$

Using $v_C = 0$ and $t = T_{res}$ in Equation (2.28) derives the equation of resonant time as:

$$0 = \frac{V_{dc}}{n+1}\left[1 + n \cdot \cos(\omega_0 \cdot T_{res})\right] \tag{2.29}$$

$$\begin{aligned} T_{res} &= \frac{1}{\omega_0} \cdot \arccos\left(-\frac{1}{n}\right) \\ &= \frac{n}{n+1} \cdot \sqrt{2 \cdot L_{eq} \cdot C_S} \cdot \arccos\left(-\frac{1}{n}\right) \end{aligned} \tag{2.30}$$

In addition to the equation of resonant time, the equation of peak resonant current can be derived from Equation (2.20). When i_r reaches its peak value, its derivative becomes zero as:

$$\begin{aligned} \frac{d}{dt}(i_r) &= -I_b \cdot \omega_0 \cdot \sin(\omega_0 t) + \frac{2n}{n+1} \cdot C_S \cdot V_{dc} \cdot \omega_0^2 \cdot \cos(\omega_0 t) \\ &= 0 \end{aligned} \tag{2.31}$$

The time of peak value (t_{peak}) can be derived as:

$$\frac{2n}{n+1} \cdot C_S \cdot V_{dc} \cdot \omega_0^2 \cdot \cos(\omega_0 t_{peak}) = I_b \cdot \omega_0 \cdot \sin(\omega_0 t_{peak}) \tag{2.32}$$

$$\begin{aligned} \frac{2n}{n+1} \cdot \frac{C_S \cdot V_{dc} \cdot \omega_0}{I_b} &= \frac{\sin(\omega_0 t_{peak})}{\cos(\omega_0 t_{peak})} \\ &= \tan(\omega_0 t_{peak}) \end{aligned} \tag{2.33}$$

$$\begin{aligned} t_{peak} &= \frac{1}{\omega_0} \cdot \arctan\left(\frac{2n}{n+1} \cdot \frac{C_S \cdot V_{dc} \cdot \omega_0}{I_b}\right) \\ &= \frac{1}{\omega_0} \cdot \arctan\left(\frac{V_{dc}}{I_b} \cdot \sqrt{\frac{2C_S}{L_{eq}}}\right) \\ &= \frac{1}{\omega_0} \cdot \arctan\left(\frac{V_{dc}}{I_b \cdot Z_{eq}}\right) = \frac{1}{\omega_0} \cdot \arctan\left(\frac{I_{eq}}{I_b}\right) \end{aligned} \tag{2.34}$$

$$\text{where } Z_{eq} = \sqrt{\frac{L_{eq}}{2C_S}} \text{ and } I_{eq} = \frac{V_{dc}}{Z_{eq}}$$

(a) If n = 1, and I_b varies:

Using $n = 1$ changes Equation (2.34) to:

$$t_{peak} = \sqrt{L_p \cdot C_S} \cdot \arctan\left(\frac{I_{eq}}{I_b}\right), \tag{2.35}$$

$$\text{where } I_{eq} = \frac{V_{dc}}{Z_{eq}} = V_{dc} \cdot \sqrt{\frac{C_S}{L_p}}.$$

Inserting Equation (2.35) into Equation (2.20) derives the equation of peak resonant current as:

$$\begin{aligned} i_{r(peak)} &= I_b \cdot \cos\left(\omega_0 \cdot t_{peak}\right) + \frac{2n}{n+1} \cdot C_S \cdot V_{dc} \cdot \omega_0 \cdot \sin\left(\omega_0 \cdot t_{peak}\right) \\ &= I_b \cdot \cos\left[\arctan\left(\frac{I_{eq}}{I_b}\right)\right] + V_{dc} \cdot \sqrt{\frac{C_S}{L_p}} \cdot \sin\left[\arctan\left(\frac{I_{eq}}{I_b}\right)\right] \\ &= I_b \cdot \cos\left[\arctan\left(\frac{I_{eq}}{I_b}\right)\right] + I_{eq} \cdot \sin\left[\arctan\left(\frac{I_{eq}}{I_b}\right)\right] \\ &= I_b \cdot \frac{I_b}{\sqrt{I_b^2 + I_{eq}^2}} + I_{eq} \cdot \frac{I_{eq}}{\sqrt{I_b^2 + I_{eq}^2}} \\ &= \sqrt{I_b^2 + I_{eq}^2} \end{aligned} \tag{2.36}$$

This equation clearly shows that I_b increases the peak value of resonant current. Section 2.3.2 shows further investigation.

(b) If I_b = 0, and n varies:

Using $I_b = 0$ changes Equation (2.34) to:

$$t_{peak} = \frac{\pi}{2\omega_0} \tag{2.37}$$

Inserting Equation (2.37) into Equation (2.20) derives the equation of peak resonant current as:

$$\begin{aligned} i_{r(peak)} &= \frac{2n}{n+1} \cdot C_S \cdot V_{dc} \cdot \omega_0 \\ &= V_{dc} \cdot \sqrt{\frac{2C_S}{L_{eq}}} = I_{eq} \end{aligned} \tag{2.38}$$

This equation shows that the turns-ratio n does not affect the peak of i_r.

C. Discharging Period

When the discharging period starts at t_3 by turning on S_2, Equations (2.39) and (2.40) show the initial values of both i_r and i_x, respectively:

$$i_r(T_{res}) = I_b \cdot \cos(\omega_0 \cdot T_{res}) + \frac{2n}{n+1} \cdot C_S \cdot V_{dc} \cdot \omega_0 \cdot \sin(\omega_0 \cdot T_{res}) \tag{2.39}$$

$$i_x(t_3) = i_L + i_r(T_{res}) \tag{2.40}$$

Because the potential of point A is the same as that of point N, the voltage of winding ② (V_{dc}) is reflected to winding ① as:

$$L_{eq} \cdot \frac{d}{dt}(i_p) = \frac{V_{dc}}{n}. \tag{2.41}$$

The discharging time is derived from Equation (2.41) as:

$$\begin{aligned} T_{dis} &= \frac{n^2}{n+1} \cdot L_{eq} \cdot \frac{i_x(t_3)}{V_{dc}} \\ &= \frac{n^2}{n+1} \cdot L_{eq} \cdot \frac{i_L}{V_{dc}} + \frac{n^2}{n+1} \cdot L_{eq} \cdot \frac{i_r(T_{res})}{V_{dc}} \end{aligned} \tag{2.42}$$

(a) If n = 1, and I_b varies:

Using n = 1 changes Equation (2.42) to:

$$T_{dis} = L_p \cdot \frac{i_L}{V_{dc}} + L_p \cdot \frac{i_r(T_{res})}{V_{dc}} \tag{2.43}$$

Inserting Equation (2.27) into Equation (2.39) derives the equation of remaining resonant current at t_3 as:

$$
\begin{aligned}
i_r(T_{res}) &= I_b \cdot \cos\left[2 \cdot \arctan\left(\frac{I_{eq}}{I_b}\right)\right] + I_{eq} \cdot \sin\left[2 \cdot \arctan\left(\frac{I_{eq}}{I_b}\right)\right] \\
&= I_b \cdot \frac{I_b^2 - I_{eq}^2}{I_b^2 + I_{eq}^2} + I_{eq} \cdot \frac{2 \cdot I_b \cdot I_{eq}}{I_b^2 + I_{eq}^2} \\
&= I_b
\end{aligned}
\tag{2.44}
$$

This equation verifies that the amount of resonant current becomes the same as I_b at the end of resonant period, as expected.

Inserting Equation (2.44) into Equation (2.43) clarifies the discharging time as:

$$
T_{dis} = L_p \cdot \frac{i_L}{V_{dc}} + L_p \cdot \frac{I_b}{V_{dc}} \tag{2.45}
$$

This equation clearly shows that the discharging time is the same as the sum of the charging time and boost time, as expected.

(b) If $I_b = 0$, and n varies:

In spite of $I_b = 0$, Equation (2.42) is unchanged.

Inserting both $I_b = 0$ and Equation (2.30) into Equation (2.39) derives the equation of remaining resonant current at t_3 as:

$$
\begin{aligned}
i_r(T_{res}) &= V_{dc} \cdot \sqrt{\frac{2C_S}{L_{eq}}} \cdot \sin\left[\arccos\left(-\frac{1}{n}\right)\right] \\
&= I_{eq} \cdot \sin\left[\arccos\left(-\frac{1}{n}\right)\right] \\
&= I_{eq} \cdot \sqrt{1 - \frac{1}{n^2}} \\
&\qquad \text{where } I_{eq} = V_{dc} \cdot \sqrt{\frac{2C_S}{L_{eq}}}
\end{aligned}
\tag{2.46}
$$

Inserting $n = 1$ into Equation (2.46) makes $i_r(T_{res})$ zero, as expected.

2.3.3 Effects of Boost Current and Turns-Ratio

Timing equations newly derived in Section 2.3.1 imply that the boost current and the turns-ratio of coupled inductors can control the duration of the zero-voltage condition. The two factors affect not only the duration of zero-voltage condition but also the other values: charging time, resonant time, discharging time and the peak of resonant current. Section 2.3.1 briefly explained the effects as each timing equation was derived. In order to understand the full impact of the phenomena, this section will summarize them together by the two factors, I_b and n.

A. Effect of Boost Current

Since the variable-timing control scheme was proposed, boost current has been a popular variable for controlling the duration of the zero-voltage condition. Although the boost current guarantees zero-voltage commutations, it also increases the conduction and turn-off losses of main switches. This fact becomes more serious in small current operations.

In general, the turns-ratio of coupled inductors (n) is 1:1, and the boost current (I_b) controls zero-voltage commutations. Inserting n = 1 into Equation (2.23) derives the voltage equation of a discharged snubber capacitor as:

$$v_C = \frac{V_{dc}}{2}\left[1+\cos\left(\frac{t}{\sqrt{L_p \cdot C_S}}\right)\right] - \frac{I_b}{2\cdot\sqrt{\frac{C_S}{L_p}}}\cdot\sin\left(\frac{t}{\sqrt{L_p \cdot C_S}}\right) \tag{2.47}$$

Because the first term only oscillates from V_{dc} to zero, it cannot provide any interval of voltage lower than zero. However, the second term uses I_b to further reduce v_C. As shown in Figure 2.8, increasing the boost current provides a longer interval under zero voltage. Figure 2.8 shows the results obtained using the following design values: V_{dc} = 300 V, L_p = 2 μH, and C_S = 0.2 μF.

Equation (2.27) describes resonant time, clearly showing that I_b is the only controllable variable. Figure 2.9 shows the resonant times as a function of I_b with the same design values, which verifies that increasing I_b shortens the resonant time.

Equation (2.36) describes the peak value of resonant current, which is the vector sum of two currents: I_b and the peak value of the resonant tank current (I_{eq}). Figure 2.10 shows the peak values as a function of I_b, with the same design values.

As shown in Equation (2.47) and Figure 2.8, the larger boost current provides a longer interval under zero voltage. However, it increases both $\frac{dv_C}{dt}$ and the peak values of resonant current, as shown in Figures 2.9 and 2.10, respectively. The $\frac{dv_C}{dt}$ is related to common-mode EMI, and the peak value of resonant current is related to the ratings of the auxiliary devices. Therefore, the boost current selection must be made toward the goal of optimizing this trade-off.

B. Effect of Turns-Ratio of Coupled Inductors

Recently, several research papers have proposed timing control schemes related to the turns-ratio of coupled inductors. Instead of boost current, changing the turns-ratio can control several timings. By removing the boost current, the converter can reduce its losses. Moreover, the feedback of load currents might not be necessary with the assistance of auto voltage detection. However, this method makes the discharging time different from the charging time, which creates two EMI sources instead of one.

Inserting $I_b = 0$ into Equation (2.28) derives the voltage equation of a discharging snubber capacitor as:

$$v_C = \frac{V_{dc}}{n+1}\left[1 + n \cdot \cos\left(\frac{n+1}{n} \cdot \sqrt{\frac{1}{2 \cdot L_{eq} \cdot C_S}} \cdot t\right)\right] \tag{2.48}$$

As shown in Figure 2.11, increasing the turns-ratio creates a longer interval under zero voltage. Figure 2.11 shows the results obtained using the following design values: V_{dc} = 300 V, L_p = 2 μH, and C_S = 0.2 μF.

Equation (2.30) describes resonant time. Figure 2.12 shows the resonant times as a function of turns-ratio with the same design values. Although increasing n shortens resonant time, the resonant time is almost saturated at 1.75 μsec. In addition, the turns-ratio does not affect the peak value of resonant current, as shown in Equation (2.38). In

conclusion, the turns-ratio has only a slight effect on the resonant period, but it can increase the interval under zero voltage. These characteristics are helpful for designing the auxiliary circuit.

Changing the turns-ratio affects not only the resonant period but also the charging period, as shown in Equation (2.12). Figure 2.13 shows the normalized charging times and normalized resonant times as functions of turns-ratio. Because increasing the turns-ratio lengthens the charging time, the system should have a longer minimum-pulse limitation than that which is normally the sum of charging and resonant times. This increased minimum-pulse limitation has more opportunity to delete short pulses, which causes more current distortion. To maintain the charging time and turns-ratio, the resonant inductance should be reduced. However, this reduction increases the peak value of resonant current. Therefore, the turns-ratio should be minimized within the range that still guarantees a proper zero-voltage interval.

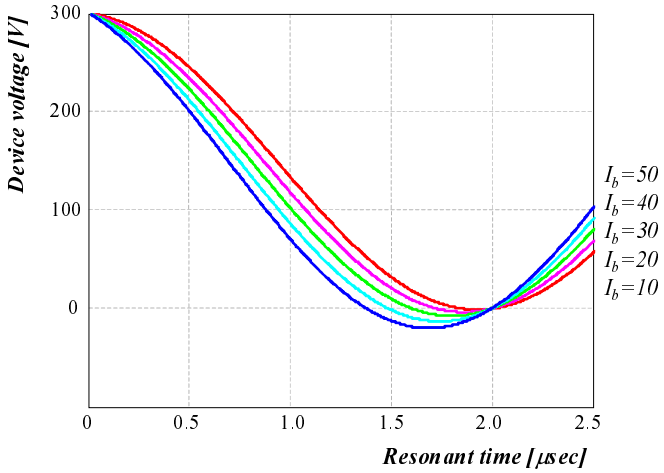


Figure 2.7 Device voltage waveforms as a function of boost current.

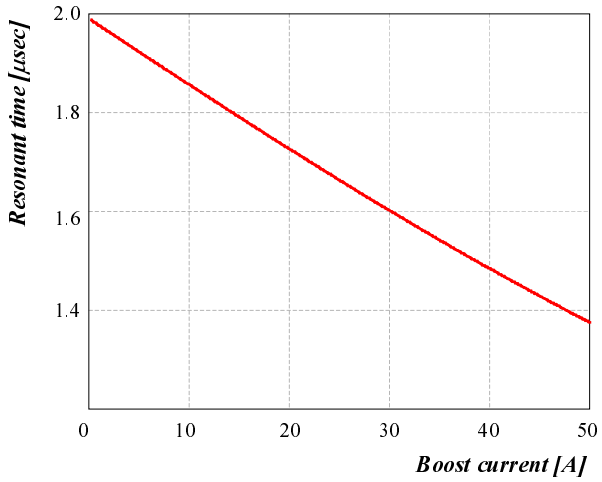


Figure 2.8 Resonant time as a function of boost current.

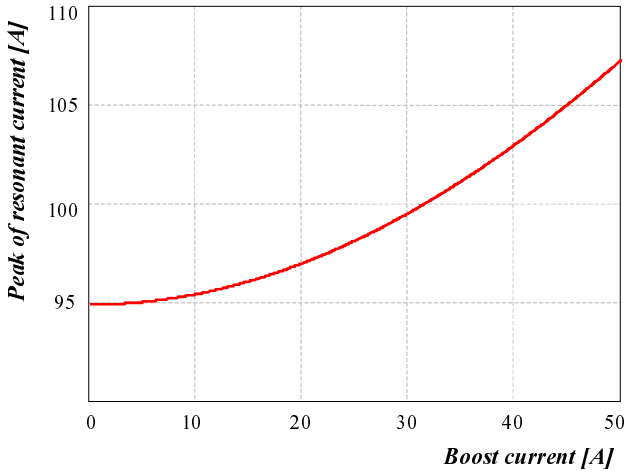


Figure 2.9 Peak value of resonant current as a function of boost current.

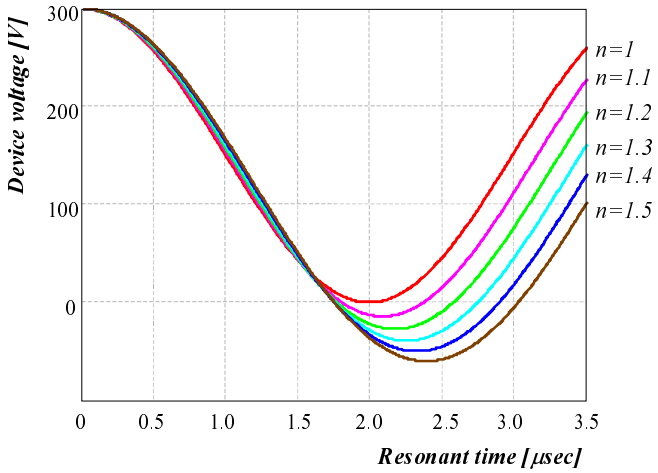


Figure 2.10 Device voltage waveforms as a function of turns-ratio.

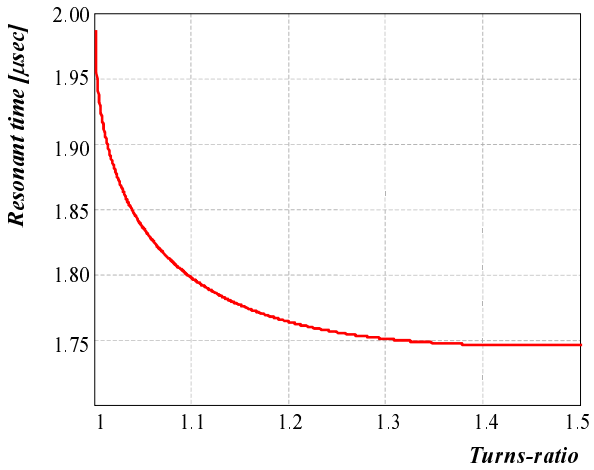


Figure 2.11 Resonant time as a function of turns-ratio.

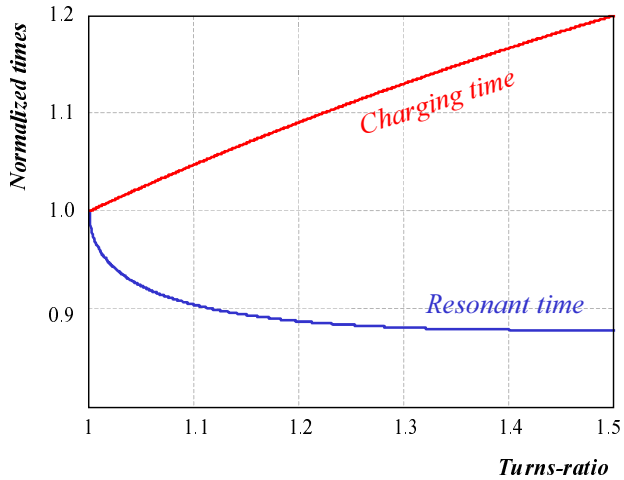


Figure 2.12 Normalized times as a function of turns-ratio.

2.4 SUMMARY

Section 2.1 reviewed and compared the conventional inductor-coupled ZVT converters. Since their first published introduction, inductor-coupled ZVT topologies have been improved several times.

Section 2.2 investigated the most advanced example, the ZVT converter with inductor feedback, based on knowledge from both former publications and real experiences. The investigation showed the advantages of the ZVT converter.

Recently, several papers have proposed the non-unity turns ratio for the coupled inductors toward the goal of advanced timing control methods. Since the former timing explanation was based on the unity turns ratio of coupled inductors, the conventional timing equations cannot be used for the non-unity turns-ratio. Section 2.3 proposed the generalized timing equations of the ZVT converter with inductor feedback, the variables of which include the turns-ratio and boost current. The generalized equations clearly show the effects of both the boost current and the turns-ratio of coupled inductors. Furthermore, the generalized equations will be used in Chapter 5, for developing the average models of the inductor-coupled ZVT topologies.

Chapter 3. NOVEL INDUCTOR-COUPLED ZERO-VOLTAGE-TRANSITION CELLS

As discussed in Chapter 2, the inductor-coupled ZVT converters achieve not only the zero-voltage commutation of main switches but also the zero-current turn-off of auxiliary switches. However, they have inherent unexpected currents. This chapter reveals the currents, and provides solutions using two novel ZVT cells.

This chapter consists of three parts: investigation of the unexpected currents, a novel ZVT cell for eliminating the currents, and another novel ZVT cell with simplified auxiliary circuit. The effort to eliminate the unexpected currents accomplishes the goal with a novel ZVT cell, and results in developing a simplified ZVT cell. The two novel ZVT cells are implemented on a 50-kW three-phase inverter, and are tested on a dynamometer.

3.1 CIRCULATING CURRENTS IN CONVENTIONAL IC ZVT CONVERTERS

Chapter 2 reviewed the literature written about the conventional inductor-coupled ZVT converters, and quantitatively established how both the boost current and turns-ratio of coupled inductors affect the timing of each operation period. The investigation verifies that the conventional inductor-coupled ZVT converters accomplish the zero-voltage commutations of main switches. However, they have inherent circulating currents through the auxiliary circuits: freewheeling current and residual magnetizing current. These circulating currents increase the losses of the auxiliary circuits and result in unexpected EMI sources. In addition, one of the currents induces the malfunction of the converters. There have been two approaches for resetting the circulating currents. One method uses saturable inductors to eliminate the residual magnetizing current [C20]. However, the saturable inductors, which increase the cost and loss of the auxiliary circuit, cannot fully eliminate the freewheeling current. Another approach uses blocking diodes in series with the auxiliary switches, but it does not help to eliminate the residual magnetizing current.

This section investigates the generating mechanism and influence of the circulating currents in conventional inductor-coupled ZVT converters. This investigation will offer insight into the elimination of the circulating currents.

3.1.1 Freewheeling Current

Figure 3.1 shows a ZVT cell of the ZVT converter with inductor feedback [C20, D10]. The cell consists of two main switches with anti-parallel diodes, two auxiliary switches with anti-parallel diodes, two additional diodes, and a coupled inductor.

When the anti-parallel diode of a main switch carries load current, the diode has its conduction voltage drop. The voltage drop is applied to the corresponding auxiliary circuit as a voltage source, and it linearly charges the leakage inductors of coupled inductors through auxiliary diodes. Since the freewheeling current is an inductor-charging current, the current is proportional to both the conduction voltage drop of the anti-parallel diode and the conduction time of the diode. Consequently, the load current is freewheeled not only through main anti-parallel diode but also through the auxiliary

circuit. For example, Figure 3.2 shows that the load current freewheels through the auxiliary circuit (D_{X1} and D_{X4}, and T_X) as well as D_1, when S_1 is in on-state.

Because the freewheeling current flows through the auxiliary diodes and coupled inductors, it induces two major problems: additional losses and EMI noise. The freewheeling current increases the conduction losses of the auxiliary circuit. Because the freewheeling paths through the auxiliary circuit include inductors as well as diodes, the increased loss of the auxiliary circuit is more than the reduced conduction loss of the main diode. Although the increased loss is not seriously large, there are newly generated instances of EMI noise. The conduction of the auxiliary diodes generates its reverse recovery current, when the opposite auxiliary switch turns on. In the case of Figure 3.3, the turn-on of S_{X2} causes the reverse recovery current of diode D_{X1}, because the diode carries the freewheeling current. The reverse recovery current provides an energy source to the resonant tank that includes the parasitic capacitance of the diode and the parasitic inductance of the auxiliary bridge. Therefore, the auxiliary switch current (i_{SX2}) contains high-frequency harmonics when the switch turns on, as indicated by the circle in Figure 3.3. These harmonics degrade the EMI performance of the converter.

3.1.2 Residual Magnetizing Current

As explained in Chapter 2, the magnetizing current of coupled inductors is generated during commutation. Since the potential of node A starts to change, the bias voltage across the magnetizing inductance of the coupled inductors increases the magnetizing current, through both the resonant and the discharging periods, as shown in Figure 3.4 (a). The magnetizing current remains in the coupled inductors after auxiliary switch S_{X1} turns off and the commutation is completed, as shown in Figure 3.4 (b). Although S_{X1} turns off, the residual magnetizing current freewheels through a turned-on main switch (S_1) and an auxiliary diode (D_{X4}), as shown in Figure 3.4 (c). Because there is no reverse bias to T_{X1}, this current cannot be reset. Eventually, it is accumulated through several switching cycles until the load current changes its direction, and it becomes a large current. The accumulated current finally induces malfunction of the converter operation.

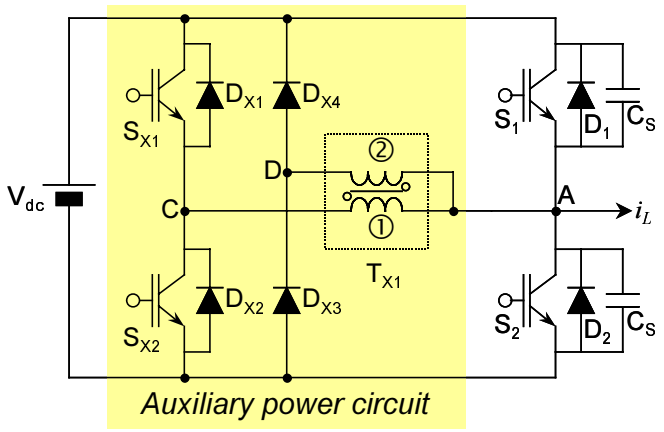


Figure 3.1 A ZVT cell of the ZVT converter with inductor feedback.

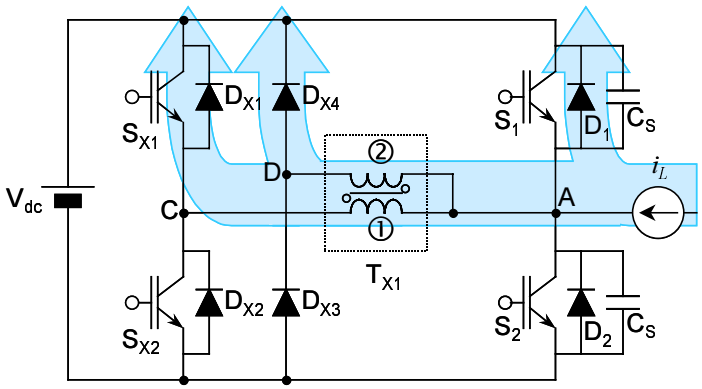


Figure 3.2 Freewheeling current paths when load current flows into the converter.

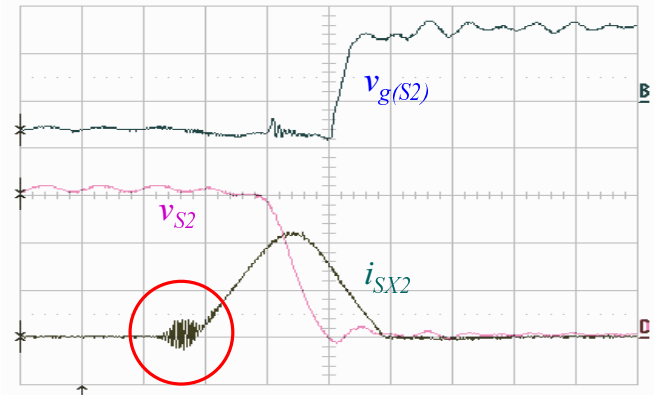


Figure 3.3 Experimental waveforms of the ZVT converter with inductor feedback.
– High-frequency harmonics on i_{SX2} when S_{X2} turns on.

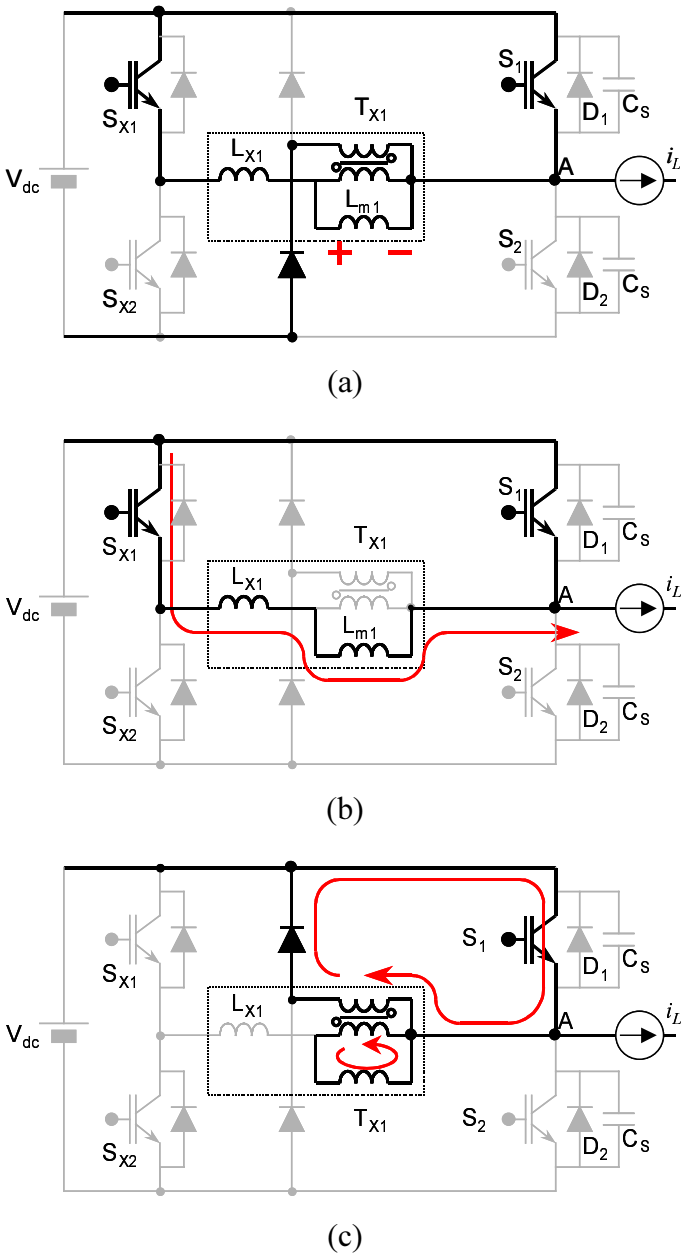


Figure 3.4 Generation and paths of magnetizing current:

(a) During discharging period,

(b) Residual magnetizing current before S_{X1} turns off, and

(c) Residual magnetizing current after S_{X1} turns off

3.1.3 Conventional Approaches for Eliminating Circulating Currents

The residual magnetizing current causes problems only in the True-PWM-Pole ZVS pole converter [C4, C23-C24] and the ZVT converter with inductor feedback [C20, C24, D10]. In the Transformer-assisted ZVS Pole converter, the residual magnetizing current is automatically reset through the secondary winding. Because the ZVT converter with inductor feedback has better performance than the Transformer-assisted ZVS Pole converter, there have been two approaches for eliminating the circulating currents [C20, C24]. Both approaches propose ideas for blocking the circulating currents. Even if the approaches eliminate the currents, they require additional components.

A. Using a Saturable Inductor

The residual magnetizing current must be reset before the next commutation. One possible way to reset the magnetizing current is to disconnect the auxiliary circuit from the main bridge. Inserting a saturable inductor in series with the coupled inductor is one of the best ways, as shown in Figure 3.5 (a). Saturable inductor M_1 is not necessary from the charging to the discharging periods. After the load current flows only through the main switch and the auxiliary switch turns off, half the DC voltage is applied to M_1 as a reverse bias. The square-loop B-H characteristic of the saturable inductor blocks any current path opposite to the former auxiliary current. Eventually, M_1 blocks the freewheeling paths of the residual magnetizing current shown in Figure3.4 (c). Figure 3.5 (b) shows the new current path for the magnetizing current, provided by a saturable inductor. The saturable inductor M_1 allows the current to flow through either D_{X2}⇨C⇨B⇨D⇨D_{X4} or D_{X3}⇨D⇨B⇨C⇨D_{X1}. These current paths give reverse bias to the coupled inductor, and the reverse bias resets the residual magnetizing current. This method has already been proposed for the ZVT inverter with inductor feedback [C20], and can be applied to the True-PWM-Pole ZVS pole inverter. It solves the residual magnetizing current problem and allows the three-phase operation of the ZVT inverter, such as that required by an induction motor driving system [D10, D17]. However, the size of the saturable inductor must be large in order to block the reverse bias during the entire reset period. It causes additional cost, space, and loss concerns. In addition, it cannot solve the problem of freewheeling current.

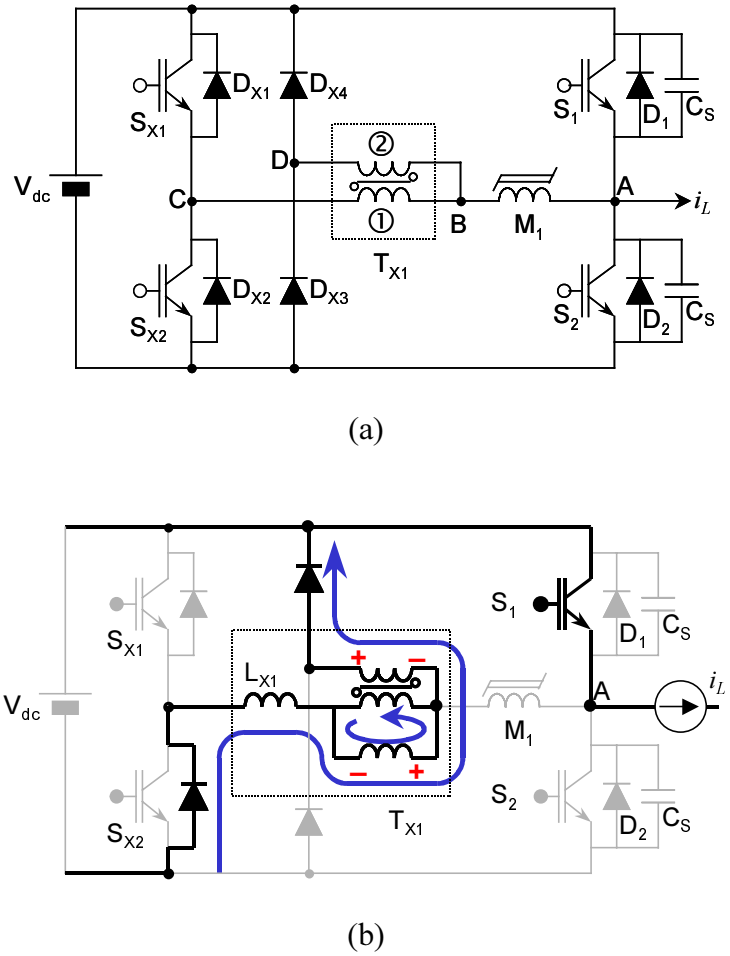


Figure 3.5 Resetting the magnetizing current using a saturable inductor:

(a) Power stage with a saturable inductor, and

(b) Current paths and reverse bias applied to T_{X1}.

B. Using a Blocking Diode

Another approach attempted to solve the circulating current problems using two blocking diodes (D_{B1} and D_{B2}) in series with auxiliary switches, as shown in Figure 3.6 [C24]. The published paper using this method claims that the diodes can reset the residual magnetizing current. However, the residual magnetizing current does not flow through any anti-parallel diodes of the auxiliary switches, as shown in Figure 3.4 (c). Therefore, the blocking diodes cannot block the residual current paths, so the current cannot be reset. Instead of resetting the magnetizing current, the blocking diodes have another function. The freewheeling current flows through the anti-parallel diode of an auxiliary switch and another auxiliary diode, as shown in Figure 3.2. Because two inductors are coupled, the freewheeling current cannot pass the auxiliary circuit by removing one of the diodes. Inserting a diode in series with an auxiliary switch is the same as removing the anti-parallel diode of the switch. Therefore, the proposed blocking diode can block the freewheeling current path through the auxiliary circuit. This function improves the loss and EMI performances. However, this method cannot reset the residual magnetizing current.

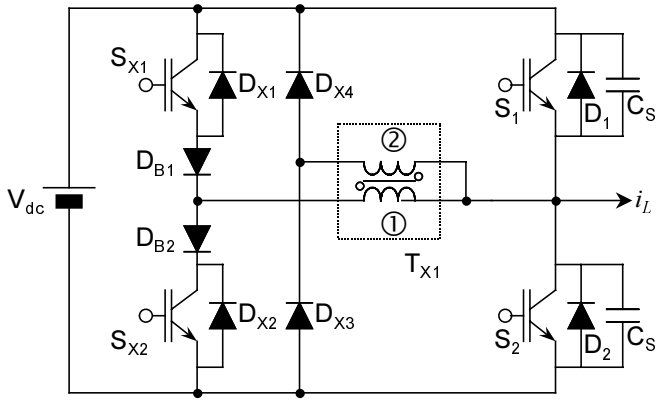


Figure 3.6 Power stage with blocking diodes.

3.2 A NOVEL IC ZVT CELL WITH IMPROVED EFFICIENCY AND EMI

No existing conventional approach can completely resolve the circulating current problems. Although the method using a saturable inductor resets the residual magnetizing current, it is disadvantageous in terms of cost and space. In addition, it still has high-frequency harmonics due to the freewheeling current. This section proposes a novel IC ZVT cell that removes the circulating currents [C38]. The proposed cell improves performance by removing the circulating current, and saves cost and space by removing a saturable inductor.

3.2.1 Power Stage of Proposed ZVT Cell

In the conventional ZVT cell with a saturable inductor shown in Figure 3.7 (a), whenever any auxiliary switch turns on, the DC input voltage V_{dc} is applied across only winding ① of T_{X1} and creates a charging current through an auxiliary inductor (the leakage inductance of T_{X1}). Therefore, winding ① serves the same function as the primary winding of a transformer. On the other hand, winding ② of T_{X1} has a current reflected from winding ①, and this winding does not have any bias voltage; it functions as a secondary winding. In summary, the conventional ZVT cell always uses winding ① as a primary winding and winding ② as a secondary winding.

In order to use both windings as primary windings, both S_{X2} and D_{X2} can simply exchange their positions with D_{X3}, as shown in Figure 3.7 (b). Then, winding ① becomes a primary winding when S_{X1} turns on, as does winding ② with S_{X2}. This modified power stage provides the same zero-voltage conditions for the main switch turn-on commutations as those provided by the conventional ZVT cell. The auxiliary current paths, however, are somewhat different from those of the conventional cell. For the commutation from D_2 to S_1, S_{X1} and D_{X2} carry the auxiliary current. During the reset period, the residual magnetizing current flows through D_{X3} and D_{X4} so that it is reset by reverse bias. In the same manner, even if S_{X2} and D_{X1} carry the auxiliary current for the commutation from D_1 to S_2, the magnetizing current still flows through D_{X3} and D_{X4}. Both D_{X3} and D_{X4} are used only for resetting the magnetizing current, no matter which type of commutation occurs. Therefore, a reset winding (winding ③) of T_{X1} in series with

D_{R1} can simply replace the reset path through D_{X3} and D_{X4}, as shown in Figure 3.7 (c). While the zero-voltage commutations of the main switch are achieved using two windings of T_{X1}, S_{X1}, D_{X1}, S_{X2} and D_{X2} of the modified ZVT cell, winding ③ and D_{R1} reset the residual magnetizing current. This ZVT cell no longer requires a saturable inductor. In addition, the coupling effect of the three windings blocks the freewheeling current before an auxiliary switch turns on. Finally, the power stage shown in Figure 3.7 (c) resets the residual magnetizing current, and blocks the freewheeling current as well. This chapter proposes the power stage as a novel inductor-coupled ZVT cell that solves the circulating current problems.

This power stage has four specific characteristics, as follows:

- There is no freewheeling current in the auxiliary circuit,
- If node A is connected to the positive DC rail, only S_{X2} can generate inductor current,
- If node A is connected to the negative DC rail, only S_{X1} can generate inductor current, and
- After an auxiliary switch turns off, the magnetizing current passes only through winding ③.

3.2.2 Operation Principles

A. Space-Vector-Modulation Scheme

The proposed ZVT cell operates independently – without any interference with other phases – so a three-phase ZVT inverter with the proposed ZVT cells is able to operate using any conventional SVM scheme, without requiring any modifications. This characteristic allows piggybacking of both the auxiliary circuit and its control circuit.

B. Zero-Voltage Turn-On Commutations

The auxiliary circuit should assist both cases of zero-voltage turn-on commutations: a commutation from diode to switch and a commutation from switch to diode with low load current. The auxiliary circuit of the proposed ZVT cell can assist both commutations.

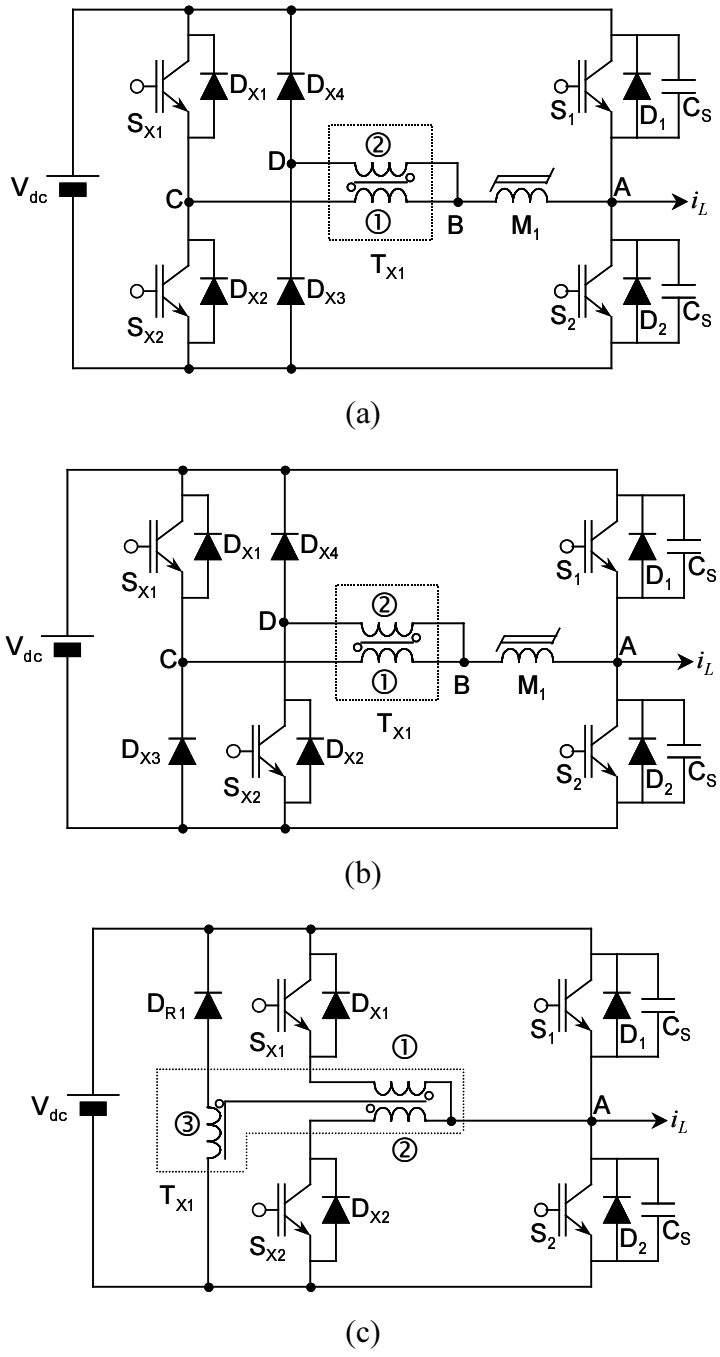


Figure 3.7 Modification procedures and a novel ZVT cell:

(a) Conventional ZVT cell with a saturable inductor,

(b) Exchanging the location of S_{X2} and D_{X3}, and

(c) A novel ZVT cell with a reset winding.

Figure 3.8 shows several waveforms of corresponding devices during the zero-voltage turn-on commutations for both cases. This figure clearly shows the zero-voltage turn-on of the main switches and the zero-current turn-off of the auxiliary switches in both cases.

For one case of zero-voltage turn-on of the main switches, Figure 3.8 (a) shows the commutation waveforms when the load current i_L is positive. At this moment, the load current conduction is changed from a main diode D_2 to a main switch S_1 with the operation of an auxiliary switch S_{X1}. Figure 3.9 shows the detailed current conduction statuses of all commutation periods. The following descriptions refer to the commutation.

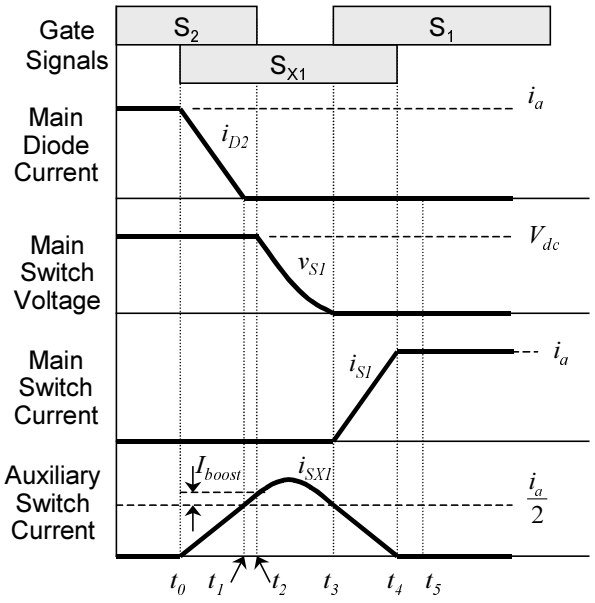
- *Before commutation* [before t_0] : Because D_2 carries the load current, the potential of node A is the same as that of the negative DC rail.
- *Charging period* [$t_0 \sim t_1$] : When S_{X1} turns on at t_0, the potential of node A allows V_{dc} to be applied to the leakage inductor L_{X1} in winding ① of T_{X1}. This applied voltage generates an auxiliary switch current through S_{X1} and D_{X2}. This current i_{SX1} increases linearly and reaches half the load current i_L at t_1. Winding ② carries the same amount of current as i_{SX1} through D_{X2}. Due to these auxiliary currents, the main diode current i_{D2} decreases linearly and reaches zero at t_1. Therefore, D_2 can turn off with a zero-current condition.
- *Boost period* [$t_1 \sim t_2$] : The boost current I_{boost} is required to compensate for loss factors during the resonant period. After t_1, both S_2 and S_{X1} maintain on-states in order to add I_{boost} to the auxiliary switch current. At t_2, i_{SX1} reaches the sum of I_{boost} and half the load current.
- *Resonant period* [$t_2 \sim t_3$] : When S_2 turns off at t_2, the leakage inductor L_X starts to resonate with the capacitors (C_S) across both S_1 and S_2. This resonant operation charges the capacitor across S_2 and discharges the capacitor across S_1. When the voltage across the main switch S_1 reaches zero at t_3, this main switch turns on with a zero-voltage condition.
- *Discharging period* [$t_3 \sim t_4$] : Since S_1 turns on with zero-voltage condition at t_3, node A remains connected to the positive DC rail. This potential applies

V_{dc} to both winding ② and L_X as the reverse bias of the inductor current. Due to this bias, i_{SX1} decreases linearly and i_{S1} increases linearly. When i_{SX1} reaches the magnetizing current of T_{X1} at t_4, S_{X1} turns off with a zero-current condition, and S_1 carries all load current i_L. The required time for this period is proportional to the load current value. The actual time should be longer than the required time, in order to ensure a real zero-current condition for the turn-off of S_{X1}.

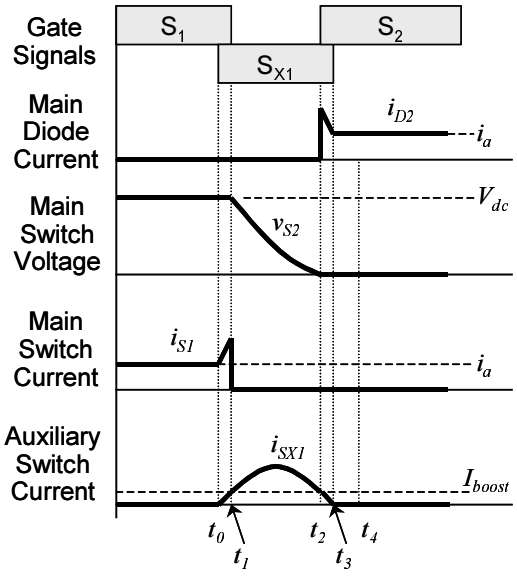
- *Reset period* [$t_4 \sim t_5$] : When S_{X1} turns off with a zero-current condition at t_5, the coupled inductor T_{X1} holds the magnetizing energy. While diodes D_{X1} and D_{X2} block the magnetizing current paths through winding ① and ② of T_{X1}, winding ③ provides the current paths through D_{R1}. This current path allows V_{dc} to be applied to winding ③ as reverse bias. Therefore, the magnetizing energy is totally reset at t_5. When winding ③ carries the magnetizing current, the reflected voltage of V_{DC} is applied to windings ① and ②.

- *After commutation* [$t_5 \sim$] : The load current flows only through S_1, and there is no energy in the auxiliary circuit.

Figure 3.8 (b) shows several corresponding waveforms of the zero-voltage commutation from a main switch S_1 to a main diode D_2 when the value of load current i_L is positive and small. Because the load current is not large enough to change the potentials of snubber capacitors in the designed commutation time, this commutation requires an energy source to accelerate the real commutation time. Turning on auxiliary switch S_{X1} creates the energy source in the auxiliary inductor. This energy source helps this commutation by quickly charging and discharging the corresponding snubber capacitors. This figure shows the zero-voltage turn-on of the main switches as well as the zero-current turn-off of the auxiliary switches.



(a)



(b)

Figure 3.8 Zero-voltage turn-on commutation waveforms:

(a) From diode to switch, and

(b) From switch to diode with low load current.

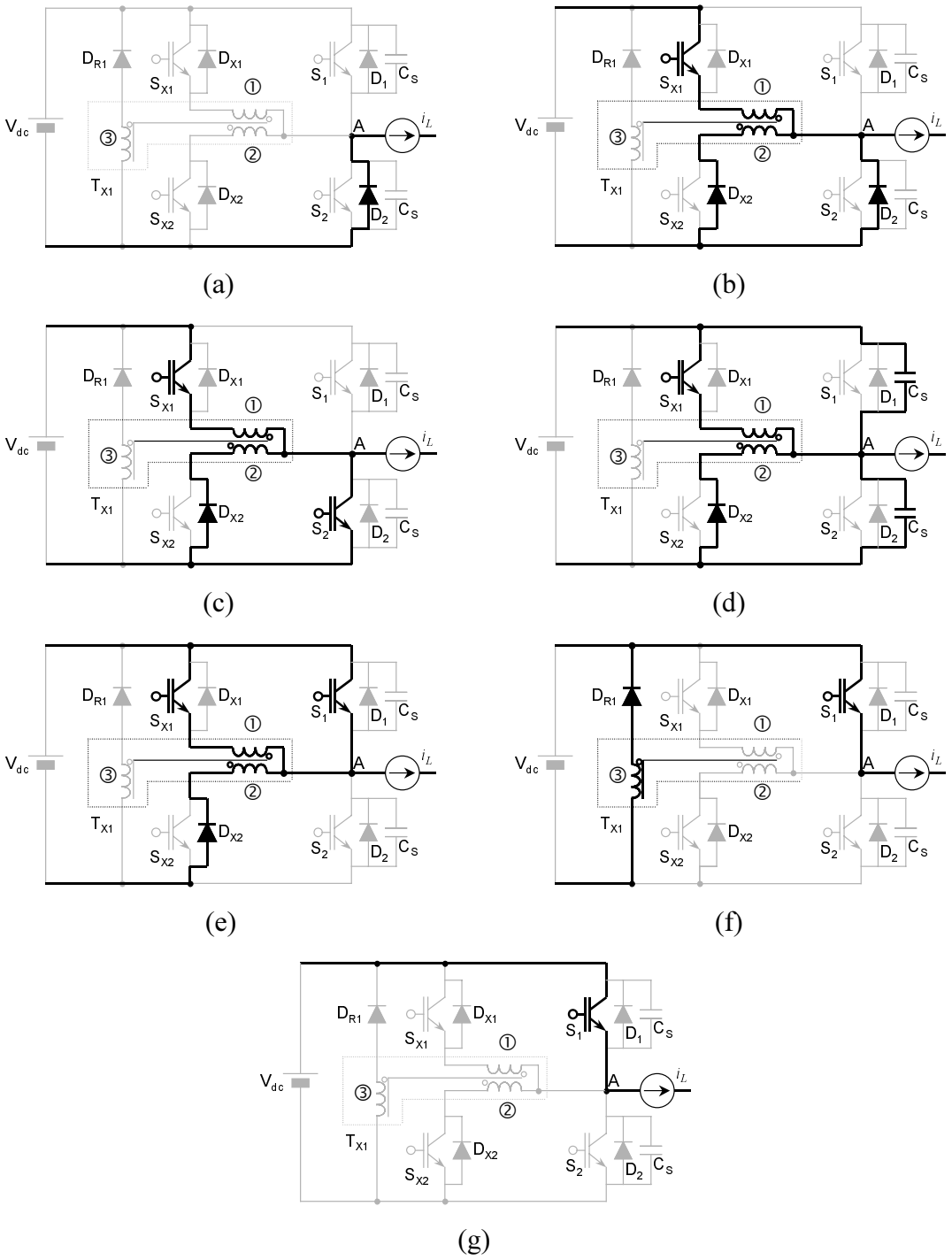


Figure 3.9 Commutation description of sequential periods from diode to switch:

(a) Before commutation, (b) Charging period, (c) Boost period,

(d) Resonant period, (e) Discharging period, (f) Reset period, and

(g) After commutation.

3.2.3 Timing Control and Design Issues

A. Timing Control

Since the operation principles are the same as those of the conventional ZVT cell, the charging, boost, resonant and discharging times can be represented by using Equations (2.12), (2.13), (2.27), and (2.45) that are newly derived in Section 2.3. The turns-ratio of coupled inductors is always 1:1. Therefore, these equations are changed to Equations (3.1)–(3.4) by using $n = 1$:

Charging time $[t_0, t_1]$ $$T_{ch} = L_p \cdot \frac{i_L}{V_{dc}} \tag{3.1}$$

Boost time $[t_1, t_2]$ $$T_b = L_p \cdot \frac{I_b}{V_{dc}} \tag{3.2}$$

Resonant time $[t_2, t_3]$ $$T_{res} = 2\sqrt{L_p \cdot C_S} \cdot \arctan\left(\frac{V_{dc}}{I_b} \cdot \sqrt{\frac{C_S}{L_p}}\right) \tag{3.3}$$

Discharging time $[t_3, t_4]$ $$T_{dis} = L_p \cdot \frac{i_L}{V_{dc}} + L_p \cdot \frac{I_b}{V_{dc}} \tag{3.4}$$

where V_{dc} : DC input voltage
i_L : load current
I_b : boost current
L_p : leakage inductance of one coupled inductor
C_S : snubber capacitance

Once the values of both L_p and C_S are selected, the resonant time of the LC tank becomes fixed regardless of the load current, as shown in Equation (3.3). The proposed ZVT topology can operate with an optimized condition by adjusting the charging period (t_0~t_1) and the discharging period (t_3~t_4) proportional to the load current value, as shown in use of Equations (3.1) and (3.4). Because the turns-ratio of the proposed ZVT cell is always 1:1, the boost current (I_b) is the only way to compensate for the resonant losses of the auxiliary circuit, as shown in Equation (3.2). Theoretically, the boost period (t_1~t_2) should be adjusted in proportion to the load current, in order to guarantee the perfect zero-voltage condition in any case. Since calculating the resonant losses is so difficult,

the boost period is set to one value that is sufficient to create the zero-voltage condition, as shown in Equation (3.2).

B. Design of Reset Winding

The magnetizing inductance (L_m) of T_X is charged during both the resonant and the discharging periods. Average value of voltage across the inductance is half the DC voltage during the resonant period, and it is DC voltage during the discharging time. Therefore, a charged voltage-second (*V-sec*) for L_m is described as Equation (3.5):

$$V \cdot \sec = \frac{V_{dc}}{2} \cdot T_{res} + V_{dc} \cdot T_{dis} \tag{3.5}$$

During the reset period, one over n_{res}-times of V_{dc} is reflected from the reset winding (winding ③) to both windings ① and ②. Therefore, a discharged *V-sec* for L_m is described as Equation (3.6):

$$V \cdot \sec = \frac{V_{dc}}{n_{res}} \cdot T_{reset} \tag{3.6}$$

In order to completely reset the magnetizing energy of T_X, Equation (3.5) must be equal to Equation (3.6).

In general, the duration of one switching period determines the available range of T_{reset}. By combining Equations (3.5) and (3.6), the available range of T_{reset} can derive the range of n_{res}, as shown in Equation (3.7):

$$n_{res} = \frac{2 \cdot T_{reset}}{T_{res} + 2 \cdot T_{dis}} \tag{3.7}$$

This equation clearly shows that T_{reset} can be shorten by using a small n. However, the reflected voltage on either winding ① or ② increases the reverse voltage across D_{X1} or D_{X2}, respectively. Equation (3.8) describes the reverse voltage:

$$v_{DX1} = V_{dc} + \frac{V_{dc}}{n_{res}} \tag{3.8}$$

Therefore, the number of turns for the reset winding should be maximized in the range of that it does not increase the voltage ratings of auxiliary devices.

3.2.4 Simulation and Loss Analysis

A. Simulation Results

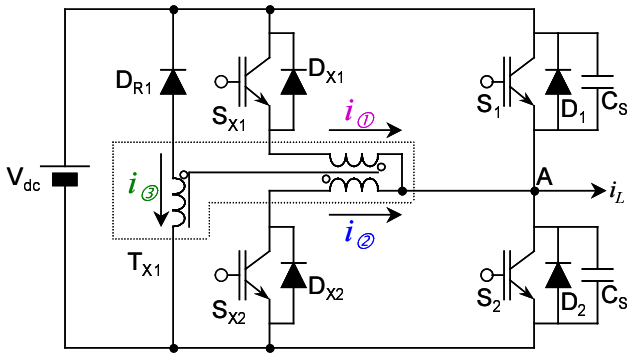
Figure 3.10 (a) defines several current variables for the simulation results of the proposed ZVT cell. The designed values of the resonant components in the proposed ZVT cell are as follows: C_S = 0.1 μF, L_X = 4 μH, I_{boost} = 10 A, and V_{DC} = 300 V. The turns-ratio for windings ①:②:③ of a coupled inductor is 1:1:10.

Figure 3.10 (b) shows the simulation results for the zero-voltage turn-on commutation from D_2 to S_1 when i_L = 200A. At t_0, the turn-on of S_{X1} starts to both increase i_{SX1} and to decrease i_{D2}. The resonant operation begins at t_2, and the main switch S_1 turns on with a zero-voltage condition at t_3. The auxiliary switch S_{X1} turns off with a zero-current condition at t_4. These waveforms verify that the proposed inverter accomplishes the expected zero-voltage turn-on commutation.

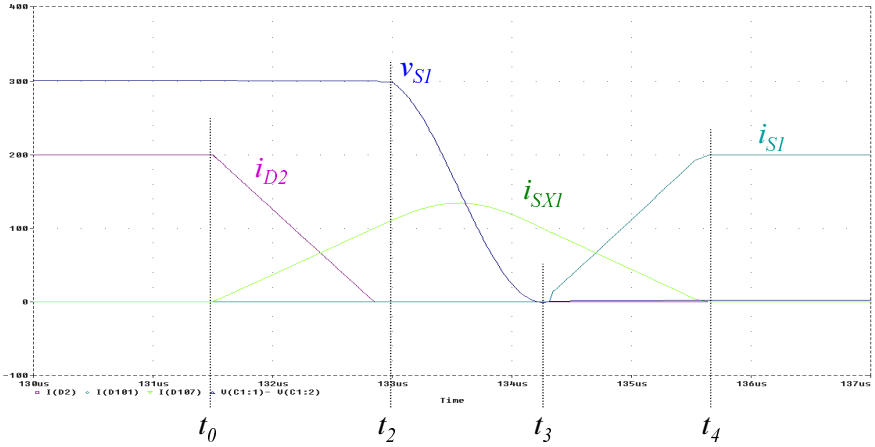
Because the proposed ZVT cell has a reset winding as a new component, verifying the reset operation through the winding is also important. Figure 3.10 (c) shows the simulation results of the reset operation. Even if the current of winding ② ($i_②$) becomes zero at t_{31}, winding ① still carries some current that is the same as the residual magnetizing current of the coupled inductor. When the auxiliary switch turns off at t_4, the magnetizing current is reflected to winding ③. Before t_{41}, currents $i_①$ and $i_②$ become zero, and only winding ③ carries the magnetizing current. This current path provides a reverse bias that can reset the magnetizing current. This simulation result clearly shows that the proposed ZVT cell resets the magnetizing current without requiring a saturable inductor.

B. Loss Analysis

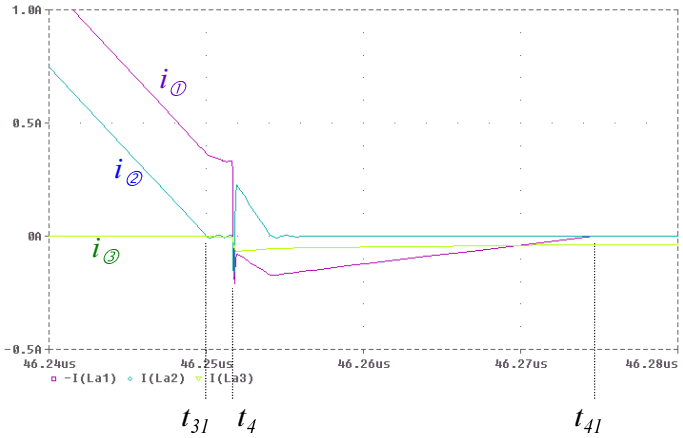
Because all commutation patterns are the same as those of the conventional ZVT converter with inductor feedback, the switching losses of the main switches are also the same values as those of the conventional ZVT converter. Eliminating the freewheeling current reduces not only the conduction losses but also switching losses of the auxiliary circuit. In addition, the losses of the saturable inductor are removed. Therefore, the novel ZVT converter with the proposed ZVT cells can achieve greater loss reduction in hard-switching converters than those achieved by the conventional ZVT converters.



(a)



(b)



(c)

Figure 3.10 Simulation results of the proposed ZVT cell:

(a) Simulation circuit and current definitions,

(b) One commutation cycle from diode to switch, and

(c) Current of each winding just before reset period.

3.2.5 Implementation and Experiments in Three-Phase Inverter

A. Implementation of Main Power Stage

The power stage of a three-phase ZVT inverter using the proposed ZVT cell is decomposed into two groups: the main power stage and the auxiliary power stage. The main power stage is the same as the power stage of a hard-switching inverter. The electric specifications of the implemented inverter are as follows:

- Maximum output power rating: 50 kW,
- Nominal DC input voltage: 325 V, and
- Switching frequency: 10 kHz.

For the maximum output power, the RMS value of the load current reaches approximately 200 A. The main power device is selected on the basis of the required current, DC voltage, and switching frequency; Toshiba half-bridge IGBT module (MG300J2YS50) is chosen, which has 300 A and 600 V ratings. Three 2400 μF capacitors comprise the DC link capacitor bank, and two laminated copper bus bars connect the main power devices and the DC capacitor bank. Two current sensors send the load current feedback of phases A and C to the control board. Figure 3.11 shows the implemented main power stage.

B. Design of Auxiliary Passive Components

The auxiliary circuit consists of auxiliary switches, auxiliary diodes, and passive components. The passive components include coupled inductors, snubber capacitors, saturable inductors, and RC snubber circuits for the auxiliary switches.

The auxiliary resonant inductance is initially determined from the proper *di/dt* value. Then, the snubber capacitance is chosen within a reasonable range of resonant characteristics and turn-off losses. This inverter uses 3.25 μH as the resonant inductance (L_X), which is calculated using di/dt = 100 A/μsec. The inverter also uses 0.22 μF as the snubber capacitance (C_S), which is chosen from commercial capacitors based on the characteristics of their turn-off loss reductions.

Because the leakage inductance of the coupled inductor is used as the resonant inductance, the coupled inductors should be designed using a proper winding method, in

order to produce the chosen resonant inductance. Throughout the design procedure using the inductance and a coupling factor (k), the coupled inductor is designed as follows:

- Core: ETD49-3C85 (Philips), and
- Number of turns of windings ① and ②: 19 turns

The designed coupled inductor has a magnetizing inductance of 1.2 mH and a leakage inductance of 3.5 μH. According to the proposed concept, the number of turns for the reset winding (winding ③) is 190 – ten times those of other windings. However, the reset winding has made serious problems in making the coupled inductors. The next section will discuss this issue and provide a new design approach.

C. Modification of Reset Circuit

Although the coupled inductor is designed in order to produce the chosen resonant inductance, the reset winding becomes another factor of the coupled inductor. In general, the number of turns for the reset winding is several times that of another winding. Due to the reset winding, the coupled inductor easily loses its characteristic at low frequency range. The formerly designed coupled inductor (19 turns for windings ① and ②, and 190 turns for winding ③) loses its magnetizing inductance at nearly 100 kHz. Since the resonant frequency is 182 kHz, the coupled inductor cannot be used as an auxiliary inductor. Therefore, the number of turns for the reset winding should become smaller, in order to improve the frequency characteristic. However, the smaller number of turns increases the collector-emitter voltage of the auxiliary switch, as explained in Section 3.2.3.B.

Figure 3.12 shows an alternative with the smaller number of turns. The original reset winding is connected to the DC bus through a diode, as shown in Figure 3.7 (c). The alternative makes a loop using the reset winding, a diode (D_{R1}), and a resistor (R_1), as shown in Figure 3.12. The diode allows a current path only for the reset operation. The number of turns for the reset winding and the resistance R_1 determine the reset time and the reflected voltage on the other two windings. This structure allows the number of turns for the reset winding small, which improves the frequency characteristics of the coupled inductor beyond the resonant frequency.

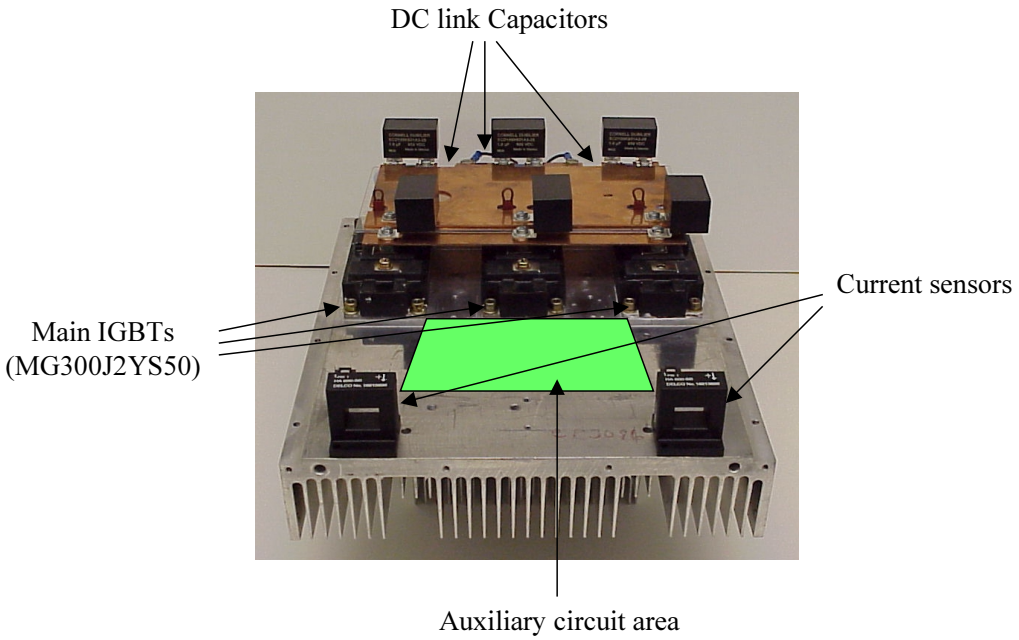


Figure 3.11 Assembled main power stage of three-phase inverter.

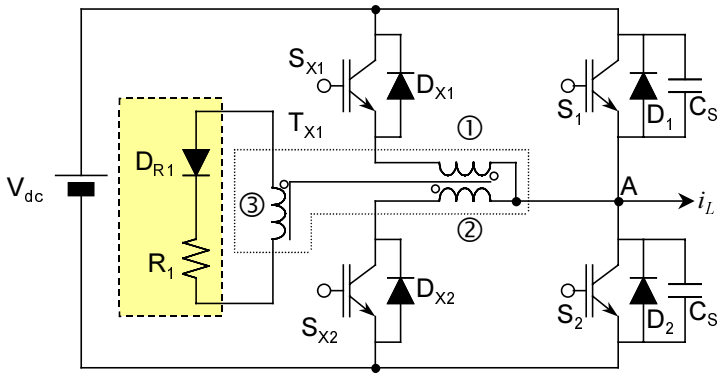


Figure 3.12 Modified reset circuit.

Figure 3.13 shows an assembled coupled inductor using the proposed reset circuit. The number of turns for the reset winding is 30 – approximately 1.5 times those of other windings. The diode is a fast recovery type diode with the rating of 800V/1A. The resistance is 100 Ω.

D. Assembled ZVT Cell

Because of the turns-ratios of the designed coupled inductor, the voltage stresses of the auxiliary switches and diodes are about 10% higher than the DC voltage. The voltage stresses are just 357.5 V, which does not exceed the voltage rating of general power devices (600 V). Therefore, the auxiliary IGBTs and diodes are chosen as follows:

- Auxiliary IGBT: IXGN200N60A (600V/200A), and
- Auxiliary diode: BYT230PIV800 (800V/150A)

Figure 3.14 shows the assembled power stage of one ZVT cell. The snubber capacitors are mounted directly on top of the main IGBT module. Since the selected IGBT does not have anti-parallel diode, the IGBT is in parallel with one diode in the selected diode (BYT230PIV800).

E. Experimental Results

Figures 3.15 and 3.16 show the experimental results of the implemented ZVT inverter using the proposed ZVT cells.

As shown in Figure 3.15 (a), the peak of the auxiliary current is moving in accordance with the load current value. The collector-emitter voltage of S_2 does not have any high peak, and most of them are almost the same as the DC voltage. Figure 3.15 (b) shows the zoomed waveform from Figure 3.15 (a) when the load current is almost zero, and Figure 3.15 (c) shows the zoomed waveform when the load current is approximately 60 A. The auxiliary switch current is properly shaped, and the device voltage is smoothly changed from zero to V_{dc} in the designed commutation time (1.8 μsec).

Figure 3.16 shows the experimental results with more load than Figure 3.15. The collector-emitter voltage of S_2 does not have any high peak, as shown in Figure 3.16 (a). Figure 3.16 (b) is the zoomed waveform when the load current is approximately 120 A, which shows the smooth change of the main device voltage.

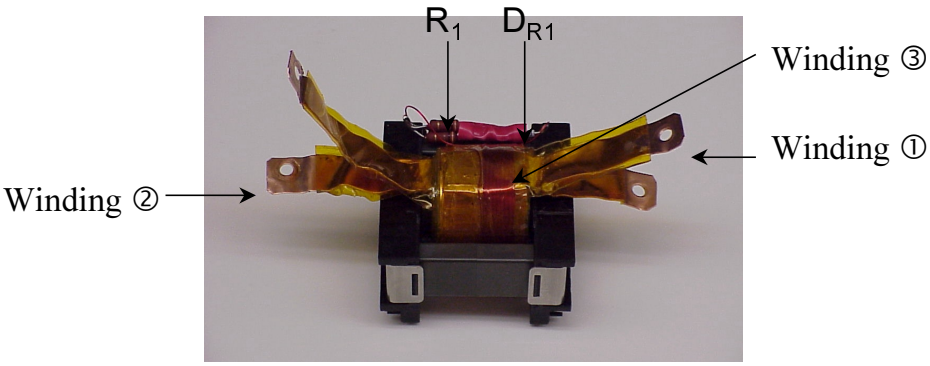


Figure 3.13 Assembled coupled inductor.

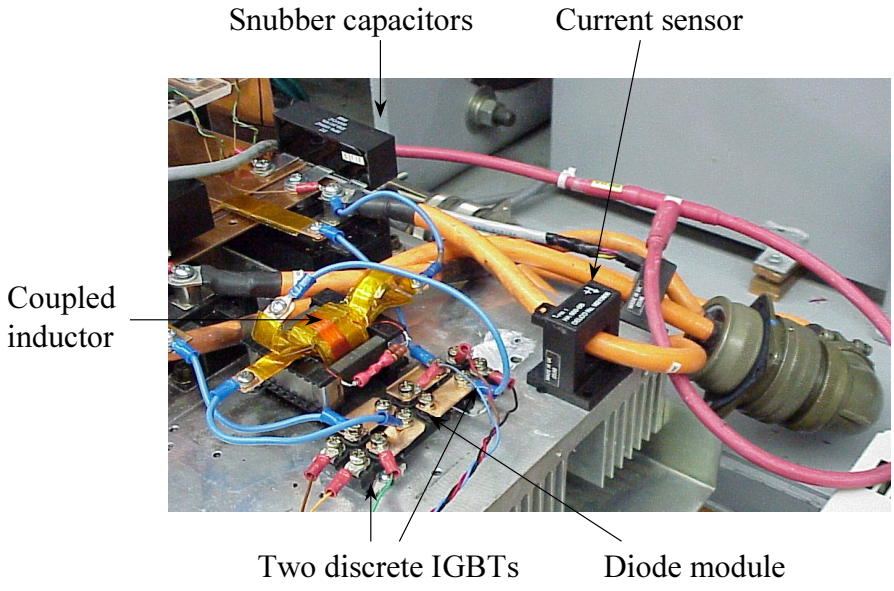
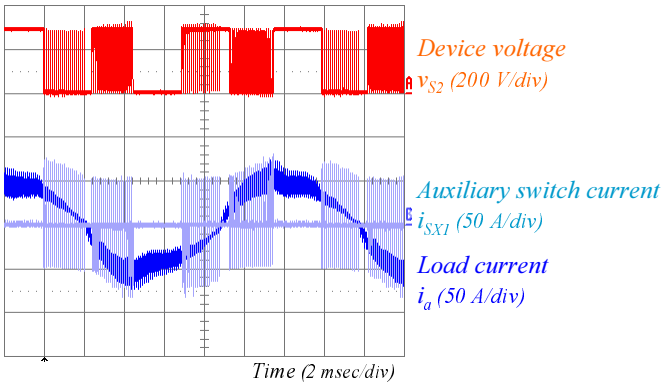
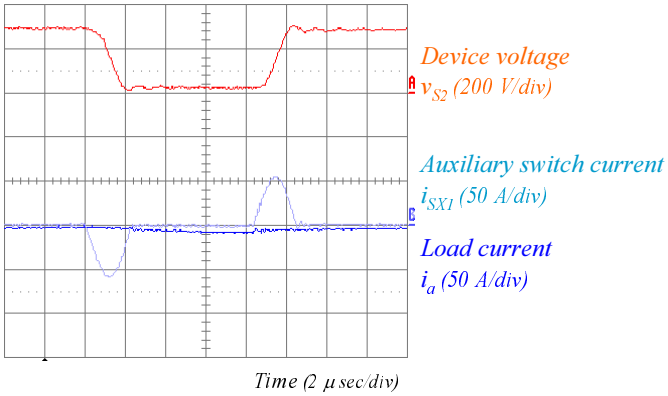


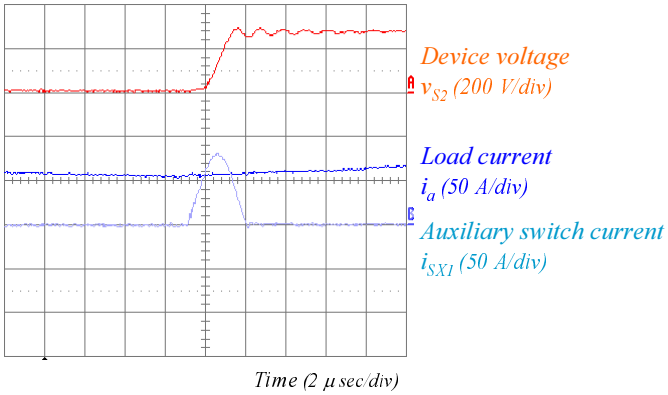
Figure 3.14 Assembled power stage of one ZVT cell.



(a)



(b)



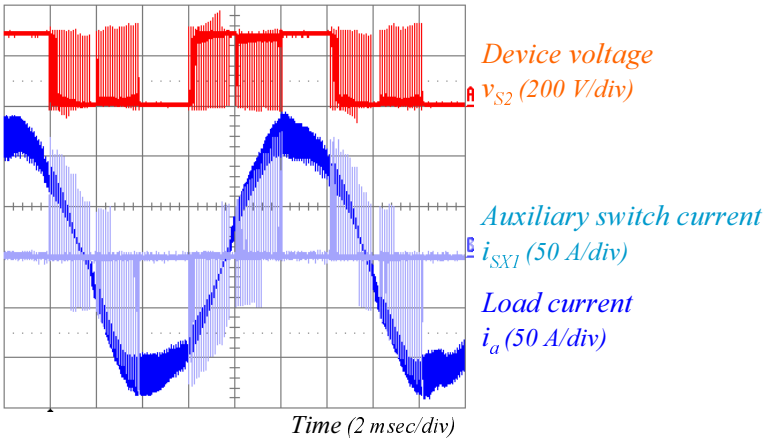
(c)

Figure 3.15 Measured experimental waveforms:

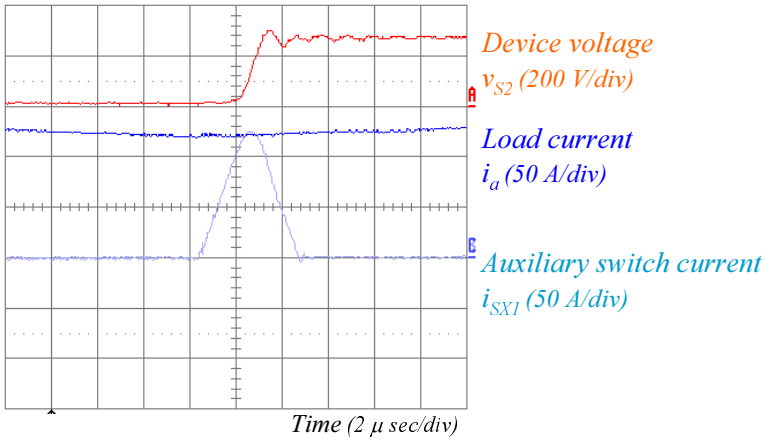
(a) Waveforms in a line cycle,

(b) Waveforms when the load current is nearly zero, and

(c) Waveforms when the load current is 60 A.



(a)



(b)

Figure 3.16 Measured experimental waveforms:

(a) Waveforms in a line cycle, and

(b) Waveforms when the load current is 120 A.

3.3 SINGLE-SWITCH SINGLE-LEG (S^3L) ZVT CELL

As mentioned in Chapter 1, several proposals have aimed to simplify the auxiliary circuit of three-phase ZVT converters. Although their performances are not as good as those of ZVT converters with six auxiliary switches, there are still demands for simplifying the auxiliary circuits. In general, the demands require that the performances of the converters with simplified auxiliary circuits should be the same as those of ZVT converters with six auxiliary switches, while the cost and space are less.

The ZVT cell newly proposed in Section 3.2 achieves better performance than does the conventional ZVT cell. This cell, however, still has two auxiliary switches. This section describes how to simplify the auxiliary circuit of the ZVT cell proposed in Section 3.2, and eventually proposes a novel ZVT cell with a simplified auxiliary circuit [C35].

3.3.1 Power Stage of Proposed ZVT Cell

As mentioned in Section 3.2.1, the power stage shown in Figure 3.17 (a) has four specific characteristics:

- There is no freewheeling current in the auxiliary circuit,
- If node A is connected to the positive DC rail, only S_{X2} can generate inductor current,
- If node A is connected to the negative DC rail, only S_{X1} can generate inductor current, and
- After an auxiliary switch turns off, the magnetizing current passes only through winding ③.

These four characteristics lead logically to simplification of the auxiliary circuit. Auxiliary switches and anti-parallel diodes (S_{X1}, S_{X2}, D_{X1} and D_{X2}) can simply move to node A, as shown in Figure 3.17 (b). When node A is connected to the negative DC rail, both S_{X1} and D_{X2} provide auxiliary current paths. Therefore, there is no difference in zero-voltage operation, although the emitter of S_{X1} is connected to the anode of D_{X2}. For the same reason, the collector of S_{X2} is connected to the cathode of D_{X1}. Eventually, the

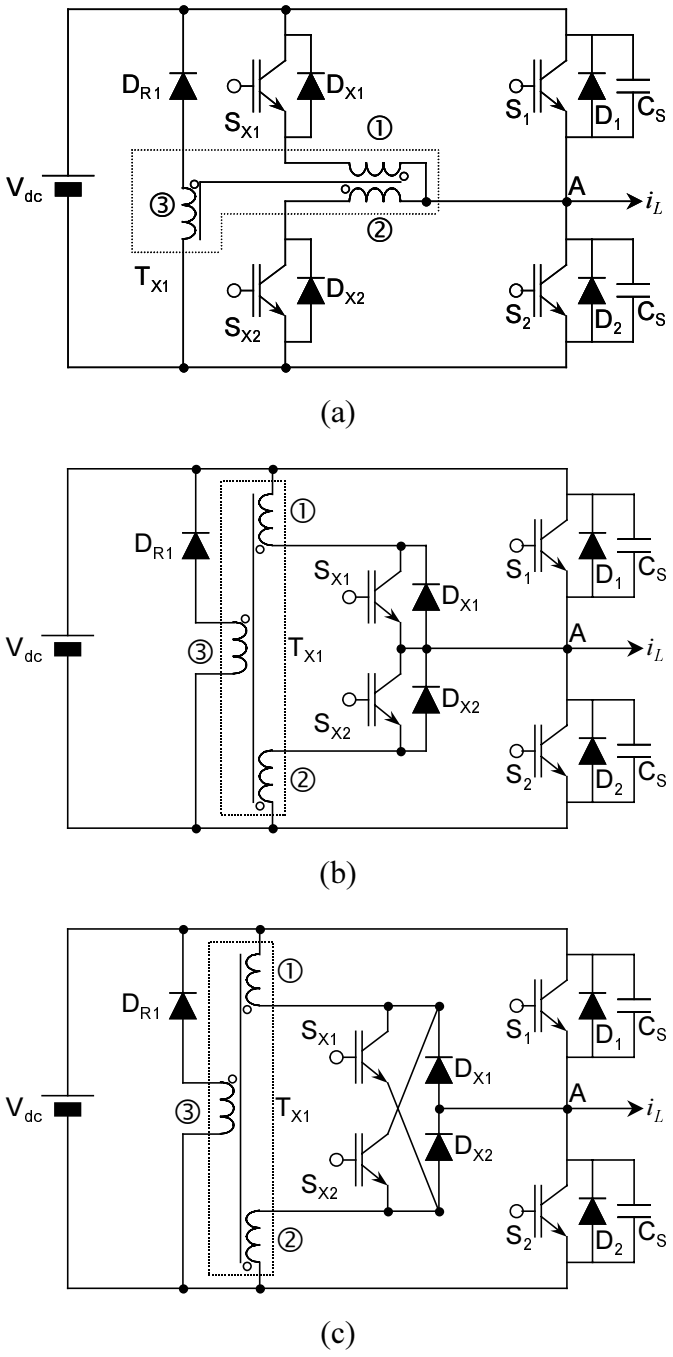


Figure 3.17 Modification procedures for IC ZVT cell:

(a) ZVT cell proposed in Figure 3.7 (c),

(b) Moving the location of S_{X1}, S_{X2}, D_{X1} and D_{X2}, and

(c) Exchanging the connection of S_{X1} and S_{X2}.

power stage shown in Figure 3.17 (b) is converted to the power stage shown in Figure 3.17 (c). This modified power stage offers insight for simplifying the auxiliary circuit. Two auxiliary switches (S_{X1} and S_{X2}) are connected in parallel, so that one auxiliary switch is sufficient for all of the zero-voltage operations, as shown in Figure 3.18. This section proposes the power stage shown in Figure 3.18 as a novel ZVT cell with simplified auxiliary circuit.

The auxiliary circuit of the proposed ZVT cell consists of one auxiliary switch, a coupled inductor with three windings, and three auxiliary diodes. The proposed ZVT cell is named the Single-Switch Single-Leg (S^3L) ZVT cell, because there is only one auxiliary switch per phase. Compared with the conventional ZVT cell shown in Figure 3.7 (a), the proposed cell saves one switch, one diode, and even one saturable inductor. By reducing one switch, this cell saves cost and space not only for the power semiconductor, but also for the corresponding gate drive circuit.

Figure 3.19 shows the power stage of a three-phase converter with the proposed S^3L ZVT cells. The auxiliary circuit consists of three switches, three coupled inductors, and seven diodes, so this circuit reduces three switches, five diodes, and three saturable inductors from the conventional three-phase ZVT converter with inductor feedback.

3.3.2 Operation Principles

A. Space Vector Modulation Scheme

In the proposed ZVT cell, the potential of node A automatically determines the direction of the auxiliary current when the auxiliary switch turns on. This means that S_{X1} turns on whenever any main switch needs auxiliary circuit operation for its zero-voltage commutation. By merging two auxiliary gate signals for the conventional ZVT cell, the auxiliary gate signal for the proposed ZVT cell can be easily generated. Therefore, the main switches of the proposed cell can use the gate signals of the conventional cell without any modification.

The proposed ZVT cell operates independently. Therefore, a three-phase S^3L ZVT converter is able to operate with the ML SVM scheme without any modifications. This characteristic allows the auxiliary circuit and its control circuit to be a piggyback type.

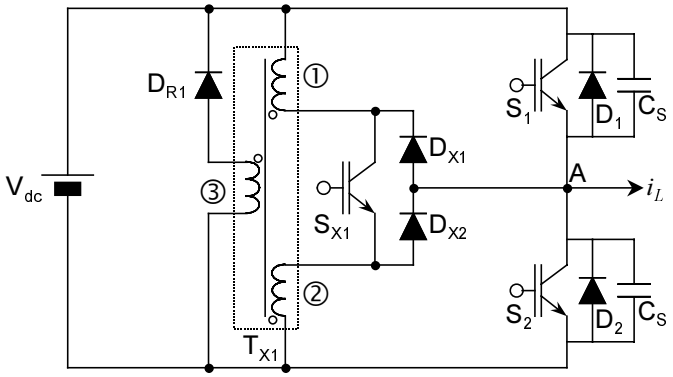


Figure 3.18 A novel ZVT cell with single switch.

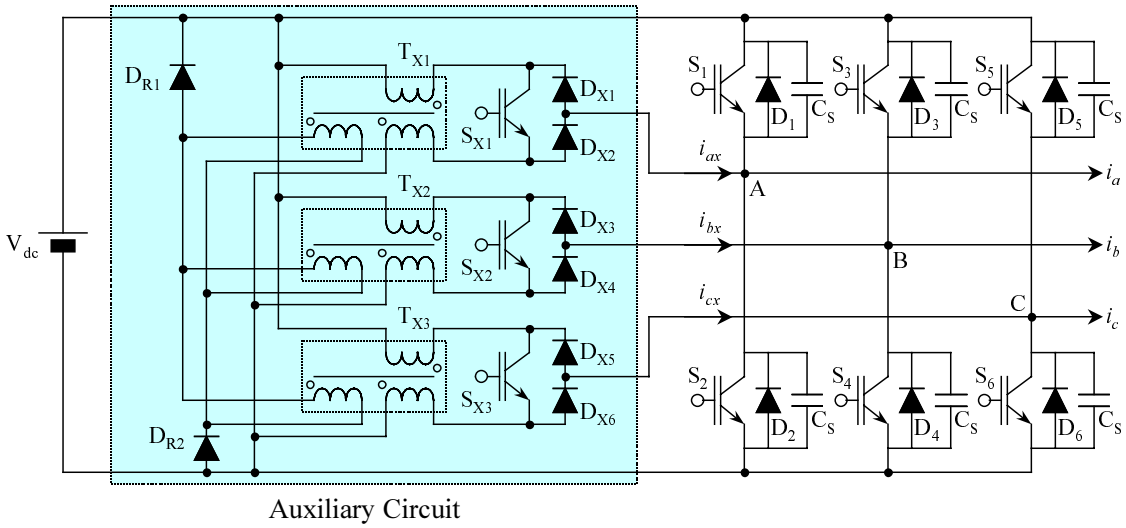


Figure 3.19 Three-phase S^3L ZVT converter with coupled inductors.

B. Zero-Voltage Turn-On Commutations

The auxiliary circuit should assist both cases of zero-voltage turn-on commutations: commutations from diodes to switch and from switch to diode with low load current. The auxiliary circuit of the proposed ZVT cell can provide its operations for both commutations. Figure 3.20 shows several waveforms of corresponding devices during the zero-voltage turn-on commutations for both cases. This figure shows the zero-voltage turn-on of main switches and the zero-current turn-off of auxiliary switches in both cases.

For one case of zero-voltage turn-on of the main switches, Figure 3.20 (a) shows the commutation waveforms when the load current i_L is positive. At this moment, the load current conduction is changed from a main diode D_2 to a main switch S_1 with the operation of an auxiliary switch S_{X1}. Figure 3.21 shows the detailed current conduction statuses of all commutation periods.

- *Before commutation* [before t_0] : Due to the load current direction, D_2 carries the load current. Therefore, the potential of node A is the same as that of the negative DC rail. Both D_{X1} and D_{X2} block the current path between the main bridge and the coupled inductor.

- *Charging period* [$t_0 \sim t_1$] : When S_{X1} turns on at t_0, the DC input voltage V_{dc} is applied to the leakage inductor L_{X1} in winding ① of the coupled inductor T_{X1} due to the potential of node A. This applied voltage generates an auxiliary switch current through S_{X1} and D_{X2}. This current i_{SX1} increases linearly and reaches half the load current i_a at t_1. Winding ② carries the same amount of current as i_{SX1} through D_{X2}. Due to these auxiliary currents, the main diode current i_{D2} decreases linearly and reaches zero at t_1. Therefore, the anti-parallel diode D_2 can turn off with a zero-current condition.

- *Boost period* [$t_1 \sim t_2$] : The boost current I_{boost} is required to compensate for loss factors during the resonant period. After i_{SX1} reaches half the load current i_a at t_1, both S_2 and S_{X1} remain in on-states in order to add the boost current I_{boost} to the auxiliary switch current. The auxiliary switch current i_{SX1} reaches the sum of I_{boost} and half the load current at t_2.

- *Resonant period* [$t_2 \sim t_3$] : When S_2 turns off at t_2, the leakage inductor L_{X1} of T_{X1} starts to resonate with the capacitors across both S_1 and S_2. This resonant operation charges the capacitor across S_2 and discharges the capacitor across S_1. When the voltage across the main switch S_1 reaches zero at t_3, this main switch turns on with a zero-voltage condition.

- *Discharging period* [$t_3 \sim t_4$] : Since S_1 turns on with a zero-voltage condition at t_3, node A remains connected to the positive DC rail. This potential applies V_{dc} to the winding ② and L_X as the reverse bias of the inductor current. Due to this reverse bias, i_{SX1} decreases and i_{S1} increases linearly. When i_{SX1} reaches the very small magnetizing current of T_{X1}, S_{X1} turns off with a quasi-zero-current condition at t_4. At the same time, S_1 carries all load current i_a.

- *Reset period* [$t_4 \sim t_5$] : When S_{X1} turns off with a quasi-zero-current condition at t_5, the coupled inductor T_{X1} carries the magnetizing energy. Diodes D_{X1} and D_{X2} block the magnetizing current paths through winding ① and ② of T_{X1}, respectively. Instead of those paths, winding ③ of T_{X1} provides the current paths through D_{R1}. When the magnetizing current flows through D_{R1}, V_{dc} is applied to winding ③ as reverse bias. Therefore, the magnetizing energy is totally reset at t_5.

- *After commutation* [$t_5 \sim$] : After the commutation is completed at t_5, the load current flows only through S_1, and there is no energy in the auxiliary circuit.

For another case of zero-voltage turn-on of the main switches, Figure 3.20 (b) shows the commutation waveforms when load current i_L is positive and small. At this moment, the load current conduction is changed from main switch S_1 to main diode D_2 with the operation of auxiliary switch S_{X1}. Because the load current is not sufficiently large to change the potentials of snubber capacitors within the designed commutation time, the auxiliary circuit operation provides more energy to accelerate the commutation.

- *Boost period* [$t_0 \sim t_1$] : When S_{X1} turns on at t_0, the DC input voltage V_{dc} is applied to the leakage inductor L_{X1} in winding ② of the coupled inductor T_{X1},

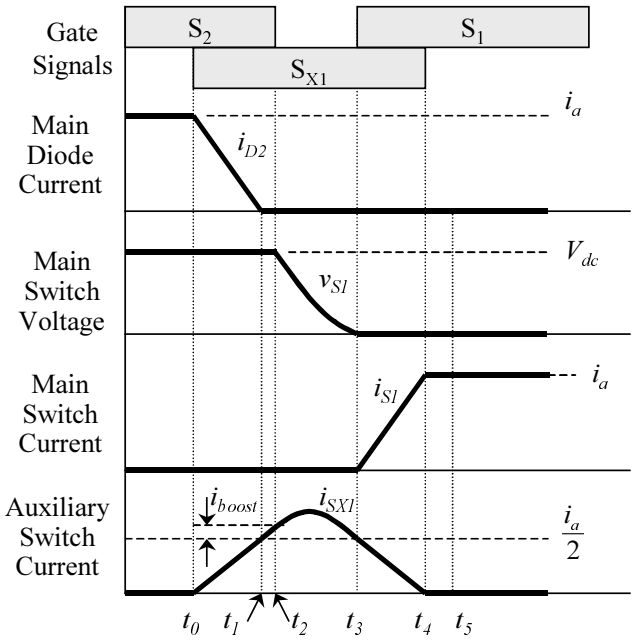
because the potential of node A is the same as that of the positive DC rail. This applied voltage generates an auxiliary switch current through S_{X1} and D_{X1}. This current i_{SX1} increases linearly and finally reaches the required boost current I_{boost} at t_1. Winding ① carries the same amount of current as i_{SX1} through D_{X1}. This auxiliary current is added to the load current in order to increase the main switch current.

- *Resonant period* [$t_1 \sim t_2$] : When S_1 turns off at t_1, the leakage inductor L_{X1} of T_{X1} starts to resonate with the capacitors across both S_1 and S_2. This resonant operation charges the capacitor across S_1 and discharges the capacitor across S_2. When the voltage across main switch S_2 reaches zero at t_2, this main switch turns on with a zero-voltage condition, and its anti-parallel diode starts to carry both the load current and the auxiliary current.

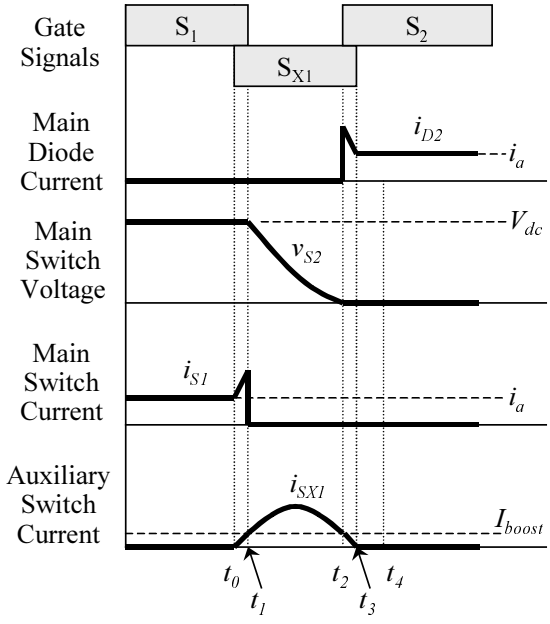
- *Discharging period* [$t_2 \sim t_3$] : Since S_2 turns on with a zero-voltage condition at t_2, node A remains connected to the negative DC rail. This potential applies V_{dc} to winding ① and L_{X1} as the reverse bias of the auxiliary inductor current. The auxiliary current i_{SX1} decreases linearly due to the reverse bias. When i_{SX1} reaches the very small magnetizing current of T_{X1}, S_{X1} turns off with a quasi-zero-current condition at t_3. At the same time, D_2 carries all load current i_a.

- *Reset period* [$t_3 \sim t_4$] : When S_{X1} turns off with a quasi-zero-current condition at t_3, the coupled inductor T_X carries the magnetizing energy. Diodes D_{X1} and D_{X2} block the magnetizing current paths through windings ① and ② of T_{X1}, respectively. Instead of those paths, winding ③ of T_{X1} provides the current path through D_{R1}. When the magnetizing current flows through D_{R1}, V_{dc} applies to winding ③ as the reverse bias. Therefore, this magnetizing energy is totally reset at t_4.

- *After commutation* [$t_4 \sim$] : After the commutation is completed at t_4, the load current flows only through D_2, and there is no energy in the auxiliary circuit.



(a)



(b)

Figure 3.20 Zero-voltage turn-on commutation waveforms:

(a) Commutation from diode to switch and

(b) Commutation from switch to diode with low load current.

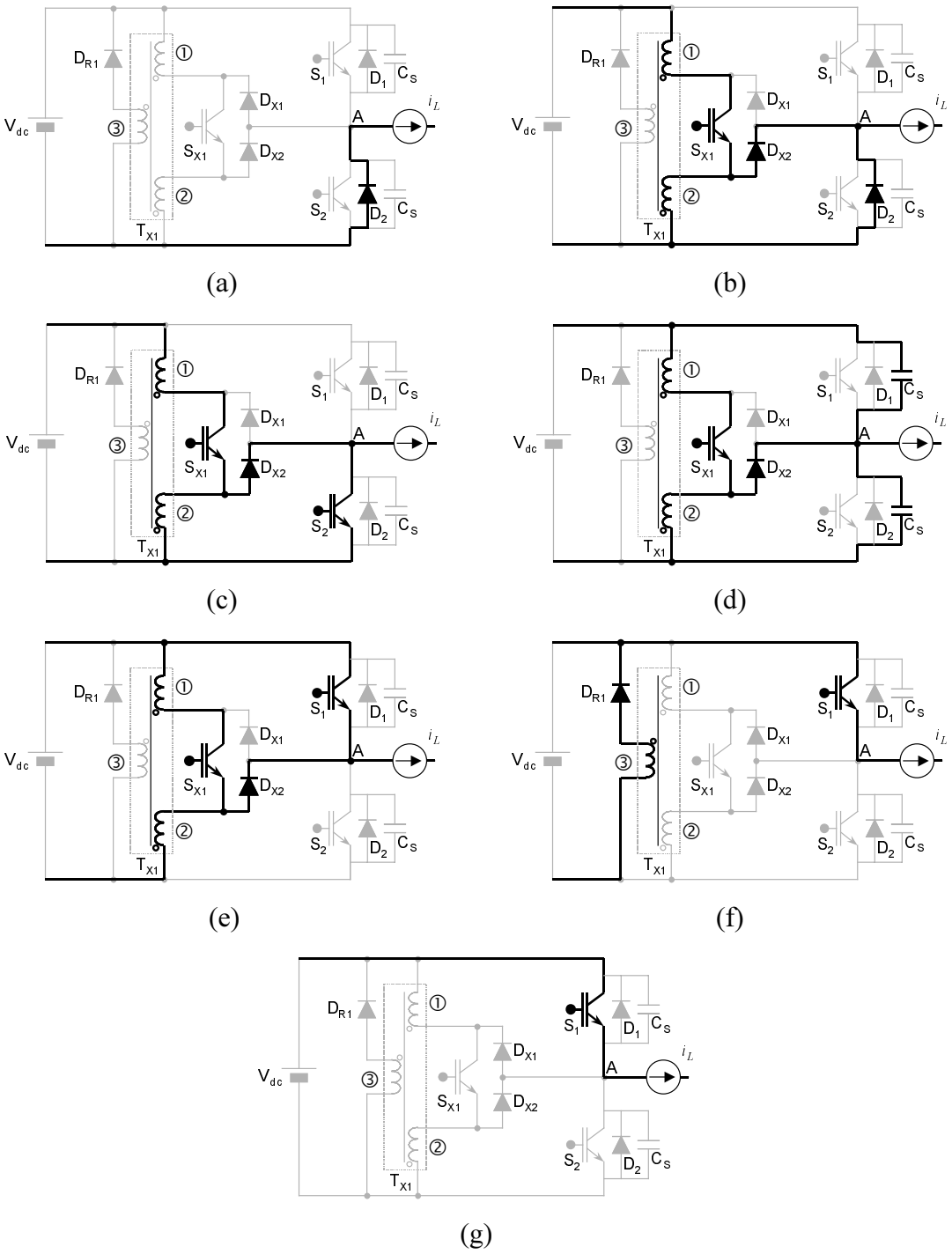


Figure 3.21 Commutation description of sequential periods from diode to switch: (a) Before commutation, (b) Charging period, (c) Boost period, (d) Resonant period, (e) Discharging period, (f) Reset period, and (g) After commutation.

3.3.3 Timing Control and Design Issues

The operation principles of the proposed ZVT cell are the same as those of the conventional ZVT cell, even though only one auxiliary switch provides zero-voltage conditions for both main switches. Therefore, the charging time, boost time, resonant time, and discharging time are the same as those give by Equations (3.1)–(3.4). The reset time can be calculated using Equation (3.7). This section explains two issues related to timing control and real implementation that do not occur in the conventional cell.

A. Auxiliary Switch Turn-off Time Control

If the auxiliary switch turns off at the exact time at which the auxiliary switch current reaches zero, then there is no problem. In the case of commutation from D_2 to S_1, if auxiliary switch S_{X1} maintains the conduction state after its current reaches zero, then the potential of node A generates auxiliary current through D_{X1} and S_{X1}. In order to prevent this current, S_{X1} should turn off as soon as the switch current reaches zero. Even if the variable timing control method provides accurate timings using load current information, there are the other unpredictable factors and time delays that determine real gating times. Therefore, this kind of timing control is practically impossible.

Originally, the variable timing control method makes the actual pulse widths of the auxiliary gate signals a little longer than the theoretical pulse widths, in order to guarantee the zero-current turn-off of the auxiliary switches. A small saturable inductor can hold V_{dc}, while blocking the reverse current path from the actual zero-current point untill turn-off time. The saturable inductor is located between the auxiliary circuit and the main bridge, as shown in Figure 3.22 (a). While the saturable inductor used in the conventional ZVT cell should block the current path during the entire reset time (almost the same as the sum of the resonant time and the discharging time), the saturable inductor of the proposed ZVT cell blocks the current path for just a short time. Therefore, this inductor is much smaller than the one used in the conventional ZVT cell.

The design sequence of the saturable inductor is similar to that for the conventional ZVT cell. If the values of control timing table are the sum of the theoretically calculated pulse width and the maximum tolerance ΔT to, the tolerance becomes the longest time in which saturable inductor blocks the reverse current. Because DC input voltage applies to

the saturable inductor during ΔT, the blocking capability of the saturable inductor should be equal to or larger than the product of V_{dc} and ΔT, as shown in Equation (3.9):

$$V \cdot \sec = V_{dc} \cdot \Delta T \tag{3.9}$$

This blocking capability determines all design factors of the saturable inductor. The METGLAS is preferred as the core material of the saturable inductor. Both the cross-section area of the core (A_C) and the number of turns (N_L) are designed using Equation (3.10). This saturable inductor should be design-optimized for minimizing its loss, space, and cost.

$$V \cdot \sec = N_L \cdot A_C \cdot \Delta B \tag{3.10}$$

where ΔB : Maximum variation of flux density

B. Snubber Circuit for Auxiliary Switch

The magnetizing current starts to increase at the beginning of the resonant period. In general, this current is less than 100 mA at the end of the discharging period. In the case of a commutation from D_2 to S_1, the auxiliary switch S_{X1} still carries some current, even if the resonant inductor current drops to zero at the end of the discharging period. This current is half the magnetizing current that passes through winding ①, S_{X1}, and winding ②. In order to allow a path for this current after S_{X1} turns off, a capacitor and a resistor are connected in parallel with the auxiliary switch, as shown in Figure 3.22 (b). Because this current is very small, the capacitance and resistance are also small.

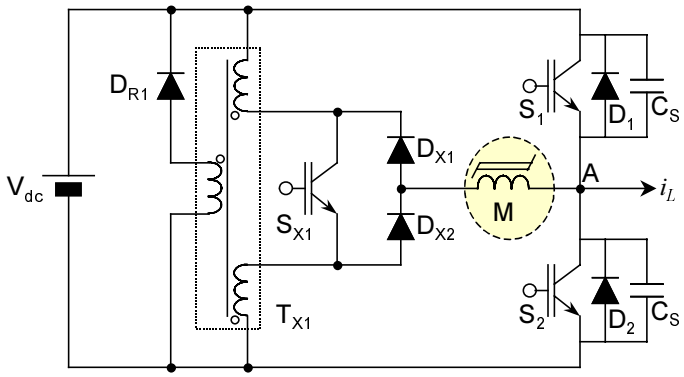
Figure 3.22 (c) shows a practical design of the proposed S^3L ZVT cell. Three components have been added to the originally proposed ZVT cell. However, the sizes of these components are small, so their inclusion is acceptable.

3.3.4 Simulation and Loss Discussion

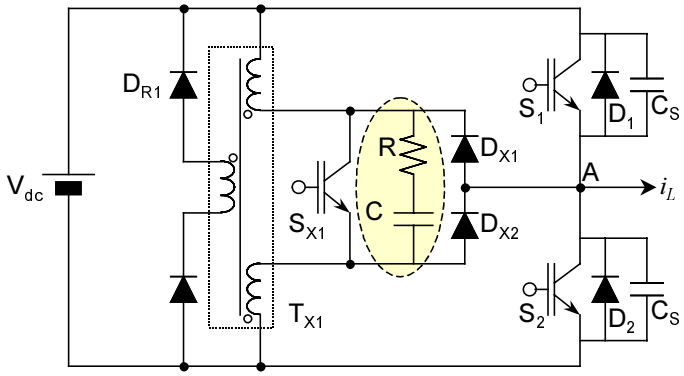
A. Simulation

Figure 3.23 shows the simulation circuit and several current definitions. The designed values of the resonant components in the proposed ZVT inverter are as follows:

C_S = 0.1 μF, L_X = 4 μH, I_{boost} = 10 A, and V_{DC} = 300 V.



(a)



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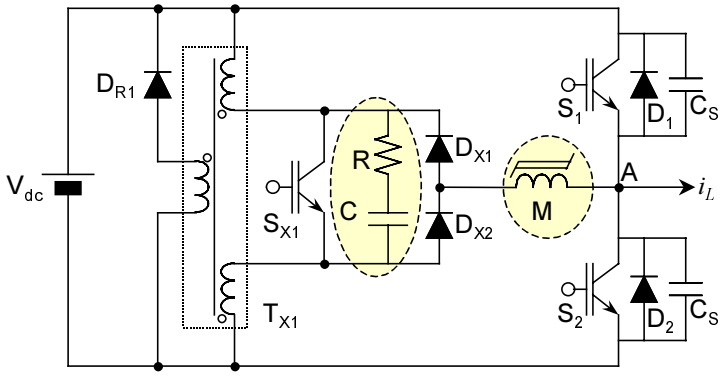


(c)

Figure 3.22 Practical design of the proposed ZVT cell:

(a) Connection of a saturable inductor,

(b) Connection of a R-C snubber circuit, and

(c) Overall power stage of the proposed ZVT cell.

The snubber circuit values are as follows: C = 100 pF and R = 500 Ω.

Figure 3.24 shows the simulation results of the zero-voltage turn-on commutation from D_2 to S_1 when i_a = 200A. The turn-on of S_{X1} starts to increase i_{SX1} and to decrease i_{D2} at t_0. The resonant operation begins at t_2, and the main switch S_1 turns on with a zero-voltage condition at t_3. The auxiliary switch S_{X1} turns off with a zero-current condition at t_4. These waveforms verify that the proposed inverter accomplishes the expected operations of zero-voltage turn-on commutation.

Figure 3.25 (a) shows detailed simulation waveforms in the reset period. Although the resonant inductor current drops to zero at t_3', both windings ① and ② have some current that is half the magnetizing current. When S_{X1} turns off at t_4, the currents of windings ① and ② ($i_{①}$ and $i_{②}$) start to decrease, and the current of winding ③ starts to increase. Finally, both $i_{①}$ and $i_{②}$ become zero, and only winding ③ carries the current.

Figure 3.25 (b) shows the reset time and the auxiliary switch voltage. Due to the turns-ratio of the reset winding, the reset time is almost ten times that of the existing ZVT cell. This value is acceptable in inverters with 10-20 kHz switching frequencies, because it is much shorter than one switching cycle. During the reset period, the auxiliary switch voltage v_{SX1} stays at 360 V, because the DC input voltage V_{dc} applied to winding ③ is reflected to both windings ① and ②.

B. Loss Discussion

Because all commutation patterns of the proposed ZVT cell are the same as those of the existing ZVT cell, both the main switch switching losses and the auxiliary circuit losses are almost the same as those of the existing ZVT cell. In the existing ZVT cell, half the load current passes through an auxiliary switch and the other half passes through an auxiliary diode. However, one of the auxiliary diodes carries the entire load current in the proposed ZVT cell. This difference causes a slight increase in the conduction losses of the auxiliary circuit.

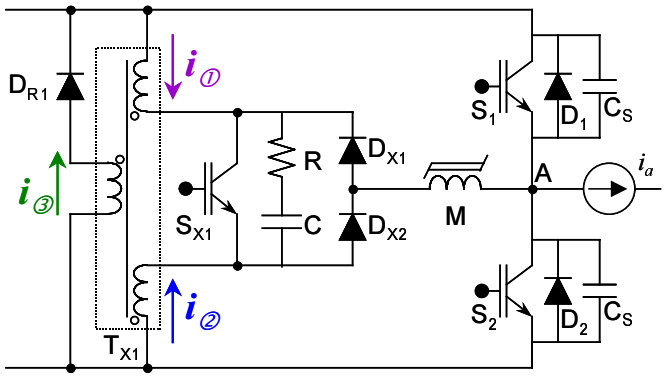


Figure 3.23 Simulation circuit and current definitions.

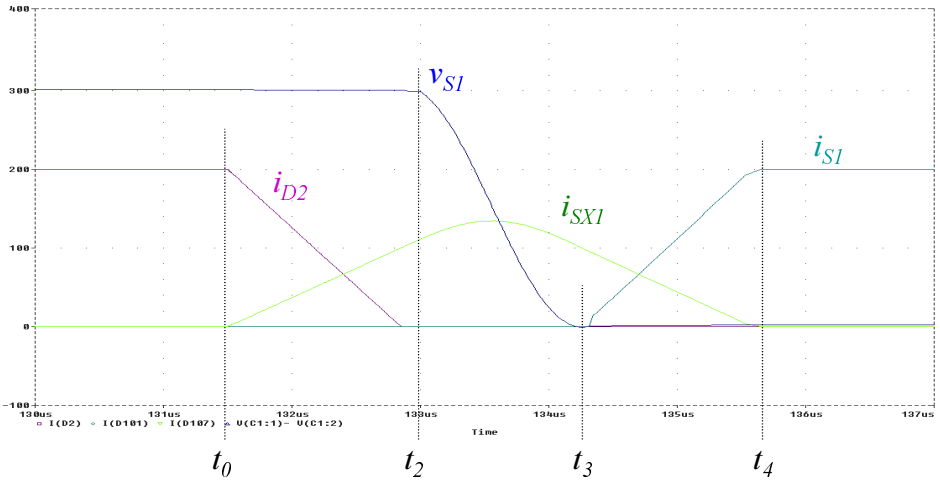
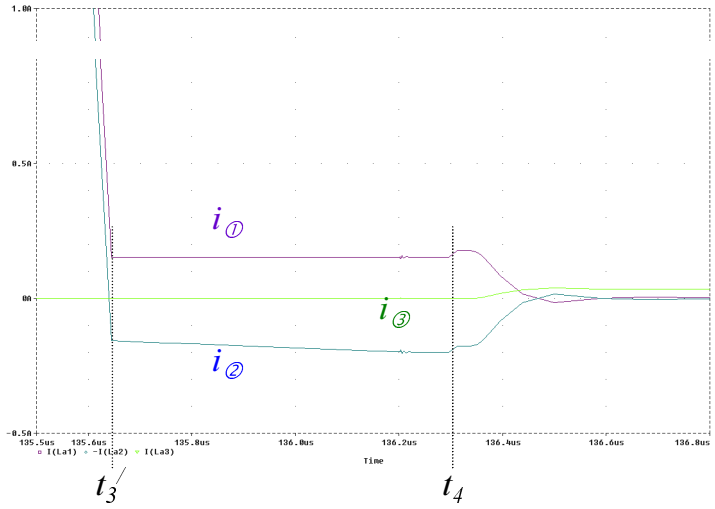
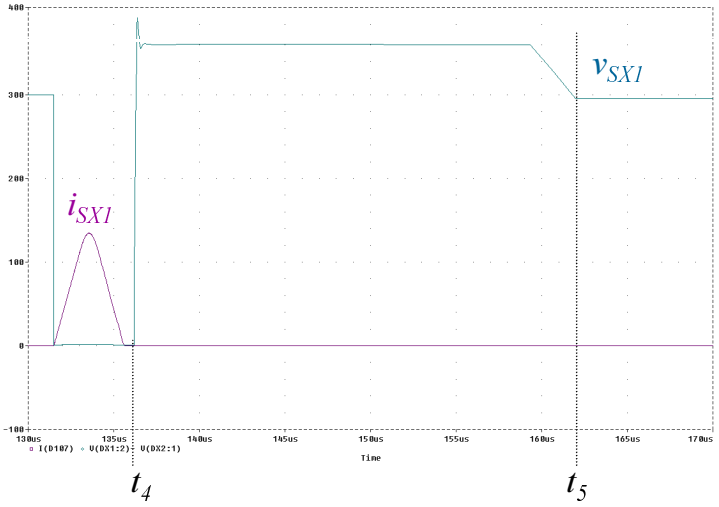


Figure 3.24 Simulation result of zero-voltage commutation from diode to switch.



(a)



(b)

Figure 3.25 Simulation results for showing the reset operation:

(a) Current of each winding just before reset period, and

(b) Voltage across auxiliary switch.

3.3.5 Experimental Results

The designed values of the resonant components for the experiments are as follows: C_S = 2×0.068 μF, L_X = 2.5 μH, and V_{DC} = 150 V. The resistance and capacitance of the RC snubber circuit are the same as those of simulation, as follows: C = 100 pF and R = 500 Ω.

Figure 3.26 shows the experimental results of a zero-voltage turn-on commutation from D_2 to S_1 when i_a = 45 A. This commutation takes about 3.2 μsec, and the resonant current (including the boost current) is approximately 20 A. Two waveforms, $v_{g(S1)}$ and v_{S1}, clearly show the expected zero-voltage turn-on commutation at t_3. The auxiliary switch current i_{SX1} becomes zero at t_4, so it turns off with zero-current condition.

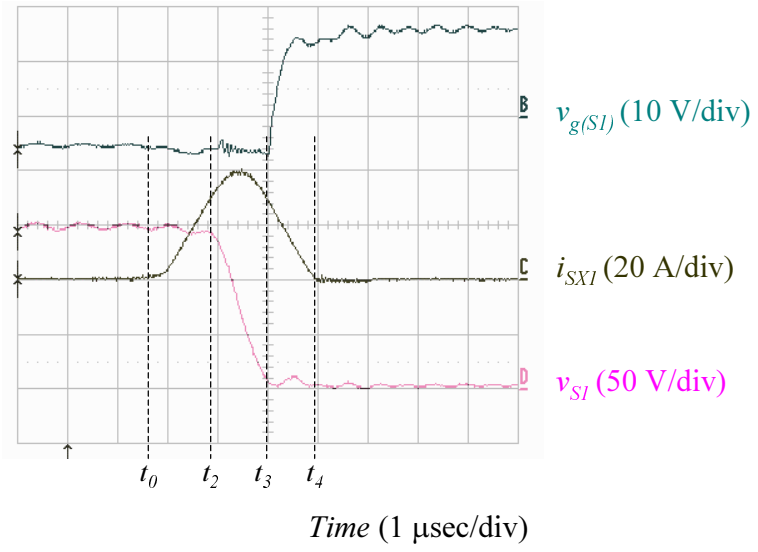


Figure 3.26 Experimental waveforms.

3.4 SUMMARY

Section 3.1 investigated conventional inductor-coupled ZVT converters. Although the ZVT converters achieve the desired zero-voltage commutations, they have inherent problems due to the freewheeling and residual magnetizing currents. The freewheeling current causes not only additional losses in the auxiliary circuit, but also high-frequency harmonics when the auxiliary switch turns on. If the magnetizing current is not reset and is accumulated through several switching cycles, the built-up magnetizing current induces inverter malfunctions.

In order to solve the problems related to the circulating currents, Section 3.2 proposed a novel inductor-coupled ZVT cell. The proposed ZVT cell prohibits the freewheeling current from passing the auxiliary circuit, so the losses and harmonics are eliminated. The coupled inductor of the proposed ZVT cell has a reset winding that provides a path for the residual magnetizing current of the coupled inductor. Therefore, the magnetizing current can be reset without requiring a saturable inductor, which reduces both losses and cost. In consequence, a three-phase converter using the proposed ZVT cells can achieve better performance than not only a hard-switching converter but also the conventional inductor-coupled ZVT converters.

The ZVT cell proposed in Section 3.2 offered insight into ways to simplify its auxiliary circuit. Section 3.3 proposed a novel inductor-coupled ZVT cell with simplified auxiliary circuit, which can comply with the demands to reduce the cost and space of the auxiliary circuits. The auxiliary circuit of the proposed S^3L ZVT cell has only one auxiliary switch. A three-phase converter with the proposed ZVT cell saves not only three auxiliary switches but also four auxiliary diodes.

Chapter 4. INDUCTOR-COUPLED ZERO-VOLTAGE-TRANSITION CONVERTERS WITH PHASE-LOCK CONCEPT

Chapter 3 proposed a novel IC ZVT cell with single auxiliary switch. Since the novel cell uses one auxiliary switch in each main half bridge, the total number of auxiliary switches in a multi-phase converter is the same as the number of phases. This simplification reduces the number of auxiliary switches to half that of the conventional ZVT converters.

There might be another way to reduce the number of auxiliary switches in conventional ZVT converters. This chapter investigates the use of one auxiliary switch to provide zero-voltage condition for all the top main switches, while another auxiliary switch does so for all the bottom main switches. As the result of the investigation, this chapter proposes the Phase-Lock (PL) concept to simplify the auxiliary circuit. The PL concept is realized using either saturable inductors or thyristors.

4.1 REDUCING THE NUMBER OF AUXILIARY SWITCHES

The novel ZVT cell proposed in Section 3.3 uses only one auxiliary switch. This simplification is made possible by combining common characteristics of the top and bottom main switches.

In general, most of ZVT converters have multi-phase structures. Therefore, there are more than two auxiliary switches on both the top and bottom sides. This section investigates the common characteristics of either the top or bottom switches. This investigation determines whether or not two auxiliary switches can provide zero-voltage conditions for any commutation of all main switches. Eventually, this section explains the limits to this simplification.

4.1.1 ZVT Cells

Figure 4.1 shows a ZVT cell of the ZVT converter with inductor feedback. In order to reveal the common characteristics, this section reviews the operation of zero-voltage commutation and defines the concepts of top and bottom ZVT cells.

The leakage inductance of T_X, L_X is used as the resonant inductance for zero-voltage commutation. When the load current i_L flows through D_2, S_1 requires auxiliary circuit operation for its zero-voltage turn-on commutation. In this case, only S_{X1} can generate the resonant inductor current through L_X, because the potential of point A is the same as that of the negative DC rail. In other words, only an auxiliary switch S_{X1} and a diode D_{X3} assist zero-voltage turn-on commutation of the top main switch S_1. This operation principle defines a top ZVT cell that consists of a main switch S_1, an auxiliary switch S_{X1}, and three diodes D_2, D_{X2} and D_{X3}, as shown in Figure 4.2 (a).

In the same manner, only S_{X2} and D_{X1} provide the zero-voltage condition for the bottom main switch S_2 when the load current i_L flows through D_1. This operation principle defines a bottom ZVT cell that consists of a main switch S_2, an auxiliary switch S_{X2}, and three diodes D_1, D_{X1} and D_{X4}, as shown in Figure 4.2 (b).

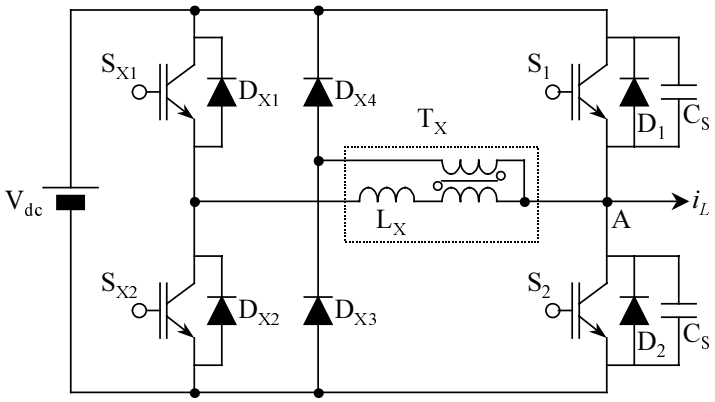
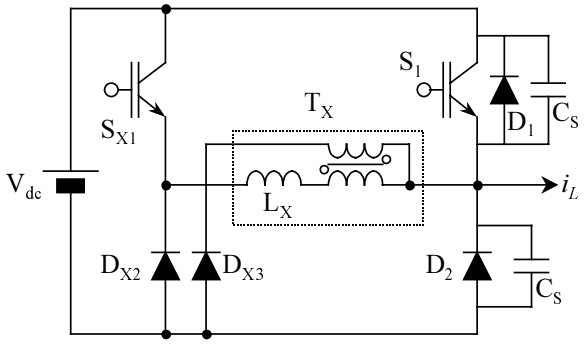
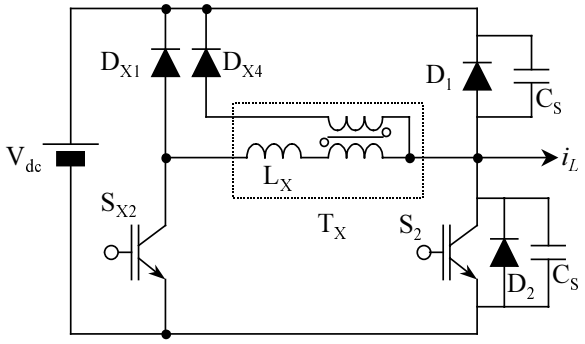


Figure 4.1 A ZVT cell of the ZVT converter with inductor feedback.



(a)



(b)

Figure 4.2 Separated ZVT cells:

(a) Top ZVT cell and (b) Bottom ZVT cell.

4.1.2 Investigation of Possibility for Switch-Number Reduction

Since the three-phase ZVT converters are so widely used, it is the example discussed throughout this chapter.

Any ZVT cell can be decomposed into either its top or bottom ZVT cell, as explained in Section 4.1.1. The auxiliary switch of a top ZVT cell provides the zero-voltage condition for the corresponding top main switch when the load current flows through the bottom anti-parallel diodes. Commutation sequences for all the top ZVT cells are identical. Therefore, one auxiliary switch seems to provide the zero-voltage conditions for all the top main switches with the help of three rectifying diodes in block D_B, as shown in Figure 4.3. In the same manner, another auxiliary switch seems to provide the required operations for all the bottom main switches with the help of three other rectifying diodes. By combining the simplified top and bottom ZVT cells, the conventional three-phase ZVT converter is simplified into a power stage with only two auxiliary switches, as shown in Figure 4.4.

However, due to interference among the phases, none of the phases can provide the zero-voltage condition for its commutations. The interference prevents the resonance of the auxiliary inductor and snubber capacitors. For example, assume that phase B needs a commutation from D_3 to S_4 with $i_b < 0$, while S_1 and S_5 stay in on-states with $i_a > 0$ and $i_c < 0$. This commutation requires the operation of the auxiliary circuit in order to provide the zero-voltage condition for S_4. When S_{X2} turns on, the load current of phase B starts to change its path from D_3 to S_{X2}. However, the resonant inductor L_{X2} cannot resonate with C_S across S_3 and S_4, even if the charging and boost periods are completed. The main reason is the potentials of nodes A and C: They are still the same as that of the positive DC rail, and they further increase the auxiliary inductor current. As in this example, the interference among phases is serious enough to render zero-voltage turn-on commutation impossible.

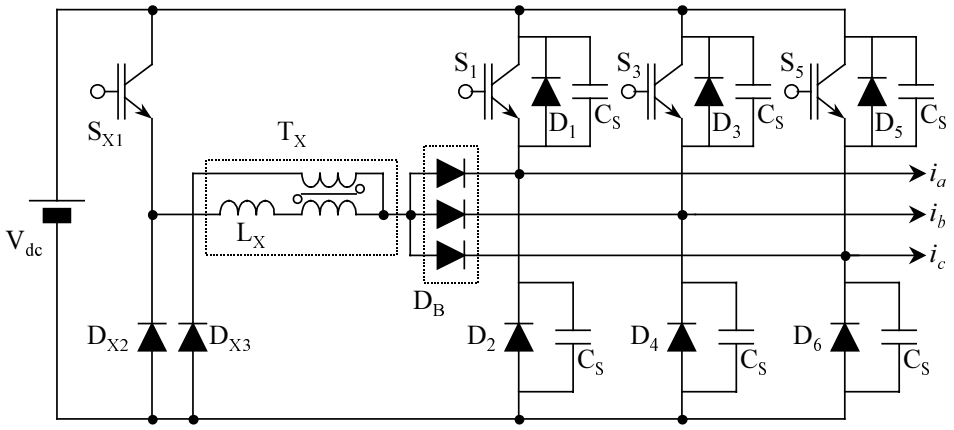


Figure 4.3 Top ZVT cells with one auxiliary switch.

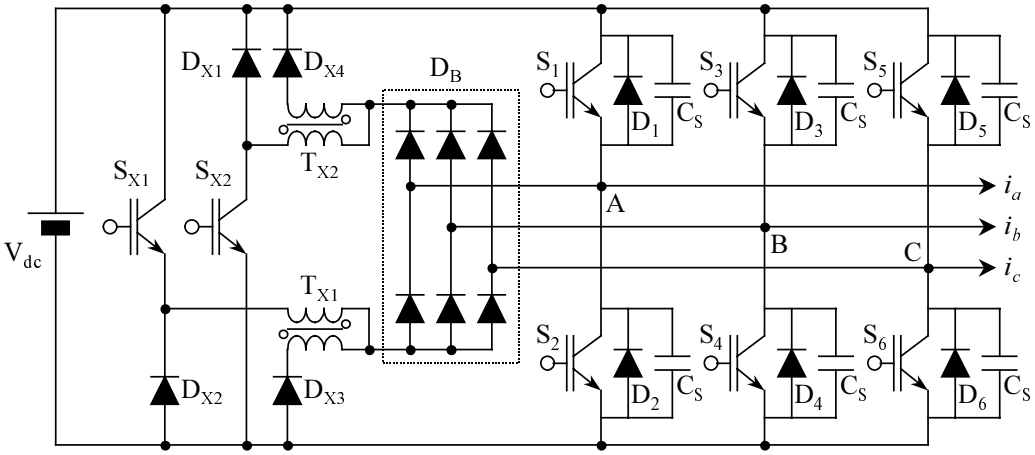


Figure 4.4 ZVT three-phase converter with two auxiliary switches.

4.2 PHASE-LOCK CIRCUIT

In order to achieve the complete zero-voltage turn-on commutation in the power stage shown in Figure 4.4, the interference among phases must be prevented. This section shows how to prevent interference and how to realize the concept [C27, C30, C32].

4.2.1 Phase-Lock Concept

The main reason for the interference is that the rectifying diodes in block D_B cannot control the connection between the auxiliary circuit and the main bridges. Therefore, a function block is necessary in order to control the connection between the auxiliary circuit and the main bridges, as shown in Figure 4.5. This function block should control the connection based on the next switching status of each phase. For example, if S_4 requires the operation of S_{X2} for its zero-voltage turn-on commutation, the function block connects the auxiliary circuit only to node B during the entire commutation period. Because this block locks or unlocks each phase to the auxiliary circuit, it is named the Phase-Lock (PL) circuit. This concept allows only two auxiliary switches to provide zero-voltage conditions for all the main switches.

4.2.2 Realization of the Phase-Lock Concept

Operation of the PL circuit is required only during the commutation period. During the main switch conduction period, the status of the PL circuit has no effect on the converter because both S_{X1} and S_{X2} are in off-states. Since the resonant inductor current flows in one direction during the commutation period in any ZVT converter, the PL circuit needs only single-direction connections. Figure 4.6 shows the functional description of the PL circuit with six single-directional switches (P_1~P_6). For example, P_1 is closed in order to connect phase B to the auxiliary circuit during the zero-voltage turn-on commutation of S_1.

Several devices satisfy this functional requirement. Among them, a saturable inductor is one of the strongest candidates because it is already used in the conventional ZVT converter with inductor feedback for reset operation. Figure 4.7 shows the B-H curve of a

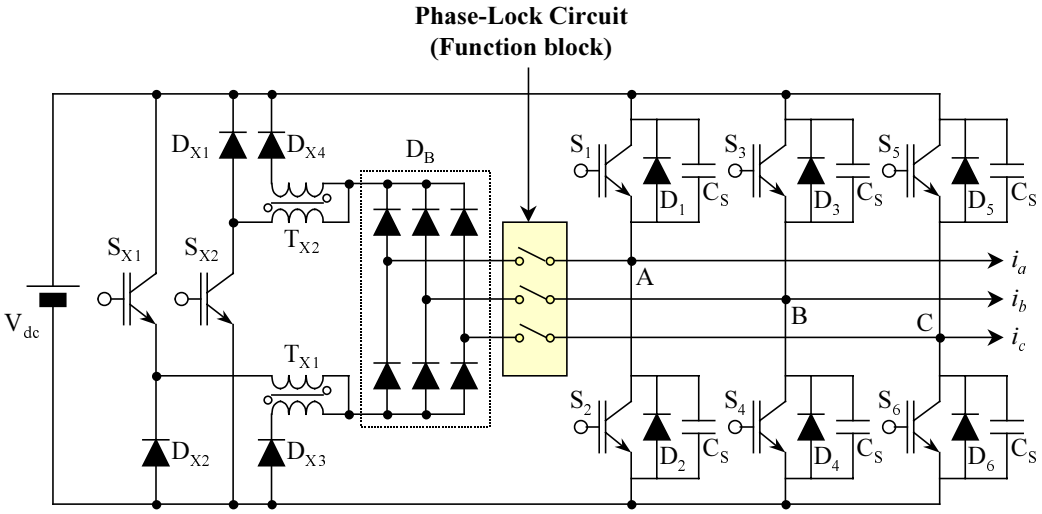


Figure 4.5 Power stage of ZVT converter with phase-lock circuit.

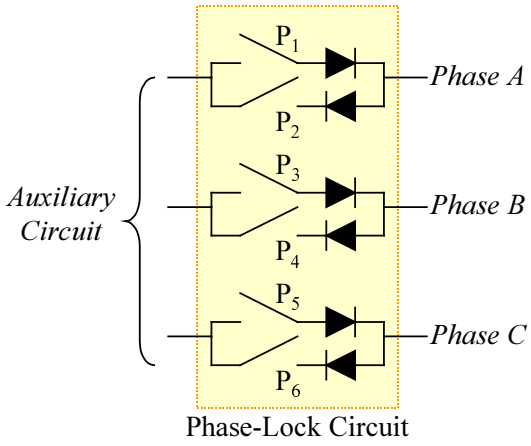


Figure 4.6 Functional description of the Phase-Lock circuit.

saturable inductor. If the initial flux density of the saturable inductor is B_1, the flux density moves to B_2 by applied positive bias voltage. During this period, the saturable inductor can limit the positive current flow to a very low value. This current-blocking characteristic allows the saturable inductors to be used as switches in the PL circuit. The required voltage-second (*V-sec*) value for zero-voltage commutation determines the design factors of the saturable inductors.

Since the initial flux densities of the saturable inductors depend on the previous switching status, they are uncertain. Therefore, a flux density controller is necessary for each saturable inductor to have proper blocking capability in any situation. This controller saturates the flux densities of the saturable inductors to the desired polarities by supplying the bias voltages before an auxiliary switch turns on. Figure 4.8 shows the realized PL circuit with the controlled saturable inductors and their flux density controllers for a ZVT three-phase converter. As shown in Figure 4.8, the flux density controller operates based on the signals from the main controller. For example, if S_4 requires the operation of S_{X2} for its zero-voltage turn-on commutation in Figure 4.5, the flux density controller saturates M_2 to connect node B to the auxiliary circuit before S_{X2} turns on, while saturating M_1 and M_3 to the opposite direction. Thus, only phase B is connected to the auxiliary circuit. This operation requires one additional period to control the saturable inductors just before the charging period of zero-voltage commutation.

4.2.3 Design of the Phase-Lock Circuit with Saturable Inductor

Figure 4.9 shows a design example of a controlled saturable inductor and its flux density controller. The required *V-sec* value to block the current path determines the inductor design factors, such as the cross-section area of the square-loop core and the number of turns for load-side winding. The flux density controller supplies the bias voltage that both saturates the inductor and limits the bias current. The controller should supply the highest possible bias voltage in order to have a short transition time of flux density. In general, the main control power supply provides the bias voltage to the flux density controller. Therefore, in order to match the low bias voltage, the number of turns for the control-side winding is one.

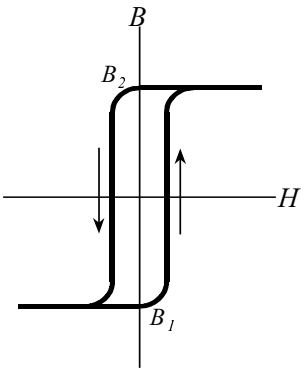


Figure 4.7 B-H characteristic curve of a saturable inductor.

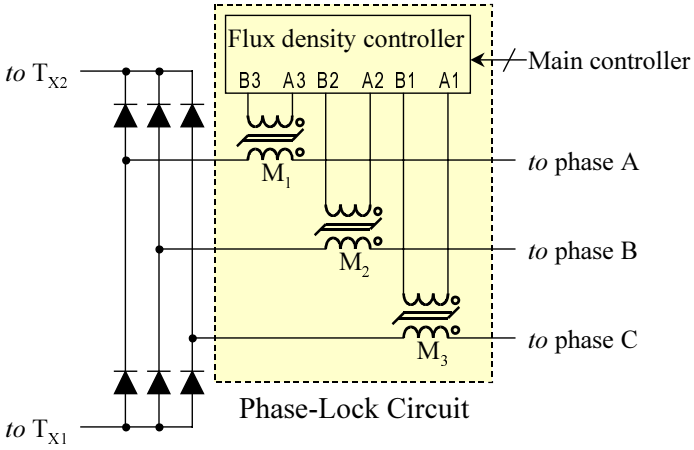


Figure 4.8 Phase-Lock circuit implemented with controlled saturable inductors.

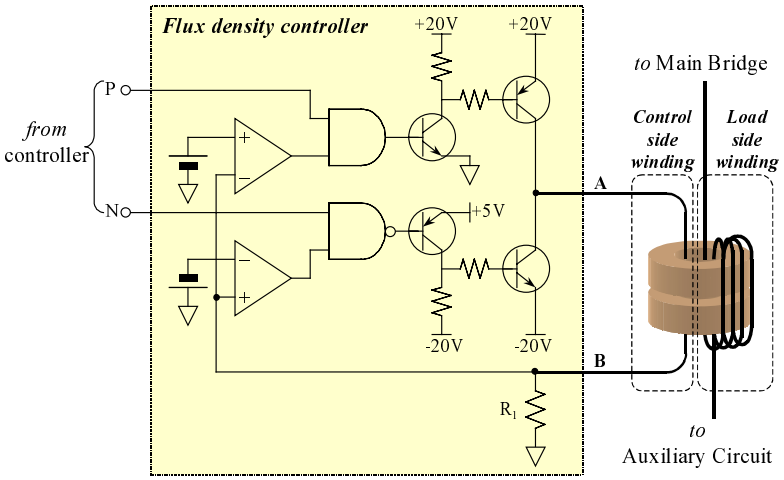


Figure 4.9 Design example of a controlled saturable inductor and its flux controller.

4.3 SIMPLIFIED ZVT CONVERTERS WITH PHASE-LOCK CIRCUIT

Section 4.2 introduced the PL concept based on the ZVT converter with inductor feedback. This section discusses the simplified auxiliary power circuit using the PL circuit, and analyzes the PL ZVT converter with inductor feedback as an example of the simplified ZVT converter.

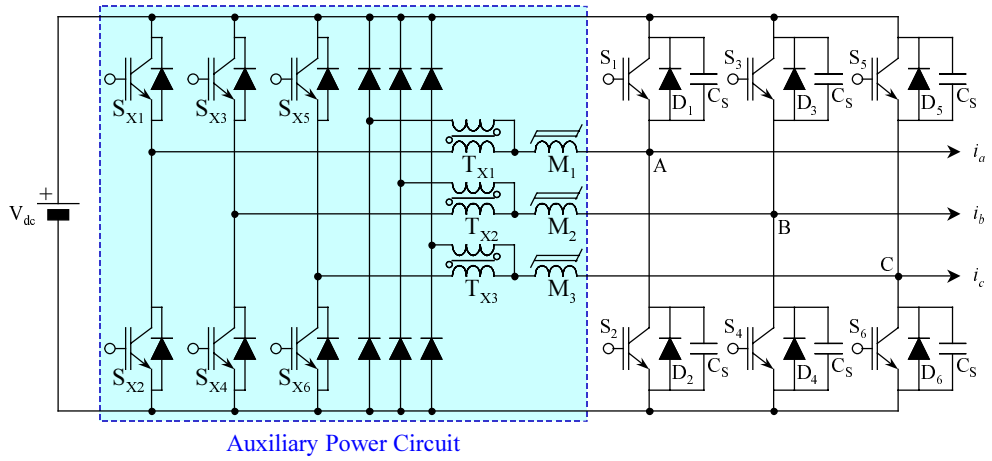
4.3.1 Power Stage

Figure 4.10 (b) shows the power stage of the three-phase PL ZVT converter with inductor feedback. The auxiliary circuit of this power stage mainly consists of two auxiliary switches and two coupled inductors, which allows the new auxiliary circuit to have lower cost and smaller space requirements than the conventional power stage shown in Figure 4.10 (a). Even if the PL circuit is added, the saturable inductors are already used in order to reset the magnetizing current of conventional ZVT converter. Therefore, the only additional part is the flux density controller, which is similar to the gate drivers of power devices.

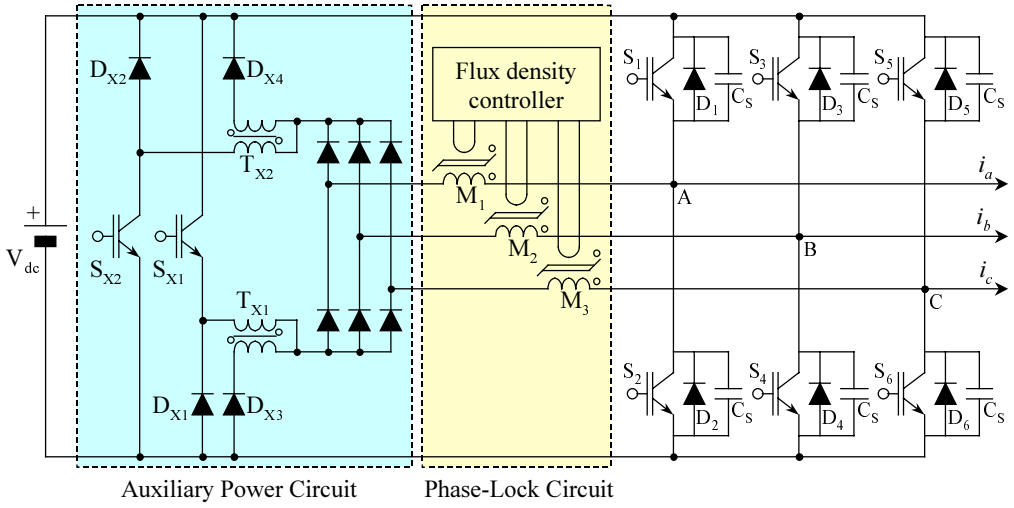
4.3.2 Operation Principles

A. Limitation of Phase-Lock Circuit Operation

The ideal PL circuit should control the connection between the phases and the auxiliary circuit for any switching pattern. However, the auxiliary power circuit (shown in Figure 4.10 (b)) limits the PL circuit operation. Figure 4.11 shows the simulation results verifying the PL circuit operation with the power stage shown in Figure 4.10 (b). This simulation is based on the positive current of phase A. Waveforms in the top block are the gate signal of S_1 and the applied voltage to the control-side winding of M_1. The lower block waveform is the voltage across the load-side winding of M_1. When S_1 carries the load current, the control-side bias voltages are exactly reflected to the load-side winding, as indicated with circle ①. Therefore, the flux controller can saturate M_1 at any polarity. The flux controller can saturate M_1 at a negative polarity to block the current path from node A to the auxiliary circuit even if D_2 carries the load current, as indicated



(a)



(b)

Figure 4.10 Three-phase ZVT converters with inductor feedback.

(a) Conventional power stage and

(b) Simplified power stage using the PL circuit.

with circle ②. However, when D_2 carries the load current, the positive bias voltage at the control-side winding does not affect the load-side winding, as indicated with circle ③. Therefore, the flux controller cannot saturate M_1 at a positive polarity, even if this saturation is required to block the current path from the auxiliary circuit to node A. The reason for this inability is clear: When D_2 carries the load current, D_{X1} and D_{X3} also carry a small amount of current through M_1, as shown in Figure 4.12. These current paths make the voltage across the load-side winding of M_1 almost zero. This voltage is reflected to the control-side mutual inductance of M_1, so the leakage inductance holds all the bias voltage.

B. Modified Space Vector Modulation Scheme

To overcome the limitation of the PL circuit operation, it is necessary to modify the switching pattern. If the same-side anti-parallel diodes of two phases carry their load currents, turn-on commutations to switches should be synchronized. The auxiliary circuit can provide zero-voltage conditions for both switches with the help of the PL switches. If not synchronized, the PL circuit cannot properly block the current path. Other situations do not require any synchronization. For example, assume both V_{ref} and I_{Load} are in either sector I or sector II, as shown in Figure 4.13 (a). During V_7 (*ppp*) status, the top anti-parallel diodes of both phases B and C carry their load currents. In order to synchronize the zero-voltage turn-on commutations of those phases, V_1 (*pnn*) should be the next switching status. The switching-state-vector (SSV) sequence finally becomes V_7 (*ppp*) ⇨ V_1 (*pnn*) ⇨ V_2 (*ppn*) in one switching cycle, according to the sequence shown in Figure 4.13 (b). This SSV sequence causes the switching patterns of three phases, as shown in Figure 4.14 (b). Even if these patterns are different from those of the ML SVM scheme shown in Figure 4.14 (a), the modified SVM scheme has the same number of commutations.

Since I_{Load} can be in any sector with a phase difference θ, the converter operation needs a generalized guide of SSV sequences. In order to reduce the switching losses, the selection of zero SSV is the same as in Table 4.1. There are 36 different SSV sequences according to the locations of both V_{ref} and I_{Load}. They can be grouped into three cases, as follows.

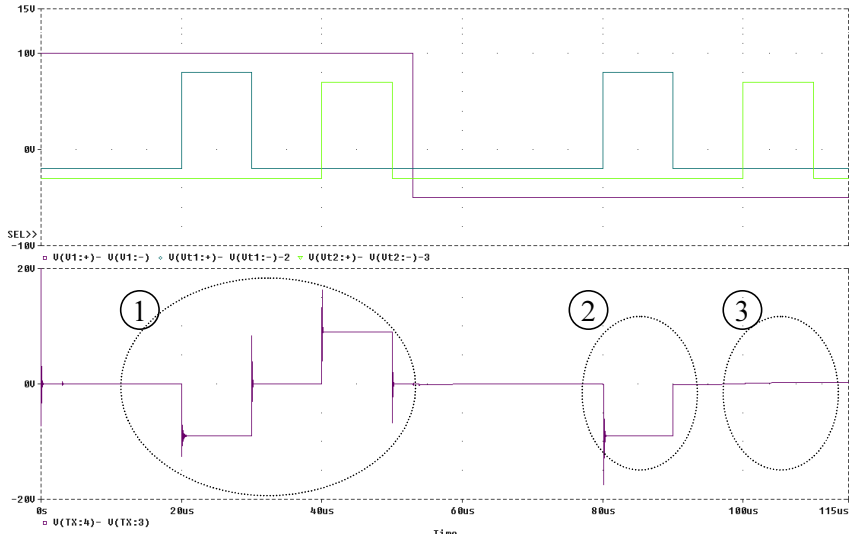


Figure 4.11 Simulation results of the flux density controller.

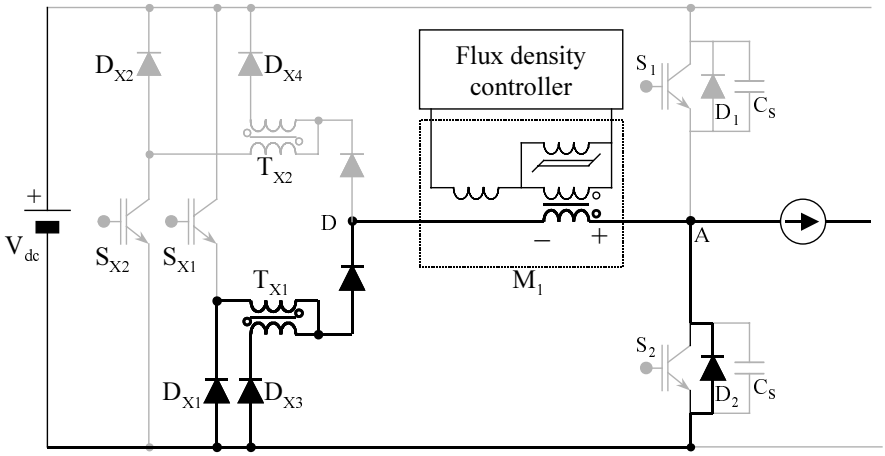


Figure 4.12 Current path description when the anti-parallel diode carries the load current.

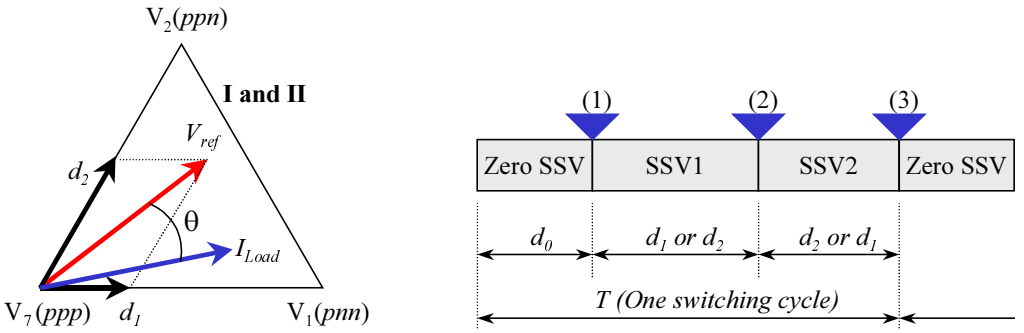


Figure 4.13 Modified SVM scheme when V_{ref} and I_{Load} are in either Sector I or II:

(a) V_{ref} and I_{Load}, and (b) Synchronized turn-on sequence of SSVs.

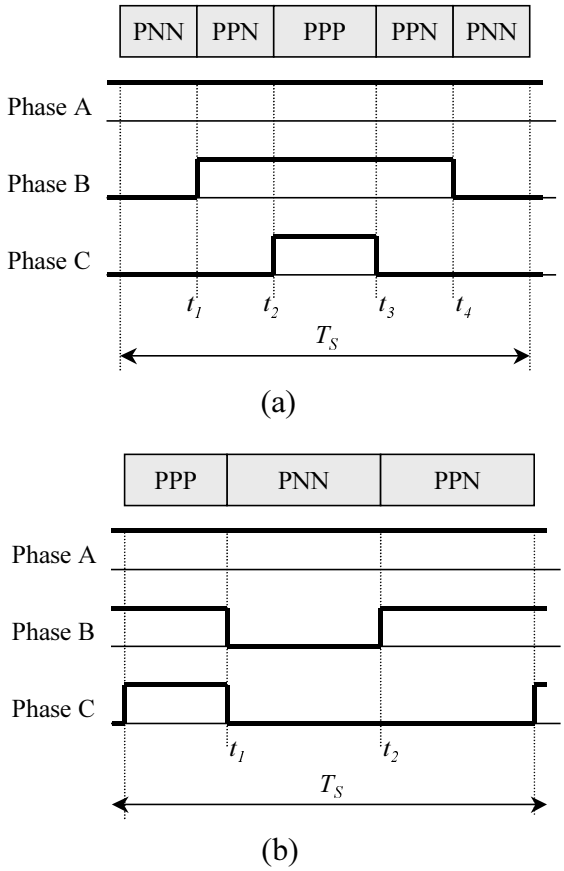


Figure 4.14 Phase control signals of both SVM schemes:

(a) Center-based SVM, and

(b) SVM with synchronized turn-on commutations.

Table 4.1

SSV SEQUENCE AND THE REQUIRED AUXILIARY SWITCH OF THE MODIFIED SVM WHEN V_{ref} IS IN EITHER SECTOR I OR II

Location of Current Vector	Sequences of SSVs and required auxiliary switches					
	First Vector		Second Vector		Third Vector	
I	*ppp*	-S_{X2}-	*pnn*	-	*ppn*	-
II	*nnn*	-S_{X1}-	*ppn*	-	*pnn*	-
III	*nnn*	-S_{X1}-	*ppn*	-	*pnn*	-
IV	*nnn*	-S_{X1}-	*ppn*	-	*pnn*	-S_{X2}-
V	*ppp*	-S_{X2}-	*ppn*	-	*pnn*	-S_{X1}-
VI	*ppp*	-	*ppn*	-	*pnn*	-S_{X1}-
VII	*ppp*	-	*ppn*	-	*pnn*	-S_{X1}-
VIII	*nnn*	-	*pnn*	-	*ppn*	-S_{X2}-
IX	*nnn*	-	*pnn*	-	*ppn*	-S_{X2}-
X	*nnn*	-S_{X1}-	*pnn*	-	*ppn*	-S_{X2}-
XI	*ppp*	-S_{X2}-	*pnn*	-	*ppn*	-S_{X1}-
XII	*ppp*	-S_{X2}-	*pnn*	-	*ppn*	-

- *If the largest load current passes through a switch of the phase throughout the entire switching period*: Commutations of both phases require the operation of the same auxiliary switch. Make the selected zero SSV the first vector, and make the second vector one of the nonzero SSVs that can synchronize the turn-on commutations of both phases. Another nonzero SSV becomes the third vector. Commutation from the first vector to the second vector requires the operation of the auxiliary circuit. This case includes the example given earlier in this section.
- *If the largest load current passes through an anti-parallel diode of the phase throughout the entire switching period*: Commutations of both phases require the operation of the same auxiliary switch. Make the selected zero SSV the first vector, and make the third vector one of the nonzero SSVs that can synchronize the turn-on commutations of both phases. Another nonzero SSV becomes the second vector. Commutation from the third vector to the first vector of the next switching cycle requires the operation of the auxiliary circuit.
- *If the largest load current phase has both switching states in a switching period* : Make the selected zero SSV the first vector, and choose any nonzero SSV as the second vector. Another nonzero SSV becomes the third vector. Both auxiliary switches are used.

This generalized guide allows the operation of the auxiliary circuit in any switching period. Since the method for choosing the SSVs is the same as in the ML SVM scheme, there is no difference in either the number of commutations or the switching losses. Table 4.1 shows the SSV sequences of the modified SVM scheme and the required auxiliary switch operations when V_{ref} is in either Sector I or Sector II.

C. Zero-Voltage Turn-On Commutations

According to the modified SVM scheme, in one switching cycle there might be a synchronized turn-on of two phases or just a single turn-on of one phase. In motor drive applications, the synchronized turn-on commutation is more common. As an example of the synchronized zero-voltage turn-on commutation from diodes to switches, Figure 4.15 (a) shows the waveforms of the commutation from V_8 (*nnn*) to V_4 (*npp*) when $i_a < 0$, $i_b >$

0 and $i_c > 0$. At this moment, phases B and C change their switching statuses from D_4 and D_6 to S_3 and S_5, respectively. Figure 4.16 shows the detailed current conduction statuses of all commutation periods.

- *Preset period* [$t_0 \sim t_1$] : The flux controller saturates the flux of M_1 to block the current flow from the auxiliary circuit to phase A. The saturated M_1 will block the current path during the resonant and discharging periods.

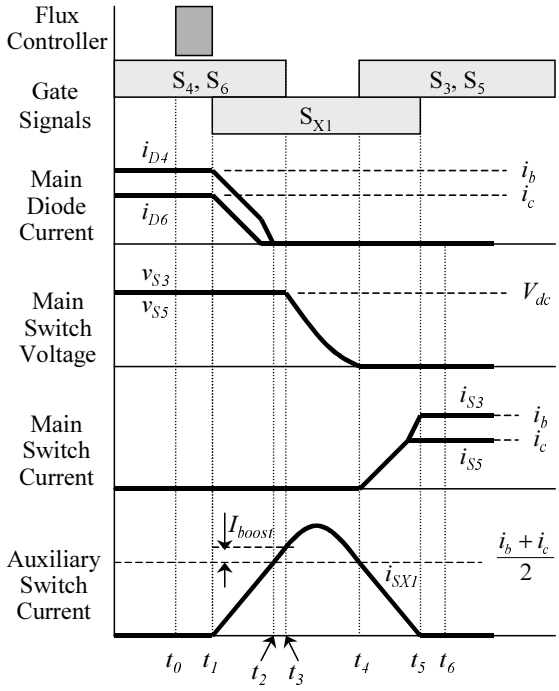
- *Charging period* [$t_1 \sim t_2$] : After S_{X1} turns on at t_1, the auxiliary switch current i_{SX1} increases and the diode currents of D_4 and D_6 decrease linearly. When i_{SX1} reaches half the sum of i_b and i_c at t_2, the anti-parallel diodes D_4 and D_6 turn off with zero-current condition.

- *Boost period* [$t_2 \sim t_3$] : After i_{SX1} reaches half the sum of i_b and i_c at t_2, this switching status continues until i_{SX1} reaches the sum of I_{boost} and half the sum of i_b and i_c at t_3.

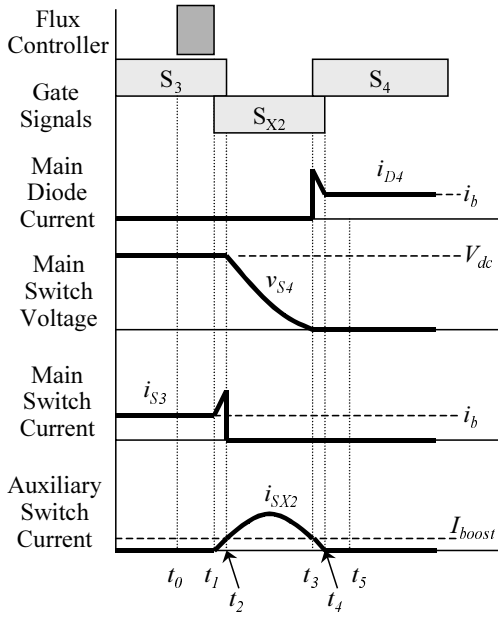
- *Resonant period* [$t_3 \sim t_4$] : When S_4 and S_6 turn off at t_3, the leakage inductance L_{X1} of T_{X1} starts to resonate with the capacitors across S_3, S_4, S_5 and S_6. This resonance charges the capacitors across S_4 and S_6 and discharges those across S_3 and S_5. At t_3, the saturable inductors M_1 start to block the current path from S_{X1} to S_2. The voltages across S_3 and S_5 finally reach zero at t_4.

- *Discharging period* [$t_4 \sim t_5$] : After S_3 and S_5 turn on with zero-voltage condition at t_4, i_{SX1} decreases linearly and both i_{S3} and i_{S5} increase linearly. While M_1 still blocks the current path, i_{SX1} reaches almost zero current, and all load currents flow through S_3 and S_5 at t_5. Therefore, S_{X1} turns off with quasi-zero-current condition at t_5.

- *Reset period* [$t_5 \sim t_6$] : After S_{X1} turns off with quasi-zero-current condition at t_5, the magnetizing current remaining in T_{X1} flows through D_{X1}. This current path provides reverse bias to T_{X1}. This reverse bias resets the magnetizing current, and the current is finally removed at t_6.



(a)



(b)

Figure 4.15 Zero-voltage turn-on commutation waveforms:

(a) Commutation from diode to switch and

(b) Commutation from switch to diode with low load current.

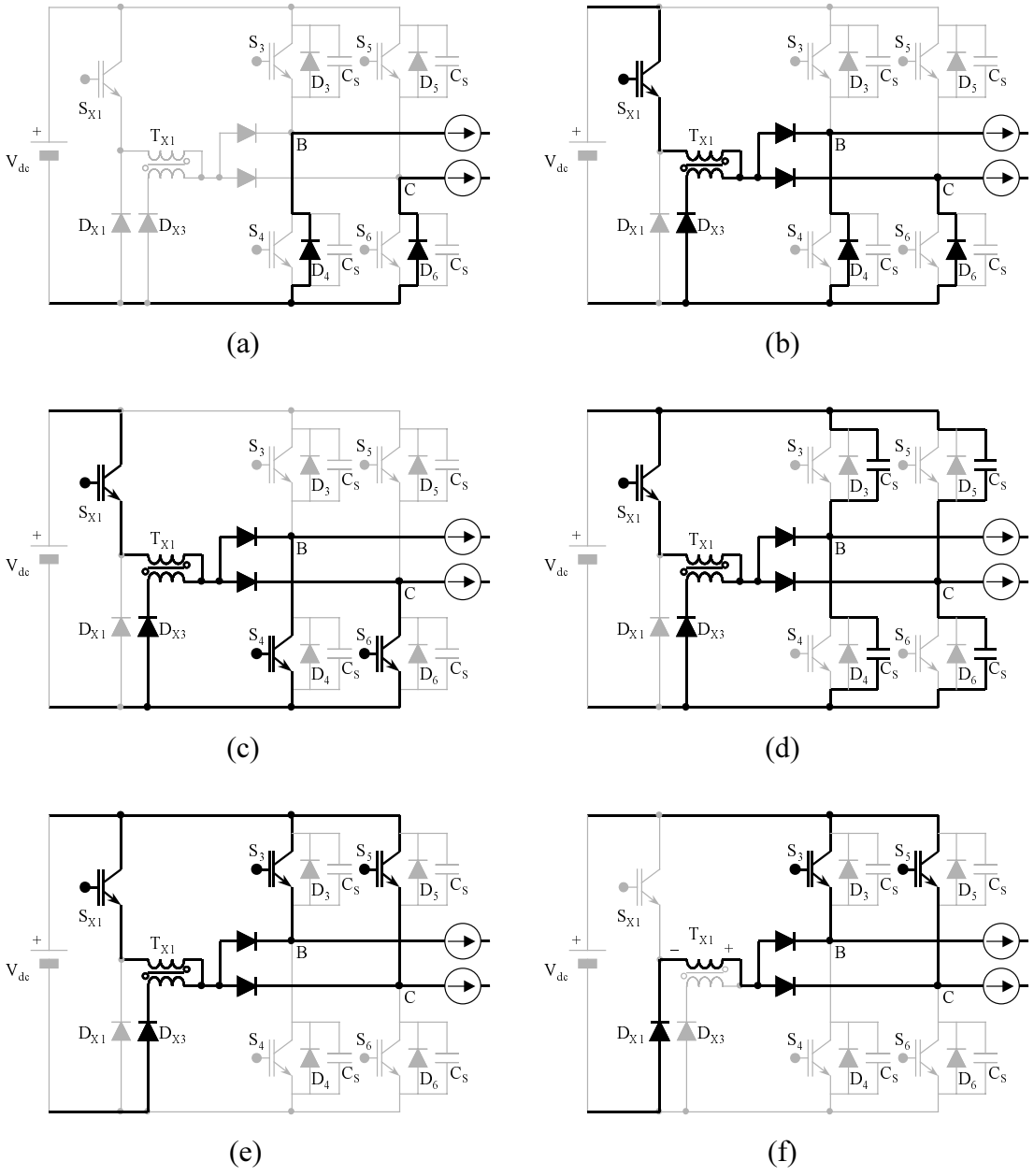


Figure 4.16 Commutation description of sequential periods from diode to switch.

(a) Before commutation including preset period, (b) Charging period, (c) Boost period, (d) Resonant period, (e) Discharging period, and (f) Reset period.

- *After commutation* [t_6 ~] : After the commutation is completed at t_6, the load currents flow through S_3 and S_5 and there is no energy in the auxiliary circuit.

As an example of zero-voltage turn-on commutation from switch to diode with small load current, Figure 4.15 (b) shows the waveforms of the commutation from V_4 (*npp*) to V_5 (*nnp*) when $i_a < 0$, $i_b > 0$, $i_c > 0$, and i_b is small. At this moment, only phase B changes its switching status from S_3 to D_4.

- *Preset period* [$t_0 \sim t_1$] : The flux controller saturates the flux of M_3 to block the current flow from phase C to the auxiliary circuit. The saturated M_3 will block the current path during the resonant and discharging periods.
- *Boost period* [$t_1 \sim t_2$] : After S_{X2} turns on at t_1, the auxiliary switch current i_{SX2} increases linearly and finally reaches the required boost current I_{boost} at t_2.
- *Resonant period* [$t_2 \sim t_3$] : When S_3 turns off at t_2, the leakage inductance L_{X1} of T_{X1} starts to resonate with the capacitors across S_3 and S_4. This resonance charges the capacitor across S_3 and discharges the capacitor across S_4. At t_2, the saturable inductors M_3 start to block the current path from S_5 to S_{X2}. The voltages across S_4 finally reach zero at t_3.
- *Discharging period* [$t_3 \sim t_4$] : After S_3 turns on with zero-voltage condition at t_3, i_{SX2} decreases linearly, and all of i_b flows through D_4. While M_3 still blocks the current path, i_{SX2} reaches almost zero current, and all load currents flow through D_4 at t_4. Therefore, S_{X2} turns off with quasi-zero-current condition at t_4.
- *Reset period* [$t_4 \sim t_5$] : After S_{X2} turns off with quasi-zero-current condition at t_4, the magnetizing current remaining in T_{X2} flows through D_{X2}. This current path provides reverse bias to T_{X2} for resetting the magnetizing current, and the current is finally removed at t_5.
- *After commutation* [t_5 ~] : After the commutation is completed at t_5, the load currents flow only through the main switches and there is no energy in the auxiliary circuit.

4.3.3 Timing Control Issues

Since the operation principles for one phase commutation are the same as those of the conventional ZVT cell, the charging, boost, resonant and discharging times can be represented by using Equations (3.1)–(3.4). However, this topology has a synchronized zero-voltage turn-on commutation. The resonant tank of this commutation consists of two capacitors of two phases, and the auxiliary current is the sum of two phases' currents. Therefore, both the resonant peak current and the commutation time increase, as shown in Equations (4.1) and (4.5):

Peak resonant current $$I_{res} = \sqrt{I_{boost}^2 + I_{res}^2} = \sqrt{I_{boost}^2 + \frac{2 \cdot C_S}{L_p} \cdot V_{dc}^2} \quad (4.1)$$

Charging time [t_1, t_2] $$T_{ch} = \frac{L_p \cdot i_{L(SUM)}}{V_{dc}} \quad (4.2)$$

Boost time [t_2, t_3] $$T_b = \frac{L_p \cdot I_{boost}}{V_{dc}} \quad (4.3)$$

Resonant time [t_3, t_4] $$T_{res} = 2\sqrt{L_p \cdot 2C_S} \cdot \arctan\left(\frac{V_{dc}}{I_{boost}} \cdot \sqrt{\frac{2C_S}{L_p}} \right) \quad (4.4)$$

Discharging time [t_4, t_5] $$T_{dis} = L_p \cdot \frac{i_{L(SUM)}}{V_{dc}} + L_p \cdot \frac{I_{boost}}{V_{dc}} \quad (4.5)$$

where V_{dc}: DC input voltage

L_p: leakage inductance of one coupled inductor

C_S: snubber capacitance across a main switch

$i_{L(SUM)}$: sum of instantaneous two phases currents

I_{boost}: designed boost current

Because both the charging time T_{ch} and the discharging time T_{dis} are proportional to the auxiliary current, the charging and discharging times become longer than those of one phase commutation, as shown Equations (4.2)–(4.5).

4.3.4 Design of Saturable Inductors and Preset Time

A saturable inductor blocks a current path during both the resonant and the discharging periods. Voltage across the saturable inductor is changed during the resonant period, and its average value is half the DC input voltage. Therefore, the blocking capability of the saturable inductor should be equal to or larger than that given in Equation (4.6):

$$V \cdot \sec = \frac{V_{dc}}{2} \cdot T_{res} + V_{dc} \cdot T_{dis} \tag{4.6}$$

This blocking capability determines all design factors of the saturable inductor. The METGLAS is the preferred core material of the saturable inductor. First, both the cross-section area of the core (A_C) and the number of turns of the load-side winding (N_L) are designed using Equation (4.7):

$$V \cdot \sec = N_L \cdot A_C \cdot \Delta B \tag{4.7}$$

where ΔB : Maximum variation of flux density

The control-side winding uses the same cross-section area as the load-side winding. If a control-side bias voltage (V_{con}) is decided, then a smaller number of turns (N_{con}) can be used to obtain a shorter preset time (T_{pre}), as shown in Equation (4.8):

$$T_{pre} = \frac{N_{con}}{V_{con}} \cdot A_C \cdot \Delta B \tag{4.8}$$

In general, just one turn is enough for the control-side winding.

4.3.5 Simulation and Loss Estimation

A. Simulation Results

The designed resonant component values for the proposed ZVT converter are as follows: C_S = 0.22 μF and L_X = 3.4 μH. The boost current I_{boost} is set to 20 A, and the V_{DC} is 300 V.

Figure 4.17 shows the simulation results of the three kinds of commutations: (a) synchronized commutations from D_3 to S_4 and D_5 to S_6 when i_a = 300 A, i_b = -200 A, and

i_c = -100 A; (b) commutation from D_5 to S_6 when i_a = -150 A, i_b = 300 A, and i_c = -150 A; and (c) commutation from S_4 to D_3 when i_b = 10 A. Figures 4.17 (a) and (b) shows that the operations of the auxiliary circuit and PL circuit achieve zero-voltage turn-on commutation in both cases. The auxiliary switch currents in Figure 4.17 (a) become larger than those in Figure 4.17 (b), because the auxiliary circuit should handle both the sum of two phases currents and the resonance of two phases in the case of Figure 4.17 (a). Figure 4.17 (c) shows that the auxiliary circuit helps one phase commutation when the load current is too small to charge and discharge the snubber capacitors.

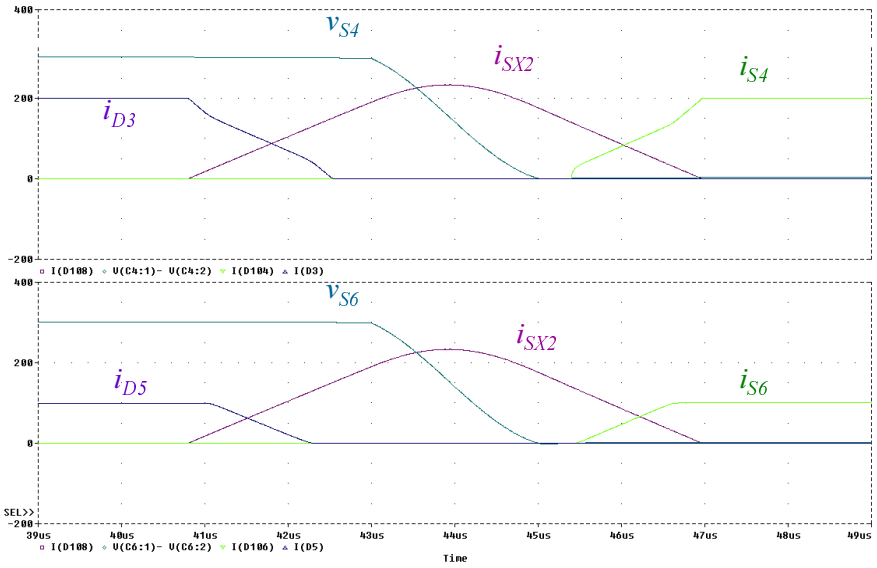
B. Loss Discussion

Figure 4.18 shows a comparison between the inverter total loss of the proposed three-phase PL ZVT inverter and those of other topologies. The inverter total losses of the proposed inverter look similar to those of the conventional three-phase ZVT inverter with inductor feedback. However, because half the auxiliary current of this inverter passes one more diode, this converter has slightly greater conduction loss than the conventional inverter. At the low current area in Figure 4.18, the boost current of this ZVT inverter still results in larger inverter losses than the hard-switching inverter.

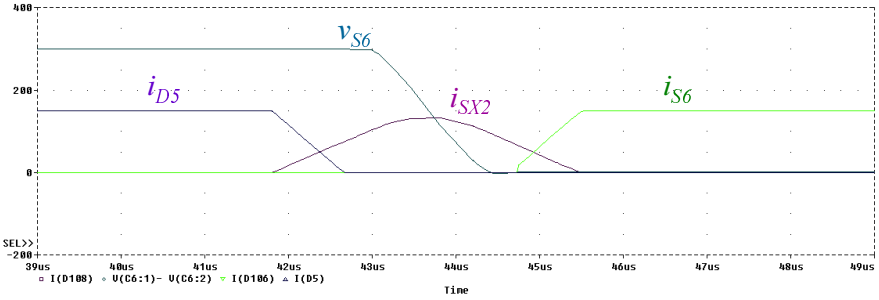
4.3.6 Experimental Results

Figure 4.19 (a) shows the experimental results of the zero-voltage turn-on commutation of the main switch S_2 when V_{dc} = 80 V and i_L = 100 A. These waveforms clearly show the zero-voltage turn-on of S_2 at t_4, as well as the near elimination of current stress at t_5.

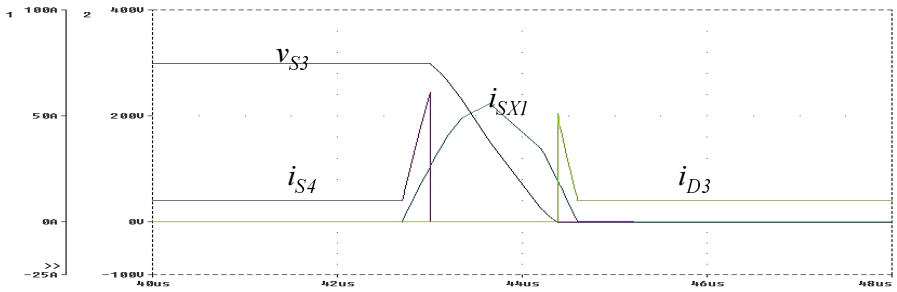
Figure 4.19 (b) shows the experimental waveforms of the PL circuit. The top waveform is the control signal from the main controller, the middle is the real applied voltage across the saturable inductor, and the bottom is the saturable inductor current measured by R_1 in Figure 4.9. For this experiment, two MP3210P cores are used to make a saturable inductor, and both polarities of 20 V are supplied in order to control the flux densities of the saturable inductors. With this design, the saturable inductor begins to be saturated at 2 μsec after the control signal goes active, as shown in Figure 4.19 (b). This means the duration of the preset period should be more than 2 μsec with this PL circuit.



(a)



(b)



(c)

Figure 4.17 Simulation results of the IC ZVT converter with PL circuit:

(a) Synchronized zero-voltage turn-on commutation from diode to switch,

(b) Zero-voltage turn-on commutation of single switch, and

(c) Commutation from switch to diode with small load current.

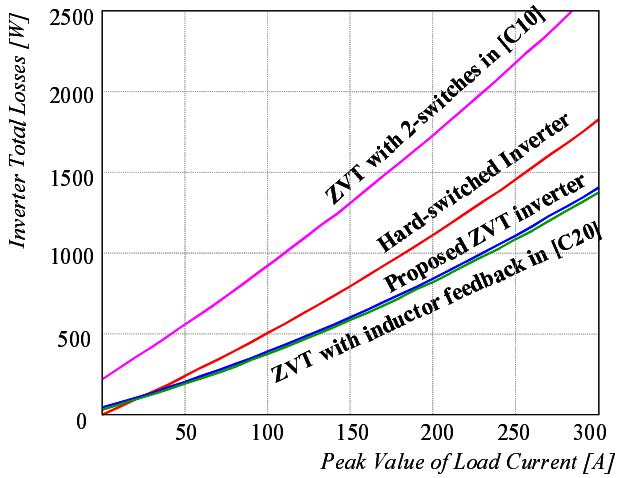
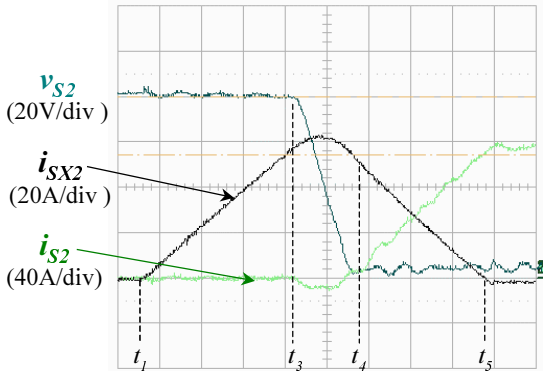
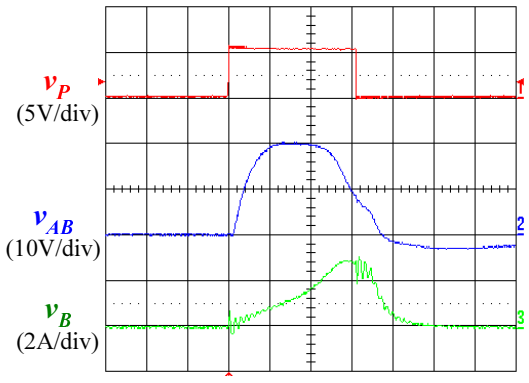


Figure 4.18 Comparison of inverter total losses.



(a)



(b)

Figure 4.19 Experimental results:

(a) Zero-voltage turn-on operation of S_2, and

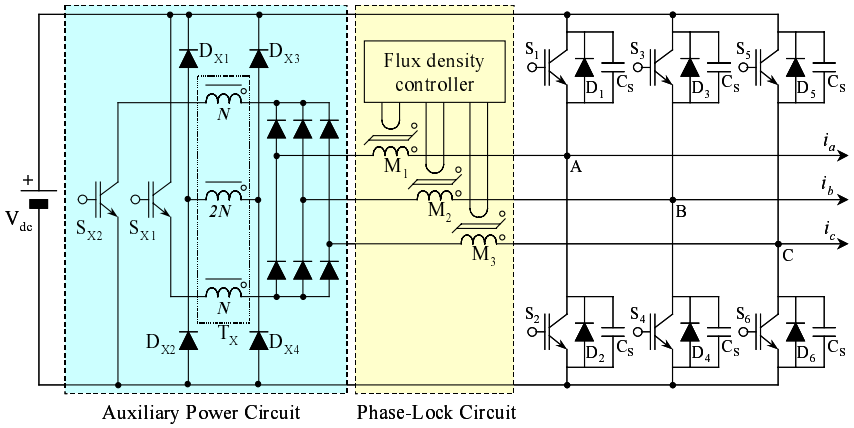
(b) PL circuit operation during preset period.

4.3.7 Other PL ZVT Converters

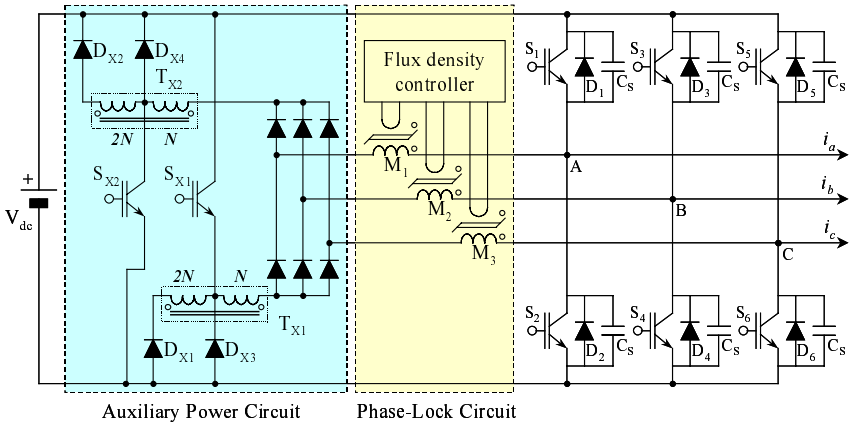
There are two ways to verify the generalized characteristics of the proposed PL circuit concept and the realized circuit: The concept could be applied to other ZVT converter topologies, and the concept could be verified in multi-phase converter structures.

First, the PL circuit can be applied to other ZVT converters with the same structure and design procedure as the ZVT converter with inductor feedback shown in Figure 4.10. Figure 4.20 shows the simplified power stages of three three-phase ZVT converters with the help of the PL circuit: the Transformer-assisted ZVS pole converter, the True-PWM ZVS pole converter, and the ARCP converter. Each auxiliary circuit of these simplified power stages has only two auxiliary switches. The auxiliary circuit of the PL Transformer-assisted ZVS pole converter consists of one coupled inductor with three windings as well as two auxiliary switches, as shown in Figure 4.20 (a). The PL ARCP converter also has only one resonant inductor, as shown in Figure 4.20 (c). These two PL converters have one more advantage over the PL ZVT converter with inductor feedback: They do not have any problems controlling the flux density of the saturable inductors, because there is no current path though the auxiliary circuit before an auxiliary switch turns on. Therefore, the ML SVM scheme can be used with these converters without requiring any modification. Although each PL ZVT converter needs a slightly different SVM scheme, none of these converters requires modification of the PL circuit itself. These real applications of the PL circuit to several ZVT converter topologies verify the generalized characteristics of the PL concept.

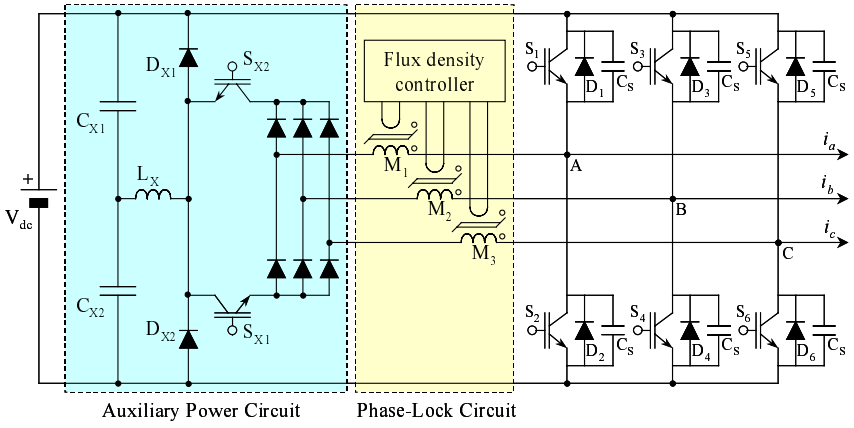
The second method of verifying the generalized characteristics involves the multi-phase application. One auxiliary switch supports all the top main switches, while another auxiliary switch supports all the bottom main switches. Therefore, the auxiliary circuit will only need two auxiliary switches, even if the number of converter phases increases. An additional phase requires just one more saturable inductor and its flux density controller. This is a significant advantage to using the PL concept in multi-phase converter applications.



(a)



(b)



(c)

Figure 4.20 PL ZVT three-phase converters with two auxiliary switches:

(a) PL Transformer-assisted ZVS pole converter,

(b) PL True-PWM ZVS pole converter, and

(c) PL ARCP converter.

4.4 IMPROVED PL ZVT CONVERTER

The PL circuit used in a PL ZVT converter with coupled inductors has some limitations of operation, as explained in Section 4.3. In order to eliminate these limitations, the modified SVM scheme synchronizes the commutations of two phases in some power factors, which complicates control. In order to use the ML SVM scheme, the PL circuit should be able to control connections between the phases and the auxiliary circuit for any switching pattern. This chapter proposes a modified power stage to improve operations of the PL circuit.

4.4.1 Power Stage

Figure 4.21 (a) shows the original structure of a PL ZVT cell for a top main switch S_1. When an anti-parallel diode D_2 carries the load current, the flux density controller cannot control saturable inductor M_1. The main reason for this inability is that both D_{X1} and D_{X3} carry a small amount of the load current whenever D_2 carries the load current. Therefore, blocking these currents might improve the control capability of the PL circuit. Because the two windings of coupled inductor T_X always have identical current directions, removing either D_{X1} or D_{X3} can block current paths. D_{X3} provides a current path during the zero-voltage turn-on commutation, so this diode cannot be removed. However, D_{X1} only provides a current path for magnetizing current during the reset period. Except for the reset period, all commutations can be handled by a power stage, as shown in Figure 4.21 (b). This modified structure does not have any current path through the auxiliary circuit when the load current passes through D_2, so the flux density controller can saturate M_1 to any polarity to allow for zero-voltage turn-on commutation. A reset winding of T_X can provide a magnetizing current path with D_{R1} and D_{R2} after S_{X1} turns off, as shown in Figure 4.22 (a). Figure 4.22 shows the modified power stages for both the top main switch S_{X1} and the bottom main switch S_{X2}. Combining these power stages creates a power stage for the PL ZVT three-phase converter with coupled inductors, as shown in Figure 4.23. The auxiliary circuit consists of two auxiliary switches and two coupled inductors with three windings. This power stage improves operations of the PL circuit, thus allowing the use of the ML SVM scheme.

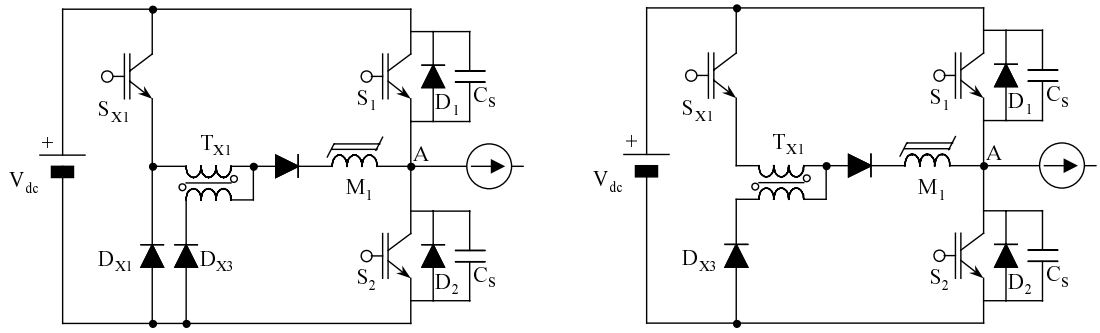


Figure 4.21 PL ZVT cells for top main switches:

(a) Original structure and (b) Modified structure.

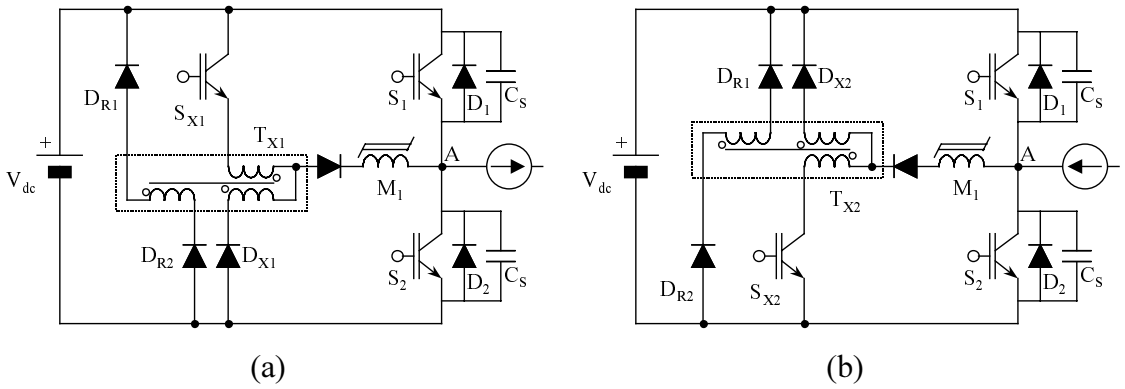


Figure 4.22 Power stage of improved PL ZVT cells for one phase:

(a) Structure for top main switches, and

(b) Structure for bottom main switches.

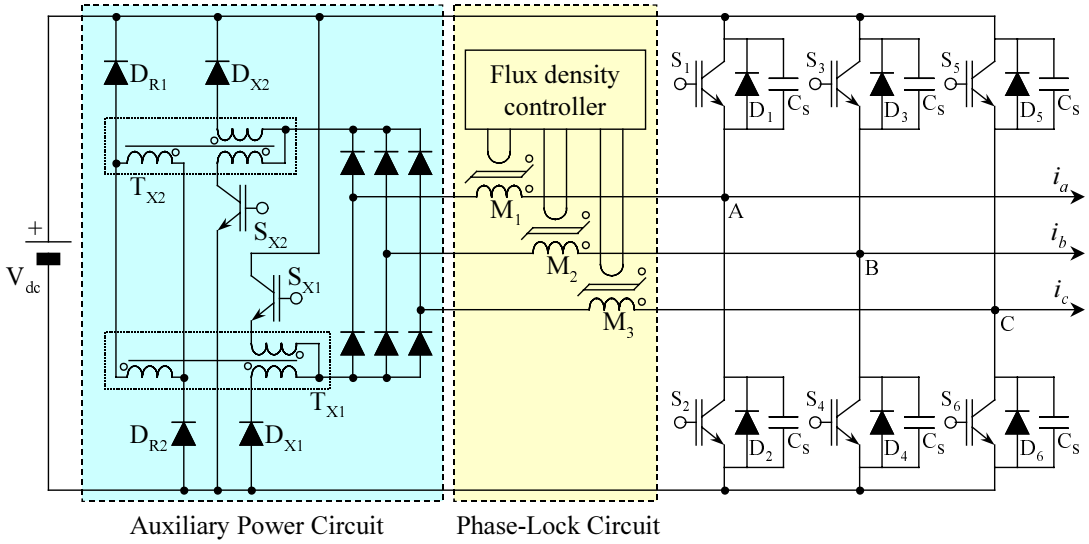


Figure 4.23 Power stage of improved PL ZVT three-phase converter.

4.4.2 Operation Principles

A. Space Vector Modulation Scheme

Since each phase of an improved PL ZVT converter can change its switching status independently without any interference with other phases, the improved PL ZVT three-phase converter operates with the unmodified ML SVM scheme. This improvement allows the auxiliary circuit and its control circuit to be a piggyback type.

B. Zero-Voltage Turn-On Commutations

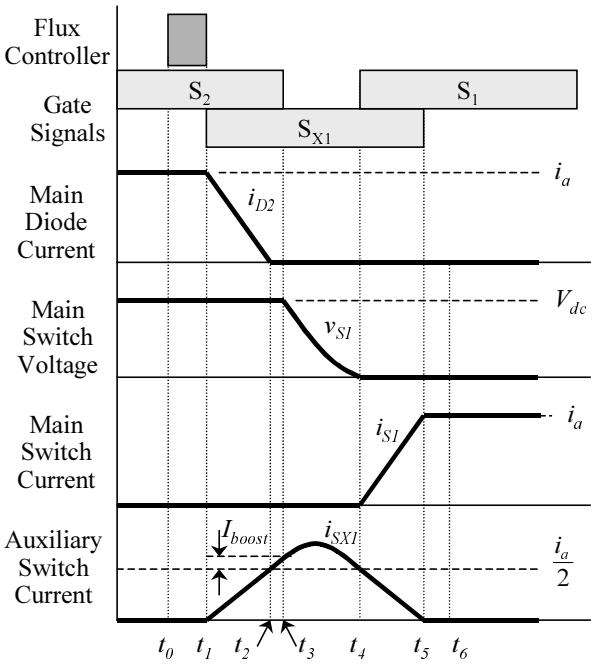
Figure 4.24 (a) shows the commutation waveforms of phase A when the load current i_a is positive. At this moment, the load current conduction is changed from main diode D_2 to main switch S_1 with the operation of an auxiliary switch S_{X1}. Figure 4.25 describes the current conduction statuses of all commutation periods.

- *Preset period* [$t_0 \sim t_1$] : The flux density controller saturates the flux of M_1 to allow the current to flow from the auxiliary circuit to phase A, while M_2 and M_3 are saturated to the opposite current direction. Thus, only phase A is connected to the auxiliary circuit.

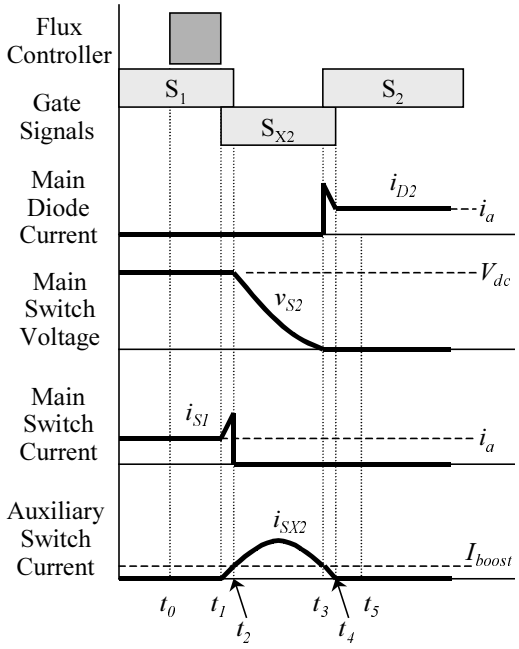
- *Charging period* [$t_1 \sim t_2$] : After S_{X1} turns on at t_1, the auxiliary switch current i_{SX1} increases and the diode current of D_2 decreases linearly. When i_{SX1} reaches half the load current at t_2, the anti-parallel diode D_2 turns off with zero-current condition at t_2.

- *Boost period* [$t_2 \sim t_3$] : After i_{SX1} reaches half the load current at t_2, this switching status continues until i_{SX1} reaches the sum of i_{boost} and half the load current at t_3.

- *Resonant period* [$t_3 \sim t_4$] : When S_2 turns off at t_3, the leakage inductance L_{X2} of T_{X2} starts to resonate with the capacitors across S_1 and S_2. At t_3, two saturable inductors M_2 and M_3 start to block the current flowing from S_{X1} to both S_4 and S_6. The voltage across S_1 finally reaches zero and S_1 turns on with zero-voltage condition at t_4.



(a)



(b)

Figure 4.24 Zero-voltage turn-on commutation waveforms:

(a) Commutation from diode to switch and

(b) Commutation from switch to diode with low load current.

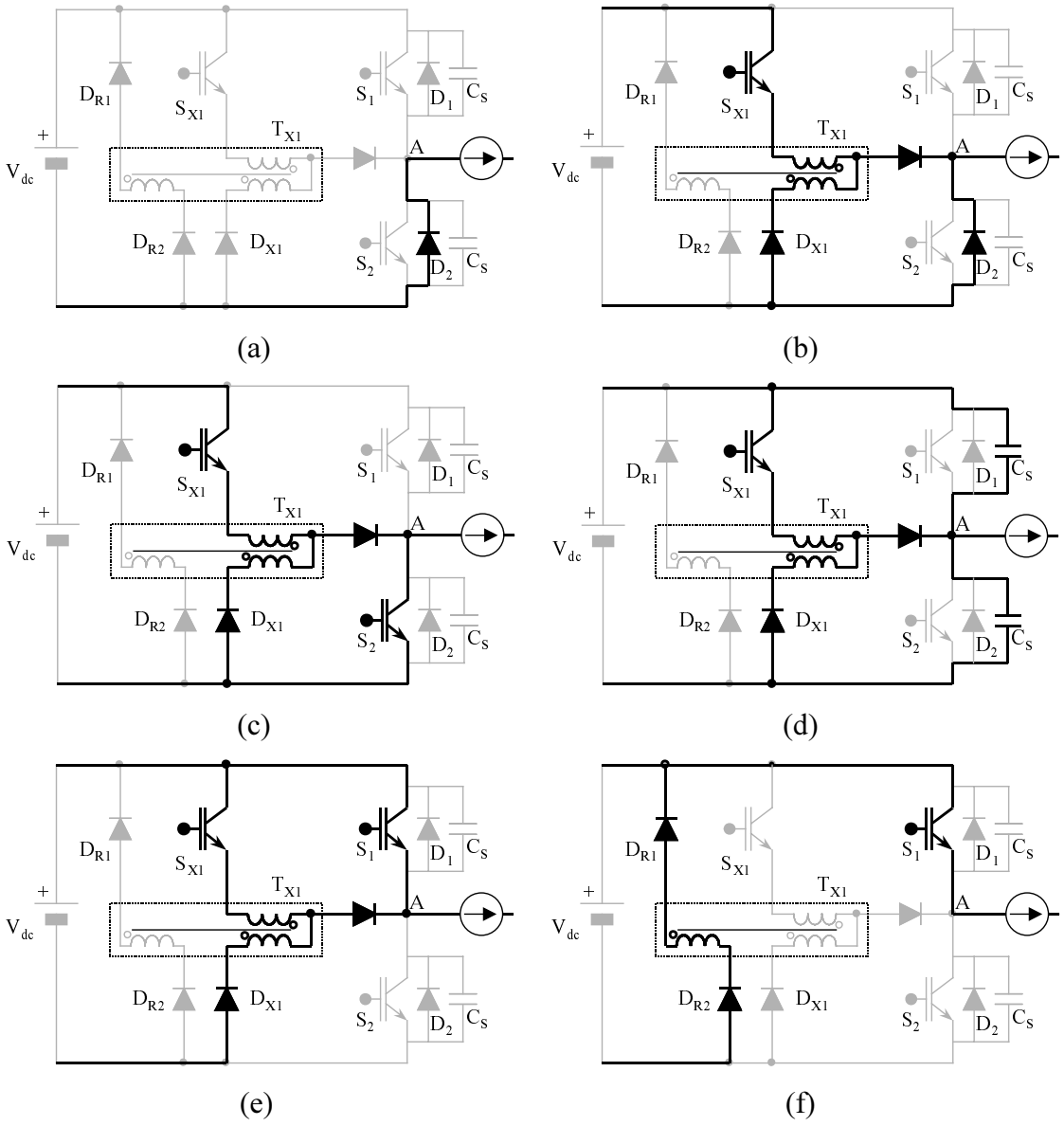


Figure 4.25 Commutation description of sequential modes from diode to switch.

(a) Before commutation including preset period, (b) Charging period,
(c) Boost period, (d) Resonant period, (e) Discharging period, and
(f) Reset period.

- *Discharging period* [$t_4 \sim t_5$] : After S_1 turns on with zero-voltage condition at t_4, i_{SX1} decreases and i_{S1} increases linearly. While M_2 and M_3 still block the current flowing, i_{SX1} reaches almost zero and all load current flows through S_6 at t_5. Thus, S_{X1} turns off with quasi-zero-current condition at t_5.
- *Reset period* [$t_5 \sim t_6$] : After S_{X1} turns off with quasi-zero-current condition at t_5, the magnetizing current remaining in T_{X1} flows through D_{X1}. This current path provides reverse bias to T_{X1}. This reverse bias resets the magnetizing current, and the current is finally eliminated at t_6.
- *After commutation* [$t_6 \sim$] : After the commutation is completed at t_6, the load currents flow through the main bridges and no energy remains in the auxiliary circuit.

As an example of a zero-voltage turn-on commutation from switch to diode with small load current, Figure 4.24 (b) shows waveforms of the commutation from S_1 to D_2. The operations of all commutation periods are the same as those of the PL ZVT converter.

4.4.3 Simulation Results

The biggest concern involved with the research of the PL ZVT converter is the actual operation of the PL circuit. Therefore, the simulation should verify not only the zero-voltage commutations but also PL circuit operations in an improved PL ZVT converter.

A. PL Circuit Operation

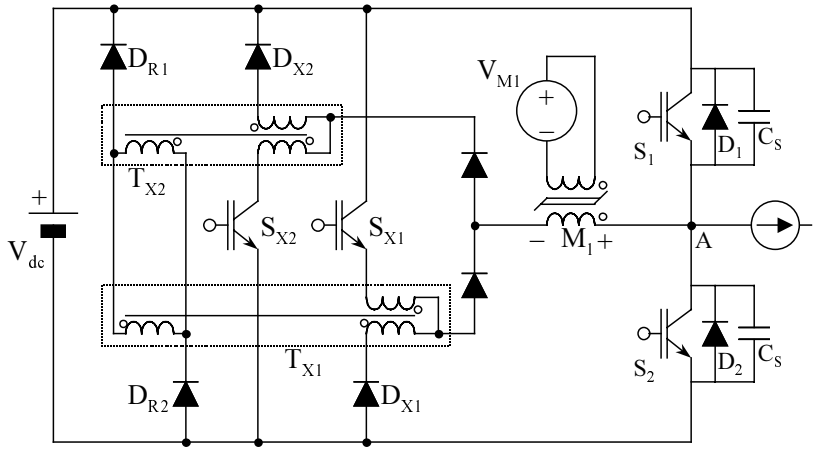
Figure 4.26 (a) shows a power stage, including the entire auxiliary circuit and a half-bridge of phase A. A power supply V_{M1} represents the control-side bias voltage that is used to saturate the saturable inductor M_1. This circuit is simulated to verify operations of the saturable inductor. Figure 4.26 (b) shows the simulation results. If V_{S1} is positive, then S_1 is in on-state and carries a load current. As shown in Figure 4.26 (b), the bias voltage V_{M1} is reflected to a load-side winding with this condition. This implies that the flux density controller can properly control the saturable inductor. Although S_1 is in off-state and D_2 carries the load current, V_{M1} is reflected to the load-side winding, as shown in

Figure 4.26 (b). This operation is impossible in the original PL ZVT converter. Therefore, the improved PL ZVT converter can properly control saturable inductors in any case.

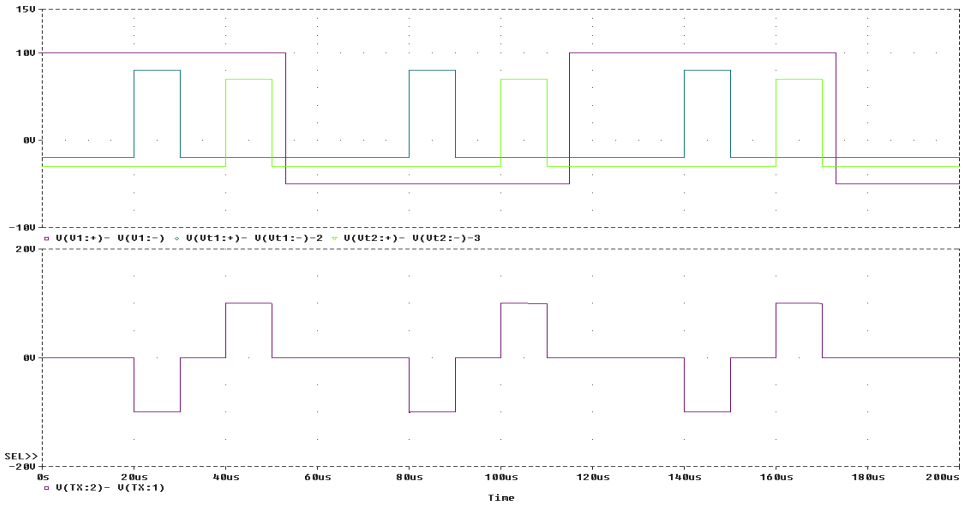
B. Zero-Voltage Turn-On Commutations

Designed values of resonant components of the proposed ZVT converter are as follows: C_S = 0.22 μF, L_X = 3.4 μH, i_{boost} = 20 A, and V_{DC} = 300 V.

Figure 4.27 shows simulation results of two kinds of commutation: (a) commutation from D_2 to S_1 with i_a = 300 A; and (b) commutation from S_1 to D_2 with small current. These waveforms verify that the improved PL ZVT converter achieves the expected zero-voltage condition in any commutation.



(a)

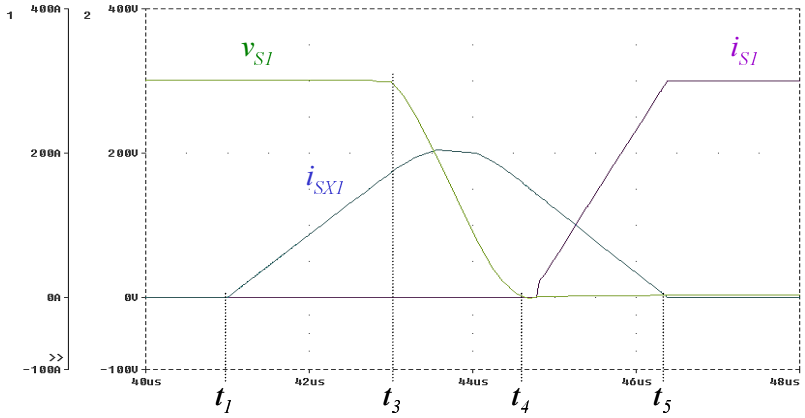


(b)

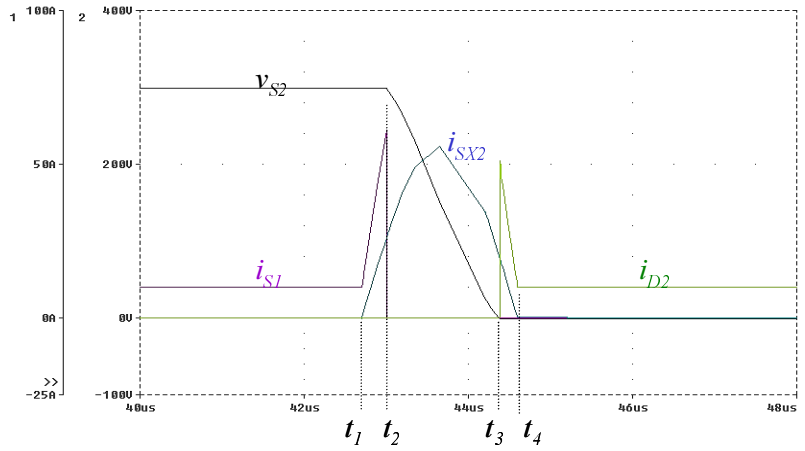
Figure 4.26 Effect of control power (V_{M1}) on the load side of the saturable inductor:

(a) Power circuit with the control power supply (V_{M1}) for flux control and

(b) Simulation results.



(a)



(b)

Figure 4.27 Simulation results of the improved PL ZVT converter:

(a) Zero-voltage turn-on commutation from diode to switch and

(b) Commutation from switch to diode with small load current.

4.5 THYRISTOR-ASSISTED (TA) ZVT CONVERTER

Since the PL circuit prevents interference among phases, the auxiliary circuit is able to achieve zero-voltage turn-on commutation for all main switches. The saturable inductor is a good candidate to realize the PL circuit, because it is already used in the conventional ZVT converter with inductor feedback. However, the higher DC voltage requires a larger cross-section area and more turns for the saturable inductor. In addition, the control-side bias voltage for controlling the flux density should increase in order to limit the preset period to an acceptable duration. Therefore, the PL circuit using saturable inductors becomes too large and expensive for high-voltage applications. This section proposes another approach, in which the PL circuit uses thyristors for high-voltage applications [C34].

4.5.1 Power Stage

In Figure 4.3, because the rectifying diodes (D_{R1}, D_{R3} and D_{R5}) cannot prevent the interference among the main bridges, controllable power devices are required in series with the diodes in order to achieve the proper zero-voltage turn-on commutations. Operation of this controllable power device is required only during the commutation periods. During the main switch conduction period, the status of this device has no effect on the converter because both S_{X1} and S_{X2} are in off-states.

Among power devices, the thyristor is one of the strongest candidates. Since a thyristor is turn-on controllable, it meets the requirements of the PL circuit. A thyristor has a very large peak current rating compared with its RMS current rating. These current ratings are the same as those of the auxiliary circuit current. In general, however, the thyristor has a very long turn-off time, making it difficult to use in high switching frequency applications. If the turn-off time is longer than a switching period, then the thyristor cannot control the connection between the main bridges and the auxiliary circuit. Fortunately, several power device companies manufacture high-speed thyristors with turn-off times of less than 20 μsec. This fast turn-off time is meaningful with a 100-μsec switching cycle (f_{sw} = 10 kHz). Therefore, three high-speed thyristors replace the

rectifying diodes for the top ZVT cells. The same method is used to place three high-speed thyristors in the bottom ZVT cell. Combining these top and bottom ZVT cells creates a new power stage that includes two auxiliary switches assisted by six high-speed thyristors. According to switching sequences, one or two thyristors with the same direction turn on for commutations. Therefore, three phases can be merged to one point between thyristors and the auxiliary circuit. This allows the top and bottom auxiliary circuits to share one set of coupled inductors. Finally, the auxiliary circuit consists of two switches and a set of coupled inductors assisted by the high-speed thyristors, as shown in Figure 4.28. This power stage is called the Thyristor-Assisted (TA) ZVT converter.

Because the peak current rating of a thyristor is much higher than its RMS current, the thyristor is preferred over other power devices for use as the auxiliary switch. By using thyristors in the PL circuit, the proposed converter becomes attractive for high-power applications.

4.5.2 Operation Principles

A. Modified Space Vector Modulation Scheme

The time intervals of SSVs might be shorter than the turn-off time of a thyristor in the ML SVM scheme. If two consecutive commutations require the same auxiliary switch operation, the time interval between the commutations should be longer than the turn-off time of the thyristor used in the PL circuit. Otherwise, reverse voltage applied to the thyristor results in reverse recovery current.

If these commutations are synchronized, the next operation of the same auxiliary switch can be in the next switching cycle. Because the turn-off time of a thyristor is much shorter than one switching cycle, this synchronization prevents the reverse recovery current problem. This modified SVM scheme is identical to the SVM scheme used in the PL ZVT converter. Therefore, the explanation given in Section 4.3.2 can be used as a general guideline for the modified SVM scheme of the TA ZVT converter.

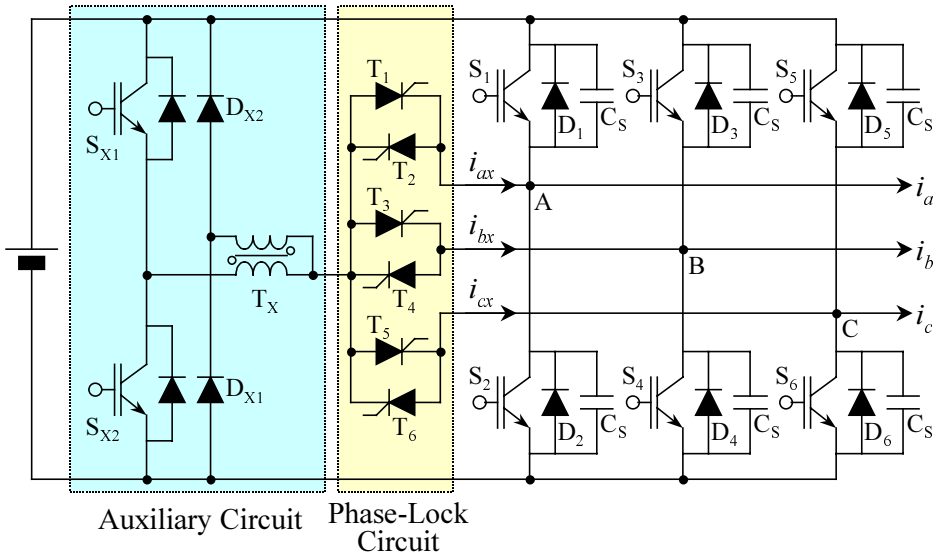


Figure 4.28 Power stage of TA ZVT three-phase converter.

B. Zero-Voltage Turn-On Commutations

Figure 4.29 shows two kinds of zero-voltage commutation waveforms: synchronized commutation from diodes to switches and commutation from switch to diode with small load current. In any case, when an auxiliary switch turns on at t_0, the corresponding thyristors turn on together. The remaining periods (charging, boost, resonant, discharging and reset periods) from t_1 are the same as those of the PL ZVT three-phase converter with coupled inductors.

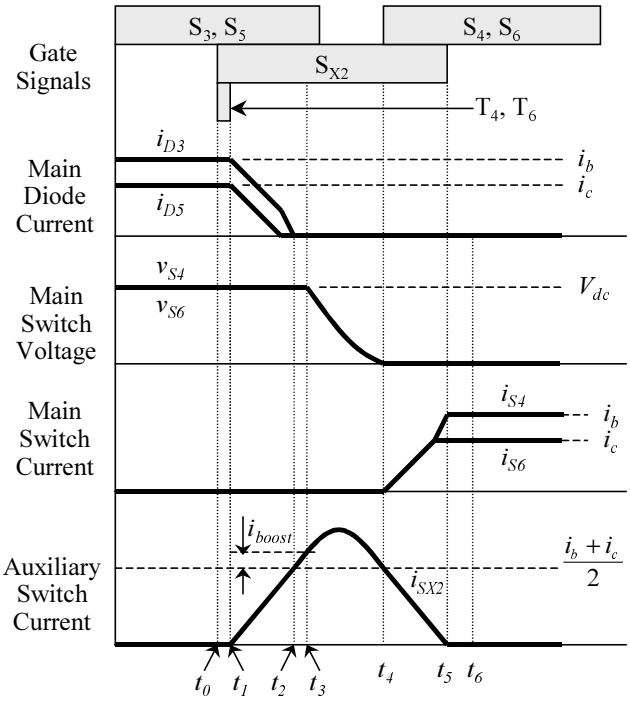
4.5.3 Implementations

Because modifying the SVM scheme only requires changing the SSV sequences, the SVM scheme can be easily implemented by modifying both the control program and the hardware of the conventional converter. In general, the conventional ZVT converter has a programmed digital-signal-processor (DSP) and/or some logic circuits, such as electrically programmable logic device (EPLD). Therefore, the modified DSP program and redesigned logic circuit can simply implement the thyristor triggering signals (T1-T6) of the proposed ZVT topology, as shown in Figure 4.30. The gate signals for the auxiliary switches (SX1 and SX2) are generated using additional two three-input OR-gates, as shown in Figure 4.30.

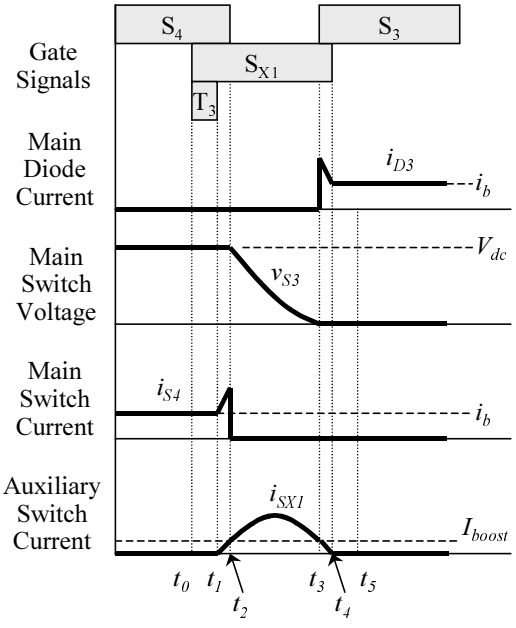
The selection of thyristor depends on the switching frequency of the converter, because the turn-off time of the thyristor should be less than the time required for one switching cycle. In general, the turn-off time of a high-speed thyristor is less than 20 μsec, so this thyristor is suitable for a converter with 10~20 kHz switching frequency. For the implementation, the proposed ZVT topology uses three modules of TT46F08EC (Eupec) for a 100-kW converter. These thyristors have 20-μsec turn-off times and 800-V/1300-A maximum ratings.

4.5.4 Other TA ZVT Converters

Six thyristors help the auxiliary circuit to operate as a PL circuit. There are two ways to verify the general usage of this PL circuit: application to the other kinds of ZVT converter topologies and application to the multi-phase converters.



(a)



(b)

Figure 4.29 Zero-voltage turn-on commutation waveforms:

(a) Commutation from diode to switch, and

(b) Commutation from switch to diode with low load current.

Figure 4.31 shows the simplified power stages of two conventional ZVT three-phase converters with the help of the thyristor PL circuit: the Transformer-assisted ZVS pole converter and the True-PWM ZVS pole converter with simplified auxiliary circuits and thyristor PL circuits. Both auxiliary circuits consist of two auxiliary switches and a set of coupled inductors. These simplified ZVT converters verify the general usage of the thyristor PL circuit.

The second method involves applying the thyristor PL circuit to multi-phase converters. An auxiliary switch supports all the top main switches, while another switch supports all the bottom main switches. Therefore, the auxiliary circuit requires only two auxiliary switches regardless of the number of phases. Two more thyristors are all that is required by an additional phase.

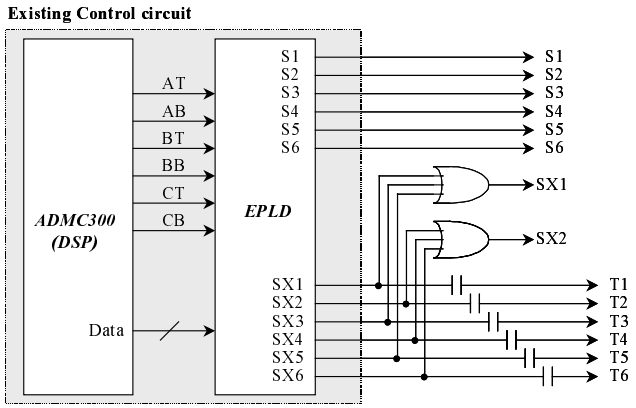


Figure 4.30 Control circuit diagram to generate the gate signals.

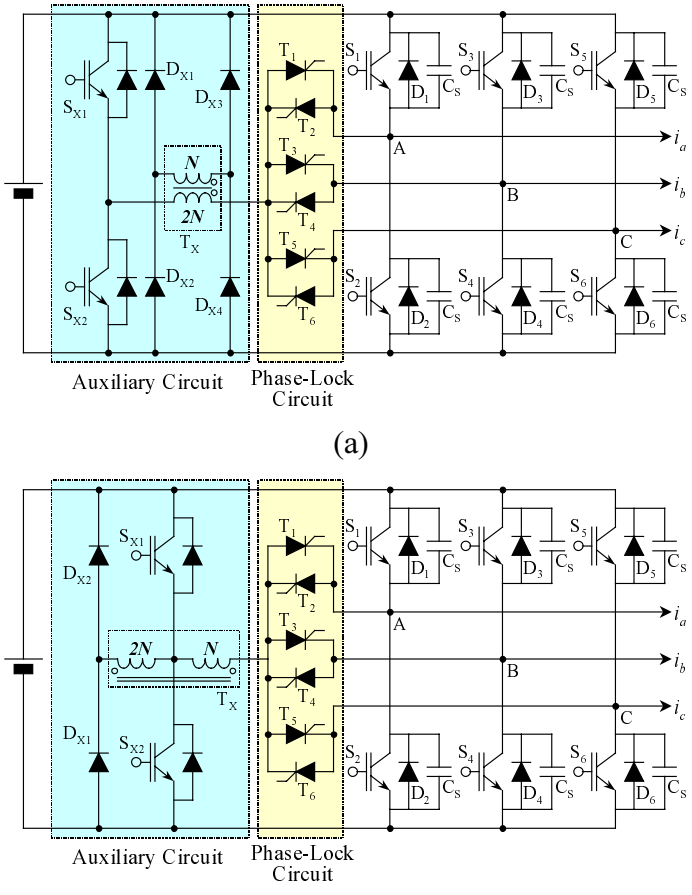


Figure 4.31 Simplified ZVT three-phase converters with thyristors:

(a) TA Transformer-assisted ZVS pole converter, and

(b) TA True-PWM ZVS pole converter.

4.6 SINGLE-SWITCH (SS) ZVT CONVERTER

The auxiliary circuit of a three-phase S^3L ZVT converter has three auxiliary switches, as shown in Figure 3.14. The real implemented auxiliary circuit also has three small saturable inductors, as explained in Section 3.3.3. These saturable inductors lead logically to ideas of combining the three-phase S^3L ZVT converter and the PL concept. This attempt creates a novel power stage with one auxiliary switch, as shown in Figure 4.32. The auxiliary circuit consists of only one auxiliary switch, one coupled inductor with three windings, and seven diodes, so this topology is named the Single-Switch (SS) ZVT converter. This structure has two fewer auxiliary switches and two fewer coupled inductors than the auxiliary circuit of the three-phase S^3L converter shown in Figure 3.14. However, the saturable inductors should be increased and their flux density controller should be added.

Operation principles are also a combination of the S^3L and the improved PL concepts. During the preset period before S_X turns on, the PL circuit controls the connection of each phase to the auxiliary circuit. Then, all the remaining periods from charging to reset are exactly the same as those of the S^3L ZVT converter.

Although the control method is more complicated than that for the S^3L ZVT converter, this converter is attractive for use in multi-phase converter applications, especially those with more than three phases.

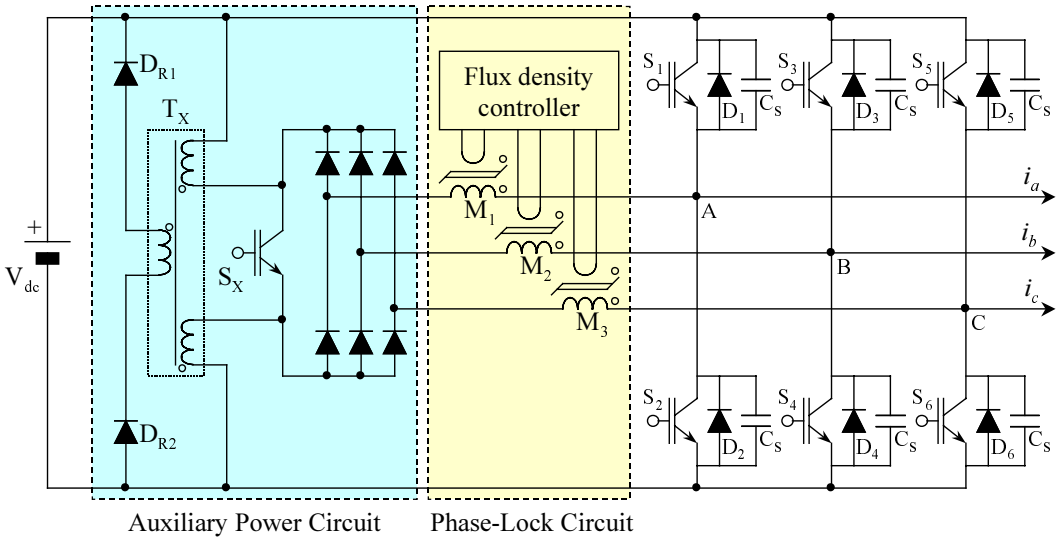


Figure 4.32 Power stage of the proposed SS ZVT three-phase converter.

4.7 SUMMARY

Since the commutation sequences for all the top ZVT cells are identical, one auxiliary switch seems to provide the zero-voltage conditions for all the top main switches. However, due to interference among the phases, none of the phases can provide the zero-voltage condition for all its commutations. In order to solve this interference problem, Section 4.2 proposed the Phase-lock (PL) concept and realized the concept using saturable inductors and their flux density controller. The PL concept allows only two auxiliary switches to assist the zero-voltage turn-on commutations of all main switches.

Section 4.3 described examples of the simplified ZVT converters using the PL circuit. As a major example, the auxiliary power stage of the ZVT converter with inductor feedback is simplified using the PL concept. With the help of the modified SVM scheme using synchronized turn-on commutations, the simplified ZVT converter achieved the zero-voltage turn-on commutations of the main switches as well as the zero-current turn-offs of the auxiliary switches. Simplifying the other ZVT converters using the PL circuits verifies the generalized characteristics of the PL concept.

In order to use the ML SVM scheme, Section 4.4 proposed an improved PL ZVT converter with coupled inductors. This topology modifies the auxiliary circuit so that the PL circuit can control the connection between the auxiliary circuit and phases in any commutation. The proposed ZVT converter topology makes the PL concept more reliable and attractive to real implementations.

For high-voltage applications, high-speed thyristors instead of saturable inductors realized the PL circuit. Section 4.4 described the power stages and operation principles of the simplified inductor-coupled ZVT converters using the thyristor PL circuit.

Combining the S^3L ZVT cell and the PL concept creates a power stage with single auxiliary switch in multi-phase inverters, as described in Section 4.5.

Chapter 5. AVERAGE MODELING OF INDUCTOR-COUPLED ZVT CONVERTERS

Soft-switching topologies change the duty ratios of gate signals as well as current paths. Therefore, the soft-switching converters definitely affect the dynamic behavior of the converters. Small signal analysis with the average models of soft-switching converters brings to light these changes.

This chapter will propose the average model of the ZVT converter with inductor feedback, using the results of the timing analysis that was discussed in Section 2.3. For developing the average model, the effects of operation timings as well as SVM schemes should be clearly analyzed. While the operation timings provide variations in duty ratios and DC currents, the SVM scheme affects the *dq*-transformation of an average model.

The small signal analysis using the developed average model is necessary for designing the closed-loop feedback control of the converters. The average models also help to easily identify the input and output characteristics of the converter.

5.1 LITERATURE REVIEW OF CONVENTIONAL AVERAGE MODELING

Several research papers have attempted to develop average models of soft-switching converters [E3-E4, E9-E13, E15-E17].

For DC-DC converters, there have been several attempts to make average models [E4, E11, E13, E17]. In particular, many papers have developed the average model of the full-bridge DC-DC converter using the phase-shift technique [E4, E11, E13]. Moreover, the converter has been analyzed in large-signal as well as small-signal cases [E17].

Unfortunately, there were few approaches to make average models of multi-phase converters [E12, E15-E16], which are the major targets of this dissertation. The attempts were either limited to either small-signal analysis [E12, E15] or characterization of output voltage [E16]. Although there was an attempt to model a three-phase boost rectifier using one of the DC-side ZVT topologies [E12], the ZVT topology is not appropriate for medium- or high-power applications. Another attempt made the average model of a three-phase ARCP inverter [E16], but it focused only on the characterization of output voltage. Thus far, there has been no approach to develop the average model of inductor-coupled ZVT converters.

The multi-phase converter has AC lines at either the input or the output side. Therefore, the timing analysis of multi-phase converters is more complicated than that of DC-DC converters, and the average models are generally developed on *dq*-coordinates. The following sections will discuss the development of the average model using the results of the timing analysis and the SVM scheme.

5.2 ANALYSIS OF AFFECTED FACTORS FOR MAKING AVERAGE MODEL

ZVT operations affect the duty ratios of the main switch gate signals. Therefore, by considering the affected duty ratios, the average model of a ZVT converter can be modified from the average model of a hard-switching converter. There are several factors that might result in the change of duty ratios. This section will analyze the factors by considering not only the operations in one switching cycle but also the SVM schemes.

Since the AC-side values of a three-phase converter are time-varying, *dq* coordinates are used for its average modeling and control. In a hard-switching converter, the *dq* components become time-invariant in steady state. However, the *dq* components of a soft-switching converter might not, because the feedback values of the load currents affect the pulse widths. This section will propose a solution to this issue, as well.

5.2.1 Average Model of Hard-Switching Converter

Figure 5.1 (a) shows the power stage of a three-phase boost rectifier. The average model of this power stage can be derived on *abc*-coordinates. The voltages and currents of the average model are still time-varying variables. Therefore, a transformation from *abc*- to *dq*-coordinates is necessary to make a time-invariant average model. Equation (5.1) shows a transformation matrix for the coordinate transformation:

$$T_{abc/dq} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos\omega t & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin\omega t & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{5.1}$$

Figure 5.1 (b) shows the time-invariant average model on *dq*-coordinates. Equations (5.2) and (5.3) describe the state equations of the model:

$$\frac{d}{dt}\begin{bmatrix} \bar{i}_d \\ \bar{i}_q \end{bmatrix} = \frac{1}{3L} \cdot \begin{bmatrix} \bar{v}_d \\ \bar{v}_q \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \bar{i}_d \\ \bar{i}_q \end{bmatrix} - \frac{1}{3L} \cdot \begin{bmatrix} d_d \\ d_q \end{bmatrix} \cdot \bar{v}_{dc} \tag{5.2}$$

$$\frac{d}{dt}\bar{v}_{dc} = \frac{1}{C} \cdot \begin{bmatrix} d_d & d_q \end{bmatrix} \cdot \begin{bmatrix} \bar{i}_d \\ \bar{i}_q \end{bmatrix} - \frac{\bar{v}_{dc}}{RC} \tag{5.3}$$

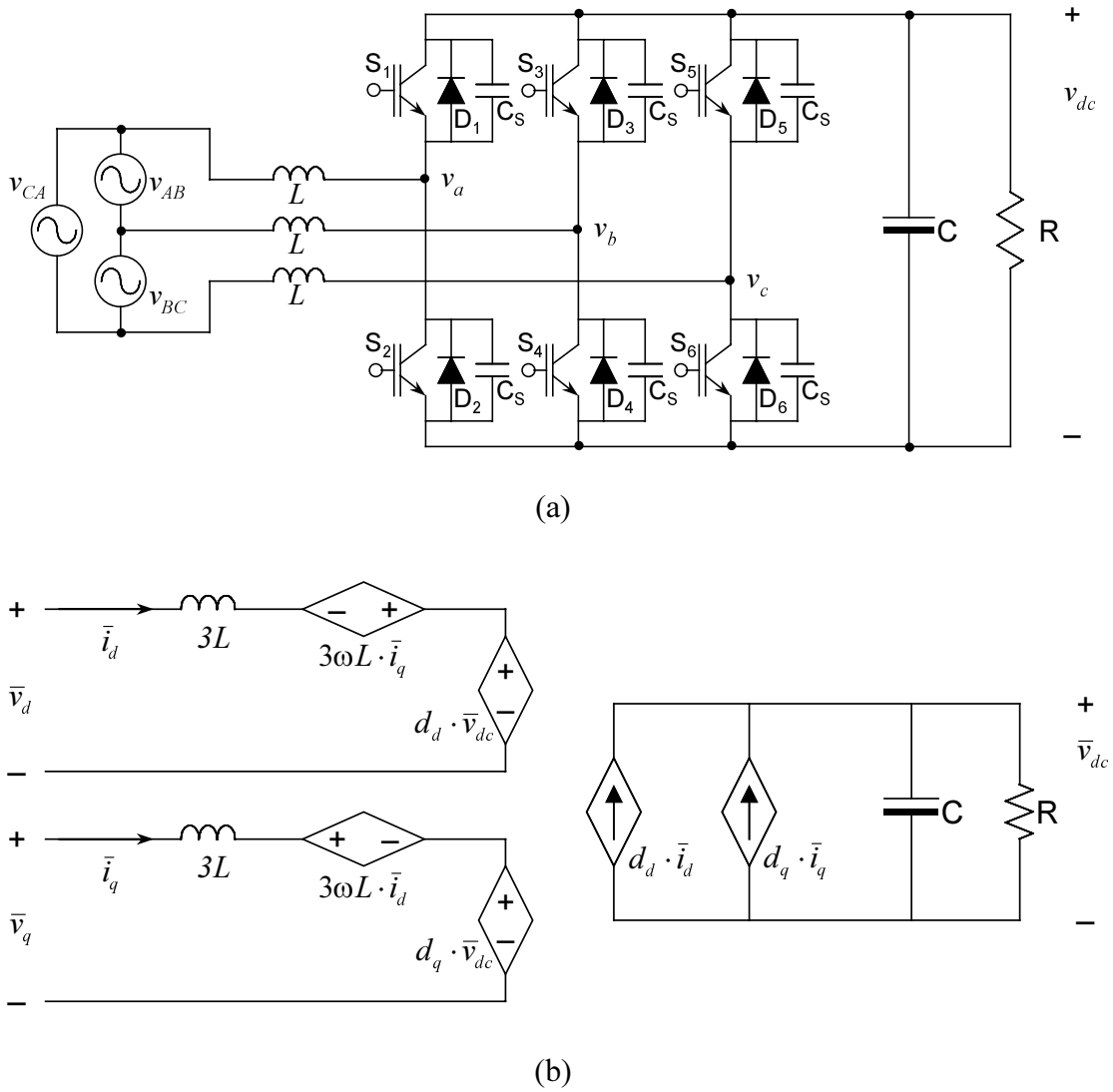


Figure 5.1 Three-phase boost rectifier and its average model:

(a) Power stage of three-phase boost rectifier, and

(b) Average model on *dq*-coordinate system.

Figure 5.2 (a) shows the power stage of a three-phase voltage-source inverter, and Figure 5.2 (b) shows the average model of the inverter on *dq*-coordinates. Equations (5.4), (5.5), and (5.6) describe the state equations of the model:

$$\frac{d}{dt}\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}=\frac{1}{3L}\cdot\begin{bmatrix}d_d\\ d_q\end{bmatrix}\cdot\bar{v}_{dc}-\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\frac{1}{3L}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix} \tag{5.4}$$

$$\frac{d}{dt}\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix}=\frac{1}{C}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix}-\frac{1}{RC}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix} \tag{5.5}$$

$$\bar{i}_{dc}=\begin{bmatrix}d_d & d_q\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}. \tag{5.6}$$

In addition to Figures 5.1 (b) and 5.2 (b), Equations (5.2)–(5.6) will be used for the average modeling of the ZVT converter with inductor feedback, as baseline models and their state equations.

5.2.2 Timing Control Schemes of ZVT Operations

There have been several kinds of timing control schemes for ZVT operations, which can be classified as either fixed-timing control or variable-timing control.

A. Fixed-Timing Control Schemes

The fixed-timing control schemes generate identical auxiliary gate signals, and maintain a constant dead time, as well. Figure 5.3 (a) shows an example of the fixed-timing control. After delay time (T_{delay}) is passed from the rising edge of original signal, the signal for a bottom main switch (S_2) becomes low (inactive), and the signal for a corresponding auxiliary switch (S_{X1}) becomes high (active). After T_{comm} from t_1, the signal for a top main switch becomes high. The auxiliary switch signal remains high during T_{aux}. All of the timing values (T_{delay}, T_{comm} and T_{aux}) are identical for any situation. The values are designed for maximum current conditions, and most of the multi-phase ZVT topologies cannot provide zero-voltage conditions for the main switches. Therefore, the voltage across the main switch might bounce back to some potential levels for most current levels. Since the timing schemes do not require any feedback, they are attractive in either low-cost or small snubber capacitance converter applications.

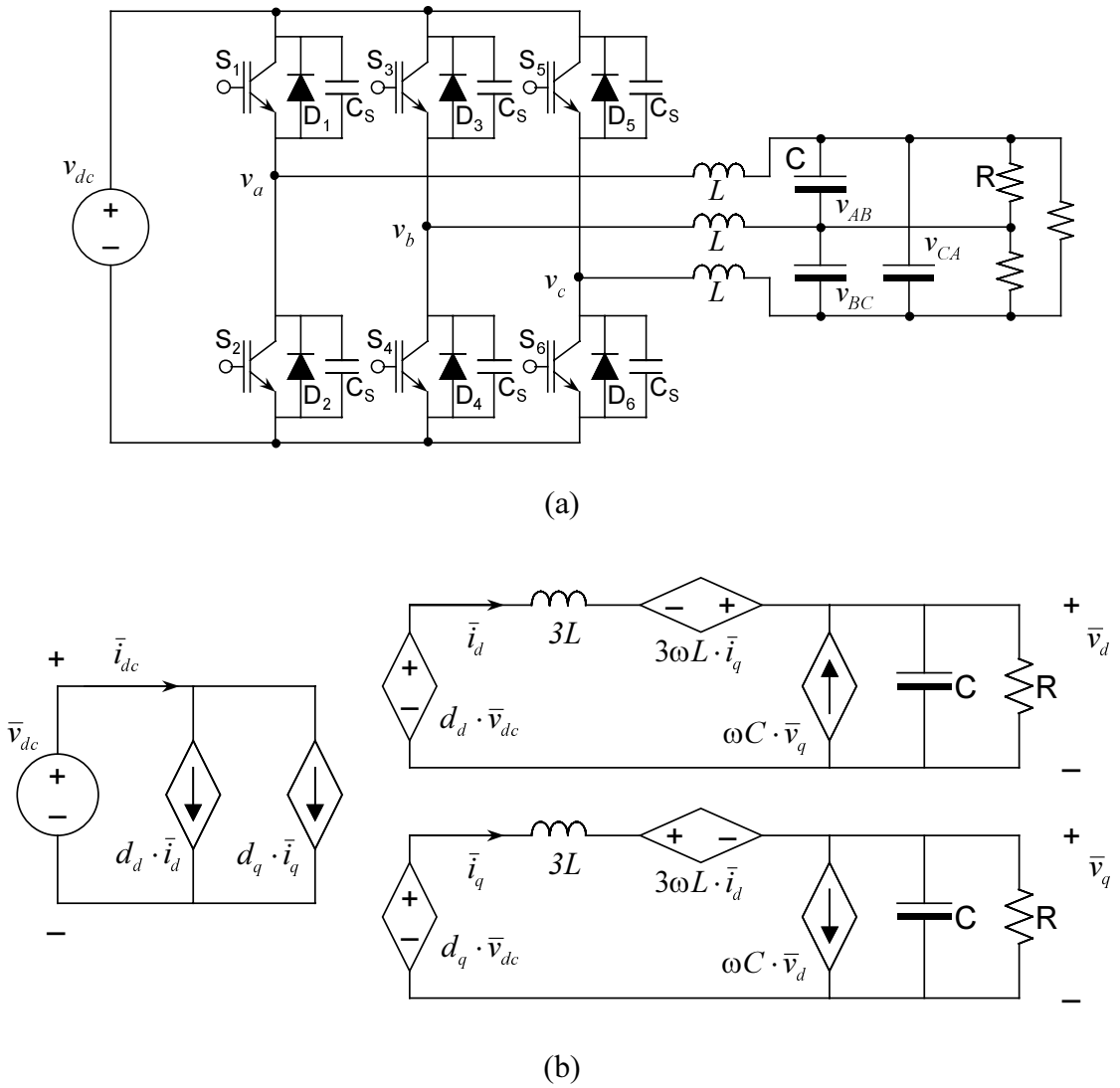


Figure 5.2 Three-phase voltage-source inverter and its average model:

(a) Power stage of three-phase voltage-source inverter, and

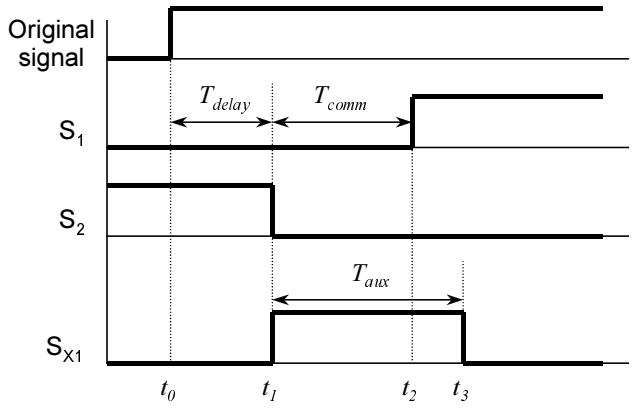
(b) Average model on *dq*-coordinate system.

B. Variable-Timing Control Schemes

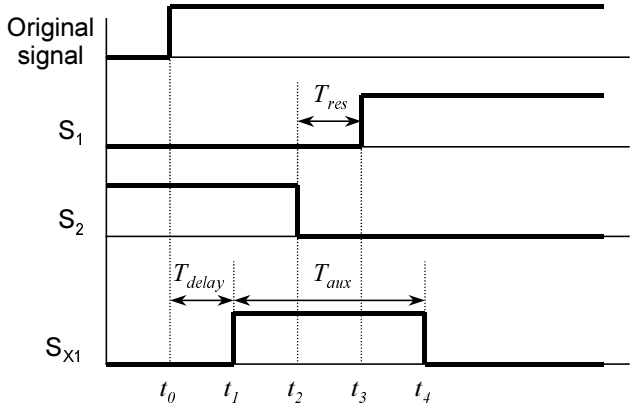
In medium- or high-power applications, it is generally preferable for converters to have snubber capacitance large enough to reduce switching losses. Although most multi-phase ZVT topologies can provide zero-voltage conditions for the main switches, the voltage across main switch bounces back to some potential levels. Therefore, a ZVT converter using a snubber capacitance of several hundred nF should turn on its main switches before the bounce-back condition. Otherwise, the converter suffers from the large discharging current of the snubber capacitors. To guarantee zero-voltage turn-on commutations, the variable-timing control schemes have been proposed.

Figure 5.3 (b) shows an example of the variable-timing control scheme (VTC 1). After delay time (T_{delay}) is passed from the rising edge of the original signal, the signal for a corresponding auxiliary switch (S_{X1}) becomes high (active). The turn-off time (t_2) of the bottom main switch can be determined by using the sum of charging time (T_{ch}) and boost time (T_b), which are easily calculated from the load current and the boost current. Therefore, by adjusting the position of t_1 according to load current, commutation time (T_{res}) can be kept to half the resonant time of the resonant tank, regardless of the load current values. After constant T_{res} is passed, the signal for the top main switch becomes high. The auxiliary switch signal remains high during T_{aux}, which is the sum of the four timing values T_{ch}, T_b, T_{res} and T_{dis}. Eventually, the main switch can turn on with a zero-voltage condition, and the auxiliary switch can turn off with zero-current condition.

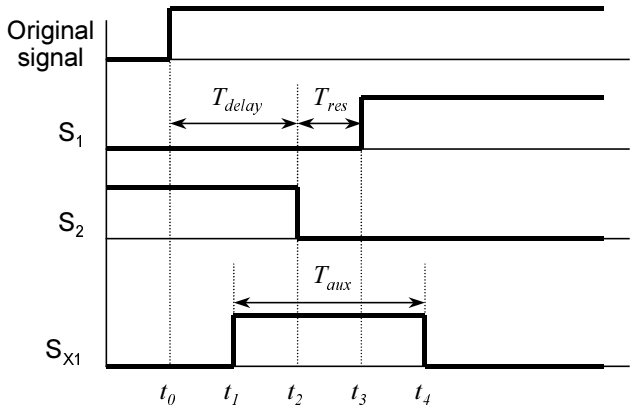
Figure 5.3 (c) shows another example of the variable-timing control scheme (VTC 2). After delay time (T_{delay}) is passed from the rising edge of the original signal, the signal for a bottom main switch (S_2) becomes low (inactive). The turn-on time (t_1) of an auxiliary switch can be determined by using the sum of T_{ch} and T_b. Because the auxiliary switch turns on before S_2 turns off, the constant T_{delay} should be larger than the sum of T_{ch} and T_b in any case. By adjusting the position of t_1 according to load current, commutation time (T_{res}) can be kept to half the resonant time of the resonant tank, regardless of the load current values. After T_{res} is passed, the signal for a top main switch becomes high. The auxiliary switch signal remains high during T_{aux}, which is the sum of the four timing values T_{ch}, T_b, T_{res} and T_{dis}. Eventually, the main switch can turn on with a zero-voltage condition, and the auxiliary switch can turn off with zero-current condition.



(a)



(b)



(c)

Figure 5.3 Descriptions of timing control schemes:

(a) Fixed-timing control scheme, (b) Variable-timing control 1 (VTC 1), and (c) Variable-timing control 2 (VTC 2).

Although the variable-timing control schemes achieve zero-voltage commutations in any case, they need the feedback information of load currents for calculating T_{ch} and T_{dis} in real time. In general, a real implemented sensing system always has its error boundary. Since high accuracy is expensive, the fixed-timing control schemes are preferred in either low-cost converters or converters that do not require large snubber capacitances. Recently, several research papers have proposed novel timing control schemes that do not require feedback about load currents [C20, C40]. Instead of boost current, the turns-ratio of coupled inductors can control the commutation time and even zero-voltage holding time of inductor-coupled ZVT topologies. The recent timing proposals take advantage of this characteristic. By using the auto detection of zero voltage, some timing schemes achieve good switching performance [C30, C40].

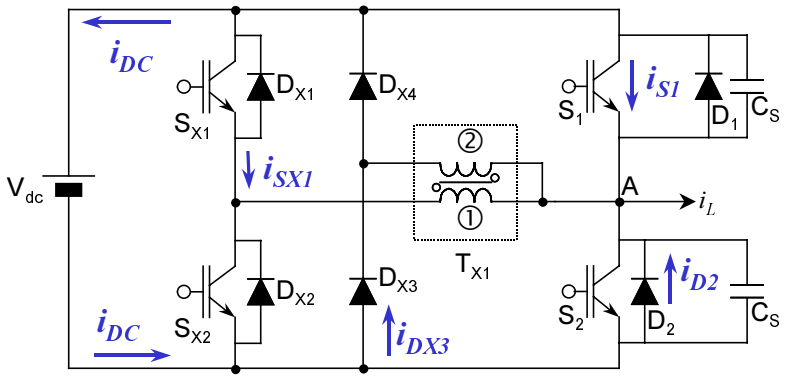
5.2.3 Effect of ZVT Operation in One Switching Cycle

Since the pulse generation method of each timing control scheme is different from those of other schemes, the influence of each timing control scheme on a converter is also different. Therefore, the selection of timing control scheme affects the average model of ZVT topologies. While the first method of variable-timing control schemes (VTC 1) puts charging time after delay time (T_{delay}), the second method (VTC 2) reverses the order. Therefore, the influence of VTC 1 might be more than that of VTC 2, and VTC 2 might be better than other schemes for minimizing the influence.

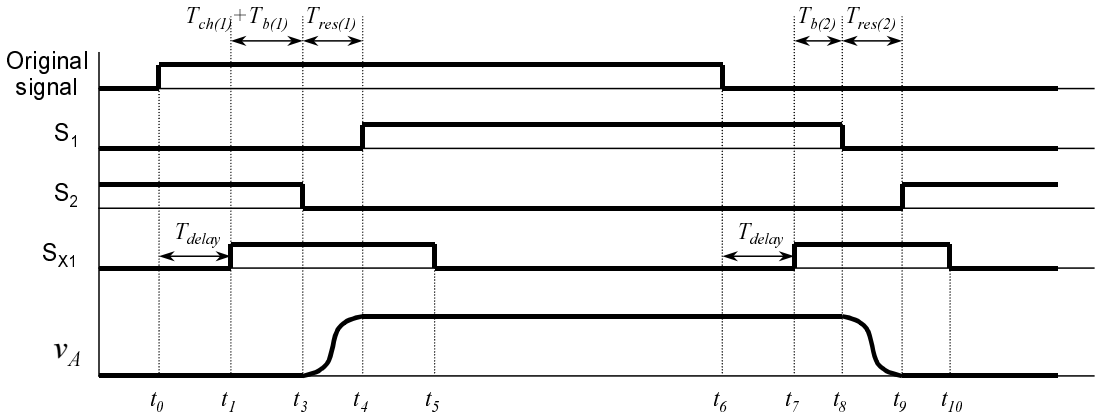
This section will first determine how ZVT operation affects the system equations of a converter using each of the variable-timing control schemes, and will then compare the results.

A. Timings of ZVT Operation in One Switching Cycle

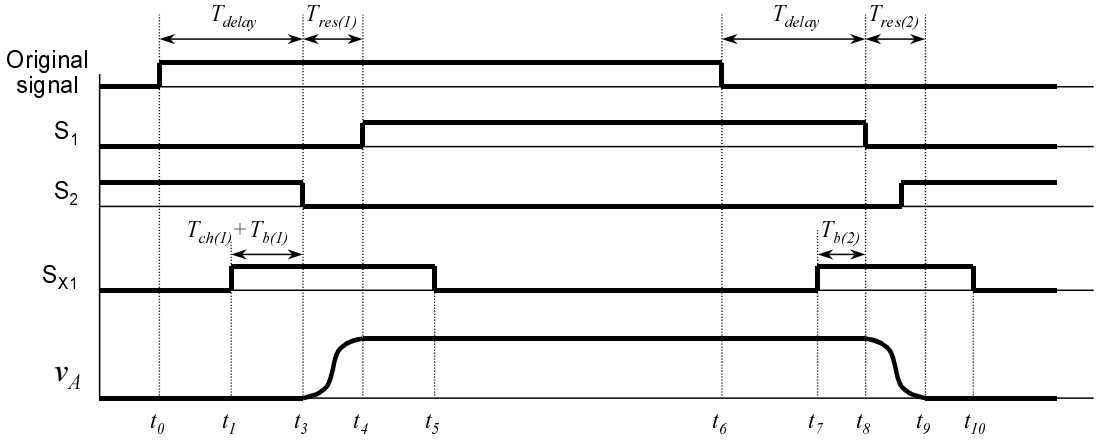
Figure 5.4 (a) shows the power stage of one phase of the ZVT converter with inductor feedback. Figures 5.4 (b) and (c) describe two kinds of timing charts in one switching cycle: (b) is with VTC 1 and (c) is with VTC 2. Assume that the turns-ratio of the coupled inductors is 1:1, and the load current flows out to the load. Except for triggering points, the timing value of each operation period of VTC 1 is the same as that of VTC 2.



(a)



(b)



(c)

Figure 5.4 Power stage and timing chart of the ZVT with inductor feedback:

(a) Power stage with current definitions,

(b) Timing chart of VTC 1 in one switching cycle, and

(c) Timing chart of VTC 2 in one switching cycle.

For the commutation from diode (D_2) to switch (S_1), the timing equations derived in Section 2.3 are converted to Equations (5.7)–(5.10) with the given assumptions:

$$T_{ch(1)} = L_p \cdot \frac{i_L}{V_{dc}} \tag{5.7}$$

$$T_{b(1)} = L_p \cdot \frac{I_b}{V_{dc}} \tag{5.8}$$

$$T_{res(1)} = 2\sqrt{L_p \cdot C_S} \cdot \arctan\left(\frac{I_{eq}}{I_b}\right) \tag{5.9}$$

$$T_{dis(1)} = L_p \cdot \frac{i_L}{V_{dc}} + L_p \cdot \frac{I_b}{V_{dc}} = T_{ch(1)} + T_{b(1)}\,, \tag{5.10}$$

$$\text{where} \quad Z_{eq} = \sqrt{\frac{L_p}{C_S}} \quad \text{and} \quad I_{eq} = \frac{V_{dc}}{Z_{eq}}\ .$$

Commutation from switch (S_1) to diode (D_2) does not require the operation of the auxiliary circuit, because this is a natural zero-voltage commutation. However, if the load current is too small to charge and discharge the snubber capacitors within an acceptable commutation time, the auxiliary circuit should help the commutation. The second commutation part of Figure 5.4 (b) describes this commutation, and Equations (5.11) – (5.13) show the timing equations of this commutation:

$$T_{b(2)} = L_p \cdot \frac{I'_b}{V_{dc}} \tag{5.11}$$

$$T_{res(2)} = 2\sqrt{L_p \cdot C_S} \cdot \arctan\left(\frac{I_{eq}}{I'_b}\right) \tag{5.12}$$

$$T_{dis(2)} = L_p \cdot \frac{I'_b}{V_{dc}} = T_{b(2)} \tag{5.13}$$

This operation is for commutating the switching status in acceptable length of time. In general, the commutation time of this operation ($T_{res(2)}$) is the same as the commutation time of an operation from diode to switch ($T_{res(1)}$). Therefore, comparing Equations (5.9) and (5.12) reveals that the boost current of this commutation (I'_b) has to be equal to I_b. A comparison of Equations (5.8) and (5.11) shows that two identical boost currents render

the boost times of the two cases identical. In general, the converter system has I_{limit} as a maximum current level that requires this operation.

B. Effect on AC Voltages

As shown in Figures 5.4 (b) and (c), the original signal is delayed as T_{delay} at not only the rising edge but also the falling edge, which is the same as shifting the original signal. Because this shifting does not cause any variation in duty ratio, the average model will not consider T_{delay}. The effect of delay, whether caused by digital implementation or by other reasons, was modeled in [E18].

- *Commutation from diode to switch*

The first commutation in Figure 5.4 (b) shows a commutation from diode to switch using VTC 1. For this commutation, the controller supposes that node A changes its potential at t_1. However, the node voltage remains constant during charging time ($T_{ch(1)}$) and boost time ($T_{b(1)}$) and is changed from t_3 during resonant time ($T_{res(1)}$) as:

$$\begin{aligned} v_C &= V_{dc} - \frac{V_{dc}}{2}\left[1+\cos(\omega_0 t)\right] + \frac{I_b}{2\cdot C_S\cdot\omega_0}\cdot\sin(\omega_0 t) \\ &= \frac{V_{dc}}{2}\left[1-\cos(\omega_0 t)\right] + \frac{I_b\cdot Z_{eq}}{2}\cdot\sin(\omega_0 t) \end{aligned} \tag{5.14}$$

This shape might be simplified with a straight line from zero to V_{dc} during $T_{res(1)}$. Considering the effect of the charging, boost and resonant periods, the variation of duty ratio (Δd_1) can be defined as:

$$\begin{aligned} \Delta d_1 &= d_{ch(1)} + d_{b(1)} + d_{res(1)} \\ &= \frac{T_{ch(1)}}{T_S} + \frac{T_{b(1)}}{T_S} + \frac{T_{res(1)}}{T_S}\cdot\frac{1}{2} \end{aligned} \tag{5.15}$$

where T_S : one switching period

With VTC 2, because both the charging time ($T_{ch(1)}$) and the boost time ($T_{b(1)}$) are included in T_{delay}, they do not cause any variation in the duty ratio, as shown in Figure 5.4 (c). The node voltage begins to change at the end of T_{delay}, moving from zero to V_{dc} during $T_{res(1)}$. Therefore, the variation of duty ratio (Δd_1) can be defined as:

$$\begin{aligned}\Delta d_1 &= d_{res(1)} \\ &= \frac{T_{res(1)}}{T_S} \cdot \frac{1}{2}\end{aligned} \tag{5.16}$$

- *Commutation from switch to diode*

As another case, if the load current is less than I_{limit}, the commutation from switch to diode needs the operation of the auxiliary circuit. The second commutations in both Figures 5.4 (b) and (c) show this kind of commutation. With VTC 1, the controller supposes that node A changes its potential at t_7. However, the node voltage remains constant during boost time ($T_{b(2)}$), and is changed from t_8 during resonant time ($T_{res(2)}$). The changing shape might be simplified with a straight line from V_{dc} to zero during T_{res}. Considering the effect of the boost and resonant periods, the variation of duty ratio (Δd_2) can be defined as Equation (5.17):

$$\begin{aligned}\Delta d_2 &= d_{b(2)} + d_{res(2)} \\ &= \frac{T_{b(2)}}{T_S} + \frac{T_{res(2)}}{T_S} \cdot \frac{1}{2}\end{aligned} \tag{5.17}$$

With VTC 2, because the boost time ($T_{b(2)}$) are included in T_{delay}, it does not cause any variation in the duty ratio, as shown in Figure 5.4 (c). The node voltage begins to change at the end of T_{delay}, moving from V_{dc} to zero during $T_{res(2)}$. Therefore, the variation of duty ratio (Δd_2) can be defined as Equation (5.18):

$$\begin{aligned}\Delta d_2 &= d_{res(2)} \\ &= \frac{T_{res(2)}}{T_S} \cdot \frac{1}{2}\end{aligned} \tag{5.18}$$

- *Variation of AC voltages*

As shown in Figures 5.1 and 5.2, the AC voltages of a converter are related to the DC voltage as:

$$\bar{v}_a = d_a \cdot \bar{v}_{dc}, \quad \bar{v}_b = d_b \cdot \bar{v}_{dc}, \quad \bar{v}_c = d_c \cdot \bar{v}_{dc} \tag{5.19}$$

Therefore, the variation of duty ratio (Δd) changes the AC voltage as:

$$\bar{v} = d_{eff} \cdot \bar{v}_{dc} = (d + \Delta d) \cdot \bar{v}_{dc} \tag{5.20}$$

With VTC 1, when the load current is larger than I_{limit}, there is no variation in the duty ratio at the second commutation. Therefore, an original duty ratio (d) is reduced to an effective duty ratio (d_{eff}) by only Δd_1, as shown in Equation (5.21):

$$\begin{aligned} d_{eff} &= d - \Delta d_1 \\ &= d - \left(d_{ch(1)} + d_{b(1)} + d_{res(1)}\right) \\ &= \frac{T - \left(T_{ch(1)} + T_{b(1)} + \dfrac{T_{res(1)}}{2}\right)}{T_S} \end{aligned} \tag{5.21}$$

When the load current is less than I_{limit}, d is changed to d_{eff} by two factors: not only it is reduced by Δd_1, but also it is increased by Δd_2, as shown in Equation (5.22):

$$\begin{aligned} d_{eff} &= d - \Delta d_1 + \Delta d_2 \\ &= d - \left(d_{ch(1)} + d_{b(1)} + d_{res(1)}\right) + \left(d_{b(2)} + d_{res(2)}\right) \\ &= \frac{T - \left(T_{ch(1)} + T_{b(1)} - T_{b(2)} + \dfrac{T_{res(1)} - T_{res(2)}}{2}\right)}{T_S} \end{aligned} \tag{5.22}$$

As mentioned earlier, $T_{b(1)}$ is equal to $T_{b(2)}$, and $T_{res(1)}$ is equal to $T_{res(2)}$. These relations change Equation (5.22), as shown in Equation (5.23):

$$d_{eff} = \frac{T - T_{ch(1)}}{T_S} = d - d_{ch(1)} \tag{5.23}$$

Therefore, the variation of duty ratio (Δd) becomes the same as $-d_{ch(1)}$.

Equation (5.24) shows d_{eff} with VTC 2 when the load current is larger than I_{limit}:

$$\begin{aligned} d_{eff} &= d - \Delta d_1 \\ &= d - d_{res(1)} \\ &= \frac{T - \dfrac{T_{res(1)}}{2}}{T_S} \end{aligned} \tag{5.24}$$

Therefore, the variation of duty ratio (Δd) becomes the same as $-d_{res(1)}$.

When load current is less than I_{limit}, there is no variation in the duty ratio, because $T_{res(1)}$ is canceled by $T_{res(2)}$.

C. Effect on DC Current

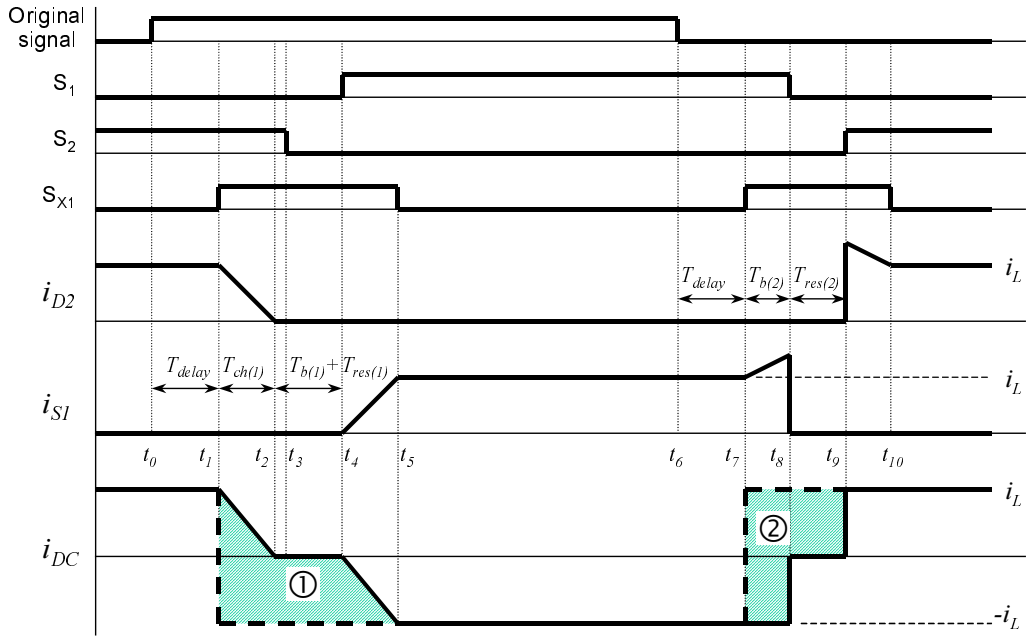
The variation of duty ratio by ZVT operation is already considered in AC voltages. This variation has another effect on the DC current. While a hard-switching converter immediately changes its DC current path at commutation points, a ZVT converter has a transition time for changing the DC current path. Therefore, the ZVT converter requires modification of the DC-side state equation.

Notably, the ZVT converter with inductor feedback has a special characteristic: Only half the auxiliary current affects the DC current.

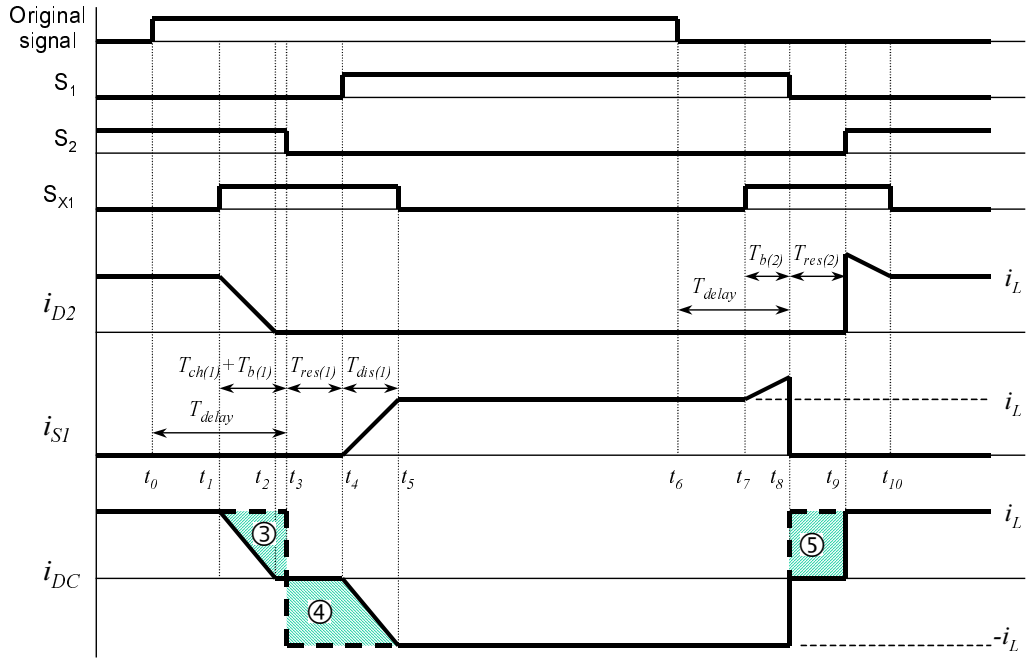
Figure 5.4 (a) shows the power stage of one phase of the ZVT converter with inductor feedback and some current definitions, as well. Figures 5.5 (a) and (b) show the defined current waveforms in one switching cycle with VTC 1 and VTC 2, respectively.

- *Commutation from diode to switch*

With VTC 1, DC current (i_{DC}) flows through D_2 before S_{X1} turns on, as shown in Figure 5.4 (a). The controller supposes that i_{DC} immediately changes its path (such as flowing through S_{X1}) when S_{X1} turns on at t_1. However, the transition of the i_{DC} path is somewhat complicated. When the main diode current (i_{D2}) linearly decreases to zero during charging time ($T_{ch(1)}$), half of i_{D2} flows through S_{X1} and another half flows through D_{X4}. Because i_{SX1} and i_{DX3} cancel each other and i_{D2} linearly decreases to zero, i_{DC} changes from i_L to zero during $T_{ch(1)}$. Half the sum of the load current and the boost current flows through S_{X1} during boost time ($T_{b(1)}$) and resonant time ($T_{res(1)}$). Because the current is canceled by another half the sum passing through D_{X4}, i_{DC} remains zero during both $T_{b(1)}$ and $T_{res(1)}$. While i_{SX1} and i_{DX4} cancel each other during discharging time ($T_{dis(1)}$), the main switch current (i_{S1}) increases to load current (i_L). Therefore, i_{DC} decreases from zero to $-i_L$ during $T_{dis(1)}$. The entire waveform of i_{DC} for this commutation is shown in Figure 5.5 (a). Shadow ① in this figure indicates the increased amount of i_{DC} with the ZVT converter, compared to i_{DC} with the hard-switching converter. Equation (5.25) describes the increase:



(a)



(b)

Figure 5.5 Current waveforms of the ZVT with inductor feedback in one switching cycle: (a) Using VTC 1, and (b) Using VTC 2.

$$\begin{aligned}\Delta i_{DC1} &= \frac{3}{2}\cdot i_L \cdot T_{ch(1)} + i_L \cdot \left(T_{b(1)} + T_{res(1)}\right) + \frac{1}{2}\cdot i_L \cdot T_{dis(1)} \\ &= \frac{i_L}{2}\cdot\left(3\cdot T_{ch(1)} + 2\cdot T_{b(1)} + 2\cdot T_{res(1)} + T_{dis(1)}\right)\end{aligned} \tag{5.25}$$

With VTC 2, because both the charging time ($T_{ch(1)}$) and the boost time ($T_{b(1)}$) are included in T_{delay}, shadow ③ in Figure 5.5 (b) decreases i_{DC} during both $T_{ch(1)}$ and $T_{b(1)}$, compared to the i_{DC} of the hard-switching converter. On the other hand, shadow ④ increases i_{DC} during both $T_{res(1)}$ and $T_{dis(1)}$, as shown in Figure 5.5 (b). Therefore, the difference of shadows ③ and ④ represents the changed amount of i_{DC} as:

$$\begin{aligned}\Delta i_{DC1} &= \left(i_L \cdot T_{res(1)} + \frac{1}{2}\cdot i_L \cdot T_{dis(1)}\right) - \left(\frac{1}{2}\cdot i_L \cdot T_{ch(1)} + i_L \cdot T_{b(1)}\right) \\ &= \frac{i_L}{2}\cdot\left(-T_{ch(1)} - 2\cdot T_{b(1)} + 2\cdot T_{res(1)} + T_{dis(1)}\right)\end{aligned} \tag{5.26}$$

- *Commutation from switch to diode*

If the load current is larger than I_{limit}, the commutation from switch to diode does not require the operation of the auxiliary circuit. The DC current path is immediately changed without any delay, which causes no variation in the DC current.

If the load current is less than I_{limit}, this commutation requires the operation of the auxiliary circuit. The second commutation in Figure 5.5 (a) shows this case with VTC 1. While boost current flows through both S_{X2} and D_{X3} during boost time ($T_{b(2)}$), load current (i_L) still flows through S_1. Therefore, i_{DC} stays at $-i_L$ during $T_{b(2)}$. Half the resonant current, including load current, flows through S_{X2}, and another half flows through D_{X3} during resonant time ($T_{res(2)}$). Because the currents cancel each other, i_{DC} remains zero during $T_{res(2)}$. At the end of the resonant period, all the load current has already passed through D_2. Therefore, i_{DC} stays at i_L during $T_{dis(2)}$. The entire waveform of i_{DC} for this commutation is shown in Figure 5.5 (a). Shadow ② in Figure 5.5 (a) decreases i_{DC} during both $T_{b(2)}$ and $T_{res(2)}$, compared to i_{DC} of the hard-switching converter. Equation (5.27) describes the variation in the DC current:

$$\begin{aligned}\Delta i_{DC2} &= 2\cdot i_L \cdot T_{b(2)} + i_L \cdot T_{res(2)} \\ &= i_L \cdot \left(2\cdot T_{b(2)} + T_{res(2)}\right)\end{aligned} \tag{5.27}$$

With VTC 2, because $T_{b(2)}$ is included in T_{delay}, it does not cause any variation in the DC current. Only shadow ⑤ decreases i_{DC} during $T_{res(2)}$, as shown in Figure 5.5 (b). Equation (5.28) describes the variation of DC current:

$$\Delta i_{DC2} = i_L \cdot T_{res(2)} \tag{5.28}$$

- *Variation of DC current*

With the average concept, Equation (5.29) denotes the average value of the DC current:

$$\bar{i}_{DC} = \frac{i_{DC}}{T_S} \tag{5.29}$$

where T_S : one switching period

Therefore, the average value of effective DC current is denoted with the variation of DC current as:

$$\begin{aligned} \bar{i}_{DC,eff} &= \bar{i}_{DC} + \frac{\Delta i_{DC}}{T_S} \\ &= \bar{i}_{DC} + \Delta \bar{i}_{DC} \end{aligned} \tag{5.30}$$

With VTC 1, when the load current is larger than I_{limit}, there is no variation in the DC current at the second commutation. Therefore, an original DC current ($\bar{i}_{DC}$) is increased to an effective DC current ($\bar{i}_{DC,eff}$) by only $\Delta \bar{i}_{DC1}$ as:

$$\begin{aligned} \bar{i}_{DC,eff} &= \bar{i}_{DC} + \Delta \bar{i}_{DC1} \\ &= \bar{i}_{DC} + \frac{i_L}{2} \cdot \frac{3 \cdot T_{ch(1)} + 2 \cdot T_{b(1)} + 2 \cdot T_{res(1)} + T_{dis(1)}}{T_S} \\ &= \bar{i}_{DC} + \frac{i_L}{2} \cdot \left(3 \cdot d_{ch(1)} + 2 \cdot d_{b(1)} + 2 \cdot d_{res(1)} + d_{dis(1)}\right) \end{aligned} \tag{5.31}$$

Therefore, the variation of DC current ($\Delta \bar{i}_{DC}$) becomes the same as $\Delta \bar{i}_{DC1}$.

When the load current is less than I_{limit}, $\bar{i}_{DC}$ is changed to $\bar{i}_{DC,eff}$ by two factors: not only is it increased by $\Delta \bar{i}_{DC1}$, but also it is decreased by $\Delta \bar{i}_{DC2}$ as:

$$\begin{aligned}
\bar{i}_{DC,eff} &= \bar{i}_{DC} + \Delta\bar{i}_{DC1} - \Delta\bar{i}_{DC2} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{3\cdot T_{ch(1)} + 2\cdot T_{b(1)} + 2\cdot T_{res(1)} + T_{dis(1)}}{T_S} - i_L\cdot\left(2\cdot T_{b(2)} + T_{res(2)}\right) \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{3\cdot T_{ch(1)} + \left(2\cdot T_{b(1)} - 4\cdot T_{b(2)}\right) + \left(2\cdot T_{res(1)} - 2\cdot T_{res(2)}\right) + T_{dis(1)}}{T_S} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{3\cdot T_{ch(1)} - 2\cdot T_{b(1)} + T_{dis(1)}}{T_S} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\left(3\cdot d_{ch(1)} - 2\cdot d_{b(1)} + d_{dis(1)}\right)
\end{aligned} \tag{5.32}$$

Equation (5.33) shows $\bar{i}_{DC,eff}$ with VTC 2 when the load current is larger than I_{limit}:

$$\begin{aligned}
\bar{i}_{DC,eff} &= \bar{i}_{DC} + \Delta\bar{i}_{DC1} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{-T_{ch(1)} - 2\cdot T_{b(1)} + 2\cdot T_{res(1)} + T_{dis(1)}}{T_S} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\left(-d_{ch(1)} - 2\cdot d_{b(1)} + 2\cdot d_{res(1)} + d_{dis(1)}\right)
\end{aligned} \tag{5.33}$$

Equation (5.34) shows $\bar{i}_{DC,eff}$ with VTC 2 when the load current is less than I_{limit}:

$$\begin{aligned}
\bar{i}_{DC,eff} &= \bar{i}_{DC} + \Delta\bar{i}_{DC1} - \Delta\bar{i}_{DC2} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{-T_{ch(1)} - 2\cdot T_{b(1)} + 2\cdot T_{res(1)} + T_{dis(1)}}{T_S} - i_L\cdot T_{res(2)} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{-T_{ch(1)} - 2\cdot T_{b(1)} + \left(2\cdot T_{res(1)} - 2\cdot T_{res(2)}\right) + T_{dis(1)}}{T_S} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\frac{-T_{ch(1)} - 2\cdot T_{b(1)} + T_{dis(1)}}{T_S} \\
&= \bar{i}_{DC} + \frac{i_L}{2}\cdot\left(-d_{ch(1)} - 2\cdot d_{b(1)} + d_{dis(1)}\right)
\end{aligned} \tag{5.34}$$

5.2.4 Effect of Space-Vector Modulation Schemes

The variations of duty ratio and DC current definitely affect the average model of a ZVT converter. However, these variations have an effect only when there is a commutation. Therefore, the influence is strongly related to the selection of SVM scheme.

Like either the sine-PWM or any SVM with six commutations in one switching period, most PWM schemes change the switching states of every phase [E40, E50]. Some SVM schemes have only four commutations in one switching period [E40, E50]. The ML SVM scheme reduces switching losses to at most half the other PWM schemes by selecting a zero SSV based on the load current condition [D40, D50]. Several research papers have compared the characteristics and performances of published PWM schemes [D40, D50]. For reducing switching losses, the ML SVM scheme is preferred. This section will reveal the influence of the SVM scheme on the average model of a ZVT converter.

A. Switching Patterns of Minimum-Loss SVM Scheme

For simplicity, assume that AC voltages and currents are in phase. Both the voltage reference vector ($\vec{v}_{ref}$) and load current vector ($\vec{i}_{Load}$) of a converter are located in the same sector of a vector space, as shown in Figure 5.6. Therefore, the ML SVM scheme does not commutate the phase that has the largest current among three phases.

Figure 5.7 shows the switching patterns generated by the ML SVM scheme in each sector. For example, when $\vec{v}_{ref}$ and $\vec{i}_{Load}$ are located in Sector XII or I, the current of phase A is larger than the other phases currents. Therefore, this phase does not commutate, as shown in Figure 5.7 (a). Among four commutations in both phases B and C, two commutations on the rising edges (bottom switch to top switch) are natural zero-voltage commutations. The other two commutations on the falling edges (top switch to bottom switch) need the operation of the auxiliary circuit for zero-voltage commutations, as circled in Figure 5.7 (a). Using the same method, the other sectors determine their switching patterns and points that require the operations of the auxiliary circuit, as shown in Figures 5.7 (b)–(f).

B. Constant and Current-dependant Parts in Variations

As an example, assume both the voltage reference vector and the load current vector are in either Sector XII or I. Figure 5.7 (a) shows the switching patterns for this case. Only the third and fourth commutations on phases B and C require the operations of the auxiliary circuit, as circled in the figure. Therefore, the duty ratios of both phases B and

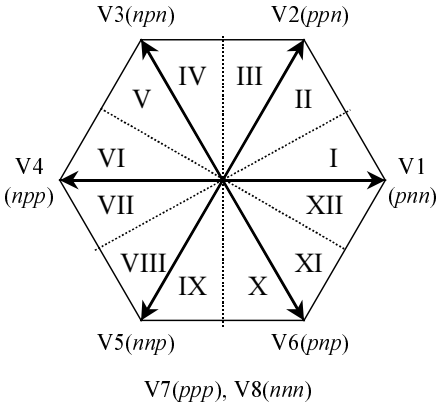


Figure 5.6 Vector space with switching state vectors.

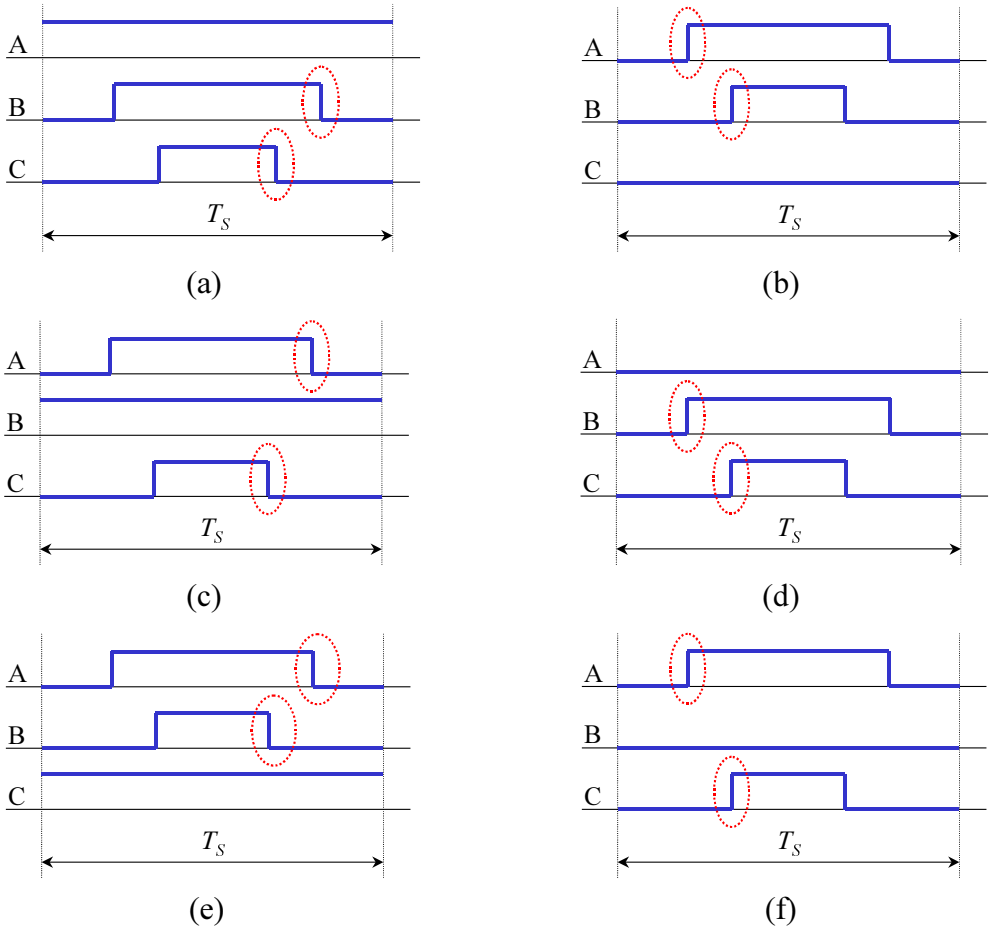


Figure 5.7 Switching patterns and positions of auxiliary operations:

(a) Sectors XII and I, (b) Sectors II and III, (c) Sectors IV and V,

(d) Sectors VI and VII, (e) Sectors VIII and IX, and (f) Sectors X and XI.

C are increased, while the DC current is reduced. From Equations (5.21), (5.24), (5.31), and (5.33), the variations of duty ratio and DC current are summarized here again as:

$$\text{With VTC 1, } \Delta d = \frac{T_{ch(1)} + T_{b(1)} + \dfrac{T_{res(1)}}{2}}{T_S} \tag{5.35}$$

$$\Delta \bar{i}_{DC} = -\frac{i_L}{2} \cdot \frac{3 \cdot T_{ch(1)} + 2 \cdot T_{b(1)} + 2 \cdot T_{res(1)} + T_{dis(1)}}{T_S} \tag{5.36}$$

$$\text{With VTC 2, } \Delta d = \frac{T_{res(1)}}{2 \cdot T_S} \tag{5.37}$$

$$\Delta \bar{i}_{DC} = -\frac{i_L}{2} \cdot \frac{-T_{ch(1)} - 2 \cdot T_{b(1)} + 2 \cdot T_{res(1)} + T_{dis(1)}}{T_S} \tag{5.38}$$

Both the boost time ($T_{b(1)}$) and resonant time ($T_{res(1)}$) are independent from load current, as shown in Equations (5.8) and (5.9). The charging time ($T_{ch(1)}$) and discharging time ($T_{dis(1)}$) are proportional to the load current, as shown in Equations (5.7) and (5.10). All of Equations (5.35)–(5.38) consist of these four timings. Equation (5.35) can be denoted using two parts as:

$$\begin{aligned}
\Delta d &= \frac{T_{ch(1)}}{T_S} + \frac{T_{b(1)} + \dfrac{T_{res(1)}}{2}}{T_S} \\
&= \frac{L_p}{T_S \cdot \bar{v}_{dc}} \cdot i_L + \left[\frac{L_p}{T_S \cdot \bar{v}_{dc}} \cdot I_b + \frac{\sqrt{L_p \cdot C_S}}{T_S} \cdot \arctan\left(\frac{I_{eq}}{I_b} \right) \right] \\
&= \frac{L_p}{T_S \cdot \bar{v}_{dc}} \cdot i_L + \left[\frac{L_p}{T_S \cdot \bar{v}_{dc}} \cdot I_b + \frac{\sqrt{L_p \cdot C_S}}{T_S} \cdot \arctan\left(\frac{\bar{v}_{dc}}{Z_{eq} \cdot I_b} \right) \right] \\
&\equiv D_1 + R_1
\end{aligned} \tag{5.39}$$

$$\text{where } \quad D_1 = \frac{L_p}{T_S \cdot \bar{v}_{dc}} \cdot i_L \quad \text{and}$$

$$R_1 = \frac{L_p}{T_S \cdot \bar{v}_{dc}} \cdot I_b + \frac{\sqrt{L_p \cdot C_S}}{T_S} \cdot \arctan\left(\frac{\bar{v}_{dc}}{I_{eq} \cdot I_b} \right)$$

While D_1 is proportional to load current (i_L), a term R_1 is always constant once the ZVT converter is designed. Equation (5.36) can also be divided into two parts as:

$$\begin{aligned}\Delta\bar{i}_{DC} &= -\frac{i_L}{2}\cdot\frac{3\cdot T_{ch(1)}+2\cdot T_{b(1)}+2\cdot T_{res(1)}+T_{dis(1)}}{T_S}\\ &= -i_L\cdot\left(\frac{2\cdot T_{ch(1)}}{T_S}+\frac{3\cdot T_{b(1)}+2\cdot T_{res(1)}}{2\cdot T_S}\right)\\ &\equiv i_L\cdot\left(-D_2-R_2\right)\end{aligned} \tag{5.40}$$

$$\text{where}\quad D_2=\frac{2\cdot T_{ch(1)}}{T_S}\ \text{and}\ R_2=\frac{3\cdot T_{b(1)}+2\cdot T_{res(1)}}{2\cdot T_S}$$

In conclusion, both variations of duty ratio and DC current using VTC 1 consist of two parts: constant part (R) and current-dependent part (D).

However, VTC 2 makes only the constant part of the variation in duty ratio, as shown in Equation (5.37). In general, discharging time ($T_{dis(1)}$) is the same as the sum of charging time ($T_{ch(1)}$) and boost time ($T_{b(1)}$). Therefore, Equation (5.38) can be simplified as:

$$\begin{aligned}\Delta\bar{i}_{DC} &= -\frac{i_L}{2}\cdot\frac{-T_{b(1)}+2\cdot T_{res(1)}}{T_S}\\ &= i_L\cdot\Delta d_{DC}\end{aligned} \tag{5.41}$$

$$\text{where}\ \Delta d_{DC}=\frac{T_{b(1)}-2\cdot T_{res(1)}}{2\cdot T_S}$$

The Δd_{DC} has only the constant part, which means the corresponding variation in the DC current using VTC 2 has only the constant part. Conclusively, VTC 2 produces only constant parts in both variations of duty ratio and DC current, as shown in Equation (5.37) and (5.41), respectively.

C. DQ Transformation of Constant Parts

This section transforms the constant part from *abc*-coordinates to *dq*-coordinates using a transformation matrix $T_{abc/dq}$ described in Equation (5.1).

The constant parts are different among Equations (5.35)–(5.38). However, for simplification, just define the constant part as R for deriving generalized *d*- and *q*-values. As mentioned in Section 5.2.4.B, assume both the voltage reference vector and the load current vector are in either Sector XII or I. Each of the commutations has an increased variation that is as high as R as:

$$\begin{aligned}\Delta d_a &= 0\\ \Delta d_b &= R\\ \Delta d_c &= R\end{aligned} \tag{5.42}$$

The line-to-line variables of the variations are necessary in order to match them to the matrix $T_{abc/dq}$ as:

$$\begin{aligned}\Delta d_{ab} &= \Delta d_a - \Delta d_b = 0 - R = -R\\ \Delta d_{bc} &= \Delta d_b - \Delta d_c = R - R = 0\\ \Delta d_{ca} &= \Delta d_c - \Delta d_a = R - 0 = R\end{aligned} \tag{5.43}$$

Using Equation (5.43) and $T_{abc/dq}$, the constant parts of the variations on the *dq*-coordinates are derived as:

$$\begin{aligned}\begin{bmatrix}\Delta d_d\\ \Delta d_q\end{bmatrix} &= T_{abc/dq}\cdot\begin{bmatrix}\Delta d_{ab}\\ \Delta d_{bc}\\ \Delta d_{ca}\end{bmatrix} = T_{abc/dq}\cdot\begin{bmatrix}-R\\ 0\\ R\end{bmatrix}\\ &= \sqrt{\frac{2}{3}}\cdot\begin{bmatrix}R\cdot\cos\left(\omega t+\frac{2}{3}\pi\right)-R\cdot\cos(\omega t)\\ -R\cdot\sin\left(\omega t+\frac{2}{3}\pi\right)+R\cdot\sin(\omega t)\end{bmatrix}\\ &= \begin{bmatrix}-\sqrt{2}\cdot R\cdot\sin\left(\omega t+\frac{1}{3}\pi\right)\\ -\sqrt{2}\cdot R\cdot\cos\left(\omega t+\frac{1}{3}\pi\right)\end{bmatrix}\end{aligned} \tag{5.44}$$

With the same method, the *d*- and *q*-values of the variations can be derived for the other sectors as:

$$\text{In either Sector II or III, } \begin{bmatrix}\Delta d_d\\ \Delta d_q\end{bmatrix} = \begin{bmatrix}-\sqrt{2}\cdot R\cdot\sin(\omega t)\\ -\sqrt{2}\cdot R\cdot\cos(\omega t)\end{bmatrix} \tag{5.45}$$

$$\text{In either Sector IV or V, } \begin{bmatrix}\Delta d_d\\ \Delta d_q\end{bmatrix} = \begin{bmatrix}-\sqrt{2}\cdot R\cdot\sin\left(\omega t-\frac{1}{3}\pi\right)\\ -\sqrt{2}\cdot R\cdot\cos\left(\omega t-\frac{1}{3}\pi\right)\end{bmatrix} \tag{5.46}$$

$$\text{In either Sector VI or VII, } \begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} = \begin{bmatrix} \sqrt{2} \cdot R \cdot \sin\left(\omega t + \frac{1}{3}\pi\right) \\ \sqrt{2} \cdot R \cdot \cos\left(\omega t + \frac{1}{3}\pi\right) \end{bmatrix} \tag{5.47}$$

$$\text{In either Sector VIII or IX, } \begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} = \begin{bmatrix} \sqrt{2} \cdot R \cdot \sin(\omega t) \\ \sqrt{2} \cdot R \cdot \cos(\omega t) \end{bmatrix} \tag{5.48}$$

$$\text{In either Sector X or XI, } \begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} = \begin{bmatrix} \sqrt{2} \cdot R \cdot \sin\left(\omega t - \frac{1}{3}\pi\right) \\ \sqrt{2} \cdot R \cdot \cos\left(\omega t - \frac{1}{3}\pi\right) \end{bmatrix} \tag{5.49}$$

As shown in Equations (5.44)–(5.49), Δd_d and Δd_q are time-varying with the factors of sin(ωt) and cos(ωt), respectively. Figure 5.8 (a) shows the shape of Δd_d with R = 1 in one fundamental period. It is periodic, having a period of 60°. Therefore, Δd_d must be averaged again in 60° in order to make an average model, which obtains $-1.17 \cdot R$ as the average value of Δd_d ($\Delta \bar{d}_d$). Figure 5.8 (b) shows the shape of Δd_q in one fundamental period. It is also periodic with a period of 60°. By averaging Δd_q in 60°, the average value of Δd_q ($\Delta \bar{d}_q$) becomes $-0.675 \cdot R$. Eventually, the *d*- and *q*-values of the variations become constant values in any sector as:

$$\begin{bmatrix} \Delta \bar{d}_d \\ \Delta \bar{d}_q \end{bmatrix} = -\begin{bmatrix} 1.17 \\ 0.675 \end{bmatrix} \cdot R \tag{5.50}$$

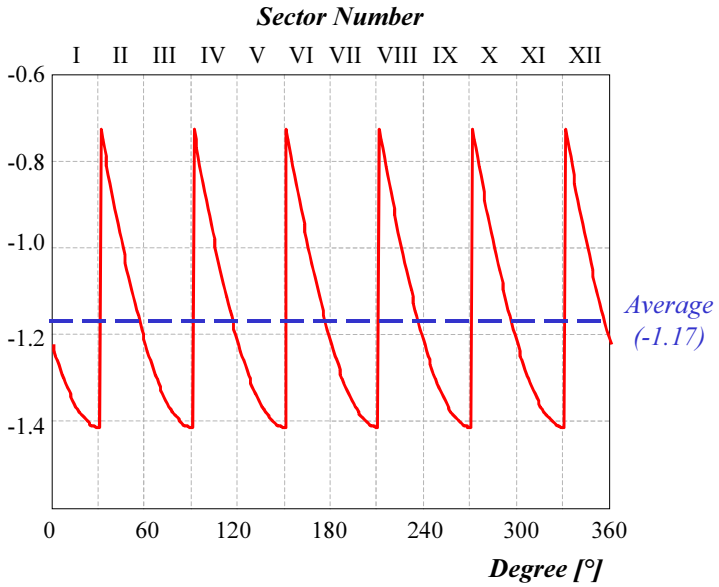
The averaging of the variables over 60° of *dq*-rotation period reduces the validity of the model to below 3-times the line frequency. Therefore, the conclusions above are only qualitative, and need further study.

D. DQ Transformation of Current-Dependent Parts

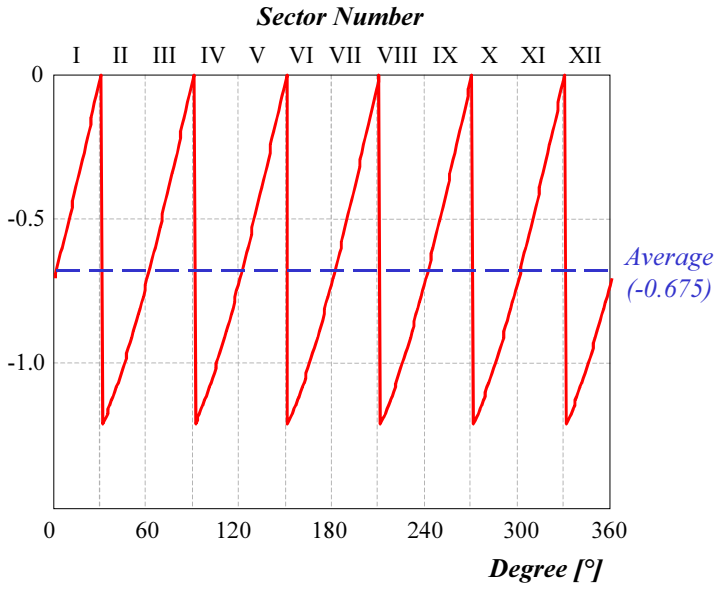
This section transforms the current-dependent part from *abc*-coordinates to *dq*-coordinates using a transformation matrix $T_{abc/dq}$ described in Equation (5.1).

Equation (5.39) has D_1 as a current-dependent part as:

$$D_1 = \frac{L_p}{T_S \cdot V_{dc}} \cdot i_L \tag{5.51}$$



(a)



(b)

Figure 5.8 Shapes of Δd_d and Δd_q in one fundamental period: (a) Δd_d and (b) Δd_q.

As mentioned in Section 5.2.4.B, assume both the voltage reference vector and the load current vector are in either Sector XII or I. Therefore, each of the commutations has an increased variation that is as high as D_1 as:

$$\Delta d_a = 0, \;\; \Delta d_b = D_1, \text{ and } \Delta d_c = D_1 \tag{5.52}$$

The line-to-line variables of the variations are shown in:

$$\begin{aligned}
\Delta d_{ab} &= \Delta d_a - \Delta d_b = -\frac{L_p}{V_{dc} \cdot T_S} \cdot i_b \\
\Delta d_{bc} &= \Delta d_b - \Delta d_c = \frac{L_p}{V_{dc} \cdot T_S} \cdot (i_b - i_c) \\
\Delta d_{ca} &= \Delta d_c - \Delta d_a = \frac{L_p}{V_{dc} \cdot T_S} \cdot i_c
\end{aligned} \tag{5.53}$$

Using Equation (5.53) and $T_{abc/dq}$, the current-dependent part of the variation on the dq-coordinates are derived as:

$$\begin{aligned}
\begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} &= T_{abc/dq} \cdot \begin{bmatrix} \Delta d_{ab} \\ \Delta d_{bc} \\ \Delta d_{ca} \end{bmatrix} \\
&= T_{abc/dq} \cdot \frac{L_p}{V_{dc} \cdot T_S} \begin{bmatrix} -i_b \\ i_b - i_c \\ i_c \end{bmatrix}
\end{aligned} \tag{5.54}$$

From the assumption of balanced loads, Equation (5.54) can be rewritten as:

$$\begin{aligned}
\begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} &= T_{abc/dq} \cdot \frac{L_p}{V_{dc} \cdot T_S} \begin{bmatrix} i_a + i_c \\ i_b - i_c \\ i_c \end{bmatrix} \\
&= T_{abc/dq} \cdot \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + T_{abc/dq} \cdot \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_c \\ -i_c \\ 0 \end{bmatrix} \\
&= \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + T_{abc/dq} \cdot \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_c \\ -i_c \\ 0 \end{bmatrix} \\
&\equiv f_1 + f_2
\end{aligned} \tag{5.55}$$

The first term (f_1) of Equation (5.55) is the function of i_d and i_q. The second term (f_2) can be rewritten as:

$$\begin{aligned} f_2 &= \sqrt{\frac{2}{3}} \cdot \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_c \cdot \cos(\omega t) - i_c \cdot \cos\left(\omega t - \frac{2}{3}\pi\right) \\ -i_c \cdot \sin(\omega t) + i_c \cdot \sin\left(\omega t - \frac{2}{3}\pi\right) \end{bmatrix} \\ &= -\frac{\sqrt{2} \cdot L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} \sin\left(\omega t - \frac{\pi}{3}\right) \\ \cos\left(\omega t - \frac{\pi}{3}\right) \end{bmatrix} \cdot i_c \end{aligned} \tag{5.56}$$

Eventually, Equation (5.55) is rewritten using Equation (5.56) as:

$$\begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} = \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \frac{\sqrt{2} \cdot L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} \sin\left(\omega t - \frac{\pi}{3}\right) \\ \cos\left(\omega t - \frac{\pi}{3}\right) \end{bmatrix} \cdot i_c \tag{5.57}$$

This equation is still time-varying, so it should be averaged again in this period. The average value of $\sin\left(\omega t - \frac{\pi}{3}\right)$ from $-\frac{\pi}{6}$ to $\frac{\pi}{6}$ is $-\frac{3\sqrt{3}}{2\pi}$. The average value of $\cos\left(\omega t - \frac{\pi}{3}\right)$ from $-\frac{\pi}{6}$ to $\frac{\pi}{6}$ is $\frac{3}{2\pi}$. Therefore, the average of Equation (5.57) is denoted using these values as:

$$\begin{bmatrix} \Delta \bar{d}_d \\ \Delta \bar{d}_q \end{bmatrix} = \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \frac{\sqrt{2} \cdot L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} -\frac{3\sqrt{3}}{2\pi} \\ \frac{3}{2\pi} \end{bmatrix} \cdot \bar{i}_c \tag{5.58}$$

Using the same method, the *d*- and *q*-values for the variations can be derived in the other sectors. If both voltage reference and current vectors are in either Sector X or XI, Equations (5.59) and (5.60) show one set of *d*- and *q*-values and its corresponding average values, respectively:

$$\begin{bmatrix} \Delta d_d \\ \Delta d_q \end{bmatrix} = \frac{L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{\sqrt{2} \cdot L_p}{V_{dc} \cdot T_S} \cdot \begin{bmatrix} \sin(\omega t) \\ \cos(\omega t) \end{bmatrix} \cdot i_a \tag{5.59}$$

$$\begin{bmatrix} \Delta\bar{d}_d \\ \Delta\bar{d}_q \end{bmatrix} = \frac{L_p}{V_{dc}\cdot T_S}\cdot\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{\sqrt{2}\cdot L_p}{V_{dc}\cdot T_S}\cdot\begin{bmatrix} -\frac{3\sqrt{3}}{2\pi} \\ \frac{3}{2\pi} \end{bmatrix}\cdot\bar{i}_a \tag{5.60}$$

E. Steady-State Values of Current-Dependent Parts on DQ-Coordinates

Equations (5.57) and (5.59) describe the variation of duty ratio on the *dq*-coordinates, including both transient and steady states. For small-signal analysis, assume that the three-phase currents are balanced sinusoidal waveforms in steady state as:

$$\begin{aligned} i_a &= A\cdot\cos(\omega t) \\ i_b &= A\cdot\cos\left(\omega t - \frac{2}{3}\pi\right) \\ i_c &= A\cdot\cos\left(\omega t + \frac{2}{3}\pi\right) \end{aligned} \tag{5.61}$$

where A : amplitude of sinusoidal waveform

Using these currents, the two terms in Equation (5.57) can be denoted as:

$$\begin{aligned} \begin{bmatrix} i_d \\ i_q \end{bmatrix} &= T_{abc/dq}\cdot\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}}\cdot\begin{bmatrix} \frac{3}{2}\cdot A \\ 0 \end{bmatrix} \\ &= \begin{bmatrix} \sqrt{\frac{3}{2}}\cdot A \\ 0 \end{bmatrix} \end{aligned} \tag{5.62}$$

$$\begin{aligned} \begin{bmatrix} \sin\left(\omega t - \frac{\pi}{3}\right) \\ \cos\left(\omega t - \frac{\pi}{3}\right) \end{bmatrix}\cdot i_c &= \begin{bmatrix} \sin\left(\omega t - \frac{\pi}{3}\right) \\ \cos\left(\omega t - \frac{\pi}{3}\right) \end{bmatrix}\cdot A\cdot\cos\left(\omega t + \frac{2}{3}\pi\right) \\ &= -A\cdot\begin{bmatrix} \frac{1}{2}\cdot\sin\left(2\omega t - \frac{2}{3}\pi\right) \\ \frac{1}{2} + \frac{1}{2}\cdot\cos\left(2\omega t - \frac{2}{3}\pi\right) \end{bmatrix} \end{aligned} \tag{5.63}$$

Inserting Equations (5.62) and (5.63) into (5.57) makes the variations of duty ratio in steady state as:

$$\begin{aligned}\begin{bmatrix}\Delta d_d\\ \Delta d_q\end{bmatrix} &= \frac{L_p}{V_{dc}\cdot T_S}\cdot\begin{bmatrix}\sqrt{\frac{3}{2}}\cdot A\\ 0\end{bmatrix} + \frac{\sqrt{2}\cdot L_p}{V_{dc}\cdot T_S}\cdot A\cdot\begin{bmatrix}\frac{1}{2}\cdot\sin\left(2\omega t-\frac{2}{3}\pi\right)\\ \frac{1}{2}+\frac{1}{2}\cdot\cos\left(2\omega t-\frac{2}{3}\pi\right)\end{bmatrix}\\ &= \frac{L_p\cdot A}{\sqrt{2}\cdot V_{dc}\cdot T_S}\cdot\begin{bmatrix}\sqrt{3}+\sin\left(2\omega t-\frac{2}{3}\pi\right)\\ 1+\cos\left(2\omega t-\frac{2}{3}\pi\right)\end{bmatrix}\end{aligned} \tag{5.64}$$

When both voltage reference and current vectors are in either Sector X or XI, Equation (5.59) is also rewritten for steady state as:

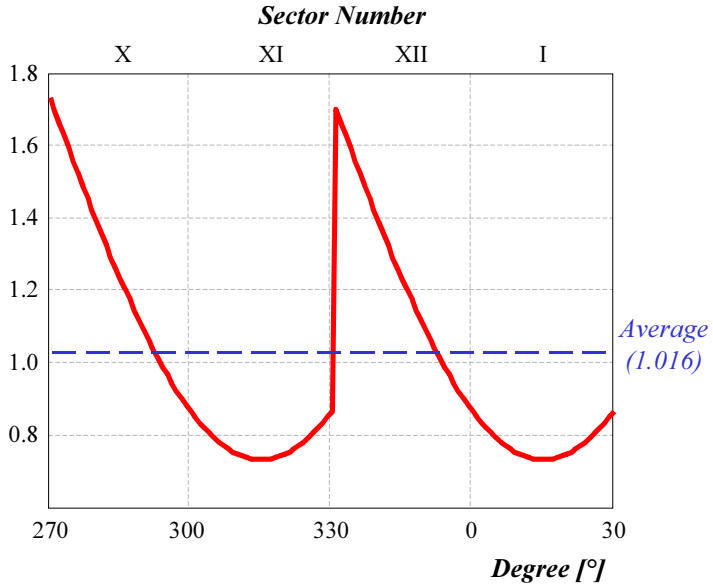
$$\begin{bmatrix}\Delta d_d\\ \Delta d_q\end{bmatrix} = \frac{L_p\cdot A}{\sqrt{2}\cdot V_{dc}\cdot T_S}\cdot\begin{bmatrix}\sqrt{3}+\sin(2\omega t)\\ 1+\cos(2\omega t)\end{bmatrix} = K\cdot\begin{bmatrix}\sqrt{3}+\sin(2\omega t)\\ 1+\cos(2\omega t)\end{bmatrix} \tag{5.65}$$

As shown in Equations (5.64) and (5.65), Δd_d and Δd_q are time-varying with the factors of sin(ωt) and cos(ωt), respectively. Figure 5.9 (a) shows the shape of Δd_d from sectors X to I, when the constant term $\frac{L_p\cdot A}{\sqrt{2}\cdot V_{dc}\cdot T_S}$ is one. It is periodic, having a period of 60°. Therefore, Δd_d must be averaged again in 60° in order to develop an average model, which obtains 1.016 as the average value of Δd_d ($\Delta\bar{d}_d$). Figure 5.9 (b) shows the shape of Δd_q from sectors X to I. It is also periodic with a period of 60°. By averaging Δd_q in 60°, the average value of Δd_q ($\Delta\bar{d}_q$) becomes 0.587. Eventually, the *d*- and *q*-values of the variations become constant values in any sector as:

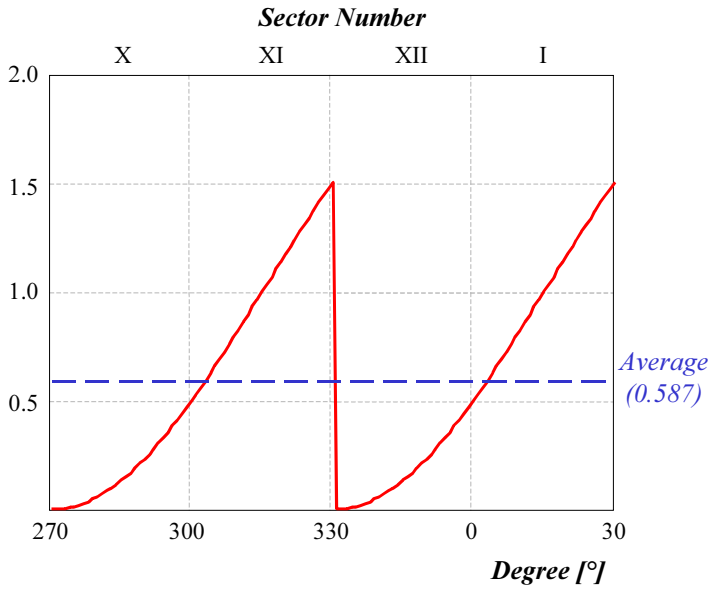
$$\begin{bmatrix}\Delta\bar{d}\\ \Delta\bar{q}\end{bmatrix} = \frac{L_p\cdot A}{\sqrt{2}\cdot V_{dc}\cdot T_S}\cdot\begin{bmatrix}1.016\\ 0.587\end{bmatrix} \tag{5.66}$$

As mentioned in Section 5.2.4.C, the averaging of the variables over 60° of *dq*-rotation period reduces the validity of the model to below 3-times the line frequency. Therefore, the conclusions above are only qualitative, and need further study.

In addition, assumption (5.61) makes the model valid only around the steady state. Therefore, the modeling is not large-signal average but small-signal average.



(a)



(b)

Figure 5.9 Shapes of Δd_d and Δd_q in four sectors: (a) Δd_d and (b) Δd_q.

5.3 AVERAGE MODEL OF THREE-PHASE ZVT CONVERTER WITH INDUCTOR FEEDBACK

As investigated in Section 5.2, both SVM schemes and zero-voltage operation change the duty ratios of the main switch signals. The variations of duty ratio affect both AC voltages and DC current. Through investigation, this section finally develops the average models of the ZVT converters with inductor feedback for both PFC rectifier and inverter applications.

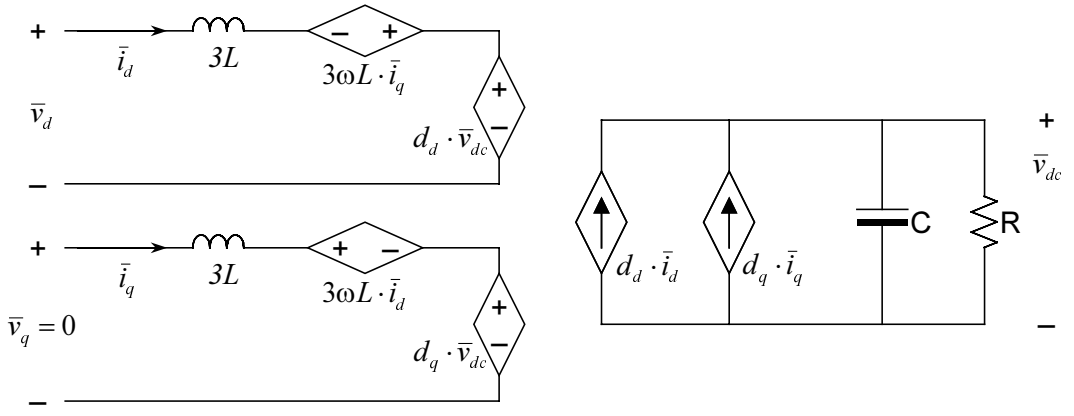
Since average models developed in this section use the results of Sections 5.2.4.C and 5.2.4.D, the models are valid below 3-times the line frequency. In addition, assumption (5.61) makes the model valid only around the steady state. Therefore, the conclusions in this section are only qualitative in the steady state, and need further study.

5.3.1 Average Model of ZVT PFC Rectifier

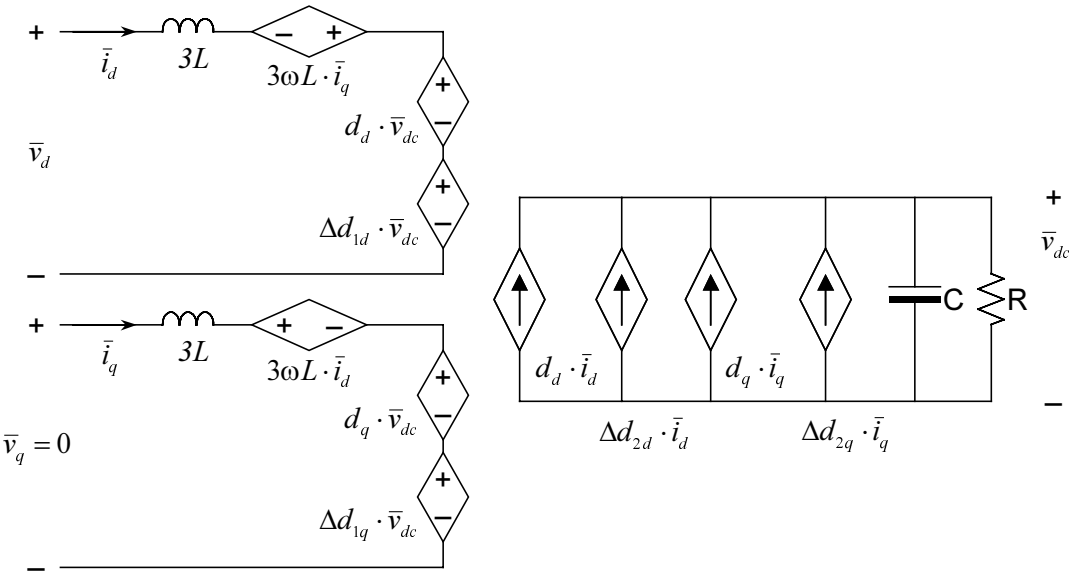
Equations (5.2) and (5.3) describe the average model of a three-phase hard-switching rectifier, and Figure 5.1 (b) illustrates the average model. By using PFC control, the q-axis voltage (v_q) becomes zero. Figure 5.10 (a) shows the average model of the PFC rectifier. Considering both the constant and current-dependent parts together, assume that the PFC rectifier uses VTC 1 as a timing control scheme.

From earlier investigation, it is already known that there are two variations in the ZVT rectifier: one at its AC voltages and one at its DC current. Therefore, the average model of a ZVT rectifier can be made by inserting these variations into the average model of a hard-switching rectifier, as shown in Figure 5.10 (b). Equations (5.67) and (5.68) describe the state equations of the ZVT rectifier:

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix} &= \frac{1}{3L}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix} - \begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix} - \frac{1}{3L}\cdot\begin{bmatrix}d_d+\Delta d_{1d}\\ d_q+\Delta d_{1q}\end{bmatrix}\cdot\bar{v}_{dc}\\ &= \frac{1}{3L}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix} - \begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix} - \frac{1}{3L}\cdot\begin{bmatrix}d_d\\ d_q\end{bmatrix}\cdot\bar{v}_{dc} - \frac{1}{3L}\cdot\begin{bmatrix}\Delta d_{1d}\\ \Delta d_{1q}\end{bmatrix}\cdot\bar{v}_{dc}\end{aligned} \tag{5.67}$$



(a)



(b)

Figure 5.10 Average models of three-phase PFC boost rectifiers:

(a) Hard-switching rectifier, and

(b) ZVT rectifier with inductor feedback.

$$\begin{aligned}\frac{d}{dt}\bar{v}_{dc} &= \frac{1}{C}\cdot\begin{bmatrix}d_d+\Delta d_{2d} & d_q+\Delta d_{2q}\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\frac{\bar{v}_{dc}}{RC}\\ &= \frac{1}{C}\cdot\begin{bmatrix}d_d & d_q\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}+\frac{1}{C}\cdot\begin{bmatrix}\Delta d_{2d} & \Delta d_{2q}\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\frac{\bar{v}_{dc}}{RC}\end{aligned} \tag{5.68}$$

Four variations (Δd_{1d}, Δd_{1q}, Δd_{2d}, and Δd_{2q}) are derived, as follows.

A. Items inserted on AC Side

As shown in Equation (5.39), Δd_1 consists of two parts: R_1 and D_1. A constant term R in *abc*-coordinates is changed to R_{dq} in *dq*-coordinates, as shown in Equation (5.50). By using Equation (5.50), R_1 can be changed to $R_{1(dq)}$ in *dq*-coordinates as:

$$\begin{aligned}R_{1(dq)} &= -R_1\cdot\begin{bmatrix}1.17\\ 0.675\end{bmatrix}\\ &= -\left[\frac{L_p}{T_S\cdot\bar{v}_{dc}}\cdot I_b+\frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\arctan\left(\frac{\bar{v}_{dc}}{Z_{eq}\cdot I_b}\right)\right]\cdot\begin{bmatrix}1.17\\ 0.675\end{bmatrix}\end{aligned} \tag{5.69}$$

In steady state with three-phase sinusoidal currents whose total amplitude is A, a current-dependent term D in *abc*-coordinates is changed to D_{dq} in *dq*-coordinates, as shown in Equation (5.65). Therefore, Equation (5.70) can describe D_1 in *dq*-coordinates:

$$D_{1(dq)} = \frac{L_p\cdot A}{\sqrt{2}\cdot T_S\cdot\bar{v}_{dc}}\cdot\begin{bmatrix}1.016\\ 0.587\end{bmatrix} \tag{5.70}$$

Now, Δd_1 is the negative sum of Equations (5.69) and (5.70), which consists of Δd_{1d} and Δd_{1q} as:

$$\begin{aligned}\Delta d_1 &= \begin{bmatrix}\Delta d_{1d}\\ \Delta d_{1q}\end{bmatrix}\\ &= R_{1(dq)}+D_{1(dq)}\\ &= -\left[\frac{L_p}{T_S\cdot\bar{v}_{dc}}\cdot I_b+\frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\arctan\left(\frac{\bar{v}_{dc}}{Z_{eq}\cdot I_b}\right)\right]\cdot\begin{bmatrix}1.17\\ 0.675\end{bmatrix}\\ &\quad+\frac{L_p\cdot A}{\sqrt{2}\cdot T_S\cdot\bar{v}_{dc}}\cdot\begin{bmatrix}1.016\\ 0.587\end{bmatrix}\end{aligned} \tag{5.71}$$

B. Items inserted on DC Side

As shown in Equation (5.40), Δd_2 consists of two parts: R_2 and D_2. By using Equations (5.50), Equation (5.72) describes R_2 in dq-coordinates:

$$\begin{aligned} R_{2(dq)} &= -\frac{3\cdot T_{b(1)} + 2\cdot T_{res(1)}}{2\cdot T_S}\cdot\begin{bmatrix}1.17\\0.675\end{bmatrix} \\ &= -\left[\frac{3}{2}\cdot\frac{L_p}{T_S\cdot\overline{v}_{dc}}\cdot I_b + \frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\arctan\left(\frac{\overline{v}_{dc}}{Z_{eq}\cdot I_b}\right)\right]\cdot\begin{bmatrix}1.17\\0.675\end{bmatrix} \end{aligned} \tag{5.72}$$

In steady state with three-phase sinusoidal currents whose total amplitude is A, by using Equation (5.66), Equation (5.73) can describe D_2 in dq-coordinates:

$$\begin{aligned} D_{2(dq)} &= \frac{2\cdot T_{ch(1)}}{T_S}\cdot\begin{bmatrix}1.016\\0.587\end{bmatrix} \\ &= \frac{\sqrt{2}\cdot L_p\cdot A}{T_S\cdot\overline{v}_{dc}}\cdot\begin{bmatrix}1.016\\0.587\end{bmatrix} \end{aligned} \tag{5.73}$$

Now, Δd_2 is the sum of Equations (5.72) and (5.73), which consists of Δd_{2d} and Δd_{2q} as:

$$\begin{aligned} \Delta d_2 &= \begin{bmatrix}\Delta d_{2d}\\\Delta d_{2q}\end{bmatrix} \\ &= -R_{2(dq)} - D_{2(dq)} \\ &= \left[\frac{3}{2}\cdot\frac{L_p}{T_S\cdot\overline{v}_{dc}}\cdot I_b + \frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\arctan\left(\frac{\overline{v}_{dc}}{Z_{eq}\cdot I_b}\right)\right]\cdot\begin{bmatrix}1.17\\0.675\end{bmatrix} \\ &\quad -\frac{\sqrt{2}\cdot L_p\cdot A}{T_S\cdot\overline{v}_{dc}}\cdot\begin{bmatrix}1.016\\0.587\end{bmatrix} \end{aligned} \tag{5.74}$$

5.3.2 Average Model of ZVT Inverter

Equations (5.4)–(5.6) describe the average model of a three-phase hard-switching inverter, and Figure 5.2 (b) illustrates the average model.

As with the PFC rectifier case discussed in Section 5.3.1, inserting variations into the average model of a hard-switching inverter can make the average model of the ZVT

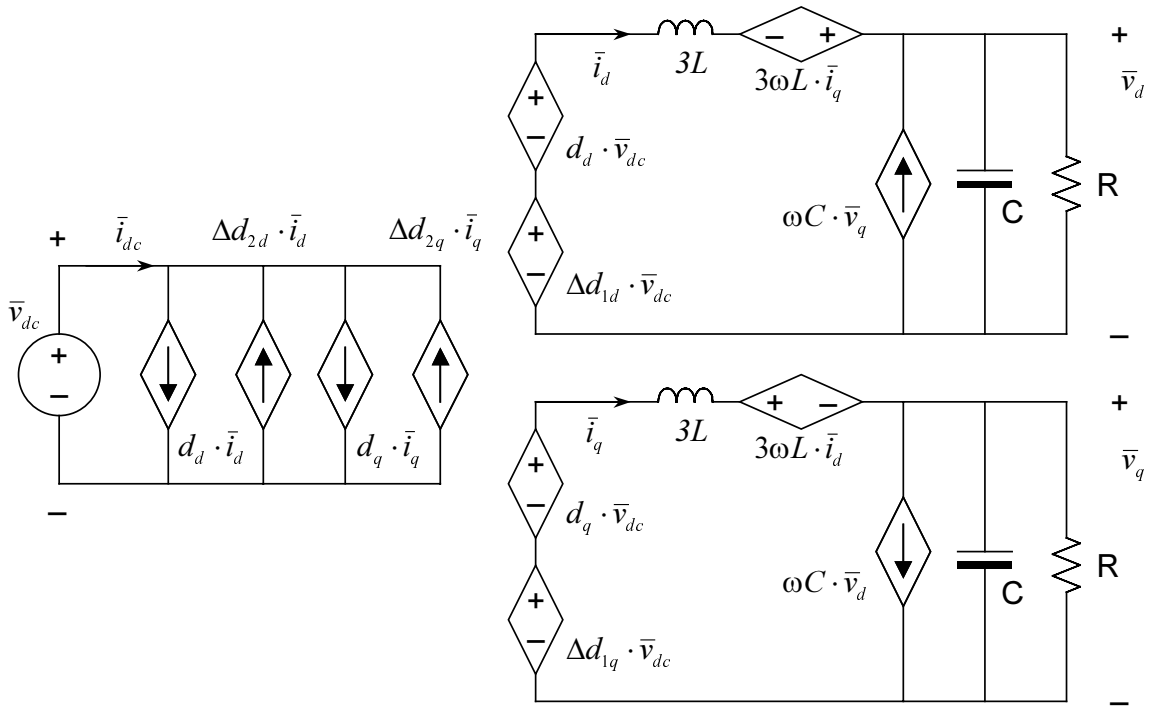


Figure 5.11 Average model of a three-phase ZVT inverter with inductor feedback.

inverter, as shown in Figure 5.11. Equations (5.75)–(5.77) describe the state equations of the ZVT inverter:

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix} &= \frac{1}{3L}\cdot\begin{bmatrix}d_d+\Delta d_{1d}\\ d_q+\Delta d_{1q}\end{bmatrix}\cdot\bar{v}_{dc}-\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\frac{1}{3L}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix}\\ &= \frac{1}{3L}\cdot\begin{bmatrix}d_d\\ d_q\end{bmatrix}\cdot\bar{v}_{dc}+\frac{1}{3L}\cdot\begin{bmatrix}\Delta d_{1d}\\ \Delta d_{1q}\end{bmatrix}\cdot\bar{v}_{dc}-\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\frac{1}{3L}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix}\end{aligned} \tag{5.75}$$

$$\frac{d}{dt}\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix} = \frac{1}{C}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix}-\frac{1}{RC}\cdot\begin{bmatrix}\bar{v}_d\\ \bar{v}_q\end{bmatrix} \tag{5.76}$$

$$\begin{aligned}\bar{i}_{dc} &= \begin{bmatrix}d_d-\Delta d_{2d} & d_q-\Delta d_{2q}\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}\\ &= \begin{bmatrix}d_d & d_q\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}-\begin{bmatrix}\Delta d_{2d} & \Delta d_{2q}\end{bmatrix}\cdot\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\end{bmatrix}\end{aligned} \tag{5.77}$$

The direction of i_{DC} defined in Figure 5.4 (a) is opposite to that defined in Figure 5.2 (b). Therefore, both Δd_{2d} and Δd_{2q} are subtracted from the original duty ratios (d_d and d_q), as shown in Equation (5.77). Their directions are opposite to those of d_d and d_q, as shown in Figure 5.11. The four variations (Δd_{1d}, Δd_{1q}, Δd_{2d} and Δd_{2q}) are the same as those for the PFC rectifier, as shown in Equations (5.71) and (5.74).

5.4 SMALL-SIGNAL MODELING AND ANALYSIS

The average models of three-phase PFC boost rectifiers shown in Figure 5.10 are used for small-signal analysis. The results of the ZVT rectifier are compared with those of the hard-switching rectifier.

5.4.1 Small-Signal Model of Hard-Switching PFC Boost Rectifier

Both Equations (5.2) and (5.3) are linearized by replacing $\bar{i}_d$, $\bar{i}_q$, $\bar{v}_d$, $\bar{v}_q$, d_d, d_q and $\bar{v}_{dc}$ with $I_d + \tilde{i}_d$, $I_q + \tilde{i}_q$, $V_d + \tilde{v}_d$, $V_q + \tilde{v}_q$, $D_d + \tilde{d}_d$, $D_q + \tilde{d}_q$, and $V_{dc} + \tilde{v}_{dc}$, respectively. Then, by putting both $\tilde{v}_d = 0$ and $\tilde{v}_d = 0$ into the linearized equations, the small-signal model of the PFC boost rectifier is developed, as shown in Equation (5.78) and Figure 5.12:

$$\frac{d}{dt}\begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \\ \tilde{v}_{dc} \end{bmatrix} = \begin{bmatrix} 0 & \omega & -\frac{D_d}{3L} \\ -\omega & 0 & -\frac{D_q}{3L} \\ \frac{D_d}{C} & \frac{D_q}{C} & -\frac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \\ \tilde{v}_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{V_{dc}}{3L} & 0 \\ 0 & -\frac{V_{dc}}{3L} \\ \frac{I_d}{C} & \frac{I_q}{C} \end{bmatrix} \cdot \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} \tag{5.78}$$

The capital letters denote steady-state operating values, and the symbol ˜ on top of each state variable denotes small-signal perturbation.

5.4.2 Small-Signal Model of ZVT PFC Boost Rectifier

Compared with the average model of the hard-switching rectifier, there are four more variables (Δd_{1d}, Δd_{1q}, Δd_{2d} and Δd_{2q}) in the average model of the ZVT rectifier. Therefore, both Equations (5.67) and (5.68) are linearized by replacing the eleven variables ($\bar{i}_d$, $\bar{i}_q$, $\bar{v}_d$, $\bar{v}_q$, d_d, d_q, Δd_{1d}, Δd_{1q}, Δd_{2d}, Δd_{2q} and $\bar{v}_{dc}$) with $I_d + \tilde{i}_d$, $I_q + \tilde{i}_q$, $V_d + \tilde{v}_d$, $V_q + \tilde{v}$, $D_d + \tilde{d}_d$, $D_q + \tilde{d}_q$, $\Delta D_{1d} + \Delta\tilde{d}_{1d}$, $\Delta D_{1q} + \Delta\tilde{d}_{1q}$, $\Delta D_{2d} + \Delta\tilde{d}_{2d}$, $\Delta D_{2q} + \Delta\tilde{d}_{2q}$ and $V_{dc} + \tilde{v}_{dc}$, respectively. Then, Equations (5.79) and (5.80) are derived by putting both $\tilde{v}_d = 0$ and $\tilde{v}_q = 0$ into the linearized equations:

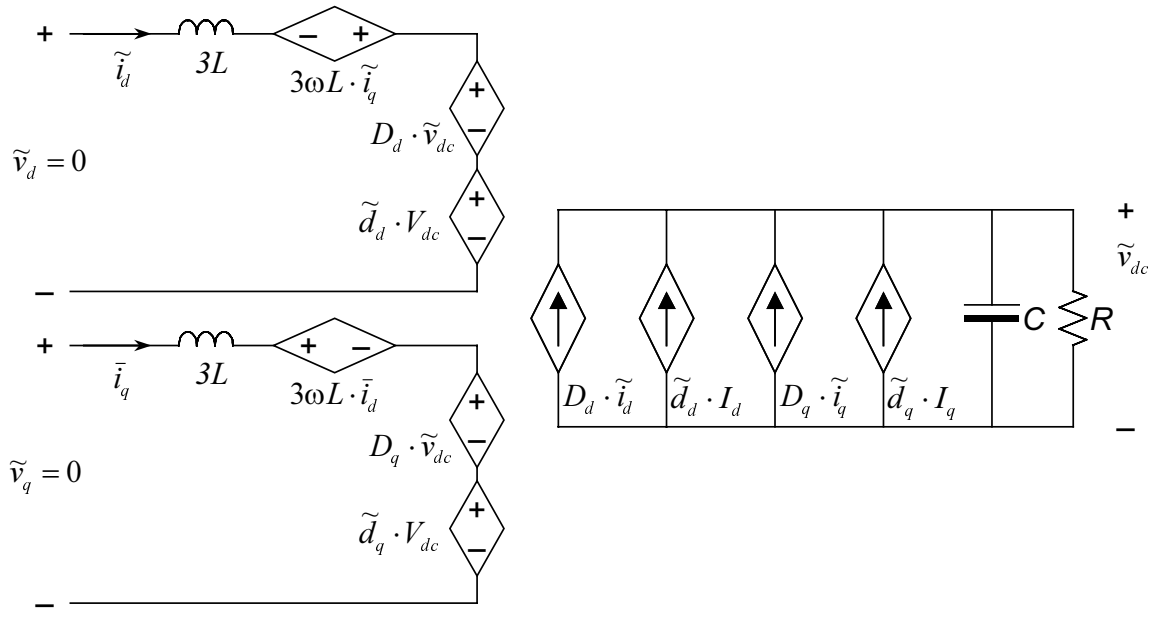


Figure 5.12 Small-signal model of three-phase PFC rectifier.

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix} &= \begin{bmatrix}0 & \omega\\ -\omega & 0\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix} - \frac{1}{3L}\cdot\begin{bmatrix}\tilde{d}_d\\ \tilde{d}_q\end{bmatrix}\cdot V_{dc} - \frac{1}{3L}\cdot\begin{bmatrix}D_d\\ D_q\end{bmatrix}\cdot\tilde{v}_{dc}\\ &\quad - \frac{1}{3L}\cdot\begin{bmatrix}\Delta\tilde{d}_{1d}\\ \Delta\tilde{d}_{1q}\end{bmatrix}\cdot V_{dc} - \frac{1}{3L}\cdot\begin{bmatrix}\Delta D_{1d}\\ \Delta D_{1q}\end{bmatrix}\cdot\tilde{v}_{dc}\\ &= \begin{bmatrix}0 & \omega\\ -\omega & 0\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix} - \frac{1}{3L}\cdot\begin{bmatrix}D_d+\Delta D_{1d}\\ D_q+\Delta D_{1q}\end{bmatrix}\cdot\tilde{v}_{dc} - \frac{V_{dc}}{3L}\cdot\begin{bmatrix}\tilde{d}_d\\ \tilde{d}_q\end{bmatrix} - \frac{V_{dc}}{3L}\cdot\begin{bmatrix}\Delta\tilde{d}_{1d}\\ \Delta\tilde{d}_{1q}\end{bmatrix}\end{aligned} \tag{5.79}$$

$$\begin{aligned}\frac{d}{dt}\tilde{v}_{dc} &= \frac{1}{C}\cdot\begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix} + \frac{1}{C}\cdot\begin{bmatrix}D_d & D_q\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix}\\ &\quad + \frac{1}{C}\cdot\begin{bmatrix}\Delta\tilde{d}_{2d} & \Delta\tilde{d}_{2q}\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix} + \frac{1}{C}\cdot\begin{bmatrix}\Delta D_{2d} & \Delta D_{2q}\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix} - \frac{\tilde{v}_{dc}}{RC}\\ &= \frac{1}{C}\cdot\begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix} + \frac{1}{C}\cdot\begin{bmatrix}D_d+\Delta D_{2d} & D_q+\Delta D_{2q}\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix} - \frac{\tilde{v}_{dc}}{RC}\\ &\quad + \frac{1}{C}\cdot\begin{bmatrix}\Delta\tilde{d}_{2d} & \Delta\tilde{d}_{2q}\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}\end{aligned} \tag{5.80}$$

The structures of the four variables Δd_{1d}, Δd_{1q}, Δd_{2d} and Δd_{2q} are identical to the different constants (c_1 and c_2) as:

$$\begin{aligned}\Delta d_{XX} &= c_1\cdot\frac{L_p\cdot I_b}{T_S\cdot\bar{v}_{dc}} + c_2\cdot\frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\arctan\left(\frac{\bar{v}_{dc}}{Z_{eq}\cdot I_b}\right) + c_3\cdot\frac{L_p}{T_S}\cdot\frac{A}{\bar{v}_{dc}}\\ &= c_1\cdot\frac{L_p\cdot I_b}{T_S\cdot\bar{v}_{dc}} + c_2\cdot\frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\arctan\left(\frac{\bar{v}_{dc}}{Z_{eq}\cdot I_b}\right) + \sqrt{\frac{2}{3}}\cdot c_3\cdot\frac{L_p}{T_S}\cdot\frac{\bar{i}_d}{\bar{v}_{dc}}\end{aligned} \tag{5.81}$$

In Equation (5.81), line-current amplitude (A) is replaced with $\sqrt{\frac{2}{3}}\cdot\bar{i}_d$ in accordance with both the dq-transformation and the PFC control. As verified in Equation (5.81), a variable Δd_{XX} consists of two variables $\bar{i}_d$ and $\bar{v}_{dc}$. Therefore, the small-signal perturbations of three right-hand terms are derived, as shown in Equations (5.82)–(5.84):

$$\text{Perturbation of first term} = -c_1\cdot\frac{L_p\cdot I_b}{T_S\cdot V_{dc}^2}\cdot\tilde{v}_{dc} \tag{5.82}$$

$$\text{Perturbation of second term} = c_2\cdot\frac{\sqrt{L_p\cdot C_S}}{T_S}\cdot\frac{Z_{eq}\cdot I_b}{\left(Z_{eq}\cdot I_b\right)^2 + V_{dc}^2}\cdot\tilde{v}_{dc} \tag{5.83}$$

$$\text{Perturbation of third term} = \sqrt{\frac{2}{3}} \cdot c_3 \cdot \frac{L_p}{T_S \cdot V_{dc}} \cdot \tilde{i}_d - \sqrt{\frac{2}{3}} \cdot c_3 \cdot \frac{L_p \cdot I_d}{T_S \cdot V_{dc}^2} \cdot \tilde{v}_{dc} \tag{5.84}$$

The sum of Equations (5.82)–(5.84) is the perturbation of Δd_{XX} $\left(\Delta \tilde{d}_{XX}\right)$ as:

$$\begin{aligned} \Delta \tilde{d} &= \left(-c_1 \cdot \frac{L_p \cdot I_b}{T_S \cdot V_{dc}^2} + c_2 \cdot \frac{\sqrt{L_p \cdot C_S}}{T_S} \cdot \frac{Z_{eq} \cdot I_b}{\left(Z_{eq} \cdot I_b\right)^2 + V_{dc}^2} - \sqrt{\frac{2}{3}} \cdot c_3 \cdot \frac{L_p \cdot I_d}{T_S \cdot V_{dc}^2} \right) \cdot \tilde{v}_{dc} \\ &\quad + \sqrt{\frac{2}{3}} \cdot c_3 \cdot \frac{L_p}{T_S \cdot V_{dc}} \cdot \tilde{i}_d \\ &\equiv k_1 \cdot \tilde{v}_{dc} + k_2 \cdot \tilde{i}_d \end{aligned} \tag{5.85}$$

$$\text{where} \quad k_1 = -c_1 \cdot \frac{L_p \cdot I_b}{T_S \cdot V_{dc}^2} + c_2 \cdot \frac{\sqrt{L_p \cdot C_S}}{T_S} \cdot \frac{Z_{eq} \cdot I_b}{\left(Z_{eq} \cdot I_b\right)^2 + V_{dc}^2} - \sqrt{\frac{2}{3}} \cdot c_3 \cdot \frac{L_p \cdot I_d}{T_S \cdot V_{dc}^2}$$

$$\text{and} \quad k_2 = \sqrt{\frac{2}{3}} \cdot c_3 \cdot \frac{L_p}{T_S \cdot V_{dc}}$$

The result of Equation (5.85) rewrites Equations (5.79) and (5.80) without the perturbations of Δd_{1d}, Δd_{1q}, Δd_{2d} and Δd_{2q} as:

$$\begin{aligned} \frac{d}{dt}\begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} &= \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} - \frac{1}{3L} \cdot \begin{bmatrix} D_d + \Delta D_{1d} \\ D_q + \Delta D_{1q} \end{bmatrix} \cdot \tilde{v}_{dc} - \frac{V_{dc}}{3L} \cdot \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} - \frac{V_{dc}}{3L} \cdot \begin{bmatrix} \Delta \tilde{d}_{1d} \\ \Delta \tilde{d}_{1q} \end{bmatrix} \\ &= \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} - \frac{1}{3L} \cdot \begin{bmatrix} D_d + \Delta D_{1d} \\ D_q + \Delta D_{1q} \end{bmatrix} \cdot \tilde{v}_{dc} - \frac{V_{dc}}{3L} \cdot \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} \\ &\quad - \frac{V_{dc}}{3L} \cdot \begin{bmatrix} k_{1(1d)} \cdot \tilde{v}_{dc} + k_{2(1d)} \cdot \tilde{i}_d \\ k_{1(1q)} \cdot \tilde{v}_{dc} + k_{2(1q)} \cdot \tilde{i}_d \end{bmatrix} \\ &= \begin{bmatrix} -\frac{V_{dc}}{3L} \cdot k_{2(1d)} & \omega \\ -\omega - \frac{V_{dc}}{3L} \cdot k_{2(1q)} & 0 \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} - \frac{1}{3L} \cdot \begin{bmatrix} D_d + \Delta D_{1d} + V_{dc} \cdot k_{1(1d)} \\ D_q + \Delta D_{1q} + V_{dc} \cdot k_{1(1q)} \end{bmatrix} \cdot \tilde{v}_{dc} \\ &\quad - \frac{V_{dc}}{3L} \cdot \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} \\ &\equiv \begin{bmatrix} -K_1 & \omega \\ -\omega - K_2 & 0 \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} - \frac{1}{3L} \cdot \begin{bmatrix} K_3 \\ K_4 \end{bmatrix} \cdot \tilde{v}_{dc} - \frac{V_{dc}}{3L} \cdot \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} \end{aligned} \tag{5.86}$$

$$\begin{aligned}
\frac{d}{dt}\tilde{v}_{dc} &= \frac{1}{C}\cdot\begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}+\frac{1}{C}\cdot\begin{bmatrix}D_d+\Delta D_{2d} & D_q+\Delta D_{2q}\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix}-\frac{\tilde{v}_{dc}}{RC}\\
&\quad+\frac{1}{C}\cdot\begin{bmatrix}\Delta\tilde{d}_{2d} & \Delta\tilde{d}_{2q}\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}\\
&=\frac{1}{C}\cdot\begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}+\frac{1}{C}\cdot\begin{bmatrix}D_d+\Delta D_{2d} & D_q+\Delta D_{2q}\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix}-\frac{\tilde{v}_{dc}}{RC}\\
&\quad+\frac{1}{C}\cdot\begin{bmatrix}k_{1(2d)}\cdot\tilde{v}_{dc}+k_{2(2d)}\cdot\tilde{i}_d & k_{1(2q)}\cdot\tilde{v}_{dc}+k_{2(2q)}\cdot\tilde{i}_d\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}\\
&=\frac{1}{C}\cdot\begin{bmatrix}D_d+\Delta D_{2d}+k_{2(2d)}\cdot I_d & D_q+\Delta D_{2q}+k_{2(2q)}\cdot I_q\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix}\\
&\quad+\frac{1}{C}\cdot\left(k_{1(2d)}\cdot I_d+k_{1(2q)}\cdot I_q-\frac{1}{R}\right)\cdot\tilde{v}_{dc}+\frac{1}{C}\cdot\begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}\\
&=\frac{1}{C}\cdot\begin{bmatrix}K_5 & K_6\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\end{bmatrix}+\frac{K_7}{C}\cdot\tilde{v}_{dc}+\frac{1}{C}\cdot\begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\cdot\begin{bmatrix}I_d\\ I_q\end{bmatrix}
\end{aligned} \tag{5.87}$$

where $K_1=\frac{V_{dc}}{3L}\cdot k_{2(1d)}$, $K_2=\frac{V_{dc}}{3L}\cdot k_{2(1q)}$,

$K_3=D_d+\Delta D_{1d}+V_{dc}\cdot k_{1(1d)}$,

$K_4=D_q+\Delta D_{1q}+V_{dc}\cdot k_{1(1q)}$,

$K_5=D_d+\Delta D_{2d}+k_{2(2d)}\cdot I_d$,

$K_6=D_q+\Delta D_{2q}+k_{2(2q)}\cdot I_q$, and

$K_7=k_{1(2d)}\cdot I_d+k_{1(2q)}\cdot I_q-\frac{1}{R}$

Finally, Equations (5.86) and (5.87) derive the small-signal model of the ZVT PFC boost rectifier, as shown in both Equation (5.88) and Figure 5.12:

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{v}_{dc}\end{bmatrix}=\begin{bmatrix}-K_1 & \omega & -\frac{K_3}{3L}\\ -\omega-K_2 & 0 & -\frac{K_4}{3L}\\ \frac{K_5}{C} & \frac{K_6}{C} & \frac{K_7}{C}\end{bmatrix}\cdot\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{v}_{dc}\end{bmatrix}+\begin{bmatrix}-\frac{V_{dc}}{3L} & 0\\ 0 & -\frac{V_{dc}}{3L}\\ \frac{I_d}{C} & \frac{I_q}{C}\end{bmatrix}\cdot\begin{bmatrix}\tilde{d}_d\\ \tilde{d}_q\end{bmatrix} \tag{5.88}$$

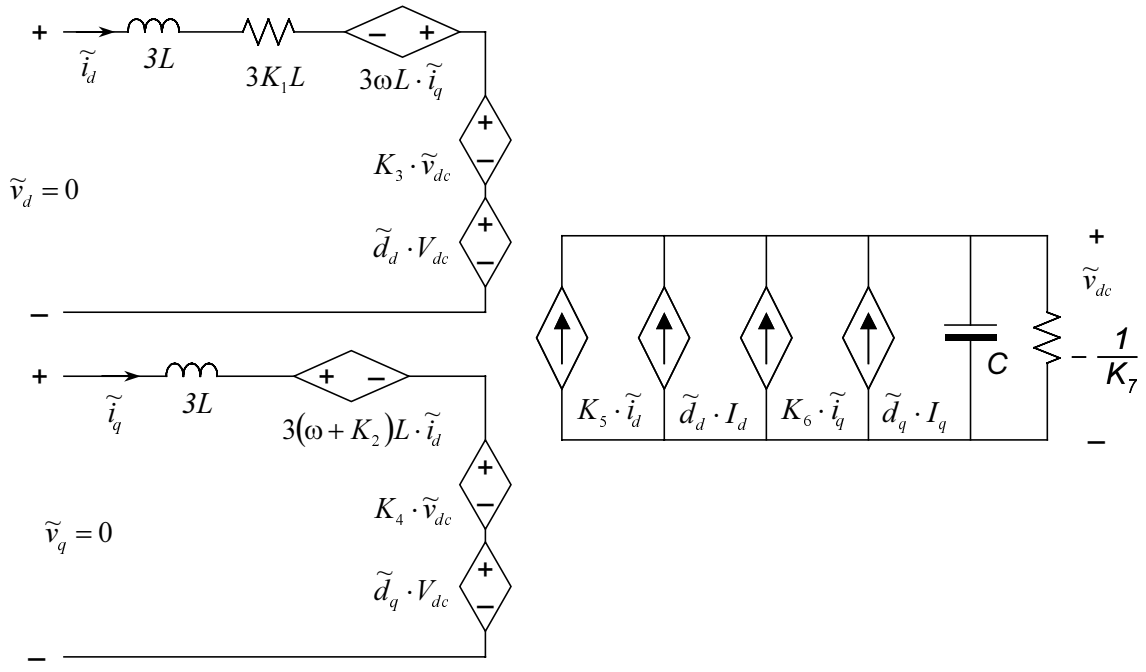


Figure 5.13 Small-signal model of three-phase PFC ZVT boost rectifier.

5.4.3 Small-Signal Analysis

A. Design Example

As an example, the small-signal analysis uses a 5 kW three-phase boost rectifier, which has following design parameters:

- Line-to-line RMS voltage V_{rms} = 180 V,
- Output voltage V_{dc} = 350 V,
- Inductance L = 100 μH,
- Capacitance C = 500 μF,
- Load resistance R = 25 Ω,
- Line frequency f = 60 Hz, and
- Switching frequency f_s = 100 kHz.

The steady-state operating point is calculated using the given system parameters and the average model shown in Figure 5.10 (a), as follows:

$$V_d = \sqrt{\frac{3}{2}} \cdot V_m = \sqrt{\frac{3}{2}} \times \left(\sqrt{2} \times 180\right) = 311.77$$

$$D_d = \frac{V_d}{V_{dc}} = \frac{311.77}{350} = 0.891$$

$$I_d = \frac{V_{dc}}{R \cdot D_d} = \frac{350}{25 \times 0.891} = 15.713$$

$$V_q = 0$$

$$D_q = -\frac{3 \cdot \omega \cdot L \cdot I_d}{V_{dc}} = -\frac{3 \times (2\pi \times 60) \times \left(100 \times 10^{-6}\right) \times 15.713}{350} = -5.077 \times 10^{-3}$$

$$I_q = 0$$

The auxiliary circuit for the ZVT operation is designed as follows:

- Auxiliary resonant inductance (L_X) = 5μH,
- Snubber capacitance (C_S) = 0.025 μF, and
- Boost current (I_b) = 5 A.

Due to the ZVT operations, there are additional operating values. The steady-state operating values of duty-ratio variations are calculated using Equations (5.70) and (5.73), as follows:

$$\Delta D_{1d} = -0.05192, \qquad \Delta D_{1q} = -0.02994,$$
$$\Delta D_{2d} = 0.04293, \text{ and } \quad \Delta D_{2q} = 0.02475.$$

Using the definitions of k_1 and k_2 shown in Equation (5.84), eight constants $k_{1(1d)}$, $k_{1(1q)}$, $k_{1(2d)}$, $k_{1(2q)}$, $k_{2(1d)}$, $k_{2(1q)}$, $k_{2(2d)}$ and $k_{2(2q)}$ are calculated, as follows:

$$k_{1(1d)} = -3.6684\times10^{-5}, \qquad k_{1(1q)} = -2.1195\times10^{-5},$$
$$k_{1(2d)} = 6.2366\times10^{-5}, \qquad k_{1(2q)} = 3.6043\times10^{-5},$$
$$k_{2(1d)} = 0.8380\times10^{-3}, \qquad k_{2(1q)} = 0.4842\times10^{-3},$$
$$k_{2(2d)} = -1.6760\times10^{-3}, \text{ and } \quad k_{2(2q)} = -0.9683\times10^{-3}.$$

Eventually, seven constants (K_1, K_2, K_3, K_4, K_5, K_6 and K_7) used in the small-signal model of the ZVT rectifier are calculated using the definitions shown in Equations (5.85) and (5.86), as follows:

$$K_1 = 977.65\ \Omega, \qquad K_2 = 564.84,$$
$$K_3 = 0.8262, \qquad K_4 = -0.04244,$$
$$K_5 = 0.9076, \qquad K_6 = 0.01967,$$
$$\text{and } K_7 = -0.03902\ \Omega^{-1}.$$

B. Coefficients of State Variables

As shown in Equation (5.87), the perturbations of the duty-ratio variations are not shown in the small-signal model of the ZVT rectifier. The state variables of the model are the same as those of the hard-switching rectifier model: $\tilde{i}_d$, $\tilde{i}_q$, $\tilde{v}_{dc}$, $\tilde{d}_d$ and $\tilde{d}_q$. The variable coefficients of the hard-switching rectifier are simply determined by the main power stage design and the line frequency. However, the variable coefficients of the ZVT rectifier are determined by not only the main power stage design, but also the auxiliary circuit design. Figure 5.14 shows the trends of the state variable coefficients using the design examples. Since the resonant inductance (L_p) mostly affects the commutation periods, Figure 5.14 chooses this value as a design variable.

The biggest difference is the coefficient of $\tilde{i}_d$ in the *d*-input loop, which is K_1 for the ZVT rectifier, while it is zero for the hard-switching rectifier. The coefficient K_1 implies that the ZVT rectifier has a damping factor (resistance) in the *d*-input loop. As shown in Figure 5.14 (a), K_1 is proportional to the resonant inductance. Therefore, the rectifier can have more damping by increasing the resonant inductance.

K_2 is added to the original coefficient of $\tilde{i}_d$ in the *q*-input loop. K_2 is always positive, as shown in Figure 5.14 (a). Therefore, this value not only makes more damping, but also increases the coupling effect from *d*-input loop.

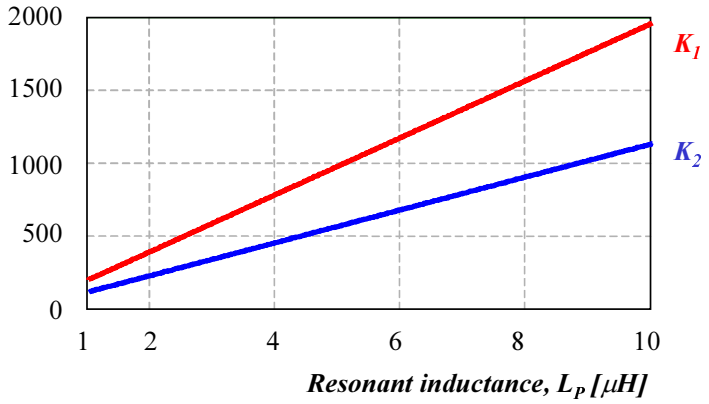
The D_d used in Equation (5.77) is replaced with K_3 and K_5 in the small-signal model of the ZVT rectifier, as shown in Equation (5.87). With a reasonable resonant inductance, K_3 is smaller than D_d, and K_5 is larger than D_d, as shown in Figure 5.14 (b). Therefore, the *d*-input loop of the ZVT rectifier becomes less sensitive, while the output loop becomes more sensitive. However, a large resonant inductance might make K_5 smaller than D_d.

The D_q used in Equation (5.77) is also replaced with K_4 and K_6 in the small-signal model of the ZVT rectifier, as shown in Equation (5.87). Figure 5.14 (c) shows the magnitudes of the K_4, K_6 and D_q; K_4 is smaller than D_q, and K_6 is larger than D_q. Therefore, the *q*-input loop of the ZVT rectifier becomes less sensitive, while the output loop becomes more sensitive.

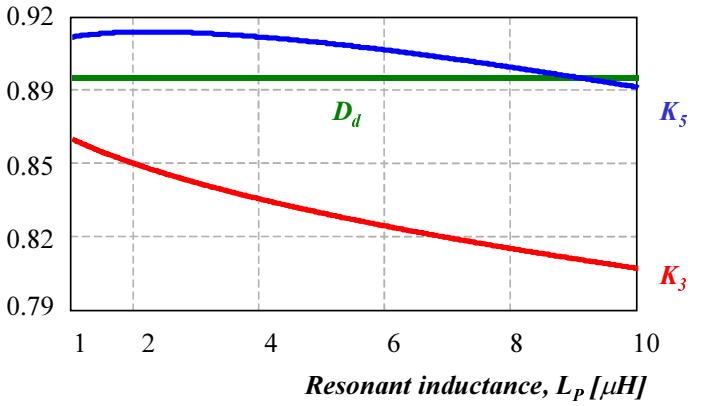
The small-signal model of the ZVT rectifier uses K_7 as a load instead of R. According to the value of K_7, the load resistance $\left(-\frac{1}{K_7}\right)$ is slightly larger than that of the hard-switching small-signal model, as follows:

$$-\frac{1}{K_7} = -\frac{1}{-0.03902} = 25.62 > 25 = R.$$

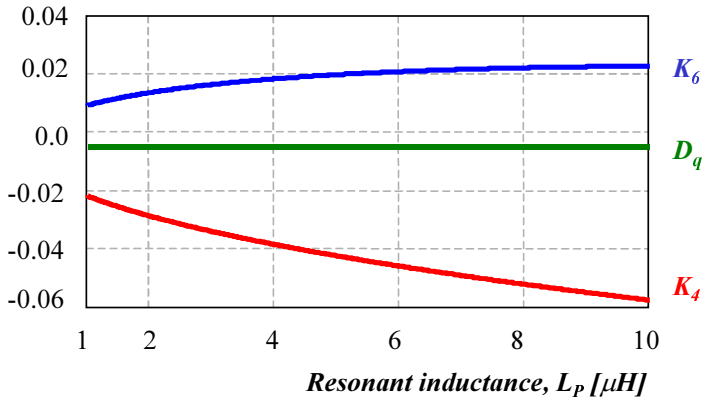
This investigation of all the coefficients predicts that the ZVT operations both increase the damping and change the DC gains. This prediction will be verified in the following section using several small-signal transfer functions.



(a)



(b)



(c)

Figure 5.14 Coefficient trends as the functions of resonant inductance: (a) K_1 and K_2, (b) K_3 and K_5, and (c) K_4 and K_6.

C. Small-Signal Transfer Functions

Figures 5.15, 5.16 and 5.17 show all the small-signal transfer functions required for control design. In these figures, the simulation results of the ZVT rectifier model are compared with those of the hard-switching rectifier model.

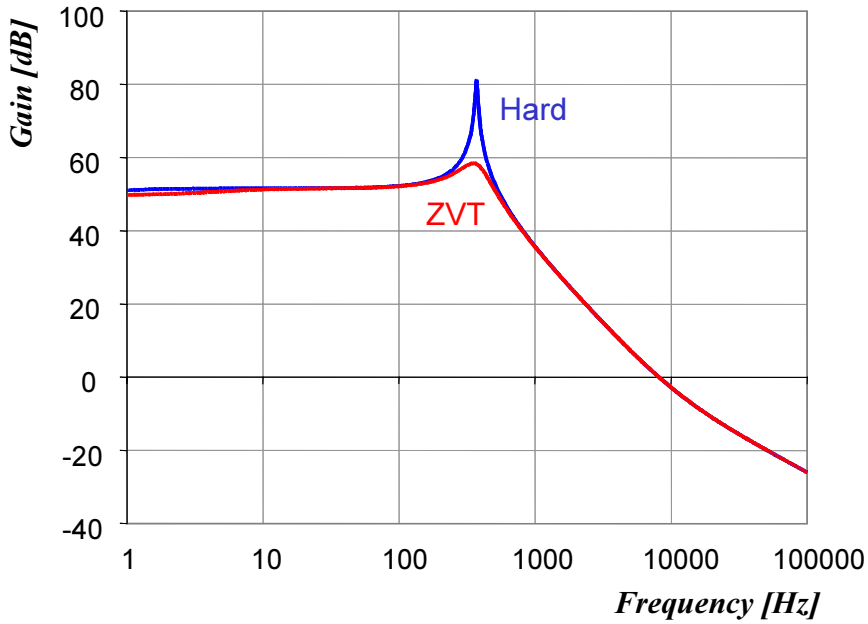
As shown in Figure 5.15, the control-to-output voltage transfer function $\left(G_{C1} = \tilde{v}_{dc} / \tilde{d}_d\right)$ of the ZVT rectifier has a slight decrease in the DC gain and a significant increase in damping as compared with those of the hard-switching rectifier. The investigation of the state variable coefficients has already predicted these phenomena: Adding K_1 as the coefficient of i_d causes the damping; since K_3 is smaller than D_d, the DC gain is reduced. Figure 5.16 verifies that another control-to-output voltage transfer function $\left(G_{C2} = \tilde{v}_{dc} / \tilde{d}_q\right)$ of the ZVT rectifier has the same characteristics as G_{C1}. The K_2 changes the coupling effect and acts as a damping factor. Since K_4 is smaller than D_q, the DC gain is reduced just as with G_{C1}. The reduced DC gains in both G_{C1} and G_{C2} imply that the output voltage regulation is not as good as that of the hard-switching rectifier.

As shown in Figure 5.17, the control-to-current transfer function $\left(\tilde{i}_d / \tilde{d}_d\right)$ of the ZVT rectifier has different characteristics from those of the control-to-output voltage transfer functions. There are increases in both the DC gain and the damping, compared with those of the hard-switching rectifier. Both K_5 and K_6 are larger than D_d and D_q, respectively, which increases the DC gain. The load $\left(-1/K_7\right)$ of the ZVT rectifier causes more damping, because it is larger than the load of the hard-switching rectifier (R).

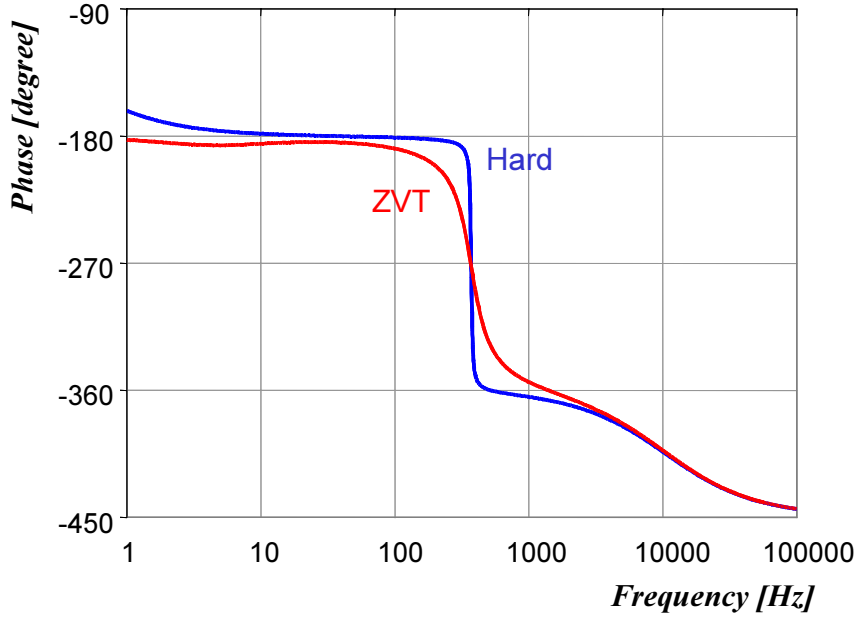
These transfer functions have two common characteristics, as follows:

- Change of DC gains, and
- Significant increase of dampings.

These analyses are the same as those of papers formerly published that covered both three-phase rectifiers and DC-DC converters [E4, E11-E13].



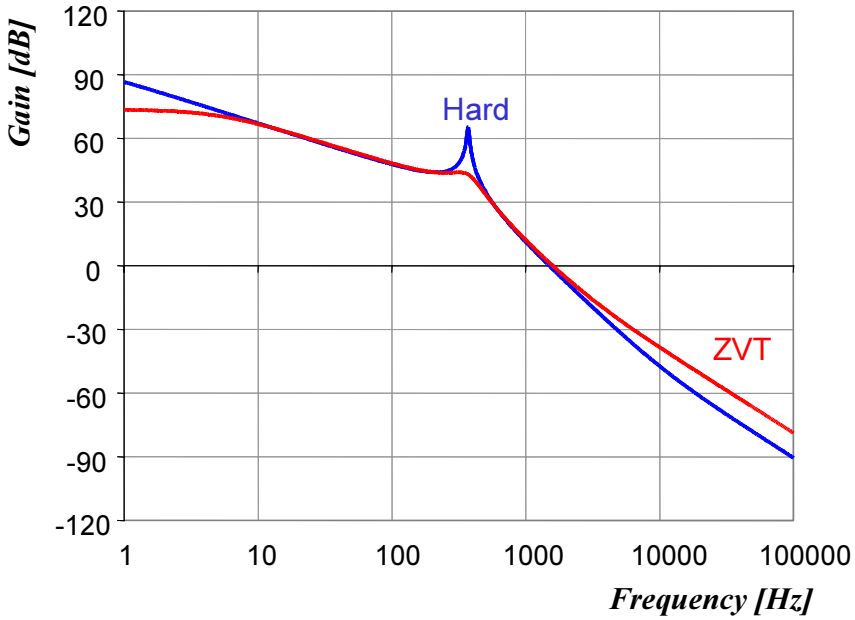
(a)



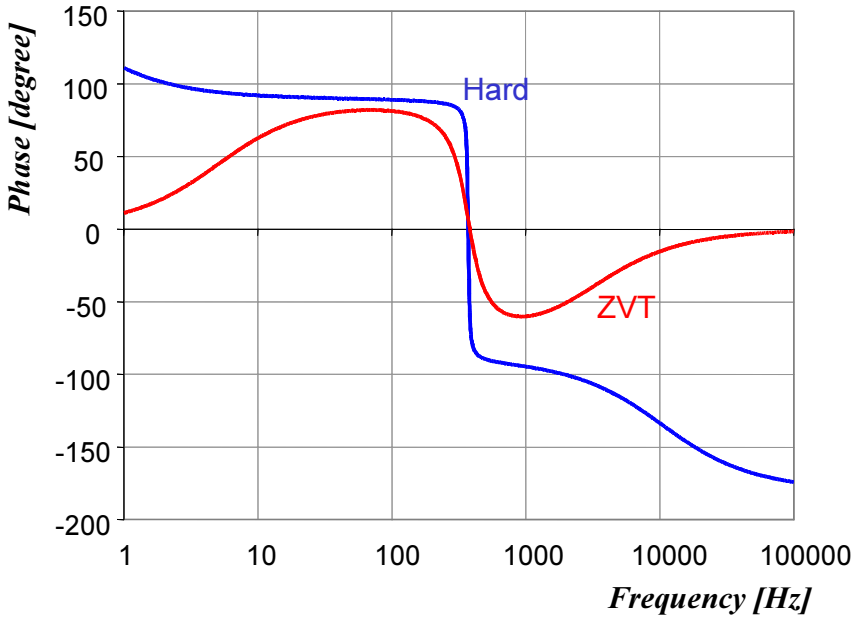
(b)

Figure 5.15 Control to output voltage transfer function $\left(G_{C1} = \frac{\tilde{v}_{dc}}{\tilde{d}_d} \right)$:

(a) Gain and (b) Phase.



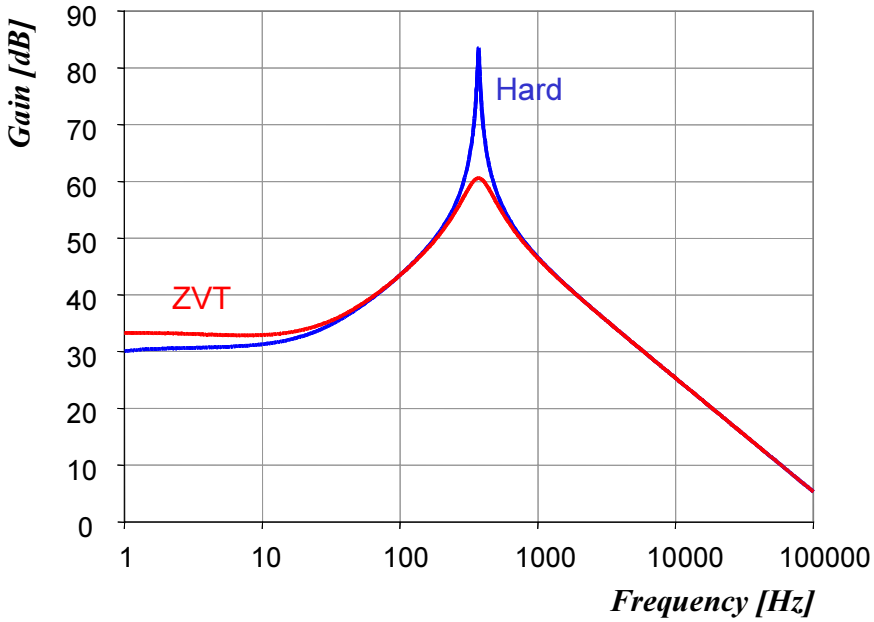
(a)



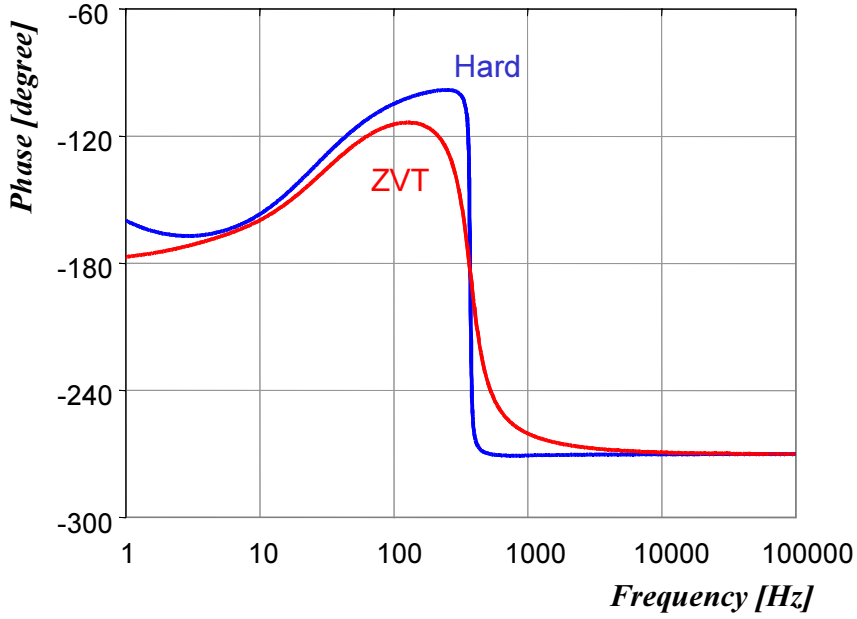
(b)

Figure 5.16 Control-to-output voltage transfer function $\left(G_{C2} = \frac{\tilde{v}_{dc}}{\tilde{d}_q} \right)$:

(a) Gain and (b) Phase.



(a)



(b)

Figure 5.17 Control-to-current transfer function $\left(\frac{\tilde{i}_d}{\tilde{d}_d}\right)$:

(a) Gain and (b) Phase.

Chapter 6. CONCLUSION

Conventional soft-switching topologies have proven the possibilities for improving the performance of multi-phase converters. For minimizing the cost and space required for the auxiliary circuits, there have been several proposals that use simplified auxiliary circuits. However, the conventional soft-switching topologies with simplified auxiliary circuits could not improve converter performance as much as anticipated. On the other hand, there have been improvements in the switching characteristics of switching power devices, and these advancements reduce the advantages of soft-switching topologies.

This dissertation has been comprehensively dedicated to suggesting the features of the ZVT topologies that allow for practical applications. In general, a multi-phase converter consists of the power stage and the controller. Therefore, the effort of this dissertation has been separately dedicated to the two parts. For the power stage, simplifying auxiliary circuits makes the ZVT topologies more attractive, and small-signal analysis with the average modeling of the ZVT converters reveals the control issues.

6.1 Accomplishments

In order to determine the base model of this dissertation, Chapter 2 has reviewed conventional inductor-coupled (IC) ZVT topologies for multi-phase converters. Although all the IC ZVT topologies are attractive for high-current applications, the ZVT converter with inductor feedback has been selected as a specific base model. This chapter reviewed the operation principles, and showed the experimental results that were obtained through the GE/DARPA project [D17]. Furthermore, the thorough operation analysis of the ZVT converter led to the generalized timing equations for all operation periods. These equations clearly show the effects of both boost current and the turns-ratio of coupled inductors.

In order to make the ZVT topologies more attractive in practical applications, simplifying auxiliary circuits is one of the major goals of this dissertation. This effort mainly creates two distinguished proposals: the Single-Switch Single-Leg (S^3L) ZVT cell and the Phase-Lock (PL) concept.

Chapter 3 began the simplification of auxiliary circuits from the investigation of the IC ZVT converters. Section 3.1 has revealed two inherent currents that cause more losses, EMI noise, and even malfunctions of the converters. Section 3.2 has proposed a novel IC ZVT cell that eliminates these inherent currents. The proposed ZVT cell not only improves the efficiency and EMI characteristics of converters by eliminating these inherent currents, but also removes a saturable inductor that is used in conventional IC ZVT converters. The ZVT cell achieves zero-voltage commutations without any modification to the controller, which allows the proposed ZVT cell to still be a piggyback. An implemented 50-kW three-phase inverter using the proposed cells verifies its operation and performance.

The proposed ZVT cell offers insight into the simplification of the auxiliary circuit. Eventually, Section 3.3 has proposed another novel ZVT cell, named the S^3L ZVT cell, which consists of one auxiliary switch and one coupled inductor with three windings. Because the operation principle is the same as that of the conventional ZVT converter with inductor feedback, its performance and benefits are almost identical. This structure

is phase-based, so it is attractive for the PEBB module. An implemented ZVT cell verifies the operation and performance of the cell.

While the S^3L ZVT cell uses one auxiliary switch for both top and bottom main switches, Chapter 4 has investigated the possibilities for using only two auxiliary switches to assist the zero-voltage turn-on commutations of all main switches. However, the investigation revealed that the simplification itself is not possible. Eventually, Section 4.2 has proposed the PL concept, which facilitates the simplification. A modified SVM scheme using synchronized turn-on commutations compromises limitations of the PL circuit operation.

The PL circuit can be realized using two methods: one uses saturable inductors with their flux density controller and the other uses high-speed thyristors. Section 4.3 has shown thorough design and evaluations of the PL ZVT converter with inductor feedback using the saturable inductors. Section 4.4 has proposed an improved power stage, which allows the minimum-loss (ML) SVM scheme to be used instead of the synchronized turn-on commutations. Section 4.5 has shown the PL circuit using high-speed thyristors. Simplifying the other ZVT converters using the PL circuits verifies the generalized characteristics of the PL concept. Combining the S^3L ZVT cell and the PL concept creates a novel power stage with single auxiliary switch in multi-phase inverters.

Chapter 5 was dedicated to developing the average model of the ZVT converter with inductor feedback. The generalized timing equations developed in Section 2.3 are used for creating the average model. Section 5.2 has investigated the duty-ratio variations in both AC and DC sides, and has quantified them in *dq*-coordinates. The entire procedure reveals that the average model of the converter requires double averaging.

Section 5.3 has developed the average models of the ZVT converters. The average model of the ZVT PFC boost rectifier has been used for the small-signal analysis required for control design. Although the state variables of the developed small-signal model are the same as those of the hard-switching rectifier, their coefficients change the characteristics of the rectifier, such that there is a change of DC gain and increased damping in the control-to-output transfer functions. The small-signal analysis evaluates the influence of ZVT operations on the control design.

6.2 SUGGESTIONS FOR FUTURE RESEARCH

Since the first soft-switching topology was proposed, there have been many approaches for multi-phase converters. Due to the improved characteristics of switching power devices, the advantages of soft-switching topologies become less and less. This is a particularly serious issue for motor drive applications.

In this circumstance, the thrust of research does not require any theoretically new soft-switching topologies, but must solve practical issues for the implementations of conventional soft-switching topologies. Therefore, this dissertation has been dedicated to simplifying auxiliary circuits. Future research should focus more on the practical issues, which can make conventional soft-switching topologies more attractive and clarify the appropriate applications of the soft-switching topologies. The followings are some issues for future research:

- Although the variable-timing control scheme optimizes timing control, it requires load current feedback. Since any sensing hardware and software have their own complexities and tolerances, the variable-timing control scheme also has the same issues. Therefore, novel timing control schemes without any feedback are preferred for practical applications.
- Since the conduction losses of auxiliary circuits comprise the majority of auxiliary circuit losses, the selection of auxiliary devices becomes important. Therefore, it is recommended that future soft-switching topologies should use low conduction loss devices such as thyristors.

Chapter 5 has developed the average models of the ZVT converters and performed their small-signal analyses. However, the models are not perfect for all cases, particularly for inverters operating with power factors of more than 30 degree. More generalized models are recommended for future research.

REFERENCES

Soft-switching Topologies for DC-DC Converters

[A1] G. Hua, F. C. Lee, and M. M. Jovanovic, "An Improved Zero-Voltage-Switched PWM Converter using a Saturable Inductor," in *Proceedings of IEEE PESC `91*, 1991, pp. 189-194.

[A2] G. Hua and F. C. Lee, "A New Class of Zero-Voltage-Switched PWM Converters," in *Proceedings of IEEE HFPC `91*, 1991, pp. 244-251.

[A3] G. Hua and F. C. Lee, "A Novel Full-Bridge Zero-Current-Switched PWM Converter," in *Proceedings of EPE `91*, 1991, pp..

[A4] G. Hua, C. Leu, Y. Jiang, and F. C. Lee, "Novel Zero-Voltage-Transition PWM Converters," in *Proceedings of IEEE PESC `92*, 1992, pp. 55-61.

[A5] D. C. Martins and I. Barbi, "A Family of DC-to-DC PWM Converter using a New ZVS Commutation Cell," in *Proceedings of IEEE PESC `93*, 1993, pp. 524-530.

[A6] G. Hua, E. Yang, Y. Jiang, and F. C. Lee, "Novel Zero-Current-Transition PWM Converters," in *Proceedings of IEEE PESC `93*, 1993, pp. 538-544.

[A7] J. P. Gegner, C. Q. Lee, "Zero-Voltage-Transition Converters using an Inductor Feedback Technique," in *Proceedings of IEEE APEC `94*, 1994, pp. 862-868.

[A8] J. P. Gegner, C. Q. Lee, "Zero-Voltage-Transition Converters using a Simple Magnetic Technique," in *Proceedings of IEEE PESC `94*, 1994, pp. 590-596.

[A9] G. Hua and F. C. Lee, "Soft-Switching Techniques in PWM Converters," *IEEE Transactions on Industrial Electronics*, Vol. 42, No. 6, Dec. 1995, pp. 595-603.

[A10] H. Mao, F. C. Lee, X. Zhou, and D. Boroyevich, "Improved Zero-Current-Transition Converters for High Power Application," in *Proceedings of IEEE IAS `96*, 1996, pp. 1145-1152.

DC-side Soft-switching Topologies for Multi-phase Converters

[B1] D. M. Divan, "The Resonant DC-link Converter – A New Concept in Power Conversion," in *Proceedings of IEEE IAS `86*, 1986, pp. 648-656.

[B2] M. Kheraluwala and D. M. Divan, "Delta Modulation Strategies for Resonant Link Inverters." in *Proceedings of IEEE PESC `87*, 1987, pp. 271-278.

[B3] D. M. Divan, and G. Skibinski, "Zero Switching Loss Inverters for High Power Applications," in *Proceedings of IEEE IAS `87,* 1987, pp. 627-634.

[B4] G. Venkataramanan, D. M. Divan, and T. M. Jahns, "Discrete Pulse Modulation Strategies for High-frequency Inverter Systems," in *Proceedings of IEEE PESC `89*, 1989, pp. 1013-1020.

[B5] R. W. De Doncker and J. P. Lyons, "The Auxiliary Quasi-Resonant DC Link Inverter," in *Proceedings of IEEE PESC `91*, 1991, pp. 248-253.

[B6] A. Mertens and H. Skudelny, "Calculations on the Spectral Performance of Discrete Pulse Modulation Strategies," in *Proceedings of IEEE PESC `91*, 1991, pp. 357-364.

[B7] V. G. Agelidis, P. D. Ziogas, and G. Joos, "An Optimum Modulation Strategy for a Novel Notch Commutated 3-ϕ PWM Inverter," in *Proceedings of IEEE IAS `91*, 1991, pp. 809-818.

[B8] R. W. De Doncker and J. P. Lyons, "An Auxiliary Quasi-Resonant DC Link Inverter for Switched Reluctance Machines," in *Proceedings of European Power Electronics Specialist Conference `91*, 1991, pp. 18-23.

[B9] G. Venkataramanan and D. M. Divan, "Control of Pulse Width Modulated Resonant DC Link Inverter," in *Proceedings of IEEE IAS `92*, 1994, pp. 737-743.

[B10] G. Venkataramanan and D. M. Divan, "Pulse Width Modulation with Resonant DC Link Converters," *IEEE Transactions on Industry Applications*, Vol. 29, No. 1, Jan./Feb. 1993, pp. 113-120.

[B11] S. Chen and T. A. Lipo, "A Passively Clamped Quasi Resonant DC Link Inverter," in *Proceedings of IEEE IAS `94*, 1994, pp. 841-848.

[B12] S. Chen and T. A. Lipo, "A Novel Soft-switched PWM Inverter for AC Motor Drives," *IEEE Transactions on Power Electronics*, Vol. 11, No. 4, July, 1996, pp. 653-659.

[B13] H. Mao, J. Zhang, F. C. Lee, and D. Boroyevich, "Soft Switching DC-Link Techniques for Three-Phase AC-DC-AC PWM Converters," in *Proceedings of VPEC Annual Seminar `96*, 1996, pp. 173-179.

[B14] K. Wang, Y. Jiang, S. Dubovsky, G. Hua, D. Boroyevich, and F. C. Lee, " Novel DC-Rail Soft-Switched Three-Phase Voltage-Source Inverters," *IEEE Transactions on Industry Applications*, Vol. 33, No. 2, Mar./Apr. 1997, pp. 509-517.

[B15] J. J. Jafar and B. G. Fernandes, "A Novel Quasi-Resonant DC-Link PWM Inverter using Minimum Number of Switching Devices," in *Proceedings of IEEE APEC `99*, 1999, pp. 1285-1290.

[B16] J. J. Jafar and B. G. Fernandes, "A New Quasi-Resonant DC-Link PWM Inverter using Single Switch for Soft Switching," in *Proceedings of IEEE APEC `99*, 1999, pp. 1291-1297.

Load-side Soft-switching Topologies for Multi-phase Converters

[C1] W. McMurray, "SCR Inverter Commutated by an Auxiliary Impulse," *IEEE Transaction on Communications and Electronics*, Vol. 8-75, Nov/Dec., 1964, pp. 824-829.

[C2] W. McMurray, "Resonant Snubbers with Auxiliary Switches," in *Proceedings of IEEE IAS `89*, 1989, pp. 829-834.

[C3] R. W. De Doncker and J. P. Lyons, "The Auxiliary Resonant Commutated Pole Converter," in *Proceedings of IEEE IAS `90*, 1990, pp. 1228-1235.

[C4] I. Barbi and D. C. Martins, "A True PWM Zero-Voltage Switching Pole with very Low Additional RMS Current Stress," in *Proceedings of IEEE PESC `91*, 1991, pp. 261-267.

[C5] V. Vlatkovic, D, Borojevic, F. C. Lee, C. Cuadros, S. Gataric, "A New Zero-Voltage Transition, Three-Phase PWM Rectifier/Inverter," in *Proceedings of IEEE PESC `93,* 1993, pp. 868-873.

[C6] C. Caudros, D. Borojevic, S. Frame, V. Vlatkovic, H. Mao, and F. C. Lee, "Space Vector Modulated Zero-Voltage-Commutation Three-Phase to DC Bidirectional Converter," in *Proceedings of IEEE PESC `94*, 1994, pp. 16-23.

[C7] M. Ohsugi, T. Shimizu, G. Kimura, A. Toba, and S. Sano, "The Analyses of ZVS Turn-off Loss and the New Snubber Circuit for the ARCP Inverter," in *Proceedings of IEEE IECON `94*, 1994, pp. 316-321.

[C8] J. S. Lai, R. W. Young, G. W. Ott, C. P. White, J. W. McKeever, and D. Chen, "A Novel Resonant Snubber Inverter," in *Proceedings of IEEE APEC `95*, 1995, pp. 797-803.

[C9] H. Matsuo, K. Iida, and K. Harada, "High Power Soft-Switching PWMAC Auxiliary Power Supply System of the Electric Railway Rolling Stock and its Deadbeat Control," in *Proceedings of IEEE PESC `95*, 1995, pp. 258-263.

[C10] H. Mao and F. C. Lee, "An Improved Zero-Voltage-Transition Three-Phase Rectifier/Inverter," in *Proceedings of IPEC `95*, 1995, pp. 853-858.

[C11] S. Kondo and H. Katayama, "Neutral Point Voltage Fluctuation Suppression Control for Auxiliary Resonant Commutated Pole Inverter," *Transactions on Institute of Electrical Engineering of Japan - Part D*, Vol. 115-D, No. 4, April, 1995, pp. 373-378.

[C12] J. S. Lai, R. W. Young, G. W. Ott, J. W. McKeever, and F. Z. Peng, "A Delta Configured Auxiliary Resonant Snubber Inverter," *IEEE Transactions on Industry Applications*, Vol. 32, No. 3, May/Jun., 1996, pp. 518-525.

[C13] Q. Li, X. Zhou, and F. C. Lee, "A Novel ZVT Three-Phase Bidirectional Rectifier with Reduced Auxiliary Switch Stresses and Losses," in *Proceedings of IEEE PESC `96*, 1996, pp. 153-158.

[C14] R. L. Lin and F. C. Lee, "Novel Zero-Current-Switching Zero-Voltage-Switching Converters," in *Proceedings of IEEE PESC `96*, 1996, pp. 438-442.

[C15] H. Mao and F. C. Lee, "Novel Soft Switched Three-Phase Voltage Source Converter with Reduced Auxiliary Switch Stress," in *Proceedings of IEEE PESC `96*, 1996, pp. 443-448.

[C16] J. A. Pomilio, L. Rossetto, P. Tenti, and P. Tomasin, "Performance Improvement of Soft-Switched PWM Rectifier with Inductive Load," *IEEE Transactions on Industry Applications*, Vol. 12, No. 1, Jan. 1997, pp. 153-160.

[C17] J. S. Lai, "Resonant Snubber-Based Soft-Switching Inverters for Electric Propulsion Drives," *IEEE Transactions on Industrial Electronics*, Vol. 44, No. 1, Feb., 1997, pp. 71-80.

[C18] K. Iida, T. Sakuma, A. Mechi, H. Matsuo, and F. Kurokawa, "The Influence of the Conducting Inductance in the Auxiliary Resonant Commutated Pole Inverter," in *Proceedings of IEEE PESC `97*, 1997, pp. 1238-1245.

[C19] F. R. Salberta, J. S. Mayer, and R. T. Cooley, "An Improved Control Strategy for a 50-kHz Auxiliary Resonant Commutated Pole Converter," in *Proceedings of IEEE PESC `97*, 1997, pp. 1246-1252.

[C20] S. C. Frame, D. Katsis, D. H. Lee, D. Boroyevich, and F. C. Lee, "A Three-Phase Zero-Voltage-Commutation Inverter with Inductor Feedback," in *Proceedings of European Power Electronics Specialist Conference `97*, 1997, pp. 4708-4716.

[C21] P. Tomasin, "A Novel Topology of Zero-Current Switching Voltage-Source PWM Inverter for High-Power Applications," *IEEE Transactions on Industry Applications*, Vol. 13, No. 1, Jan. 1998, pp. 186-193.

[C22] K. Iida, H. Matsuo, T. Sakuma, and H. Ochiai, "A Novel Firing Control and Overcurrent Protection of the Main Power Switches in the ARCP Three Phase Inverter," in *Proceedings of IEEE PESC `98*, 1998, pp. 594-599.

[C23] X. Yuan and I. Barbi, "Soft-Switched Three Level Capacitor Clamping Inverter with Clamping Voltage Stabilization," in *Proceedings of IEEE APEC `99*, 1999, pp. 502-508.

[C24] X. Yuan and I. Barbi, "Control Simplification and Stress Reduction in a Modified PWM Zero Voltage Switching Pole Inverter," in *Proceedings of IEEE APEC `99*, 1999, pp. 1019-1025.

[C25] X. Yuan and I. Barbi, "A Transformer Assisted Zero Voltage Switching Scheme for the Neutral-Point-Clamped (NPC) Inverter," in *Proceedings of IEEE APEC `99*, 1999, pp. 1259-1265.

[C26] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee "A Novel ZVT Three-Phase Inverter with Coupled Inductors," in *Proceedings of IEEE PESC `99,* 1999, pp. 975-980.

[C27] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee "A SVM Strategy and Design of a ZVT Three-Phase Inverter for Electric Vehicle Drive Applications," in *Proceedings of IEEE IAS `99,* 1999, pp. 65-71.

[C28] X. Yuan and I. Barbi, "ARCPI Resonant Snubber for the Neutral-Point-Clamped (NPC) Inverter," in *Proceedings of IEEE IAS `99,* 1999, pp. 1157-1164.

[C29] X. Yuan and I. Barbi, "Analysis, Designing, and Experimentation of a Transformer-Assisted PWM Zero-Voltage Switching Pole Inverter," *IEEE Transactions on Power Electronics*, Vol. 15, No. 1, Jan. 2000, pp. 72-82.

[C30] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee, "Improved ZVT Three-Phase Inverter with Two Auxiliary Switches," in *Proceedings of IEEE APEC `00*, 2000, pp. 1023-1029.

[C31] Y. Li, F. C. Lee, J. Lai, and D. Boroyevich, "A Novel Three-Phase Zero-Current-Transition and Quasi-Zero-Voltage-Transition (ZCT-QZVT) Inverter/Rectifier with Reduced Stresses on Devices and Components," in *Proceedings of IEEE APEC `00*, 2000, pp. 1030-1036.

[C32] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee, "Phase-Lock Circuit for ZVT Inverters with Two Auxiliary Switches," in *Proceedings of IEEE PESC `00*, 2000, pp. 1215-1220.

[C33] Y. Li, F. C. Lee, J. Lai, and D. Boroyevich, "A Low Cost Three-Phase Zero-Current-Transition Inverter with Three Auxiliary Switches," in *Proceedings of IEEE PESC `00*, 2000, pp. 527-532.

[C34] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee, "Thyristor-assisted ZVT Inverters with Single Coupled Inductor for High Power Applications," in *Proceedings of IEEE IAS `00*, 2000, pp. 2156-2163.

[C35] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee, "A Novel ZVT Inverter with Simplified Auxiliary Circuit," in *Proceedings of IEEE APEC '01,* 2001, pp. 1151-1157.

[C36] Y. Li and F. C. Lee, "Design Considerations for a 50-kW Soft-Transition Inverter with Zero-Current and Near-Zero-Voltage Switching," in *Proceedings of IEEE APEC `01*, 2001, pp. 931-937.

[C37] Y. Li and F. C. Lee, "A Comparative Study of a Family of Zero-Current-Transition Schemes for Three-Phase Inverter Applications," in *Proceedings of IEEE APEC `01*, 2001, pp. 1158-1164.

[C38] **J.-Y. Choi**, D. Boroyevich, and F. C. Lee, "A Novel Inductor-Coupled ZVT Inverter with Reduced Harmonics and Losses," in *Proceedings of IEEE PESC '01,* 2001, pp.

[C39] Y. Li and F. C. Lee, "Design Methodologies for High-Power Three-Phase Zero-Current-Transition Inverters," in *Proceedings of IEEE PESC `01*, 2001, pp..

[C40] W. Dong, D. Peng, H. Yu, F. C. Lee, and J. Lai, "A Simplified Control Scheme for Zero Voltage Transition (ZVT) Inverter using Coupled Inductors," in *Proceedings of IEEE PESC '00,* 2000, pp. 1221-1226.

[C41] W. Dong, H. Yu, F. C. Lee, and J. Lai, "Generalized Concept of Load Adaptive Fixed Timing Control for Zero-Voltage-Transition Inverters," in *Proceedings of IEEE APEC '01,* 2001, pp. 179-185.

Soft-Switching Topology Evaluations

[D1] A. Cheriti, K. Al-Haddad, and D. Mukhedkar, "Calculation of Power Loss in Soft Commutated PWM Inverters," in *Proceedings of IEEE IAS `91*, 1991, pp. 782-788.

[D2] M. Dehmlow, K. Heumann, and R. Sommer, "Comparison of Semiconductor Device Losses in Hard Switched and Zero Voltage Switched Inverter Systems," in *Proceedings of EPE `93*, 1993, pp. 419-424.

[D3] J. S. Lai, R. W. Young, and J. W. McKeever, "Efficiency Consideration of DC Link Soft-Switching Inverters for Motor Drive Applications," in *Proceedings of IEEE PESC `94*, 1994, pp. 1003-1010.

[D4] J. S. Lai, R. W. Young, G. W. Ott, and J. W. McKeever, "Efficiency Modeling and Evaluation of a Resonant Snubber Based Soft-Switching Inverter for Motor Drive Applications," in *Proceedings of IEEE PESC `95*, 1995, pp. 943-949.

[D5] H. J. Beukes, J. H. R. Enslin, and R. Spee, "Performance of the Auxiliary Resonant Commutated Pole Converter in Converter Based Utility Devices," in *Proceedings of IEEE PESC `96*, 1996, pp. 1033-1039.

[D6] P. P. Mok, H.-J. Gutt, R. Spee, H. J. Beukes, and J. H. R. Enslin, "Control Complexities Related to High Power Resonant Inverters," in *Proceedings of IEEE PESC `96*, 1996, pp. 1040-1046.

[D7] K. M. Smith Jr. and K. M. Smedley, "A Comparison of Voltage-mode Soft-switching Methods for PWM Converters," *IEEE Transactions on Power Electronics*, Vol. 12, No. 2, March 1997, pp. 376-386.

[D8] C. Chen, X. Xu, and D. M. Divan, "Conductive Electromagnetic Interference (EMI) Noise Evaluation for An Actively Clamped Resonant DC Link Inverter (ACRDCLI)," in *Proceedings of IEEE IAS `97*, 1997, pp. 1550-1557.

[D9] M. Ehsani, K. M. Rahman, M. D. Bellar, and A. Severinsky, "Evaluation of Soft Switching for EV and HE Motor Drives," in *Proceedings of IEEE IECON `97*, 1997, pp. 651-657.

[D10] D. Katsis, M. Herwald, **J.-Y. Choi**, D. Boroyevich, and F. C. Lee, "Drive Cycle Evaluation of a Soft-Switched Electric Vehicle Inverter," in *Proceedings of IEEE IECON `97*, 1997, pp. 658-663.

[D11] M. D. Bellar, T. S. Wu, A. Tchamdjou, J. Mahdavi and M. Ehsani, "A Review of Soft-switched DC-AC Converters," *IEEE Transactions on Industry Applications*, Vol. 34, No. 4, Jul./Aug. 1998, pp. 847-860.

[D12] R. Teichmann and S. Bernet, "Investigation and Comparison of Auxiliary Resonant Commutated Pole Converter Topologies," in *Proceedings of IEEE PESC `98*, 1998, pp. 15-23.

[D13] **J.-Y. Choi**, M. Herwald, D. Boroyevich, and F. C. Lee, "Effect of Switching Frequency of Soft Switched Inverter on Electric Vehicle System," in *Proceedings of IEEE WPET `98*, 1998, pp..

[D14] W. Dong, **J.-Y. Choi**, Y. Li, H. Yu, J. Lai, D. Boroyevich, and F. C. Lee, "Efficiency Considerations of Load-side Soft-Switching Inverters for Electric Vehicle Applications," in *Proceedings of IEEE APEC '00,* 2000, pp. 1049-1055.

[D15] W. Dong, **J.-Y. Choi**, H. Yu, F. C. Lee, D. Boroyevich, and J. Lai, "Comprehensive Evaluation of Auxiliary Resonant Commutated Pole Inverter for Electric Vehicle Applications," in *Proceedings of IEEE PESC '01,* 2001, pp.

[D16] W. Dong, **J.-Y. Choi**, Y. Li, D. Boroyevich, S. Hiti, F. C. Lee, and J. Lai, "Comparative Experimental Evaluation of Soft-Switching Inverters for Electric Vehicle Applications," in *Proceedings of IEEE IAS Annual Meeting 01,* 2001, pp.

[D17] "Development of a Low-Cost High-Performance Electric Vehicle Inverter," *GE/DARPA project final report*, 1997.

[D18] "Soft-Switching Inverters for AC Adjustable Speed Drives," *PNGV project final report*, 2001.

Modeling and Control of PWM Converters

[E1] J. A. Houldsworth and D. A. Grant, "The Use of Harmonics Distortion to Increase the Output Voltage of a Three-Phase PWM Inverter," *IEEE Transactions on Industry Applications*, Vol. 20, No. 5, Sep./Oct. 1984, pp. 1124-1128.

[E2] H. W. Van Der Broeck, H. Skudelny, and G. V. Stanke, "Analysis and Realization of a Pulsewidth Modulator Based on Voltage Space Vectors," *IEEE Transactions on Industry Applications*, Vol. 24, No. 1, Jan./Feb. 1988, pp. 142-150.

[E3] C. T. Lim, D. Y. Hu, and G. H. Cho, "Transformers as Equivalent Circuits for Switches: General Proofs and D-Q Transformation-Based Analyses," *IEEE Transactions on Industry Applications*, Vol. 26, No. 4, Jul./Aug. 1990, pp. 777-785.

[E4] V. Vlatkovic, J. A. Sabate, R. B. Ridley, F. C. Lee, and B. H. Cho, "Small-Signal Analysis of the Zero-Voltage-Switched, Full-Bridge PWM Converter" in *Proceedings of IEEE HFPC `90*, 1990, pp. 262-272.

[E5] J. Holtz, "Pulsewidth Modulation – A Survey," in *Proceedings of IEEE PESC `92*, 1992, pp. 11-18.

[E6] V. R. Stefanovic and S. N. Vukosavic, "Space-Vector PWM Voltage Control with Optimized Switching Strategy," in *Proceedings of IEEE IAS `92*, 1992, pp. 1025-1033.

[E7] S. Legowski and A. M. Trzynadlowski, "Minimum-Loss Vector PWM Strategy for Three-Phase Inverter," in *Proceedings of IEEE PESC `93*, 1993, pp. 785-792.

[E8] L. Malesani and P. Tomasin, "PWM Current Control Techniques of Voltage Source Converters – A Survey," in *Proceedings of IEEE IECON `93*, 1993, pp. 670-675.

[E9] S. Hiti and D. Boroyevich, "Control of Front-End Three-Phase Boost Rectifier," in *Proceedings of IEEE APEC `94*, 1994, pp. 927-933.

[E10] S. Hiti, D. Boroyevich, and C. Cuadros, "Small-Signal Modeling and Control of Three-Phase PWM Converters," in *Proceedings of IEEE IAS `94*, 1994, pp. 1143-1150.

[E11] S. Korotkov, V. Meleshin, A. Nemchinov, and S. Fraidlin, "Small-Signal Modeling of Soft-Switched Asymmetrical Half-Bridge DC/DC Converter," in *Proceedings of IEEE APEC `95,* 1995, pp. 707-711.

[E12] R. Ambatipudi, D. Boroyevich, S. Hiti, and F. C. Lee, "Average and Small Signal Modeling of Zero-Voltage Transition Three-Phase PWM Boost Rectifier," in *Proceedings of IEEE PESC `95*, 1995, pp. 870-874.

[E13] C. Cuadros, C. Y. Lin, D. Boroyevich, R. Watson, G. Skutt, F. C. Lee, and P. Ribardiere, "Design Procedure and Modeling of High-Power, High-Performance, Zero-Voltage Zero-Current Switched, Full-Bridge PWM Converter," in *Proceedings of IEEE APEC `97*, 1997, pp. 790-798.

[E14] V. H. Prasad, D. Boroyevich, and S. Dubovsky, "Comparison of High Frequency PWM Algorithms for Voltage Source Inverters," in *VPEC Seminar Proceedings,* 1997, pp. 115-122.

[E15] C. Cuadros, S. Chandrasekaran, K. Wang, D. Boroyevich, and F. C. Lee, "Modeling, Control and Implementation of Quasi-Single Stage Three-Phase Zero-Voltage Zero-Current Switched Buck Rectifier," in *Proceedings of IEEE APEC `99*, 1999, pp. 248-254.

[E16] B. T. Kuhn, S. D. Sudhoff, and C. A. Whitcomb, "Performance Characteristics and Average-Value Modeling of Auxiliary Resonant Commutated Pole Converter Based Induction Motor Drives," *IEEE Transactions on Energy Conversion,* Vol. 14, No. 3, Sep., 1999, pp. 493-499.

[E17] C. Cuadros and D. Boroyevich, "Accurate Large Signal Modeling of Zero-Voltage Zero-Current Switched, Full-Bridge PWM Converter,"

[E18] S. Hiti and D. Boroyevich, "Small-Signal Modeling of Three-Phase PWM Modulators," in *Proceedings of IEEE PESC `96*, 1996, pp. 550-555.

Motor Losses and Degradation

[F1] F. G. De Buck, "Losses and Parasitic Torques in Electric Motors Subjected to PWM Waveforms," *IEEE Transactions on Industry Applications,* Vol. IA-15, No. 1, Jan/Feb. 1979, pp. 47-53.

[F2] K. Venkatesan and J. F. Lindsay, "Comparative Study of the Losses in Voltage and Current Source Inverter Fed Induction Motors," *IEEE Transaction on Industry Applications*, Vol. IA-18, No.3, May/Jun. 1982, pp. 240-246.

[F3] F. De Buck, P. Gistelinck, and D. De Backer, "A simple but Reliable Loss Model for Inverter-Supplied Induction Motors," *IEEE Transaction on Industry Applications*, Vol. IA-20, No.1, Jan./Feb. 1984, pp. 190-202.

[F4] E. C. Andersen and K. Bieniek, "On the Torques and Losses of Voltage- and Current-Source Inverter Drives," *IEEE Transaction on Industry Applications*, Vol. IA-20, No.2, Mar./Apr. 1984, pp. 321-327.

[F5] A. H. Bonnett, "Analysis of the Impact of Pulse-Width Modulated Inverter Voltage Waveform on AC Induction Motors," *IEEE Transaction on Industry Applications*, Vol. 32, No.2, Mar./Apr. 1996, pp. 386-392.

[F6] G. Skibinski, D. Leggate, and R. Kerkman, "Cable Characteristics and Their Influence on Motor Over-Voltages," in *Proceedings of IEEE APEC `97*, 1997, pp. 114-121.

[F7] R. J. Beeckman, J. J. Harber, and S. J. Wentz, "Study on Magnet Wire Degradation with Inverter Driven Motors," in *Proceedings of IEEE EEIC/EMCW `97*, 1997, pp. 383-387.

VITA

Jae-Young Choi

The author was born in Ulsan City, Korea on May 5th, 1965. He received his B. S. and M. S. degrees from Department of Electrical Engineering, Seoul National University, Korea in 1988 and 1990, respectively. His master thesis was about a current-source three-phase four-leg active power filter. From 1990 to 1996, he worked for LG Electronics Ltd., Korea as a research engineer. He joined several R&D projects that developed inverter built-in motors, high-torque induction motors for electric vehicles, and a linear compressor controller. His major tasks were the development of motor controllers.

In August 1996, he joined Virginia Power Electronics Center (VPEC), Virginia Tech as a graduate research assistant. His research works have been concentrated on soft-switching topologies for motor drive applications. His research interests are soft-switching topologies for multi-phase converters, motor controls, and power distribution systems.

The author has been a student member of both IEEE Power Electronics Society and IEEE Industry Applications Society since 1999.