Investigation on Interleaved Boost Converters and Applications

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Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

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July 21st, 2009
Blacksburg, Virginia

Keywords: Boost Converter, Power Factor Correction (PFC), Multi-Channel Interleaving, Phase Angle Control

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(Abstract)

With the rapid evolving IT technologies, today, the power factor correction (PFC) design is facing many challenges, such as power scalability, high entire-load-range efficiency, and high power density. Power scalability is a very desirable and cost-effective approach in the PFC design in order to keep up with servers' growing power requirements. Higher power density can eventually reduce the converter cost and allows for accommodating more equipment in the existing infrastructures. Driven strongly by economic and environmental concerns, high entire-load-range efficiency is more and more required by various organizations and programs, such as the U.S. Energy Star, Climate Savers, and German Blue Angel. Today, the existing boost PFC is reaching its limitations to meet these challenges simultaneously. Using the cutting-edge semiconductor devices, further efficiency improvement at light load is still needed. There are limited approaches available for increasing the power density due to the large EMI filter and inductor size.

Interleaved multi-channel boost PFC is a promising candidate to meet those challenges, but the interleaved boost converter is a less explored area. On the other hand, the multi-channel interleaved buck converter for the VR application has been intensively studied and thoroughly explored. One basic approach of this study is trying to extend the existing knowledge and techniques obtained from multiphase buck converters to the multi-channel interleaved boost converters since there are similarities existed between the multi-phase buck and the multi-channel boost converters.

The existing studies about the interleaving impact on the EMI filter design are based on the time domain ripple cancellation effect. This approach is good enough for most of the filter designs. However, unlike the conventional filter designs, the EMI filter design is a specification related process. Both the EMI standard and the EMI measurement are based

on the frequency domain spectrum. Limited by the existing analysis approaches, it is difficult to provide a clear picture about how exactly the multi-channel interleaving will impact the EMI filter design. The interleaving impact on the Common Mode (CM) noise also has not been studied in any existing literatures for the same reason. In this study, the frequency domain analysis method was adopted. With the double Fourier integral transformation, a closed-form expression of all the harmonics of the noise sources can be obtained. With all the detailed phase relationship of the switching frequency harmonics and all the side band harmonics, the multi-channel interleaving impact on both the differential mode (DM) and CM filter design can be clearly understood and summarized. According to the design curves provided, the EMI filter size can be effectively reduced by properly choosing the interleaving channel number and the switching frequency. The multi-channel interleaving impact on the output capacitor current ripple is also studied and summarized in this dissertation.

It should be pointed out that interleaving only reduces the total input and output current ripples; the inductor current in each channel still has large ripple if small inductance is used. Similar to the multi-phase buck converter, coupling inductors result in different equivalent inductances for input current ripple and inductor current ripple for boost converters. Keeping the inductor current ripple magnitude the same, inverse coupling inductors between the interleaved channels can reduce the inductor size. However, the DM filter size is increased due to larger input current. Based on the investigation on the total magnetic component weight, inverse coupling inductor can reduce the total magnetic component weight. The reduction is more pronounced for lower switching frequency design when the inductor size is dominating among the total magnetic components.

Based on the harmonic cancellation, and with all the detailed phase relationship of the switching frequency harmonics and all the side band harmonics, a novel phase angle control method is proposed to maximize the reduction of the EMI filter. For example, in a 2-channel interleaved PFC, just by changing the interleaving scheme to 90 degree phase shift, 39% total volume reduction of the EMI filter can be achieved. The proposed phase angle controlled multi-channel PFC is experimentally demonstrated and verified on a digital controlled 4-channel PFC. The phase angle control method proposed in the multi-channel boost converter can be applied back to the multi-phase buck converter as well. The

harmonic cancellation principle will be the same as the multi-channel boost converter. The same benefits can be obtained when the requirement is defined in the frequency domain, e.g. the EMI Standard.

The interleaved multi-channel configuration makes it possible to implement the phase-shedding to improve the PFC light load efficiency. By decreasing the number of active channels according to the load, the PFC light load efficiency can be optimized. However, shedding phases can reduce the ripple cancellation effect as well, which will result in the EMI noise increase and losing the benefit on the EMI filter. By applying the proposed phase-shedding with phase angle control strategy, the phase shedding impact on the EMI filter design can be minimized. The light load efficiency can be improved without compromising the EMI filter size. Then, adaptive frequency controlled PFC is proposed to further improve the PFC light load efficiency. The proposed light load efficiency improvement strategies are combined and implemented on the platform of the digital controlled 4-channel PFC. The benefit of improving the light load efficiency is experimentally verified. The EMI performance is also evaluated with the EMI measurement results obtained from the PFC prototype.

Following the same approach explored, the benefits of interleaved boost converter can be further extended other applications, such as the boost converter in the Hybrid Electric Vehicles (HEV) and photovoltaic (PV) system.

To my family:

My parents: Huanhua Wang and Huizhu Ni

My sister: Yuling Wang

Acknowledgments

I would like to express my deep and sincere gratitude to my advisor, Dr. Fred C. Lee, for his continuous guidance, encouragement and support. His broad knowledge and his logical way of thinking have been of great value for me. What I learned from him is something beyond just solving technical problems. I am also deeply grateful to my advisor Dr. Ming Xu, for his enthusiastic help during my research at CPES. His understanding, insightful suggestions, encouraging and personal guidance have provided a great basis for my research. Without his continuously encouragement and support, I would not be able to finish my Ph. D study successfully. It is an honor to be one of their students here in the Center for Power Electronics Systems (CPES), the Top-One in the list of power electronics places around the whole world.

I am grateful to the other members of my advisory committee, Dr. Dushan Boroyevich, Dr. William T. Baumann, and Dr. Linbing Wang for their support, comments, suggestions and encouragement.

It has been a great pleasure to work in CPES, not only because of the talented colleagues but also the friendship. I would like to thank Dr. Bing Lu, Dr. Yang Qiu, Dr. Wei Dong, Mr. Yonghan Kang, Dr. Francisco Canales, Dr. Peter Barbosa, Dr. Julu Sun, Dr. Shuo Wang, Dr. Kaiwei Yao, Dr. Linyin Zhao, Dr. Rengang Chen, Dr. Jia Wei, Dr. Jinghai Zhou, Dr. Yuancheng Ren, Dr. Jinghong Guo, Dr. Xigen Zhou, Mr. Yu Meng, Mr. Xiangfei Ma, Dr. Wei Shen, Dr. Huiyu Zhu, Dr. Jian Yin, Dr. Wenduo Liu, Dr. Ning Zhu, Dr. Ching-Shan Leu, Mr. Doug Sterk, Dr. Kisun Lee, Mr. Dianbo Fu, Dr. Yan Jiang, Dr. Jian Li, Dr. Pengju Kong, Dr. Jing Xu, Dr. Yan Liang, Dr. Michele Lim, Dr. Chucheng Xiao, Dr. Hongfang Wang, Dr. Honggang Sheng, Dr. Rixin Lai, Mr. Bin Huang, Mr. Ya Liu, Mr. Yan Dong, Mr. Qiang Li, Mr. Qian Li, Mr. Zheng Luo, Mr. Yi Sun, Mr. Pengjie Lai, Mr. Zijian Wang, Mr. Daocheng Huang, and Mr. Yucheng Ying, It was real a honor working with you guys.

I would also like to thank the wonderful members of the CPES staff who were always willing to help me out, Ms. Teresa Shaw, Ms. Linda Gallagher, Ms. Teresa Rose,

Ms. Ann Craig, Ms. Marianne Hawthorne, Ms. Elizabeth Tranter, Ms. Linda Long, Mr. Robert Martin, Mr. Jamie Evans, Mr. Dan Huff, Mr. Gary Kerr, and Mr. David Fuller.

My heartfelt appreciation goes toward my parents, Huanhua Wang and Huizhu Ni, who have always provided support and encouragement throughout my further education.

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Chapter 1. Introduction

1.1 Research Background - Interleaving technique

The concept of interleaving, or more generally that of increasing the effective pulse frequency of any periodic power source by synchronizing several smaller sources and operating them with relative phase shifts, is not new [1]. Interleaving technique actually exists in different areas of moden technologies in different forms. Take a typical automobile engine as an example. In today's internal combustion engine, several cylinders are connected to a common crankshaft and that the power stroke portions of their cycles are non-simultaneous. By firing each cylinder in sequence, the effective pulse frequency of the engine is increased and the net torque ripple is reduced. Increasing the number of cylinders raises the pulse frequency and total output power of the engine without increasing the firing frequency of the individual cylinders. This could be considered as a very good example of interleaving technique being applied in the field of mechnical engineering.

In the field of power electronics, application of interleaving technique can be traced back to very early days, especially in high power applications. In high power applications, the voltage and current stress can easily go beyond the range that one power device can handle. Multiple power devices connected in parallel and/or series could be one solution. However, voltage sharing and/or current sharing are still the concerns. Instead of paralleling power devices, paralleling power converters is another solution which could be more beneficial. Furthermore, with the power converter paralleling architecture, interleaving technique comes naturally. Benefits like harmonic cancellation, better efficiency, better thermal performance, and high power density can be obtained. In earlier days, for high power applications, in order to meet certain system requirement, interleaving multi-channel converter could be a superior solution especially considering the available power devices with limited performance at that time. One of such example can be found in the application of Superconducting a Magnetic Energy Storage System (SMES) [2]. The current stress of such application is extremely high, yet certain system performance still

need to be met. On the ac side, the total harmonic distortion (THD) in voltages and currents of the regulatory standards must be respected. A further constraint comes from the switching loss that is proportional to the valve switching frequency. The proposed solution in the referred paper consists of using multiple interleaved three-phase current-source converters. With this multimodular converters the current stress can be divided to a level that can be handled by gate turn-off thyristor (GTO), the static induction thyristor (SI), etc, and reduces the ohmic component of their conduction losses. The results shows interleaving technique was applied quite successful in this application. Such examples also can be found in many other applications, such as Static VAR Generator (SVG) [3], high-voltage direct current (HVDC) applications [4], etc.

Interleaving technique was also investigated in the early days for the smaller power spacecraft, satellite or avionic applications, and was introduced as unconventional SMPS power stage architecture [5][6][7]. In such applications, one major concern is the input and output filters rely almost exclusively on tantalum capacitors due to the highest available energy-storage-to-volume ratio at that time. However, the ESR of this filter capacitor causes high level thermal stress from the high switching pulsed current. The input and output filter capacitance is usually determined by the required number of capacitors sufficient to handle the dissipation losses due to the ripple current. Interleaving multiple converters can significantly reduce the switching pulsed current go through the filter capacitor. By properly choosing the channel number with considering the duty cycle, the ripple current may be reduced to zero. Further more, interleaving increases the ripple frequency to be n (n is the total channel number) times the individual switching frequency. The ESR of the tantalum capacitors is inversely proportinal to the frequency. Interleaving technique can effectively reduce the filter capacitor size and weight. Another concern of this application is packaging. Due to the thermal management issues, the power loss of non-interleaved converter exceeds the typical dissipation capability of a slot mount circuit packaing card. In addition, the substantial bulky converter usually requires a custom designed mainframe. Interleaving technique can divide the power transfer into multiple modules, lighter and smaller parts can be mounted on the printed circuit card. Each module has limited power loss which the slot mounted cards can conduct away. The third concerns of such application lies in the necessity to redesign virtually the entire power supply in the

event that higher power levels are required than initially specified at start of the design. With the interleaving architecture, increased output power may be supplied by adding additional identical modules. The interleaved converter was designed and developed which can well demonstrate the benefits on input/output filter, packaging, and modularity.

Interleaving technique has been studied and investigated in varieties of applications and systems, as reflected in the literature [1] - [16]. Among these studies, the multi-channel interleaved buck converter for the Voltage Regulator (VR) application has been intensively studied and thoroughly explored [12][13][14][15][16].

1.2 Review of Multi-Phase Buck for VR Application

Since 1971, when the first microprocessor, Intel's 4-bit 4004 chipset, was released, more and more transistors have been integrated into the microprocessor, following Moore's Law, which states that the number of components on an integrated circuit doubles roughly every two years. Figure 1.1 shows the historical data of the number of transistors integrated into Intel's microprocessor [17]. The dual-core processor, which was released in 2006, has more than one billion transistors in it.

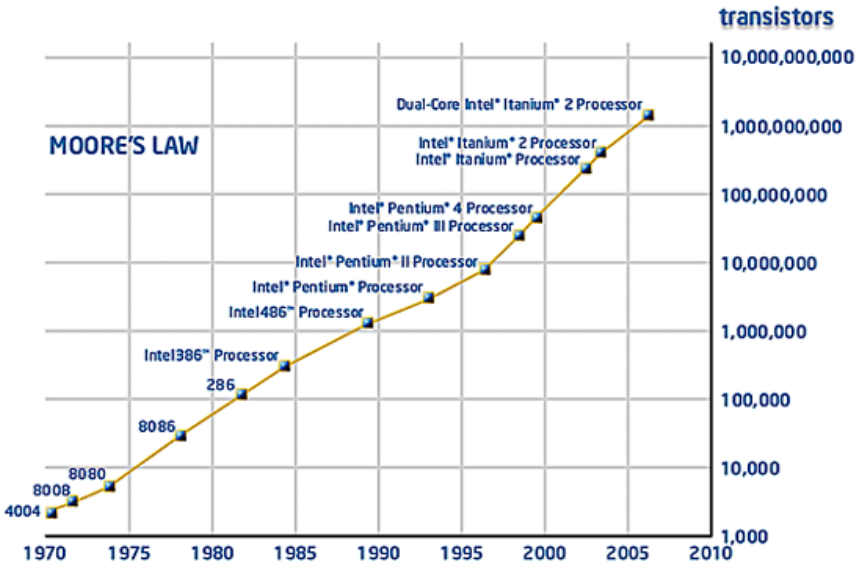


Figure 1.1. The number of transistors integrated on the die for Intel microprocessors. [17]

More integrated transistors leads to better computing performance. However, with more transistors packed into smaller spaces, more power are needed to suppy the microprocessors as well. Since all the electric power consumed by the microprocessor is transferred to heat eventually, new power management technologies for the transisters have been introduced in the past decade. One of the soultions is to decrease the microprocess supply voltage. Starting with the Intel Pentium processor, microprocessors began to use a non-standard voltage which is less than 5V. Therefore, the VR is introduced as the dedicated power supply for the microprocessors. The distributed power system (DPS) architecture with the VR is shown in Figure 1.2.

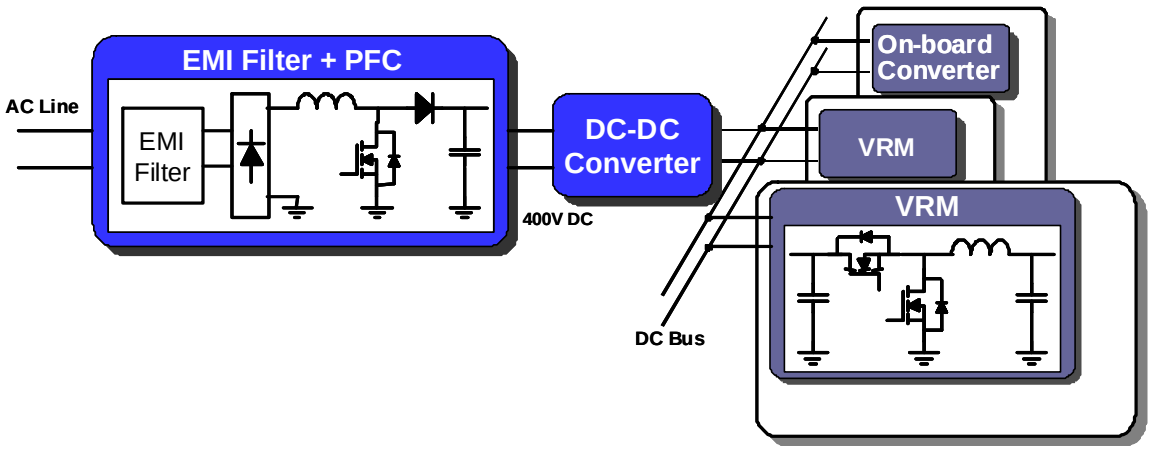


Figure 1.2. Distributed power system architecture with single-phase VR.

For the older generation microprocessor VR, a single conventional buck or synchronous buck topology, as shown in Figure 1.2, is utilized for power convertion [18][19][20]. As the microprocessors power consumption increase coninuously, it becomes impossible for a single device to handle the high current stress. Normally, more devices are used in parallel, as shown in Figure 1.3. The bulk capacitor is used for energy storage, and the decoupling capacitor is nearer to the processor in order to limit the transient voltage spike. To meet the future voltage regulation specification, it was deemed necessary to increase the decoupling capacitor by a factor of 23 and the VRM bulk capacitor by a factor of 3 [21][22]. This is not a practical solution, for two reasons. Firstly, there is simply not enough real estate in the motherboard to accommodate such a large increase in the number of capacitors. Secondly, the cost increase would also be significant.

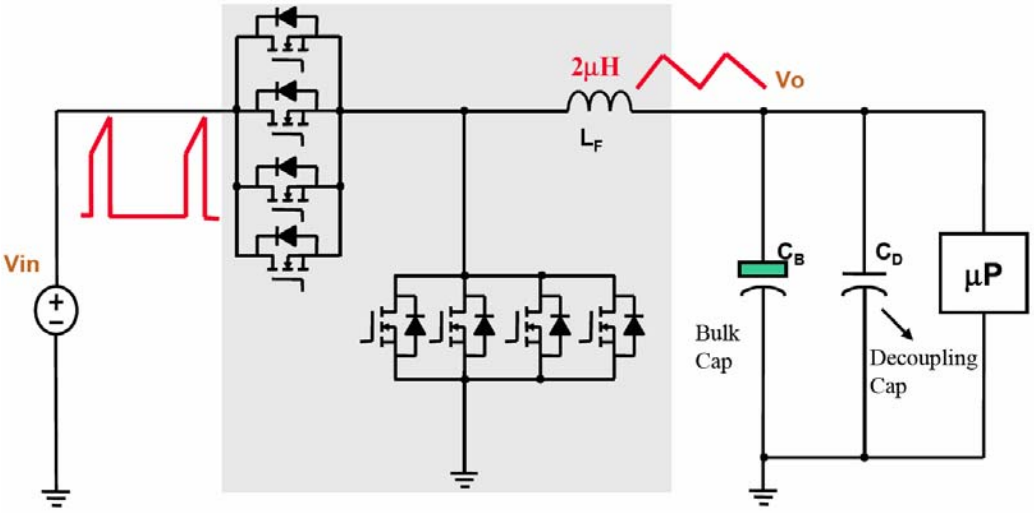


Figure 1.3. Single-phase synchronous buck converter with paralleling devices.

With the computing speed continuously increasing, the power consumption of CPUs is also trended higher, as shown in Figure 1.4. CPU current increases from 20A to 100A range, and is expected continuously increase beyond 140 A in the near future. Figure 1.4 shows the road map of voltage and current of Intel microprocessors' power [23].

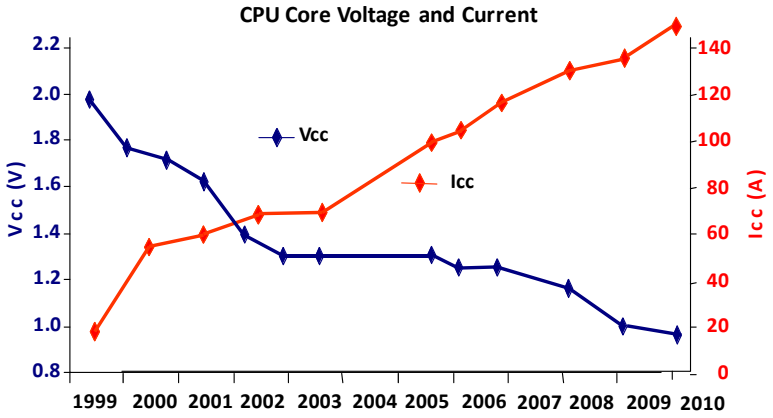


Figure 1.4. Intel microprocessors' power road map.

Instead of paralleling devices, VPEC/CPES proposes multi-phase interleaved buck converter, as shown in Figure 1.5 [12][22]. The multi-phase buck has benefits such as better transient performance, power scalability characteristics, better light load efficiency, etc. The concept of applying interleaving to VRs is so successful that it has become an industry standard practice in the VR applications. A number of companies (National

Semiconductor, Semtech, Intersil, Maxim, Linear Technology, Analog Device, Fairchild Semiconductor, Texas Instruments and STMicroelectronics) have developed their IC controllers to facilitate the implementation of the proposed multiphase approach.

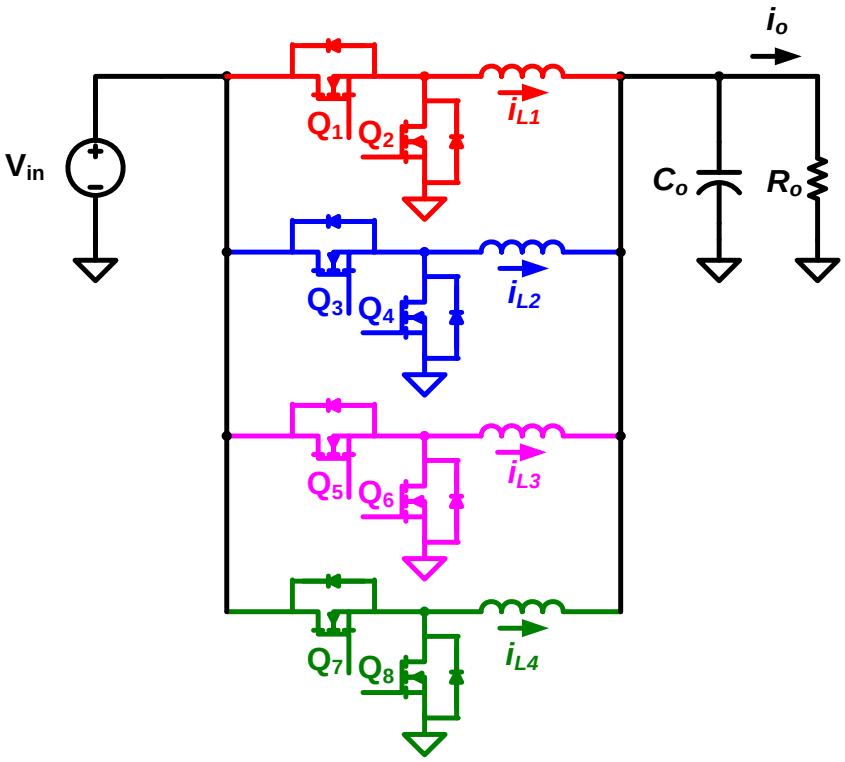


Figure 1.5. A multi-phase interleaved synchronous buck converter.

a. Less output filter capacitor

With the microprocessors' load transition speeds increase, the voltage deviation window during the transient is becoming smaller and smaller, since the output voltage keeps decreasing. The low votlage, high current, fast load transient speed, and the tight voltage regulation impose challenges on the VR design of the microprocessors.

In order to reduce the VR output capacitance to save the total cost and to increase the power density while still meet all the VR specifications, high inductor current slew rates are preferred. The single-phase buck VRs use large output filter inductance, which limits the energy transfer speed. In order to greatly increase the transient inductor current slew

rate, the inductances need to be reduced significantly, as compared with those in conventional designs. On the other hand, small inductances result in large current ripples in the circuit's operation at the steady state. The large current ripple usually causes a large turn-off loss. In addition, it generates large steady-state voltage ripples at the VR output capacitors. The steady-state output voltage ripples can be so large that they are comparable to transient voltage spikes. It is impractical for the converter to work this way.

The multi-phase interleaved buck converter consists of *n* identical converters with interconnected inputs and outputs. Each converter utilizes an inductor that is about *1/10* the size of the original. As a result, these mini-converter cells can quickly and efficiently transfer power to the microprocessor. Furthermore, these cells are controlled by phase-shifting their gate signals. The proposed interleaving approach not only results in cancellation of the current ripple generated at the output of each converter cell, as shown in Figure 1.6, but also increases its effective ripple frequency, and thus reduces by a factor of 10 the output filter capacitor requirement. In 1997, the immediate benefits of using the multiphase approach were demonstrated in the prototype hardware, which showed a six-fold improvement in power density, a threefold reduction in profile, and a fourfold improvement in its transient response [15].

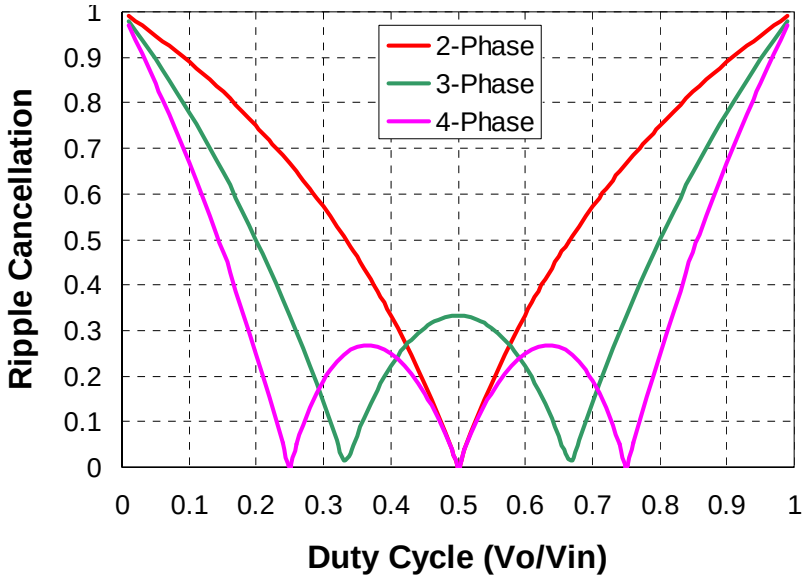


Figure 1.6. Current ripple cancellations in multiphase VRs.

b. Better power scalability characteristics

Due to the rapid evolving IC technologies, the CPUs as products have relatively short lifespan in the market. As shown in Figure 1.7, the power consumption of the two major CPU makers, AMD and Interl, are continuously increasing the the past decades [24]. New designs are needed for the single-phase buck converters to meet the power consumption requirement of every new generation of the CPUs. It is time consuming and not cost effective.

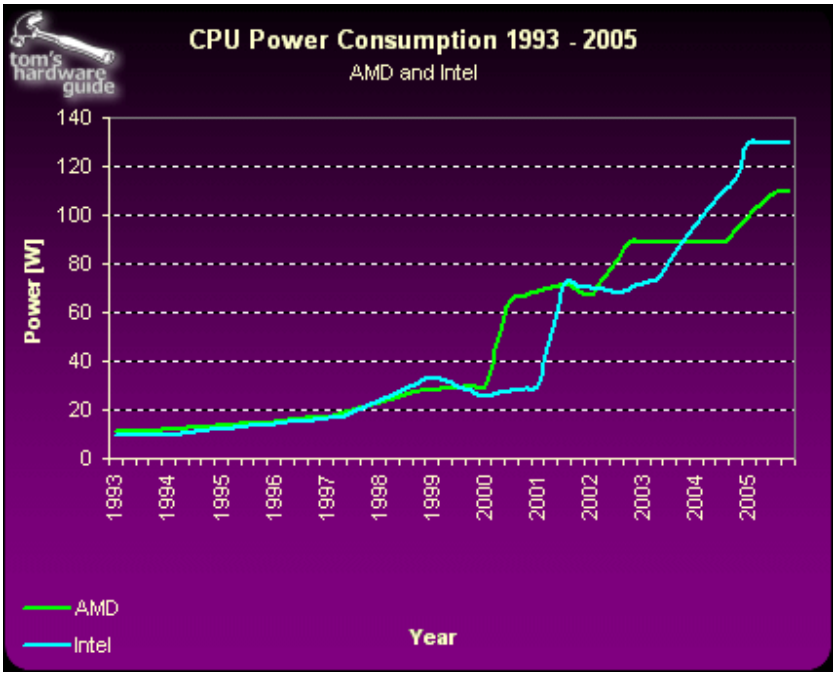


Figure 1.7. AMD and Intel CPU power consumption 1993 - 2005. [24]

The power scalability characteristics of the multi-phase buck make it very attractive in terms of its ability to keep step with the microprocessor power requirement. The number of the paralleled phases can be configured according to the power requirement of the CPU. Today, after several years optimization, the 20 A rating buck converter cells are becoming a standard approach. Since the cells are identical, the design and manufacturing can be much easier and faster with lower cost.

c. Better light load efficiency

Light-load efficiency of the VR is very important, since the CPU goes into sleep state very frequently to save power. When the computer is in hibernate mode, or when there is no software running, the operating system (OS) sends a signal through the advanced configuration and power interface (ACPI), and the system goes into sleep mode. When the CPU goes into sleep mode, the clock frequency and the supply voltage are reduced. The light-load efficiency is particularly important for laptop voltage regulators, since the laptop VR goes to sleep about 80% of the time, and light-load efficiency is very important for battery life extension.

Figure 1.8 shows an example of the light-load efficiency expectation from Intel. The expected efficiency is 90% for the active state (9A to 45A), 80% at 1A, and 75% at 300mA for the sleep state. Since the fixed power loss, which consists of gate driving losses, core losses, etc., becomes dominant at light load, it is very challenging to meet the efficiency requirement.

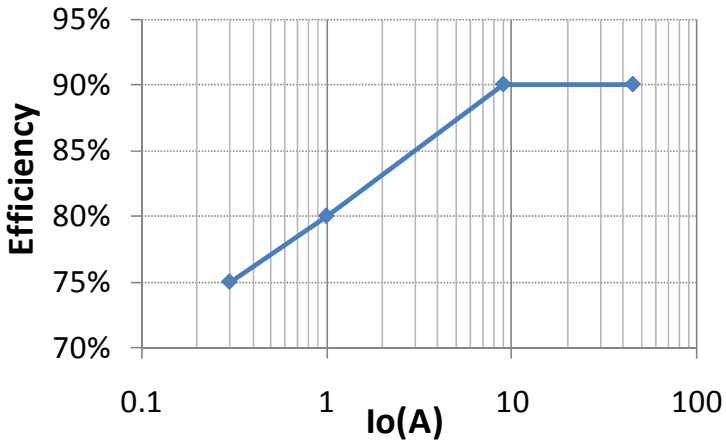


Figure 1.8. Light-load efficiency target for laptop voltage regulators.

With the multiphase interleaved architecture, phase shedding to improve light-load efficiency becomes possible. Optimal number of phases (ONP) was proposed to improve the VR efficiency at light load conditions [25]. Reducing the number of active channels accordingly can result in an efficiency increase at light load, as shown in Figure 1.9.

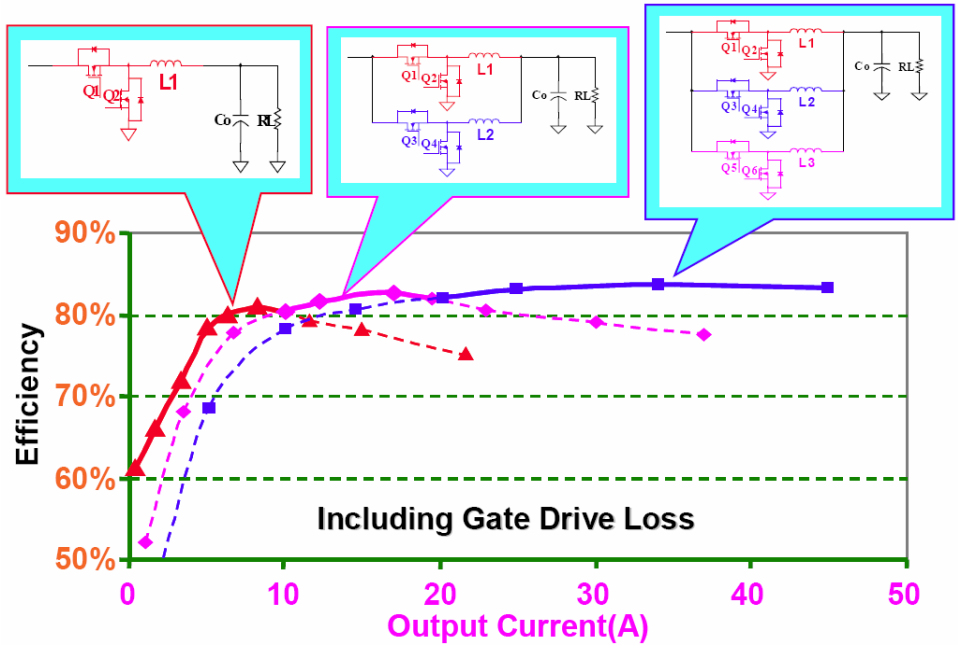
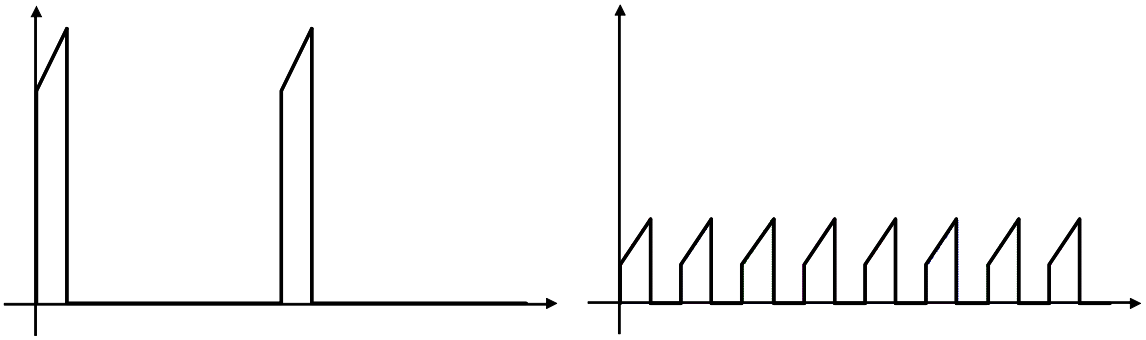


Figure 1.9. Efficiency improvement by applying optimal number of phases for VR applications. [25]

d. Smaller input filter capacitor

In the same way, the interleaving approach can also significantly reduce the input filter capacitor requirement.



(a) Single-phase buck converter **(b) 4-phase buck converter**

Figure 1.10. Input current comparison of single-phase buck and 4-phase buck.

The input ripple current waveform of single-phase buck converter and 4-phase buck converter is shown in Figure 1.10. The current ripple is greatly reduced by interleaving.

Current ripple reduction can either reduce the input filter capacitor size or prolong the input capacitor life time by reducing the power loss of the electrolytic capacitor.

Not only the ripple magnitude is reduced, the ripple frequency increased four times as well. Considering both the magnitude and the frequency factors, the input capacitor filter requirement can be significantly reduced.

e. Coupled inductor for multi-phase buck

Ripple cancellation is one of the important features of interleaving technique. However, it is important to note that interleaving only reduces the total input and output current ripple; the inductor current in each channel still has large ripples if small inductances are used. The large conduction and switching losses in the MOSFET and the copper losses in the inductors that occur due to the large current ripples are problems that cannot be solved by interleaving technique. Therefore, coupled inductor concept is introduced to the multiphase interleaved buck converter. The benefit of coupled inductor can be summarized as follows.

- Less component counts
- Smaller channel inductor current ripple
- Improve the steady-state efficiency

Besides the benefits mentioned above, the multiphase buck converter makes the thermal dissipation more evenly distributed. Studies also show that in high-current applications, the overall cost of the converter can be reduced using this technology. Therefore, it has become an industry standard practice in the VR applications, as shown in Figure 1.11.

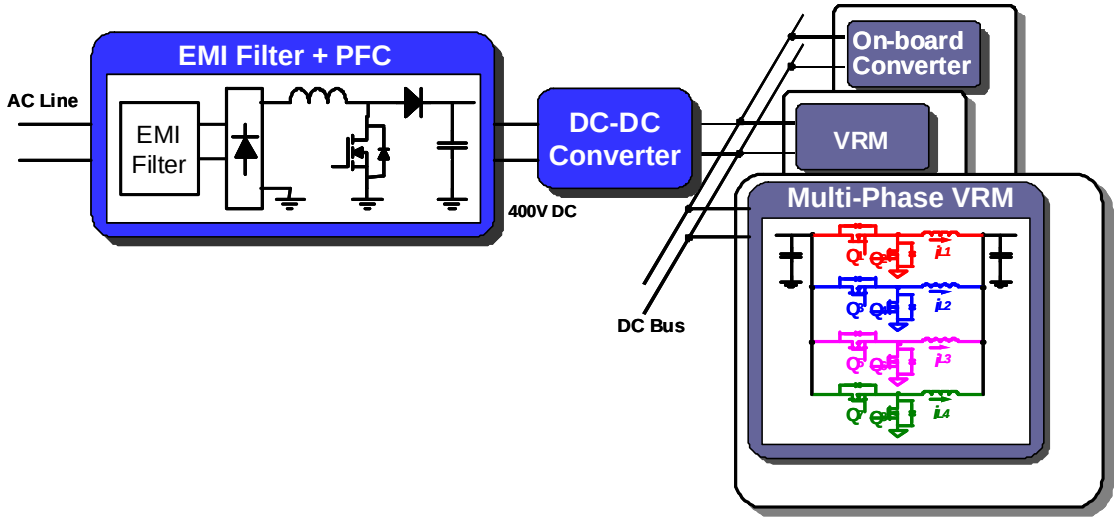


Figure 1.11. Distributed power system architecture with multi-phase VR.

1.3 Interleaved Boost Converters for AC-DC Front-End Converter Application

A great portion of electrical and electronic devices currently in use is designed to operate using direct current (DC) power while, for reasons of distribution efficiency, most power is ultimately delivered to such devices as alternating current (AC) power. Therefore, the AC-DC front-end converter is needed to converter the AC power to the DC power in many electrical and electronic devices. Two-stage approach is widely used in the AC-DC front-end converters for high power application. Because of its continuous input current and simplicity, Continuous Conduction Mode (CCM) boost topology, as shown in Figure 1.12, is the most popular topology for the power factor correction (PFC) stage.

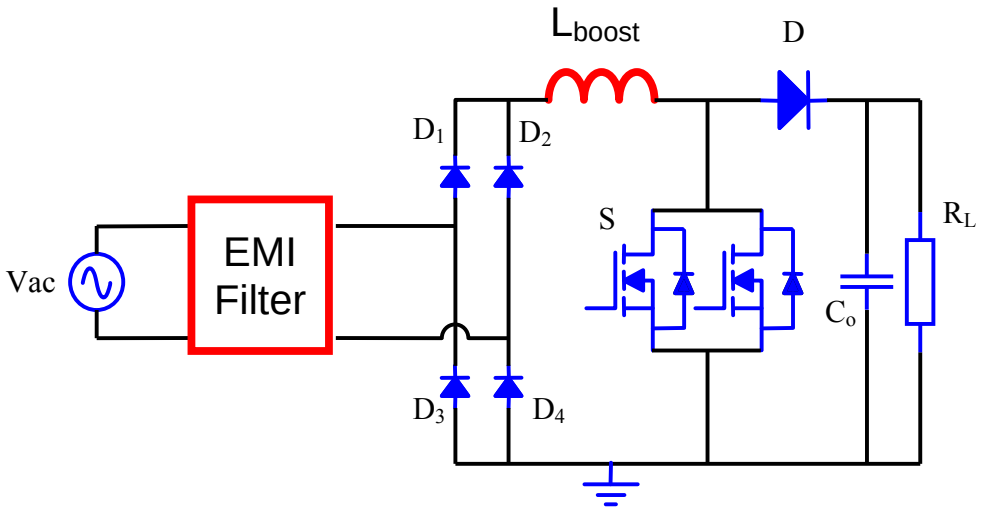


Figure 1.12. CCM boost topology for PFC application.

1.3.1 Design challenges for AC-DC front-end converters

High power density, high efficiency, and power scalability are becoming more and more desired for the AC-DC front-end converters in the distributed power systems. Higher power density can eventually reduce the converter cost and allows for accommodating more equipment in the existing infrastructures. Driven strongly by economic and environmental concerns, high entire-load-range efficiency is more and more required by various organizations and programs, such as the U.S. Energy Star [26], Climate Savers [27], and German Blue Angel [28]. Due to the rapid evolving IC technologies, the AC-DC front-end converters as products in the market have relatively short lifespan. Power scalabiltiy characteristics are important features to cost effective solutions. This continuously increasing power density and efficiency target, and the power scalability requirement pose challenges for today's AC-DC front-end converter technology.

a. High efficiency

80 plus is a basic efficiency requirement for the front-end converter, as shown in Figure 1.13. It requires the efficiency to be higher than 80% at 20%, 50%, and 100% load. Other than the 80 plus requirement, Climate Savers is targeting at higher efficiency. It even

target to achieve 4% or 3% efficiency improvement every year in these coming two years. By June, 2010, it is expected to achieve 88% efficiency at 20% and 100% load, and 92% effciency at 50% load. The computer giant, Dell, is targeting at even more aggressive effciencies, as shown in Figure 1.13. Not only the efficiency target is set higher, but also 10% and 5% load efficiency is required.

Based on these activity of varies organizations and companies, the trend is that the efficiency requirement keeps increasing and is extending to lighter load conditions. Today, the power supply industry is at the beginning of a major focus shift that puts efficiency improvements across the entire load range. This focus on efficiency has been prompted by economic reasons and environmental concerns caused by the continuous, aggressive growth of the Internet infrastructure and a relatively low energy efficiency of power delivery systems of large Internet-equipment hosting facilities [29].

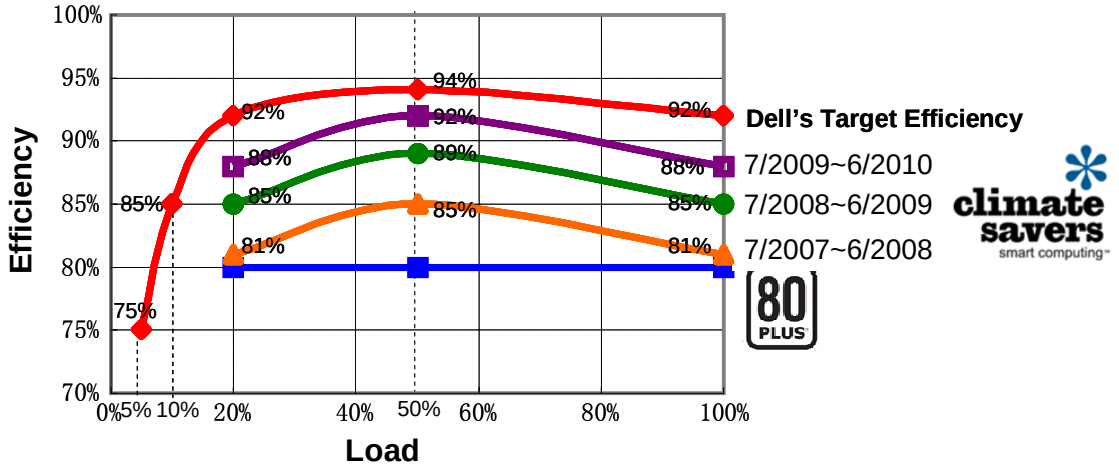


Figure 1.13. Efficiency requirement for AC-DC front-end converters.

The conduction loss and the reverse recovery loss used to be a big limitation to the efficiency of the power factor correntionn (PFC) stage. With the advancement in the power semiconductor device technologies, the PFC efficiency has been improved significantly in the past decades. The on-resistance of today's high voltage MOSFETs has been reduced approximately ten times compared to the same voltage rating MOSFETs available in the nineties by super-junction technologies. For example, the on-resistance of the CoolMOS IPW60R099CS, developed by Infineon, is only 99 mΩ. With this super-junction technology, even lower on-resistance can be achieved with larger die size. By adopting

CoolMOS devices, the MOSFET conduction loss is not a dominating factor in the PFC effciency anymore. Similarly, today's high-voltage ultra-fast recovery diode can achieve much better reverse recovery performance, which greatly reduced the switching related losses. Furthermore, with the introduction of the high voltage silicon carbide (SiC) Schottky diodes, the PFC diode reverse recovery loss problem is virtully eliminated.

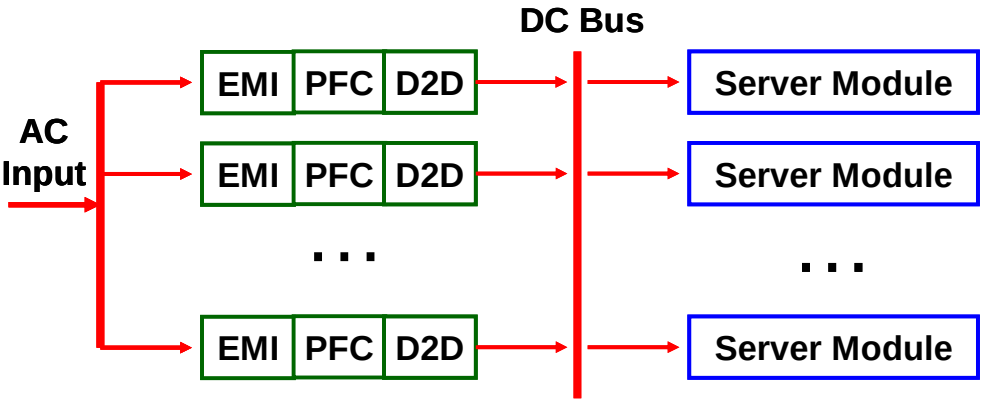


Figure 1.14. Power architecture of today's DPS for server applications.

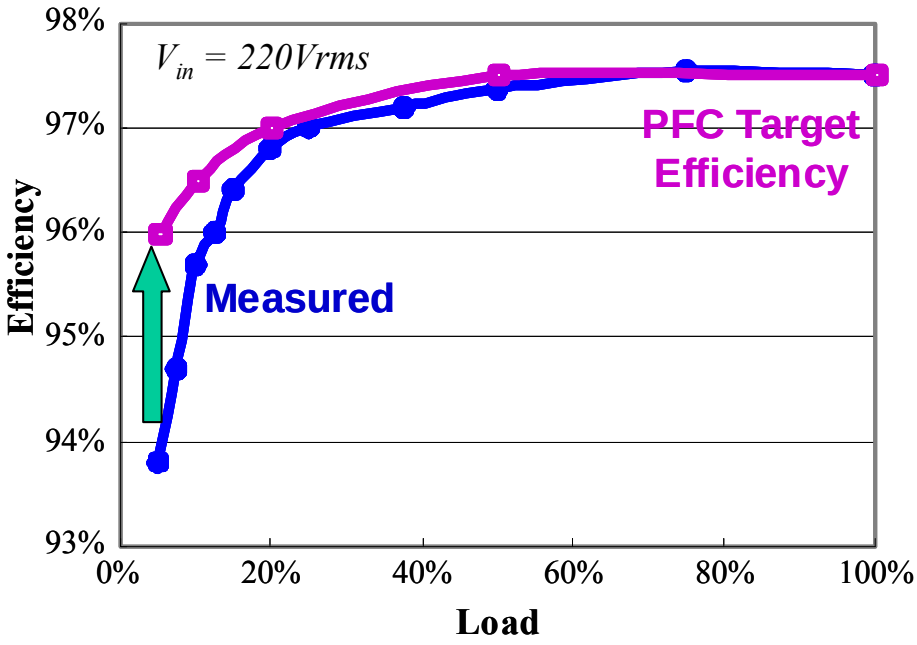


Figure 1.15. Measured PFC high line efficiency with CoolMOS and SiC diode.

Using today's most advanced semiconductor devices, the existing power architecture shown in Figure 1.14, which is widely used in today's server systems, still has its

limitations facing today's extremly challenging requirements for simultaneous maximization of both the entire-load-range efficiency and high power density. Designed with the new generation CoolMOS (IPW60R099CS) and the SiC diode (SDP06S60), switching at 130 kHz, the measured PFC efficiency is shown in Figure 1.15. Further improvement at light load is still needed to meet today's efficiency challenges.

b. High power density

With the evolving information technologies, the computational density increases significantly. For example, the data center power density is increasing by approximately 15% annually. As shown in Figure 1.16 the rack power increases every year. It is predicted that the power could go as high as 25 kW in 2009 [30]25]. The servers per rack increase dramatically. In 1996, there was an average of seven servers per rack. This number increased to ten servers per rack in 2002 and 14 in 2005. It is projected to increase to 20 servers per rack by 2010.

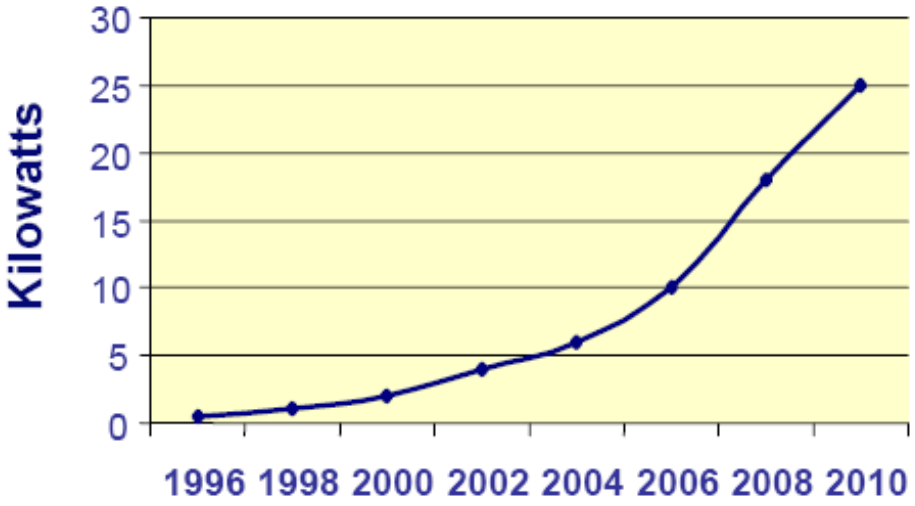


Figure 1.16. Rack drawing more power [14].

With these rapid growth of the Internet technologies, AC-DC front-end power supplies see a dramatic change in power density since the data-processing, networking, and storage equipment creates a strong demand for power supplies with much higher power densities. Figure 1.17 [31], the power density roadmap, shows the power density of the

front-end converter has increased dramatically in the past years. A typical power density of server front-end power supplies was in the 5 W/in^3 range about ten years ago [32]. The power density of these power supplies today is in the 25 W/in^3 range. As this trend continuous, the power densities is expected to be pushed up even over 30 W/inch^3 in the near future in order to meet industrial needs.

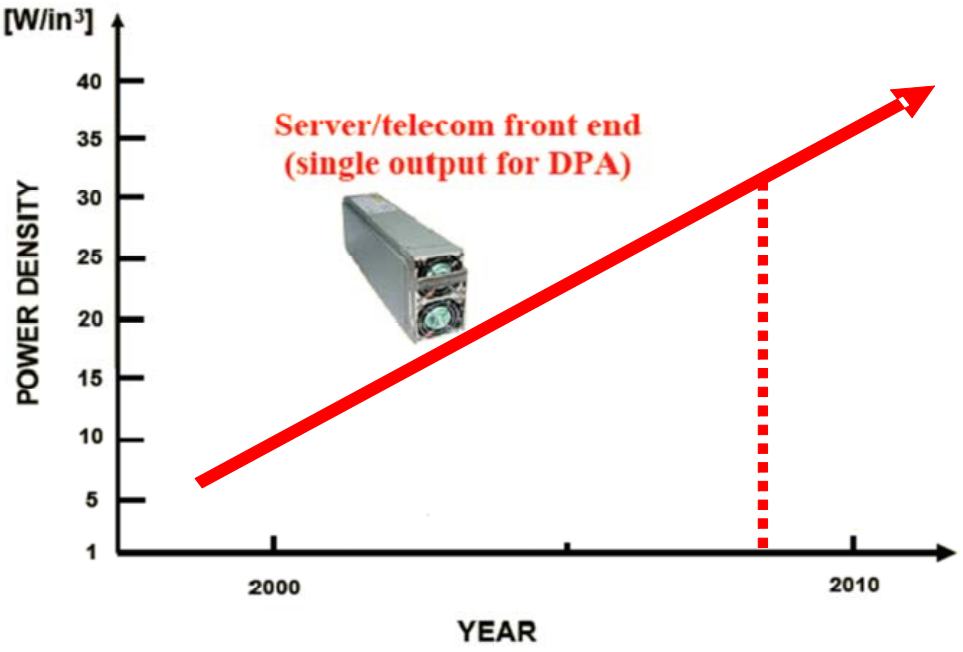


Figure 1.17. Power density roadmap for server power supplies [31].

Figure 1.18 shows a today's the state-of-the-art power supply. The EMI filter, PFC inductor, the hold up bulk cap and the magnetic components of DC-DC converter occupy significant amount of the space. In order to achieve higher power density, studies and researches regarding the size reduction of these components are highly demanded. As for the DC-DC converter stage, it has been demonstrated that a 1 MHz LLC converter can effectively reduce the size of the magnetic components and the bulk cap [33]. For the power factor correction (PFC) stage, the inductor size can be reduced with increasing switching frequency, as show in Figure 1.19. It is a design trade-off between size and switching loss.

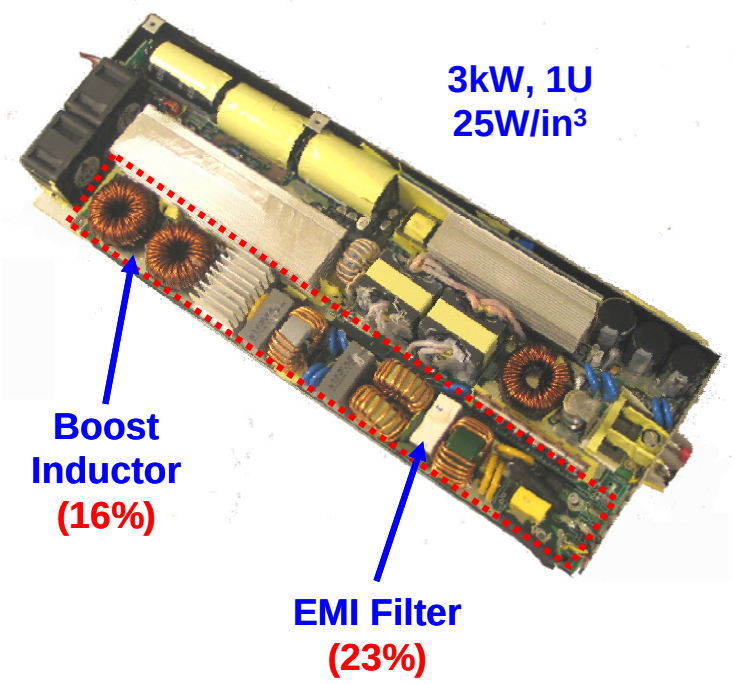


Figure 1.18. The state-of-the-art front-end converter.

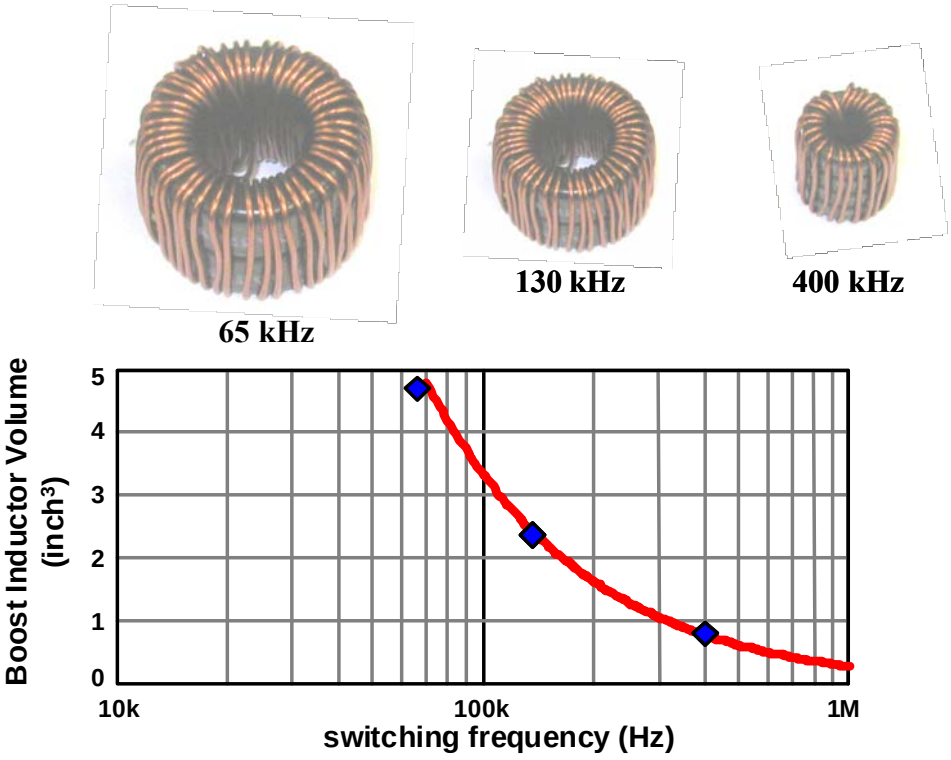


Figure 1.19. Inductor size reduction with increasing switching frequency.

The EMI filter, however, is difficult to reduce and can take up to 23% of the total front-end converter size in today's the-state-of-the-art power supply design. Existing studies show that the EMI filter may not be reduced by increasing the switching frequency, as shown in Figure 1.20. Choosing the PFC switching frequency to be 65 kHz, 130 kHz, and 400 kHz, the EMI filter sizes are essentially the same. In another word, increasing swiching frequency is not an effective way to reduce the EMI filter size. The EMI filter actually runs into a big penalty in terms of size when the switching frequency is higher than 150 kHz, unless it can be operated higher than 400 kHz [33][34][35]. Unfortunately, the efficiency suffers at such extreme switching frequencies even relying on the advanced circuit topologies [36][37][38].

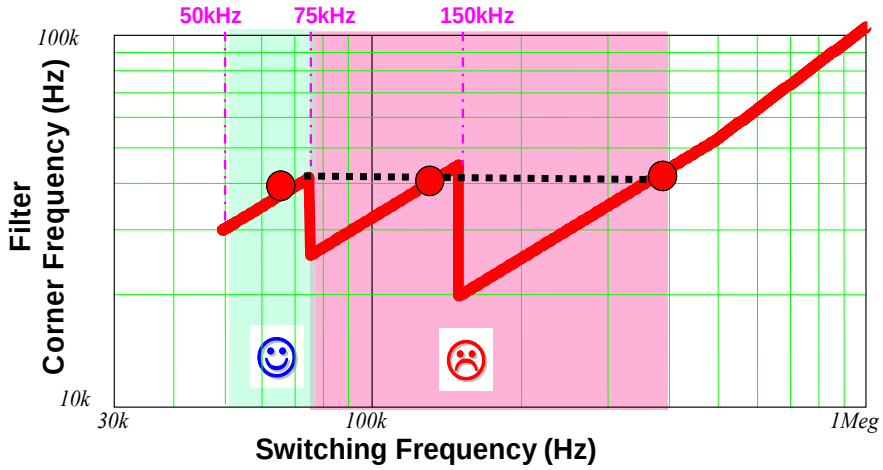


Figure 1.20. Relationship between the filter corner frequency and the switching frequency.

c. Power scalability

Due to the rapid evolving technologies, the PFC designs for the server products have relatively short lifespan. For example, the IBM server power roadmap shows that PFCs need to be redesigned every one or two years, as shown in Figure 1.21 [39]. The HP server products roadmap shows the similar situation, in Figure 1.22. The HP servers have several different series. For each series, due to the performance upgrade, the PFC needs to be redesigned every one or two years. It is very time consuming and not cost-effective. To solve this prolem, in the future, HP proposed to have essentially one design used for all applications.

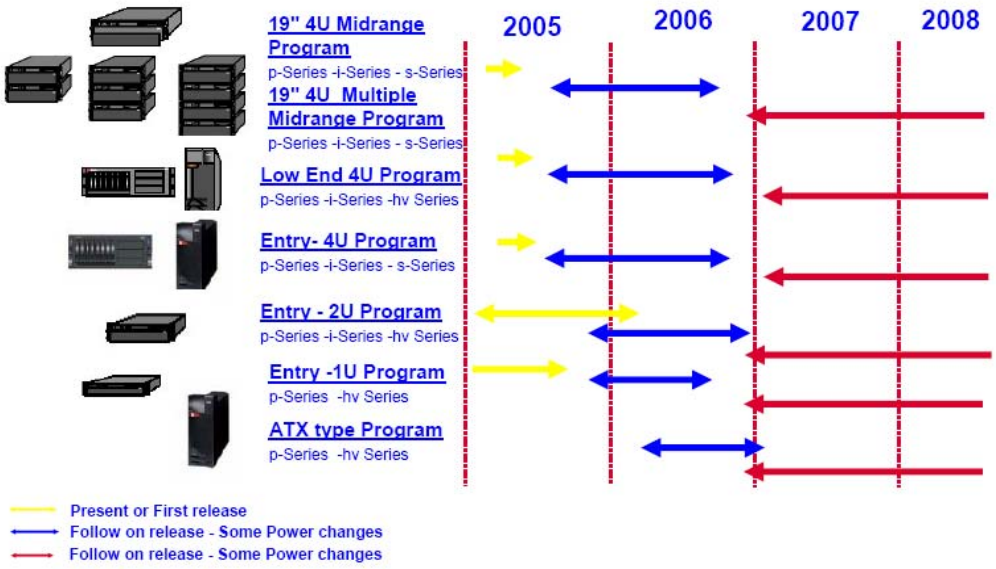


Figure 1.21. IBM Server Power Roadmap (p & i series) [10].

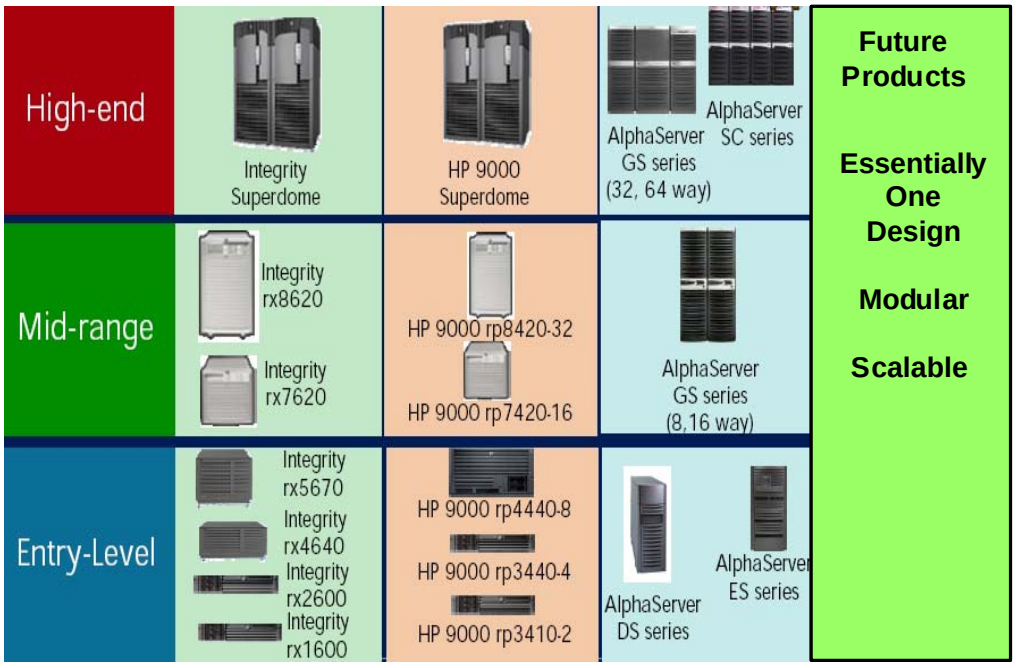


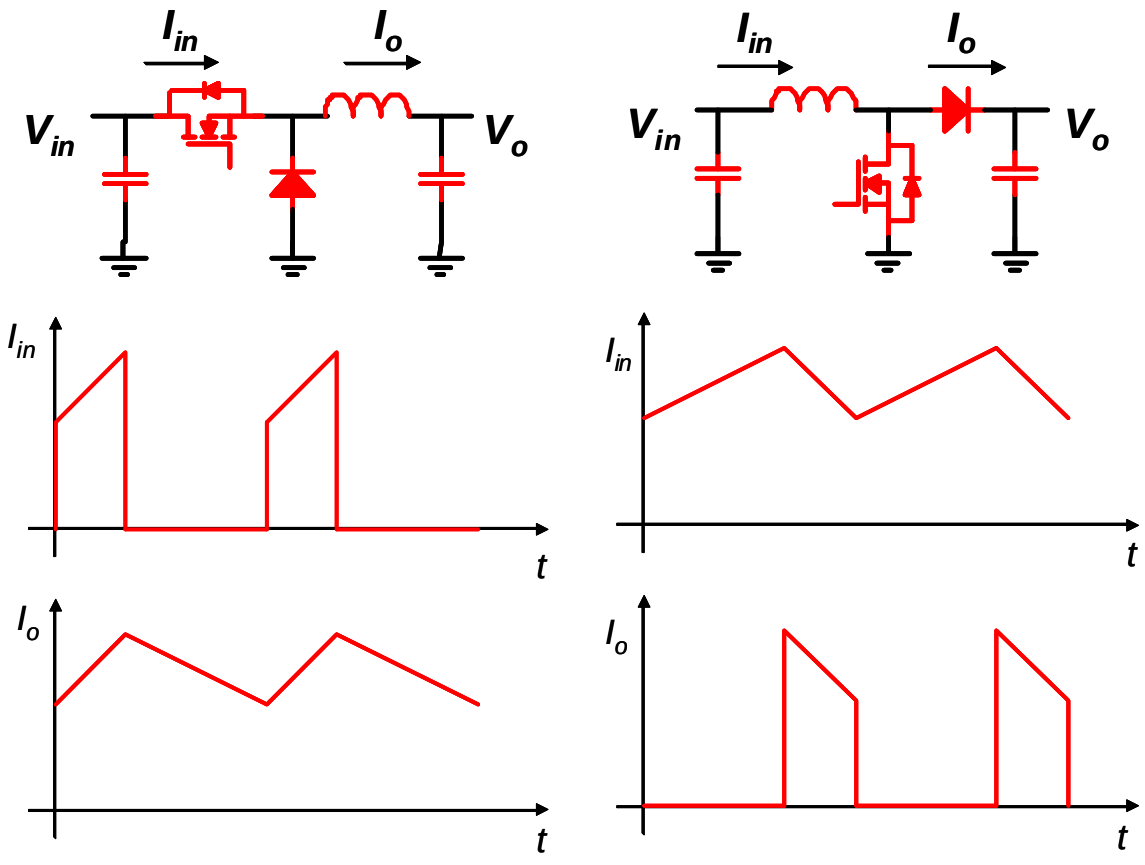
Figure 1.22. HP Server Products.

Different number of PFC modules should be used corresponding to different power needs. With the standadized PFC modules, the cost can be reduced and performance can be

optimumized. This method essentially requires the PFC to be modular and scablable. It make the system extendable, easy reconfiguration and much more cost-effective.

1.3.2 Similarity between multi-phase buck and boost converters

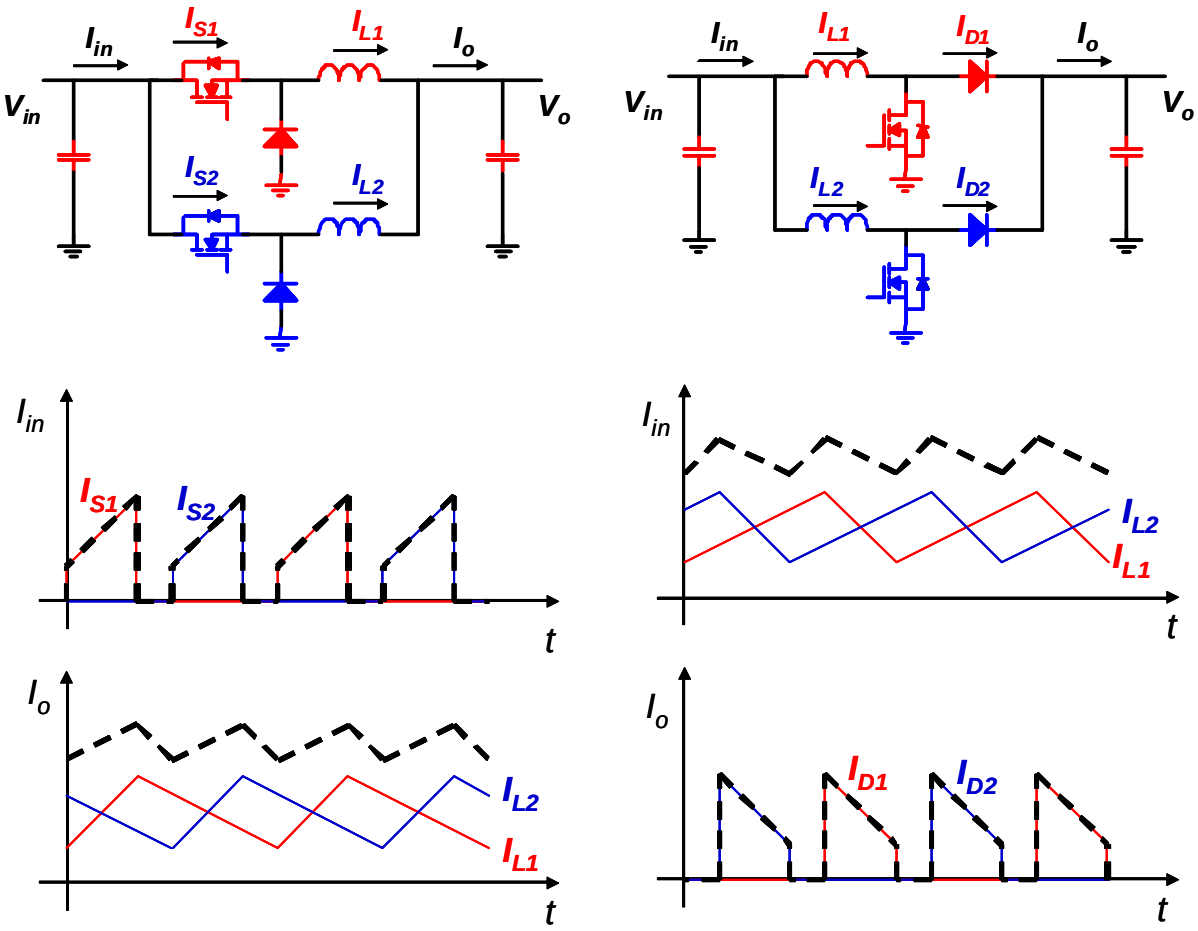
Buck converter and boost converter are actually the same circuit topology with different direction of power flow. This conclusion is most obvious when the bi-directional buck / boost DC-DC converter is considered. Therefore, the input of the buck converter is the same as the output of the boost converter, as shown in Figure 1.23. Both the input of the buck and the output of the boost are pulsating current. On the other hand, the output of the buck is the same as the input of the boost converter. As shown in Figure 1.23, both the output of the buck and the inut of the boost converter are continuous current.



(a) Buck converter **(b) Boost converter**

Figure 1.23. Input and output current waveform comparison of Buck and Boost converters.

Since the buck and the boost are the same circuit topology basically, the interleaving impact on both converters is also very similar, as shown in Figure 1.23. It is quite obvious that the input and output current ripple cancellation phenomenon of the multi-phase buck converter also exist in the output and input of the multi-channel boost converter correspondingly.



(a) 2-phase buck converter **(b) 2-phase boost converter**

Figure 1.24. Input and output current waveform comparison of 2-phase Buck and Boost converters.

Because of the similarity between the multi-phase buck and the boost converter application, the knowledeg obtained via the previous studies and research should be able to be extended to multi-channel interleaved boost for the PFC application. All the features existed in the multi-channel interleaved buck converter should also exist in the multi-channel interleaved boost converter, such as ripple cancellation, evenly distributed thermal

stress, modularity and scalability, etc. The benefits obtained in the buck converter by multi-channel interleaving should also be able to be realized in the multi-channel interleaving boost converter, in one form or another depending on the applications. The techniques, such as phase shedding, applied in the multi-channel interleaved buck converter should also apply. With the multi-channel interleaved PFC included, the distributed power system further evolves into the architecture in Figure 1.25.

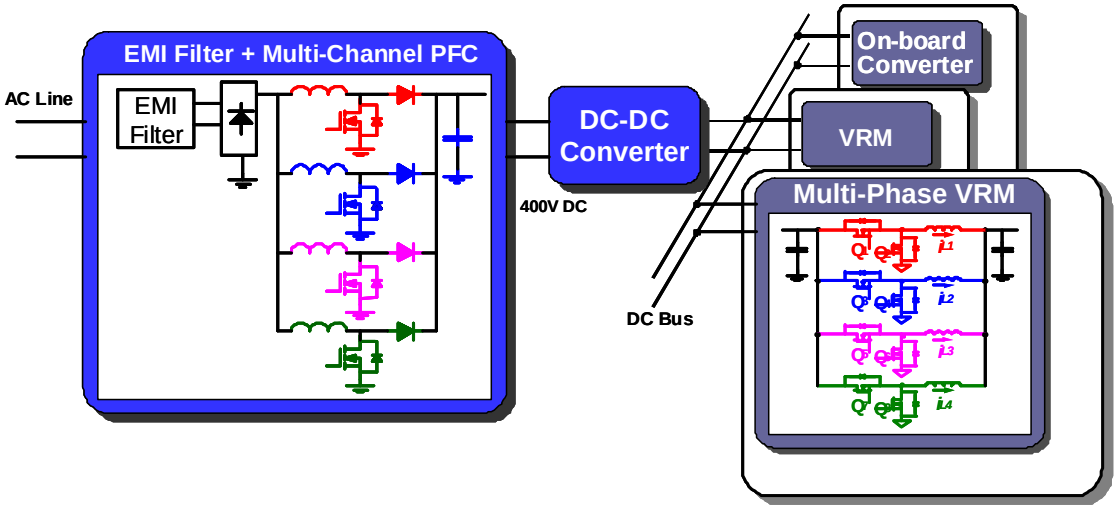


Figure 1.25. Distributed power system architecture with multi-phase VR and multi-channel PFC.

A side by side comparison between the multiphase VR and the multi-channel interleaved PFC is shown in Table 1-1. More detailed investigation and exploration will be discussed in the following chapters of this dissertation.

Table 1-1. Interleaving comparison between the multiphase VR and the multi-channel PFC

Multi-channel buck converter for VR	Multi-channel boost converter for PFC
• Improve the power density o Smaller inductance – better transient performance o Smaller output filter - smaller output current ripple o Smaller input filter – smaller input current ripple	• Improve the power density o Same inductance – keep the same efficiency o Smaller EMI filter - smaller input current ripple o Smaller bulk capacitor – smaller output current ripple

• Thermal dissipation more evenly distributed • Overall cost reduced – less capacitors, standardized cells • Scalability – keep step with future CPU power management design • Better light load efficiency – phase shedding technique	• Thermal dissipation more evenly distributed • Overall cost reduced – possible (smaller EMI filter, standardized cells) • Scalability – keep step with future sever power requirement • Better light load efficiency – phase shedding technique

Same as the multiphase VR, interleaving only reduces the total input and output current ripple of the multi-channel interleaved PFC; the inductor current in each channel still is the same. Coupled inductor concept also can be introduced to the multi-channel interleaved boost converter. A side by side comparison between the multiphase VR and the multi-channel interleaved PFC is shown in Table 1-2. A more detail investigation will be discussed in the following chapters.

Table 1-2. Coupled inductor comparison between the multiphase VR and the multi-channel PFC.

Multi-channel buck converter for VR	Multi-channel boost converter for PFC
• Less component counts • Smaller channel inductor current ripple • Improve the steady-state efficiency	• Less component counts • Same channel inductor current ripple • Reduce the inductor size

1.4 Dissertation Outlines

The dissertation consists of six chapters and is organized as follows. First, the interleaving technique is introduced and reviewed. Among the existing studies, the multi-channel interleaved buck converter for the VR application has been intensively studied and thoroughly explored. Generally speaking, multi-channel interleaving architecture can be applied to different topologies. Other than buck converter, boost converter is another simplist and widely used topology. One basic approach of this study is trying to extend the existing knowledge and principle obtained from multiphase buck converters to the multi-

channel interleaved boost converters since there is similarities existed between the multi-phase buck and the multi-channel boost converters. One typical application of the boost converter is the PFC circuit in the AC-DC front-end converter. The background of the AC-DC front-end converters and the challenges of today's AC-DC front-end converters are firstly introduced. To meet the challenges, the multi-channel interleaved PFC is proposed to improve the power density and the light load efficiency. The knowledge obtained from multiphase VR is utilized and the impact of multi-channel interleaving is thoroughly explored for the PFC application. The study shows multi-channel interleaved PFC can benefit the power density and the light load efficiency of the AC-DC front-end converter, and the featherbility of extending the existing knowledge on multiphase VR approach is verified.

The detail outline is elaborated as follows:

Chapter 1 introduces the background of interleaving technique. One of the most successful applications, the multiphase VR, is reviewed and the features are summarized. The knowledge obtained from multiphase VR will be extended to multi-channel interleaved boost converter. For the AC-DC front-end converters, the challenges of achieving high entire-load-range efficiency and high power density are firstly discussed. According to the state-of-the-art power supply, even with today's most advanced semiconductor devices, today's single-channel PFC still has its limitations to meet the challenging requirements due to the poor light load efficiency and the large EMI filter size. The multi-channel interleaved PFC, on the other hand, shows good potential to improve the power density and increase the light load efficiency.

Chapter 2 investigates the multi-channel interleaving impact on the PFC design. The double Fourier integral transformation is used to characterize the noise source spectrum. Based on the harmonic cancellation effect, the multi-channel interleaving impact on both the DM and CM filter design are summarized, and the design guidelines are provided. The multi-channel interleaving impact on the output capacitor current ripple is also studied and summarized in this chapter. It should be pointed out that interleaving only reduces the total input and output current ripple; the inductor current in each channel still has large ripple if small inductance are used. Coupling inductors have different equivalent inductances for input current ripple and inductor current ripple. Inverse coupling inductors between the

interleaved channels reduce the inductor current ripples while maintaining the same input current ripple. The magnetic component weight reduction of coupled inductor was also investigated in this chapter.

Chapter 3 compares the output requirement of the VR application and input requirement of the PFC application. It can be found that the VR input requirement is defined in the time domain while the PFC output requirement is defined in the frequency domain. Since the requirement is different, although the interleaving impact on the circuits are exactly the same, the interleaving design consideration also could be different. In this chapter, different interleaving strategy for multi-channel PFC is investigated considering the EMI requirement for this AC-DC application. A novel phase angle control method is proposed to maximize the reduction of the EMI filter. For 2-channel interleaved PFC, just by changing the interleaving scheme to 90 degree phase shift, 39% total volume reduction of the EMI filter can be achieved. The phase angle control impact on the output capacitor current ripple is also studied. To realize and demonstrate the previously discussed features of the multi-channel phase angle controlled PFC, as an example, a digital controlled 4-channel PFC prototype is designed and developed. The PFC control algorithm, control program flow chart, current sensing implementation, and the digital implementation of phase angle control are discussed. The 4-channel PFC and the digital control with phase angle control scheme is design and experimentally verified by the developed prototype.

In Chapter 4, phase shedding technique is proposed to improve the PFC light load efficiency. Generally, phase-shedding can be used for any power converters with multi-channel configuration. However, reducing the number of active channels can improve the light load efficiency, but it reduces the ripple cancellation effect as well, which will result in the EMI noise increase and losing the benefit on the EMI filter. Then, following the same concept discussed in Chapter 3, phase shedding with phase angle control scheme is proposed. To further improve the PFC light load efficiency, the constant on-time controlled PFC control scheme is proposed. Although constant on-time controlled PFC can improve the efficiency at light load as expected, the EMI filter size may need to increase to meet the standard due to the wide switching frequency range. To resolve the issues, adaptive frequency controlled PFC is further proposed to improve the EMI performance at light load. By using the proposed method, the light load efficiency can be improved with

much less penalty on the EMI filter. The proposed light load efficiency improvement strategies are combined and implemented on the platform of the digital controlled 4-channel PFC. The benefit of improving the light load efficiency is experimentally verified. The EMI performance is also evaluated with the EMI measurement results obtained from the PFC prototype.

Chapter 5, another simple and straightforward extension, the multi-channel interleaved boost converter for the battery charging / discharging of the hybrid vehicle application is discussed. Adopting the proposed 3-channel interleaved DCM boost converter, the improvement over the benchmark converter design, the single-channel boost converter, is demonstrated. The switching related power loss is significantly reduced by DCM operation. The inductor size of the boost inductor is also greatly reduced because of the DCM operation. Following the same principle explored in the previous chapters, the benefits of interleaved boost PFC can be further extended other applications, such as the boost converter in the PV system.

Chapter 6 is the summary of this dissertation.

Chapter 2. Interleaved PFC for AC-DC Front-End Converter Applications

2.1 Introduction

Most of the information technology devices used in the telecom and computer systems are designed to operate using DC power while most power available for such systems are AC power. Therefore, the Distributed Power Systems (DPS) are usually needed for these systems, as shown in Figure 1.2. In the distribued power systems, from the AC line to the DC bus is the AC-DC front-end converter. With the fast growing information technology, telecom and computer systems is now a large market for the AC-DC front-end converters, sometimes also referred as power supplies. Recent studies show that the demands for these systems are continuously increasing [40].

In the AC-DC front-end converters, two-stage approach is widely used for high power applications. Because of its continuous input current and simplicity, Continuous Conduction Mode (CCM) boost topology, as shown in Figure 1.12, is the most popular topology for the power factor correction (PFC) stage.

Today, high efficiency is becoming the first priority in the PFC design, driven strongly by economic and environmental concerns emphisised by various organizations and programs, such as the U.S. Energy Star [26], Climate Savers [27], and German Blue Angel [28]. It indicates the efficiency requirement keeps increasing and is extending to lighter load conditions. Higher power density is also greatly desired in the PFC design since it can eventually reduce the converter cost and allows for accommodating more equipment in the existing infrastructures. From the power density roadmap shown in the Figure 1.17 [31], one can see that the power density of the front-end converter is expected to be pushed up even over 30 W/inch^3 in the near future in order to meet industrial needs. For the high density PFC design, the key is to reduce the EMI filter and the boost inductor size without comprimizing the efficiency. Due to the rapid evolving IC technologies, the AC-DC front-end converters as products in the market have relatively short lifespan. Power scalabiltiy characteristics are important features to cost effective solutions. This

continuously increasing power density and efficiency target, and the power scalability requirement pose challenges for today's AC-DC front-end converter technology. The single-channel PFC shows its limitations on improving the efficiency, power density, and power scalability.

An alternative approach for futher improving the PFC performance is the multi-channel interleaving technique. By staggering the channels at uniform intervals, multi-channel interleaved PFC can reduce the EMI filter size due to the ripple cancellation effect [41]. Based on the existing modular approach, one EMI filter can actually be put in front of all the PFC modules, as shown in Figure 2.1, and by interleaving these PFC modules the EMI filter size can be reduced due to the ripple cancellation effect. The reduced input ripple current means lower differential-mode (DM) EMI noise magnitude. Not only the noise magnitude is lower, by interleaving *m* channels, the ripple current frequency will be increased by *m* times, which in some case will make EMI filter size smaller, and eventually will help to increase the power density, which is greatly desired in today's front-end converter design. Not only it has the opportunity to benefit the input EMI filter, interleaving can also reduce the output capacitor current ripple due to the ripple cancellation effect. Smaller current ripple can increase the electrolytic capacitor life time, which could be a design concern in the AC-DC power supply design.

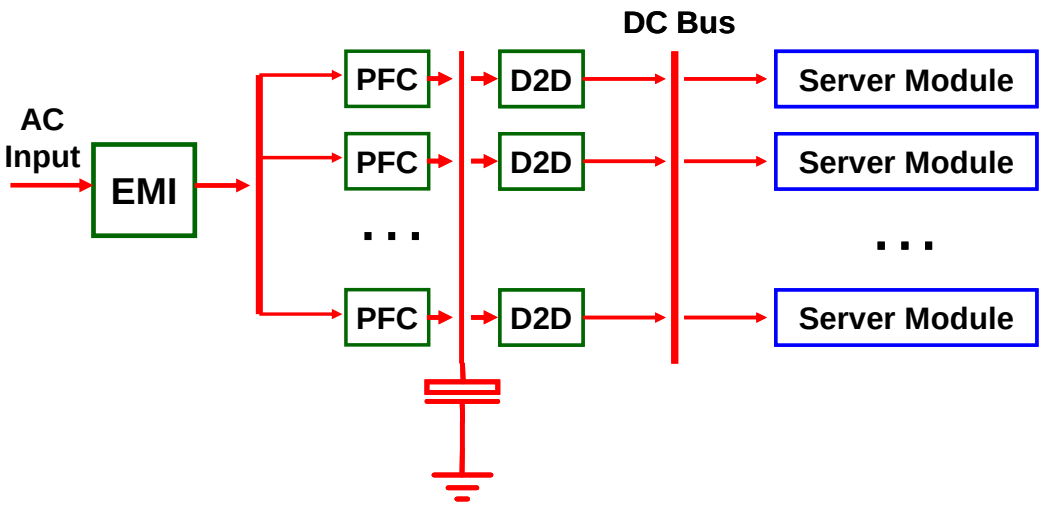


Figure 2.1. Front-end converter with interleaved multi-channel PFC.

2.2 Benchmark PFC – State-of-the-Art Single-Channel PFC

Because of its continuous input current and simplicity, single switch CCM boost PFC is the most popular topology for the high power applications. Nevertheless with the wide universal input voltage range, this PFC circuit can not maintain a high efficiency at low line due to the high conduction loss and switching loss.

Figure 2.2 shows the loss breakdown of a 1 kW CCM boost PFC design with 90 Vrms input. The boost PFC is designed at 100 kHz switching frequency. Two MOSFETs, IRFP460A, are used in parallel as the boost switch. Ultra-fast recovery diode RHRP860 from Intersil is used as the boost diode. 314 uH boost inductor designed with Koolmμ toroidal core is used. According to the loss breakdown, the MOSFETs conduction is one of the dominating factor for poor efficiency. With the evolving device technology, new generation CoolMOS IPW60R099CS with small R_{dson}, more than 60% conduction loss reduction can be achieved comparing with using IRFP460A. This improvement is purely accomplished by the power semiconductor device technology. The high MOSFET turn-on loss is another well known issue for the PFC design. Reducing the operating frequency is one way to reduce the switching loss, but it is not a good solution in terms of power density. The high MOSFET turn-on loss is caused by the boost diode reverse recovery problem. Lots of research effort has been putting on solving the boost diode reverse recovery loss problem. The state-of-the-art solution is to control the current decreasing rate *di/dt* of the diode during its turn-off. To accomplish this function, either a simple auxiliary circuit with an active switch or a complex network consisting only of passive components is needed.

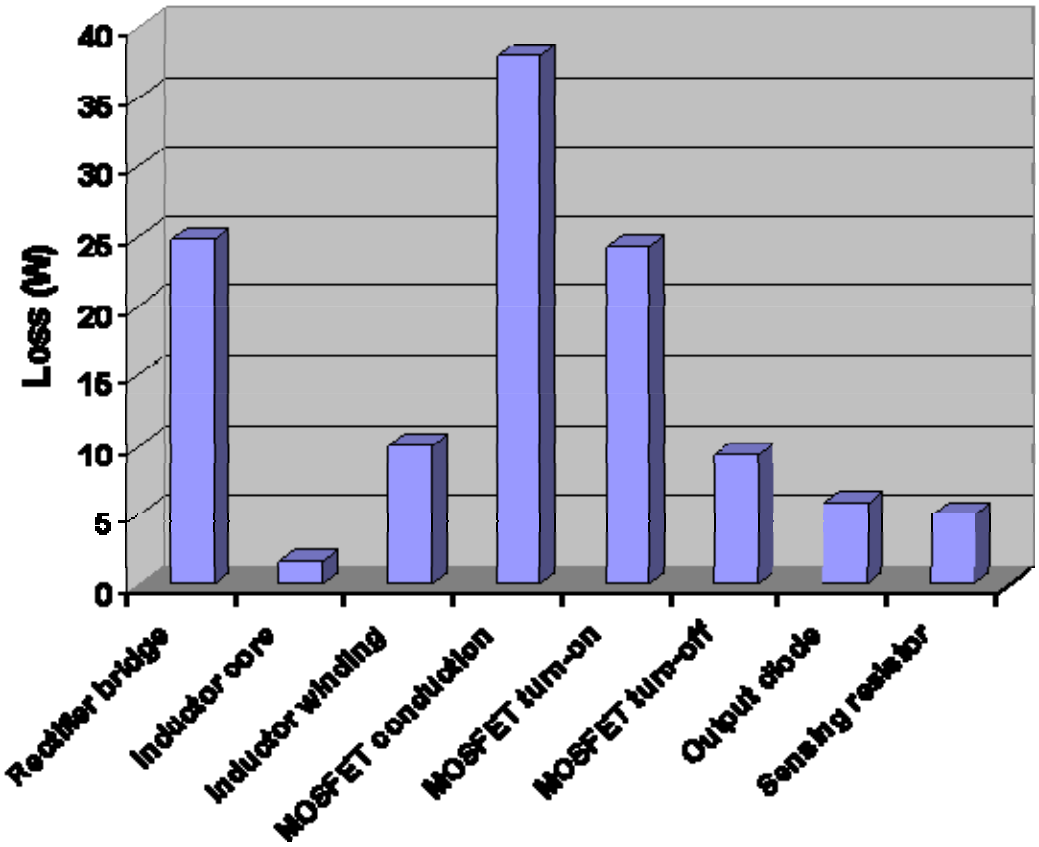


Figure 2.2. 1 kW CCM boost PFC loss breakdown at 90 Vrms.

A state-of-the-art solution for the diode reverse recovery is shown in Figure 2.3. It is simple yet effective for alleviating the diode reverse-recovery problem [43]. The diodes, D_{a1}, and D_{a2}, can be implemented with one TO-220 device with serial connection package, FEP16JTD. The other two diodes , D_o,*and* D_a, can be implemented with another TO-220 device with common cathod package, ISL9K860P3. Eventually, only one TO-220 device is added comparing with the conventional boost PFC topology.

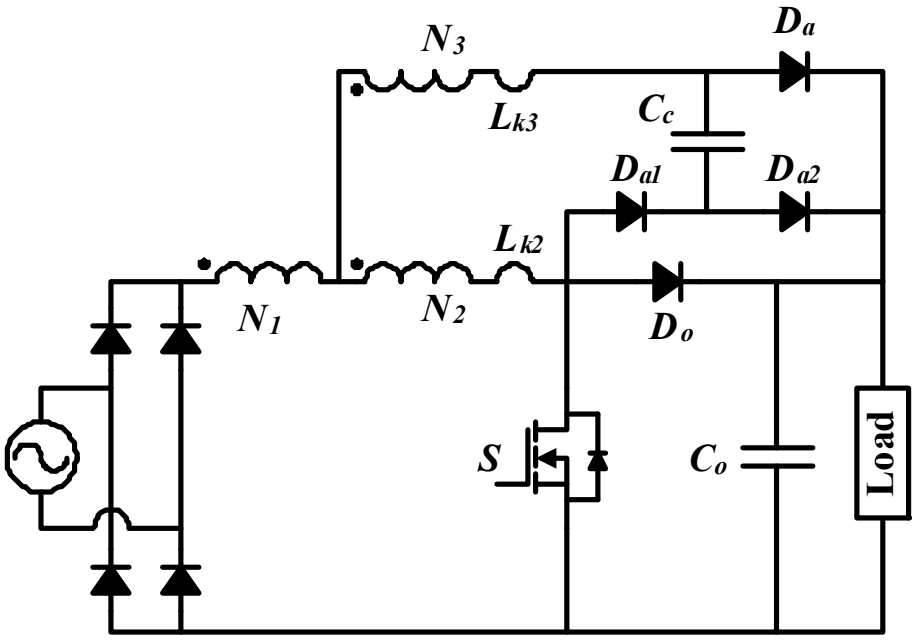


Figure 2.3. State-of-the-art CCM boost PFC with diode reverse recovery solution.

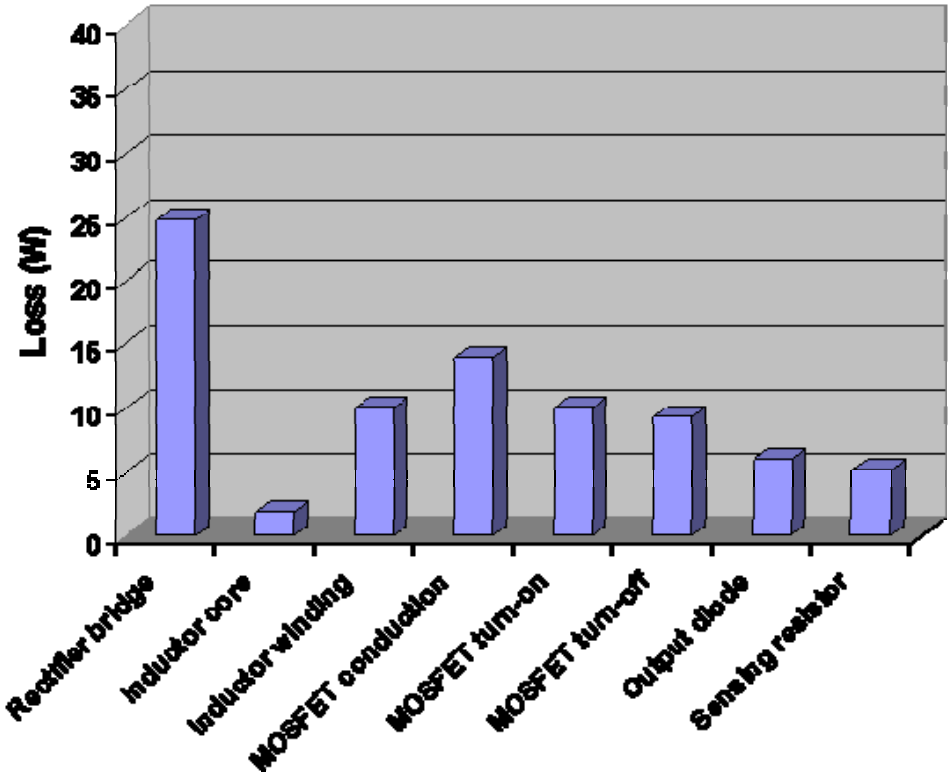


Figure 2.4. Loss breakdown for 1 kW state-of-the-art CCM boost PFC at 90 Vrms.

Two Infineon CoolMOS 60R099 with TO-247 package are used in parallel. With the state-of-the-art CCM boost PFC design the MOSFEET conduction loss and the turn-on loss is significantly reduced. Figure 2.4 shows the loss breakdown of the PFC design. More than 60% MOSFET conduction loss reduction can be achieved due to the smaller R_{dson}. About 70% turn-on loss is reduced due to the reverse recovery alliviation.

The switching frequency is designed at 130 kHz in order to have a better trade-off between efficiency and power density, which will be discussed later.

The measured PFC efficiency is shown in Figure 2.5. With the state-of-the-art diode reverse recovery solution and the new generation CoolMOS device the efficiency can be significantly improved comparing with the conventional PFC design without diode reverse recovery alliviation and the IRFP460A MOSFET.

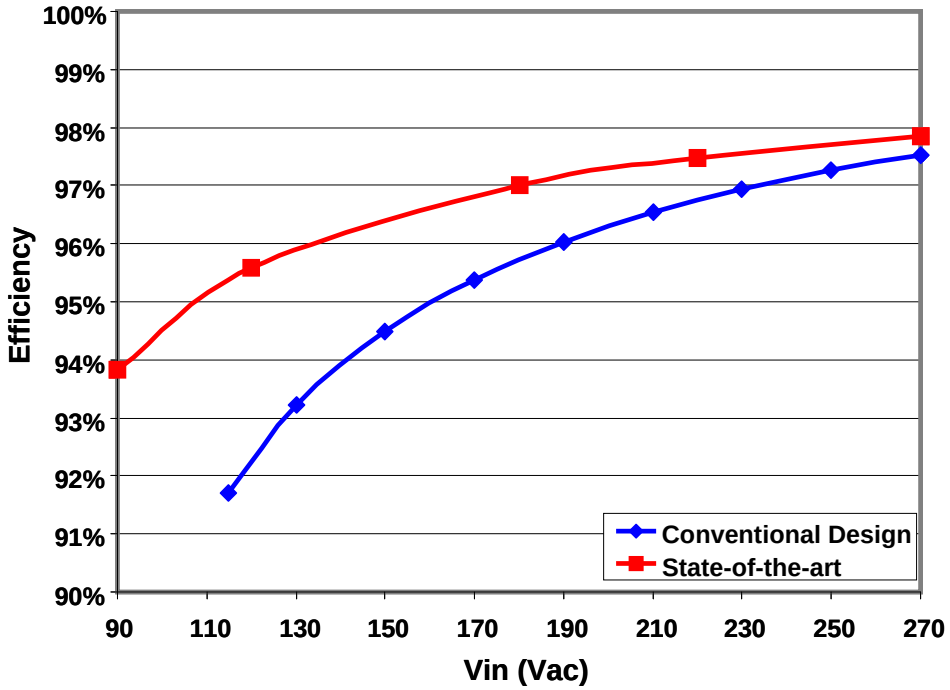


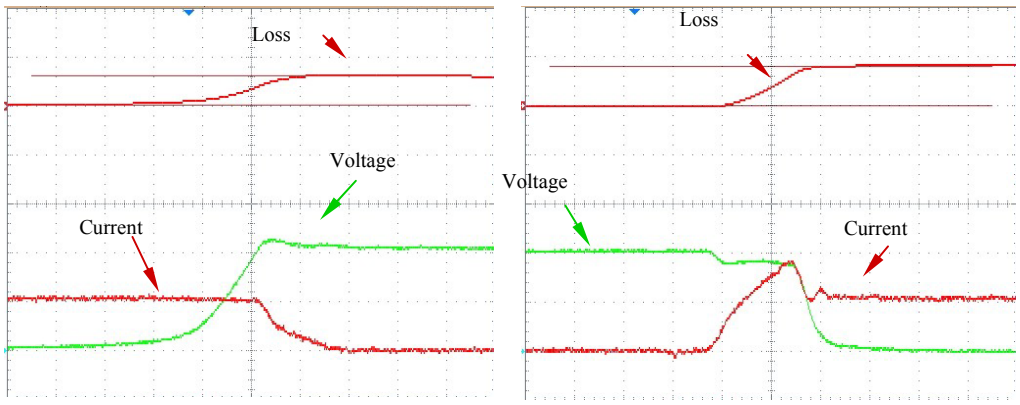
Figure 2.5. Measured PFC efficiencies.

The reverse recovery problem of the high voltage rating diode can be solved not only by the improved circuit toplogies but also new power semiconductor technologies, the SiC Schottky diode. The most significant feature of SiC diode is almost no reverse-recovery charge. Therefore, the turn-on loss of the MOSFET is expected to be substantially reduced.

Since SiC is a wide band gap semiconductor material, SiC Schottky diode can have a very low on-resistance with high rated voltage. Theoretically, the SiC Schottky diode can have a voltage rating more than 1000 V. At present, the 600 V voltage rating SiC Schottky is a commercially acceptable for some high-end applications. The voltage rating much higher than the Si Schottky diode.

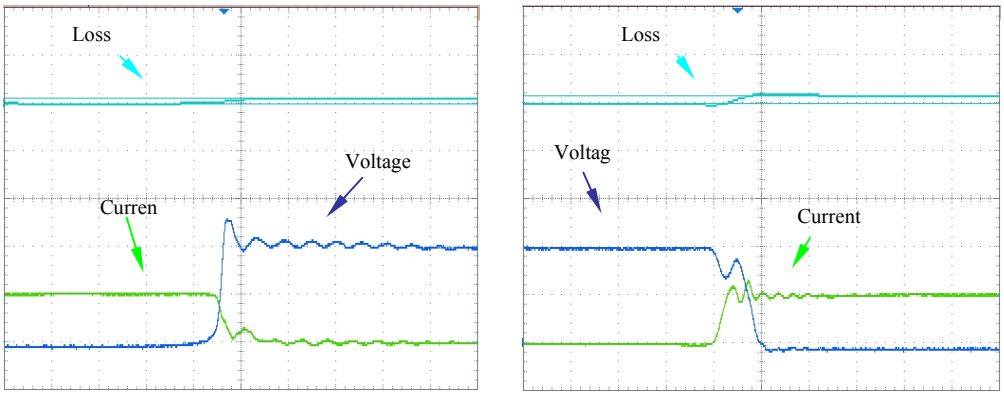
Significant switching loss can be saved if the CoolMOS is used together with SiC diode (SDP06S60) comparing with IRFP460A and RHRP860. The new generation CoolMOS from Infineon offers not only very low on-state resistance but very fast switching speed as well. To evaluate the device switching performance, a switching loss test-bed is used to obtain the switching waveforms [34]. In the test circuit PCB layout, the parasitic inductance of the commuting loop are minimized, composed of the MOSFET, the diode and the bus capacitor. The switching waveforms of different devices combinations can be measured on this test circuit. The switching loss can be calculated and compared based on the switching waveforms. The switching losses of two sets of device combinations are compared: the MOSFET IRFP460A and the fast recovery diode RHRP860, the Infineon new generation CoolMOS IPW60R099CS and SiC Schottky SDP06S60.

For the device combination of IRFP460A and RHRP860, the measured switching waveforms are shown in Figure 2.6 (a) and (b), 9.1 Ω gate resistor is used in the test. The waveform shows about 16 A diode reverse recovery current, so the turn-on loss is much larger than the CoolMOS and SiC diode combination. For the device combination of IPW60R099CS and SDP06S60, the measured switching waveforms are in Figure 2.6 (c) and (d). Because the SiC Schottky diode eliminates the diode reverse recovery current, faster switching speed can be applied. 4.3 Ω gate resistor is used in the test without causing excessive voltage stress. According to the waveform, the CoolMOS and SiC diode combination has much shorter turn-on and turn-off time. Therefore, the switching losses are greatly reduced.



(a) Turn off **(b) Turn on**

IRFP460A + RHRP860



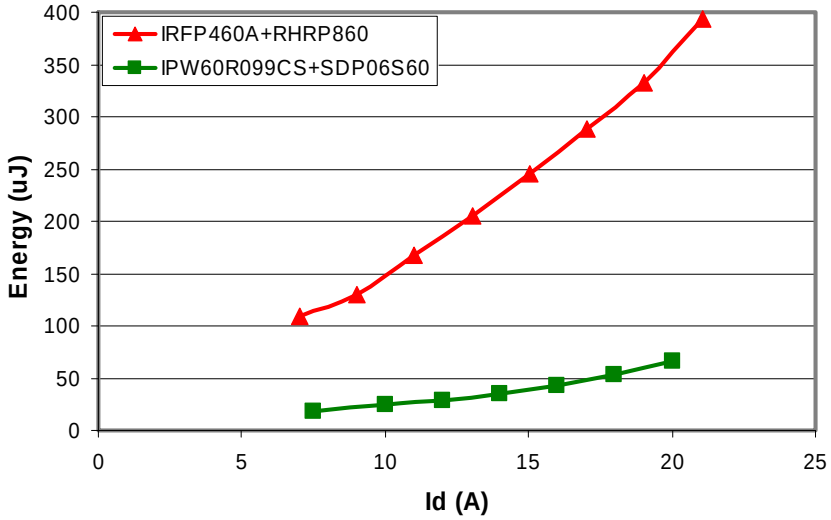
(c) Turn off **(d) Turn on**

IPW60R099CS + SDP06S60

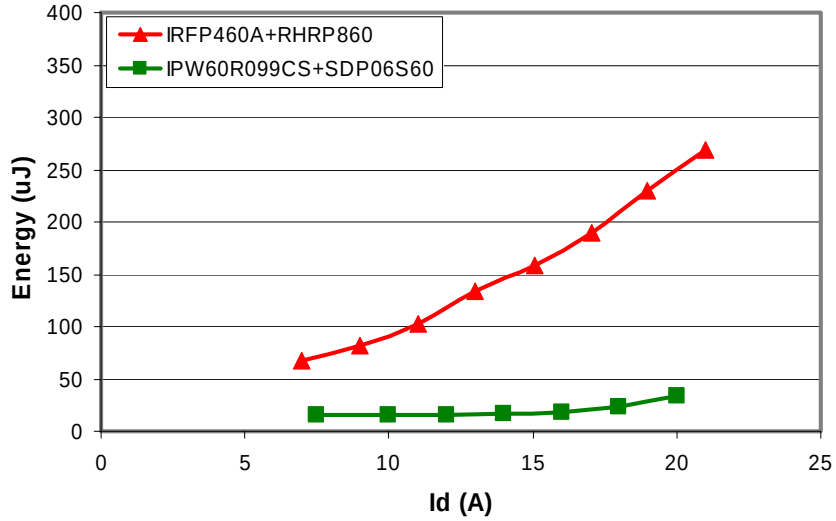
Voltage: 200V/div; current: 20 A/div; loss: 400μJ/div; time: 20nS/div.

Figure 2.6. Measured switching waveforms.

Keeping the bus voltage at 400 V, the switching losses are measured at different drain current I_d for each device combination. The turn-on loss data at different MOSFET drain current is summarized in Figure 2.7 (a) and the turn-off loss data is summarized in Figure 2.7 (b). According to these data, the CoolMOS IPW60R099CS and SiC diode SDP06S60 are expected to lead to considerable improvement on the switching performance. Comparing with the conventional devices, about 80% switching loss reduction can be achieved by this new generation CoolMOS and the SiC diode for both the turn-on and turn-off.



(a) Measured turn-on loss



(b) Measured turn-off loss

Figure 2.7. Measured switching loss data.

The measured efficiency curve of the boost PFC with CoolMOS and SiC diode is shown in Figure 2.8. Since the SiC diode can fully eliminate the reverse recovery loss, the efficiency is further improved compared with the other two designs. The efficiency can be as high as 96% at low line (Vin = 110 Vrms) and 97.5% at high line (Vin = 220 Vrms).

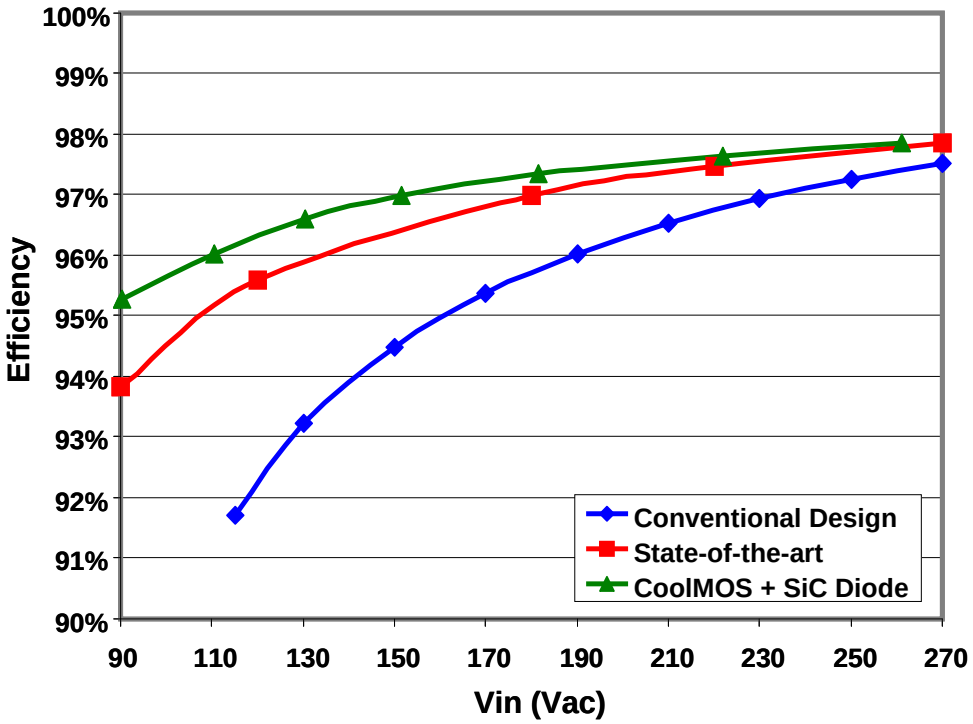


Figure 2.8. Measured PFC efficiencies.

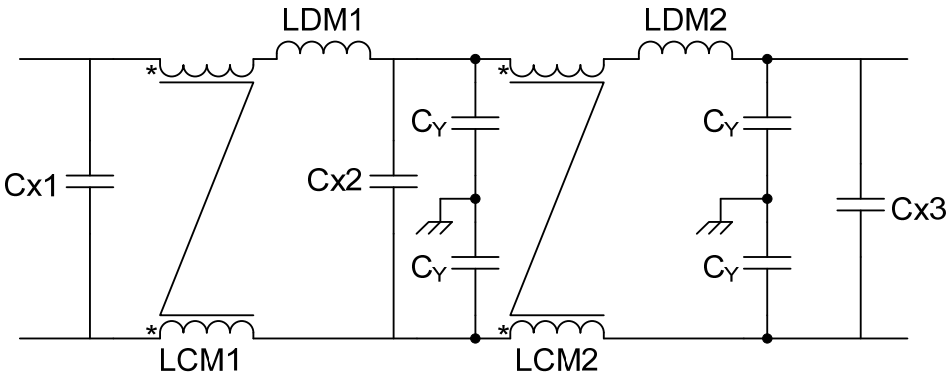


Figure 2.9. Two-stage EMI filter.

To meet the EMI standard requirement, passive EMI filters are widely used. Normally two-stage EMI filters are used because they can achieve higher attenuation comparing with single stage EMI filter. A typical two-stage EMI filter is demonstrated in Figure 2.9. In the later part of this dissertation, the filter corner frequency is plotted based on two-stage EMI filter.

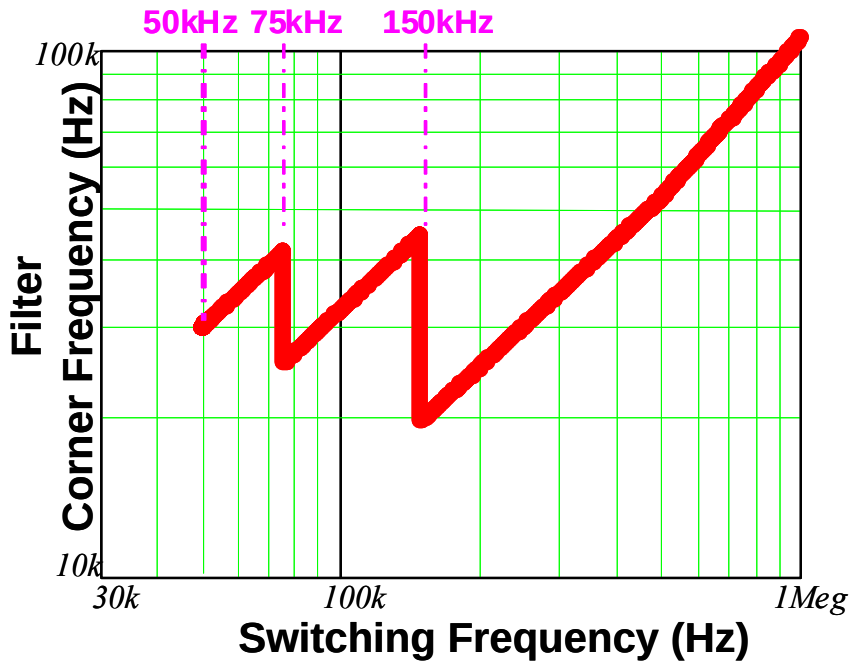
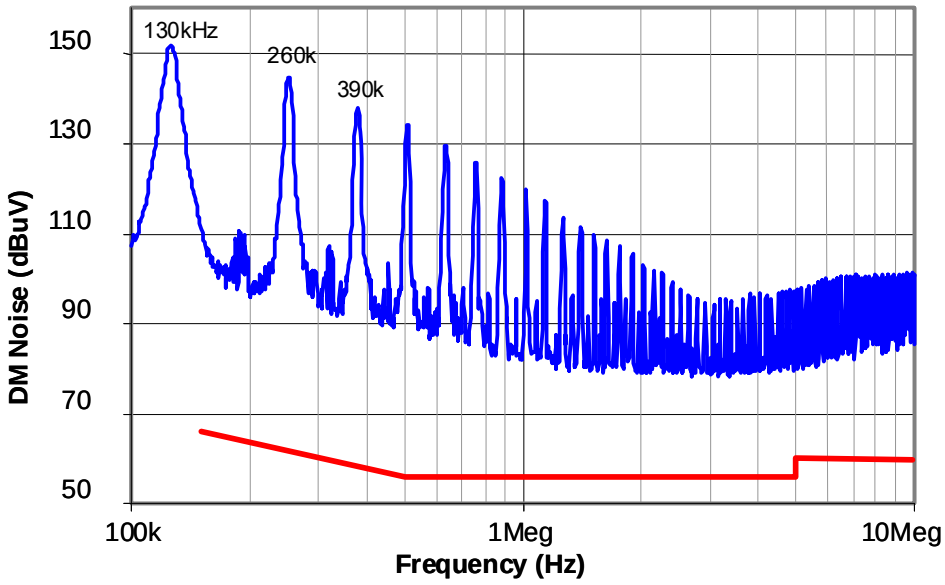


Figure 2.10. Filter corner frequency for different switching frequency design.

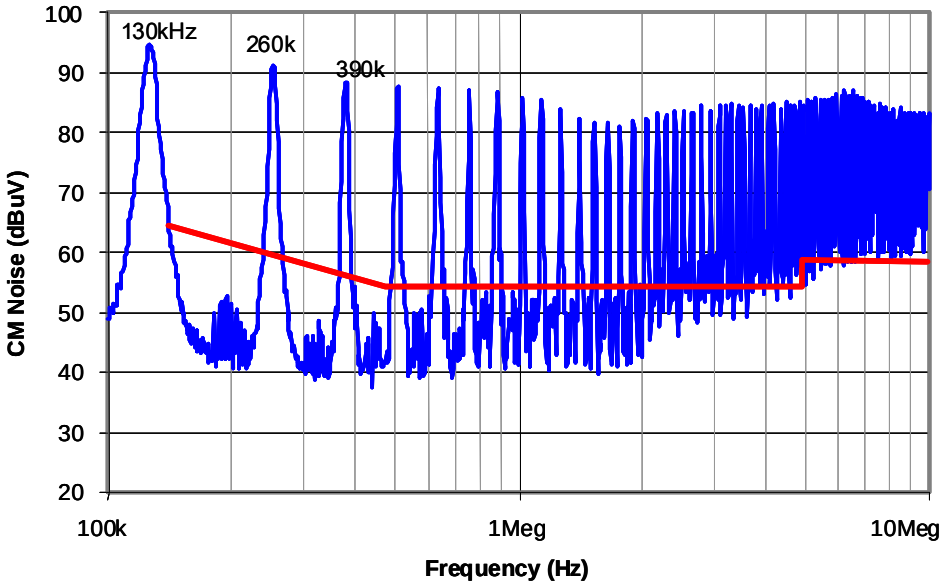
The switching frequency of the PFC is increased up to 130 kHz based on the EMI filter design considerations since the switching loss is greatly reduced. According to the previous studies [31][33], based on the filter attenuation requirement and the filter attenuation curve, we can get the relationship between the filter corner frequency and the switching frequency, as shown in Figure 2.10.

This zigzag shape of the curve is caused by the EMI standard, such as EN55022B, starts the regulation from 150 kHz. These jumping points frequency is *1/n* of 150 kHz, such as 150 kHz, 75 kHz, 50 kHz and etc. When the switching frequency is slightly lower than these frequencies, the filter corner frequency is much higher. As we know, the higher filter corner frequency will give smaller EMI filter size because the filter can be implemented with smaller capacitors and inductors. So from the EMI filter size standpoint, there are some preferred switching frequency regions. 65 kHz, 100 kHz and 130 kHz are some typical switching frequency adopted by industry products based on those concerns. Choosing 130 kHz becomes a better trade-off between the efficiency and the power density due to the reduction of the switching loss.

The measured Differential Mode (DM) and Common Mode (CM) noise is shown in Figure 2.11 (a) and (b) respectively. By designed the PFC switching at 130 kHz, the first noise peak is out of the regulation range. The EMI filter will be designed based on the second noise peak at 260 kHz.



(a) Measured DM noise



(b) Measured CM noise

Figure 2.11. Measured 130 kHz benchmark PFC EMI noise.

Based on the measured DM and CM noise, the filter attenuation requirement can be calculated as shown in Table 2.1.

Table 2-1. Filter attenuation requirement for the benchmark PFC

	Frequency	Noise Level	Standard	Desired Attenuation
DM	260 kHz	143 dBuV	61.4 dBuV	87.6 dB
CM	260 kHz	93 dBuV	61.4 dBuV	37.6 dB

An EMI filter is designed based on the calculated attenuation requirement. Two 4.7 nF capacitors are used as the Y capacitor. A 1.5 mH common mode inductor is implemented with ZJ-42908TC with 21 turns. The measured leakage inductance of the CM chock is 17 uH. With two additional DM inductors, the total DM inductance is 28 uH. To obtain the desired attenuation, two X capacitors are used, each capacitance is 2.15 uF.

The developed EMI filter prototype is shown in Figure 2.12. To meet the EMI Standard, the filter size is relatively large. It could take up to 23% of the whole AC-DC front-end converter for the state-of-the-art industry power supply products.

Figure 2.12. EMI filter prototype for the benchmark PFC.

130 kHz is also good in terms of the boost inductor size. For the benchmark PFC design, the boost inductor is implemented with two Koolmμ toroidal cores, 77083, in parallel. Due to the high current stress at low line, AWG#14 wire is used. The number of turns is 39. The inductor is also relatively large. It could take up to 16% of the total space

of a typical AC-DC front-end converter design. Although the boost inductor size can be reduced by higher switching frequency, the efficiency will be degraded due to the increasing switching loss. Since the efficiency is becoming the first priority now days, 130 kHz could be a good trade-off considering the both the efficiency and the EMI filter and inductor size.

2.3 Performance Evaluation of Interleaved PFC

In high power applications, paralleling devices in order to handle the high current stress is inevitable. Instead of paralleling devices, paralleling converters (modular approach) is more effective. This modular approach is widely used in distributed power systems for different applications. In this approach, the EMI filter is built inside each frond-end converter module and designed based on its own the EMI noise, as shown in Figure 1.14. Based on that architecture, one EMI filter can actually be put in front of all the PFC modules, and by interleaving these PFC modules the EMI filter size can be reduced due to the ripple cancellation effect. The reduced input ripple current means lower differential mode (DM) EMI noise magnitude. Not only the noise magnitude is lower, by interleaving m channels, the ripple current frequency will be increased by *m* times, which in some case will make the DM filter corner frequency higher. As it is known, higher corner frequency can be realized by smaller inductance and capacitance with smaller size. Finally the smaller EMI filter size will help to increase the power density, which is greatly desired in today's front-end converter design.

However, multi-channel interleaving impact on the PFC design actually has not been throughly explored according to the existing literatures. It is one of the objective of this study to fully investigate the multi-channel interleaving impact on the PFC in terms of EMI filter, hold-up bulk capacitor, and some system level power management designs.

2.3.1 Interleaved PFC and the existing studies

Multi-channel interleaving PFC has been studied by a lot of researchers in the past. The challenges of implementing the interleaving control has been well studied and analyzed [41][44][45][46][47], and several approaches have been proposed. There are also studies tried to quantify the input current ripple reduction by interleaving technique [1][47][48]. A general method for analyzing interleaved converters to predict ripple amplitudes has been proposed for both CCM and DCM [1], and was demonstrated with 8-channel interleaving DCM PFC operating at 25 kHz. The EMI filter size reduction was verified by prototype. The high frequency input RMS current reduction by interleaving is also analyzed and quantified [47], and used to predict the EMI noise reduction. A 3-kW telecom power supply using 2-channel interleaving CCM PFC operating at 100 kHz is prototyped and verified the study. The existing studies about the interleaving impact on the EMI filter design are based on the time domain ripple cancellation effective. However, both the EMI standard and the EMI measurement are based on the frequency domain spectrum. It is difficult to provide a clear picture about how exactly the multi-channel interleaving will impact the EMI filter design. Limited by the analysis approaches, the interleaving impact on the Common Mode (CM) noise also has not been studied in any existing literatures.

Frequency domain analysis method has been proposed to study the switching frequency impact on the EMI filter design for the single-channel PFC [33][49]. The noise source characteristic was obtained either from simulation or measurement results. Based on the obtained noise source spectrum, the switching frequency impact on both the DM and CM filter design for single channel PFC has been clearly plotted. Frequency domain analysis method is quite effective for studying the PFC EMI filter design. However, the frequency domain analysis method has not been investigated in the multi-channel interleaving architecture.

In this study, the frequency domain analysis method was adopted and improved with double Fourier integral transformation. With the double Fourier integral transformation, a closed-form expression of all the harmonics of the noise source can be obtained. With all the detail phase relationship of the switching frequency harmonics and all the side band harmonics, the multi-channel interleaving impact on the EMI filter design is investigated.

2.3.2 Interleaving impact on EMI filter design

For the interleaved PFC, the switching instances are phase shifted with uniform intervals. Ripple cancellation can be observed from the time domain waveforms, as shown in Figure 2.13 (2-channel interleaving as an example). The benefit and impact are easy to identify and understand. Based on the waveform, the ripple cancellation effect can be summarized in Figure 2.14 [50]. The effectiveness of ripple cancellation is a function of the converter duty ratio and the interleaving channel number. At certain condition, the ripple can even be totally eliminated, such as 2-channel interleaving with 50% duty ratio.

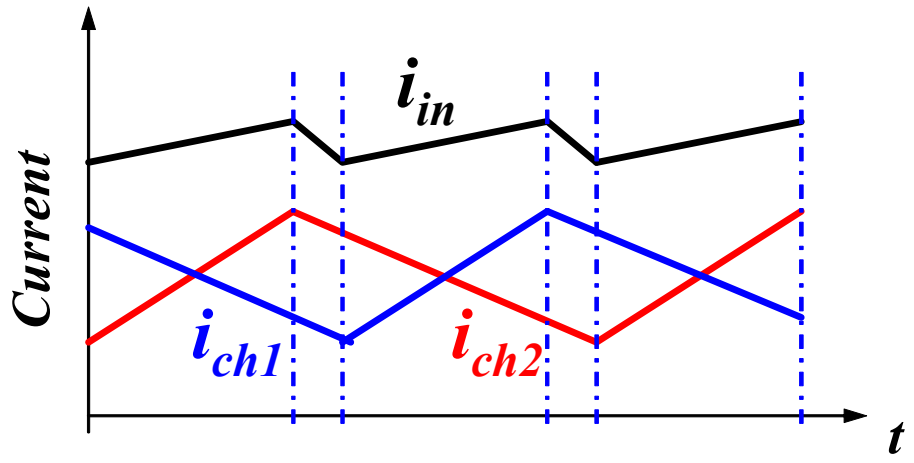


Figure 2.13. Ripple cancellation effect of 2-channel interleaving.

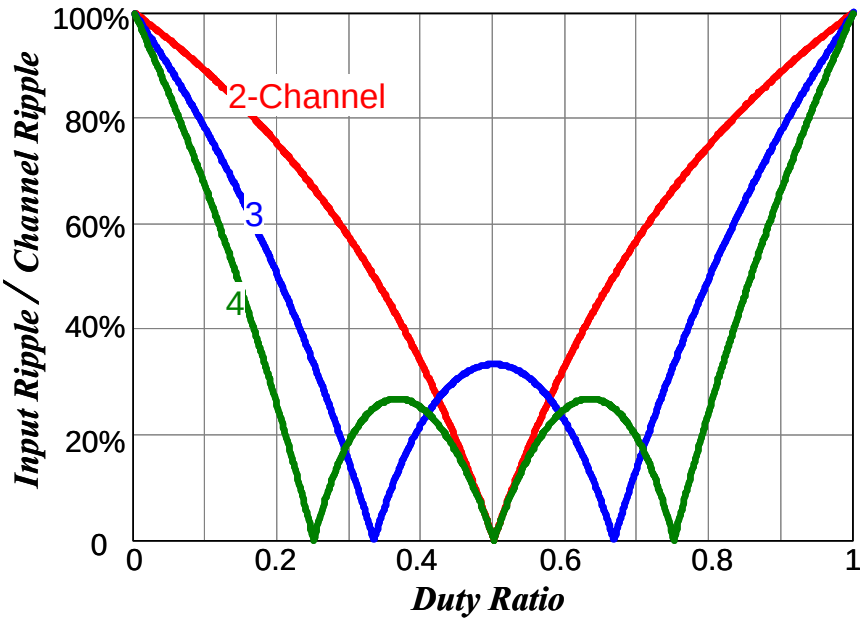


Figure 2.14. Effectiveness of ripple cancellation for interleaved converters.

The time domain waveform and ripple cancellation curves are quite effective to evaluate the benefit on the multi-channel interleaved DC-DC converters. However, it is a little more complicated when is applied to evaluate the benefit on EMI filter design for multi-channel interleaved PFC. The duty ratio varies with the input voltage in the PFC circuit. The duty ratio could vary from 1 to almost 0 within half of the line cycle depending on the input line voltage condition and the output voltage design. Accordingly, the cancellation will have a big variation within half of the line cycle. To make things more complicated, the PFC input current ripple magnitude is not a constant either. All these factors make it difficult to analyze and identify the interleaving impact on the EMI filter design.

An alternative view angle of this issue is from the harmonic cancellation effect in the frequency domain. In order to make it easier to explain, the 2-channel interleaving is used as an example. The analysis method and results can be easily extended to other channel number designs. Figure 2.15 shows a 2-channel interleaved PFC circuit diagram with Line Impedance Stabilization Networks (LISN). Two identical boost converters are parallel connected. Two gate signals controlled with 180° phase shift.

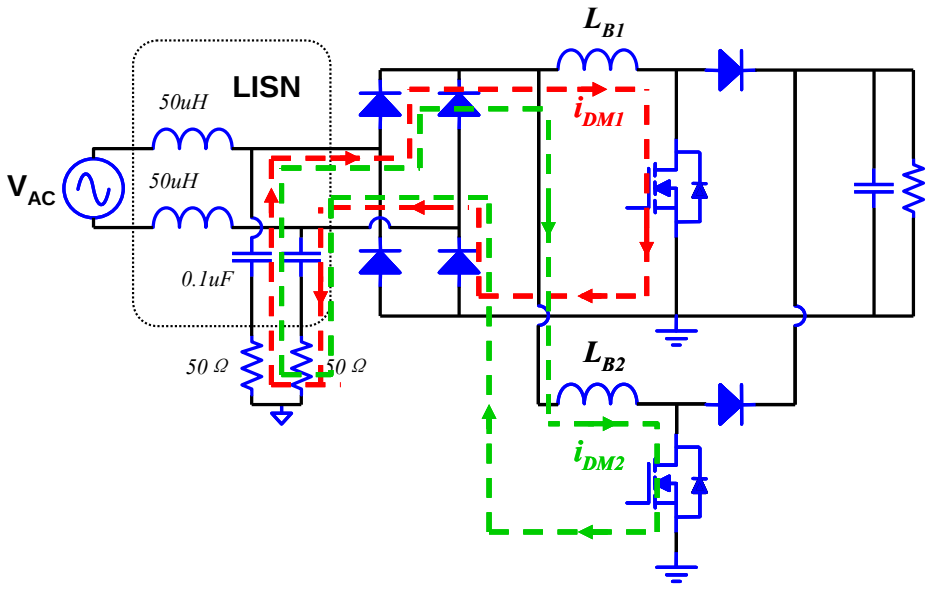


Figure 2.15. 2-Channel interleaved PFC circuit diagram with LISN.

The MOSFET drain-source voltage can be considered as the EMI noise sources. The differential mode (DM) noise model for single channel PFC has been proposed [51]. For 2-channel interleaved PFC, following the same procedure, the simplified conducted DM noise model is shown in Figure 2.16. L_1 and L_2 are the boost inductors of two interleaved channels. V_{n1} and V_{n2}, represent the two pulsating noise sources generated by two channels. The DM noise is defined as,

$$\left|V_{DM}\right| = \left|\frac{V_2 - V_1}{2}\right| \tag{2-1}$$

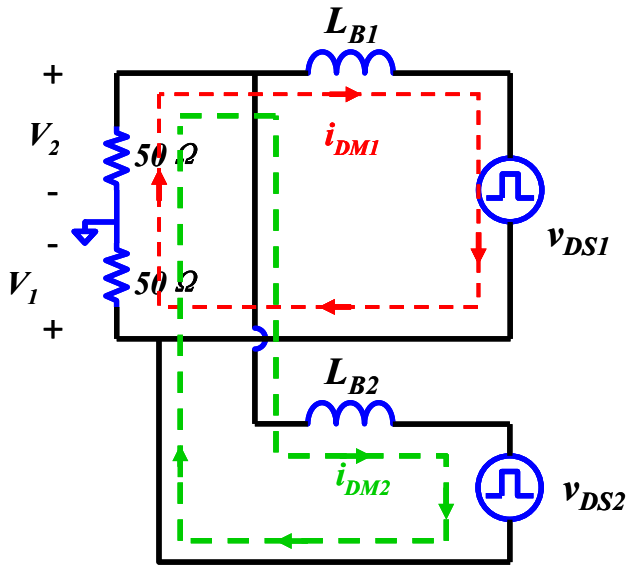


Figure 2.16. DM noise model for two-channel interleaved PFC.

The time domain waveform of two noise sources are shown in Figure 2.17, $v_{DS}(t)$. For illustration, much lower switching frequency is used in the drawing. The average voltage of the noise source follows a sinusoidal waveform as shown in Figure 2.17.

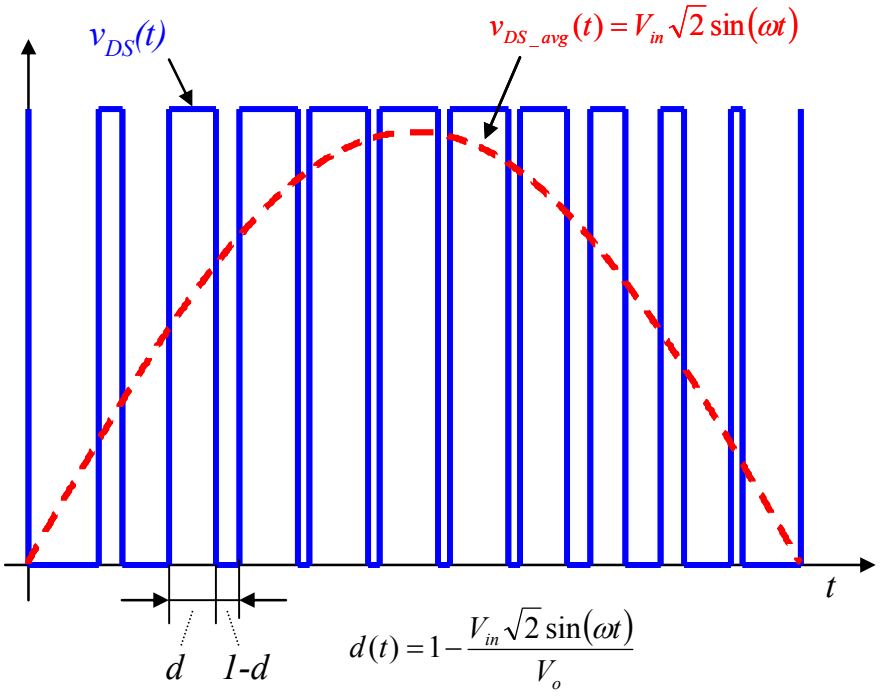


Figure 2.17. Noise sources time domain waveform.

Using Double Fourier integral transformation [52], the noise source can be expressed as,

$$\begin{aligned} v_{DS}(t) &= V_o + V_o M\cos(\omega_o t + \theta_o) \\ &\quad + \frac{2V_o}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\left[\cos m\pi - J_0(m\pi M)\right]\sin\left(m\left[\omega_c t + \theta_c\right]\right) \\ &\quad + \frac{2V_o}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n(m\pi M)\begin{bmatrix}\sin n\frac{\pi}{2}\cos\left(m\left[\omega_c t + \theta_c\right] + n\left[\omega_o t + \theta_o\right]\right) \\ -\cos n\frac{\pi}{2}\sin\left(m\left[\omega_c t + \theta_c\right] + n\left[\omega_o t + \theta_o\right]\right)\end{bmatrix} \end{aligned} \tag{2-2}$$

Where,

ωc – switching angular frequency;

ωo – fundamental angular frequency;

θc – arbitrary phase offset angle for switching waveform;

θo – arbitrary phase offset angle for fundamental waveform;

m – order of switching frequency harmonic;

n – order of side band harmonic;

Based on Equation (2-2), the spectrum of the two noise sources v_{DS1} and v_{DS2} can be obtained. For the switching frequency,

Phase 1:

$$\frac{2V_o}{\pi}\frac{1}{m}\left[\cos m\pi - J_0(m\pi M)\right]\sin\left(m\omega_c t\right) \tag{2-3}$$

Phase 2:

$$\frac{2V_o}{\pi}\frac{1}{m}\left[\cos m\pi - J_0(m\pi M)\right]\sin\left(m\omega_c t + m\theta_s\right) \tag{2-4}$$

Where θs is the phase shift angle for switching waveform. In this 2-channel interleaving case, it is π.

For the Sideband harmonics,

Phase 1:

$$\frac{2V_o}{\pi}\frac{1}{m}J_n(m\pi M)\begin{bmatrix}\sin n\frac{\pi}{2}\cos(m\omega_c t+n\omega_o t)\\ -\cos n\frac{\pi}{2}\sin(m\omega_c t+n\omega_o t)\end{bmatrix} \tag{2-5}$$

Phase 2:

$$\frac{2V_o}{\pi}\frac{1}{m}J_n(m\pi M)\begin{bmatrix}\sin n\frac{\pi}{2}\cos(m\omega_c t+n\omega_o t+m\theta_s)\\ -\cos n\frac{\pi}{2}\sin(m\omega_c t+n\omega_o t+m\theta_s)\end{bmatrix} \tag{2-6}$$

The voltage drop on the two LISN resistors corresponds to the measured DM noise, and they can be solved for each switching frequency harmonics. With phase shift of π, according to Equations (2-3), (2-4), (2-5) and (2-6), all the first order harmonics of two channels are out of phase. Assume two channels are identical. Solving the circuit or simply using the superimposition principle, there will be zero voltage on the LISN resistors at this frequency. They cancelled each other. For all the two second order harmonics, the phase shift between them becomes 2π; therefore, they are in phase. The LISN resistors will see the sum of these two noise sources at this frequency, which will be the same as the single channel PFC design if they were kept the same channel current ripple percentage. For the third order harmonics, the phase shift is 3π. They are again cancelled each other. For this 2-channel interleaving case, it is obvious that all the odd order harmonics are cancelled and the even order harmonics are added together.

For 3-channel interleaved PFC ($3\pi/2$ phase shifted), applying the same analysis approach, the $(3n+1)^{th}$ and $(3n+2)^{th}$ $(n = 0, 1\ldots \infty)$ order harmonics are cancelled. Only $3n^{th}$ order harmonics exist in the EMI noise measurement results. The analysis and results can be easily extended to other multi-channel interleaved PFC.

The equivalent EMI filter corner frequency can be used to quantify the EMI filter size [33][34][35]. As it is known, higher EMI filter corner frequency is desirable because it can be realized by smaller inductance and capacitance with smaller size. Based on the EMI noise attenuation requirement and the EMI filter attenuation curve, the relationship

between the filter corner frequency and the switching frequency for different interleaving channel numbers is shown in Figure 2.18 (Assume two-stage EMI filter is used).

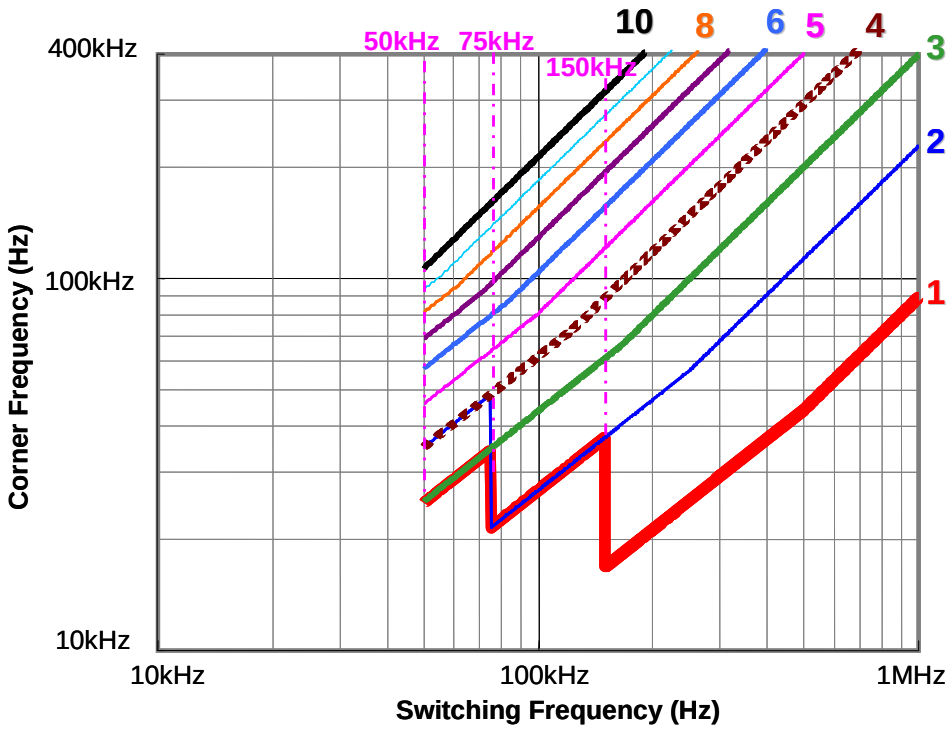


Figure 2.18. DM filter corner frequency v.s. switching frequency for different interleaving channel numbers.

Because the EMI standard, such as EM55022B [53], starts the regulation from 150 kHz, for single channel PFC, it is recognized that there are some preferred switching frequency regions in terms of the EMI filter size. Normally, the switching frequency is designed either below 75 kHz or 150 kHz, because slight higher than 75 kHz or 150 kHz there will be a big size penalty on the EMI filter. From Figure 2.18, considering the EMI filter size, the preferred PFC switching frequency region for interleaved PFC is quite different for different channel numbers. For the 2-channel interleaving PFC, it is preferred to operate either below 75 kHz or higher that 200 kHz. There is no benefit in terms of filter size when the switching frequency is designed between 75 kHz and 200 kHz. For 3-channel interleaving, the switching frequency is preferred to be designed either below 50 kHz or higher than 140 kHz. With more channels to interleave, the preferred switching frequency will keep changing. It should be pointed out that by properly choosing the

interleaving channel number and the switching frequency the filter corner frequency can be significantly improved as can be observed in Figure 2.18.

The noise cancellation effect not only happens for the DM, it also happens for the CM. The simplified conducted CM noise model for 2-channel interleaved PFC is shown in Figure 2.19. C_{d1} and C_{d2} are the parasitic capacitors between MOSFETs' drains and the ground. V_{n1} and V_{n2}, represent the two pulsating noise sources generated by two channels. The CM noise is defined as,

$$\left|V_{CM}\right| = \left|\frac{V_2 + V_1}{2}\right| \tag{2-7}$$

The analysis results show that similar conclusions can be made for the CM noise. For the 2-channel interleaved PFC, the odd order CM noises get cancelled and no impact on the even order CM noises. The analysis and results can be easily extended to other multi-channel interleaved PFC.

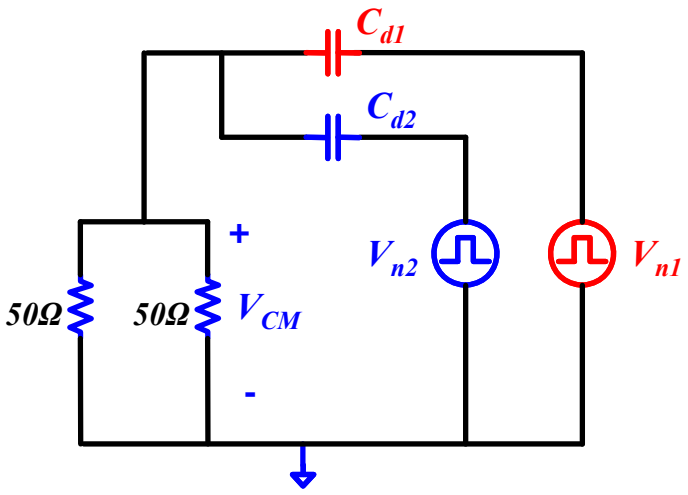


Figure 2.19. CM noise model for two-channel interleaved PFC.

Using the same approach, the CM filter corner frequency v.s. the switching frequency for different interleaving channel numbers is shown in Figure 2.20 (Assume two-stage EMI filter is used). The trend and the preferred switching frequency region are similar to the DM filter.

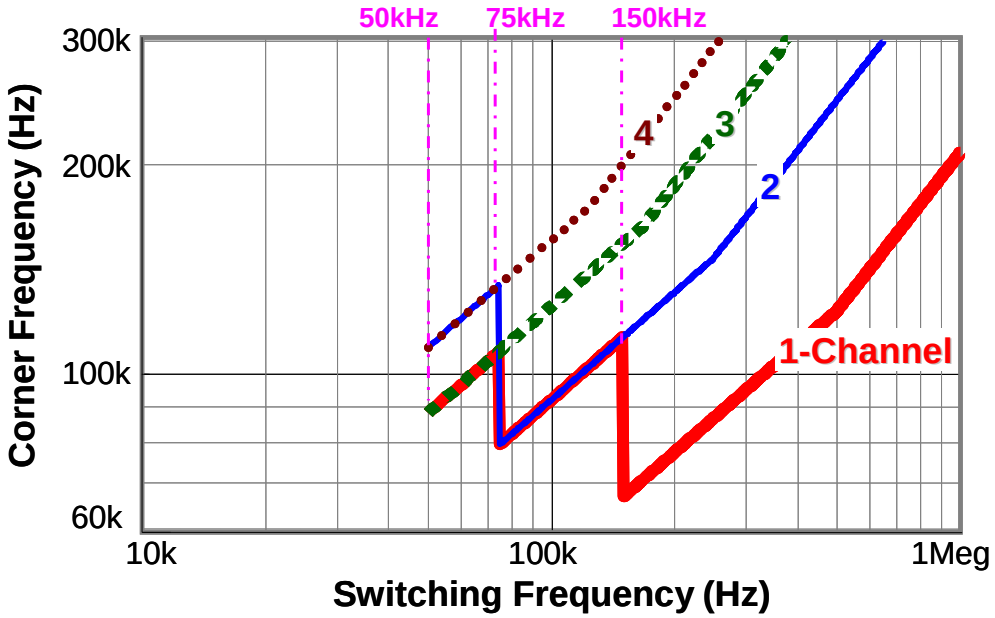


Figure 2.20. CM filter corner frequency v.s. switching frequency for different interleaving channel numbers.

2.3.3 Interleaving impact on output capacitor

Bulky electrolytic capacitors are usually used at the PFC output terminals to provide the energy during the hold-up time. Due to the equivalents series resistance (ERS) of the capacitor, the ripple current generates power loss. The temperature rise caused by the power loss may seriously shorten the capacitor life time. The life time of these electrolytic capacitors could be a big concern in the AC-DC power supplies. According to the capacitor manufactures, the capacitor life time can be estimated based on the equation below [35],

$$L_n = L_o \times 2^{\frac{T_0 - T_n}{10}} \times 2^{\alpha\left\{1-\left(\frac{I_n}{I_m}\right)^2 \times 2^{-\left(\frac{T_o - T_n}{30}\right)}\right\}} \tag{2-8}$$

Where,

L_n: Estimated life time (hour) at ambient temperature of T_n (℃) with a ripple current I_n (Arms) applied;

L_o: Specified life time (hour) at maximum operating temperature T (℃) with the specified maximum allowable ripple current I_m (Arms) at T (℃) applied

T_o: Maximum operating temperature of the capacitor (℃)

T_n: Ambient temperature of the capacitor (℃)

I_m: Rated ripple current (Arms) at maximum operating temperature T (℃)

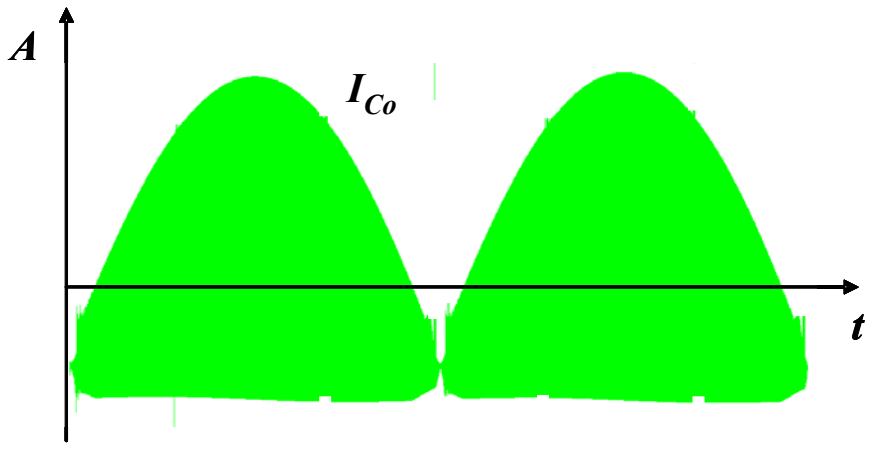
I_n: Ripple current (Arms) actually applied at ambient temperature T_n (℃)

α : Life constant

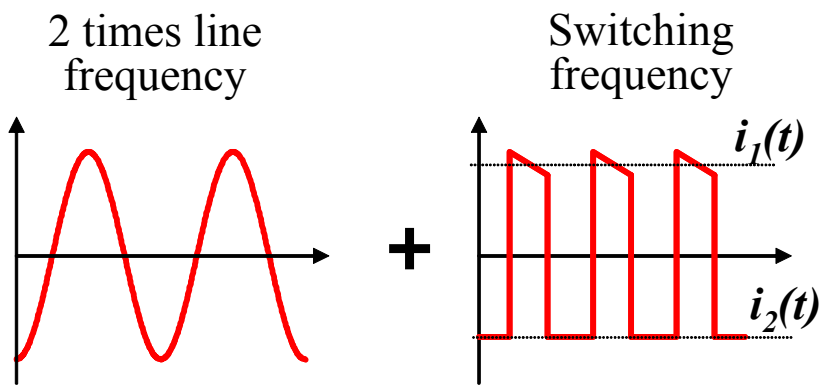
To achieve the desired capacitor life time, either the larger or more capacitors need to be used to have enough rated current ripple I_m, or the actual ripple current I_n of capacitor need to be controlled below certain value. Interleaving multi-channel PFC can reduce this current ripple I_n of the output capacitor due to the ripple cancellation effect. The output capacitor ripple current reduction of the interleaving PFC will be investigated in this part.

a. PFC output capacitor current ripple

For the boost PFC circuit, the output capacitor ripple current can be decomposed into two components, the high frequency ripple and the low frequency ripple, as shown in Figure 2.21. The low frequency ripple is mostly at two times the line frequency (100 Hz or 120 Hz), assuming the power factor is almost unity. The high frequency ripple is the switching frequency ripple current.



(a) Simulation waveform of the output capacitor



(b) Decomposed capacitor ripple current (Different time scales are used for 2 times line frequency and the switching frequency)

Figure 2.21. PFC output capacitor current ripple.

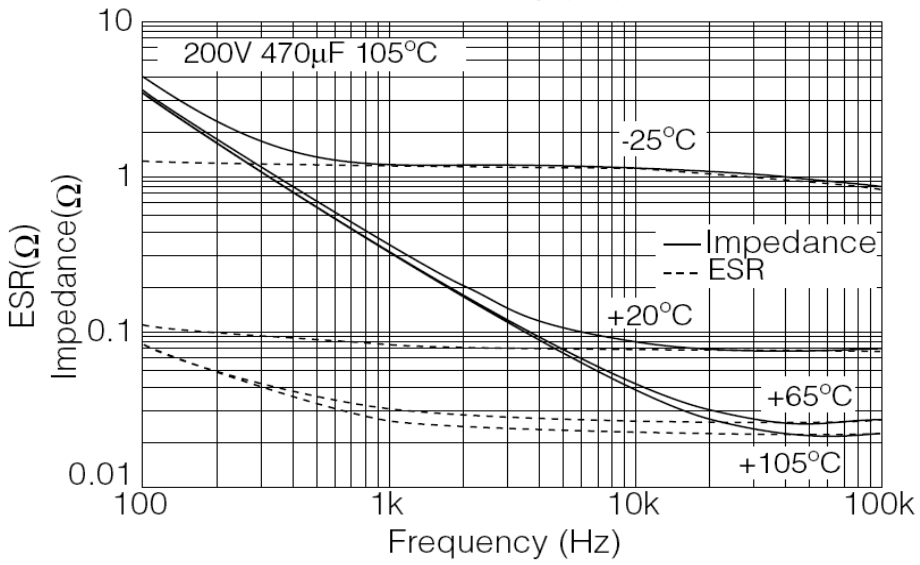


Figure 2.22. Impedance, ESR v.s. frequency (Example).

To estimate the capacitor life time, both components need to be considered. The ESR of the electrolytic capacitor is frequency dependant, Figure 2.22 [54] showing one good example. The ESR decreases as the frequency increases, which means to keep the same temperature rise, larger current is allowed when the frequency is higher. To calculate the effective capacitor ripple I_n in Equation (2-9), frequency coefficient K_f need to be considered. The effective capacitor current ripple can be calculated by using the following equation,

$$I_n = \sqrt{\left(\frac{I_L}{K_{fL}}\right)^2 + \left(\frac{I_H}{K_{fH}}\right)^2} \tag{2-9}$$

Where, I_L is the low frequency ripple current; I_H is the high frequency ripple current; K_{fL} is the low frequency coefficient; K_{fH} is the high frequency coefficient.

Interleaving has no impact on the low frequency current ripple as long as the power factor function is well achieved, since this ripple current is caused by the pulsating input power of PFC. However, interleaving will impact the switching frequency ripple greatly.

b. Single-channel PFC

The output capacitor current ripple of the benchmark PFC design, the single-channel PFC, is calculated in this section for the comparison purpose.

To simplify the calculation, the inductor current ripple impact is neglected, assuming the capacitor switching frequency ripple is a square wave. The envelope of the capacitor square wave is a function of time, which can be calculated as,

$$\begin{cases} i_1(t) = i_{in}(t)d(t) = I_{in\_peak}\left|\sin(2\pi f_L t)\right|\left(1 - \dfrac{V_{in\_peak}\left|\sin(2\pi f_L t)\right|}{V_o}\right) \\ i_2(t) = i_{in}(t)\left[1 - d(t)\right] = I_{in\_peak}\dfrac{V_{in\_peak}\sin^2(2\pi f_L t)}{V_o} \end{cases} \tag{2-10}$$

Where, $i_1(t)$ and $i_2(t)$ represent the maximum and minimum current; f_L is the line frequency; $i_{in}(t)$ is the input current; $d(t)$ is the duty ratio.

The switching frequency current ripple RMS value can be calculated as,

$$i_{rms\_1}(t) = \sqrt{i_1(t)^2\left[1 - d(t)\right] + i_2(t)^2 d(t)} \tag{2-11}$$

Based on Equation (2-11), the RMS current variation within half of the line cycle can be plotted out, as shown in Figure 2.23 (a) (b), which is calculated based on a 1200 W PFC design. The high frequency current I_H can be calculated as,

$$I_{H\_1} = \sqrt{\frac{2}{T_{line}}\int_0^{\frac{T_{line}}{2}} i_{rms\_1}(t)dt} \tag{2-12}$$

The high frequency RMS ripple current I_H varies with the input line voltage, and can be plotted out, as shown in Figure 2.24, which again is calculated based on a 1200 W PFC design.

The low frequency RMS current I_L can be calculated as,

$$I_{L\_1} = \sqrt{\frac{2}{T_{line}} \int_0^{\frac{T_{line}}{2}} \left[I_{in\_peak} \frac{V_{in\_peak} \sin^2(2\pi f_L t)}{V_o} - I_{load} \right] dt} \tag{2-13}$$

Where, I_{load} is the average load current.

Finally, the effective capacitor current ripple can be calculated based on Equation (2-8), (2-12) and (2-13), with frequency coefficient obtained from the corresponding capacitor datasheet or manufacture.

c. Multi-channel Interleaved PFC

Interleaving multi-channel PFC can reduce the high frequency current due to the ripple cancellation effect. A 2-channel interleaved PFC will be one example to study the output current reduction achieved by interleaving.

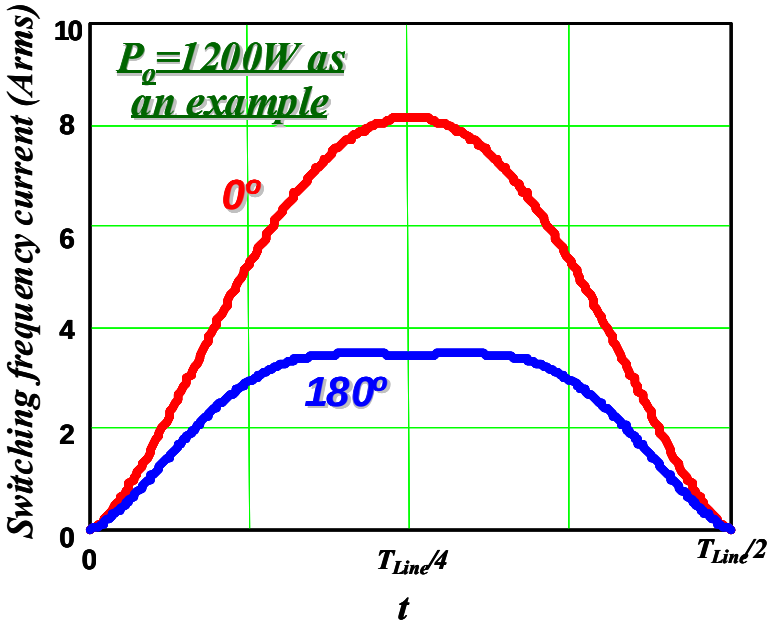
The switching frequency current ripple RMS value can be calculated as,

$$I_{rms\_2}(t) = \begin{cases} 2d(t)\left[i_2(t) - i_1(t)\right]^2 + 8i_1(t)^2\left[0.5 - d(t)\right] & when d \le 0. \\ 2\left[1 - d(t)\right]\left[i_1(t) - i_2(t)\right]^2 + 8i_2(t)^2\left[d(t) - 0.5\right] & when d > 0. \end{cases} \tag{2-14}$$

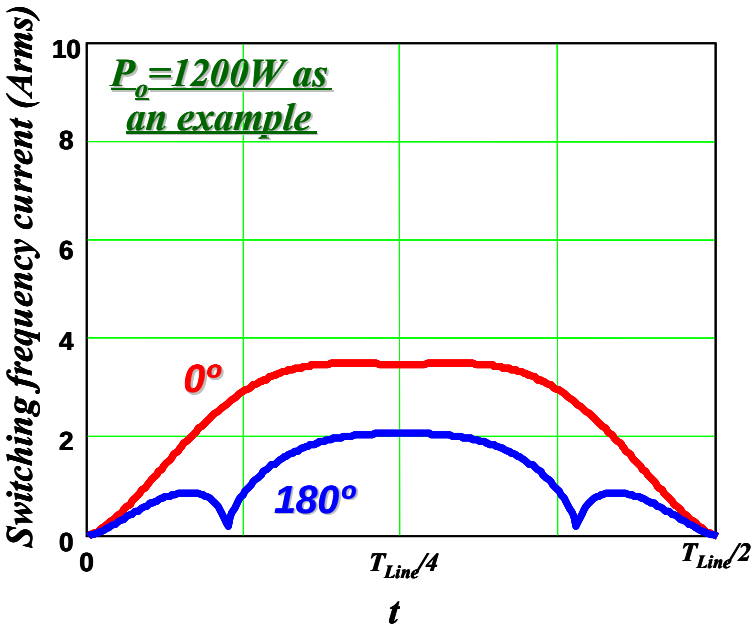
For two-channel interleaving, the RMS current variation within half of the line cycle is plotted out in Figure 2.23 (a) (b). 2-channel interleaved PFC can effectively reduce the switching frequency current ripple for both low line and high line.

The high frequency current I_H can be calculated as,

$$I_{H\_2} = \sqrt{\frac{2}{T_{line}} \int_0^{\frac{T_{line}}{2}} i_{rms\_2}(t) dt} \tag{2-15}$$



(a) Low line: V_{in} = 110 Vac



(b) High line: V_{in} = 220 Vac

Figure 2.23. Output capacitor RMS current within half line cycle.

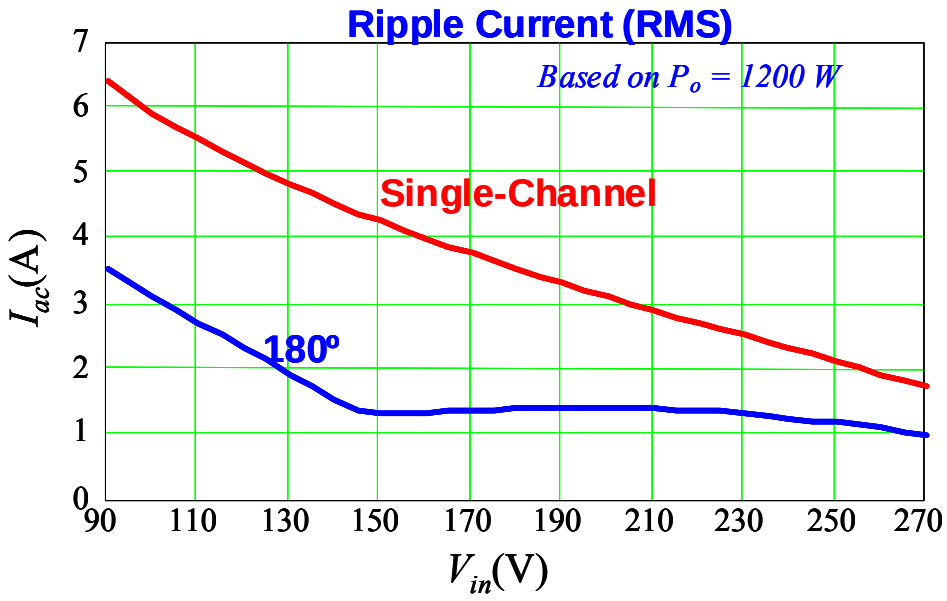


Figure 2.24. High frequency RMS current at different input line voltage.

The high frequency RMS current I_H varies with the input line voltage, and can be plotted out, as shown in Figure 2.24. Based on calculation, with two-channel interleaving, more than 50% of the high frequency RMS ripple current is reduced for both typical high line and low line input voltage. Using Equation (2-8), the effective capacitor current ripple can be calculated.

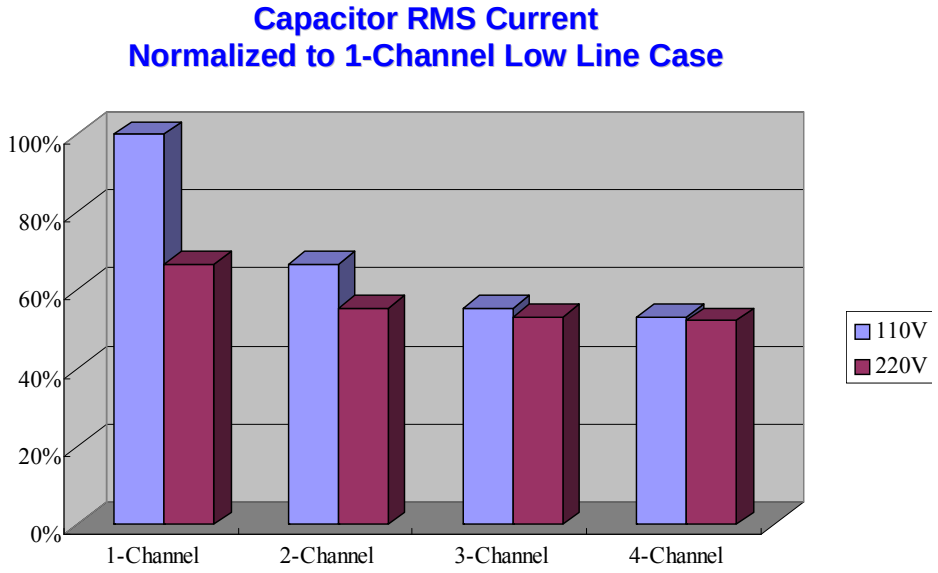


Figure 2.25. Output capacitor RMS current reduction with multi-channel interleaving.

Following the same procedure, the effective capacitor current ripple of other multi-channel interleaved PFC can be obtained, as shown in Figure 2.25.

2.4 Coupled Inductor for Interleaved PFC

Ripple cancellation is one of the most important features of interleaving technique. However, it should be pointed out that interleaving only reduces the total input and output current ripple; the inductor current in each channel still has large ripple if small inductance are used. The large conduction and switching losses in the MOSFET and the copper losses in the inductors that occur due to the large current ripples cannot be solved by interleaving technique.

The situation was the same for the multi-phase VR application until the concept of applying coupling inductors between the interleaved channels was introduced to the multiphase interleaved buck converter. Coupling inductors have different equivalent inductances for steady-state and transient responses. Inverse coupling inductors between the interleaved channels reduce the steady-state current ripples while maintaining the same transient resoponses.

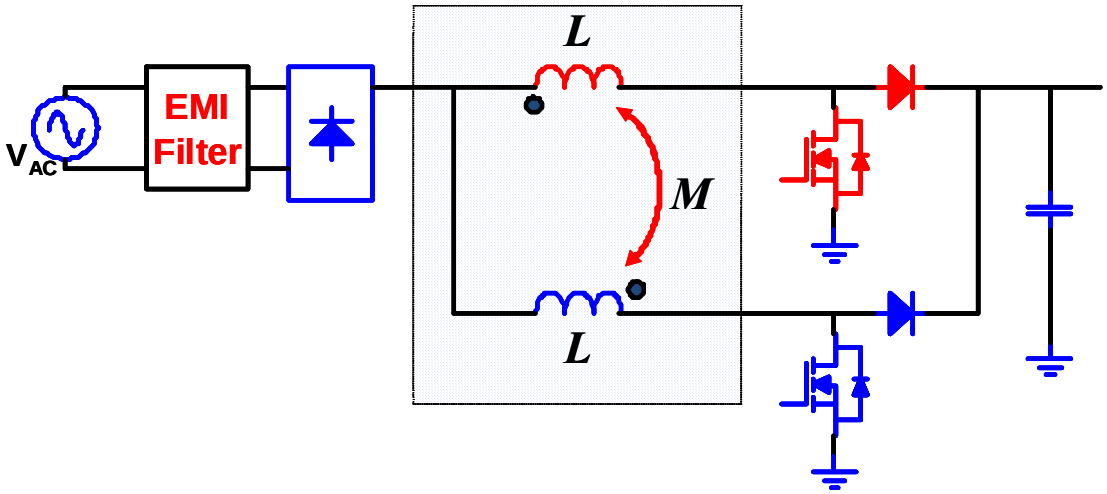


Figure 2.26. Two-channel interleaved PFC with coupled inductor.

The coupled inductor concept also can be introduced into multi-channel interleaved PFC. In this section, the interleaved PFC with coupled inductor will be investigated. For simplisity, two-channel interleaved PFC is used as an example for exploration, as shown in Figure 2.26.

2.4.1 Non-linear inductor of interleaved PFC

Because of the coupling effect, the two inductors in the two channels can no longer be considered as two individual inductors any more. Coupling inductance *M* between the two inductors is introduced to represent the inverse coupling effect, as shown in Figure 2.27, the simplified circuit diagram.

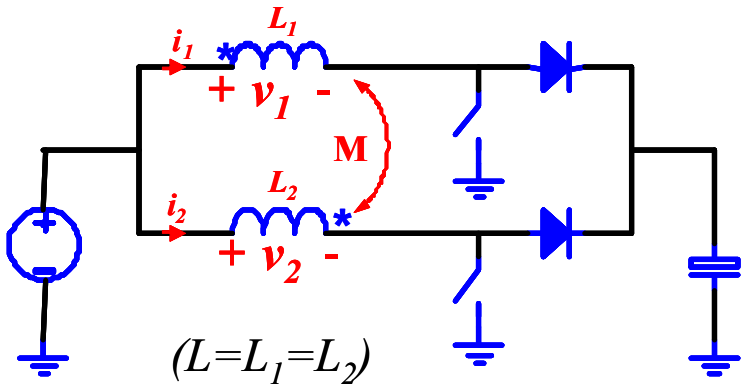


Figure 2.27. Interleaved 2-channel boost converter with inverse coupled inductors.

With the variables defined in Figure 2.27, the following equations can be obtained:

$$\begin{cases} v_1 = L_1 \cdot \dfrac{di_1}{dt} - M \cdot \dfrac{di_2}{dt} \\ v_2 = L_2 \cdot \dfrac{di_2}{dt} - M \cdot \dfrac{di_1}{dt} \end{cases} \tag{2-16}$$

v_1 and v_2 are the voltages applied to the two corresponding inductors. There are two possible voltage values for v_1 and v_2: v_a, corresponding to the boost switch conducting period; and v_b, corresponding to the diode conducting period:

$$\begin{cases} v_a = v_{in} \\ v_b = v_{in} - v_o \end{cases} \tag{2-17}$$

Where v_{in} and v_o are the input and output voltage of the boost converter respectively. The waveforms for v_1 and v_2 for duty cycle $D < 0.5$ are shown in Figure 2.28.

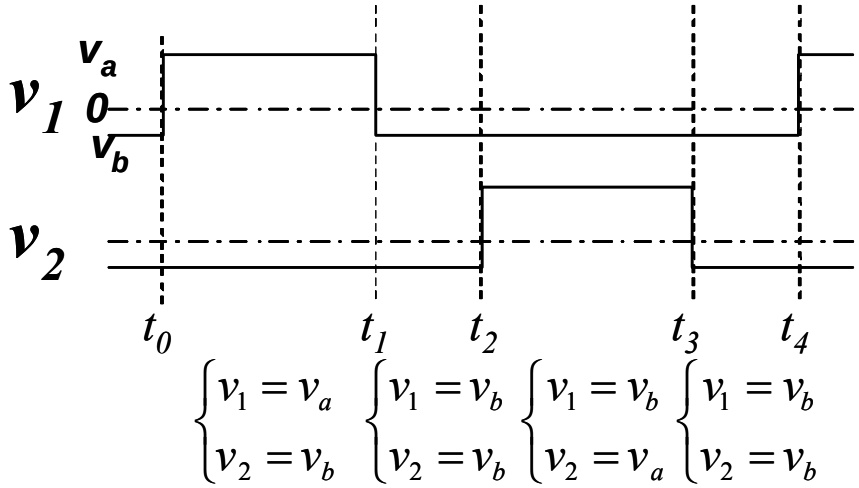


Figure 2.28. Inductor voltage waveforms (D < 0.5).

One switching cycle can be divided into four time intervals. The relationships between v_1 and v_2 are different in each time interval. During ($t_0 \sim t_1$), the boost switch of the first channel is on ($v_1 = v_a$), and the boost diode of the second channel is on ($v_2 = v_b$). With (2-16), and (2-17), v_1 can be rewritten as follows:

$$v_1 = \frac{L^2 - M^2}{L - \frac{D}{D'} \cdot M} \cdot \frac{di_1}{dt} \tag{2-18}$$

For the non-coupled inductor case ($M = 0$), (3.1) can be rewritten as follows;

$$\begin{cases} v_1 = L_1 \cdot \dfrac{di_1}{dt} \\ v_2 = L_2 \cdot \dfrac{di_2}{dt} \end{cases} \tag{2-19}$$

Using the preceding mathematical operations, the equations for the two-channel interleaved boost with coupled inductor can be decoupled. The v_1 expression in (2-19) has the same format as (2-18). An equivalent inductance can be defined by comparing (2-18) and (2-19). For simplicity, only the equivalent inductance in the first channel is discussed.

The equivalent inductance in the second channel is similar except for a phase shift. For the first channel, the equivalent inductance in the time interval of ($t_0 \sim t_1$) is as follows:

$$L_{eq1} = \frac{L^2 - M^2}{L - \frac{D}{D'} \cdot M} \tag{2-20}$$

For different time intervals, (2-16) is always true. However, (2-17) will change according to the relationship between the two inductor voltages in the time intervals. Thus, different equivalent inductances can be derived for each time interval in one switching cycle.

For time interval ($t_1 \sim t_2$), the boost diodes of both channels are turned on. The voltages applied to the two channels are the same. In this time interval, (2-17) needs to be changed to:

$$\begin{cases} v_1 = v_b \\ v_2 = v_b \end{cases} \tag{2-21}$$

With (2-17), and (2-21), v_1 can be rewritten as follows:

$$v_1 = (L - M) \cdot \frac{di_1}{dt} \tag{2-22}$$

Based on (2-22), the equivalent inductance for the first channel during time interval ($t_1 \sim t_2$) can be defined as follows:

$$L_{eq2} = L - M \tag{2-23}$$

Similarly, for time interval ($t_2 \sim t_3$), the equivalent inductance can be derived as follows:

$$L_{eq3} = \frac{L^2 - M^2}{L - \frac{D'}{D} \cdot M} \tag{2-24}$$

During time interval ($t_3 \sim t_4$), the voltages applied to the two inductors are exactly the same as during time interval ($t_1 \sim t_2$). Thus, the equivalent inductance in this time interval is L_{eq2}. There are three different equivalent inductances in one switching cycles.

The voltage waveforms for the case of steady-state duty cycle $D > 0.5$ are shown in Figure 2.29.

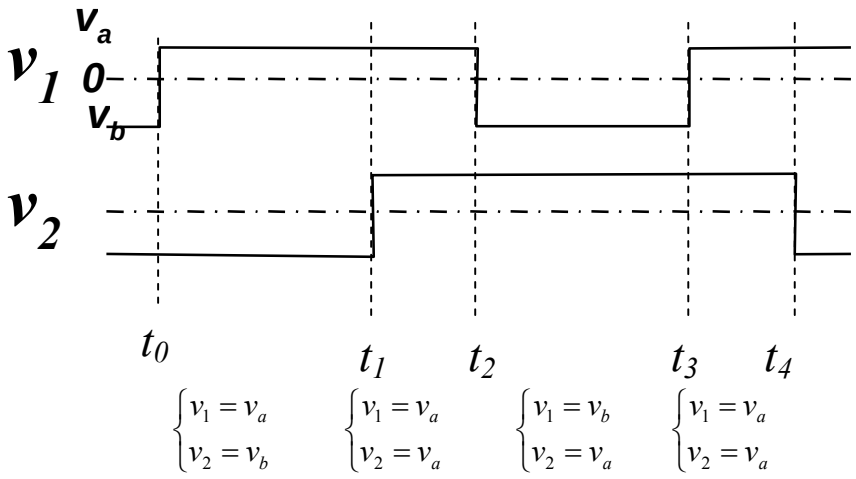


Figure 2.29. Inductor voltage waveforms (D > 0.5).

Following the same procedure as for the case in which $D < 0.5$, the equivalent inductances for all the four time intervals in one switching cycle can be found. The results shows that the equivalent inductances are the same for case of $D > 0.5$ and case of $D < 0.5$

The equivalent inductances can be used to mathematically decouple the coupled inductors so that they are comparable to the non-coupled inductors. The coupled inductor case has different equivalent inductances during each time interval in one switching cycle, while the inductance in for the non-coupled inductor case is always constant for the whole switching cycle.

For the non-coupled inductor there is only one inductance for both the input and the inductor current ripples. However, for the coupled inductor case, the total input current ripple and the inductor current ripple are determined by different equivalent inductance.

Figure 2.30 compares the input and inductor current ripple of coupled inductor and non-coupled inductor case when $D < 0.5$. The inductor voltage waveforms are exactly the same for both cases. The solid lines are the inductor current waveforms, while the dotted-

dashed lines are the inductor current waveforms for non-coupled inductor case. Assume the inductor design resulting in the same input current waveform.

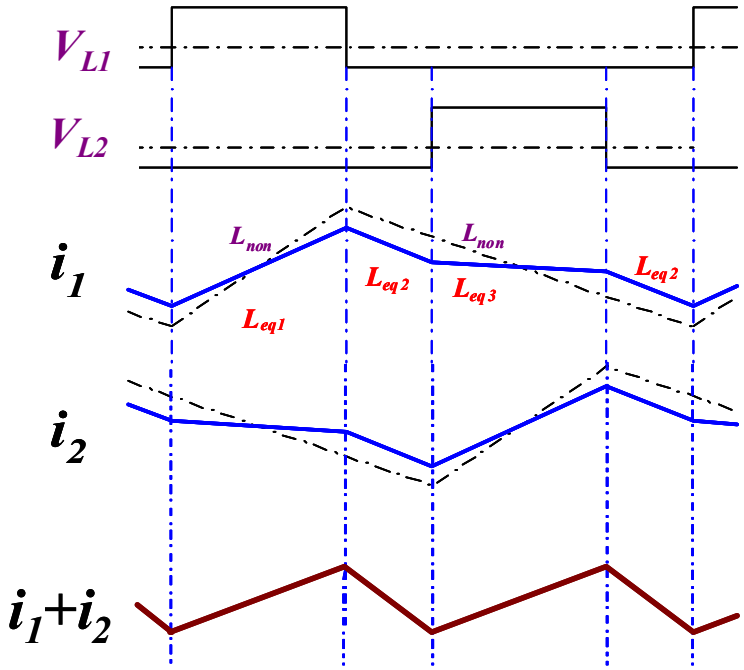


Figure 2.30. Inductor current and input current waveforms comparison for coupled inductor and non-coupled inductor (D < 0.5).

According to the current waveforms in Figure 2.30, the inductor current ripple is determined only by L_{eq1} for the coupled inductor case. The inductor peak-to-peak current ripple is described in (2-25).

$$I_{cL\_pp} = \frac{v_{in} D}{L_{eq1} f_s} \tag{2-25}$$

The inductor peak-to-peak current ripple of the non-coupled inductor case is described in (2-26).

$$I_{ncL\_pp} = \frac{v_{in} D}{L_{non} f_s} \tag{2-26}$$

The input current ripple is determined only by L_{eq2} for the coupled inductor case. For the non-coupled inductor case, the input current ripple is determined by L_{non}. The input current peak-to-peak ripple will be the same when $L_{eq2} = L_{non}$.

According to (2-20), the inductor current ripple is always smaller for the inverse coupled inductor case when $L_{eq2} = L_{non}$.

Figure 2.31 compares the input and inductor current ripple of coupled inductor and non-coupled inductor case when $D > 0.5$. The results and the conclusions are similar the case when $D < 0.5$.

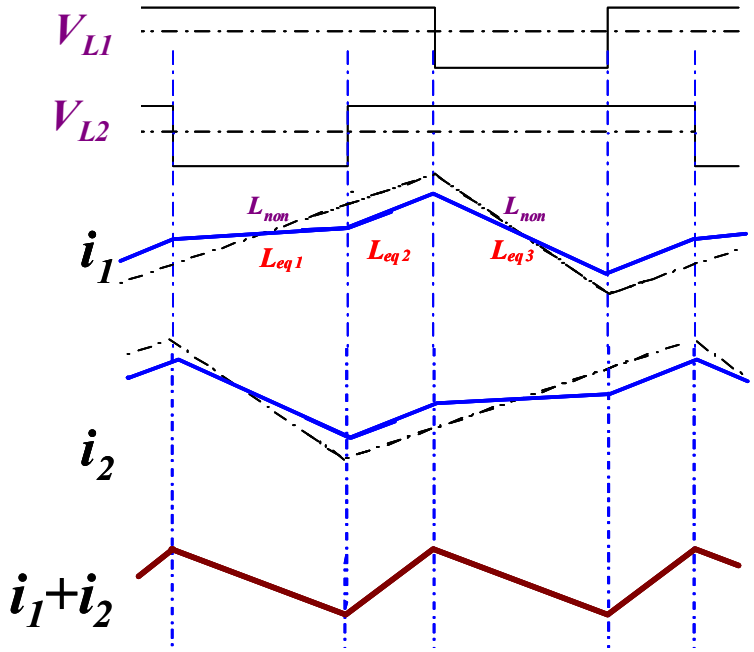


Figure 2.31. Inductor current and input current waveforms comparison for coupled inductor and non-coupled inductor (D > 0.5).

2.4.2 Implementation of coupled inductor for interleaved PFC

The Ferrite E-I cores was used in the multi-phase VR to implement the coupled inductors. For the CCM boost PFC, toroidal cores are usually used to implement the boost inductor. For the toroidal cores, Molypermalloy Powder (MPP), High Flux, and Kool Mu are popular materials. These toroidal cores have a distributed air gap which makes them

free of gap loss problems associated with ferrite cores. The higher saturation level of these materials provides a higher energy storage capability than can be obtained with gapped ferrite E-I cores, resulting in smaller core size. These factors make the toroidal cores the most popular for the CCM boost PFC applications. The coupled inductor can be implemented either by toroidal cores or EE cores.

a. EE core implementation

Kool Mu toroidal cores are very popular for the CCM boost PFC applications because they have distributed air gap, high saturation level, and low core loss. The Kool Mu E-cores are also available which could be used to implement the coupled inductors.

The coupled inductor implemented with EE cores can be explained in Figure 2.32. Two channels interleaving is assumed. Conventionally, the two inductors L_1 and L_2 are implemented with two Kool Mu toroidal cores. The air gap is distributed. The two inductors can also be implemented with U-cores without any performance change. The two pairs of U-cores can then be moved together and combined into a pair of E-cores. Since the air gap is distributed, the two inductors L_1 and L_2 are coupled with E-core implementation.

The lumped equivalent magnetic model is shown in Figure 2.33. By the definition of the inductor and the mutual inductor, the following equations can be obtained.

$$\begin{cases} L_{11}i_1 = n_1\phi_{11} \\ Mi_1 = n_2\phi_{12} \\ L_{lk}i_1 = n_1\phi_{lk} \end{cases} \tag{2-27}$$

According to the equivalent magnetic circuit model, the flux in each branch can be calculated,

$$\begin{cases} \phi_{11} = \dfrac{n_1 i_1}{R_1 + R_c // R_2} \\ \phi_{12} = \dfrac{n_1 i_1}{R_1 + R_c // R_2} \cdot \dfrac{R_c // R_2}{R_2} \\ \phi_{lk} = \dfrac{n_1 i_1}{R_1 + R_c // R_2} \cdot \dfrac{R_c // R_2}{R_c} \end{cases} \tag{2-28}$$

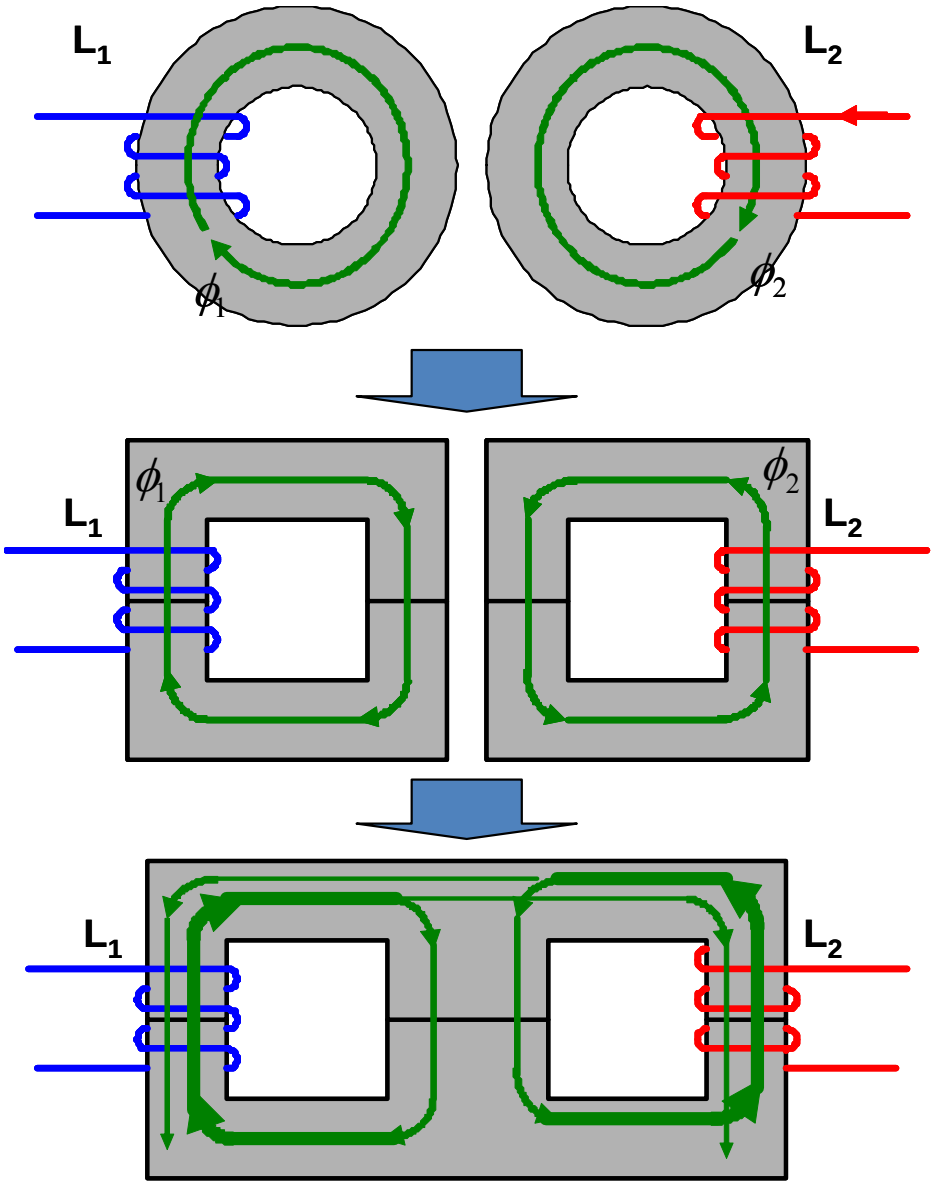


Figure 2.32. Coupled inductor with EE core implementation.

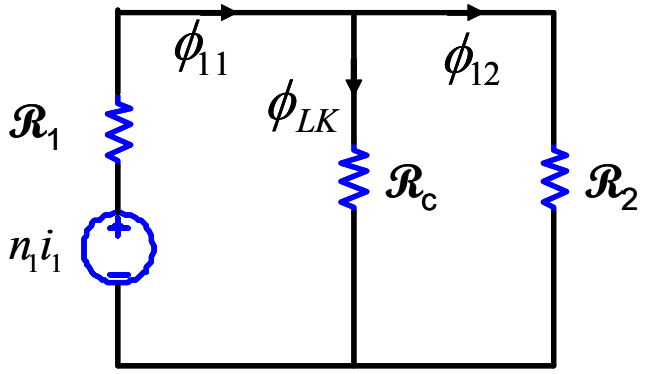


Figure 2.33. Lumped equivalent magnetic model of the coupled inductor with EE cores.

Based on the definition in (2-27) and the results in (2-28) the self inductance, mutual inductance, and the leakage inductance can be obtained in (2-29).

$$\begin{cases} L_{11} = \dfrac{n^2}{R_1 + R_c // R_2} \\ M = \dfrac{n^2}{R_1 + R_c // R_2} \cdot \dfrac{R_c // R_2}{R_2} \\ L_{lk} = \dfrac{n^2}{R_1 + R_c // R_2} \cdot \dfrac{R_c // R_2}{R_c} \end{cases} \tag{2-29}$$

Based on the definition, the coupling co-efficient of the EE core implementation can be calculated.

$$k = \frac{M}{\sqrt{L_{lk1} L_{lk2}}} = \frac{M}{L_{lk}} = \frac{R_c}{R_2} \tag{2-30}$$

Instead of counting on the magnetic reluctance from the distributed air gap, an air gap can be added in the center leg to control the R_c. Higher coupling co-efficient can be obtained by increasing the air gap in the center leg.

b. Toroidal core implementation

The coupled inductor can be implemented with toroidal cores by introducing one additional differential mode choke.

The equivalent circuit of the coupled inductor can be derived, as shown in Figure 2.34. It shows that the coupled inductor can be equivalent to two individual inductors plus one differential mode choke. The two individual inductors are the leakage inductors of the coupled inductor. According to the discussion about the non-linear inductance in the last section, the leakage inductance, L_{eq2}, will determine the input current peak-to-peak ripple.

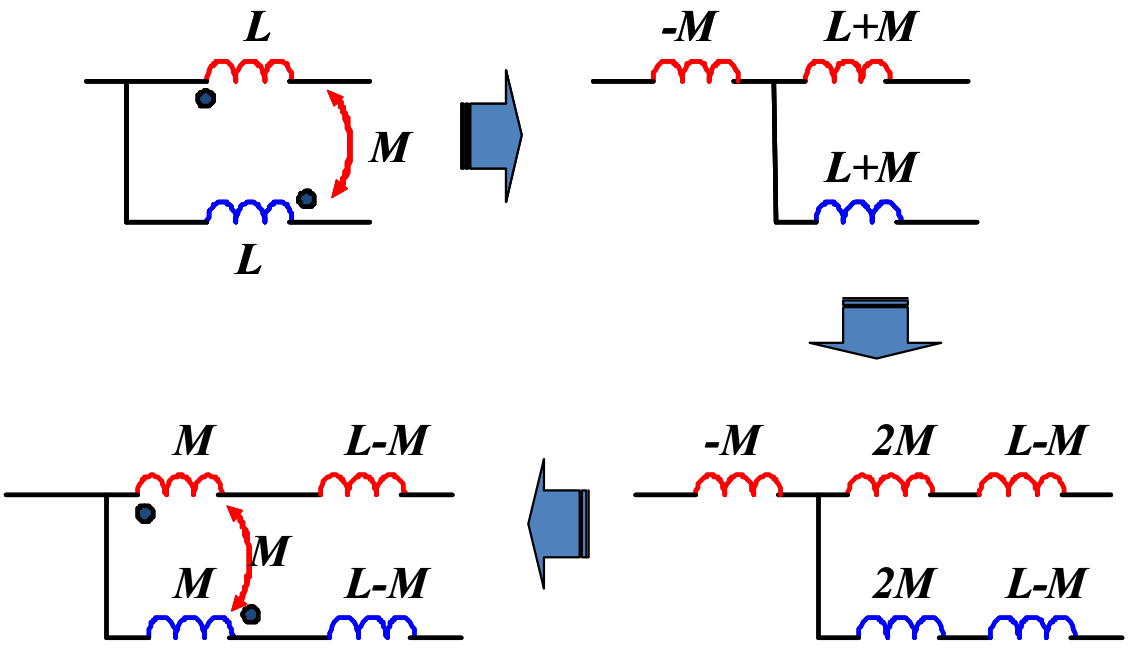


Figure 2.34. Derivation of the equivalent circuit for the coupled inductor.

The two leakage inductors and one differential mode inductor can be implemented with toroidal cores, but with quite different requirements. As shown in Figure 2.35, one winding is wound on the toroidal core; both the DC flux and the AC flux are in the core. However, for the differential mode inductor, there are two windings on the core. Assume two channels are identical; the currents in two windings have the same DC current and same peak-to-peak current ripple. Since the DC components have the same magnitude, but opposite direction, the DC components are cancelled each other. The AC components have the same magnitude but phase shifted 180º; the AC components are partial cancellation and frequency doubled.

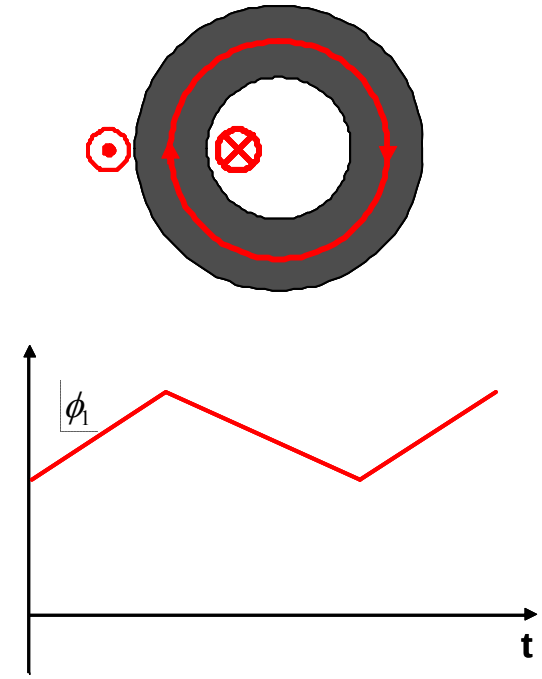


Figure 2.35. Leakage inductor implementation and the waveform of the flux in the core.

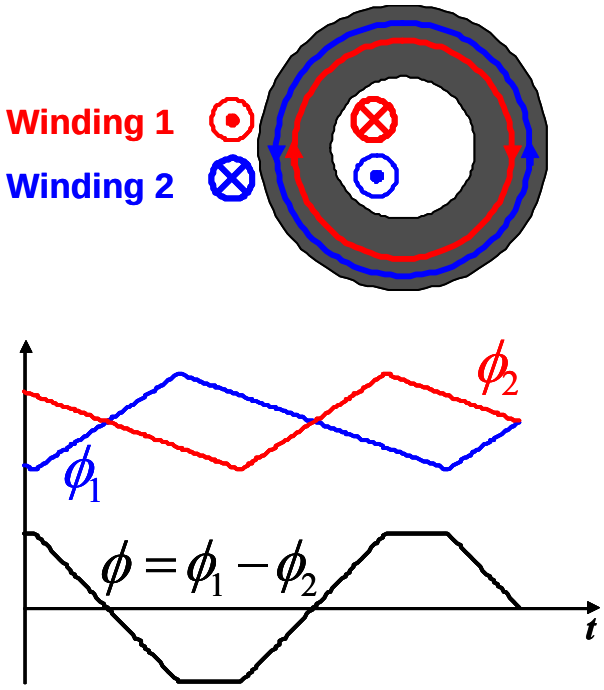


Figure 2.36. Differential mode choke implementation and the waveform of the flux in the core.

The leakage inductors and the differential mode inductor can be implemented with toroidal cores, but with different requirements. For the leakage inductor, the requirement is

very similar to conventional boost PFC inductors. The core size is normally determined by the energy storage requirement because of the DC bias flux in the core and relatively smaller AC flux. The core materials with high saturation flux density, such as MPP, High Flux, and Kool Mu, are preferred since smaller core size can be obtained. For the differential mode inductor, there is no DC bias flux in the core. The core is designed based on the applied volt-second. Core loss is the dominating factor for the core size. Materials with small core loss, such as Ferrite, are preferred for implementation. Choosing different core material to implement this coupled inductor can achieve optimized designed of the inductors.

A two-channel interleaved PFC prototype is used as one example for the coupled inductor size reduction. 600 W for each channel. The switching frequency is designed at 130 kHz. Two separate cases are implemented, the non-coupled inductor and the coupled inductor. For the non-coupled inductor, one Kool Mu toroidal core 77083-A3 is used with 64 turns of the winding for each channel, as shown in Figure 2.37. For the coupled inductor case, the leakage inductor is implemented with two 77059-A3 with 32 turns. The differential mode choke is implemented with Ferrite toroidal core, ZJ-42908TC, with 53 turns. By introducing the coupled inductor, 48% volume reduction on inductor can be achieved.

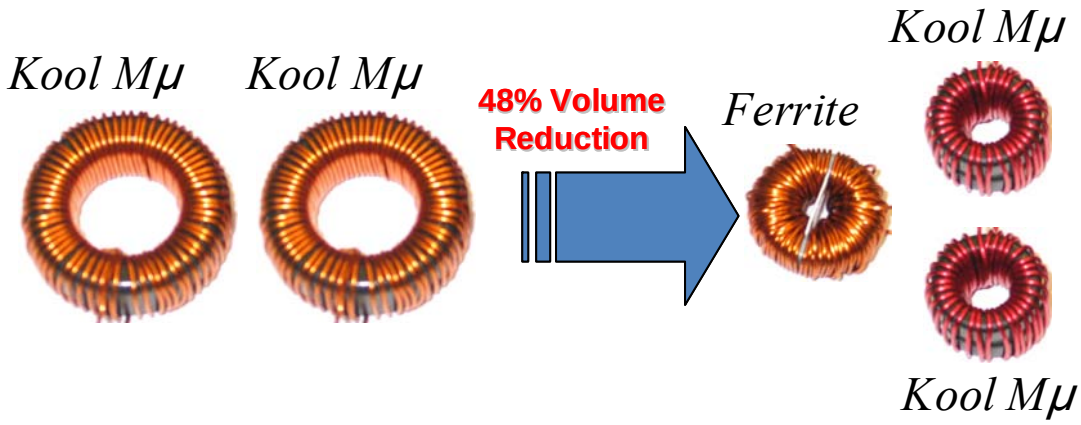


Figure 2.37. Coupled inductor size reduction.

With the designed inductors in the two-channel interleaved PFC prototype. The input and inductor current waveforms of the non-coupled case are shown in Figure 2.38. The

inductor peak-to-peak current ripple is 2.6 A. The input peak-to-peak current ripple is 1.5 A due to the ripple cancellation.

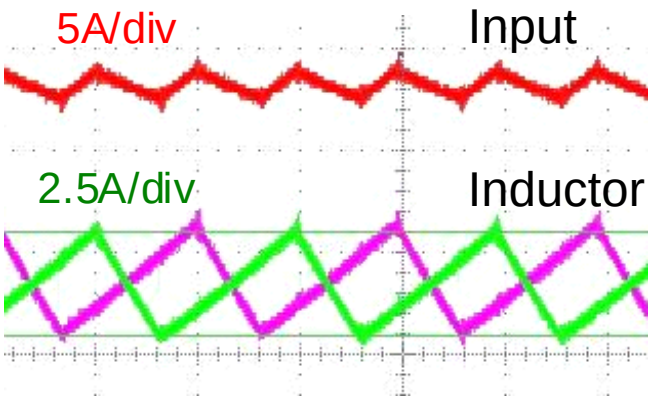


Figure 2.38. Input and inductor current waveforms for non-coupled case.

With the designed coupled inductor in the two-channel interleaved PFC prototype. The input and inductor current waveforms are shown in Figure 2.39. The inductor peak-to-peak current ripple is 1.7 A. The input peak-to-peak current ripple is 3.3 A.

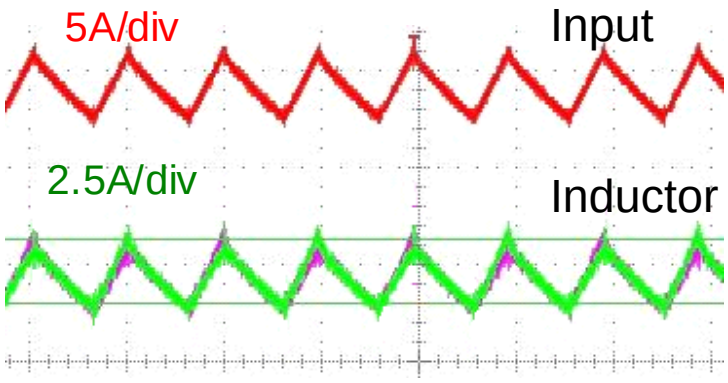


Figure 2.39. Input and inductor current waveforms for coupled inductor case.

For the coupled inductor case, although the two leakage inductor is much smaller than the non-coupled case, the inductor current ripple still can be 35% smaller. However, the input current ripple magnitude is about 2.2 times larger than the non-coupled case. The higher input current ripple will result in higher DM noise, 6.8 dB higher in this case. Larger DM filter size is expected. However, when the inductor size dominating, the total size could be reduced. To identify the benefit of the coupled inductor on the total DM filter

and the inductor size reduction, the total inductor weight trend of two channel interleaving is plotted and compared.

The inductor design procedure discussed in [55] is adopted to plot the inductor weight trend. The Kool Mu power core material is used in the design. The temperature rise has been always limited to less than 55ºC. Figure 2.40 shows the amount of magnetic core material (Kool Mu power core) and the copper material needed for implementing the boost inductor and the DM filter for the non-coupled two-channel interleaved.

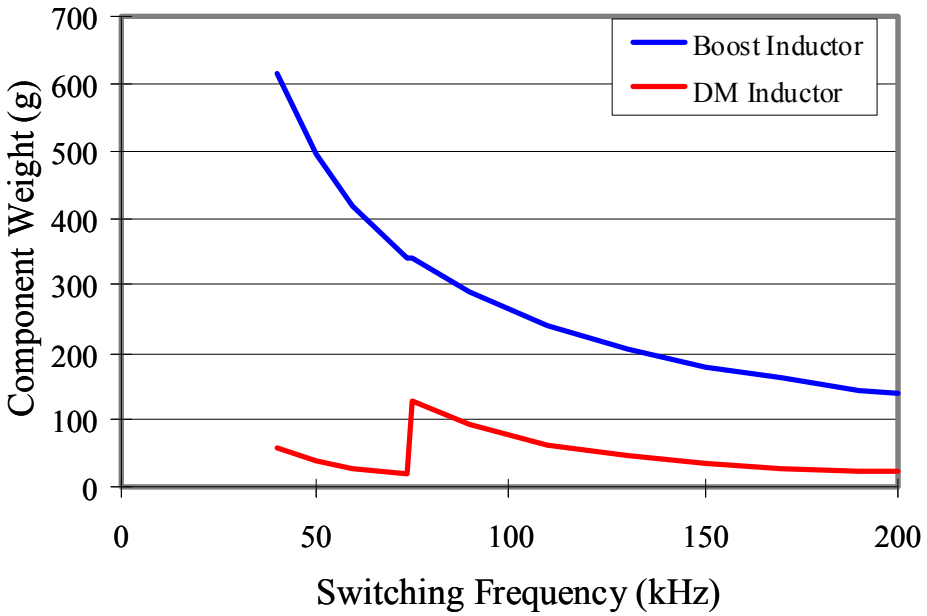


Figure 2.40. Magnetic component weight trend for two-channel interleaved PFC.

Figure 2.41 shows the amount of magnetic core material (Kool Mu power core) and the copper material needed for implementing the boost inductor and the DM filter for the coupled two-channel interleaved PFC with high coupling co-efficient. The total inductor material weight is reduced by introducing the coupling between the two channels. The total material weight for DM filter is increased due to the ripple magnitude increase caused by coupling between the two channels.

Figure 2.42 shows the total material weight needed for implementing the boost inductor and the DM filter for non-coupled and coupled two-channel interleaved PFC. The total material weight can be reduced by introducing coupling. The reduction is more significant when the boost inductor size is large.

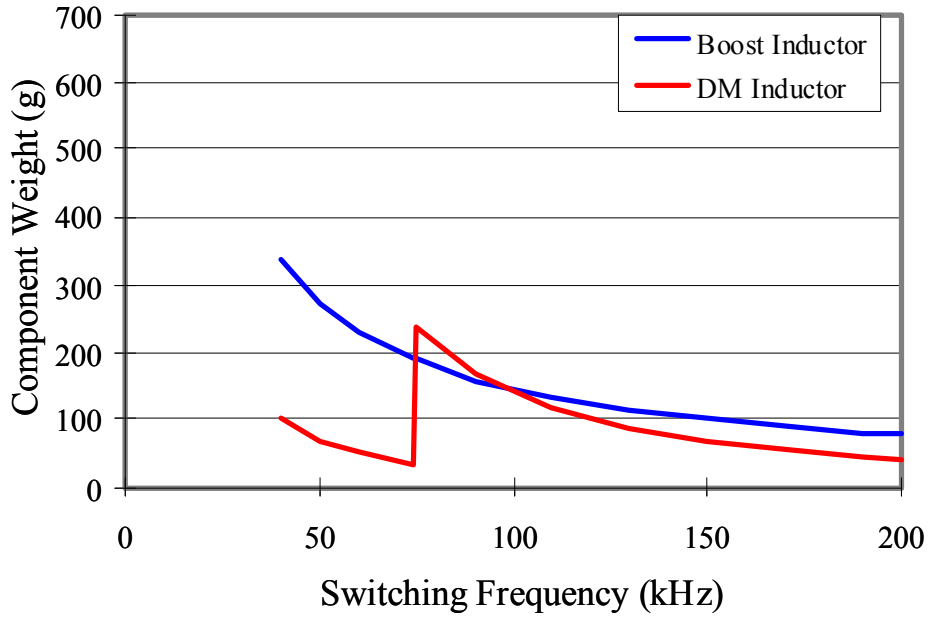


Figure 2.41. Magnetic component weight trend for coupled two-channel interleaved PFC.

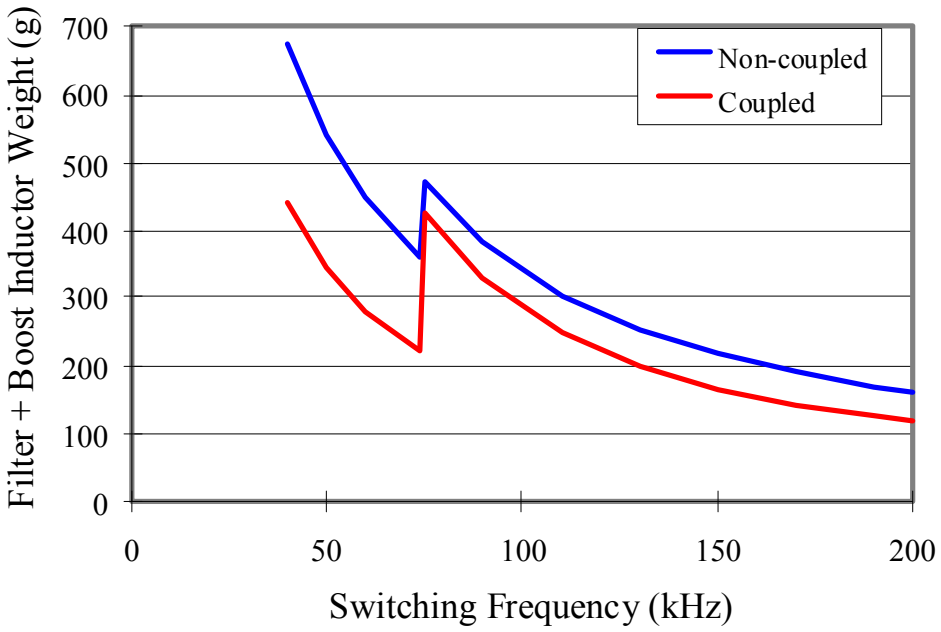


Figure 2.42. Total material weight comparison for two-channel interleaved PFC.

2.5 Harmonic Analysis for Boost Converter

Switching power converters are not easy to analyze due to the non-linearity of the switching networks. It is normally analyzed by dividing switching period into several sections. In these sections, the equations are derived based on different equivalent circuits. This method is straightforward and intuitive. However, some of the results are hard to relate to physical meanings, such as the L_{eq1} and L_{eq3} in the coupled inductor analysis.

Harmonic analysis is the branch of mathematics that studies the representation of functions or signals as the superposition of basic waves. It investigates and generalizes the notions of Fourier series and Fourier transforms. The basic waves are called "harmonics". Harmonic analysis can be applied to switching converters for ripple analysis. Using boost converter as an example, the converter circuit diagram is shown in Figure 2.43. In CCM operation, since the MOSFET drain-to-source voltage can be considered as a square wave, the circuit can be simplified for ripple analysis, as shown in Figure 2.44.

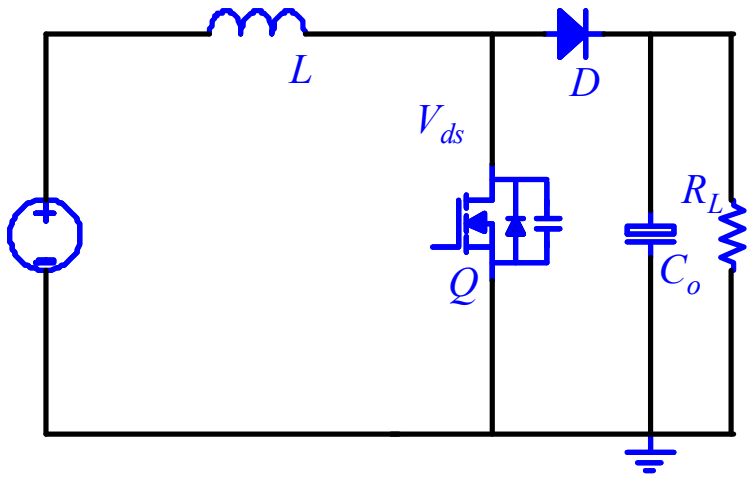


Figure 2.43. Boost converter circuit diagram.

The drain-to-source voltage can be further decomposed into DC component and all the switching frequency harmonics by using the Fourier series.

$$v_{ds}(t) = dV_o + \frac{2V_o}{\pi}\sum_{n=1}^{\infty}\frac{\sin(nd\pi)}{n}\cos(n\omega_s t) \tag{2-31}$$

Where d is the duty cycle of the drain-to-source voltage. V_o is the output voltage. n is the order of the harmonics. At steady state the DC component will be equal to the input voltage V_{in}. For the ripple current analysis, the DC components in the equivalent circuit can be ignored since they have no impact to the current ripple at steady state. The circuit can be further simplified, as shown in Figure 2.45.

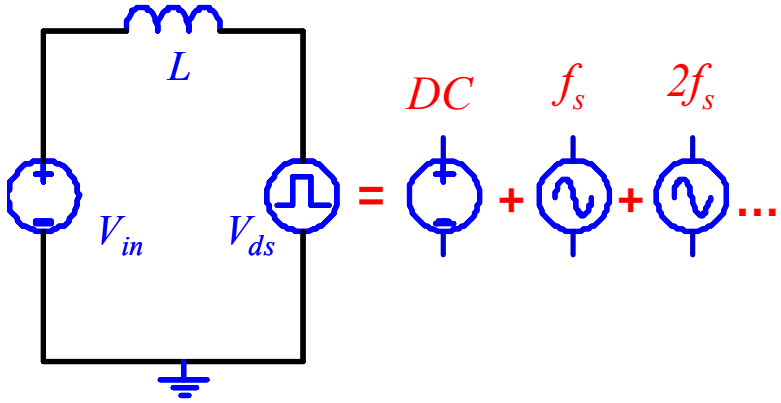


Figure 2.44. Equivalent circuit with DC component.

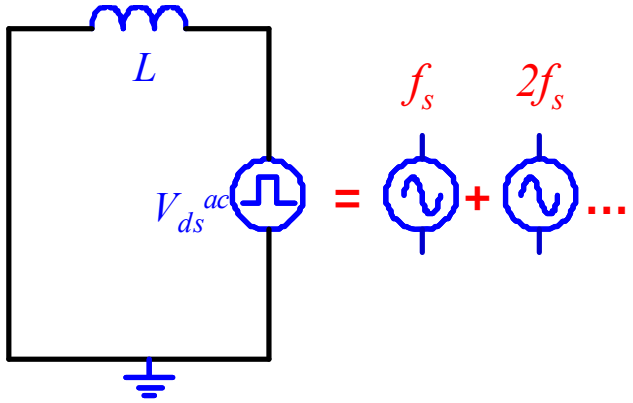


Figure 2.45. Equivalent circuit without DC component.

The equivalent circuit shown in Figure 2.45 is now a linear circuit. All the theories and analysis methods for the linear circuit can be applied. The inductor current ripple can be calculated by calculating each switching frequency harmonics, and add them together. The triangular current ripple waveform is obtained, as shown in Figure 2.46. When duty cycle changes, the current ripple changes accordingly since the harmonics magnitude of the square wave voltage source changes.

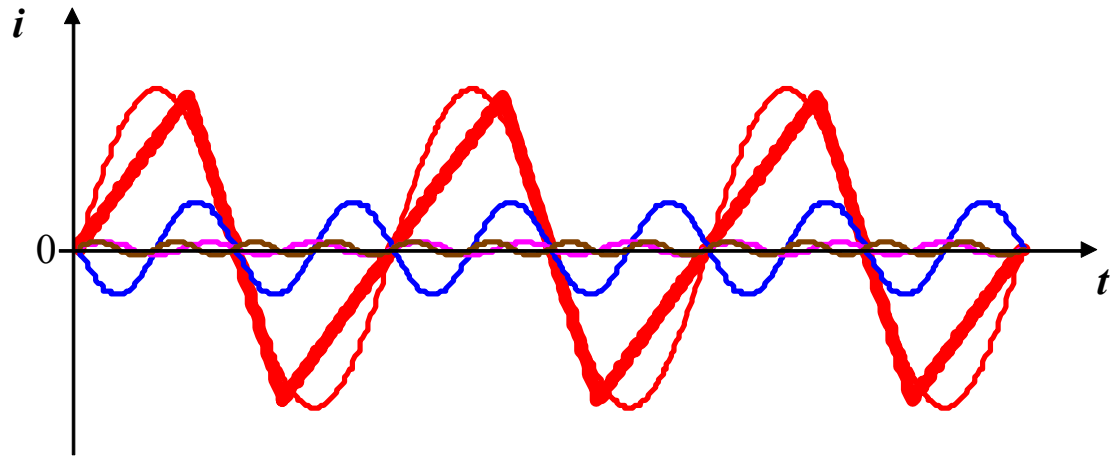


Figure 2.46. Inductor current ripple and harmonics.

a. Interleaved boost converters

The harmonic analysis can be used for interleaved boost converters. The equivalent circuit for current ripple analysis of two-channel interleaved boost converter is shown in Figure 2.47.

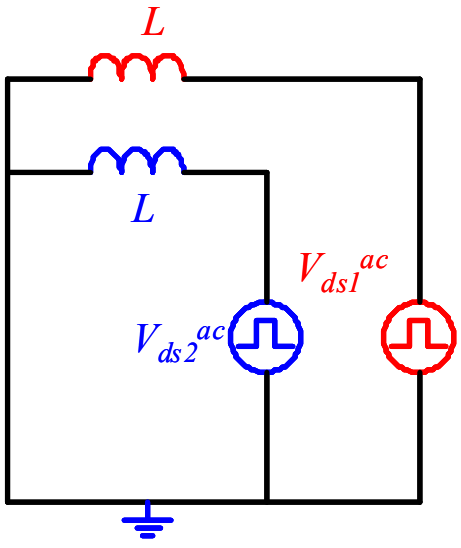


Figure 2.47. Equivalent circuit for 2-channel interleaved boost converter.

Since the switching action of two identical channels are shifted 180 degrees, all the odd order harmonics are out of phase, and all the even order harmonics are in phase.

Calculating the inductor and input current harmonics, the input and inductor current ripple can be obtained. Since all the odd order harmonics of two channels are out of phase, they are cancelled at the input terminal. On the other hand, since the even order harmonics are in phase, they add together at the input terminal. The input current ripple frequency is doubled because it only contains the even order harmonics. The input current ripple magnitude is reduced because the first order harmonic is cancelled which has the largest magnitude. However, interleaving has no impact on the inductor current ripple since the entire inductor current ripple harmonics are the same for both interleaving and non-interleaving cases.

Another special case is the input current ripple is totally cancelled when the duty cycle is equal to 0.5. From the harmonic analysis point of view, this is only because there is no even order harmonics exist in the voltage source. Since the even order harmonics are the only components at the input side, the ripple current is zero when all the even order harmonics are zero.

This harmonic analysis can be extended to interleaved converters with more channels.

b. Interleaved boost converters with inversed coupled inductor

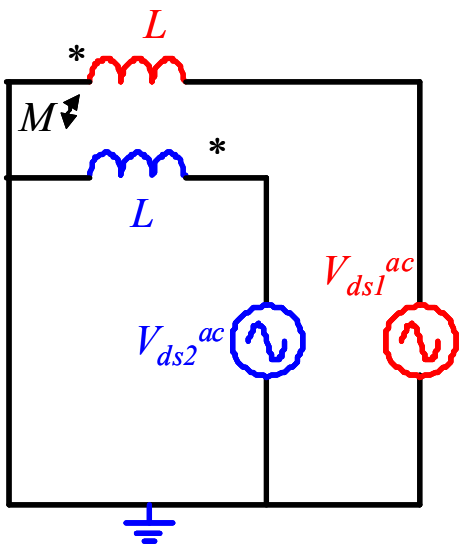


Figure 2.48. Equivalent circuit for 2-channel interleaved boost converter with inverse coupled inductor.

The harmonic analysis can be further extended to interleaved boost converters with coupled inductors. The equivalent circuit for current ripple analysis of two-channel interleaved boost converter with inversed coupled inductor is shown in Figure 2.48.

The inductor current ripple for the odd order harmonics and even order harmonics becomes different due to the introducing of inverse coupling. The equivalent circuit for the odd order harmonics with inverse coupled inductor is shown in Figure 2.49. Due to the phase relationship of the odd order harmonics in the two channels, the impedance between the two channels is increased by mutual inductance. The larger the mutual inductance, which is the higher coupling coefficient case, the larger the impedance is. The impedance could be so high that the odd order harmonics of current ripple can be strongly suppressed between the two channels.

Same as the non-coupled case, the odd order harmonics only exist or circulating between the channels. There is no odd order harmonics at the interleaved boost converter input terminal. The coupling coefficient will not impact the input current ripple waveform.

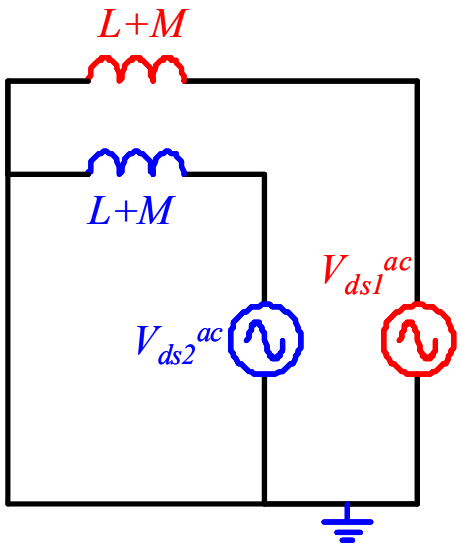


Figure 2.49. Equivalent circuit for odd order harmonics with inverse coupled inductor.

The equivalent circuit for the even order harmonics with inverse coupled inductor is shown in Figure 2.50. Due to the phase relationship of the even order harmonics in the two channels, the impedance between the two channels is purely the leakage inductance of the coupled inductor. Since the even order current ripple harmonics are the only components

exist at the input side, the input current ripple is only determined by the leakage of the coupled inductor. This matches with the conclusion drawn in non-linear inductor analysis, which claims the input current ripple is determined by L_{eq2}.

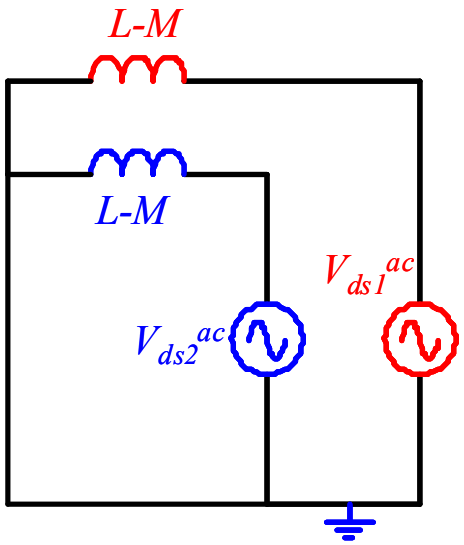


Figure 2.50. Equivalent circuit for even order harmonics with inverse coupled inductor.

Based on the harmonic analysis for the interleaved boost converters with inversed coupled inductor, the input current ripple will always keep the same as long as the leakage inductance of the coupled inductor are the same. Once the leakage inductance is fixed, the even order current ripple harmonics for the inductor and the input are fixed. Coupling coefficient will only impact the odd order inductor current ripple harmonics. The higher the coupling coefficient, the smaller the odd order harmonics are, which results in smaller inductor current ripple. In another word, coupling of the inductor introduced a mechanism to adjust the ratio between the odd order harmonics and the even order harmonics of the inductor current ripple.

The harmonic analysis can be further extended to coupled inductors with more channels with different phase shift angles. It also can be used for analyzing direct coupled inductors.

2.6 Roadmap for Multi-Channel PFC with Coupled Inductor

Most of today's PFCs are designed according to the single channel PFC knowledge base. With the multi-channel interleaving and coupled inductor techniques, the design philosophy could have a dramatic change. It is the intension of this section to plot out the benefits of applying interleaving and coupled inductor with more channels.

Using the same inductor weight trend estimation discussed in the previous chapter, the boost inductor and DM inductor weight for interleaved PFC can be plotted, as shown in Figure 2.51. In accordance with the benchmark PFC design, 1.2 kW total power is assumed for different channel number designs. Single-channel, 2-channel, 4-channel, and 8-channel designs are plotted in Figure 2.51. With the assumption of same inductor current ripple percentage, the total boost inductor weight of different designs are the same since interleaving has no impact on inductor ripples.

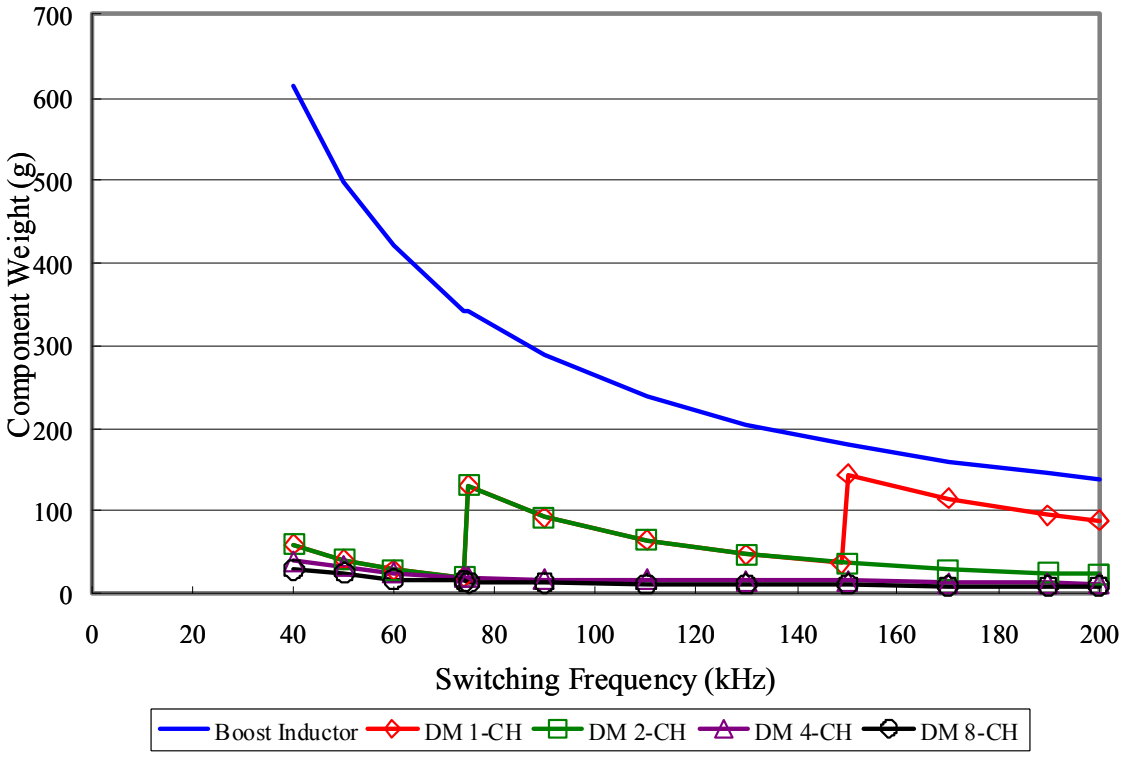


Figure 2.51. Magnetic component weight trend for multi-channel interleaved PFC.

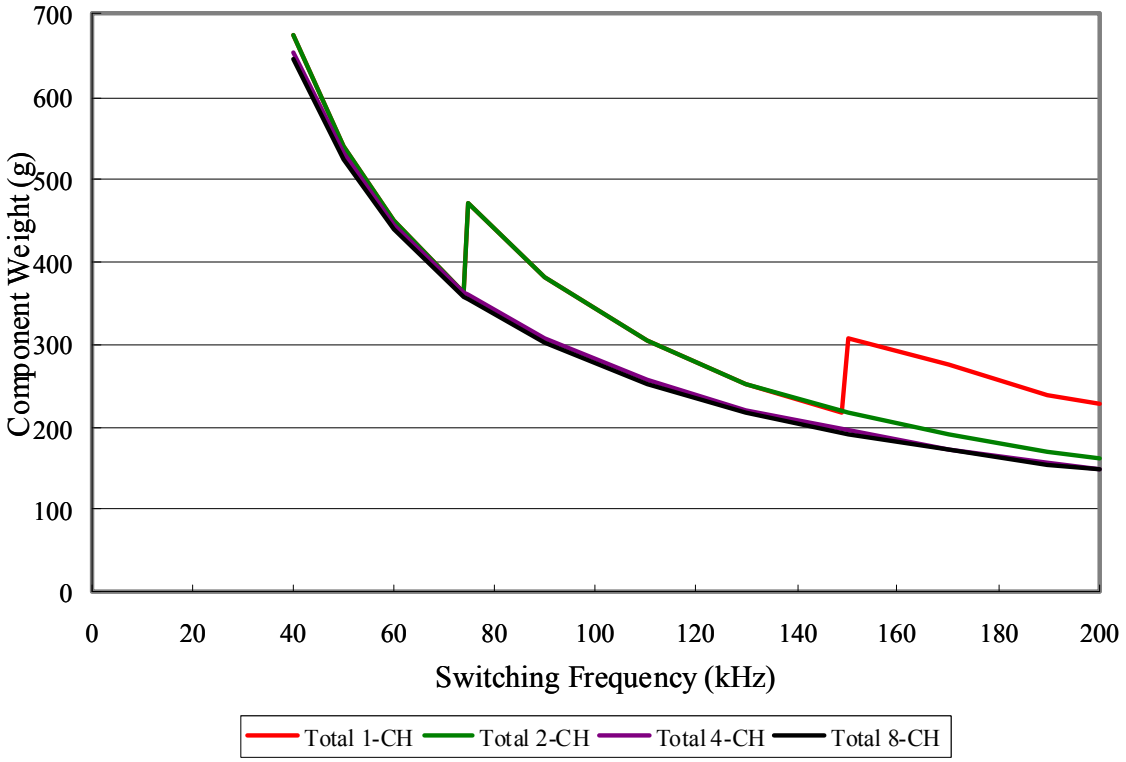


Figure 2.52. Total material weight comparison for multi-channel interleaved PFC.

The total magnetic component material weight of single-channel, 2-channel, 4-channel, and 8-channel interleaved PFCs is shown in Figure 2.52. Although the DM inductor weight can be reduced by interleaving, to have a PFC design with good power density, the switching design is still at 100 kHz range since the inductor size will dominate the total magnetic components size.

With the inverse coupled inductor, the boost inductor weight can be reduced. As shown in Figure 2.53, the boost inductor weight of single-channel, 2-channel, 4-channel, and 8-channel PFC designs with coupled inductor are plotted. With more channel interleaving, the inductor weight is reduced. The weight reduction is more pronounced at lower switching frequency range.

The total magnetic components material weight for the single-channel, 2-channel, 4-channel, and 8-channel are plotted in Figure 2.54. With the boost inductor weight reduction from coupling and the DM inductor weight reduction from interleaving, the switching frequency design trade-off become very different to the conventional single-

channel PFC design. With more channels interleaving, the zigzag shape of the curve changed into a simple curve. Total magnetic component weight at lower switching frequency range is greatly reduced. A good switching frequency trade-off between the power density and the efficiency can be found at much lower switching frequencies with more channels interleaving and coupling. Since high efficiency is becoming more and more important these days, the multi-channel coupled inductor PFC with low switching frequency design could be a promising candidate to achieve high efficiency goals without compromise the power densities. With lower switching frequencies, the PFC can also easily achieve better light load efficiencies which is also one of the very desirable features of today's PFC design.

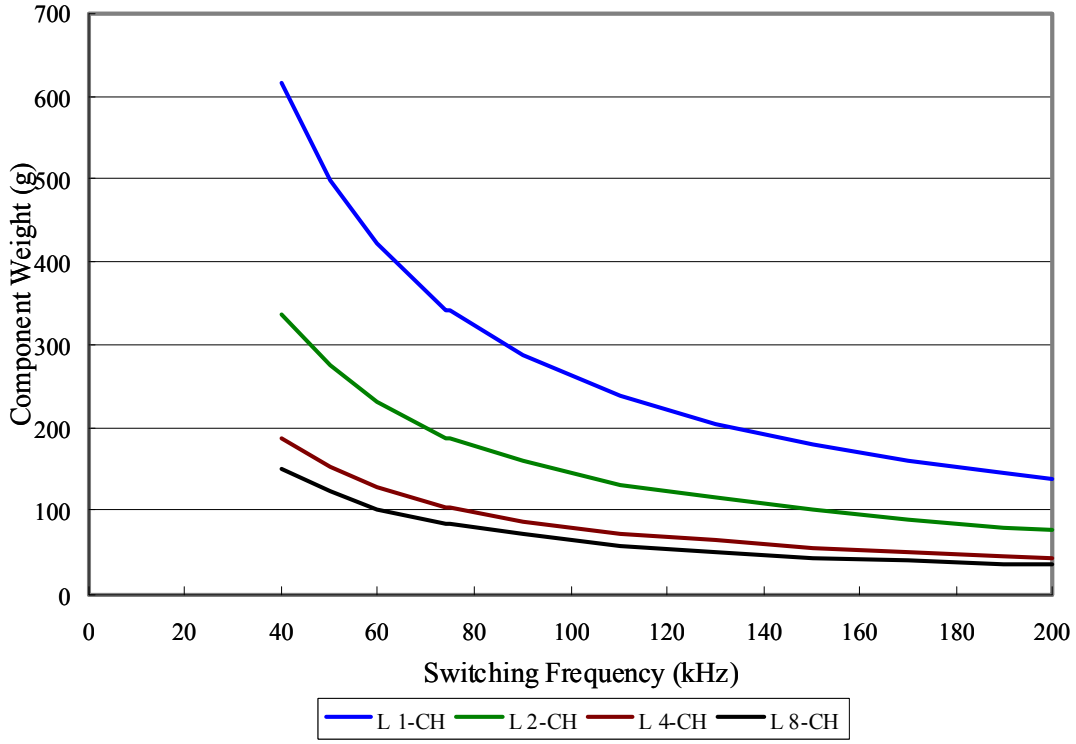


Figure 2.53. Boost inductor weight trend for multi-channel interleaved PFC with coupled inductor.

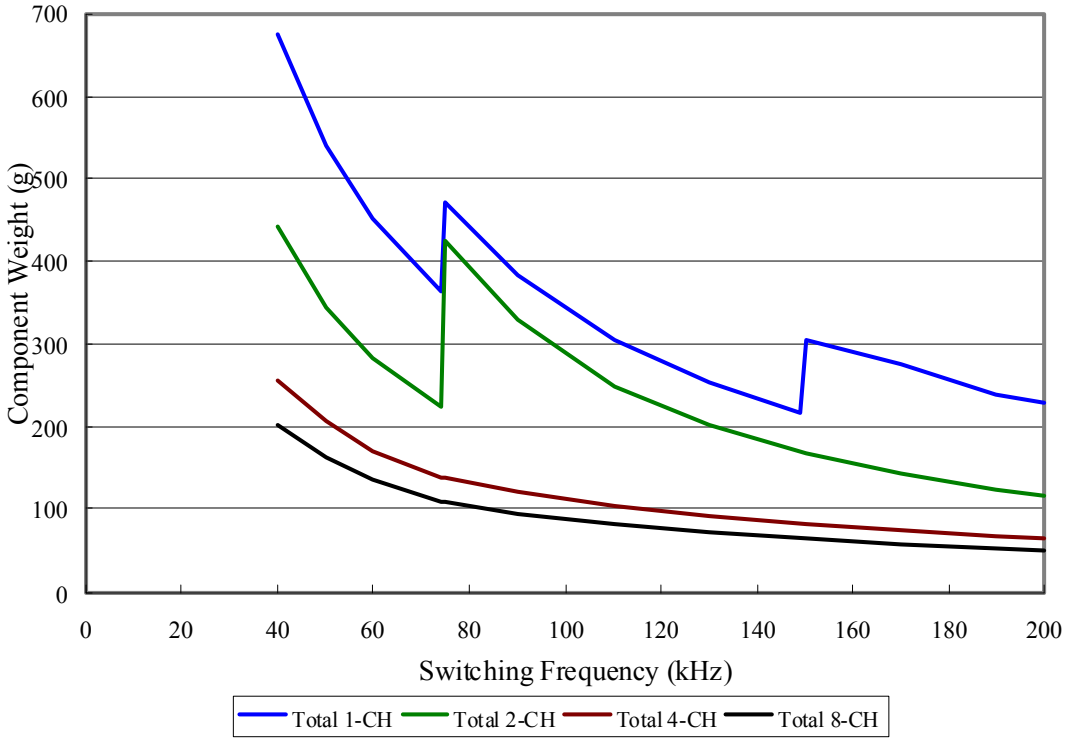


Figure 2.54. Total material weight comparison for multi-channel interleaved PFC with coupled inductor.

2.7 Summary

CCM boost PFC is the most popular topology for the high power application because of its continuous input current and simplicity. With the fast growing information technologies, the single-channel boost PFC design is facing extremely tough challenges due to the continuously increasing power density and efficiency requirement. In addition to that, power scalability is another very desirable feature in today's PFC design in order to meet different server power requirements. Lots of techniques has been studied and proposed during the last several years. Among these techniques, multi-channel interleaving is a quite promising one. By staggering the channels at uniform intervals, multi-channel interleaved PFC can reduce the EMI filter size due to the ripple cancellation effect.

The existing studies about the interleaving impact on the EMI filter design are based on the time domain ripple cancellation effective. However, both the EMI standard and the EMI measurement are based on the frequency domain spectrum. It is difficult to provide a

clear picture about how exactly the multi-channel interleaving will impact the EMI filter design. Limited by the analysis approaches, the interleaving impact on the Common Mode (CM) noise also has not been studied in any existing literatures. In this chapter, the frequency domain analysis method was adopted. With the double Fourier integral transformation, a closed-form expression of all the harmonics of the noise source can be obtained. With all the detail phase relationship of the switching frequency harmonics and all the side band harmonics, the multi-channel interleaving impact on both the DM and CM filter design is investigated. According to the design curve provided, the EMI filter size can be effectively reduced by properly choosing the interleaving channel number and the switching frequency.

The lifetime of the electrolytic capacitor at the PFC output is also a design concern since it is normally the first component in the power supply to fail. The capacitor lifetime can be lengthened by interleaving due to the ripple cancellation effective at the PFC output side. The multi-channel interleaving impact on the output capacitor current ripple is studied and summarized in this chapter.

It should be pointed out that interleaving only reduces the total input and output current ripple; the inductor current in each channel still has large ripple if small inductance are used. Similar to the multi-phase buck converter, coupling inductors have different equivalent inductances for input current ripple and inductor current ripple. Keeping the inductor current ripple magnitude same, inverse coupling inductors between the interleaved channels can reduce the inductor size. However, the DM filter size is increased due to larger input current. Based on the investigation on the total magnetic component weight, inverse coupling inductor can reduce the total magnetic component weight. The reduction is more pronounced for lower switching frequency design when the inductor size is dominating among the total magnetic components.

Chapter 3. Phase Angle Controlled Multi-Channel PFC

3.1 Introduction

Interleaved buck converter and interleaved boost converter are in dual in a lot of aspects. The features existed at the output side of the interleaved buck also can be found at the input side of the interleaved boost converter. Although the interleaving impact on the circuits is exactly the same, the converter design could be different for different applications since the requirements could be different.

For the VR application, there is a stringent requirement at the output side. There is only a small window for the output voltage variation with very fast load transient requirement. Huge output filter capacitor and decoupling capacitors are needed to meet the specified output voltage requirement for the single-phase buck converter. To reduce the VR output capacitance, high inductor current slew rates are preferred. With smaller inductance, larger inductor slew rate can be obtained. On the other hand, small inductances result in large steady-state voltage ripple at the output. The steady-state voltage ripples can be so large that they are comparable to transient voltage spikes [16]. The interleaved multi-phase buck converter can greatly reduce the steady-state output voltage ripple magnitude, making it possible to use very small inductances to improve the transient response.

For the PFC application, there is also a stringent requirement at the input side. The input current ripple needs to be small enough to meet the EMI standard, as shown in Figure 3.1. FCC Part 15 Class A/B and EN 55022 Class A/B are used as examples. The interleaved multi-channel boost converter can greatly reduce the input current ripple and benefit the EMI filter design.

Comparing the output requirement of the VR application and input requirement of the PFC application, it can be found that the VR input requirement is defined in the time domain while the PFC output requirement is defined in the frequency domain. Since the requirement is different, the interleaving design consideration also could be different. In

this chapter, different interleaving strategy for multi-channel PFC is investigated considering the EMI requirement for this AC-DC application.

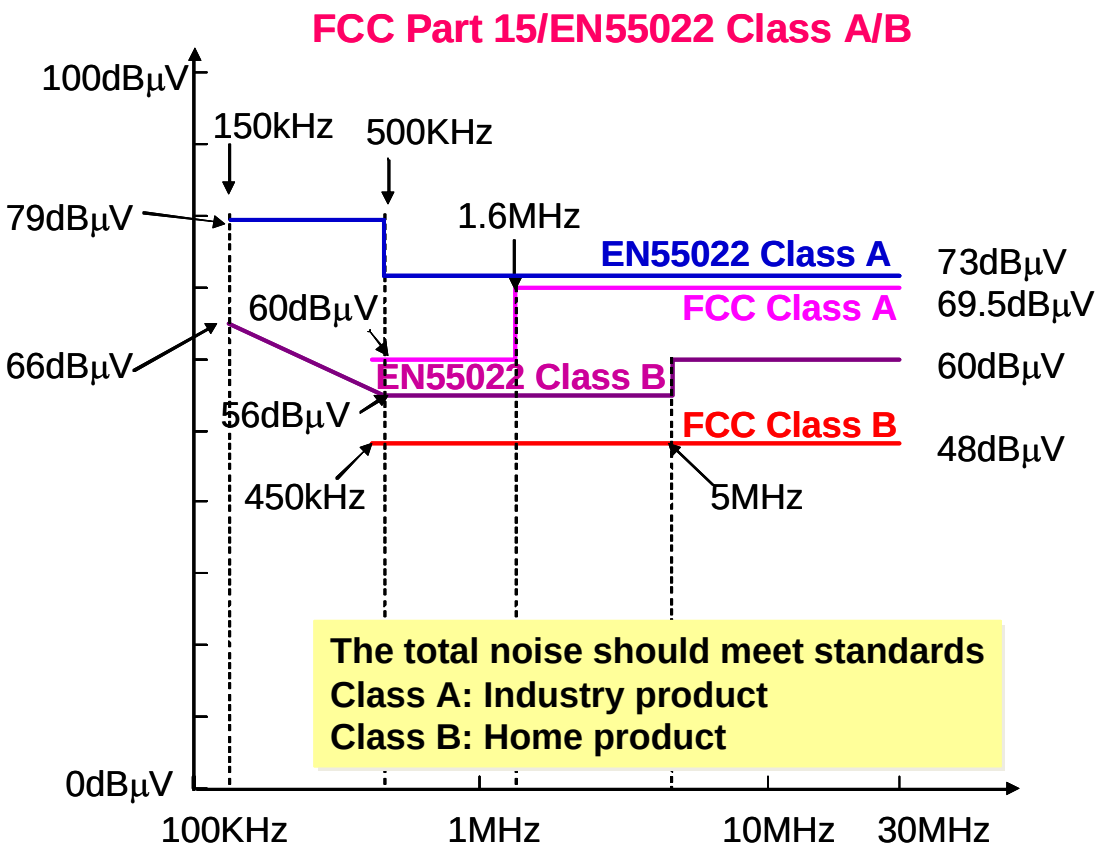


Figure 3.1. EMI requirement of FCC Part 15 Class A/B and EN 55022 Class A/B Standards. [53][56]

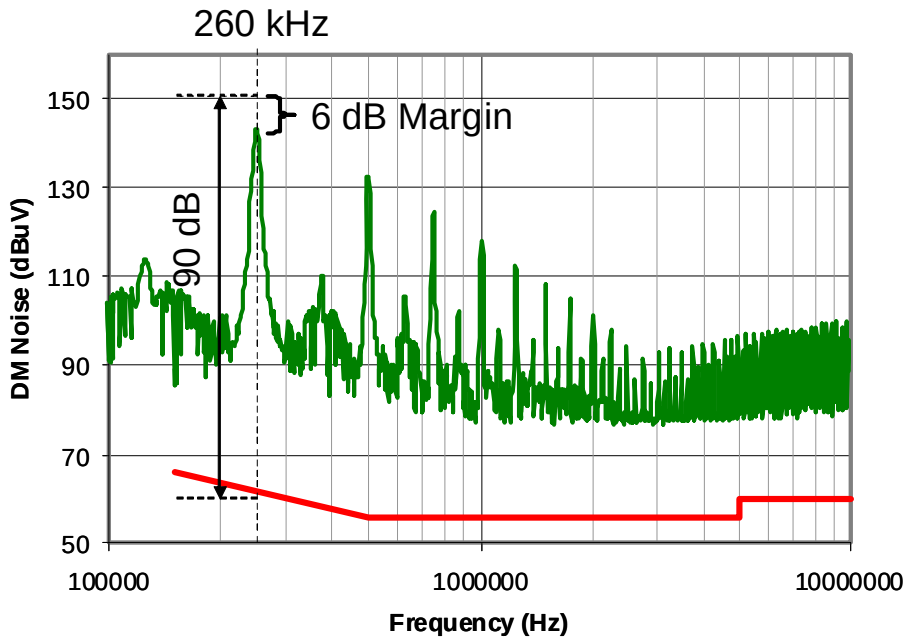
3.2 Proposed Phase Angle Control for Multi-Channel PFC

As discussed in the previous chapter, for multi-channel interleaved PFC, some switching frequency ranges will provide a benefit in allowing reduction of EMI filter size, while others will not; thus constituting a significant limitation on the use of interleaved multi-channel PFCs to provide a benefit in reducing size and cost of EMI filter design. Generally, *360°/m*, the symmetrical interleaving in a multi-channel PFC circuit running at different frequencies can only cancel the certain order harmonics and will always have no

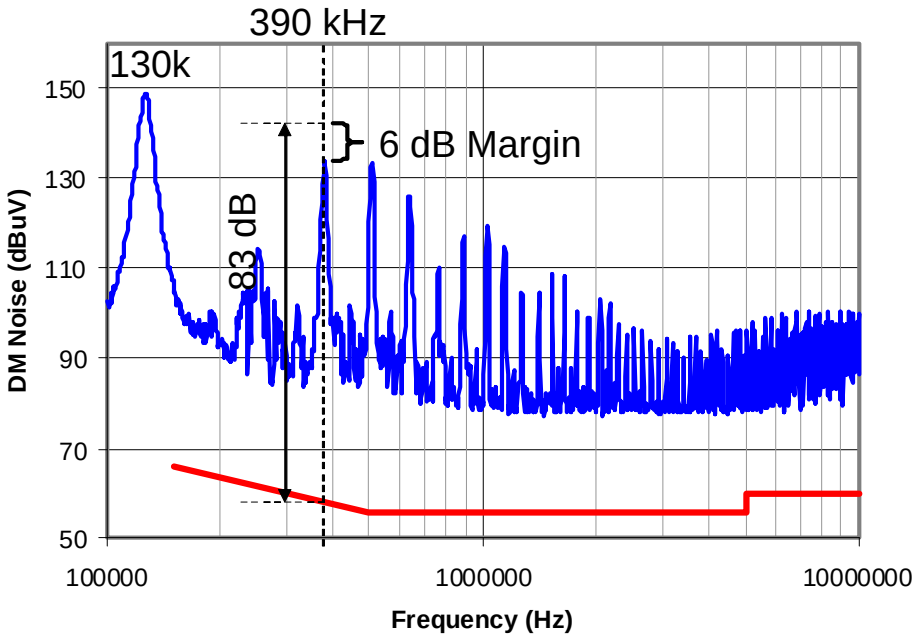
impact on the other harmonics. When the EMI filter is designed based on these un-impacted EMI noise, there will be no filter size reduction for that design.

75 kHz ~ 150 kHz is a quite popular switching frequency range for PFC circuit used by today's industry products. Paralleling two MOSFETs to handle the large current is a common practice for a kilo watt power rating PFC, so it is very likely to take this 2-channel interleaving PFC solution running in this popular switching frequency range. Unfortunately, by using the conventional interleaving scheme, there will be no benefit on the EMI filter at all. However, in accordance with the basic principles of harmonics cancellation analysis, other phase shift angles between the PFC channels can provide cancellation or partial cancellation effects can provide benefits in regards to EMI filter design for reduction of size and cost. In this switching frequency range, a two-channel PFC operating with a 90º or 270º phase shift can cancel the second order harmonic and reduce the third order harmonic, allowing the EMI filter to be designed based on the reduced third order harmonic noise; so that the filter size can be substantially reduced.

With the proposed 90º phase shift for 2-channel PFC, the fundamental frequency component noise sources have 90º phase shift, so the noise magnitude will be reduced 3dB. For the 2^{nd} order harmonic, the noise sources are out of phase, so it gets cancelled. For the 3^{rd} order harmonic, the noise sources has 270º phase shift, so again the magnitude will be reduced 3dB. For the 4^{th} order harmonic, the noise sources are in phase, so they add together. The 4^{th} order will keep the same magnitude as the non-interleaved PFC. The higher order harmonics will repeat in this pattern. In summary, all the odd order harmonics reduced 3 dB; the 2^{nd}, 6^{th}, 10^{th}, 14^{th}… order harmonics get cancelled; no impact on the 4^{th}, 8^{th}, 12^{th}… order harmonic.



(a) 2-channel interleaved PFC DM noise (phase shift *180°*)



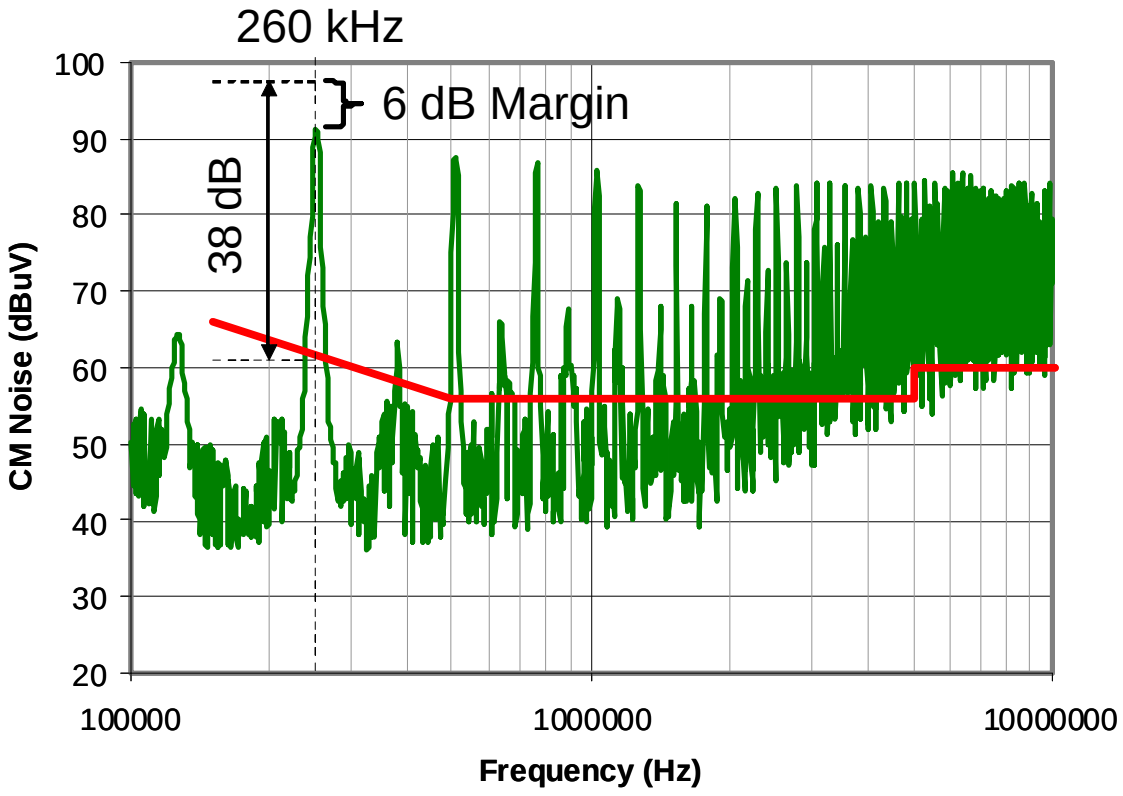
(b) 2-channel interleaved PFC DM noise (phase shift *90°*)

Figure 3.2. Measured DM noise of 2-channel PFC with different phase angle.

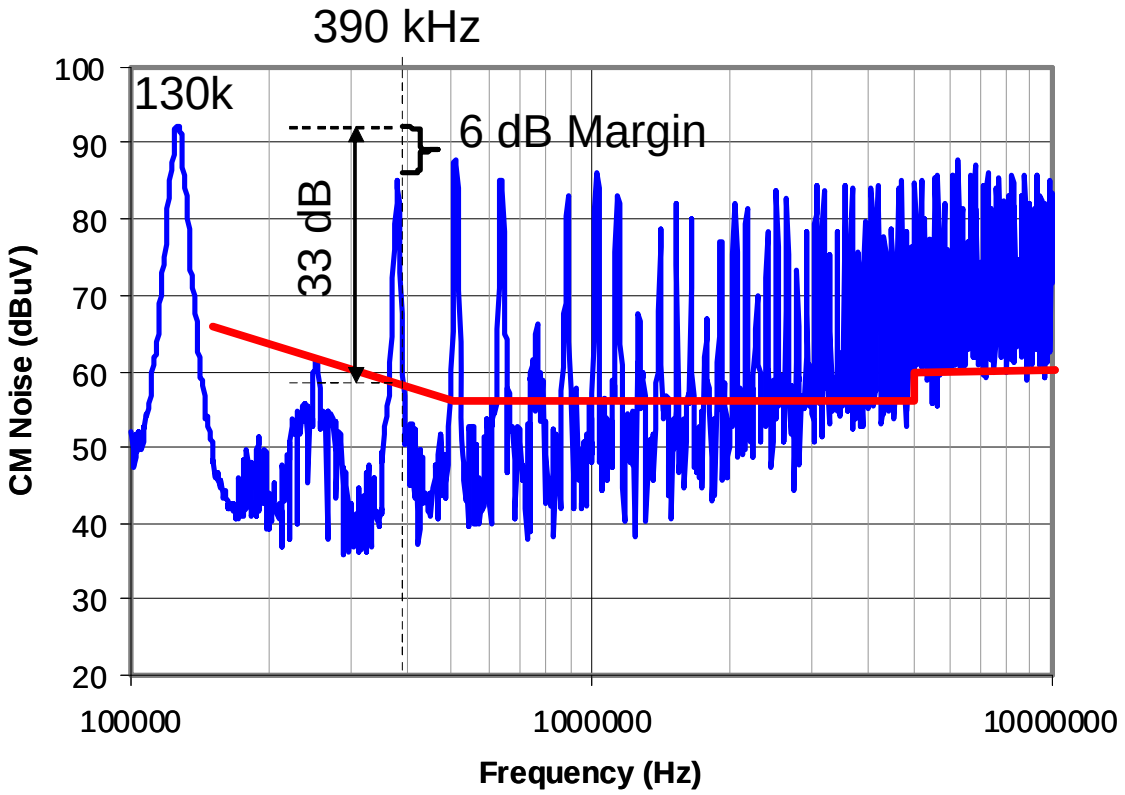
This 90º phase shift 2-channel interleaving scheme is experimentally verified on a 2-channel PFC prototype. The measured DM noise for two-channel PFC is illustrated in Figure 3.2 (a) and (b).

For the DM noise, the 2nd order harmonic gets cancelled. The 3rd order harmonic reduced 3 dB, which is 10 dBuV lower than the original 2nd order harmonic. For the 2-channel PFC with 90º phase shift, the DM filter is designed based on the higher frequency noise with smaller magnitude, so the DM filter size will be smaller.

For the CM noise, the noise cancellation phenomenon is the same. The 2nd order harmonic also gets cancelled. The 3rd order harmonic reduced 3dB. The CM filter also can be reduced, as shown in Figure 3.3 (a) and (b).



(a) 2-channel interleaved PFC CM noise (phase shift *180º*)



(b) 2-channel interleaved PFC CM noise (phase shift *90º*)

Figure 3.3. Measured CM noise of 2-channel PFC with different phase angle.

The DM filter corner frequency for non-interleaving (1-Channel), conventional interleaving (2-Channel phase shift 180º) and the proposed 90º phase shift are summarized and compared in Figure 3.4. Using the proposed 90º phase shift scheme, the EMI filter corner frequency can be greatly improved. For a 2-channel PFC with 90º phase shift, each channel running at 130 kHz switching frequency, the EMI filter size is equivalent to a conventional 2-channel interleaving PFC with 250 kHz switching frequency, and is equivalent to a single channel PFC with more than 600 kHz switching frequency.

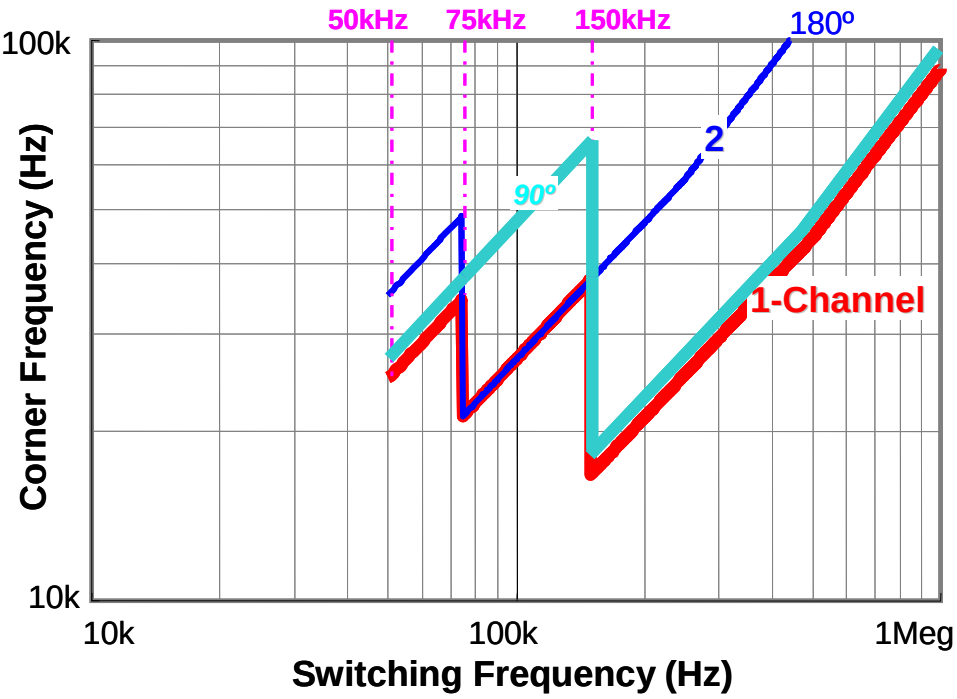


Figure 3.4. Relationship between the filter corner frequency and the switching frequency (DM Filter) for single channel, conventional 2-channel interleaving and 2-channel with *90º* phase shift

3.3 Performance Evaluation of Phase Angle Controlled Multi-Channel PFC

3.3.1 EMI filter evaluation

The benefit on the EMI filter of the proposed interleaving scheme is demonstrated by the EMI filter prototype. For the non-interleaving PFC, based on the measured DM and CM noise, the filter attenuation requirement can be calculated as shown in Table 3.1. For the conventional interleaving PFC, since there is no impact on the 2nd order harmonic, the filter attenuation requirement is exactly the same. An EMI filter is designed based on the calculated attenuation requirement. Two 4.7 nF capacitors are used as the Y capacitor. A 1.5 mH common mode inductor is implemented with ZJ-42908TC with 21 turns. The measured leakage inductance of the CM chock is 17 uH. With two additional DM inductors, the total DM inductance is 28 uH. To obtain the desired attenuation, two X

capacitors are used, each capacitance is 2.15 uF. The measured total EMI noise of the single-channel and 2-channel conventional interleaved PFC with the designed EMI filter prototype is shown in Figure 3.5. Both of them can meet the standard and have the same 2nd order harmonic.

Table 3-1. Filter attenuation requirement for single-channel and 2-channel conventional interleaved PFC.

	Frequency	Noise Level	Standard	Desired Attenuation
DM	260 kHz	144 dBuV	61.4 dBuV	88.6 dB
CM	260 kHz	91 dBuV	61.4 dBuV	35.6 dB

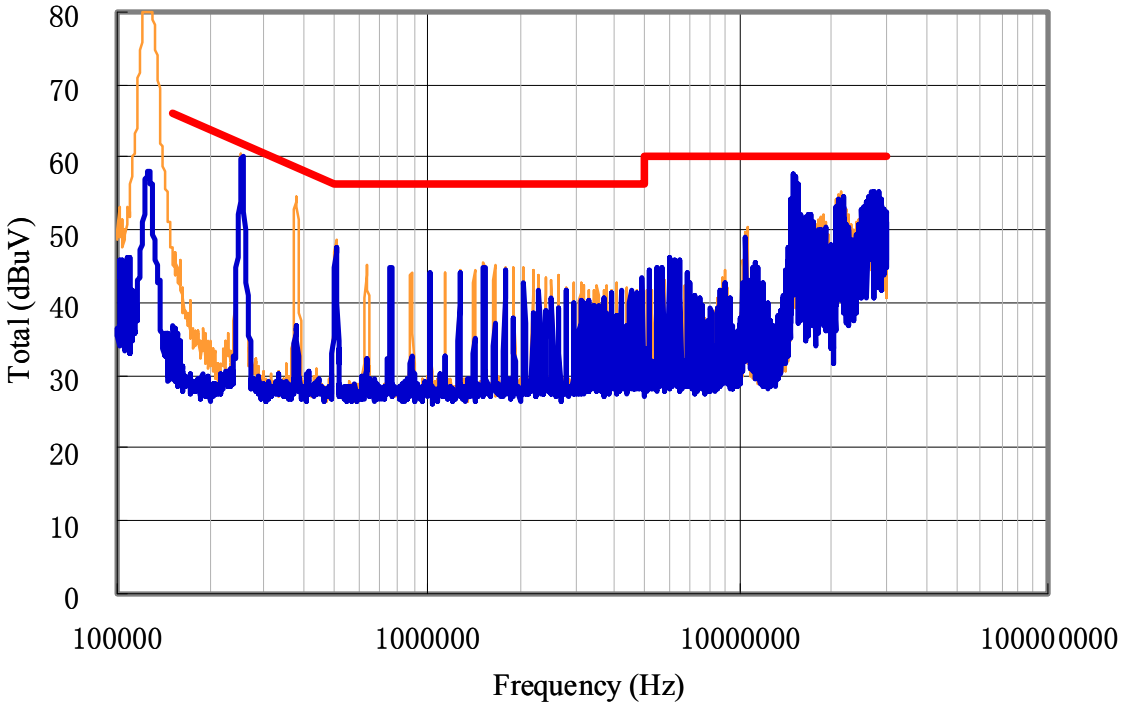


Figure 3.5. Measured total EMI noise with EMI filter (Orange line: Single channel; Blue line: Conventional 2-channel interleaving).

For the proposed 2-channel PFC with phase angle control, based on the measured DM and CM noise, the filter attenuation requirement can be calculated as shown in Table 3.2.

An EMI filter is designed based on the calculated attenuation requirement. Two 4.7 nF capacitors are used as the Y capacitor. A 0.61 mH common mode inductor is

implemented with ZJ-42206TC with 15 turns. The measured leakage inductance of the CM chock is 7 uH. With two added DM inductors, the total DM inductance is 18 uH. To obtain the desired attenuation, two X capacitors are used, each capacitance is 1 uF. The measured total EMI noise with the designed EMI filter prototype is shown in Figure 3.6. The EMI noise with the designed filter can pass the standard.

Table 3-2. Filter attenuation requirement for 2-channel PFC with phase angle control.

	Frequency	Noise Level	Standard	Desired Attenuation
DM	390 kHz	133 dBuV	58 dBuV	81 dB
CM	390 kHz	91 dBuV	58 dBuV	33 dB

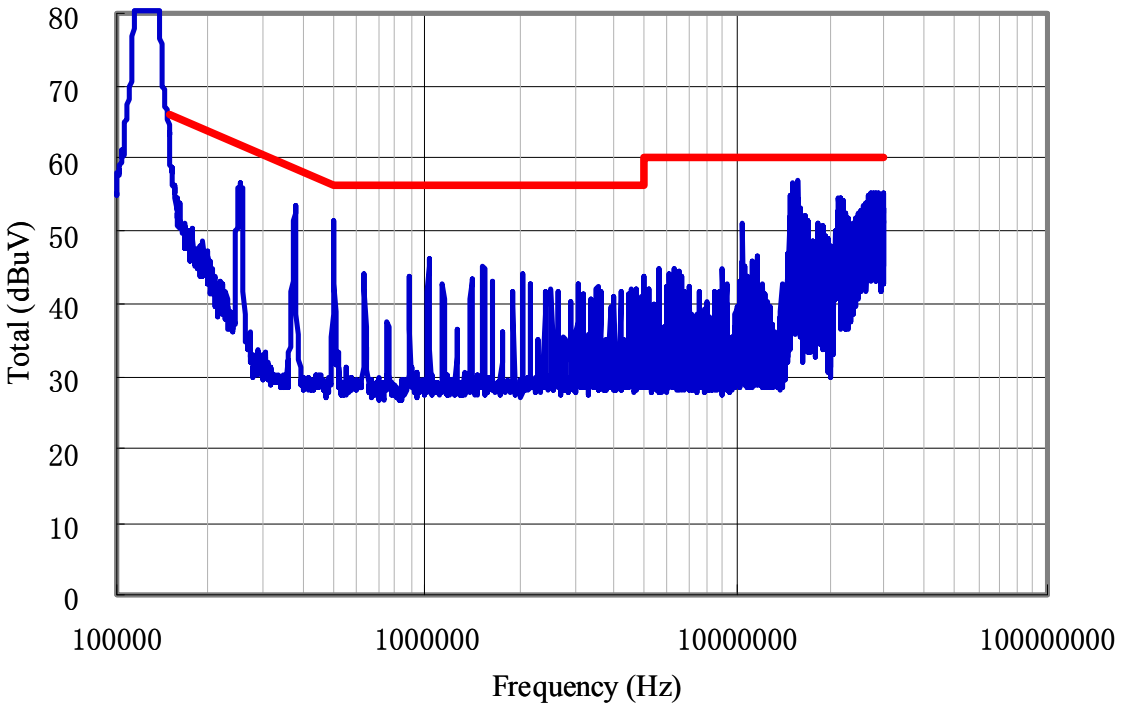
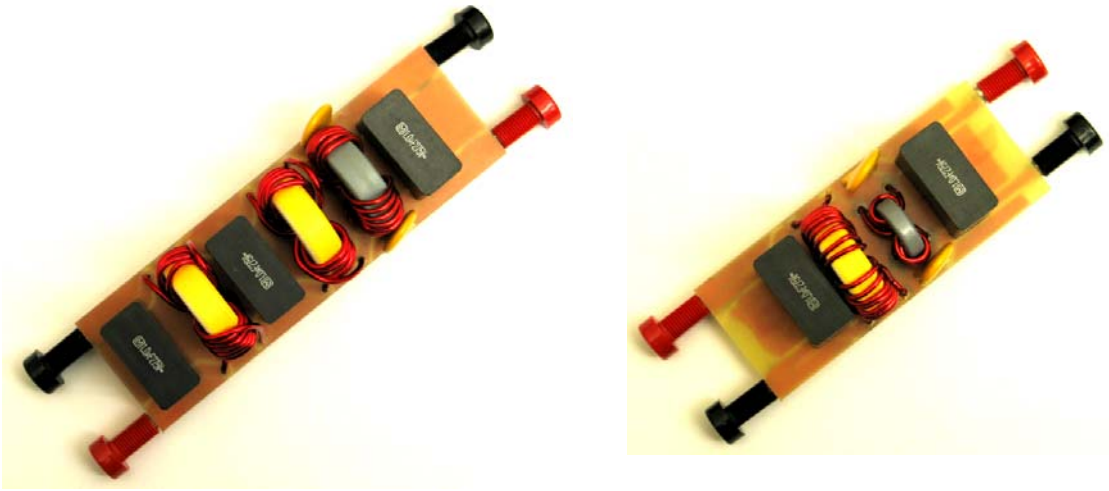


Figure 3.6. Measured EMI noise with EMI filter for proposed 2-channel PFC *90°* degree phase shift.

The designed two EMI filter prototype is shown in Figure 3.7. Based on the same PFC hardware, same switching frequency, just by changing the interleaving scheme to *90°* phase shift, 39% total volume reduction of the EMI filter can be achieved.



(a) Single-channel and 2-channel conventional interleaved PFC

(b) Proposed 2-channel *90°* degree phase shift PFC

Figure 3.7. EMI filter prototypes comparison.

The basic idea of the proposed interleaving scheme is that, not like the conventional interleaving, we can actually choose which order harmonic to cancel. By controlling the phase shift angle, we can target the cancellation effect to happen at any order of the harmonics. The *90°* phase shift scheme is specially proposed to cancel the 2nd order harmonic for the 2-channel PFC running at the switching frequency range of 75 kHz to 150 kHz. However, in the switching frequency range from 37.5 kHz to 50 kHz, neither the *90°* phase shift nor the conventional interleaving can reduce the EMI filter size, as shown in Figure 3.7. Based on the same concept, *45°* phase shift scheme can benefit the EMI filter design when the switching frequency ranges from 37.5 kHz to 50 kHz. *45°* phase shift for 2-channel PFC can cancel the 4th order harmonic and reduce the 5th order harmonic. By this *45°* phase shift the EMI filter can be designed based on higher frequency noise with smaller magnitude, so the EMI filter size can be reduced. Same concept can be further extended to even lower switching frequency range, as shown in Figure 3.8.

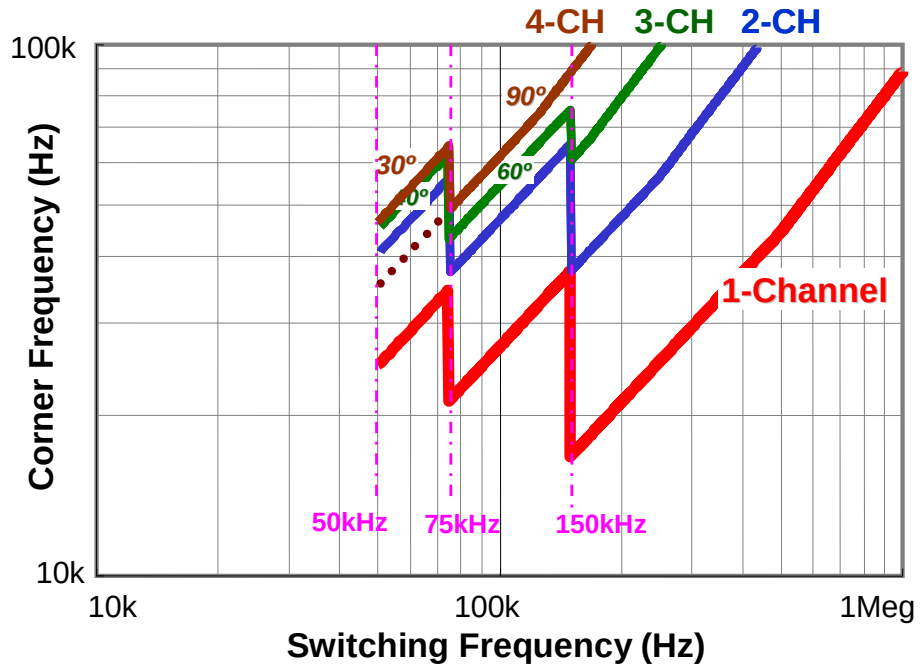


Figure 3.8. DM filter corner frequency v.s. switching frequency for multi-channel PFC with phase angle control.

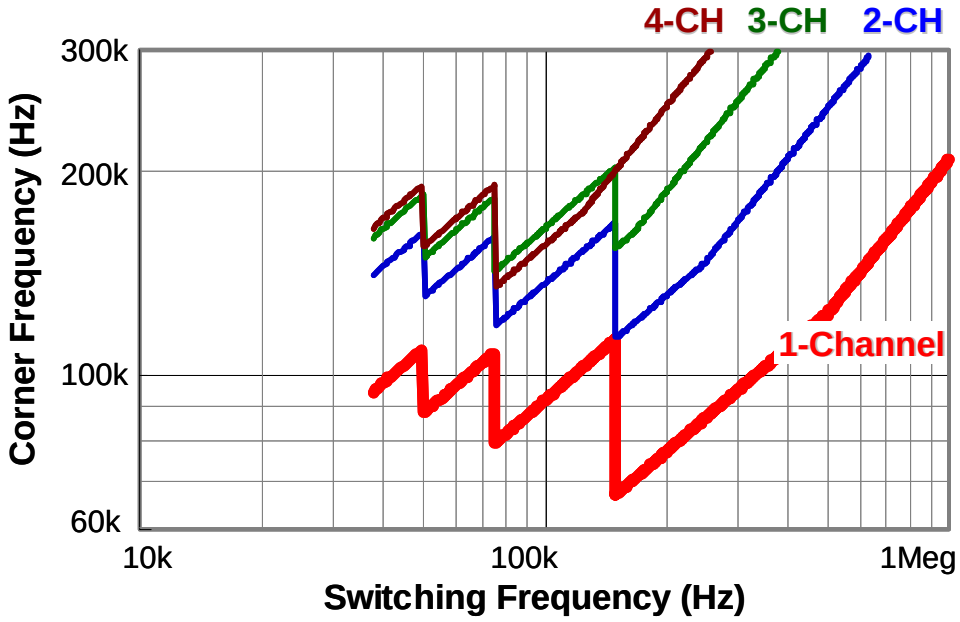


Figure 3.9. CM filter corner frequency v.s. switching frequency for multi-channel PFC with phase angle control.

The phase angle control strategy can also be extended to other multi-channel PFC. The DM filter corner frequency for non-interleaving (1-Channel) and the proposed phase angle control strategy are summarized and compared in Figure 3.8.

The CM filter corner frequency will also have the similar trend as the DM filter as shown in Figure 3.9.

3.3.2 Output capacitor evaluation

The conventional interleaving method can maximize the output current ripple reduction since the switching frequency component, which has the largest magnitude, is cancelled. For the proposed asymmetrical although it is not optimal in terms of output current ripple reduction, it also can reduced significant amount of the current ripple. Again, interleaving scheme will only impact the switching frequency current ripple. 2-channel *90°* phase shift PFC will be used as one example illustrate the output ripple cancellation effect for phase angle control strategy.

The switching frequency current ripple RMS value for 2-channel *90°* phase shift can be calculated as,

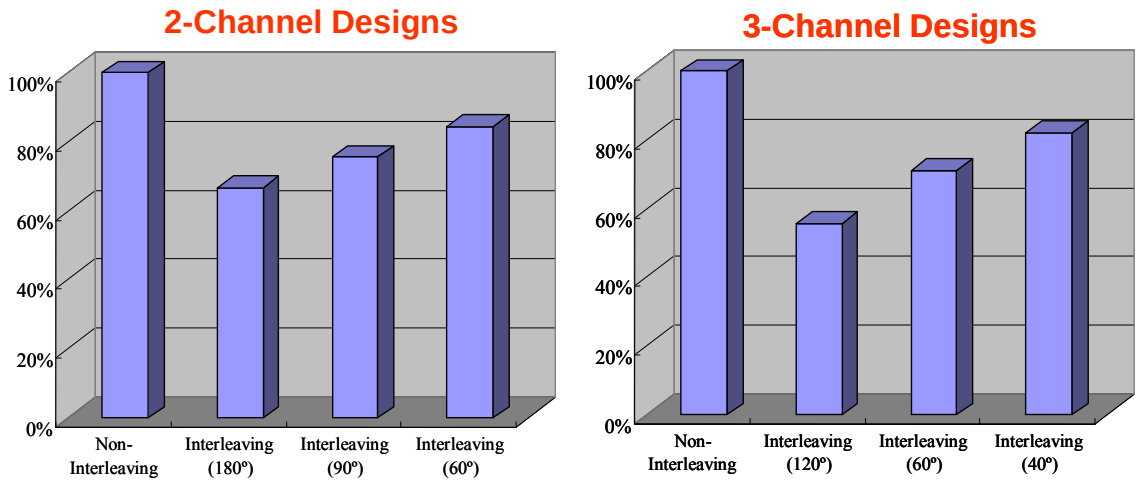
$$I_{rms\_3}(t)=\begin{cases} 2d(t)\left[i_2(t)-i_1(t)\right]^2+8i_1(t)^2\left[0.5-d(t)\right] & d\le 0.25 \\ 0.5\left[i_2(t)-i_1(t)\right]^2+4i_1(t)^2\left[0.75-d(t)\right]+4i_2(t)^2\left[d(t)-0.25\right] & 0.25<d(t)\le 0.75 \\ 2\left[1-d(t)\right]\left[i_1(t)-i_2(t)\right]^2+8i_1(t)^2\left[d(t)-0.5\right] & d>0.75 \end{cases} \tag{3-1}$$

Based on Equation (3-1), the high frequency current I_H can be calculated as,

$$I_{H\_3}=\sqrt{\frac{2}{T_{line}}\int_0^{\frac{T_{line}}{2}} i_{rms\_3}(t)dt} \tag{3-2}$$

The high frequency RMS ripple current I_H varies with the input line voltage.

Following the same procedure discussed in the previous chapter, the effective capacitor current ripple of other multi-channel PFC with phase angle control can be obtained, as shown in Figure 3.10 (a) and (b).



(a) 2-channel design **(b) 3-channel design**

Figure 3.10. Output capacitor RMS current reduction with phase angle control

3.4 Digital Controlled Multi-Channel PFC with Phase Angle Control Strategy

To realize and demonstrate the previously discussed features of the multi-channel phase angle controlled PFC, as an example, a digital controlled 4-channel PFCprototype is designed and developed, as shown in Figure 3.11. It consists of three major parts, the 4-channel PFC power stage, the interface board, and the DSP controller. The 4-channel PFC power stage consists of four small boost converters. Each boost converter has a boost inductor, a MOSFET, and a diode. The boost inductor is implemented with Kool Mu core, 77894-A3. The inductor has 115 turns, and AWG#22 magnite wire is used because the smaller current stress. The Infineon CoolMOS, IPB60R199CP, is used as the boost switch to achieve both small conduction loss and switching losses. The Infineon SiC diode, SDD04S60, is used as the boost diode. Four channels are designed and implemented to be indentical.

The feedback and PWM signals need to be exchanged between the power stage and the DSP controller. The interface board is in the middle to process the analog signals. The

sensed feedbacks need to be scaled appropriately, and then connected to the ADC(analog to digital converter) pins. The ADC samples these quantities and turns them into a numerical representation.The PWM outputs of the DSP chip need to be convertered to appropriate level for the gate drive chip on the power stage.

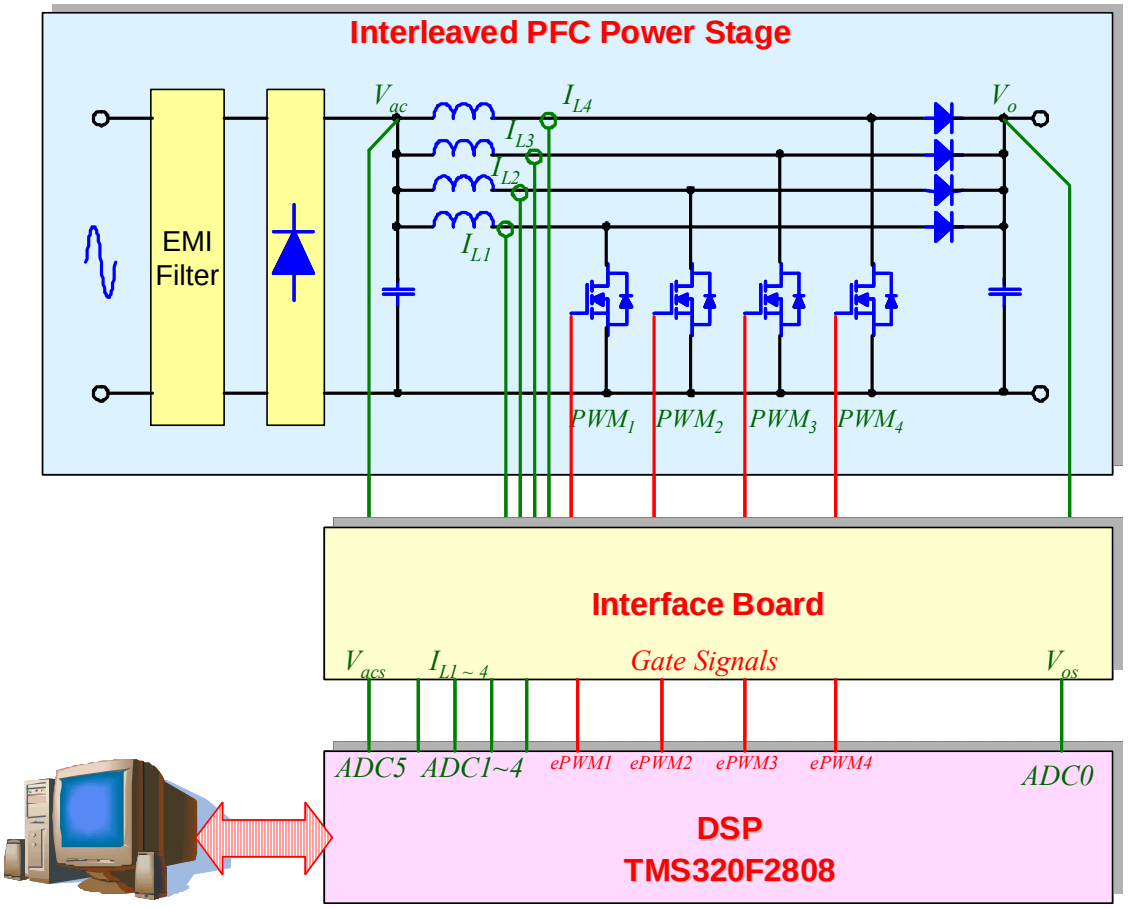


Figure 3.11. System diagram of digital controlled 4-channel PFC with phase angle control strategy.

The feedback signals include rectified AC line voltage, PFC output voltage, and four inductor currents. These signals are scaled properly by the interface board, and then send to the ADC pins of a TMS320F2808 signal processor. After processed by the control software of the DSP, the PWM signals are sent out to the PWM modules. After a voltage level conversion, the PWM signals are sent to the four corresponding MOSFET gate drives to control the switches.

3.4.1 PFC control algorithm

The block diagram of PFC software algorithm is shown in Figure 3.12. Each block in the diagram represents a function module in the DSP program.

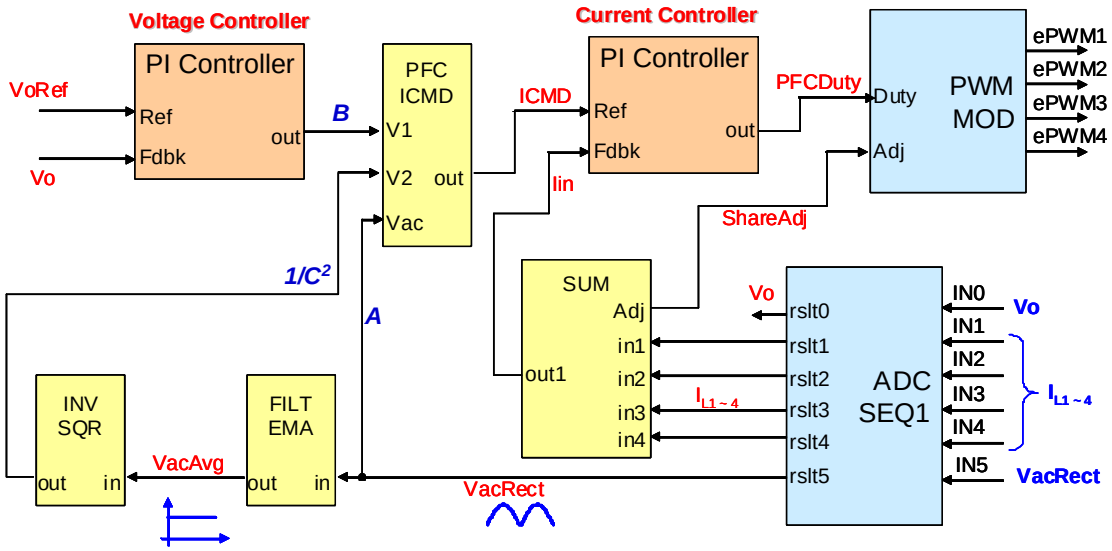


Figure 3.12. Block diagram of PFC software algorithm.

The following is the list of the function modules:

ADC SEQ1: Six channel continuous conversion ADC driver;

FILT EMA: A low pass filter using Exponential Moving Average (EMA) algorithm;

INV SQR: Inverse square computaion module;

PI Controller: PI controller module;

PFC ICMD: Current command calculator module;

SUM: Total current calculation and channel duty cycle adjustment;

PWM MOD: PWM distribution module;

ADC SEQ1 software module controls the ADC on the TMS320F2808 devices. It sets up the ADC in continuous conversion mode, to convert six channels of feedback signals into corresponding variables. The feedback signals are sensed at each switching cycle.

FILT EMA software module performs a numerical low pass filter using EMA algorithm. The input of this module is the sensed rectified input line voltage after AD converter. The output is the average value of the rectified input line voltage. Comparing with the conventional moving average algorithm, EMA applies weighting factors which decrease exponentially to each data point. The EMA algorithm can be described by the follwing equation:

$$EMA(n) = EMA(n-1) + \alpha * (p(n) - EMA(n-1)) \tag{3-3}$$

Where $\alpha = \frac{2}{N+1}$.

Because the frequency of AC line voltage varies, the performances of conventional moving average and EMA are almost the same. The benefit of using EMA is that it can average the input without storing large amont of sensing data.

INV SQR software module performs a numerical inverse square calcuation of the input. The input of this module is an average of a rectified input voltage processed by the FILT EMA module.

The INV SQR module function can be described by Figure 3.13. The input signal is clamped to a minimum to allow the PFC system to work with very low line voltages without overflows, which can cause undesired effects. The maximum and minimum limit specify the magnitude boundary of the PFC current command.

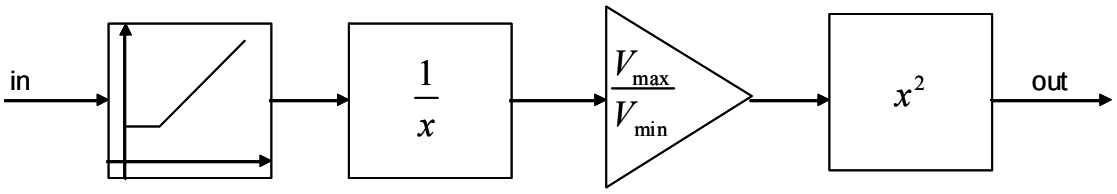


Figure 3.13. Block diagram for the INV SQR module.

The PI Controller software module implements a proportional-integral controller by implementing the difference equation,

$$U(n) = K_p \cdot e(n) + K_I \cdot I(n) \tag{3-4}$$

$$I(n) = I(n-1) + e(n) \tag{3-5}$$

The PFC ICMD software module performs a computation of the current command for the power factor correction, as described in Figure 3.14. The inputs are generally connected to the inverse-squared/averaged line voltage, the rectified line voltage and the output of the voltage controller.

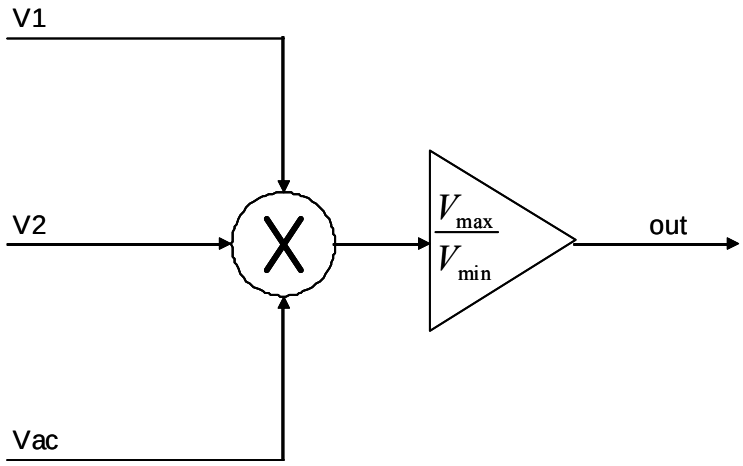


Figure 3.14. Block diagram for the PFC ICMD module.

The PFC ICMD software module is actually mimic the analog controller of PFC.

$$I_{ref} = \frac{A \cdot B}{C^2} \tag{3-6}$$

where $A = K_{in} \cdot v_{in}$ (K_{in} : Input voltage gain), $B = v_c$ (v_c : Voltage compensator output) and $C = K_{ff} \cdot v_{in\_rms}$ (K_{ff} : Input voltage feed forward gain). The PFC_ICMD block generates an output command profile that is rectified sinusoidal, with an amplitude dependent on the output of the voltage controller. The output is then connected to the current controller to produce the required inductor current.

The SUM software module calculates the total input current by add the sensed four channels' inductor currents. The average current of the four channels is also calculated. The difference between the channel current and the average current is used for current sharing adjustment.

The PWM MOD module controls the EPWM1, 2, 3, and 4 generators to drive the four-channel interleaved PFC stage. This module forms the interface between the control software and the device PWM pins.

3.4.2 PFC control program flow chart

The flowchart of main program is shown in Figure 3.15. One task of the main program is to setup the processor envirement, including system initialization, variables initialization, ADC configuration, and EPWM modules initialization. After that the main program is in the background loop, waiting for the ADC interrupt triggered by the EPWM modules.

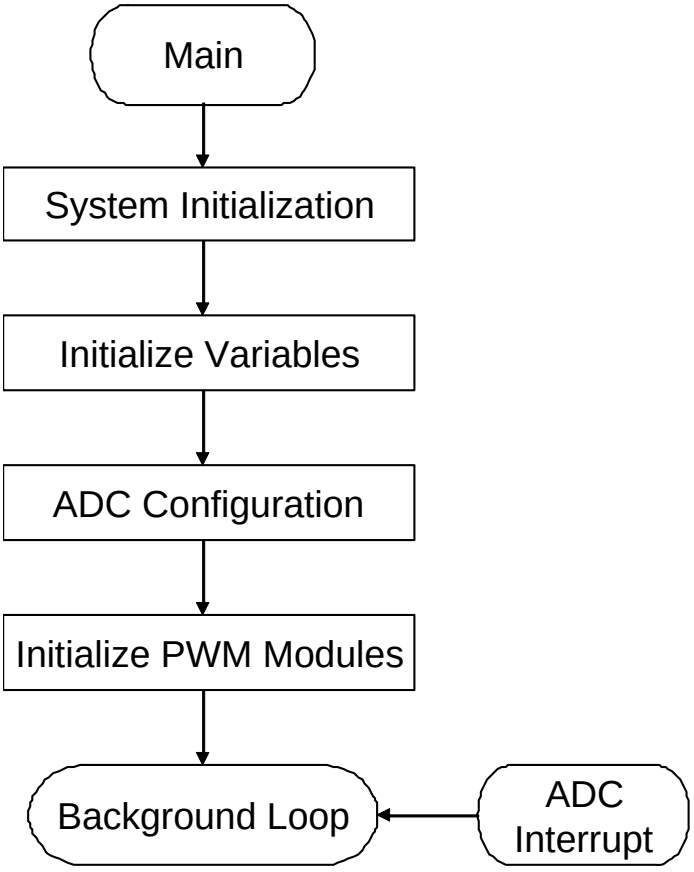


Figure 3.15. Flowchart of main program.

The flowchart of ADC interrupt program is shown in Figure 3.16. The ADC interrupt program is triggered by the EPWM module. The ADC interrupt program is called every switching cycle. In every switching cycle, the sensed signals are read. The feedback data are used to calculate the duty cycles for the four channels. The duty cycle of the four EPWM modules are update every switching cycle. After that, the program reinitialize the ADC sequence and return to the main program until the next trigger generated by the EPWM module.

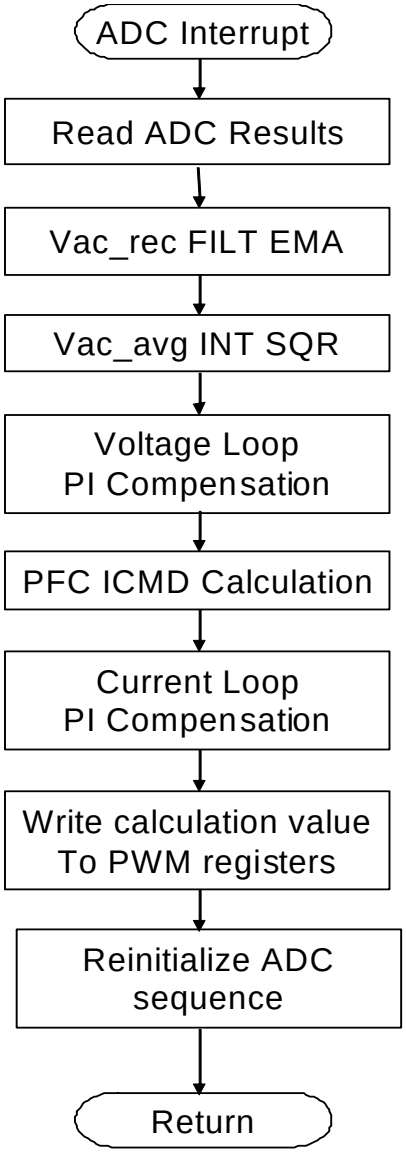


Figure 3.16. Flowchart of ADC interrupt program.

3.4.3 PFC current sensing

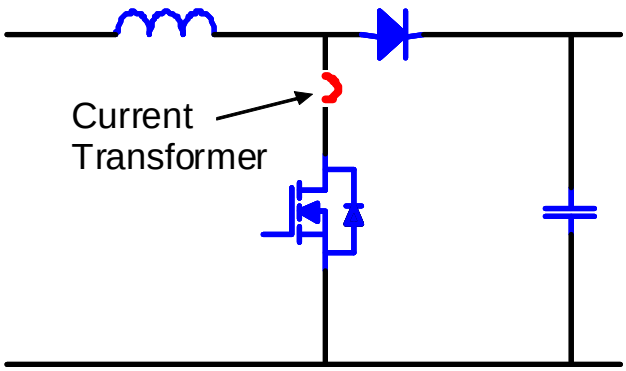


Figure 3.17. Current transformer in boost module.

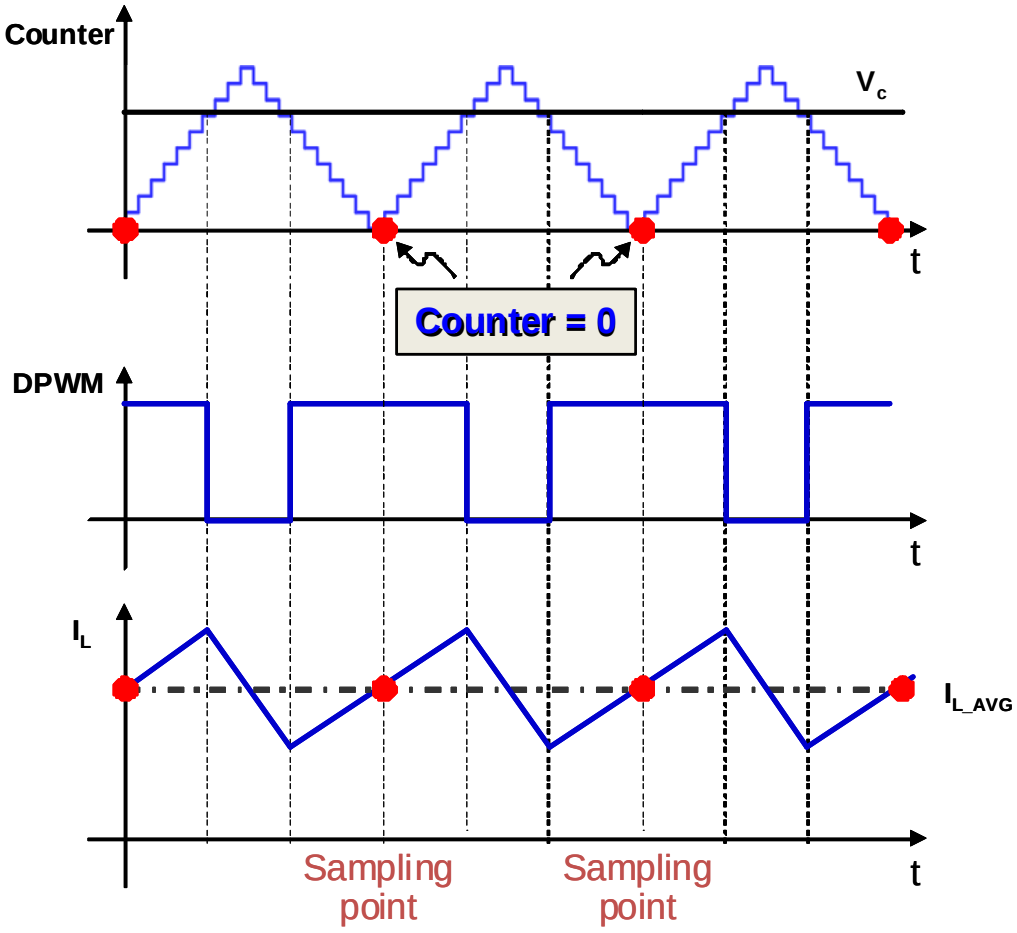


Figure 3.18. Current sampling strategy with one current transformer.

Average mode current control is used for the current loop of PFC. For analog implementation, the inductor current can be sensed and due to the low bandwidth of current control loop, average current can be automatically obtained and controlled through the current loop. For digital implementation, the current information is discrete, so the sampled current must represent the average of total current in order to implement the average current control.

The inductor average current can be sensed at the middle point of either the boost switch turn on period or the turn off period. As shown in Figure 3.17, one current transformer is in series with the boost switch. With this implementation, the inductor average current can be always sampled at the middle point of the turn on period.

The sampling point is set at the point when the ramp counts to zero as shown in Figure 3.18, since up-down counter is configured in the EPWM control register. The experimental waveform is shown in Figure 3.19. The average inductor current can be well represented when the sampling point is controlled at the middle of the turn-on period, marked with white dot.

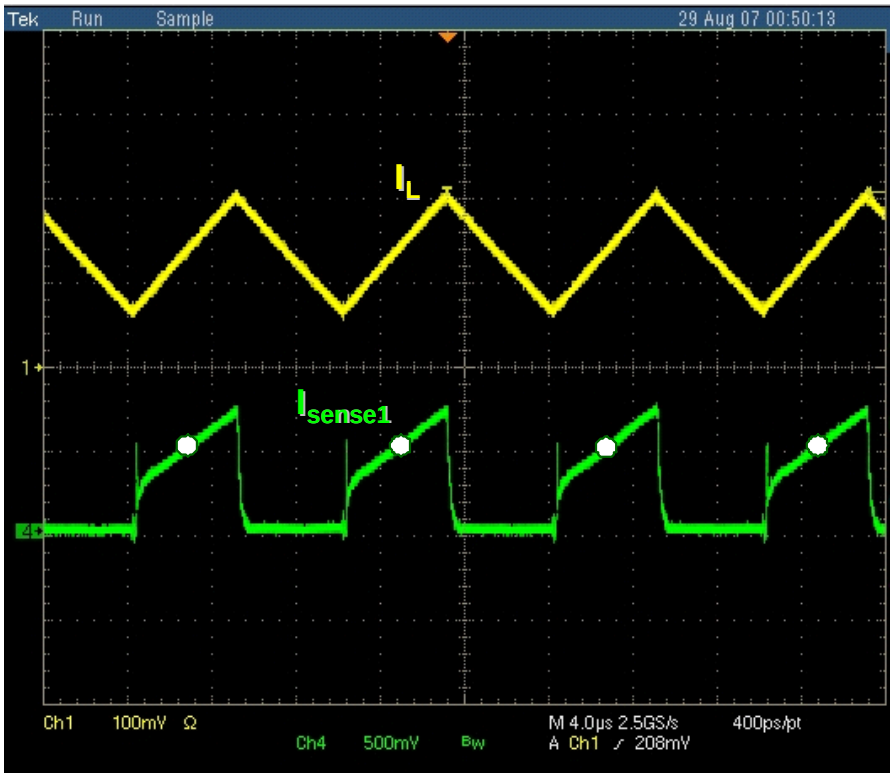


Figure 3.19. Experimental current sensing waveform.

3.4.4 Digital implementation of phase angle control

In the DSP chip, TMS320F2808, a time-base synchronization scheme connects all of the ePWM modules. Each ePWM module has a synchronization input (EPWMxSYNCI) and a synchronization output (EPWMxSYNCO). The input synchronization for the first instance (ePWM1) comes from an external pin. The synchronization connections for the remaining ePWM modules are shown in Figure 3.20.

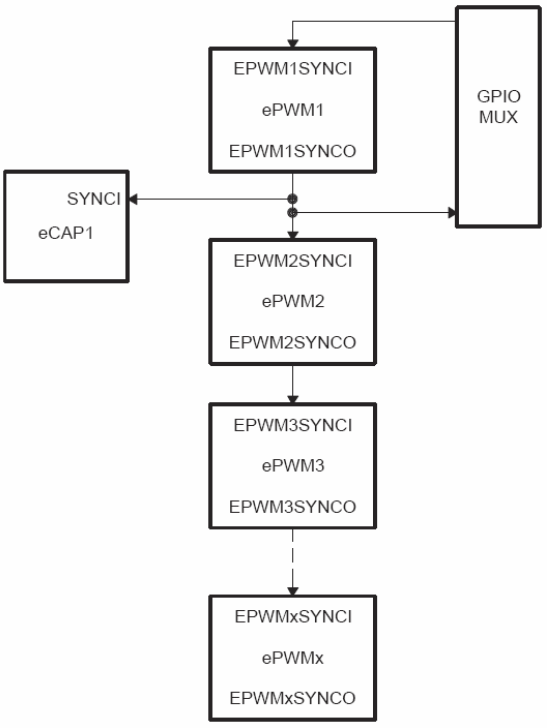


Figure 3.20. Time-base counter synchronization scheme.

The value of the phase register is loaded into the counter register when an input synchronization pulse is detected (TBPHS → TBCNT). This operation occurs on the next valid time-base clock (TBCLK) edge.

This feature enables the ePWM module to be automatically synchronized to the time base of another ePWM module. Lead or lag phase control can be added to the waveforms generated by different ePWM modules to synchronize them. In up-down-count mode, the TBCTL[PSHDIR] bit configures the direction of the time-base counter immediately after a

synchronization event. The new direction is independent of the direction prior to the synchronization event.

By configuring the TBCTL[PSHDIR] register bit and storing the right value to the TBPHS register, any phase angles between the channels can be controlled with certain resolution. The resolution is determined by the system clock frequency and the PFC switching frequency.

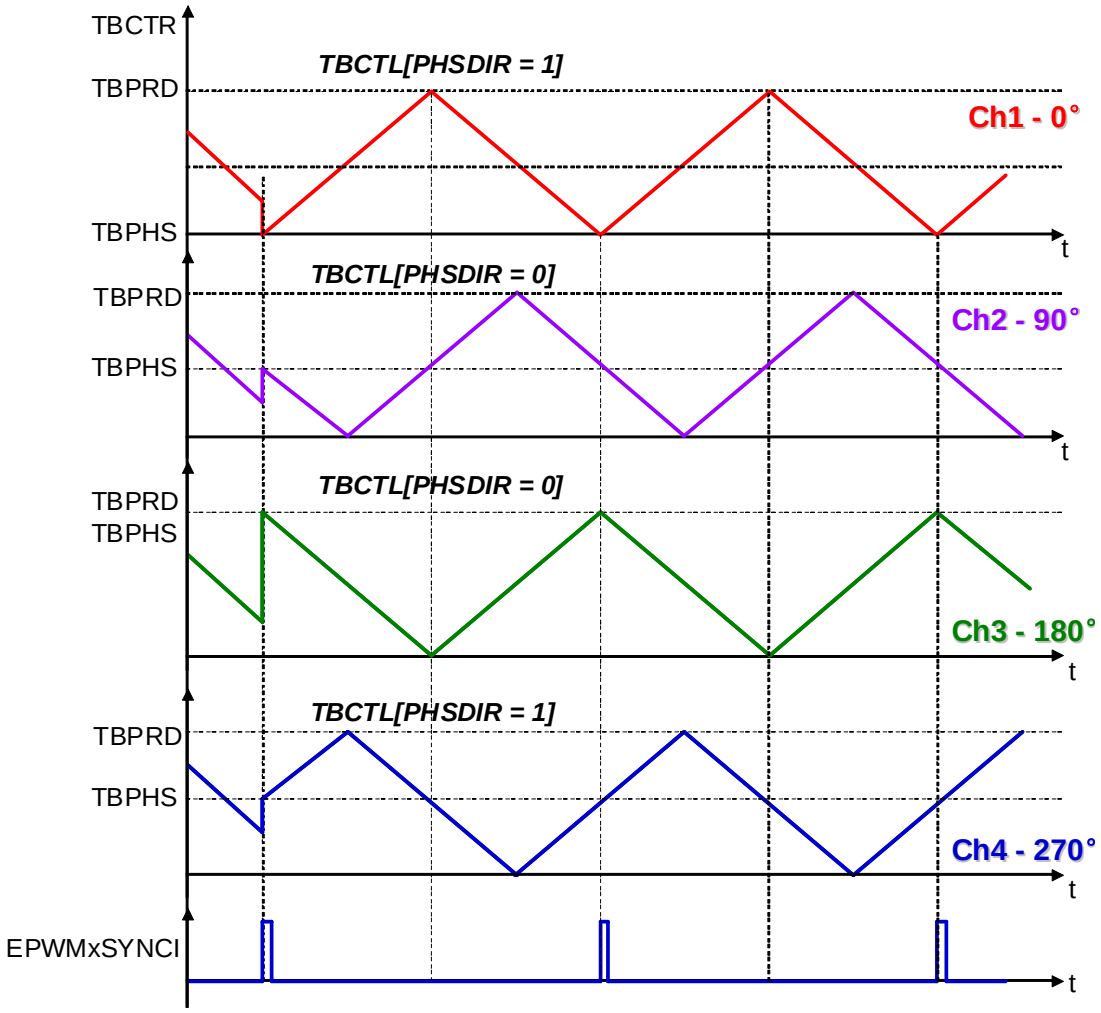


Figure 3.21. Digital implemental of phase angle control for 4-channel PFC.

Figure 3.21 shows one example of the registers configuration of phase angle control for 4-channel PFC. Channel-1 is considered as the reference of phase shift for all the other three channels. The value stored in the TBPHS register of channel-1 is zero. The TBCTL[PSHDIR] register bit is configured to be 1. For channel-2, half of TBPRD (Time-

Base Period Register) value is stored in the TBPHS register. TBCTL[PSHDIR] register bit is configured to be 0. The counter register will load the TBPHS value and start to count down once the EPWMxSYNCI clock comes. Thus, 90º phase delay is achieved for channel-2 is realized. For channel-3, TBPRD (Time-Base Period Register) value is stored in the TBPHS register. TBCTL[PSHDIR] register bit is configured to be 0. For channel-4, half of TBPRD (Time-Base Period Register) value is stored in the TBPHS register. TBCTL[PSHDIR] register bit is configured to be 1. In this way, 90º phase shift between four channels are realized.

Following the described approach, any phase shift angle between the channels can be easily realized.

3.4.5 Prototype and experimental verification

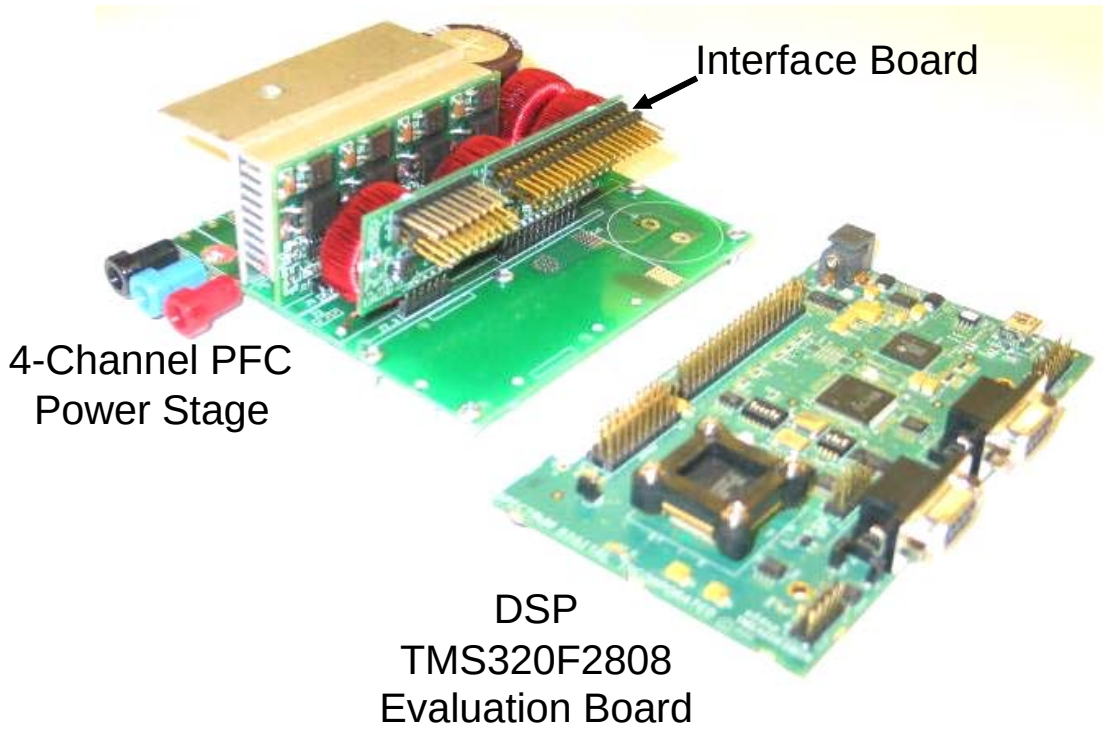


Figure 3.22. Prototype picture of digital controlled 4-channel interleaved PFC.

Corresponding to the design described in Figure 3.11, the digital controlled 4-channel interleaved PFC prototype is developed as shown in Figure 3.22. The blank space on the

power stage board is for the DC-DC converter stage. The interface board is plugged in the power stage board. The 4-channel PFC control is implemented with the TMS320F2808 evaluation board from TI. The interface board and the evaluation board are connected through flat cables.

The experimental waveforms of the digital controlled 4-channel interleaved PFC are shown in Figure 3.23. Th input AC voltage 110 Vrms, 60 Hz. The output is regulated at 400 V. 300 W for each channel, the total power is 1200 W. The phase shift angle of the channel is 90 º.

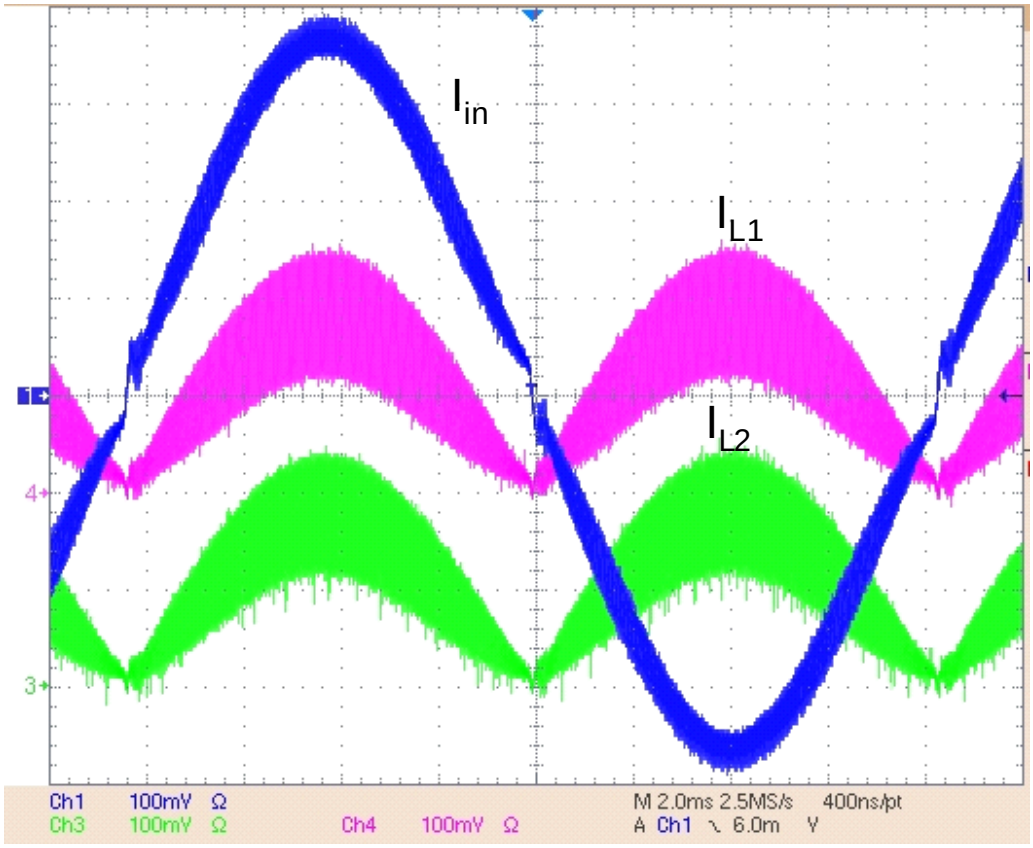


Figure 3.23. Experimental waveforms of the digital controlled 4-channel interleaved PFC.

3.5 Summary

Comparing the output requirement of the VR application and input requirement of the PFC application, it can be found that the VR input requirement is defined in the time domain while the PFC output requirement is defined in the frequency domain. Since the requirement is different, although the interleaving impact on the circuits are exactly the same, the interleaving design consideration also could be different. In this chapter, different interleaving strategy for multi-channel PFC is investigated considering the EMI requirement for this AC-DC application.

According the analysis in the previous chapter, EMI filter size can only be reduced when the interleaving channel number and the switching frequency are properly chosen. Based on the harmonic cancellation, and with all the detail phase relationship of the switching frequency harmonics and all the side band harmonics, a novel phase angle control method is proposed to maximize the reduction of the EMI filter. For 2-channel interleaved PFC, just by changing the interleaving scheme to 90 degree phase shift, 39% total volume reduction of the EMI filter can be achieved. The phase angle control impact on the output capacitor current ripple is also studied. To realize and demonstrate the previously discussed features of the multi-channel phase angle controlled PFC, as an example, a digital controlled 4-channel PFC prototype is designed and developed. The PFC control algorithm, control program flow chart, current sensing implementation, and the digital implementation of phase angle control are discussed. The 4-channel PFC and the digital control with phase angle control scheme is design and experimentally verified by the developed prototype.

The phase angle control method discovered in the multi-channel boost converter can be applied back to the multi-phase buck converter too. The harmonic cancellation principle is the same as the multi-channel boost converter. The same benefits can be obtained when the requirement is defined in the frequency domain, e.g. the EMI Standard.

Chapter 4. Light Load Efficiency Improvement for PFC

4.1 Introduction

Driven strongly by economic and environmental concerns, high efficiency is more and more required by various organizations and programs, such as the U.S. Energy Star [26], Climate Savers [27], and German Blue Angel [28].

80 plus is a basic efficiency requirement for the front-end converter, as shown in Figure 1.6. It requires the efficiency to be higher than 80% at 20%, 50%, and 100% load. Other than the 80 plus requirement, Climate Savers is targeting at higher efficiency. It even target to achieve 4% or 3% efficiency improvement every year in these coming two years. By June, 2010, it is expected to achieve 88% efficiency at 20% and 100% load, and 92% effciency at 50% load. The computer giant, Dell, is targeting at even more aggressive effciencies, as shown in Figure 1.6. Not only the efficiency target is set higher, but also 10% and 5% load efficiency is required.

Based on these activity of varies organizations and companies, the trend is that the efficiency requirement keeps increasing and is extending to lighter load conditions. Today, the power supply industry is at the beginning of a major focus shift that puts efficiency improvements across the entire load range. This focus on efficiency has been prompted by economic reasons and environmental concerns caused by the continuous, aggressive growth of the Internet infrastructure and a relatively low energy efficiency of power delivery systems of large Internet-equipment hosting facilities [29].

Using the most advanced semiconductor devices, the existing modular approach still has its limitations facing today's extremly challenging requirements for simultaneous maximization of both the entire-load-range efficiency and high power density. Designed with the new generation CoolMOS (IPW60R099CS) and the SiC diode (SDP06S60), switching at 130 kHz, the measured PFC efficiency is shown in Figure 4.1. Further improvement at light load is still needed to meet today's efficiency challenges.

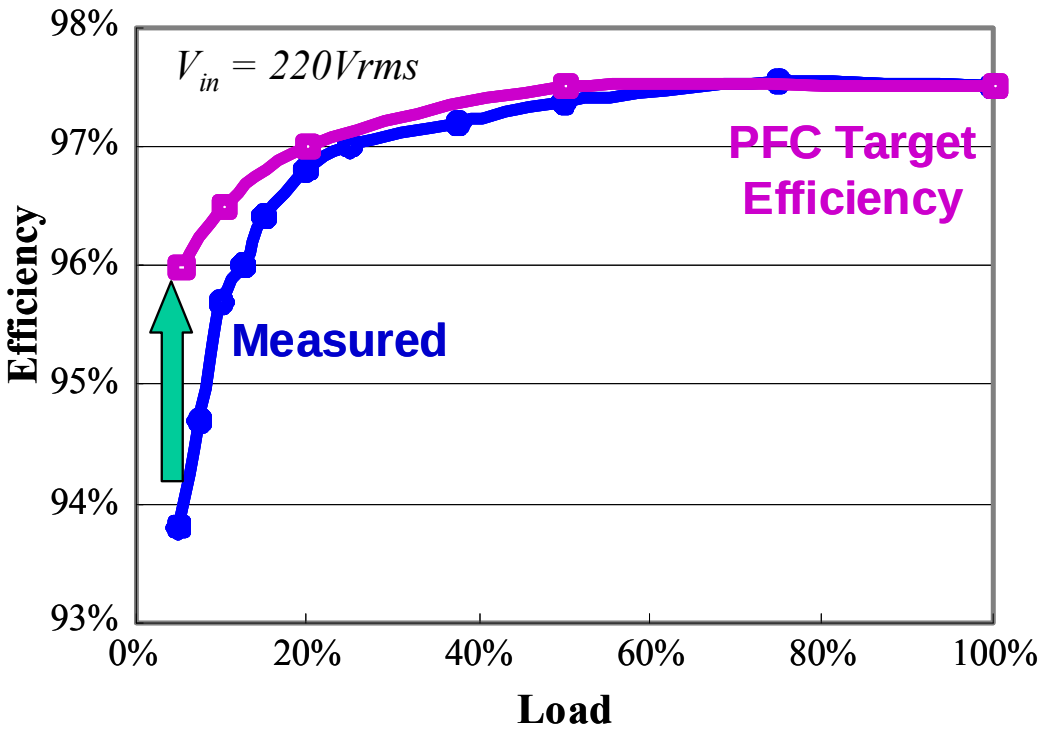


Figure 4.1. Measured PFC high line efficiency with CoolMOS and SiC diode.

4.2 Phase Shedding for Multi-Channel PFC

In a multi-channel configuration, it is possible to use phase-shedding, or sometimes also referred as the Optimal-Number-of-Phases (ONP) control scheme [25], to improve the light load efficiency, as shown in Figure 4.2. At heavy load, all channels are active and share the current so that high efficiency can be obtained. When the load becomes light, the power processed by each channel is actually dramatically reduced; if all the channels are still operating, the switching loss, reverse-recovery loss, inductor core loss, etc. still exist in all channels. This makes it very inefficient. Reducing the number of active channels accordingly can result in an efficiency increase at light load [25]. It has actually already been widely used for the POL applications [57].

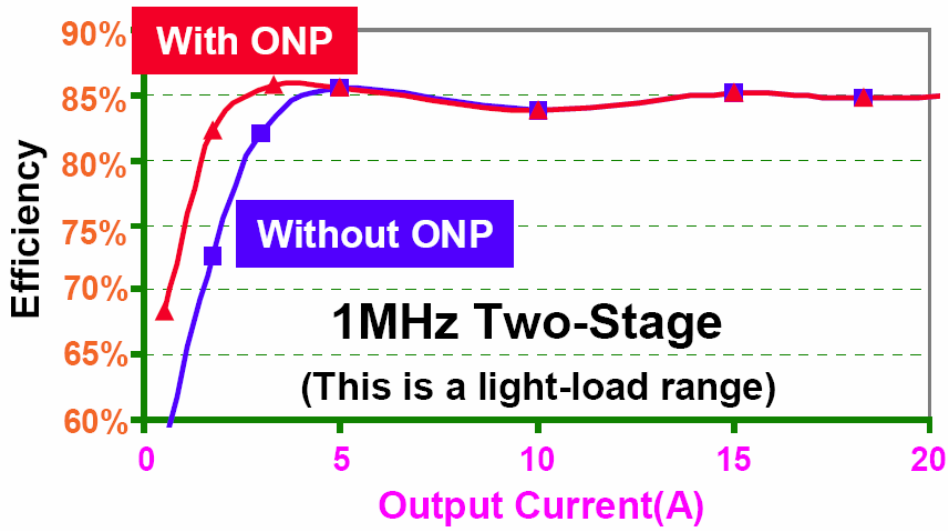


Figure 4.2. Efficiency improvement by applying phase-shedding for VR applications. [25]

Generally, phase-shedding can be used for any power converters with multi-channel configuration to improve the light load efficiency. Figure 4.3 shows the measured efficiency at 220 Vrms input of the 4-channel interleaved PFC at 130 kHz switching frequency. By phase-shedding, the light load efficiency can be improved.

However, PFC circuit has stringent EMI requirement at the input side. Reducing the number of active channels can improve the light load efficiency, but it reduces the ripple cancellation effect as well, which will result in the EMI noise increase and losing the benefit on the EMI filter.

With the phase-shedding control, the multi-channel PFC needs to operate at any channel number configuration which is defined by the controller. The PFC also needs to meet the EMI standard at any given load conditions, so the EMI filter needs to be designed according to the worst case EMI noise.

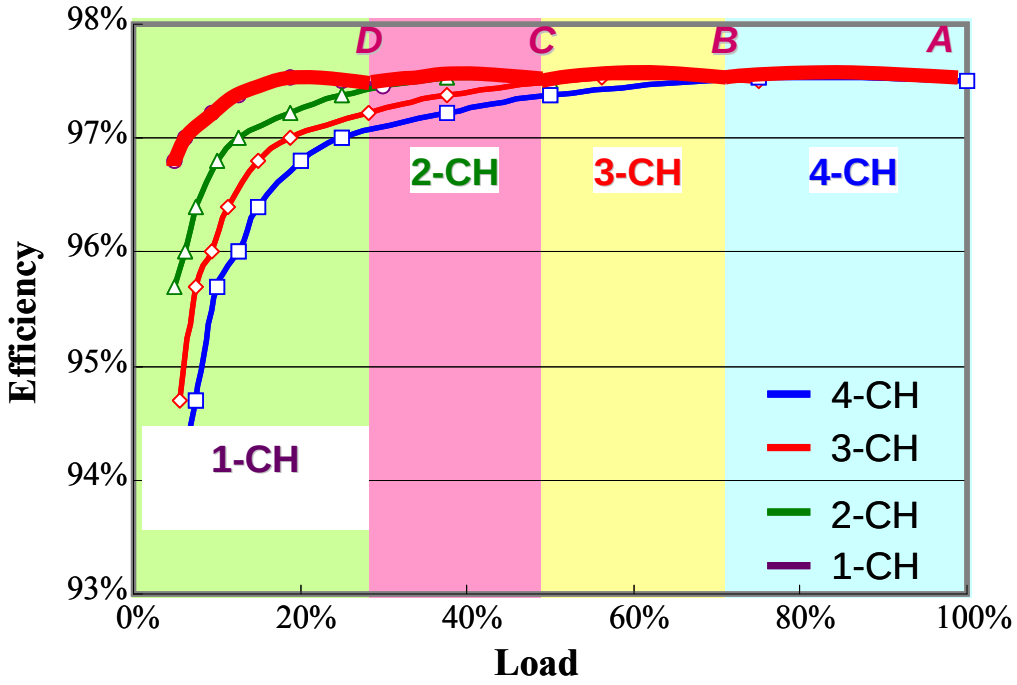


Figure 4.3. Measured PFC efficiency with phase shedding (Vin = 220 Vrms).

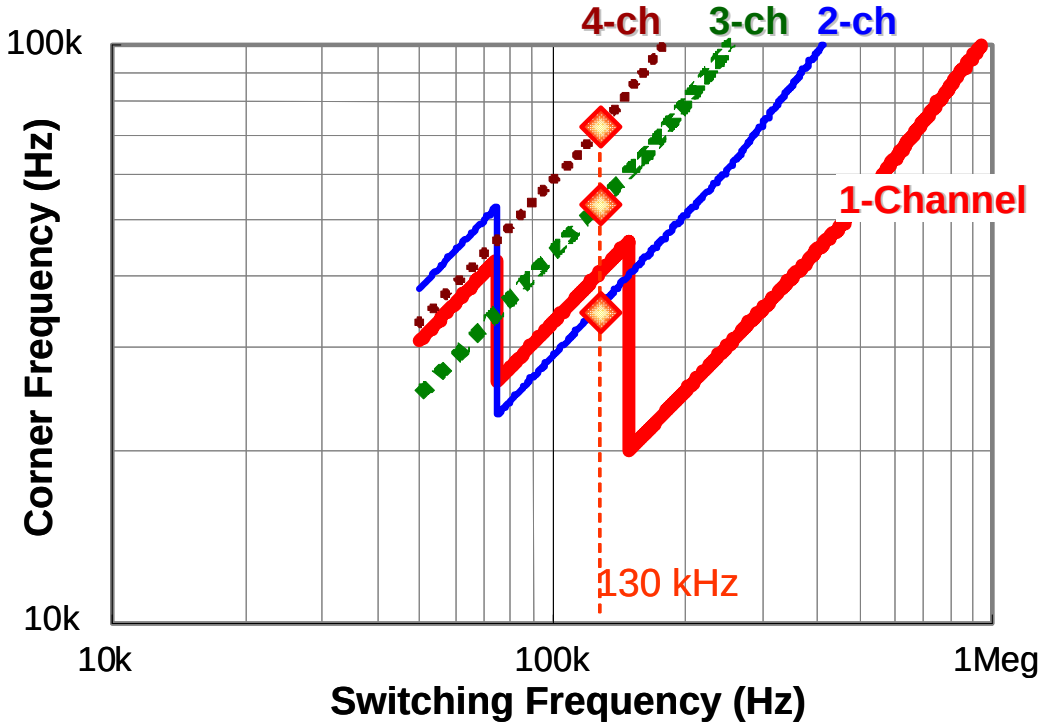


Figure 4.4. Relationship between the filter corner frequency and the switching frequency (DM filter).

The relationship between the filter corner frequency and the switching frequency for different active channel numbers is shown in Figure 4.4. Designing at different switching frequency range, the worst case EMI noise happens for different channel number configuration. For example, when the switching frequency is chosen between 75 kHz to 150 kHz, the worst case EMI noise happens for 2-channel interleaving. While for switching frequency chosen between 50 kHz to 75 kHz, the worst case EMI noise happens for 3-channel interleaving. For switching frequency design between 37.5 kHz to 50 kHz, the worst case EMI noise happens for 4-channel interleaving. Based on this observation, the EMI filter reduction obtained from multi-channel PFC configuration may loss if phase shedding technique is used to improve the light load efficiency.

Take 130 kHz switching frequency 4-channel interleaving PFC design as an example. The gate signals for each channel are shifted with uniform time intervals. The worst case in terms of EMI filter design happens when 2 channels are operating. Based on the measured DM and CM noise, an EMI filter for the 4-channel PFC with phase shedding control is design and prototyped, as shown in Figure 4.5. For the CM filter, to minimize the size, the single stage filter topology is chosen. Two 10 nF capacitors are used as the Y capacitors. A 0.8 mH common mode inductor is implemented with ZW-42507TC core with 22 turns. For the DM filter, the two-stage filter topology is chosen. Two 12.7 uH DM inductors are implemented with T106-26A cores with 22 turns. Three 1 uF capacitors are used as the X capacitors.

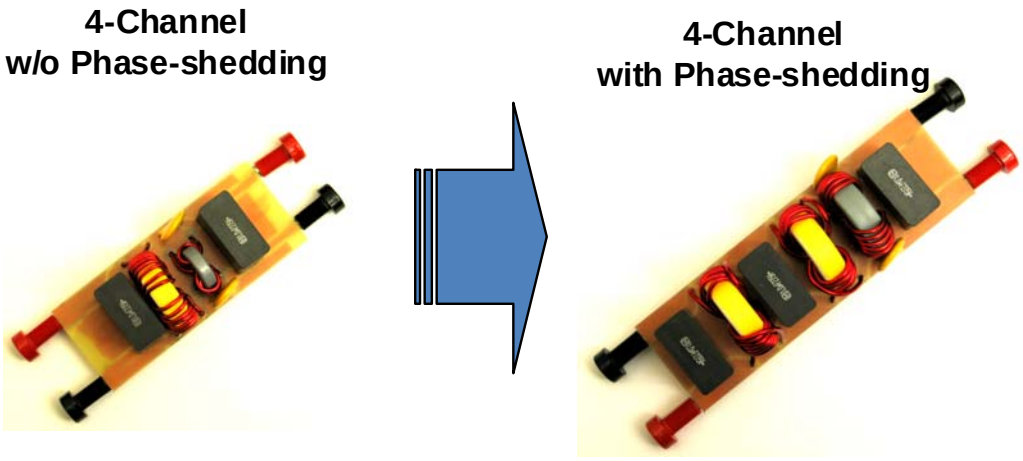


Figure 4.5. Filter prototype for the 4-channel PFC with phase shedding control.

Based on the above discussion, although the EMI filter can be reduced significantly by a 4-channel interleaved PFC, a larger filter is needed for the worst case EMI noise which happens when 2 channels are operating. It is obvious that with the phase-shedding, the benefit on the EMI filter will be lost for this multi-channel PFC design. This issue also exists for other switching frequency and channel number designs. For example, when the switching frequency is design between 50 kHz to 75 kHz, the EMI filter needs to be design based on the 3-channel interleaving, which is the worst case.

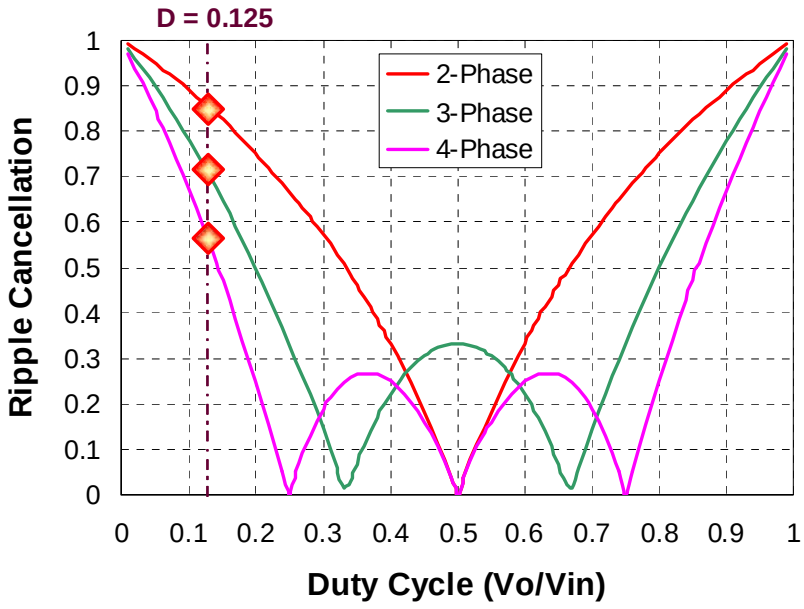


Figure 4.6. Phase shedding impact on ripple cancellation effect.

Phase shedding reducing the ripple cancellation effect also happens for the multi-phase buck converter, as shown in Figure 4.6. Take 4-phase buck VR as an example. The purple dashed line is the case when V_{in} = *12 V* and V_o = *1.5 V*, so the voltage gain is 0.125. A buck converter needs a duty cycle equal to 0.125 to do the conversion. With the phase shedding control strategy the ripple cancellation effec reduces. This issue was not raised majorly due to the output capacitance design is dominated by the transient energy buffer requirement instead of the steady state ripple requirement. It should be pointed out that for applications, where steady state output voltage ripple dominate the output capacitance design, the limitation of phase shedding method needs to be taken in to consideration.

4.3 Proposed Phase Shedding with Phase Angle Control

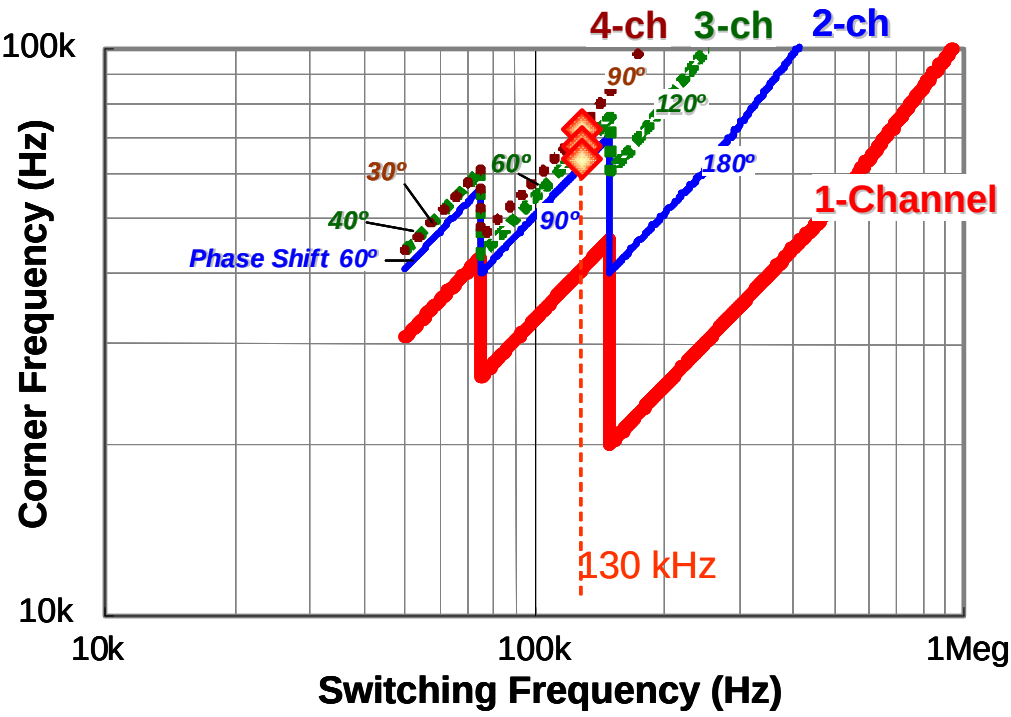
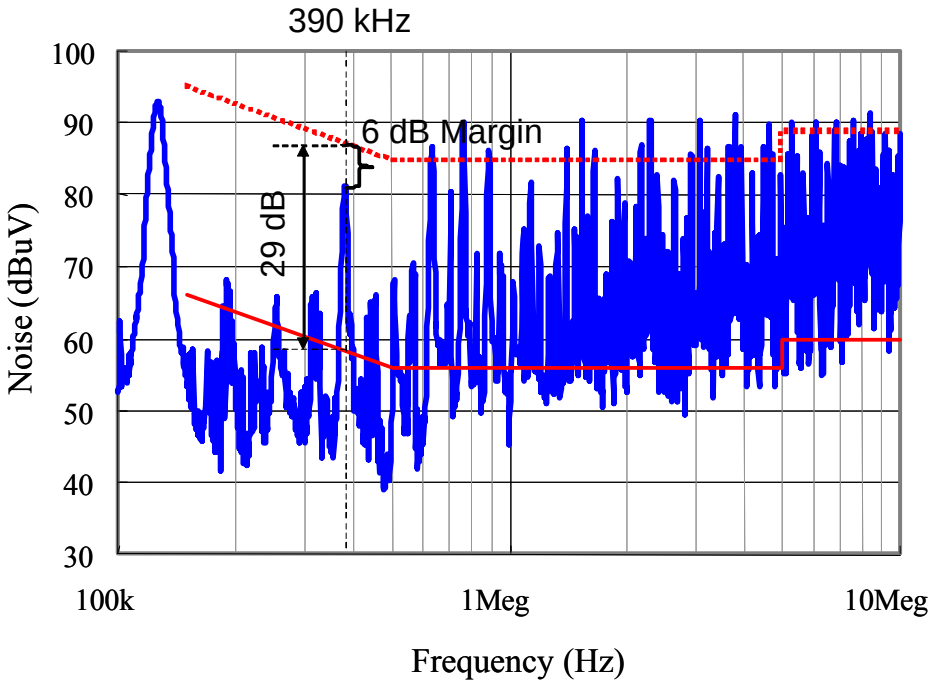


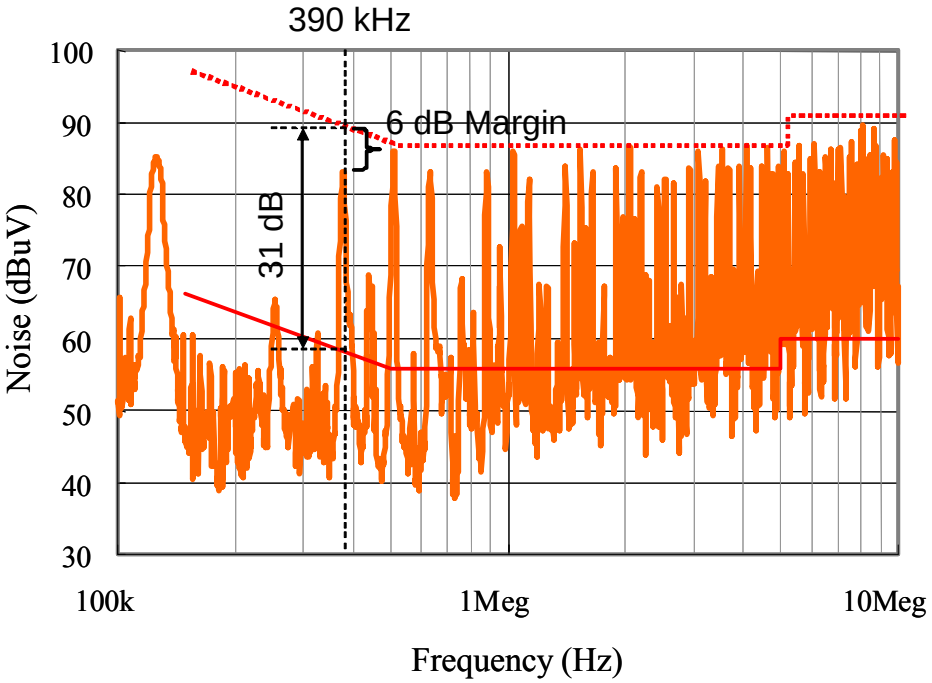
Figure 4.7. Relationship between the filter corner frequency and the switching frequency (DM filter).

By adopting phase angle control strategy, the penalty on the EMI filter design due to the phase shedding can be minimized, as shown in Figure 4.7. At light load condition, two channels are operating with 90 degrees phase shift to keep both high efficiency and small EMI filter size.

To meet the EMI standard, the filter will be designed based on the worst case, which is the 2-channel 90 degrees phase shift operation. As can be observed from Figure 4.7, the filter design criterion between 2-channel, 3-channel, and 4-channel operation is only slightly different. Thus, adopting such phase angle control strategy, the light load efficiency can be improved by phase shedding technique without compromising the EMI filter. This method also can be extended to other multi-channel PFC design with different switching frequencies and channel numbers.



(a) 3-channel π/3 phase shift



(b) 2-channel π/2 phase shift

Figure 4.8. Measured CM noise for phase shedding with phase angle control.

As for the CM noise, the above conclusions still can be applied. The measured CM noise for both 3-channel operation and 2-channel operation are shown in Figure 4.8 (a) and (b) respectively.

For 3-channel operation with 60 degrees phase shift, the 2nd noise peak is cancelled and the 3rd noise peak is reduced by 9.5 dBuV comparing with the single channel PFC case. For 2-channel operation with 90 degrees phase shift, the 2nd noise peak is also cancelled and the 3rd noise peak is reduced by 6.5 dBuV. The CM filter will be designed based on the worst case, which is the 2-channel 90 degrees phase shift operation. As can be observed, the filter design criterion between 2-channel and 3-channel operation is only slightly different. The impact on the CM filter design from phase shedding is also minimized.

According to the measured DM and CM noise, an EMI filter prototype for the 4-channel PFC with phase shedding and phase angle control is designed, as shown in Figure 4.9. Due to the low EMI noise, single-stage DM filter topology is chosen. One 10.8 uH DM inductor is implemented with T106-26A cores with 18 turns. Two 1 uF capacitors are used as the X capacitors. For the CM filter, two 10 nF capacitors are used as the Y capacitors. A 0.25 mH common mode inductor is implemented with ZW-42109TC core with 12 turns. Comparing with the filter prototype for the 4-channel PFC without phase angle control in Figure 4.5, about 50% volume reduction can be achieved by applying the proposed control strategy.

Figure 4.9. Filter prototype for the 4-channel PFC with phase shedding and phase angle control.

The above proposed adaptive channel management is implemented with digital control. The PFC output voltage and input current is controlled in the software using digital compensator sampling at the PWM switching frequency. The PWM units on the

TMS320F2808 controller support software synchronization and phase angle control. This allows dynamic re-adjustment of the phase angle of each channel. All the DM and CM noise measurement results are obtained from the same multi-channel PFC prototype. The efficiency curves are also measured from the same prototype.

4.4 Proposed Constant On-Time Controlled PFC and Its Issues

To further improve the light load efficiency, the Pulse Frequency Modulation (PFM) operation can be introduced to the PFC. This operation mode has be successfully implemented for DC-DC converter applications, and it is demonstrated the light load efficiency can be effectively improved.

For the DC-DC applications, constant on-time control is adopted to implement this PFM operation. Figure 4.10 shows how the inductor current changes with different loads for constant on-time control. When the load current is larger than critical current (I_{crit}), the buck converter works at CCM and the switching frequency is constant. When the load current is below I_{crit}, the buck converter works at DCM and keeps the same on-time for the control switch. The voltage gain at DCM can be easily derived:

$$M = \frac{2}{1+\sqrt{1+\frac{8 \cdot L}{R T_{on}{}^{2} f_s}}} \tag{4-1}$$

Where $M = V_o / V_{in}$, L is the output inductance, R is the load resistance, T_{on} is the on-time of control switch, and f_s is the switching frequency of the buck converter. If T_{on} is constant, the switching frequency should be inversely proportional to the load resistance to regulate the output voltage. This means that if the load current decreases, the switching frequency decreases correspondingly. Figure 4.10 shows that when the load current is half of I_{crit}, the switching period is doubled, which indicates that the switching frequency decreases by half.

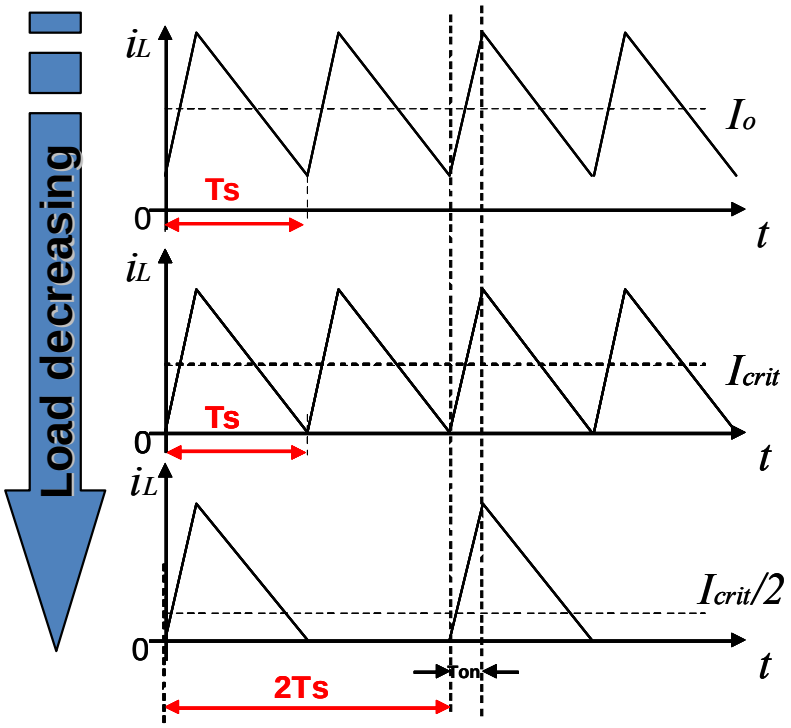


Figure 4.10. Inductor current waveforms for constant on-time control with different loads.

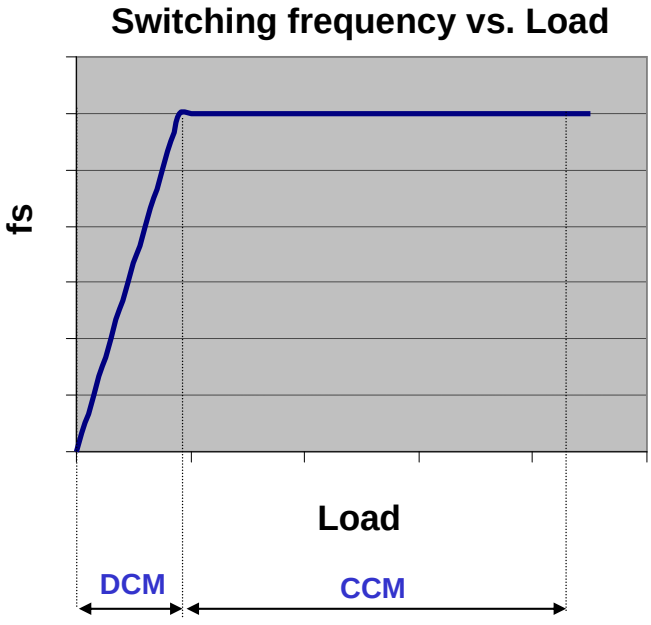


Figure 4.11. Constant on-time controlled buck converter with PFM operation.

The basic operation can be illustrated as Figure 4.11. At heavy load condition, the converter is operating at CCM with constant switching frequency. When the load is

decreased to certain critical point, the converter starts to operate at DCM. With constant on-time control, the switching frequency decreases with the load decreasing.

Average current mode control is one of the most popular techniques used to implement power factor correction. However, this control technique is normally implemented with constant switching frequency. It cannot achieve the desired operation mode. Other than average current mode control, peak current mode controlled PFC and constant frequency DCM PFC are also implemented with constant switching frequency operation. Critical Mode (CRM) PFC is a variable switching frequency control. However, the switching frequency increases with load decreasing.

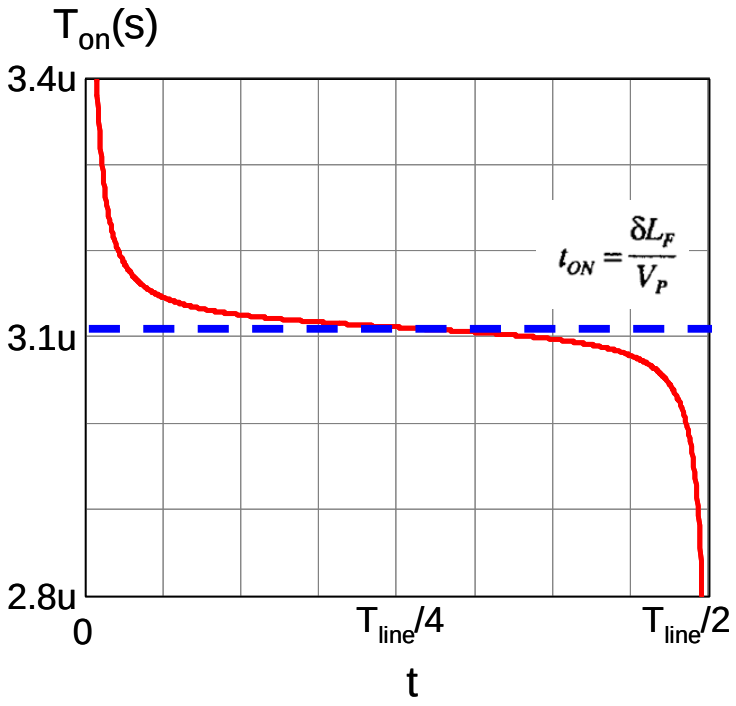


Figure 4.12. On-time of the variable-hysteresis controlled PFC.

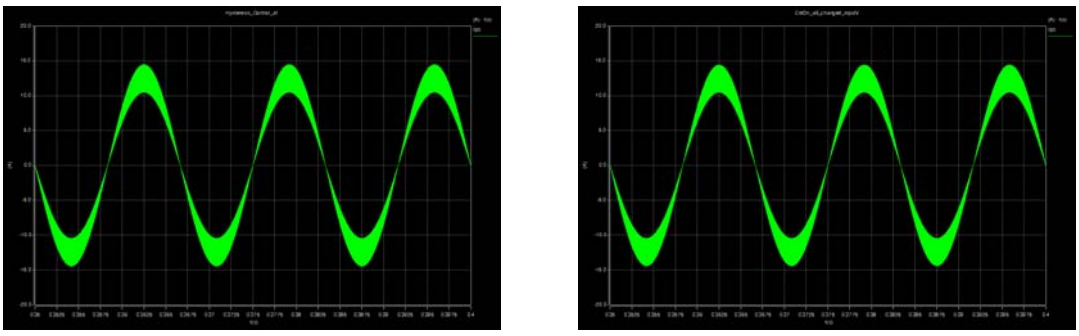
The variable-hysteresis control has been proposed for PFC circuit [58]. According to the study, the on time can be calculated as,

$$t_{ON} = \frac{\delta L_f}{V_P - \omega L_F I_P \cot(\omega t)} \tag{4-2}$$

The variation within half of the line cycle is shown in Figure 4.12. As can be observed, the on time is close to a constant value for most of the time. The large difference

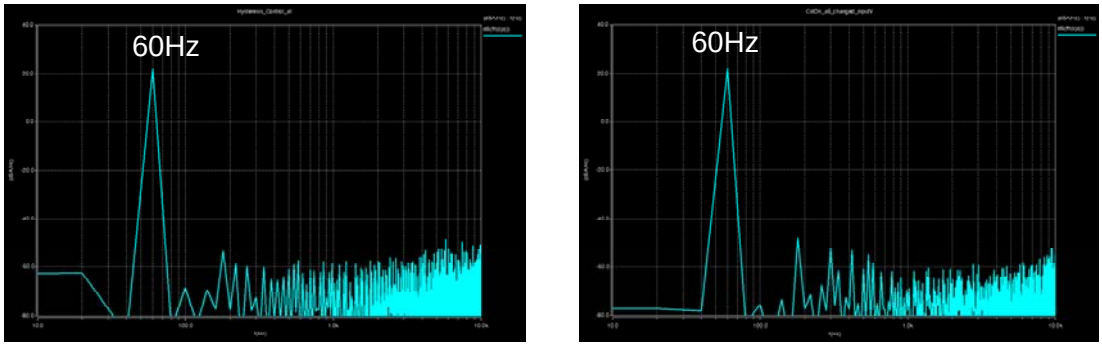
shows at the input current crossover portion, which normally has small impact to the whole circuit performance.

The PFC with the variable-hysteresis control and the constant on-time control is simulated in Saber. The input current waveforms are shown in Figure 4.13. The simulation results show the input current waveform of the constant on-time control is very close to the variable-hysteresis control. To further verify the difference impact on the PFC performance the frequency spectrum simulation results of the input current are shown in Figure 4.14. It also indicate that the constant on-time controlled PFC can achieve comparable performance as the variable-hysteresis control method.



(a) Variable-hysteresis control **(b) Constant on-time control**

Figure 4.13. Simulation results of input current.



(a) Variable-hysteresis control **(b) Constant on-time control**

Figure 4.14. Frequency spectrum simulation of input current.

To implement the constant on-time control, a control scheme shown in Figure 4.15 is proposed. This control scheme can achieve the desired functions when the circuit is operating in CCM and CRM operation.

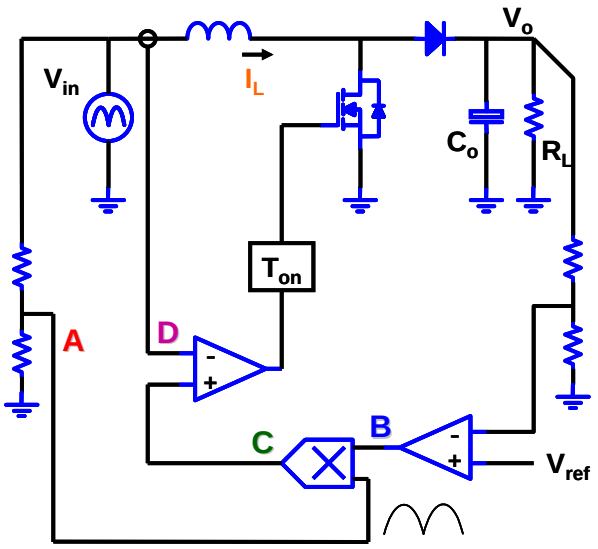


Figure 4.15. Control scheme for constant on-time controlled PFC.

The proposed control scheme cannot achieve PFM automatically. To solve this issue, an addition ramp is introduced in the control scheme. With the ramp, the switching frequency of the PFC decreases with load decreasing. However, another issue with this control scheme is the negative voltage is needed, which is undesirable from the control IC point of view. To solve that issue, a bias is added with the sensed inductor current. With the added bias, the controlled scheme can achieve PFM with single control power supply. The proposed final control scheme is shown in Figure 4.16.

The sinusoidal sensing signal of the input voltage multiplies with the voltage loop compensator output as the input current valley reference. When the switch is on, it will be turned-on for a constant time period. After it is turned off, the switch will turned on again when the inductor current touches the current bottom reference. This control scheme can achieve the desired functions when the circuit is operating in CCM and CRM operation. In DCM operation, the compensator output will be below zero. The additional ramp is introduced in the control scheme. The ramp is initiated at the moment the current touches zero. When the ramp reaches the zero level, the switch is turned on again. With the ramp, the switching frequency of the PFC decreases with load decreasing. The key waveforms of the constant on-time control in CCM and DCM are shown in Figure 4.17 (a) and (b), respectively.

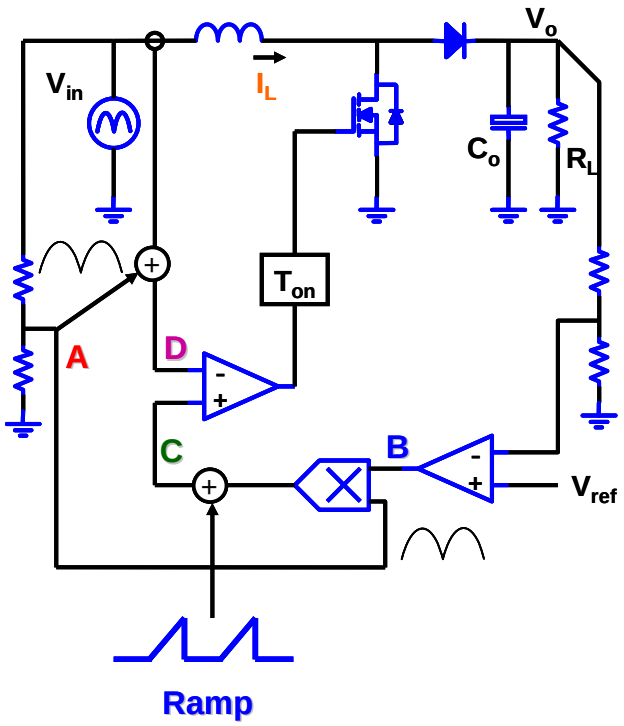
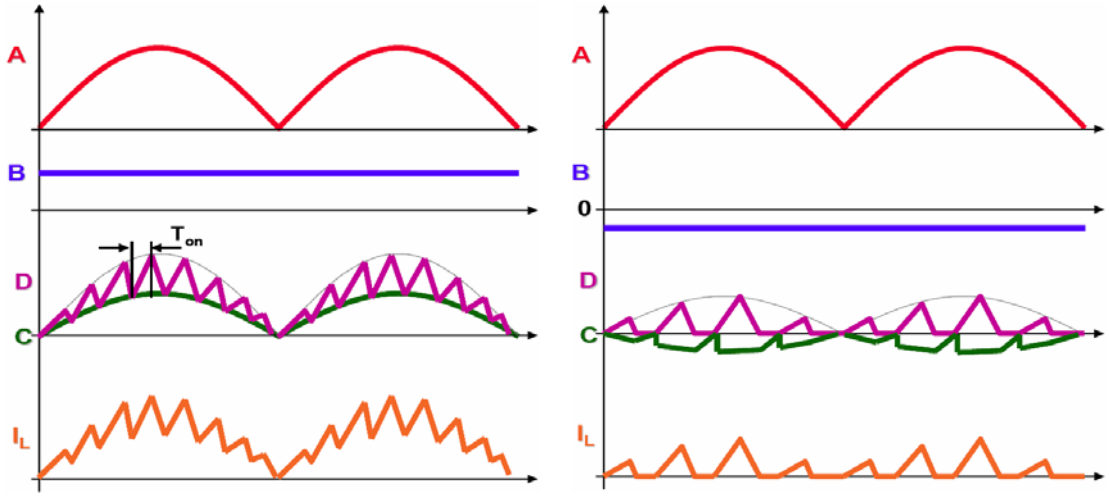


Figure 4.16. Control scheme for constant on-time controlled PFC with PFM operation.



(a) CCM **(b) DCM**

Figure 4.17. Key waveforms of the constant on-time control in CCM and DCM

The proposed control scheme is also built in a PFC saber model. The simulation results shown in Figure 4.18 verify the proposed scheme. The PFM for the PFC can be achieved.

The efficiencies of the constant on-time control PFC and the conventional constant frequency control PFC are measured on the same PFC prototype. The circuit parameters and the operating conditions are shown below.

Input voltage: V_{in_rms} = 90 V

Output voltage: V_o = 400 V

Boost inductance: L_b = 270 uH

Rated output power: P_o = 400 W

Switching frequency (constant frequency control): f_s = 130 kHz

On time (const-on control): T_{on} = 5.25 us

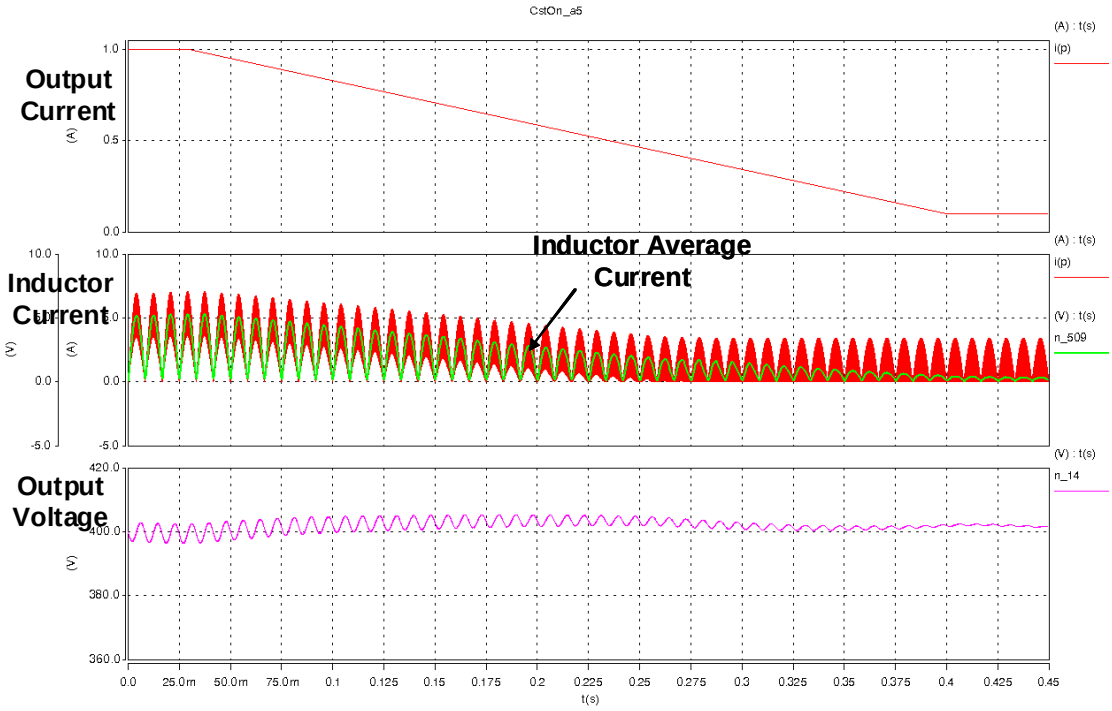


Figure 4.18. Simulation verification of the proposed constant on-time controlled PFC.

For the constant frequency control case, with the switching frequency of 130 kHz, the inductor current will reach its maximal value, 7.5 A, at low line, 90 Vrms input. To maintain the same peak current in constant on-time control case at low line, the T_{on} is chosen to be 5.25 us to fully utilize the inductor current capability.

The efficiency comparison of constant on-time control and constant frequency control is shown in Figure 4.19. As expected, light load efficiency improvement can be observed (4% improvement at 5% load). However, the efficiency of the constant on-time control PFC suffers from 20% load to full load.

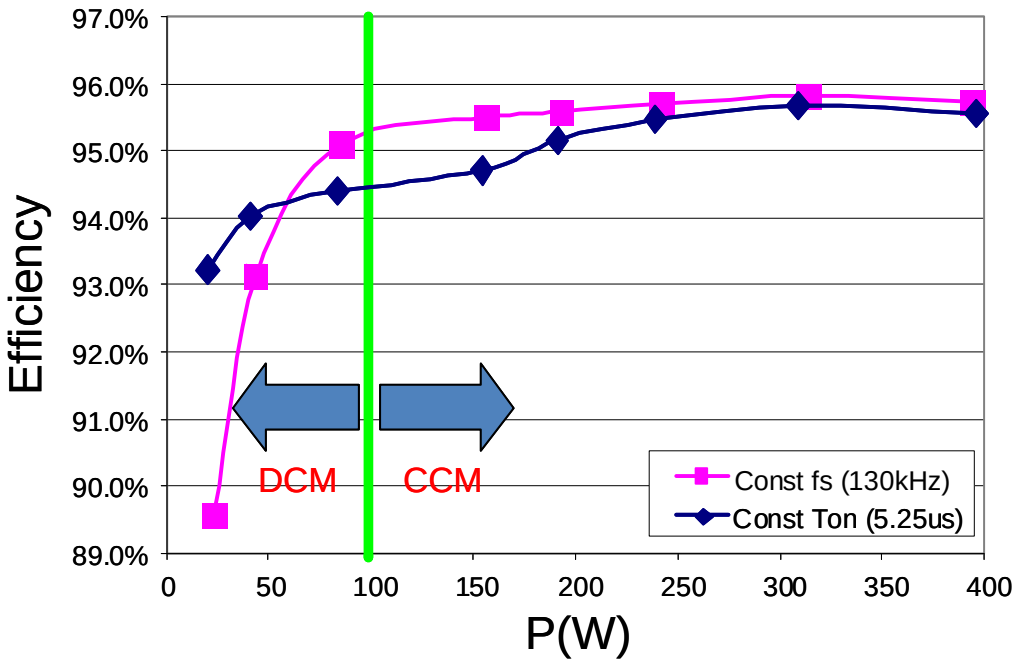


Figure 4.19. Efficiency comparison of constant on-time control and constant frequency control.

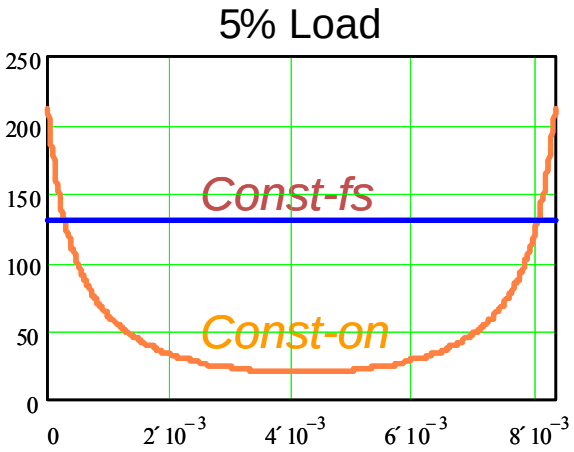
The switch on time of constant on-time control is a fixed value, while the on time of the constant frequency control can be expressed as equation (4-3) below,

$$t_{on} = \frac{v_o(t) - v_{in}(t)}{v_o(t) f_{const}} \tag{4-3}$$

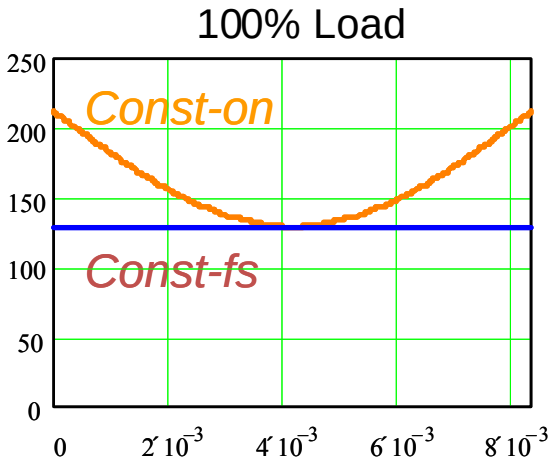
where $v_o(t)$ and $v_{in}(t)$ are the instantaneous value of output and input voltage, and the f_{const} is a constant switching frequency, which is 130 kHz in this case. The switching frequency of the constant frequency control is a fixed value, while the frequency of the constant on-time control in CCM can be expressed as equation (4-4) below,

$$f_{s\_CCM}(t) = \frac{v_o(t) - v_{in}(t)}{v_o(t) T_{on\_const}} \tag{4-4}$$

The switching frequency of both constant on-time control and constant frequency control at 5% and 100% load conditions are shown in Figure 4.20 (a) and (b) respectively.



(a) 5% load condition



(b) 100% load condition

Figure 4.20. Switching frequency for constant on-time control and constant frequency control.

The proposed constant on-time control PFC can reduce the switching frequency with load decreasing. At 5% load condition, the switching frequency is much low than the constant frequency control PFC for most part of the half line cycle. However, the constant on-time control PFC has higher switching frequency than the constant frequency control PFC in CCM. Higher switching frequency leads to higher switching related losses, so the efficiency suffers.

The constant on-time control PFC is essentially a variable switching frequency controlled PFC. The frequency modulation impacts on the EMI performance has been studied for lots of applications. It has been reported the benefit on the EMI filter design by modulate the switching frequency. However, the EMI benefit from frequency modulation

is largely depending on the EMI Standard. The EMI Standard EN55022B requires both the Quasi-Peak and the Average. The frequency modulation can greatly reduce average measurement results. However, the Quasi-Peak noise is maintained very high, due to the Quasi-Peak noise detector characteristic which is defined by the basic EMI Standard, CISPR 22. The EMI filter size is determine by the quasi-peak noise for the constant on-time control PFC.

The harmonic magnitudes of the noise source varies within half of the line cycle due to the duty cycle variation. In CCM, the harmonics magnitudes variation within half of the line cycle is shown in Figure 4.21. For the conventional constant frequency controlled PFC, all these harmonics stay at certain fixed frequencies. The meausrement results show the noise spikes at the corresponding frequencies. For the constant on-time controlled PFC, both the magnitudes and the frequencies of the harmonics vary within half of the line cycle. EMI measurement will show quite different results comparing with the constant switching frequency controlled PFC. The EMI noise will not constrate at certain frequenies any more, but spreaded into a frequency range instead, which is determined by the switching frequency range of the PFC, as shown in Figure 4.22.

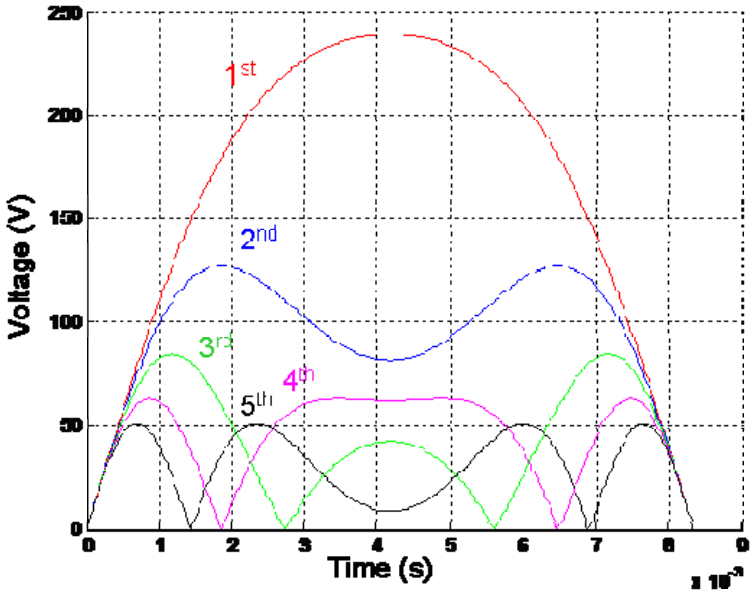


Figure 4.21. 1st to 5th order harmonics of the voltage noise source within half of the line cycle.

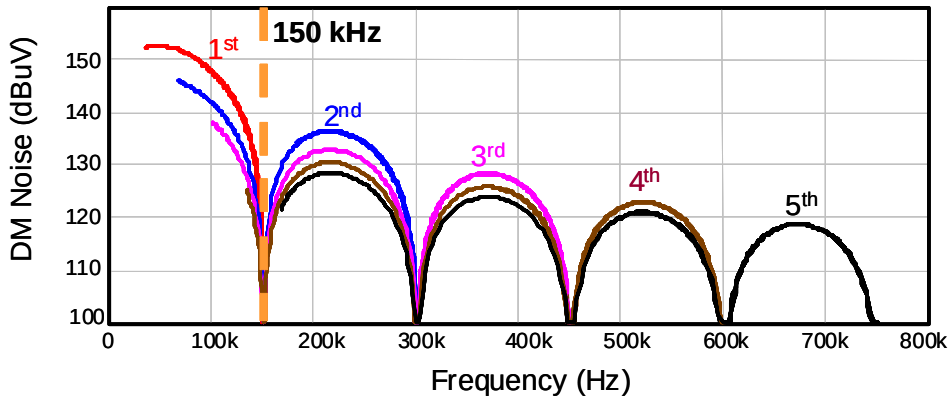


Figure 4.22. Predicted DM noise for constant on-time controlled PFC in CCM. (Vin = 220 Vrms)

At high line, due to the wide switching frequency range, the harmonics have a lot of over lappings. The valleies of the noise are caused by the duty cycle variation as shown in Figure 4.21. The over lappings could be greatly reduced at narrower switching frequency range conditions, such as low line case, as shown in Figure 4.23.

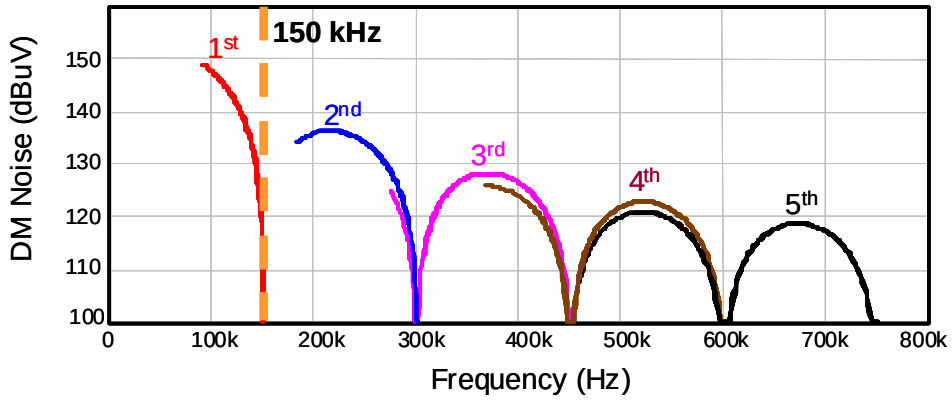


Figure 4.23. Predicted DM noise for constant on-time controlled PFC in CCM. (Vin = 110 Vrms)

With interleaving technique, harmonic cancellation still can apply for the constant on-time controlled PFC, however, the benefit on the EMI filter design is much less than the constant switching frequency controlled PFC. Cancelling certain order harmonic may only reduce the noise for several dBuV, since the higher order harmoincs still exist. Figure 4.24 shows the predicted DM noise for 2-channel interleaved constant on-time controlled PFC in CCM at high line. By cancelling all the even order harmoincs the noise magnidute only reduced by 3 dBuV. The filter design will be based on the 3rd order harmonic, which appears at the frequency range from 100 kHz to 450 kHz.

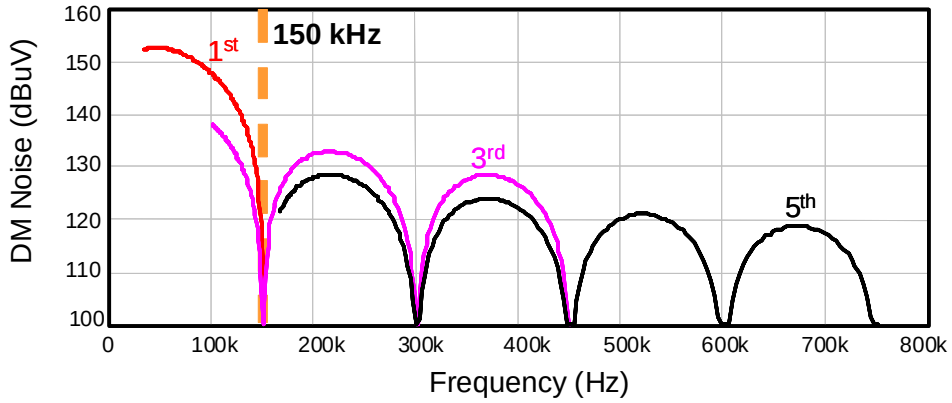


Figure 4.24. Predicted DM noise for 2-channel interleaved constant on-time controlled PFC in CCM. (Vin = 220 Vrms)

By controlling the on-time, the noise valley can be controlled, in CCM. However, the worst case for the EMI filter design for the constant on-time controlled PFC actually appears at DCM. High noise magnitude could appear at 150 kHz which demands the EMI filter most, as shown in Figure 4.25.

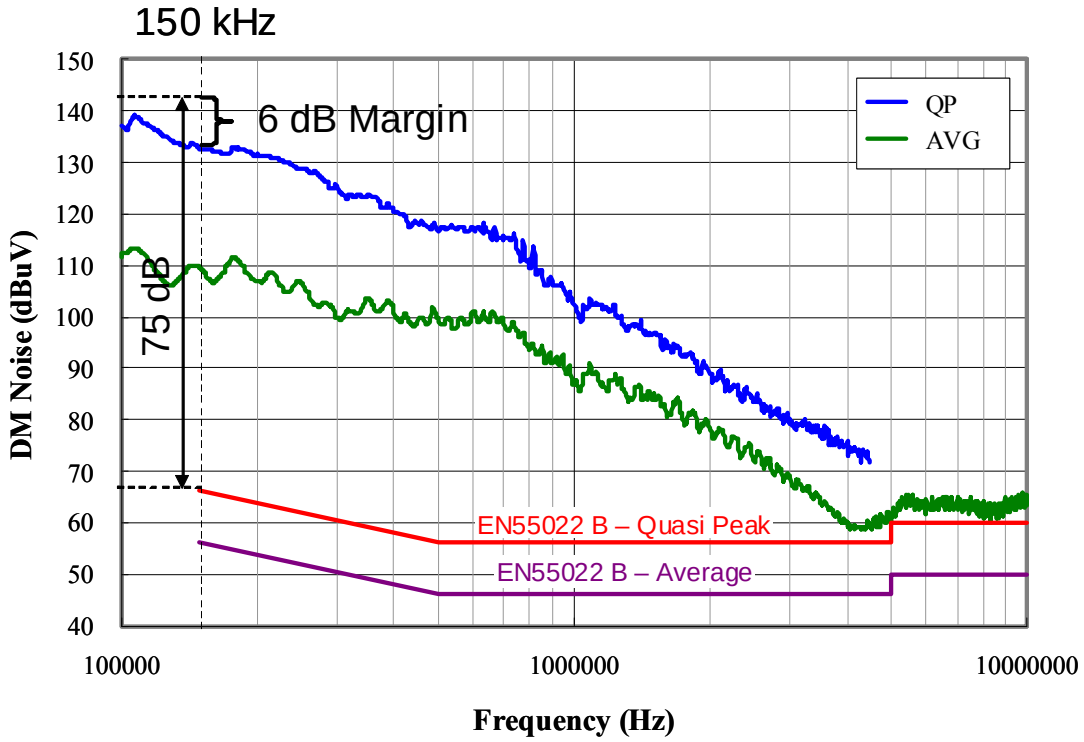


Figure 4.25. Measured Quasi-Peak and Average DM EMI noise for constant on-time control PFC (Vin = 110 V, Ton = 5.25us, Po = 100 W).

As shown in Figure 4.25, the measured Quasi-Peak and Average detection mode DM EMI noise, the frequency modulation can greatly reduce average measurement result. However, the Quasi-Peak noise is maintained very high, due to the Quasi-Peak noise detector characteristic which is defined by the basic EMI Standard, CISPR 22. Since the EMI Standard EN55022B requires both the Quasi-Peak and the Average, the EMI filter size is determine by the quasi-peak noise for the constant on-time control PFC. Thus, the filter should be designed to provide 75 dB attenuation at 150 kHz. This is almost as bad as the constant frequency PFC switching at slight higher that 75 kHz, a much undesired switching frequency design for constant frequency PFC. Based on this attenuation requirement, the corner frequency of the EMI filter is 28 kHz. A very large EMI filter will be needed since the corner frequency is relatively low comparing to the 55 kHz corner frequency for the phase shedding with phase angle control.

In summary, the constant on-time control PFC can greatly improve the light load efficiency as expected. However, the efficiency is lower comparing with the constant frequency PFC from 20% load to full load. In addition to that, larger EMI filter is needed due to the high quasi-peak noise at 150 kHz comparing with the constant frequency control PFC.

4.5 Proposed Adaptive Frequency Controlled PFC

According to the discussion above, the variable switching frequency can effectively improve the light load efficiency by reducing the switching frequency related power loss. However, it is unfavorable to the EMI filter design since the high quasi-peak noise magnitude shows up at 150 kHz. The reason for that is that the line and load combinations will always make the constant on-time control PFC switching at undesired frequency in terms of EMI filter design, such as 75 kHz, 50 kHz, ect. The undesired switching frequency will cause high quasi-peak EMI noise shows up at 150 kHz. Therefore, in the EMI performance aspect, the constant switching frequency is preferred since the switching frequency can be always chosen to be in certain desired range to benefit the EMI filter.

Combining the advantages of constant on-time control PFC and the constant frequency PFC, adaptive frequency controlled PFC is proposed to achieve both high light load efficiency and the small EMI filer design. As shown in Figure 4.26, after the load is decreased to certain level, the switching frequency is discretely reduced to lower switching frequencies. The switching frequency is programmed to change from 130 kHz to 65 kHz when the load decreased to certain condition. The PFC operates as any conventional constant frequency controlled PFC both before and after the switching frequency change.

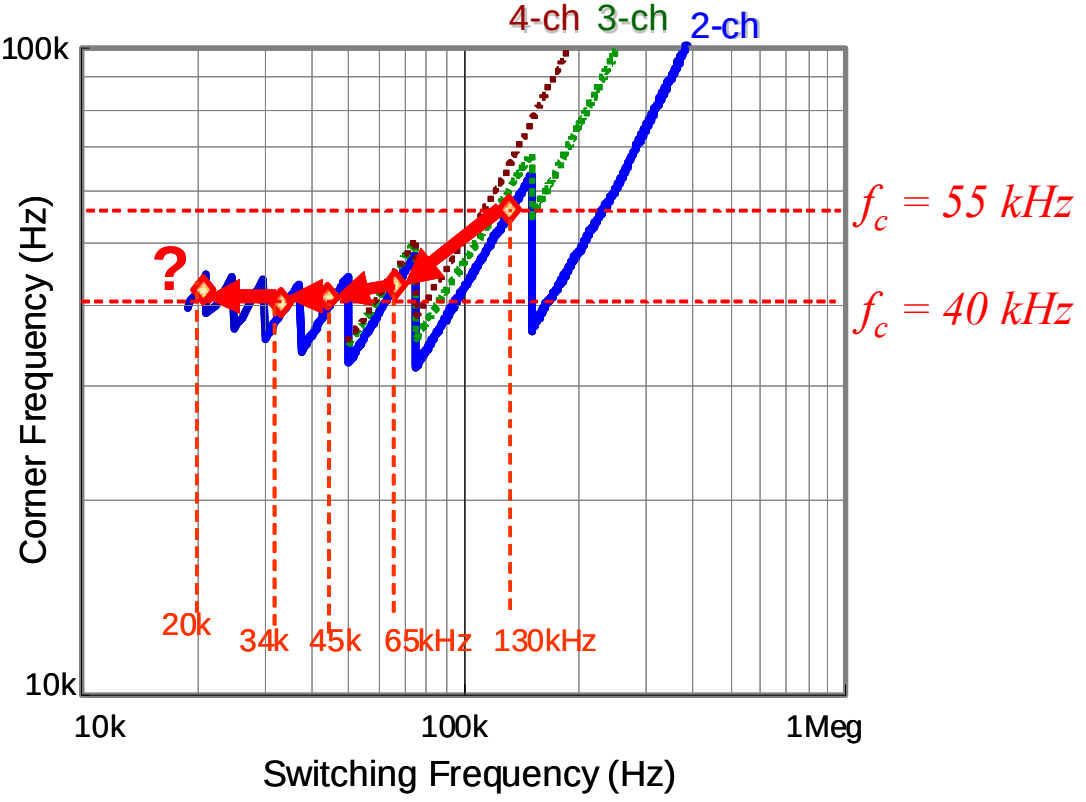


Figure 4.26. EMI filter corner frequency for the adaptive constant switching frequency control.

For 130 kHz switching, the phase angle between the active two channels is 90º so that the second order harmonic of switching frequency is cancelled and the filter is designed based on the reduced third order harmonic at 390 kHz. For 65 kHz switching, the phase angle between the active two channels is 60º so that the third order harmonic is cancelled and the filter is designed based on the reduced forth order harmonic at 260 kHz. The switching frequency is programmed to reduce to even lower range, such as 45 kHz ,34 kHz, 20 kHz, when the load further decrease and the phase angle is arranged accordingly.

Similar to the constant on-time control PFC, the proposed adaptive constant frequency PFC reduces the switching frequency with load decreasing, so that the light load efficiency can be improved. The difference is that the switching frequency reduces in a programmed discrete form. Based on the EMI consideration, only the desired switching frequencies are adopted when the switching frequency is reducing.

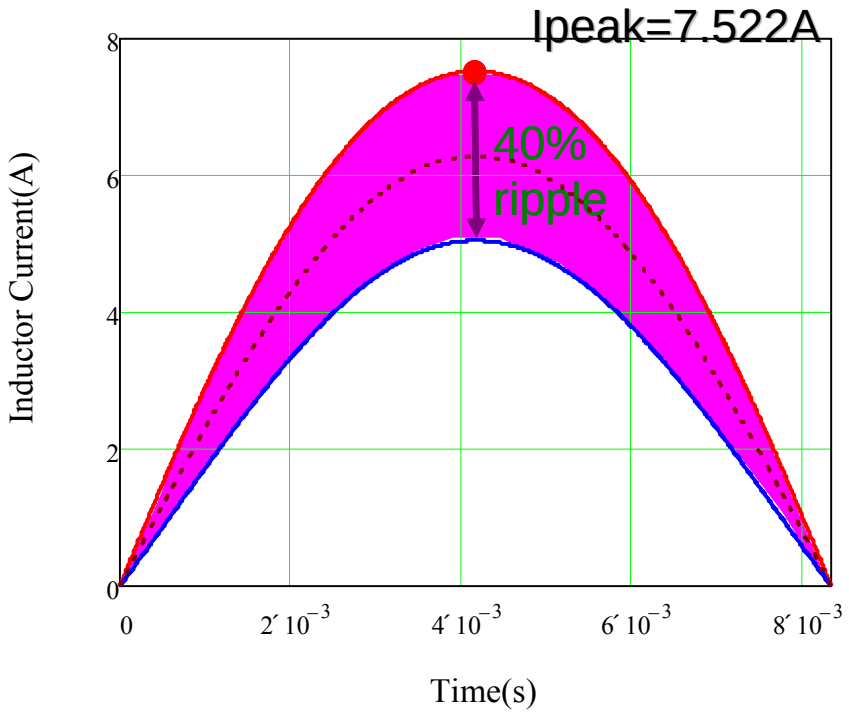


Figure 4.27. The inductor current waveform at Vin = 90 Vrms, full load condition.

Reducing the switching frequency results in higher inductor current ripple. Larger current ripple can saturate the core. So, it is a concern whether the adaptive constant frequency control will saturate the core or not. To verify the feasibility of the proposed control method, inductor designed for a 400 W, 130 kHz switching frequency is used as an example. In a 400 W, 130 kHz frequency PFC design, 270 uH inductor is needed to keep 40% ripple. Within all the combination of line voltage and load condition, the peak inductor current happens at the middle of half line cycle when Vin = 90 Vrms, full load, as shown in Figure 4.27. The inductor is designed to handle this peak current 7.5 A.

To avoid the saturation of the core, the maximum inductor current must be kept below this designed value when the switching frequency is decreasing. The peak inductor current is a function of load and line voltage, and can be derived and expressed as following.

$$I_{peak}(P_o, V_{in\_rms}) = \begin{cases} \sqrt{2}\dfrac{P_o}{V_{in\_rms}} + \dfrac{\sqrt{2}V_{in\_rms}}{2L_f f_s}\left(1 - \dfrac{\sqrt{2}V_{in\_rms}}{V_o}\right) & CCM \\ \sqrt{2}V_{in\_rms}\sqrt{\dfrac{2P_o\left(1 - \dfrac{\sqrt{2}V_{in\_rms}}{V_o}\right)}{L_f f_s V_{in\_rms}^{\,2}}} & DCM \end{cases} \tag{4-5}$$

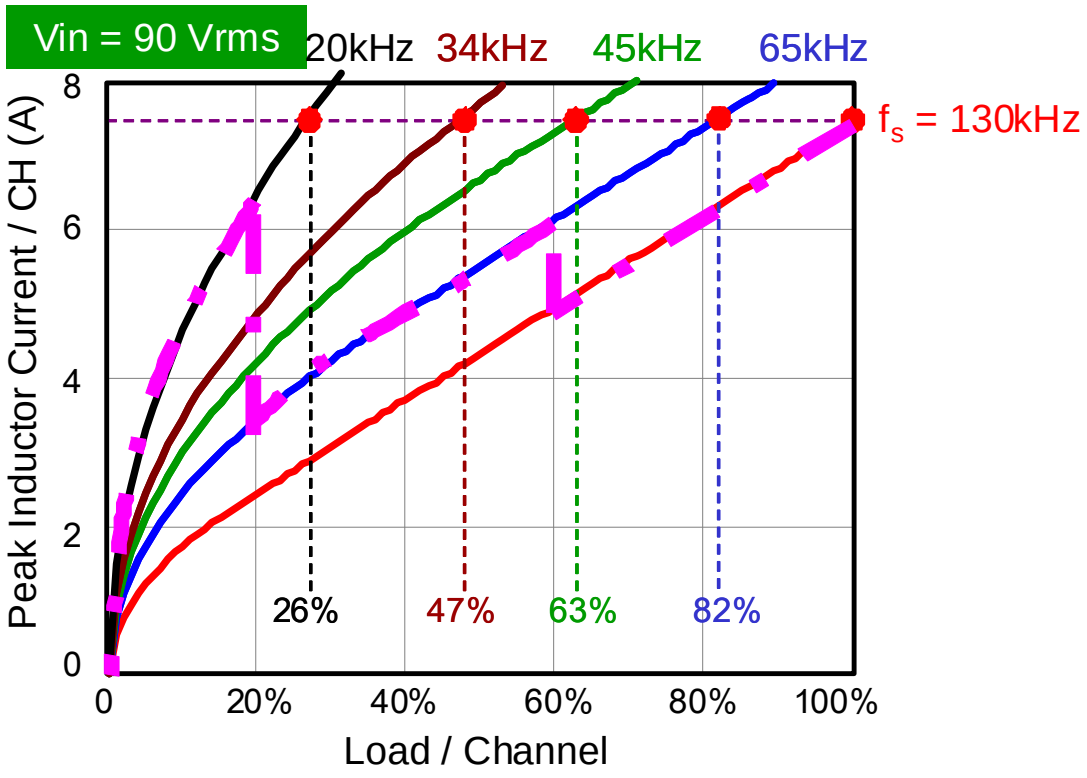


Figure 4.28. Inductor peak current as a function of load at Vin = 90 Vrms.

As a function of load for different switching frequency, the inductor peak current can be plotted in Figure 4.28 for 90 Vrms input line voltage. Keeping the inductor peak current below the designed value which happens at 130 kHz switching frequency, full load

condition, the critical load condition for each discrete switching frequency can be calculated. According to the calculation, the switching frequency can be reduced to 65 kHz without saturate the core when the load is decreased to 82% of the full load. It can be reduced to 45 kHz without saturate the core when the load is decreased to 63% of the full load and so on. These are the limitation of the switching frequency can be programmed for reducing. Following these limitation, the same inductor can be used with lower switching frequency at light load. The chosen adaptive frequency control strategy for low line input voltage is illustrated with pink line in Figure 4.28. The frequency switching point is determined based on the measured PFC efficiency.

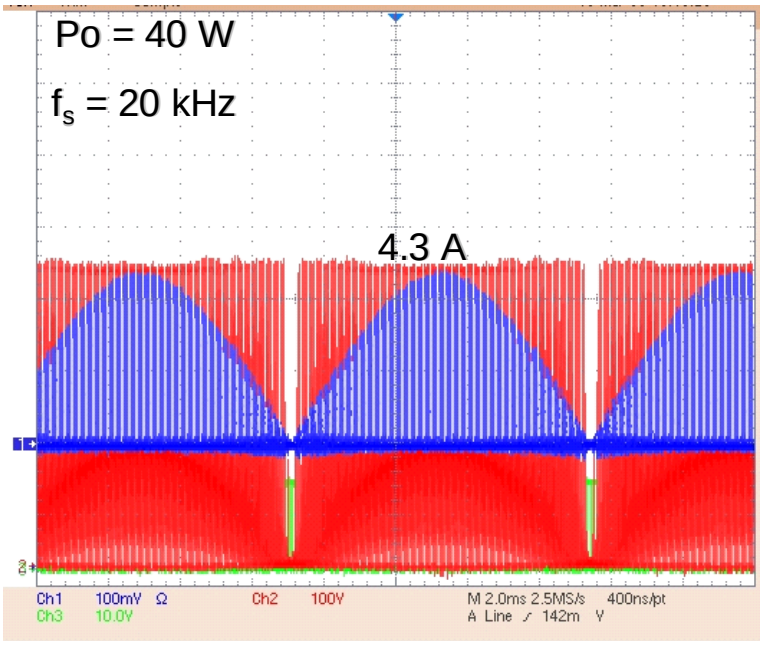


Figure 4.29. Experimental inductor current waveform with adaptive constant frequency control at light load condition.

Figure 4.29 shows the experimental inductor current waveform with adaptive constant frequency control at 10% load condition. Dropping the switching frequency from 130 kHz to 20 kHz as programmed, the peak inductor is 4.3 A which is smaller than the designed maximum inductor peak current, 7.5 A. The PFC can operate with 20 kHz at this load condition without saturate the core.

With the adaptive switching frequency control implemented, the light load efficiency can be further improved without any significant penalty on the EMI performance. As

shown in Figure 4.30, 2% efficiency improvement at 10% load, and 5.3% efficiency improvement at 5% load.

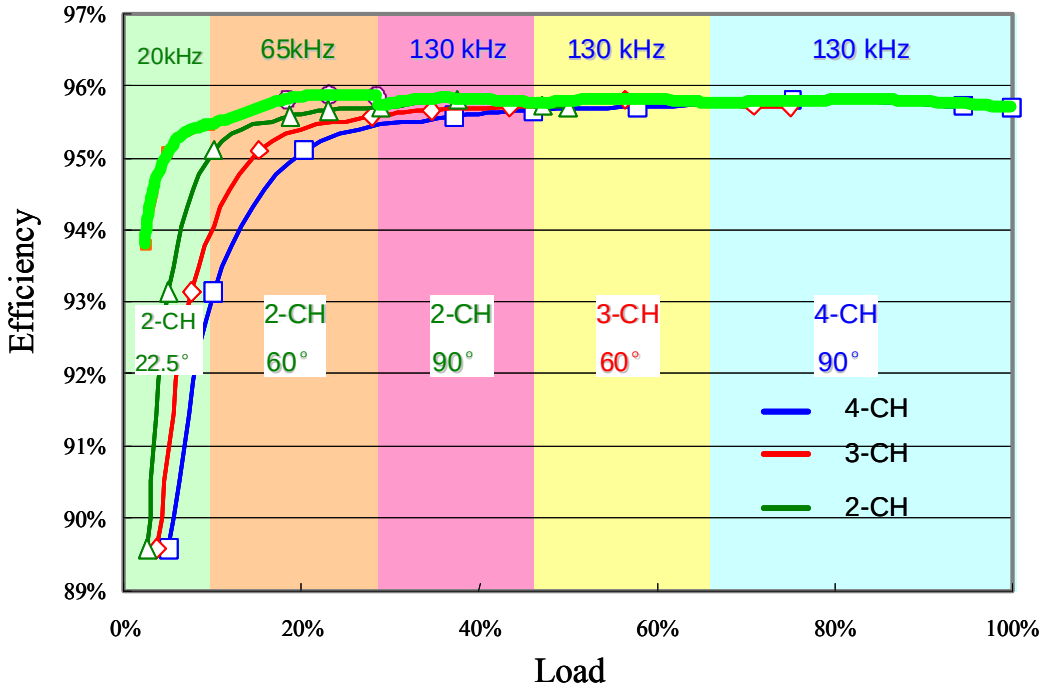


Figure 4.30. Measured 4-channel PFC efficiency with phase shedding and adaptive constant switching frequency control (Vin = 110 Vrms).

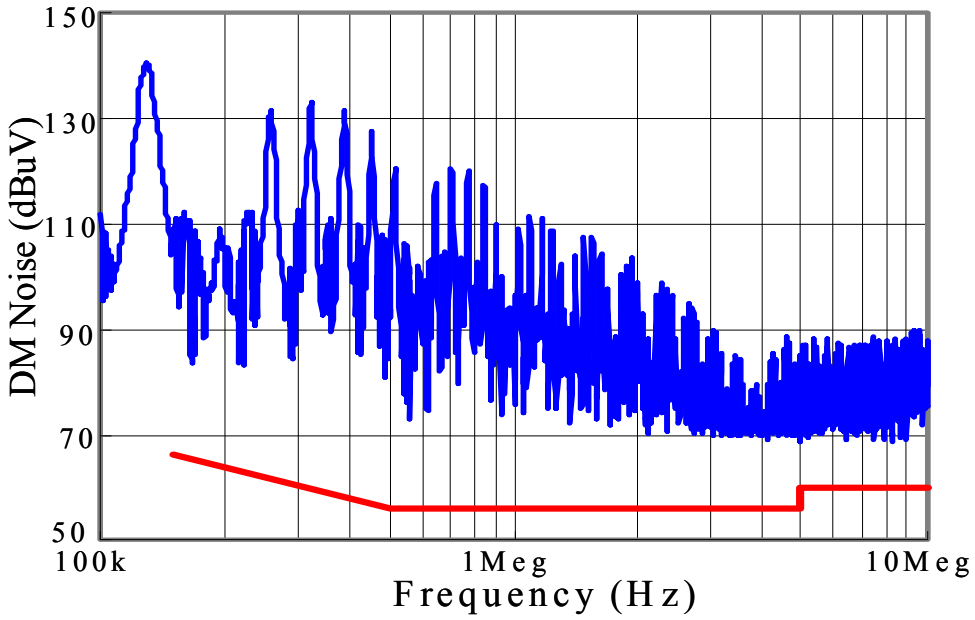


Figure 4.31. Measured DM noise with two channels operating at 65 kHz with 60º phase angle.

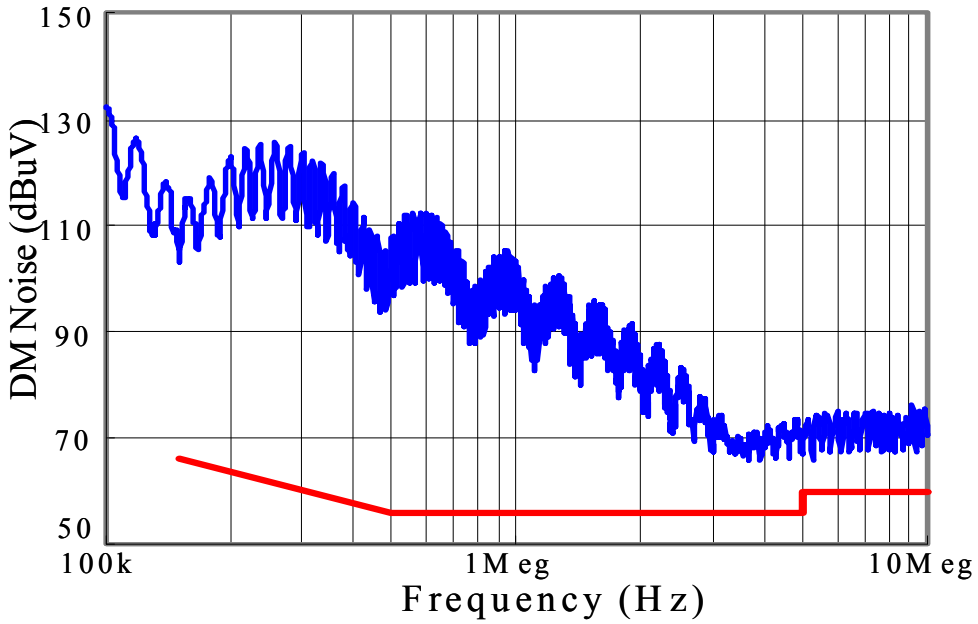


Figure 4.32. Measured DM noise with two channels operating at 20 kHz with 22.5º phase angle.

The measured DM noise with two channels operating at 65 kHz with 60º phase angle is shown in Figure 4.31. The measured DM noise with two channels operating at 20 kHz with 22.5º phase angle is shown in Figure 4.32. By discretely change the switching frequency and control the phase shift angle accordingly, the DM filter corner frequency is kept higher than 43 kHz as predicted.

4.6 Digital Controlled PFC with Light Load Efficiency Improvement Strategies

As discussed above, both the phase-shedding and adaptive constant switching frequency control can improve the PFC light load efficiency. These two control strategies can be combined and realized with digital controlled PFC. The digital controlled multi-channel PFC implementation has been discussed in the previous chapter. Based on that control implementation, the light load efficiency improvement strategies can be integrated into that control implementation.

The desired PFC light load efficiency control strategies are shown in Figure 4.30. From full load to 65% load, the PFC is operating with four channels active and 90º phase shift between the channels. When the load decreased into the range of 45% ~ 65%, the PFC is operating with three channels active and 60º phase shift between the channels. From 45% to 28% load, the PFC is operating with two channels active and 90º phase shift between the channels. Phase shedding control strategy is used from full load to 28% load.

When the load decreased into the range of 10% ~ 28%, the PFC operating frequency is reduced to 65 kHz and phase shift angle changed to 60º between the channels. When the load is below 10%, the switching frequency is reduced to 20 kHz and phase shift angle changed to 22.5º between the channels. The adaptive switching frequency control is used when the load is below 28%.

To implement the light load efficiency improvement strategies, the load condition needs to be known for the control. Thus, output power sensing is needed.

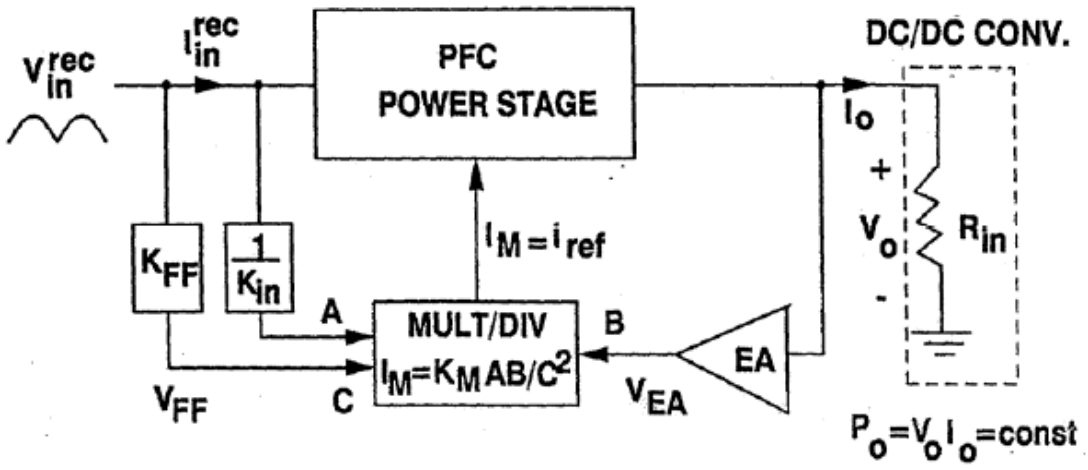


Figure 4.33. PFC control diagram.

Figure 4.33 shows the typical PFC analog control diagram. As discussed in the previous chapter, the digital implementation is just mimicking the analog control. All the control variables can be found in the digital control implementation correspondingly. According to Figure 4.33,

$$\begin{cases} A = \dfrac{V_{in}^{rec}}{K_{in}} \\ B = V_{EA} \\ C = K_{FF} V_{in}^{rec} \end{cases} \tag{4-6}$$

The current command for the current loop can be expressed as,

$$I_M = K_M \frac{AB}{C^2} = K_M \frac{\dfrac{V_{in}^{rec}}{K_{in}} \cdot V_{EA}}{K_{FF}^{\ 2} V_{in}^{rec^2}} = \frac{K_M}{K_{FF}^{\ 2} K_{in}} \frac{1}{V_{in}^{rec}} V_{EA} \tag{4-7}$$

Assume the inductor current can be controlled to follow the current command, which is normally valid for the PFC; the PFC input power can be obtained.

$$P_{in} = V_{in}^{rec} I_{in}^{rec} = V_{in}^{rec} I_M = \frac{K_M}{K_{FF}^{\ 2} K_{in}} V_{EA} \tag{4-8}$$

Where K_M, K_{FF}, and K_{in} are all constant. According to Equation (4-8) V_{EA} is proportional to the input power.

$$P_{in} = K V_{EA} \tag{4-9}$$

The load, which determines the output power, is almost equal to the input power when the PFC efficiency is high. Therefore, V_{EA} is proportional to the load.

V_{EA} is a calculated value in the digital control. It is the output of the voltage PI controller. To the digital control implementation, it is a known variable. It can be used to compare with the critical load point in Figure 4.30, and to program the light load efficiency improvement strategies accordingly. The block diagram of PFC software algorithm with power management is shown in Figure 4.34. The power management functions include phase shedding, phase angle control, and adaptive switching frequency control. The input of the module is the output of the voltage controller, V_{EA}.

The flow chart of ADC interrupt program with light load efficiency improvement strategies is shown in Figure 4.35. In this flow chart, the V_{EA}, the output of the voltage loop PI controller, is used as an indication of the load conditions. After it is obtained from the voltage loop PI controller, it is compared with the predetermined values, V_{EA1}, V_{EA2}, V_{EA3}, and V_{EA4}, which are corresponding to 65%, 45%, 28%, and 10% load conditions. The

comparison results will define the light load mode. Each light load mode is corresponding to one PFC operating mode, including the active channel number and the switching frequency. After that, the light load mode is compared with the current light load mode the program is using. The ePWM modules and the PI compensator parameters are reconfigured accordingly when mode change is detected.

The ePWM modules reconfiguration will define the active channel number, the switching frequency, and the phase shift angle. The PI compensator parameters also are reconfigured accordingly when the channel number or the switching frequency is changed. Beyond this point, the rest of the flow chart is the same as the one discussed in the previous chapter.

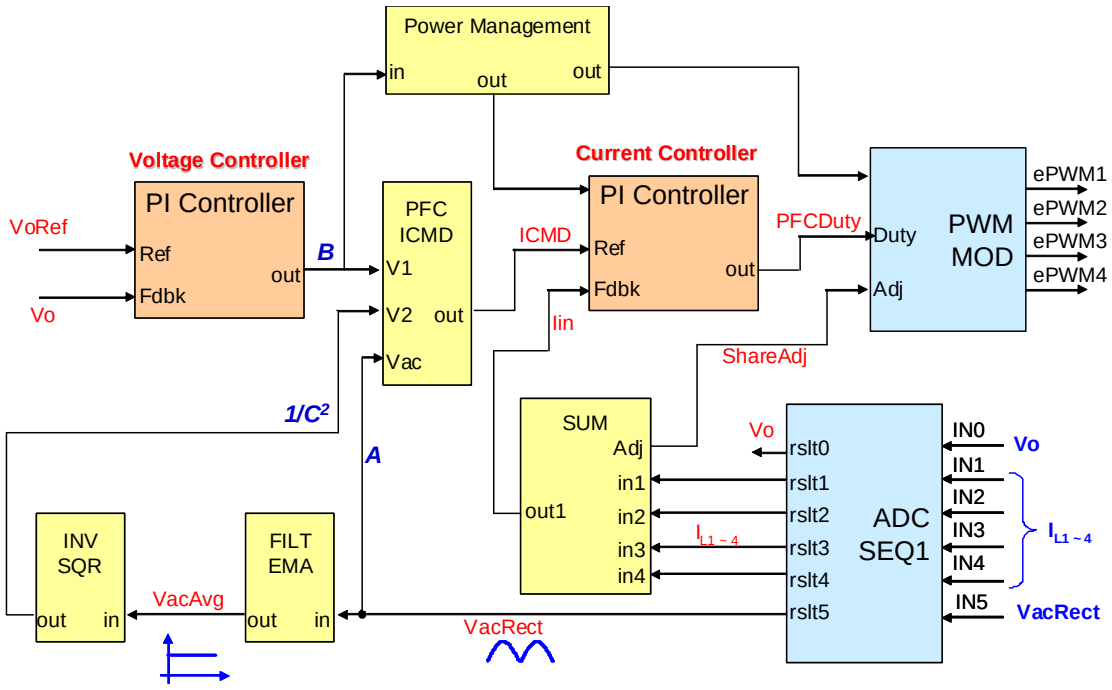


Figure 4.34. Block diagram of PFC software algorithm with power management.

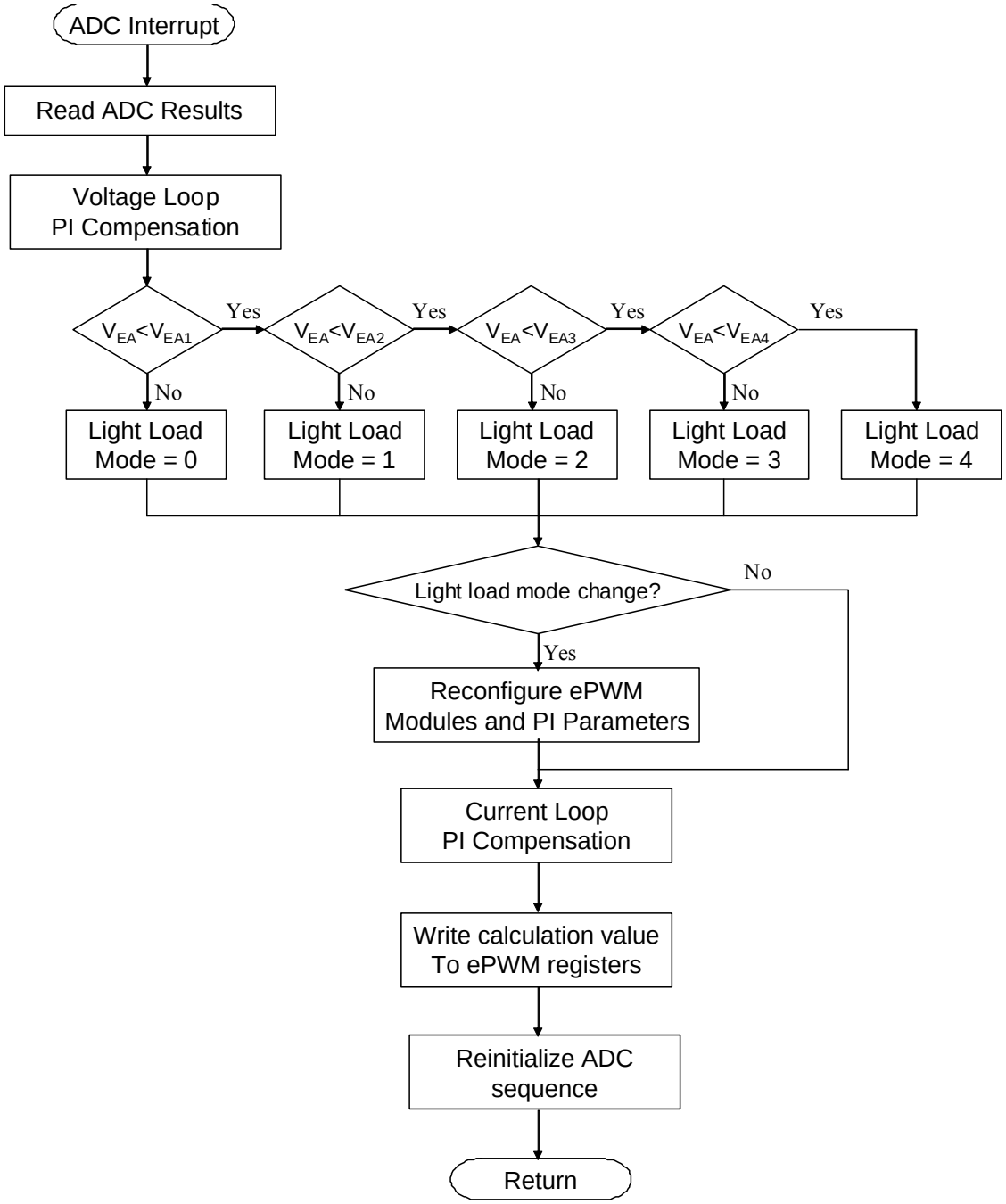


Figure 4.35. Flowchart of ADC interrupt program with light load efficiency improvement strategies.

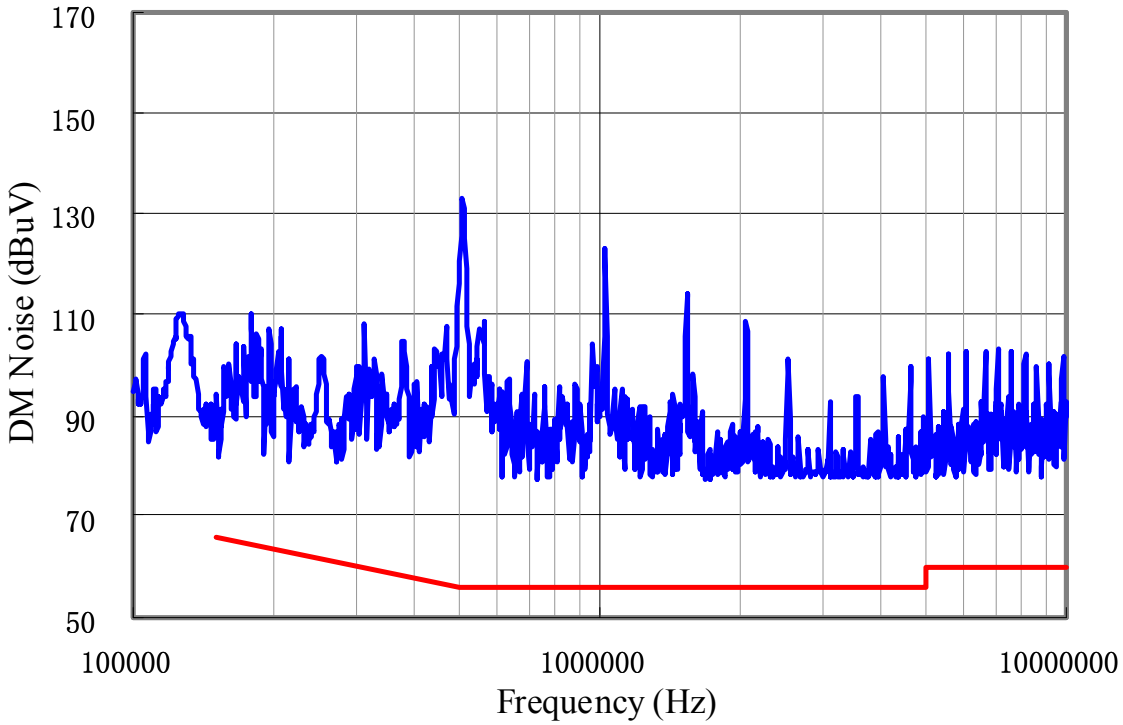


Figure 4.36. Measured DM noise of four channels operating with 90° phase angle.

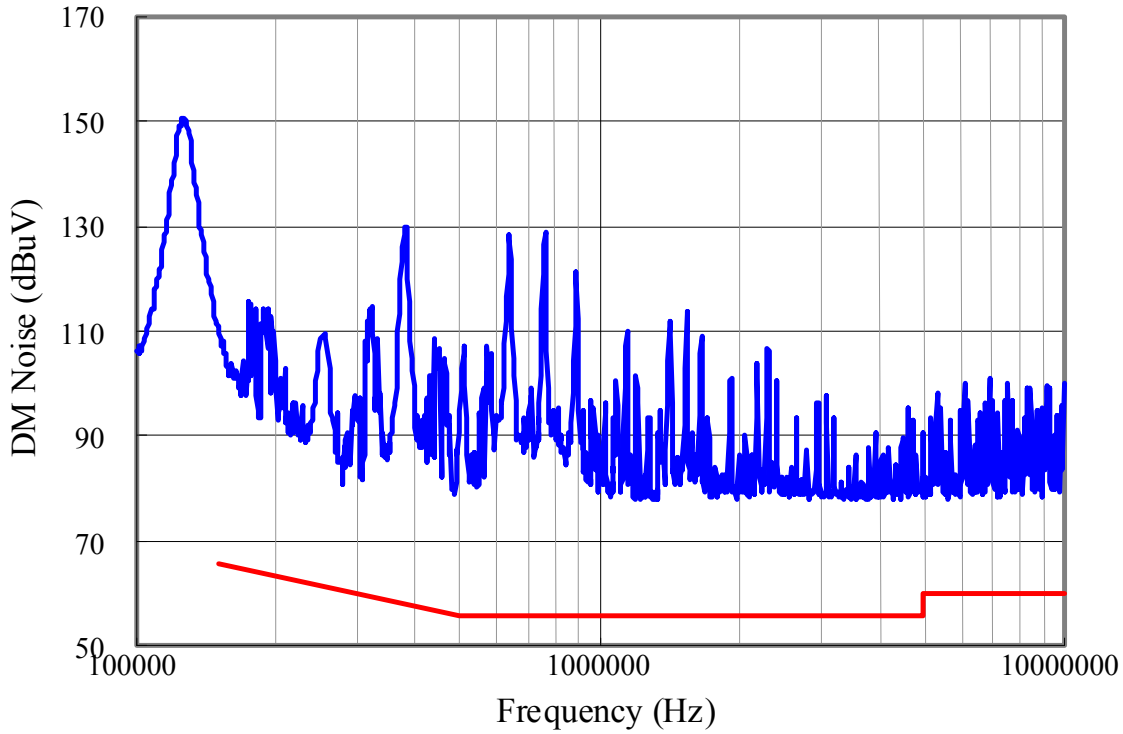


Figure 4.37. Measured DM noise of three channels operating with 60° phase angle.

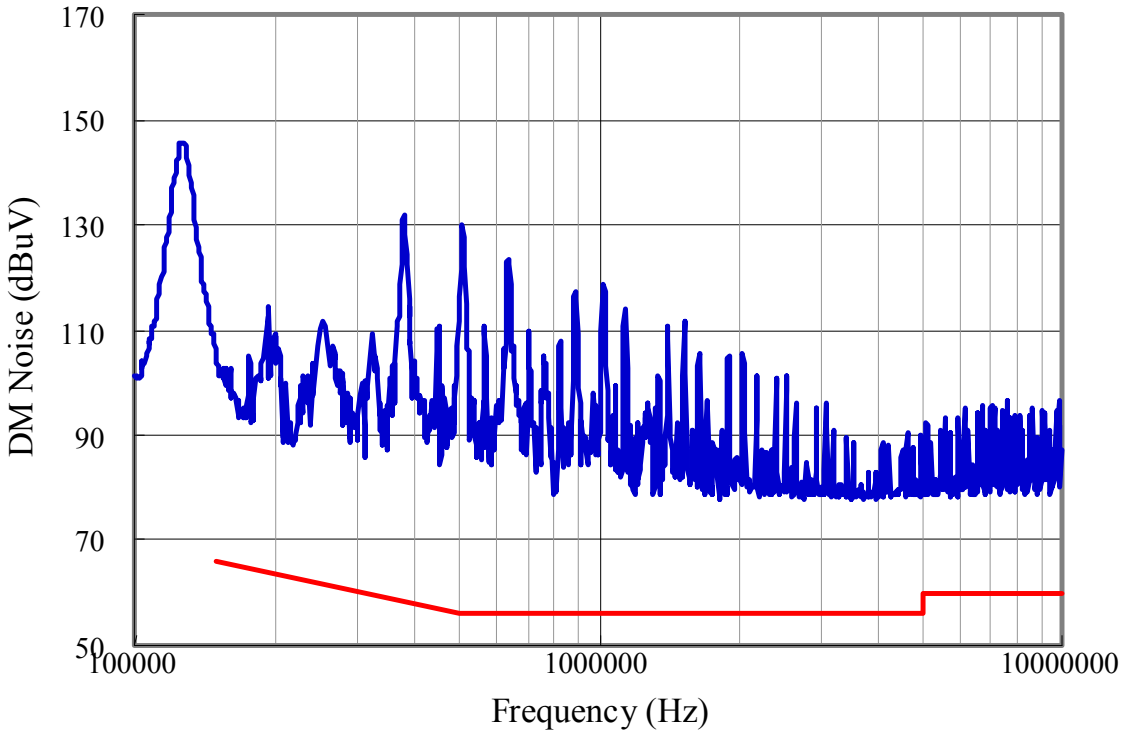


Figure 4.38. Measured DM noise of two channels operating with 90º phase angle.

With the proposed power management, the measured DM noise of four channels operating at 130 kHz with 90º phase angle is shown in Figure 4.26. The measured DM noise of three channels operating at 130 kHz with 60º phase angle and two channels operation with 90º phase shift angel is shown in Figure 4.37 and Figure 4.38 respectively. The measured DM noise with lower switching frequencies are shown in the previous section.

4.7 Summary

Today, the power supply industry is more focusing on improving the PFC light efficiency due to the economic reasons and environmental concerns. The interleaving multi-channel configuration makes it possible to implement the phase-shedding to improve the PFC light load efficiency. By decreasing the number of active channels according to the load, the PFC light load efficiency can be optimized. However, shedding phases can reduce the ripple cancellation effect as well, which will result in the EMI noise increase and losing the benefit on the EMI filter.

By applying the proposed phase-shedding with phase angle control strategy, the phase shedding impact on the EMI filter design can be minimized. The light load efficiency can be improved without compromising the EMI filter size, and is verified and demonstrated by the experimental results.

To reduce the switching loss at light load condition, constant on-time control with pulse skipping mode has been successfully used in various POL applications, and substantial efficiency improvement has been demonstrated. The constant on-time control concept is extended to the PFC application. However, after a careful study, although constant on-time controlled PFC can improve the efficiency at light load, the EMI filter size may need to increase to meet the standard due to the wide switching frequency range.

Since the issue is majorly caused by the wide switching frequency range, an adaptive frequency controlled PFC is further proposed to improve the EMI performance at light load. By using the proposed method, the light load efficiency can be improved with much less penalty on the EMI filter.

The proposed light load efficiency improvement strategies are combined and implemented on the platform of the digital controlled 4-channel PFC. The benefit of improving the light load efficiency is experimentally verified. The EMI performance is also evaluated based on the EMI measurement results obtained from the PFC prototype.

Chapter 5. Extension of Interleaved Boost Converter for Other Applications

5.1 Battery Charger / Discharger Applications

Batteries are widely used as the energy storage component for mobile applications. The battery charger/discharger is normally needed as the interface between the equipment and the battery. The boost converter is one of the simplest and most widely used topologies for the battery charger/discharger converter when isolation is not required. For example, the boost converter is used as the battery charger/discharger in the Hybrid Electric Vehicles (HEVs) applications.

5.1.1 Introduction

With the more stringent regulations on emissions and fuel economy, global warming, and constraints on energy resources, the electric, hybrid, and fuel cell vehicles have attracted more and more attention by automakers, governments, and customers [59]. Among these technologies, hybrid electric vehicle (HEV) traction is the most promising technology that has the advantages of high performance, high fuel efficiency, low emissions, and long operating range. Moreover, the technologies of all the component hardware are technically and markedly available. At present, almost all the major automotive manufacturers are developing hybrid electric vehicles, and some of them have marketed their productions, such as Toyota and Honda [60].

Compared to conventional vehicles, hybrid electric vehicles use two power sources to power the vehicle. Mostly, one power source is the internal combustion (IC) engine (gasoline or diesel fueled) and the other power source is the battery plus electric motor drives. In HEVs, high peak power and quick power response of the electric traction system is important since it will impact the vehicle performance such as quick acceleration. Several factors, including small internal combustion engine, optimal operating points, and regenerative braking result in much better fuel economy and lower emissions than

conventional vehicles which are powered by IC engine alone. High energy density of petroleum fuel and convenient fueling systems result in long operating range and easy refueling. All these advantages make HEVs the most promising alternatives for the next generation vehicle. As a result the hybrid vehicle market is growing rapidly recently [61].

The big difference between the HEVs and the conventional vehicles is that the HEVs have the second power source, the battery plus electric motor drives. This second power source includes battery, motors and lots of power electronics. All the power electronics part in this second power source is called the Power Control Unit (PCU). Today, a typical PCU consists of a boost converter and two inverters controlling each one of the two motor/generators (MGs). Figure 5.1 shows a typical schematic of a PCU main circuit.

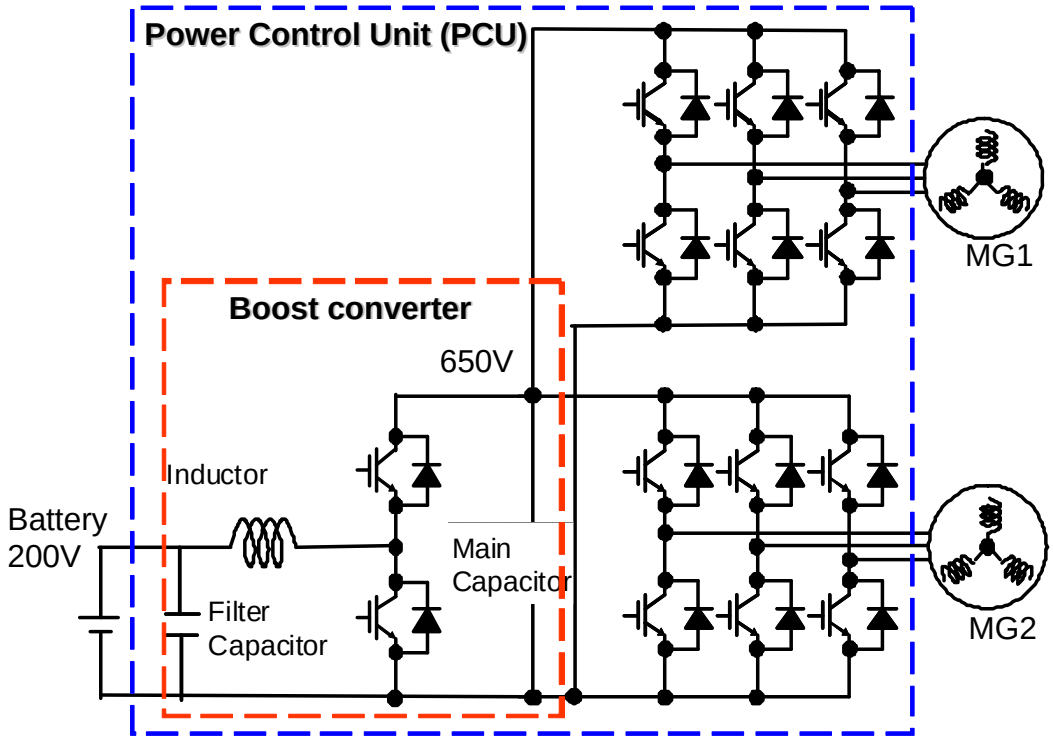


Figure 5.1. Sechmatic of the Power Control Unit (PCU) [59].

In the PCU the boost converter serves as a battery charger/discharger converter. It consists of two capacitors and one inductor for the passive components, and two Insulated-Gated Bipolar Transistors (IGBTs) and two Free Wheeling Diodes (FWDs) for the active components.

The boost converter provides a bus voltage significantly higher than the battery voltage to achieve a higher power output from the propulsion motor. With the high output voltage from the boost converter the motor power was increased to 1.5 times higher [63]. The output power of the boost converter is roughly 20-30 kW [62].

When converting an existing gasoline-powered vehicle design into a hybrid version, the space available in the engine compartment is usually very limited for the additional component, the PCU. So it is imperative for the inverters and converters of the PCU to have a small physical size and weight so that they can fit into the limited space available in the vehicle. With the rapidly growing hybrid vehicle market and the needs from the customers, the carmakers are expanding their lineup of hybrid vehicles from the compact size to the full-size or Sport Utility Vehicles (SUVs). It requires the PCU to have higher output power to propel heavier vehicles, yet still be able to fit into the limited engine compartment. All these factors result in a need for higher output power per volume, or higher power density. As shown in Figure 5.2, the relative power density of the PCU, the density has already been improved about 5 times within 4 years, and it is going to continuously increase.

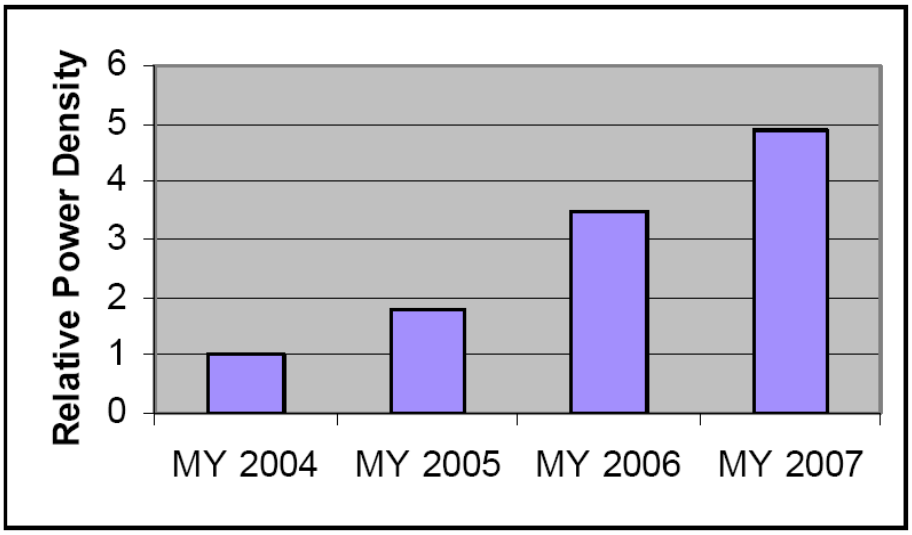


Figure 5.2. Toyota Hybrid Power Control Unit Relative Power Density Increase, 2004-2007 [61][64].

Improving the power density of the boost converter to meet the future needs is one of the focus of the PCU design. Although the converter looks simple, it consists of several

large passive components and active components. One of the major focus of this study is to investigate topologies to improve the power density and efficiency of the boost converter.

Figure 5.3 shows the available hybrid vehicals from Toyota and Lexus. For available models, the engine power varias from 134 horse power to 438 horse power. It would be time consuming and high cost to design the power control unit for each model. Modularized power control unit could be very desirable in such situation. It makes the power scalable to the engine power requirement.

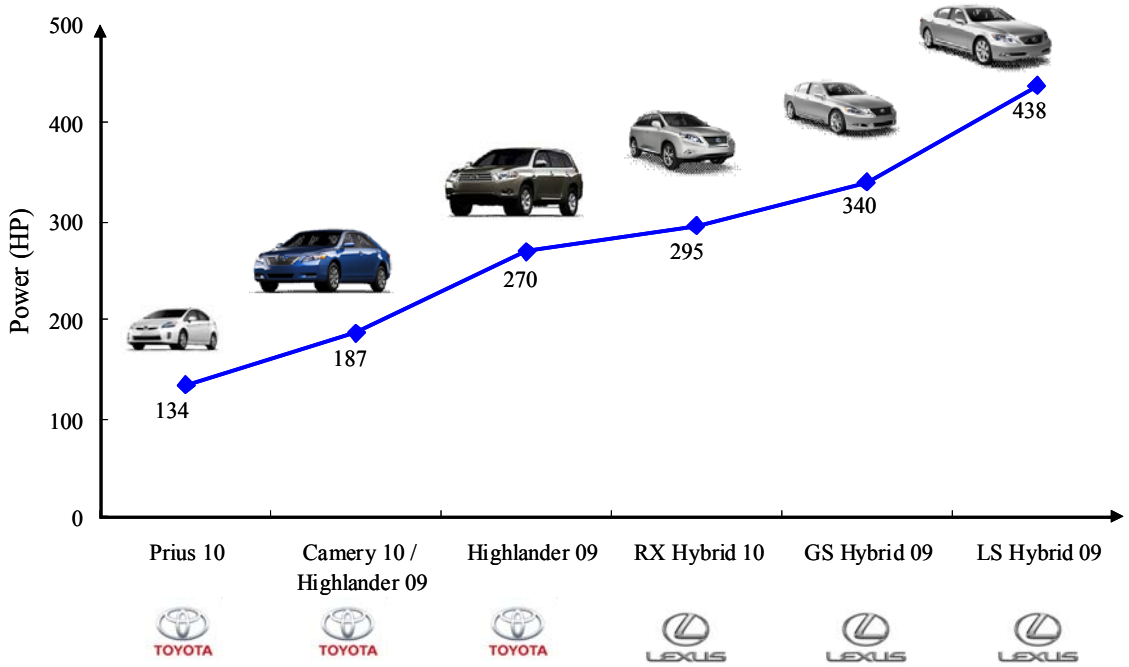


Figure 5.3. Engine power of Toyota and Lexus hybrid vehicles.

5.1.2 Benchmark Converter – Single-Channel Boost Converter

Figure 5.1 shows the circuit configuration of the PCU. The battery voltage is first raised by the boost converter inserted between the battery and the inverters. The raised voltage is then supplied to the motor and the generator through the inverters. The voltage supplied to the motor and the generator has been increased from the battery voltage of 202 V DC to a maximum voltage up to 650 V DC. The power capacity of the boost converter is about 20 kW, which is corresponding to the instantaneous power of the the battery.

The benchmark boost converter design is shown in Figure 5.4. It is a continuous conduction mode (CCM) boost converter. It consists of input filter capacitor, main capacitor, boost inductor, two IGBTs and two free wheeling diodes. To handle the huge current stress, for each IGBT, there are two dice connected in parallel. For each diode, there are also two dice in parallel. The CCM boost converter is a simple and reliable topology, but it has several limitations for further improvement. For this boost topology, high voltage rating devices are needed because the 650V output voltage will determine the devices' voltage stress. High voltage rating devices will result in high conduction losses and high switching losses. Most importantly, high voltage rating diodes could have severe the reverse recovery loss problem. To keep the switching related power loss low, lower switching frequency is preferred. However, this can result in large passive components size and make the input and output current ripple difficult to filter out. The large passive components could be one major bottle neck for the high density converter design.

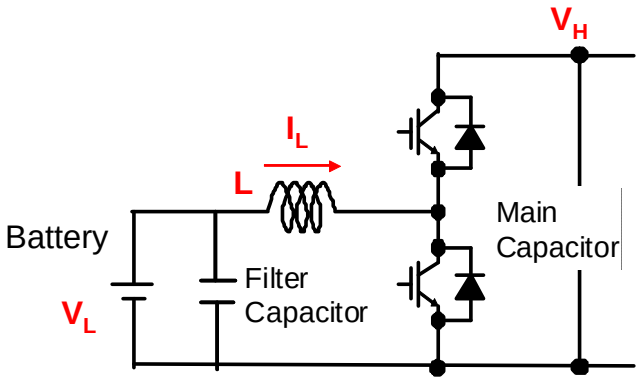


Figure 5.4. Benchmark converter circuit diagram.

a. Evaluation on semiconductor power loss

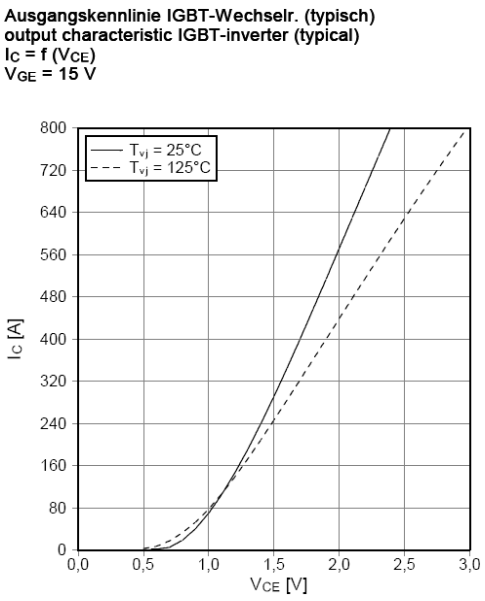
To illustrate the issues mentioned above, the semiconductor power loss can be calculated for the benchmark converter. The circuit parameters are as follows,

Battery voltage: $V_L = 202$ V;

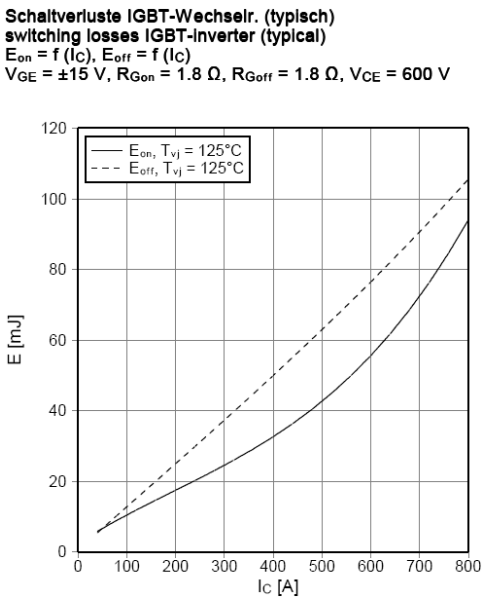
Bus voltage: $V_H = 650$ V;

Switching frequency: $f_s = 10$ kHz;

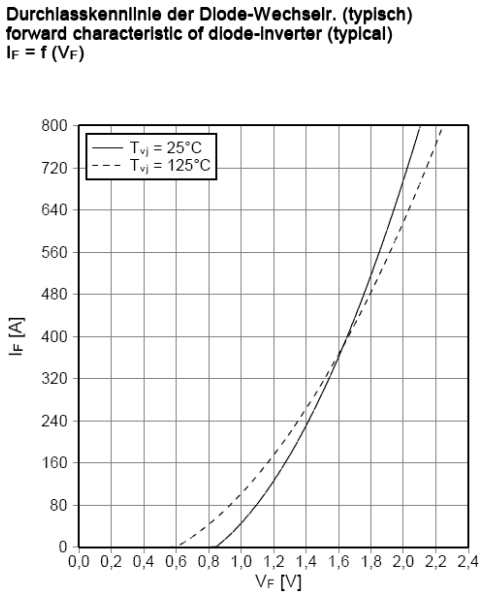
Boost inductor: L = 370 uH.



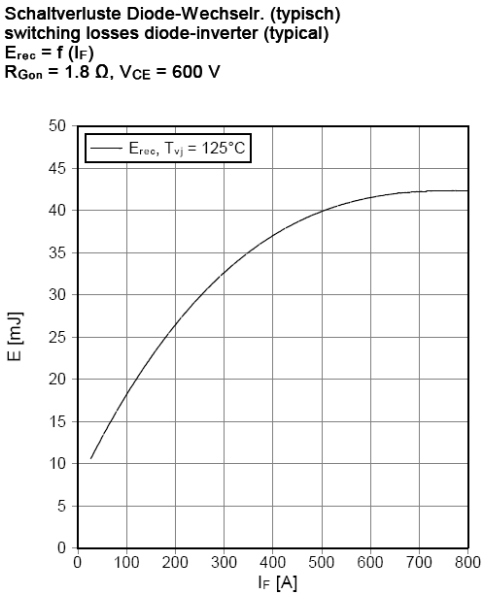
(a) IGBT output characteristic



(b) IGBT switching losses



(c) Diode forward characteristic



(d) Diode reverse recovery loss

Figure 5.5. Device characteristics for semiconductor power loss evaluation.

The 1200 V, 400 A Infineon IGBT module FF400R12KT3 is used to evaluate the power loss of this converter. According the datasheet, the output characteristic, turn-on loss, and turn-off loss of the IGBT, and the forward characteristic, and the reverse recovery

loss of the diode can be obtained, as shown in Figure 5.5. All these data can be included into a loss evaluation program by curve-fitting method.

The calculated device power loss at different output power is shown in Figure 5.6. A loss break down at P_o = 25 kW is shown in Figure 5.7. It clearly shows that the switching related power loss takes up to 77% of the total power loss, which includes 18% turn on loss, 29% turn off loss, and 30% reverse recovery loss. The switching related loss is the dominate factor for the semiconductor power loss since the conduction loss is only about 23%. Reducing the switching related power loss would be the key to reduce the power loss, so that better efficiency, easier thermal management, and higher density can be achieved.

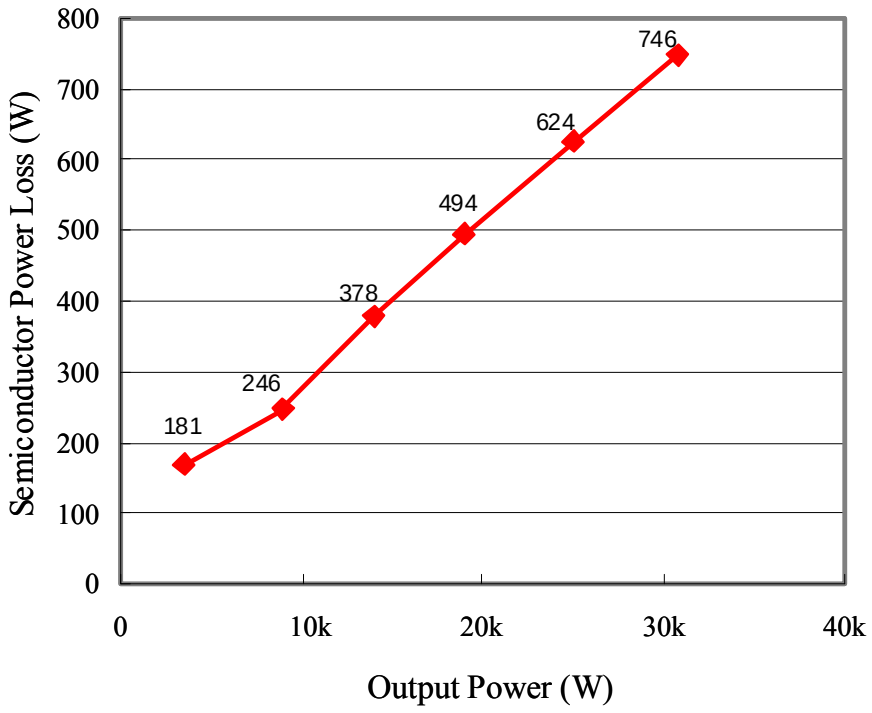


Figure 5.6. Calculated semiconductor power loss of benchmark converter.

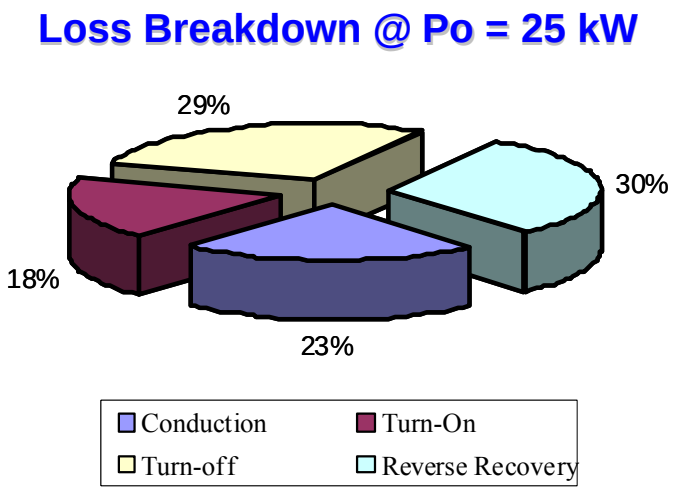


Figure 5.7. Semiconductor loss breakdown at P_o = 25 kW.

b. Evaluation on inductor power loss

By studying the inductor prototype, as shown in Figure 5.8, the basic parameters can be obtained to estimate the inductor power loss. The number of turns is 46. The cross section area of the windings is 7.742 mm^2. The cross section area of the core is 146mm^2. More than 70% window area is utilized. It is assumed the amorphous core material is used, which is one of the most suitable core materials for this application.

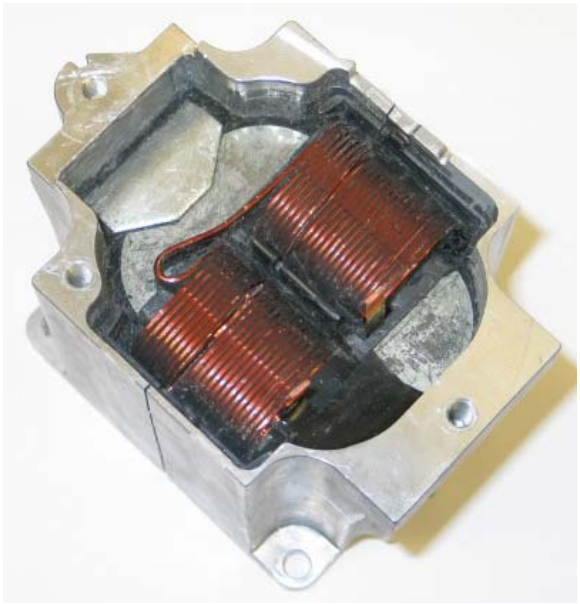


Figure 5.8. Benchmark inductor prototype.

For the benchmark design, the inductor power loss estimation at different output power is as shown in Table 5.1. The inductor core loss calculation is based on V_L = 202 V, and V_H = 650 V. Since the input and output voltages are the same, the core losses of the inductor are the same at different load conditions. Based on the calculation results, the power loss is unevenly distributed in the inductor. The winding loss dominates, and the core loss is negligible.

Table 5-1. Estimated power loss for the benchmark inductor design.

Output Power	**9 kW**	**25 kW**	**30.8 kW**
Winding loss	45W	347W	526W
Core loss	12W	12W	12W
Total loss	57W	359W	538W

c. Limitation of the benchmark converter design

Although the benchmark converter design is simple, according to the evaluation, there are several limiations for further improving the power density. Due to the high voltage and current stress, the power loss of the semiconductors are very high. The power loss evantually needs to be dissipated in the form of heat. Increasing the power density without reducing the power loss will, sooner or later, make the thermal management impossible. Failing to manage the heat can course sever problems for the power converter. The switching related power loss dominates the power loss of the semiconductor devices, since the conduction loss is only 23%. The reverse recovery loss from the freewheeling diode contributes a big part of the switching related power loss due to the limited recovery performance of the high voltage rating fast recovery Si diodes. To eliminate the diode recovery power loss problem, one simple solution is to use the SiC diode. Furthermore, the SiC diode can operate at much higher junction temperature due to the wide bandgap material. In principle, SiC devices could operate at a junction temperature as high as 500 ºC, as compared to a tiypical 150 ºC for the silicon devices [62]. The increased operating temperature will reduce the weight, volume, cost, and complexity of the thermal

management. However, there are still many technical barriers, including the high defect density and high cost of SiC wafters, prevent SiC technology from large scale commercialization in the near future. Currently, the cost of the SiC devices ranges from five to ten times that of silicon devices with the same voltage and current rating.

The boost inductor is a significant components in terms of size and weight of the total package. Generally, the inductro size can be reduced by increasing the switching frequency. However, due to the large switching related power loss, lower switching frequency is prefered. Since the large energy storage capability is needed, the inductor of the boost converter operating at CCM is difficult to reduce and could be one of the major barrier for further improving the power density.

Large input filter capacitor and the output main capacitor of the boost converter are needed to reduce the voltage ripple since the switching frequency is lower. Especially, the main capacitor at the output needs to handle high RMS current. To obtain a reasonable capacitor lifetime, a large capacitor is needed. At the input side, the filter capacitor also could be large because small voltage ripple is preferred for the battery.

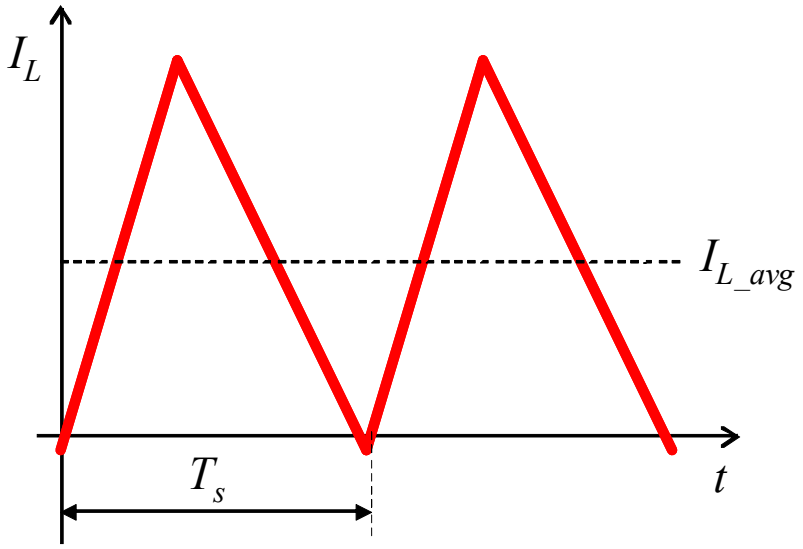
5.1.3 Proposed interleaved boost converter

Although the SiC diode can be introduced to remove the reverse recovery loss, there are still some technical and economical barriers preventing it from large scale commercialization in the near future. Without replacing the conventional Si diode, other circuit operation mode can be introduced to eliminate the diode reverse recovery loss.

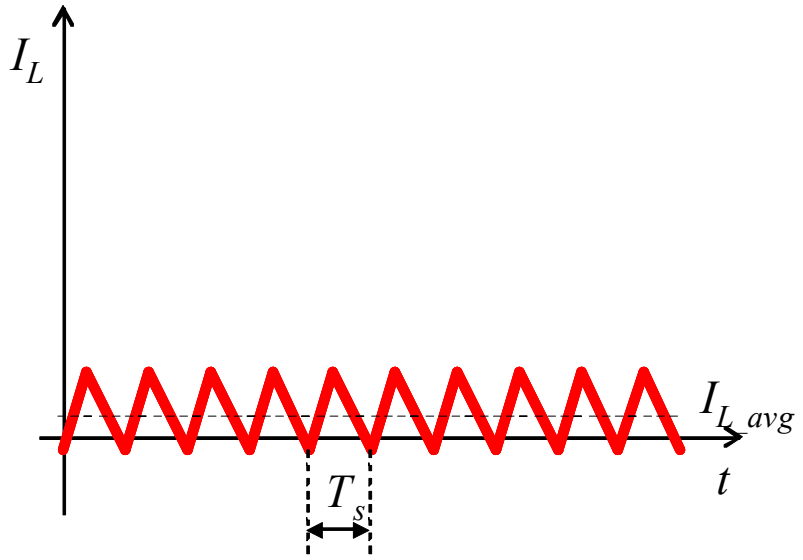
Operational modes of switching mode power converters are normally divided into two types, continuouse conduction mode (CCM) and discontinuous conduction mode (DCM) by their condiction of the inductor current. Critical conduction mode (CRM) is at the boundary of CCM and DCM, which is also sometimes referred as CCM/DCM boundary mode, or transition mode.

In critical mode boost converter, the switching transistor is turned on as soon as the inductor current reaches zero. Since the diode is turned off at zero current, as shown in Figure 5.9, the boost diode does not have the reverse recovery problem any more. Not only

the reverse recovery loss, the turn-on loss can be eliminated as well since the turn-on current is virtually zero every time when the switch is turned on. Thus, the switching related power loss can be significantly reduced. Although the inductor peak current will be increased to two times of the average inductor current, the total power loss still can be reduced since the conduction is relatively low comparing with the switching related power loss.



(a) Inductor current at heavy load condition



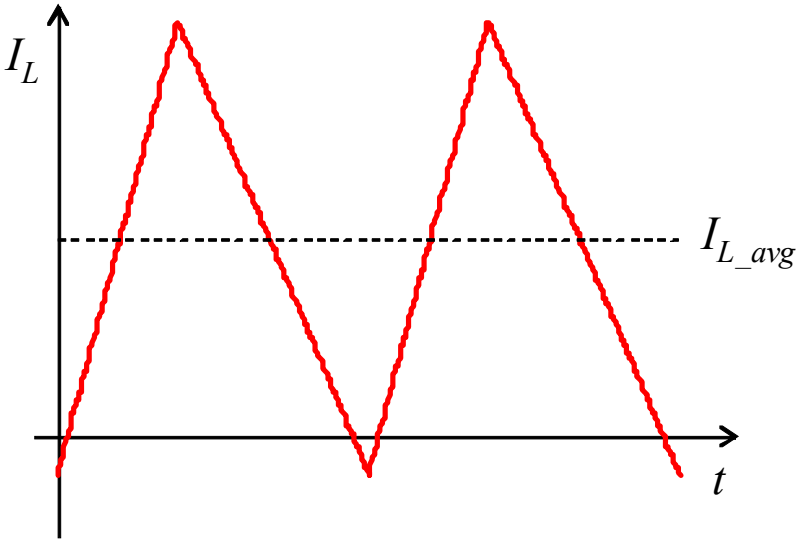
(b) Inductor current at light load condition

Figure 5.9. Boost inductor current waveform of critical mode operation.

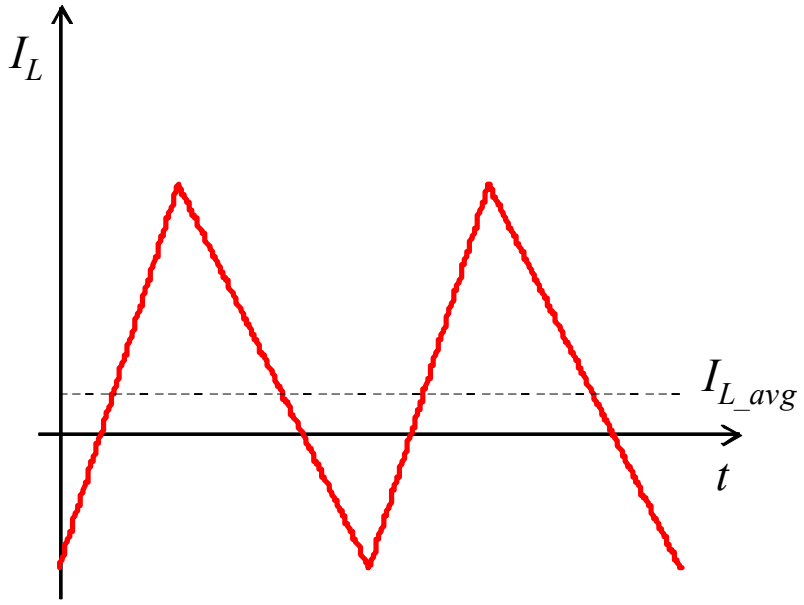
The major concern of the CRM operation is the varible switching frequency. To keep the converter operating at critical mode for all load and line conditions, the switching frequency could vary in a quite large range. For example, the switching frequency could be extremely high when the converter is operated at very light load condition, as shown in Figure 5.9. High switching frequency will make the power converter inefficient eventually.

Since the battery charger/discharger is a bi-directional converter, the Quasi-Square Wave (QSW) mode operation can be introduced to eliminate the diode reverse recovery loss. To operate in QSW mode, the inductance is reduced to a certain value compared with the CCM operation so that the current always starts from a negative value. The inductor will contain a peak-to-peak current ripple always at least twice the average battery current. As shown in Figure 5.10, when the bottom IGBT (as shown in Figure 5.4) turns on, the inductor current rises from a negative value to a level equal to at least twice the DC current. When the bottom IGBT turns off, the output capacitor of the bottom IGBT will be charged and the output capacitor of the top IGBT will be discharged. The current commutated to the top freewheeling diode. A short period of time later, the top IGBT is turned on yielding synchronous rectification. The inductor current linearly decreases through zero. The current slew rate is determined by the inductance and independent to load. With proper inductance design, the top freewheeling diode current naturally commutates, so the diode reverse recovery loss is eliminated. At this point, the top IGBT is turned off. During the dead-time that both IGBTs are off,the stored energy in the inductor charges and discharges the output capacitors of the IGBTs, thus zero voltage switching is achieved.

By operating the converter in QSW mode, the freewheeling diode reverse recovery loss can be eliminated and the zero-voltage-switching turn-on can ba achieved for the IGBTs. Although the turn-off loss may increased, this still can significantly reduced the switching related power losses. However, since the inductor peak-to-peak current ripple is always at least twice the average battery current, the conduction loss is increased. Especially at light load, the inductor peak-to-peak current is much higher than the current in the CCM mode operation, as shown in Figure 5.10 (b). This can dramatically impact the converter light load efficiency, and eventually impair the fuel effieincy of the hybrid electric vehicle.



(a) Inductor current at heavy load condition

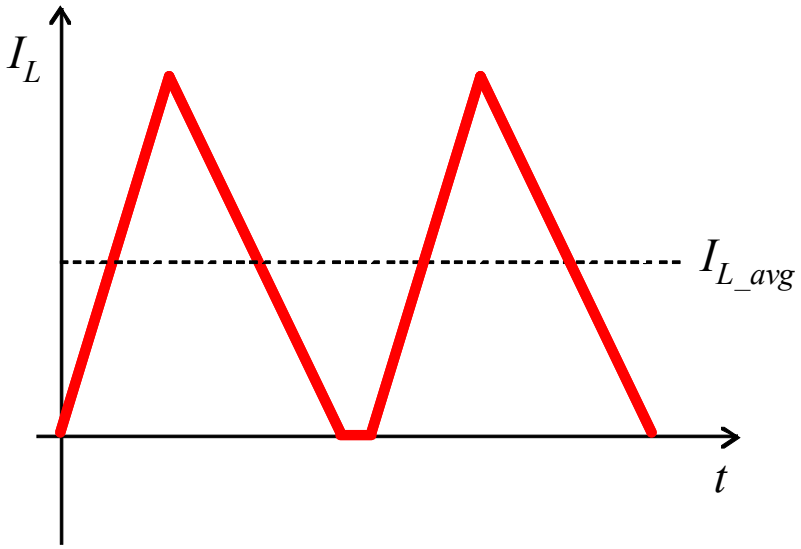


(b) Inductor current at light load condition

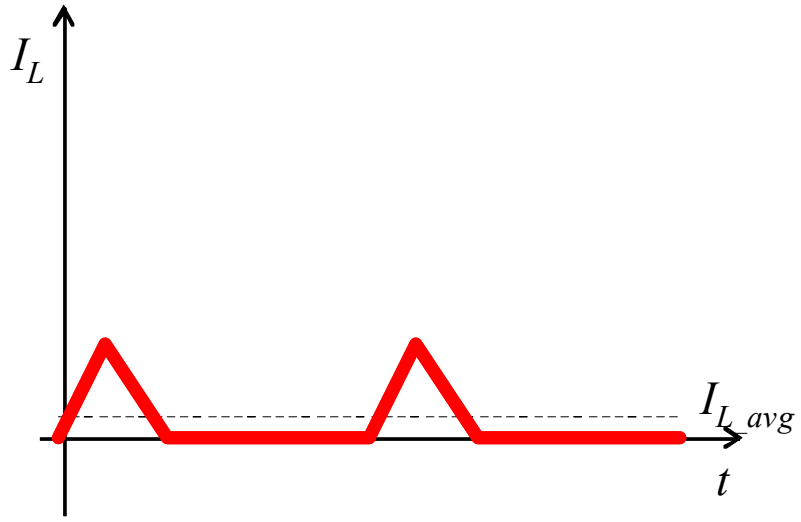
Figure 5.10. Boost inductor current waveform of quasi-square wave mode operation.

Other than the CRM and QSW mode, converter operates at DCM can also solve the diode reverse recovery problem. By properly reducing the inductance to a certain value, the inductor current always reaches zero before the IGBT turns on. In DCM operation the inductor peak current is always at least twice the average battery current. Since the diode

current slew rate is well controlled by the inductor, the freewheeling diode current naturally commutates, so the diode reverse recovery loss is eliminated.



(a) Inductor current at heavy load condition



(b) Inductor current at light load condition

Figure 5.11. Boost inductor current waveform of discontinuous conduction mode (DCM) operation.

Not only the reverse recovery loss, the turn on loss also becomes negligible since the IGBT turn-on current is always zero. The energy stored in the output capacitor of the IGBT is greatly reduced since the IGBT only sustains the input voltage which is much lower than the output voltage. Althoug the turn-off loss of the IGBT is increased due to the high turn-

off current, the total switching related power loss still can be greatly reduced. A detailed power loss estimation will be introduced to demonstrate this loss reduction. Since the inductor peak current is always twice the average battery current, not like the QSW mode, the inductor peak-to-peak current ripple is proportional to the load, as shown in Figure 5.11, which means the conduction loss reduces with the load decreasing.

Both the CRM and QSW operation modes can eliminate the diode reverse recovery loss and the turn-on loss. The CRM operation has no circulating current. However, it is basicaly a variable frequency control. The control is complicated, especially when interleaving is considered, and the efficiency is lower at light load due to the high switching frequency. QSW mode operation is a simple constant frequency control. Bi-direction power flow can be natually realized. However, the circulating current could be huge at light load and no load conditions, which will result in poor light load efficiency. The DCM operation can also eliminate the diode reverse recovery loss and minimize the turn-on loss. It can be realized with simple constant frequency control and there is no circulating current.

DCM operation has the benefits of reducing the switching related power loss, simple constant frequency control, and no circulating current. However, same as the CRM and QSW mode operation, it has large inductor peak-to-peak current ripple which will cause large input and output current ripple of the converter. To meet the ripple requirement, large input and output filter capacitor will be inevitable which will hurt the converter power density. To solve this problem, multi-channel interleaving can be introduced. The ripple cancellation effect can reduce both the input and output current ripple. The other benefits of multi-channel interleaving, such as phase shedding, also can be applied to further improve the light load efficiency. In order to have a thorough exploration, the multi-channel interleaved boost converter is considered as a dual of multi-channel VR, as shown in Table 5.2, since the thorough investigation has been done on the VR application.

The side by side comparison of the mutli-channel interleaving for VR and battery charger/discharger application shows that the benefits identified for the VR also can be found in the battery charger/discharger. By adopting DCM operating not only the switching related power loss is lower but also the inductro size can be reduced. Size

reduction of the filter capacitor and the main capacitor also can be achieved by ripple cancellation effect in spite of the larger inductor peak-to-peak current ripple. By using several channels to share the power, the thermal dissipation is more evenly distributed which makes the thermal design much easier. The overall cost could be reduced considering the smaller passive components size and the standardization of the cell design. The multi-channel interleaving also makes the system scalable. More channels can be added if the electric drive power needs to be upgraded for heavier duty vehicles in the future. This could be very cost effective compare with redesigning the whole power converter. With the multi-channel architecture, the phase shedding technique can be applied to further improve the light load efficiency.

Table 5-2. Interleaving comparison between the multiphase VR and the multi-channel battery charger/discharger.

Multi-channel buck converter for VR	Multi-channel boost converter for battery charger/discharger
• Improve the power density o Smaller inductance (QSW) – better transient performance o Smaller output filter - smaller output current ripple o Smaller input filter – smaller input current ripple • Thermal dissipation more evenly distributed • Overall cost reduced – less capacitors, standardized cells • Scalability – keep step with future CPU power management design • Better light load efficiency – phase shedding technique	• Improve the power density o Same inductance (DCM) – reduce the switching related power loss o Smaller fiter capacitor - smaller input current ripple o Smaller main capacitor – smaller output current ripple • Thermal dissipation more evenly distributed • Overall cost reduced – possible (smaller capacitors, standardized cells) • Scalability – keep step with varias engine power requirement • Better light load efficiency – phase shedding technique

Coupled inductor has been succesfully introduced to multi-phase VR application. However, it runs into some issues at light load condition when the converter goes into DCM operation. Analysis shows the inductor current will touch zero twice in one switching cycle [65]. The twice zero current touching in the DCM of coupled inductor VRs caused by the coupling effects between the phase inductors results in poor VR light load efficiency. To avoid the similar problem, the coupled inductro is considered for this battery charger/discharger application since DCM operation is adopted.

In conclusion, using multi-channel interleaved DCM boost converter for the battery charger/discharger can achieve much better performance comparing with the benchmark design, the single-channel boost converter.

a. Semiconductor power loss estimation

Based on the study and analysis on the benchmark converter, a three-channel interleaved discontinuous conduction mode (DCM) converter was proposed for the test bed demonstration.

The switching frequency is designed to be 10 kHz to meet the minimum switching frequency requirement. The boost inductor is designed to be 149 uH. 1200 V, 150 A Infineon IGBT module FF150R12KT3G is used to evaluate the power loss of this converter. Same as the evaluation proceedure of the benchmark converter, the information of the output characteristic, turn on loss, and turn off loss of the IGBT, and the forward characteristic, and the reverse recovery loss of the diode are included in a loss evaluation program by curve-fitting method. The estimated semiconductor devices power loss is shown in Figure 5.12. Compared with the benchmark design, the designed 3-channel interleaved DCM converter has less semiconductor power loss at different operating conditions as predicted. For example, as can be observed, about 124 W power loss can be saved at P_o = 25 kW. Lower power loss will not only result in higher efficiency, but also easier thermal management.

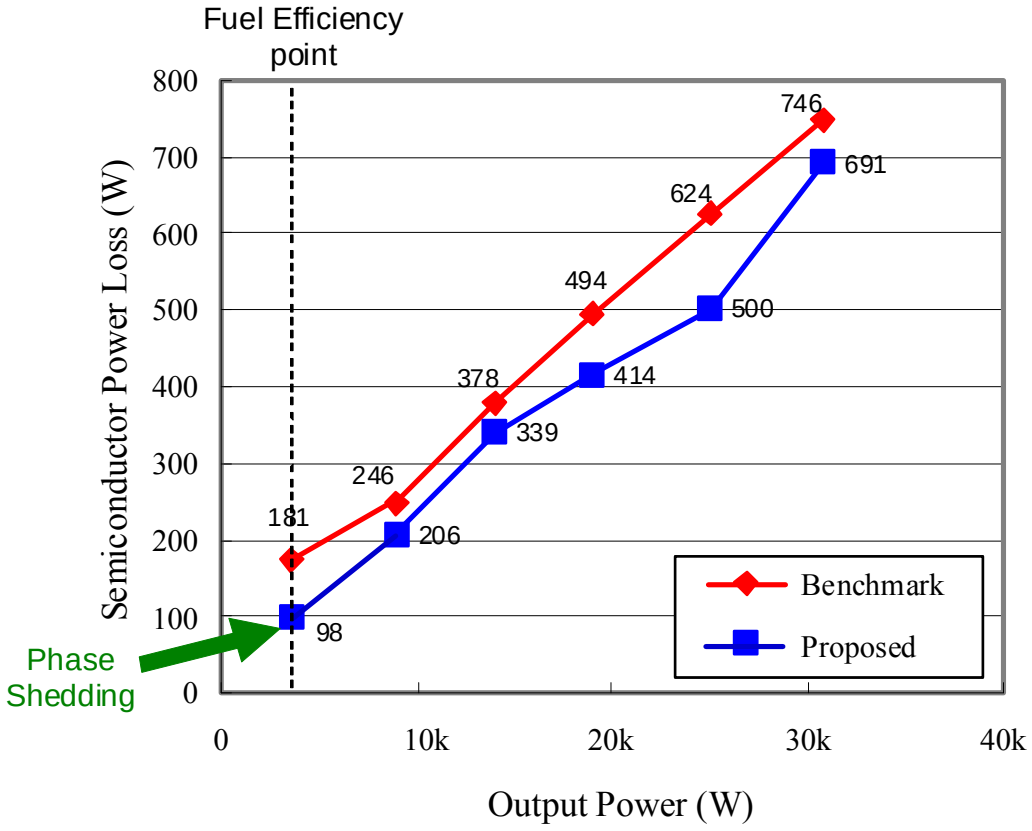


Figure 5.12. Calculated semiconductor power loss of benchmark converter and proposed 3-channel interleaved DCM boost converter.

b. Boost inductor design and loss estimation

The inductor used in the three-channel interleaved DCM converter design is as follows:

- $L_1 = L_2 = L_3 = 149\ uH$.
- Switching frequency is 10 kHz.
- The maximum inductor average current is 51.3 A (154 A / 3).

After surveying different company's core material, Iron Based Amorphous Alloy from Metglas is chosen. This material is manufactured with iron based metglas amorphous alloy 2605SA1, POWERLITE® C-Cores. It can provide significant cost, design and

performance benefits over ordinary Si-Fe, ferrite and MPP cores due to the following characteristics.

- High Saturation Flux Density (1.56 T)
- Low Height - enables weight and volume reductions of up to 50%
- Low Temperature Rise - enabling smaller compact designs
- Low Loss - resulting from micro-thin Metglas® ribbon (25 µm)

It is a commercial core product with a list of dimensions to choose from.

According to the material saturation flux density, 1.56 T, and considering leaving some design margin, the maximum flux density is chosen to be,

$$B_{max} = 1.4\ T \tag{5-1}$$

To obtain similar winding loss as the bench mark, the current density is firstly chosen to be,

$$J_m = 13\ A/mm^2 \tag{5-2}$$

The window area usage coefficient is assumed,

$$K_u = 0.5 \tag{5-3}$$

According to the converter design, considering three-channel interleaving, the maximum peak current for each inductor can be calculated,

$$I_{lp3} = \frac{I_{\max}}{n_{CH}} + \frac{I_{ripple}}{2} \tag{5-4}$$

Where I_{max} is the maximum inductor average current; I_{ripple} is the peak-to-peak current ripple; n_{CH} is the channel number. The rms current can be calculated,

$$I_{rms3} = \sqrt{\left(\frac{I_{\max}}{n_{CH}}\right)^2 + \frac{\left(\frac{I_{ripple}}{2}\right)^2}{n_{CH}}} \tag{5-5}$$

The switching frequency is

$$f_s = 10\ kHz \tag{5-6}$$

Based on the selected parameters and the inductance, the area-product can be calculated,

$$A_{p3} = L_{p3}\frac{I_{lp3}I_{rms3}}{K_u B_{\max} J_m} \tag{5-7}$$

The core is chosen based on the calculated area-produce. Once the core is selected, the geometry data of the core can be obtained from the data sheet, such as the cross section area of the core A_{cb3} ;The core window area W_{ab3} ;

The number of the turns can be calculated,

$$n_{b3} = L_{p3}\frac{I_{lp3}}{A_{cb3}B_{\max}} \tag{5-8}$$

Based on the rms current and the selected current density, the winding wire cross section area can be calculated,

$$A_{wb3} = \frac{I_{rms3}}{J_m} \tag{5-9}$$

According to the calculated winding wire cross section area, proper wire is chosen. The window area usage can be verified as follows

$$k_{b3} = \frac{A_{wmb3}N_{b3}}{W_{ab3}} \tag{5-10}$$

The winding length per turn can be calculated according to the core geometry

$$L_{en3} = 2a+2d \tag{5-11}$$

Where the *a* and *d* are defined by the datasheet, as shown in Figure 5.13.

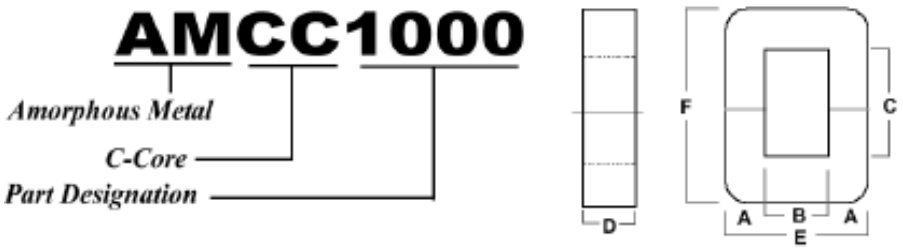


Figure 5.13. Core geometry parameters definition

The winding resistance can be calculated,

$$R_{Cub3} = \frac{N_{b3} l_{en3} C_{oe3} 17 \cdot 10^{-9}}{A_{wmb3}} \tag{5-12}$$

Where C_{oe3} is the winding length coefficient. The total winding loss of three inductors at 100 degree ºC can be calculated,

$$P_{Cu3} = I_{rms3}{}^2 R_{Cub3} \cdot (1 + 0.004 \times (100 - 25)) \times n_{CH} \tag{5-13}$$

The core loss density can be calculated as,

$$P_{ld} = 6.5 \cdot f_{s3}{}^{1.51} \cdot B_{mH}{}^{1.74} \tag{5-14}$$

According to the geometry, the core volume can be calculated,

$$Volum = \frac{d \cdot e \cdot f - d \cdot b \cdot c}{1000} \tag{5-15}$$

The total core loss of three inductors is,

$$P_{core} = \frac{P_{ld} 7.18 \cdot Volum}{1000} n_{CH} \tag{5-16}$$

The total inductor size can be estimated as

$$Volume = \frac{(d+b)(e+b) f}{1000} n_{CH} \tag{5-17}$$

Following the same design procedure, trade-off between the inductor size and winding loss can be made by varying the winding current density.

Using the commercially available core dimensions, the winding loss dominates the total power loss when the inductor size is small. According to the estimation, the winding loss could be 4 to 9 times higher than the core loss. This unevenly distributed power loss will make the thermal difficult to manage for the inductor. The loss distribution can be altered by changing the core dimensions. With design iterations, the following dimensions are selected for the customized core, with *a, b, c, d, e, f* defined in Figure 5.13,

a = 13mm; b = 14mm; c = 14mm; d = 60mm; e = 40mm; f = 40mm;

With this core dimensions, the number of turns is reduced. At Po = 25 kW, the estimated power loss is 167 W, 70% of the bench mark. The estimated total inductor is 479 cm3, 50% of the bench mark design. The inductor evaluation results are shown in Table 5.3.

Table 5-3. Inductor design with customized core dimensions

(Power loss is estimated at Po = 25 kW)

Core	PS0725AA
Turns	30
Copper loss (W)	167
Core loss (W)	68
Estimated size (cm^3)	479

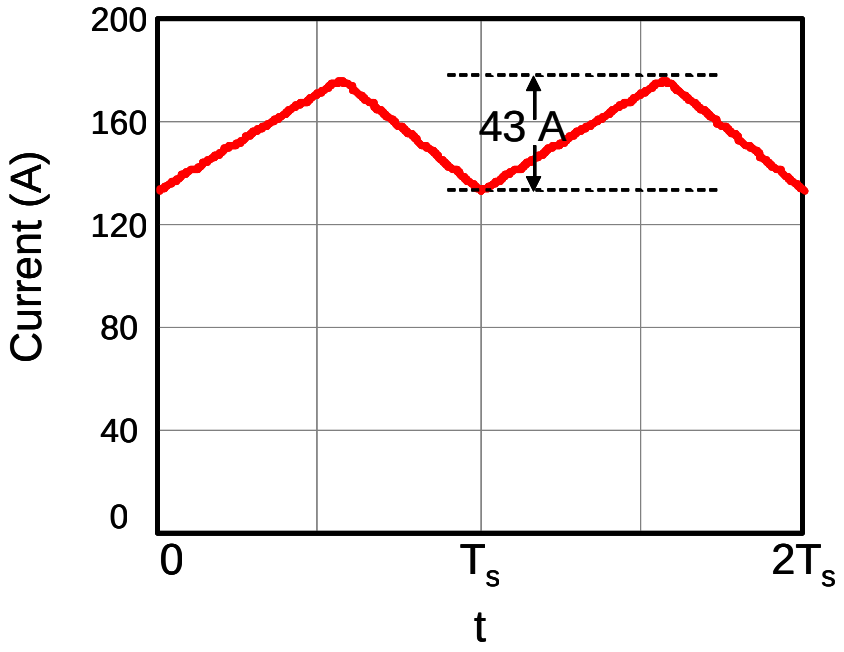
Due to the DCM operation, the energy storage requirement of the interleaved three-channel converter is greatly reduced. Comparing with the bench mark inductor design, either the winding loss can be reduced or the inductor size can be reduced. A good trade-off can be made to achieve both the power loss and the size reduction. By using the customized core dimensions, the inductor power loss is reduced to 70% and the size is reduced to 50% of the bench mark design.

c. Input current ripple reduction

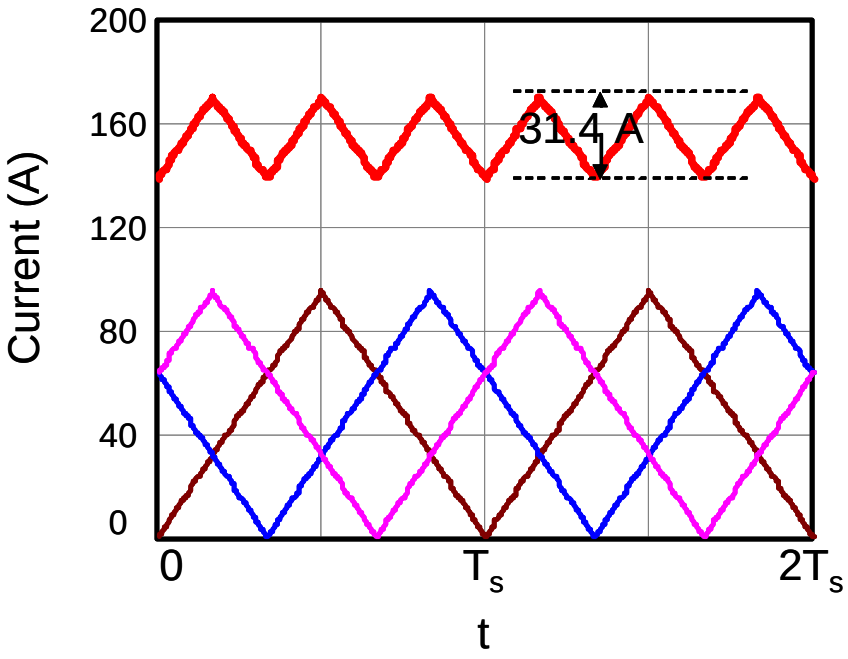
Adopting 3-channel interleaved DCM boost converter, although the inductor is greatly reduced and the inductor peak-to-peak current ripple is much larger, the input current ripple is not increased at all due to the ripple cancellation effect.

In the benchmark design, large input filter capacitor is needed to keep the battery ripple current below certain level. For the three-channel interleaved converter design, this input filter capacitor can be significantly reduced due to the smaller magnitude and higher frequency current ripple.

The worst case input current ripple sinario is identified for both the benchmark converter design and the proposed 3-channel interleaved converter design respectively. For the benchmark converter design the input current ripple magnitude is 43 A, as shown in Figure 5.14 (a). For the proposed 3-channel interleaved converter design, although the inductor peak-to-peak current is increased, the input current ripple magnitude is reduced to 31.4 A as shown in Figure 5.14 (b). 27% ripple current reduction is achieved.



(a) Benchmark converter input current waveform



(b) Proposed 3-channel interleaved converter input current waveform

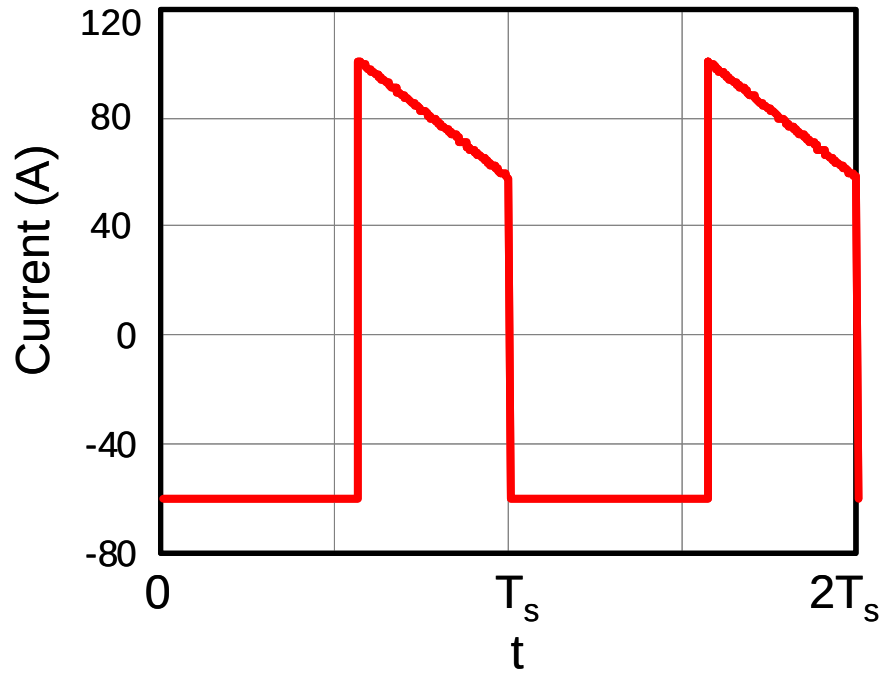
Figure 5.14. Input current ripple comparison.

Not only the current ripple magnitude is reduced, but also the ripple frequency is three times higher. With this 27% small current ripple and three times higher ripple frequency, the input filter capacitor can be much smaller than the benchmark design.

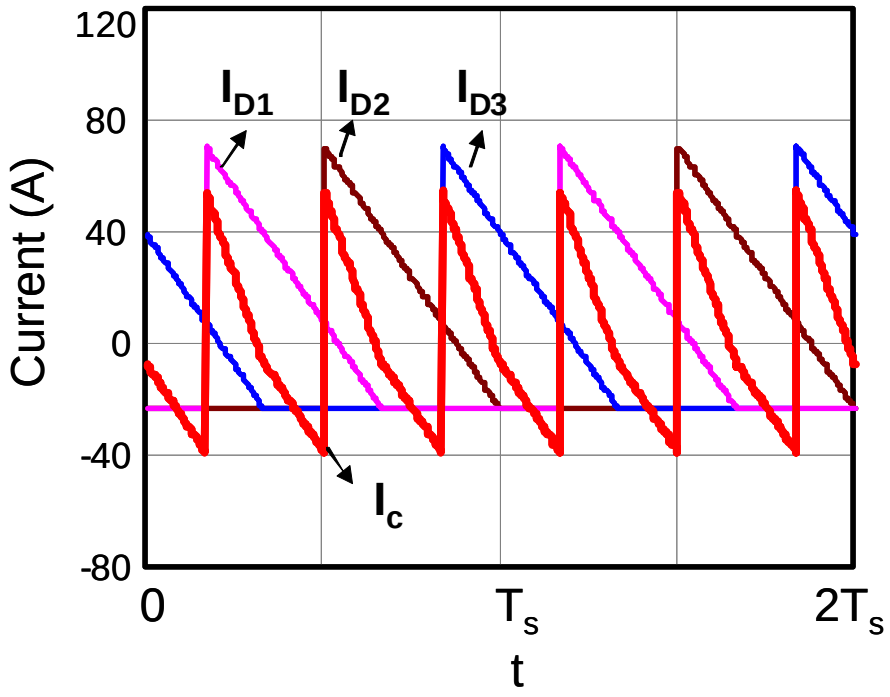
d. Output current ripple reduction

In the boost converter, the AC current goes through the output capacitor is large, as shown in Figure 5.15 (a), and normally could be design criteria for the output capacitor. In the benchmark converter design, the CCM boost, the RMS of output current ripple is 69.3 A and difficult to reduce since it is almost independent to the converter design.

By interleaving, the AC current goes through the output capacitor also can be reduced due to the ripple cancellation effect, as shown in Figure 5.15 (b). The output ripple RMS current is reduced from 69.3 A to 27.2 A. 60% RMS ripple reduction is achieved. The smaller RMS ripple current can either reduce the output capacitor (main capacitor) size or prolong the output capacitor life time by reducing the power loss of the capacitor.



(a) Benchmark converter output current waveform



(b) Proposed 3-channel interleaved converter output current waveform

Figure 5.15. Output current ripple comparison.

For the main capacitor in this charger/discharger application, the factors that affect the choice of the capacitance are the output voltage ripple, the RMS of ripple current, and the energy buffer requirement. For very low switching frequency design, the output voltage ripple requirement could be the dominating factor of the output capacitance. The energy buffer requirement comes with system design. In the Power Control Unit (PCU) design the main capacitor is chosen based on the energy buffer requirement for transient. Since the main capacitor is predetermined, the interleaved 3-channel DCM boost converter can prolong the capacitor life time by reducing the AC current goes through it.

5.2 Other Applications

Boost converters are also used in lots of other applications. The explored impact in the previous chapters of the interleaved boost converters may or may not give benefits depends on the requirements of the applications. However, the features, such as scalability, ripple cancellation effective at the input and output, phase shedding, coupled inductor, and even thermal distribution are always exist in the multi-channel interleaved boost converter. These features could be used to evaluate the design for different applications.

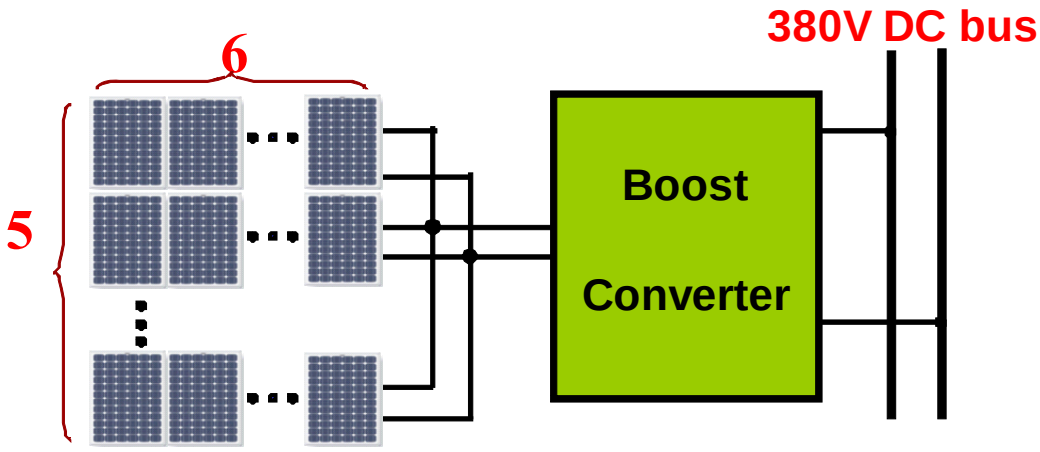


Figure 5.16. Boost converter in PV system.

For example, Figure 5.16 shows a photovoltaic system with boost converter. By applying multi-channel interleaving, the input and output current ripple can be reduced and

the effective ripple frequency can be increased. The reduced higher frequency ripple can either make the filter size smaller or make the filter capacitor lifetime longer or both. The intensity of the sun light for the PV may vary in a wide range depend on whether condition or simply different time of a day. In order to achieve high power converter, efficiency a light load could be important. With multi-channel structure, phase shedding may be introduced to improve the light load efficiency. More benefits can be further explored, depends on the design considerations of the PV systems.

5.3 Summary

The boost converter is one of the simplest and most widely used topologies for the battery charger/discharger converter when isolation is not required. Similar to the multi-channel interleaved buck converter, the multi-channel interleaving boost converter has advantages over the conventional single-channel boost converter. In this chapter, the benefits of multi-channel interleaved boost converter are investigated for the battery charger/discharger in the Hybrid Electric Vehicles (HEVs) applications. Adopting the proposed 3-channel interleaved DCM boost converter, the improvement over the benchmark converter design, the single-channel boost converter, is demonstrated.

The switching related power loss is significantly reduced by DCM operation. Although the conduction loss is increased, 124 W the total semiconductor power loss is reduction can be achieved at Po = 25 kW. The energy storage requirement of the boost inductor is also greatly reduced because of the DCM operation. Comparing with the benchmark inductor design, the inductor power loss is reduced to 70% and the size is reduced to 50%. The input current ripple is reduced by 27% and the ripple frequency tripples due to the ripple cancellation of 3-channel interleaving. Thus, the input filter capacitor can be greatly reduced. The RMS of AC current goes through the output capacitor reduced by 60% due to interleaving. The main capacitor life time can be prolonged since the capacitor size is determined by the system energy storage requirement for the transient.

By using several channels to share the power, the thermal dissipation is more evenly distributed which makes the thermal design much easier. The overall cost could be reduced considering the smaller passive components size and the standardization of the cell design. The multi-channel interleaving also makes the system scalable. More channels can be added if the electric drive power needs to be upgraded for heavier duty vehicles in the future. This could be very cost effective compare with redesigning the whole power converter. With the multi-channel architecture, the phase shedding technique can be applied to further improve the light load efficiency which eventually can make the vehicle more fuel efficient.

Following the same principle explored in the previous chapters, the benefits of interleaved boost PFC can be further extended other applications, such as the boost converter in the PV system.

Chapter 6. Summary

With the rapid evolving IT technologies, today, the power factor correction (PFC) design is facing many challenges, such as power scalability, high entire-load-range efficiency, and high power density. Power scalability is a very desirable and cost-effective approach in the PFC design in order to keep up with servers' growing power requirements. Higher power density can eventually reduce the converter cost and allows for accommodating more equipment in the existing infrastructures. Driven strongly by economic and environmental concerns, high entire-load-range efficiency is more and more required by various organizations and programs, such as the U.S. Energy Star, Climate Savers, and German Blue Angel. Today, the existing boost PFC is reaching its limitations to meet these challenges simultaneously. Using the cutting-edge semiconductor devices, further efficiency improvement at light load is still needed. There are limited approaches available for increasing the power density due to the large EMI filter and inductor size.

Interleaved multi-channel boost PFC is a promising candidate to meet those challenges, but the interleaved boost converter is a less explored area. On the other hand, the multi-channel interleaved buck converter for the VR application has been intensively studied and thoroughly explored. One basic approach of this study is trying to extend the existing knowledge and techniques obtained from multiphase buck converters to the multi-channel interleaved boost converters since there are similarities existed between the multi-phase buck and the multi-channel boost converters.

The existing studies about the interleaving impact on the EMI filter design are based on the time domain ripple cancellation effective. This approach is good enough for most of the filter designs. However, unlike the conventional filter designs, the EMI filter design is a specification related process. Both the EMI standard and the EMI measurement are based on the frequency domain spectrum. Limited by the existing analysis approach, it is difficult to provide a clear picture about how exactly the multi-channel interleaving will impact the EMI filter design. The interleaving impact on the Common Mode (CM) noise also has not been studied in any existing literatures for the same reason. In this study, the frequency domain analysis method was adopted. With the double Fourier integral transformation, a

closed-form expression of all the harmonics of the noise sources can be obtained. With all the detailed phase relationship of the switching frequency harmonics and all the side band harmonics, the multi-channel interleaving impact on both the differential mode (DM) and CM filter design can be clearly understood and summarized. According to the design curves provided, the EMI filter size can be effectively reduced by properly choosing the interleaving channel number and the switching frequency. The multi-channel interleaving impact on the output capacitor current ripple is also studied and summarized in this dissertation.

It should be pointed out that interleaving only reduces the total input and output current ripples; the inductor current in each channel still has large ripple if small inductance are used. Similar to the multi-phase buck converter, coupling inductors result in different equivalent inductances for input current ripple and inductor current ripple for boost converters. Keeping the inductor current ripple magnitude the same, inverse coupling inductors between the interleaved channels can reduce the inductor size. However, the DM filter size is increased due to larger input current. Based on the investigation on the total magnetic component weight, inverse coupling inductor can reduce the total magnetic component weight. The reduction is more pronounced for lower switching frequency design when the inductor size is dominating among the total magnetic components.

Based on the harmonic cancellation, and with all the detailed phase relationship of the switching frequency harmonics and all the side band harmonics, a novel phase angle control method is proposed to maximize the reduction of the EMI filter. For example, in a 2-channel interleaved PFC, just by changing the interleaving scheme to 90 degree phase shift, 39% total volume reduction of the EMI filter can be achieved. The proposed phase angle controlled multi-channel PFC is experimentally demonstrated and verified on a digital controlled 4-channel PFC. The phase angle control method proposed in the multi-channel boost converter can be applied back to the multi-phase buck converter as well. The harmonic cancellation principle will be the same as the multi-channel boost converter. The same benefits can be obtained when the requirement is defined in the frequency domain, e.g. the EMI Standard.

The interleaved multi-channel configuration makes it possible to implement the phase-shedding to improve the PFC light load efficiency. By decreasing the number of

active channels according to the load, the PFC light load efficiency can be optimized. However, shedding phases can reduce the ripple cancellation effect as well, which will result in the EMI noise increase and losing the benefit on the EMI filter. By applying the proposed phase-shedding with phase angle control strategy, the phase shedding impact on the EMI filter design can be minimized. The light load efficiency can be improved without compromising the EMI filter size. Then, adaptive frequency controlled PFC is proposed to further improve the PFC light load efficiency. The proposed light load efficiency improvement strategies are combined and implemented on the platform of the digital controlled 4-channel PFC. The benefit of improving the light load efficiency is experimentally verified. The EMI performance is also evaluated with the EMI measurement results obtained from the PFC prototype.

Following the same approach explored, the benefits of interleaved boost converter can be further extended other applications, such as the boost converter in the Hybrid Electric Vehicles (HEV) and photovoltaic (PV) system.

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