Chapter 2. Design and development of the Dimple Array interconnect

2.1 Prior arts of dimpled structures in microelectronic assemblies

A quick search in the United State Patent archives rendered a wealth of information in regards to the usefulness of the dimpled structures in microelectronics devices and systems.

US Patent 6,284,563 (Joseph Fjelstad) describes a method of making compliant microelectronic assemblies. This technique introduces a compliant layer (140) with a number of concave areas on top of a microelectronic element. Conductive flexible bond ribbons (175) are plated in these concave areas and extend to the periphery of the device. Electrical contacts can be formed with precision by placing solder balls within these areas that are then reflowed to attach the package to a substrate. The function of the concave dimples is to form the interconnection and to precisely retain the solder balls in the cup-like areas.

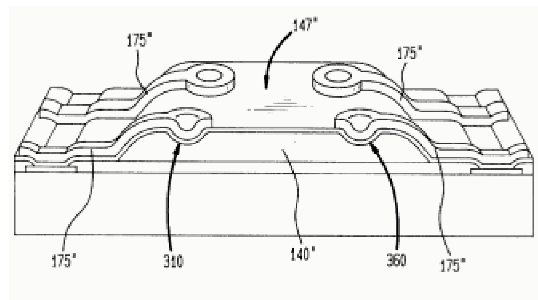


Figure 2.1 US Patent 6,284,563: compliant microelectronic assemblies.

In one United States Patent application (US 2001/0041370 A1) (Mike Brooks & Walter L. Moden), a method is described for fabricating a semiconductor package with a heat sink: A dimpled structure (14S) is stamped in the heat sink (10) and attached to the package. This method facilitates the assembly of the heat sink to the board (28). The function of the dimple in this patent is thermal conduction and attachment of the heat sink to the board.

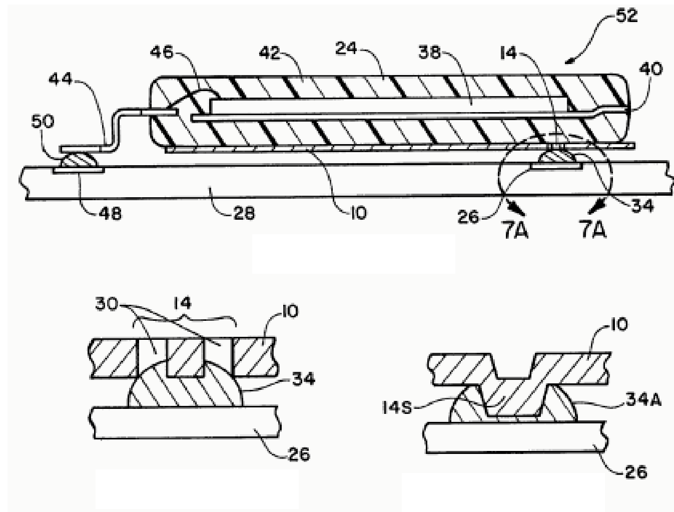


Figure 2.2 US Patent application 2001/0041370: A method for fabricating a semiconductor package with a heat sink.

In the United States Patent application 2001/0045643 (Yoshitsugu Katoh, Shinya Nakaseko, and Takashi Hozumi), a lid element (36G or 36H) has an adhesive contact with a semiconductor device package (24). In order to counteract the thermal stresses applied to both the lid and the package, the lid has a number of dimpled structures that force the lid material to deform. The main function of the dimples in this application is stress-relief.

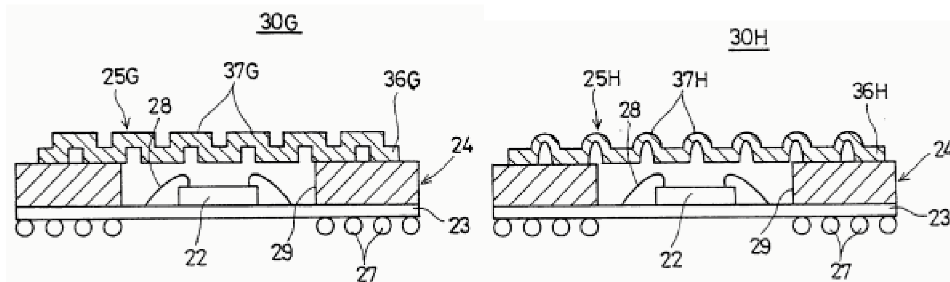
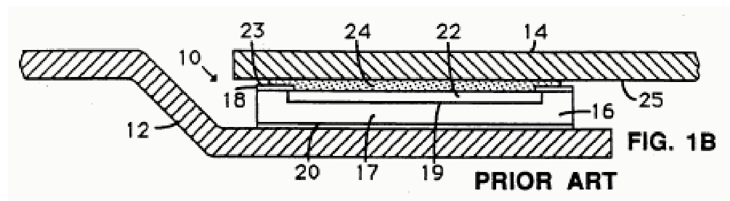


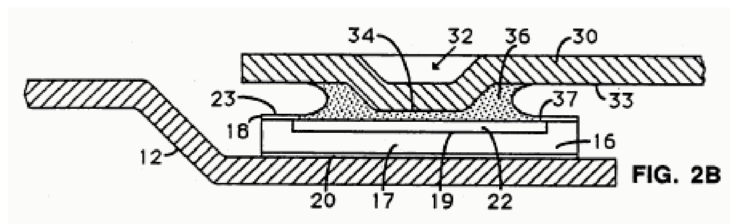
Figure 2.3 US Patent application 2001/0045643: A stress-relief structure for the semiconductor package.

United States Patent 5,110,761 (Martin Kalfus and Eugene L. Foutz) describes a method to form top contact for non-flat semiconductor devices. In the original configuration (Figure 2.4), solder connecting a flat metal lead (14) to a non-flat device (16) will result in an undesired cross-bridge between the metal lead and the raised device dielectric

region (18). In the case of excessive solder, shorting between the device PN junction is likely to occur (Figure 2.4 (a)). By forming a contact dimple (32) on the metal lead, the air spacing between the lead surface (33) and the device surface (23) can be adjusted using different dimple curvature and depth. Figure 2.4 (b) and (c) illustrate two of the suggested dimple shapes. The main function of the dimple in this patent is to increase the solder standoff height and avoid die-edge shorting.



(a)



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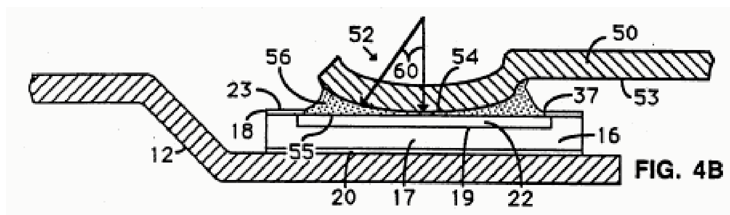


(c)

Figure 2.4 US Patent 5,110,761, method to form top contact for non-flat semiconductor devices: (a) flat metal lead interconnection; (b) and (c) dimpled metal lead interconnection.

The dimpled plate, as described in United States Patent application 2001/0028109 (Kozo Shimizu, Masayuki Ochiai, Yasuo Yamagishi), can be used to form solder balls in an area array format, which is then transferred to a substrate prepared for flip chip bonding. Figure 2.5 shows the flowchart of this flip chip bonding process. The function of the

dimpled plate in this method is positioning the solder paste and reflow and transfer of the solder balls.

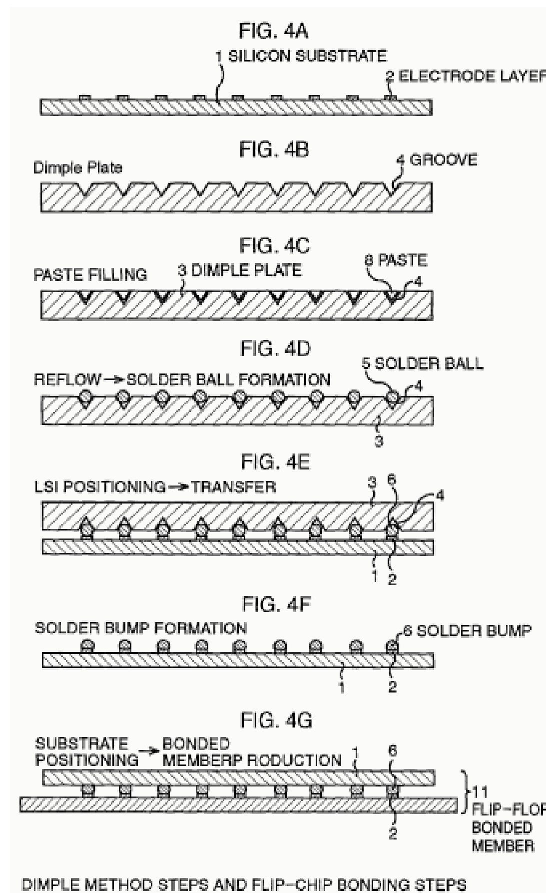


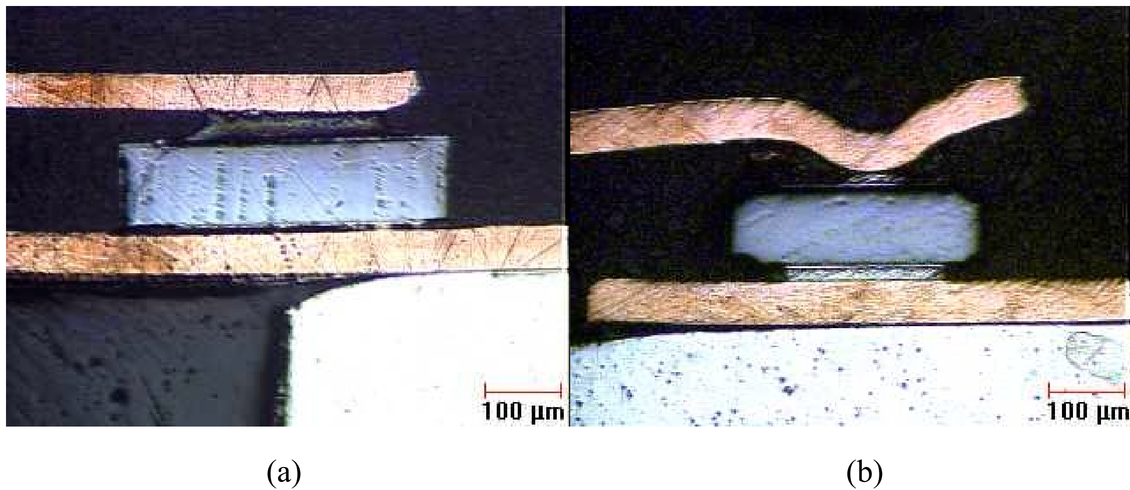
Figure 2.5 US Patent application 2001/0028109: A method for area array flip chip bonding.

In summary, in the found patents and applications, dimpled structures play key roles in implementing these innovative methods for fabricating microelectronic devices and packages. The roles of the dimple are summarized in Table 2.1.

In addition to the above-referenced patents, a series of patent-claimed power packages, the Powermite® from Microsemi, eliminate the wire bond; instead using copper strap with an extended portion to allow for the formation of solder fillets during the surface-mounted reflow process, “adding a significant amount of thermal dissipation capability” [51]. This technique also reduces high-frequency losses and dramatically increases surge ratings as compared to the wire-bonded packages (Figure 2.6).

Table 2.1 Dimpled structures in US patents and patent applications.

US Patent	*Roles of dimples*
6,284,563 (2001)	Form interconnection on a compliant layer, define solder ball location
0,041,370 (2001 Application)	Thermal connection and heat sink attachment
0,045,643 (2001 Application)	Stress-relief and improved package compliance
5,110,761 (1992)	Form top contact for non-flat device
0,028,109 (2001 Application)	Reflow and transfer area array solder balls for flip chip application



(a) (b)

Figure 2.6 Metallographic images of Powermite® packages (a) flat copper strap; and (b) dimpled copper strap.

Having realized the advantages of using the dimple structure for improved compliance, easier alignment, extra standoff height, and good thermal performance, this research aggressively extends the dimple structure to power semiconductor packaging, including discrete components and multichip modules. The feasibility of the DAI for these applications is fully demonstrated in this thesis work.

2.2 Investigation of the DAI for power semiconductor devices and modules

In this research, another dimpled structure, the DAI, has been applied to the packaging of power semiconductor devices and modules. The DAI packaging concept is illustrated in Figure 2.7. Devices are first attached to a base plate using high-melting temperature solder. A solderable metal strap or flex sheet is stamped with an array of dimple structures, which are then aligned with dispensed low-melting temperature solder paste on silicon devices for the second reflow. This method requires no solder mask to define the pad and the solder is naturally confined around the dimple region. Interconnection between the metal strap and the package leads is accomplished at the second reflow. The package is then encapsulated with a polymer underfill and glob-top.

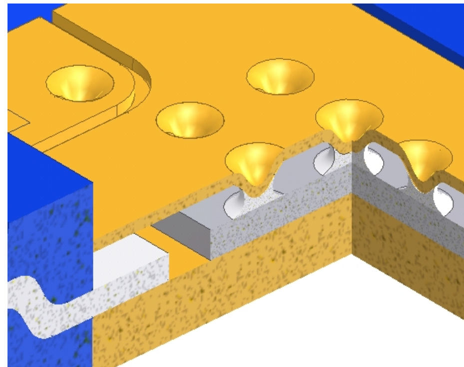


Figure 2.7 Artistic view of the Dimple Array interconnected package.

The DAI packaging is also one of the under-developed 3D packaging approaches for IPEMs currently being pursued at CPES. Other 3D packaging technologies being evaluated include the GE Power Overlay, the Embedded Power, and the flip chip on flex technologies, as mentioned in Chapter 1. Significant improvements in reliability as well as electrical and thermal performances are expected by taking a system approach with a multi-disciplinary effort in integrating these 3D active modules with the integrated passive components.

In order to meet the performance goals when designing the DAI packages, a few critical issues, such as current handling capability, thermal performance, parasitic inductance and capacitance, and interconnect materials, need to be carefully considered.

2.2.1 Current handling capability

A major difference between the IC interconnects and those in power packages is the requirement of current handling capability. Power devices using conventional aluminum wires have a very limited surge rating due to the small contact area between the wire bond and the chip. Excessive current level often results in hot spots and fusion of bond wires [39]. Figure 2.8 shows the variations of temperature in a power device [52]. As much as ~20°C difference in the die temperature was observed across the device area. The advantage of being able to implement high I/O count in area array solder bumping for IC packaging may be used to increase the portion of the conductive contact area between the interconnect and the device, therefore improving current handling capability and minimizing the non-uniformity in temperature distribution.

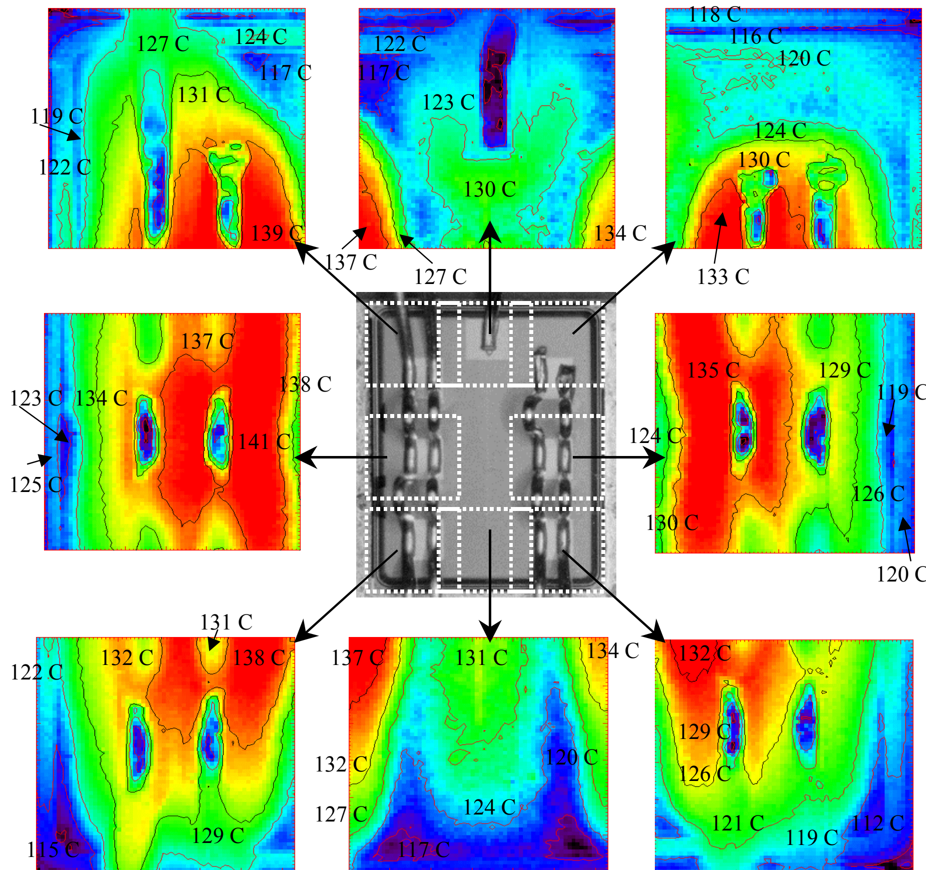


Figure 2.8 Infrared microscopy image of the temperature distribution of a power transistor interconnected by wire bonds.

Figure 2.9 shows a comparison of the contact geometry of wire bond and area array solder bump interconnects [53]. Wire bonds have a much smaller contact area, as shown in this figure. The only way to change this situation is to replace the thick bond wires with a greater number of thinner ones, which requires significantly increased processing time and labor due to the sequential bonding process. Being an alternative area array solder bumping technology, the DAI technique has significantly larger contact area than the wire bonds. For even higher contact area ratio, increasing the number of the solder contact pads and reducing the pitch can be painlessly achieved utilizing standard wafer-level processing without affecting processing time, since all solder bumps are reflowed at the same time.

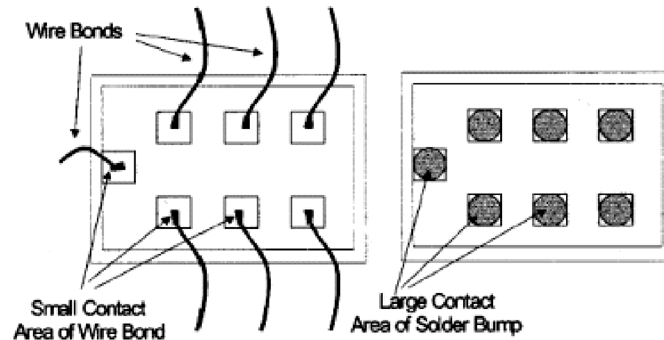


Figure 2.9 Comparison of contact geometry of wire bond and flip chip interconnects.

2.2.2 Thermal

In IC packaging, flip chip technology is undoubtedly the most desirable package technology in the industry today when cooling considerations are important [54]. A 50% increase in power dissipation capability using BGA interconnections can be achieved over those using Pin Grid Array (PGA). Furthermore, the structure of the area array solder bumping allows for easy implementation of a variety of internal and external thermal enhancement techniques. It becomes apparent that if wire bonds can be eliminated from the power package and using area array solder bumping similar benefits can be achieved.

In the power semiconductor industry, one of the key approaches to enhancing thermal characteristics is a reduction in junction-to-ambient thermal resistance [55]. To achieve this, the number of thermal interfaces that the heat has to go through from the device to the ambient must be reduced. Another important aspect is the reduction in package-related resistance in order to achieve a lower on-resistance $R_{DS(on)}$, and therefore a lower power loss due to packaging. An example is Fairchild's flip chip in a leaded molded package (FLMP) also known as the "Bottomless SO-8" package. Figure 2.10 shows a comparison between the conventional wire bond SOIC-8 package and the FLMP SOIC-8 package. Thermal resistance is reduced due to the elimination of die-to-paddle clearance to expose the drain side of the device, and package resistance has been reduced from 3mohm to 0.5mohm by using the flip chip (80% improvement). Another package from this company using BGA technology for MOSFETs brings about a 40 to 80% improvement in junction-to-ambient thermal resistance over other leaded surface-mounted packages [56].

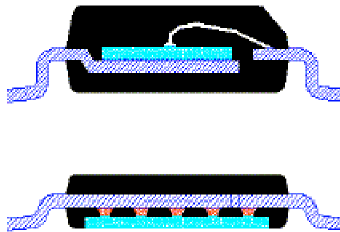


Figure 2.10 Conventional wire bond SOIC-8 (top) and the FLMP SOIC-8 package (bottom) (reprinted with permission of Rajeev Joshi, Fairchild Semiconductor).

Compared with the flip chip package, the DAI package further reduces the interconnect length, i.e., the height of the solder bumps, and brings the junction even closer to the convective fluid. Figure 2.11 shows a comparison of the electrical resistance and the thermal resistance of wire bond (3mm long, 10 mil in diameter), flip chip solder joint (1mm tall, 1 mm cross-section area), and the DAI solder joint (0.33 mm tall, 1 mm cross-section area) that are necessary for packaging a particular type of power devices. Significant improvement is found in electrical and thermal resistance per bond in flip chip and the DAI solder joint. A DAI solder joint further offers a 67% improvement in both Rth and resistance over a flip chip solder joint.

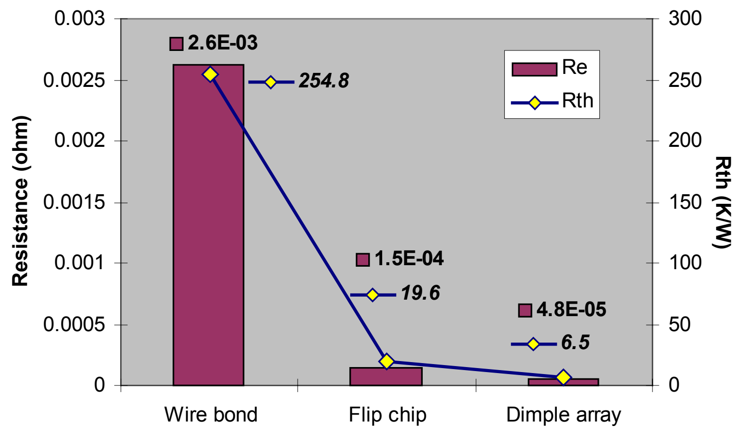


Figure 2.11 Comparison of the electrical and thermal resistance of individual wire bond, flip chip solder joint and the Dimple Array solder joint.

For high-power applications, however, where IGBT and MOSFET devices are typically mounted on DBC using large area soldering, the contribution of interconnect in thermal conductance is less than 1% that of the die-attached solder. However, by applying proper double-sided cooling, a thermal improvement of as much as 30% can be achieved [57].

2.2.3 Parasitics

Interconnect parasitics, one of the key parameters in determining electrical performance of a module, depends heavily on the interconnect technique and the module layout design. A major impact of large interconnect parasitic inductance in a fast-switching circuit is the voltage overshoot that may exceed the device rating and thus damage the device. In the wire bond packages, the self-inductance of the wire bonds and the lead frames is rather large, and the mutual inductance between the parallel wire bonds can cause uneven current distribution, which is often known as the proximity effects [58].

The DAI significantly reduces loop inductance by eliminating wire bonds and shortening leads connecting to the power device. Since both the self-inductance and the mutual inductance have been dramatically reduced in the DAI modules, the proximity effects are minimized.

Capacitive effects, on the other hand, may cause a different type of damage, such as the common mode EMI [50]. Electrical modeling using Maxwell-3D® on a multilayer structure, i.e., the Embedded Power module, suggested that parasitic capacitance can be significant and harmful to the module performance. In the DAI package, the distance between two parallel conductive planes, such as the source and the drain of a power MOSFET, can be adjusted using dimples of different heights, and thus can minimize the capacitive effects.

2.2.4 Interconnect materials

Among available choices of interconnect materials, including silver, copper, Alloy 42, and aluminum, copper appears to be the best fit because of its availability, low cost, high electrical conductivity and high thermal conductivity. A comparison of material properties of Cu, Ag, Alloy 42 and Al is given in Table 2.2 [59,60].

Table 2.2 Properties for various interconnect materials.

	Thermal conductivity k (W/m-K)	*Electrical (dc) resistivity ρ (Ω-m)*	*Young's modulus E (GPa)*	*CTE (/ppm-^{o}C)*	*Skin depths δ_s (μm) at 1GHz*
Copper	393	1.7×10^{-8}	135	17	2.09
Aluminum	240	4.3×10^{-8}	70	23	2.64
Alloy 42	10.5	6.1×10^{-7}		5.3	2.1
Silver	419	1.6×10^{-8}	76	19.6	2.03

Silver has superior electrical conductivity that reduces lead resistance. Silver also has an excellent elongation and low modulus good for building a compliant interconnect structure. However, silver is much more expensive than other lead frame materials.

Alloy 42 (A nickel-iron controlled-expansion alloy contains 42% nickel [60]), a commonly used lead frame material for ceramic-to-metal and glass-to-metal seals, has a controlled, low coefficient of thermal expansion from room temperature to about 570°F

(300°C). Its iron content serves as the remainder, and its nickel content is adjusted to meet expansion requirements.

Aluminum is the only non-solderable material considered. Like wire bonding and aluminum ribbon bonding, an aluminum DAI can be ultrasonically bonded to power semiconductor devices [61]. Due to the limited time for this research, this bonding method is not discussed.

Another important consideration in determining the interconnect material is the frequency effects of different metals. The frequency effects, also known as "skin effects," are closely related to the internal mutual inductance inherent in a conductor, which forces the current to concentrate near the surface of a conductor to reduce the total inductance when the frequency increases [62]. The skin depth δ_s, defined as the distance from the surface where the current is equal to 1/e of its surface value, is given by:

$$\delta_s = \sqrt{\frac{\rho}{\pi \mu f}} \qquad \text{(Eq. 2.1)}$$

where

$\rho =$ the resistivity of the conductor

$\mu =$ the magnetic permeability of the conductor

$f =$ the frequency

Figure 2.12 gives the measured inductance and resistance as a function of frequency for some lead frame materials [62]. Alloy 42 has a very high inductance at frequencies of less than 0.5 MHz. This is because Alloy 42 is a magnetic material with a permeability greater than 1. Even so, it continues to be used as a lead frame conductor because at high frequencies (> 100 MHz), its internal inductance is not much larger than the copper because the skin depth becomes so thin. The resistance of Alloy 42, however, increases constantly when the frequency increases. The onset of these effects occurs at roughly 0.5MHz. Therefore, when choosing an interconnect material, the application frequency

range must be considered. For many power electronics applications in which the frequency is less than 0.5MHz, Alloy 42 is not a desirable interconnect material.

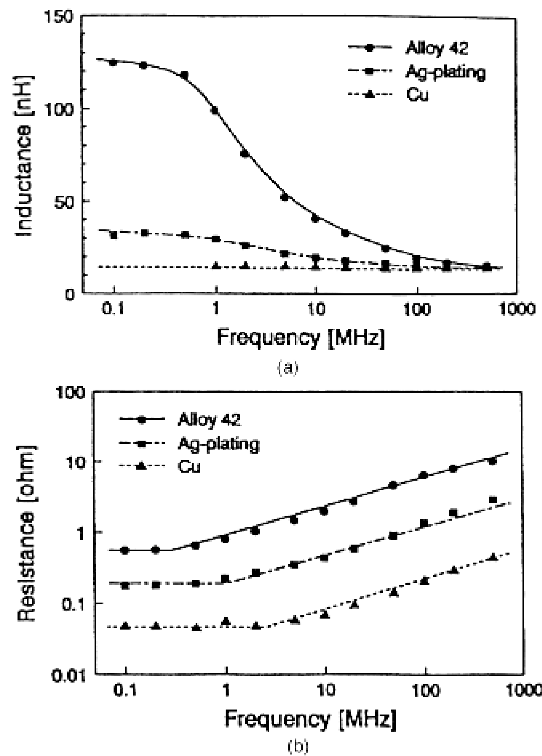


Figure 2.12 Inductance (a) and resistance (b) of some lead frame materials as a function of frequency (reprinted with permission of Kluwer Academic Publishers).

2.2.5 Solder alloy systems

Eutectic Pb-Sn solder alloys have been used for many years in the electronics industry to conveniently join two solderable parts at relatively low processing temperature ranges. With the continuous growth of the complexity of electronic assemblies, multiple reflows are generally required. This drives the development of many other lead-based solder alloys with non-eutectic mixtures of Pb and Sn. In addition, industry's move for lead-free solders makes the use of ternary alloys increasingly important. Figure 2.13 [63] shows the phase diagram of some of the most commonly used solder systems: Sn-Pb (183-302°C), Sn96.5-Ag (221 °C), Sn93.6-Ag4.7-Cu (217 °C), and Sn42-Bi (138 °C).

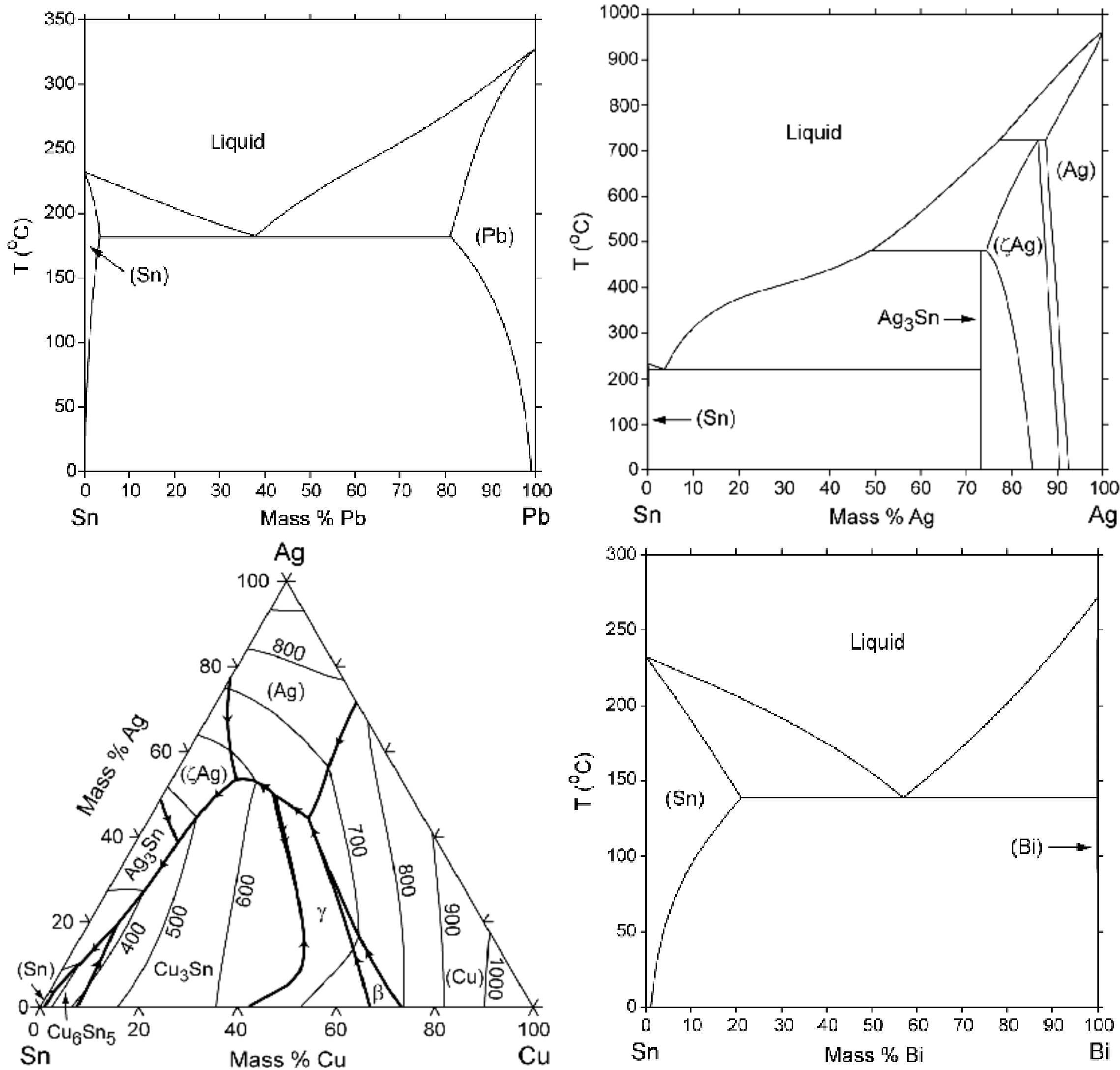


Figure 2.13 Phase diagrams of some solder alloy systems.

Solder selection is of significant importance to the development of the assembly process of power electronic modules.

- First, some flip chip bumping processes use two or more solder alloys with various melting temperatures [30]. This potentially complicates the fabrication process.
- Secondly, no two types of solders can be joined together without side-effects. For instance, reflowing high-lead-content solder, such as Pb90-Sn10 solder ($T_{liquidus}$ = 302 ^oC, and $T_{melting}$ = 268^oC) with a high-tin-content solder, such as eutectic Sn-Ag solder ($T_{melting}$ = 221 ^oC), will result in the formation of undesirable eutectic Pb-Sn solder at

the interface, which leads to collapse of the solder joint at reflow temperature. IBM is using a high-tin-content solder (Sb5-Sn95) to join the Pb90-Sn10 solder at the ceramic substrate side for their ceramic column grid array (CCGA) interconnection. In order to prevent mixing of these two solders at the interface, the column is coated with a Cu-Sn barrier layer [64] (Figure 2.14).

- Thirdly, using lead-free solder sets many technical challenges. Eutectic lead-tin (Pb37-Sn63) solder has a melting temperature of 183°C. In contrast, essentially all the proposed lead-free solders have a much higher tin content and a raised liquidus [65]. The problem is that these two factors accelerate the reaction between solder and the UBM.

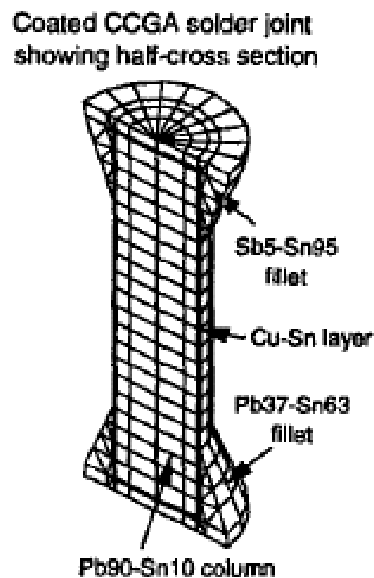


Figure 2.14 FEM model of IBM's ceramic column grid array interconnection with coated solder columns.

The Dimple Array solder joint uses copper dimples to support standoff height of the solder joint. Therefore only one type of solder material is needed. This substantially broadens the choices for solder systems and simplifies the fabrication process.

Other than the difference in melting point, solders differ substantially in thermal and mechanical properties. Thermal and mechanical properties and fatigue reliability (as CBGA package fillets) of some solder systems are listed in Table 2.3 [66].

Table 2.3 Properties of some solder materials.

Solder fillet (32mm CBGA, 0/100 °C)		*Pb37-Sn63*	*Zn9-Sn91*	*Ag3.5-Sn96.5*	*Sb5-Sn95*
Melting temperature (°C)		183	199	221	238
Thermal conductivity (W/m-K)		51	NA	33	28
CTE (ppm/°C)		25	23	22-28.7	22-29.6
Surface tension (mN/m)	Air	417	518	431	468
	N_2	464	487	493	495
Contact angle (degree)		17±4	58±1	41±3	43±4
Flux		RMA	RMA	RMA/RA	RMA
Wettability		Excellent	Poor-fair	Fair-good	Fair-good
Plastic resistance		1 x	0.34 x	0.37 x	0.19 x
Creep resistance		1 x	2.30 x	2.03 x	1.97 x
Viscoplastic resistance		1 x	1.76 x	1.64 x	1.31 x
Thermal fatigue resistance		1 x	3.01 x	2.62 x	1.69 x
Micro coarsening resistance		Weak	Strong	Strong	Strong
Cost ($/lb) raw/ingot		1.34/3.75	1.86/NA	4.58/8.04	1.94/NA
Toxicity		High	Low	Low	Low (?)

This table shows that the eutectic Sn-Ag solder has less plastic resistance but is more than two times stronger against creep than the eutectic Pb-Sn solder. These results were based on finite element modeling of CBGA packages using a Pb90-Sn10 solder ball and various solders for fillet material. The scope of this study will still focus on the reliability evaluation of the eutectic Sn-Pb solder, although attempts will be made to study the performance of the eutectic Sn-Ag solder as a power device interconnect.

2.2.6 Shape design

Although the Dimple Array solder joints are easier to fabricate than the CCB solder joints due to the elimination of solder masking steps, the solder shape is more complicated. Figure 2.15 shows the geometrical parameters of the DAI assembly. The standoff height of the solder, h, depends heavily on the weight of the copper interconnect. For maintaining sufficient standoff height, a fixture or spacer may be used for external support during reflow. The dimple height t2 is also critical for the formation of good quality solder joints.

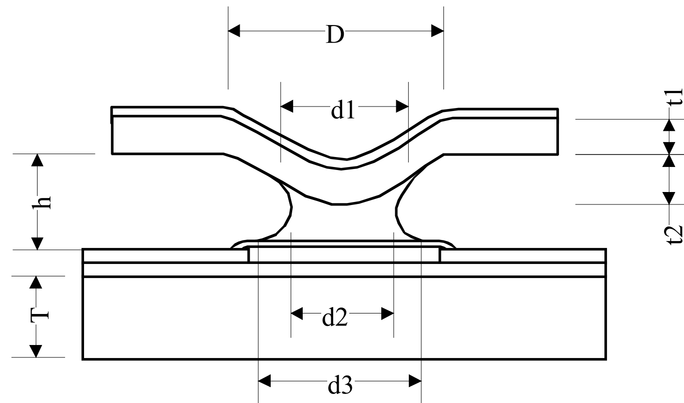


Figure 2.15 Shape parameters of the Dimple Array solder joint.

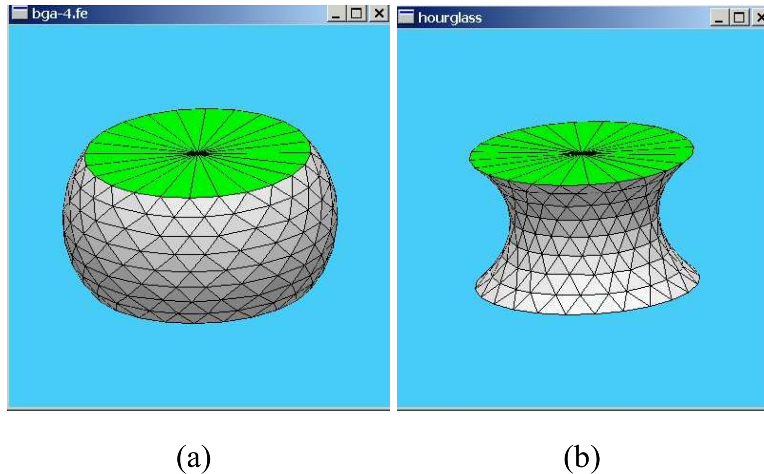
Solder joint shapes were found to be closely related to solder joint reliability in past studies [67,49]. A few simplified methods to predict the reflow shape of the BGA and flip chip solder joints have been proposed, including:

- The truncated sphere method;
- The force-balanced analytical solution [68]; and
- The energy-based method.

The truncated sphere method, being a purely geometric approximation, assumes that the solder bump after reflow is a perfect sphere truncated at one side or at both top and bottom. It is easy to derive the standoff height and the diameter of the solder ball, once the pad diameters and the volume of the solder are known. The forced-balanced analytical solution includes the consideration of the surface tension of liquid solder and assumes that the meridian defining the free surface of the solder joint is approximated by a circular arc. The energy-based method considers more of the realistic effects such as surface tension, gravity and internal/external pressures. This method appears to be a more reliable way to estimate the BGA solder joint. In this investigation, attempts were made to use this method for prediction of the Dimple Array solder joint shape.

The Surface Evolver [69] is a handy software package that allows for full 3D simulation of the BGA solder joint shape by defining an initial surface. The Evolver then evolves the surface toward minimal energy, and when necessary, discretizes the surface into

interconnected smaller triangular facets. Figure 2.16 (a) and (b) show the prediction of a BGA solder joint between two circular pads. In the compression force case (a), the solder joint is a barrel shape. In the tension case (b), it is a stretched hourglass shape.



(a) (b)

Figure 2.16 BGA solder joints shape prediction using Surface Evolver: (a) barrel shape solder joint and (b) hourglass shape solder joint.

Figure 2.17 shows the evolution of the solder surface between a half sphere (representing the copper dimple), and the bottom circular pad. It is clearly shown that due to the wetting of the solder to the dimple (sphere), the solder wetting area at the bottom pad shrinks for minimum surface energy, even though the gravitational effect and the wetting to the bottom pad tend to spread out solder to cover the whole pad. It is necessary to point out that in the dimple case, in spite of the compressive force exerted on the solder (from the weight of the copper dimple), an hourglass shape is formed.

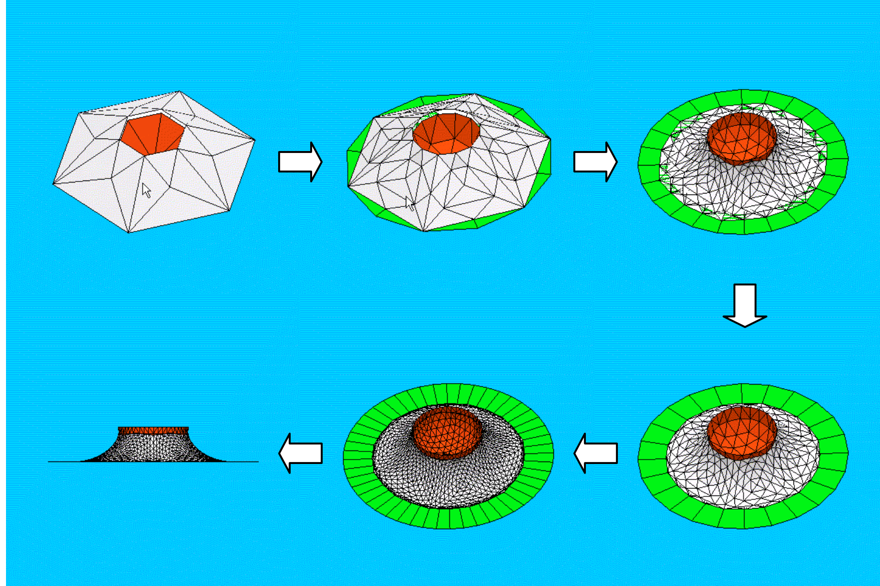


Figure 2.17 Dimple solder joint shape evolution as predicted by Surface Evolver.

2.3 Design of the Dimple Array solder joints for improved reliability

Solder joint fatigue in real applications is mainly caused by a global CTE mismatch between the substrate and the silicon chip. A first-order estimation of the fatigue life based on the Coffin-Manson low-cycle fatigue model is given by D.S. Patterson, et al. [70], in Figure 2.18.

Figure 2.18 A first-order estimation of the fatigue life of solder joints.

As shown in Figure 2.18, the solder bump is off from the center of the package by Le, the solder joint standoff height is h, and the Coffin-Manson equation relates the median fatigue life in cycles N_f with plastic shear strain range $\Delta\gamma = \frac{Le}{h}\left|(\Delta\alpha \cdot \Delta T)\right|$ by:

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f^{'}}\right)^{\frac{1}{c}} \qquad \text{(Eq. 2.2)}$$

where $\varepsilon_f^{'}$ is the fatigue ductility coefficient, and c is the fatigue ductility exponent ~ -0.5 for flip chip solder joints. Therefore, $N_f \propto (\frac{h}{Le \cdot \Delta\alpha \cdot \Delta T})^2$. This simple first-order approximation suggests that increase of solder standoff height, reduction of die size, finding a more CTE-compatible material system (smaller $\Delta\alpha$), and better thermal management (a smaller ΔT) will be the basic approaches to improving the reliability of area array flip chip solder joints.

2.3.1 Documented approaches for improving solder joint reliability

2.3.1.1 Geometry design of solder joints

Reported improvements have been achieved mainly from the increase of the solder joint standoff height, and thus improved compliance. Among these efforts are IBM's column grid array, Motorola's double-bump, Technical University of Berlin's S3-Diepack, self-stretching technology from Japan, and Motorola's mechatronics power package.

- Ceramic column grid array

A series of papers were published by IBM researchers in the 1990s [71,72,73]. Figure 2.19 shows the configuration of the ceramic column grid array (CCGA) in comparison with a ceramic ball grid array (CBGA).

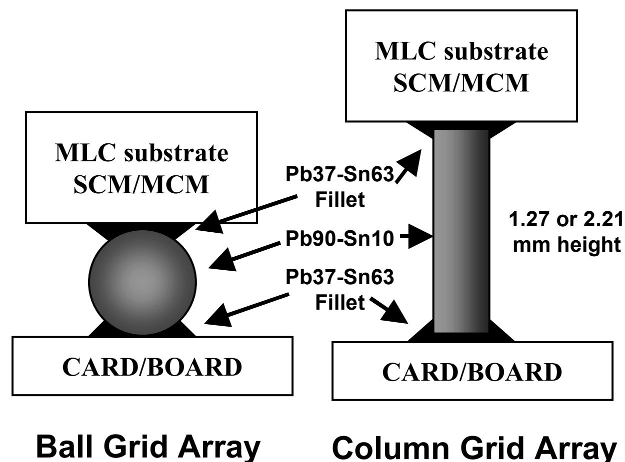


Figure 2.19 IBM's BGA and column grid array.

CCGA increases thermal fatigue reliability by up to tenfold as compared to CBGA packages. For ceramic substrate (MLC) size larger than 32 mm CCGA is recommended. For telecommunication systems or workstations, even a 25mm package size needs CCGA to meet the reliability requirement. Figure 2.20 gives the cumulative fails as a function of number of thermal cycling at –55/125°C and 0/100°C, respectively [74].

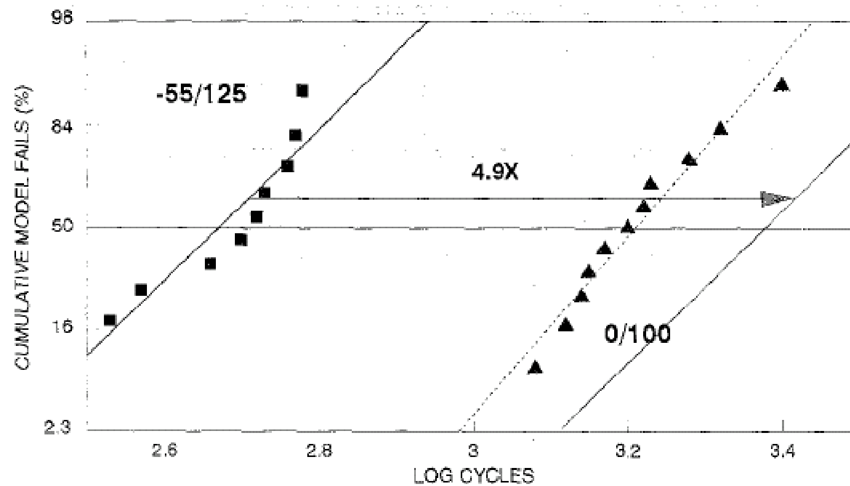


Figure 2.20 Fatigue of 50mil solder columns subjected to –55/125°C thermal cycles.

From the data obtained from thermal cycling test at –55/125°C condition, a linear-fit was performed. This curve was then correlated with FEM modeling to set up an empirical lifetime equation. This equation was used to predict the cumulative model fails trend for 0/100°C test, which turned out to be a 4.9x improvement. The dotted line denotes the linear-fit curve from experimental data from the 0/100°C thermal cycling test.

- Double-bump

Motorola's wafer-level chip scale packaging (WL-CSP) is an encapsulated double-bump technology [75,76,77,78]. This technology not only eliminates the underfill process, but also provides extra thermomechanical stress relief using a wafer-level encapsulation process and the attachment of a second solder bump to create a double-bump structure, as shown in Figure 2.21.

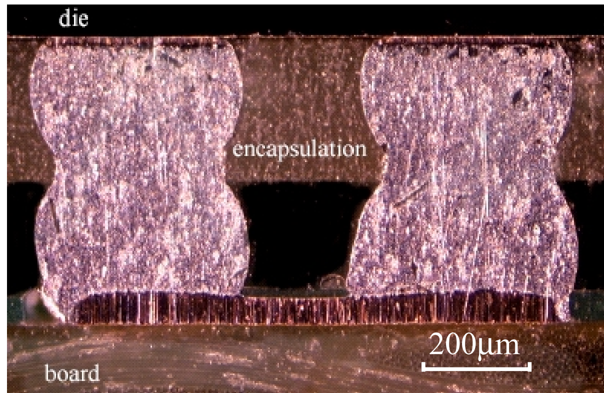


Figure 2.21 Double-bump structure in Motorola's wafer-level chip scale package (courtesy of Motorola, magnification was estimated).

The process flow is shown in Figure 2.22. A TiW:Cu seed layer is sputtered on the redistribution BCB dielectric and pad openings on the wafer. Photoresist is coated to define opening pads on this seed layer. After electroplating the copper, the photoresist is stripped and the Cu and TiW are etched. Flux is then stencil-printed onto the wafer and preformed solder balls are dropped onto the wafer, reflowed, and cleaned. Next, the encapsulation layer is stencil-printed onto the wafer, and the openings to the first level of bumps are patterned. The wafer is fluxed again, preformed solder balls are dropped, reflowed, and cleaned, and then the encapsulation layer is cured.

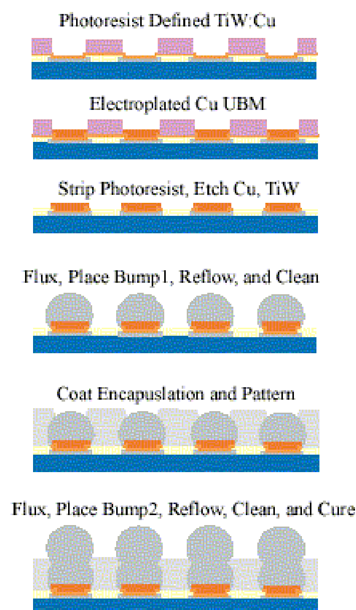


Figure 2.22 Motorola's wafer-level chip scale packaging processing (courtesy of Motorola).

Motorola's initial double-bump approach used a stencil-printing process for both levels of solder bumps with a collapse height of 330 μm. The first failure was found at 200 cycles in air-to-air thermal cycling of -55 to 125°C and 60% of the parts failed after 600 cycles. After increasing the standoff height of the second-level solder bumps by using large preformed solder balls, the collapse height becomes 425 μm and first failure was found after 800 cycles. Only 20% failed after 1000 cycles. The latest processing used preformed solder balls in both levels of solder bump formation, therefore further increasing collapse height.

- S3-Diepack

Simon, et al. at Technical University of Berlin developed the S3-Diepack process for wafer-level CSP [79,80]. The redistributed area array pads are in a 0.5mm pitch using polyimide or BCB as the dielectric layer. A first layer of solder spheres with a diameter of 300 μm is reflowed. The solder balls are reinforced by a solder support structure (S3) using a filled epoxy, which prevents the collapse of the solder balls in the second reflow. The package is then polished to expose a flat solder surface for the second layer of solder attachment. Figure 2.23 shows the cross-section of the S3-Diepack.

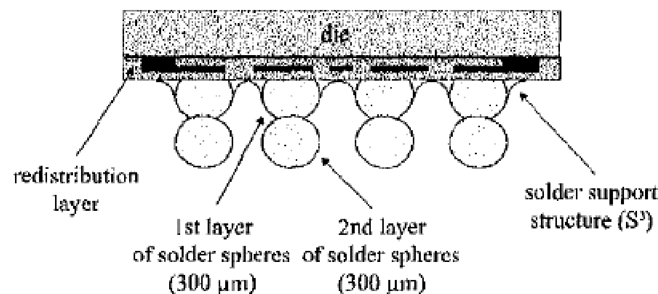
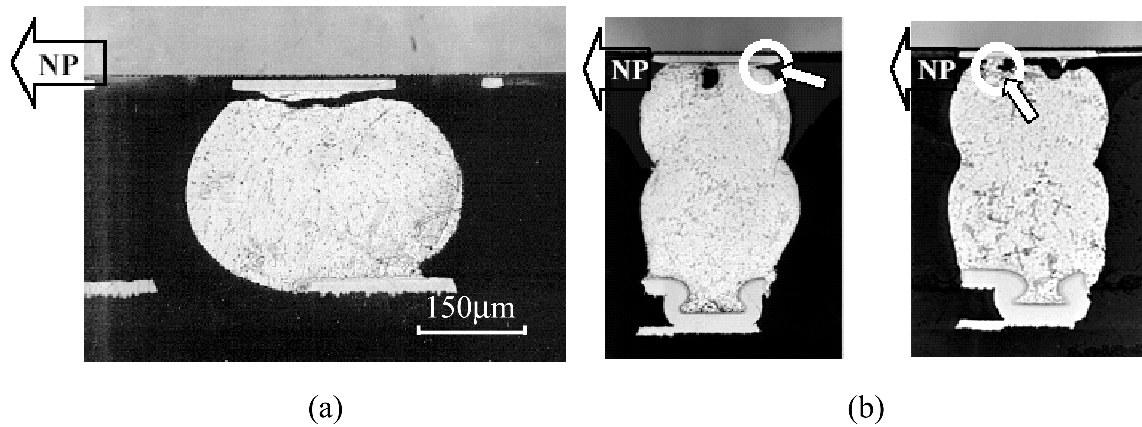


Figure 2.23 S3-Diepack schematics.

Reliability testing of the S3-Diepack WL-CSP is reported. For the conventional WLCSP (Figure 3.14 (a)), after 200 thermal cycles, crack propagates through the chip and solder joints. The S3-Diepack (Figure 2.24) shows the first crack (white arrows) after 500 cycles and the crack after 700 cycles.

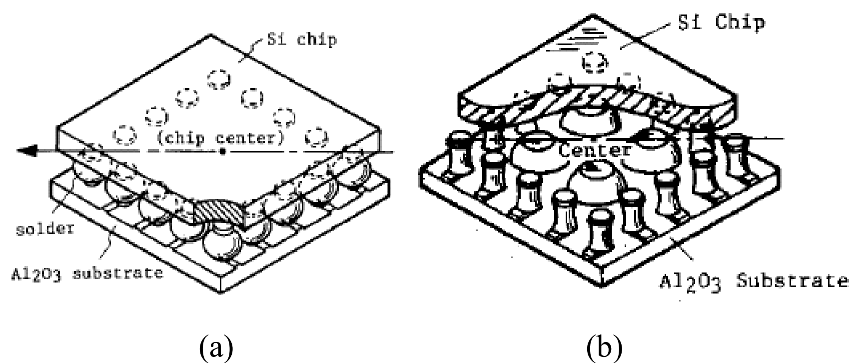


(a) (b)

Figure 2.24 Failure modes of the conventional WLCSP (a) and the S3-Diepacks (b).

- Self-stretching technology

The self-stretching flip chip package is shown in Figure 2.25 (b) [49]. A solder paste with a slightly higher melting temperature than the eutectic tin-lead solder is dispensed in the center. During reflow, the eutectic solder melts and forms solder bumps in the periphery of the chip, then the inner solder melts, forming high-standoff solder balls, which push the silicon chip upward and thus stretch the edge joints. At the cooling stage, the high-standoff-height solder balls solidify first, supporting the silicon chip so that the edge joints will retain the hour-glass shape.



(a) (b)

Figure 2.25 Comparison of flip chip structures: (a) CCB; and (b) SST solder joints.

Reliability testing of the SST package showed a threefold improvement in fatigue reliability over the barrel-shaped CCB solder joints.

- Solder fillet

Motorola has been using a soldered backside clip attachment to connect the flip chip MOSFET drain in their multichip Mechatronics power packages for automotive applications [81]. In order to reduce the stress concentration at the solder joint corner, a U-shaped copper strap is used to form a solder fillet between the copper clip and the backside of the die (Figure 2.26).

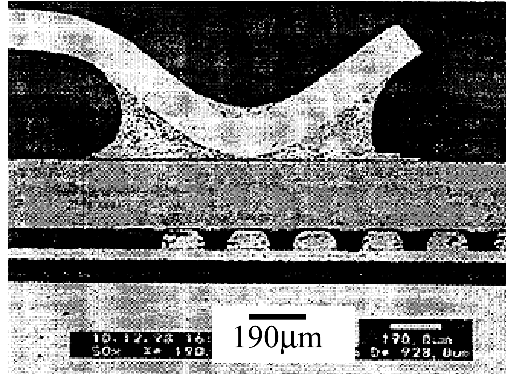


Figure 2.26 Backside clip attachment of Mechatronics power packages from Motorola.

2.3.1.2 Underfill

It is a common practice in industry to use underfill to improve flip chip and board-level BGA reliability. As manufacturing cost drives the size of the BGA package smaller and smaller, the solder joint pitch and standoff heights get smaller, too. Reliability concerns are raised due to the reduced compliance in the package. To explore whether the existing underfill process helps the BGA package meet board-level reliability requirement, T. Burnette, et al. [82] studied the reliability of fine-pitch plastic BGA packages (232- and 280-lead flexBGA and 196-lead mold array process (MAP)) with various epoxy-based underfill materials that have different CTEs and moduli. The selected underfill properties at room temperature are listed in Table 2.4.

Thermal cycling experiments (-40 to 125°C) and numerical analysis were conducted to determine the optimum set of underfill properties. Non-underfilled packages were tested as a control. Epoxy D with a CTE of 26 ppm/K and a modulus of 5.5 GPa shows the best reliability compared with other systems. However, this is not the optimum set of underfill

properties. Parametric numerical modeling shows that a CTE of 15 ppm/K is the optimum property for board-level reliability.

Table 2.4 Properties of some underfill materials.

Epoxy	*CTE*	*E*	*Cure*
A	70 ppm/K	2.6 GPa	7 min/165°C
B	44	5.6	7 min/165°C
C	40	8.5	7 min/165°C
D	26	5.5	7 min/165°C
Control (non-underfilled)			

Chen, et al. [83] studied the effects of underfill material on the reliability of flip chip packages using FEA and an experimental procedures. In the experiment, two types of test chips with sizes of 5.6 x 6.4mm sq. (96 bumps with 203 μm pitch) and 6.3 x 6.3mm sq. (48 bumps with 457 μm pitch) were examined. Both test chips were bumped peripherally with eutectic 60Sn40Pb solder in a daisy-chain structure. The thermal cycling test cycles the samples from –55°C to 125°C with a ramp rate of 36°C/min and a dwell time of 25 min at peak temperatures. The failure of solder joints was detected by monitoring 10% decreases in electrical conductivity of the joints. The thermal fatigue lifetimes of the underfilled packages were about 20 times the level of those without underfill. The authors concluded, based on their FEM work, that this enhancement is due to the change of deformation mode from shear-dominated in the case without underfill to more uniform strain with package warpage for underfilled packages.

2.3.1.3 Plastic core solder balls

The stress relaxation approach has been taken by Okinaga, et al. at Sekisui Chemical Co. Ltd, Japan to improve the thermomechanical reliability of BGA and CSP packages. In this research, a plastic core is coated with solder material to form a bump that interconnects the ceramic package to the motherboard [84]. Reliability testing shows excellent structure compliance from the plastic core solder balls (PCSBs). Figure 2.27 shows different fatigue failure patterns in a plastic core solder ball (a) and a conventional BGA solder joint (b). Arrows point to the cracks in the solders.

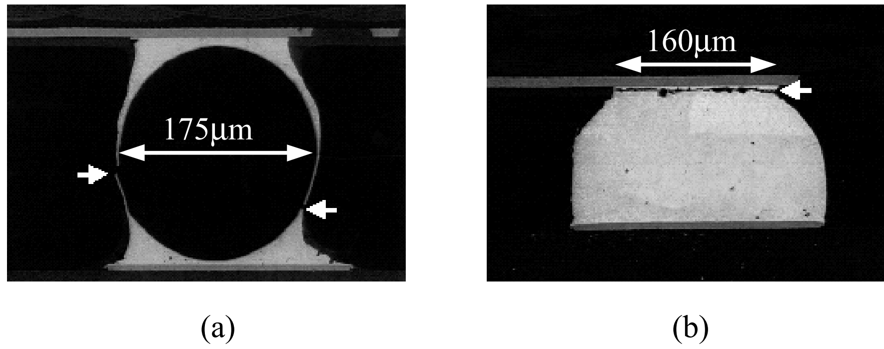


Figure 2.27 Fatigue failure modes for PCSB (a) and a conventional BGA solder joint (b).

Figure 2.28 shows the accumulated failure as a function of the number of cycles. A reliability improvement of six- to sevenfold is accomplished using the PCSB approach.

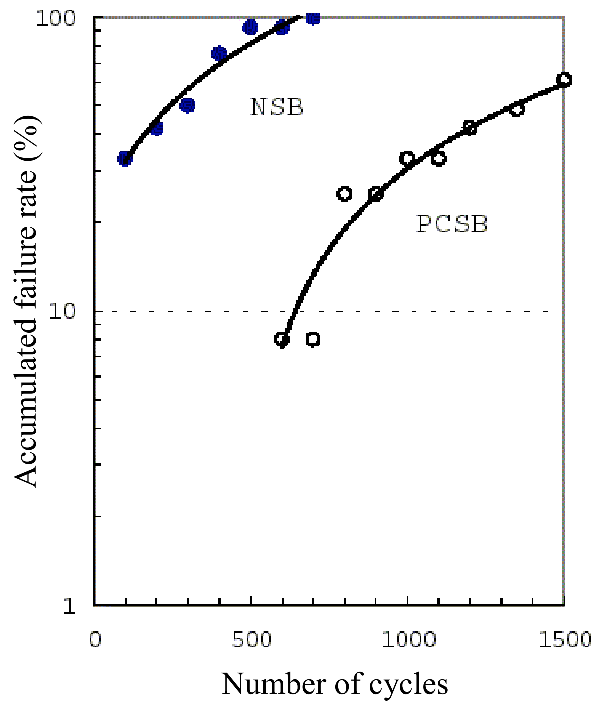
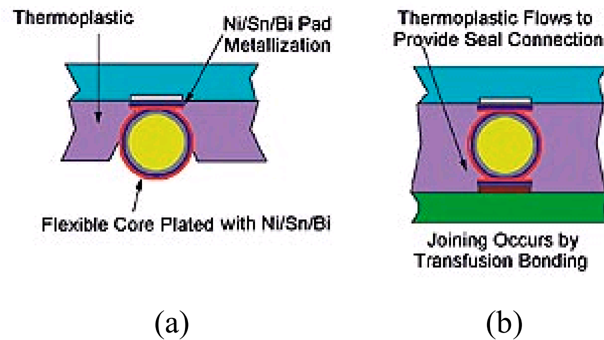


Figure 2.28 Accumulated fatigue failure rate of PCSBs and conventional BGA solder joints.

Nokia also patented a polymer core bump plated with Ni/Sn/Bi [85,86], as shown in Figure 2.29. The Ni is the barrier and adhesion layer while the Sn/Bi is the solderable layer. A thermoplastic resin is applied while the die are in wafer form. A transfusion bonding process which joins metals below their melting temperatures was used. During assembly, the package is heated and pressure is applied to facilitate the transfusion

bonding. Continued heating causes the thermoplastic underfill to flow around the solder bumps.



(a) (b)

Figure 2.29 Nokia's polymer core bump (a) and transfusion bonding process (b) (reprinted with permission of Chip Scale Review).

2.3.2 Design of the DAI reliability

Copper has been the preferred material in power electronics because of its excellent high-frequency performance, high conductivity and thermal conductivity, and good malleability. When using copper as the first-level interconnect material, however, there is a reliability concern because of the large CTE mismatch between the copper and the silicon.

Let's make a first-order estimation of the stress/strain in the solder. The CTE mismatch between the copper and the silicon $\Delta\alpha$ is about 13 ppm/K. Assuming that the distance from the edge solder joint to the neutral point L is 5 mm, Young's modulus of solder E is roughly 32GPa at room temperature and the poisson ratio ν of 0.36, $\Delta T = 100^{o}$C, and the solder-standoff height h of 0.5 mm, the shear modulus of the solder is:

$$G = \frac{E}{2(1+\nu)} = 11.8GPa \quad \text{(Eq. 2.3)}$$

(Data from another source: www.matweb.com: Sn63-Pb37: E=32Gpa, G=12GPa
Sn63-Pb37 high tensile strength: 43MPa, low shear strength: 37MPa;
Sn95-Ag5 low tensile strength: 32MPa, high shear strength: 73MPa;
Indalloy 121 Sn96.5-Ag3.5 tensile: 38.7MPa.)

The total shear strain due to temperature change is:

$$\gamma = \frac{\Delta\alpha \cdot L \cdot \Delta T}{h} = 0.013 \qquad \text{(Eq. 2.4)}$$

Therefore, the shear stress in the solder is:

$$\tau = G\gamma = 153MPa \qquad \text{(Eq. 2.5)}$$

For eutectic tin-lead solder, the shear strength is about 37MPa (in the uniaxial-tension test, the maximum shear stress τ_{max} occurs at the 45° direction. When eutectic solder yields at 43 MPa, τ_{max} is only 21.5MPa). Obviously, direct interconnection between the copper and the silicon for a medium-sized chip results in a large amount of plastic deformation in the solder joints, even though the above approximation over-simplifies the real condition. This calculation poses a serious reliability concern for using copper interconnect and flip chip solder joints to connect power devices.

For conventional controlled collapse bonded (CCB) solder joints, the situation is aggravated by the stress concentration at the structural singularity in the solder joint near the silicon. Figure 2.30 shows the analytical schematics of stress distribution for the solder joint (IBM 1969) [87]. As shown in Figure 2.30 (b), when the solder joint is distorted due to CTE mismatch between the substrate and the chip, shear stresses are imposed at both ends. For the momentum to be balanced, normal stresses must exist at the corner of the solder joint.

In the DAI, however, since a copper dimple is used to prevent the solder joint from collapsing, simultaneous solder wetting to the copper dimple and the chip UBM effectively produces a solder fillet, and thus eliminates the structural singularity at solder/silicon interface that occurs in CCB solder joints. This alleviates the stress/strain concentration around that region and postpones the crack initiation time.

Generally, improvements in the reliability of Dimple Array solder joints can be achieved by the following approaches:

- Increase flexibility of the interconnect sheet or flex (improve **structural compliance**);

- Increase the solder joint height (improve **structural compliance**); and
- Underfill (increase stiffness of the substrate [80]).

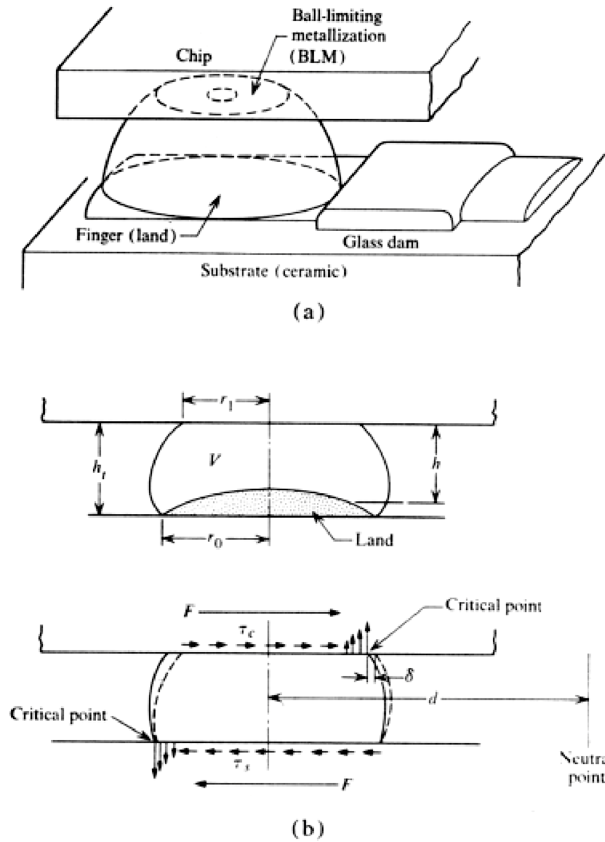


Figure 2.30 Schematics of C4 solder joint: (a) 3D sketch; and (b) sections before and after thermal displacement.

2.3.2.1 Increase flexibility of the interconnect metal sheet/flex

The elastic modulus, the stress that is needed to create unit recoverable strain, largely contributes to the rigidity of a material. The thickness of the interconnect substrate significantly affects its flexibility. Flexibility of the substrate can also be improved using patterned copper traces. A highly compliant interconnect substrate essentially eliminates the global CTE mismatch and increases fatigue life by orders of magnitude.

The commercially available copper flex is a class of highly compliant flexible substrates that has been widely used in portable devices and systems that require lightweight packaging. A copper flex substrate can be single-sided or double-sided. Figure 2.31

shows the construct of a single-sided copper flex circuit [88]. The single-sided flexible circuits consist of a single copper conductor layer on a flexible dielectric film (the base material). Single-sided circuits can be fabricated with or without the top coverlayers.

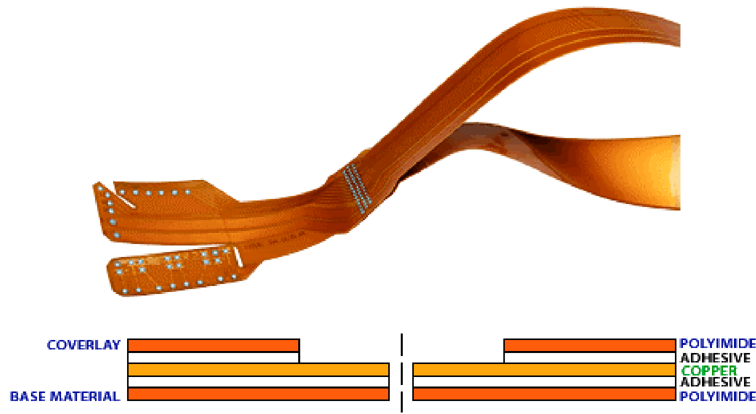
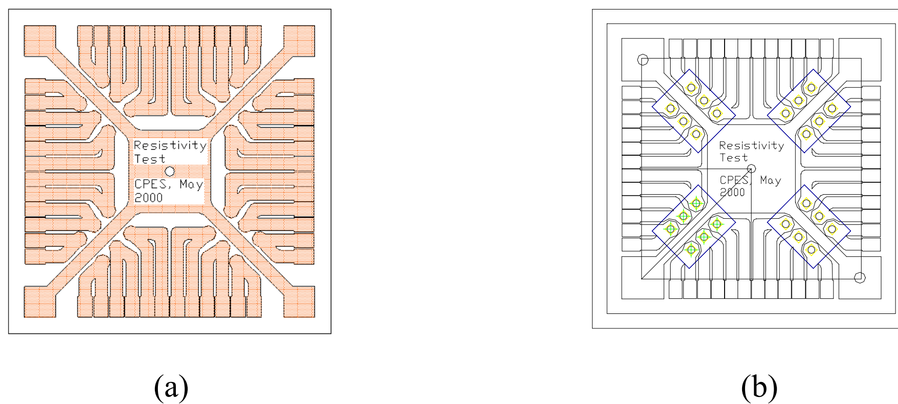


Figure 2.31 Sample flex substrate and the construct of a single-sided flex circuit (courtesy of Allflex, Inc).

Using this type of copper-clad substrate material, lead frame-like flexible DAI can be implemented. Figure 2.32 shows the Dimple Array lead frame design that includes four power semiconductor devices. With the combined advantage of a dimple-shaped solder joint and the flex substrate, solder joint reliability can be significantly improved.



(a) (b)

Figure 2.32 Test vehicle design for measuring resistance change during thermal cycling: (a) dimple copper flex pattern; and (b) CAD layout showing four underlying devices.

This design can also serve as a thermal cycling or power cycling test vehicle. The isolated copper traces are ideal for resistance measurement of the dimple structure using the four-

point method. As shown in Figure 2.32 (b), four devices and 24 solder joints can be incorporated per test vehicle.

In order to gain extra compliance and in the same time avoid sacrificing thermal and current handling capability, holes can also be stamped in the vicinity of each dimple [61]. Stamped lead frames with dimples can essentially package devices with increased I/O count. The thermomechanical stress due to global CTE mismatch is minimized in this type of Dimple Array package.

2.3.2.2 Increase solder joint height

Increasing the height of the solder joint is a major approach for improving the reliability of CCB solder joints. For the CCB solder joint used in typical BGA and flip chip packages, the height of the solder joint is a function of the solder volume, weight or forces exerted on the solder, and the size of the solder mask-defined land area. However, increasing solder joint height is usually accompanied by high processing cost.

The height of the naturally formed Dimple Array solder joint is a function of the cone angle θ of the dimple and the weight of the copper flex. For a given dimple radius and solder paste volume, lower dimple-protrusion (larger θ) results in low-aspect ratio solder joints. The height of the solder joint is also affected by the material elongation limit. For instance, copper has a maximum elongation of 55% before break (with conjugate thinning). The approximate maximum dimple height for a 1-D copper strap is *1.88r* if the radius of the dimple is r, as illustrated in Figure 2.33.

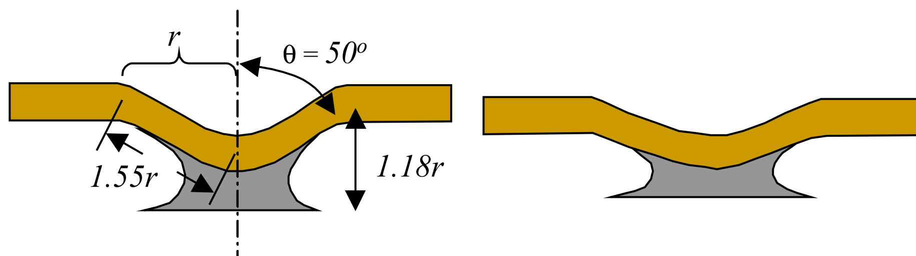


Figure 2.33 Effects of dimple height on solder joint shape.

An effective method for increasing solder joint standoff height is to stretch the liquid solder joints during reflow, which requires a much more complicated fixture. Flip chip bonders capable of stretching solder joint reflow are available (such as the SET 950 bonding machine from Karl Suss).

2.3.2.3 Enhancement using underfill

The third approach is to use underfill for a more robust support of the solder joints. As previously discussed, underfilling of flip chip packages is widely used as an effective approach in the IC packaging industry to improve solder joint reliability.

In this research, a high-performance, fast-curing, liquid epoxy, the LOCTITE® 3565 high Tg underfill, has been selected due to its good reliability and the capability of penetrating gaps as small as 1 mil. This underfill can be easily dispensed with preheating chips to 80°C and cured at 150°C for 30 minutes. The glass-transition temperature Tg is 155°C. Below Tg, the CTE of this material is 25 ppm/^{o}C, and above Tg, the CTE becomes 80 ppm/^{o}C. It is essential to cure the underfill below its glass-transition temperature in order to avoid damage caused by the large CTE above Tg. The properties of this underfill material are listed in Table 2.5.

Table 2.5 Properties of LOCTITE 3565 underfill.

Properties		*Values*
Linear CTE (ppm/^{o}C)	Post Tg	25
	Pre Tg	80
Thermal conductivity (W/m-^{o}C)		0.48
Capillary Flow Rate @ 100°C, glass-to-glass, 1mil/25micron gap, ¼ inch		<30 sec
Glass transition temperature Tg (^{o}C)		155
Dielectric strength (volts/mil)		750
Dielectric constant (1kHz~100kHz) @ 25°C		3.2

2.4 Process development of the Dimple Array interconnected devices

The Dimple Array interconnected package consists of active devices, dimpled copper flexes, the substrate, solder joints, underfill and encapsulation. The following sections present the detailed process for each of the above steps.

2.4.1 Chip-level UBM processing

Most power devices, such as Insulated Gate Bipolar Transistor (IGBT) and MOSFET, are vertical devices with drain (collector) on one side, and gate and source (emitter) on the other side. The contact metal for the drain is normally deposited with gold for die-attach soldering. Source and gate metals are aluminum, since wire bonding is the prevalent interconnection method. In order for the device to be ready for a solder reflow process, a metallization layer over the unsolderable aluminum pad of the chip is formed using either thin-film evaporation, sputtering, or an electroplating process. This layer is usually referred to as the UBM.

The UBM consists of several layers of metals that serve a few purposes:

1. The adhesion layer insures a strong bond of the bumps on the Al. Typical thickness is 1k~2k Å.
2. The reaction barrier or diffusion layer prevents solder diffusion and protects the aluminum on the chips.
3. The main solderable metallurgy forms the basis of the solder wetting surface on silicon.
4. The oxidization barrier layer protects UBM from oxidization and promotes solder wettability. Typically <1000 Å.

UBM can be deposited by sputtering, evaporation, or electroless plating. In IBM's C4 process, UBM (or ball-limiting metallurgy (BLM)) is made through sequential evaporation of chromium, copper and gold [89]. Kulicke & Soffa's flip chip division (FCD)'s standard flip chip bumping process uses a low stress, sputtered Al/NiV/Cu thin-film UBM system [90]. The comparison of various UBM deposition processes is summarized in Table 2.6.

Table 2.6 Various UBM deposition processes.

UBM deposition Techniques	*Vacuum process*	*Wet chemical process*	*Mask*	*UBM system*	*Compatible solder bumping process*
Sputtering	Yes	No	No	Various	Various
Evaporation	Yes	No	Yes	Cr/Cu	Evaporation solder bumps
Electroless plating	No	Zincation pretreated plating	No	Ni	Electroplating solder bumps Low cost

Typical UBM systems are listed in Table 2.7 [91], along with their applicable processing techniques.

Table 2.7 Typical UBM systems and their applicable processing techniques.

UBM	*Evaporated (typical of C4)*	*Plating I*	*Plating II*	*Solder paste printing*	*Electroless Nickel*
Adhesion layer	Cr	TiW	CrCu	Al	Ni
Solder diffusion layer	Phased Cr-Cu	Cu stud/mini bump	CrCu	Ni	Ni
Oxide prevention	Au	Au	Au	Cu	Au
Suitability for 63Sn37Pb	No	Poor	No	Yes	Yes
Use with probed wafers	No	No	No	Yes	Mixed

In this research, devices from manufacturers come with the aluminum metallization contact. An optimized sputtered-UBM process has been developed using existing sputtering facilities. Figure 2.34 and Table 2.8 show the proposed UBM process for power semiconductor devices used for the Dimple Array solder bumping.

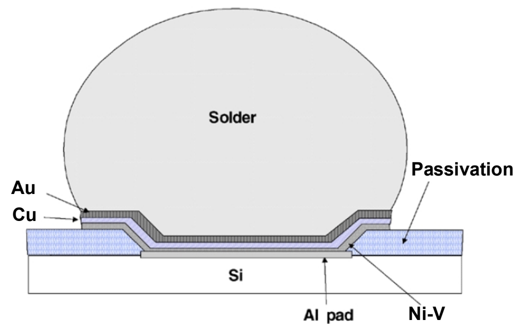


Figure 2.34 Proposed UBM structure for the Dimple Array solder bumping.

Table 2.8 UBM system for the Dimple Array solder bumping.

UBM	*Roles*	*Thickness*
Au	Oxidization protection	0.1 μm
Cu	Wetting layer	0.5 μm
Ni-V	Adhesion/diffusion barrier	0.3 μm
Al	Contact metal on silicon	

This approach uses a low-stress Ni (93%)-V as the adhesion layer as well as the reaction barrier layer. Another advantage of using Ni-V is that it's also a solderable layer and can ensure a good adhesion even if gold and copper are consumed by high-Sn solder.

Device wafers are first sputtered for 15 minutes with Ni-V, followed by 25 minutes of copper deposition. The UBM is patterned using AZ P4400 positive photoresist from Clariant. Then, the wafer is placed into a sodium persulfate solution to remove non-needed metal deposition. Last, after resist peeling, a thin layer of gold flash is electroless-plated to the pads using Oromerse MN from Technic, Inc. at a temperature bath of 60-70°C for one hour.

2.4.2 Dimple flex interconnect fabrication

The dimple flex fabrication is a major step that separates the DAI technique from others. Conventional CCB solder joints are reflow-joined to the PCB or other flat substrates. The dimple flex interconnect structure is a flexible substrate with an array of protrusions on one side. The combination of flex circuit material and the dimple structures brings about many advantages. First, the formability of a flexible substrate enables a reduced package size. Second, solder-interconnected flex substrate reduces assembly cost due to the ability to conduct a burn-in test of the power devices before power module assembly. Third, the dimpled flex substrate significantly reduces the stress concentration, enabling a more reliable package assembly. Furthermore, the polyimide has good dielectric strength and is a good insulation layer for high-power devices.

The flex substrate described here, such as Dupont's Pyralux®, is a family of flexible, solderable, copper-clad laminates. Copper is bonded to the polyimide film either by sputter deposition of tiecoat metal and copper, or by applying a proprietary, flame-retardant, C-staged acrylic adhesive. The final copper thickness is achieved through electroplating.

The process starts with a single-sided flexible copper-clad laminate photo-lithographically defined on the copper side to have the desired lead frame pattern. Etching of the substrate is done in ferro-chloride etchant or sodium persulfate solution. Then, a stamping fixture is used to produce the dimples on the copper flex. The stamping fixture has a base plate with holes following the same pattern as on the dimpled flex. The top plate of the fixture has smaller-sized holes but the same pattern. Stainless-steel pins with specially designed lengths are inserted into the holes on the top plate. The difference between the length of these pins and the thickness of the top plate defines the height of the dimples that are to be formed. Figure 2.35 shows a fixture for making the dimple flex.

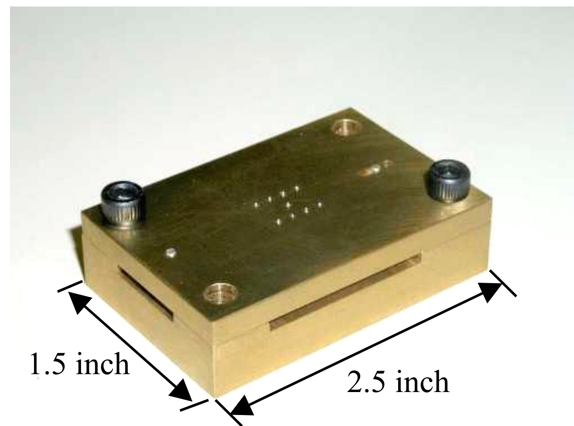
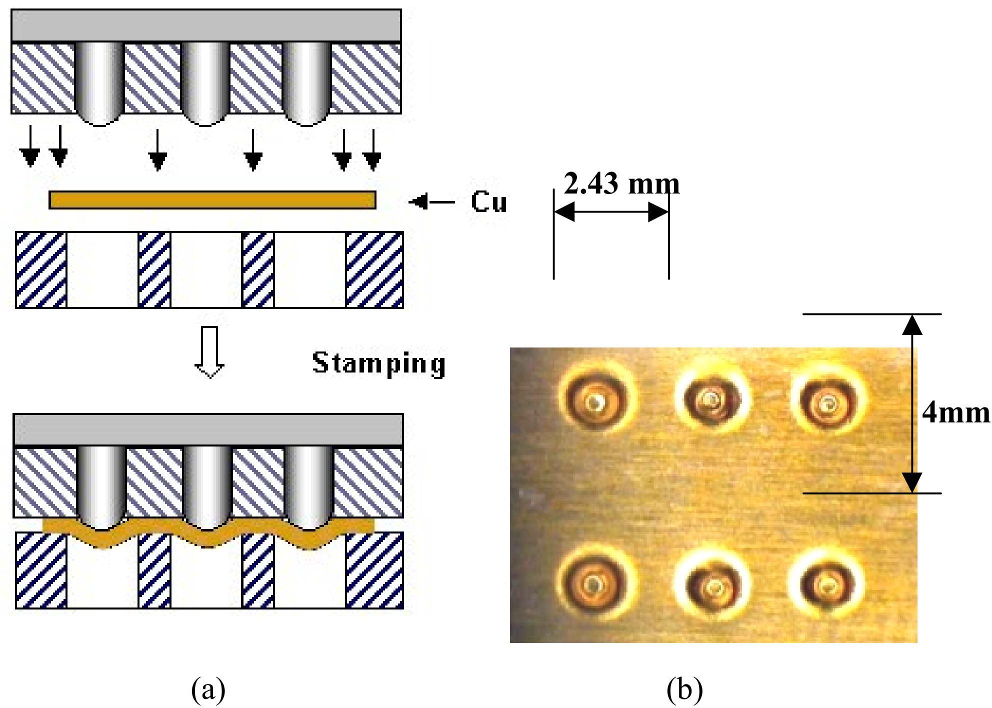


Figure 2.35 A fixture used to stamp the dimple flex.

Next, the etched copper flex is sandwiched between the base plate and the top plate. Then, a flat, stiff piece of metal pushes the pins down until the metal piece reaches the surface of the top plate. Figure 2.36 shows the fabrication process for the dimpled flex using the stamping tool and a top view of a finished dimple structure.



(a) (b)

Figure 2.36 Fabrication of the dimple flex using stamping fixtures: (a) stamping process; and (b) top view of a stamped dimple copper flex.

2.4.3 Dimple area array bumping and assembly

In the conventional flip chip fabrication, there are three major bumping processes according to the different bump materials: solder bump flip chip, stud bump flip chip, and conductive adhesive bump flip chip.

The Dimple Array solder bumping process uses a screen-printed method. A solderable device is first placed in a fixture with a vacuum chuck underneath to hold it in position. The device is then covered with a stainless-steel stencil with openings aligned to the solder pad on the device. Next, solder paste is applied using a squeegee. The squeegee also removes excessive solder. After the stencil is lifted off, the DAI is picked up by a vacuum pick and aligned with the solder paste on the device. The solder bumping of the DAI is completed with a standard solder reflow. A flux-clean step is normally required to ensure the quality of the solder bumping. Figure 2.37 shows the process of the Dimple Array solder bumping.

Since DAI only uses a single type of solder material on the device level, there are many options for selecting solder alloys. For discrete device packaging, the device can first be soldered to the copper heat spreader or DBC with a high-melting temperature solder such as a Pb90-Sn10 solder. Then the subsequent solder bumping is processed at the eutectic temperature of 183°C. For multichip module fabrication, the devices are first packaged with the DAI using high-melting temperature solder, then the die-attach is processed at a lower soldering temperature.

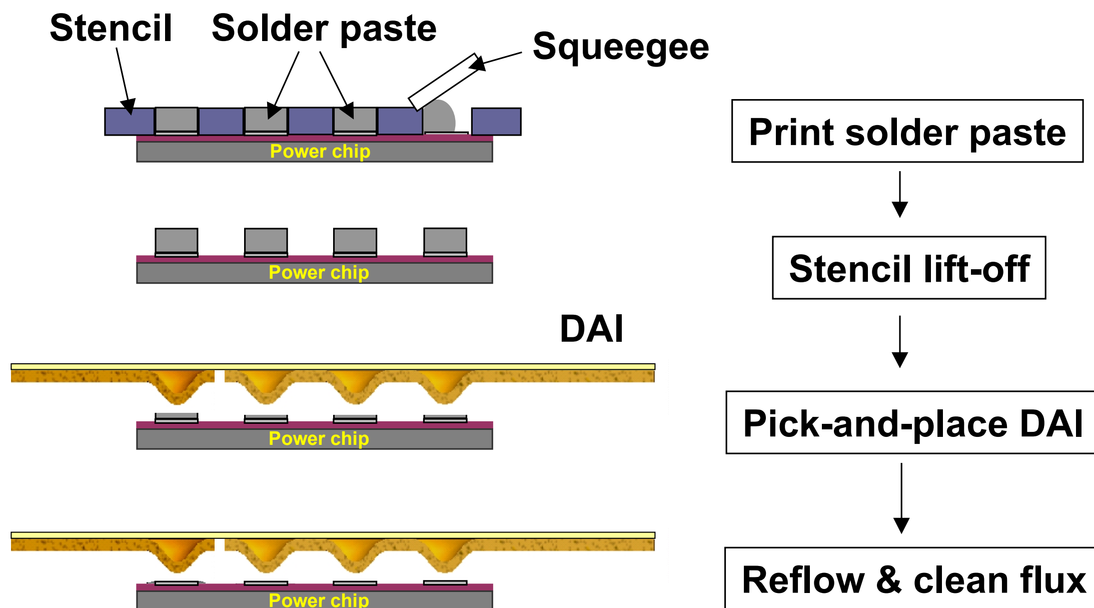


Figure 2.37 Process flow of the Dimple Array solder bumping.

2.4.4 Underfill

For area array solder bumping packages, underfill is a major reliability enhancement approach [92,93,94,95,96,97]. Only the small die size does not require underfill. Underfill is an epoxy-based material that mediates the thermal mismatch between the silicon die and the substrate and enhances thermal conduction. It is applied in a liquid form to flow into the gap between the silicon and the substrate, and is cured in a specified thermal profile. For flip chips in the power electronics application, since copper is usually the selected interconnect material and thus CTE mismatch between the interconnect and the device is large, underfill is of particular importance for reliability.

In DAI processing, underfill flow is processed after solder reflow and chip attachment. Figure 2.38 illustrates this process. Pre-heating of the assembly is normally required to ensure a good underfill flow. The underfill paste is first dispensed to one edge of the chip and an edge next to it. Underfill will flow and spread out due to the capillary effect, and will ultimately fill in the whole gap. A higher temperature is required to thermal-set or cure the polymer. The L-shape in which it is dispensed is important because it minimizes the chance of forming voids.

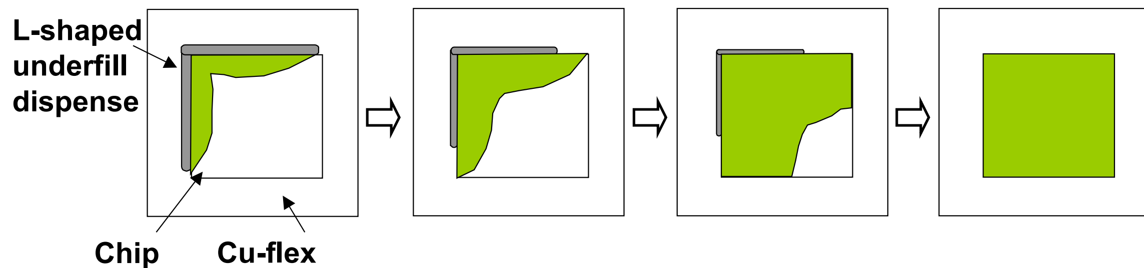


Figure 2.38 Conventional underfill-flow process.

The schematic of the underfilled Dimple Array package is shown in Figure 2.39. The finished DAI package can proceed to burn-in test at full power. Fabrication of power MCMs using the DAI-packaged devices is convenient, since the only requirement is that a high-temperature solder must be used for the dimple solder joints.

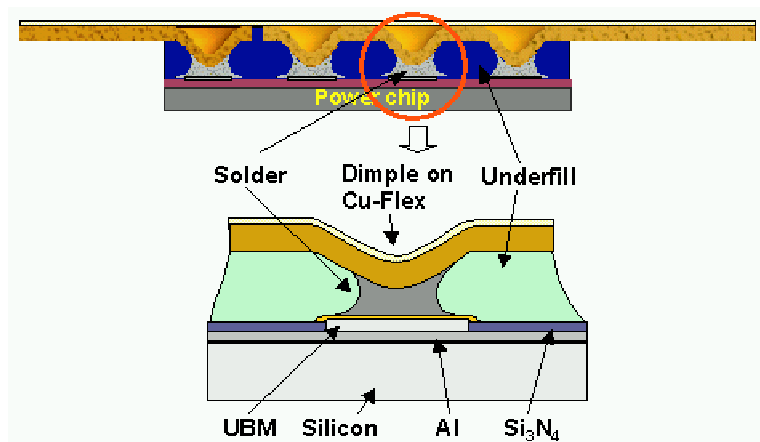


Figure 2.39 Underfilled power device with Dimple Array interconnects.

2.4.5 Dimple Array interconnected power switching stage module integration

The power switching stage module is a fully functional unit in power systems, and comprises active switches, gate drives, control circuits and heat-dissipation components, including the base substrate and heat spreader. A schematic of the DAI power switching stage module is shown in Figure 2.40.

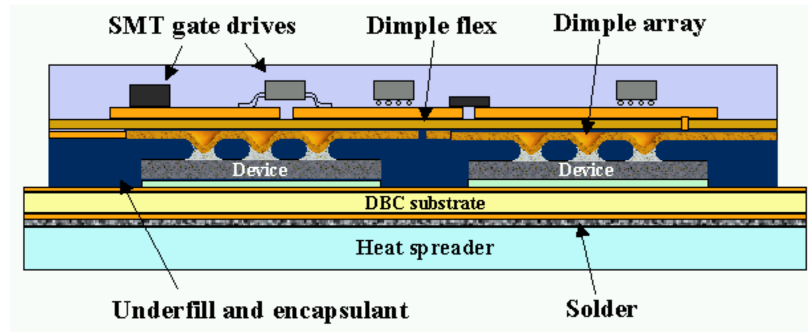


Figure 2.40 Schematic of Dimple Array interconnect and integrated DAI power switching stage module.

The module is made by solder-attaching DAI power devices, such as diodes and IGBTs, onto a DBC substrate. Since power devices are vertical, attachment of the device to a base substrate serves two purposes: the electrical connection for the drain as well as the major heat-dissipation path. Solder also serves as a buffer layer to absorb the strain due to CTE mismatch between the device and the substrate. Typical solders for the die-attach include:

- 63Pb-37Sn (183°C),
- 95Pb-5Sn (310°C),
- Pb-In-Ag (310-314°C),
- 80Au-20Sn (280°C), and
- 65Sn-25Ag-10Sb (233°C).

Because only one type of solder is needed to form the dimple solder joint, there are more options for selecting a solder of a different melting temperature for the surface-mounted gate drive and control components. In the end, the fabrication of the power switching

stage is finished with a housing/encapsulation process for protection of the power devices and other auxiliary components.

2.4.6 Process complexity evaluation

Process complexity can be the determining factor in switching from the existing packaging technology to an alternative. Initially, performance improvement in packaging technologies is often accompanied by manufacturability difficulty. The question is whether or not it is possible to transfer the laboratory process to mass production. The following figures (Figures 2.41) show the fabrication flowcharts for the wire bond module versus some developing 3D interconnected modules, including the flip chip, the deposit metallization, and the DAI.

The comparison of the fabrication flowcharts given in Figures 2.41 (a), (b) and (c) indicates the following facts: The fabrication process for the wire bond module is very simple and mature; and the alternative 3D interconnect packaging methods for power modules have a longer manufacturing cycle and complicated processing steps that require more expensive equipment.

The fabrication flowchart of power modules using DAI is shown in Figure 2.41 (d). The simplicity of processing the DAI module is comparable to that of the wire bond module. Lead frame fabrication equipment in IC packaging can be easily modified to fabricate the dimple flex. In addition, in contrast to the flip chip process (within the solder bumping step), there is no need for solder masking to control the collapse of solder joints in DAI processing. Furthermore, instead of a sequential wire bond fabrication process, the DAI fabrication needs only one solder-reflow step to attach the interconnect metal flex. With current industrial positioning and the pick-and-place system, this step can be easily automated.

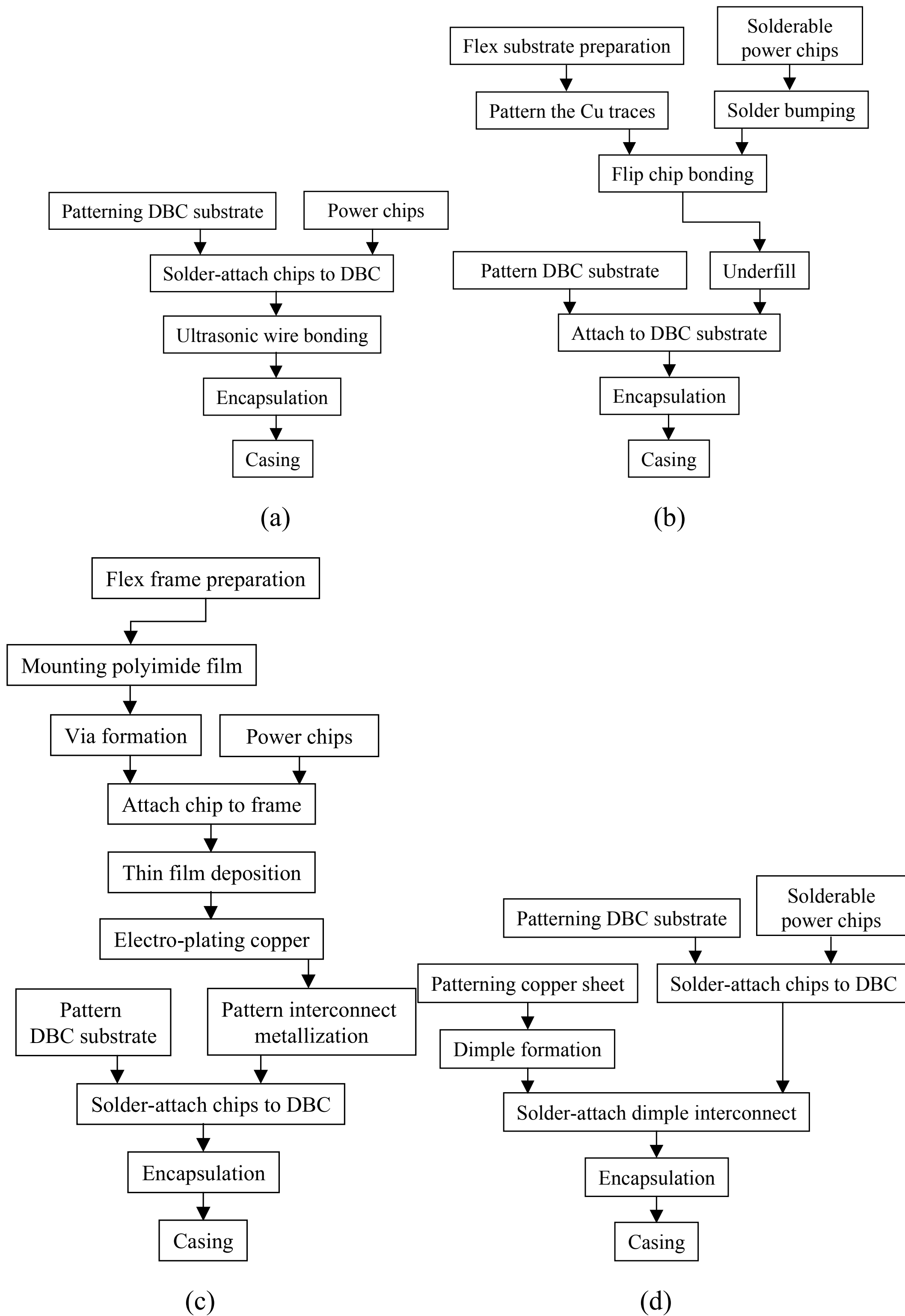


Figure 2.41 Flowchart for manufacturing various power modules: (a) wire bond; (b) flip-chip; (c) deposit-metallization; and (d) DAI modules.

2.5 Implementation of the Dimple Array interconnect approach on a half-bridge power IGBT module

2.5.1 Existing power module packaging technology

The half-bridge power module circuit (shaded box) and its driver circuit are shown in Figure 2.42.

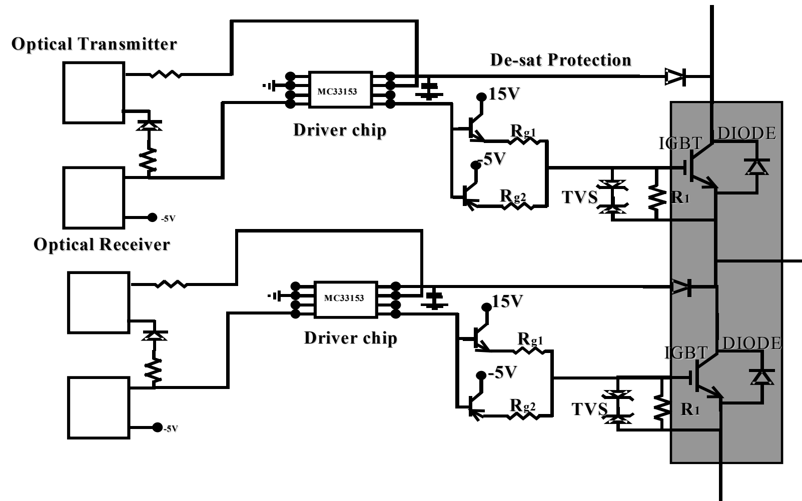


Figure 2.42 Circuit diagram of half-bridge power IGBT module (shaded region) and its drive circuit.

Commercial half-bridge power IGBT modules on the market are mostly wire bond interconnected packages. These modules comprise a number of power devices (IGBT and diode) solder-attached to alumina or aluminum nitride DBC substrates. Aluminum wires are used to connect device electrodes to the copper pads on the DBC, and are then routed to the top of the plastic case using soldered copper leads/terminals. Silicone gel is commonly used to fill in the space housed by the case and to protect the wire bond and device from moisture and other contamination. To spread heat more evenly to the heat sink, the assembly is soldered down to a copper base plate with the bottom side machined to ensure an optimal thermal contact. Figure 2.43 (a) shows the construct of these modules [98].

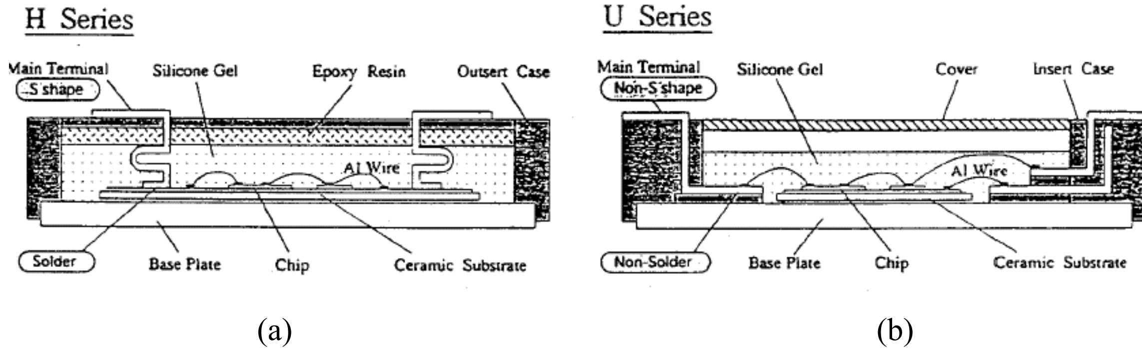


Figure 2.43 Cross-sections of the conventional package (a) and the improved package (b).

Figure 2.43 (b) [98] shows an improved design from Mitsubishi, which is aimed at reducing parasitic inductance and saving expensive AlN substrate areas. The wire diameter has been increased from 300 μm to 400 μm for an additional reduction of stray inductance. Figure 2.44 shows a top view of these two types of packages [98].

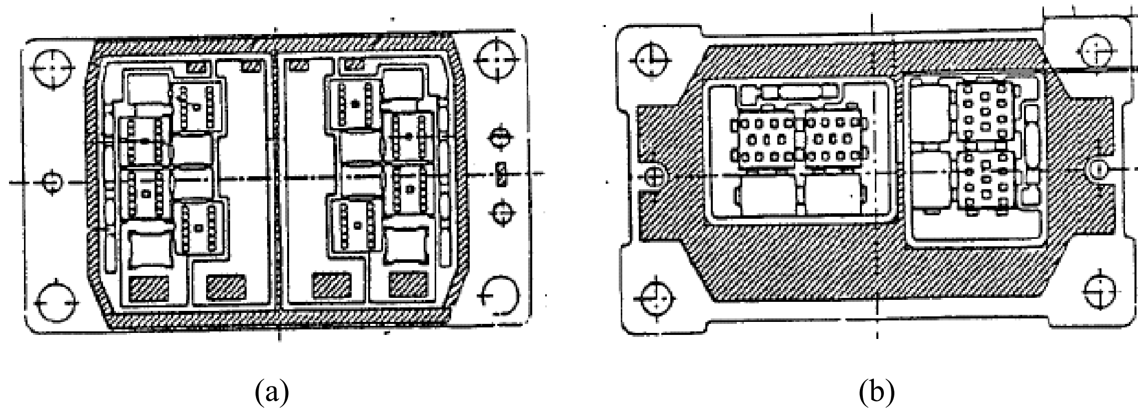


Figure 2.44 Top views of (a) the conventional package and (b) the improved package .

It is obvious that enhancement through layout optimization and the wire bond diameter increase is very limited. In order to demonstrate the electrical advantage of the DAI in the application of power modules, a half-bridge power IGBT module is built.

2.5.2 Dimple Array module layout design and fabrication

Figure 2.45 shows the layout of the components of the DAI module. This module is about 50 mm long and 35 mm wide. Two IXYS IXSD 35N120A IGBT (rating: 1200V, 70A) chips and two IXYS C-DWEP 69-12 diodes were integrated in this module.

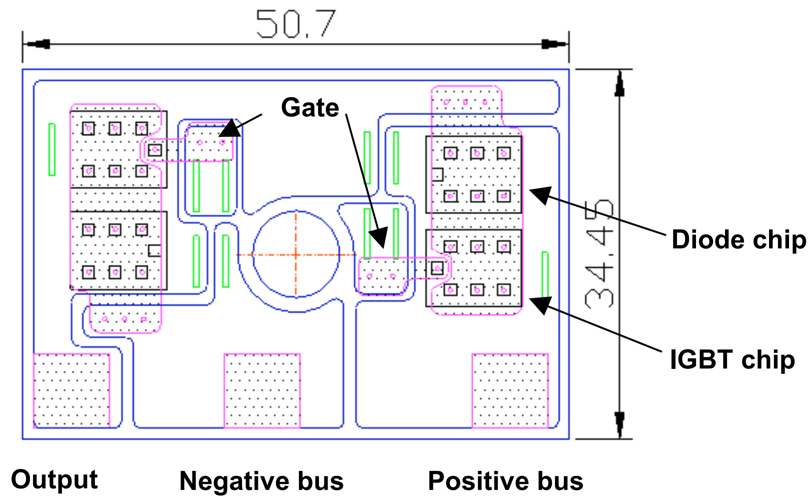
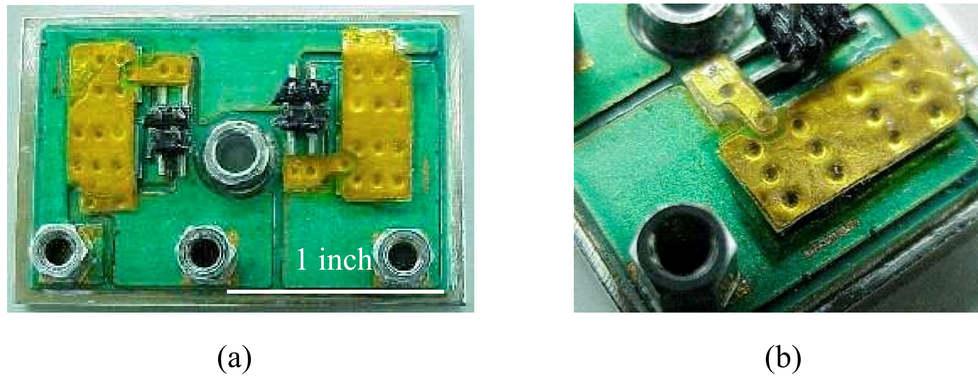


Figure 2.45 The circuit layout design of the Dimple Array interconnected module.

The first prototypes are built and shown in Figure 2.46.



(a) (b)

Figure 2.46 A demonstration half-bridge IGBT module (a) and a close-up look (b).

A second-phase prototype module is shown in Figure 2.47. Silicone gel was used to encapsulate the module. Compared with the conventional wire bond module, the DAI modules have a much lower profile, shorter interconnect path, and much greater interconnect cross-section area.

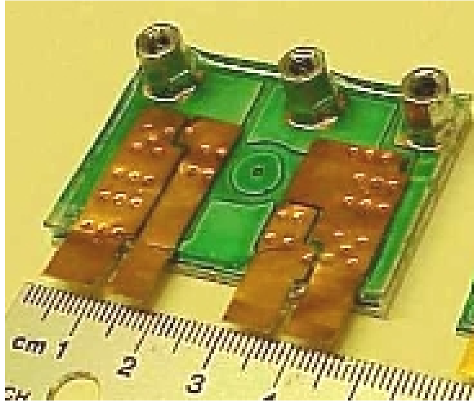


Figure 2.47 A second-phase prototype module.

2.5.3 Electrical performance of the Dimple Array module

Before the assembly of the power modules, each individual device must be screened using a TEKTRONIX 576 curve tracer to ensure its functionality. After the full assembly of the modules, a SONY/TEKTRONIX 371 high-power curve tracer is used to push the current pulse up to more than 200A. Once the power modules have passed the high-power curve tracer test, a power stage test will be performed to test their switching characteristics. The results will be compared with that of a commercial power module. The available test circuit topologies for the power stage test are shown in Figure 2.48.

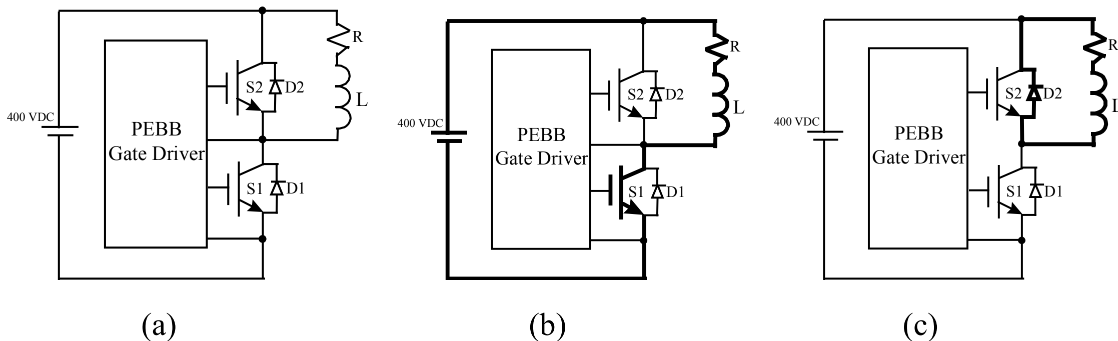
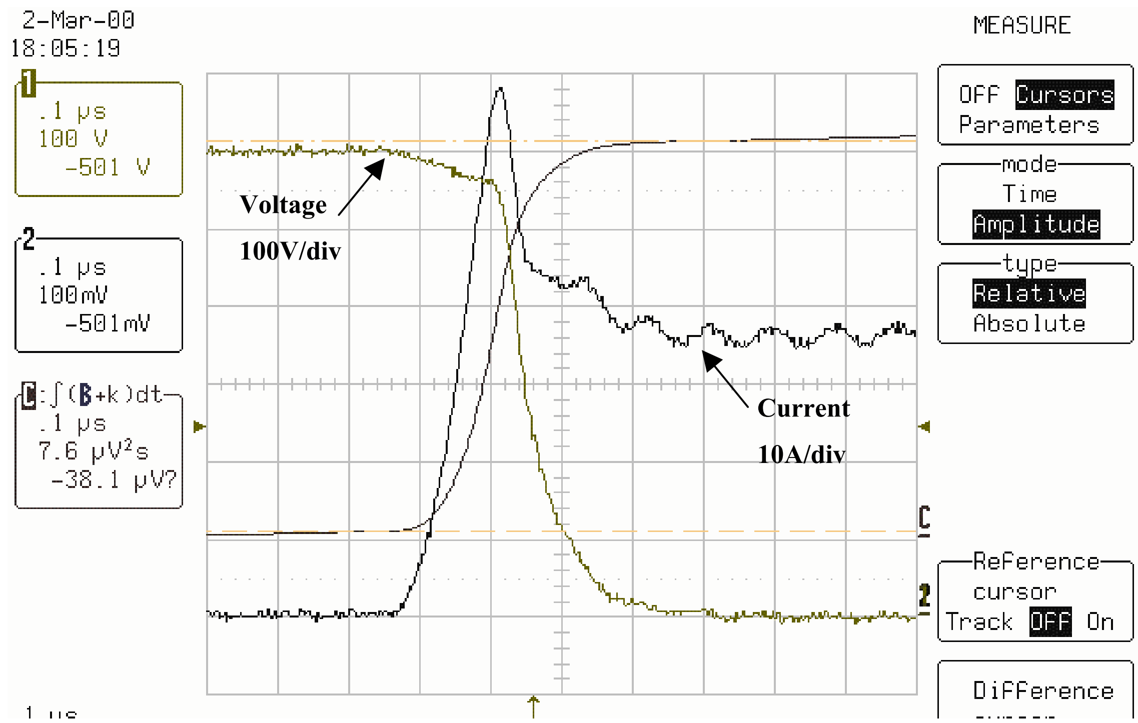
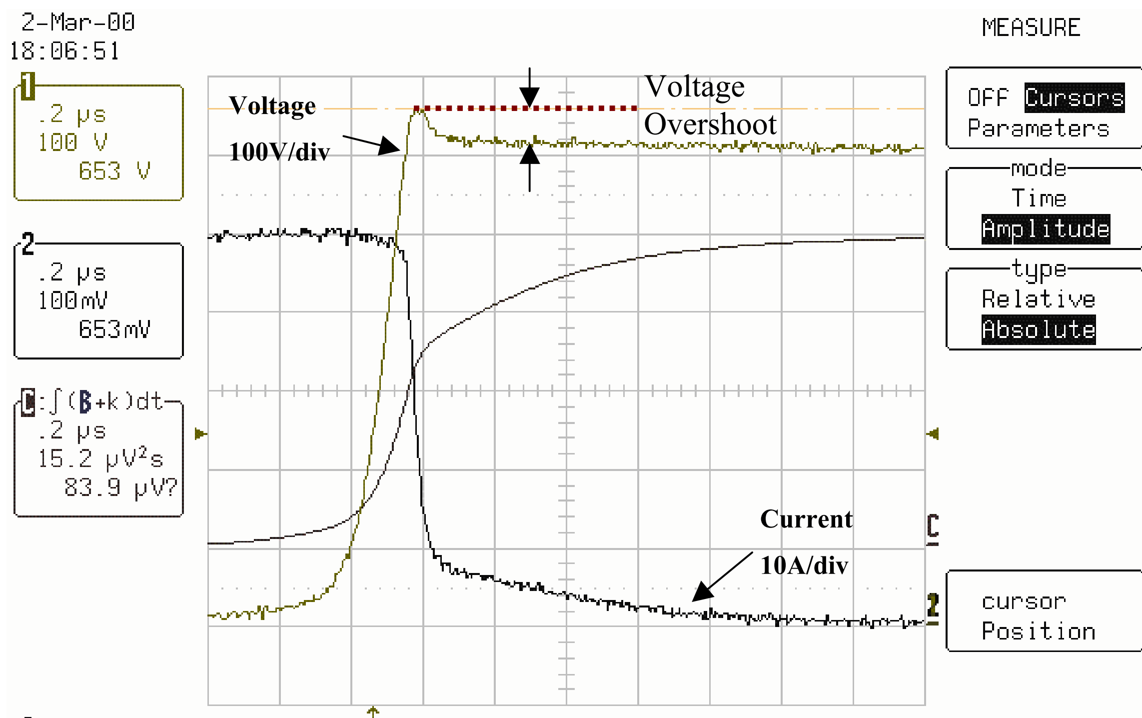


Figure 2.48 Power module test circuits: (a) for the low-side switch; (b) inductor charging path (thick line); and (c) inductor discharging path (thick line).

Figure 2.49 shows some power stage test results. At 600V and 50A, the I-V curves are very clear. A low turn-off voltage overshoot of 60V is present. Compared with an overshoot of more than 100V for the commercial module (using the same devices with wire bonds) tested at the same condition, the Dimple Array module shows a significant reduction in parasitic noises.



(a)



(b)

Figure 2.49 Power stage switching characteristics at 600V and 50A: (a) turn-on; and (b) turn-off.

Another important parameter is the switching energy loss. Figure 2.50 shows the switching energy losses of both a commercial wire bond power module and the Dimple Array module at different testing currents. The DAI module exhibits significantly reduced switching energy loss at each test point as compared to the commercial module. This is mainly attributed to the low parasitic inductance associated with the short interconnects of the solder joints. A reduction in switching loss directly improves the power conversion efficiency and saves energy.

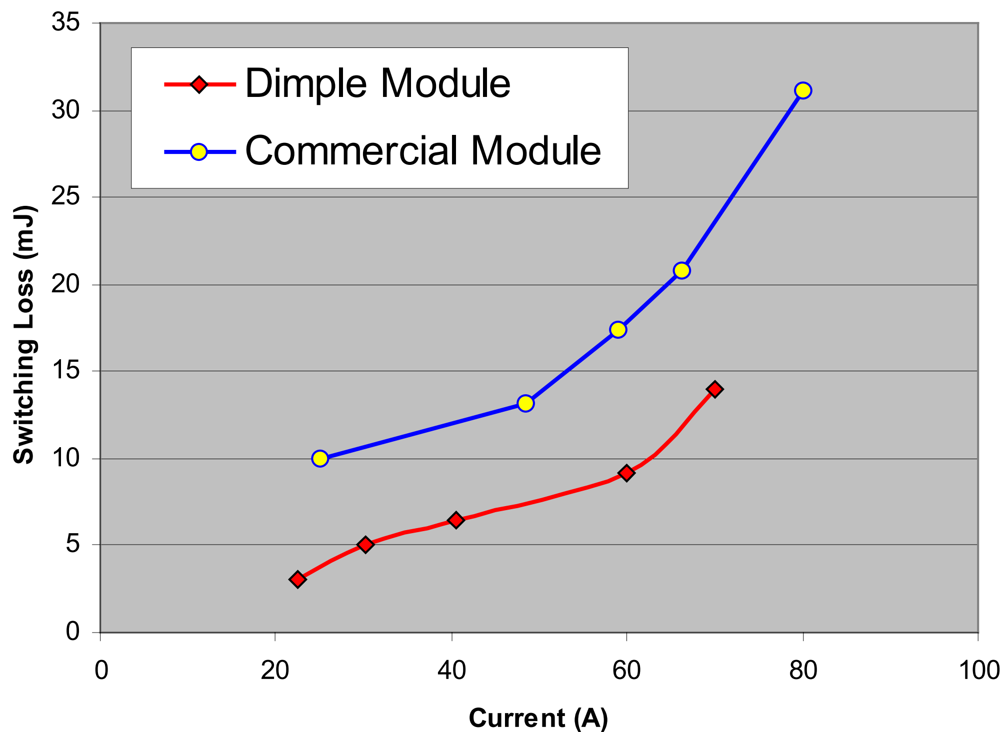


Figure 2.50 Switching energy comparison of the commercial wire bond module and the Dimple Array module.

Summary

This chapter introduced the Dimple Array interconnect technique in the application of power semiconductor devices and modules. Design considerations of the DAI, including current handling capability, thermal management, parasitic inductance and capacitance, geometry, interconnect material, solder alloy systems, and reliability, are discussed. It was found that due to the use of solder material, the current handling capability and thermal management of DAI devices are significantly better than those of the wire bond

ones. In addition, the shorter and wider solder joints reduce parasitics, which is a serious problem in wire bond interconnects. Then, the fabrication process of the DAI has been developed, and is found to be simpler than other developing integrated power packaging technologies. And last, the DAI was successfully demonstrated in a half-bridge power electronics module with much-improved electrical characteristics.