Chapter 6. Summary and conclusions

The Dimple Array interconnect (DAI) technique is a novel technique for interconnecting power devices and packaging high-performance power electronics modules. This research presents the development of the DAI for these applications.

As a first-level interconnection, the Dimple Array solder joint plays a vital role because it directly interfaces electrically, thermally, and mechanically with the numerous transistor cells in the chip. Therefore, it is imperative to investigate the feasibility of the DAI technique in terms of process, materials, and electrical, thermal, and thermomechanical reliability.

This research has accomplished two main objectives:

1. It designed and implemented a high-performance DAI technique for packaging power electronics devices and modules; and
2. It analyzed the electrical, thermal and thermomechanical performance of the DAI technique, with a particular focus on its thermal fatigue reliability and physics of failure.

The study of the reliability and physics of failure of the DAI is approached from two perspectives: numerical modeling prediction and the thermal/power cycling experiment and failure analysis.

In the following sections, conclusions from this research are summarized.

6.1 Design and development of the Dimple Array interconnect

In this subthrust, the design of the DAI for power semiconductor devices and modules was first presented. Then, the fabrication process of the DAI was developed, including UBM processing, dimple flex interconnect stamping, die-attach, dimple area array

bumping and assembly, and underfilling. Using the DAI, significant breakthroughs can be made in the following aspects:

- They offer a higher current handling capability, due to a larger cross-section of the solder joint, as compared with bond wires;
- There are reduced levels of thermal resistance in device interconnects;
- Circuit parasitic noises can be dramatically reduced because there are shorter current paths in DAI;
- Since only one type of solder is needed, the designer can have more options when choosing solder systems; and
- DAI processing is simpler, requires fewer processing steps and less expensive equipment, and has shorter processing cycles.

The electrical advantages of the DAI were successfully demonstrated in packaging half-bridge IGBT modules. Due to the reduced parasitic inductance in the DAI structure, the turn-off voltage overshoot was smaller than in its wire bond counterpart, which makes the operation of the DAI module safer. Also, the switching energy loss at device turn-on and turn-off has been significantly reduced, leading to a higher efficiency. Furthermore, package-volume reduction and increased power density offered by the low-profile DAI modules make it possible to implement a multilayered package with control circuit and gate driver integration.

6.2 Thermomechanical reliability of the Dimple Array interconnect

In this section, the thermomechanical reliability of the DAI has been evaluated using accelerated testing, including thermal cycling and power cycling; these are compared with the conventional CCB.

Figure 6.1 summarizes the typical thermal cycling results for non-underfilled CCB and dimple solder joints made using Pb37-Sn63 solders. The normalized resistance change

R/R_0 is a sensitive parameter for determining solder joint integrity. The dimple solder joints show an eightfold reliability improvement over the conventional CCB solder joints.

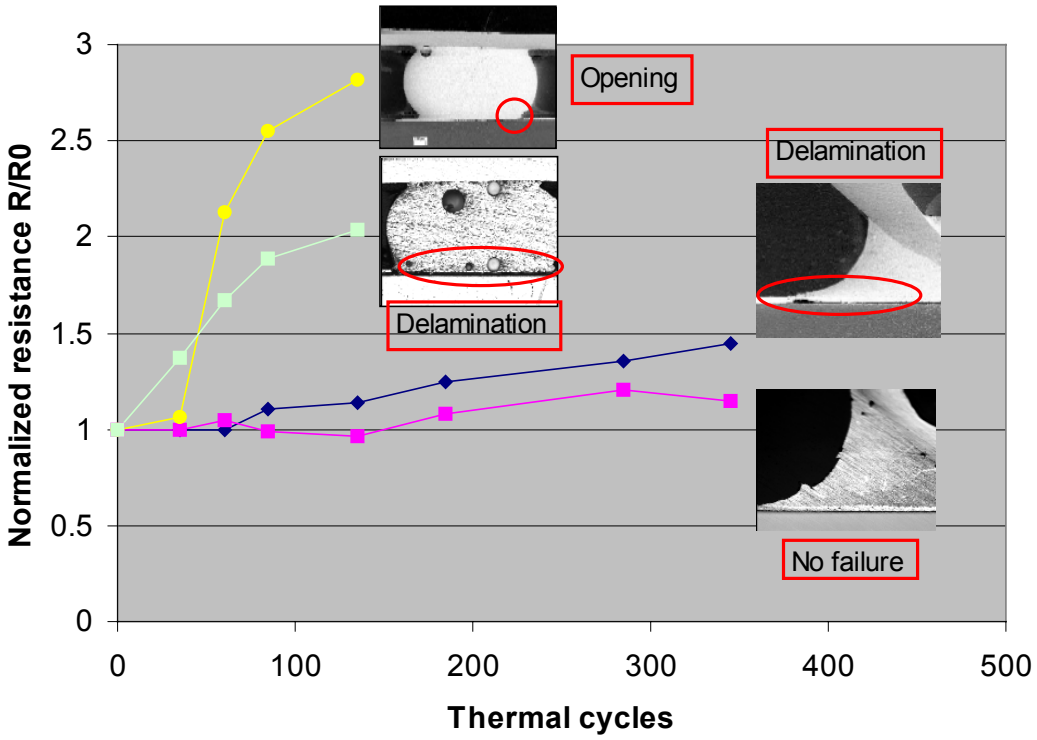

Figure 6.1 Summary of the Pb37-Sn63, non-underfilled samples for the thermal cycling test.

Power cycling test results on the Pb37-Sn63, underfilled samples are summarized in Figure 6.2. It was found that the measured forward voltage can not reliably reflect the integrity of the solder joint interconnect. From metallographic cross-sectioning of the test samples, it was concluded that power cycling incurs less damage in Dimple Array solder joints than in the CCB solder joints within the same period of testing. Even after 12,700 power cycles of 60 seconds per cycle, the Dimple Array solder joints retain some areas of ohmic contact with the aid of the underfill, whereas the CCB solder joints have a clear broken band at the solder/device interface after 8,500 cycles.

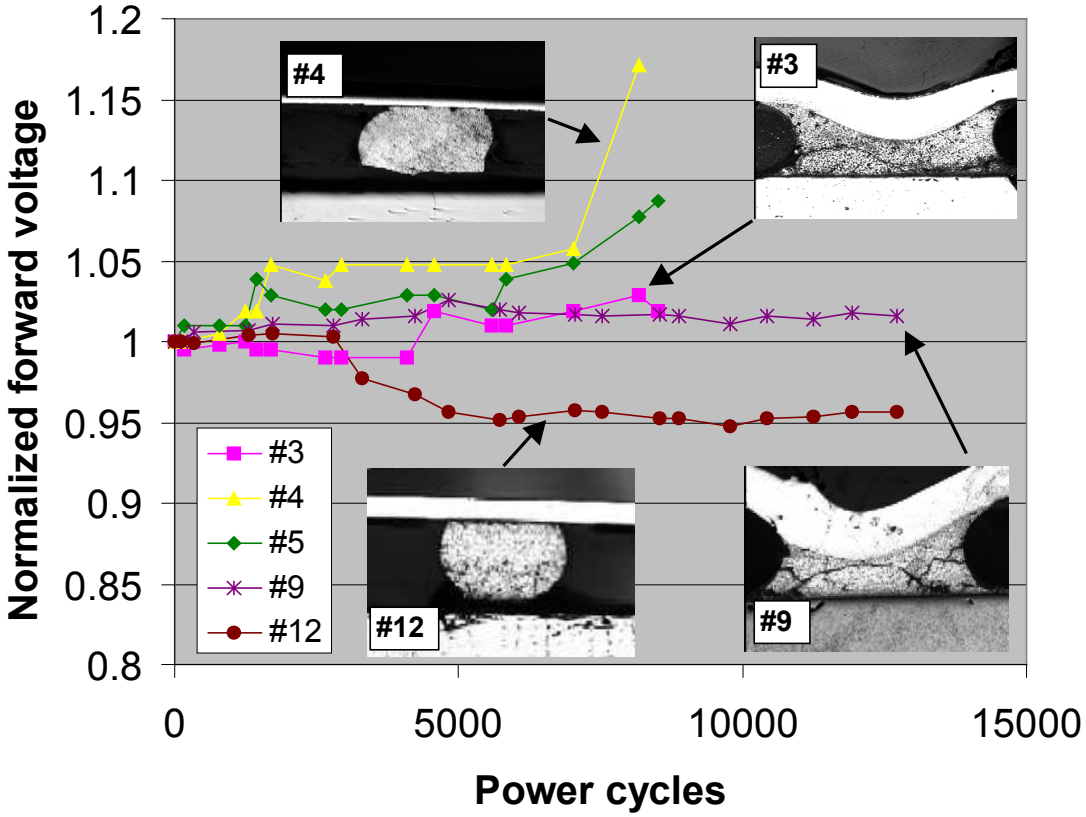

Figure 6.2 Summary of the Pb37-Sn63, underfilled samples for the power cycling test.

Based on the above test results, it is clearly shown that the DAI displays a significant reliability improvement in both temperature cycling and power cycling conditions over the conventional CCB interconnect.

6.3 Numerical analysis using finite element simulation

In this section, the FEM has been extensively used to model the thermomechanical stresses/strains within the overall Dimple Array and CCB packages, as well as the thermoviscoplastic behavior of solder joints. Results and conclusions from the modeling are given as follows:

- FEM modeling results predict a five to tenfold improvement in thermal cycling reliability for both the Dimple Array solder joint and the conventional CCB solder joint, while the thermal cycling experiment shows an eight- to more than tenfold improvement in the Dimple Array solder joint. Furthermore, FEM shows much

higher normal stresses at the outer edge of the solder/device interface of the CCB than those occurring in the dimple solder joint, this explains the early UBM delamination failures in CCB samples.

- FEM modeling results also predict better power cycling reliability for the Dimple Array package; this was proved through metallographic cross-sectioning of samples at different testing stages. Underfill significantly improves CCB solder joint reliability, as shown in FEM modeling. Crack initiation and propagation paths in the power cycling samples correlate very well with FEM modeling, indicating that FEM is very effective and accurate in failure-mode prediction for solder joints.

- Choice of the stress-free state in modeling the thermal fatigue of a solder joint does not contribute to a major change in stress/strain patterns in subsequent temperature/power cycles.

- Effect of the die-attach solder and DBC substrate was examined. The omission of these components and the use of a vertical constraint at the bottom of the silicon device instead result in approximately a 20% increase in the predicted equivalent inelastic strain.

- Underfill dramatically reduces the stresses that are responsible for shape distortion in solder joints. Parametric modeling for the effects of the mechanical properties of underfill suggests the use of a stiffer underfill to further enhance the reliability of the Dimple Array solder joints.

In summary, the advantages in processing, as well as the improved electrical, thermal and reliability performances of the DAI, as demonstrated in this research, manifestly show the feasibility of this technique for use in evolutionary 3D planar packaging techniques for power semiconductor devices and modules.