1. Chapter 1: Introduction

Non-volatile memories with ferroelectric capacitor materials are also known as ferroelectric random access memories (FRAMs). Present research focuses on integration of ferroelectric materials into high-density non-volatile random access memories.

1.1 Ferroelectric memories

There are fourteen generically different kinds of digital memories in use today. These memories range from slow, inexpensive tapes or discs used for archival storage to fast but expensive static random access memories (SRAMs) and dynamic random access memories. Some of the more expensive memories include electrical erasable programmable read only memory (EEPROMs). While flash memory and EEPROMs suffer from a drawback of very limited lifetime, SRAMs need to be backed by a battery continuously. These drawbacks can be completely eliminated if SRAMs, EEPROMs and flash memories can be replaced by Ferroelectric random access memories (FRAMs) which can be tailored to possess longer lifetimes and higher speeds.

In the current commercial world, there are few widely used non-volatile memories, which constitute of flash memories and EEPROMs. These non-volatile memories have an inherent limitation of lower lifetime. For example, the number of times a memory bit could written into a flash memory is limited only to a maximum of 10^5 cycles. (The unit that is generally used to signify the lifetime is cycles). In terms of lifetime, FRAMs have been shown to be potential candidates for non-volatile random access memories, where the lifetime could extend atleast to a value of 10^8 cycles [(1)].

In the current commercial world, use of FRAMs is limited to applications which include low density memories in video game devices, TV sets, FAX machines, printers, mobile phones and fully embedded ferroelectric memories in silicon microprocessors and microcontrollers. Some of the state-of-art FRAMs, available commercially, are 4 Mbit RAMs from Samsung [(2)], 1Mbit RAMs from NEC and 256 kbit RAMs from Matsushita [(3)]. However, currently available commercial FRAMs are limited to low density structures, where one transistor/one capacitor structure (1T/1C) is used with the capacitor being seated adjacent to the transistor[(4)]. FRAMs could possess an appreciable market in the field of non-volatile memories, provided high density FRAMs are commercialized. In order to realize high density FRAM structures (in Gigabit range), an FRAM cell is required to possess a capacitor on the top of the transistor (Fig. 1.1). Current research focuses on the fabrication of the ferroelectric capacitor which could be integrated directly on to the top of the transistor. While the transistor in the 1T/1C memory structure acts as an access switch to the capacitor, the actual memory is stored in the ferroelectric capacitor.

1.2 Basic operation

Ferroelectric materials are characterized by reversible spontaneous polarization[(5-8)]. Spontaneous polarization arises due to noncentrosymmetric arrangements of ions in its unit cells which produces a permanent electric dipole moment associated with the unit cell. Adjacent dipoles also tend to orient themselves in the same direction to form a region called ferroelectric domain. Ferroelectricity is most commonly observed in ABO_3 perovskite structures as shown in Fig.1.2. Above the Curie temperature these materials

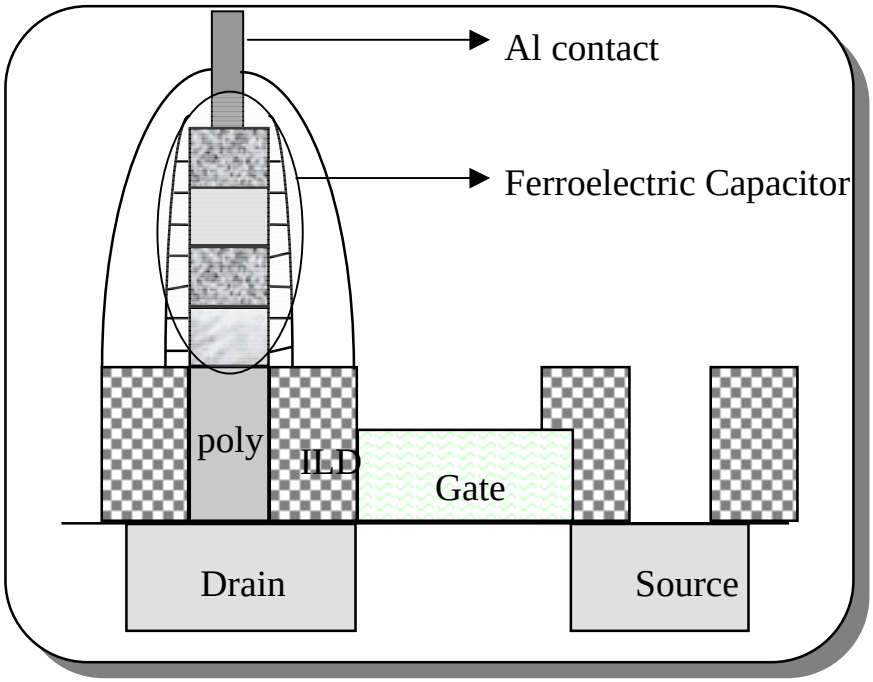

Fig. 1.1 Typical high density 1T/1C FRAM structure

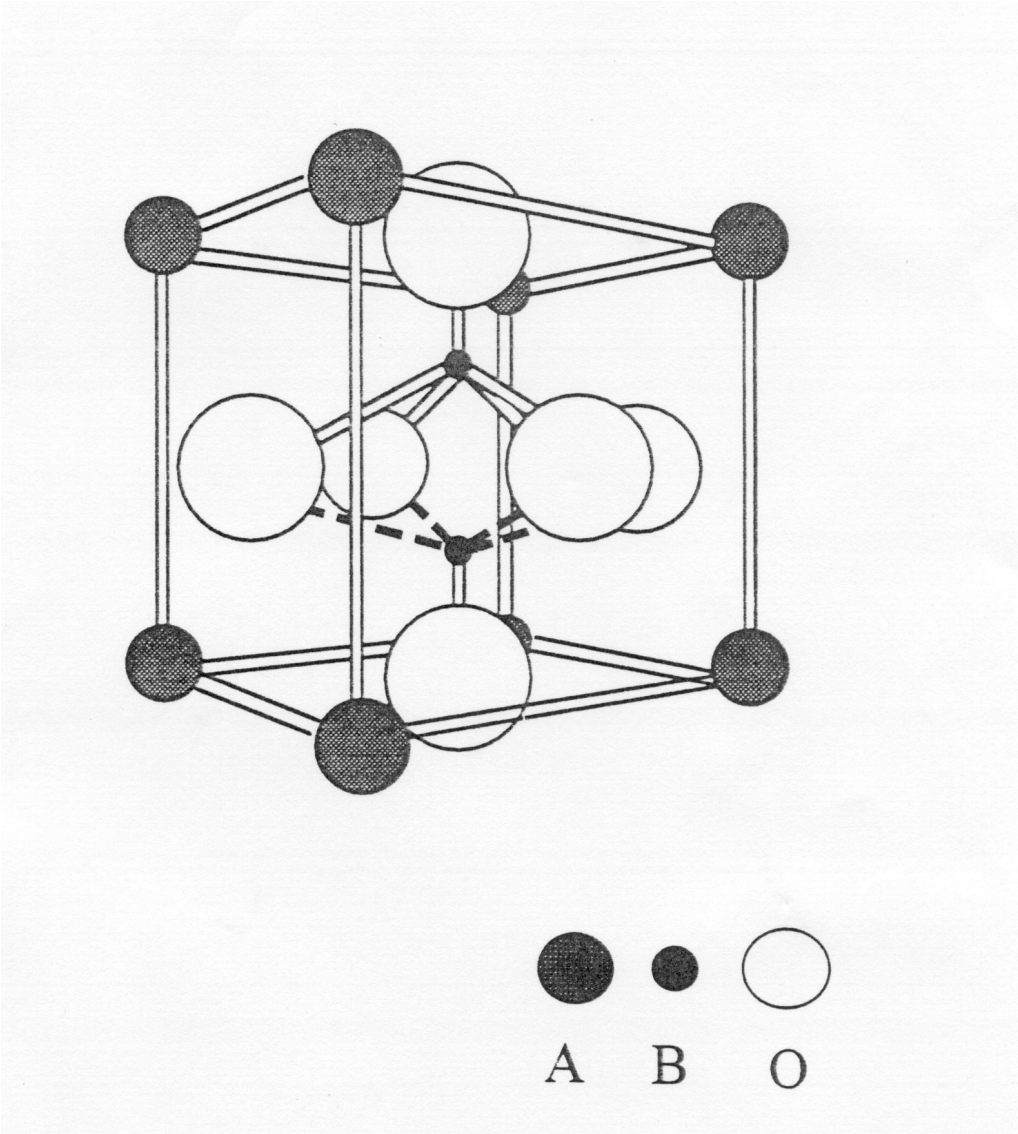

Fig 1.2 ABO_3 perovskite unit cell

have a centrosymmetric structure and hence do not exhibit any spontaneous polarization. This phase is known as paraelectric phase. As the temperature is lowered below the Curie point phase transformation takes place from paraelectric state to ferroelectric state. The center ion is displaced from its body center position and the cubic unit cell deforms to one of the noncentrosymmetric structures such as tetragonal rombhohedral or monoclinic structures. The polarization response with the electric field of these materials is highly non-linear and exhibits a hysteresis loop as shown in Fig.1.3. As applied electric field is increased the ferroelectric domains which are favorably oriented with respect to the electric field grow at the expense of other domains. This phenomenon continues until total domain growth and reorientation of all the domains has occurred in a direction favorable to external field. At this stage the material is assumed to possess saturated polarization (P_{sat}). If the electric field is removed at this point some of the domains do not reorient into a random configuration and thus leaving the material still polarized. This polarization is known as remanent polarization (P_r). The strength of the electric field required to return the polarization to zero is called the coercive field (E_c). Although these features of a ferroelectric material could be used in a wide range of applications the primary focus of the recent research is directed towards development of non volatile random access memories. In principle the memory application is based on the hysteresis behavior of polarization with electric field as shown in Fig.1.3. When an external voltage is applied to a ferroelectric capacitor, there is a net ionic displacement in the unit cells of the ferroelectric material. The individual unit cells interact constructively with their neighbors to produce domains within the material. As the voltage is removed a majority of the domains will remain in the direction of the previously applied field, requiring

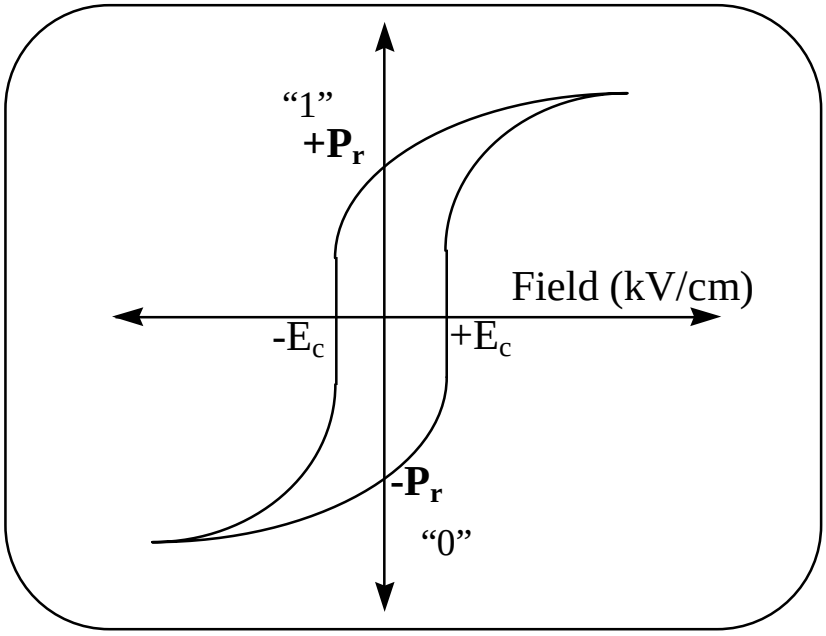

Fig. 1.3 Typical polarization hysteresis loop of a ferroelectric capacitor

compensating charge to remain on the plates of the capacitor. At zero applied field, there are two states of polarization ($\pm P_r$) which are equally stable. Either of these two states could be encoded as " 1" or "0" and since no external field is required to maintain these states the memory device is non volatile. Obviously to switch the state of the device a threshold electric field greater than coercive field is required. Since ferroelectric materials have very high coercive fields (in the order of kV/cm), it is necessary to fabricate these materials in the form of thin films in order to be able to switch the domains from one orientation to the other.

From a digital point of view if a voltage is applied to a ferroelectric capacitor in a direction opposite to that of previous voltage the remanent domains will switch, requiring a compensating charge to flow on to the capacitor plates. If the field is applied in the direction of the previously applied field, no switching takes place, no change occurs in the compensating charge and hence a very reduced amount of charge flow to the capacitor takes place. This phenomenon can be used to read the state or write a desired state into a ferroelectric storing device. Most often ferroelectric memory cells are read destructively by sensing the current transient that is delivered to a small load resistor when an external voltage is applied to the cell. For example, if a memory cell is in a negative state (say $-P_r$) and a positive switching voltage is applied to it, there will be a switching charge and a corresponding switching current. This switching current will consist of a linear dielectric response and a displacement current. A non switching current, for example, is the response of a memory cell in a positive state ($+P_r$) to a positive applied voltage. This current would consist of only a small linear dielectric

response. A sense amplifier and other associated circuitry is used in a FRAM device to determine this transient currents and thereby read the state of the device.

1.3 Purpose of Research

The current research is an effort to realize and solve the problems which could be encountered while fabricating a ferroelectric capacitor for high density FRAM cell. In a high density memory structure, the ferroelectric capacitor is fabricated on the top of a poly-silicon plug, which in turn is connected to the drain of the transistor, as shown in Fig.1.1. Such a configuration would result in constraints for (a) processing of the ferroelectric material and (b) in the choice of the bottom electrode material.

(a) Constraints on the processing of ferroelectric material:

(1) In a high-density memory configuration, transistor is fabricated prior to the fabrication of the capacitor. In order to preserve the integrity of the transistor, the processing temperature of the ferroelectric capacitor should be as low as possible.

(2) Even at low processing temperatures, a ferroelectric capacitor should exhibit well-defined ferroelectric properties.

(3) The ferroelectric capacitor should possess high remanent polarization so that the memory stored in these capacitors could be read in an unambiguous manner.

(4) Coercive field required to switch the memory from one state to the other state should be as low as possible.

(5) The ferroelectric capacitor should possess reproducible properties.

(6) The ferroelectric capacitor should possess minimal fatigue while maintaining low leakage current density.

(b) Choice of the bottom electrodes:

Suitable bottom electrodes should be chosen that would enable the integration of the capacitor on the top of the poly-silicon plug. Bottom electrode structures have to fulfill the most stringent requirements in order to maintain a conductive path between a transistor and a capacitor and preserve the integrity of the devices during the fabrication of the memory structures. The electrode structures which enable the integration of the capacitor on the top of the transistor should satisfy the following conditions.

1. Should resist to the formation of an insulating oxide and remain electrically conductive after the fabrication of the dielectric.
2. Should act as a barrier to the oxygen diffusion.
3. Should act a s a barrier to the silicon diffusion.
4. Should not interact with the dielectric or with the plug material (silicon), or the interaction should be limited and the product of the interaction should be electrically conductive.
5. Should act as a diffusion barrier to the elements in the ferroelectric materials.
6. Should maintain their smoothness during the fabrication process.
7. Should maintain low leakage currents through the capacitor.
8. Should prevent the fatigue of the ferroelectric capacitor.
9. Should promote the crystallization of the ferroelectric material.

1.4 Objectives of the Research

In view of fundamental ferroelectric properties, namely remanent polarization (Pr) and coercive field (E_c), there are two potential ferroelectric materials for FRAM applications[9]. These materials are $Pb(Zr_{0.57}Ti_{0.43})TiO_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT).

(1) **PZT**: PZT possesses a low processing temperature of 650 ^{0}C, a low coercive field of 30 kV/cm and a high remanent polarization of 40 $\mu C/cm^2$. However, PZT capacitors possess a very high fatigue rate (greater than 60% at the end of 10^8 switching cycles) and high leakage current densities (greater than 10^{-5} A/cm^2 at 500 kV/cm). The objective of the current research is to understand the reasons for the high fatigue rate and leakage current densities of PZT based capacitors and provide a solution from a high density memory integration point of view.

(2) **SBT**: Inherently, SBT possesses a fatigue free nature. However, processing temperature of SBT is as high as 800 ^{0}C, which is unsuitable for high density memory integration. SBT could be processed at temperatures as low as 650 ^{0}C, but, these SBT capacitors would not exhibit detectable remanent polarization. The objective of the current research is to lower the processing temperature of SBT while obtaining appreciable remanent polarization. In addition, the current research also focuses on obtaining suitable bottom electrodes that could be used to integrate the SBT based capacitors into high density memories.

1.5 Presentation of results

Results in the current research have been divided into two separate sections. While one of the section deals with the solution for integration of PZT based capacitors, the other

section deals with the integration of SBT based capacitors into high density memory structures.

(1) **Integration of PZT based capacitors**: As discussed in the previous section, the limiting factor for the integration of PZT thin films into high density memory structures involves resolving the fatigue and current density issues of PZT based capacitors. High fatigue rates and high leakage current densities in PZT based capacitors have been attributed to the presence of secondary phases in addition to the pure perovskite phases in PZT based capacitors. In order to enhance the growth of pure perovskite PZT phases over the growth of secondary phases, adequate nucleation sites for the nucleation of perovskite phases are formed by modifying the topographical nature of the bottom electrodes. In the current research, IrO_2/Ir bottom electrode structures are modified to behave not only as electrode and diffusion barrier layers, but also to enhance the growth of pure perovskite phase growth in PZT based capacitors. Subsequently, PZT capacitor, built on the modified IrO_2/Ir electrode structure, is integrated onto a poly-Si plug and the ferroelectric properties of the integrated capacitor structure are studied.

(2) **SBT**: As discussed in the earlier section, integration of SBT thin films into high density memory structures involves lowering the processing temperatures while improving the remanent polarization of SBT based capacitors. In order to achieve lower processing temperatures for SBT thin films, firstly, structure-property relationship of SBT thin films are studied. Ferroelectricity (especially remanent polarization) is referred to as property measured. Structure-property study performed constitutes of three different categories: (1) Grain-orientation-property relationship,

(2) Composition-property relationship and (3) Grain-size property relationship. Knowledge of structure-property relationship revealed the quantitative dependence of remanent polarization of SBT based capacitors on grain-orientation and grain-size. Consequently, processing parameters are manipulated to obtain desirable grain orientation and grain size at lower processing temperatures. Subsequently, electrode structures that could behave as diffusion barriers as well as electrodes are investigated to enable the integration of SBT based capacitors into high density FRAMs.

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