Analysis and Evaluation of Soft-switching Inverter Techniques in Electric Vehicle Applications

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Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

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April 22, 2003
Blacksburg, Virginia

Keywords: soft-switching, zero-voltage-transition, parameter extraction, electromagnetic interference (EMI), electric vehicle

ANALYSIS AND EVALUATION OF SOFT-SWITCHING INVERTER TECHNIQUES IN ELECTRIC VEHICLE APPLICATIONS

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(ABSTRACT)

This dissertation presents the systematic analysis and the critical assessment of the AC side soft-switching inverters in electric vehicle (EV) applications. Although numerous soft-switching inverter techniques were claimed to improve the inverter performance, compared with the conventional hard-switching inverter, there is the lack of comprehensive investigations of analyzing and evaluating the performance of soft-switching inverters.

Starting with an efficiency comparison of a variety of the soft-switching inverters using analytical calculation, the dissertation first reveals the effects of the auxiliary circuit's operation and control on the loss reduction. Three types of soft-switching inverters realizing the zero-voltage-transition (ZVT) or zero-current-transition (ZCT) operation are identified to achieve high efficiency operation.

Then one hard-switching inverter and the chosen soft-switching inverters are designed and implemented with the 55 kW power rating for the small duty EV application. The experimental evaluations on the dynamometer provide the accurate description of the performance of the soft-switching inverters in terms of the loss reductions, the electromagnetic interference (EMI) noise, the total harmonic distortion (THD) and the control complexity. An analysis of the harmonic distortion caused by short pulses is presented and a space vector modulation scheme is proposed to alleviate the effect.

To effectively analyze the soft-switching inverters' performance, a simulation based electrical modeling methodology is developed. Not only it extends the EMI noise analysis to the higher frequency region, but also predicts the stress and the switching losses accurately. Three major modeling tasks are accomplished. First, to address the issues of complicated existing scheme, a new parameter extraction scheme is proposed to establish the physics-based IGBT model. Second, the impedance based measurement method is developed to derive the internal parasitic parameters of the half-bridge modules. Third, the finite element analysis software is used to develop the model for the laminated bus bar including the coupling effects of different phases. Experimental results from the single-leg operation and the three-phase inverter operation verify the effectiveness of the presented systematic electrical modeling approach. With the analytical tools verified by the testing results, the performance analysis is further extended to different power ratings and different bus voltage designs.

TO MY WIFE YING, SON DANIEL

AND

MY PARENTS
SHUZHEN CHEN AND CHANGSONG DONGYE

ACKNOWLEDGEMENT

I would first like to express my deep appreciation to my advisor, Dr. Fred C. Lee. It is my valued opportunity to learn the rigorous attitude toward research and presentation from him. His broad vision, keen insight on the technical issues and creative thinking have greatly inspired me during my stay at Virginia Tech. I am grateful to Dr. Dushan Boroyevich, Dr. Jason Lai, Dr. Dan Y. Chen and Dr. Douglas Nelson for their valuable discussions about my research.

I am especially grateful to receive numerous encouragement, help and guidance from Dr. Qun Zhao, Dr. Jinrong Qian, Dr. Jose Renes Pinheiro, Dr. Chingchi Chen, Dr. Ning Xu, Mr. Kun Zhao, Dr. Ming Xu, Dr. Zhiguo Lu, Dr. Lizhi Zhu, Mr. Bing Lu, Mr. Bo Yang, Mr. Dengming Peng, Dr. Jae-Young Choi, Dr. Peter Barbaso, Dr. Kunrong Wang, Mr. Marcelo Cavalcanti, Mr. Jerry Francis, Mr. Matt Turner, Mr. Michael Pochet, Mr. Changrong Liu, and Mr. Huijie Yu.

It has been a great pleasure to work with so many talented colleagues in the Center for Power Electronics Systems (CPES). I would like to thank Dr. Richard Zhang, Dr. Alex Huang, Dr. Yuxin Li, Dr. Kun Xing, Dr. Xiaogang Feng, Dr. Yunfeng Liu, Dr. Ray-Lee Lin, Dr. Zhenxian Liang, Mr. Dan Huff, Dr. Yong Li, Dr. Dimos Katsis, Dr. Pit-leong Wong, Dr. Xunwei Zhou, Dr. Fengfeng Tao, Dr. Qiong Li, Dr. Peng Xu, Mr. Jianwen Shao, Mr. Huibin Zhu, Mr. Zhenxue Xu, Mr. Rengang Chen, Mr. Jinghai Zhou, Mr. Yuhui Chen, Mr. Mao Ye, Ms. Yingfeng Pang Mr. Wei Shen, Ms. Qian Liu, and Mr. Dion Minter for their great help and meaningful discussions.

I am especially indebted to my colleagues in the DPS (distributed power system) group. Special thanks to Mr. Bing Lu, Mr. Bo Yang, Mr. Francisco Canales, Dr. Zhiguo Lu, Dr. Jinjun

Liu, Dr. Peter Barbosa, Mr. Yang Qiu, Miss. Manjing Xie, Miss. Tingting Sang, Mr. Liyu Yang, Mr. Shuo Wang, Ms. Juanjuan Sun, Mr. Dianbo Fu and Mr. Chuanyun Wang for their delightful discussions. It was my great pleasure to work with such talented and creative team members.

I would also like to acknowledge the CPES administrative and lab management staff, Ms. Linda Gallagher, Ms. Trish Rose, Ms. Marianne Hawthorne, Mr. Robert Martin, Mr. Steve Chen, Mr. Gary Kerr Ms. Teresa Shaw, Ms. Elizabeth Tranter, Ms. Ann Craig, Mr. Mike King, Mr. Jeffery Baston, Ms. Linda Fitzgerald and Mr. Jamie Evans, for their countless help in my CPES work. Thanks to Ms. Amy Shea, who polishes all of my publications, including this dissertation.

I highly appreciate my wife, Ying Zhan, for her continuous love, understanding, encouragement and sacrifice. I am indebted too much to her in the past six years. Thanks to my lovely and naughty son, Daniel, who brings me the pride and happiness of being a father.

My deepest gratitude is sent to my parents, Mr. Changsong Dongye and Ms. Shuzhen Chen, for their countless love, care and sacrifice. I greatly value my father's vision when he encourages me to study abroad and appreciate his great support.

This work was supported by PNGV (partnership of a next generation of vehicles) and the ERC program of the National Science Foundation under Award Number EEC-9731677.

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Chapter 1. Introduction

1.1. Research Background

Since the beginning of the last century, three-phase power inverters have been widely used in industrial drive applications due to their simplicity, as shown in Fig. 1.1. Throughout the development of the power inverter, the power device technique, from the early switching devices, including mercury arc rectifier then the thyristor, to modern devices such as the BJT (bipolar junction transistor), the MOSFET (metal oxide field effect transistor), and the IGBT (insulated gate bipolar transistor), always serve as the major force for further performance advancement of inverters [A1]-[A4][A6]. Among modern power devices, the BJT is a bipolar device. Its advantage is the low conduction loss, but its disadvantage is the very slow switching speed, which causes significant switching losses and prevents its use in operations involving high switching frequencies. The MOSFET is a voltage-controlled channel conduction device [A5] that can achieve very fast switching speed, for example tens of nS. However, there is a conflict in terms of requirement of channel length between the forward conduction voltage drop and the blocking voltage capability. High-voltage-rating MOSFETs (usually >500 V) show much higher conduction losses than the BJT devices. Aiming to combine the low-conduction-loss feature of the BJT and the fast-switching-speed capability of the MOSFET, the IGBT device was introduced in late 1980s as an implementation of the concept of a MOS-controlled bipolar device [A7]. As a result, IGBT devices have become the most popular choice for industrial drive applications [A8]-[A11], which range from a few kW up to several MW and usually require a voltage rating higher than 500V.

The conventional three-phase inverter operates in hard-switching mode, which means the IGBT devices are driven "hard" directly by the gate driver during the switching transient. Due to non-ideal characteristics of the semiconductor switch, the hard-switching operation usually brings relatively high switching losses and a high electromagnetic interference (EMI) noise level [A12]. The typical switching waveforms of the IGBT, measured on a 600V and 300A IGBT, MG300J2YS50 from Toshiba, are given in Fig. 1.2. Normally the high EMI noise level is directly related to high di/dt and dv/dt rates in hard-switching operation, which can be more than 1,000 A/μS and 1,000 V/μS, respectively. High switching frequency, from 10 kHz to 20 kHz, is desired in most drive applications in order to achieve fast dynamic response, manageable audible noise and smaller filtering components. Consequently, the relatively high switching losses and high EMI noise are the major concerns in designing the hard-switching inverter.

Aiming to solve the drawback of the hard-switching inverter, many soft-switching inverter techniques have been proposed [B1]-[B20]. Soft-switching inverters are expected to achieve an efficiency improvement and lower EMI noise. However, past literature indicates that experimental results in different power ratings and applications are sometimes not consistent with the theoretical predictions. The performance limitation and constraints of the soft-switching inverter often puzzle people, and require a fundamental and clear understanding. Furthermore, the development of the electric vehicle (EV) or hybrid electric vehicle (HEV) technology [A13] has undergone substantial progress in recent years. This is mainly driven by the environmental concern in the near future and the petroleum energy concern in the long run. As a core power electronics technology, the three-phase inverter forms the major part of the drive train, as shown Fig. 1.3. This figure indicates that the power provided from the power sources, whether battery

or fuel cell, is delivered to the motor via the three-phase inverter to control the torque of the motor. Due to its simplicity, the hard-switching inverter is employed in several current versions of EVs, such as EV1 from General Motors (GM), Pirus from Toyota, and Insight from Honda; however, the potential use of soft-switching inverters is attractive to all the automakers. Since it has been only a few years since the introduction of the first EV and HEV commercial automobiles using the hard-switching IGBT-based inverter, it is important to now study the general performance aspects of the soft-switching techniques and to make a critical assessment of their use in EV applications. Besides civil transportation use, the next generation of military ships and vehicles all target the use of an electric drive instead of ICE (internal combustion engine) or Turbo engine version. Therefore, a fundamental understanding and analysis of the soft-switching inverter will benefit a variety of important industrial and military applications.

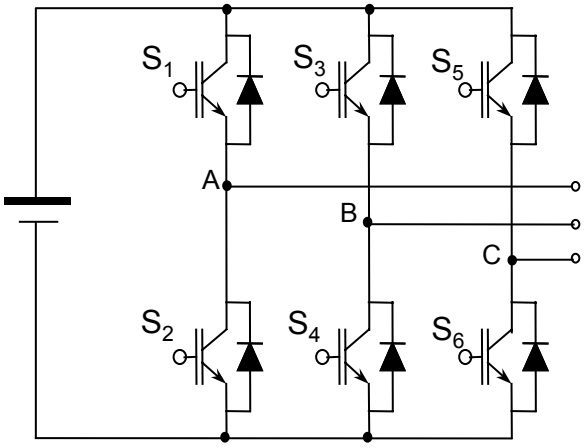
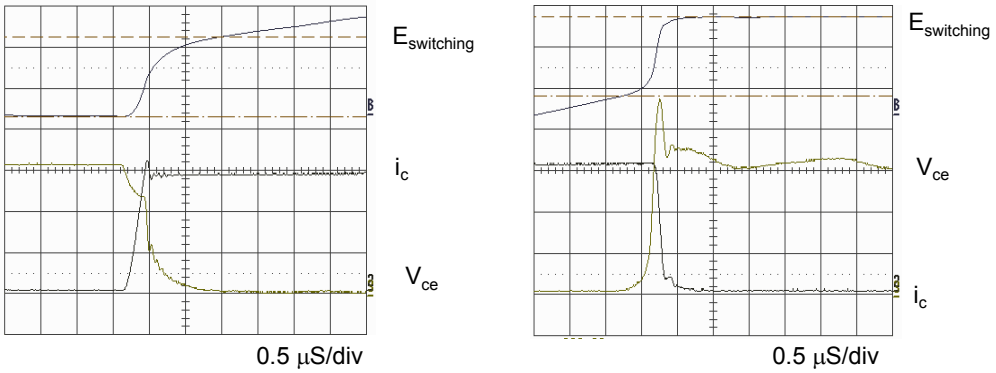


Fig. 1.1. The schematic of a three-phase inverter.



(a) Turn-on (b) Turn-off

Fig. 1.2. Hard-switching of a 600V and 300A IGBT MG300J2YS50, 11.4 mJ/div, 100 A/div, 100 V/div: (a) turn-on and (b) turn-off.

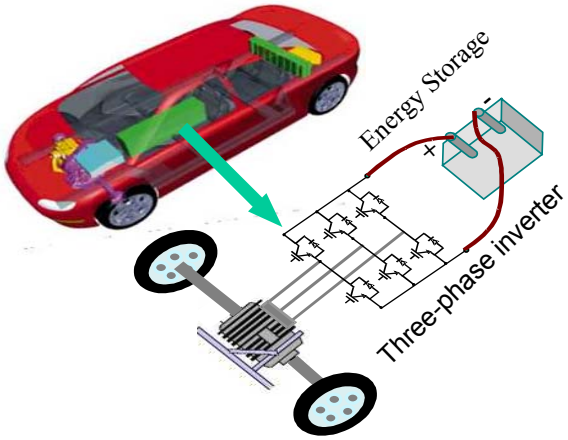


Fig. 1.3. Illustration of a three-phase inverter in the drive train of an EV.

1.2. Classification of Soft-switching Inverters

There have been many soft-switching inverter techniques proposed in the past two decades. According to whether active auxiliary devices are used, these techniques are classified into two types: active approach and passive approach. The categories of the soft-switching inverter techniques are illustrated in Fig. 1.4. Within the category of the passive approach, there exist two major methods, the lossless snubber and lossy R-C-D snubber [B41]-[B45]. The basic principle of the turn-on snubber is to equivalently insert a series inductance at the turn-on path of the

switch, and thus limit the current-rising speed. The principle of the turn-off snubber is to use the parallel capacitor to divert the current during the turn-off, limiting the dv/dt. The energy stored in the snubber inductor and the snubber capacitor needs to be either circulated in the circuit or to be dissipated into the resistor. The circuit approach to circulate the snubbered energy is called the lossless snubber. If the snubber energy is dumped into the resistor, the method is called an R-C-D snubber. Some snubber techniques employ both concepts to reduce the switching losses in the main devices.

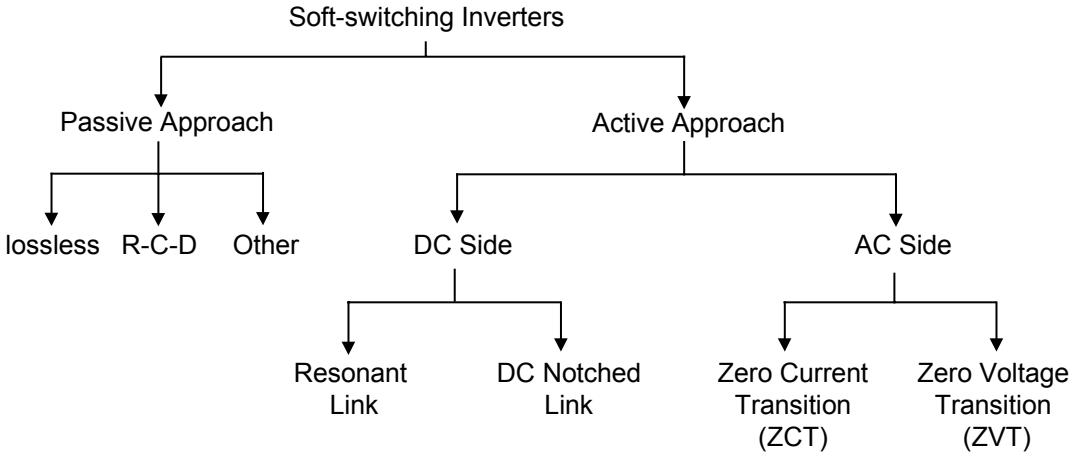


Fig. 1.4. Classification of soft-switching inverter techniques.

One phase of a lossless snubber circuit is shown in Fig. 1.5(a). Auxiliary circuitry does not include the active devices. One set of components, composed of L_s, C_s, D_s, D_r, C_o and D_o, is used to realize the snubber function for the top device S_1. With the same number of components, the other set is used for the bottom devices. Without loss of any generality, it is assumed that the load current is out of node. This means the load current is commutated between the top device and bottom diode. When turning on S_1, the inductor L_s prevents the immediate rise of the S_1 current and withstands the DC bus voltage. So the turn-on loss of S_1 is smaller due to reduced overlap of its voltage and current. The current of L_s is gradually increased until it reaches the

level of the load current. Thus the S_1 starts to carry the full load current. When S_1 is turned on, the energy of C_s begins to discharge, also through the inductor L_s.

When S_1 turns off, the energy stored in L_s must be diverted to components other than the device. Otherwise, the voltage stress will appear on S_1. At turn-off, the energy of L_s is exchanged with the capacitor C_o via D_r and D_s. Therefore, the current of L_s is decreased without any voltage stress induced on device S_1. The snubber capacitor has to be charged to V_{dc} each time S_1 turns off; this charging current comes from the load. So if the load current level is small, an excessive amount of time is required to charge the snubber capacitor. This will either cause the problem of voltage distortion at the inverter output or the high voltage turn-on of the opposite device. Another example of the passive snubber configuration is given in Fig. 1.5(b). This circuit suffers from the stress problems similar to the circuit shown in Fig. 1.5(a).

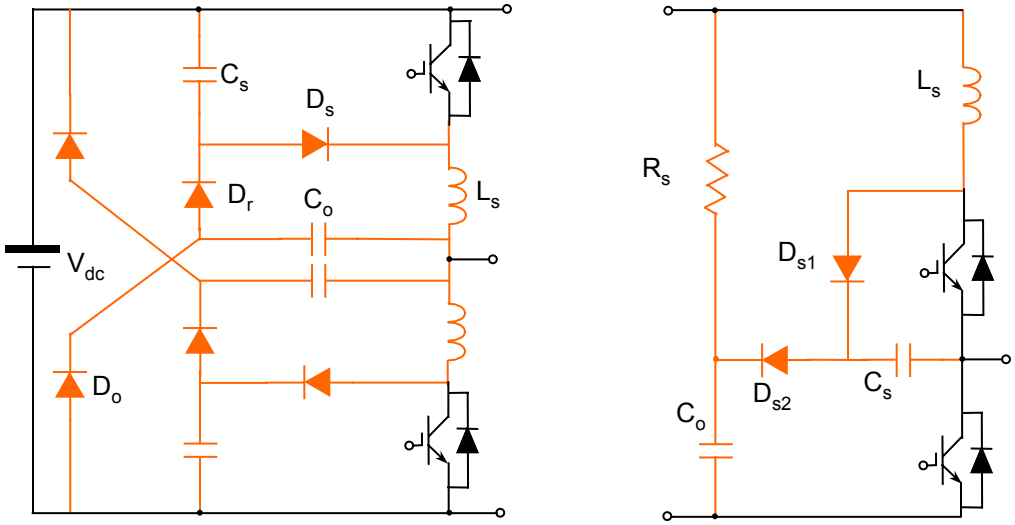


Fig. 1.5. Passive snubber for inverter: (a) Lossless snubber and (b) R-C-D snubber.

As mentioned previously, passive snubber circuits in principle cannot achieve the true soft-switching operation in terms of zero-current switching (ZCS) or zero-voltage switching (ZVS).

Therefore the extent of loss reduction is limited. Because of their high component counts and high current distortion, the passive snubber approaches are deemed an impractical solution in switching frequencies of tens of kHz. There is little interest in applying those techniques in the EV applications. Therefore it is worthwhile to look at the active snubber approaches.

Among the active approaches, there are two basic configurations with which the soft-switching function is realized: DC-side and AC-side soft-switching. The fundamental philosophy of the DC-side soft-switching inverter is to use the auxiliary circuitry to create the zero-voltage duration of the DC bus at the desired switching instant [B3][B4]. Then the corresponding devices in the three phase legs can be switched under the zero-voltage condition. Some components must be installed between the DC input source and the bus of the three-phase bridge switches. As seen in Fig. 1.6, the auxiliary circuit between the DC source and the inverter bus usually connects to the negative terminal of the input DC source. If there is no auxiliary device in series with the DC link, the voltage stress of the DC link is much higher than that of the hard-switching inverter. But if the auxiliary device is in series with the DC link, the current stress will be very high. Different from the DC-side soft-switching concept, AC-side soft-switching inverters realize ZVS or ZCS of individual devices without changing the DC bus voltage [B5]-[B10] [B12]-[B18]. Therefore, the auxiliary circuit needs to be connected with each AC output node of the phase leg, as shown in Fig. 1.7. The main advantage of AC-side soft-switching inverters is that the auxiliary circuit is in shunt with the main bridge. Therefore, the auxiliary circuit does not necessarily carry the load current throughout the inverter operation. It is noted that the DC-side soft-switching inverter requires that some auxiliary components carry the load current.

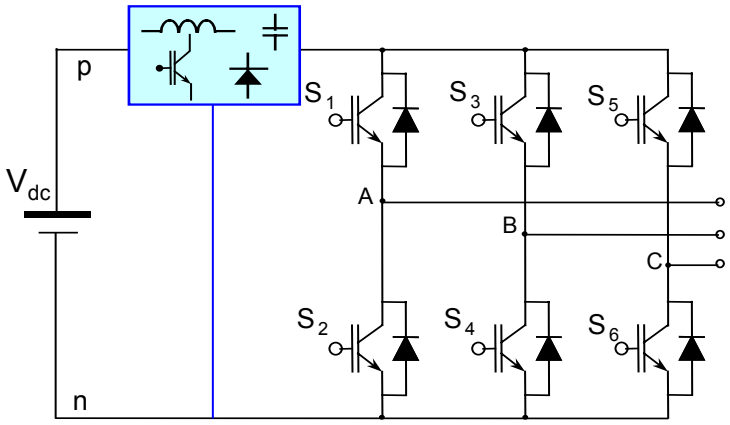


Fig. 1.6. Typical configuration of DC-side soft-switching inverters.

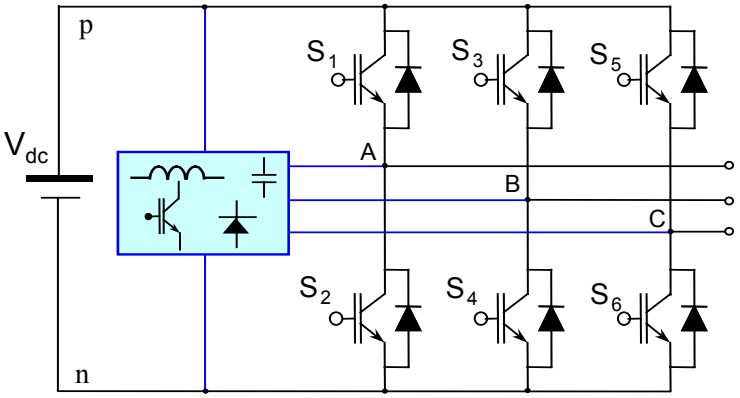


Fig. 1.7. Typical configuration of AC-side soft-switching inverters.

The DC-side converters realize the zero-voltage duration for the link voltage, during which the phase leg's device needs to be switched. Since the link voltage's zero hold event usually has to be created in a constant frequency, the main devices' switching needs to somehow be synchronized. Therefore, the DC-side soft-switching inverters can be further divided into two types according to the control pattern. One type uses the pulse density modulation (PDM) control. The other uses the synchronized pulse-width-modulation (PWM) control. Among the PDM-control types of converters, the RDCL (resonant DC-link converter) and ACRDL (active clamped resonant DC-link converter) are two most representative ones, as shown in Fig. 1.8 and Fig. 1.9. In addition, past research efforts have carefully evaluated the performance of PDM

inverters in EV applications. Two major concerns limit its potential application in EV field. One is that the control scheme is not compatible with the most popular space-vector-modulation (SVM) control in the motor-drive applications. Without a substantial performance improvement, it is very difficult to make industry adopt a totally different control scheme while discarding the well-established SVM control. The other concern is that the device voltage stress is usually 1.3-1.5 times that of the dc-link.

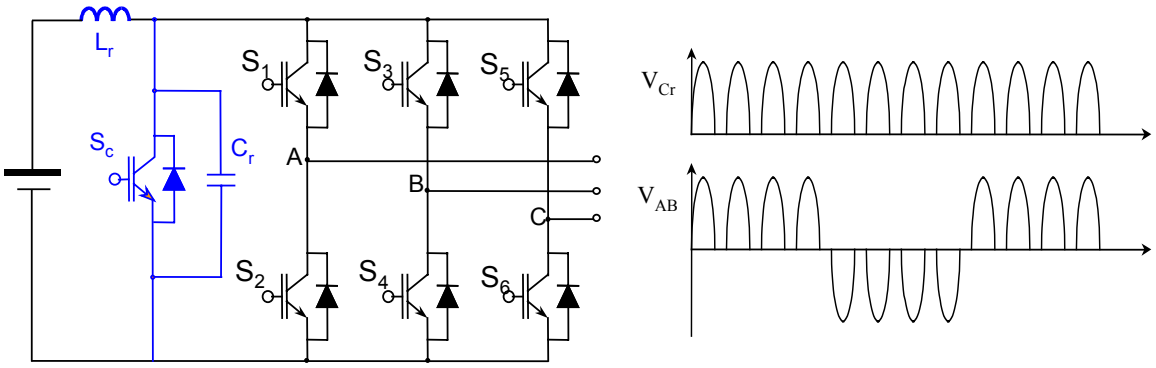


Fig. 1.8. Resonant DC-link converter and its waveforms.

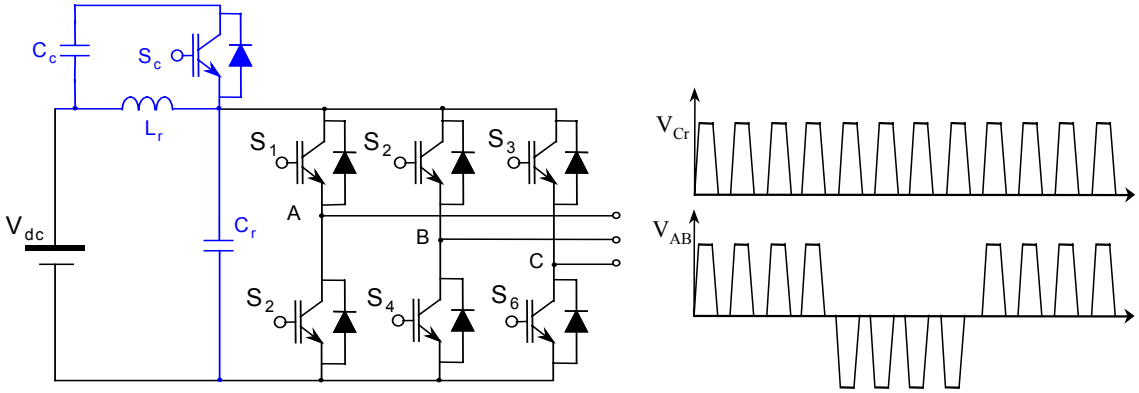


Fig. 1.9. Active-clamped resonant DC-link converter.

Therefore it is important to thoroughly investigate the AC-side soft-switching inverter. Two typical examples of the AC-side soft-switching inverters are shown in Fig. 1.10 and Fig. 1.11. The first figure shows the auxiliary resonant pole converter (ARCP) [B2][B5]. Each set of the auxiliary circuit is composed of two switches that form a bi-directional switch configuration and

one resonant inductor. The snubber capacitor is usually paralleled with each main switch. The ARCP inverter can realize ZVS turn-on and snubber capacitor-assisted turn-off. Another inverter is the zero-current-transition (ZCT) inverter [B12]-[B15], as shown in Fig. 1.11. One set of auxiliary circuits consists of one half-bridge, smaller rated-current switch and the L-C resonant tank. By controlling the timing of the auxiliary switches, the ZCT converter can realize zero-current turn-off and near-zero-current turn-on. Both types of AC-side soft-switching inverters put the auxiliary circuit in shunt with the main power-processing bridge circuit. Therefore, the auxiliary circuit does not need to carry the full load current. This is one major advantage of the AC-side inverter over the DC-side inverter, which often put the auxiliary circuitry in series with the main power flow path.

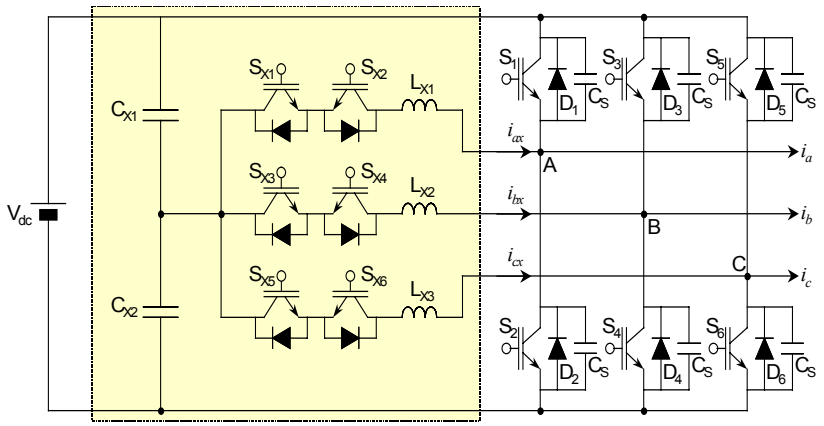


Fig. 1.10. The ARCP inverter.

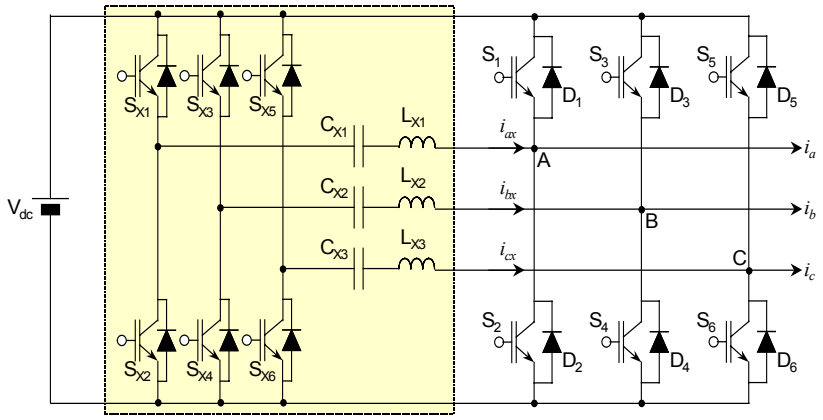


Fig. 1.11. The six-switch ZCT inverter.

1.3. Motivation of Study

As stated in earlier sections, many soft-switching inverter techniques have been proposed to improve the performance over the conventional hard-switching inverters. Among those, it is clear, based on the background explanation of classified soft-switching inverters, that the performance of AC-side soft-switching converters need to be thoroughly understood in the EV or HEV applications in order to help the auto-makers make a wise choice. Besides the performance improvement, performance constraints also require special attention in the study.

When an extensive survey about soft-switching inverter techniques was conducted by the author, it was found that very few research activities have targeted an overall performance study and general analysis of the soft-switching inverter [B23]-[B25]. Due to the lack of thorough investigations into the general performance limitation and comparison of different soft-switching techniques, it is very difficult to choose a soft-switching inverter for particular applications. Although some papers did touch on a comparison of the different soft-switching inverters [B28]-[B31], those papers usually investigated the particular topologies and the research results become ambiguous when applied to EV applications. Some papers only attempted to treat the limited

aspects of the soft-switching inverters, for example EMI in the specified soft-switching techniques, and some only relied on the simulation method to draw an unconvincing conclusion [B32][B33]. Therefore, a systematic study of general performance characterization of the soft-switching inverters is mandatory in order to form any conclusions about their performance not also for general applications but also for particular applications, such as EV and HEV. Some research efforts have shown benefits in EV applications [B34][B35], which again raise the already high interest in potential applications for soft-switching technology.

From past studies, important performance aspects can be identified as follows: the loss-reduction related thermal management, EMI noise level, harmonic quality and control complexity. Therefore, the generic analysis of those performance aspects is conducted through theoretical modeling, simulation and experimental verification. A comprehensive assessment of the soft-switching inverter in EV applications would be very beneficial for automobile industry manufacturers when a lot of research and development efforts aim to greatly improve the drive train performance.

One major challenge in understanding the soft-switching technique's performance is its effects on EMI noise. The EMI performance of the soft-switching inverter is always claimed to be better than that of the hard-switching inverter. What the real performance is and with what mechanism the EMI noise is generated in the soft-switching inverter is not yet well addressed.

1.4. Dissertation Outline

This dissertation presents the systematic analysis and critical assessment of the AC-side soft-switching inverters in EV applications.

Starting with an efficiency comparison of a variety of AC-side soft-switching inverters, using analytical calculation, the implications of loss reduction due to the auxiliary circuit's operation and control are revealed in chapter 2. Three soft-switching inverter candidates, the ARCP inverter, the six-switch ZCT inverter, and the three-switch ZCT inverter, are identified as achieving high-efficiency operation.

Then, Chapter 3 first presents the design and implementation of one hard-switching inverter and the three chosen soft-switching inverters. Targeted at a small-duty EV application, these inverters are designed and implemented with the continuous power rating of 55 kW. Based on the dynamometer, the comprehensive evaluation results are summarized in terms of the efficiency, the EMI performance and the total harmonic distortion (THD). In particular, the EMI noise spectrum comparison offers important insights into the soft-switching inverter's EMI performance since little understanding has been achieved so far in previous literature. Besides, the harmonic distortion effects of the short pulse limitation in soft-switching inverters are analyzed. A new SVM control strategy is proposed to alleviate the potential harmonic problem caused by the minimum pulse width set by the soft-switching operation.

Then, Chapter 4 presents the proposed advanced IGBT model for the electrical performance analysis. To address the issues of the overly complicated scheme of existing parameter-extraction methods, a new parameter-extraction scheme is proposed to establish an accurate physics-based IGBT model. Then, the impedance-based measurement method is also developed to derive the internal parasitic parameters of the popular half-bridge IGBT modules. Using the concept of a Δ-connection converted to a Y-connection network, a step-by-step procedure is developed to extract the parasitic inductance of the IGBT package. A complete IGBT simulation

model is then implemented in Saber. The comparison between simulation and experiments verifies the effectiveness of the presented IGBT modeling method.

Chapter 5 presents the modeling and analysis of the three-phase hard-switching and soft-switching inverters. Following the detailed IGBT modeling work described in Chapter 4, the finite element analysis (FEA) software is adopted to develop the model for the laminated bus bar, which is often used to interconnect different phases' devices. This model includes the coupling effects of different phases. Then the complete three-phase inverter model is developed. Experimental results from the single-phase and three-phase operations verify the accuracy of the presented systematic EMI modeling approach for three-phase inverter. Based on the inverter system EMI simulation, the dominant factors affecting noise generation and modeling accuracy are analyzed. The EMI noise prediction can be accurate up to tens of MHz. With the developed calculation and modeling method, the performance analysis is extended to different power ratings and to different power bus voltage designs for EV applications.

Chapter 6 presents the final conclusions of this study in the analysis of soft-switching inverter techniques and an evaluation of their performance in EV applications. Some useful guidance for applying soft-switching inverters is summarized and suggestions for future work are given.

Chapter 2. Topology Selection of Soft-switching Inverters

2.1. Introduction

One of the major aims of soft-switching techniques is to reduce the switching loss and dynamic switching stress, thereby achieving high-switching-frequency operation. However, when considering the overall inverter efficiency, one must be aware that, due to non-ideal soft-switching conditions and losses in the auxiliary circuit, not all the soft-switching inverters have better efficiencies than the hard-switching inverters. In addition, the different timing control for the auxiliary switches may also affect loss reduction [B36]-[B38].

This chapter analytically evaluates the efficiencies of six typical AC-side soft-switching inverters for EV applications [B40]. These inverters include the ARCP inverter, the ZVT inverter with coupled inductors (ZVTCI) [B9], the ZCT inverter including both six-switch [B15] and three-switch versions, the ZVT inverter with a single switch (ZVTSS) [B8], and the ZVT inverter with a single inductor (ZVTSI) [B7]. The selection of these converters mostly covers the variation of the AC-side soft-switching inverters. One common feature of these inverters is that the auxiliary resonant circuit is placed out of the main power path, which is important for reducing the conduction loss and the electrical stress of the auxiliary circuit in high-power applications. The operation principles of these soft-switching inverters are described. Then, targeting a specified EV application, a suitable design is presented. To compare the loss-reduction performance, an IGBT module with 600V and 300A rating is adopted as the main power devices. The device losses are experimentally characterized for both hard-switching and

soft-switching conditions. Finally, based on the loss-evaluation results, three candidate soft-switching inverters are chosen for hardware implementation and experimental evaluation.

2.2. Operation Principle and Design of Soft-switching Inverters

The electrical specification of a small-duty EV is adopted as the design target of different soft-switching inverters. It is similar to the rating of General Motors' EV-1, which is a two-passenger electric car first introduced in 1997. Without the loss of generality, the inverter specifications for the loss analysis are given as follows.

Po: continuous output power 55 kW

Vdc: the nominal DC bus voltage is 324 V

PF: the load power factor is 0.9

M: the modulation index is assumed to be 0.86.

For the targeted power rating and the bus voltage, the MG300J2YS50, a 600V and 300A IGBT from Toshiba, is chosen as the main power devices. As explained in the previous chapter, there are also a variety of AC-side soft-switching inverters. They belong to two major categories, ZVT and ZCT. Six soft-switching inverters are selected to represent the typical AC-side soft-switching schemes. These are the ARCP ZVT inverter, the ZVTCI, the six-switch ZCT inverters, the three-switch ZCT inverter, the ZVTSS, and ZVTSI.

2.2.1. Auxiliary Resonant Commutated Pole Inverter

The ARCP inverter realizes ZVS turn-on by using three independently controlled auxiliary branches, as shown again in Fig. 2.1. This is a ZVT topology that appears to be suited for high power DC/AC applications. Since the control of the auxiliary circuit is piggy-backed on the main

power stage circuit, the traditional SPWM (sine pulse-width-modulation) and SVM (space-vector-modulation) techniques can be directly applied. The auxiliary branch is turned off under ZCS and the auxiliary switches only need to block half the DC bus voltage. The auxiliary circuit is composed of the snubber capacitor C_S, the resonant inductor L_X, and the auxiliary switch S_X. S_X has the bi-directional voltage blocking capability and can conduct bi-directional current. Usually S_X is composed of one pair of switches, S_{X1} and S_{X2}. In Fig. 2.1, S_{X1} allows the auxiliary current to flow only into the main inverter leg, and S_{X2} enables the auxiliary current to flow out of the main inverter leg. For the convenience of explaining the control timing during the load current commutation, the load current is considered to be constant during one switching cycle, and the middle point of the bus voltage is constant.

2.2.1.1. Principles of Operation

Through most of a switching cycle, the auxiliary switch is off and the ARCP inverter behaves like a standard PWM inverter. S_X is only turned on during the load current commutation. Fig. 2.2 shows the ZVS turn-on principle when the load current is commutated from D_2 to S_1.

- Pre-charging stage [t1, t2]: Before t1, the load current i_a flows through the diode D_2. At t1, S_{x2} is turned on. The voltage across the resonant inductor is half of the DC bus voltage. The current of the auxiliary inductor L_{x1}, i_{ax}, linearly increases until it reaches the load current i_a at t2. Correspondingly, at the same time, the current of D_2 decreases to zero at t2.
- Boost-charging stage [t2 t3]: After D_2 is turned off naturally at t2, S_2 is kept on and conducts the extra current portion of i_a. i_{ax} keeps increasing until it is equal to $i_a + i_{boost}$, in which i_{boost} is the pre-designed level.

- Resonant stage [t3, t4]: The main switch S_2 is turned off at t3. So the two main switches and their anti-paralleled diodes are off at t3. Then the resonant inductor L_{x1} starts to resonate with the two snubber capacitors C_S across the main switches. Due to the resonance, the voltage of S_1 decreases to zero at t4.
- Discharging stage [t4, t6]: Once D_1 starts conduction at t4, the voltage across L_{x1} is reversed from the positive $1/2V_{dc}$ to the negative $1/2V_{dc}$. The inductor current i_{ax} is thus decreased linearly. Before the inductor current decreased to load current at t5, the main switch S_1 could be turned on under the zero-voltage condition. D_1 naturally turns off at t5, and S_1 gradually takes over the load current from D_1. After the resonant inductor current decreases to zero at t6, the auxiliary switch S_{x2} can be turned off under ZCS condition. Then the circuit resumes normal operation.

When the load current is commutated from switch to diode, it is not usually necessary for the auxiliary switch to be turned on except at very low load current, when the switch turns off under snubbered conditions. The snubber capacitor C_S limits the voltage-rising rate. Therefore, the overlap between the device voltage and current is reduced, and thus the turn-off switching loss is reduced. Due to the ZVS turn-on capability, the energy stored in C_S will not dissipate into the device. When the load current becomes very small, the auxiliary switch needs to be turned on so as to ensure that the ZVT is completed within the dead time. Otherwise, the energy of C_S that exists due to remaining voltage will dissipate into the switch that is to be turned on. In the ARCP inverter, the main switch turns on under ZVS and turns off under the assistance of the snubber capacitor. The auxiliary switch turns on and off with ZVS.

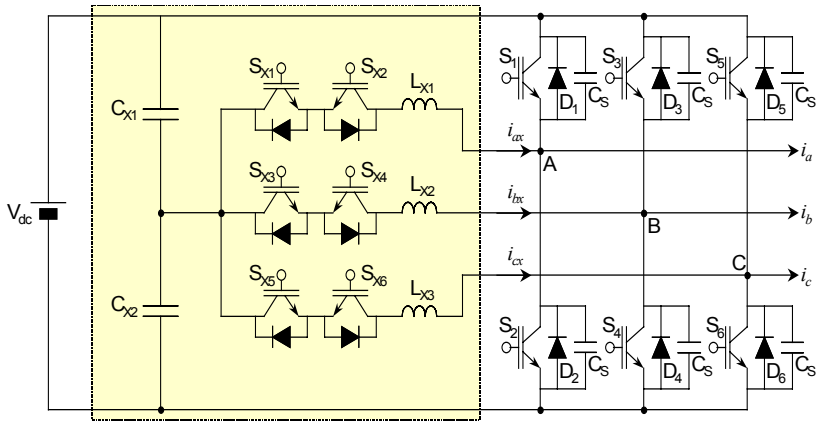


Fig. 2.1. The three-phase ARCP.

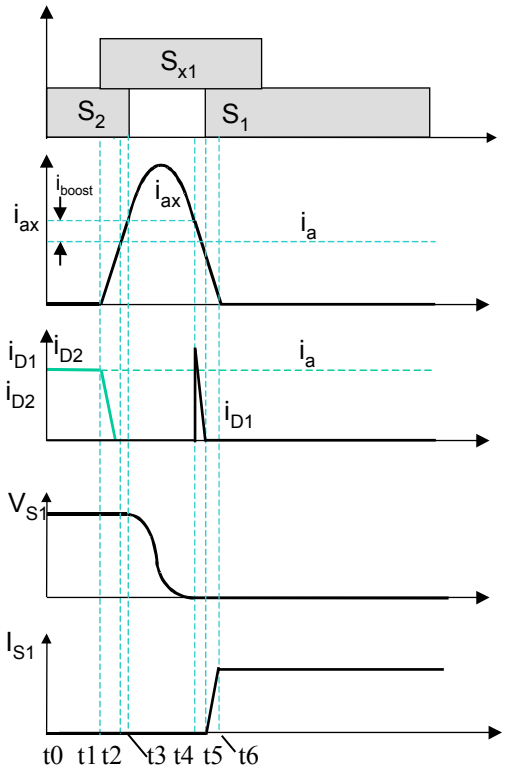


Fig. 2.2. Key waveforms of ZVT turn-on.

2.2.1.2. Design Considerations

Similar to all other ZVT schemes, the turn-off loss is reduced by adding snubber capacitors across the main switches. Thus, the first step of the design is to select the suitable resonant

capacitance according to the dv/dt requirement and the achieved turn-off loss reduction. C_S is selected such that a further increase of C_s will not help much to reduce the turn-off losses. On the other hand, C_s should not be so small that the auxiliary circuit branch conducts a relatively high current during the switching transition. Usually a capacitance value between 0.05μF to 0.47μF is selected according to different power levels. The resonant inductor value should not be too small either, since a small L_x causes a high peak resonant current. A reasonable transition time dictates the maximum value of L_x. Based on this explanation, the design guideline is presented as follows.

1. Choose the initial value of C_s to ensure sufficient turn-off loss reduction and to meet the dv/dt requirement.
2. Determine the resonant tank impedance $Z_r = \sqrt{L_x/C_r}$ based on the peak current allowed in the auxiliary branch. Notice that C_s is the equivalent resonant capacitance during the ZVS turn-on. For the ARCP inverters, $C_r = 2C_s$.
3. Determine L_x using C_r and Z_r. Adjust L_x and C_r to get a suitable T_r, such that $T_r = 2\pi\sqrt{L_r C_r}$.
4. Choose dead time T_d according to resonant circle T_r. Usually T_d should be around half of T_r.
5. Determine the pre-charging time to control the boost current level i_{boost}. The selection of i_{boost} is to compensate the practical circuit losses in order to guarantee that the resonance between the resonant inductor and the snubber capacitor leads to the zero-voltage condition for the switch that is to be turned on. The pre-charging time T_{pre}, indicated by t3-t1 in Fig. 2.2, is given by

$$T_{pre} = \frac{2 \cdot L_x \cdot (i_{boost} + i_{load})}{V_{dc}} : \tag{2.1}$$

As seen from (2.1), the pre-charging time is actually designed to vary according to the instantaneous load current i_{load}. This is the so-called variable timing control, which builds the auxiliary circuit current adaptive to the load current in order to minimize unnecessary losses in the auxiliary branch.

For the targeted inverter specification, a design of the ARCP inverter is obtained. The resonant tank is designed as L=2 μH, C=0.1 μF. T_d is chosen as 1.4 μS.

2.2.2. Six-switch Zero-current-transition Inverter

The six-switch ZCT inverter, as shown in Fig. 2.3, features three independent auxiliary branches, each consisting of a resonant tank composed of a series-connected inductor L_x and capacitor C_x and a half-bridge switching module containing two IGBTs and two freewheeling diodes. It can realize zero-current turn-off for all of the switches and diodes in both the main power stage and the auxiliary circuits. Thus, the turn-off loss can be almost eliminated. Also, the main switches can be turned on at zero-current condition and the diode reverse recovery problem can be alleviated. Furthermore, the control of the auxiliary circuit is piggy-backed on the main power stage circuit. The control scheme of the six-switch ZCT inverter adjusts the auxiliary switch timing to control the circulating energy and voltage stress across the resonant capacitor. Therefore, it is an improved version of the ZCT inverter, as compared with the other ZCT control schemes proposed by Mao and Hua [B12][B14].

2.2.2.1. Principles of Operation

Since the three phases are identical, the discussion can focus on only one phase. Since the auxiliary switch control is dependent on the load current direction and the level, it can be illustrated from one half-bridge phase-leg circuit, as shown in Fig. 2.4. Depending on the

directions of i_{load}, there are two cases for gating the switches. Since the circuit operation for the cases of $i_{load}>0$ and $i_{load}<0$ are symmetrical, the operating principle only needs to be explained for one case. Fig. 2.5 shows the key operational waveforms within one switching cycle for the $i_{load}>0$ case. For the convenience of explanation, the load current is assumed to be constant during one switching cycle.

- Turn-on transition I [t0, t2]: Before S_1 is turned on, S_{x2} is turned on at t0. L_{x1} and C_{x1} start to resonate, and the resonant current i_{ax} increases in the negative direction to a peak and then decreases to zero at t1. After t1, i_{ax} reverses its direction and flows through D_{x2}. S_{x2} is then turned off at the zero-current condition. As i_{ax} increases in the positive direction, the current in D_1 is diverted into the auxiliary circuit. i_{ax} reaches i_{boost} at t2, and the current in D_1 drops to zero. The main switch S2 should turned off before t2.
- Turn-on Transition II [t2, t3]: Since D_1 has stopped conducting and the top switch S_1 is still off, i_{load} can flow only through the resonant tank, charging C_x linearly. There is no voltage drop across L_x; thus, the voltage across the main switch S_1 is the difference between V_{dc} and V_x, and is less than V_{dc}.
- Turn-on Transition III [t3, t4]: S_1 is turned on at t3 with the reduced switch voltage. The current in D_2 has been diverted to the auxiliary circuit since t2, and the time between [t2, t3] allows the carrier in D_2 to be recombined properly. After t3, i_{ax} decreases toward zero because the negative V_{dc} is applied to the resonant tank.
- Switch-on Stage [t4, t5]: At t4, i_{ax} drops to zero, and D_{x2} is turned off naturally. The auxiliary circuit stops resonance and is functionally disconnected from the main circuit. i_{load} flows

through the top main switch S_1, and PWM operation resumes. C_x keeps a negative voltage during this period.

- Turn-off Transition I [t5, t7]: Before S_1 is turned off, S_{x1} is turned on at t5. L_x and C_x start to resonate again. As i_{ax} increases in the positive direction, the current in S_1 decreases. After t6, i_{ax} exceeds i_{load}, the current in S_1 drops to zero, and D_1 starts to conduct the remaining current. S_1 is turned off at the zero-current condition. i_{ax} increases to a peak and then drops to i_{load} at t7. S_1 should be gated off between t6 and t7 without causing turn-off loss.
- Turn-off Transition II [t7, t8]: After t7, D_1 stops conduction. Since S_1 has been turned off and D_2 is still reverse-biased, i_{load} can flow only through the resonant tank, charging C_x linearly.
- Turn-off Transition III [t8, t10]: At t8, the voltage on C_x is charged to V_{dc}; thus, D_2 is forward-biased and starts to conduct current. V_{dc} is applied to the resonant tank, and L_x and C_x start to resonate again. i_{ax} decreases to zero and V_x reaches a peak at t9. Since V_x is still greater than V_{dc}, the resonance of the resonant tank continues. i_{ax} later reverses its direction again and starts to flow through D_{x1}. S_{x1} is turned off under the zero-current condition. S_2 can be turned on after t8.
- Diode-on Stage [after t10]: i_{ax} decreases to zero at t10, and thus D_{x1} turns off naturally. i_{load} flows through the bottom main diode D_2, and PWM operation resumes.

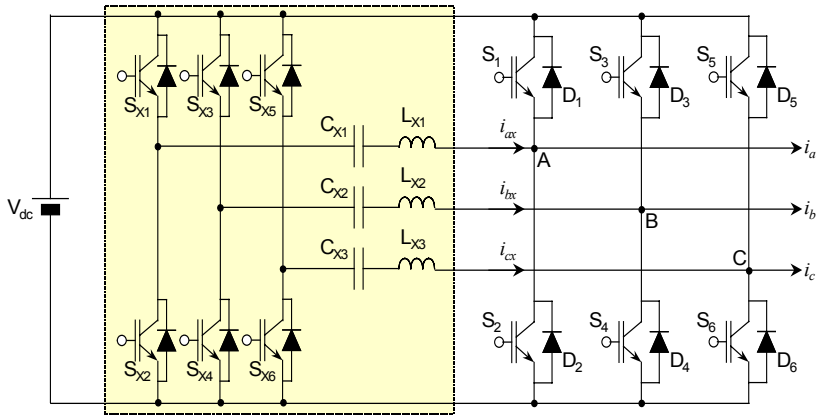


Fig. 2.3. The six-switch ZCT inverter.

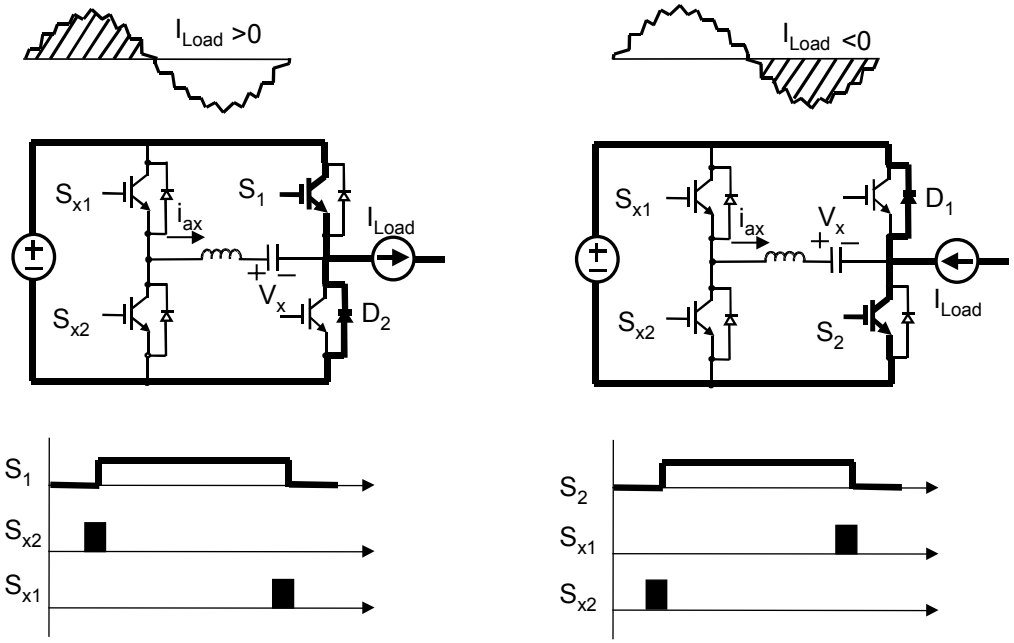


Fig. 2.4. ZCT control schemes at different load current directions.

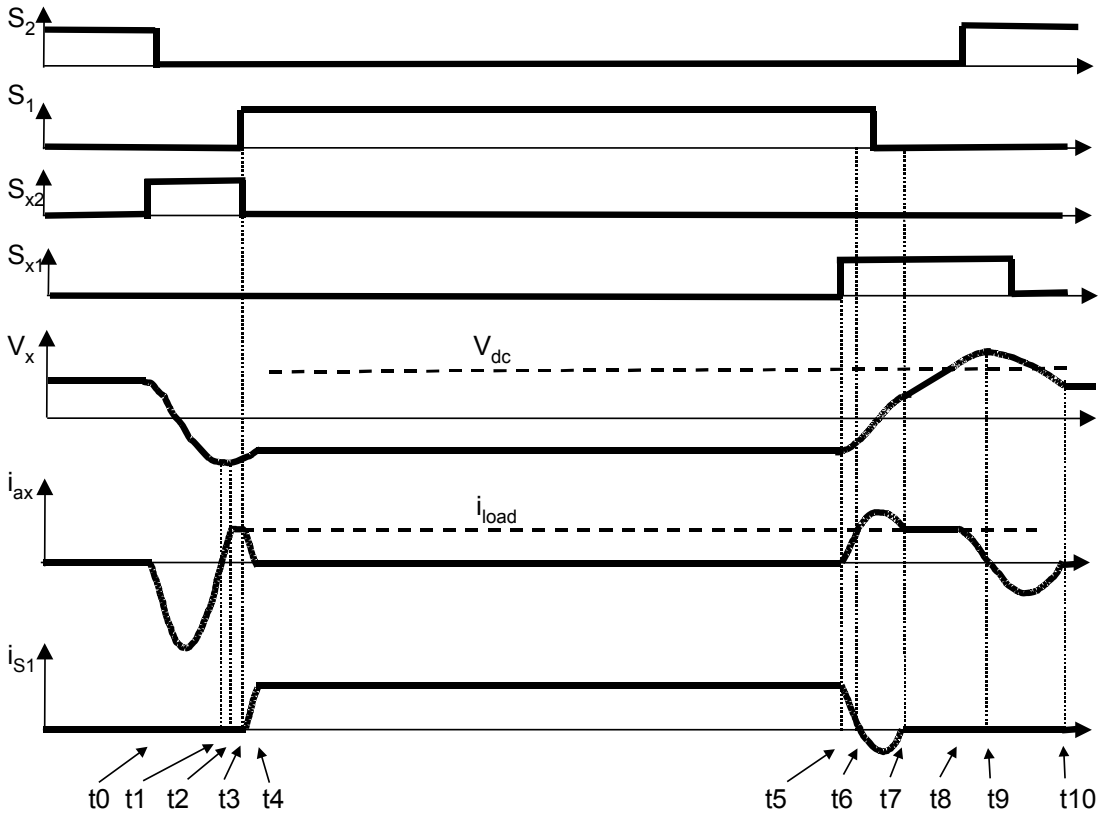


Fig. 2.5. The operational waveforms of the six-switch ZCT inverter.

2.2.2.2. Design Considerations

The design rule is to choose the resonant impedance Z_o that ensures the ZCT turn-off for the maximum load current subject to the zero current turn-off, I_{max}. On the other hand, the resonant period T_o needs to avoid an excessively long duration. The detailed design optimization has been discussed in [B15]. Once the resonant tank impedance and T_o are determined, the resonant inductor and the capacitor values can be obtained by the following expressions:

$$L_X = \frac{1}{2\pi} T_o Z_o \text{, and} \tag{2.2}$$

$$C_X = \frac{1}{2\pi} \frac{T_o}{Z_o} \text{ .} \tag{2.3}$$

2.2.3. Zero-voltage-transition Inverter Using Coupled Inductors

The ZVTCI, as shown in Fig. 2.6, is actually same as the ARCP inverter. The ZVTCI uses coupled inductors with a turns ratio of 1:1 to get the equivalent half of V_{dc}, while the ARCP directly uses the capacitor bank to obtain the half of V_{dc}. The operation principle of ZVS turn-on can be explained from Fig. 2.7 and the load current is assumed to be constant, $i_a=i_{load}$.

- Pre-charging stage [t1, t2]: At t1, S_{x2} is turned on. The voltage across the resonant inductor is the DC bus voltage. The inductor current is charged linearly until it reaches half of the load current i_{load}. The D_2 current is decreased to zero at t2 when the resonant inductor current reaches half of the load current.
- Over-charging stage [t2, t3]: After D_2 is turned off naturally at t2, S_2 is kept on and conducts the extra boost current. The auxiliary inductor current keeps increasing to a certain designed level to ensure the zero-voltage condition.
- Resonant stage [t3, t4]: Main switch S_2 is turned off at t3. The leakage inductor of the coupled inductor becomes resonant with the two capacitors across the main switches. The lower capacitor voltage reaches V_{dc} at t4 and is clamped at V_{dc} by diode D_1.
- Discharging stage [t4, t6]: Once diode D_1 begins to conduct at t4, the resonant inductor is applied by a negative half of V_{dc}. The inductor current is thus decreased linearly. Before the inductor current decreases to the level of the load current at t5, the S_1 voltage is zero. The main switch S_1 could be turned on under zero-voltage condition. Diode D_1 is naturally turned off at t5 after its current decreases to zero and S_1 gradually takes over the load current. After the resonant inductor decreases to zero at t6, the auxiliary switch S_{x2} can be turned off under the zero-current condition.

The design guideline is the same as that described for the ARCP inverter except that the equivalent resonant capacitor is $C_r = C_s/2$.

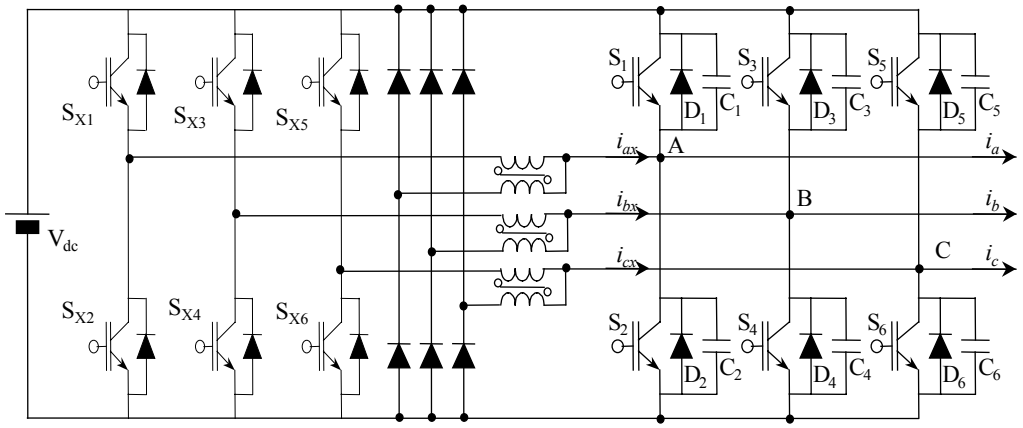


Fig. 2.6. ZVT inverter using coupled inductors.

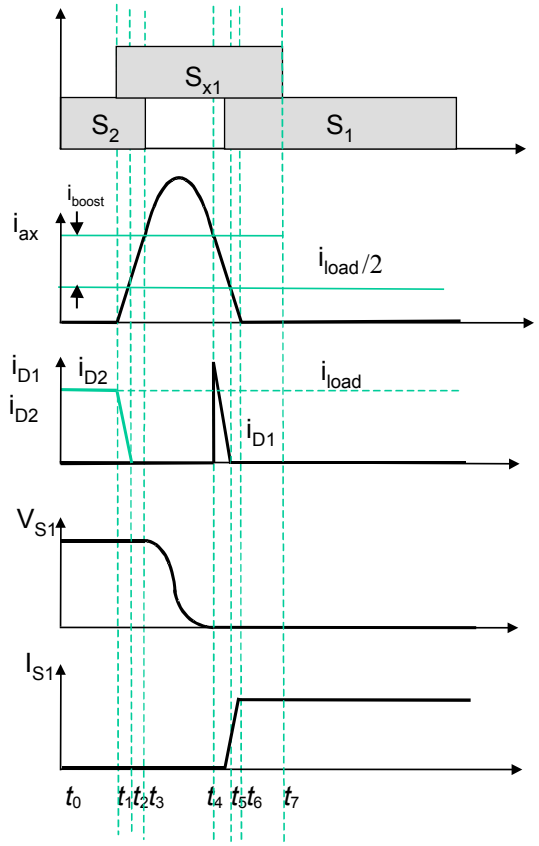


Fig. 2.7. Operating waveforms of ZVT inverter using coupled inductors.

2.2.4. Three-switch Zero-current-transition Inverter

The three-switch ZCT inverter is shown in Fig. 2.8, and also has the three independently controlled auxiliary circuit branches. Since only one auxiliary switch can be used to control the resonant tank's resonance for each leg, the operation principle is different when the load current direction is different. Based on the one-leg configuration in Fig. 2.9, the operating principle can be explained from Fig. 2.10. The load current I_{Load} is assumed to the same over the switching cycle.

I_{Load} >0 case: Sx is turned on at t_0 and so L_x and C_x start to resonate, as shown in Fig. 2.11. At t2, the resonant current I_x reaches a peak and S_1 is turned on. Ideally, this peak equals I_{Load}, and the current in D_2 drops to zero before S_1 is turned on. Although it will be attenuated by the power loss in the resonant path, this peak can still be close to I_{Load}, and S_1 is turned on at the near-zero-current condition. Before S_1 is turned off, S_x is turned on again at t5. After t7, I_x is greater than I_{Load}, and the anti-parallel diode across S_1 starts to conduct the surplus current. S_1 is turned off under the zero-current condition.

I_{Load} <0 case: The operation goes through eight topological stages, as shown in Fig. 2.11. The initial stage is that I_{Load} freewheels through diode D_1. In the steady state, there is a positive voltage, V_x, across C_x, where $0<V_x<V_{dc}$. V_x cannot be negative; otherwise, diode D_c will conduct.

- Turn-on Transition I [t0, t1]: S_x is turned on at t0, and L_x and C_x start to resonate. I_x increases to a peak at t1 and the current in D_1 is reduced to near zero. The gate-driver signal for the top main switch S_1 should be removed before t1.

- Turn-on Transition II [t1, t3]: S_2 is turned on at t1 under the near-zero-current condition without much turn-on loss. After t1, the resonant tank is short-circuited by S_2, and I_x decreases toward zero. At t_2, I_x drops to zero and continues to resonate in the negative direction in which D_x conducts. S_x is turned off at the zero-current condition. After half a resonant cycle, I_x returns to zero at t3.
- Turn-on Transition III [t3, t4]: At t3, D_x is turned off naturally. Since the magnitude of V_x is still greater than V_{dc}, the auxiliary circuit continues to resonate; I_x flows in the positive direction and is conducted by D_c.
- Switch-on Stage [t4, t5]: At t4, I_x again returns to zero, and D_c is turned off naturally. I_{Load} flows through S_2, and PWM operation resumes
- Turn-off Transition I [t5, t7]: Before S_2 is turned off, S_x is turned on again at t5. L_x and C_x start to resonate. After t6, I_x increases to I_{Load}, and the current in S_2 is reduced to zero. As I_x keeps increasing, the surplus current flows through diode D_2. S_2 is turned off at the zero-current condition.
- Turn-off Transition II [t7, t8]: At t7, I_x falls to I_{Load}, and D_2 stops conducting. Since D_1 is still reverse-biased, I_{Load} can flow only through the resonant tank, charging C_x linearly.
- Turn-off Transition III [t8, t10]: At t8, C_x is charged to V_{dc}, and D_1 starts to conduct. The resonant tank begins to resonate again. As I_x decreases toward zero, the current in D_1 increases gradually. At t9, I_x returns to zero and reverses its direction, D_x starts to conduct, and S_x is turned off at the zero-current condition. The gate-driver signal for the top main switch S_1 can be applied after t8.

- Diode-On Stage [after t10]. When Ix drops to zero at t10, the auxiliary circuit stops resonating. I_{Load} is conducted by D1, and the inverter resumes PWM operation.

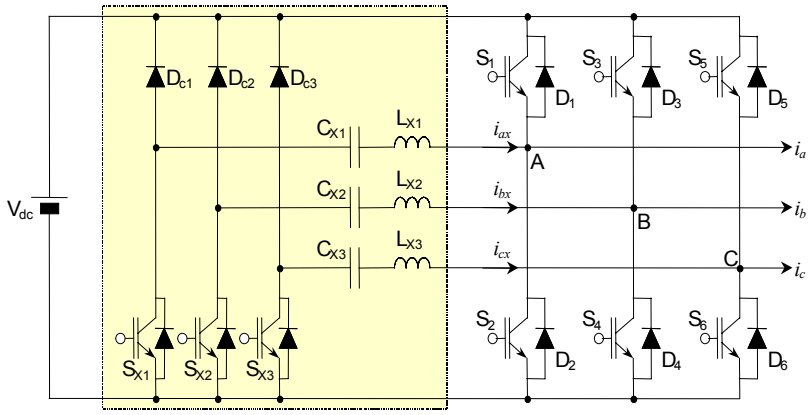


Fig. 2.8. The three-switch ZCT inverter.

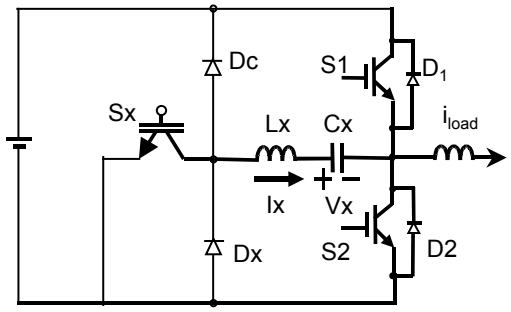


Fig. 2.9. One phase leg of the three-switch ZCT inverter.

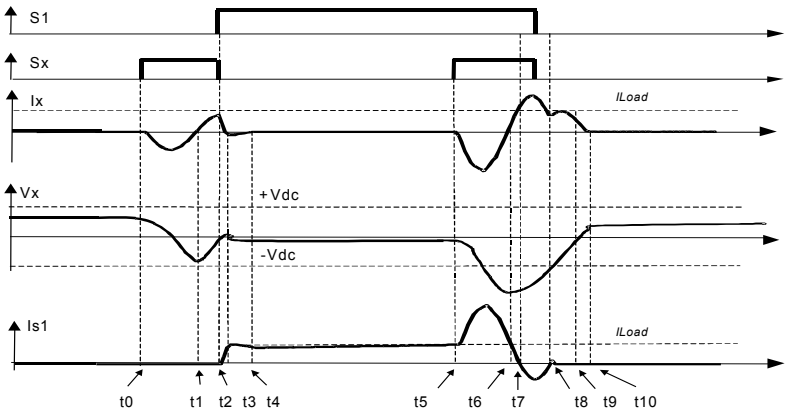


Fig. 2.10. Operation waveforms when $I_{Load}>0$.

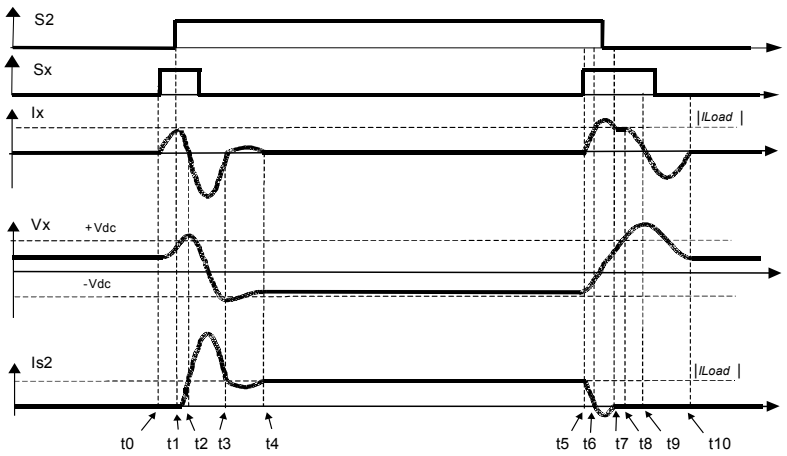


Fig. 2.11. Operation waveforms when $I_{Load}<0$.

2.2.4.1. Design Considerations

To ensure zero-current turn-off for the main switches, the resonant current peak at the turn-off transition, I_{xpk}, must be larger than the maximum load current subjected to the zero-current turn-off, I_{max}. Similar to the case of six-switch ZCT inverter, the magnitude of the resonant current peaks can be approximated as V_{dc}/Z_o. Thus, the requirements for the resonant tank for both cases are the same. Another variable to be considered is the resonant time period T_o. T_o should allow the turn-off time to be long enough to ensure that the minority carrier in the device is recombined properly, but the turn-off time should not be too long or a large control delay would be created. The design equations for Lx and Cx are the same as those given in equations 2.2 and 2.3.

2.2.5. ZVT Inverter with a Single Switch

This topology is an AC-side ZVT inverter that requires a modified SVM scheme since the auxiliary branch can only realize the zero-voltage turn-on once per switching cycle. With only one auxiliary switch and three auxiliary inductors, the circuit is a low-cost soft-switching

solution. However, the auxiliary inductor charging current, which reaches to more than $\sqrt{3}$ times the required maximum phase current, can cause significant conduction loss in the auxiliary circuit, which results in extra turn-off losses and conduction losses in the main switches.

2.2.5.1. Design Considerations

A brief description of the operation principles is given as follows.

- Pre-charging stage [t0, t1]: At t0, the main switch S_1 turns off under hard-switching. Then D_2 starts to conduct, so the node voltage of phase A drops to the negative rail of DC.
- Charging stage [t1, t2]: After S_2, S_{X1} and S_{X2} turn on at t1, the auxiliary inductor currents i_{ax}, i_{bx} *and* i_{cx} start to increase linearly beyond the phase currents, and the currents in the three main diodes reduce. After the auxiliary inductor currents reach the level of the phase currents, the three main diodes turn off naturally and the overcharged currents start to flow through S_2, S_3, and S_5. The overcharged inductor currents are necessary to create the perfect zero-voltage condition.
- Resonant stage [t2, t3]: When S_2, S_3 and S_5 turn off at t2, the auxiliary inductors start to resonate with the node capacitance of nodes A, B and C. The node voltages resonate towards their opposite DC rails, with switch voltages reducing gradually to zero. Because the initial energy levels of the auxiliary inductors at the beginning of resonant stage are different from each other, different lengths of time are required for the voltages across the main switches S_1, S_4 and S_6 to reach zero. The auxiliary inductor of each phase starts to individually discharge the current after the switch voltages across S_1, S_4 and S_6 drop to zero.
- Discharging stage [t3, t4]: After the main switches S_1, S_4 and S_6 turn on with zero-voltage conditions at t3, the auxiliary inductor currents decrease to zero. Because the initial current

values of the discharging stage are different from each other, the auxiliary inductor current of the phase that has the smallest phase current among three phases, i_{cx}, reaches zero first. This inductor current flows to the opposite direction after it reaches zero. However, the other two auxiliary inductors L_A and L_B still carry some current when i_{cx} reaches zero.

- Resetting stage [t4, t5]: Because the initial current values of the resetting stage are different from each other, it is almost impossible for the three auxiliary inductor currents to reach zero at the same time, except when $i_b = i_c$. Therefore, when the auxiliary inductor current of the phase that has the largest main current among three phases, i_{ax}, reaches zero at t4, the auxiliary switch S_X turns off. Therefore, the auxiliary switch is not turned off at zero current. After the auxiliary switch S_X turns off, the auxiliary inductors restore the inductor energy to V_{dc} through D_{Xp} and D_{Xn}. When the auxiliary inductor currents reach zero, D_{Xp} and D_{Xn} turn off naturally.

At t5, the commutation is completed, and the auxiliary circuit stays inactive until the next switching cycle. For this circuit, the trade-off consideration similar to those of the ARCP and the ZVTCI exist.

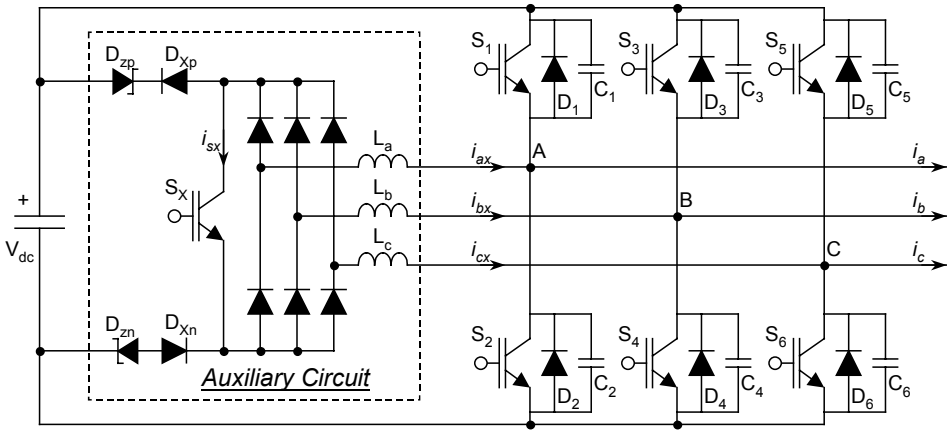


Fig. 2.12. The ZVT inverter with a single switch.

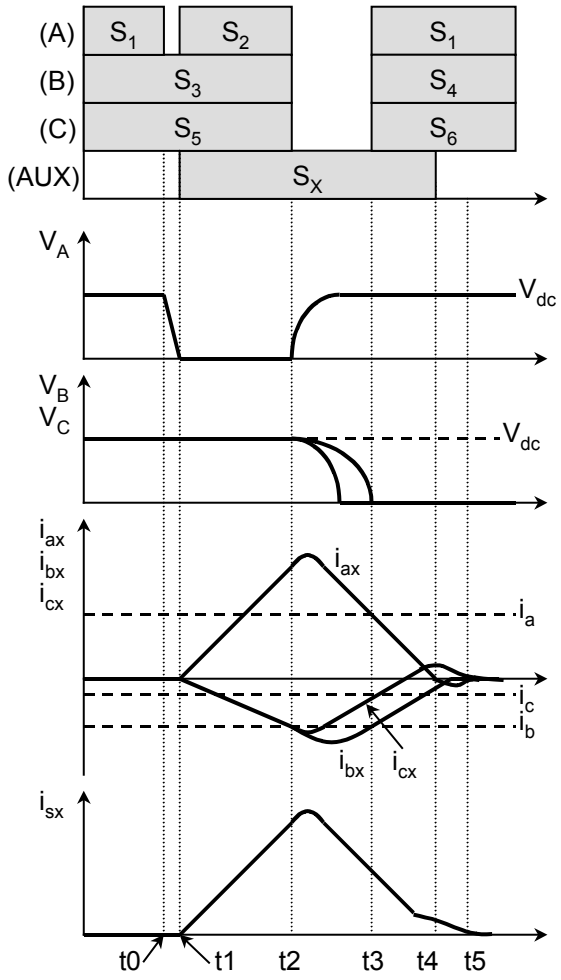


Fig. 2.13. Operation waveforms of ZVT inverter with a single switch.

2.2.6. ZVT Inverter with a Single Inductor

The inverter power circuit with this topology is shown in Fig. 2.14. The auxiliary circuit consists of only two switches S_{X1} and S_{X2}, one inductor L_X, an auxiliary diode bridge, two auxiliary inductor energy discharging diodes D_{X1} and D_{X2}, and two clamping diodes, D_{X3} and D_{X4}. Similar to ZVTSS, this ZVTSI also requires a modified SVM scheme since the turn-on of the three-phase legs needs to be switched simultaneously. Another potential problem is that the main

devices are switched under reduced voltage stress instead of ZVS. It is noted that two auxiliary switches are controlled with a same timing.

2.2.6.1. Principles of Operation

In order to explain the operations, assume the main circuit stage is from V7(*ppp*) to V1(*pnn*), $i_a>0$, $i_b<0$, and $i_c<0$. The switching timing charts and the key waveforms are shown in Fig. 2.15.

- Pre-charging stage [t0, t1]: At t0, the main switch S_1 turns off under hard-switching. Then D_2 starts to conduct, so the node voltage of phase A drops to the negative rail of DC.
- Charging stage [t1, t2]: Prior to the main switches, the auxiliary switches S_{X1} and S_{X2} turn on at t1. Then the auxiliary inductor current i_{LX} starts to increase linearly, and the currents in the three main diodes reduce.
- Resonant stage [t2, t3]: When the auxiliary inductor current i_{LX} reaches the phase A current i_a, the three main diodes turn off naturally and L_X starts to resonate with the node capacitances of node A, B, and C. The node voltages resonate towards their respective opposite DC rails, with switch voltages reducing gradually.
- Freewheeling stage [t3, t4]: When the node voltages reach $2/3$ of the DC voltage at t3, the auxiliary diode bridge is shorted and the resonance ends. The resonant current term in i_{LX} freewheels through S_{X1}, S_{X2} and the shorted auxiliary diode bridge. Therefore, every state keeps constant before the main switches turn on.
- Discharging stage [t4, t5]: After t2, all main diodes stop conducting. Also, the voltage across S_1 reduces to $\frac{V_{dc}}{3}$, and the voltages across both S_4 and S_6 reach to $\frac{2}{3}\cdot V_{dc}$. Therefore, the main

switches S_1, S_4 and S_6 can turn on with reduced voltages and without reverse recovery currents at t4. At the same time, the auxiliary switches S_{X1} and S_{X2} turn off, so L_X discharges by V_{dc} through D_{X1} and D_{X2}. When the auxiliary inductor current i_{LX} reaches zero at t5, D_{X1} and D_{X2} turn off naturally.

At t5, the commutation is completed, and the auxiliary circuit stays inactive until the next switching cycle. It is noted that these design considerations are similar to those of other ZVT inverters.

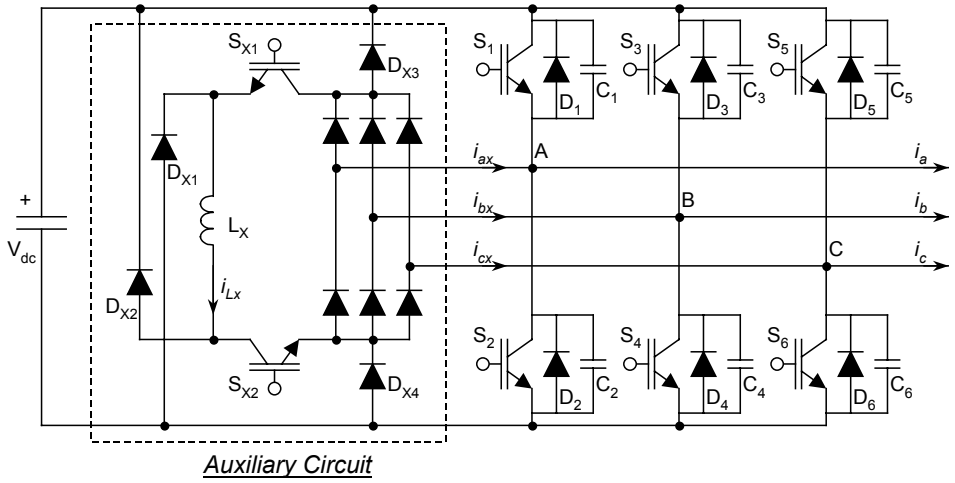


Fig. 2.14. The ZVT inverter with single inductor.

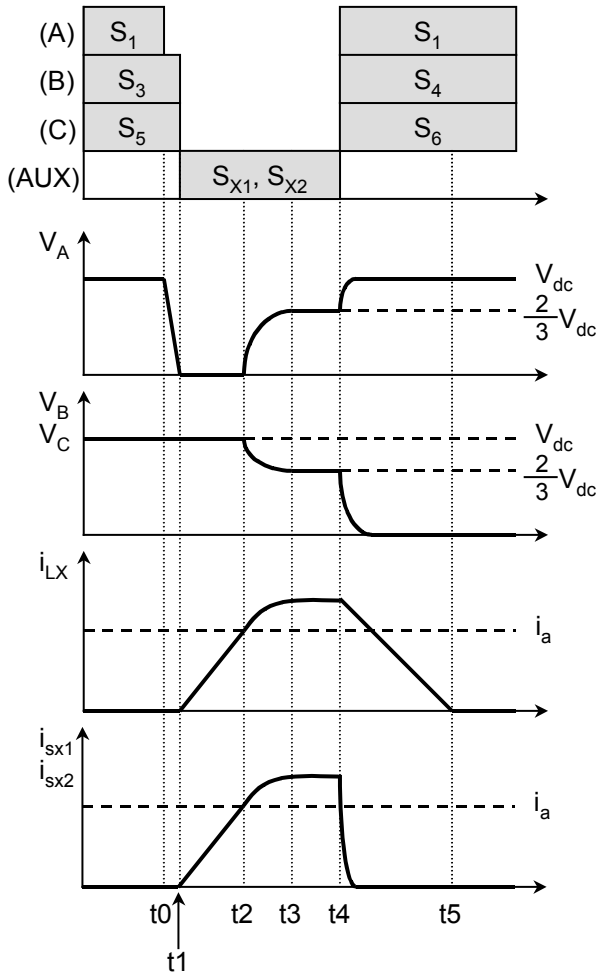


Fig. 2.15. Operation principle of zero-voltage turn-on.

2.3. Inverter Loss Modeling and Analysis

There are two main types of methods for calculating the losses of three-phase inverters. One uses the delicate simulation circuit to directly integrate the product of the device voltage and the current [C5]. This method should have a good accuracy if an accurate device model can be obtained. However, quite often the device model with enough precision is difficult to obtain. Besides, the simulation-based approach may be excessively time-consuming and will not quickly generate the loss data for comparison purpose. Another method is to experimentally characterize

the conduction losses and switching losses. Then the curve-fitted device-loss model is obtained and applied to the inverter loss calculation [C1]. The second approach is chosen for the efficiency and loss evaluation in order to identify the candidate soft-switching inverters with high-efficiency capability [C2]-[C4]. According to the inverter specifications and design guidelines presented previously [C7]-[C11], the soft-switching inverter design parameters are obtained as follows.

The ARCP inverter, L_x=1 μH, C_s=0.22 μF

The six-switch ZCT inverter, L_x=0.6 μH, C_x= 1 μF

The three-switch ZCT inverter, L_x=0.86 μH, C_x= 0.625 μF

The ZVT inverter with coupled inductors, L_x=1.2 μH, C_s= 0.22 μF

The ZVT inverter with single switch, L_x=1.08 μH, C_s= 0.15 μF

The ZVT inverter with single inductor, L_x=1.6 μH, C_s=0.1 μF.

In order to evaluate the efficiency performance, the power devices need to be chosen for the three-phase inverter legs. The test circuit for measuring the switching loss is implemented, as shown in Fig. 2.16. The top switch S_1 is kept off and the double-pulse gate signal is applied to S_2 [C16]. By adjusting the width of the first pulse, the inductor current can be established at any pre-defined current level. Then the second gate pulse is used to switch the IGBT. Several commercial IGBT half-bridge modules have been tested [C18]. The switching loss data is summarized in Table 2-1, where hon is the ratio of the turn-on losses to the product of the switched voltage and current, and hoff is the ratio of the turn-off losses to the product of the switched voltage and current. Since the switching losses approximately are proportional to the switched voltage and current level, the sum of hon and hoff reflects the level of the switching

losses. Finally, the IGBT module, MG300J2YS50 from Toshiba, is selected due to lowest switching losses. The loss models for MG300J2YS50 are developed and explained in the following sections.

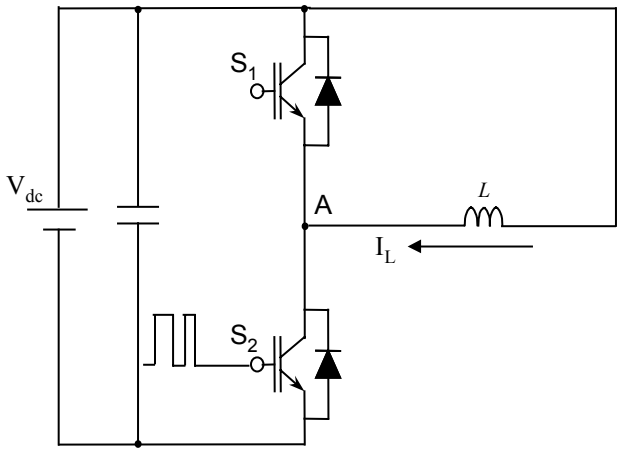


Fig. 2.16. Device switching loss test circuit configuration.

Table 2-1. Switching loss comparison of IGBT modules.

Device	Manufacturer	Package	hon (10^{-7}·J/V·A)	hoff (10^{-7}·J/V·A)
SKM400GB062 600 V, 400 A	Semikron	Half-bridge	1.91	3.08
PM300CVA060 600 V, 300 A	Powerex	Half-bridge	0.87	2.2
6MBP300RA060 600 V, 300 A	Fuji	Six-pack	1.11	1.93
MG300J2YS50 600 V, 300 A	Toshiba	Half-bridge	1.51	1.5

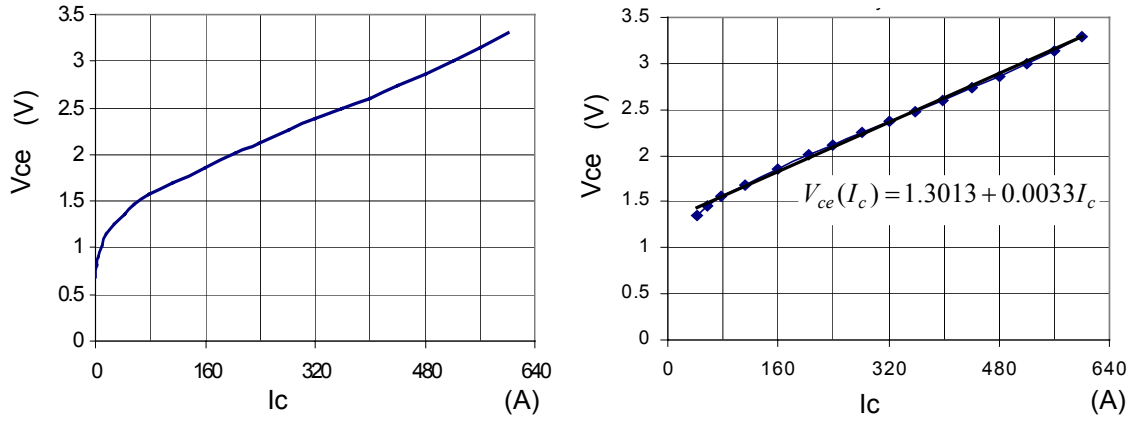
2.3.1. Device Conduction Loss Model

Since the IGBT data sheet from the manufacturer provides typical on-voltage drop information, a reasonable conduction loss model can be obtained via the curve-fitting method. IGBT physics implies that the on-state voltage is approximately the sum of the voltage drop in the conductivity modulation layer and the internal MOS channel resistive voltage drop.

Therefore, the simplified curve-fitting model, using a constant voltage source and the resistor, represents the conduction voltage drop of both the IGBT and the anti-parallel diode.

Fig. 2.17 shows that the linear representation of conduction voltage drop makes a good approximation except at low current levels. For the purpose of calculating losses at heavy loads, such a linear model is able to produce accurate results. Similarly, the anti-parallel diode model is shown in Fig. 2.18.

The auxiliary devices of soft-switching inverters actually only handle the small ROMS and average current. Due to the nature of the relatively high peak current pulse, the selection of the auxiliary devices mainly focuses on the peak current-handling capability. A 600V 100A IGBT, IRG4ZU70UD, is chosen as the auxiliary devices for the soft-switching inverters. Its conduction loss model can also be easily obtained.



(a) (b)

Fig. 2.17. Conduction voltage-drop of MG300J2YS50 (Tic=25 °o): (a) data sheet and (b) curve-fitting model.

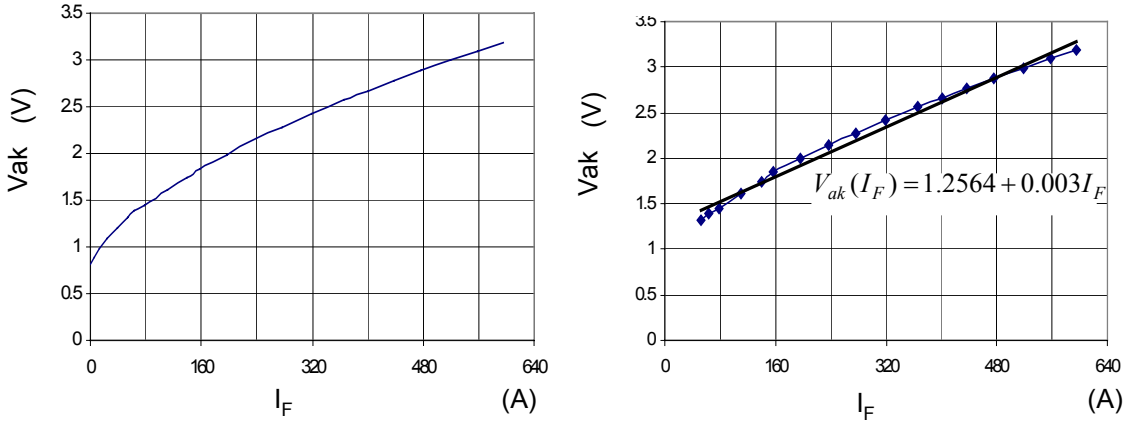


Fig. 2.18. Conduction voltage-drop of the anti-parallel diode of MG300J2YS50: (a) data sheet and (b) curve-fitting model.

So in general, the conduction loss model for IGBT and diode in both the main and the auxiliary circuits are expressed by equations 2.4 and 2.5, respectively:

$$V_{ce}(i) = V_t + i \cdot R_{ce}, \text{ and} \tag{2.4}$$

$$V_{ak}(i) = V_f + i \cdot R_{ak}. \tag{2.5}$$

Regarding the conduction losses in the resonant inductor, the core loss is found to be dominant in the total inductor losses. The winding loss is quite small considering tens of kHz operation and the small RMS current value. Since there is no well-established simple formula for calculating the core losses of the inductor with non-sinusoidal current pulses, one inductor is actually designed for the ARCP inverter. Three MPP cores of 55551 from Magnetics are stacked together, and three turns of AWG#14 wires are assembled to obtain a 1μH inductor with the peak current capability of about 300 A. If under the sinusoidal flux excitation, the core loss density is $W_{core} = 0.161 \cdot f_s^{1.31} \cdot (B_{max} \cdot 0.5)^{2.21}$. One core of 55551 is 0.161 lb, therefore, the worst-case core loss, assuming the core is magnetizing from zero to B_{max} every switching cycle, at 10 kHz is 23

W. In reality, the auxiliary circuit does not operate for almost 1/3 of the line cycle due to the use of six-step SVM and the fact that the inductor current is adjusting according to the load current level, the actual core loss will be much smaller than 23 W. Unless the performance difference is affected by the inductor loss, the inductor losses will be ignored in the loss and efficiency comparison.

2.3.2. Device Switching Loss Model

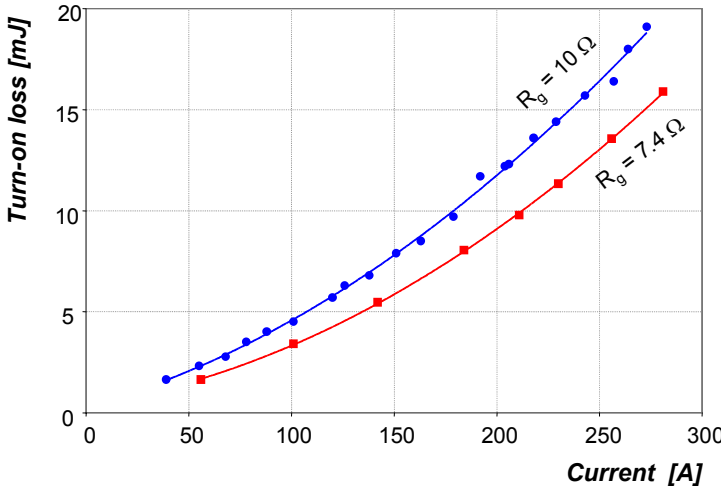
As described previously, the double-pulse circuit tester was developed to conduct the switching loss test [C12]. The experimentally characterized hard-switching losses are shown in Fig. 2.19. As shown in Fig. 2.19, for these third generation devices, MG300J2YS50, the turn-on losses are slightly more than the turn-off losses. Actually, the IGBT technology innovation in recent years has mainly focused on the reduction of the turn-off loss and the further reduction of the conduction losses. It is worthwhile to point out that the second-generation device, for example MG300J2YS45 from Toshiba, may be more suitable for the soft-switching inverter since its conduction losses are less dominant. While the conduction loss and the switching losses are still similar among the second and third generations, the third generation device has achieved more than 50% turn-off loss reduction as compared with the second-generation devices.

The turn-off process of the ZVT inverter and the turn-on transition of the ZCT inverter are not ideal soft-switching operations, and thus incur some losses. To account for these losses, the one-leg soft-switching tester circuits of ARCP converter and ZCT converter were built and used to establish these switching conditions. The experimental waveforms are shown in Fig. 2.20 and Fig. 2.21. As shown in Fig. 2.20, during the snubbered turn-off, the overlap between the device voltage and current is reduced due to the slowed voltage-rising rate caused by the snubber

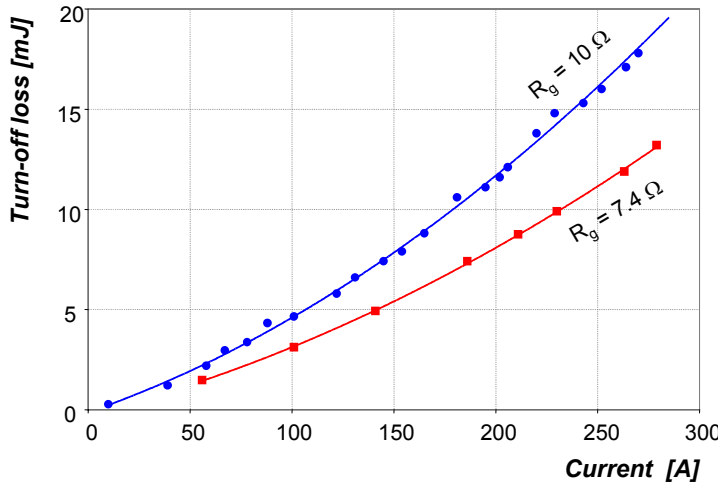
capacitor. Therefore, the turn-off losses are largely reduced by the snubber capacitor. A negative effect during the snubbered turn-off is the ringing that appears on the device voltage. This ringing is mainly due to the resonance between the commutation inductance and the snubber capacitor. Packaging efforts for reducing the parasitic inductances can alleviate this ringing. Since the ringing frequency is usually below a few MHz, the EMI filter is expected to attenuate the ringing-related EMI noise.

The three-switch ZCT inverter can not exactly control the time instant at which the resonant tank current starts to rise during the turn-on transition. Consequently, there is a lossy overlap between the device voltage and the current. For the six-switch ZCT inverter, the turn-on losses can be maintained much smaller than three-switch ZCT since the device current rising can be somewhat controlled via the resonant tank. The corresponding turn-on waveforms of the ZCT are shown in Fig. 2.21.

Therefore, based on the measured switching loss data under soft-switching operation, the switching loss model for the main switches in the ZVT or ZCT inverter can be obtained using the curve-fitting technique. It is noted that the snubbered turn-off losses are also related to the snubber capacitance value. So the correlation between the turn-off losses and the snubber capacitance is experimentally characterized, as shown in Fig. 2.22. The overall switching loss comparison at different load current levels is illustrated in Fig. 2.23. It is noted that the ZCT inverter almost eliminates the turn-off losses of the main devices, and the ZVT inverter actually removes the turn-on losses.

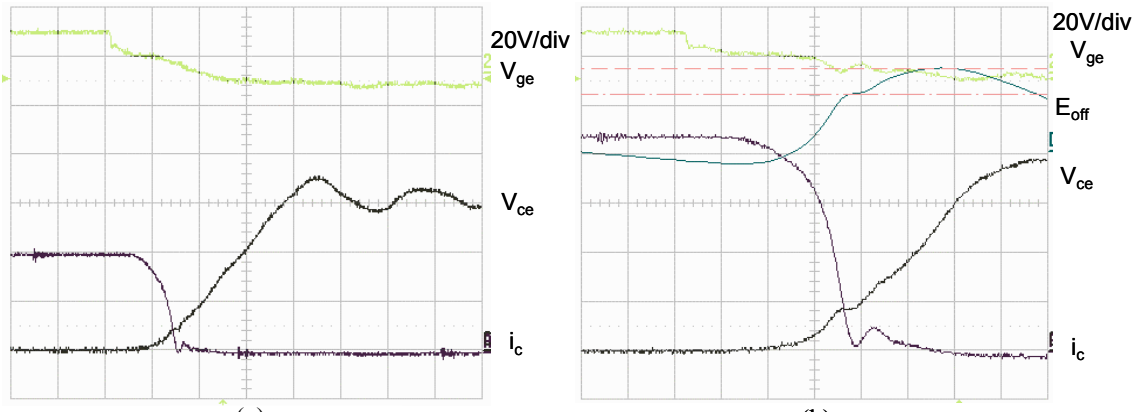


(a)



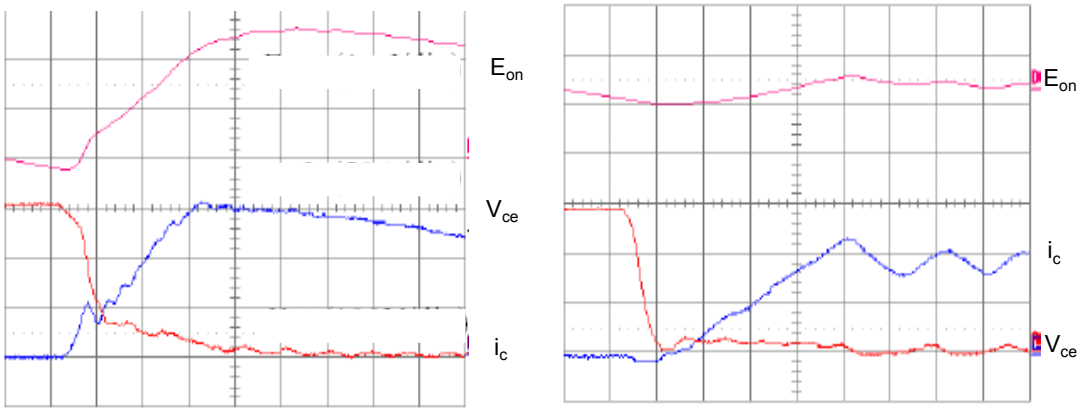
(b)

Fig. 2.19. Switching losses of MG3000J2YS50: (a) turn-on loss and (b) turn-off loss.



(a) (b)

Fig. 2.20. Turn-off waveform with snubber capacitor: (a) 100A turn-off and (b) 220A turn-off (100V/div, 50A/div, 1mJ/div, 0.5μS/div).



(a) 3-switch ZCT (b) 6-switch ZCT

Fig. 2.21. Turn-on waveform in the ZCT inverter: (a) three-switch ZCT and (b) six-switch ZCT (50A/div, 100V/div, 1mJ/div, 0.2μS/div).

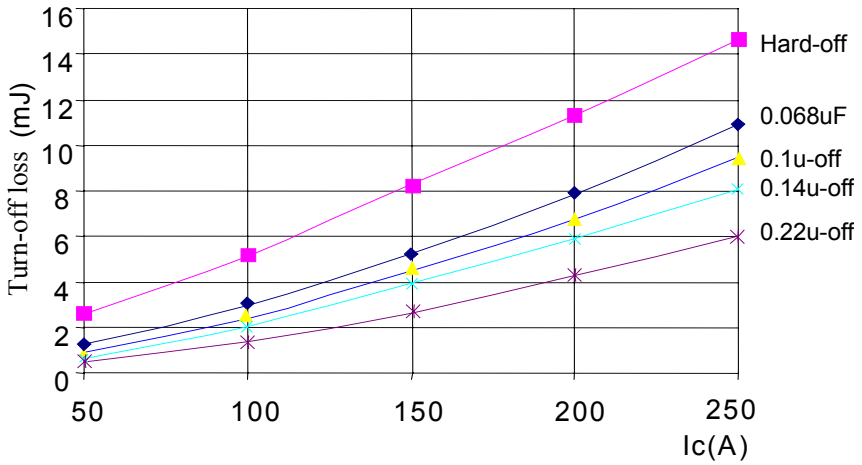


Fig. 2.22. Turn-off loss with hard-switching and the snubber capacitor.

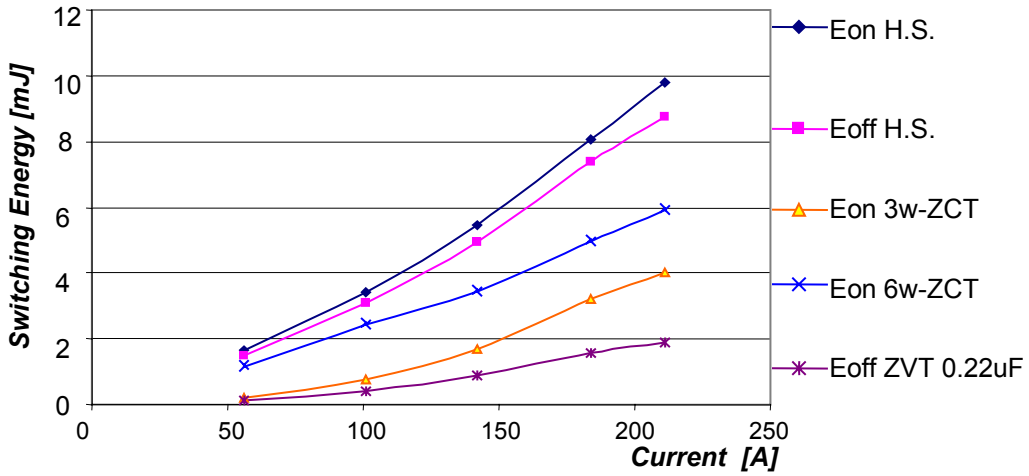


Fig. 2.23. Comparison of hard-switching and soft-switching losses.

It is observed that the switching losses are nearly linear to the switched current. Therefore, the turn-on and turn-off loss models can be expressed by:

$$E_{on}(i) = k_{on} i, \text{ and} \tag{2.6}$$

$$E_{off}(i) = k_{off} i. \tag{2.7}$$

The loss coefficient for the soft-switching inverter will be much smaller than that of the hard-switching inverter. For MG300J2YS50 under the hard-switching condition, when the gate resistor is 7.4 ohm, k_{on}=0.049 mJ/A, and k_{off}=0.043 mJ/A. For the ZVT converter, k_{on}=0.0025

mJ/A, and k_{off}=0.009 mJ/A. For the six-switch ZCT inverter, k_{on}=0.018 mJ/A, and k_{off}=0.002 mJ/A. For the three-switch ZCT inverter, k_{on}=0.025 mJ/A, and k_{off}=0.002 mJ/A.

2.3.3. Loss Calculation for Inverter Operation

The difference in conduction loss between the SVM and the SPWM is only marginal if the same fundamental output voltage is generated. Therefore, the expression that is valid for the SPWM can be used with enough accuracy to also evaluate the conduction loss. Equations 2.8 and 2.9 calculate the conduction loss for one IGBT and its anti-parallel diode, respectively:

$$P_{cs\_main}=\frac{1}{2}I_pV_t(\frac{1}{\pi}+\frac{m}{4}\cos\varphi)+I^2_pR_{ce}(\frac{1}{8}+\frac{m}{3\pi}\cos\varphi), \text{ and} \quad (2.8)$$

$$P_{cd\_main}=\frac{1}{2}I_pV_f(\frac{1}{\pi}-\frac{m}{4}\cos\varphi)+I^2_pR_{ak}(\frac{1}{8}-\frac{m}{3\pi}\cos\varphi). \quad (2.9)$$

where m is the modulation index, I_p is the peak of the load current, and cosφ is the power factor. The total conduction loss of the hard-switching inverter is given by $P_{c\_main\_had}=6(P_{cs\_main}+P_{cd\_main})$.

Since Equations 2.6 and 2.7 suggest that the switching energy loss is proportional to the switched current, then averaging the switched phase current with the fundamental cycle will get the switching loss for one phase. To reduce the number of switching actions, the six-step SVM control (also called two-phase modulation) is usually applied. Under the six-step SVM control, only two phase-legs' devices have the switching actions in each switching cycle. The duty cycle under a six-step SVM scheme is shown in Fig. 2.24 with a modulation index of 0.5. The synthesized AC voltage of phase A and the corresponding load current with a power factor of 0.866 are also shown. Since the nominal operating points of the motor usually have a power factor higher than 0.866 (power factor angle of less than 30 degree), the six-step SVM can

always achieve no switching actions for the maximum phase current. Therefore, the average value of the switched phase current and switching loss can be found in Equations 2.10, 2.11, and 2.12:

$$I_{a\_sm\_hard} = I_p / \pi , \tag{2.10}$$

$$P_{on\_ph} = E_{on} f_s = k_{on} I_{a\_sm\_hard} f_s , \quad \text{and} \tag{2.11}$$

$$P_{off\_ph} = E_{off} f_s = k_{off} I_{a\_am\_hard} f_s , \tag{2.12}$$

where f_s is switching frequency. The total switching loss is found by $P_{s\_main\_hard} = 3(P_{on\_ph} + P_{off\_ph})$.

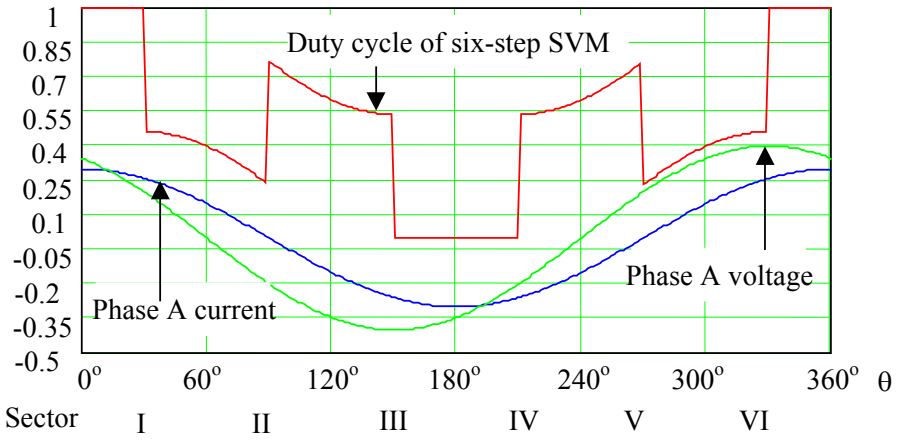


Fig. 2.24. Six-step SVM allows no switching for the maximum phase current.

For the soft-switching inverter's loss calculation, the detailed waveforms need to be analyzed to derive the switched current and the average and RMS currents in the auxiliary circuit. The losses of main devices in the soft-switching inverters are calculated with similar way to that of the hard-switching inverter except k_{on} and k_{off} should be updated. Numerical equations are used to calculate the switching losses and the conduction losses in the auxiliary circuit. The derivation of the auxiliary circuit current is illustrated in Fig. 2.25 for ZVT inverters. In most ZVT inverters

including ARCP, $V_x=V_{dc}/2$. Since the goal is to derive the expressions of the auxiliary circuit current for the purpose of calculating the conduction loss, the zero time instant is assigned at the beginning of the current rising. In period [0, t2], the auxiliary inductor is linearly charged and the current is given as follows.

$$i_x(t) = \frac{V_x \cdot t}{L_x}, \qquad 0<t<t2, \tag{2.13}$$

where $t2 = \frac{L_x(i_{Load} + i_{boost})}{V_x}$. i_{boost} is the specified current level and usually is set to be small, for example 20 A. In period [t2, t3], the resonance among the auxiliary inductor L_x and the snubber capacitor C_x starts and the voltage of S_1 decreases toward zero. The expression of i_x is obtained as follows.

$$i_x(t) = i_{Load} + i_{boost}\cos\omega_r(t-t2) + \frac{V_x}{Z}\sin\omega_r(t-t2), \; t2<t<t3, \tag{2.14}$$

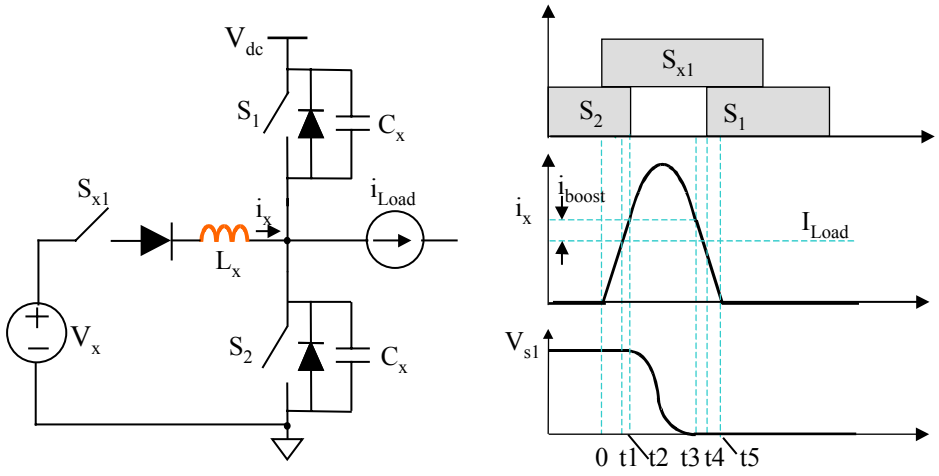
where Z is the characteristics impedance of the resonant circuit, $Z = \sqrt{L_x/2C_x}$, ω_r is the resonant angular frequency, $\omega_r = 1/\sqrt{2L_xC_x}$, and $t3 = t2 + \text{asin}(V_x/\sqrt{V_x^2 + i_{boost}^2}) \cdot 1/\omega_r$.

After V_{s1} reach zero at t3, it stays at zero until S_1 is gated on since the anti-parallel diode of S_1 conducts current. Therefore, in period [t3, t5], L_x is linearly discharged and i_x decreases to zero. Since ix is ideally equal to the sum of i_{Load} and i_{boost} at t3, i_x can be expressed in the following.

$$i_x(t) = i_{Load} + i_{boost} - \frac{V_x}{L_x}(t-t3), \qquad t3<t<t5, \tag{2.15}$$

where $t5 \approx t3 + t2$. Therefore, the complete expressions of the auxiliary circuit current during ZVS transition is derived. The similar way can be applied to ZCT inverter. Since it is a quite

tedious process to derive the auxiliary circuit current for the soft-switching inverters, it will not be explained in detail for each soft-switching inverter. The details can be referred to [C19].



(a) (b)

Fig. 2.25. Illustration of auxiliary circuit current: (a) Equivalent circuit during ZVS and (b) Key waveforms.

2.4. Comparison of Different Soft-switching Inverters

Considering the general inverter specifications for EV applications, the input DC voltage is selected as 324 V. The load conditions are specified as follows: I_{rms}=200 A, M=0.8, and cosϕ=0.86. The switching frequency fs is selected as 10 kHz and 20 kHz. Fig. 2.26 shows the efficiency compared with the hard-switching inverter. It can be seen that the ZVTSS and the ZVTSI show the lowest efficiency and are inefficient compared to the hard-switching inverter. The detailed loss breakdown is shown in Fig. 2.27. There is a tremendous increase in the turn-off losses of the main devices in these two inverters. The modified SVM control schemes for these converters result in one more turn-off transition in every switching cycle. The other reason is that the ZVTSS and ZVTSI cannot utilize the large snubber capacitor to effectively reduce turn-off loss. As mentioned earlier, the commutation from switch to diode requires the activation of the

auxiliary circuit when the load current is small. Due to topology limitations, it is difficult for the ZVTSS or the ZVTSI to activate their auxiliary circuits for this purpose. Therefore, to be turned on, the device is subjected to the large capacitive discharging current that occurs with a large snubber capacitor. It is also noteworthy that the non-zero-current switching of the auxiliary devices incurs large turn-off losses in both the ZVTSS and the ZVTSI.

Fig. 2.28 furthers reveals the importance of the variable pre-charging time control in the ZVT inverters in the case of 20 kHz. If for the simplicity of the auxiliary switch control the pre-charging time is fixed, the penalty is huge, which causes greater switching losses in the main switches and also more conduction losses in the auxiliary circuit.

Capable of simultaneously reducing turn-on and turn-off losses, the ARCP inverter, the two ZCT inverters, and the ZVTCI show better performance than that is affected by the hard-switching inverter. The overall comparison of soft-switching inverters is summarized in Table 2-1. From the component-count standpoint, the ZVTSS and ZVTSI belong to the low-cost soft-switching inverter type since they only uses one or two auxiliary switches. However, these two inverters are not suitable for EV applications due to inferior efficiency performance as compared with the hard-switching inverter. The ARCP inverter and the ZVTCI both provide greater efficiency. It is relatively difficult to decide which one should be chosen. The ARCP inverter is more popular than the ZVTCI and allows a low voltage rating for the auxiliary device, which might save some cost. Regarding the auxiliary diode count, the ZVTCI needs additional 3 pairs of half-bridge diodes as compared with the ARCP. This slightly increases the cost. On the other hand, the coupled winding and the additional resonant inductors in the ZVTCI may create the issues for the practical implementation. The reason is that the coupled inductor's volt-second

balance is realized over the fundamental line cycle, which potentially increase the size of the coupled inductors. It is noted that the coupled inductor brings a benefit that the current stress of the auxiliary diode in ZVTCI is reduced to half as compared with ARCP. From the loss standpoint, the ARCP and the ZVTCI should offer a similar level of performance. Due to the low-voltage switching of the auxiliary switches, the ARCP inverter may gain the edge in EMI performance. The six-switch ZCT inverter gains better loss reduction than the 3-switch ZCT due to its better control timing for the turn-on transition and its control of circulating energy. Overall, except ZVTSI and ZVTSS, the other four soft-switching inverters can apply any existing SVM schemes to optimize the performance. For example, six-step SVM can be used to reduce the number of switching actions and thus further reduce the switching losses.

For the evaluated EV ratings, the efficiency gain itself may not be so important since the hard-switching inverter can achieve a good level of efficiency, 96.75% at 20 kHz. But the loss reduction percentage plays a more important role since the loss reduction extent determines the possible thermal management. For the evaluated cases, the loss reduction is about 14% at 20 kHz. The reason for the small percentage is that the third-generation device we chose has dominant conduction losses. Actually if the second-generation devices are used, for example the MG300J2YS45, the loss reduction can be about 25%. So it is clear that device technology affects the performance of the soft-switching inverters [C13]. For the state-of-art devices, depending on the power inverter ratings and the power stage design, whether the soft-switching inverter will show the greater benefit remains a question.

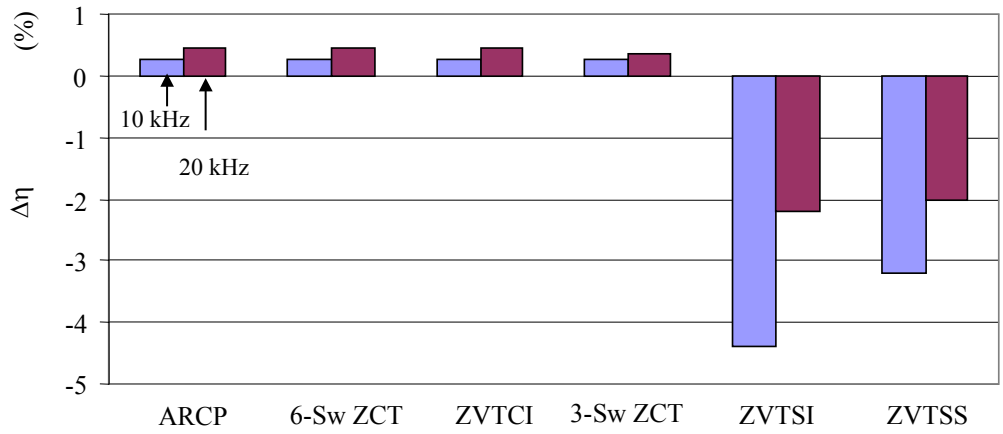


Fig. 2.26. Efficiency improvement comparison.

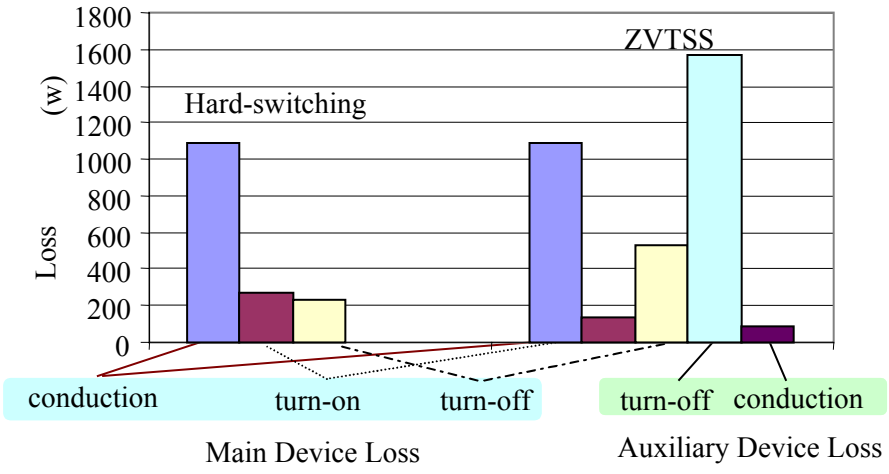


Fig. 2.27. Loss breakdown comparison of hard-switching and ZVTSS inverters.

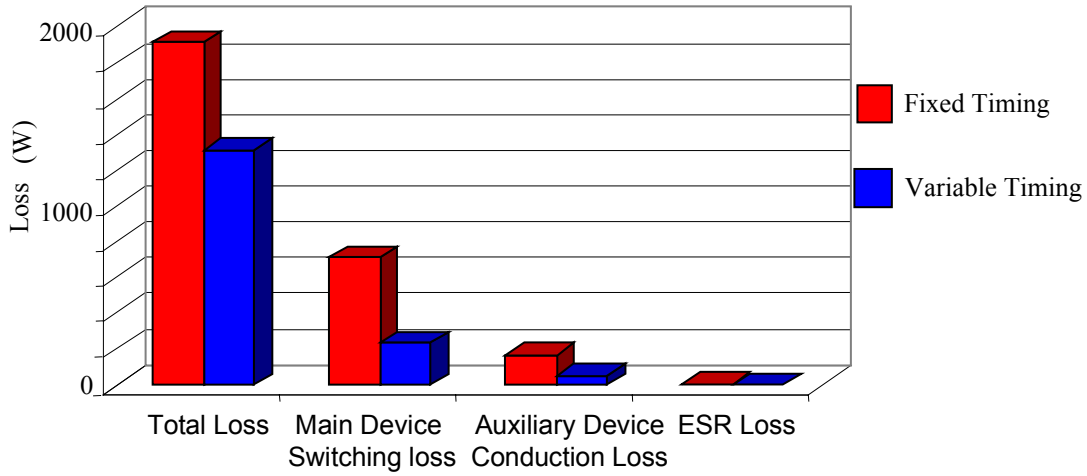


Fig. 2.28. Loss reduction comparison between fixed and variable timing control.

Table 2-2. Overall comparison of the soft-switching inverters.

		ARCP	6-Sw. ZCT	ZVTCI	3-Sw. ZCT	ZVTSI	ZVTSS
η (%)	fs=10kHz	97.57	97.5	97.5	97.5	95.5	96.4
	fs=20kHz	97.4	97.2	97.2	97.1	93	94.9
Num. of Auxiliary Switches		6	6	6	3	2	1
Num of Auxiliary Diode		6	6	6+6	6	10	10
Peak Current Stress of Auxiliary Inductor		314	418	157	277	585	394
Value of Auxiliary Passive Components		Lx=1 uH Cx=0.22 uF	Lx=0.6 uH Cx=1 uF	Lx=1.2 uH Cx=0.22 uF	Lx=0.86 uH Cx=0.63 uF	Lx=1.08uH Cx=0.15 uF	Lx=1.6 uH Cx=0.1 uF
PWM		Optimal SVM	Optimal SVM	Optimal SVM	Optimal SVM	Modified SVM	Modified SVM

2.5. Summary

In this chapter, the typical AC-side soft-switching inverters are analyzed to understand the soft-switching mechanism. Then the device loss models are developed through extensive device testing under the hard-switching and soft-switching conditions. The realistic loss reduction gained by soft-switching operation is identified. Based on the device loss models, the inverter loss calculation is conducted for a specified EV rating design. The efficiency and loss

comparison among the various soft-switching inverters and the hard-switching inverter leads to four important observations. First, some soft-switching inverters do indeed have greater losses than the hard-switching inverter. The reason is the existence of some extra hard-switching actions and some design constraints for limiting the loss reduction, for example, the limitation of the snubber capacitors. Second, the control timing plays an important role in the performance of the soft-switching inverter. Actually, varying the timing control according to the load current information is desired for both ZVT and ZCT inverters. This is a unique feature for the inverter operation since the load current varies over the fundamental output cycle. Without carefully controlling the auxiliary circuit's operation, it is possible that a much worse efficiency could result. Therefore, the soft-switching control needs to be carefully designed. Third, the device technology, especially the trade-off between the on-voltage drop and the switching loss, together with the application specification, plays an important role in the effectiveness of the soft-switching inverters. Finally, the loss reduction percentage is a major motivation for applying soft-switching inverters since the hard-switching inverters already achieves efficiency levels that are quite high. However, even with the 96-97% efficiency for the studied case, the total semiconductor losses reach about 1500 W, which will impose a challenge for thermal management [C14]-[C16].

Through the analytical efficiency evaluation, we select the ARCP, the six-switch ZCT inverter and the three-switch ZCT inverter for hardware development. The continuous output power is designed to be 50 kW, which is similar to GM EV-1. One hard-switching inverter and the three soft-switching inverters will be designed and operated at the dynamometer. In the next

chapter, the design, implementation of these soft-switching inverters and the comprehensive experimental evaluations will be presented.

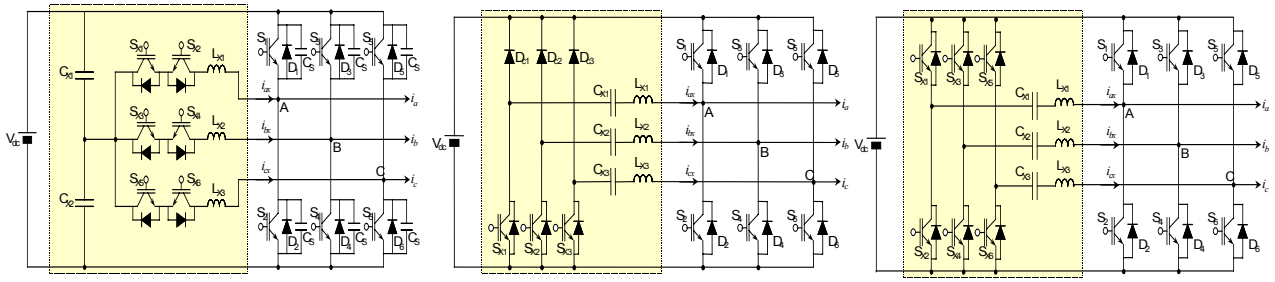
Chapter 3. Design, Implementation and Evaluation of Soft-switching Inverters for 55kW EVs

3.1. Introduction

This chapter will first present the design and development of the three soft-switching inverters for the small duty EV application: the ARCP inverter, the six-switch ZCT inverter and the three-switch ZCT inverter. These inverters, as shown in Fig. 3.1, are chosen based on the study presented in Chapter 2. In fact, the inverters are designed to be mounted onto the chassis of the EV-1 made by General Motors. The maximum continuous output power is 55 kW and the nominal bus voltage is 324 V. Therefore, the inverters are designed to emulate the operating conditions of EV-1's original hard-switching inverter. As discussed in the last chapter, the control timing is important for the soft-switching inverter's performance. Therefore, besides the power stage implementation, both a variable timing control structure suitable for all these converters and the necessary open loop control software need to be developed, and these results are also reported in this chapter. Then, extensive tests on the dynamometer are carried out to collect the performance data, such as the efficiency and the EMI noise at different operating points, corresponding to the operating range of the real vehicle.

Although some published research projects have evaluated the soft-switching inverter's performance in the EV, most use either crude analysis or simulation tools. There have been no experimental verifications at the full operating range of an EV application. The comparisons made between the soft-switched and hard-switched inverters, as reported in previous literature,

was based on analytical evaluations of the inverters' performance and were supported by simulation results only. The experimental comparisons normally do not include comprehensive evaluations of the whole converter over its entire operating range. The evaluation results presented in this chapter will serve as the first-ever comprehensive experimental evaluation for the soft-switching inverters in EVs.



(a) (b) (c)

Fig. 3.1. Selected soft-switching topologies: (a) ARCP, (b) Three-switch ZCT and (c) Six-switch ZCT.

3.2. Design and Development of Three Soft-switching Inverters

The 600V 300A IGBT, MG300J2YS50, is selected as the main power devices for all the soft-switching inverters because it fulfills the power-rating requirement. This device is a third-generation IGBT half-bridge module from Toshiba, first introduced in late 1997. It is intended to replace the second-generation IGBT, MG300J2YS45. The design of each soft-switching inverter involves determining the resonant component values and their implementation, the selection of the auxiliary power devices, and the soft-switching control pattern.

3.2.1. Design and Implementation of the ARCP Inverter

The high ratio between the peak and RMS values of the resonant current and the zero-current switching behavior at both turn-on and turn-off make thyristors ideal auxiliary devices. However,

even fast thyristors are not fast enough for the 10kHz to 20kHz inverter operations. MOS-controlled-thyristors (MCTs) are not yet mature enough for medium-voltage and -current applications. Since the voltage rating of the auxiliary device is about half of the DC input voltage, MOSFETs can also be considered as candidates. Unfortunately, with from 200V to 400V ratings, commercial MOSFETs have unacceptably high on-resistance, which results in much higher conduction losses as compared to IGBT devices. Among the present commercial devices, the modern IGBT seems the best suited to be used as the auxiliary devices for the specified inverter ratings.

Theoretically, IGBTs with 300V or 400V ratings should be reasonable for the auxiliary devices since they only need to block half of the DC voltage in the ARCP inverter. On the other hand, the RMS value of the resonant current is about one-fourth of the load current at the highest switching frequency, which means about 50 A for the targeted specification. The peak current of the auxiliary devices equals the sum of the maximum load current and resonant peak current. Since the resonant peak current is determined only by half the DC voltage and the resonant tank impedance, $\sqrt{L/2C}$, it is generally designed at less than 100 A. Consequently, the auxiliary devices need to handle about 50A RMS current and 400A peak current. Among the commercial IGBTs with 300V or 400V ratings, almost no available devices satisfy such current requirements. This implies that the benefit of low voltage ratings for the auxiliary devices in the ARCP inverter could not be fully utilized for the low bus voltage design. Finally, the IGBT IRG4ZC70UD with surface-mounted packaging from International Rectifiers is selected as the auxiliary device. Fig. 3.2 shows the implementation of two IRG4ZC70UDs using an insulated

metal substrate (IMS) board. The IMS board uses alumina (Al_2O_3) instead of ceramics as the substrate material, which is a low-cost solution for thermal management.

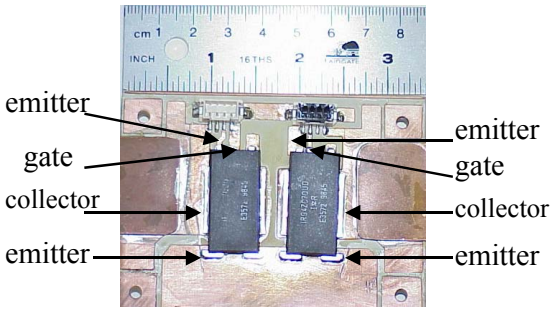


Fig. 3.2. Implementation of auxiliary devices in the ARCP inverter.

Following the formulated design procedures, as explained in Chapter 2, the resonant inductance and snubber capacitance is finally selected as L=1 μH and C=0.22 μF. The resulting resonant frequency is 219 kHz. The RMS value of the resonant inductor current is calculated to be about one-fourth of the load current. The final designed inductor uses five 55551 MPP cores and stacks them together. The MPP cores from Magnetics Company have distributed air gaps for storing high energy. Four AWG-14 copper wires with zinc-insulated outer layers are paralleled to form the inductor winding. The number of turns is three.

When the resonant inductor current is linearly discharged to zero, the current of one auxiliary diode reaches zero. After that, the auxiliary diode needs to block half of the DC voltage. The diode reverse recovery current will flow in the auxiliary circuit and help to build the necessary voltage potential in the diode. This is commonly known as the diode reverse recovery phenomenon. The typical waveform describing the diode reverse recovery phenomenon is shown in Fig. 3.3. Before t3, the diode current decreases linearly. After the diode current reaches zero, it continues to build up at the same rate due to the diode's reverse recovery. Until t3, the diode

starts to block the reverse voltage. The reverse recovery current starts to. It should be mentioned that the peak reverse recovery current is related to the forward conduction current level and the decreasing rate during diode turn-off. Usually the parasitic inductor is in the reverse recovery current path in power converters. The resonance between the parasitic inductor and the diode junction capacitor will have caused severe ringing and the voltage spike if not properly clamped. In the auxiliary branch of the ARCP inverter, as shown in Fig. 3.1, the tremendous voltage spike across the auxiliary device (diode) happens since there is no automatic voltage clamping mechanism for the auxiliary devices. Experimental waveforms verify the concern of the voltage spike, as shown in Fig. 3.4. The voltage spike is overwhelmingly high and the ringing is severe. The ringing is due to the resonance between the resonant inductor and junction capacitor of the auxiliary device.

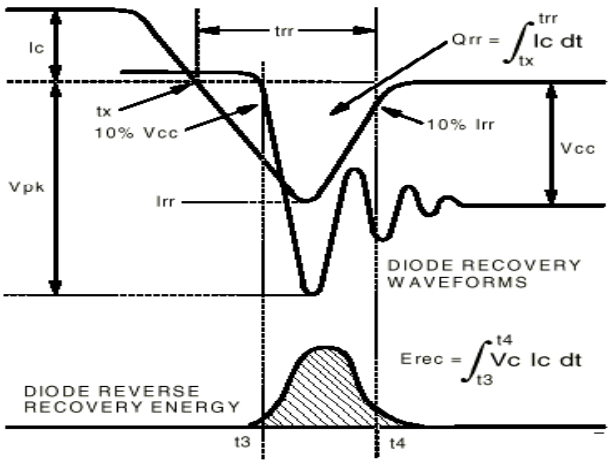


Fig. 3.3. Diode reverse recovery characteristics (from data book of IRG4ZC70UD).

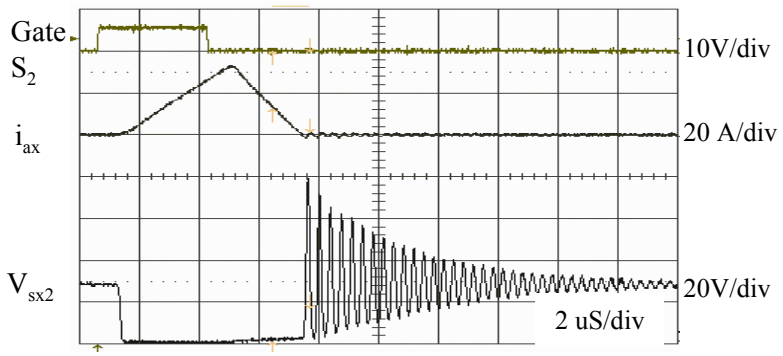
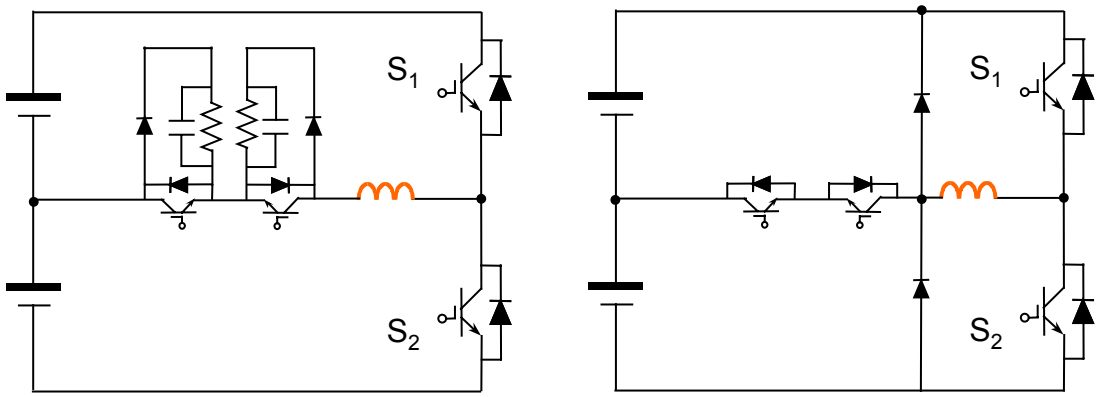


Fig. 3.4. Voltage spike across the auxiliary devices (without any spike suppressing schemes).

There were several schemes developed to deal with suppressing over-voltage. One scheme is the passive snubber circuit shown in Fig. 3.5(a). The R-C-D snubber is across each auxiliary IGBT. It is effective to reduce the voltage spike; however, the R-C-D snubber is lossy since the added snubber capacitor energy has to be completely dissipated. In addition, a careful layout design is required in order to place the snubber circuit close to the auxiliary devices. Another scheme using freewheeling diodes is shown in Fig. 3.5(b). In order to effectively kill the voltage spike, the loop inductance in the freewheeling diode path has to be minimized, which significantly increases the complexity of auxiliary circuit layout design. Additional diodes with the capability to block V_{dc} are required. If there is little inductance in the freewheeling diode path, the main device switching will cause the unexpected current building up in the resonant inductor, which contributes to the conduction loss.

Another method is characterized by splitting the resonant inductor. It is found that splitting the resonant inductors help reduce the voltage ringing between junction capacitor of the auxiliary diode and the conducting resonant inductor. The problem with this method is requiring the additional diodes and resonant inductors. The voltage spike due to the diode reverse recovery may not be reduced by this scheme.



(a) (b)

Fig. 3.5. Voltage suppressing schemes in practical implementation of ARCP inverter.

The previous methods rely on the clamping mechanism to cure the diode reverse recovery problem. From the previous analysis, the voltage spike is directly related to di/dt during the diode reverse recovery. A new method is presented to use a saturable inductor in series with the auxiliary switch, as shown in Fig. 3.6. If the di/dt can be altered to be soft, the voltage stress will be alleviated. When the resonant inductor reaches zero, the saturable inductor enters into its switching region. The abrupt volt-second blocking capability of the saturable inductor helps to reduce the di/dt related to the diode reverse recovery current. In other words, the forwarding current, di/dt, is much reduced with the saturable inductor. Correspondingly, di/dt is also reduced and the voltage spike will be suppressed, as demonstrated in Fig. 3.7. The ringing between the resonant inductor and the junction capacitor of the auxiliary device almost disappears. Based on the estimation of the volt-second requirement, the implementation uses the saturable core METGLAS MP3210P-4as with only one turn winding. Therefore the implementation is very easy and no strict layout requirement is needed.

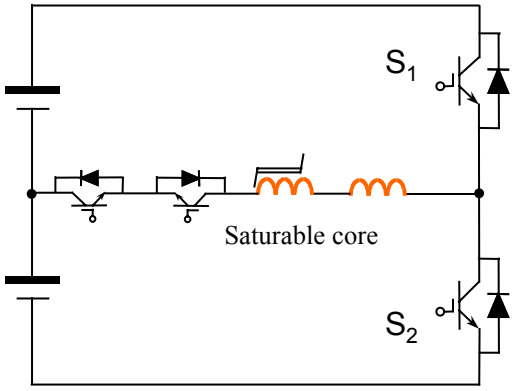


Fig. 3.6. Saturable core suppresses the voltage stress of auxiliary devices in ARCP.

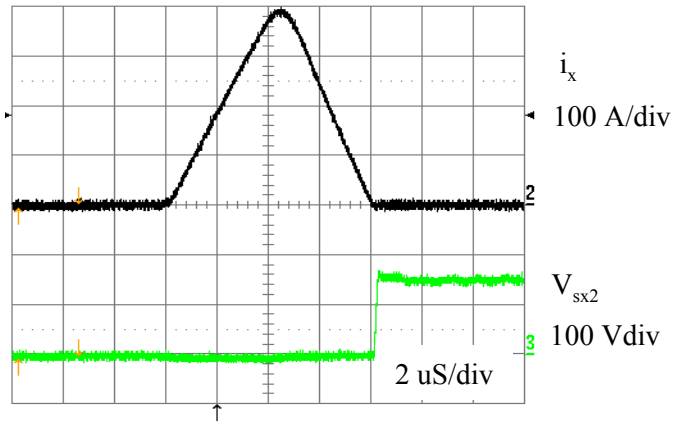


Fig. 3.7. Key auxiliary circuit waveforms when using a saturable core.

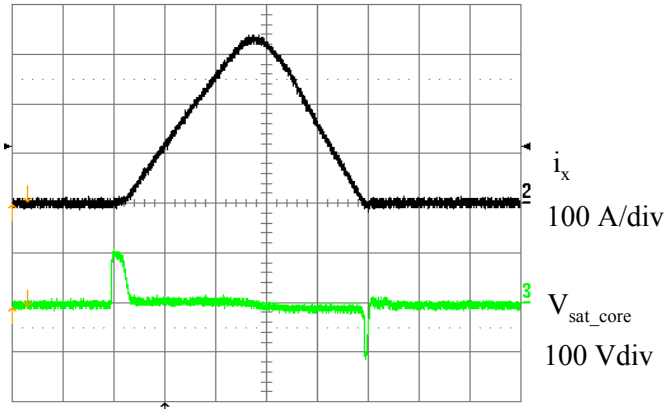


Fig. 3.8. Volt-second applied to the saturable core.

. Volt-second blocking of the saturable inductor is shown in Fig. 3.8. Since the time delay caused by the saturable inductor is less than 400 nS at the DC voltage of 325 V, the compensation of this delay in the auxiliary switch's timing signals is adequate to ensure the zero-voltage soft-switching operation. This imposes no additional complexity of the control timing implementation. Such a short blocking time will not cause any significant reduction of minimum pulse width either.

Fig. 3.9 shows three sets of the designed resonant inductors and the saturable cores. Finally, 0.22μF polypropylene film capacitors with 600V DC rating (SBE 716P224J from the SB electronics company) are chosen as the snubber capacitor.

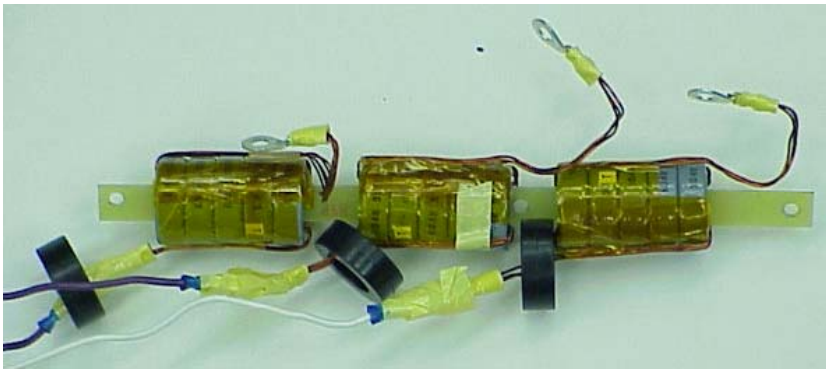


Fig. 3.9. Implementation of the three-phase resonant inductors of the ARCP.

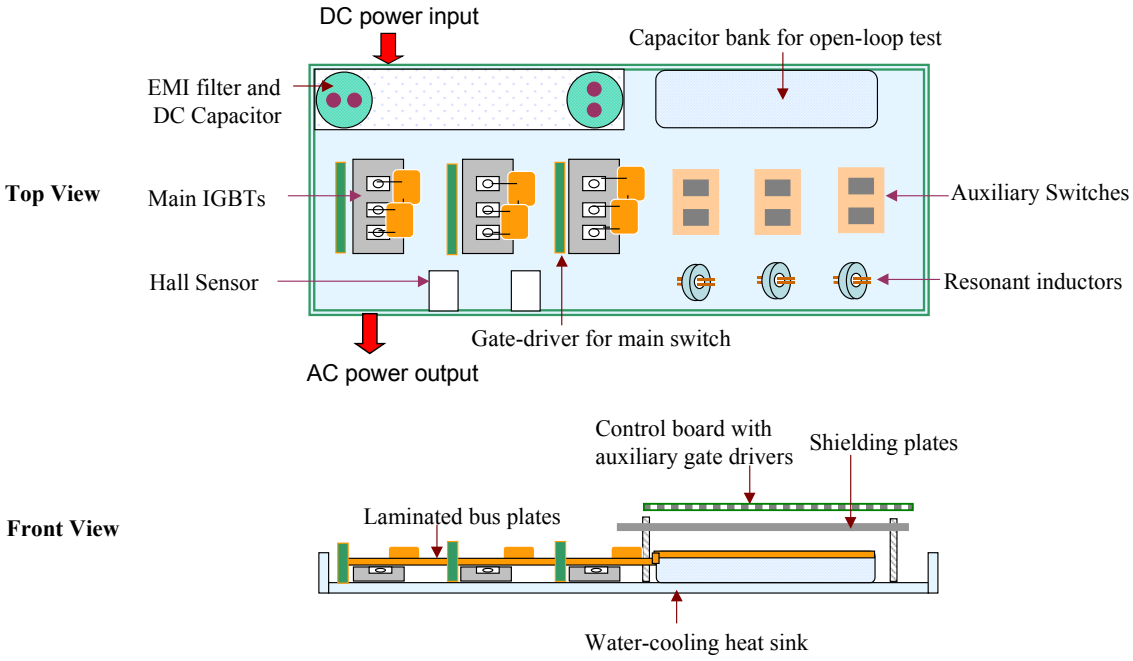


Fig. 3.10. The illustration of the final layout design of an ARCP inverter.

From Fig. 3.10, the DC capacitor and required capacitor banks for the midpoint are connected using the laminated bus plates, providing the positive bus rail, negative bus rail, and the midpoint of the input DC voltage. Each bus plate is made from a 32-mil-thick copper sheet. Insulation material (Mylar type) is placed on both sides of each plate. Connecting holes for the capacitor bank are also made on all of the bus plates. Based on the layout design, the final assembly of the ARCP inverter is shown in Fig. 3.11. Underneath the bus bar and the control board, the power devices and two 150V film capacitors are exposed to show the position of those components, as pictured in Fig. 3.12.

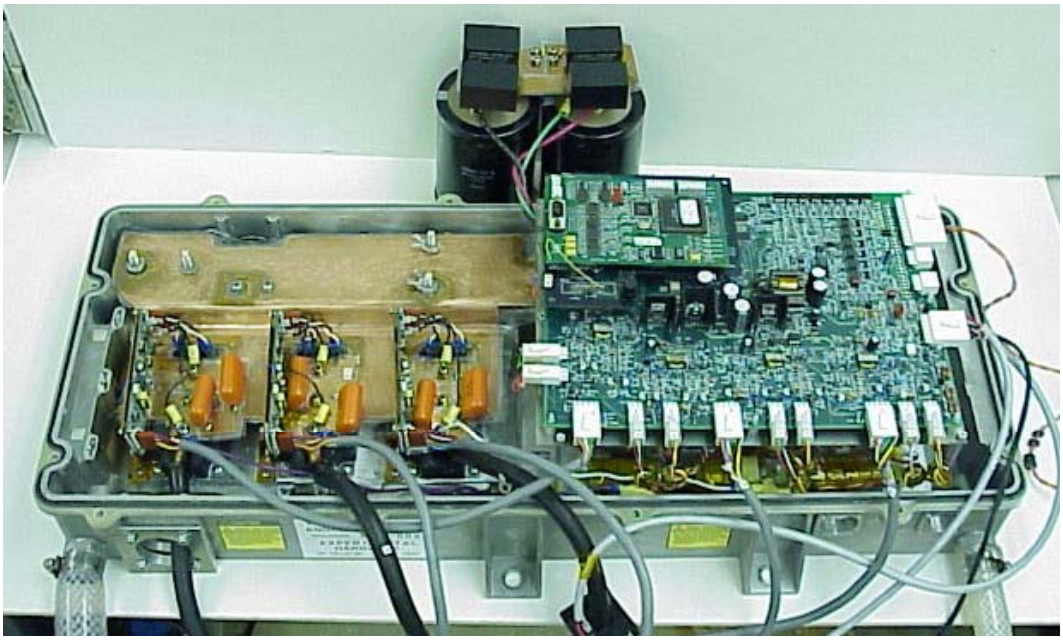


Fig. 3.11. The complete assembly of the ARCP inverter.

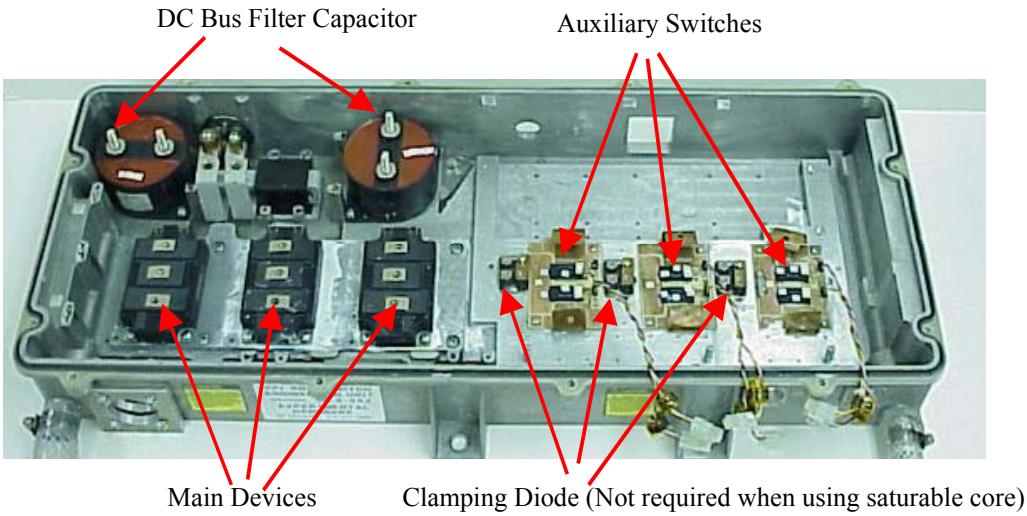


Fig. 3.12. Location of power devices and bus capacitors.

3.2.2. Design and Implementation of Six-switch ZCT Inverter

As explained in Chapter 2, the design of the resonant tank in the six-switch ZCT inverter should aim to achieve an optimal efficiency over the entire speed/torque range of EV drives, with a proper trade-off between switching losses and conduction losses. The resonant tank parameters are finally designed as C_x=1 μF and L_x=600 nH, which creates a resonant time period of 5 μs and a resonant tank impedance of 0.75 Ω. A one-turn inductor structure is chosen to minimize the core loss at high-switching-frequency operation and to avoid saturation with a high peak resonant current. Consequently, small-size cores can be used. In order to achieve the required inductance, several cores may be stacked to increase the total cross-section area.

Since the inductance required for the resonance is only 600 nH, the stray inductance caused by the inverter layout is also counted into the total inductance. Both theoretical analysis and experimental measurements show that the inductance of a one-inch-long AWG 20 wire is about 20 nH, and that of a one-inch-long, 0.3-inch-wide, 32-mil-thick copper foil is about 15 nH at a high-frequency range (100-500 kHz). The difference is caused by the high-frequency parasitic capacitor effect. In the designed ZCT inverter power stage, the distance from the main devices to the resonant inductor is about 15 inches, which causes about 220nH stray inductance. Including the stray inductance caused by the laminated bus bar, about 280nH stray inductance is counted into the total resonant inductance.

Molypermalloy powder (MPP) cores, composed of nickel, iron, and molybdenum, are suitable for this application. They typically saturate at 0.8 T and offer low losses at high frequencies. The MPP core with a permeability of μ=60, Magnetics 55894-A2, is selected. Its major parameters are: the cross-section area Ac=0.654 cm^2, the magnetic path length L=6.35cm,

and the inner dimension ID=0.555 inch. Several 55894-A2 cores need to be stacked in order to achieve the desired inductance with one turn of conductor going through. The inductance caused by one 55894-A2 core with one turn, ΔL_x, is obtained as

$$\Delta L_x = \frac{0.4 \cdot \pi \cdot A_c \cdot \mu_r}{L} \cdot 10^{-8} = 80\text{nH} \cdot \tag{3.1}$$

When four 55894-A2 cores are stacked, they generate total inductance of 320 nH. Adding the 280 nH stray inductance, the total resonant inductance is about 600 nH, satisfying the design requirements.

With V_{dc} = 325 V, C_x = 1 μF and L_x = 600 nH, the maximum resonant peak current, I_{x_peak}, is

$$I_{x\_peak} = \frac{V_{dc}}{\sqrt{L_x / C_c}} = 440\text{A} \cdot \tag{3.2}$$

The maximum flux density B_m is given by

$$B_m = \frac{0.4\pi \cdot I_{x\_peak} \cdot \mu_r}{L} = 5200\text{gauss}, \tag{3.3}$$

where B_m is in the linear region of a 55894-A2 core. During a fundamental line cycle of the inverter operation, however, the resonant current peak reaches this maximum value I_{x_peak} only at the no-load condition, or at the zero-crossing region of the inverter load current. At the light-load condition, in order to achieve a reasonable trade-off between the switching losses and conduction losses, the ZCT function normally is disabled at the light load to avoid a high conduction loss, since the switching loss is relatively small at this moment. As a result, the flux density at the normal inverter operation is around 4000 gauss. In summary, the resonant inductor is designed to be four Magnetics MPP 55894-A2 cores in a stack, with one turn of conductor going through them.

Similar to the ARCP inverter, the auxiliary device is selected based on the RMS current and peak current requirements. The auxiliary switches are activated for only a very short time (several microseconds) at the main switch turn-on and turn-off transitions; consequently, the RMS current requirement is relatively low. At the same time, the auxiliary switches must conduct a narrow, high-peak resonant current. For the 55kW inverter, the RMS current required for the auxiliary switches is about 50 A, but the maximum resonant peak current can be up to 400 A. Therefore, the device selection is mainly determined by the peak current handling capability.

The relatively high ratio between the peak and RMS values of the resonant current and the feature of zero-current switching make thyristor-based devices the ideal auxiliary devices. But, again, the commercial MCTs are not yet mature enough for high-power applications. The power MOSFETs are not suitable either, because the conduction loss inherent in the 600V-class MOSFETs is not acceptable. Thus, the selection of the auxiliary devices focuses on the 600V-class IGBTs.

Data sheets of commercial IGBT devices, however, normally do not specify the maximum peak value of a repetitive narrow pulse current with the time width down to the resonant period (3~6 μs). In addition, as a bi-polar device, when the IGBT collector current I_C exceeds the maximum allowable peak current, the on-state collector-emitter voltage V_{ce} tends to increase dramatically and uncontrollably, which will prevent I_C from increasing further. If this effect occurs in a resonant circuit, the resonance will become highly nonlinear and the resonant current will be distorted. Since the auxiliary switches are turned off at the zero-current condition, with a device stress much less than that which occurs in a conventional hard-switching turn-off,

experimental testing of the auxiliary devices is a must. A series resonant circuit is used to test the peak current capability of the IGBT modules, as shown in Fig. 3.13. Several IGBT modules from different manufacturers have been chosen and tested to verify the capability of handling the high peak current. The test results are shown in Fig. 3.14. Both Eupec BSM150GD60DLC and IR IRG4ZC70UD can meet the requirement of the peak current. The Eupec BSM150GD60DLC is six-pack module while IRG4ZC70UD is a single IGBT. Therefore Eupec BSM150GD60DLC is selected for the auxiliary switches for easy implementation. Within this module, six IGBT switches and their anti-parallel diodes are integrated into one package, which simplifies the inverter layout.

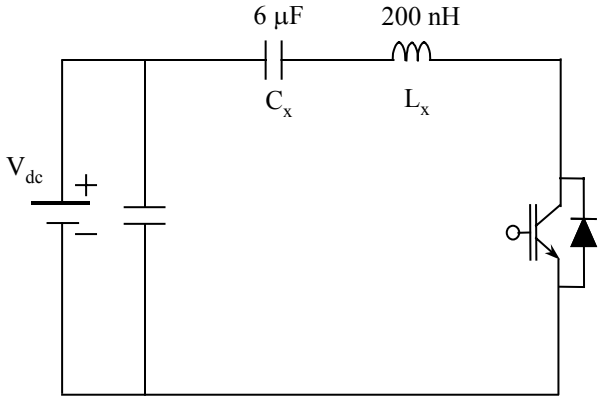


Fig. 3.13. The series resonant circuit for testing the auxiliary device.

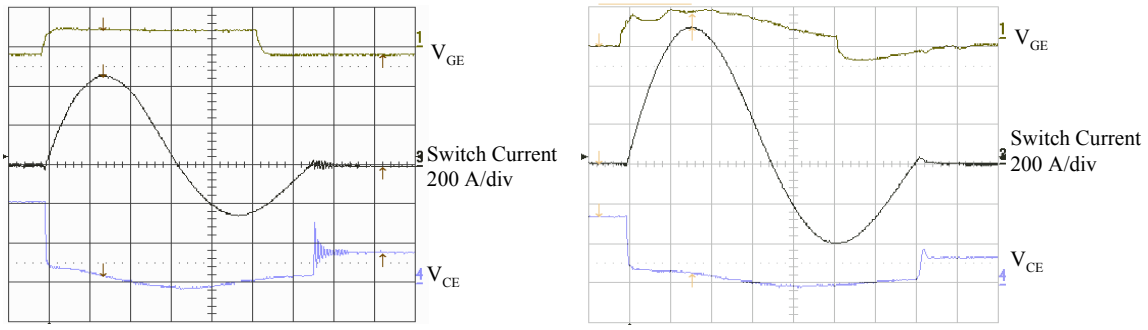


Fig. 3.14. Waveforms of auxiliary device testing: (a) IRG4ZC70UD 100A/600V (b) the Eupec BSM 150GD60DLC IGBT six-pack module, 150A/600V.

Fig. 3.15 illustrates the inverter layout design, and Fig. 3.16 shows photos of the hardware implementation. In the chassis, there are two DC film capacitors and an input filter, which are mounted on the left side of the water-cooling chassis. The main switches, three MG300J2YS50 300A/600V half-bridge IGBT modules, are located on the left side of the chassis, near the DC capacitors. This location is beneficial to the thermal management of the main devices, because exactly underneath this position, the contact area between the cooling water and the heat sink is larger than that in other positions. To reduce the EMI, three gate-driver boards for the main switches are placed close to the corresponding main switches. The auxiliary device, one BSM150GD60DLC 150-A/600-V six-pack IGBT module, is located on the right side of the chassis, adjacent to the DC capacitors. The control board is placed on top of the power stage. There are six gate-driver circuits built in the control board, which are used for gating the auxiliary device. To minimize the parasitic effects in the DC link, a laminated bus bar made of copper sheets is designed and built to connect the DC capacitors and the three main IGBT modules. Another laminated bus bar made of printed circuit board (PCB) is designed to connect the six-pack auxiliary IGBT module. These two bus bars are interconnected as a unit and they cover the power stage. The stray inductance of the conductors is counted into the total desired resonant inductance. The three-phase stray inductance should be as balanced as possible; thus, the lengths of the three-phase connections should be equal.

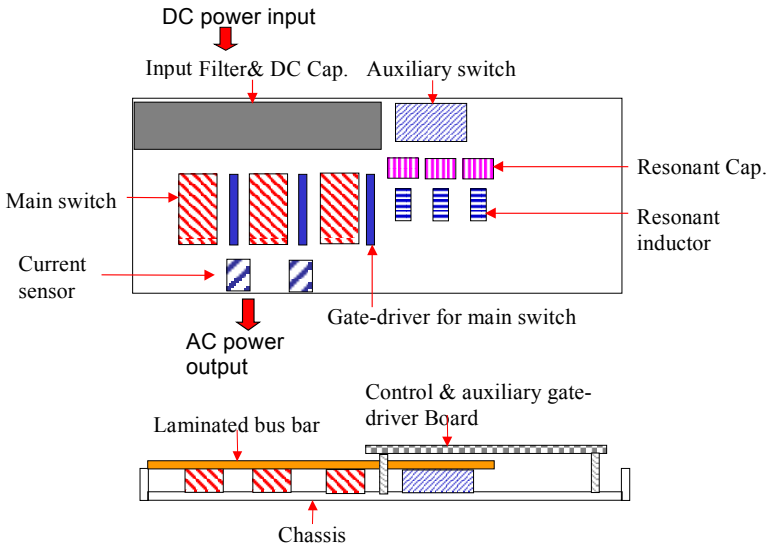
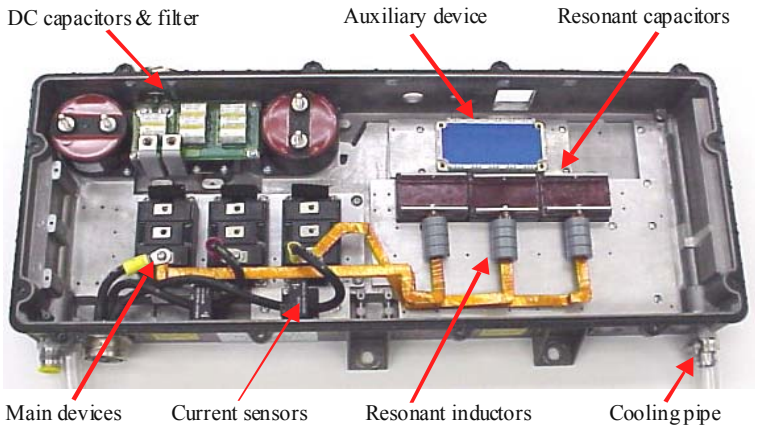
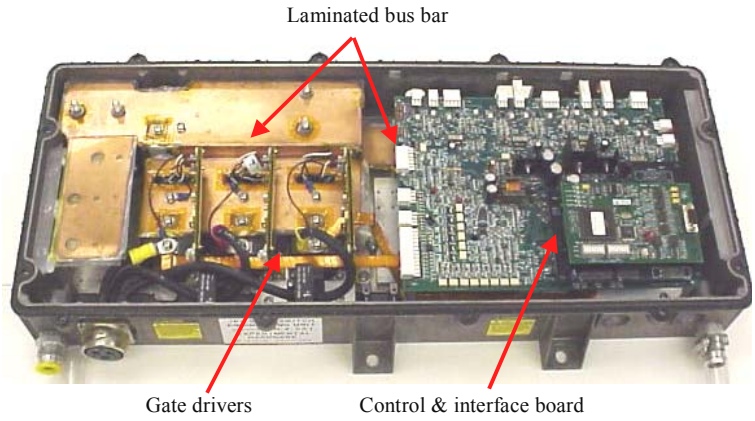


Fig. 3.15. Illustration of six-switch ZCT inverter layout.



(a)



(b)

Fig. 3.16. The six-switch ZCT inverter assemblies: (a) power stage assembly and (b) final assembly with the control board.

3.2.3. Design and Implementation of Three-switch ZCT Inverter

Since EV motor drives cover a rather wide speed and torque range, the design of the resonant tank aims to achieve an optimal efficiency over the entire speed/torque range, with a proper trade-off between switching losses and conduction losses. Design considerations similar to those for the six-switch ZCT inverter apply to the three-switch ZCT inverter. However, the three-switch ZCT may not be as optimal as the six-switch ZCT due to the limited soft-switching control variables. The resonant tank parameters are designed to be C_x = 0.625 μF and L_x = 820 nH, which create a resonant time period of 4.5 μs and a tank impedance of 1.15 Ω.

A one-turn inductor structure is also chosen for the resonant inductor in order to minimize the core loss at high-frequency operation and to avoid saturation with a high-peak resonant current. Since the inductance required for resonance is only 820 nH, the stray inductance caused by the inverter layout is taken into account for the total inductance. The final design leads to a resonant inductor made of six Magnetics MPP 55894-A2 cores in a stack.

To select a suitable 0.625μF resonant capacitor, both voltage rating and conduction loss should be considered. The maximum resonant capacitor voltage can be twice the DC bus voltage, which occurs at either the no-load condition or the zero-crossing region of the inverter load current. Considering that the battery voltage may be charged up to 400 V in some cases, a capacitor with at least an 800V rating should be chosen. A polypropylene film capacitor is the ideal choice for minimizing the conduction loss during the high-resonant-frequency operation. Finally, SBE 716P series 1000V/0.625μF metalized polypropylene film capacitors with an RMS current rating of 50 A are selected. These capacitors have a dissipation factor (DF) of approximately 0.08% at 100 kHz and an ESR of about 1.4 mΩ at 50 kHz.

The rule for selecting auxiliary devices is similar to those for the 6-switch ZCT inverter and the ARCP inverter. The RMS current requirement for the auxiliary switches is relatively low. Because the auxiliary switches must conduct a narrow, high-peak resonant current, the device selection is mainly determined by the peak-current-handling capability. In addition, the auxiliary switches are turned off at zero current, so the device stress is much smaller than it would be if it was hard-switched.

Different from the six-switch ZCT inverter, the selection of the auxiliary devices focuses on the 600V class discrete IGBT modules. The selection of the auxiliary switches is assisted by a simple device tester, which creates the series resonance so that the resonant current flows through the devices. Whether or not the waveform is distorted, determines whether the device can handle the high peak current. After several discrete IGBT modules were tested, the IRG4ZC7 100A/600V surface-mounted IGBT with anti-parallel diode was selected. This is the same device that was used in the ARCP ZVT inverter. It has only one-third the DC current rating

of the main switches (300A half-bridge IGBTs), and the data sheet specifies that its over-current capability is four times over the nominal current within the time width of 1 mini-second at 25^{o}C. The device test performed for this work shows that this device can handle a peak current of up to 800 A within the time width of down to several micro-seconds, which is in the range of the resonant period designed for the three-switch ZCT inverter. When the resonant current peak value is increased up to 800 A, the switch current waveform is still close to sinusoidal. This means that the IRG4ZC7 is suitable for use as the auxiliary switch of soft-switching inverters. In addition, the IR60EPF06 60A/600V fast-recovery diode is selected as the clamping diode in the auxiliary circuit.

The auxiliary devices are directly surface-mounted on a two-inch-by-two-inch isolated–metal-substrate (IMS) board. As explained for the design of the ARCP inverter, the IMS board uses Al_2O_3, which is a low-cost solution for thermal conduction and electrical isolation. Besides the IGBT and the clamping diode, three copper studs are also soldered onto the IMS board to connect the positive DC rail, the negative DC rail, and the resonant tank. A mini-socket is also soldered on in order to connect the gate-driver board. The IMS board will be mounted onto the heat sink in the inverter chassis through four mounting holes. Fig. 3.17 shows one photo of the auxiliary switch package.

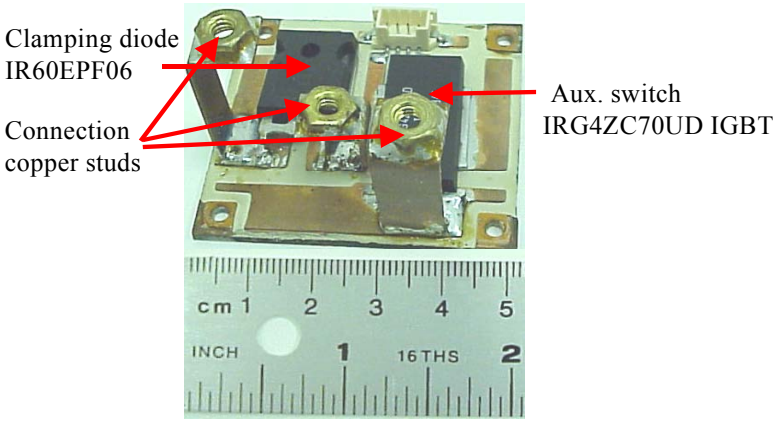


Fig. 3.17. Auxiliary switch/diode pair implementation for three-switch ZCT inverter.

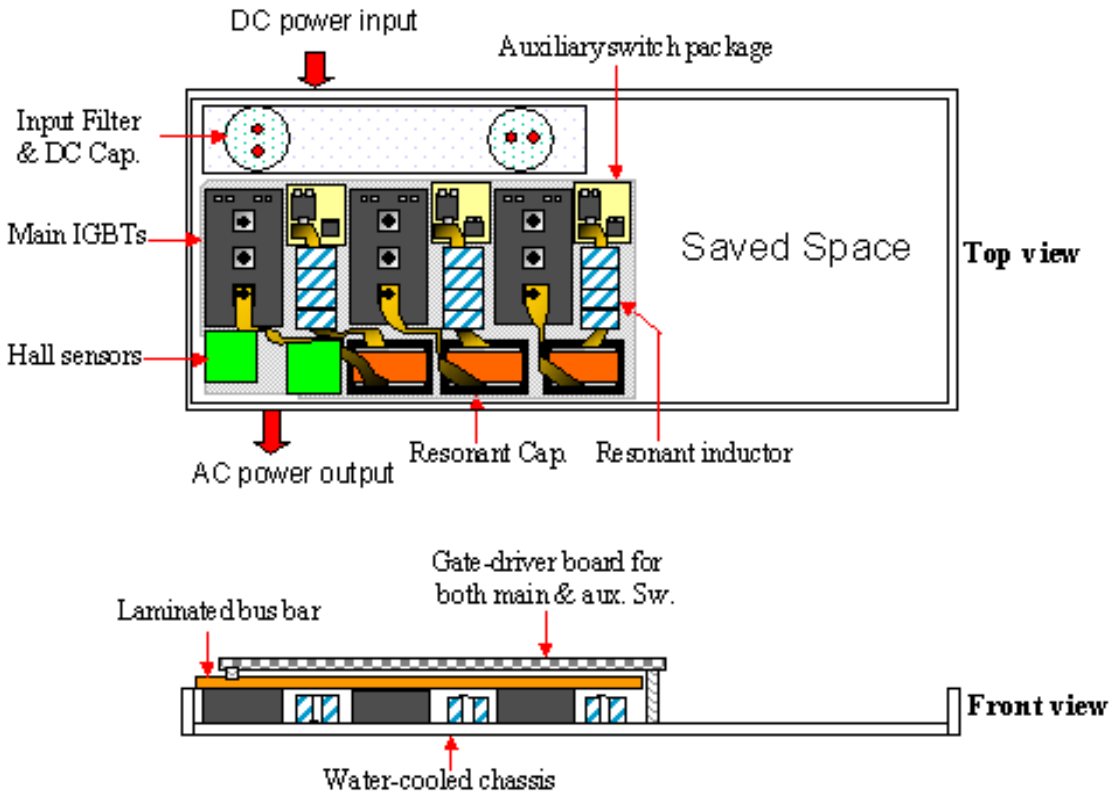


Fig. 3.18. Illustration of the layout design for the three-switch ZCT inverter.

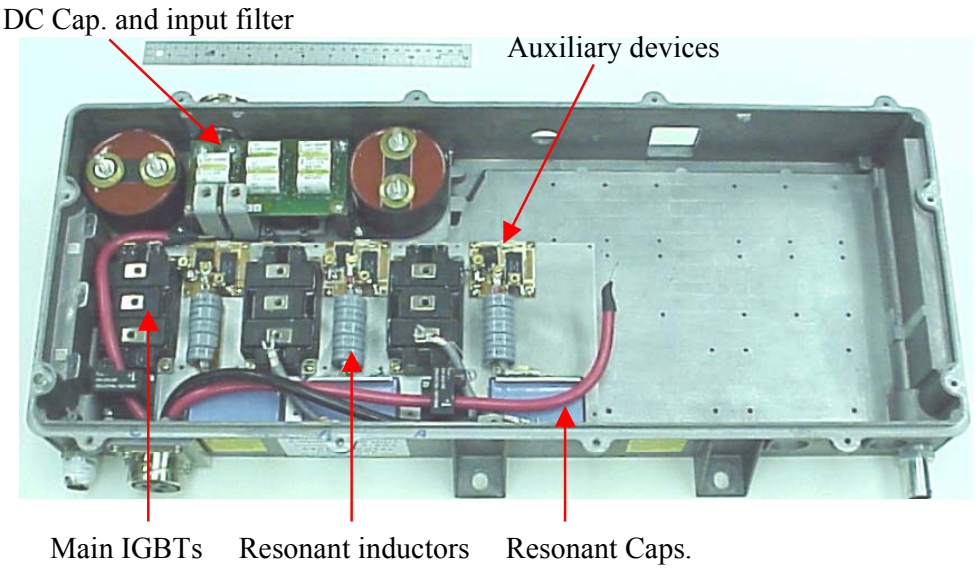


Fig. 3.19. Power stage layout of three-switch ZCT inverter.

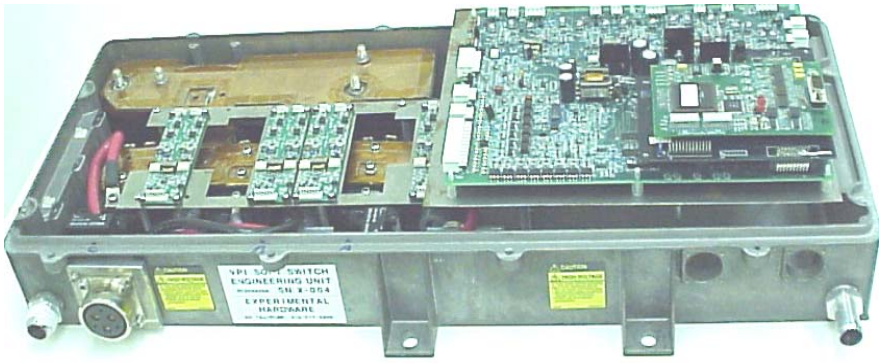


Fig. 3.20. Overall assembly of three-switch ZCT inverter.

As can be seen from Fig. 3.18, two DC film capacitors and an input filter are mounted on the left side of the water-cooled chassis. The main switches, three MG300J2YS50 300A/600V half-bridge IGBT modules, are located on the left side of the chassis, near the DC capacitors. Each of the auxiliary-switch IMS packages are located adjacent to the corresponding main IGBTs. The resonant tank for each phase, which consists of the resonant capacitor and inductor, is also located adjacent to its corresponding main IGBTs. As pictured in the real layout arrangement in Fig. 3.19, a lot of space in the right side of chassis has not been used. This indicates that by

reducing the main switch number from six to three, not only is the number of gate drivers and the active devices (IGBT in this case) reduced, but also the packaging flexibility offers a great savings in terms of space. The obtained three-switch ZCT inverter is shown in Fig. 3.20.

3.3. Implementation of Variable-timing Soft-switching Control

The soft-switching control implementation is very important when different soft-switching inverters are tested on one dynamometer testbed. Two control aspects need to be carefully considered. One is the interface between the inverter soft-switching controller and the motor drive core controller. The other is whether one controller structure can generate the soft-switching control signals for different soft-switching inverters. This section describes the development of the controller, which is designed with the flexibility to serve both hard- and soft-switching operations. An interface circuit, implemented with an electronically programmable logic device (EPLD), allows the controller of the hard-switching inverter to perform soft-switching operation with up to six auxiliary switches. This is considered to be the "piggy-back" concept from the power stage to the control. As shown in Fig. 3.21, the original DSP controller was developed for hard-switching inverter operation only. In order to generate the auxiliary gate signals according to the main PWM signals, a EPLD board is introduced. Its major function is to interface with the main DSP controller and to obtain the information of time delay between the main devices' and auxiliary device's control signals. With this concept, the hard-switching inverter system will easily be capable of performing soft-switching control, as shown in Fig. 3.21 and Fig. 3.22.

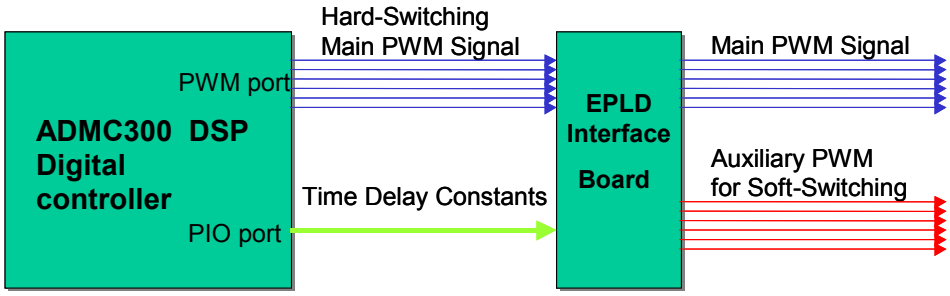


Fig. 3.21. Principle for soft-switching PWM signal generation based on hard-switching core.

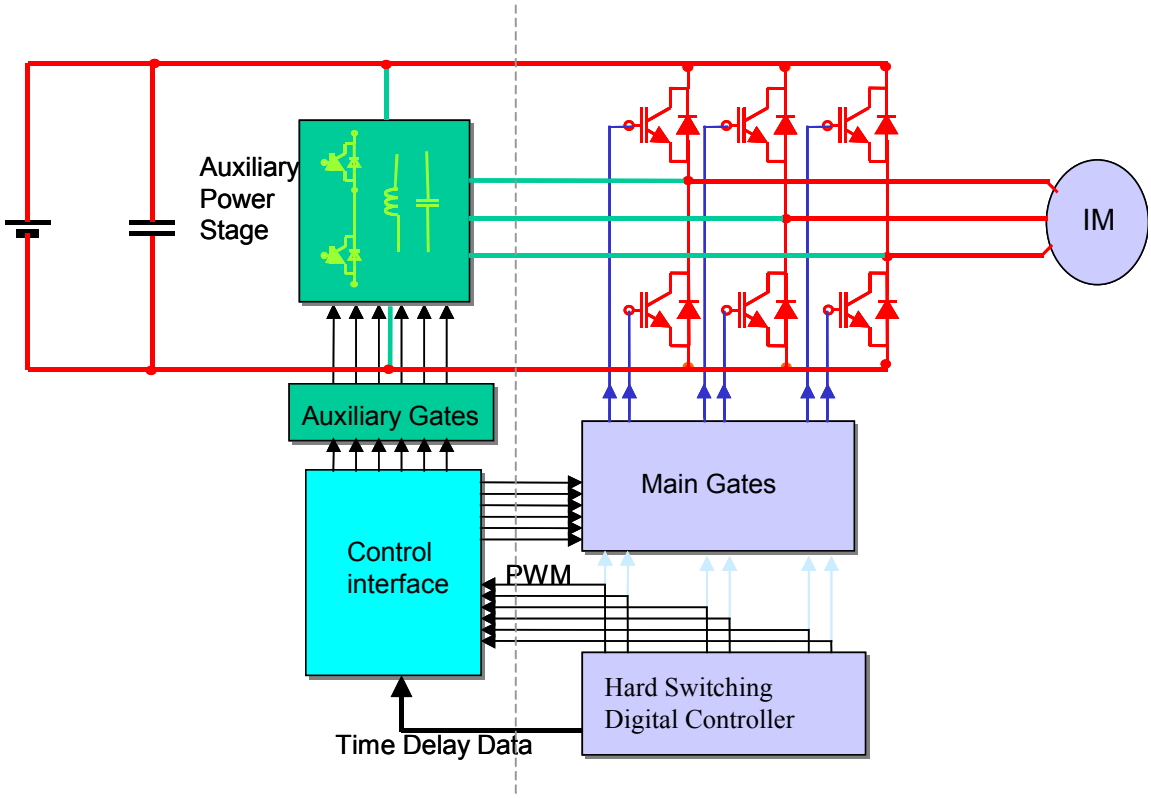


Fig. 3.22. A flexible controller structure for soft-switching inverters.

The main DSP control program needs to generate the time delay information between the main PWM signals and the auxiliary switch's gate signals, and then transfer them to the EPLD. After the time delay data is transferred successfully to the EPLD, the next objective is to use these data to generate auxiliary PWM signals. The approach here is to generate the auxiliary pulses based on the edges of the main PWM signals. The turn-on time and pulse width of the

auxiliary pulse can be specified by the time delay data written to the EPLD. However, to generate the auxiliary pulse earlier than a corresponding main PWM pulse, it is necessary to first delay the main PWM pulse for a certain amount of time. The main PWM pulse is delayed so that it can accommodate the maximum pre-triggering time needed for the auxiliary switches. This idea is illustrated in Fig. 3.23. The main PWM signals have been delayed so that this delay time, noted as $t_{maindly}$, should be at least no less than t_{delay}.

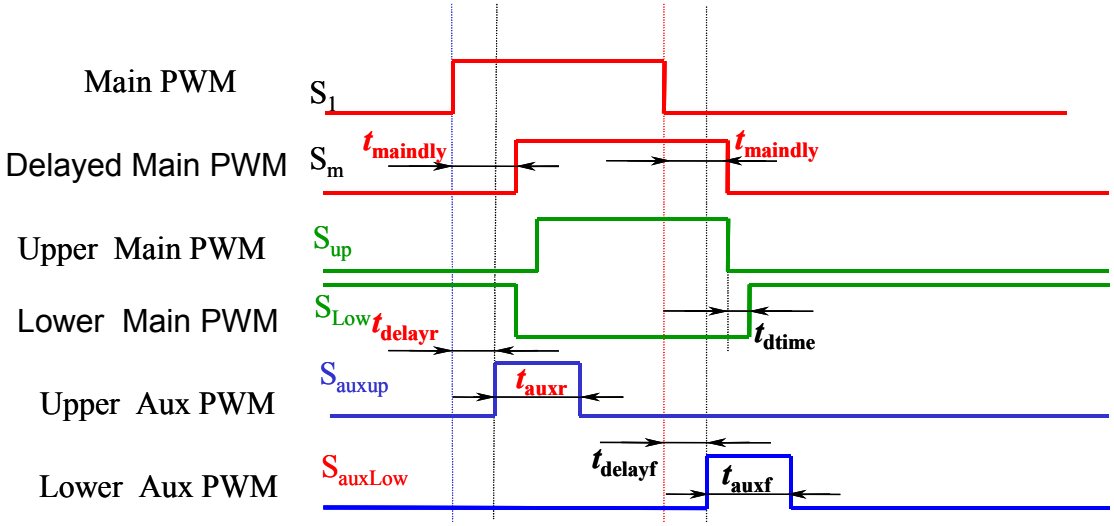


Fig. 3.23. Generation of auxiliary PWM signals based on the edges of main PWM signals.

Based on the concept illustrated in Fig. 3.23, the detailed function block diagram inside the EPLD, for generating the PWM pulses, is shown in Fig. 3.24.

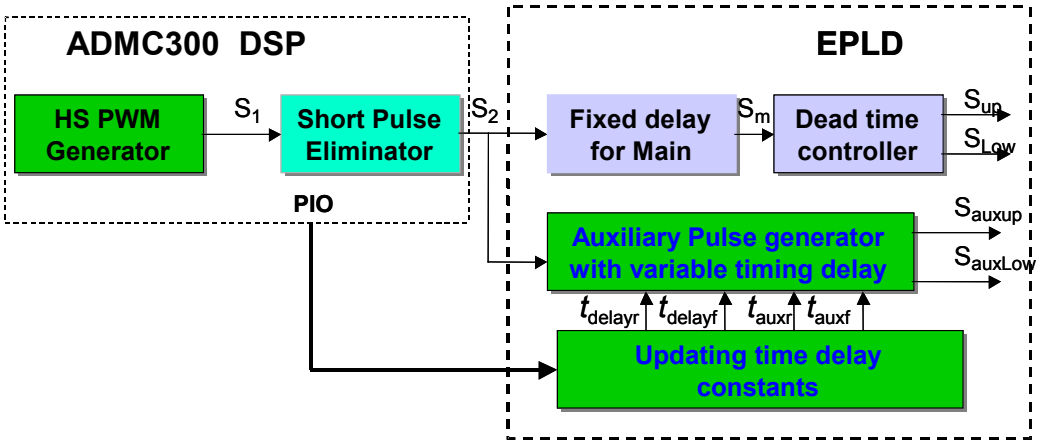


Fig. 3.24. Functional diagram for auxiliary PWM pulse generation in EPLD.

Besides the variable timing control signals, the intermediate step for achieving closed-loop torque control is to realize the open-loop VVVF SVM control. Fig. 3.25 shows the flow chart of the main subroutine of the open-loop control program. Besides the setup of the interrupt vector and PWM configuration, the duty-cycle information of the first switching cycle is calculated. After this, the program enters the infinite loop, waiting for the entire PWM interrupt or the monitor interrupt. Fig. 3.26 shows the flow chart of the PWM interrupt subroutine. Right after entering the PWM interrupt service routine, the DSP writes the newest duty-cycle information to the PWM port of ADMC300. Then, the position of the voltage vector in the next switching cycle is calculated; information of the sector where the voltage vector is located and the vector angle in this sector needs to be derived. The next step is to calculate the duty cycle for the voltage vector that falls within the boundary of the sector and the zero-vector. Finally, the duty cycle for each phase is calculated. Currently, the six-step SVM PWM control is realized, where in 60 degrees of fundamental period one phase has no switching action.

The monitor interrupt is a software interrupt, which is enabled once for every ten PWM interrupts. It reads the voltage-vector amplitude and frequency signal through the A/D ports so that both amplitude and frequency can be changed during the open-loop test.

For the hard-switched inverter test, the above-described open-loop test software is sufficient. For the soft-switching inverter test, the load current information will be processed to determine the suitable width of the auxiliary switch's gate signals even in the open-loop test.

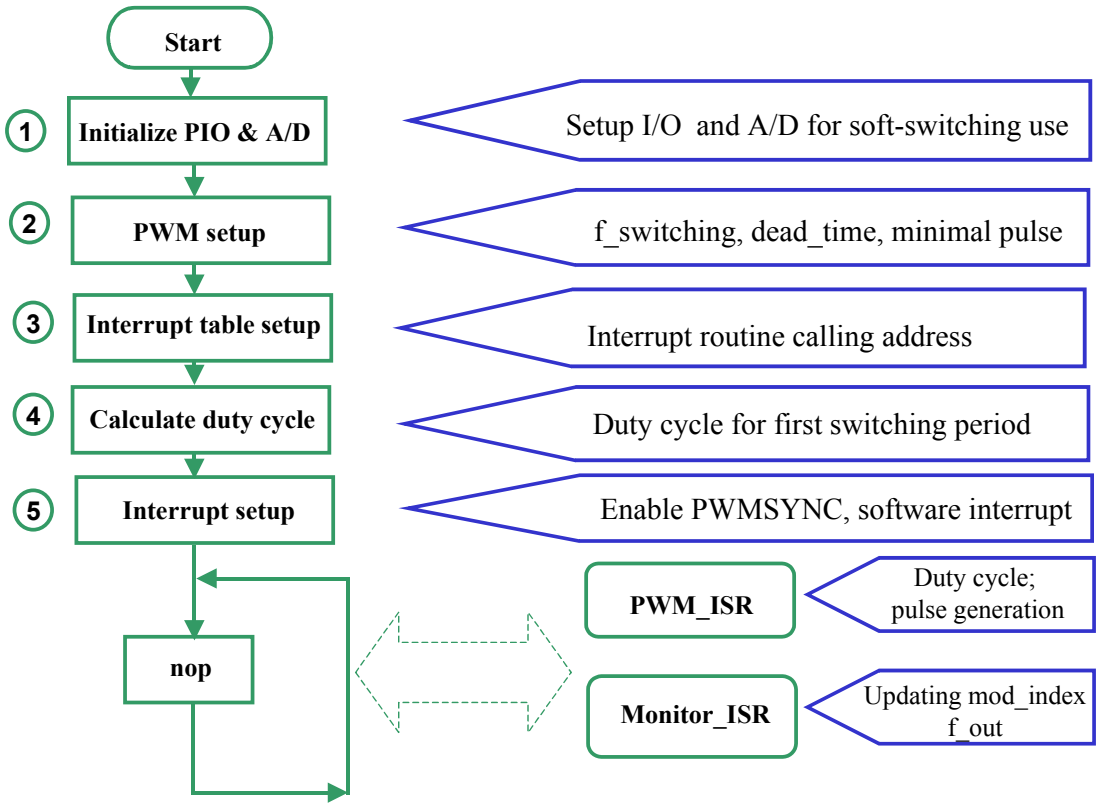


Fig. 3.25. Flow chart of main program routine in open-loop control software.

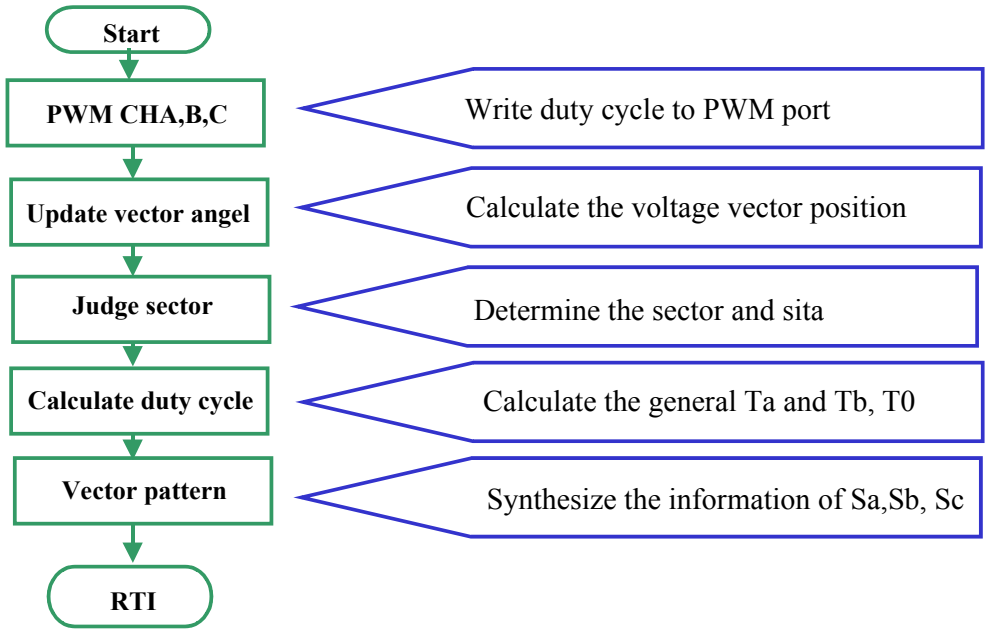


Fig. 3.26. Flow chart of PWM interrupt service routine for open-loop testing.

3.4. Efficiency Evaluation of Soft-switching Inverters on the Dynamometer

3.4.1. Dynamometer Testbed System

The inverter testbed at CPES can measure the electrical values of a tested inverter as well as the mechanical values of a tested motor. In addition, both the inverter and motor efficiencies are measured with two methods. First is the steady-state test to measure the efficiency over the full range of usable motor torque and speed. Second is the drive-cycle test to measure the transient efficiency or the efficiency of the drive system when the vehicle is on the road in a dynamic driving situation.

The inverter testbed consists of a dynamometer, an automated controller, and a data acquisition system. The dynamometer has a simple mechanical connection of two drive systems, such as the tested system and the load system, and the torque and speed meters, as shown in Fig. 3.27. Twenty-six battery packs are located under the dynamometer platform.

As shown in Fig. 3.28, the control box controls the DC input line connection for both the tested system and the load system. This control box can control the operation, such as setting the rotation direction and setting the speed and torque, of the tested system as well as of the load system. For precise control of a drive cycle test, the external computer can control the operation through RS-232 communication. The data-acquisition system measures and calculates the necessary data at all input/output points of the drive system. This consists of a torque/speed computer, a power analyzer, and a data-acquisition computer and board.

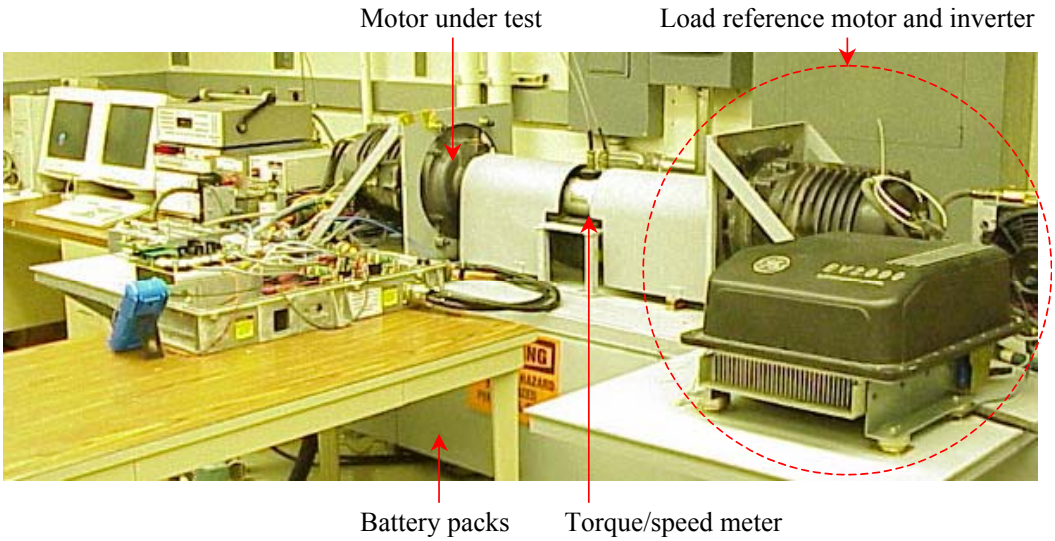


Fig. 3.27. Dynamometer structure.

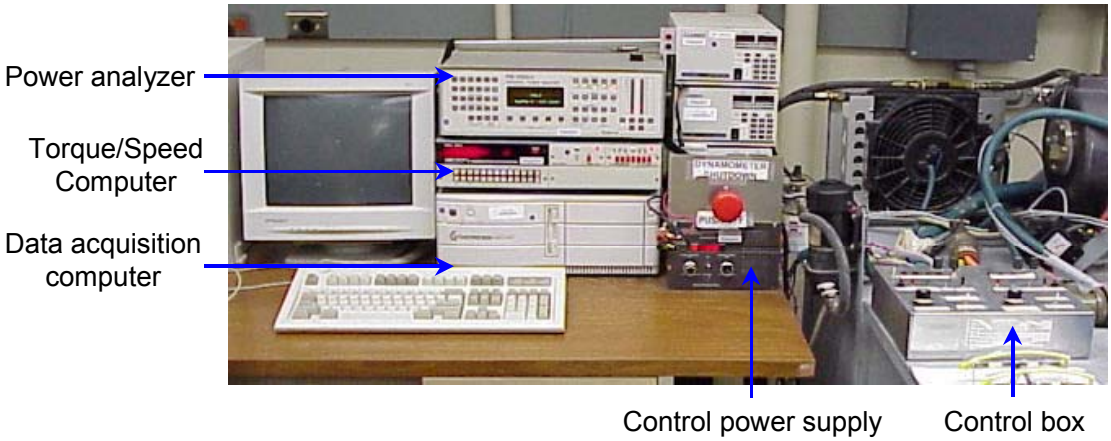


Fig. 3.28. Control and measuring equipment on dynamometer system.

The torque/speed meter and the torque/speed computer measure the mechanical data of the motor, and the power analyzer measures the electrical data of the inverter and motor system. Fig. 3.28 shows the connections of the measuring instruments.

The torque/speed meter includes two parts: the torque meter and the speed meter. The torque meter is a non-contact strain gauge that measures the mechanical deformation of a solid shaft connecting the test and the load motors. A hall-effect pulse counter is also built into the housing for speed measurement. A 60-tooth wheel mounted on the shaft creates speed output. The maximum speed and torque ratings are 8,000 rpm and 1,111 N-m.

The Himmelstein torque/speed computer on the dynamometer is connected to a torque/speed meter. This computer is calibrated to measure shaft torque in pound-inch (lb-in) from a torque meter designed for 10,000 lb-in full-scale torque. The torque/speed computer displays the measured torque and speed, and calculates both positive and negative shaft power between the motors.

Analog voltage outputs from the torque/speed computer are connected to the data-acquisition unit. The data-acquisition unit provides a means for high-speed sampling to a data file. Once

captured, the torque and speed data are integrated over the drive-cycle interval for a measurement of drive cycle efficiency.

The Voltech power analyzer is used to measure the DC input power and AC output powers of the dynamometer. It combines all energy measurements and interfaces with a data-acquisition unit for data logging. Channel 3 is used to measure all of the electrical values of DC input, and both channels 1 and 2 measure all the electrical values of AC outputs. Because there are only two channels for three-phase AC outputs, the two-wattmeter method is used, as shown in Fig. 6.4. Figure 6.5 shows the detailed hardware setup of the power analyzer. The PM3000A can measure current up to 200A peak. Because the maximum load current reaches 200 Arms and 300A peak, three external current sensors (CTs) are installed at each line of two AC output lines and DC input line, as shown in Fig. 6.5. This CT makes the output signal (M) proportional to the current. A closed-loop hall-effect current sensor, LEM LT-300, is used as the CT in the CPES dynamometer. This sensor requires bipolar voltage inputs (+15 V and –15 V) that the power analyzer provides. PM3000A provides these bipolar voltages and a ground potential. The output signal of the current sensor is connected to the A-EXT terminal of the power analyzer. The output signal is a current-type, but PM3000A requires a voltage-type signal for terminal input. Therefore, a shunt resistor is required across both the output signal of a CT and the ground potential that is connected to the A-LO terminal of the same channel. Fig. 3.29 shows three shunt resistors (R1, R2 and R3) installed between the output signals of three CTs and the ground potential provided by the power analyzer. In real installation, a 10 Ω / 0.5 % resistor is used as the shunt resistor. In order to measure the DC input voltage, the positive DC line is connected to the V-HI terminal of channel 3, and the negative line is connected to the V-LO terminal of

channel 3. For measuring AC output voltages, two phases are connected to the V-HI terminals of both channel 1 and channel 2. These two phases should be the same as those for current measurement. The remaining phase is connected to the V-LO terminals of both channel 1 and 2.

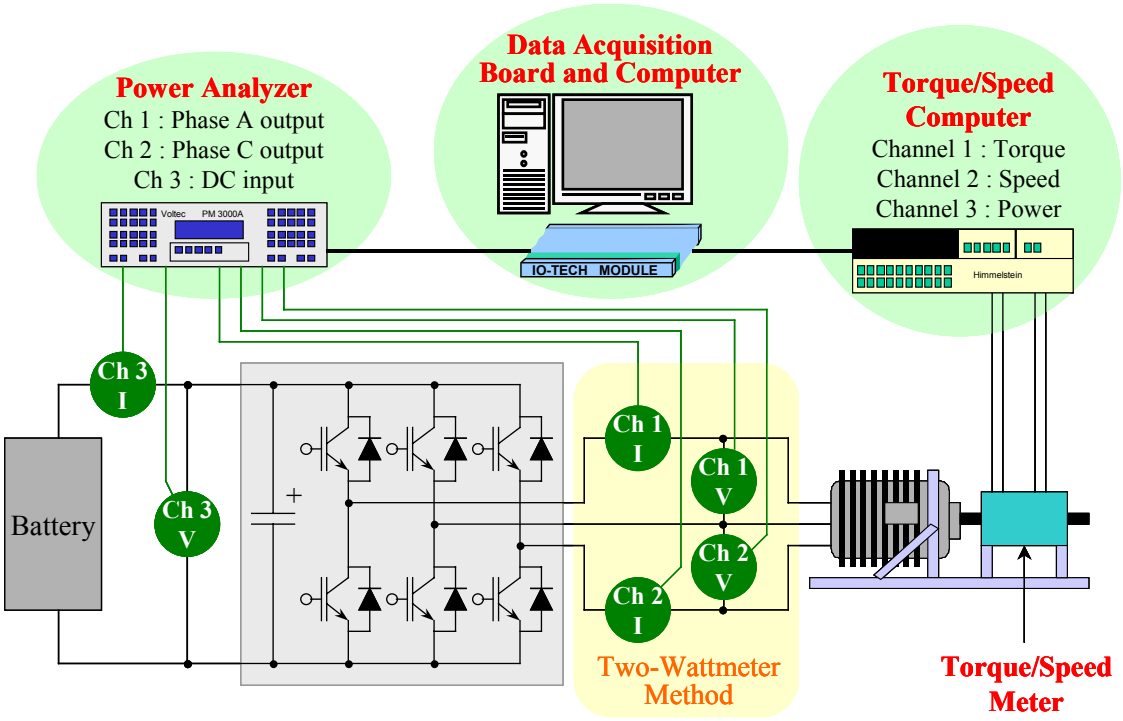


Fig. 3.29. Dynamometer measurement instrument connection.

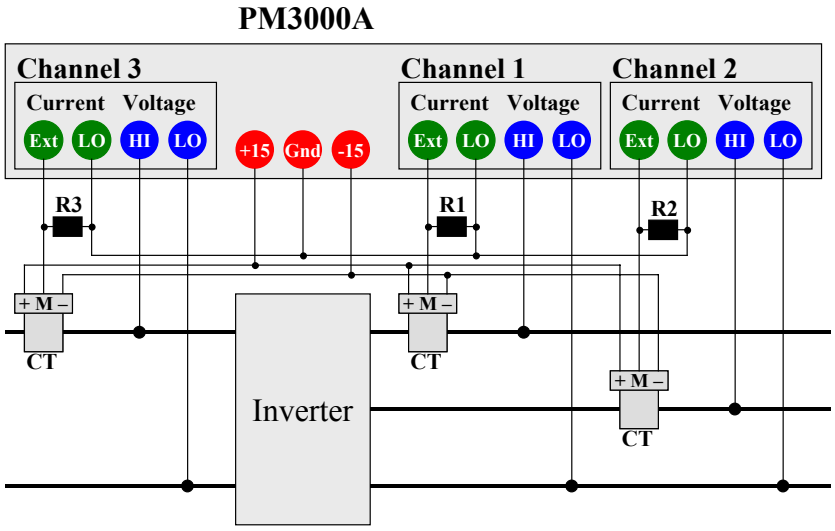


Fig. 3.30. Setup for measuring voltage and currents using PM3000A.

3.4.2. Efficiency Evaluation

To compare the performance of several soft-switching inverters with that of the hard-switching inverter, 14 test points are chosen based on the drive cycle, covering a range of torques and speeds, as shown in Fig. 3.31.

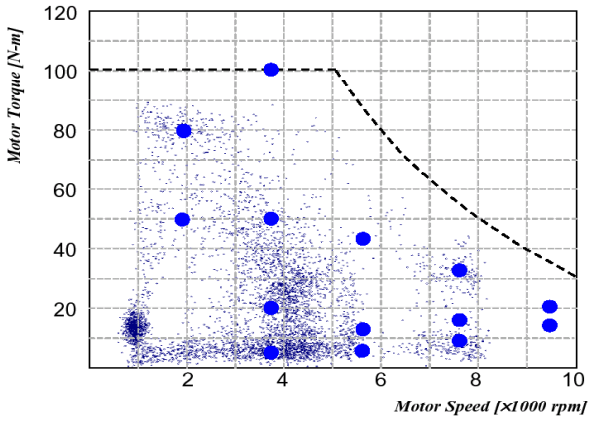
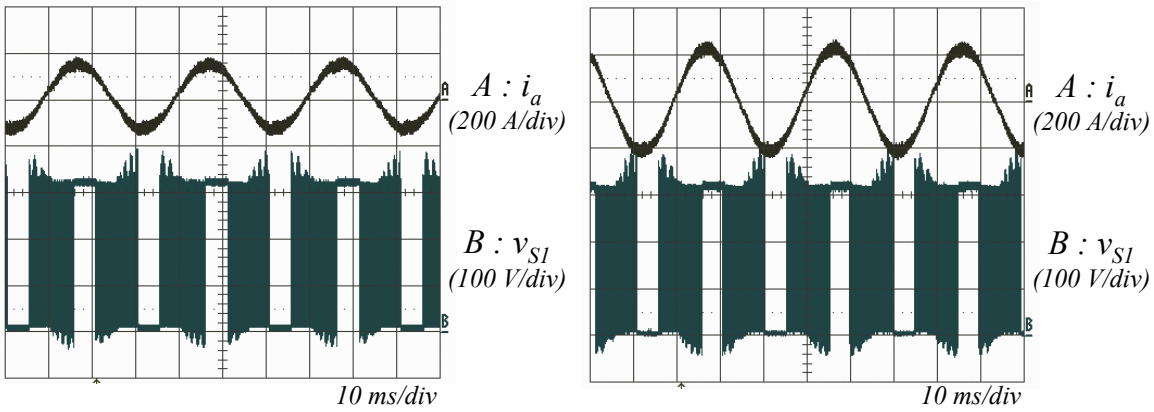


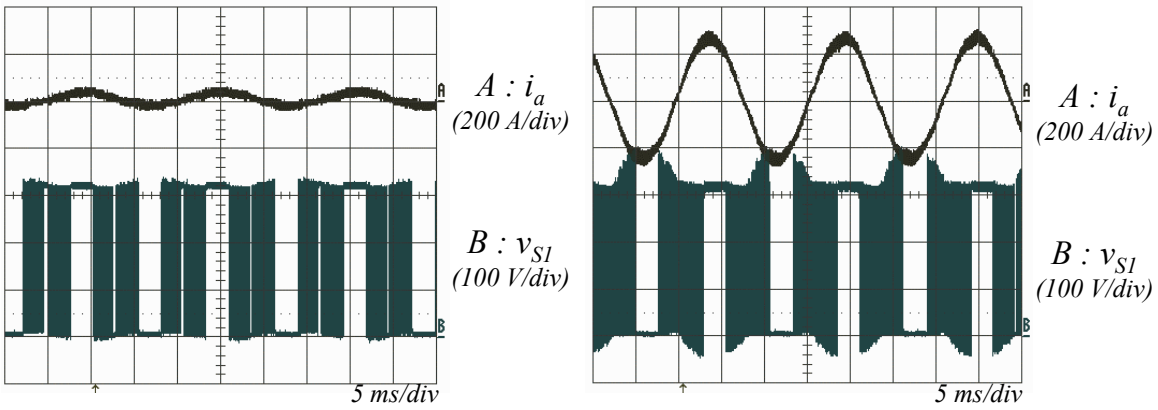
Fig. 3.31. Recommend test points based on drive cycle.

3.4.2.1. Verification of Closed-loop Operation

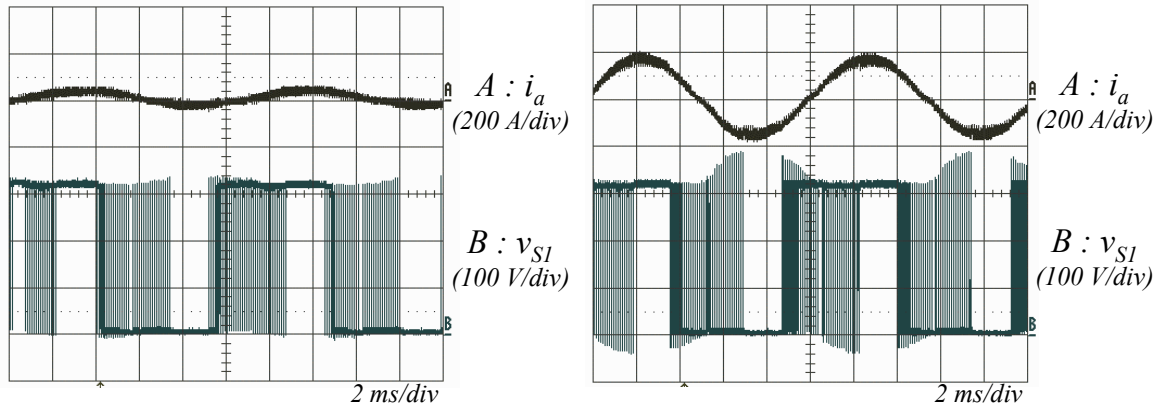
Before taking the efficiency measurement, it is mandatory to check whether the hard-switching and soft-switching inverters are able to operate correctly over all the test points. Fig. 3.32 shows the measured waveforms of both the load current and the main IGBT voltage during the steady-state test for the hard-switching inverter. The current waveforms are well balanced and sinusoidal at most of the test points. However, there are some low-frequency fluctuations in the current waveform at high speed, as shown in Fig 6.9 (i) and (j). It is suspected that the mechanical vibration of the testbed might have caused these current fluctuations. The IGBT voltage waveforms reveal information about the voltage spike level. The voltage spikes reach almost 400 V at the high-current cases. However, these values are much less than the voltage rating of the MG300J2YS50 (600 V). Therefore, it is verified that the developed hard-switching inverter operates well in the entire test range. Both the current and voltage waveforms will be compared with those of soft-switching inverters.



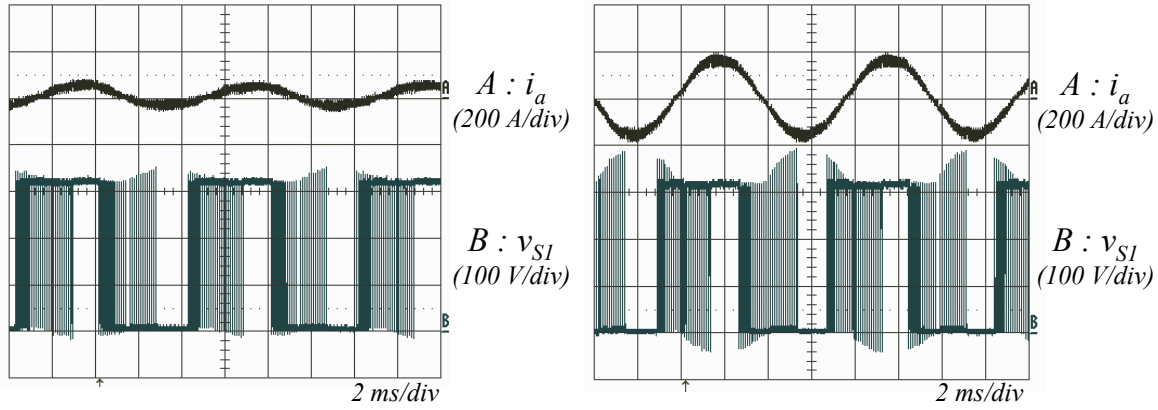
(a) (b)


A : i_a
(200 A/div)
B : v_{S1}
(100 V/div)
5 ms/div

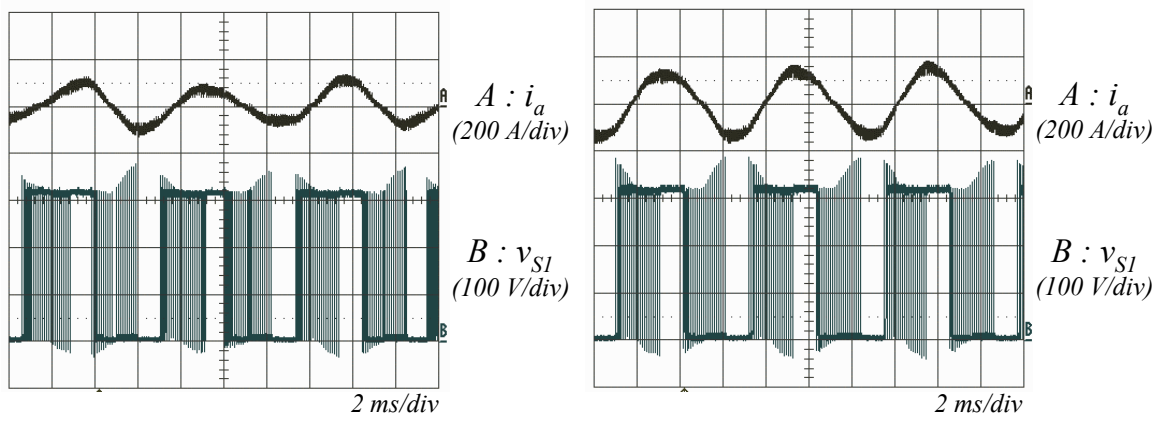
(c) (d)


A : i_a
(200 A/div)
B : v_{S1}
(100 V/div)
2 ms/div

(e) (f)


A : i_a
(200 A/div)
B : v_{S1}
(100 V/div)
2 ms/div

(g) (h)



(i) (j)

Fig. 3.32.Measured waveforms of the hard-switching inverter during steady-state test: (a) S = 1922 rpm, T = 50.57 N-m, (b) S = 1926 rpm, T = 80.94 N-m, (c) S = 3771 rpm, T = 5.17 N-m, (d) S = 3775 rpm, T = 101.31 N-m, (e) S = 5628 rpm, T = 5.79 N-m, (f) S = 5628 rpm, T = 41.87 N-m, (g) S = 7546 rpm, T = 9.83 N-m, (h) S = 7542 rpm, T = 31.95 N-m, (i) S = 9459 rpm, T = 12.99 N-m, (j) S = 9459 rpm, T = 20.02 N-m.

Fig. 3.33 shows the measured load-current and resonant-current waveforms during the steady-state test, at different torque and speed points. The maximum peak load current reaches about 280 A at 100 N-m, as shown in Fig. 3.24(b). The load-current waveforms are quite sinusoidal at most points, which demonstrates that ZCT implementation does not interfere with the fundamental control functions of the closed-loop induction motor-drive system. Otherwise, the load-current waveforms would be distorted, or even unstable at certain points. In Fig. 3.24 (a), the torque is below 5 N-m, and the peak load current is less than 40 A. With such a small amount of current, the switching loss is relatively small. To avoid unnecessary circulation energy and conduction losses in the auxiliary circuit, the gate signals for the auxiliary switches are disabled at the light load; thus, there is no resonant current produced. For this test case, the threshold instantaneous load current value is set to about 50 A, below which the gate signals for the auxiliary circuit are disabled. A further design trade-off examination is underway to find an optimal threshold value for the entire speed/torque range. Because the six-step SVM is used, no

switching actions occur at the main switch when the load current is at the highest point within one line cycle; and the auxiliary switches are only activated at the main switch turn-on and turn-off transitions. That is why during certain time intervals of the waveforms, there is no resonant current generated even though the load current is high.

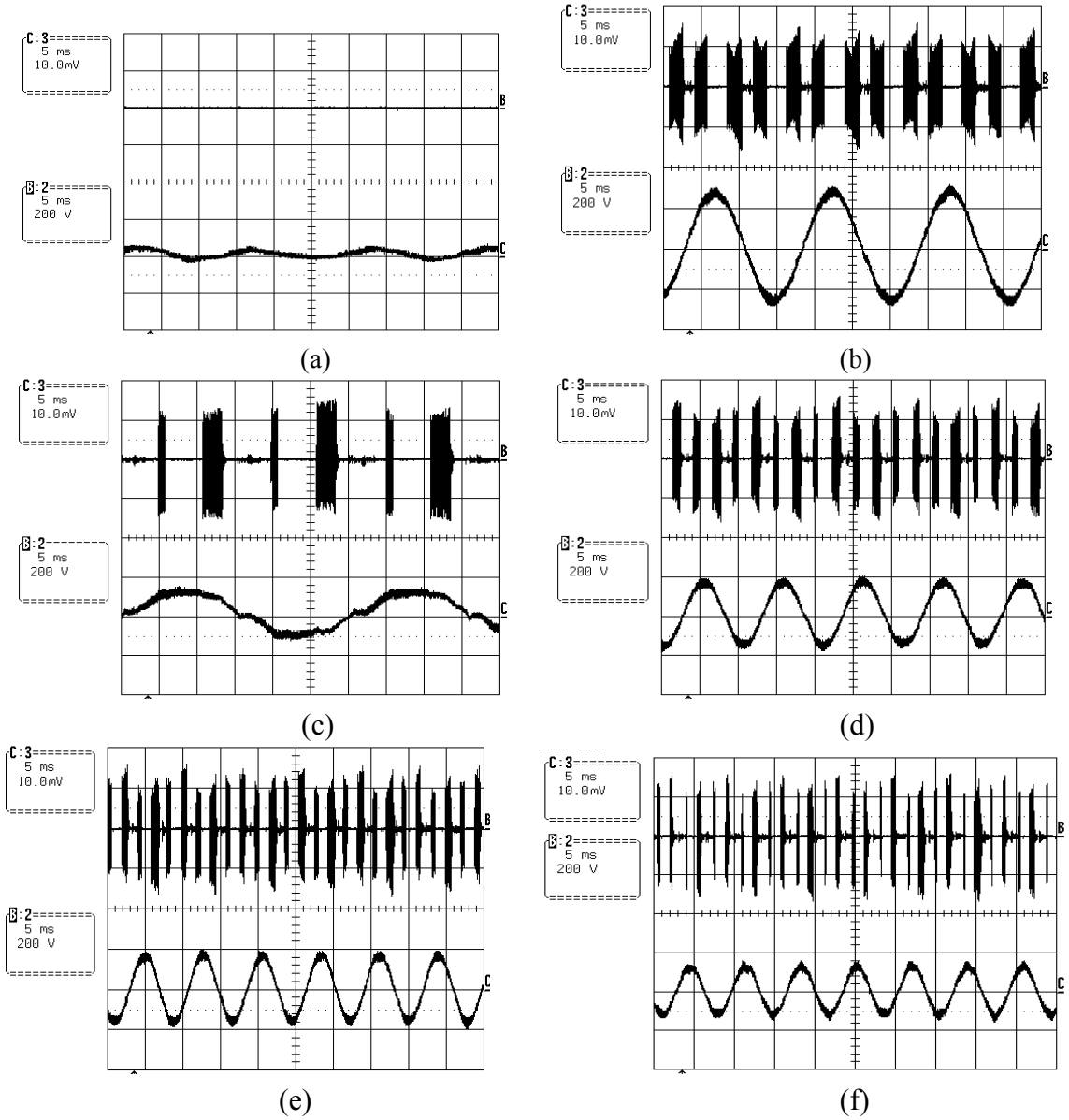
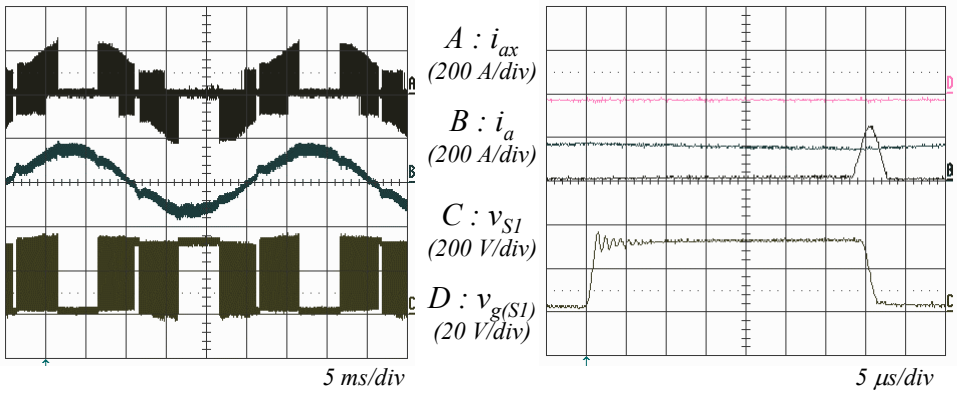


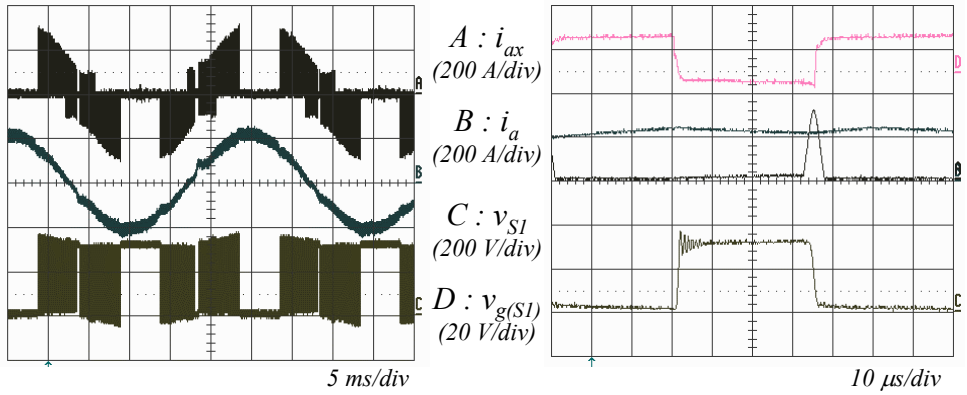
Fig. 3.33. Measured current waveforms of the ZCT inverter during the steady-state test:

S=3840 rpm T=4.92 N-m, (b) S=3758 rpm T=100.42 N-m, (c) S=1952 rpm T=50.75 N-m, (d) S=5697 rpm T=41.77 N-m, (e) S=7568 rpm T=31.26 N-m, (f) S=8584 rpm T=19.65 N-m. Channel C: the load current (200 A/div); channel B: the resonant current (200 A/div); time (5 mS/div).

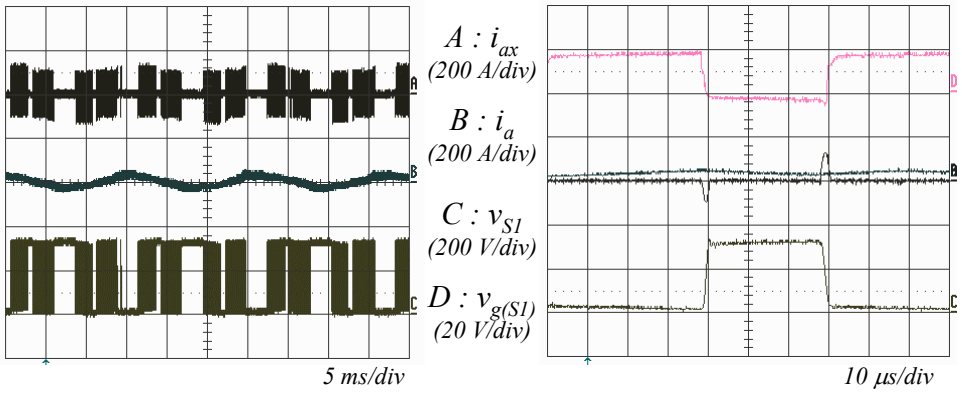
Fig. 3.34 shows the auxiliary inductor currents, load currents, and device voltages at several speed and torque conditions for the ARCP inverter. The left-side waveforms of this figure show the line cycle, and those on right side display the zoomed switching cycle waveforms for each condition. As shown in the line-cycle waveforms, load current shapes are well balanced, and the auxiliary inductor currents are appropriately generated. In general, there is a one-direction auxiliary inductor current for the zero-voltage turn-on commutation. However, a both-direction auxiliary inductor current is required at low load current in order to help not only the zero-voltage turn-on but also the snubber capacitor discharges. The line-cycle waveforms basically identify these kinds of operations as those of a ZVT inverter. The switching-cycle waveforms are directly zoomed from the line-cycle waveforms at the highest-load-current condition. At any speed and torque condition, the auxiliary inductor current is properly generated, and the device voltage of the main switch shows clear ZVT operation. When the load current is less than about 50 A, there are two auxiliary inductor currents in one switching cycle, as shown in (c), (e), (g) and (i) of Fig. 3.25, as expected. These line- and switching-cycle waveforms verify the appropriate operations of the ARCP inverter on the dynamometer.


A : i_{ax}
(200 A/div)
B : i_a
(200 A/div)
C : v_{S1}
(200 V/div)
D : $v_{g(S1)}$
(20 V/div)
5 ms/div
5 μs/div

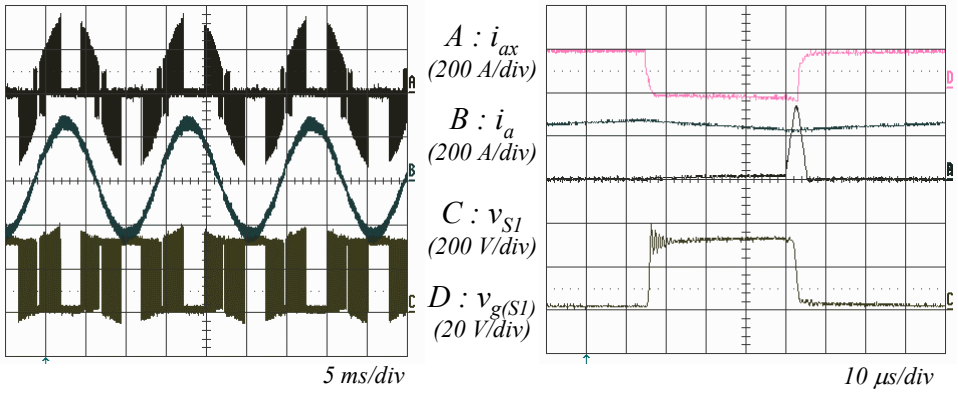
(a)


A : i_{ax}
(200 A/div)
B : i_a
(200 A/div)
C : v_{S1}
(200 V/div)
D : $v_{g(S1)}$
(20 V/div)
5 ms/div
10 μs/div

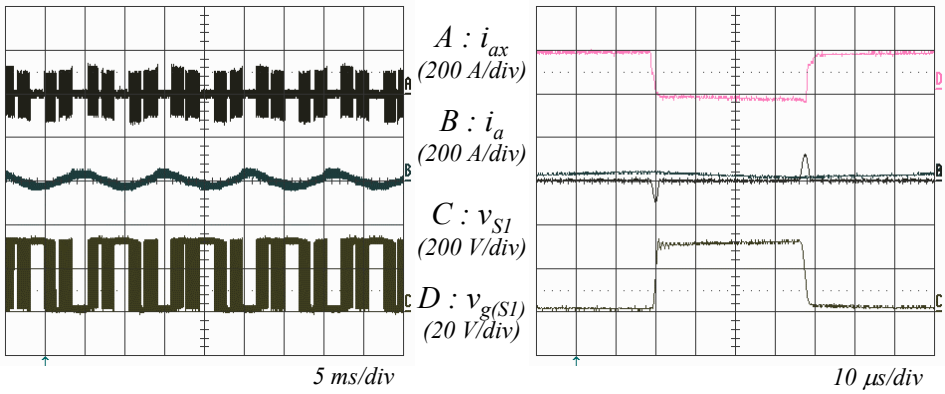
(b)


A : i_{ax}
(200 A/div)
B : i_a
(200 A/div)
C : v_{S1}
(200 V/div)
D : $v_{g(S1)}$
(20 V/div)
5 ms/div
10 μs/div

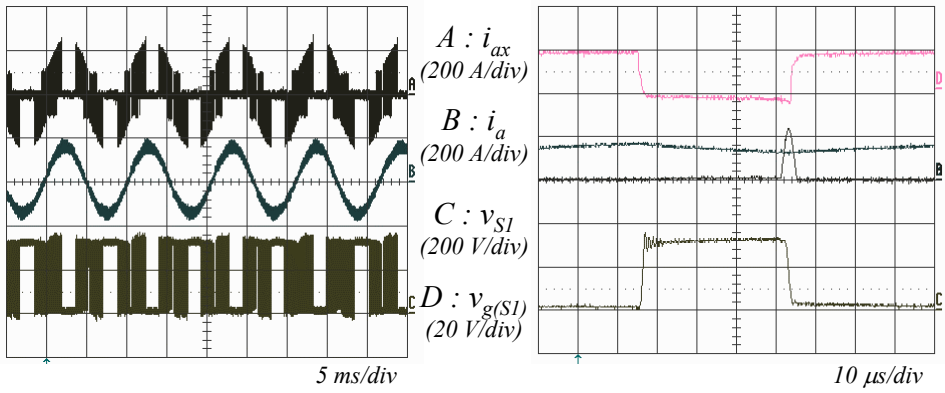
(c)



(d)



(e)



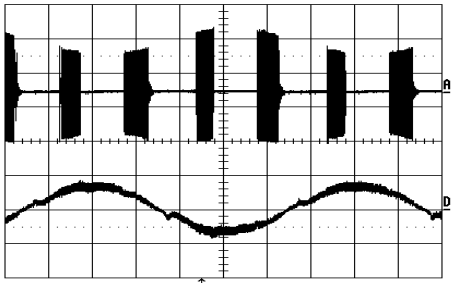
(f)

Fig. 3.34. Measured waveforms of ARCP inverter at steady-state test:

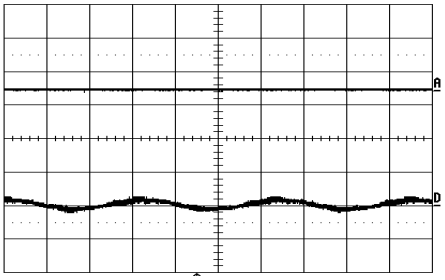
(a) s = 1918 rpm, T = 50.6 N-m, (b) s = 1918 rpm, T = 80.8 N-m, (c) s = 3771 rpm, T = 5.0 N-m, (d) s = 3783 rpm, T = 101 N-m, (e) s = 5621 rpm, T = 5.8 N-m, (f) s = 5633 rpm, T = 41.8 N-m.

For the three-switch ZCT inverter, Fig. 3.35(a)~(h) show the waveforms of the measured load current and auxiliary resonant current during the steady-state test, at different torque and speed points. Since a piggyback structure is used for the design of the inverter software and hardware, there is no change in or compromise to the dynamometer control functions that are based on hard-switching inverters. Fig. 6.27 also shows that the load-current waveforms are quite close to sinusoidal at most points. Such results demonstrate that the implementation of the soft-switching operation does not interfere with the fundamental control functions of the closed-loop induction motor-drive system, which was designed based on hard-switching inverters. If this was not so, the load-current waveforms would be distorted, and the overall system would become unstable at certain points.

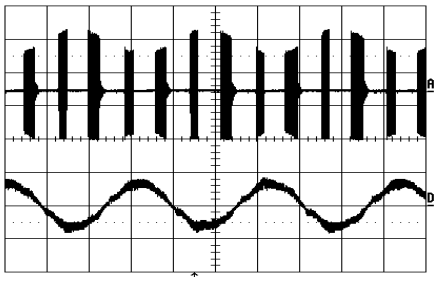
The minimum peak load current is about 30 A, which occurs at 3,770 rpm/5 N-m, with the minimum power of about 3 kW, as shown in Fig. 3.35(b). The maximum peak load current reaches about 280 A, which occurs at 3,770rpm/100 N-m, with the maximum power of around 48 kW at the DC input, as shown in Fig. 3.26(d). At the highest speed (S=9470 rpm), the load-current waveform oscillates slightly, as shown in Fig. 3.26(h). This oscillation is most likely due to the mechanical vibration of the encoder that measures the shaft speed becoming more severe with very high-speed rotation of the motor. Similar to the trade-off considerations for the six-switch ZCT inverter, the control signals of the auxiliary switches are disabled at the light load, so there is no resonant current produced at the light-load points. Because of the six-step SVM, during certain time intervals of the waveforms, there is no resonant current generated even though the amplitude of the load current is quite high.



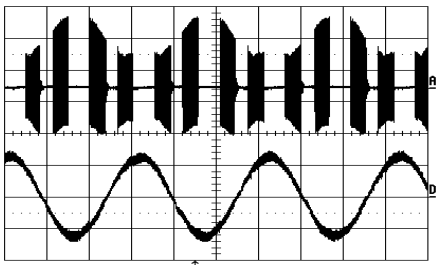
(a) S=1920 rpm, T=50 N-m.



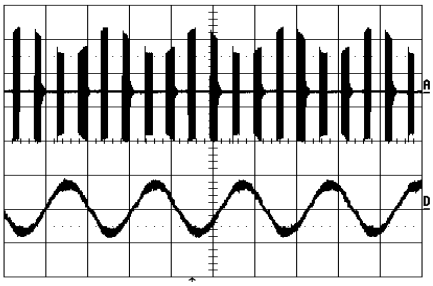
(b) S=3770 rpm, T=5 N-m.



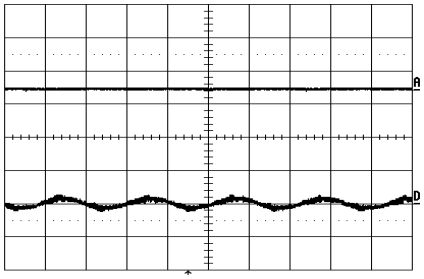
(c) S=3770 rpm, T=50 N-m.



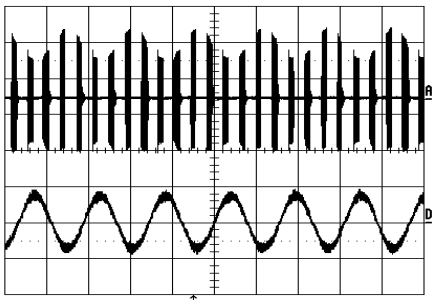
(d) S=3770 rpm, T=101 N-m.



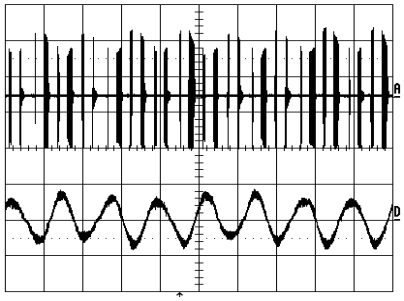
(e) S=5680 rpm, T=42 N-m.



(f) S=5680 rpm, T=6 N-m.



(g) S=7550 rpm, T=31 N-m.



(h) S=9470 rpm, T=20 N-m.

Fig. 3.35. Measured current waveforms of 3-swich ZCT inverter at steady state:

Channel D (bottom): the load current (200A/div).

Channel A (top): the resonant current (200A/div).
Time: 5ms/div.

All the waveforms presented for the hard-switching and soft-switching inverters indicate that each developed inverter operate correctly on the dynamometer. Therefore, efficiency levels of different switching topologies can be directly compared.

3.4.3. Efficiency and THD Comparison

Table 7.3 lists the measured efficiency data for the hard-switching inverter and three kinds of soft-switching inverters. Based on this table, the efficiencies at different operating points are shown in the graph, as shown in Fig. 7.1. It can be seen from Fig. 7.1 that a very small efficiency difference exists between the hard-switching inverter and the soft-switching inverters. Actually, the efficiency difference is within the margin of measurement error. The current sensor LT-300 from LEM company is used to sample the DC-link current and two-phase AC load current. The accuracy of LT-300 is ±0.5%. The voltage-sensing channel of the power analyzer is about ±0.1%. Consequently, both the input DC power measurement and the three-phase output power measurement are subject to an error margin of ±0.6%. The detailed derivation of efficiency error is given in Equations 7.1 to 7.3. Δ_{Po} represents the measurement error of the three-phase output power, and Δ_{Pin} represents the measurement error of the inverter DC input power. P_o and P_{in} stand for the actual output power and input DC power, respectively. $P_{o\text{-}m}$ and $P_{in\text{-}m}$ stand for the measured output power and input DC power, respectively.

$$\eta = \frac{P_o}{P_{in}} \tag{3.4}$$

$$\eta_m = \frac{P_{o\_m}}{P_{in\_m}} = \frac{P_o(1+\Delta_{po})}{P_{in}(1+\Delta_{pin})} \tag{3.5}$$

$$\eta_m - \eta = \frac{P_{o\_m}}{P_{in\_m}} - \frac{P_o}{P_{in}} = \frac{P_o(1+\Delta_{po})}{P_{in}(1+\Delta_{pin})} - \frac{P_o}{P_{in}} = \eta\frac{\Delta_{po}-\Delta_{pin}}{(1+\Delta_{pin})} \tag{3.6}$$

Equation (3.6) expresses the deviation of calculated efficiency. It suggests that if the polarity of Δ_{Po} and Δ_{Pin} is opposite, the error of the resulting efficiency value can be the sum of the absolute value of Δ_{Po} and Δ_{Pin}. Therefore, the accuracy of the efficiency calculation, based on the input DC power and three-phase output power measurement, can be ±1.2% at the worst case.

Error! Reference source not found. and Table 3-1 basically suggest that the efficiency difference between hard-switching and soft-switching inverters is within the margin of measurement error. It can be concluded that the evaluated soft-switching inverters do not make a remarkable improvement in efficiency over the hard-switching inverter for EV applications at 10 kHz. There are several reasons for this.

The main IGBT devices are not optimized for soft-switching operation. It is known that the switching loss at 10 kHz is less than 300 W when using 7.4 Ω as the gate-driver resistor. The switching loss is less than one-third of the conduction loss. In order to maximize the efficiency benefit of the soft-switching operation, the inverter devices should have a low conduction loss and higher switching loss. However, almost all commercial IGBTs are designed to reduce the switching loss as the conduction voltage drop increases.

The efficiency comparison also tells that the loss of the auxiliary circuit in the soft-switching inverters cannot be ignored. The switching loss of the main device is reduced, and this has been verified by the device switching waveforms presented in the previous chapters. However, the auxiliary components in the soft-switching inverters, such as the active semiconductor devices and passive components, are not ideal and they incur losses too. The auxiliary component's design and selection is important to achieve an overall improvement in inverter efficiency.

Otherwise, the loss reduction of the main devices is offset by the additional conduction loss or switching loss in the auxiliary components.

Table 3-2 and Fig. 3.36 show the motor efficiency under the operation of different inverters. Similar to the inverter efficiency comparison, the motor efficiency difference at most points is also within the margin of measurement error. Soft-switching inverters do not offer a noticeable improvement in motor efficiency. On the other hand, these soft-switching inverters do not impair the motor efficiency either. Although the THD of the motor current is given in Table 3-3 and Fig. 3.37, it seems that there is no clear indication of the relationship between the motor current THD and motor efficiency. It is noted that the fundamental frequency of the inverter output is less than 100 Hz when the speed is below 7,550 rpm. Since the power analyzer calculates only up to 99^{th} harmonic number, for the operating points where the speed is below 7,550 rpm, the switching-frequency ripple (10 kHz) of the current is not included for the THD calculation.

Table 3-4 and Fig. 3.38 show the system efficiency comparison based on the obtained inverter and motor efficiency comparison. Due to the similar inverter and motor efficiency of the hard-switching and soft-switching inverters, the difference of the system efficiency is also within the margin of measurement error.

Table 3-1. Inverter efficiency comparison of soft-switching inverters.

Speed [rpm]	Torque [N-m]	Hard-sw. Efficiency [%]	6-switch ZCT		ARCP ZVT		3-switch ZCT	
			Eff. [%]	Improvement	Eff. [%]	Improvement	Eff. [%]	Improvement
1,923.5	50.7	93.46	93.20	**-0.26**	93.42	**-0.05**	93.18	**-0.29**
1,921.0	80.9	93.28	93.45	**0.17**	93.08	**-0.21**	93.26	**-0.03**
3,770.4	5.2	91.84	90.67	**-1.17**	90.81	**-1.04**	90.97	**-0.88**
3,770.9	20.7	95.52	95.24	**-0.28**	95.22	**-0.30**	95.25	**-0.27**
3,772.5	50.8	96.41	96.21	**-0.20**	96.23	**-0.18**	96.20	**-0.21**
3,772.0	101.3	96.20	96.18	**-0.02**	95.95	**-0.25**	96.03	**-0.17**
5,629.0	5.9	94.02	93.41	**-0.61**	93.36	**-0.66**	93.43	**-0.59**
5,629.0	12.1	95.92	95.54	**-0.39**	95.58	**-0.35**	95.58	**-0.35**
5,630.1	41.9	96.65	96.49	**-0.16**	96.57	**-0.08**	96.62	**-0.04**
7,546.6	10.1	96.40	96.03	**-0.37**	96.06	**-0.34**	96.14	**-0.26**
7,549.9	15.1	96.49	96.28	**-0.21**	96.28	**-0.21**	96.36	**-0.12**
7,550.4	31.9	96.66	96.49	**-0.17**	96.53	**-0.13**	96.55	**-0.11**
9,463.2	13.0	96.53	96.33	**-0.20**	96.35	**-0.18**	96.38	**-0.15**
9,464.3	20.1	96.68	96.42	**-0.26**	96.52	**-0.16**	96.50	**-0.18**

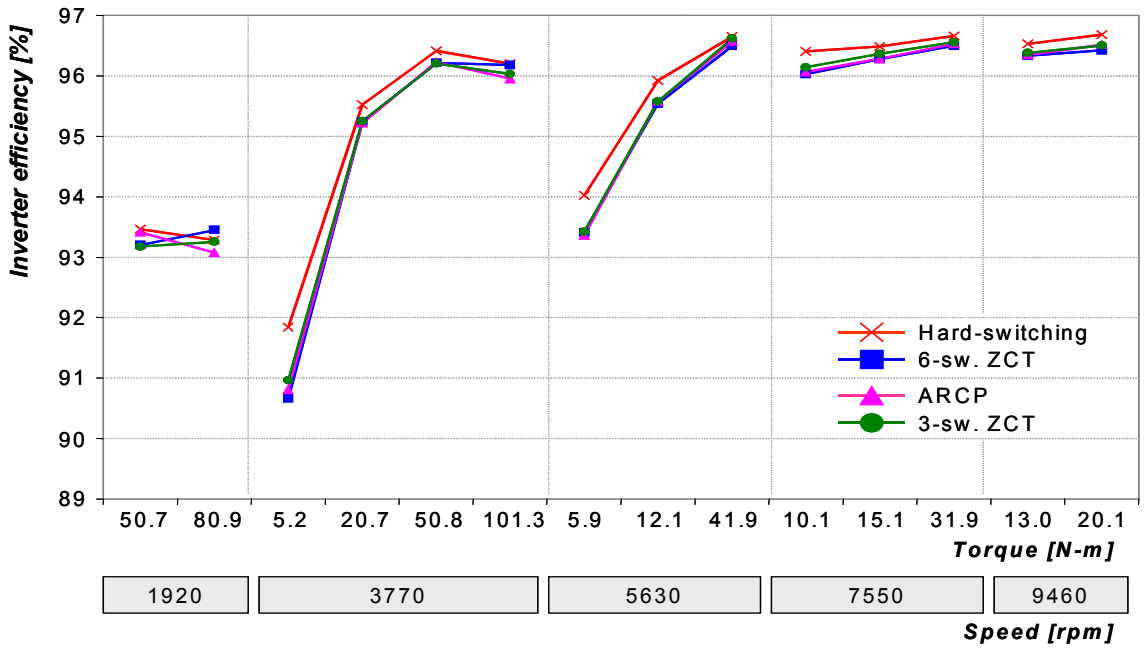


Table 3-2. Motor efficiency comparison of soft-switching inverters.

Speed [rpm]	Torque [N-m]	Hard-sw. Efficiency [%]	6-switch ZCT		ARCP ZVT		3-switch ZCT	
			Eff. [%]	Improvement	Eff. [%]	Improvement	Eff. [%]	Improvement
1,923.5	50.7	85.59	85.29	**-0.30**	85.27	**-0.32**	85.43	**-0.16**
1,921.0	80.9	82.56	82.37	**-0.19**	82.62	**0.06**	82.18	**-0.39**
3,770.4	5.2	76.45	75.42	**-1.02**	75.54	**-0.91**	75.16	**-1.28**
3,770.9	20.7	87.78	87.50	**-0.28**	87.81	**0.03**	87.70	**-0.09**
3,772.5	50.8	89.33	89.10	**-0.23**	89.24	**-0.08**	88.86	**-0.47**
3,772.0	101.3	86.86	86.43	**-0.43**	86.83	**-0.03**	86.13	**-0.73**
5,629.0	5.9	80.94	79.17	**-1.77**	81.00	**0.06**	79.13	**-1.81**
5,629.0	12.1	87.32	87.12	**-0.20**	87.28	**-0.04**	86.56	**-0.76**
5,630.1	41.9	88.88	88.48	**-0.40**	89.10	**0.22**	88.95	**0.07**
7,546.6	10.1	87.25	86.30	**-0.95**	87.34	**0.09**	86.33	**-0.92**
7,549.9	15.1	89.06	88.02	**-1.03**	88.78	**-0.27**	88.15	**-0.90**
7,550.4	31.9	87.55	87.15	**-0.40**	87.78	**0.23**	87.07	**-0.47**
9,463.2	13.0	87.64	86.28	**-1.36**	87.78	**0.14**	87.06	**-0.58**
9,464.3	20.1	87.17	86.33	**-0.84**	87.19	**0.02**	86.53	**-0.64**

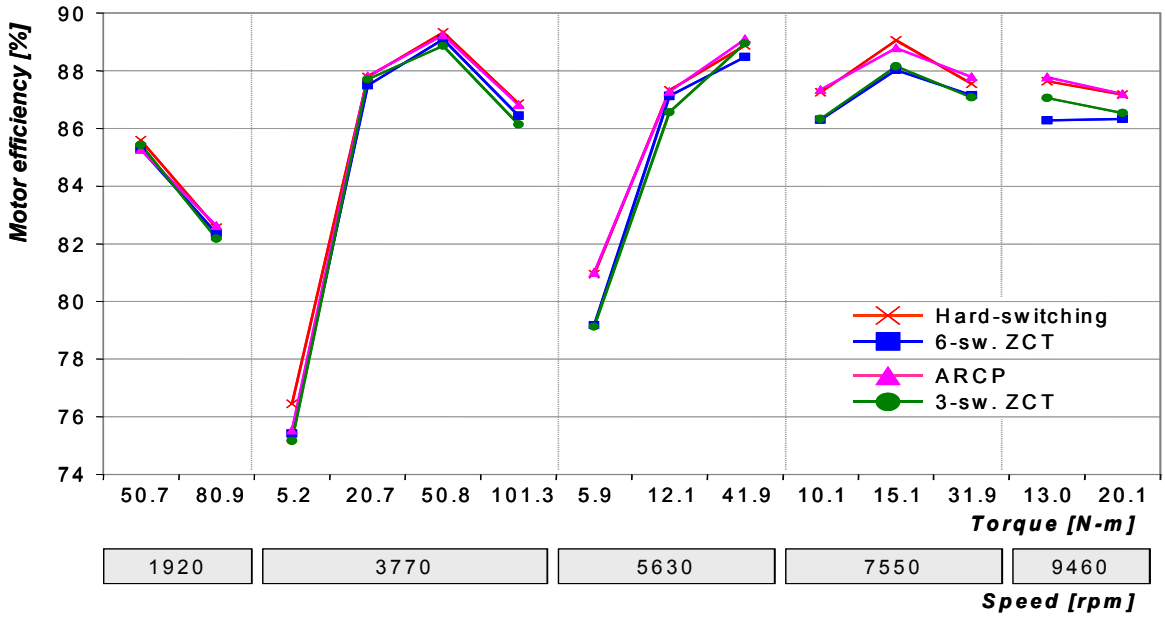


Fig. 3.36. Motor efficiency comparison of soft-switching inverters.

Table 3-3. Output current THD comparison of soft-switching inverters.

Speed [rpm]	Torque [N-m]	Hard-sw. current THD [%]	6-switch ZCT		ARCP ZVT		3-switch ZCT	
			THD [%]	Improvement	THD [%]	Improvement	THD [%]	Improvement
1,923.5	50.7	13.74	13.34	**0.40**	12.94	**0.80**	12.04	**1.70**
1,921.0	80.9	11.23	13.28	**-2.05**	10.14	**1.10**	10.36	**0.87**
3,770.4	5.2	38.61	27.55	**11.06**	27.95	**10.67**	26.86	**11.75**
3,770.9	20.7	22.32	19.55	**2.77**	18.71	**3.61**	19.29	**3.02**
3,772.5	50.8	14.06	14.21	**-0.15**	12.70	**1.36**	13.10	**0.96**
3,772.0	101.3	17.33	17.51	**-0.18**	15.58	**1.76**	17.89	**-0.56**
5,629.0	5.9	34.08	25.17	**8.91**	25.37	**8.71**	25.08	**8.99**
5,629.0	12.1	26.88	21.94	**4.94**	21.74	**5.14**	21.65	**5.22**
5,630.1	41.9	12.42	11.64	**0.78**	10.99	**1.43**	10.98	**1.44**
7,546.6	10.1	26.93	20.43	**6.50**	20.81	**6.12**	20.01	**6.92**
7,549.9	15.1	20.09	17.08	**3.01**	16.62	**3.47**	16.41	**3.68**
7,550.4	31.9	12.77	11.35	**1.43**	11.26	**1.52**	10.72	**2.05**
9,463.2	13.0	29.59	28.96	**0.63**	27.89	**1.70**	28.60	**0.99**
9,464.3	20.1	20.90	20.38	**0.51**	20.86	**0.04**	19.85	**1.04**

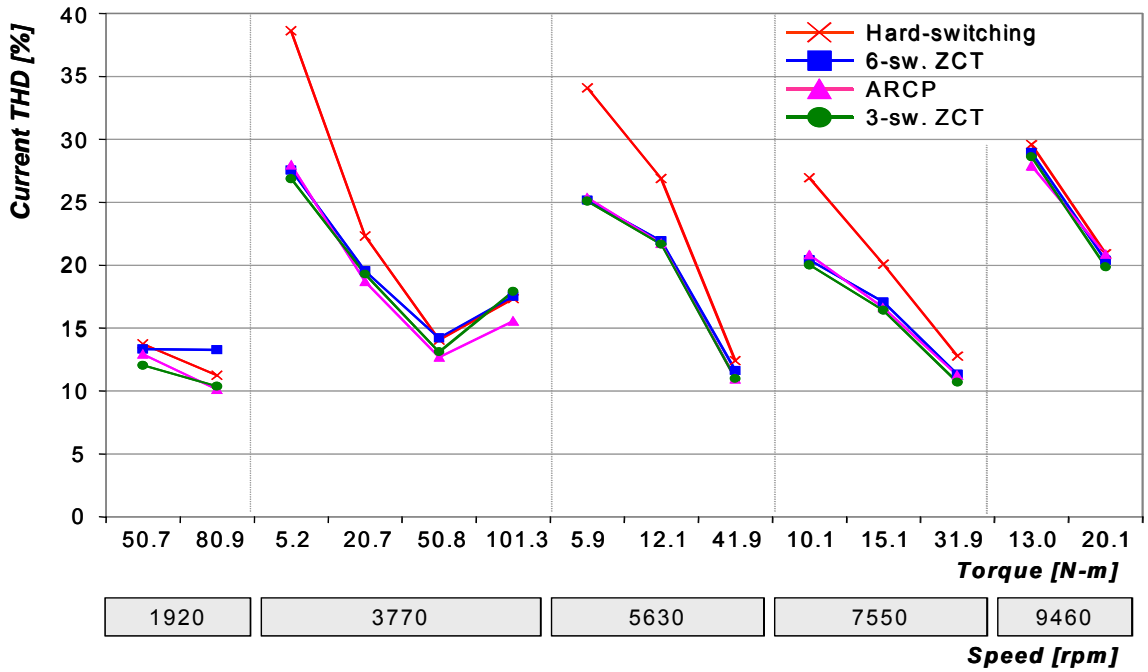


Fig. 3.37. Output current THD comparison of soft-switching inverters.

Table 3-4. System efficiency comparison of soft-switching inverters.

Speed [rpm]	Torque [N-m]	Hard-sw. Efficiency [%]	6-switch ZCT		ARCP ZVT		3-switch ZCT	
			Eff. [%]	Improvement	Eff. [%]	Improvement	Eff. [%]	Improvement
1,923.5	50.7	79.99	79.49	**-0.50**	79.65	**-0.34**	79.60	**-0.40**
1,921.0	80.9	77.02	76.98	**-0.04**	76.90	**-0.11**	76.63	**-0.38**
3,770.4	5.2	70.21	68.38	**-1.83**	68.59	**-1.62**	68.37	**-1.83**
3,770.9	20.7	83.85	83.33	**-0.52**	83.62	**-0.23**	83.53	**-0.32**
3,772.5	50.8	86.12	85.72	**-0.40**	85.88	**-0.24**	85.48	**-0.63**
3,772.0	101.3	83.56	83.13	**-0.43**	83.31	**-0.25**	82.71	**-0.85**
5,629.0	5.9	76.10	73.96	**-2.15**	75.62	**-0.48**	73.93	**-2.17**
5,629.0	12.1	83.76	83.24	**-0.52**	83.42	**-0.34**	82.73	**-1.03**
5,630.1	41.9	85.90	85.37	**-0.52**	86.04	**0.14**	85.94	**0.04**
7,546.6	10.1	84.11	82.87	**-1.24**	83.90	**-0.21**	83.00	**-1.11**
7,549.9	15.1	85.93	84.74	**-1.18**	85.48	**-0.45**	84.95	**-0.98**
7,550.4	31.9	84.63	84.10	**-0.53**	84.74	**0.11**	84.07	**-0.55**
9,463.2	13.0	84.60	83.11	**-1.49**	84.57	**-0.03**	83.91	**-0.69**
9,464.3	20.1	84.28	83.24	**-1.04**	84.16	**-0.12**	83.50	**-0.77**

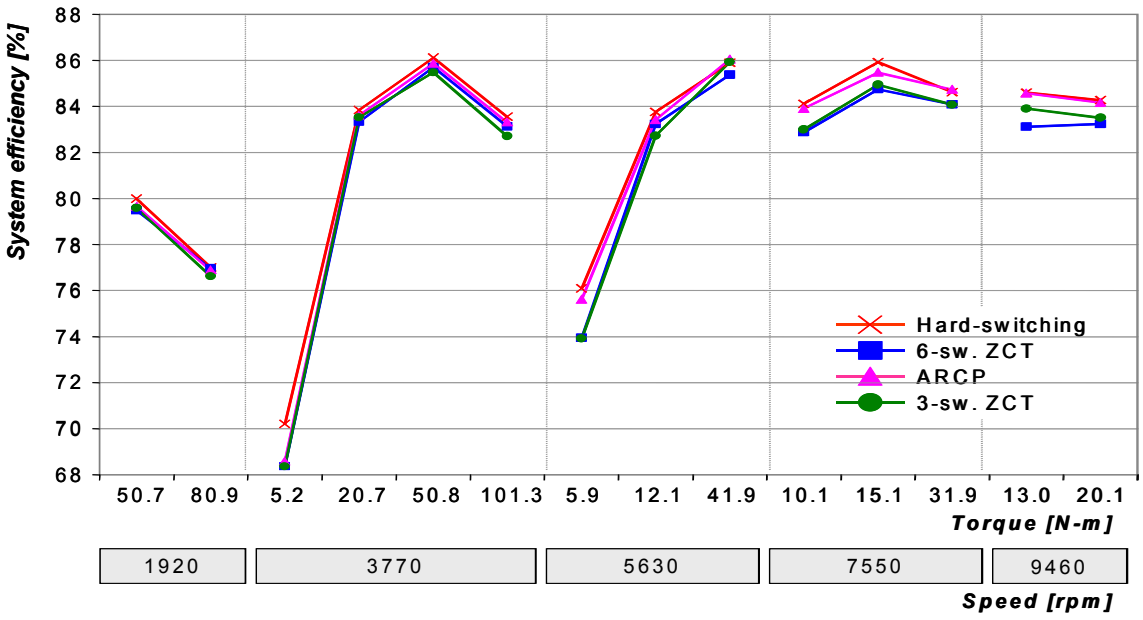


Fig. 3.38. System efficiency comparison of soft-switching inverters.

3.5. Conducted EMI Noise Evaluation

3.5.1. Conducted EMI Measurement Setup

Fig. 3.39 illustrates the test setup, and Fig. 5.2 depicts the actual setup with the dynamometer. The metal bench of the dynamometer, which stands on the floor of the CPES laboratory, is used as the ground plane. The inverter chassis is connected to the ground plane via a copper sheet. Two LISNs are used to measure the conductive EMI. The LISNs used in the test are the single-line type, and are screwed onto the bench. They are connected in series to the positive and negative DC rails. The HP 4195A spectrum analyzer is used to measure the noise emission of the inverter. The noise data captured by the spectrum analyzer is transferred to a computer via the HPIB interface. In the computer, through the HP VEE Evaluation software, the noise data are saved in a spreadsheet format. Then, they are processed using MS Excel software, and the EMI spectra are plotted.

To measure the total EMI noise generated by the inverter, the output of one LISN (either the one inserted in the positive rail or the one inserted in the negative rail) is connected to the spectrum analyzer; the output of the other LISN is terminated with a 50Ω feed-through resistor, which functions as a dummy load. To measure the common- mode (CM) noise, outputs of the LISNs are connected to a differential-mode rejection network (DMRN). Likewise, to measure the differential-mode (DM) noise, a common-mode rejection network (CMRN) is used.

Noises of the low-frequency range (10 kHz~300 kHz) and high-frequency range (100 kHz~30 MHz or 300kHz~30 MHz) are measured. For the low-frequency measurement, the resolution bandwidth is set at 300 Hz. For the high-frequency measurement, the resolution bandwidth is set

at 10 kHz. To decrease measurement fluctuations, the video filter of the spectrum analyzer is turned on. Thus, the spectrum analyzer performs four measurements and displays the average of the four measurements as the results. In addition, background noises during the tests are also measured.

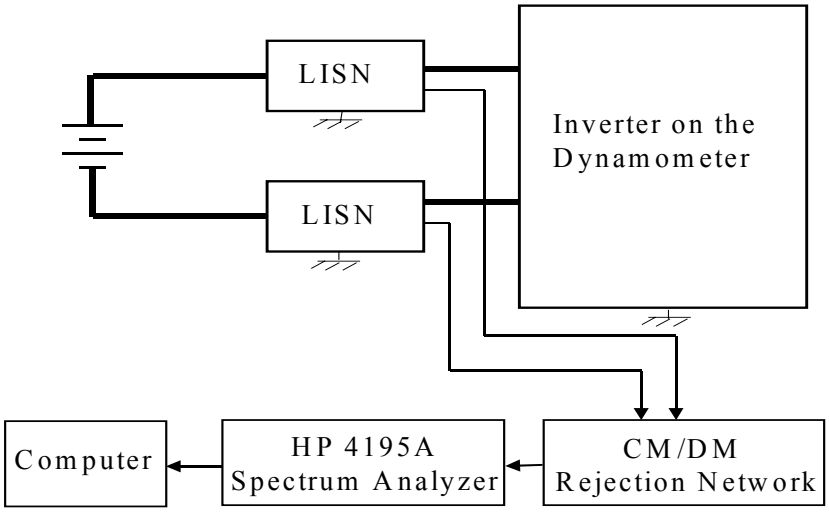


Fig. 3.39. Illustration of the EMI test setup.

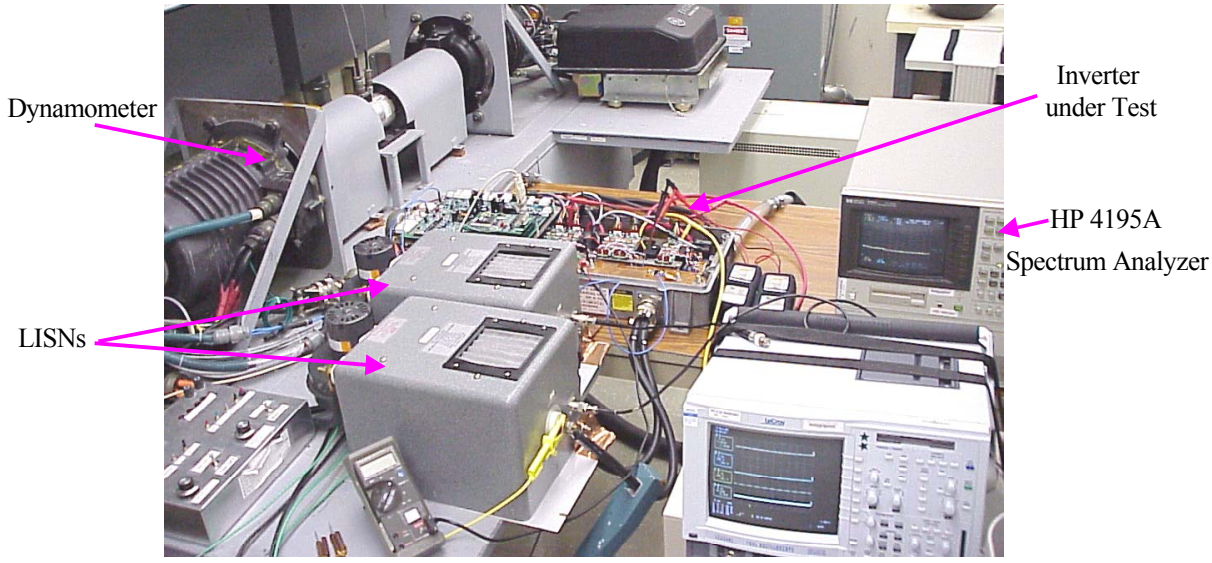


Fig. 3.40. EMI test setup with the dynamometer.

3.5.2. Conducted EMI Noise Comparison

EMI tests have been conducted using the hard-switching inverter and the three different soft-switching inverter topologies on the dynamometer. Fig. 3.41 shows the background EMI noise, which indicates that all the inverters are tested under a similar EMI environment. Since the inverter layout potentially impacts the EMI noise spectrum, the EMI noise of the hard-switching inverters obtained by disabling the auxiliary switches is also measured, as shown in Fig. 3.42. At most of the frequencies above 1 MHz, the noise difference is less than 2 dB among the different layouts. Therefore, the specified hard-switching inverter (based on the ARCP ZVT inverter) can provide the baseline EMI noise information for this frequency region. The EMI noise of around a few-hundred kHz will be compared between the soft-switching inverter and the corresponding hard-switching inverter based on the same layout.

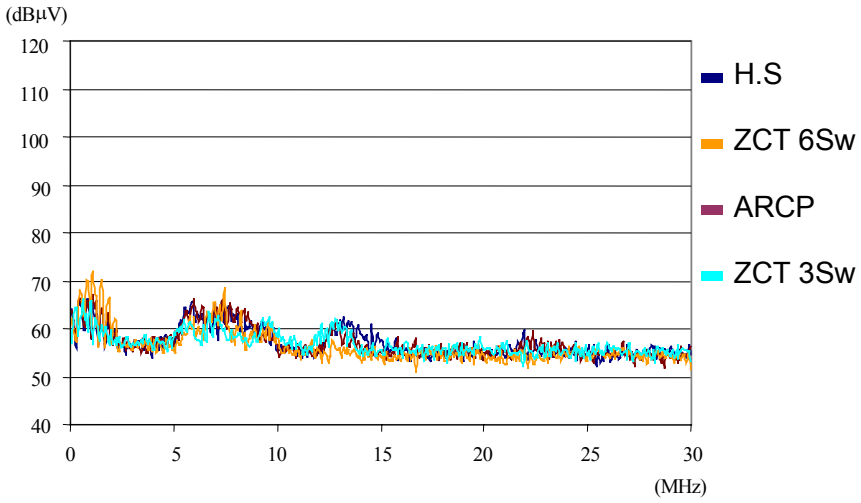


Fig. 3.41. Background noise of the tested inverters.

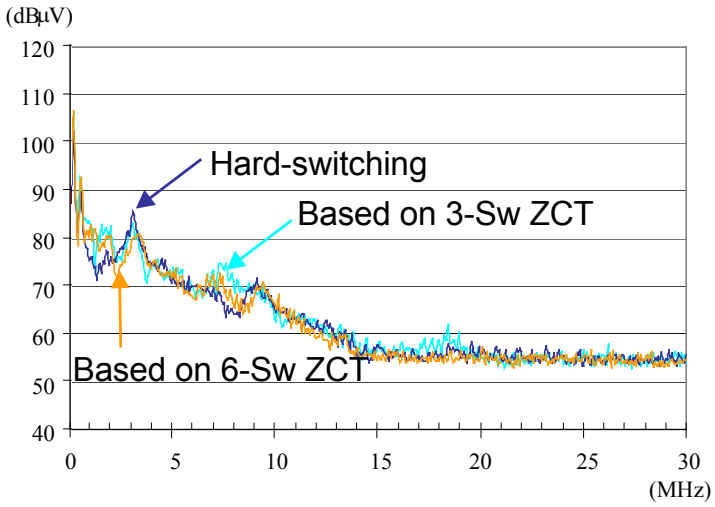


Fig. 3.42. EMI noise based on inverter disabling soft-switching operation.

Fig. 3.43 shows the total EMI noise measurement at the operating point of 101 N-m/3,780 rpm. Compared with the hard-switching inverter, the six-switch ZCT inverter shows a 5dB reduction around 3 MHz and a similar level of EMI noise at the rest of the frequency range. The three-switch ZCT inverter exhibits a 2dB reduction around 3 MHz and a 4dB attenuation from 8 to 9 MHz. Meanwhile, the three-switch ZCT inverter shows higher EMI noise than the hard-switching inverter at frequencies above 10 MHz, which is 4dB higher than most of that frequency region. Figure 3.35 also indicates that the ARCP ZVT inverter achieves about 10dB lower EMI noise than the hard-switching inverter from 3 to 5 MHz and 5dB lower EMI noise from 8 to 12 MHz. Around 23 MHz, the ARCP inverter has 3dB higher EMI noise than the hard-switching inverter. These observations suggest that only the ARCP ZVT inverter achieves substantial EMI noise reduction between 3 to 12 MHz.

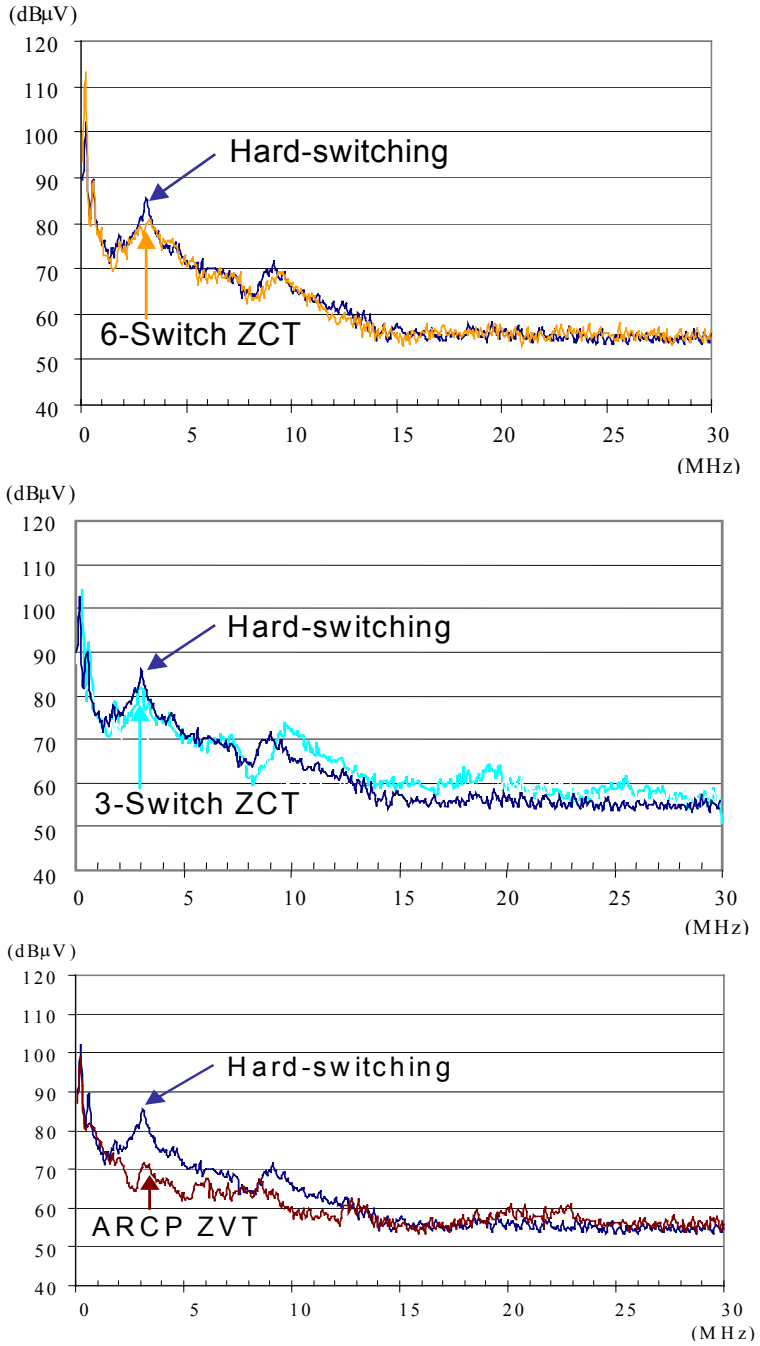
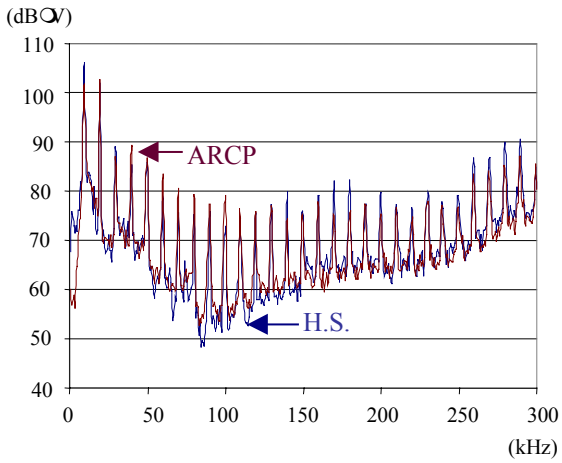


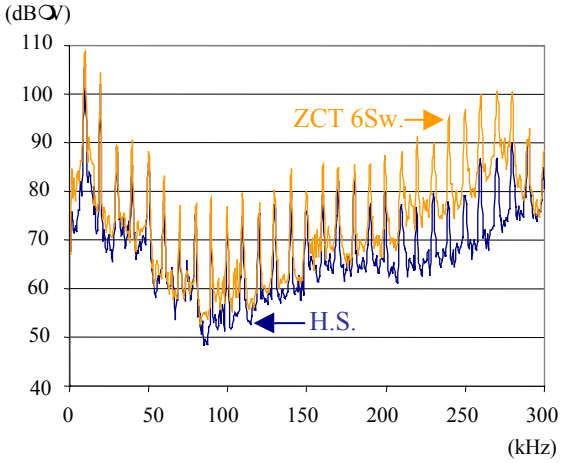
Fig. 3.43. Total EMI noise comparison.

The more detailed EMI spectra at the low frequency range from 1 kHz to 300 kHz are shown in Fig. 3.44 for all the inverters. Usually the EMI measurement data needs to be compensated at the frequency below 150 kHz since the LISN impedance shows the decrease. Since the

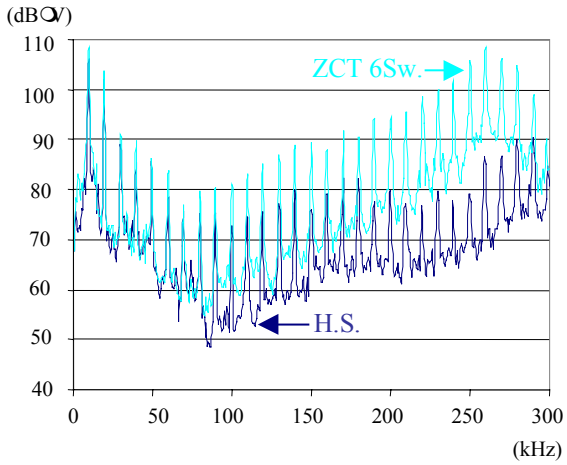
comparison among the different inverters is of more interest than the absolute EMI noise level characterization, the measurement results are directly shown without any compensation. The ARCP inverter almost exhibits the same EMI performance as the hard-switching inverter at the frequency from 1 kHz to 300 kHz except it has slightly lower EMI noise between 200 kHz and 250 kHz. It can be seen from Fig. 3.44(b) and (c), the ZCT inverters shows the much higher EMI spectra between 200 kHz and 250 kHz. The ZCT inverter with 3 switches shows the highest peak of EMI noise. Since the resonant frequency of the auxiliary L-C circuit is designed around this frequency range, it contributes additional EMI noise compared to the hard-switching inverter. It is also clearly seen that due to the PWM control, the hard-switching, the ZCT with 6 switches, the ARCP and the ZCT with 3 switches all have the discrete noise peak at the multiple switching frequency.



(a)



(b)



(c)

Fig. 3.44. Total noises of the different inverters at the low frequency range: (a) ARCP, (b) Six-switch ZCT and (c) Three-switch ZCT.

To further characterize the EMI performance, the differential mode (DM) and common mode (CM) EMI noise are separated by applying the corresponding noise rejection network for the ARCP inverter and the hard-switching inverter. As seen from Fig. 3.44, the DM noise is dominant in the frequency range from 100 kHz up to 1 MHz in the hard-switching inverter. It is usually true in the PWM controlled hard-switching inverter that the DM noise dominates the very narrow low frequency band of the span from 150 kHz to 30 MHz, over which normal EMI standards regulate. Fig. 3.46 shows the EMI spectra of the ARCP inverter. Compared with the hard-switching inverter, the ARCP inverter significantly reduces both DM and CM noise from 2 MHz to 10 MHz. Actually this can be qualitatively explained by the soft-switching operation of the ARCP inverter. Since the ZVS turn-on of the main device is achieved in the ARCP inverter, the diode reverse recovery current of main device is much reduced. The major part of DM current, especially at a few MHz, is the result of the diode reverse recovery current and its associated ringing between the layout parasitic inductance and device junction capacitor. Consequently, the ARCP inverter can substantially reduce the DM noise. The rate of voltage

change of the main devices is also effectively reduced in the ARCP inverter. The resultant CM noise is expected to be smaller. Although the rate of voltage change of the auxiliary devices is not changed by the soft-switching operation, the auxiliary devices only block half of Vdc. The overall effect is the CM noise is reduced, as confirmed by Fig. 3.46.

Fig. 3.47 shows the EMI noise feature of the hard-switching inverter at the No. 1 operating point. Compared with Fig. 3.45, the total noise, DM and CM noise spectra pattern almost has no change. Only the DM noise level at the heavier load, No. 6 point, is slightly increased compared to that at the light load, No. 1 point.

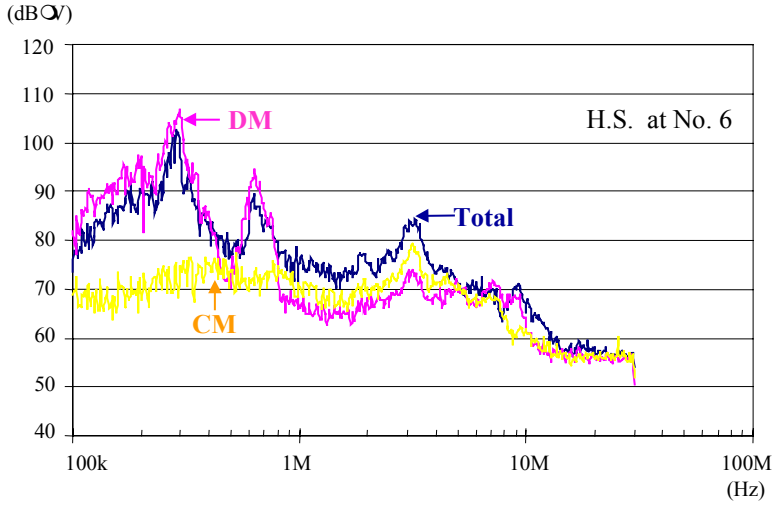


Fig. 3.45. EMI noise of the hard-switching inverter at No. 6 operating point.

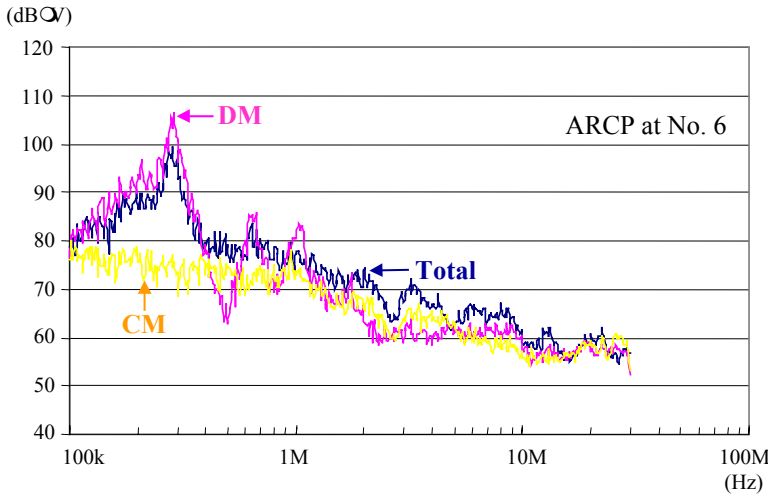


Fig. 3.46. EMI noise of the ARCP inverter at No. 6 operating point.

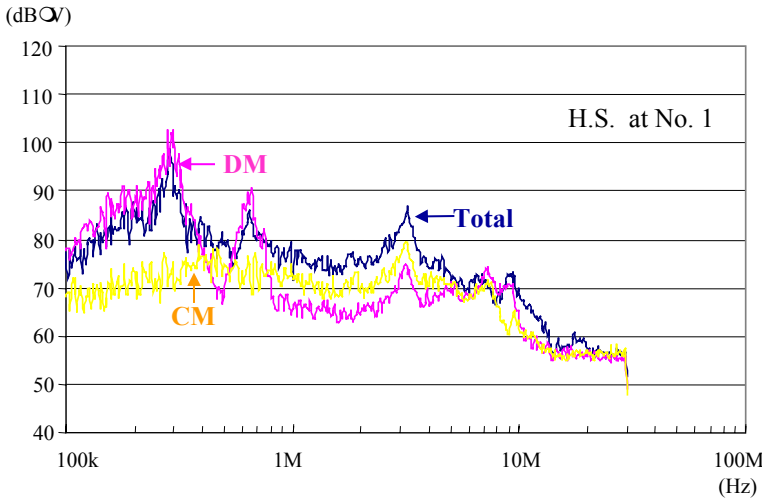


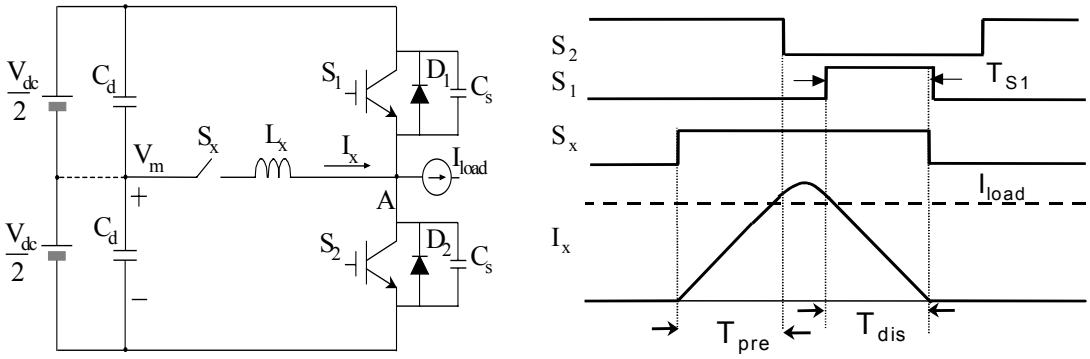
Fig. 3.47. EMI noise of the hard-switching inverter at No. 1 operating point.

3.6. Minimum Pulse Width SVM for Soft-switching Inverters

As explained previously, the minimum pulse width is required for the soft-switching inverters. Therefore, the PWM control signals will be eliminated before being sent to the gate driver of the devices if their width is below than the specified minimum pulse width.

As an example of ZVT inverter, the auxiliary resonant commutated pole inverter (ARCPI) in one leg configuration is shown in Fig. 3.48(a). The main devices are S_1 and S_2. The soft-switching operation is briefly illustrated in Fig. 3.48(b). The commutation from D_2 to S_1 is explained as follows. At first, S_x is turned on and the inductor current I_x increases linearly. After the duration of T_{pre} (when I_x is above the load current level), S_2 is turned off. The resonance of L_x and C_s begins and decreases the voltage of S_1 to zero. S_1 is turned on at ZVS. After that, the inductor current I_x is discharged to zero within the duration of T_{dis}. Then S_x can be turned off under a zero-current condition. The on time of S_1 has to be longer than T_{dis} and on the other hand, the on time of S_2 needs to be longer than T_{pre}. Otherwise, the inductor current I_x cannot be reset to zero. As a result, the hard-switching turn-off of S_x may destroy the device or cause more switching loss. Therefore, there has to be the limitation of the minimum pulse width (noted as T_{min} hereafter) for the PWM signals of main devices. The ZCT inverters also require T_{min} for the similar reason of resetting the energy storage component. Therefore, for the load side soft-switching inverters, T_{min} is generally required for both positive and negative pulses of main device gate signals. This leads to an increase of total harmonic distortion (THD) of the load current and a voltage conversion ratio loss. The higher the switching frequency is, the worse low frequency harmonic the load current contains. In the past, the circuit designers constrained the values of the auxiliary inductor and capacitor to limit the resonant transition time. However, there is always a considerable amount of the transition time due to many intertwined design factors such as di/dt, dv/dt, the peak current stress and the switching loss reduction.

A simple graphic method is presented to aid identifying the space vector modulation (SVM) scheme, which has the maximum pulse width (MPW). The proposed MPW SVM scheme can alleviate the negative effects of Tmin in the three-phase load side soft-switching inverters.



(a) (b)

Fig. 3.48. Illustration of minimum pulse requirement in ARCP:
(a) One leg configuration and (b) Soft-switching control timing.

3.6.1. Analysis of Narrow Pulses in SVM Control

Each phase of the three-phase inverter power stage can generate two different normalized voltages: +1 when the upper switch is on, and –1 when the lower one is on. The base value of the voltage is half of the Vdc. Thus, totally 2^3=8 possible different combinations of output voltages exist. Using the transformation matrix defined in Equation 3.7, three phase quantities are transformed into eight voltage vectors in a-b plane, expressed in Equation 3.8.

$$T = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{3.7}$$

$$\vec{V} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = T \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}. \tag{3.8}$$

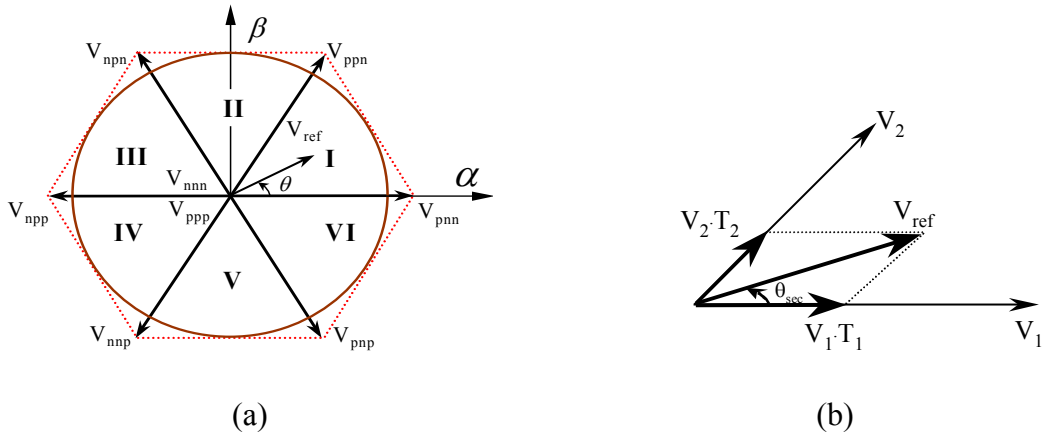


Fig. 3.49. Space voltage vectors: (a) Eight voltage vector distributions and (b) adjacent vectors to compose the reference vector.

The distribution of the space voltage vectors is shown in Fig. 3.49(a). The p and n indexes correspond to the voltage state of each phase following the sequence of phase A, B and C. For example, Vpnn represents VA=Vdc/2 and VB=VC=_Vdc/2. Using Equations 3.7 and 3.8, it is easy to know $\left|V_{pnn}\right| = V_{dc}$. The length of the basic non-zero vectors is the same. Furthermore, there are six sectors formed by the six basic non-zero vectors. Generally, two adjacent basic vectors realize the reference vector Vref with their duration determined in such a way that the resulting average output voltage vector coincides with the reference vector. Fig. 3.49(b) shows the typical vector decomposition, where V1 and V2 stand for the starting and ending vector of one sector, respectively. There is 60 degree from V1 to V2 anti-clockwise. Therefore, the duration of non-zero vectors of V1 and V2, noted as T1 and T2, can be expressed by Equations 3.9 and 3.10. The modulation index m is defined as $m = \left|V_{ref}\right| / \left|V_{pnn}\right|$ and Ts is the switching period. θsec represents the angle between Vref and V1.

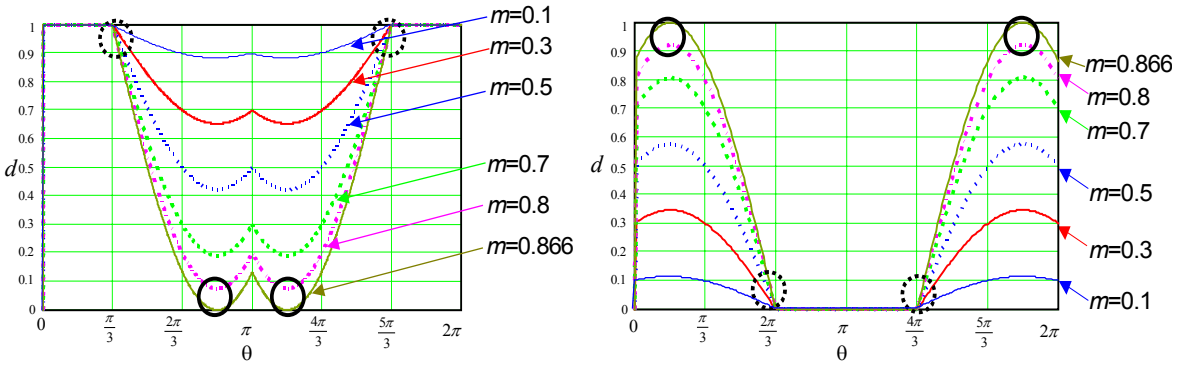
$$T_1 = T_s \cdot m \sin(60^\circ - \theta_{sec}) / \sin 60^\circ . \tag{3.9}$$

$$T_2 = T_s \cdot m \sin\theta_{sec} \big/ \sin 60^\circ . \tag{3.10}$$

Obviously the total zero vector duration can be given by:

$$T_{zero} = T_s - T_1 - T_2 = T_s \cdot (1 - m\cos(\theta - 30^\circ)) \big/ \sin 60^\circ \tag{3.11}$$

How to distribute the time between Vnnn (V0) and Vppp (V7) can lead to different SVM schemes. For convenience of the analysis, we define the duration ratio of V7 to the total zero vector duration as λ. The past research efforts [C21] have verified that the conventional SVM schemes with λ=0, λ=0.5, λ=1, or λ=0.5·(1+sgn(sin3θ)) exhibit reasonably low THD and easy implementation, where q represents the angle of the reference vector corresponding to Vpnn (V4). To reveal the narrow pulses of PWM signals, the duty cycle of the upper switch of phase A (also noted as phase duty cycle) under two of these SVM schemes are shown in Fig. 3.50. It can be seen that both SVM schemes introduce the narrow pulses indicated by the phase duty cycle close to either one or zero.



(a) (b)

Fig. 3.50. Phase duty cycle for SVM schemes: (a) λ=1 and (b) λ=0.

From the modulation index viewpoint two kinds of short pulses are observed in Fig. 3.50. The dotted circles indicate that the existence of narrow pulse is independent of the modulation index m. The solid circles correspond the narrow pulses more dependent on m. From the voltage sector

point of view, the narrow pulses locate around either the boundary or the center of some voltage sectors. If these two SVM schemes are used for soft-switching inverters, it is expected that some PWM pulses will be eliminated due to the minimum pulse limitation required by the soft-switching operation. Therefore, the popular SVM schemes used in the hard-switching inverters may not be suitable for soft-switching inverters. It is desired to derive a SVM scheme realizing the widest pulse of the PWM signals to alleviate the problem of minimum pulse deletion.

3.6.2. Maximum Pulse Width SVM Control

Based on the space vector plane, the possible vector combinations to synthesize the reference vector located in the group of sector I, III and V are graphically shown in Fig. 3.51(a). The unchanged sequence of the shaded blocks emphasizes the common pulse pattern of the PWM waveforms of the inverter's output poles' voltage. When the pulse width is of concern, the analysis of any individual sector is valid for the other two sectors. Generally the SVM schemes can be classified into two types, one applying two types of zero vectors and the other utilizing only one type of zero vector in one switching cycle. If two kinds of zero vectors are used in one switching period, the width of the shortest positive pulse is the duration of V7 and width of the shortest negative pulse is the duration of V0. The largest pulse width of the narrow pulses (both positive and negative pulses) can be realized when the duration of V7 and V0 is set to be the same. Therefore the MPW SVM applying two zero vectors is the one with λ =0.5.

If only one type of zero vector is used, the total number of switching actions will be reduced due to modulating only two phases' devices. As seen from Fig. 3.51(a), when only Vo is used as the zero vector, the minimum pulse width is expressed by Equation 3.12. When only V7 is used as the zero vector, the minimum pulse width is given in Equation 3.13. Tpos_min stands for the

minimum width of the positive pulse and Tneg_min represents the minimum width of the negative pulse. Therefore, the SVM with maximum pulse width (MPW) should be obtained by Equation 3.14 through properly selecting the zero vectors.

$$\begin{cases} T_{pos\_min} = T_2 \\ T_{neg\_min} = T_{zero} \end{cases} \tag{3.12}$$

$$\begin{cases} T_{pos\_min} = T_{zero} \\ T_{neg\_min} = T_2 \end{cases}. \tag{3.13}$$

$$\max\{\min\{T_2, T_{zero}\}, \min\{T_{zero}, T_1\}\} \Big|_{select V_o or V_7} \tag{3.14}$$

From Equations 3.9 and 3.10, it is known that $T_1>T_2$ at $0^o<\theta_{sec}<30^o$ and $T_2>T_1$ at $30^o<\theta_{sec}<60^o$. In addition, the total zero vector duration is determined only by the modulation index *m*. By choosing different zero vectors, we can only change the minimum pulse width part, which is decided by the non-zero vector duration. Therefore, the proposed MPW SVM scheme applies V_7 at $0^o<\theta_{sec}<30^o$ and V_0 at $30^o<\theta_{sec}<60^o$ in the sectors I, III and V. The pulse patterns due to various vector combinations in Sector II, IV and VI are shown in Fig. 3.51(b). Following the similar derivation process used for sector I, III and V, the resultant MPW SVM control utilizes V_0 at $0^o<\theta_{sec}<30^o$ and V_7 at $30^o<\theta_{sec}<60^o$.

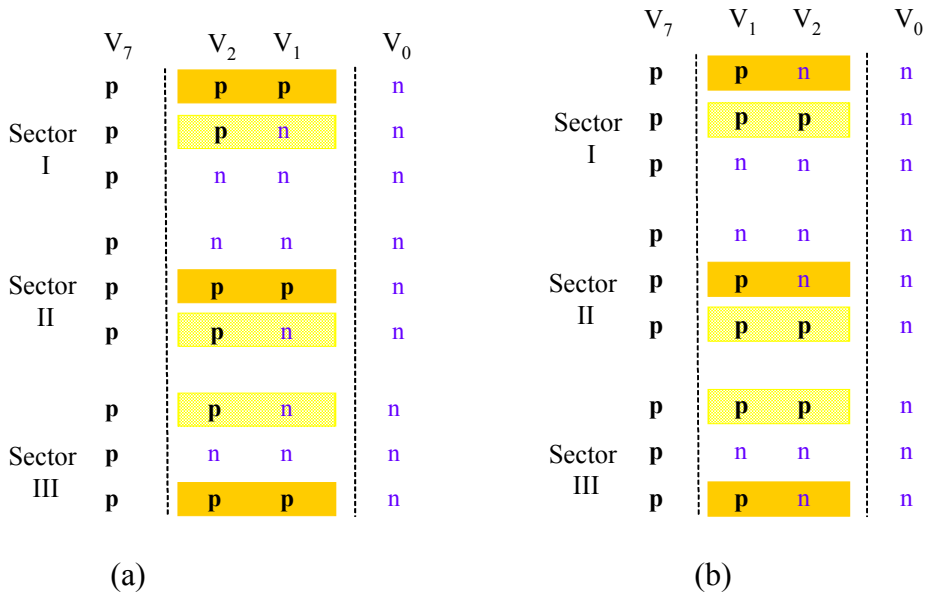


Fig. 3.51. Pulse pattern of inverter's output voltage: (a) sectors I, III and V and (b) sectors II, IV and VI.

The phase duty cycle of the proposed MPW SVM applying one zero vector in each switching cycle is shown in Fig. 3.52. Compared with that in Fig. 3.50, the short pulses around the sector boundary disappear. The minimum pulse width of PWM signals significantly increases for most range of the modulation index. It is also noted that when the modulation index (not in over-modulation range) approaches to the largest allowable value, 0.866, the relatively short pulses still exist near the center of certain voltage sectors. It is because the minimum pulse width of the gate signals near the center of the voltage sector is determined by the duration of the zero vector when the modulation index *m* is large. The zero vector duration becomes very short when the modulation index is quite large. Therefore the selection of the zero vectors can not have significant effects on improving the minimum pulse width under such a circumstance. Under the proposed MPW SVM control using one zero vector in each switching cycle, the shortest pulse width in each switching cycle can be expressed as follows.

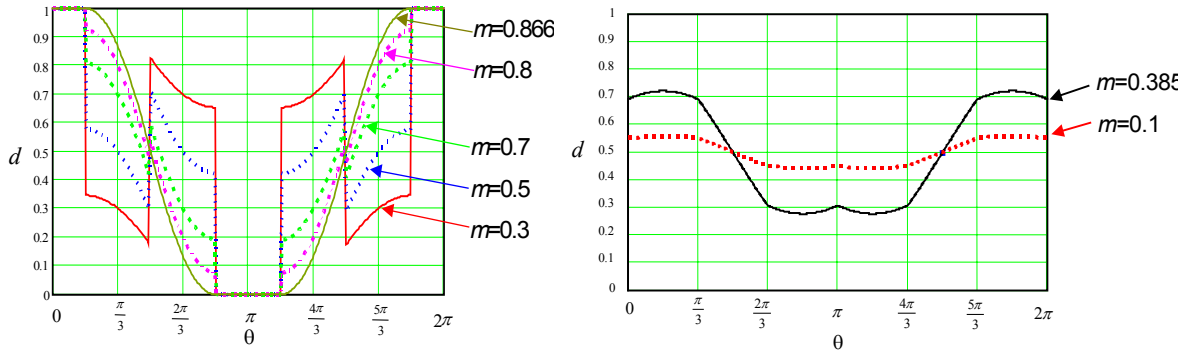
$$T_{min} = \begin{cases} \min\{T_1, T_{zero}\} & 0^o \le \theta_{sec} < 30^o \\ \min\{T_2, T_{zero}\} & 30^o \le \theta_{sec} < 60^o \end{cases} \tag{3.15}$$

Furthermore, the overall MPW SVM control needs to consider both cases of applying two zero vectors and applying only one zero vector. It is noticed that when the modulation index *m* is below certain value, half of the total duration of the zero vectors can be even longer than the duration of either non-zero vector. From Equations 3.9, 3.10 and 3.11, this derives the following relation.

$$\sin(\pi/3 - \theta_{sec}) + \frac{1}{2}\cos(\theta_{sec} - \pi/6) < \frac{1}{2m}. \tag{3.16}$$

Due to the symmetry, $0^\circ \le \theta_{sec} < 30^\circ$ is considered. The ultimate solution of *m* and θ_{sec} may not be convenient to implement although it is not difficult to get in mathematics. Solving the modulation index *m* valid for the full range of θ_{sec} is more practical. It is derived that *m* is no more than 0.385. Therefore, the proposed MPW SVM applies the zero vectors based on the following basic rules. When *m*> 0.385, apply V_7 at $0^o<\theta_{sec}<30^o$, and V_0 at $30^o<\theta_{sec}<60^o$ in the sectors I, III and V; apply V_0 at $0^o<\theta_{sec}<30^o$, and V_7 at $30^o<\theta_{sec}<60^o$ in the sectors II, IV and VI. When *m*<= 0.385, apply V_0 the same duration as V_7 in each switching cycle.

Fig. 3.52(b) shows the phase duty cycle when applying the MPW SVM methods of using two zero vectors. It can be seen that at *m*=0.385, the MPW SVM with λ=1 improves the minimum pulse width. The smallest pulse width is longer than 25% of the switching cycle. For the case of *m*=0.1, the MPW SVM control with λ=1 also substantially increases the pulse width of the inverter output pole voltage.

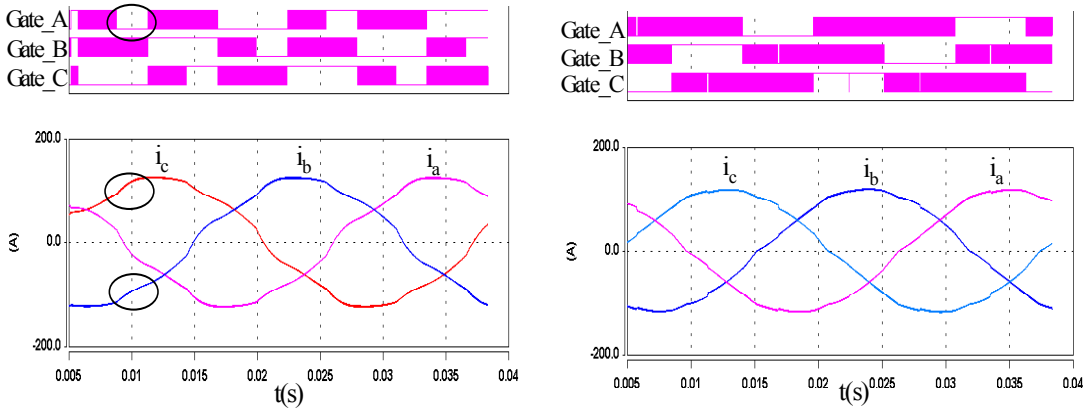


(a) (b)

Fig. 3.52. Phase duty cycle of the proposed MPW SVM: (a) High m and (b) Low m.

3.6.3. Verification of the Proposed MPW SVM

The ARCP was simulated in the Saber to verify the effect of the MPW SVM control. The specifications include: Vdc=325 V, I_{load}=200 Arms, L_x=1.0 μH, C_s=0.22 μF and dead-time=1.8 μS. The maximum T_{dis} is about 3 μS. Therefore, the actual T_{min} for the PWM gate signals prior to inserting the dead-time is set as 6.8 μS. One operating point with *m*=0.40 and f_o=30 Hz when supplying the inductive load is simulated for both conventional SVM and the MPWSVM. Fig. 3.53 shows the current waveform comparison between the conventional SVM and MPW SVM at f_s=20 kHz. The circle on the upper device's gate signals indicates the large blank portion as a result of minimum pulse deletion for the conventional SVM. Correspondingly, the distortion of the load current appears. The MPW SVM gate signals show little blank portion in the gating signals and the resulting load current waveform is much better than the usual SVM. Fig. 3.54 shows the detailed harmonic current comparison. Clearly, the proposed MPW SVM leads to significantly reduced low frequency harmonic than the conventional SVM method.



(a) (b)

Fig. 3.53. Upper switches' gate signals and the load current of ARCP inverter: (a) SVM of $\lambda=0.5\cdot(1+\mathrm{sgn}(\sin 3\theta))$ and (b) the proposed MPW SVM.

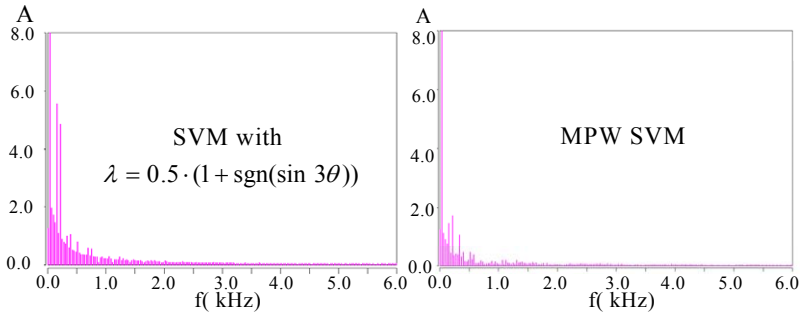
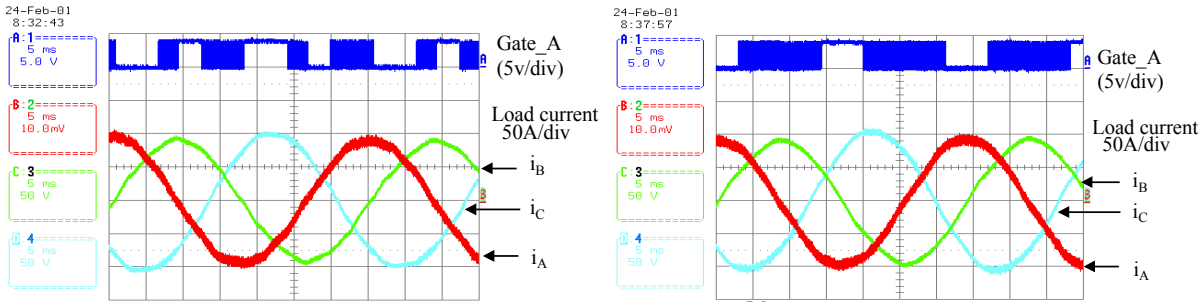


Fig. 3.54. Harmonics comparison of the load current.

The hard-switching inverter is tested at m=0.4 and f_o=30 Hz with the inductor load. The minimum pulse width is set to be 6.8 μS. The corresponding waveforms are shown in Fig. 3.55. Obviously, the proposed MPWSVM almost has no elimination of the short pulse gate signals while the conventional SVM has the large portion of deleted gate signals. The load current waveforms confirm that the MPW SVM reduces the harmonic distortion of the load current compared with the conventional SVM scheme. The ARCP inverter is also tested with the motor load at the switching frequency f_s=10 kHz. The waveforms with m=0.52 are shown in Fig. 3.56.

As seen from Fig. 3.56, the quality of load current waveform is improved by the MPW SVM compared with the conventional SVM.



(a) (b)

Fig. 3.55. Load current comparison of the three-phase inverter: (a) Conventional SVM and (b) The proposed MPW SVM.

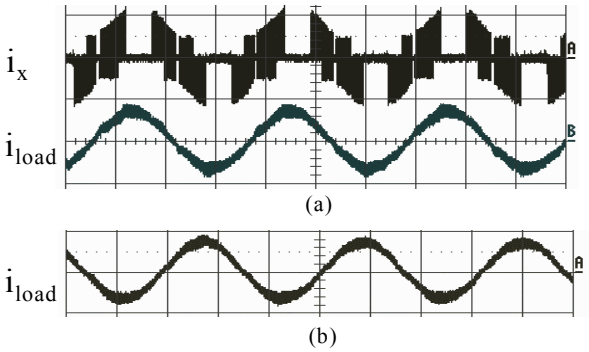


Fig. 3.56. Key current waveforms of the ARCP inverter: (a) Conventional SVM; (b) The proposed MPW SVM. (5 ms/ div, 200 A/div)

3.7. Summary

Three types of soft-switching topologies – the six-switch ZCT, the ARCP ZVT, and three-switch ZCT topologies – are implemented and successfully tested in the 55 kW inverters for EV applications.

The efficiency comparison indicates that the evaluated soft-switching inverters do not show improvements over the hard-switching inverter at 10 kHz switching frequency when using 600 V devices. With modern IGBT and diode characteristics, this comparison reveals both the

importance of auxiliary circuit design and the possibility of more improvement with higher switching frequencies or higher operating voltages.

Only the ARCP ZVT inverter shows a significant reduction of conducted EMI from 2 MHz to 10 MHz, while the two types of ZCT inverters do not significantly improve the EMI characteristics. The EMI reduction in the MHz range can lead to a cost reduction of EMI filter.

Although the three-switch ZCT inverter requires the least cost and space for its auxiliary circuit as compared with the other inverters, any soft-switching inverter needs additional cost and space. It is still very difficult to say that the improved performance of the soft-switching inverters can justify the additional cost and space, at least with the devices rated up to 600 V and operating at switching frequencies below 20 kHz.

Although the soft-switching inverter has a minimum pulse-width limitation, at 10kHz operating frequency, the effects on the THD due to the minimum pulse-width limitation is not severe to cause considerable motor losses. The actual measurement reveals almost identical THD for the soft-switching and hard-switching inverters. To alleviate the harmonic distortion at higher switching frequency, a MPWSVM is proposed for soft-switching inverters. This scheme can maximize the pulse width of the SVM signals and is verified to be effective in reducing the effect of the minimum pulse limitation.

The test waveforms show that the soft-switching inverters can significantly reduce voltage stress. The ARCP ZVT's voltage stress at turn-off is about 30 V, and the hard-switching inverter has a voltage spike of about 80 V. The ZCT inverters have the least voltage stress at turn-off.

All the evaluation data indicate that for the small-duty EV applications, the device technology greatly offsets the soft-switching inverter's performance. It may be worthwhile to take a look at

the design of other power ratings. Since the efforts to develop fully functional soft-switching inverters are tremendous, it would be advantageous to develop an effective modeling tool for analyzing the soft-switching inverter's performance. The next chapter will present the electrical modeling for the three-phase inverter and the performance of the soft-switching inverters are analyzed using the developed model method.

Chapter 4. Modeling and Simulation of IGBT Devices

4.1. Introduction

From the previous chapters, it is known that the tremendous efforts are required and have been made to design and implement the soft-switching inverters in order to experimentally evaluate their performance. Although a lot of valuable information has been obtained through the experimental assessment and the qualitative analysis, it is still lack of the deep understanding of the overall effects of the soft-switching inverters, designed for different application specification, as compared with the hard-switching inverters in terms of the electrical performance such as the electrical stress, the EMI noise level and the loss reduction. It is desired that some quantitative analysis of the soft-switching inverter's performance are presented. To provide the detailed and the insightful analysis, the electrical modeling and simulation of the soft-switching inverters are conducted. This chapter presents the electrical modeling of the IGBT devices and demonstrates the accuracy of the device model at the aspects of the EMI noise, the voltage stress and the switching losses. The proposed modeling approach can be used to establish the accurate IGBT model for the electrical simulation in Saber software. Since the accurate device model is used to predict the EMI noise, the electrical stress and the switching losses, it is worthwhile to explain the significance of the device model in the electrical simulation.

From controlling EMI noise level viewpoint, the purpose of analysis of EMI noise is to mainly investigate the fundamental mechanism of the conducted noise generation and predict the worst-case scenario for EMI compliance design [D1]-[D5]. One insightful analysis should be very helpful to diagnose noise distribution and then to figure out the noise reduction technique such as

the EMI filter design or noise source modification. Regarding to the analysis of EMI noise from soft-switching inverters, there exist two levels of challenges, which determines it is a rather difficult task. One aspect is related to understanding of the hard-switching inverters. Some research works [D8]-[D10] have been focusing on the hard-switching inverter EMI analysis since 1990s. Compared with the conventional single-phase switched mode power supply, the three-phase inverter leads to a more challenging task for EMI noise analysis due to multiple switches' configuration of the power stage and the variety of PWM control methods.

Several approaches were presented to analyze the basic mechanism of the EMI noise generation from hard-switching inverters. Simplified time domain models were proposed to predict the switching noise across the LISN measurement resistor [D1][D22]. Although the model is simple, it made several important assumptions, which impairs a great deal of accuracy of model in practice. One is the idealized CM noise source model, in which the source voltage and impedance parameters are neither well derived and nor derived [D18]. One assumption is the ideal switching waveform of the power devices. Neither of the diode reverse-recovery current's effect and the internal interconnect parasitics has been addressed. Another assumption is the ideal bus plates for the power inverter. As we know, the three-phase inverter makes interconnection of IGBTs using the laminated bus bars to reduce the parasitic inductance. However the model did not explain any effects resulted from the bus bars. In summary, the simplified model does not explain the EMI noise at the input power supply side although it models fairly accurate the EMI noise at the motor side. A frequency domain model is also used to quickly predict the EMI spectrum. Since it is based on the assumptions used for the simplified time domain model, the inherent drawbacks are apparent.

It is our intent to develop a systematic modeling approach to analyze or predict the EMI noise of the three-phase inverter. The proposed research work involves two major aspects. First, a new parameter extraction scheme is presented to effectively build 1-D physics-based IGBT simulation model, so called Hefner model [E3]. In addition to the physics-based IGBT model representing the behavior of the silicon die, a systematic measurement-based method is presented to extract the internal parasitic inductance of the half-bridge IGBT module [D11]. With the parasitic model and the IGBT device model, the single leg testing is conducted. The switching waveform and the EMI noise waveform obtained via the test is compared with the simulation. The good agreement between the test and the simulation result is obtained. Also the switching losses are predicted to compare with the experimental results. It is found that we can also use the developed simulation model to predict the switching losses. Second, the planar bus plate is modeled using the finite element analysis [D13][D14]. The couplings among different phases are included in the model. The complete three-phase inverter model was developed in Saber and provided the detailed explanation of the experimental results. The modeling and simulation work at the inverter level will be presented in Chapter 5.

4.1.1. Device Model's Effects on DM Noise Prediction

The modern IGBTs exhibit very high dv/dt and di/dt during the switching instant, which is the major noise source. The switching pattern of the three-phase devices modulates the DC link current. Thus, the waveform of the DC link current consists of pulses with different amplitudes and different durations. The intrinsic conducted EMI noise is directly caused by the pulsating DC link current. Without including the effect of the finite slew rate of the DC link current and the potential ringing due to the layout or interconnect parasitics, the idealized pulse current helps to

understand the basic features of the DM noise. One inverter leg is shown in Fig. 4.1. As shown in Fig. 4.2, the amplitude is A, the period is T, and the duration of the positive value duration is τ.

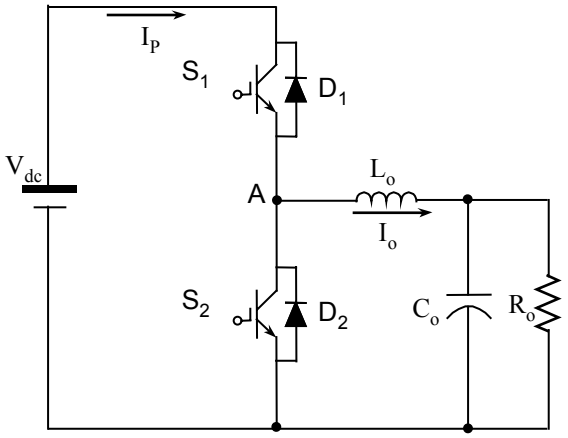


Fig. 4.1. One leg configuration.

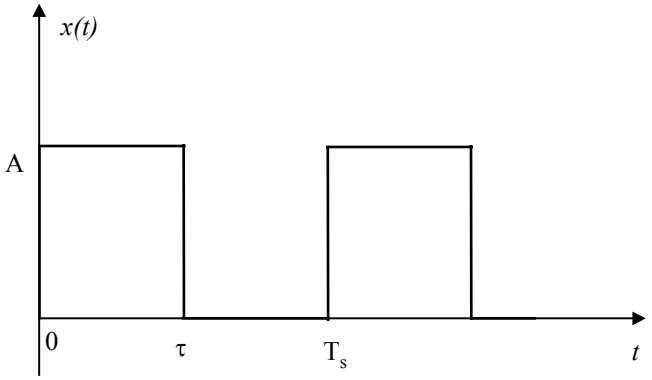


Fig. 4.2. DC link current waveform in one inverter-leg.

Via the Fourier analysis, the periodic square wave, indicated in Fig. 4.2, can be represented as follows.

$$x(t) = A \cdot D + \sum_{n=1}^{\infty} C_n \cos(n\omega_o t + \varphi_n), \tag{4.1}$$

$$C_n = 2AD\left|\frac{\sin(n\pi D)}{n\pi D}\right|, \text{ and} \tag{4.2}$$

$$\varphi_n = \pm n\pi D, \tag{4.3}$$

where C_n is the amplitude of the n^{th} harmonic, n is the phase angle of n^{th} harmonic, and D is the duty cycle, equal to τ/T_s. The $\pm$ sign of the angle comes because the $\sin(n\pi D)$ term may be positive or negative. Based on Equation 4.1, the amplitude spectrum of the square wave is illustrated in Fig. 4.3. The spectrum upper-bound curve is a function of sinx/x, which is shown in Fig. 4.4. Although the spectral components only exist at frequency f=n/Ts, the envelop of these spectral components follows two asymptotes. The first asymptote has a slope of 0 dB/decade and the second asymptote has a slope of –20dB/decade [D26]. The corner frequency is at $1/\pi\tau$. This indicates that the larger the duty cycle, the lower the corner frequency. So the narrow pulse contains more high frequency spectrum than the wide pulse, which agrees with the intuition.

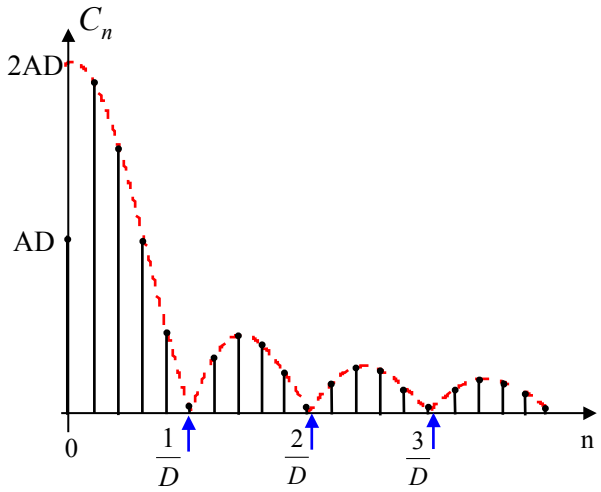


Fig. 4.3. Magnitude spectrum of the square wave.

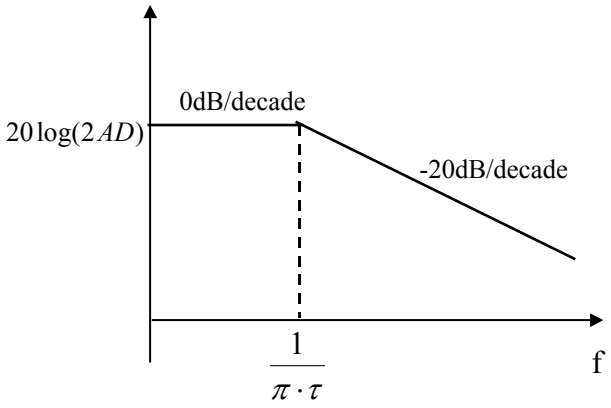


Fig. 4.4. Envelop of the amplitude spectrum of a square wave.

The trapezoidal waveform, as shown in Fig. 4.5, is more close to the practical situation than the ideal square wave. For the purpose of convenience, it is assumed that the rise time τ_r and fall time τ_f are equal. Therefore, the amplitude of harmonic spectrum can be expressed as follows.

$$C_n = 2AD\left|\frac{\sin(n\pi D)}{n\pi D}\right|\left|\frac{\sin(n\pi t_r/T_s)}{n\pi t_r/T_s}\right|. \tag{4.4}$$

Compared with Equation 4.2, the spectrum magnitude of the trapezoidal pulse train is also related to the rise or fall time. In fact, the spectrum bound envelope has one more corner frequency, as illustrated in Fig. 4.6. Compared with the expressions for square wave, the finite rise and fall time leads to effect of modulating amplitude envelope. The slower rise and fall edge leads to a smaller corner frequency noted as $1/\pi t_r$, and thus the higher order harmonic attenuates faster.

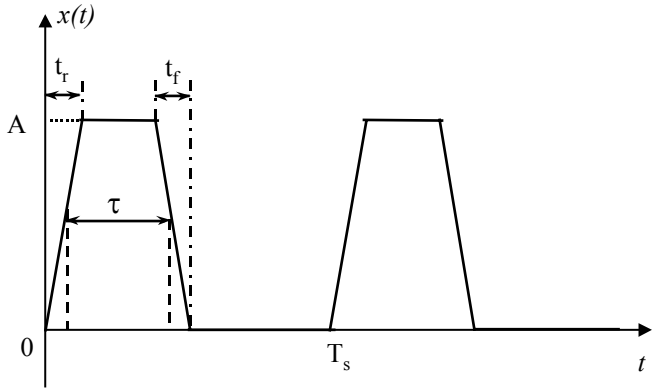


Fig. 4.5. Trapezoidal pulse train.

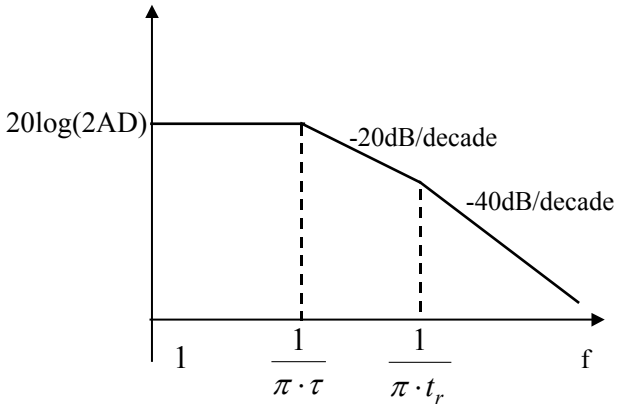


Fig. 4.6. Envelope of the amplitude spectrum of a trapezoidal pulse train.

The analysis of the square wave and the trapezoidal pulse train provides a basic understanding of the effect of the duty cycle and the rise/fall time on the harmonics [D19][D20]. As mentioned previously and shown in Fig. 4.7, the DC link current is of pulse train with different amplitude and the duty cycle over the AC fundamental cycle. Due to the symmetric operation of the three phase-legs, the DC link current can be approximately characterized with the frequency six times of fundamental load current frequency. Extensive simulations based on a three-phase inverter have been conducted. Summarizing the feature of the idealized DC link current, the conclusion is that the PWM patterns or SVM schemes have little impacts on the harmonic spectrum. Although the trapezoidal waveform provides the basic understanding of the DM noise current in the

inverter operation, the practical current waveforms are more complicated. The real current waveforms may not be described via a simple trapezoidal waveform, and include the ringing caused by parasitic inductors and capacitors. One example of the practical circuit current and its approximation is shown in Fig. 4.8. The current overshoot at the rise transition is actually resulting from the diode reverse recovery. The approximation curve uses piece-wise linear lines to approximate the real device current during the transition. Such an approximation might give people impression that the accuracy is enough. However, the comparison of noise spectrum at the frequency domain, as shown in Fig. 4.9, indicates that the trapezoidal curve's approximation does not match the real spectrum well at high frequency region, more than 15 dB higher around 10 MHz. The major reason is that the diode reverse recovery related current is not modeled and the high frequency ringing is not modeled either. Another approximation is made in Fig. 4.10 using triangle waveform to model the diode reverse recovery current. However, the spectrum comparison suggests that the high frequency noise approximation is still far from the real noise level, as shown in Fig. 4.11. It is true that the more careful piece-wise linear approximation in Fig. 4.10 increases the frequency range, which is modeled with an acceptable accuracy. As a result, approximation I curve models the noise accurately up to 5 MHz while approximation II curve models the noise accurately up to 15 MHz. These investigations illustrate that accurate current waveforms need to be reconstructed in the EMI noise quantification study. Simple trapezoidal approximation can only give the qualitative noise information and should not usually be used for the EMI analysis and the filter design especially the high frequency noise is concerned.

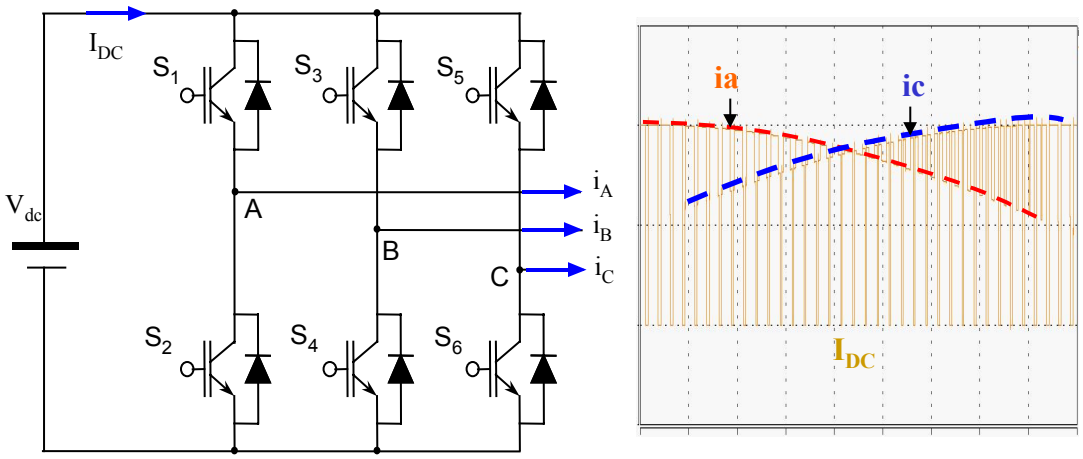
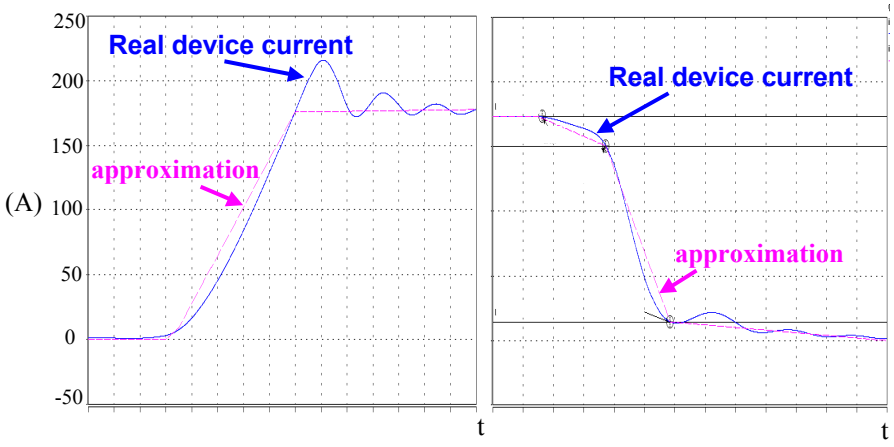


Fig. 4.7. Illustration of DC link current in a three-phase inverter.



(a) (b)

Fig. 4.8. Approximation method I with trapezoidal waveforms:
(a) rise transition approximation, and (b) fall transition approximation. Time: 40 nS/div.

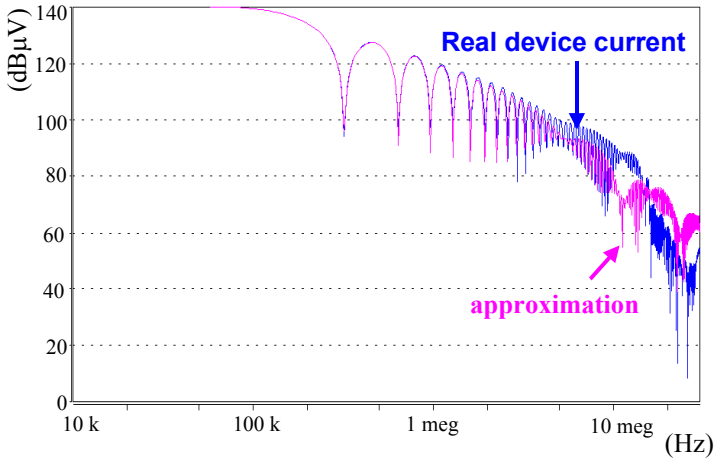
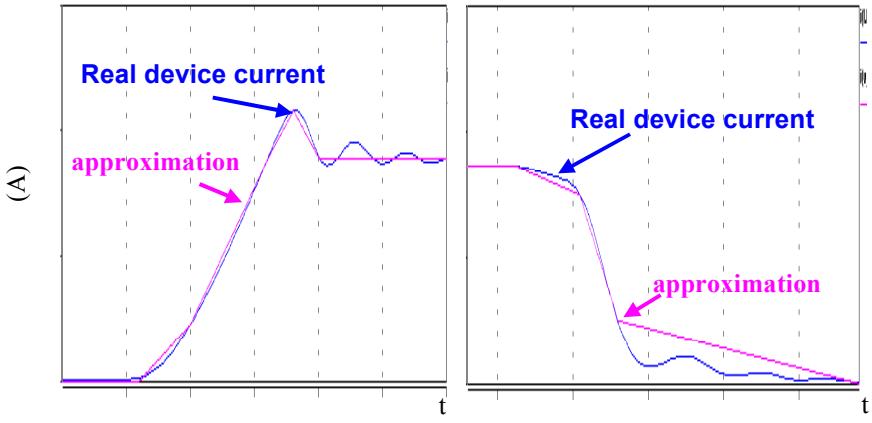


Fig. 4.9. Noise spectrum comparison of approximation I and real current.



(a) (b)

Fig. 4.10. Approximation method II with trapezoidal waveforms:
(a) rise transition approximation, and (b) fall transition approximation. Time: 40 nS/div.

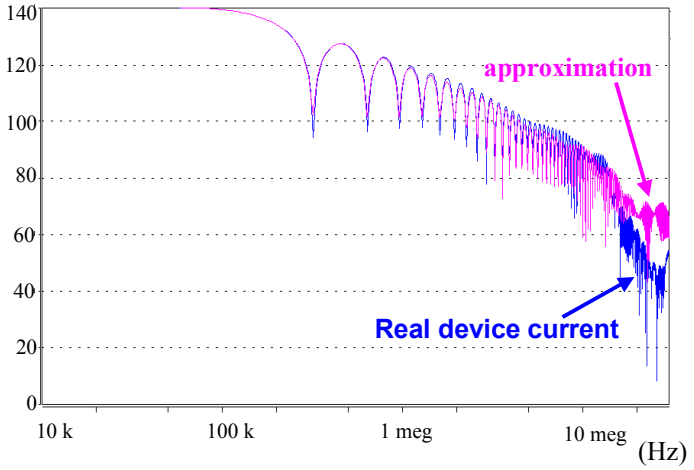


Fig. 4.11. Noise spectrum comparison of approximation II and real current.

4.1.2. Device Model's Effects on CM Noise Prediction

In general, the CM noise is the result of the fluctuation of voltage level of devices in a three-phase inverter to the earth ground. So power devices' switching is the real CM noise source. Usually there is no direct connection between the power circuit and ground plane. The actual CM noise current path is allowed by the parasitic stray capacitance between various points of the circuit layout and the earth ground. Thus the CM noise path is really unseen from the normal circuit schematic and determined mainly by the parasitic parameters [D20][D29][D31]. The most dominant parasitics for the CM noise generation is the stray capacitance between the power device's terminal and the heat sink, which is usually grounded for a three-phase inverter. Since the inverter output nodes have most significant voltage fluctuations compared with other points of the power inverter, the majority of the CM noise current is generated during the voltage transition of the output nodes. To explain the CM noise generation and propagation path, one phase-leg's operation with inverter parasitics is shown in Fig. 4.12. C_{pc1}, C_{pe1} and C_{pe2} are the stray capacitance from the IGBT terminals to the ground. The shown example corresponds the turn-on transition of top switch S_1. The induced voltage polarity on the bus parasitic inductance L_{bus} leads to that the CM noise current flows into the ground through $C_{pc1}$and flows out of the ground into C_{pe2}. Since the voltage of node A rises during the transition, the CM noise current flows out of A into the ground through C_{pe1}. The CM noise current flows through both positive and negative bus, forming a closed loop via the ground plane. In the standard conducted EMI test setup, the CM noise current flows through 50 ohm of LISN to or from the ground plane. Most of previous studies do not carefully model all the stray capacitance, and instead focuses on the modeling of stray capacitance between node A to ground. This is not correct practice since the

CM noise current I_{c1_g} and I_{e2_g} also contributes to the CM noise current. It is also found that the impedance measured between half-bridge IGBT module's any terminal to ground is the same as the measurement result when shorting all three terminals together. This indicates that when doing the small signal measurement, as most impedance analyzer does, the anti-parallel diode or IGBT appears at short at high frequency. This phenomenon tells that some of past publications mistakenly model the stray capacitance value.

When the IGBT is switched, the dv/dt of device voltage is affected by the switching speed, the load current and stray inductance. When modeling the CM noise as the current source, it is not straightforward to put the meaningful model in the circuit. Most previous research simply shorted DC bus lines when assuming the bus is very low impedance to the ground [D21]. However, such an approach does violate one basic observation about the noise path un-symmetry caused by two devices, one is IGBT and the other is diode, during commutation. For example, if the top device is turned on, the CM noise is initiated by the sudden change of the device voltage. During the switching transition, the junction capacitance of two devices in one leg is quite different. Therefore, the noise path impedance is smaller compared with the bottom device. So even with symmetric bus plate structure, the CM noise current splits at the different level in two devices. The ground current is flowing out of node A to the earth. However this current is not evenly divided into two equal parts flowing into two devices. To accurately model the CM noise current, the simulation using the accurate device model is preferred, which can reflect the real voltage waveforms at a large extent.

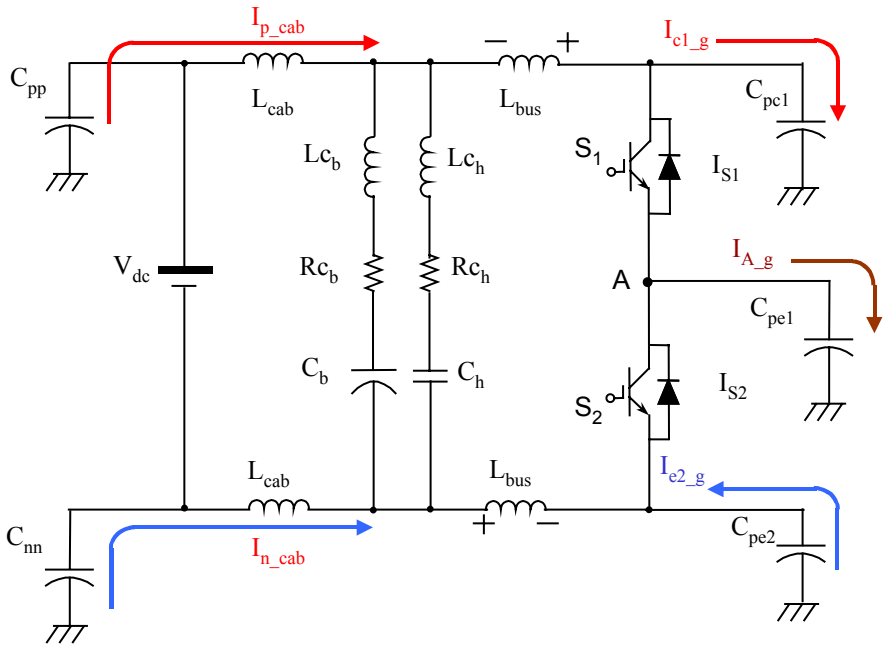


Fig. 4.12. Example of CM noise current flowing path.

From the preceding analysis, the accurate device model, which can represent the actual switching waveforms, is crucial to predict the EMI noise. If the switching waveforms are predicted accurately using the accurate device model, it can be expected that the voltage stress, the current stress and the switching losses are also reflected correctly.

4.2. Developing 1-D Physics Based IGBT Model

Modern IGBTs have become the popular device choices in the variety of power electronics applications, which usually requires relatively high power and medium switching frequency (a few of kHz to hundred kHz). Typical applications include the industrial motor drive and the electric or hybrid vehicles. Among several IGBT models developed in the past, the one-dimensional (1-D) physics-based IGBT model developed by Hefner has been demonstrated to achieve acceptable accuracy. Such a model has been implemented in the commercial circuit

simulator Saber to facilitate the circuit designer's design. However, it needs to be noted that the associated parameter extraction scheme requires the designated sets of experiments and the elaborate software tools, which makes the model parameter extraction work a very complex task for the electrical engineers. The lack of the practical parameter extraction method greatly limits the use of the IGBT model in the inverter study since most device manufacturers are not willing to disclose their device's parameters due to the technical proprietary techniques. Most recently, there have been some attempts in simplifying parameter extraction schemes [E6]. But a number of different experiment setups are still required. Moreover, the extraction scheme only applied to non-punch-through (NPT) IGBTs and the vague information is provided for punch-through (PT) IGBTs. The report released from NIST (national institute of standards and technology) indicates due to the lack of the proper tools for the IGBT model parameter extraction, the model itself is underused. Currently there exists Hefner's extraction scheme for the IGBT model. However, the learning curve is too deep so that many application engineers were scared away. In addition, the extraction process required the professional software and the designated test equipment. To overcome these issues, the efforts were made to derive a method that is easier to use, which might not require the user to have the strong device physics background.

4.2.1. 1-D Physics Based IGBT Model

The fundamental concept of the 1-D physics-based IGBT model developed by Hefner is to consider the IGBT as an integration of the power MOSFET and PNP transistor, as shown in Fig. 1(a). In principle, the MOSFET channel current I_{mos} provides the base current I_n to the PNP transistor. The amplification effect of the PNP transistor leads to the collector current I_p. The equivalent circuit is supported by the physical structure of IGBT. As seen from Fig. 4.13(b), n+

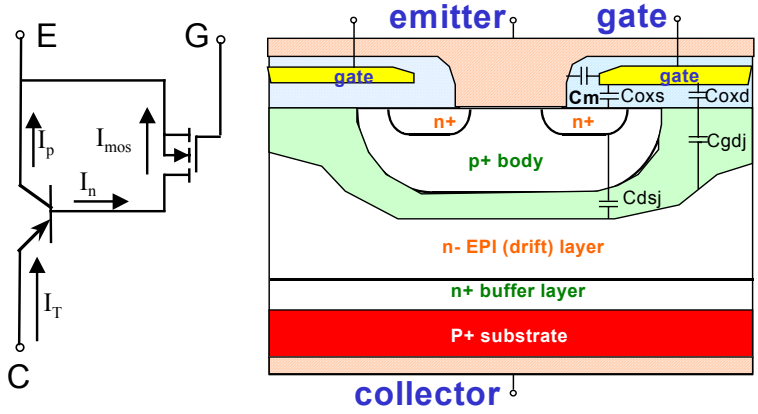
region under the gate electrode, p+ body and n- region form a structure of power MOSFET. The p+ substrate, n- layer and p+ body compose of a structure of PNP transistor. In the IGBT model implementation, the behavior model of power MOSFET is adopted and mainly uses transconductance parameters to model the V-I characteristics of MOSFET. The unique modeling work lies in the PNP transistor. Since it is operated under a high level injection and low gain condition, the electron and hole current are coupled with each other, which is different from the conventional bipolar junction transistor case. Therefore, the ambipolar equations are used to solve the excess carrier's distribution.

The spatial coordinate systems are shown in Fig. 4.14 using x representing the position in the base region and using x* representing the position in the buffer layer. Based on the coordinate system, the excess carrier concentration can be obtained by the followings:

$$\delta p_{buf}(x^*) = \frac{p_{buf\,0}\sinh(W_{buf} - x^*)/L_{buf} + p_{buf\,W}\sinh(x^*/L_{buf})}{\sinh(W_{buf}/L_{buf})}, \text{ and} \tag{4.5}$$

$$\delta p_b(x) = p_{b0}\frac{\sinh[(W_b - x)/L_b]}{\sinh(W_b/L_b)}, \tag{4.6}$$

where L_{buf} is the diffusion length of the buffer layer, and L_b is the diffusion length in the base region. The excess carrier concentrations at the boundary between emitter and the buffer layer, and between the buffer layer and base region, are illustrated in Fig. 4.15. These boundary conditions relate the IGBT terminal current with the doping density of the each region. Therefore, the complete mathematical description about the IGBT terminal current and the internal carrier density can be established. In one IGBT model, the main parameters are listed in Table 4-1. All these parameters need to be obtained in order to develop an accurate simulation model



(a) (b)

Fig. 4.13. IGBT physics: (a) equivalent circuit and (b) cell structure.

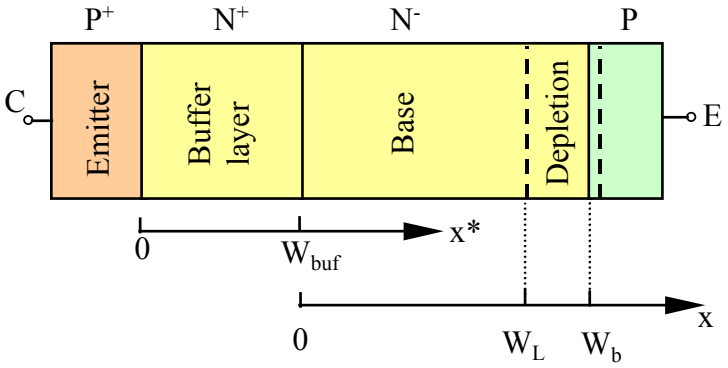


Fig. 4.14. The coordinate system adopted in Hefner IGBT model.

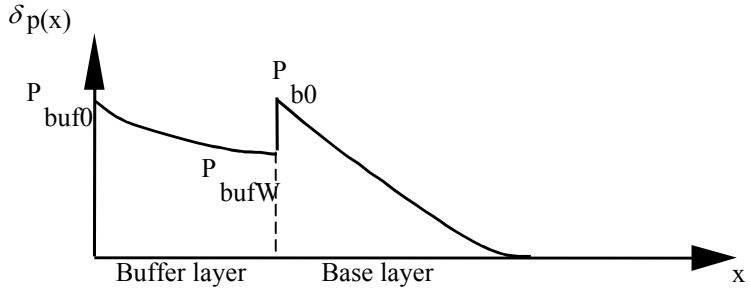


Fig. 4.15. Excess carrier distribution and level at boundary.

Table 4-1. Key parameters in Hefner IGBT model.

	Symbol	Description
MOS Gate	V_T	Threshold voltage
	K_P	Transconductance factor
	K_f	Triode region factor
	θ	Transconductance reduction factor
	C_{gs}	Gate-source capacitance
	C_{oxd}	Gate-drain overlap oxide capacitance
Geometry	A	Active area
	A_{gd}	Gate-drain area
PNP Transistor	N_b	Base doping concentration
	W_b	Metallurgical base width
	N_{buf}	Buffer layer doping concentration
	W_{buf}	Buffer layer width
	τ_{hl}	High level excess carrier life time
	τ_{ll}	Buffer layer excess carrier life time

4.2.2. New Parameter Extraction Scheme for IGBT Model

Due to the complexity of applying Hefner's parameter extraction scheme, it is our interest to simplify the procedure so that the ordinary electrical engineer can use the IGBT model. It is noted that the proposed scheme tries to take full advantage of the device datasheet, which is usually provided by the device manufacturer. The detailed parameter extraction schemes are explained as follows. The followings illustrate the parameter extraction process using a punch-through (PT) IGBT with ratings of 600 V and 300 A as an example. The device is MG300J2YS50 from Toshiba and has been selected and implemented into the soft-switching inverter hardware, as described in Chapter 3.

1. Derive C_{gs} and C_{oxd}.

C_{gs} is the capacitance formed between the gate and source in the MOSFET portion of an IGBT device. As can be seen from Fig. 4.13(b), C_{gs} is a structure-determined capacitance, and equal to the sum of C_{cm} and C_{oxs}, where C_{cm} is the gate to source overlap-metallization capacitance and C_{oxs} is the gate-source overlap oxide capacitance. C_{gs} can be obtained either

from the gate charge curve or the inter-electrode capacitance data, which is normally provided in the data sheet. If derived from the gate charge curve, the expression for C_{gs} is given by:

$$C_{gs} = \frac{Q_{g1}}{V_{ge1}}, \tag{4.7}$$

where Q_g is the accumulative gate charge into the gate terminal of IGBT and V_{ge} is the gate-emitter voltage. The point (Q_{g1}, V_{ge1}) should be located at the linear line section of the gate charge curve and corresponds to the condition under which V_{ce} is still equal to applied DC bus voltage. During this period, the gate voltage is below the threshold voltage and thus the IGBT is not turned on. The current injected into the gate terminal mainly charges C_{gs} because C_{gc} at high DC bus voltage is very small compared with C_{gs}. As shown in as shown in Fig. 4.16, Q_{g1}=93.0 nC and V_{ge}=4 V, so C_{gs}=23.2 nF. On the other hand, C_{ies}, C_{oes}, and C_{res} are the capacitance often measured by IGBT manufacturers. If derived from the capacitance curve of IGBT, as shown in Fig. 4.17, the relationship between these capacitors and the inter-electrode capacitance are illustrated in Fig. 4.18. Therefore, C_{gs}=C_{ge}= C_{ies} - C_{res}. For example, from Fig. 4.17, at V_{ce}=0.1 V, C_{gs}= C_{ies} - C_{res}=23.1 nF. Since the data sheet only contains diagrams instead of data files, it is worthwhile to point out that reading the value from a data sheet's diagram can be easily done. For example, the SABER sketch software provides one tool called scanned data, which can import an image and then convert a curve in it to a data file.

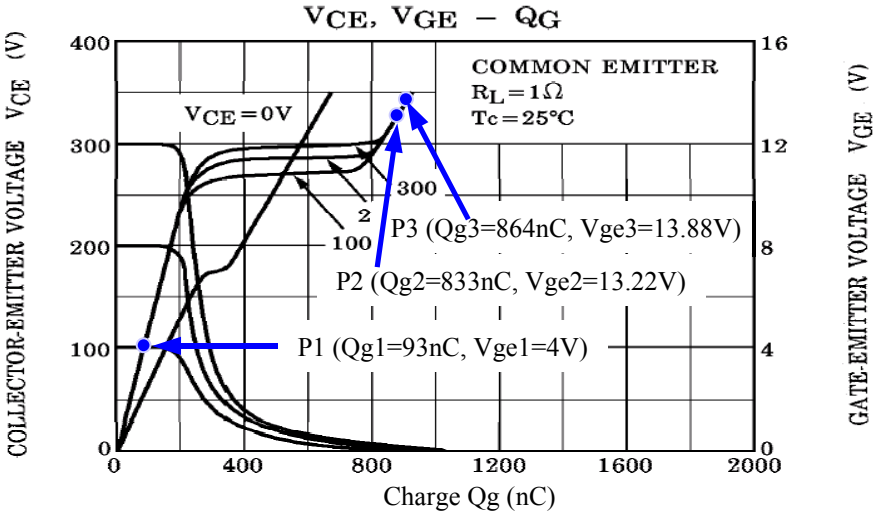


Fig. 4.16. Sample points of gate charge curve to derive C_{gs}.

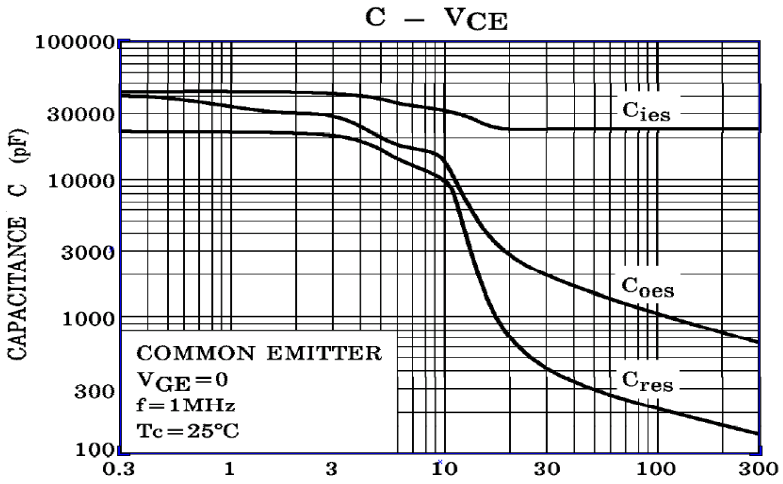
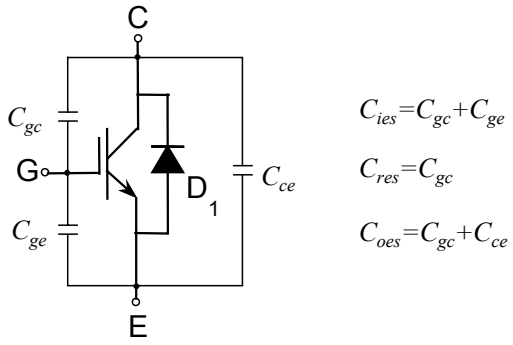


Fig. 4.17. Capacitance curve in datasheet of IGBT.



$C_{ies}=C_{gc}+C_{ge}$

$C_{res}=C_{gc}$

$C_{oes}=C_{gc}+C_{ce}$

Fig. 4.18. Relationship of inter-electrode capacitance of IGBT.

As seen from Fig. 4.13(b), C_{oxd} is the oxide capacitance between the gate and the drain region of the internal MOSFET, which does not change over the applied device voltage level. C_{gc} is almost equal to the series value of C_{oxd} and C_{gdj}, where C_{gdj} is the depletion capacitance in the drain region. When V_{ce} is quite small, the C_{gdj} is very large due to the very thin depletion layer. Consequently, the capacitance of the C_{gs} and C_{gdj} in series is almost equal to C_{oxd}. Therefore, C_{oxd} is considered to be the same as C_{gc} at the very low device voltage. As shown in Fig. 4.17, C_{oxd} is equal to about 22 nF since $C_{gc} = C_{res}$ =22 nF at V_{ce}=0.3 V. Similarly, C_{oxd} can also be derived using the gate charge information. As shown in Fig. 4.16, C_{ies} can be derived using the information of P2 and P3. The express of C_{ies} is given by

$$C_{ies}=\frac{Q_{g3}-Q_{g2}}{V_{g3}-V_{g2}}. \tag{4.8}$$

C_{ies} is calculated to be 46.8 nF. Since P2 and P3 correspond the very low level of V_{ce}, the C_{ies} is considered to be the sum of C_{gs} and C_{oxd}. Consequently, the subtraction of C_{gs} from C_{ies} obtains the value of C_{oxd}, 23.2 nF. It can be seen that either the gate charge curve or the inter-electrode capacitance curve can be used to derive the structural capacitance, C_{gs} and C_{oxd}.

2. Derive N_b, $A_{gd,}$ and V_{td}.

N_b is the doping density of the lightly doped N^- base layer and A_{gd} is the area of the gate-drain region when A represents the active silicon area of an IGBT. In Hefner's originally proposed method, the doping parameters are derived from the measured ratio β_{tr} of the abrupt current drop portion to the current prior to IGBT's turn-off. β_{tr} is defined as follows:

$$\beta_{tr}=\frac{I_T(0^+)}{I_T(0^-)-I_T(0^+)}, \tag{4.9}$$

where $I_T(0^+)$ is the tail current level of IGBT at turn-off and $I_T(0^-)$ is the device current before turn-off. According to the analytical analysis, the ratio can then be related with the IGBT's internal design parameters as follows.

$$\beta_{tr} = \beta_{tr}^{max}(1+\frac{I_T(0^+, V_{dc})}{I_k})^{-1} \tag{4.10}$$

$$\beta_{tr}^{max} = \frac{W^2 + (\frac{2D_{pl}}{D_{ph}})W_{buf}^2}{2D\tau_{eff}(V_{on})}, \text{ and} \tag{4.11}$$

$$W = W_b - \sqrt{2\varepsilon_{si}(V_{ce}+0.6)/qN_b} \ . \tag{4.12}$$

The main idea is to experimentally obtain the relationship among β_{tr}, $I_T(0^+)$ and V_{dc}. This requires a number of measurement results from the switching test under different bus voltages and the load-current levels. As seen from Equation 4.10, theoretically β_{tr} is expressed by a function of $I_T(0^+)$, β^{max}_{tr} and V_{dc}. The parameters used in the function are W, W_{buf}, D_{pl}, D_{ph}, N_b, ε_{si}, W_b. The meanings of symbols are given in Table 4-2. Through the experiment-derived relationship β_{tr}, $I_T(0^+)$ and V_{dc}, a specialized software is used to curve fit three IGBT design parameters such as W_b, W_{buf} and N_b. The issues of using this method are: 1. It requires a professional software that is not usually accessible and this software is not even commercially available; 2. A delicate set of the test equipments is required with the capability of automatically transferring the measurement data to a computer for the data processing; 3. Users are required to have strong device knowledge in order to extract the IGBT parameters since the accuracy of the curve-fitting functions in the extraction software strongly replies on users' input and judgment in properly changing the parameters. Due to the above reasons, the extraction software is seldom used by the application engineers and shows little value since its introduction in 1991.

Table 4-2. Parameters used in Hefner's extraction method for W_b, W_{buf}, and N_b.

Symbols	Description
W_b	width of N- base layer (cm)
W_{buf}	width of buffer layer in PT device (cm)
W	width of quasi-neutral layer in base region (cm)
D_{pl}	hole diffusivity in N- base layer (cm^2/s)
D_{ph}	hole diffusivity in buffer layer (cm^2/s)

To efficiently extract the parameters, a different approach is taken to derive the doping density N_b. It is noticed that the doping density N_b in the lightly doped base region has direct impacts on the depletion capacitance. Therefore, the measured IGBT capacitance is possibly used to derive the internal doping density. First, the device active area A is obtained by visually measuring the IGBT die area inside the field ring. Some device company like Infineon supplies such die-area information to the customers. Another approximation of calculating the active die area is to use the normal current density value, from 90 A to 150 A/cm^2. The 1-D IGBT modeling approach adopted by Hefner considers that the total active area of the IGBT die consists of two parts. One is the gate-drain overlap area A_{gd} and the other is the drain-source overlap area A_{ds}. The corresponding depletion capacitance C_{gdj}, the gate-drain depletion capacitance of the internal MOSFET, and C_{dsj}, the drain-source depletion capacitance of the internal MOSFET, are indicated in Fig. 4.13(b). The expressions of A_{gd} and A_{ds} are given as follows.

$$A_{gd} \approx \frac{C_{gdj}}{\sqrt{\frac{qN_b\varepsilon_{si}}{2(V_{dg}+V_{td})}}}, \text{ and} \tag{4.13}$$

$$A_{ds} = \frac{C_{dsj}}{\sqrt{\frac{qN_b\varepsilon_{si}}{2(V_{ds}+0.6)}}}. \tag{4.14}$$

Where ε_{si} is the dielectric constant of the silicon, q is the electric charge of an electron, V_{dg} is the voltage across the drain and gate terminal of the internal MOSFET, and V_{ds} is the drain-source voltage of the internal MOSFET. The depletion capacitance is proportional to the corresponding overlap area and the inverse proportional to the width of the depletion layer. Since A= A_{gd}+A_{ds}, Equations 4.4 and 4.5 can be used to further derive the relationship between the active die area A and the doping density. Then the doping density N_b can be expressed as follows.

$$N_b = \frac{1}{A^2}\frac{2}{q\varepsilon_{si}}(C_{gdj}\sqrt{(V_{gd}+V_{td})}+C_{dsj}\sqrt{(V_{ds}+0.6)})^2 \tag{4.15}$$

It is noticed that at relatively high voltage level of V_{ce}, C_{res} is almost equal to C_{gdj} because C_{gdj} is become much smaller compared with C_{oxd}. The expression of C_{res} is given as follows.

$$C_{res} \approx C_{gd} = \begin{cases} C_{oxd} & \text{for} \quad V_{ds} \le V_{ge} - V_{td} \\ C_{oxd}C_{gdj}/C_{oxd} + C_{gdj} & \text{for} \quad V_{ds} > V_{ge} - V_{td} \end{cases}, \tag{4.16}$$

where V_{ds} is the drain-source voltage drop of the MOSFET and V_{td} is the gate-drain depletion threshold voltage. According to Equation 4.16, when V_{ds} is higher than V_{ge}-V_{td}, the depletion region starts to form. When V_{ds} is lower than V_{ge}-V_{td}, the C_{gd} is equal to the oxide capacitance C_{oxd}. When the IGBT is forward biased, the voltage drop is mainly supported in the base region. Thus V_{ce} is almost equal to V_{ds}. When the depletion layer is formed at the relatively high voltage level of V_{ce}, C_{gdj} can be expressed via C_{res} as follows.

$$C_{gdj} = \frac{C_{oxd} \cdot C_{res}}{C_{oxd} - C_{res}}. \tag{4.17}$$

The drain-source depletion capacitance C_{dsj} can be also expressed via the inter-electrode capacitance as follows.

$$C_{dsj}=C_{oes}-C_{res}. \tag{4.18}$$

Usually, the IGBT data sheet provided by the device manufacturer includes the inter-electrode capacitance curve, as shown in Fig. 4.17. When V_{ce}=300 V, the capacitance curve tells that C_{res1}=144 pF, C_{oes1}=640 pF. According to Equations 4.17 and 4.18, C_{gdj}=144.9 pF and C_{dsj}=516 pF. The active device area A is directly measured to be 2.88 cm^2. Equation 4.15 is then used to calculate N_b as $1.87 \cdot 10^{14}/cm^3$ and equation 4.13 obtains A_{gd} as 0.623 cm^2. It needs to be mentioned that one implying condition for Equation is that the depletion region does not reach the buffer layer. So choosing the $V_{ce} \leq 0.5\ V_{ces}$ will usually guarantee the depletion region does not punch through the N^- base region. V_{ces} is the rated blocking voltage. V_{ce} should not be chosen to be small since the value of C_{gdj} is very difficult to obtain. When V_{ce} is quite small, the model accuracy of the inter-electrode capacitance still needs to improve in Hefner 1-D IGBT model. Different IGBT devices might exhibit much different capacitance curve shape, especially at relatively low bus voltage. Therefore it is recommended that V_{ce} should be chosen based on two principles. First V_{ce} can not be too small. In capacitance curve of any IGBT data sheet, the quick change of C_{res} and C_{oes} due to V_{ce} can usually be observed. Such a sudden change normally happens when V_{ce} is less than a few tens volts and is not modeled by Equation 4.8. Second, V_{ce} can not be too large. Too large V_{ce} may result the depletion region extend to the buffer layer region, which causes Equation 4.8 to be invalid. For most IGBT data sheets, we can found the region where the difference between the value of C_{res} and C_{oes} is nearly changed, and V_{ce} is at its medium level compared with the device's voltage rating.

With the derived values of N_b, A, A_{gd}, C_{oxd} and $C_{gs,}$ the gate-drain-overlap depletion threshold voltage V_{td} can be determined. It is shown in Equation 4.16 that the V_{td} in the 1-D physics-based

IGBT model will lead to a sharp change of the inter-electrode capacitance. In practice, the capacitance abrupt change of the IGBT device is somehow smooth. Therefore, the model presented in Equation 4.16 can be improved. The first step of deriving V_{td} is to judge the approximate range of V_{td} according to the capacitance curve. As seen in Fig. 4.17, the first slope change of the inter-electrode capacitance happens in the region of 2V-20V. Therefore, it is reasonably considered that the absolute value of V_{td} is within this range. By inputting the derived values of N_b, A, A_{gd}, C_{oxd} and C_{gs} into the IGBT model in Saber, C_{ies} can be characterized in the simulation, as shown in Fig. 4.19. Thus, V_{td} is chosen to be –9V for the studied IGBT.

3. Derive W_b.

After N_b is derived, W_b will first be derived from the maximum breakdown voltage of the IGBT. For a NPT IGBT design, the electric field is distributed in the lightly doped N- base region. The maximum electric field occurs at the junction of P+ body and N- base layer. The distribution of the electric field across the base layer is like a triangle where the peak electric field happens at the junction. When the maximum electric field reaches the critical field level E_m, the avalanche breakdown happens. More pairs of electrons and holes are generated and the device starts to lose the voltage blocking capability. The critical electric field is given in empirical expression as follows.

$$E_m = 4010 \cdot N_b^{1/8}. \tag{4.19}$$

For a NPT device, the breakdown voltage V_{br_NPT} can be expressed as follows.

$$V_{br\_NPT} = 5.34 \cdot 10^{13} \cdot N_b^{-3/4}. \tag{4.20}$$

The reach-through width at the breakdown voltage is given by the following.

$$W_{rt\_NPT} = 2.67 \cdot 10^{10} \cdot N_b^{-7/8}. \tag{4.21}$$

For a punch-through (PT) IGBT, the electric field extends to the buffer layer at the breakdown voltage. Since the slope of the electric field in the buffer layer is much steep than in the N- layer, the distribution of the electric field in the N- layer is like a rectangle. Therefore, the voltage blocking capability of a PT IGBT is higher than that of a NPT IGBT if keeping the same width and doping density of the N- layer. Still using Equation 4.19, the avalanche breakdown voltage of a PT IGBT can be approximated as follows:

$$V_{br\_PT} = E_m W_b - \frac{qN_b W_b^2}{2\varepsilon_{si}}. \tag{4.22}$$

Based on Equations 4.21 and 4.22, the relationship between the blocking voltage and the doping density of the lightly doped N- layer design is shown in Fig. 4.20. From this diagram, the information of W_b for any given breakdown voltage can be obtained. It needs to be mentioned that the actual breakdown voltage will be somehow lower than the value indicated in Fig. 4.20 due to the effects of 2-D electric field distribution such as the electrical field crowding, which is not modeled in the 1-D IGBT model. Therefore, it is suggested that 150 V to 250 V added to the actual breakdown voltage is used to derive W_b from Equations 4.19 and 4.21. We only need to limit a range of W_b instead of exactly pinpointing its value since the fine-tuning is conducted to finally decide all the IGBT model parameters. It also needs to be pointed out that the practical design of the IGBT chip may not strictly stick to the theoretical value of W_b due to the limitation of the wafer processing techniques or cost concern. For the 600V 300A PT IGBT, the minimum width of W_b is obtained as 48 um when 850 V is used as the breakdown voltage in Equation 4.21. The maximum W_b will be the NPT design value, which is 85 um for N_b=1.7·10^{14} 1/cm^3.

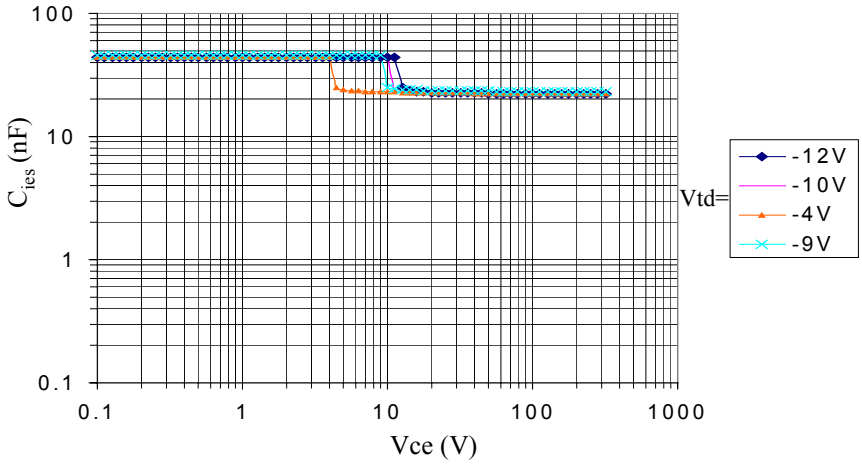


Fig. 4.19. Vtd's effects on the input capacitance Cies.

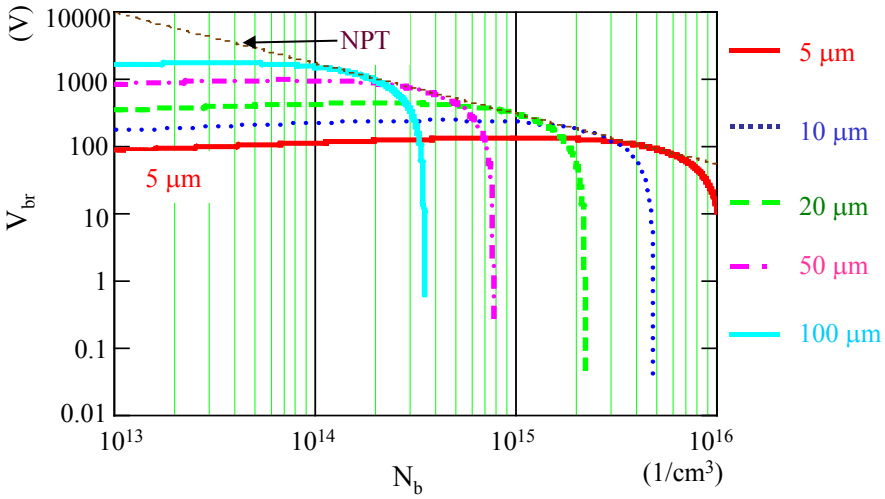
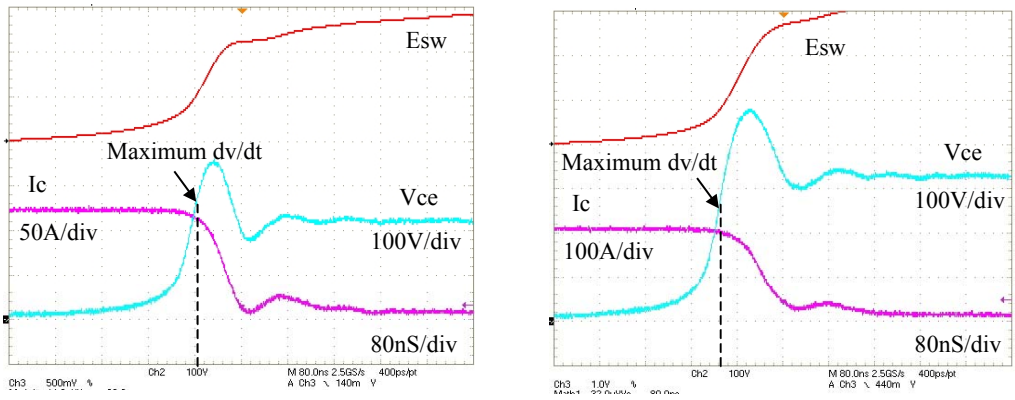


Fig. 4.20. PT IGBT breakdown voltage vs. doping density of lightly loped region.

It needs to be mentioned that the Equations 4.20 and 4.21 are actually derived for the parallel plate P-N junction. In actual devices, the junction terminations are not like the ideal parallel plates. Therefore, the electric field around the junction termination is not evenly distributed. The manufacturers have developed several techniques to make the electric filed distribution as even as possible. For example, the field rings are implemented into the junction terminations. Still, the device blocking voltage capability has to be degraded due to non-ideal electric field distribution.

Usually 80% degrading is adopted to calculate the breakdown voltage when the formula of the parallel plate P-N junction is used. In addition, usually 10% design margin is kept for the device designer. Consequently, the equivalent breakdown voltage for 600V IGBT is set to be 833 V. By solving Equations 4.19 and 4.22, the thickness of the N- layer is calculated to be 47 μm. So far the breakdown voltage information is used to derive the lower limit of the N- layer width W_b. Since the actual breakdown voltage is also related to the local electric field crowding, it is rather difficult to exactly determine the N- layer thickness. Besides the breakdown voltage aspects, the switching characteristics are used to further decide W_b. Based on the theory in [E1], the turn-off voltage rising slope reaches the maximum value when the depletion width of N- layer is half of W_b. From the turn-off waveform shown in Fig. 4.21, the maximum voltage-rising slope happens at around 270V. It indicates that the W_b has approximate reach-through voltage of 540V. This corresponds to 62-63 um width according to Equation 4.21. In fact the waveform in indicates the device does not reach through at the peak voltage of about 480V. If the device reach through the N- layer, the V_{ce} waveform will exhibits abruptly changed slope.



(a) (b)

Fig. 4.21. Turn-off switching waveforms indicating Vce's slope: (a) 200V bus and (b) 300V bus.

4. Derive the lifetime parameters: τ_{hl} and τ_{ll}.

In most practical applications, the IGBT switches under the clamped inductive load conditions. The turn-off process usually involves three periods. In period I, V_{ce} rises up while the IGBT still carries the full load current. Until V_{ce} reaches the clamped voltage V_{dc}, the rising voltage acts to reduce the MOSFET channel current with a displacement current from the base-collector junction depletion capacitance and with an increased PNP collector current I_p. In period II, V_{ce} is clamped to V_{dc} and the MOSFET channel current is quickly cut off due to the gate voltage drops below the threshold voltage. The abrupt fall of the IGBT current is observed in period II. After the initial rapid fall, the IGBT current slowly decays in period III. The 1-D IGBT model dictates that the slowly decaying current in period III can be described as follows.

$$I_T(t) = \frac{I_T(0^+)}{\left(\frac{I_T(0^+)}{I_k}+1\right)e^{t/\tau_{eff}} - \frac{I_T(0^+)}{I_k}}, \tag{4.23}$$

where I_k is an introduced variable only related to the IGBT design parameters and τ_{eff} is the equivalent time constant. The equivalent time constant τ_{eff} is given as follows.

$$\frac{1}{\tau_{eff}} = \frac{\frac{W^2}{\tau_{hl}} + \left(\frac{2D_{pl}}{D_{ph}}\right)\frac{W_{buf}^2}{\tau_{ll}}}{W^2 + \left(\frac{2D_{pl}}{D_{ph}}\right)W_{buf}^2}. \tag{4.24}$$

Although τ_{eff} is a complicated function of τ_{hl} and τ_{ll}, some approximations can be made to simplifying the process of extracting τ_{hl} and τ_{ll}. It is assumed that D_{pl}/D_{ph} is about the same for different load current. For derived N_b, the ratio is about 2 according to [E9]. When the IGBT is switched under three different voltage levels, three sets of τ_{eff} can be measured from the current

waveforms. Since there are three unknown variables τ_{hl}, τ_{ll} and W_{buf}, for these given voltages, the group of three equations can be used for solving these variables. The experimental waveforms of the IGBT turn-off need to be used to derive τ_{eff}. From Equation 4.23, the following relationship can be derived and solved to obtain the equivalent time constant.

$$\left(\frac{I_T(0^+)}{I_T(t_2)}-1\right)e^{\frac{t_1}{\tau_{eff}}}+\left(1-\frac{I_T(0^+)}{I_T(t_1)}\right)e^{\frac{t_2}{\tau_{eff}}}=\frac{I_T(0^+)}{I_T(t_2)}-\frac{I_T(0^+)}{I_T(t_1)}. \tag{4.25}$$

where t_1 and t_2 are two time instants specified in the waveforms of slowly decaying IGBT current at turn-off. One example of the turn-off waveform at 350 V for the 600V and 300A IGBT is shown in Fig. 4.22. According to Equation 4.25, τ_{eff} is calculated to be 56 nS. Since the modern IGBT turn-off speed is quite fast, the current ringing is commonly happened. Therefore, it is more appropriate to derive the τ_{eff} using the averaged current waveform. Then the curve fitting method is applied to approximate the current tail with the exponential function. As shown in Fig. 4.23, the envelope of the tail current and the average value is obtained. Then the average current data is curve fitted to get τ_{eff} as 177 nS. Similarly, τ_{eff} is derived to be 113 nS for 200V and 86 nS for 300V switching from Fig. 4.21. The neutral base layer width is calculated to be 17.13 um for 300V, 25 um for 200V and 44.2 um for 50V. Then solving equation group defined by Equation 4.24, the IGBT parameters are calculated to be: τ_{hl} =346 nS, τ_{hl} =59 nS and W_{buf}=10 um.

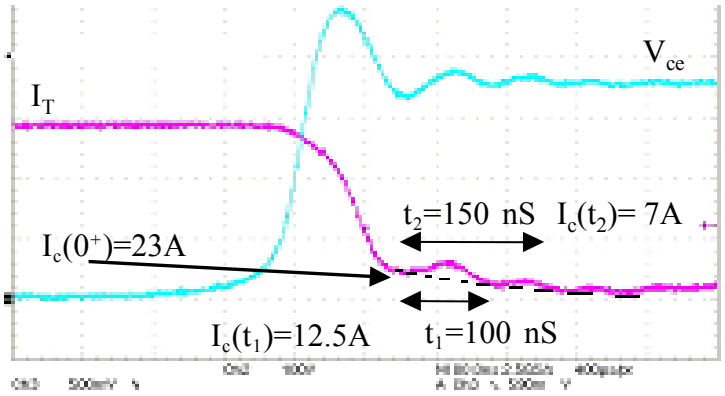


Fig. 4.22. Turn-off tail current to derive carrier lifetime.

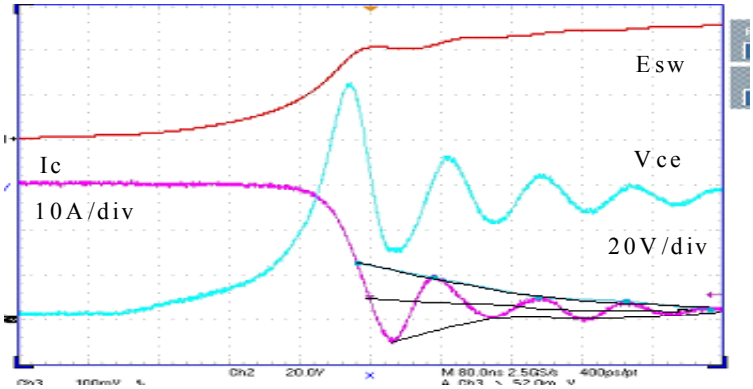


Fig. 4.23. Illustration of deriving the $\tau_{eff.}$ (80 nS/div)

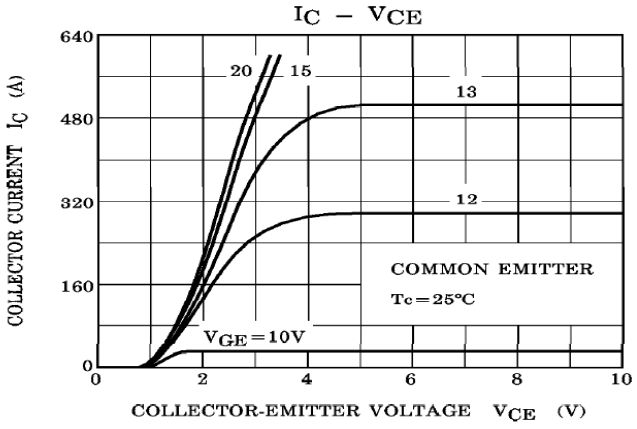


Fig. 4.24. I_c-V_{ce} relationship from the data sheet.

5. Derive K_p, K_f, θ and V_t.

From the data sheet information shown in Fig. 4.24, the limits of the internal MOSFET parameters such as K_p, θ and V_t can be extracted. Since N_b, W_b and the lifetime have been derived through step 1 to step 4, the current gain of the PNP transistor of the IGBT is approximately uniquely determined when the forward voltage is small. The current gain of the PNP transistor is mainly determined by the emitter injection efficiency and the N- layer transport ratio. For the modern IGBT devices, the emitter injection efficiency is almost unity. Thus, the transport ratio mainly decides the current gain, as expressed by

$$\alpha_T = \frac{1}{\cosh(W/L_a)}, \tag{4.26}$$

where W is the non-deplete region length and L_a is the ambipolar diffusion length. When the forward voltage at the steady state is small, the W is almost equal to W_b. The V/I transfer curve of the data sheet in Fig. 4.24 can then be used to refine the derived value of K_p, K_f, V_t and θ. According to Fig. 4.24, the IGBT saturation current is 34 A when V_{ge}=10V, 296 A when V_{ge}=12V, and 504A when V_{ge}=10V. With the derived the base layer doping and the lifetime data, the IGBT model is established in Saber. The simulation finds the current gain of I_{cp}/I_{mos} is about 0.41. Then, the following equation can be used to obtain that K_p=55.75, V_t=9.049 V and θ=0.063.

$$I_{mos}(V_{gs}) = \frac{K_p(V_{gs} - V_T)^2}{2[1 + \theta(V_{gs} - V_T)]}. \tag{4.27}$$

Then the following equation is used to derive K_f using the current information in the linear region of Fig. 4.24. Consequently, K_f is derived to be equal to 3.

$$I_{mos} = \frac{K_p K_f (V_{gs} - V_T) V_{ds} - K_p K_f^2 \frac{V_{ds}^2}{2}}{1 + \theta (V_{gs} - V_T)} \quad . \tag{4.28}$$

6. Fine-tune N_{buf}.

In modern IGBT design, there is a range of buffer layer design parameters. Usually is about 4~16 μm and is from 10^{16} to $5 \cdot 10^{17}$ 1/cm^3. If the reverse voltage is applied to the IGBT, the similar method to that used for the lightly doped base layer can be used to derive the doping and width of the buffer layer. However, most IGBT modules for the three-phase inverter operation have been packaged with an anti-paralleled diode. Therefore, it is very difficult to apply the high reverse voltage to the commercial IGBT module. The concept of fine-tuning N_{buf} is to use the simulation results to match the test waveforms. The buffer layer is used in the IGBT design to mainly modify the turn-off characteristics. Taking advantages of the function of parametric simulation of Saber, the proper range of N_{buf} and W_{buf} can be programmed into Saber simulation. Since N_b, W_b and the lifetime have been derived through step 1 to step 5, the current gain of the PNP transistor of the IGBT is approximately uniquely determined when the forward voltage is small.

With these values of K_p, K_f , V_t and θ, the simulation circuit of inductive load switching is established. Since the parasitic inductance of the bus bar and the IGBT module package affects the turn-off waveforms, the simulation circuit needs to include the parasitic inductance. The detailed parasitic extraction or modeling for the IGBT and the bus bar is explained in the following section. The general effects of N_{buf} and W_{buf} at turn-off are illustrated in Fig. 4.25. The waveforms confirm the general IGBT switching characteristics. The longer buffer layer has more

effects on the turn-off and the switching speed becomes fast. The higher doping of the buffer layer also makes the turn-off speed faster. As can be seen from Fig. 4.25, the device voltage rise time becomes smaller when the doping density changes from $2\cdot10^{17}$ to $3.5\cdot10^{17}$ 1/cm^3. For the same doping density of $3.5\cdot10^{17}$ 1/cm^3, the rise time of V_{ce} from 0 to V_{dc} increases about 30 nS when the buffer-layer width changes from 9 to 7 um. Another observation from Fig. 4.25 is the abrupt fall time of the IGBT current does not change significantly when the buffer layer design parameters vary. Since W_{buf} is determined as 10 μm in step 4, it is usually adequate to only seek proper N_{buf} value to match the experimental switching waveform. However it is still beneficial to slightly change W_{buf} around the previously derived value. After comparing the turn-off waveforms of various combinations of N_{buf} and W_{buf}, it is decided that N_{buf} =$1.4\cdot10^{17}$ 1/cm^3, and W_{buf} =10 μm.

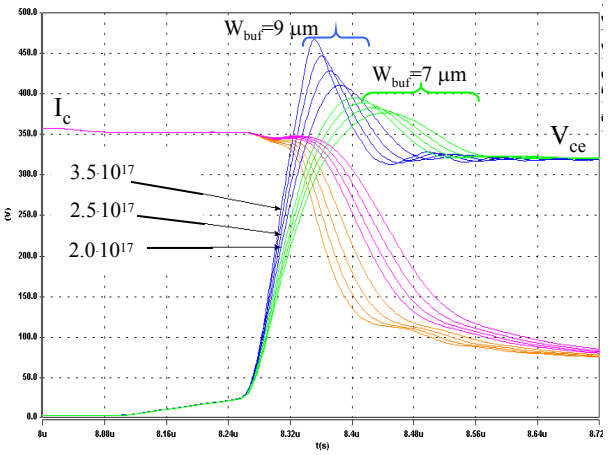


Fig. 4.25. Impacts of W_{buf} and N_{buf} on turn-off waveforms.

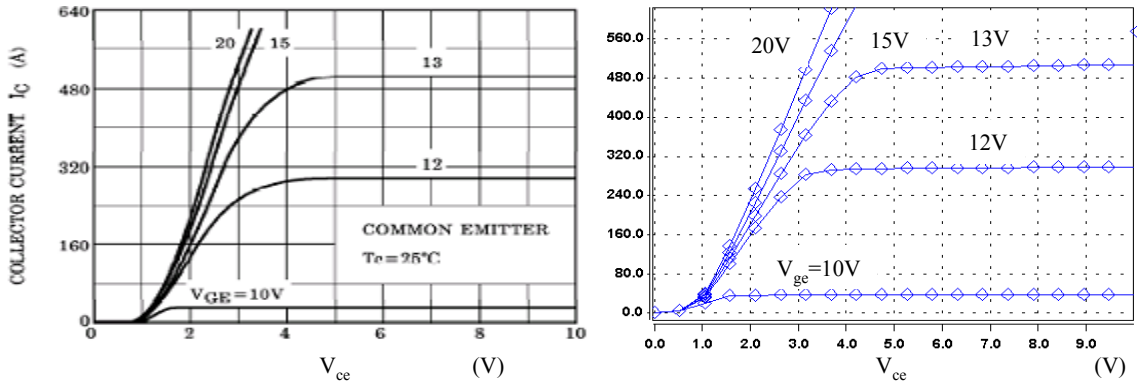
Finally, the key model parameters are listed in Table 4-3.

Table 4-3. Extracted model parameters for the 600V and 300A IGBT.

	Symbol	Value
MOS Gate	V_T	9.049 V
	K_P	55.3
	K_f	3
	θ	0.063
	C_{gs}	23.2nF
	C_{oxd}	23.2 nF
Geometry	A	2.88 cm2
	A_{gd}	0.623 cm2
PNP Transistor	N_b	1.87e14
	W_b	63 um
	N_{buf}	1.4e17
	W_{buf}	10 um
	τ_{hl}	346 nS
	τ_{ll}	59 nS

4.2.3. Comparison of IGBT Model and Data Sheet

After all the IGBT model parameters are derived with the proposed method, the key characteristics of the IGBT simulation model is extracted and compared with those of the data sheet. Fig. 4.26 shows the comparison of I_c-V_{ce} curve. The saturation current level is accurately modeled for V_{ge}=10 V, 12V and 13 V. The relationship of I_c and V_{ce} in linear region is also modeled well except at high gate voltage and high load current. Since the normal operating current is below 400A, the slight inaccuracy will not cause any issues in simulation. Another static characteristics, I_c-V_{ge}, is shown in Fig. 4.. It is clear that the developed IGBT model parameters truthfully represent the I_c-V_{ge} even at the different temperature.



(a) (b)

Fig. 4.26. Comparison of I_c-V_{ce} curve between data sheet and IGBT model. (a) datasheet and (b) IGBT model.

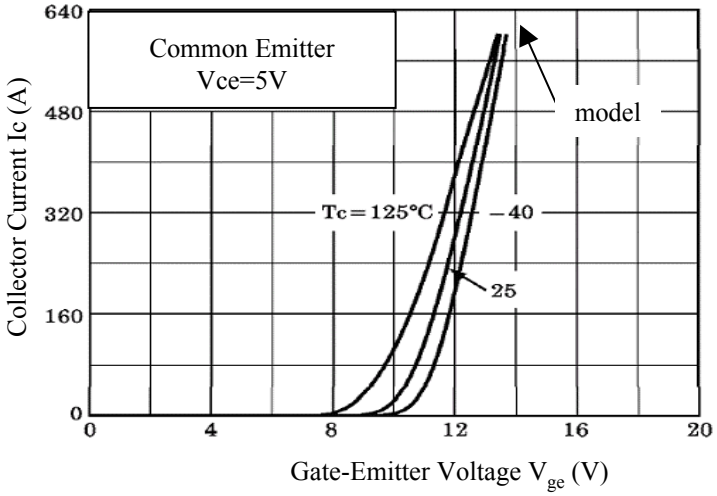


Fig. 4.27. Comparison of I_c-V_{ge} curves.

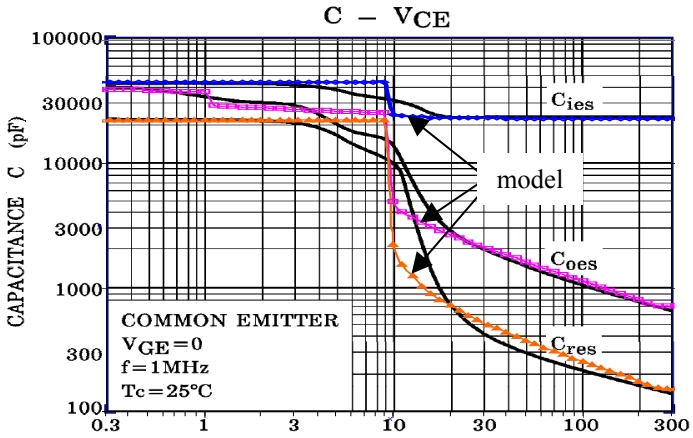
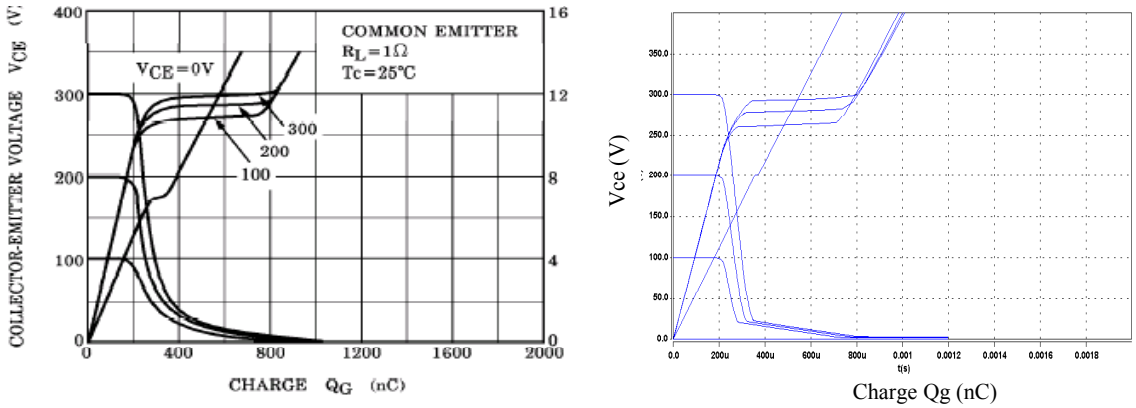


Fig. 4.28. Comparison of inter-electrode capacitance.

The inter-electrode capacitance mainly affects the switching speed. Fig. 4.28 illustrates that the developed IGBT model also exhibits the good agreement of the inter-electrode capacitance. The discrepancy between the model and datasheet is mainly around 10 V. The reason is that the 1-D IGBT model does not model the details of the capacitance variations caused by the gate-drain-overlap depletion threshold voltage V_{td}. Since the capacitance is not modeled accurately at the small portion of V_{ce} range, the switching waveforms obtained by the developed IGBT model are expected to match the actual waveforms. This is confirmed by the experimental results presented in later sections. The gate charge features are compared in Fig. 4.29. The good agreement between the simulation model and the data sheet is clearly shown.



(a) (b)

Fig. 4.29. The comparison of gate charge curve. (a) datasheet and (b) simulation model.

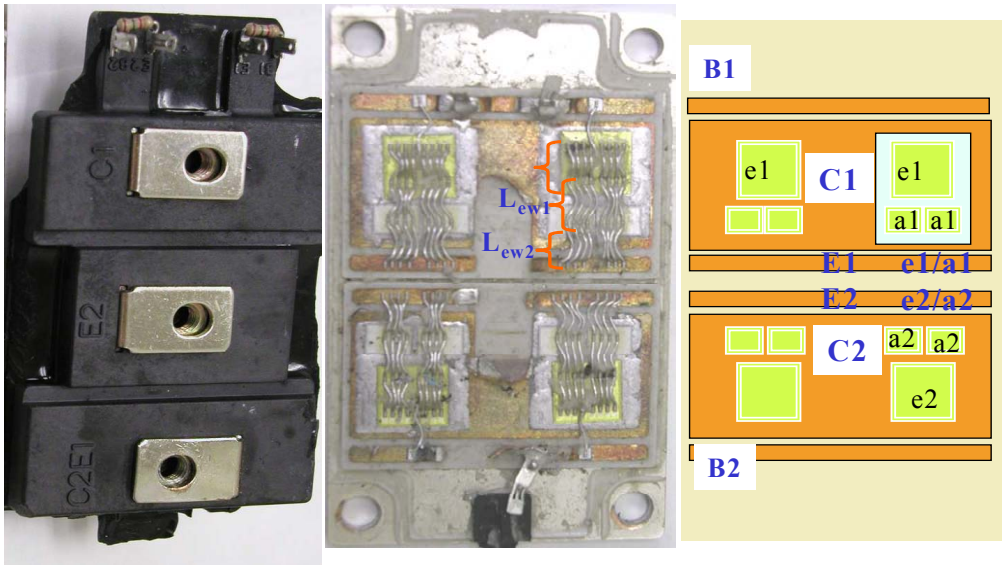
4.3. Parasitic Modeling of IGBT Module

The good device model has to be incorporated with the accurate parasitic model since the parasitic inductance, for instance, will greatly affect the switching losses and the switching waveforms. In last section, when we perform the simulation to compare the result with the experiment, one implying condition is we have already obtained the parasitic models of the

device. This section will present an impedance based measurement method to extract the parasitic inductance of the half-bridge IGBT module.

In the past, both finite-element-analysis and the measurement-based approaches have been developed by other researchers. The finite element method is too tedious for the IGBT's wire bonding package. As shown in Fig. 4.30, multiple dies form one IGBT or diode inside the plastic package. Modeling so many bonding wires itself with their geometry data is a big task. Besides the FEA method, the TDR (time domain reflectometry) based method was also proposed to derive the IGBT package parasitic. However, the model parameter derivation procedures over simplify the issue. As shown in Fig. 4.31, the filled blocks represent the missing inductance in the model. It is found the common inductance affects the turn-on dv/dt greatly. Without modeling this inductance, the correct switching waveform cannot be obtained. Two empty blocks indicate the derivation procedures assume the equal terminal inductance for C_1 and E_2, which is not true in the real IGBT packaging. In reality these inductance could be 50% different due to un-symmetric terminal or S-bend length. The arrows indicates during the derivation, couplings among two gate terminal interconnects are not modeled. To carefully consider all these effects, the targeted parasitic model structure is presented as shown in Fig. 4.32. Totally eleven parasitic inductance and two coupled inductance need to be derived. In order to derive the complicated parasitic distribution, the basic concept, three-terminal impedance network, is applied, as shown in Fig. 4.33. This indicates that for the lumped linear three-terminal network, if we can measure the equivalent Δ-connected terminal impedance, the branch impedance of Y-connected network can be directly derived. By properly measuring the three terminal network's terminal-to-terminal impedance, it is possible to derive all the parasitic inductance inside the package in Fig. 4.32.

One step-by-step method is proposed to derive all the parasitic inductance based on the measured terminal impedance.



(a) (b) (c)

Fig. 4.30. Half-bridge IGBT module and wire-bond arrangement:
(a) top view, (b) wire-bonding pattern, and (c) arrangement of die and copper pad.

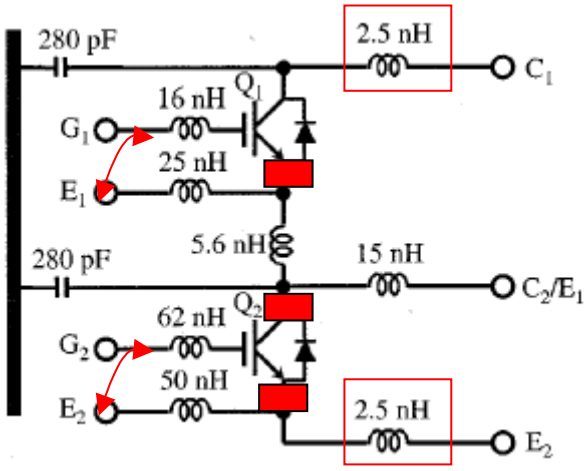


Fig. 4.31. Internal parasitic inductance assumption.

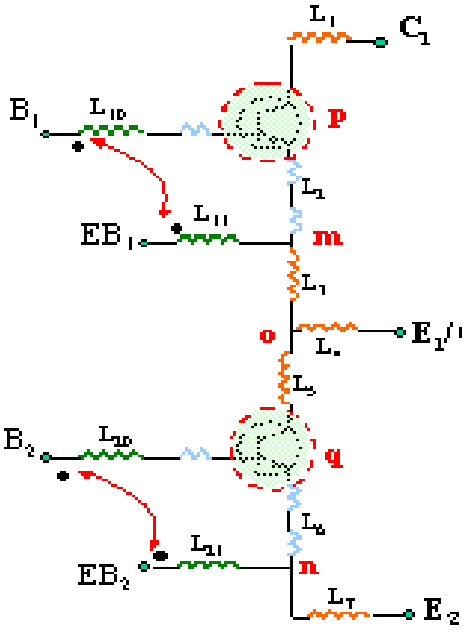
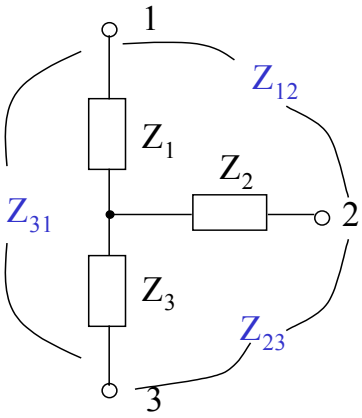


Fig. 4.32. Internal parasitic inductance distribution inside half-bridge module.



$$Z_1 = \frac{Z_{12} + Z_{13} - Z_{23}}{2}$$

$$Z_2 = \frac{Z_{12} + Z_{23} - Z_{31}}{2}$$

$$Z_3 = \frac{Z_{31} + Z_{23} - Z_{12}}{2}$$

Fig. 4.33. Δ-connected terminal impedance to derive internal Y-connected impedance.

The procedure is illustrated in Fig. 4.34. Step 1, measure the terminal impedance of the three-terminal network formed by three terminals C_1, E_1/C_2 and E_2. The impedance result of Z_{C1E2} is shown in Fig. 4.35 and the bottom device terminal impedance is shown in Fig. 4.36. Since there is zero DC voltage applied to the IGBT module, the IGBT's C_{oes} is in series due to two IGBT

devices in one module package. Therefore, the total inductance across C_1 and E_2 is 60.37 nH. After obtaining three across-terminal impedances, the inductance of L_4 can be uniquely determined as 18.05 nH. The inductance value of L_{c1o} and L_{oE2} is also obtained.

Step 2, measure the impedance of the network formed by B_1, C_1 and E_1/C_2. The inductance of L_1 is determined as 21.2 nH. The self-inductance of L_{10} is obtained as 26.3 nH. Based on L_{c1o} and L_1, $L_{po}= L_2+ L_3$=5 nH.

Step 3, measure the impedance of the network formed by EB_1, C_1 and E_1/C_2. The self-inductance of L_{11} is derived as 39.95 nH. Based on L_{c1m}, L_2 is derived as 1 nH. Then L_3 is calculated to be 4 nH.

Step 4, measure the total impedance of B_1 to EB_1. Since the self-inductance has been derived for L_{10} and L_{11}, the coupled inductance can be easily calculated to be 3.38 nH.

By performing four steps of measurement and derivation, all the parasitic inductance related to the top IGBT of a half-bridge module have been extracted. During the measurement, it is found that the across-terminal impedance can be easily measured when there is IGBT die in between. If only wire or copper bend inductance exist between two terminals, the impedance measurement is prone to noise. Therefore, it is recommend not to use the impedance of only the inductance, for example the impedance of EB_1-E_1/C_2. Indeed, the previously explained procedure does not use the impedance of EB_1-E_1/C_2 in step 4.

Applying similar sequence to the bottom IGBT, the parasitic inductance of the bottom device can also be derived. Besides the parasitic inductance, the stray capacitance between semiconductor die and the base plate is important for the CM noise generation. Most current packaging technique has the collector side of the IGBT die directly soldered onto the direct-

bond-copper since the collector is at the bottom side of an IGBT wafer. The emitter of the IGBT die usually is bonded onto the copper pad via the aluminum wire since the emitter terminal is located on the top of the wafer. Based on these understandings, the stray capacitance distribution is presented in Fig. 4.37. It is noted that when measuring the capacitance from any IGBT package terminal to the base plate, the sum of these capacitance value is always measured. The reason is that the IGBT inter-electrode capacitance is quite large as compared with the stray capacitance. For example, C_{oes} of the 600V 300A IGBT is about 40 nF and the stray capacitance of die to the base plate is in the range of hundreds of pF. Therefore, IGBT dies are equivalently shorted when measuring the capacitance from the IGBT terminal to the base plate. In fact, no matter whether two or three IGBT terminals are shorted or not, the measured capacitance value between the terminal and the base plate is always about 318 pF. Then according to the area of copper pad associated with the die terminal, the stray capacitance can be calculated accordingly. The final obtained parasitic model of the 600V and 300A IGBT module is shown in Fig. 4.38. It can be seen that the parasitic inductance associated with wire bonding only composes of the small percentage of total parasitic inductance. This suggests that the paralleling several bonding wire effectively reduces the inductance. On the other hand, the major portion of the parasitic inductance is caused by the terminal interconnect, for example S-bend. It is expected the new packaging techniques will reduce the parasitic inductance by properly designing the terminal interconnects.

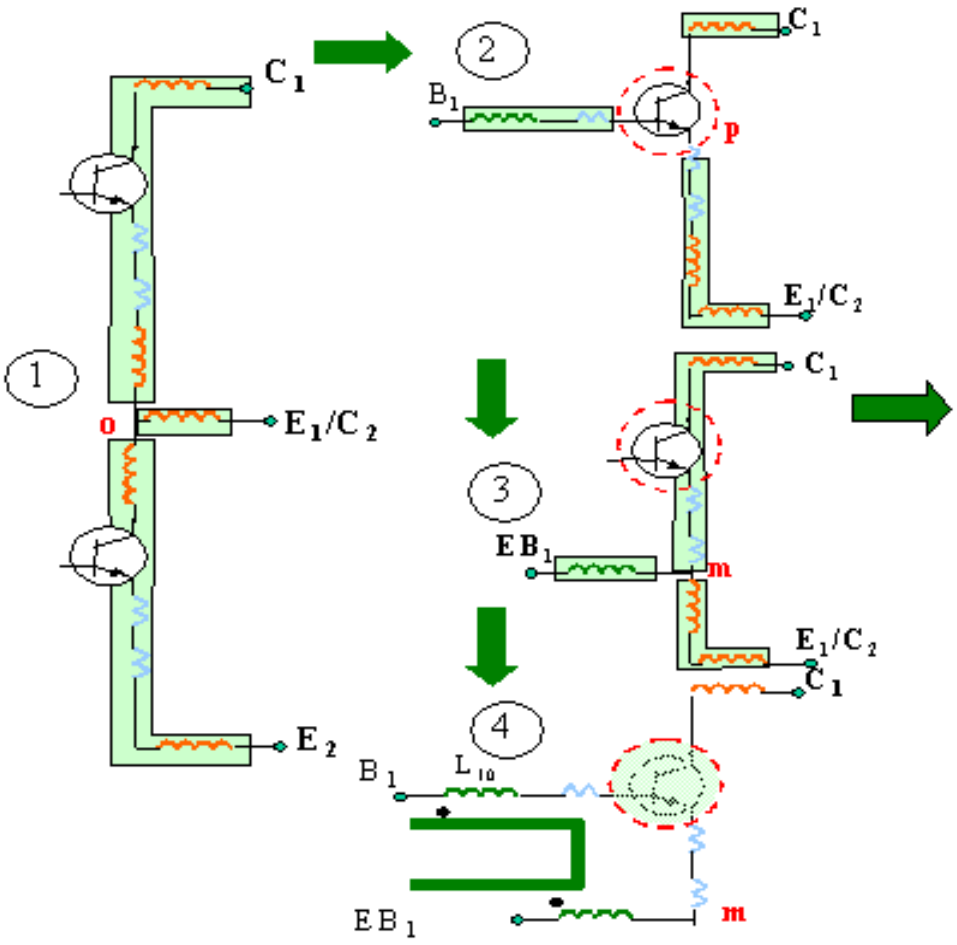


Fig. 4.34. Measuring procedure to identify the parasitic inductance.

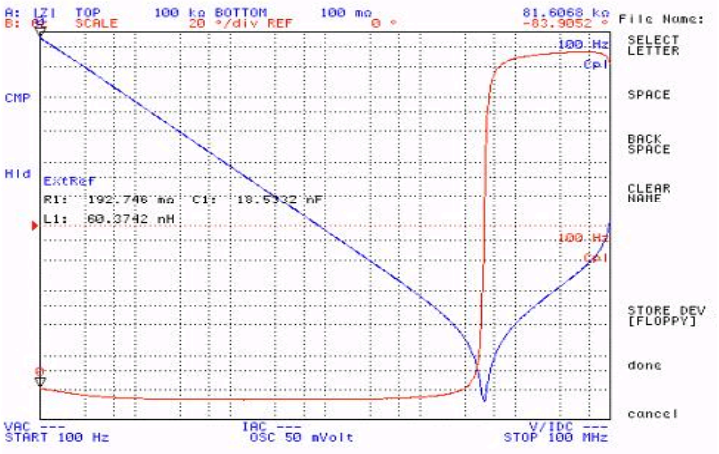


Fig. 4.35. Impedance measured across C_1 and E_2.

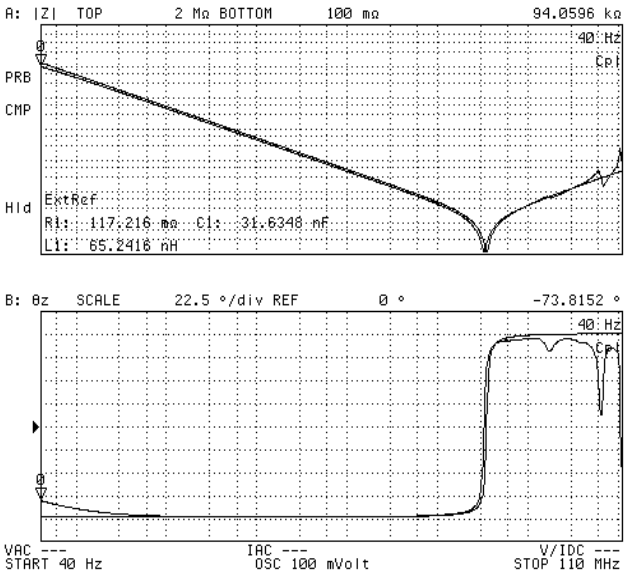


Fig. 4.36. Impedance measured across C_1 and E_1/C_2.

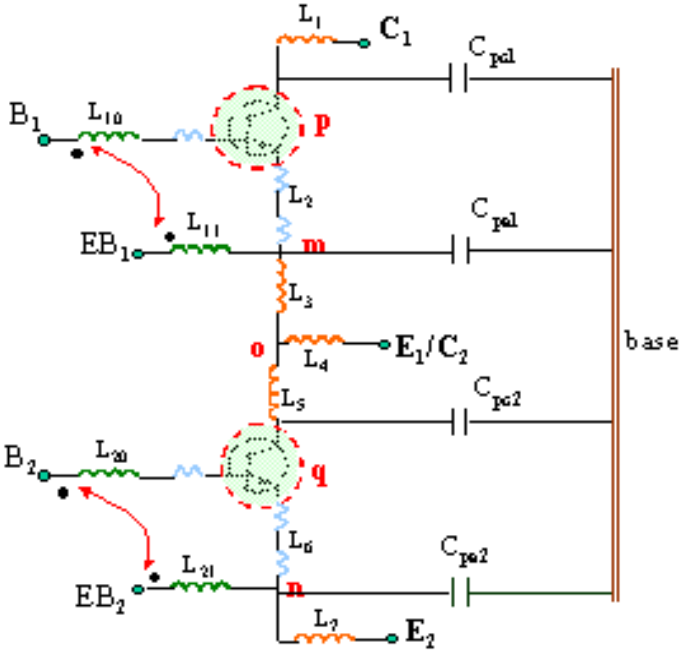


Fig. 4.37. Complete parasitic distribution of half-bridge IGBT module.

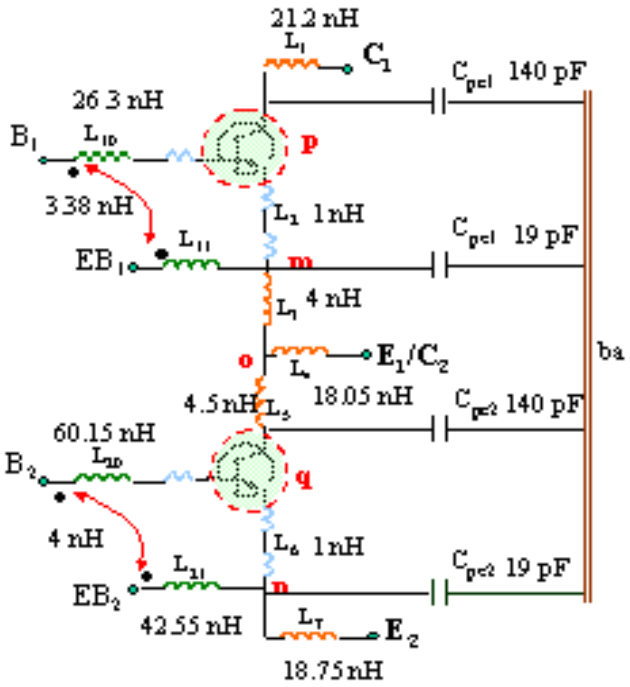


Fig. 4.38. Parasitic parameter inside the half-bridge IGBT module.

4.4. Experimental Verification of IGBT Simulation Model

The single-leg chopper circuit using the MG300J2YS50 is implemented. The circuit is operated with the double-pulsed mode to measure the switching waveforms and the switching losses. The LISN is also inserted between the chopper and the DC power supply to measure the EMI noise. Meanwhile, with the developed IGBT model and the packaging parasitic model, the saber simulation circuit is established for the tested single-leg chopper. The electrolytic capacitor is modeled using the measurement results from the impedance analyzer HP4195A. The equivalent circuit of the bus bar between the DC bus terminals and the IGBT device terminals are also derived from the measured impedance from HP419A.

A single-leg test circuit is established, as shown in Fig. 4.39. When studying the EMI noise, the LISN is connected into the circuit. When studying the switching waveforms and stress, the

LISN is disconnected and a 7 mm high copper washer is inserted between the laminated bus plate and the IGBT module so that the current probe can be used to measure the device current. To compare the switching waveforms, the model of the planar bus bars can be simplified to one phase with couplings between positive and negative bus plates. In test setup, the double pulses with very low repeating frequency (a few Hz) are applied to the gate driver of the bottom IGBT. The first pulse is used to control the IGBT current level and the second pulse is used to turn on or turn off the IGBT at the specified current level. In simulation, the ideal current source is used to emulate the inductor current level in the real test. The capacitor bank is composed of four electrolytic and four polypropylene capacitors. The impedance of each capacitor is measured using the impedance analyzer and R-L-C series circuit is applied to model the capacitor. The small inductance between capacitors in the actual setup via the copper bus is also estimated. The cable inductance is measured. In the test setup, the wires connecting LISN and bus bars are twisted together to reduce the effective inductance. Since the real layout of the cables are very flexible, one common position is assumed to measure their impedance. It is found via simulation that the cable inductance has little effects on the EMI noise level.

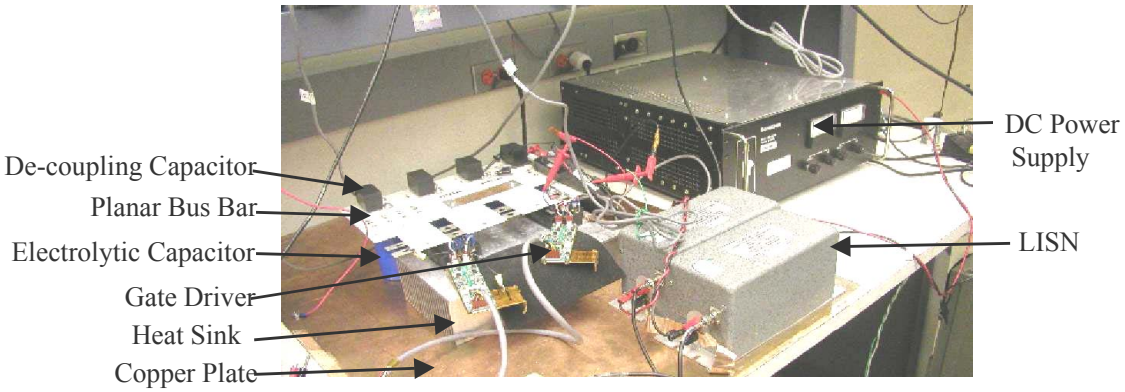


Fig. 4.39. Single-leg chopper test setup.

When studying the EMI noise, the LISN is connected into the circuit. When studying the switching waveforms and stress, the LISN is disconnected and a 7 mm high copper washer is inserted between the laminated bus plate and the IGBT module so that the current probe can be used to measure the device current. To compare the switching waveforms, the model of the planar bus bars can be simplified to one phase with couplings between positive and negative bus plates. In test setup, the double pulses with very low repeating frequency (a few Hz) are applied to the gate driver of the bottom IGBT. The first pulse is used to control the IGBT current level and the second pulse is used to turn on or turn off the IGBT at the specified current level. In simulation, the ideal current source is used to emulate the inductor current level in the real test. The capacitor bank is composed of four electrolytic and four polypropylene capacitors. The impedance of each capacitor is measured using the impedance analyzer and R-L-C series circuit is applied to model the capacitor. The small inductance between capacitors in the actual setup via the copper bus is also estimated. The cable inductance is measured. In the test setup, the wires connecting LISN and bus bars are twisted together to reduce the effective inductance. Since the real layout of the cables are very flexible, one common position is assumed to measure their impedance. It is found via simulation that the cable inductance has little effects on the EMI noise level.

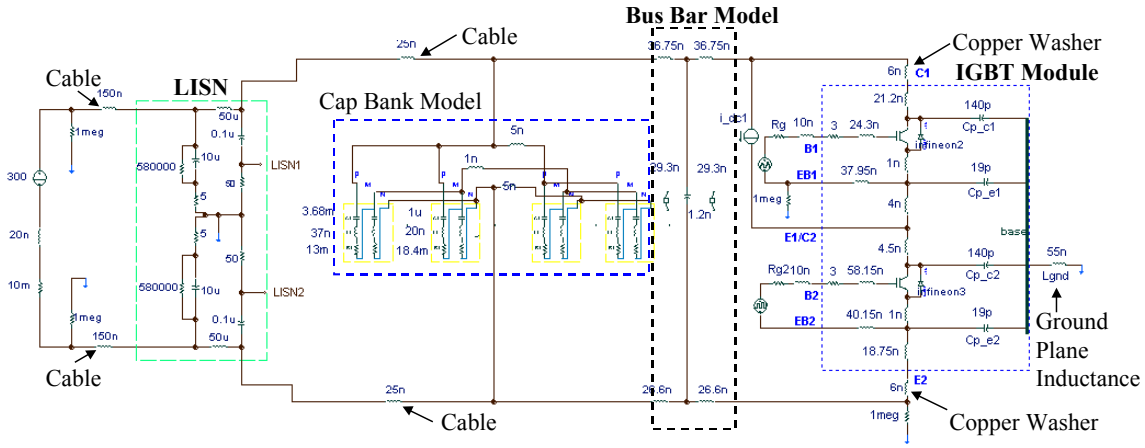
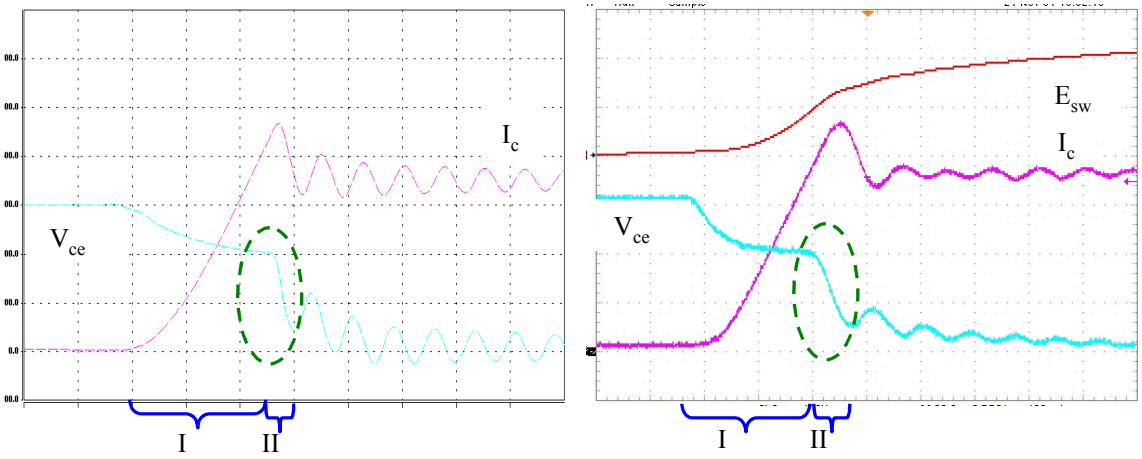


Fig. 4.40. Single-leg simulation model in saber.

First the simulation is performed to compare the switching waveforms. The purpose of this is to verify the accuracy of the IGBT model and the parasitic models. The corresponding simulation circuit is developed using the models explained in preceding sections, as depicted in Fig. 4.40. It is noted that the attention needs to be paid to the diode model. Although Saber provides a diode-modeling tool to establish the diode model according to the feature of the forward voltage drop, the junction capacitance and the reverse recovery current, the model is not accurate enough to reflect the diode reverse recovery. As shown in Fig. 4.41, even with the correct di/dt during the turn-on transition in period I, the dv/dt in simulation is quite different from that in test for period II. During period I, the conducting diode is still on. Thus the IGBT current rises and causes the voltage drop across the parasitic inductance. Consequently, the voltage of the device that is turned on starts to decrease in period I. Simulation reproduces the similar voltage drop across the device and the similar di/dt. This indicates the model of the IGBT and the parasitic inductance is correct. However, the simulated device voltage is quite different from the experimental results during period II, in which diode starts to reverse recover. It is found that the diode model established through the Saber diode tool has one common feature that

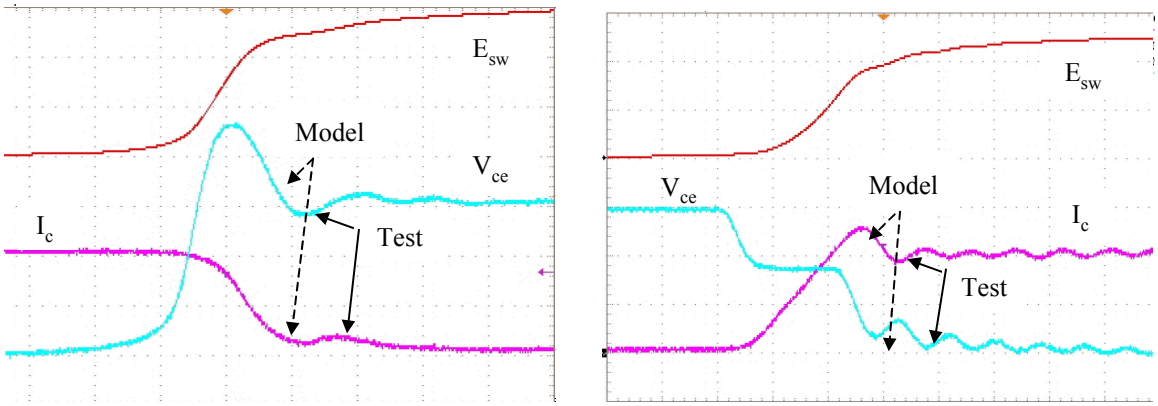
the diode voltage starts to block only when its reverse recovery current reaches its peak value. The actual test results reveal that the practical diode recovers before its current reaches the negative peak. The reason for this is that the Saber's diode model does not consider the transit time of the minority carrier during the reverse recovery. If considering the transit time effect, some minority carriers recombine before the diode current reaches its negative peak value. After surveying the existing diode models, a diode model developed by Infineon is adopted. This diode model was developed for Pspice. The author translates this Pspice diode model into Saber and develops the parameters. The detailed diode model template in saber is listed in Appendix A.

After adopting the diode model from Infineon, the comparison of the switching waveforms when the gate resistor is 2 Ω is shown in Fig. 4.42. For turn-on and turn-off transitions, the simulated waveforms match the experimental results quite well. Although the Infineon diode model achieves better reverse recovery waveforms than Saber diode model, the current ringing amplitude of simulation has some deviation from the test results at turn-on. The main reason is that the diode model parameters still need to be refined since there is no systematic approach to extract the parameters for the Infineon diode model. From the switching losses viewpoint, the accuracy achieved in Fig. 4.42 should be enough. To further verify the accuracy of the simulation model, the switching waveform comparison with a 4 Ω gate resistor is shown in Fig. 4.43 and Fig. 4.44. The switching waveforms and the switching losses from simulation agree with that from experiment. Therefore, the developed parameter extraction method and the IGBT parasitic extraction scheme have been verified to be effective in predicting the switching waveforms and the switching losses. The Infineon diode model is demonstrated to be accurate in modeling the diode reverse recovery characteristics.



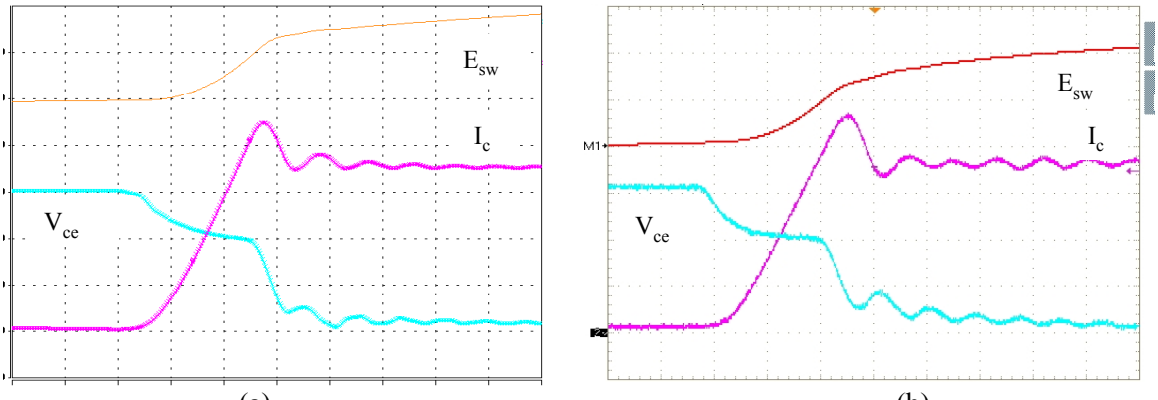
(a) (b)

Fig. 4.41. Comparison of turn-on waveforms when using Saber library diode: (a) simulation and (b) test. (50 A/div, 100 V/div and 80 nS/div).



(a) (b)

Fig. 4.42. Switching waveform comparison at Rg=2 Ω: (a) turn-off and (b) turn-on. (50 A/div, 100 V/div, 80 nS/div)



(a) (b)

Fig. 4.43. Turn-on waveform comparison at Rg=4 Ω: (a) simulation and (b) test.

(50 A/div, 100 V/div, 80 nS/div)

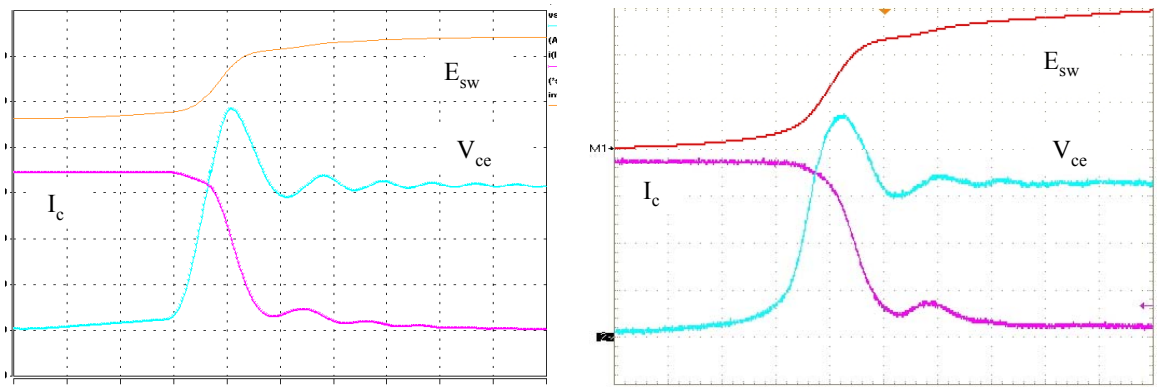


Fig. 4.44. Turn-off waveform comparison at Rg=4 Ω: (a) simulation and (b) test.
(50 A/div, 100 V/div, 80 nS/div)

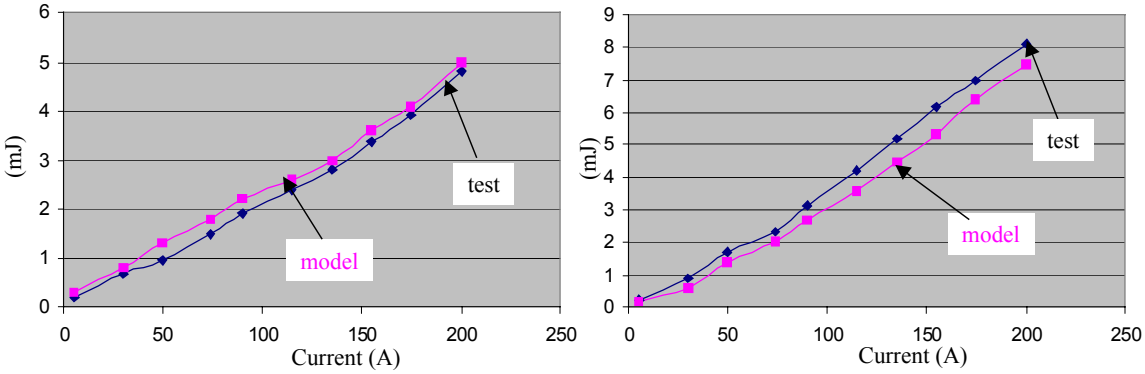
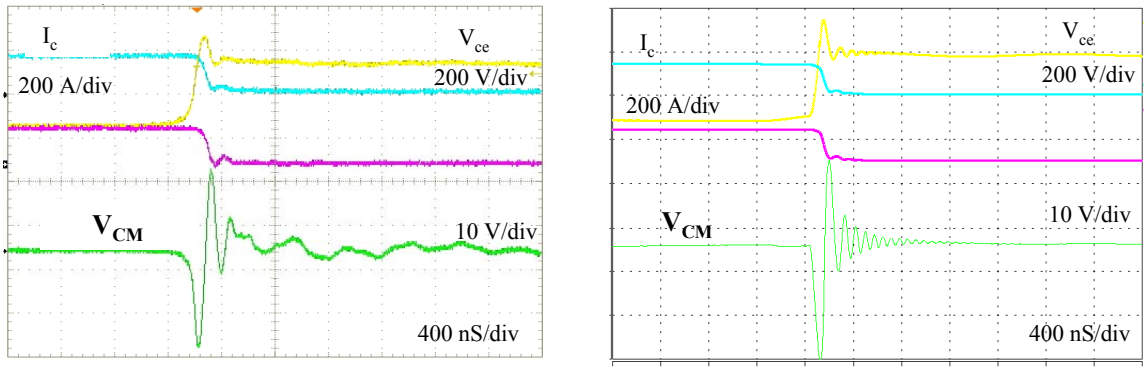


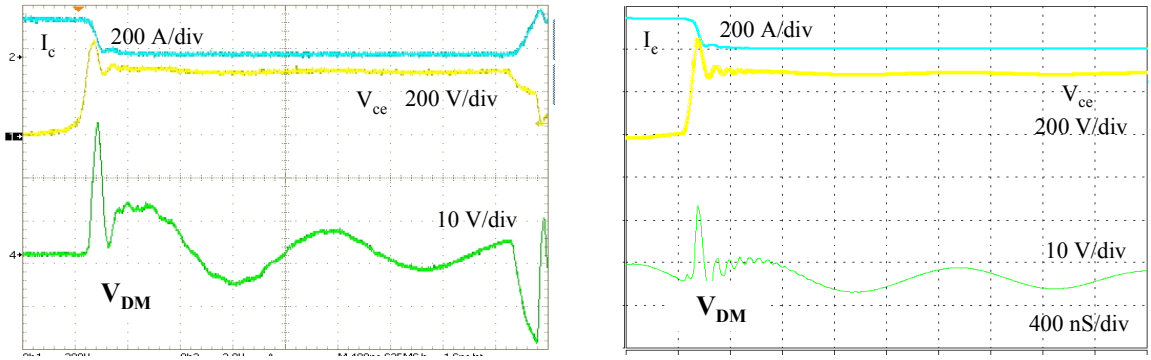
Fig. 4.45. Switching loss comparison. (a) turn-on losses and (b) turn-off losses.

Since the switching waveforms without LISN is quite accurate based on the simulation model, it is expected the EMI noise prediction with LISNs can be also accurate. In the past, researchers often verify the EMI noise prediction only from the noise amplitude spectrum. Since the spectrum is an overall aspect, it is difficult to figure out the exact details if mismatch between model and test exists. We decide to take a more rigorous step to compare the simulation model and the test results. The EMI noise waveforms in time domain are directly measured and compared.



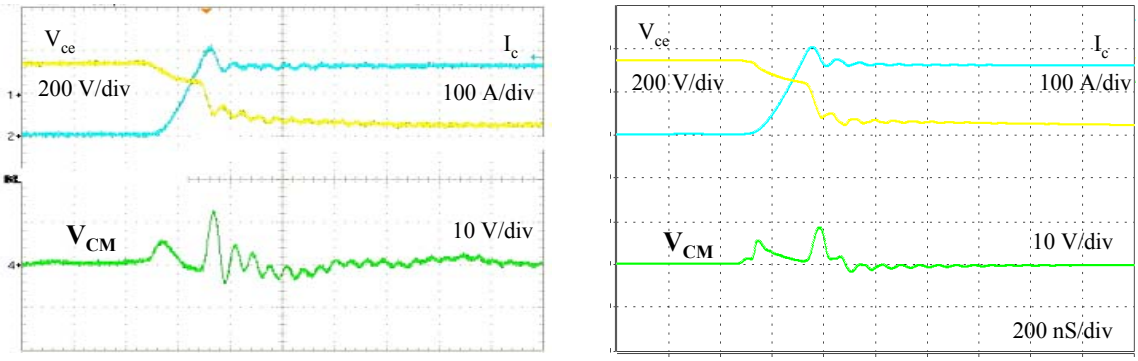
(a) (b)

Fig. 4.46. Comparison of CM noise waveforms at turn-off: (a) test and (b) simulation.



(a) (b)

Fig. 4.47. Comparison of DM noise waveforms at turn-off: (a) test and (b) simulation.



(a) (b)

Fig. 4.48. Comparison of CM noise waveforms at turn-on: (a) test and (b) simulation.

It can be seen from Fig. 4.46 that the device voltage rise at turn-off causes the CM noise and the voltage spike portion also generates severe CM noise due to the fast dv/dt. Since the voltage spike is related to the switching speed and the parasitic inductance, reducing parasitic inductance

will decrease the CM noise at turn-off. The simulation results matches the major spike part of the CM noise well because the dv/dt is modeled correctly. The high frequency ringing is also reasonable. However, 1-2 MHz CM voltage ringing is not modeled well. Since the switching waveforms are predicted well, it is believed that the modeling of the CM noise path is not quite accurate.

It can be seen from Fig. 4.47 that the DM noise at the turn-off is predicted well in the simulation. The spike of the DM noise current is due to fast switching of IGBT and the capacitor bank is not capable of providing such a fast change of the DC bus current. Therefore, it appears at the LISN side. The low frequency component of DM noise is mainly caused by the characteristics of the capacitor bank. The good agreement between simulation and test indicates that the model of the capacitor bank is accurate.

From Fig. 4.48, it is clear that both decrease stage of the device voltage leads to the CM noise. The voltage drop due to the voltage across the parasitic inductor, which is slow in dv/dt, corresponds to the relatively low noise current spike. The fast decrease of the device voltage is because of the diode reverse recovery. Therefore, the fast recovery diode may cause high CM current spike due to its high dv/dt. Considerable high frequency CM noise current is observed. These ringing current is the result of resonance between the junction capacitance of diode and the IGBT and the parasitic inductance in the commutation loop. High reverse recovery current implies higher ringing amplitude. The acceptable accuracy of the turn-on dv/dt is achieved in the simulation. The turn-on di/dt is modeled fairly accurate. Therefore, the DM noise at turn-on is predicted well via the simulation, as shown in Fig. 4.49.

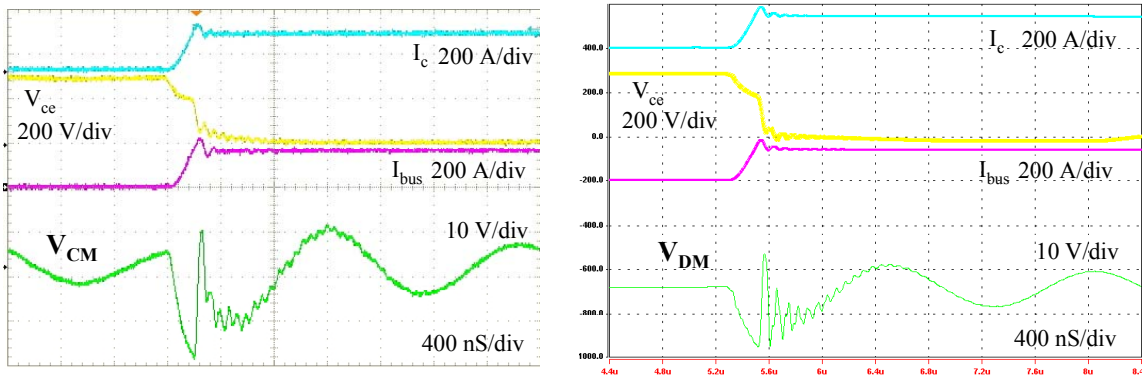


Fig. 4.49. Comparison of DM noise waveforms at turn-on: (a) test and (b) simulation.

4.5. Summary

In this chapter, an effective electrical simulation modeling approach for the IGBT device is proposed. The important modeling methods include a new parameter extraction scheme for the 1-D physics-based IGBT simulation model and an impedance-based parasitic extraction scheme for half-bridge IGBT module. The new parameter extraction scheme is much simpler as compared with existing schemes, and can facilitate building the advanced IGBT model in Saber simulation. Comparison of the gate charge, the inter-electrode capacitance, Ic-Vge curve and Ic-Vce curve between the device data sheet and the simulation model has clearly shows the proposed IGBT model parameter extraction procedures can effectively build the device matching the data sheet characteristics. Besides the comparison of the IGBT characteristics specified in the data sheet, the experimental circuit is developed to rigorously compare the dynamic switching waveforms with the simulation results.

The simulation model of the single-leg test circuit utilizes the important parasitic parameters obtained by the proposed impedance-measurement based extraction method. The very detailed

information of the parasitic inductance and capacitance inside the popular half-bridge IGBT module can be accurately derived. Together with the equivalent bus bar modeling and the corresponding capacitor bank modeling, the single-leg simulation circuit is established for the cases with and without the LISN. The extensive experiment and simulation in single-leg and there-phase inverter level confirms the validity of proposed IGBT model parameter extraction schemes and the parasitic modeling approach. As a conclusion, the proposed IGBT modeling approach has been demonstrated to be able to predict the electrical stress, the switching losses and the EMI noise level. In the next chapter, the complete simulation model of the three-phase inverter will be developed to further analyze the performance of the soft-switching inverters.

Chapter 5. Electrical Modeling and Analysis of Three-phase Inverter

5.1. Introduction

Since the IGBT device model has been developed in Chapter 4, it is a natural step to further develop the three-phase inverter simulation model in order to quantitatively analyze the performance effects of the soft-switching inverter operation. Although the significance of the accurate device model has been fully demonstrated in Chapter 4, the electrical simulation of the three-phase inverter needs more modeling work. One dominating research task is to model the laminated bus plates, which are often used in the inverter application and connects the DC power source and the IGBT devices. Since the three-phase operation differ much from the single-leg test circuit in terms of interactions among different phase legs, the parasitic inductance and capacitance of a three-phase planar bus bar needs to be properly modeled to reflect the coupling effects.

Therefore, this chapter is arranged as follows. First, the finite-element-analysis (FEA) is conducted via the Maxwell software simulation and the three-phase planar bus bar is modeled as a linear multi-terminal network. This new modeling concept is different from the conventional total equivalent impedance circuit model. The coupling effects among different phases can be accurately represented by the partial element equivalent circuit (PEEC) and the better accuracy is achieved as compared with the lumped π type circuit. Then the electrical simulation model is systematically developed for a three-phase hard-switching inverter. Through the extensive

simulations and experiments, the accuracy of the simulation modeling approach for the three-phase inverter is fully verified in wide conducted EMI noise spectrum. The much better EMI noise prediction of the three-phase inverter has been achieved compared with the current state-of-art. Based on the parametric study, the three-phase simulation model then is used to summarize the key EMI features of the three-phase inverter operation. Because the hardware implementation of 55 kW inverters in Chapter 3 has all included an EMI filter in the power stage, the direct modeling is difficult due to the particular challenges of modeling the EMI filter. Since the inverter modeling approach and the major EMI noise characteristics are verified via a newly developed inverter without the EMI filter, the analysis is extended to the 55kW hard-switching inverter. Besides the EMI aspects, the losses of the 55 kW inverter are evaluated via the simulation model. The satisfactory results have been achieved.

Third, the model of the three-phase ARCP inverter is developed and the conducted EMI noise characteristics are summarized. Although Chapter 3 has experimentally shown that the ARCP inverter can achieve the EMI noise reduction in certain frequency region, the insightful analysis from the detailed circuit simulation is not provided. It is worthwhile to use the simulation model to further analyze the effect of the ARCP inverter on the conducted EMI noise. It is noted that the experimental results obtained from Chapter 3 are with the EMI filter on the DC link, the EMI filter effects have been included in the measurement results together with the soft-switching operation's effect. To focus on the soft-switching inverter, the simulation model for the ARCP inverter is developed without the EMI filter. To model the EMI filter and study its actual attenuation in a three-phase inverter is out of scope of this dissertation. The three-phase

ZCT inverter is also developed. The simulation results are used to make insightful analysis of the experimental results.

The efficiency evaluation in Chapter 3 has indicated that at small power EV applications, the soft-switching inverters do not show the benefit since the IGBT devices already exhibits the dominant conduction loss components. Although the switching loss reduction in the main phase legs has been demonstrated, its impact on the thermal management reduction can not be significant due to small percentage of loss saving. The EV applications cover wide power rating range and the inverter designs possible have different bus voltage selection and use different power devices. Therefore, it is impossible to implement the soft-switching inverters for each inverter design and conduct the experiment. The significance of the accurate simulation model is that we can use the model to evaluate the loss reduction scenario for different inverter designs. Usefulness of the model in terms of extending evaluation to other EV applications is demonstrated through the example of inverter design at 300 kW. It is extremely difficult to exhaust the modeling efforts for all EV applications since too many EV ratings and many inverter design options exist. Application engineers can apply the proposed modeling method to develop the hard-switching inverter and the soft-switching model for their specific application. It is expected the quantitative performance comparison can be obtained through the simulation models instead of the time-consuming hardware prototyping process.

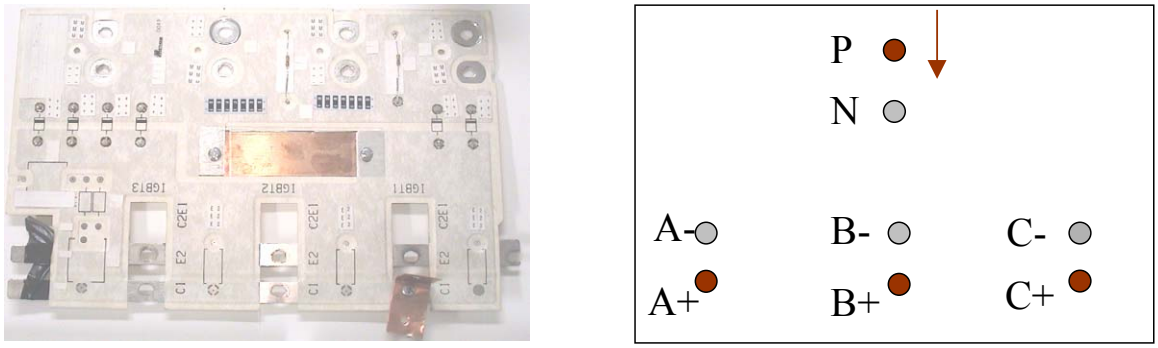
5.2. FEA Based Modeling of Three-phase Planar Bus Bar

Usually the laminated bus plate is used in three-phase inverter applications since it can effectively reduce the loop inductance. In the past, the common practice of treating these bus

bars as a lumped parameter group such as L-C network. Different phases share the same lumped parameter network in the simulation circuit or different phases use purely independent lumped network. Only the end close to the DC power supply is connected together. With FEA tools becomes more time efficient in recent years, it is appropriate to re-examine the bus bar model. Here, the bus bar is modeled as a linear network with couplings between different phases. A laminated bus plates for a three-phase inverter is shown in. The total thickness of the bus bar is less than 6 mm. There are 8 input terminations for connecting four electrolytic capacitors. Two in series form a bank and then two banks are in parallel. For the purpose of simplifying the analysis, only one pair of capacitor terminals P and N are shown in Fig. 5.1 (b). A+, B+ and C+ stand for the C_1 terminal of each phase leg. A-, B- and C- stand for the E_2 terminal of each phase leg. The FEA analysis of the current distribution on the bus bar, using MAXWELL 3-D, is shown in Fig. 5.2. For the vector (1,0,0), the net DC bus current is equal to the phase A current, flowing from P to A+ on the P bus plane. For the vector (0,1,0), the net DC current is equal to the phase B current, flowing from B- to N on the N bus plane. Obviously, the bus current distribution is quite different under different voltage vectors. The relative position of the sourcing current path and the return current path in the bus plates are depending on the load current direction and the type of the voltage vector. Even for the same load current, applying different vectors cause different bus current flowing paths, as shown in Fig. 5.3. To correctly model the current distribution requires accurately modeling the impedance of the current path. Since the planar bus bar usually has the low permeability insulation material between the two plates, the bus bar can be considered to be electrically short. The three-phase planar bus bar is modeled as a lumped time-invariant linear network, as shown in Fig. 5.4. It is an eight-terminal

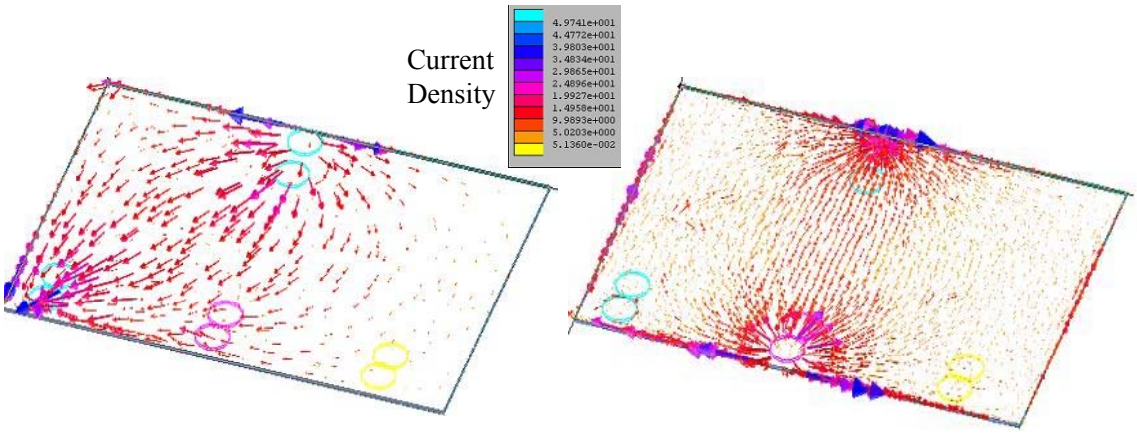
linear network and its inductance matrix is illustrated in Fig. 5.5. Six branches are considered to model the couplings among different current paths. L_{ii} represents the self-partial inductance and L_{ij} stands for the mutual partial inductance.

Maxwell Q3D can be used to directly extract the inductance matrix. For the positive bus conductor, A+, B+ and C+ are defined as the source terminals and P terminal is the sink terminal. For the negative bus conductor e, A-, B- and C- are defined as the source terminals and N terminal is the sink terminal. The resultant inductance matrix is shown in Fig. 5.6. Maxwell Q3D is also used to extract the total capacitance between two laminated bus bars. In the final model of the planar bus bars, the capacitance is evenly distributed into three lumped capacitors, as shown in Fig. 5.7.



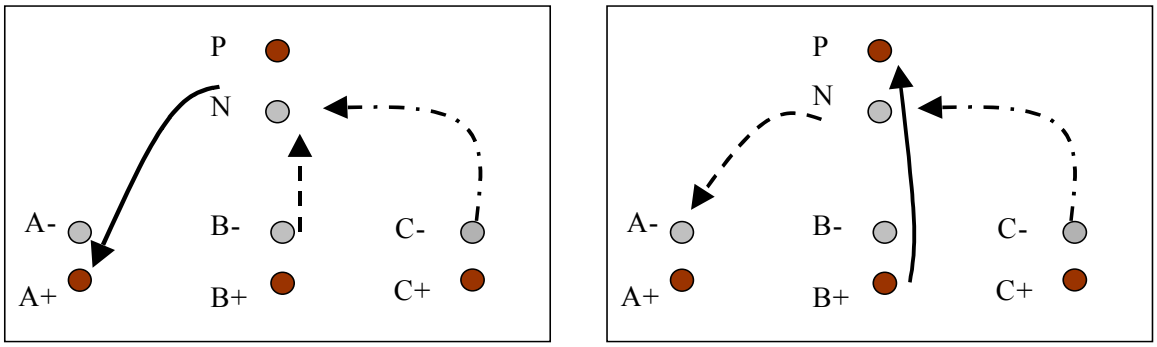
(a) (b)

Fig. 5.1. Laminated bus plate and its electrical terminal representation:
(a) Implementation of three-phase bus bar, and (b) terminal representation.



(a) (b)

Fig. 5.2. Current distribution on the laminate bus bar: (a) Vector (1,0,0), and (b) vector (0,1,0).



(a) (b)

Fig. 5.3. Current flowing path changes over the applied vectors: (a) vector (1,0,0), and (b) vector (0,1,0).

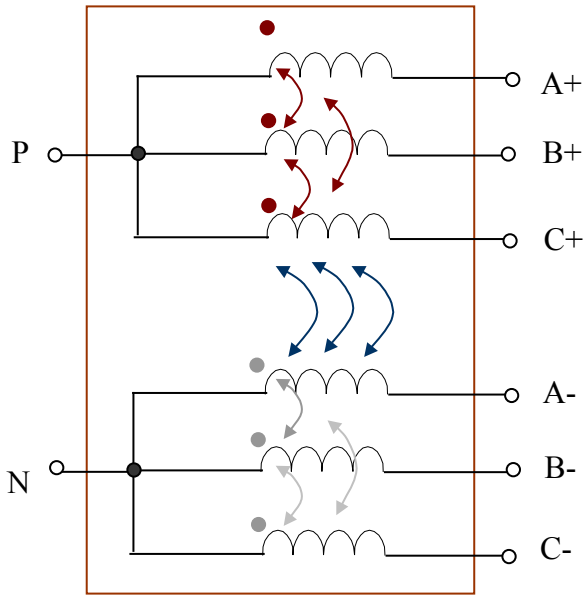


Fig. 5.4. The multi-terminal network modeling three-phase bus bar.

$$\begin{bmatrix} L_1 & & & & & \\ & L_2 & & L_{ij} & & \\ & & L_3 & & & \\ & & & L_4 & & \\ & L_{ij} & & & L_5 & \\ & & & & & L_6 \end{bmatrix}$$

Fig. 5.5. Inductance matrix for the electrical network of the three-phase bus bar.

	A+	B+	C+	A-	B-	C-
A+	73.569	46.762	29.769	58.659	34.622	19.463
B+	46.762	55.325	45.935	34.744	40.54	34.549
C+	29.769	45.935	71.66	19.082	33.98	57.937
A-	58.659	34.744	19.082	53.219	28.325	13.816
B-	34.622	40.54	33.98	28.325	34.45	28.119
C-	19.463	34.549	57.937	13.816	28.119	52.679

Fig. 5.6. Inductance matrix value obtained from Maxwell Q3D. (Unit is nH)

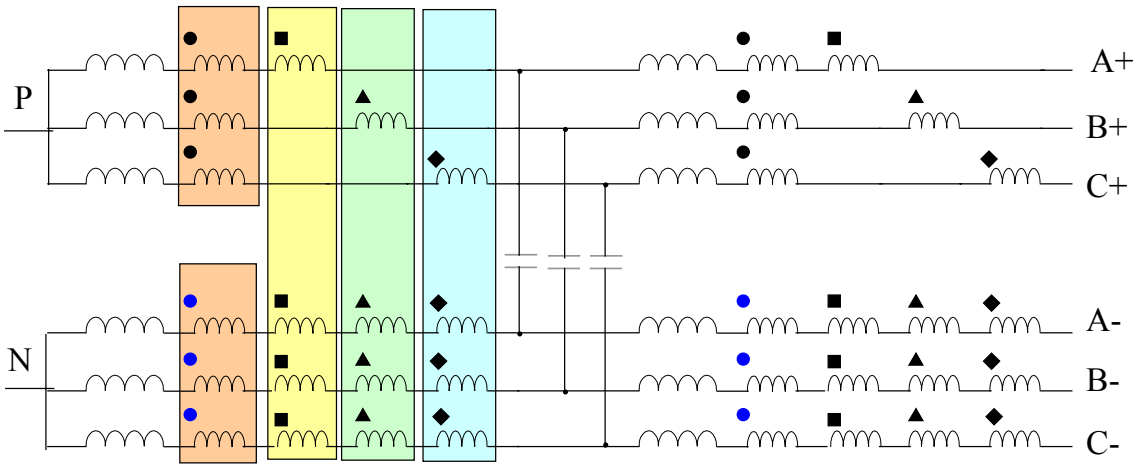


Fig. 5.7. Complete three-phase bus bar model.

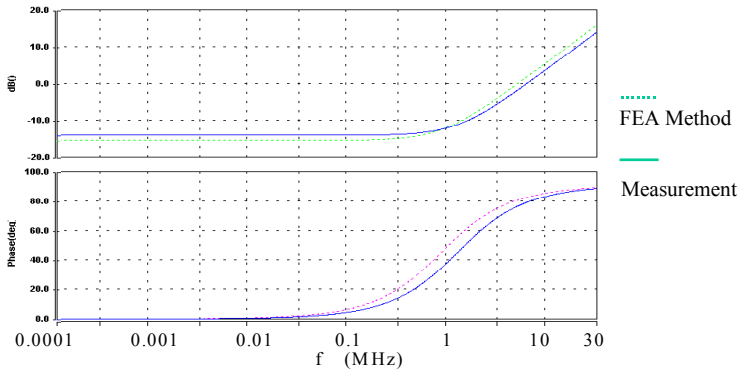


Fig. 5.8. Comparison of the total loop inductance between FEA method and the measurement.

The impedance measurement of the laminated bus bar is conducted when shorting the IGBT terminals of one phase leg. This measurement actually gives the total equivalent loop inductance. Since the direct measurement cannot obtain the mutual coupling coefficient among different current path, this total loop inductance is used to indirectly verify the accuracy of the model of the bus bar. Fig. 5.8 shows the comparison of the loop inductance when shorting the middle leg IGBT. The good agreement between the measurement and FEA results is observed. In fact the loop inductance from the input DC bus terminals to the middle leg and to the outer leg is different. The results show the middle leg's loop inductance is about 13 nH and the outer leg's loop inductance is about 17 nH.

5.3. Modeling and Analysis of Three-Phase Hard-switching Inverter

Based on the successful one leg simulation and testing described in Chapter 3 and the three-phase bus bar model, a three-phase inverter using the laminated bus plates is further developed with three-phase inductor-resistor load. The experimental setup and the corresponding simulation circuit in Saber are shown in Fig. 5.9 and Fig. 5.10. The major difference between the single-phase and three-phase simulation model is that the three-phase planar bus bar models are used for three-phase inverter simulation and the PWM or SVM control is applied. The test condition is fs=10 kHz, the modulation index is 0.3, and the load current is 40 Arms.

From the comparison results shown in Fig. 5.11 and Fig. 5.12, it can be seen the high frequency noise location is basically predicted right by the simulation model. Until 15 MHz, the DM noise difference at most is smaller than 5 dB and the basic envelop of simulated noise is very close to the measurement results. The CM noise prediction in the most range is also good except at very high frequency >20 MHz. The detailed check found the ringing frequency around 15 MHz is the result of the resonance between the device output capacitance and the commutation loop inductance.

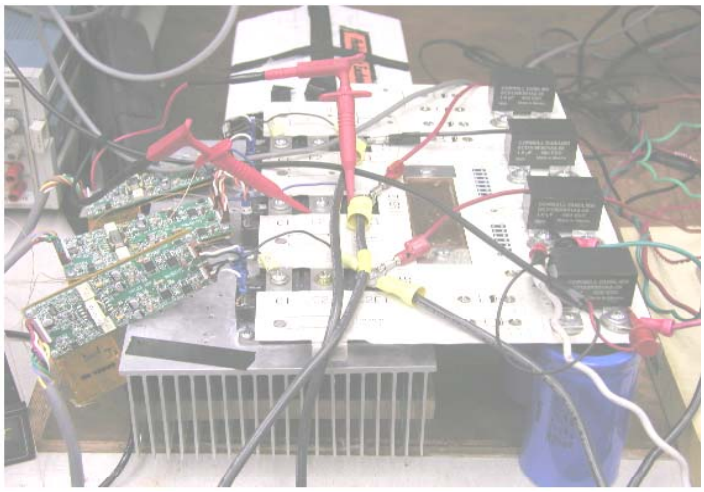


Fig. 5.9. Three-phase inverter for EMI testing.

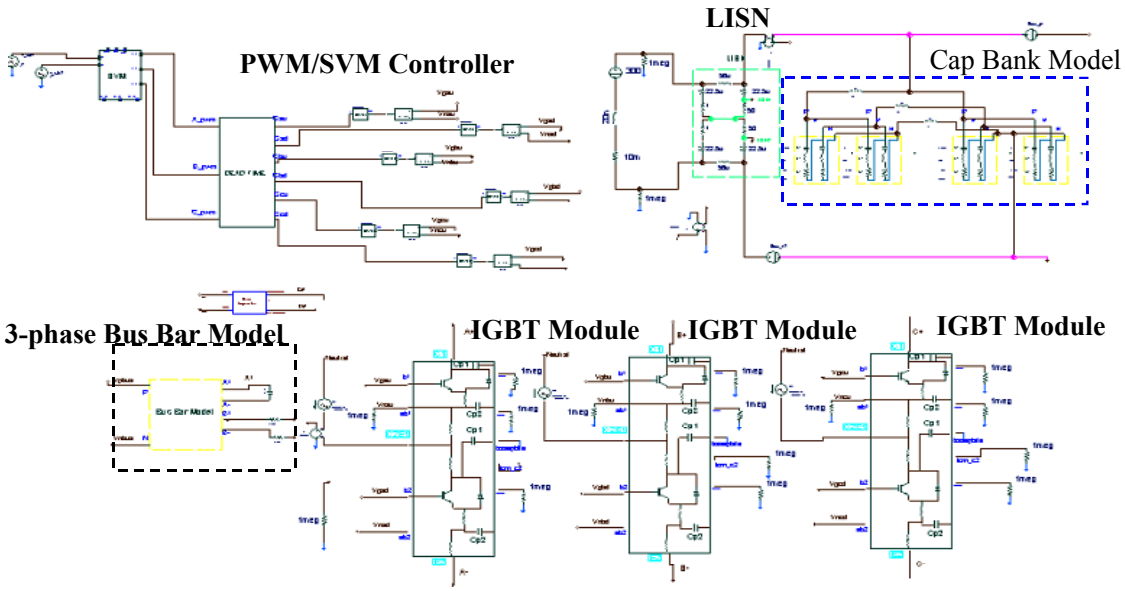


Fig. 5.10. Three-phase inverter simulation circuit.

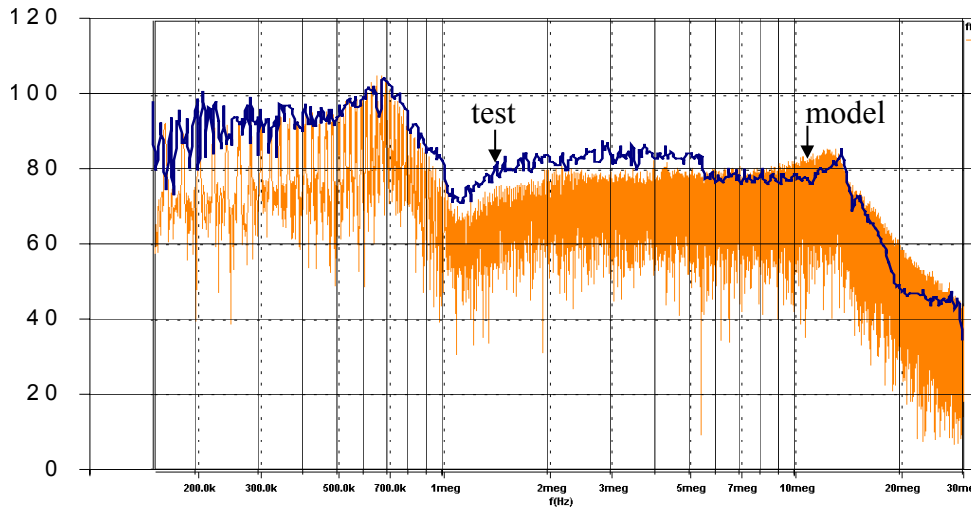


Fig. 5.11. Comparison of simulated DM and measured DM for three-phase operation.

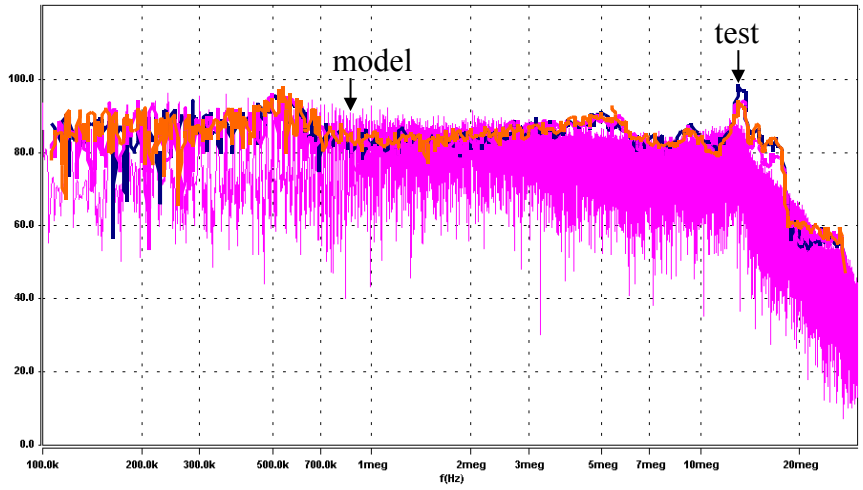


Fig. 5.12. Comparison of CM noise between test and simulation for three-phase operation.

Several important observations can be made for the EMI noise of the three-phase inverter via parametric study of the simulation circuit. First, the DM noise peak and valley at low frequency region, for example below 2 MHz, are mainly the results of the capacitor bank. As shown in Fig. 5.13, the electrolytic capacitor has a resonance frequency at about 7 kHz and the high frequency decoupling polypropylene capacitor resonates at 1.5 MHz. When the electrolytic capacitor and

the decoupling capacitor are paralleled together, there is usually a parallel resonance below the resonance frequency of the decoupling capacitor. The reason is that the electrolytic capacitor becomes inductive and the decoupling capacitor is still capacitive. Therefore, the impedance of the capacitor bank exhibits multiple resonances. The lowest resonant frequency is the same as that of the electrolytic capacitor. The newly added resonant frequency is about 700 kHz, at which the impedance of the electrolytic capacitor is almost equal to that of the decoupling capacitor. The impedance peak of the capacitor bank is detrimental to filtering function of the DM noise. Thus, the DM noise spectrum measured at LISN has a peak at the similar frequency spot, about 700 kHz. The DM noise valley at low frequency is due to the impedance valley of the decoupling capacitor.

Another observation is that the frequency of the high frequency ringing at DM and CM noise is mainly determined by the commutation inductance, between the capacitor bank and the IGBT devices, and the device's junction capacitance. Since the accurate IGBT and diode models have been developed, the diode reserve recovery current can be modeled with an acceptable accuracy. Therefore, the amplitude of the high frequency ringing can be reasonably predicted. For the studied case, the commutation inductance is about 85 nH, and the total junction capacitance of IGBT and diode is about 900 pF. Thus the characteristic resonant frequency is about 18 MHz. Due to the damping caused by the conduction losses in the device, the actual ringing frequency is about 14 MHz.

The significant advantage of the 1-D physics-based IGBT model and the detailed parasitic modeling is that the high frequency EMI noise can be predicted more accurately than using the ideal switch, or the simplified calculation, or using the behavior device model. The comparison

between the simulation and the experimental results confirms the validity of developed IGBT parameter extraction method and the IGBT module parasitic extraction method. By systematically developing a simulation circuit using the developed modeling approach, the frequency range in which the predicted EMI noise achieves the acceptable accuracy is extended compared with the past practice. The established IGBT MG300J2YS50 model is listed in Appendix B.

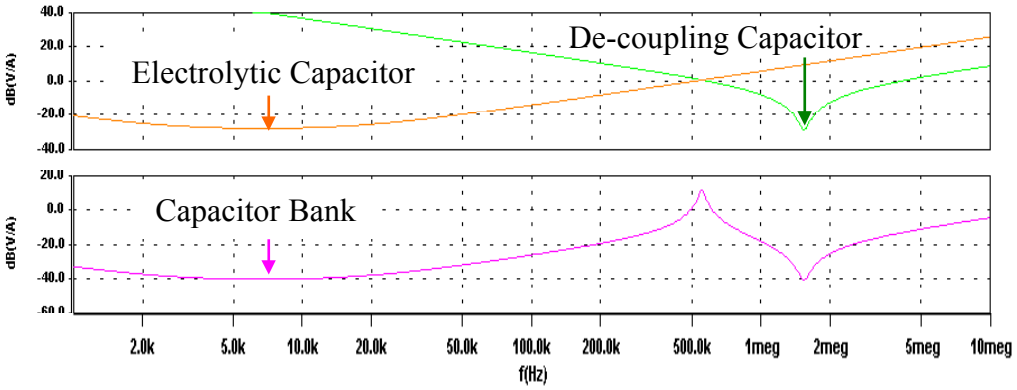


Fig. 5.13. Relationship of capacitor impedance and the capacitor bank impedance.

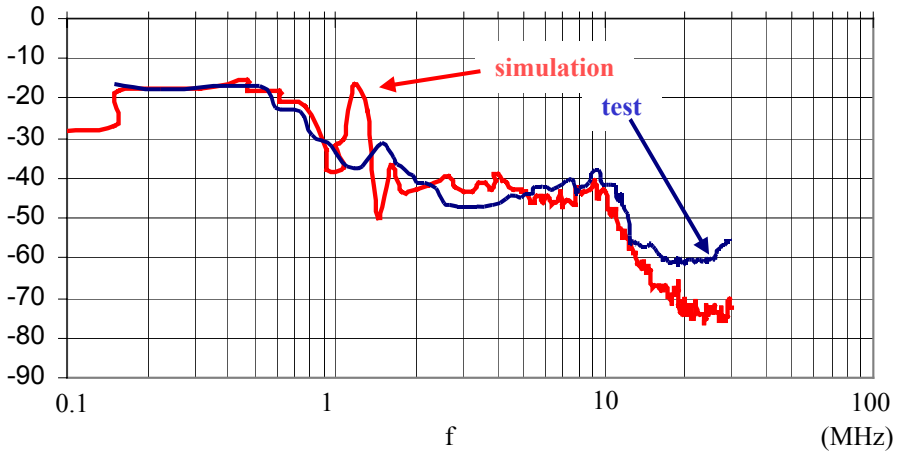


Fig. 5.14. Summary of DM noise results from [D11].

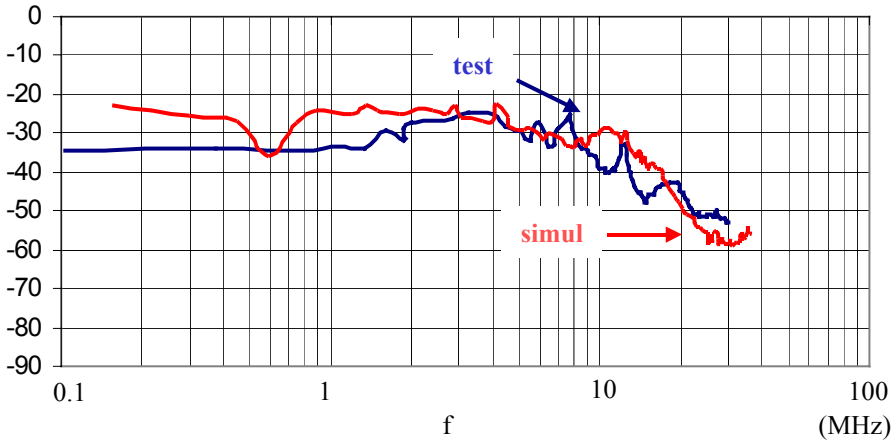


Fig. 5.15. Summary of CM noise results from [D11].

To better understand the significance the three-phase inverter model has achieved, the conducted EMI noise prediction results of the three-phase inverter are shown in Fig. 5.14 and Fig. 5.15 based on the results in [D11]. Although 1-D physics based IGBT model is used in [D11], the overall accuracy of conducted EMI noise prediction is much worse than the results presented previously. There are several reasons for this. First, the device packaging parasitics has been more accurately modeled using the proposed method discussed in Chapter 4 while the approach in [D11] made inaccurate assumptions of the parasitic inductance distribution and does not take into account the mutual inductor's effects. Second, although the TDR method is used in [D11], the total loop inductance is the bus bar parameters for the simulation. The proposed bus bar modeling method completely includes the coupling effects among different inverter legs. Another significant benefit is the presented IGBT parameter extraction method offers a simple and accurate way of developing the IGBT models as compared with the complicated modeling approach used in [D11].

To further illustrate the EMI noise characteristics of the hard-switching inverters, the model of the 55 kW hard-switching inverter is also developed. Since the EMI filter is implemented

when testing 55 kW three-phase inverter, its model is obtained from the measured impedance of the X-capacitor, Y-capacitor and the common mode choke. Fig. 5.16 shows the measured impedance of one 1 uF capacitor and the resonant frequency is about 2MHz. Once three 1 uF capacitors are paralleled together in the PCB board, the resonant frequency at the impedance valley is changed to around 200 kHz, as shown in Fig. 5.17. The interconnect inductance also contributes to the variation of the resonance frequency. The common mode choke's impedance is measured and shown in Fig. 5.18. It can be seen that the inter-winding capacitor must be considered in the simulation model since the resonance frequency is only 2 MHz. Based on the derived equivalent circuit parameters from the impedance measurement, the overall EMI filter model is established in Saber, as shown in Fig. 5.19.

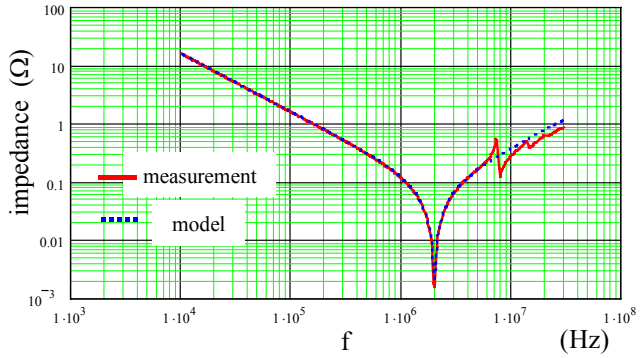


Fig. 5.16. The impedance of 1 uF capacitor used in EMI filter.

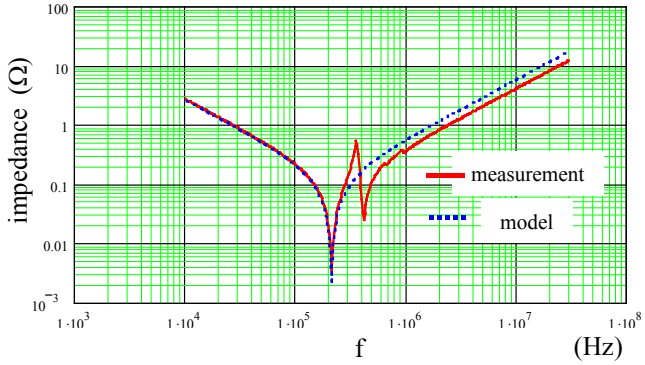


Fig. 5.17. The impedance of X-capacitor composed of three parallel 1 uF capacitor.

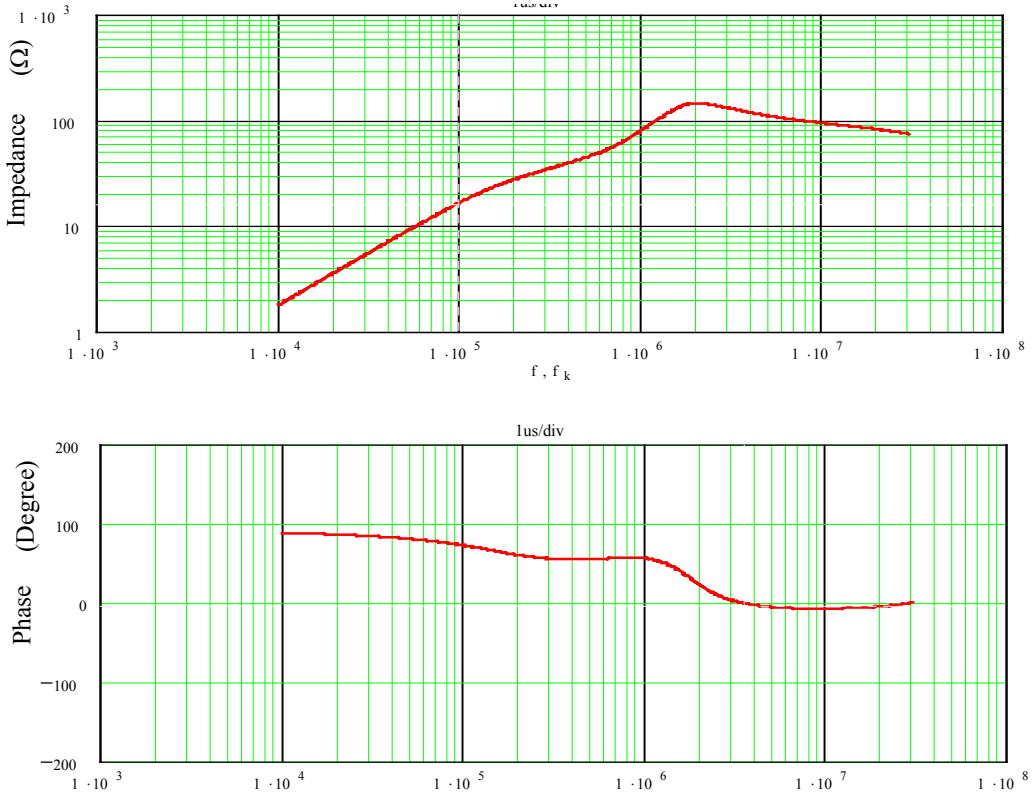


Fig. 5.18. The measured impedance of common mode choke.

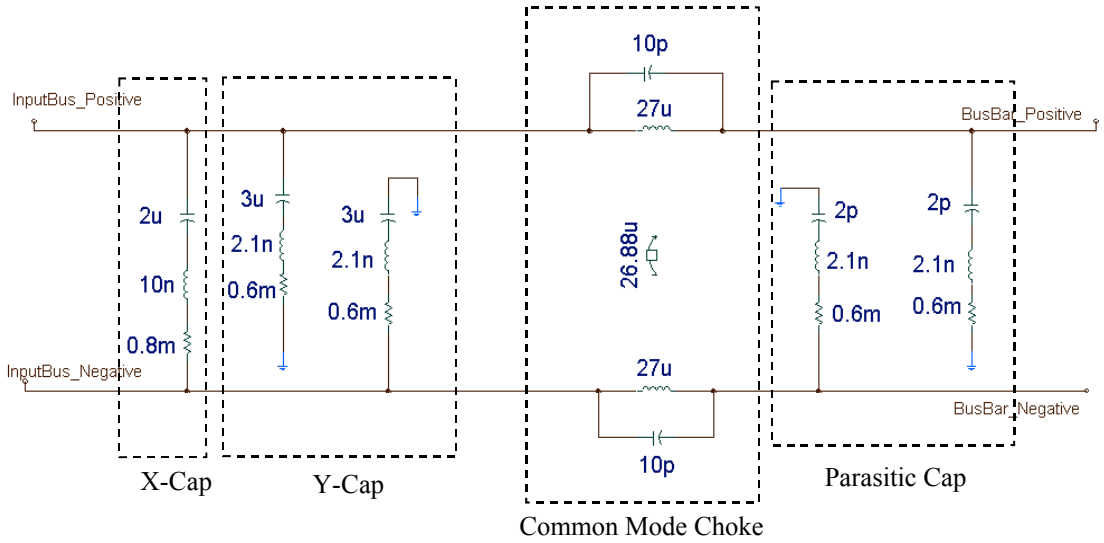


Fig. 5.19. Simulation model of the EMI filter for 55 kW inverters.

The simulation results are shown in Fig. 5.20 and Fig. 5.21 to compare with the experimental results for the 55 kW hard-switching inverter. It can be seen from the most of frequency range, the simulation results match the test results. In the DM noise spectrum, there exist several noise peaks at different frequency spot. The simulation can explain all these noise peaks well. For example, the DM noise peak at about 200 kHz is mainly caused by the parasitic resonance of the EMI filter. The predicted DM noise gain in the simulation is shown in Fig. 5.22. The noise valley at 500 kHz, as explained in the previous section, results from the DC bus filter capacitor and the EMI filter's parallel type of resonance. Another noise peak at 700 kHz is related to the EMI filter high frequency resonance. As shown in Fig. 5.22, the filter resonance peak is at 1.5 MHz when its parasitic inductance is about 2-4 nH. When connected with the DC bus, the DC bus inductance is about 10-15 nH, therefore, the resonant peak is reduced twice and then move to a lower frequency, near 700 kHz. The layout of 55 kW inverter has a ringing frequency of about 10 MHz. Since the filter still has certain attenuation at 10 MHz, the noise peak with the EMI filter implemented into the inverter is not obvious. Regarding the CM noise, Fig. 5.21 shows the simulation results matches the test results except at low frequency and above 20 MHz range. The noise valley at 2 MHz is associated with the high attenuation of the CM filter, as shown in Fig. 5.23.

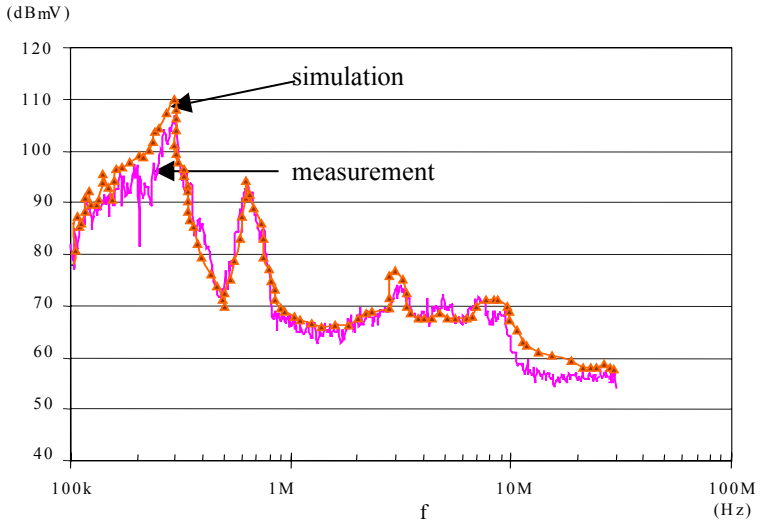


Fig. 5.20. Comparison of the measured and simulated DM noise for 55 kW inverter.

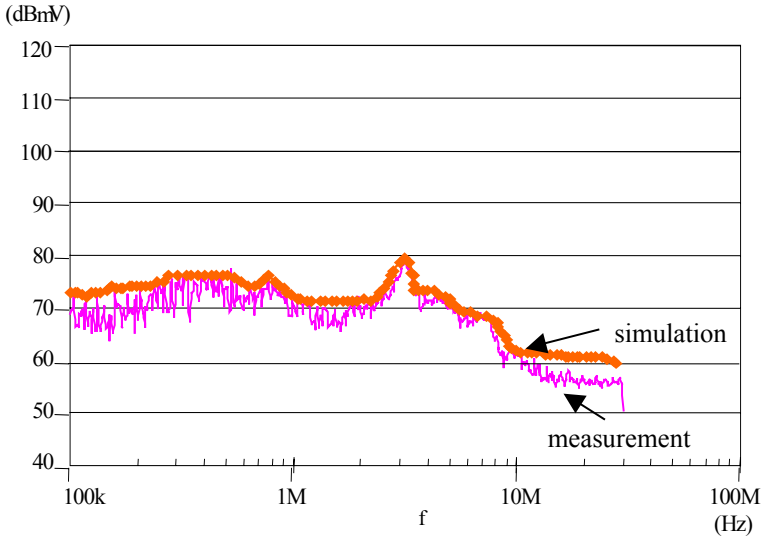


Fig. 5.21. Comparison of the measured and simulated CM noise for 55 kW inverter.

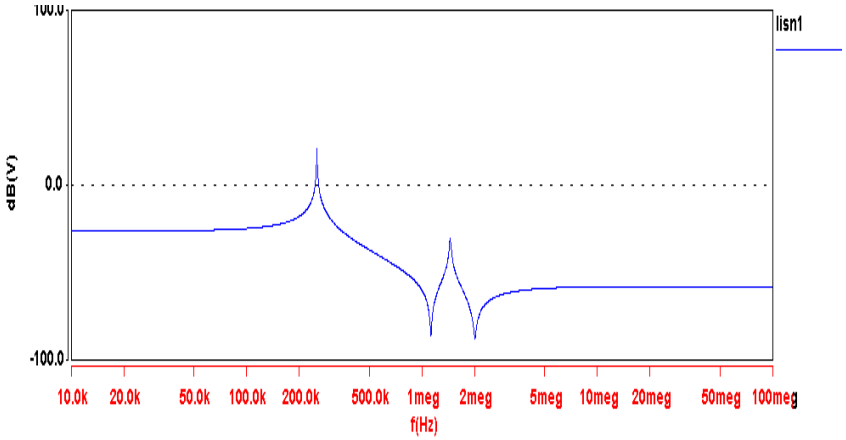


Fig. 5.22. Predicted DM noise attenuation gain of the EMI filter.

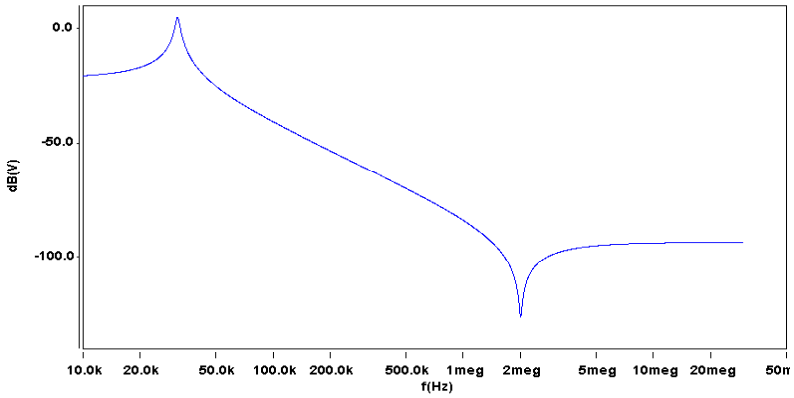


Fig. 5.23. CM noise attenuation gain of EMI filter.

5.4. Modeling and Analysis of Three-Phase Soft-switching Inverter

The electrical simulation model for the three-phase hard-switching inverter is presented in preceding sections. Through the extensive simulations and experiments, the accuracy of the simulation model is fully verified. The good accuracy of the EMI noise prediction and the switching loss prediction mainly rely on the accurate modeling of the switching waveforms. It has been demonstrated that the accurate IGBT simulation model, the accurate IGBT package's parasitic model, and the detailed model of the three-phase bus bar ensure the accurate switching waveforms. Actually the IGBT model, the Hefner Model in Saber, has been validated to be able

to reflect the switching waveforms under the soft-switching conditions [E2]. Therefore, the presented three-phase inverter simulation model can also be applied to the soft-switching inverters.

This section intends to present the analysis of EMI and losses for soft-switching inverters. Since Chapter 3 has experimentally shown that the ARCP inverter can achieve the EMI noise reduction in certain frequency region. However the insightful analysis from the detailed circuit simulation is not provided. It is worthwhile to use the simulation model to further analyze the effect of the ARCP inverter on the conducted EMI noise. It is noted that the experimental results obtained from Chapter 3 are with the EMI filter on the DC link, the EMI filter effects have been included in the measurement results together with the soft-switching operation's effect. To focus on the soft-switching inverter, the simulation model for the ARCP inverter is developed without the EMI filter. To model the EMI filter and study its actual attenuation in a three-phase inverter is out of scope of this dissertation.

5.4.1. Conducted EMI Simulation of Three-phase Soft-switching Inverter

Although the experimental evaluations have demonstrated that the ARCP inverter can achieve the EMI noise reduction in certain frequency region, the fundamental reasons are still not very clear and the limitations are not understood. The ZCT inverters inherently do not change the dv/dt since the device voltage is quickly charged or discharged. Therefore, the CM noise is not expected to change by the ZCT operation. This has been confirmed via the experimental evaluation on the 55 kW ZCT inverters. Regarding to the impacts on the di/dt, the resonant tank's operation in ZCT inverters causes the resonant current to add on the DC link. Therefore, the DM noise at the resonant tank frequency is increased.

Regarding the switching loss reduction, there are various EV applications, which correspond to different power ratings. When analyzing different power ratings with different bus voltage designs, it is impossible or very labor-intensive to experimentally study the soft-switching inverter's impacts on the loss reduction. So the device models are developed and their losses can be obtained through the simulation. Some suggestions are made toward the application of the soft-switching inverters based on the simulation results.

Based on the simulation circuit in Fig. 5.10, the ARCP inverter model is developed by developing the auxiliary switch control, the snubber capacitor models, and the auxiliary circuit models. The referring power devices and the auxiliary components of the ARCP inverter is the developed 55 kW ARCP inverter. In order to verify the accuracy of the simulation model for the turn-off process, the single-leg test circuit is measured when the snubber capacitor is paralleled with both IGBTs in one half-bridge module, as shown in Fig. 2.16. To measure the device current, twp 1 cm high copper washers are inserted between the IGBT module and the laminated bus plate. These two copper washers are connected to C1 terminal and E2 terminal, respectively. Therefore the additional commutation inductance is introduced between the IGBT module and the planar bus bar. The corresponding simulation circuit for the single-leg test circuit models the inductance, which distributes the parasitic inductance of 10 nH for each copper washer. The turn-off waveforms with snubber capacitor 0.22 μF are shown in Fig. 5.24. It is indicated that the falling di/dt of the device current and rising dv/dt of the device voltage match the experimental result well. Especially the ringing frequency of the voltage is also modeled fairly accurately. In the implementation of the three-phase ARCP inverter, the copper washers are removed. So the three-phase ARCP model has to exclude the corresponding parasitic inductance. The complete

ARCP inverter model is illustrated in Fig. 5.25. The switching speed of the auxiliary devices almost has no change over the load current level due to ZCS. Therefore, the ideal switch model can be used to reflect the dv/dt during switching transition. The snubber capacitance is modeled via the measured impedance using the impedance analyzer HP4195A. The simulation model parameters for the auxiliary branch are illustrated in Fig. 5.26. The parasitic capacitance between auxiliary IGBT die to the ground is measured to be 30 pF.

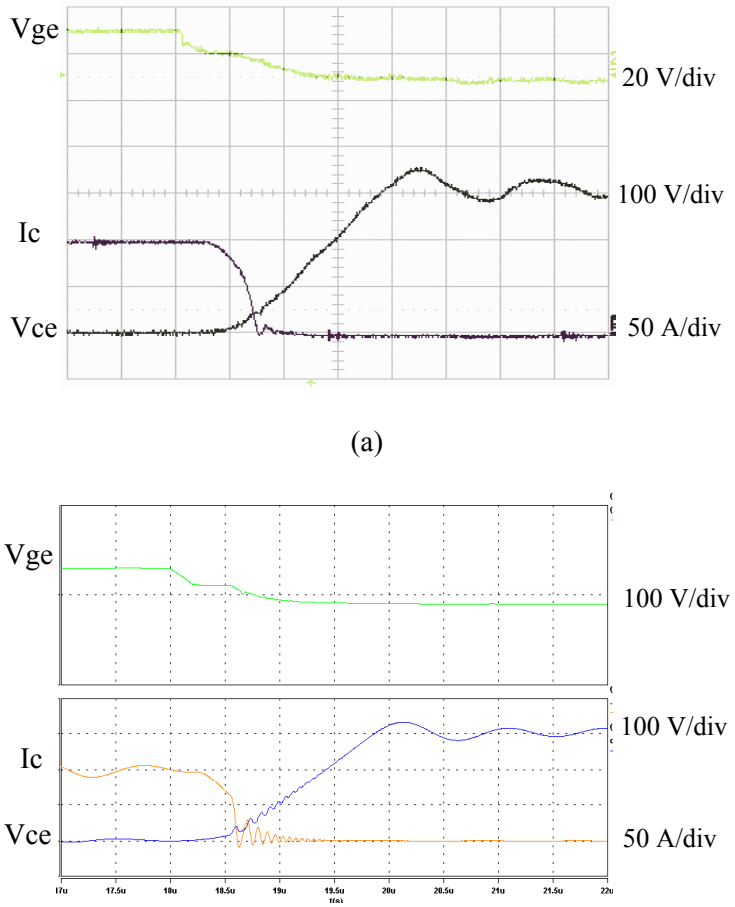


Fig. 5.24. Waveforms of turn-off with snubber capacitor 0.22 μF: (a) test and (b) simulation. (0.5 μS/div)

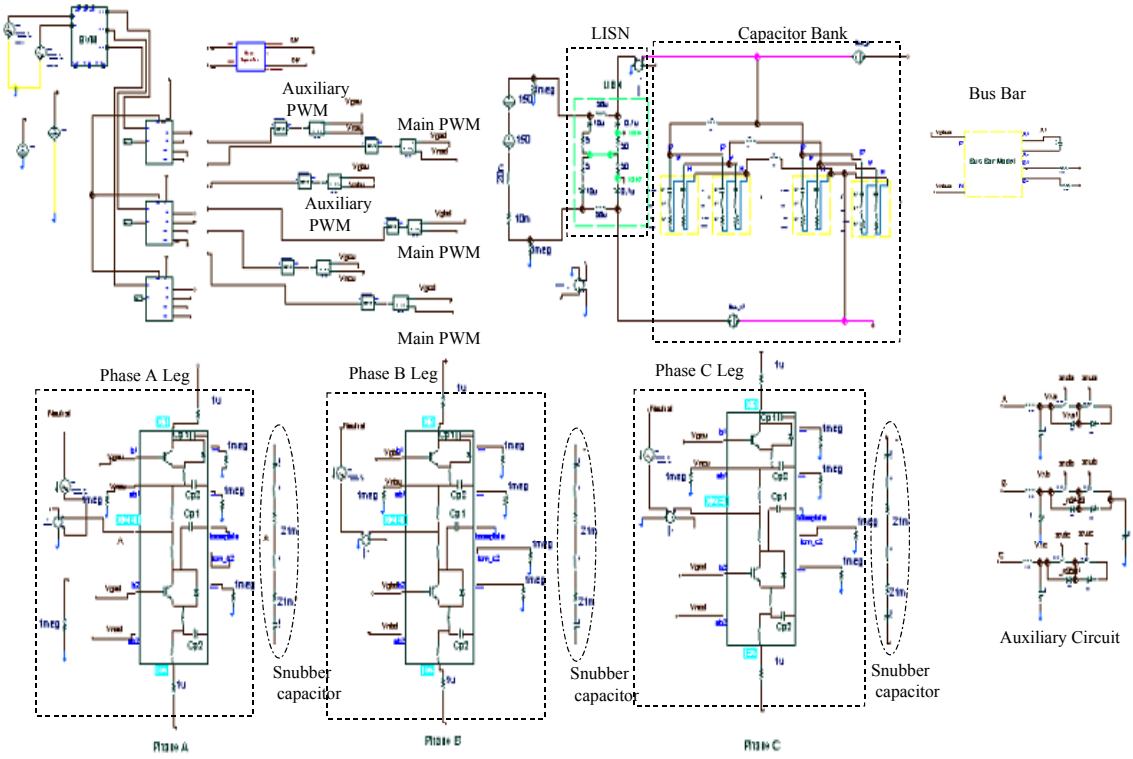
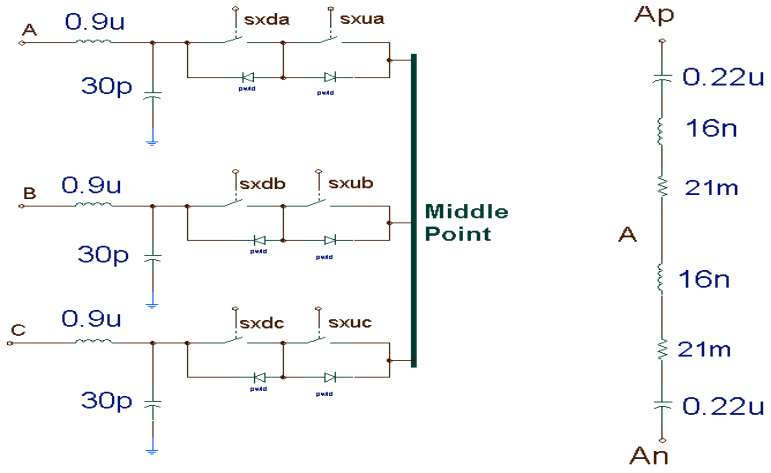


Fig. 5.25. Simulation circuit of ARCP inverter in Saber.



(a) (b)

Fig. 5.26. Detailed component models for the ARCP inverter: (a) auxiliary circuit and (b) snubber capacitor.

The simulation results of the three-phase ARCP inverter are obtained and then compared with that of the hard-switching inverter, as shown in Fig. 5.27. There are three distinct observations, similar to those made from experimental results in Fig. 3.46 and Fig. 3.47. First, the DM noise level at 1.4 MHz is increased by the ARCP inverter. The main reason is that the snubbered turn-off causes the ringing with a frequency determined by the parasitic inductance and the snubber capacitor. In this case, snubber capacitor is 0.44 uF and the total equivalent inductance is 23 nH. Then the resonance frequency is about 1.5 MHz. The simulation results are verified by the experimental results shown in Fig. 3.34. Second, the di/dt is reduced and thus the DM noise level becomes lower at high frequency region. From 2 to 10 MHz, the ARCP inverter realizes 10 dB lower DM noise than the hard-switching inverter. Third, the high frequency DM noise peak around 15 MHz in the hard-switching inverter disappears in the ARCP inverter. This is because the ARCP inverter greatly alleviates the diode reverse recovery. Therefore, the high frequency ringing due to the diode reverse recovery current is much reduced. The further details at the turn-on demonstrate that the ARCP inverter greatly reduces the ringing of the device current, as shown in Fig. 5.29.

The effect of the ARCP inverter on the CM noise is shown in Fig. 5.30. Similarly, there are three main observations. First, the snubbered turn-off also causes ringing and thus increases the CM noise at the particular frequency. The ringing frequency is mainly determined by the commutation parasitic inductance, the parasitic inductance of the snubber capacitance, and the snubber capacitance. Second, due to much reduced dv/dt for both turn-on and turn-off, the high frequency CM noise level is reduced. From 2 to 10 MHz, about 10 dB reductions is achieved. Third, the alleviated diode reverse recovery at turn-on reduces the CM noise ringing. The

suppressed ringing at the device voltage at turn-on is clearly demonstrated in Fig. 5.32. It is concluded that the ARCP inverter is able to reduce the DM and CM noise at the high frequency region and attenuate the ringing significantly. A potential issue is to minimize the ringing caused by the snubber capacitor and the parasitic inductance, which causes the DM and CM noise increase at the resonance frequency. By carefully designing the ARCP inverter, it is possible to maximize the EMI noise reduction, mainly at the high frequency region. Another potential issue is the slightly increased CM noise at low frequency region, as also indicated in Fig. 3.46 and Fig. 3.47. Most soft-switching inverters have additional switching actions of auxiliary devices as compared with the hard-switching inverters. Since the switched voltage level and the parasitic capacitance mainly determine the CM noise level at low frequency region, soft-switching inverters will have slightly higher CM noise at low frequency region. Since the auxiliary switch's loss is very small, the suitable insulation material between the device base plate and the heat sink can be chosen to reduce the parasitic capacitance to ground. Since the high frequency EMI noise is more difficult to be filtered in practice due to degraded filter performance and the careful packaging design can alleviate the CM noise level for the ARCP inverter, the ARCP inverter can effectively reduce the EMI filter requirement. Comparing Fig. 5.27 and Fig. 5.28, it is found that the simulation circuit without the EMI filter well explains the noise attenuation observed at the inverter with the EMI filter. Apparently, the noise peak at 500 kHz without EMI filter is moved to 200 kHz with the effect of the EMI filter for both hard-switching and the ARCP inverter. The turn-off snubber ringing at 1MHz cannot be filtered by the EMI filter since it is close to the resonance frequency of the filter. Therefore the ARCP show higher noise at 1 MHz. In the mid-frequency range, the ARCP inverter has achieved the noise attenuation without

the EMI filter. Therefore, the EMI filter does not mainly changes the noise level difference between the ARCP and the hard-switching inverter. Similarly, by comparing Fig. 5.30 and Fig. 5.31, the CM noise envelope of the ARCP inverter without the EMI filter at high frequency is similar to that with the EMI filter since the EMI filter attenuation becomes saturated at high frequency range. The noise valley at around 2-3 MHz of the ARCP inverter is matching the test results fairly well too.

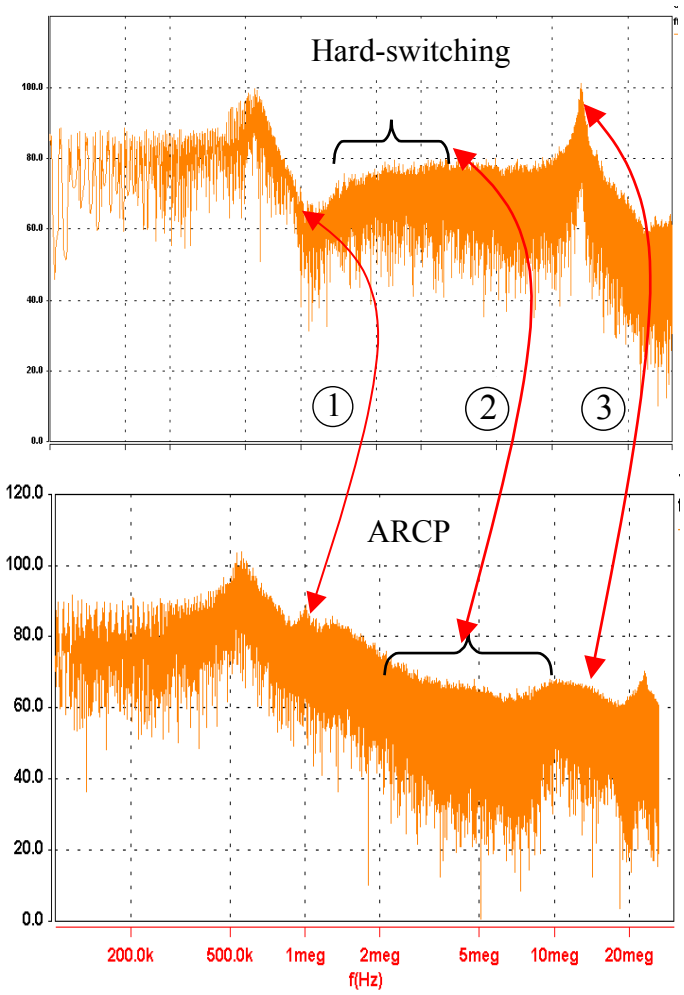


Fig. 5.27. DM noise comparison of hard-switching and ARCP inverter without EMI filter.

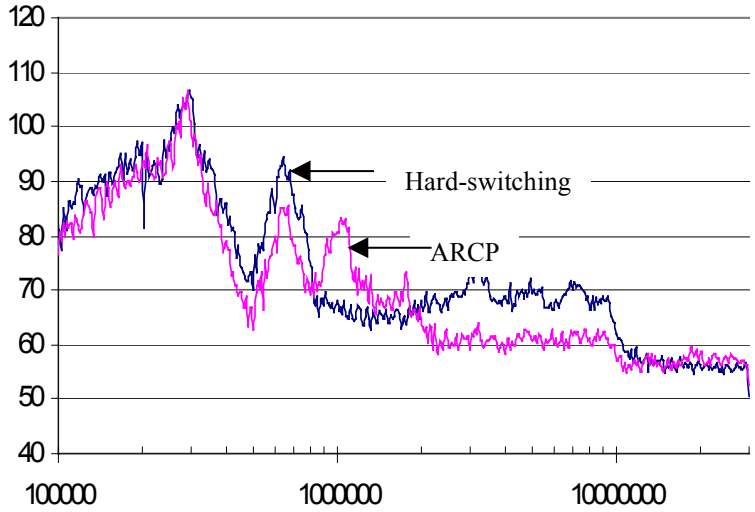


Fig. 5.28. Experimental DM noise comparison of hard-switching and ARCP with the EMI filter.

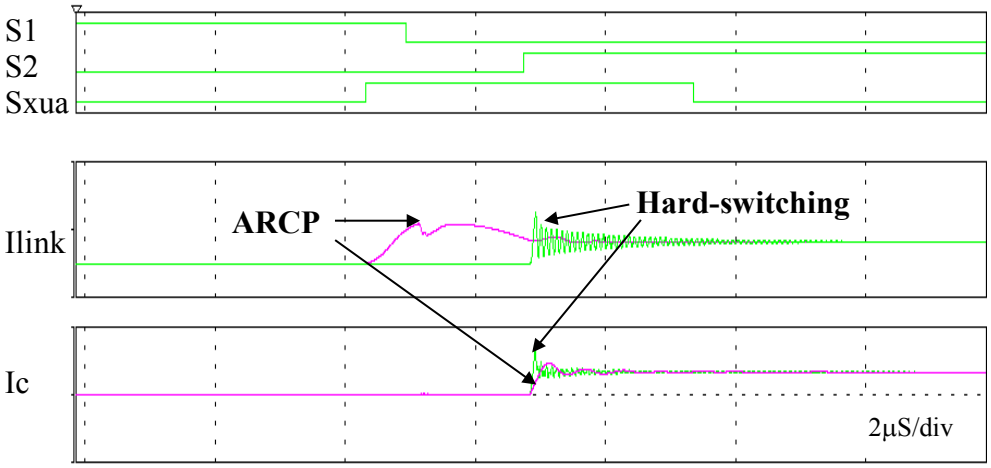


Fig. 5.29. Comparison of device current at turn-on.

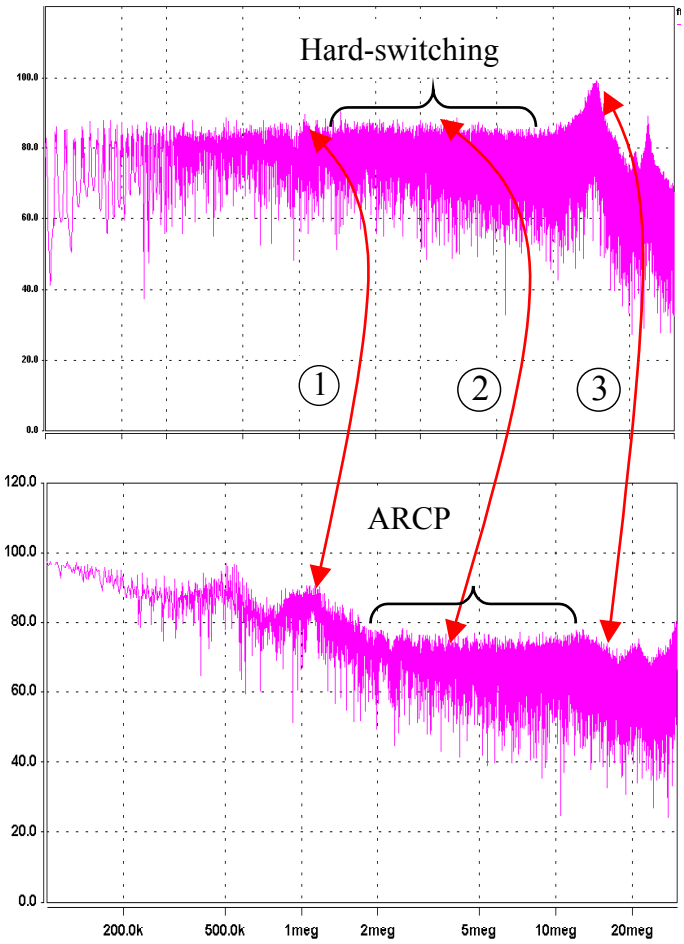


Fig. 5.30. CM noise comparison of hard-switching and ARCP inverter.

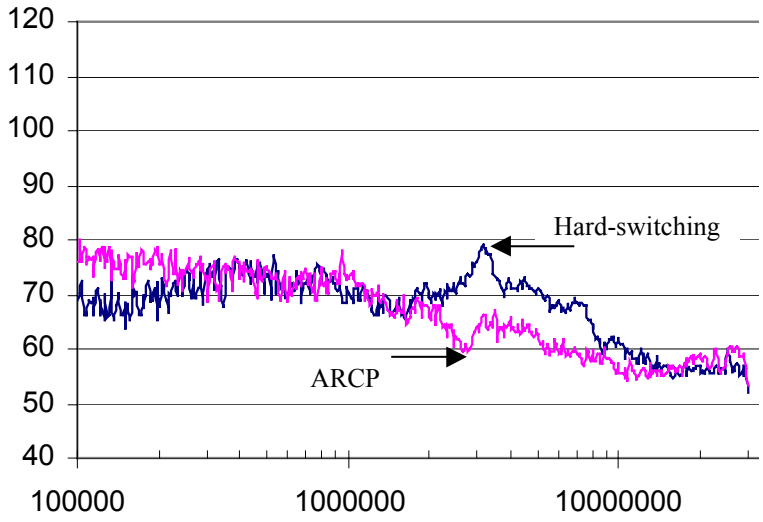


Fig. 5.31. Experimental CM noise comparison of hard-switching and ARCP with the EMI filter

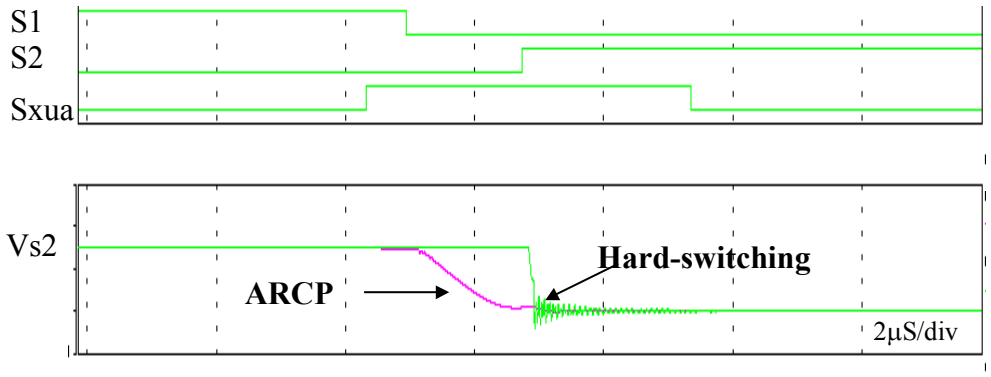


Fig. 5.32. Comparison of device voltage at turn-on.

5.4.2. Loss Analysis of Soft-switching Inverters via Simulation Model

The efficiency evaluation in Chapter 3 has indicated that at small power EV applications, the soft-switching inverters do not show the benefit since the IGBT devices already exhibits the dominant conduction loss components. Although the switching loss reduction in the main phase legs has been demonstrated, its impact on the thermal management reduction can not be significant due to small percentage of loss saving. The EV applications cover wide power rating range and the inverter designs possible have different bus voltage selection and use different power devices. Therefore, it is impossible to implement the soft-switching inverters for each inverter design and conduct the experiment. The significance of the accurate simulation model is that we can use the model to evaluate the loss reduction scenario for different inverter designs. Usefulness of the model in terms of extending evaluation to other EV applications is demonstrated through the example of inverter design at 300 kW. It is extremely difficult to exhaust the modeling efforts for all EV applications since too many EV ratings and many inverter design options exist. Application engineers can apply the proposed modeling method to develop the hard-switching inverter and the soft-switching model for their specific application. It

is expected the quantitative performance comparison can be obtained through the simulation models instead of the time-consuming hardware prototyping process.

Our experimental evaluation has indicated for the small duty EV applications, soft-switching inverter did not gain much performance improvement. However it is worthwhile to take a look at other EV applications. If we can build the device model for different applications, then the evaluation of the soft-switching inverter's performance can be made. In previous chapters, the developed electrical model has been demonstrated to be able to provide fairly accurate switching loss estimation. On the other hand, it is interesting to point out that the low current device model can be easily extended to the high current device model by enlarging the active silicon area. The assumption is that the physical doping design is the same for different current rating devices. That is to say, for the same series IGBT device in one device company, that if the model for one current rating is correct, the model for the different current rating of IGBT can be approximated by increasing or decreasing the active silicon area. In fact, this assumption is valid for most manufacturers' IGBT devices. For example, the IGBT BSM50GD120DN2, with 1200V and 50A rating, and the IGBT BSM100GD120DN2, with 1200V and 100A rating, have the same doping design of the IGBT chip from Infineon. The difference is the chip area due to different current rating. The active chip area is 63.5 mm^2 for BSM50GD120DN2 and 132.6 mm^2 for BSM100GD120DN2. It is reasonably approximated that the active chip area is proportional to the current rating for the same series of IGBT devices.

For the general EV applications, the power rating of the inverter could range from 50 kW to 300 kW. For given power rating, it is also possible to have different bus voltage design if the DC power source is flexible. For a three-phase inverter, the relationship among the output power Po,

the voltage modulation index M, the bus voltage and the output RMS current can be derived as follows.

$$I_{rms} = \frac{P_o}{3 \cdot PF \cdot \frac{\sqrt{3}}{3} \cdot \frac{1}{\sqrt{2}} \frac{M \cdot V_{bus}}{0.866}}. \tag{5.1}$$

where P_o is the output power, V_{bus} is the bus voltage, PF is the power factor, and I_{rms} is the output RMS current. According to Equation 5.1, different device options for different designs are illustrated in Fig. 5.33. For example, for 300 kW power rating, if the bus voltage is 900V, then the device current rating should be larger than 310A. So 1200V and 400A IGBTs are suitable for the 900V bus design to deliver 300 kW output power. Several commercial devices for nine different EV inverter designs are shown in Fig. 5.34. It is our intent to demonstrate the approach for the analysis and it is not our interest to exhaust evaluations of all kinds of possible devices.

The inverter loss evaluation method is described in Chapter 2. The conduction loss model of the IGBT is obtained from the data sheet. The switching losses, under either hard-switching or soft-switching, are modeled from the experimental results. Different from the switching loss modeling approach in Chapter 2, the IGBT will be simulated under the hard-switching and soft-switching to get the loss data. Then the curve fitting method is used to derive relationship between the switching losses and the switched current.

First, the device models need to be developed. In Chapter 4, the simulation model parameters for 600V 300A IGBT MG300J2YS50 have been derived. The model for PM800HSA060 is obtained under the assumption that its active chip area is proportional to the current rating and it has similar chip design to that of MG300J2YS50. Therefore, it is easy to get the Saber simulation model for PM800HSA060. Following the proposed IGBT parameter extraction method, the

model for CM150DY-24H from Powerex is developed and the simulated waveforms are shown in Fig. 5.35 and Fig. 5.36. The comparison of the simulated waveforms and test waveforms indicates it is acceptable to use the simulation model to calculate the switching losses.

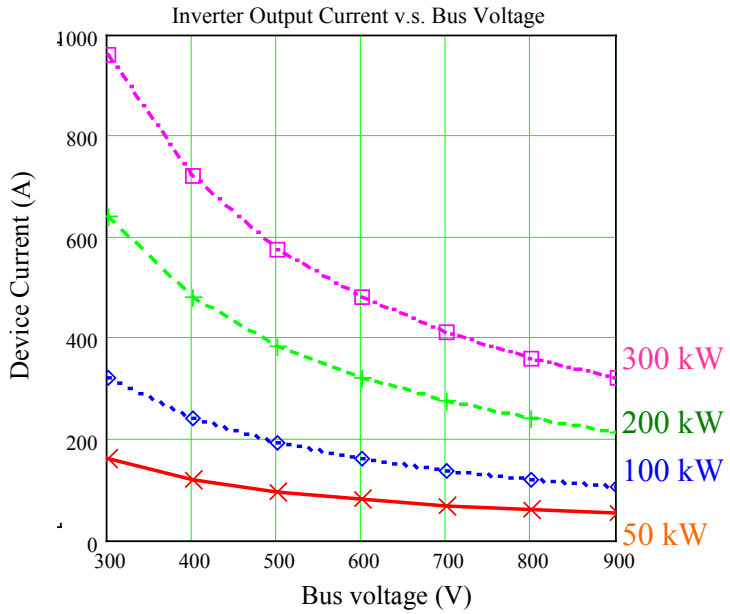


Fig. 5.33. Device current rating decided by power rating and bus voltage.

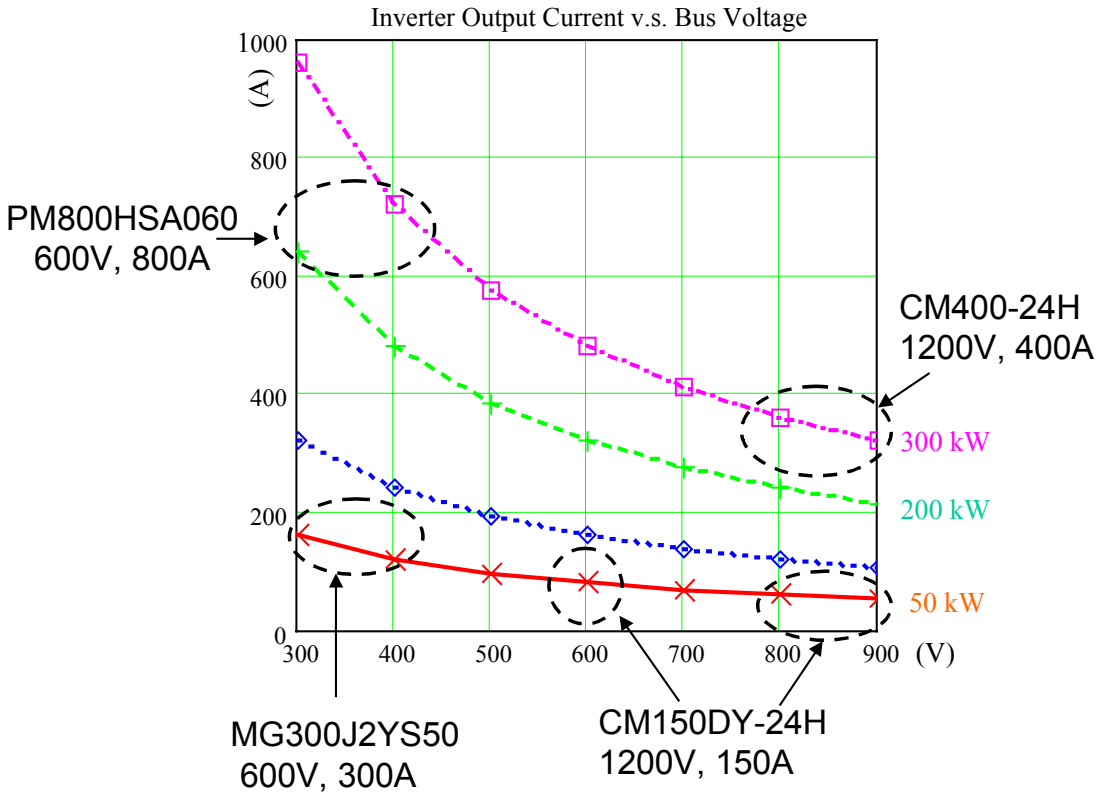


Fig. 5.34. Candidate devices for different EV inverter design.

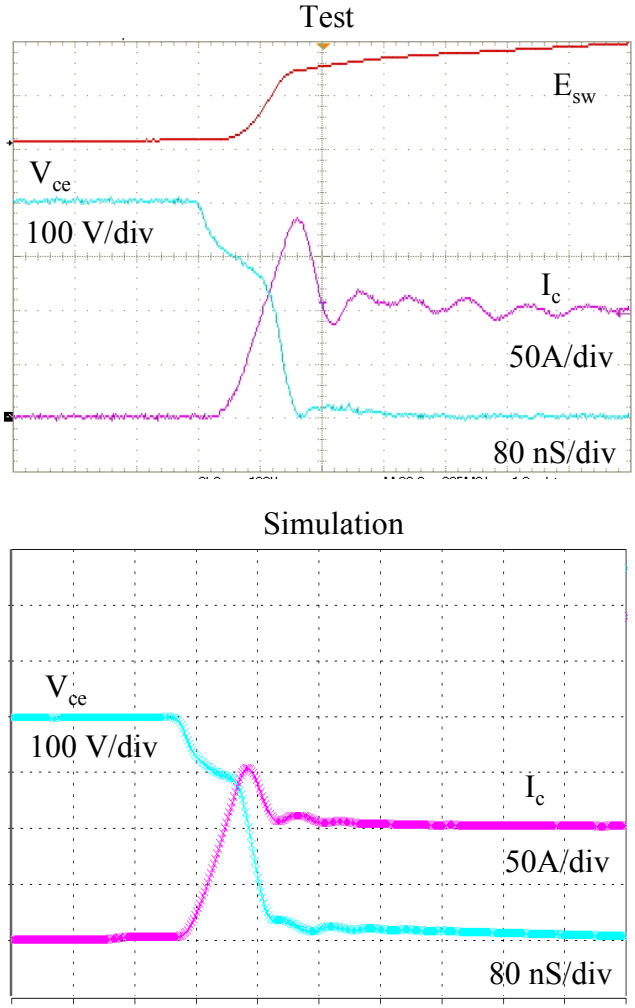


Fig. 5.35. Comparison of turn-on waveforms for CM150DY-24H.

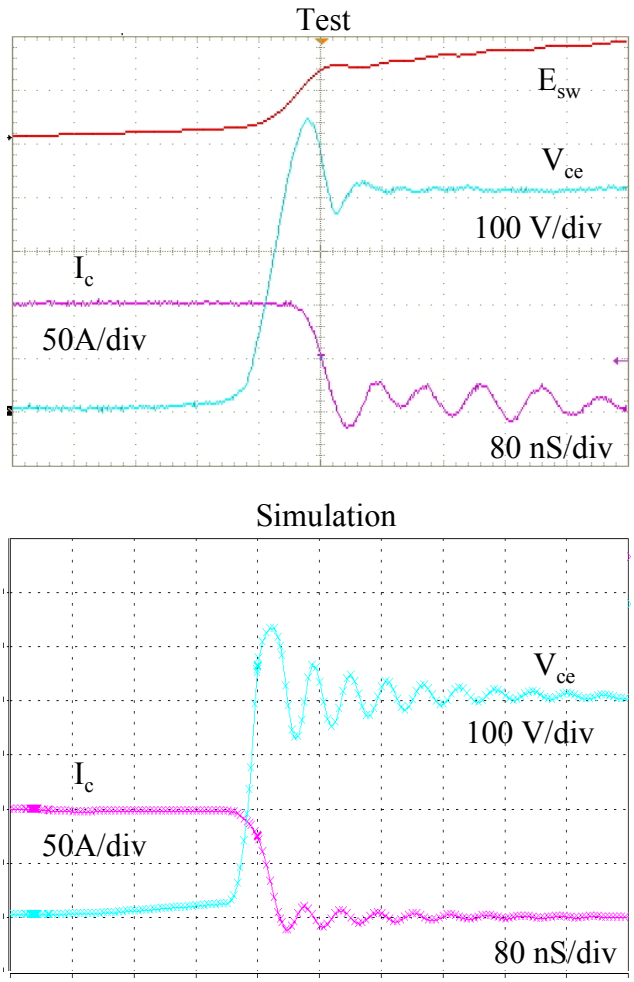


Fig. 5.36. Comparison of turn-off waveforms for CM150DY-24H.

Proportionally increasing the active silicon area of model for CM150DY-24H results in the model for CM400DY-24H. The derived loss data for CM400DY-24H is illustrated in Fig. 5.38. As can be seen from Fig. 5.38 and Fig. 5.37, the switching losses are greatly increased for high current and high voltage rating devices. With the loss model of the power devices, the inverter losses can be derived for these nine inverter designs. The percentage of the switching losses in the total inverter losses is shown in Fig. 5.39. It is obvious that the switching loss becomes dominant at the high voltage high power inverter. For 55 kW rating and Vdc design below 400 V, the switching losses compose about 30% of the total losses at 20 kHz. Even with high voltage

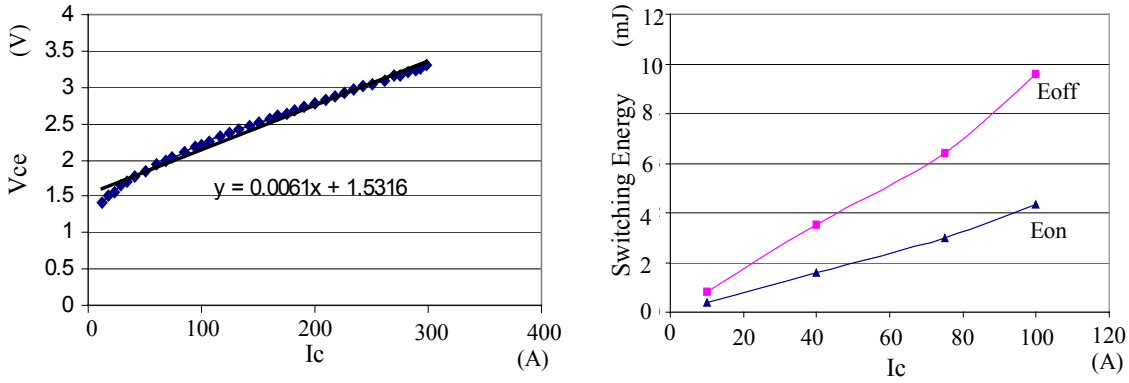
bus design for 55 kW, the switching loss percentage is still about 30%. This indicates the soft-switch inverter will not show much benefit if designed for 55 kW power rating. However for 300 kW inverter designed at 800V and 900V bus voltage, the switching loss becomes dominant. In fact the efficiency of the inverter of 300 kW is quite high, almost reaching 98%. The thermal design benefit could be significant if the soft-switching inverter achieves considerable loss reduction. Therefore, it is interesting to evaluate the soft-switching inverter's performance for 300 kW rating at 800V and 900V bus voltage.

First the soft-switching inverter design needs to be completed. Following the design guideline presented in Chapter 2, the auxiliary passive component parameters are designed as follows.

The ARCP inverter needs more snubber capacitance for the main power devices since the bus voltage is increased to 800 V or 900 V. While 0.22 μF capacitor is finally chosen for 55kW 324V inverter, the 0.47 μF capacitance is selected for 300 kW 800V ARCP inverter. To maintain the reasonable transition time, the resonant period is kept to be below 7 μS. This leads to the resonant inductor of 1.3 μH. Consequently, the resonant peak current during ZVS transition is about 340 A as defined by $V_{dc}/2\sqrt{2L_sC_s}$. The 600V 150A device IRG4ZC70UD can still be used as the auxiliary device since it can handle more than 600 A peak current, which is more than the peak current in the auxiliary circuit. The turn-off losses of the main power device under the snubber capacitance can be obtained through the simulation. As an example, the accuracy of the simulated turn-off loss under the snubber capacitor for MG300J2YS50 has been clearly verified in Fig. 5.40. The switching waveforms of the simulation match the test results fairly well for the load current 270 A. It is also noted that the measured turn-off energy E_{off} curve starts to drop after the device current drops to zero. It is because the measured device current has small

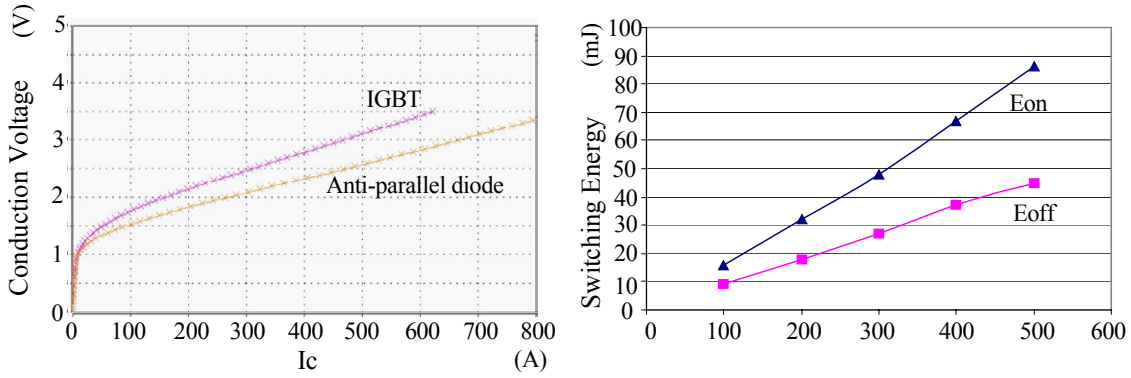
negative offset. Nevertheless, the maximum increase of integration results of the device voltage and current is similar for both the measurement and the simulation. The simulation results for CM400DY24H indicate 0.47 μF snubber capacitor can achieve about 85% turn-off loss reduction.

The design rule for the six-switch ZCT inverter is to choose the resonant impedance Z_o that ensures the ZCT turn-off for the maximum load current subject to the zero current turn-off. The resonant tank impedance is chosen to be 2.2 then the resonant peak current is about 363 A. The resonant period is limited to be 7 μS. Therefore L_x and C_x can be obtained via Equations 2.2 and 2.3. The resultant design parameters are: L_x=2.4 μH and C_x=0.47 μS. The auxiliary device has to use 1200 V IGBT. Since the current handling capability needs to be experimentally verified, two IRG4ZC70UD are in series to form on auxiliary power device for the convenience.



(a) (b)

Fig. 5.37. Loss model for 1200V and 150A IGBT CM150DY-24H:
(a) conduction voltage drop and (b) switching energy at 800 Vdc.



(a) (b)

Fig. 5.38. Loss model for 1200V and 400A IGBT CM400DY-24H: conduction voltage drop and (b) switching energy at 800 Vdc.

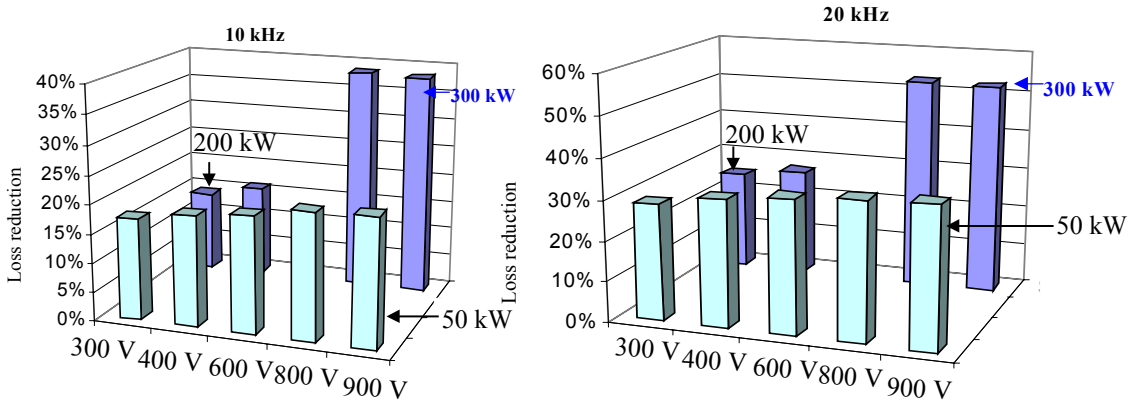
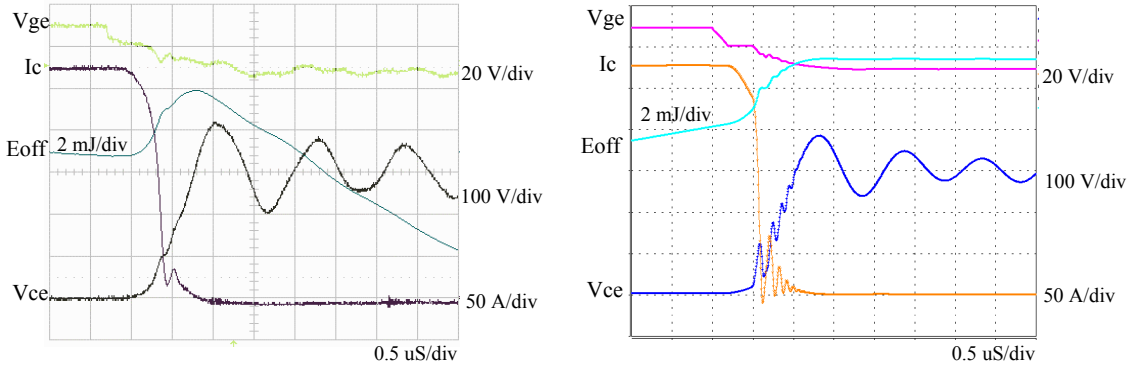


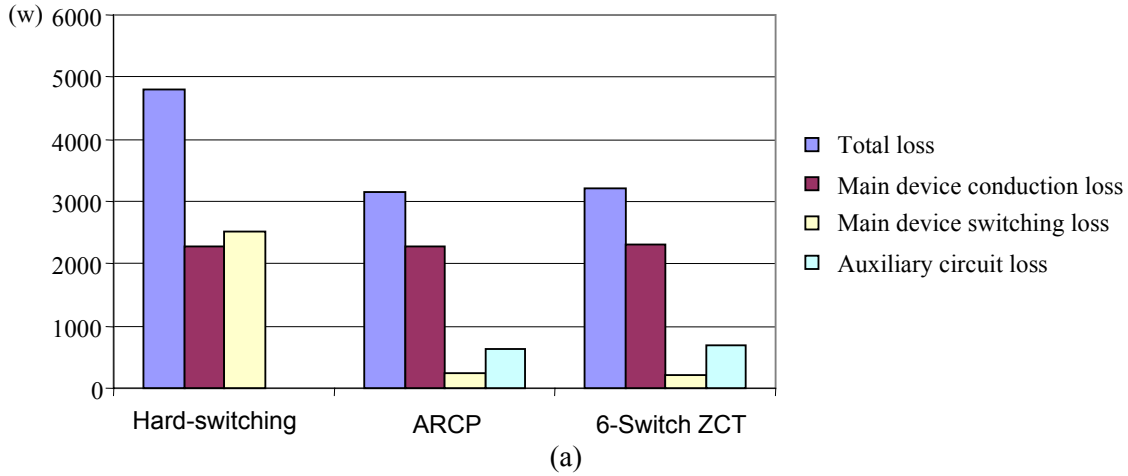
Fig. 5.39. Percentage of the switching loss in the total inverter losses for inverter design.



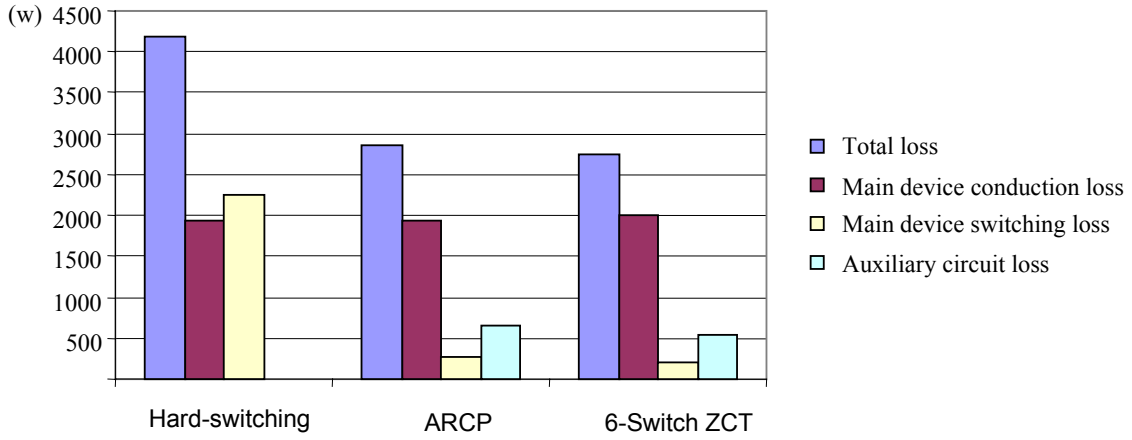
(a) (b)

Fig. 5.40. Turn-off waveform with 0.22 uF snubber capacitor of MG300J2YS50: (a) test and (b) simulation.

The inverter loss breakdown of the hard-switching and soft-switching inverters is shown in Fig. 5.41 for 300 kW power rating and 20 kHz switching frequency. Several observations can be made through the detailed loss data. First, both ARCP and six-switch ZCT inverters can achieve significant loss reduction because the switching loss of the hard-switching inverter is dominant. Second, the conduction loss in the auxiliary circuit of the ARCP inverter is as high as 600 W for 800 V bus voltage. The major reason is that in order to limit the resonant period below 7 uS, the resonant tank design leads to quite high resonant peak current, about 340 A. Even the variable timing control is used, the conduction loss caused by the added resonant peak current portion is considerable. So for the inverter designed at high bus voltage, the MPWSVM should be used to alleviate the effect of the short pulse deletion. Then the resonant inductor value can be increased to reduce the resonant peak current. Third, the auxiliary circuit losses in six-switch ZCT inverter become smaller than that of ARCP inverter for 900 V operation. The reason is that the six-switch ZCT inverter manages to adjust the resonant tank current according to the load current but the ARCP inverter suffers from the higher resonant current.



(a)



(b)

Fig. 5.41. The inverter loss breakdown comparison: (a) 800V bus and (b) 900V bus.

5.5. Summary

So far, an effective systematic electrical simulation modeling approach for the three-phase inverter is proposed. The important modeling methods include a new parameter extraction scheme for the IGBT simulation model, an impedance based parasitic extraction scheme for half-bridge IGBT module and the three-phase bus bar model using the FEA simulation. The new parameter extraction scheme is much simpler as compared with existing schemes, and can facilitate building the advanced IGBT model in Saber simulation. The presented impedance based parasitic extraction method provides a simple and effective means to extract the important parasitic parameters of the IGBT modules, which is crucial for the EMI noise analysis and prediction. Together with the laminated bus bar modeling based on the FEA analysis, the IGBT model parameter extraction and the parasitic extraction forms the key elements of the system simulation. The extensive experiment and simulation in single-leg and there-phase inverter level confirms the validity of proposed extraction schemes and the modeling approach. As a result, the three-phase inverter simulation is able to predict the inverter EMI noise up to tens MHz. The

acceptable accuracy of predicting the switching losses and the switching waveform is also verified through the experiment. Therefore, the systematic electrical modeling approach proposed in this chapter provides an effective means to analyze the performance of the three-phase inverter design. This will greatly save the efforts of developing prototypes. Besides, the optimal design becomes possible with the help of the electrical modeling tool.

With the developed electrical modeling approach, the complete model for ARCP inverter is also developed to further explain the effects of the soft-switching inverter on the conducted EMI. The complete simulation of three-phase ARCP inverter reveals the fundamental mechanism of reducing or increasing the EMI noise. It is concluded that the ARCP inverter can achieve the EMI noise reduction at the high frequency region. There are two reasons for this. One is the much-reduced dv/dt and di/dt brought by the ZVT operation and the other is the alleviated diode reverse recovery leads to suppressed ringing.

The loss reduction possibility is also investigated by developing IGBT models for different EV application designs. Then the loss models for the corresponding IGBT devices are then developed. The loss evaluation of the soft-switching inverter and hard-switching inverter shows that when the EV inverter is designed at 800 V or 900 V to deliver 300 kW output power, the soft-switching inverter shows great loss reduction.

Chapter 6. Conclusions and Future Work

6.1. Conclusions

The major contribution of this dissertation is summarized as follows. First, by developing the accurate device loss model based on experimental characterization, the efficiencies of different soft-switching inverters are compared. High efficiency soft-switching inverters are identified. The correlation of loss reduction, the soft-switching control timing, and the device technology are revealed.

Second, through designing and developing fully operational soft-switching inverters and conducting the extensive dynamometer testing, the comprehensive evaluations of the soft-switching inverter's performance, such as efficiency, conducted EMI performance, THD and voltage stress, are directly conducted for 55 kW EV applications. The evaluation results indicate for 55 kW EV applications and 324 Vdc inverter bus voltage, the soft-switching inverters do not show considerable loss reduction because the conduction losses of power devices are dominant under the switching frequency below 20 kHz.

Third, to provide an effective analysis tool for three-phase inverter design, a simulation based systematic electrical modeling methodology is presented. The electrical modeling approach is systematically composed of three major parts: a new parameter extraction scheme for IGBT simulation model; a measurement based IGBT module parasitic parameter extraction scheme; FEA based model for laminated three-phase inverter bus bar. The new parameter extraction scheme is proposed to facilitate the development of the physics-based IGBT simulation model. This scheme greatly simplifies the existing extraction procedures and allows ordinary application

engineers to develop their own IGBT model. Although simpler than the existing parameter schemes, the accuracy of the new IGBT model parameter extraction method has been fully verified through extensive simulations and experiments. To account for the effect of the parasitic parameters, an impedance-measurement based approach is presented to characterize the parasitic inductance of the half-bridge IGBT module. To include the coupling effects among different phases of three-phase inverter, the laminated bus bar is modeled via the FEA tool.

With the developed IGBT model parameters, the IGBT packaging parasitic model, and the laminated bus bar model, the three-phase inverter EMI simulation is established in a systematic way. The resultant electrical model for the three-phase inverter not only provides a good estimation of the switching losses, but also can predict the conducted EMI noise with an acceptable accuracy at high frequency region up to tens of MHz. Experimental results from hard-switching inverter and soft-switching inverters demonstrate that the developed electrical modeling tool can be used to analyze the switching losses, the voltage stress and the EMI noise.

Some important conclusions have been drawn about the soft-switching inverters' performance in EV applications and physical insights have been obtained with the help of the developed electrical model. In general, the soft-switching inverters' performance on the loss reduction really depends on the device technologies, the soft-switching control schemes, and the application specifications. Although it is clear that the soft-switching inverters do not gain the considerable loss reduction for the small duty EV applications with low bus voltage design, our study suggests the high power and high voltage inverter design offers a great opportunity for the ARCP inverter and the six-switch ZCT inverter to gain significant loss reduction and improve the thermal management. The major reason is that the state-of-art 600V rated IGBT devices have

been optimized to achieve quite small switching losses. However, 1200V rated IGBT devices still leads to more switching losses than the conduction losses when applied to the high voltage bus inverter in EV applications. For the high voltage design, the constraint on the minimum pulse width limits the design of the ARCP inverter. The negative effect is the resultant high resonant peak current. Along with the analysis and evaluation study of the soft-switching inverters, a new SVM scheme, MPWSVM, is proposed to alleviate the harmonic distortion effect caused by the minimum pulse width limit set by the soft-switching inverters. Both simulation and experimental results have verified the effectiveness of the proposed SVM scheme. The MPWSVM offers a promising solution to alleviate the constraints on the resonant inductor design of the ARCP inverter and possibly reduce the resonant current in the auxiliary circuit.

The ZVT inverters can achieve the conducted EMI noise reduction at high frequency region due to reduced dv/dt and suppressed ringing due to the alleviated diode reverse recovery. The detailed reasons of reducing DM and CM are revealed. The ZVS turn-on reduces the diode reverse recovery related ringing and thus the resultant DM noise is much attenuated around the ringing frequency. Besides, the reduced di/dt at ZVS turn-on contributes the DM noise reduction at high frequency region. The slowed dv/dt at ZVS turn-on and the snubbered turn-off can reduce the CM noise at high frequency region. Attentions need to be paid to the snubber capacitor and its layout since the turn-off ringing associated with the snubber capacitor may hurt the conducted EMI performance at particular frequency.

6.2. Future Work

Developing an effective electrical modeling tool not only benefits the analysis and evaluation of the soft-switching inverters in EV applications, but also have great potential in optimizing the design of three-phase inverter, either hard-switching or soft-switching inverters. Although it is verified that the proposed electrical model can achieve fairly accurate analysis results about the switching losses, the stress and the conducted EMI performance, further refinement of modeling work is still needed. For example, some low frequency CM noise is not well modeled and the careful modeling of the CM noise path needs further investigations.

The planar bus bar model based on the Maxwell Q3D has realized the satisfying results in terms of EMI noise prediction. However the modeling process requires a lot of efforts in order to correctly model the geometry data of the bus bar structure. It will be beneficial to study what level of complexity is required for the bus bar model and how to identify the better bus bar design. In general investigations on what is the required accuracy and complexity of component and interconnect models for the three-phase inverter will be very useful for ultimately achieving the integrated electrical-thermal design.

The study suggests that there is great potential to apply soft-switching inverter techniques in high power high voltage EV applications. Therefore, further interesting work is to design and implement an inverter to experimentally verify the analytical results. Although the dissertation has analyzed the effects of the soft-switching inverters using the developed simulation models, the accuracy is achieved with relatively long simulation time due to complicated inverter structure and the detailed device model. It is very interesting to study the effect of the complexity of the overall simulation model on the accuracy of predicted losses, EMI and electrical stresses.

Time-efficient simulation model will be important to optimize the design of a three-phase inverter.

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Appendix A.

Mast Source Code of Anti-parallel Diode Model

#This template is transformed from INFINEON EMCOM Diode Model and it can be directly #used in Saber. The template code for Saber is listed as follows. The listed parameter values are #used for the anti-parallel diode of MG300J2YS50.

```
template l4xxx_met_ns anode kath = a, n_ideal, tj, nd, w0, tau, cj0, a0, kw
electrical anode, kath
number a =  1              # silicon area of diode
number w0 =  70e-4         # length of lightly doped layer
number n_ideal =  1        # scaling factor
number a0 =  -0.71         # coefficient to model the reverse recovery charge
number tj =  27            # junction temperature
number nd =  1.2e14        # doping density
number tau =  .9u          # life time
number cj0 =  2n           # junction capacitance at zero voltage
number kw = 0.3            # coefficient
{
electrical ano, mi, mi1, ano1, ano2, kat, kathv, q_ns, xj1, xj0, jct, cp

#external number ism0
#external number ise0
#external number n_ideal
#external number cj0
#external number n
number epsi =  11.8        # dielectric constant of silicon
number q =  1.602e-19      # electric charge of an electron
number un =  1350          # mobility of electron
number t0 =  273           # absolute temperature
number up =  450           # mobility of holes
#number w0 =  70e-4
number ni0 =  1.45e10
number eps0 =  8.85e-14    # permittivity of vacuum
#number tau =  .9u
number kb =  1.38e-23      # boltzman constant
#number nd =  1.2e14
number bv =  600           #
number rc =  .6m           # resistor of diode
number vlimit =  1.5e7     # voltage limit
number vdiff =  397u       #
```

```
number ut =  25.8m
number d =  17.44          #
number l =  3.96m          #
number xf =  3610          #
number vpt =  450          #
#number a0 =  -0.71
#number a1 =  0.3*(1+a0)/(1-a0)
number a1 =  kw*(1+a0)/(1-a0)
number a2 =  0.1/((1-0.5*(1-a1*a1)*(1-a0)))
number ise0 =  a*391p
number ise_g =  a*0.33p
number ism0 =  a*20.46u
number ism_g =  a*3.204e-19
#number cj0 =  a*4.196n
#number cj0 =  a*1.196n
number qn =  a*0.135u
number rd0 =  0.27/a
number ra =  0.74m/a

var i i1,i2,i3

val nu EGIR, GID, GRQB, GIQ, EXJ, EJUNCT,GD0,GDE
val nu EG,EG27,DA,DA27,ISE,ISE27,ISM,ISM27,xj,w_Td,Td,IQ,Rd

d..model d1 = (is=ise0,n=n_ideal,ibv=1e-10)
d..model d2 = (is=ism0,n=2,ibv=1e-10)
d..model dxxx = (is=1p,cjo=cj0,ibv=1e-10)

r.serie  anode ano =  ra
c.cgde  ano mi =  10p
spv.de  ano ano1 =  dc=0
d.e ano1 mi = model=d1
d.0 ano2 mi1 = model=d2
spv.d0  ano ano2 =  dc=0
spv.id0  mi1 mi =  dc=0
spv.itot  kat kathv =  dc=0
spv.EVDIFF          kathv   kath     =dc = (TJ + t0)* Vdiff
c.qb  q_ns 0 =  1u
r.help  q_ns 0 =  rnom=1meg
c.xj0  xj0 0 =  1
spv.dxj  xj1 xj0 =  dc=0
spv.ijct  jct cp =  dc=0
d.jct 0 cp = model=dxxx
```

```
    values {

    EG=1.16 - 7.02e-4*(TJ + t0)**2/(TJ + t0 + 1108)
    EG27=1.16 - 7.02e-4*(27 + t0)**2/(27 + t0 + 1108)
    DA=2*kb*un*up/q/(un + up)*(TJ + t0)*(((TJ + t0)/300)**-1.5)
    DA27=2*kb*un*up/q/(un + up)*(27 + t0)*(((27 + t0)/300)**-1.5)

    ISE=(TJ + t0)*un*(((TJ + t0)/300)**-1.5)*((ise_g*(ni0*((TJ + t0)/300)**1.5*exp(1/(2*8.61e-
5) \
     *(-300*EG+(t0 + TJ)*EG27)/(TJ + t0)/300)))  \
     *(kb*(ni0*((TJ + t0)/300)**1.5*exp(1/(2*8.61e-5)*(-300*EG+(t0 + TJ)*EG27)/(TJ +
t0)/300))))
    ISE27=(27 + t0)*un*(((27 + t0)/300)**-1.5)*((ise_g*(ni0*((27 +
t0)/300)**1.5*exp(1/(2*8.61e-5) \
     *(-300*EG27+(t0 + 27)*EG27)/(27 + t0)/300)))  \
     *(kb*(ni0*((27 + t0)/300)**1.5*exp(1/(2*8.61e-5)*(-300*EG27+(t0 + 27)*EG27)/(27 +
t0)/300))))

    ISM=Ism_g*(ni0*((TJ + t0)/300)**1.5*exp(1/(2*8.61e-5)*(-300*EG+(t0 + TJ)*EG27)/(TJ +
t0)/300)) \
     *sqrt(DA/(Tau*((TJ + t0)/300)**2))
    ISM27=Ism_g*(ni0*((27 + t0)/300)**1.5*exp(1/(2*8.61e-5)*(-300*EG27+(t0 +
27)*EG27)/(27 + t0)/300)) \
     *sqrt(DA27/(Tau*((27 + t0)/300)**2))

    xj=(XF*SQRT(1-limit_lu(V(ano,mi),-VPT,0)))/SQRT(Nd + MAX(up*(-I(spv.ITOT))/(un +
up),0)/A/q/vlimit)
    w_Td=MAX(w0-xj*(1 + a1),1e-4)
    Td=a2*w_Td*w_Td/DA/(1 + w_Td*MAX(I(spv.DXJ),0)/4/DA)
    IQ=((Tau*((TJ + t0)/300)**2)*I(spv.ID0) - MAX(V(q_ns),1m*QN)*1e-6)/Td

    Rd=w0*w0/(un*QN*(((TJ + t0)/300)**-1.5) + (un + up)*MAX(V(q_ns),1m*QN)*1e-6*(((TJ
+ t0)/300)**-1.5))

    GDE=((ISE**((t0 + TJ)/(t0 + 27)))/ISE27)**((t0 + 27)/(t0 + TJ))    \
     * MAX(I(spv.DE),0)**((t0 + 27)/(t0 + TJ)) - MAX(I(spv.DE),0)
    GD0=((ISM**((t0 + TJ)/(t0 + 27)))/ISM27)**((t0 + 27)/(t0 + TJ))    \
     * MAX(I(spv.D0),0)**((t0 + 27)/(t0 + TJ)) - MAX(I(spv.D0),0)

    EGIR=I(spv.ITOT)*Rd
    GID=IQ - I(spv.IJCT)
    GRQB=1u*V(q_ns)/(Tau*((TJ + t0)/300)**2)
    GIQ=MAX(I(spv.ID0),0) + IQ
```

```
if (time> 25n) {
            EXJ=xj
            }
        else {
            EXJ=0
            }

EJUNCT=LIMIT_lu(V(kat,ano),0,VPT)
}

equations {

      i(ano) += GDE
      i(mi) -= GDE

      i(ano) += GD0
      i(mi1) -= GD0

      i(ano) += GID
      i(mi) -= GID

      i(q_ns) += GRQB

      i(q_ns) -= GIQ

      i(mi) += i1
      i(kat) -=i1
      i1:v(mi)-v(kat) = EGIR

      i(xj1) += i2
      i2:v(xj1) = EXJ

      i(jct) += i3
      i3:v(jct) = EJUNCT

}
}
```

Appendix B.
Model Parameters for IGBT MG300J2YS50

The below is the parameters used for IGBT MG300J2YS50 in Saber simulation as discussed in the dissertation. For the clarify purpose, the exact parameter forms of IGBT model are duplicated from Saber software in Fig. B.1.

tauhl	3.46e-7
tauhltexp	1.4000
taubuf	5.9e-8
taubufexp	1.500001
wb	6.3e-3
wbuf	10e-4
nb	1.87e14
nbuf	1.4e17
a	2.88
agd	0.623
isne	6.0e-13
isnetexp	0.5
vt	9.049
vttco	-0.009
rs	0.003
theta	0.063
thetatexp	0
kf	3
kftexp	0.001
kp	55.75
kptexp	0.8
cgs	2.3e-8
coxd	2.3e-8
vtd	-9
vtdtco	0
bvcbo	800

bvcbotexp	0.35
bvn	4
bvntexp	0
tnom	27
alpha	2.5
gmin	1p
mun	1500
mup	450
pb	0.6
pbuf	1
fc	0.5
mj	0.5
fxjbe	0.5
fxjbm	0.75
vbigd	0.6
a_ref	2.88
kfl	0.05
dvtl	1.140492
rg	0
taurat	1
taurat_texp	
taumod	4
taugen	1.1u
taugen_texp	3
rs_tc1	0
rs_tc2	0

Fig. B. 1. Parameters of the developed MG300J2YS50 Saber simulation model.

As can be seen in Fig. B.1, the saber IGBT model has also other parameters for the purpose of the simulation convergence control and the temperature effects. These non-design parameters are used the same as the default value of the Saber IGBT library model.

Vita

The author, Wei Dong, was born in Dalian, Liaoning Province, P. R. China in 1972. He received his B.S. degrees in electrical engineering and in economics from Tsinghua University, Beijing, China in 1994. Then he received his M. S. degree in electrical engineering in 1996 at the same school.

In 1996, he joined the Virginia Power Electronics Center (VPEC) - now the Center for Power Electronics Systems (CPES) as a research assistant. He joined Ford Motor Company as a summer intern in 1998. He has been the team leader for several research projects such as the PNGV project, the distributed power system (DPS) team, and the pulsed load high density DC-DC converter project. He chaired the 2000 CPES annual seminar. From May of 2001, he started to work in CPES as the DPS research program manager. His research interests include soft-switching inverters, the EMI modeling, DC-DC converters and the power factor correction techniques.