Silicon-Based RFIC Multi-band Transmitter Front Ends for Ultra-Wideband Communications and Sensor Applications

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submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

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March 27, 2007

Blacksburg, Virginia

Keywords: PLL, UWB, VCO, Mixer

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(ABSTRACT)

Fully integrated Ultra-Wideband (UWB) RFIC transmitters are designed in Si-based technologies for applications such as wireless communications or sensor networks. UWB technology offers many unique features such as broad bandwidth, low power, accurate position location capabilities, etc. This research focuses on the RFIC front-end hardware design issues for proposed UWB transmitters. Two different methods of multiband frequency generation — using switched capacitor VCO tanks and frequency mixing with single sideband mixers — are explored in great detail. To generate the required UWB signals, pulse generators are designed and integrated into the transmitter chips.

The first prototype UWB transmitter is designed in Freescale Semiconductor $0.18\mu m$ SiGe BiCMOS technology for operation over three 500 MHz bands at center frequencies of 4.6/6.4/8.0 GHz, and generates pulses supporting differential BPSK modulation. The transmitter output frequency is controlled by a two-bit code which sets the state of a switched capacitor tank array for coarse tuning of the VCO. While selecting between the different bands, the transmitter is capable of settling and re-transmitting in less than $0.7\mu s$ using an integrated, wide band phase-locked loop (PLL). Various issues such as mismatch/inaccuracy of the pulses and high power consumption of the prescaler were identified during the first design and were addressed in subsequent design revisions.

The pulse generator is a critical part of the proposed UWB transmitter. The initial pulse generator design used CMOS delay lines and logic gates to synthesize the required pulse bandwidth; however this approach suffered from inaccurate pulse timing control due to delay time sensitivity to device modelling and process variations. Subsequently, a novel pulse generator design capable of achieving accurate timing control was implemented using digital logic and a fixed oscillator frequency to provide timing information, integrated into a modified transmitter circuit, and subsequently fabricated in Jazz Semiconductor's $0.18\mu m$ CA18 RFCMOS process. Experimental results

confirm the generation of accurate one-nanosecond pulses.

Finally, a new multiband UWB transmitter based on a new single sideband (SSB) resistive mixer with superior linearity and zero static power consumption was also designed and fabricated using Jazz CA13 0.13μm RF CMOS process. This design is based on a fixed frequency phase-locked VCO and generates different bands through frequency mixing. In the prototype design, two additional carrier frequencies are generated from the VCO center frequency (5 GHz) by mixing it with its output divided-by-4 (1.25 GHz). By switching the relative I/Q phases of the LO/IF inputs to this single side band mixer, either the upper side band (6.25 GHz) or lower side band (3.75 GHz) frequency is selected at the mixer output, while the other sideband is rejected. Simulation results show that the transmitter is capable of generating the desired carrier frequencies while suppressing the image component by more than 40 dB.

Overall, this work has explored various aspects of UWB transmitter design and implementations in fully integrated silicon chips. The major contributions of this work include: proposed hardware architectures for pulse-based multiband UWB transmitters; implemented a fully integrated multiband UWB transmitter with embedded phase-locked switched-tank VCO capable of wide frequency tuning; demonstrated an all digital pulse generator capable of generating accurate one-nanosecond pulse trains in the presence of various mismatches; and investigated resistive SSB mixer topologies and their implementation in a multiband UWB generation architecture.

Acknowledgements

First of all, I would like to thank my advisor, Dr. Sanjay Raman for his guidance and support throughout this work. His dedication and ingenious ideas to the excellency of RF microelectronics research provides the constant resource and insight to this research.

I would also like to thank Dr. Athanas, Dr. Bostian, Dr. Buehrer and Dr. Guido for reviewing my thesis and serving on my advisory committee.

I would like to thank M. Burnham, B. Kump, D. Monk, K. Kraver, and C. Dozier. of Freescale Semiconductor, Tempe, AZ for their Support.

I would like to thank George Studtmann, Jian Zhao of M/A-COM, Roanoke, VA, for their help with the testing board design and fabrication.

I would like to thank Ryan Bunch of RFMD for his help with the chip package.

I would like to thank C. Anderson from MPRG for his help with the Tektronix CSA8000 Signal Analyzer.

I would like to thank M. Hoffman from Agilent for help with Infiniium DSO8124A real-time oscilloscope.

I would like to thank Dan Huff at Virginia Tech for fabrication assistance.

I would like to thank previous WML members, Christopher Maxey, Arvind Narayanan and Richard Svitek.

It has been a pleasure to work with the Graduate Research Assistants at the wireless microsystems lab, Ibrahim ichamas, Krishna Vummidi Murali and Mark Lehne. They have been constant source of technical advice and entertainment throughout my study

at Virginia Tech.

After all, this is for my wife.

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Chapter 1

Introduction

With the rapid advances in wireless technology since the early 1990s, wireless communication services have expanded from voice-based analog cellular networks to complex digital voice and data networks. Concurrent developments include wireless local and personal area networks (LANs/PANs), enabling connectivity among computers, home electronics, cell phones and personal data devices, etc. However, as such wireless communication networks expand to support more users and multimedia data, more bandwidth is needed. A given frequency band can only support a limited number of applications and users simultaneously at a certain location; in addition mutual interference increases as the bands become more crowded with ever increasing demand from users. For example, the now ubiquitous WiFi and Bluetooth standards both reside in the 2.4 GHz ISM[1] band along with cordless phones, greatly increasing the interference level in this range. In addition, microwave ovens operate near the same frequency, further increasing the interference. In the 5-6 GHz range, both UNII[2] bands and ISM bands are defined with overlap around 5.8 GHz which may create potential interferences between different applications such as cordless phone and in-home wireless LANs operating near those frequencies.

Given the congestion at lower frequencies, the emergence of Ultra-Wideband (UWB) technologies has attracted significant attention due to the much greater available bandwidth. The primary UWB spectrum occupies a total of 7500 MHz of band-

[1] ISM stands for *Industrial, Science and Medical* [1].
[2] UNII stands for *Unlicensed National Information Infrastructure* [2].

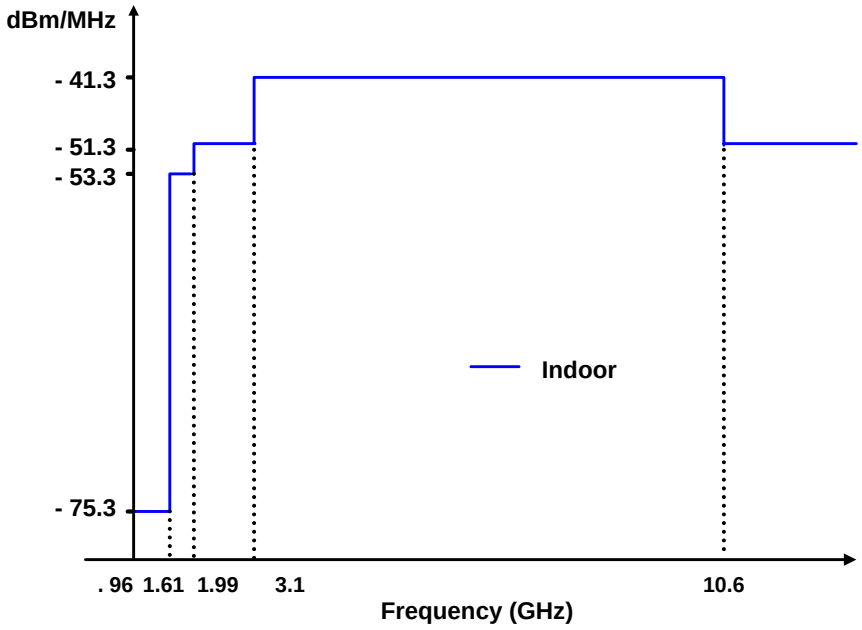


Figure 1.1: Ultra wide band spectrum mask for indoor applications.

width from 3.1-10.6 GHz, with an emission mask of -41.3 dBm/MHz. The Federal Communications Commission (FCC) has defined a UWB device *as any device where the fractional bandwidth is greater than 0.20 or occupies 500 MHz or more of spectrum while meeting the spectral mask requirement* (Fig. 1.1) [2]. The formula for the fractional bandwidth BW_f is:

$$BW_f = \frac{BW}{f_c} \times 100\% = \frac{f_H - f_L}{\frac{1}{2}(f_H + f_L)} \times 100\% \tag{1.1}$$

where f_H and f_L are the upper and lower -10 dB emission point frequencies, respectively.

1.1 Unlicensed Frequency Bands

With the addition of UWB, there are currently three major unlicensed bands below 10 GHz available in the US assigned by FCC targeting home networking, short-range communications, etc. As mentioned above, the other two unlicensed bands are the ISM bands, with available bandwidths of 26 MHz at 900MHz and 83.5 MHz at 2.4

GHz [1], and the UNII bands with available bandwidth of 555 MHz in the 5-6 GHz range [2]. Table 1.1 lists the frequency allocations of these unlicensed bands. For the ISM bands, there are three primary frequency ranges at 902-928 MHz, 2.4-2.48 GHz and 5.725-5.85GHz, with a maximum transmitted power level of 1W. The UNII band is composed of four ranges 5.15-5.25GHz, 5.25-5.35 GHz, 5.47-5.725 GHz and 5.725-5.825 GHz, with maximum transmitted power levels of 50mW, 250mW, 250mW and 1 W, respectively.

In comparison to the above technologies, UWB has two unique features: first it has enormous bandwidth, i.e. a total bandwidth of 7.5 GHz ranging from 3.1 GHz to 10.6 GHz, which is more than 10 times the total bandwidth of the other unlicensed bands below X-band combined; second, it is required to emit very low power levels of -41.3dBm/MHz, significantly lower than typical narrow band systems. For example, the maximum output power for a UWB transmitter with a bandwidth of 528 MHz is:

$$P_{out} = -41.3 + 10\log 528 = -14.07dBm(39.1\mu W) \tag{1.2}$$

which is less than 0.1% of the maximum UNII band transmitted power. The significantly larger bandwidth of UWB offers the potential for very high data rates (up to the Gbps range) for short range communications, and enables bandwidth-intensive applications such as multimedia and wireless USB. Meanwhile, the extremely low power mask requirement specified by the FCC ensures that UWB can coexist benignly with all the existing wireless communication devices, including GPS systems[3], satellite communication systems, cell phones, and wireless LAN.

1.2 Wireless Data Standards

Currently, there are several existing wireless data network standards available in the US operating in the unlicensed ISM and UNII bands (Table 1.2). WLANs comply with the IEEE 802.11 standards: 802.11b uses CCK[4] (high data rate mode) and

[3]GPS stands for Global Positioning System and is used extensively for automotive navigation, military and surveying applications etc. GPS is currently the only full functional satellite navigation system, using frequency at 1575.42 (L1), 1227.60 (L2), 1381.05 (L3), 1379.913 (L4) and 1176.45 (L5) MHz.

[4]CCK stands for *Complementary Code Keying.*

Unlicensed Band	Frequency (GHz)	B (MHz)	Power	Power (dBm)
ISM (< 10 GHz Range)	0.902-0.928	26	1 W	30
	2.4-2.4835	83.5	1 W	30
	5.725-5.850	125	1 W	30
UNII	5.15-5.25	100	50 mW	17 (4 + 10logB)
	5.25-5.35	100	250 mW	24 (11 + 10logB)
	5.47-5.725	255	250 mW	24 (11 + 10logB)
	5.725-5.825	100	1 W	30 (17 + 10logB)
UWB	3.1-10.6	7500	74 nW/MHz	-41.3 + 10logB

Table 1.1: US spectrum allocation for ISM, UNII and UWB bands. B=Bandwidth

	IEEE Standard	R_b (Mbps)	Frequency (GHz)
WLAN	802.11a	$\leq$54	5 (UNII)
	802.11b	$\leq$11	2.4 (ISM)
	802.11g	$\leq$54	2.4 (ISM)
WPAN	802.15.1 (Bluetooth)	$\leq$1	2.4 (ISM)
	802.15.4	$\leq$0.25	2.4, 0.915/0.868 (ISM)

Table 1.2: Dominant short range wireless data standards. R_b=BitRate

DSSS[5] (low data rate mode) as its modulation techniques, supporting data rates up to 11Mbps in the 2.4 GHz ISM band [3]; 802.11g uses OFDM[6] as its modulation technique, supporting data rates up to 54 Mbps in the 2.4 GHz ISM band [4]; 802.11a uses OFDM as its modulation technique, supporting data rates of up to 54 Mbps in the 5 GHz UNII band [5]. Meanwhile, WPANs comply with the IEEE 802.15 standards: Bluetooth resides in the 2.4 GHz ISM band, and is based on FHSS[7] technique, transmitting at a symbol rate up to 1 Ms/s [6]; 802.15.4 Task Group targets low data rate (less than 250kbps) applications such as interactive toys, sensor and automation needs using both 900 MHz (800 MHz in Europe) and 2.4 GHz ISM bands [7].

Figure 1.2 (data from [1]-[5]) shows various wireless standards in their respective frequency locations. As can be seen, the UWB emission levels are well below any other technologies. It is required that a UWB device operating between 3.1 - 10.6 GHz have an output level less than -41.3dBm/MHz. In order to protect the GPS

[5]DSSS stards for *Direct Sequence Spread Spectrum.*

[6]OFDM stands for *Orthogonal Frequency-Division Multiplexing.*

[7]FHSS stands for *Frequency Hopping Spread Spectrum .*

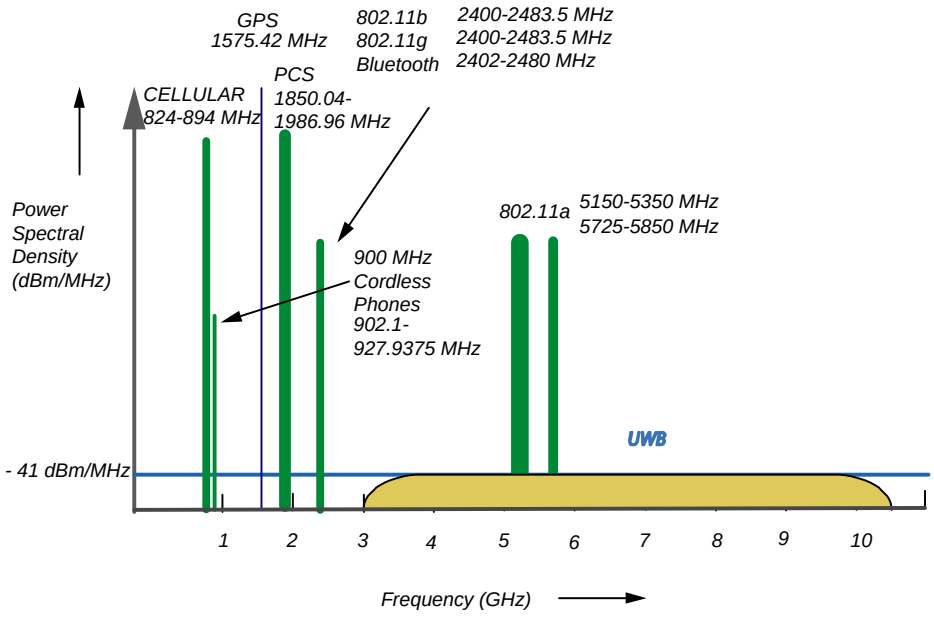


Figure 1.2: Ultra wide band spectrum and current wireless standards (not to scale).

spectrum, the emission level of an indoor UWB device between 0.96 - 1.61 GHz should be less than -75.3 dBm/MHz. Note that the 5GHz UNII bands are in the middle of the maximum UWB emission mask of -41.3 dBm/MHz. The interference between the UNII bands and the UWB spectrum can be alleviated by avoiding 5-6 GHz range entirely for UWB devices.

1.3 Impulse Radio-based UWB System

Ultra-wide band technology has its origin in *impulse radio,* which has been studied since the early 1940s [8]. An impulse radio may generate very short pulses directly from baseband without a carrier, with the corresponding spectrum extending from DC all the way up to microwave frequencies [9]. Due to their extremely wide bandwidth, such systems are capable of reduced interference, resistance against jamming, enhanced encryption and low probability of interception. Potential modulation schemes for UWB impulse radio are shown in Figure 1.3 [8], including On-Off Keying (OOK), Pulse Amplitude Modulation (PAM), Binary Phase Shift Keying (BPSK) and Pulse Position Modulation (PPM).

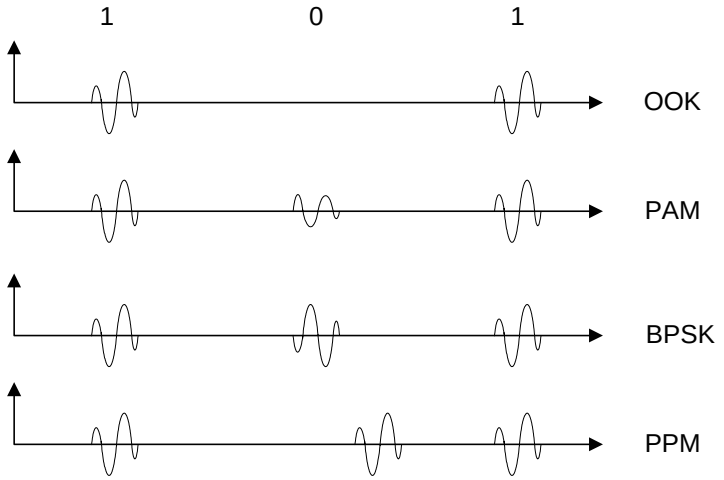


Figure 1.3: Various modulation techniques for impulse radio.

Potential advantages of an impulse radio based UWB system includes low complexity, low power, relaxed phase noise requirements, lower sensitivity to multipath, lower interference level, position location capability, low probability of interception and lower susceptible to interference [10]. UWB signals have also been demonstrated to propagate through certain obstructions that cannot be penetrated by conventional narrowband systems [11]; this property can be exploited for through-wall imaging systems and ground penetrating radar.

Of particular interest to wireless data applications, UWB impulse radio systems are resistant to multipath fading compared to narrow band systems. In narrow band systems, received multipath signals of a given symbol can overlap with a subsequent received symbol due to multipath delay; because multipath delays are less than the symbol duration, the received signal from multipath can add either constructively or destructively (Fig. 1.4) [12]. On the other hand, for a pulsed UWB system, the multipath delay is longer than the pulse width, such that the received pulse due to multipath can be resolved. Meanwhile, the multipath delay is shorter than the timing between two consecutive pulses, and no overlap will occur between the multipath signals of the two symbols.

Owing to its ultra short time-domain pulses, impulse radio based UWB systems are also excellent candidates for position and ranging applications. Impulse radio based systems transmit with very short pulse durations ($\sim ns$), similar to those used in

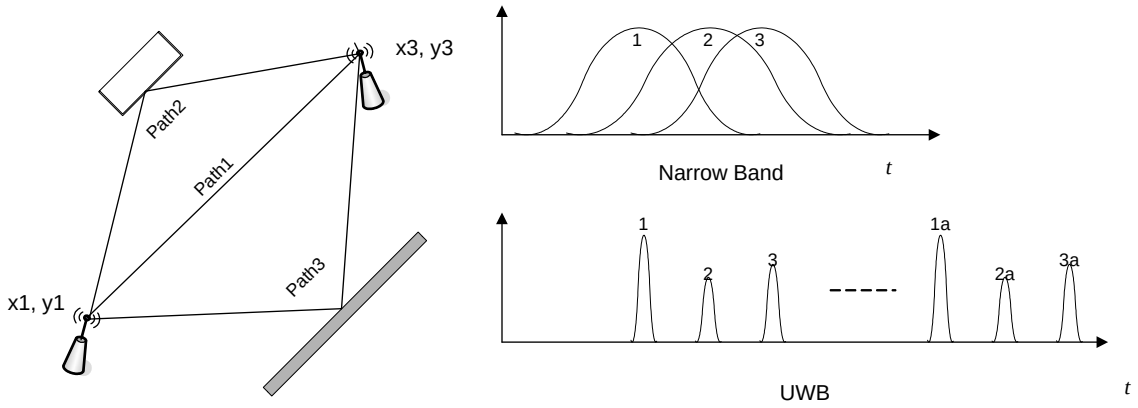


Figure 1.4: Multipath fading in narrow band vs. UWB systems.

radar systems. The resulting fine range resolution enables the system to have very accurate position location capability. The range resolution possible with a UWB system is much better than that of narrow band systems since the receiver is able to resolve much smaller time intervals between two incoming pulses. This is a very useful feature for various applications where GPS position location is not available. A UWB-based position location system is also less susceptible to jamming due to its wide bandwidth; GPS systems are more sensitive to narrow band interference and jamming.

There are four basic techniques for radio-based ranging: Time of Arrival (ToA), Time Difference of Arrival (TDoA), Received Signal Strength Indication (RSSI) and Angle of Arrival (AoA) [13][14]. The first three techniques require a minimum of three base stations in communication with each sensor in the network, while AoA requires at least two base stations. A straightforward UWB position location concept based on ToA is shown in Fig. 1.5(a) [15]. The two dimensional target position (x, y) can be defined using three reference wireless nodes, by computing the following quantities:

$$\Delta_i = r_i - \sqrt{(x - x_i)^2 + (y - y_i)^2} \qquad i = 1, 2, 3 \tag{1.3}$$

$$where \quad r_i = \frac{c}{2}(t_i - t_{i0}) \tag{1.4}$$

and where $(x,\ y)$ and $(x_i,\ y_i)$ are the coordinates for the target and reference wireless nodes respectively; t_{i0} is the time at which a reference sends out a beacon to the target sensor, t_i is the signal arrival time at the i^{th} reference node from a sensor, which sends

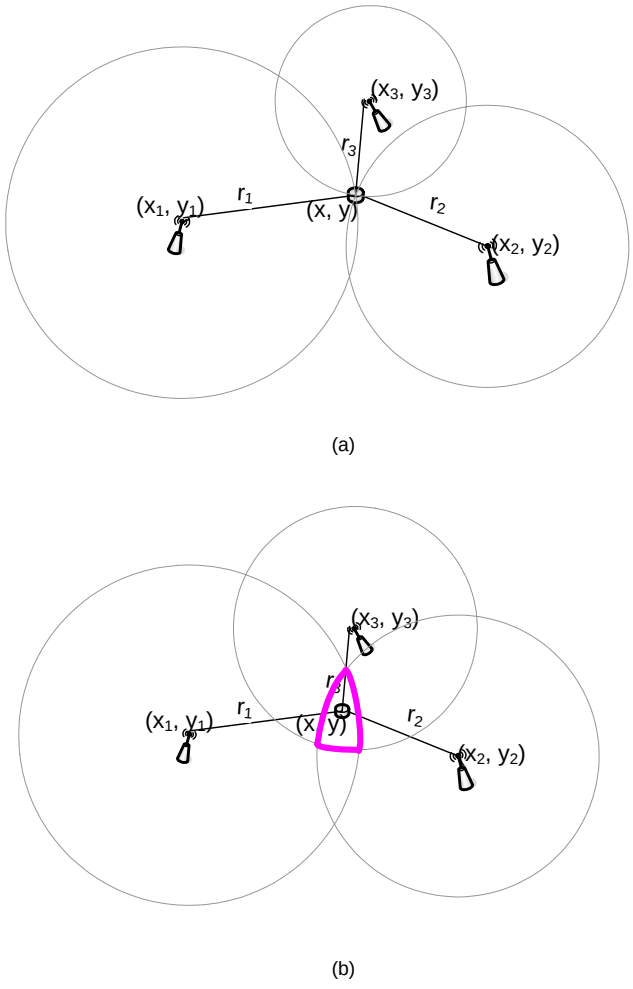


Figure 1.5: (a) ToA for position location with perfect timing information. (b) ToA for position location with timing measurement errors.

out beacon immediately after receiving an inquiry from the reference node; and c is the speed of light. The target sensor location may be found by computing the minimum square error Δ^2 :

$$\Delta^2 = \min \sum \Delta_i^2 \tag{1.5}$$

The accuracy of the system depends on both the pulse width and time synchronization between the wireless reference nodes. Due to the inevitable measurement errors, the estimated target sensor is actually located inside the intersection of three measured circles 1.5(b).

One example of commercial UWB ranging is the UWB RFID tag system developed

by Ubisense [12]. This real-time positioning system was certified by the FCC for commercial use in December 2004. Ubisense UWB RFID tags have been advertised as being able to locate objects to less than 6 inches of accuracy.

1.4 UWB Standards

In the late 90s, UWB technology emerged as a potential solution for the IEEE 802.15.3a standard for WPAN, targeting high-data-rate, short-range multimedia applications. The proposed UWB technology for 802.15.3a uses one or more carrier frequencies modulated by a baseband signal, which is essentially an extension of conventional narrowband wireless technology. Meanwhile, UWB technology has also been adopted as a physical layer by the 802.15.4a low data rate task group.

1.4.1 IEEE 802.15.3a Task Group

In the early stages of UWB standards development, two industrial alliances competed to define the UWB standard with their own proposals. On one side, major companies such as Texas Instruments, Intel, Phillips, NEC, Infineon, etc. (the so called MBOA alliance) promoted Multiband Orthogonal Frequency Division Multiplex Ultra-Wideband (MB-UWB), a similar technology to that now in use for the 802.11a and 802.11g standards; on the other side, an alliance formed by Freescale Semiconductor, Xtreme Spectrum, etc. were pursuing Direct Sequence Ultra Wide Band (DS-UWB).

In the MBOA proposal, the UWB frequency spectrum from 3.1 GHz to 10.6 GHz is divided into 14 channels, 528 MHz for each channel (Fig. 1.6) [16]. The center frequency of each band can be expressed as:

$$f_c = 2904 + 528 \times n(MHz),\ where\ n = 1, 2 \ldots 14 \tag{1.6}$$

The basic principle of OFDM is to split a high data rate signal into a number of lower data rate signals which are simultaneously transmitted over equally spaced subcarriers. In the case of the MBOA proposal, each 528 MHz channel is divided into $128 \sim 4$ MHz tones. As proposed, OFDM UWB could support variable transmission

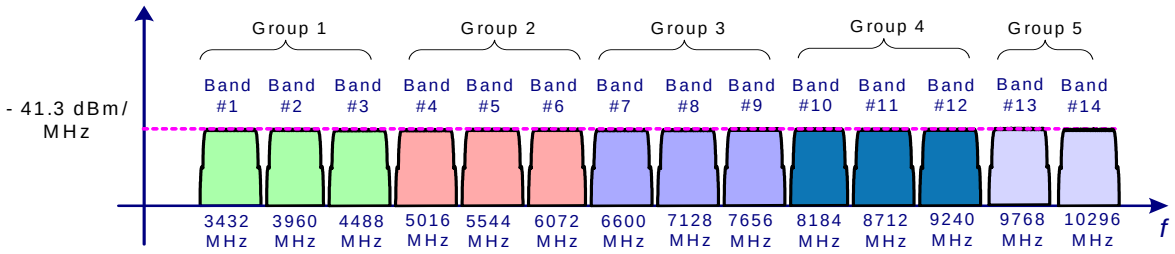


Figure 1.6: OFDM UWB frequency band allocations.

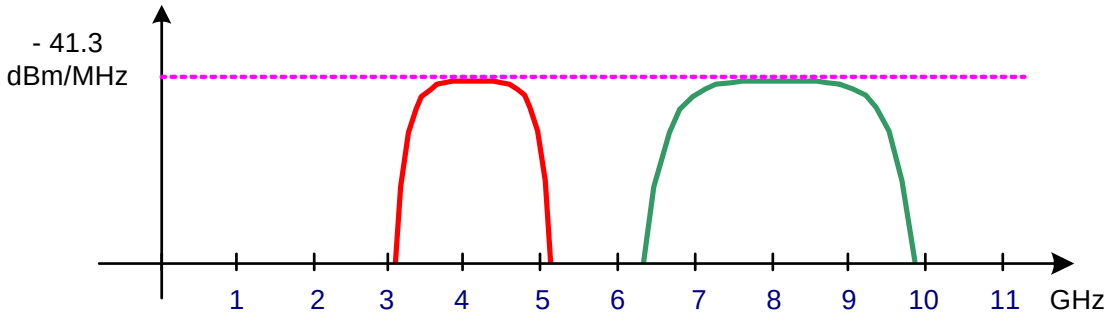


Figure 1.7: DS-UWB frequency band allocations.

rates of 55, 80, 110, 160, 200, 320 and 480 Mbps. This system is robust to multipath fading and intersymbol interference due to the low symbol rate carried by each of the orthogonal sub-carriers.

Meanwhile, the DS-UWB alliance proposed a system employing direct sequence spreading of binary phase shift keyed (BPSK) UWB signal. This system is capable of transmitting variable data rates of 28, 55, 110, 220, 500, 660, and 1320 Mbps. DS-UWB supports operation in two independent bands: the lower band occupies spectrum from 3.1 GHz to 4.85 GHz (1.75 GHz of bandwidth) and the upper band occupies spectrum from 6.2 GHz to 9.7 GHz (3.5 GHz bandwidth), as shown in Fig. 1.7 [17]. DS-UWB uses BPSK as the basic modulation method due to its low complexity and ease of implementation.

Because the two sides were unable to reach to a compromise, or gather over 75% of the votes to be accepted as the sole standard, the IEEE 802.15.3a task group was officially disbanded by the IEEE standards association in the spring of 2006. The MBOA proposal supporters evolved into the WiMedia alliance [18], continuing the development

of the MB-OFDM UWB systems, while DS-UWB group continues to work under the auspices of the UWB Forum [19]. Freescale Semiconductor subsequently left the UWB Forum in 2006 to develop its own "Cable Free" UWB solutions.

1.4.2 IEEE 802.15.4a Task Group

Concurrently, the IEEE 802.15.4a Low Rate Alternative Physical Layer (PHY) Task Group for Personal Area Networks (WPANs) was established in March 2004 to develop an alternative PHY to amend 802.15.4 [20]. TG4a focuses on wireless specifications for providing low data rate communications and ranging/location capability (1 meter accuracy and better), high aggregate throughput, longer range, and lower power consumption and cost [20]. Impulse radio based UWB is an excellent candidate for TG4a applications due to its position location capability.

The 802.15.4a TG selected a baseline specification with two optional PHYs consisting of: (1) UWB impulse radio or (2) chirped spread spectrum in the 2.4 ISM band. In contrast to 802.15.4 (low data rate), the UWB impulse radio will be able to deliver both communication and precision ranging. The baseline specification for UWB impulse radio covers the 3.1 GHz - 4.9 GHz range and offers data rates up to 10 Mbps.

1.5 UWB Transmitter for Sensor Networks

Wireless sensor networks are a rapidly emerging technology for commercial, industrial and military systems, including control and monitoring operations (Fig. 1.8) [21]. Meanwhile, sensor technology is evolving towards miniaturization, multi-sensor platforms, and wireless system integration [22].

An impulse radio based UWB system is a competitive candidate for complex wireless sensor systems, owning to its low transmitted power, flexibility, resistance to interference jamming and multipath, ability to be operated in certain obstructed environments, and precision ranging capabilities typically not available from narrow band wireless systems. A UWB based sensor network can accommodate information of various data rates, such as high data rate video sensors, medium data rate acoustic sensors, as well as low data rate environmental sensors, etc. In UWB based

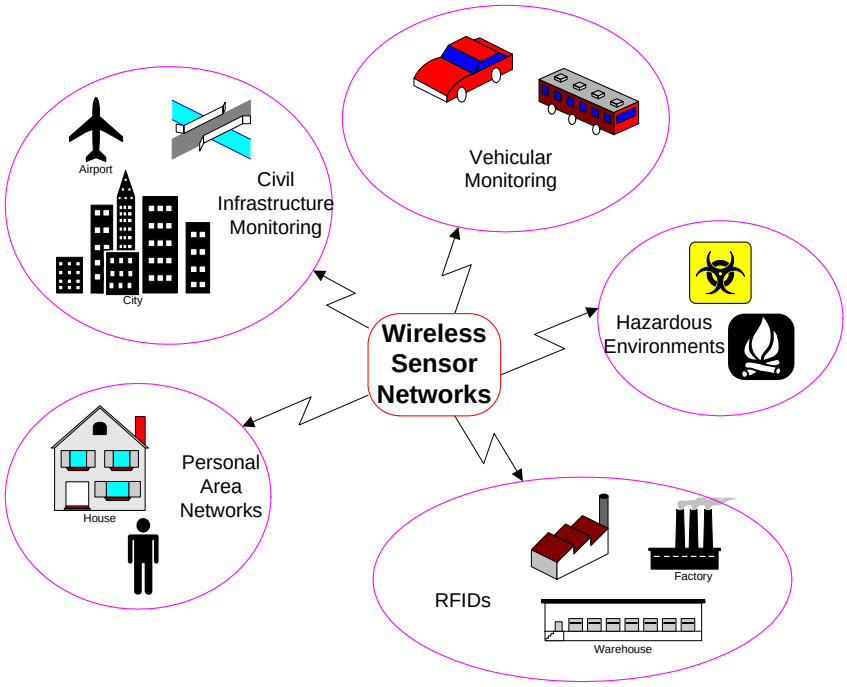


Figure 1.8: Potential wireless sensor network applications (RFID stands for Radio Frequency Identification).

sensor networks, different sensor nodes could share the same band by employing time division multiple access or code division multiple access. In addition, by employing short UWB pulses, a distributed wireless sensor network could obtain good position location information for each node owing to the short UWB pulse widths. Such a position location system is also robust against jamming signals compared to GPS-based systems due to its wide bandwidth, and will continue to operate in the areas absence of GPS coverage, especially for indoor and sky-obstructed locations.

The operation of the wireless sensor network can be viewed as a hierarchical architecture (Fig. 1.9). Multiple sensor nodes inside of the a network communicate either to an access point or to each other. A clusters of sensor nodes can be networked together through a control center. For each sensor node, a sensor interface circuit acts as the bridge between the specific sensor devices and the wireless transmitter. The interface might vary due to different sensing mechanisms; however there is a fundamental need for conversion from analog sensor signals to digital data streams. This requires a sensor interface circuit which converts sensor information to a voltage

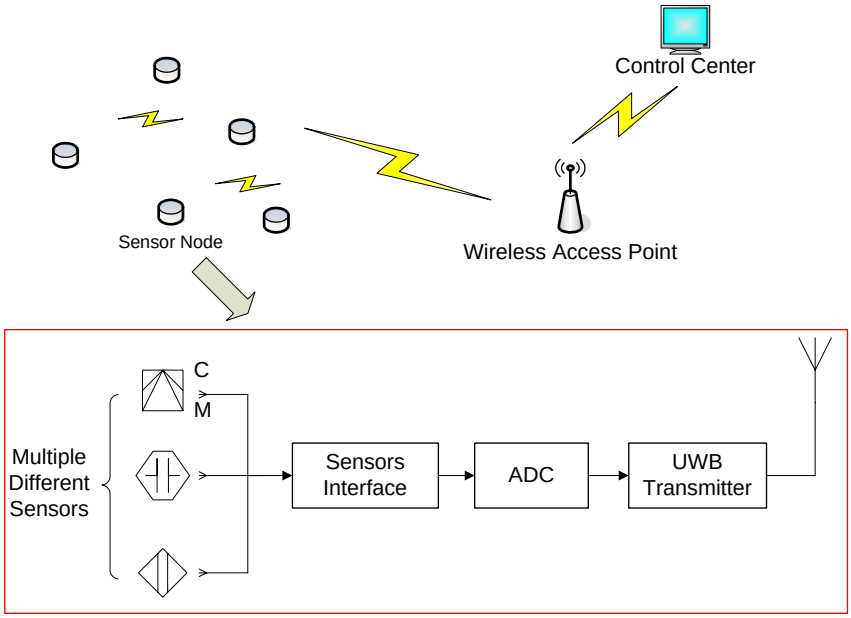


Figure 1.9: Architecture of a wireless sensor network

or current signal; as well as an analog-to-digital converter that matches the specific data rate speed requirement of the sensors.

1.6 Proposed Multiband UWB Architecture

In order to design a communications framework for a sensor network, the major requirements of such systems must be considered. A typical sensor network is to be deployed for extended periods of time in hostile or remote areas. The sensor nodes comprising the network should have the following properties: low maintenance; robust in harsh environments; low cost to allow deployment in large quantities; and low profile. Since wireless sensor nodes are to be employed in large quantities, ultra-miniature, low cost RF microsystems operating at UWB spectrum are in demand for those sensor systems. Meanwhile, the advance of RFIC technologies has led to a continuous reduction in the size of wireless components; complete "system-on-chip" (SOC) solutions are now prevalent for various mainstream applications. Therefore, low cost, single chip, UWB-based RFIC nodes are excellent candidates for wireless sensor networks where precise position location is of interest.

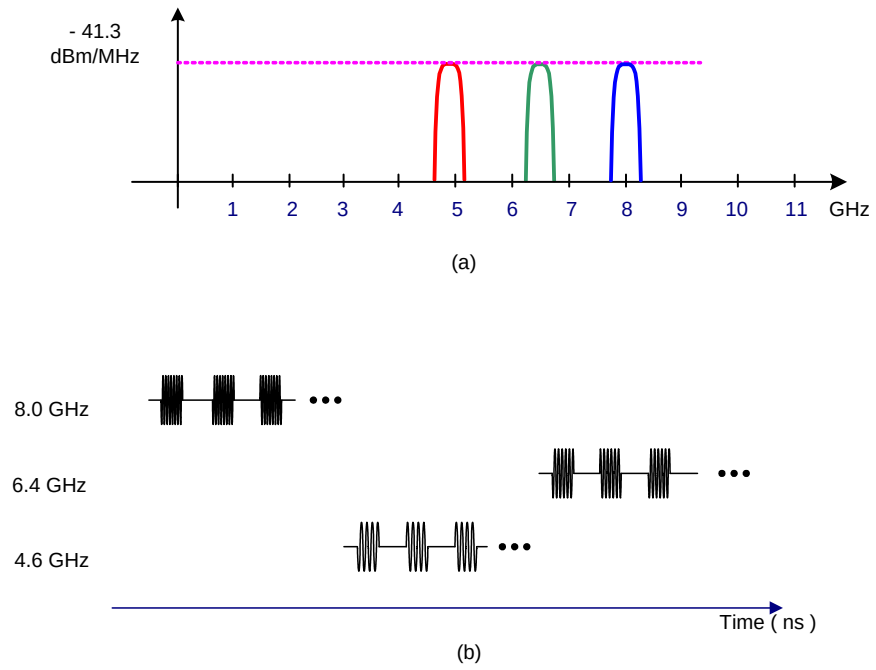


Figure 1.10: Proposed three channel UWB system for the wireless sensor nodes. (a) Three frequency channels. (b) Transmitted DBPSK symbols in three channels.

Instead of using a baseband UWB system, this work proposed to employ multiband carrier-based UWB transmitter in which the majority of the transmitting power is concentrated around the carrier frequency complying with FCC UWB mask. In the initially proposed sensor network architecture, a three channel approach is employed for proof of concept purposes. The three selected bands are centered at frequencies of 4.8 GHz, 6.4 GHz, and 8 GHz, with each band occupying a 500 MHz (Fig. 1.10) bandwidth. The 5-6 GHz unlicensed (UNII) bands are avoided here to reduce potential interference. This design can ultimately be modified to include additional bands in the 3.1-10.6 GHz space.

The proposed transmitter architecture uses pulsed noncoherent Differential Binary Phase Shift Keying (DPSK) as the modulation scheme [23]. DPSK is a noncoherent modulation technique with information encoded in the phase difference of any consecutive symbols which avoids the need for coherent reference at the receiver [24]. The differential encoded binary sequence $\{d_k\}$ is generated from binary input $\{m_k\}$

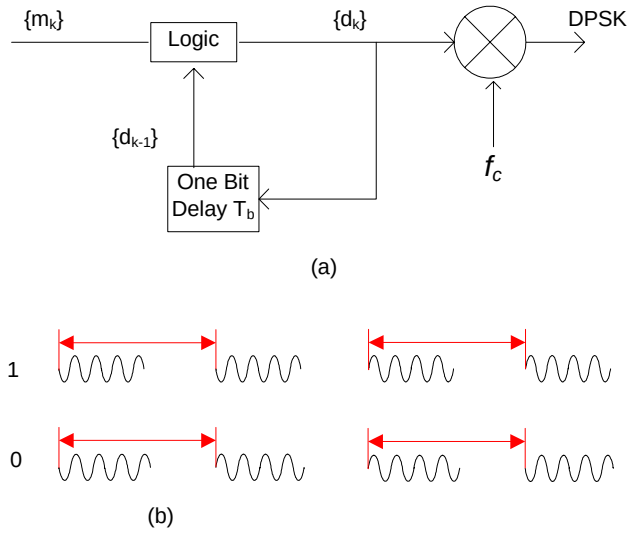


Figure 1.11: Differential binary shift keying: (a) Block diagram of DPSK transmitter, (b) DPSK signal.

by complementing the modulus sum of m_k and 1-bit delayed output d_{k-1} (Fig. 1.11):

$$d_k = \overline{m_k \oplus d_{k-1}} \tag{1.7}$$

This work initially focuses on the design of RF front end and UWB pulse generation hardware based on this scheme; a detailed baseband scheme can be found in [25].

This UWB transmitter may support multiple users through using PN sequences processed at baseband. By employing a long spreading code, the operating range may be extended at the expense of a lower data rate. A combination of convolution coding and spread spectrum coding may also be used at base band to increase the energy to noise ratio through coding gain, therefore extending the transmit range.

In this work, a DPSK signal with pulse width of 4ns and a guard time of 6ns is transmitted. The power spectrum of transmitted signal in the frequency domain has a first-null bandwidth of ∼500 MHz. One pulsed DPSK symbol is transmitted every $10ns$. A Matlab simulation of the transmitted signal spectrum of a pulsed DPSK with random data inputs is shown in Fig. 1.12.

In this work, a RFIC wireless front end was developed to support the proposed carrier based multiband UWB approach for wireless sensor network applications [26].

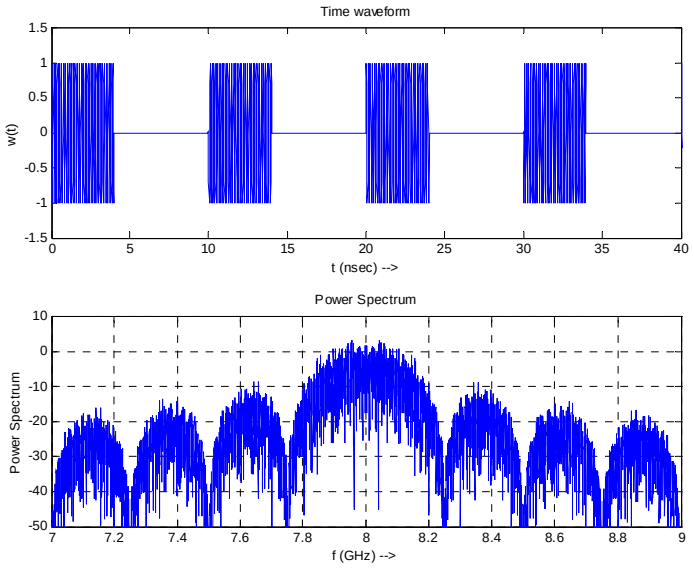


Figure 1.12: Simulated time waveform and frequency spectrum of the DBPSK pulse generator output with random data input (carrier frequency at 8 GHz).

The majority of the RF/analog/mixed-signal circuitry part of the transmitter was planned to be integrated in a single chip, except for an off-chip clock reference, power amplifier and antenna. The wireless sensor transmitter architecture is composed of three major on-chip components (Fig. 1.13): (1) a fast lock PLL, which switches frequency bands under the control of a pseudorandom code generator; (2) a moderate speed and accuracy analog to digital converter (ADC) used to digitize the received analog sensor data; and (3) a pulse generator, designed to synthesize the short pulses needed for Ultra-Wideband transmission.

The design challenges include, but are not limited to: (1) design of a complete UWB transmitter front end from system level down to the circuit level and implementing on the Si chip; (2) development of new circuit topologies for the system; (3) integration of complicated multiband transmitter including both RF and digital components on the same RFIC; (4) Phase locked loop is complicated system by itself and present a big challenge to be designed and integrated on a Si chip with other circuit components and interference (5) Theoretical development of the single side band mixer demand extensive mathematical derivations and literature research as well as sound understanding of the related technologies.

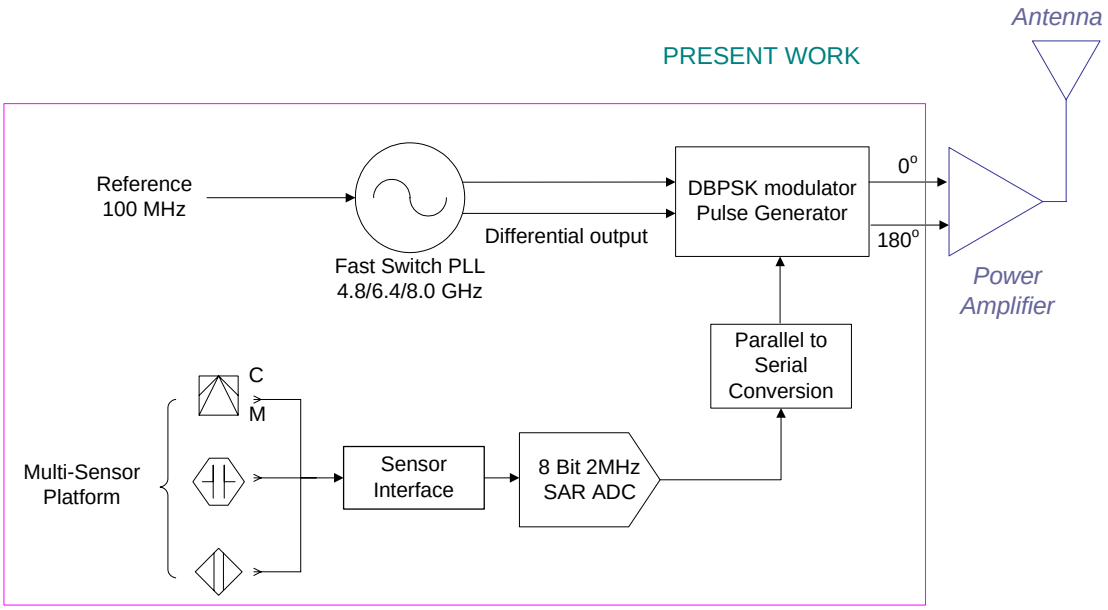


Figure 1.13: Prototype UWB RFIC transmitter architecture.

1.7 IC Technology

Advances in IC technology over the last two decades have enabled dramatic improvements in the performance and functionality of electronic devices such as personal computers and cell phones. Moore's law predicts that the performance of the integrated circuit doubles at regular intervals. This has been the trend for the IC technology over the last 40 years, with the minimum feature size of transistors shrinking from several μm to 45 nm in today's state-of-the-art process. In the 90s, RFIC technology development led to more and more RF front end functions being packed into a single Si chip, with a few exceptions such as power amplifiers still being produced as separate GaAs chips and PA modules. With the low transmit power requirement (no high power PA required) and relaxed specifications compared to narrow band systems, it is potentially cost-effective to offer complete UWB solutions in a single low cost Si chip.

Characteristic	Value	Unit
$f_t/f_{\max}$ (HBT)	50/90	GHz
$f_t/f_{\max}$ (NMOS)	60/50	GHz
MIM capacitor	1.6	fF/μm^2
Inductor (Q @ 2 GHz)	18	(L=3nH)
Metal Layers	5	Layers

Table 1.3: Characteristics of devices in the HiP6WRF Technology

1.7.1 Freescale 0.18μm SiGe RF BiCMOS

The first prototype UWB transmitter in this work is designed using Freescale's HiP6WRF 0.18μm SiGe RF BiCMOS. This process features a 0.18μm low-power 1.8 V CMOS process with dual gate oxide MOS devices and 5 layers of Cu metallization [27]. Low V_t CMOS, isolated CMOS, analog BJT, high quality passive devices and a SiGe:C HBT device are integrated for mixed signal and high performance RF applications. SiGe HBT transistors provide higher speed, better current gain and lower noise figure than MOS transistors [28]. The transconductance of a HBT device is directly proportional to its collector bias current, while for a long channel MOS transistor the transconductance is proportional to the square root of its drain current. With the same bias current, a HBT transistor provides considerably higher transconductance than a NMOS transistor at these minimum gate lengths. Published typical devices characteristics are summarized in Table 1.3 [27].

1.7.2 Jazz CMOS

Two subsequent UWB transmitters are designed and fabricated using Jazz CA18HR 0.18μm and CA13HA 0.13μm CMOS processes, respectively. Both process offer high quality RF passive components such as high density MIM capacitors and high Q inductors. Table 1.4 [29][30] shows some typical values for the Jazz RF CMOS technology.

Characteristic	CA18HR	CA13HA	
V_{dd}	1.8/3.3	1.2/3.3	V
f_t (NFET)	-	90	GHz
MIM capacitor	4	5.6	fF/μm^2
Inductor (Q @ 2.4 GHz)	>25		
Metal Layers	6	6	#
Top Metal thickness	3	3	μm

Table 1.4: Characteristics of devices in the Jazz CA18HR and CA13HA Technology

1.8 Objective

The objectives of this work are to:

- Design and demonstrate monolithic ultra wide band transmitters in Silicon-based RFIC technologies for wireless sensor node applications;
- Design high speed prescalers for both PLL and I/Q phase generation;
- Design multiband switched tank VCO for wide band PLL;
- Integrate a new carrier based UWB multiband transmitter with SSB mixer and quardrature VCO;
- Research multiband fast locking phase locked loop designs based on switched tank VCO cell capable of extremely wide tuning range.

The pulse generator is a critical component for the proposed UWB system: this work proposes and implements a new digital pulse generator. In addition to a PLL based UWB transmitter system, this work also develops another multiband system based on a new low-voltage resistive single sideband mixer design. Different aspects of each multiband system and their unique properties are researched in great detail. Novel components and circuit topologies are developed and researched to enhance the performance of the multiband UWB transmitter.

1.9 Overview of Dissertation

This chapter has covered the background and motivation for a UWB transmitter design targeting the application of sensor networks; it also presents the initial prototype UWB transmitter architecture. Chapter Two covers the design of an integrated switched tank VCO which is a key part of the initial transmitter design, including detailed analysis of the switched tank circuit. Passive on-chip components including on-chip inductors and varactors are also discussed in this chapter. Chapter Three presents the design issues related to different PLL components including frequency dividers, the phase frequency detector, and the charge pump circuitry. The pulse generator and lock detector designs are also covered in this chapter. Measurement results of phase locked loop performance and pulse generator performance are presented in Chapter Four. Then, an improved CMOS UWB transmitter design with a novel pulse generator is presented in Chapter Five, along with its measured results. Chapter Six presents a single sideband resistive mixer design required for a multiband UWB transmitter. Chapter Seven presents the new multiband transmitter design. This multiband design can also be extended to MB-OFDM systems. Chapter Eight presents conclusions and further work. Sensor interface blocks designed as part of this work are discussed in the Appendix, including a capacitance-to-voltage conversion circuit, operational amplifier, and analog-to-digital converter.

Chapter 2

SiGe BiCMOS Switched-Tank VCO for Multi-band UWB Transmitter

The prototype multiband UWB transmitter was designed to select one of three carrier frequencies at 4.8/6.4/8.0 GHz. It is not possible to use a single set of the available varactors to achieve this wide frequency tuning range from 4.8 GHz to 8.0GHz (67%). Therefore, in this work, a *switched capacitor tank* VCO was designed to achieve the wide overall band tuning range. This VCO is designed to oscillate at its highest frequency while the additional capacitor states are turned off. The VCO is tuned into lower frequency bands with combinations of the extra capacitor states switched in. At the time this work was started this approach was relatively new, but has now become relatively common in commercial designs. The main challenges are: design of a multiband switching VCO with adjustable tuning range in each band; maintain good performance at the high band since it is most sensitive to additional tank parasitics; insertion loss and limited isolation of CMOS switches which may lower the VCO performance. All of the above issues are to be considered carefully when designing the VCO switching scheme. Understanding on-chip tank components such as capacitor tank switches, NMOS varactors and integrated inductors is critical to this VCO design.

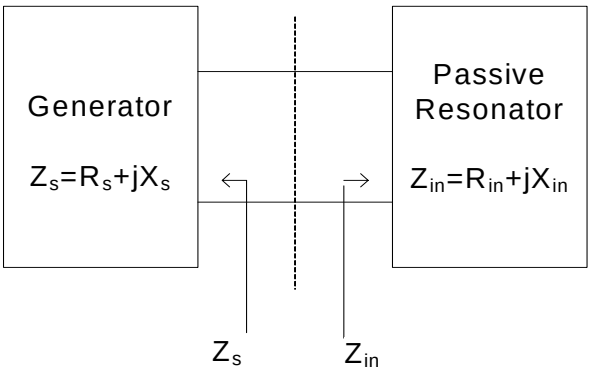


Figure 2.1: One-port negative resistance view of an oscillator.

2.1 Oscillator Core

An oscillator can be viewed as a negative resistance in parallel with a RLC network (Fig. 2.1). The parallel inductor/capacitor tank circuit sets the resonant frequency of the oscillator. The loss in the tank circuit is represented by the real part R_{in} which dissipates the energy of the circuit. The negative resistance part represents the energy supplied to the system by an active circuit. In the stable oscillation condition, the energy generated by the negative resistance part will exactly offset the losses represented by the tank resistance. This can be expressed mathematically as:

$$R_s + R_{in} = 0 \tag{2.1}$$

$$X_s + X_{in} = 0 \tag{2.2}$$

In order to start the oscillation, the sum of R_s and R_{in} should actually be *less* than zero, so that the oscillation amplitude can build up until an amplitude limiting mechanism brings the sum back to zero for the stable oscillation condition.

The LC tank is viewed as a parallel RLC network with quality factor

$$Q = \frac{R_p}{\omega L} = R_p \omega C \tag{2.3}$$

The tank quality factor is a very important indicator of the oscillator performance since it is directly related to the phase noise of the oscillator. The quality factor of the VCO tank degrades as extra load R_L is applied to the tank, and is defined as the

loaded quality factor.

$$Q_L = \frac{R_p \parallel R_L}{\omega L} = Q \cdot \frac{R_L}{R_p + R_L} \tag{2.4}$$

A semi-empirical equation for the phase noise of a tank oscillator was developed by Leeson, based on a linear time invariant assumption [31]:

$$L\{\Delta\omega\} = 10 \log \left\{ \frac{2FkT}{P_s} \left[1 + \left(\frac{\omega_0}{2Q_L \Delta\omega} \right)^2 \right] \left(1 + \frac{\Delta\omega_{1/f^3}}{|\omega|} \right) \right\} \tag{2.5}$$

where F is an empirical parameter called the "device excess noise factor" contributed by the active devices, k is the Boltzmann's constant, T is the absolute temperature (in Kelvin), P_s is the power output of the oscillator, ω_0 is the resonant frequency, Q_L is the loaded quality factor, $\Delta\omega$ is the frequency offset from ω_0, and $\Delta\omega_{1/f^3}$ is the corner frequency between the $1/f^3$ and $1/f^2$ regions. From Leeson's equation, it can be seen that a lower Q of the tank degrades the phase noise while all other conditions remain the same. Alternatively, the power supplied by the active circuit must be increased to achieve the same phase noise, which results in higher DC power consumption. As an integrated VCO uses on-chip varactors and inductors for the LC tank, it is important to understand the operation and loss mechanisms of these components.

A simplified diagram of a cross-coupled bipolar transistor pair LC oscillator is shown in Fig. 2.2. It consists of a negative resistance pair providing the energy to start up and sustain oscillations, and a passive LC tank circuit to set the resonant frequency. The impedance of the parallel LC tank peaks at its resonant frequency and decreases as the frequency deviates from the center frequency.

The transistor pair cross-couples between the base and collector of the two transistors, providing positive feedback. A small voltage increase at the collector of Q_1 increases the base to emitter voltage V_{be} of Q_2. As a result, the collector current I_{c2} increases. Since the tail current $I_{tail} = I_{c1} + I_{c2}$ is assumed to be constant the collector current I_{c1} of Q_1 decreases which in turn decreases the collector voltage of Q_2. This process will continue until the collector current I_{c2} of Q_2 reaches it maximum and I_{c1} becomes zero. Meanwhile the collector voltage of Q_1 reaches its maximum and that of Q_2 reaches its minimum. At this point, if the tank circuit were just a resistor, the whole circuit behaves as a latch and reaches its stable state. For an LC tank however, the

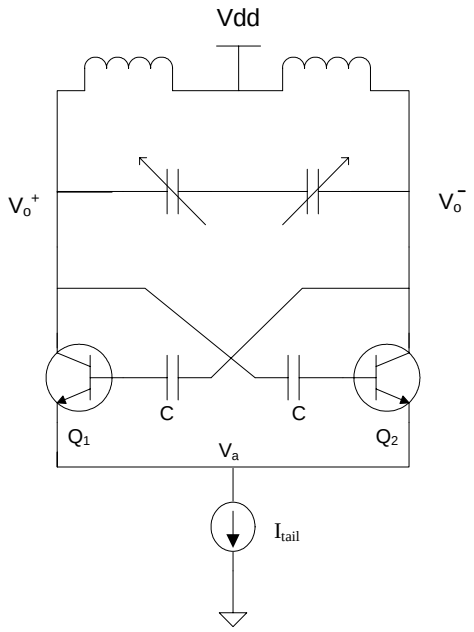


Figure 2.2: Schematic of a cross-coupled transistor pair VCO.

energy stored in the capacitor starts to release at this point and reverses the voltage swing.

The differential small signal equivalent circuit of the cross-coupled transistor pair is shown in Fig. 2.3 (parasitic capacitances are neglected here). The differential input voltage V_{in} of the cross-coupled transistor pair is the difference between its positive and negative collector voltages:

$$V_{in} = V_o^+ - V_o^- \tag{2.6}$$

and the collector voltages are complementary to each other:

$$V_o^+ = -V_o^- \tag{2.7}$$

Therefore, the collector voltages can be expressed in terms of the differential input voltage:

$$V_o^+ = 0.5V_{in} \tag{2.8}$$

$$V_o^- = -0.5V_{in} \tag{2.9}$$

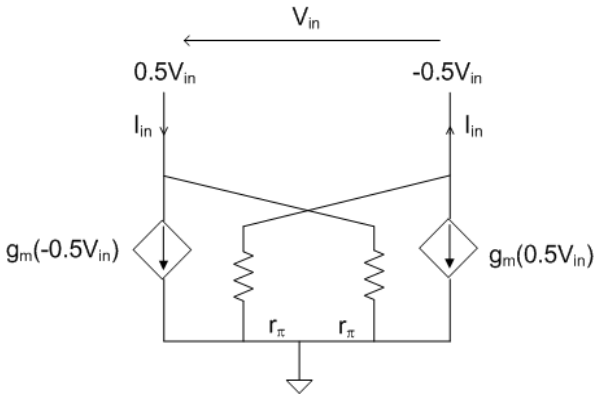


Figure 2.3: Equivalent differential small signal circuit of a cross-coupled transistor pair.

Consequently, the voltage controlled current source of Q_1 is

$$I_{c1} = -0.5 g_m V_{in} \tag{2.10}$$

and the voltage controlled current source of Q_2 is

$$I_{c2} = 0.5 g_m V_{in}. \tag{2.11}$$

The differential current flow I_{in} in and out of the collectors of the cross-coupled transistor pair is therefore

$$I_{in} = I_{c1} = -I_{c2} = -0.5 g_m V_{in} \tag{2.12}$$

Finally, the equivalent resistance R_a of the cross-coupled transistor pair can be expressed as:

$$\begin{aligned} R_a &= \frac{V_{in}}{I_{in}} \\ &= \frac{V_o^+ - V_o^-}{I_{in}} \\ &= \frac{V_{in}}{-0.5 g_m V_{in}} \\ &= -\frac{2}{g_m} \end{aligned} \tag{2.13}$$

Please note that the g_m here is the "small signal" transconductance of the transis-

tor at the DC bias point. To accurately model the VCO operation, the large signal transconductance should be used instead due to the large signal nature of the VCO. For bipolar transistors, the small signal transconductance g_m is defined as the derivative of collector current I_c of base to collector voltage V_{be}: $g_m = \frac{\partial I_c}{\partial V_{be}} = \frac{I_c}{V_T}$. Generally, this transconductance is used to set the absolute value of the negative resistance to be about 2-3 times of the equivalent parallel tank resistance, therefore ensuring that the oscillator will start up. The actual final value of the bias current is determined through simulation.

2.2 Varactors

On-chip varactors with reasonable performance are now used extensively in commercial RF ICs. There are two main categories of monolithic varactors: PN junction diode varactors and MOS varactors. MOS varactors can be further classified as standard PMOS varactors, inversion mode MOS varactors, and accumulation mode MOS varactors [32][33]. PN junction diode varactors use a reverse bias voltage to change the depletion width of the junction, thereby varying the capacitance. Due to their junction resistance, diode varactors tend to have lower Q and smaller tuning range compared to MOS varactors. In order to achieve wider tuning range, diode varactors need to reduce the reverse bias voltage to operate in the moderate reverse biased or even weakly forward regions with resulting low quality factor.

For a standard PMOS device used as a varactor, the drain/source/bulk are connected to the same terminal (D=S=B). A conceptual diagram of PMOS varactor operation is shown in Figure 2.4. In accumulation mode, the gate has a positive voltage with respect to bulk and attracts electrons under the gate ($V_{bg} < 0$); the maximum capacitance is approximately equal to the gate oxide capacitance ($C_{ox} \cdot W \cdot L_{eff}$). As the gate voltage is decreased, electrons under the gate are repelled and a depletion region is formed under the gate. The capacitance is therefore reduced since it is now the gate capacitance and channel-bulk depletion capacitance in series. A further decrease in gate voltage with respect to bulk will cause an inversion layer to form under the gate with $V_{bg} > |V_{th}|$, and capacitance again reaches the gate oxide capacitance. A MOS varactor can be modified to operate only in accumulation mode or inversion mode. An inversion mode varactor (I-MOS) is achieved by tying its bulk connection

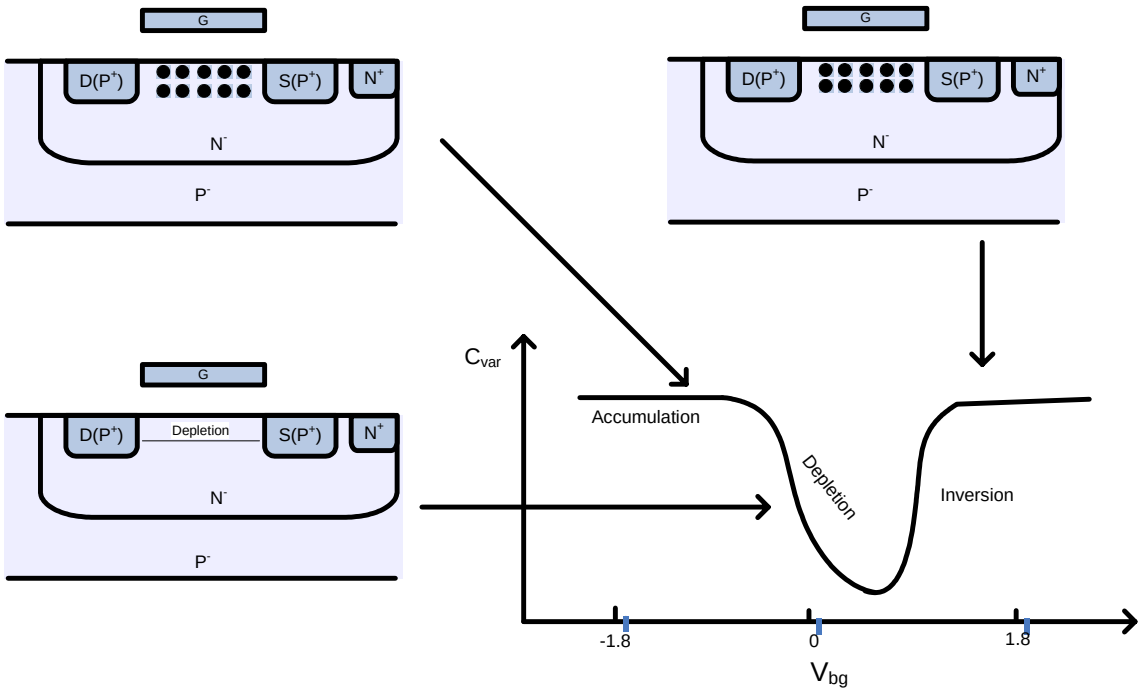


Figure 2.4: A PMOS varactor operating curve in three regions: accumulation, depletion and inversion.

to the highest supply voltage, therefore preventing that transistor from entering the accumulation region [33].

An accumulation mode MOS varactor (A-MOS) is a PMOS device with its P^+ drain/source regions replaced by N^+ regions (Figure 2.5) [32]. The A-MOS varactor operates in accumulation mode with a positive gate voltage and depletion mode with reduced gate voltage. However, as the gate voltage decreases further below the threshold, the device does not go into inversion due to the lack of supply of holes (no P^+ D/S regions). The capacitance reaches its minimum value at the gate threshold. The A-MOS varactor gives excellent control of its capacitance (monotonic function vs. tuning voltage) and wide tuning range. Other advantages include smaller size since no bulk connection needed and high quality factor due to the higher electron mobility compared to the lower hole mobility.

An accumulation mode MOS varactor is available in the HIP6WRF BiCMOS process used in the initial stages of this research, with Q values between 10 to 40. The varactor is simulated using S-parameter simulation in SpectreRF[34] with its gate

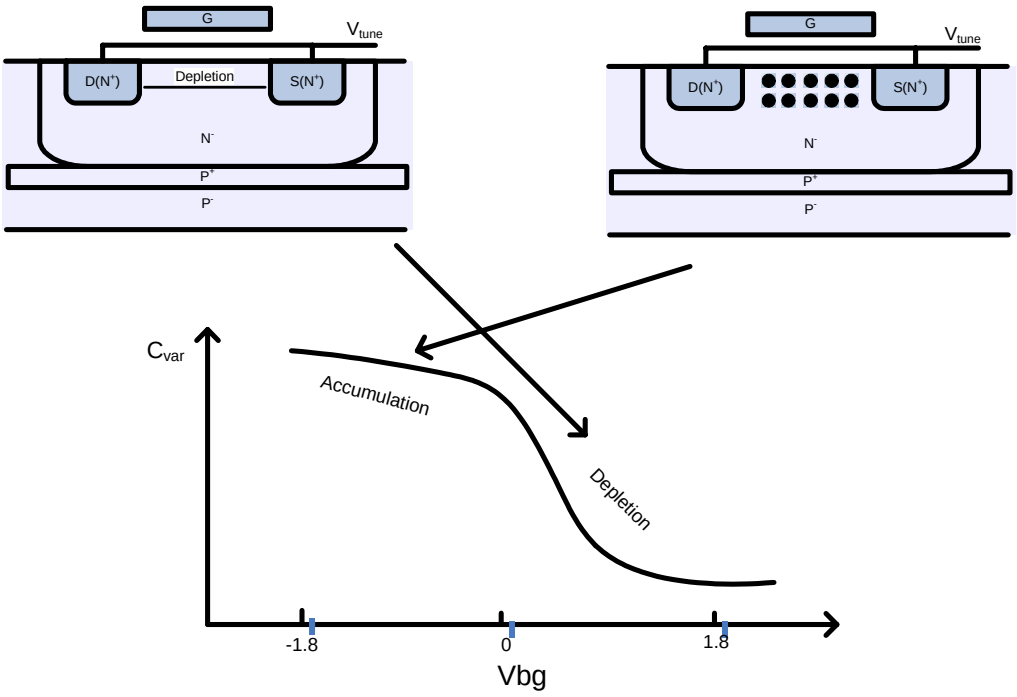


Figure 2.5: An A-MOS varactor operating curve in accumulation and depletion regions.

voltage fixed at 1.8V and sweeping its bulk voltage V_b from 0 to 2V (Fig. 2.6). The effective capacitance and quality factor are calculated using

$$C_{eff} = \frac{\mathrm{Im}(Y_{11})}{j\omega} \tag{2.14}$$

$$Q_{eff} = \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}\,(Y_{11})} \tag{2.15}$$

The Q of the varactor can also be approximated as:

$$Q = \frac{1}{\omega C R_n} \tag{2.16}$$

where C is the equivalent series capacitance and R_n is parasitic nwell resistance in series with the capacitor. The quality factor Q of the varactor is therefore lowered at high capacitor values since R_n changes little with the tuning voltage, while C varies with the tuning voltage. As the capacitance decreases from the maximum value in accumulation region, the varactor Q tends to increase due to the smaller series capacitance.

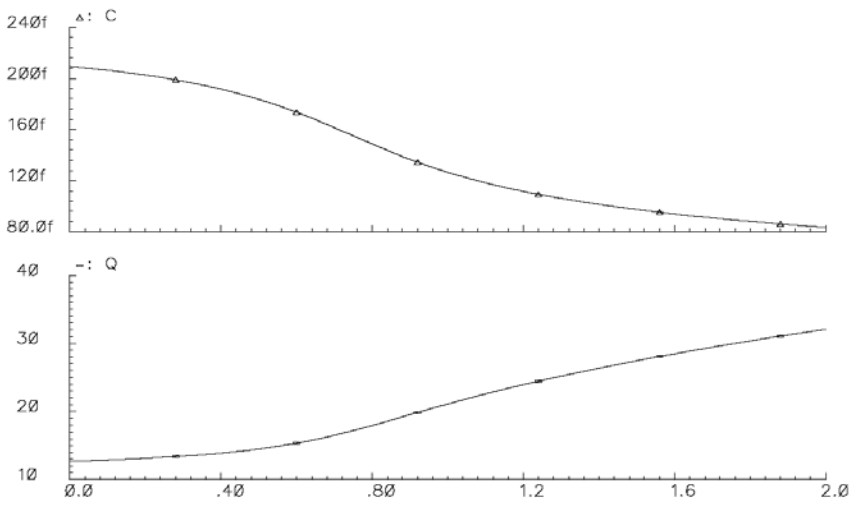


Figure 2.6: SpectreRF simulated quality factor and capacitance curve of an A-MOS varactor.

2.3 Monolithic Inductors

Monolithic spiral inductors with reasonable Q (peak Q around 10-20) are now commonly available in silicon technologies for RFIC/MMIC applications. A simple equivalent circuit model for an on-chip inductor is shown in Figure 2.7 [35]. In this model, the inductor L_S represents the series inductance of the spiral; at first order it is determined by the number of turns and overall size of the inductor, as shown in equation 2.17:

$$L_s \approx \mu_0 N^2 r \tag{2.17}$$

where μ_0 is permeability of free space, N is the number of turns, and r is the radius of the spiral. The resistor R_s in series with the inductor L_s accounts for the loss of the metal trace and other interconnections. R_s is a function of frequency and can be given by the equation:

$$R_S \approx \frac{l}{w \cdot \sigma \cdot \delta(1 - e^{-t/\delta})} \tag{2.18}$$

where, δ is the skin depth

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \sigma}} \tag{2.19}$$

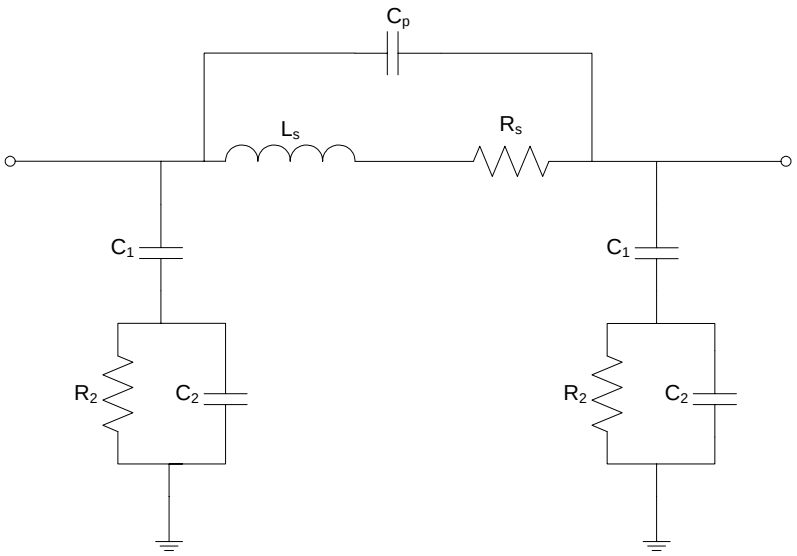


Figure 2.7: Silicon monolithic inductor equivalent circuit model.

and where l is the total trace length, t is the metal thickness, w is the width of the trace, σ is the conductivity of the metal, and ω is the radian frequency. R_s tends to increase at higher frequencies due to the skin effect. A parallel capacitor C_P models the inter-winding parasitics (Eq. 2.20) and shunt capacitors C_1 (Eq. 2.21) model the parasitics between the metal trace of the inductor and the substrate

$$C_P = n \cdot w^2 \cdot \frac{\varepsilon_r}{t_r} \tag{2.20}$$

$$C_1 = \frac{1}{2} w \cdot l \cdot \frac{\varepsilon_r}{t_r} \tag{2.21}$$

where, ε_r and t_r are the permittivity and thickness of the dielectric from metal trace to substrate, respectively. R_2 and C_2 model the the substrate loss and coupling, respectively.

$$R_2 \approx \frac{2}{w \cdot l \cdot G_{sub}} \tag{2.22}$$

$$C_2 \approx \frac{w \cdot l \cdot C_{sub}}{2} \tag{2.23}$$

where G_{sub} is the effective substrate conductance per unit area, C_{sub} is the effective substrate capacitance per unit area.

It is beneficial to use octagonal shaped differential inductors as shown in Figure 2.8. The V_{cc} supply is connected to the common mode output at the top of the inductor while VCO output nodes are connected to the differential inductor inputs at the bottom. A differential inductor has higher Q value ($\approx 150\%$) due to mutual coupling between its plus and minus turns compared to two series connected single-ended inductors laid out symmetrically. The magnetic fields of differential currents are in the same direction and reinforce each other, resulting in a higher mutual coupling coefficient. An octagonal inductor also has a smaller footprint compared to a rectangular inductor with the same inductance value, and therefore has less substrate coupling loss and series loss. A custom octagonal differential inductor was designed for this work and simulated using Agilent EEsof Momentum EM simulation software[36]. For the same inductance value, a larger size inductor with less turns has higher Q since the inner turns provides less inductance but more loss (due to eddy currents) compared to the outer turns. The custom inductor is designed with small area while still having reasonable Q values. The extracted three port S-parameters are then used in Cadence to simulated the VCO performance.

A simplified two port model to calculate differential inductance and quality factor is shown in Figure 2.9. Two port S-parameters are converted to equivalent Z-parameters. A differential voltage ($+V_{in}/2,\ -V_{in}/2$) is applied across the differential input of the inductor. The relationship between the differential input voltage and differential current is then:

$$V_{diff} = I_{diff}Z_{11} + Z_{12}\left(-I_{diff}\right) - Z_{21}I_{diff} + Z_{22}I_{diff} \tag{2.24}$$

and the equivalent differential impedance is:

$$Z_{diff} = \frac{V_{diff}}{I_{diff}} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \tag{2.25}$$

From the equivalent differential impedance Z_{diff}, the differential quality factor and effective inductance can be calculated:

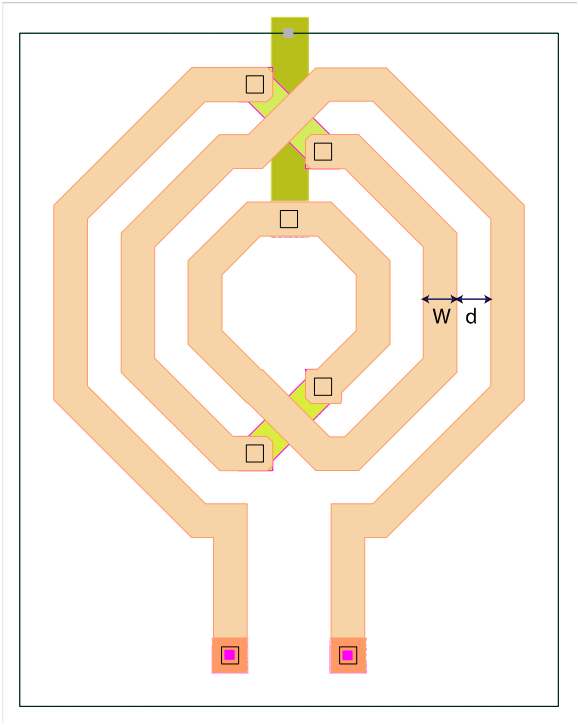


Figure 2.8: Octagonal differential inductor structure to be simulated using Agilent EEsof Momentum ($w = 20\mu m, d = 80\mu m$) .

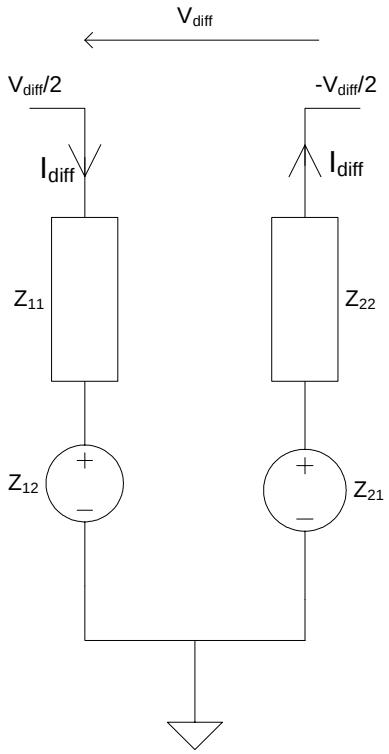


Figure 2.9: Differential inductor Z-parameter equivalent circuit.

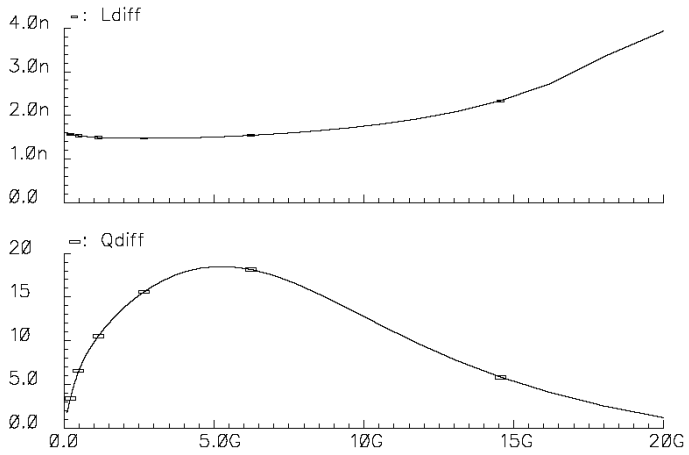


Figure 2.10: Simulated equivalent inductance and Q of a octagonal differential inductor.

$$Q_{diff} = \frac{\mathrm{Im}(Z_{diff})}{\mathrm{Re}\,(Z_{diff})} \tag{2.26}$$

$$L_{diff} = \frac{\mathrm{Im}(Z_{diff})}{\omega} \tag{2.27}$$

The above equations are used in Cadence to calculate the simulated differential inductance and quality factor (Figure 2.10). This 2-port S-parameter simulation uses the extracted 3-port S-parameter file from Agilent EEsof Momentum EM simulation with common mode connection grounded. The differential inductor saves chip area by roughly 50% while providing higher quality factor compared to single ended inductors.

2.4 CMOS Band Select Switches

The prototype negative $-G_m$VCO is designed to generate three different center frequencies at 4.8/6.4/8 GHz using a switched capacitor bank (Fig. 2.11). The VCO oscillates at its highest frequency of 8GHz with all switches turned off (branch with only varactors in the tank is connected). Additional capacitors are switched in by a two bit control code, shifting the VCO frequency to 6.4 or 4.8 GHz depending on the

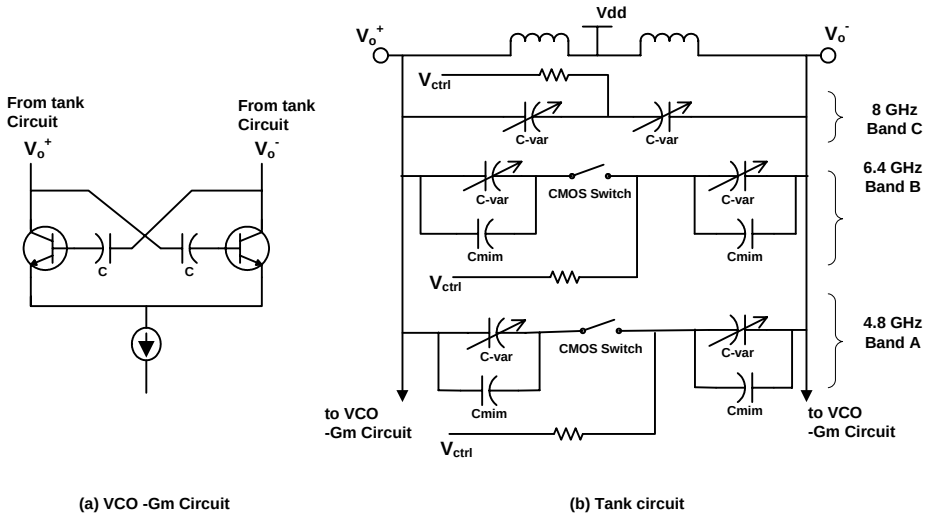


Figure 2.11: Simplified schematic of switched capacitor circuit. (a) Negative G_m circuit, (b) Switched tank circuit.

combination of capacitors selected.

The VCO output voltage swing tends to decrease when the additional capacitors are switched into the tank circuit, due to the additional loss associated with these components. In other words, the additional loss reduces the tank parallel resistance at the oscillation frequency. In this design, this effect is compensated by automatically switching to a higher bias current for the $-G_m$ circuit for the lower frequency bands where there is more tank loss. Note that the resonant tank Q will drop even if a capacitor bank with the same Q value is switched in to lower the resonant frequency (given a fixed L).

The capacitor states of the VCO are controlled by CMOS transmission gate switches (Fig. 2.12). The varactor control voltage V_{ctrl} is connected to the drain and source of the transmission gate simultaneously. When the switch is turned on, the VCO core circuit is symmetric along its center axis, which is equivalent to a differential ground and common-mode open. The large-signal RF voltage at the tank resonant frequency will swing across the capacitor pair and the transmission gate. The two resistors in series with the V_{ctrl} are designed to be larger than the transmission gate on-resistance such that minimal RF current leaks through this two path. During the positive half cycle of V_o^+, the RF current is from V_o^+ to V_o^-; during the negative half cycle of V_o^+,

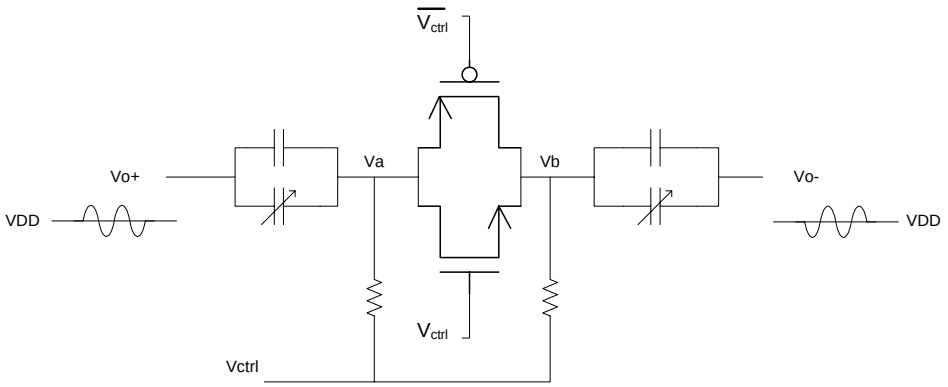


Figure 2.12: CMOS transmission gate analog switches for switched VCO.

the RF current is from V_o^- to V_o^+. The RF voltages at the drain (V_a) and source (V_b) of the transmission gate are opposite to each other and their absolute values depend on the product of transmission gate on-resistance and RF current:

$$V_a^{RF} = -V_b^{RF} = I_{RF} R_{on}/2 \tag{2.28}$$

$$I_{RF} = (V_o^+ - V_o^-)/Z_s \tag{2.29}$$

where R_{on} is the on resistance of the transmission gate and Z_s is the series differential impedance between V_o^+ to V_o^- due to tank capacitance, switch on-resistances and parasitics. The overall voltages at the drain/source nodes of the switch are then:

$$V_a = V_{ctrl} + I_{RF} R_{on}/2 \tag{2.30}$$

$$V_b = V_{ctrl} - I_{RF} R_{on}/2 \tag{2.31}$$

The drain and source voltages of the transistor have a direct impact on the transmission gate on-resistance. To reduce the loss of the tank circuit, the on-resistances of the transistors in the gate need to be as small as possible. This is generally realized by increasing the width of the transistor. However, this also increases the parasitic capacitances which may significantly shift the resonant frequency of the tank when the switch is off.

The transmission gate transistors should operate in the linear region to achieve small

on-resistance. While in the linear region ($V_{DS} \ll V_{GS} - V_{th}$) the on-resistance of the NMOS transistor in long channel region is given by:

$$R_{on\_N} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)} \tag{2.32}$$

in the switch on state. For the transmission gate NMOS transistor, the gate voltage is biased at the highest voltage V_{DD}. As the source voltage increases from zero, R_{on_N} increases until $V_{GS} = V_{th}$ where the transistor is cutoff. For the PMOS transistor, the scenario is opposite to NMOS case since the gate voltage of PMOS is biased at the lowest voltage V_{ss} (ground). As the source voltage of PMOS decreases from V_{dd}, its on-resistance R_{on_P} increases until it moves from linear to cutoff region. The on-resistance of the transmission gate pair is the parallel combination of the NMOS and PMOS on resistances. Assuming

$$k = \mu_n C_{ox} \frac{W_n}{L_n} \approx \mu_p C_{ox} \frac{W_p}{L_p} \ ,$$

$$\begin{aligned} R_{on} &= R_{on\_N} \parallel R_{on\_P} \\ &= \begin{cases} R_{on\_N} & V_s < |V_{thp}| \\ \frac{1}{k(V_{dd} - |V_{tn}| - |V_{tp}|)} & |V_{thp}| < V_s < V_{dd} - V_{thn} \\ R_{on\_P} & V_{dd} - V_{thn} < V_s \end{cases} \end{aligned} \tag{2.33}$$

where V_s is the source voltage of the transistors. From equation 2.33, it can be seen that the on-resistance of the transmission gate is symmetric about $V_S = V_{dd}/2$ assuming equal threshold voltage for both NMOS and PMOS transistors. The on-resistance curve R_{on} is near constant when both NMOS and PMOS are conducting based on the above assumptions (Fig. 2.13) and drops off towards the two supply rails.

However, for CMOS transistors, the threshold voltages of NMOS and PMOS devices are generally not the same; this causes the resistance curve to shift towards that of the device with the larger threshold voltage. An S-parameter simulation of a CMOS switch shows that the equivalent on-state differential resistance increases significantly as the varactor tuning voltage is increased above 1.1 V (Fig. 2.14). This increase in series switch resistance decreases the Q of the tank and reduces the equivalent

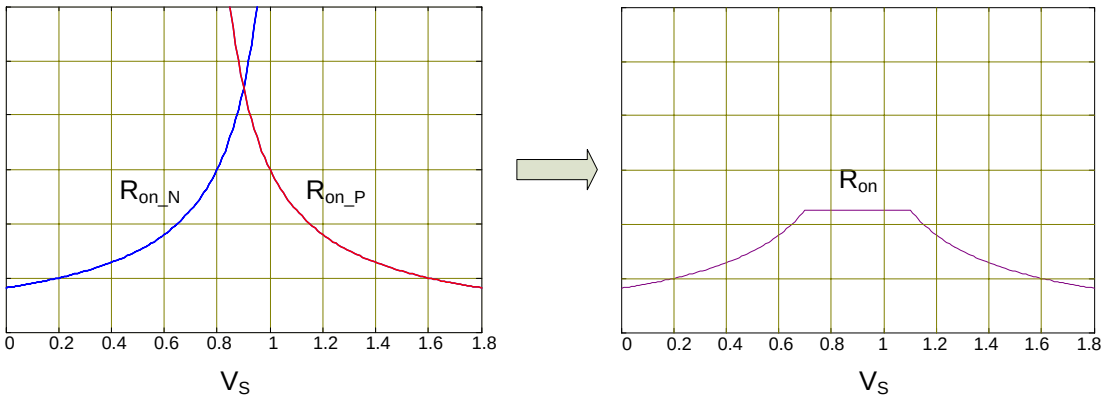


Figure 2.13: Conceptual diagram of on-state resistance variation of transmission gates (Y-axis is resistance value).

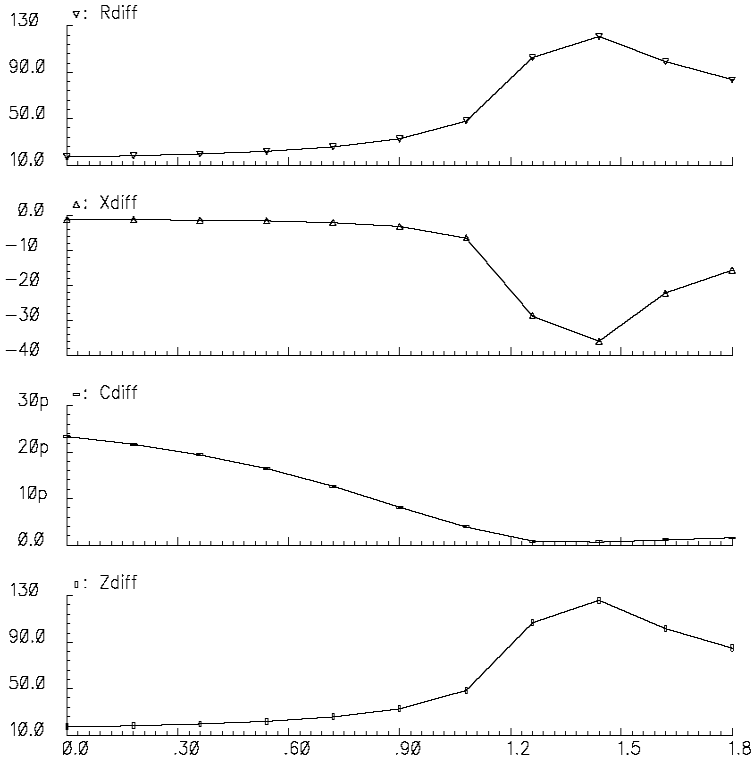


Figure 2.14: SpectreRF simulated equivalent resistance of an on-state CMOS switch vs. varactor tuning voltage (R_{diff}: differential resistance; X_{diff}: differential reactance; C_{diff}: differential capacitance; Z_{diff}: differential impedance).

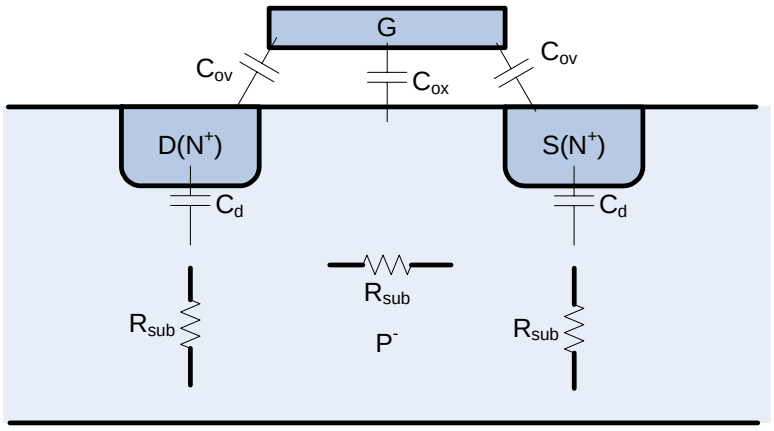


Figure 2.15: Parasitic capacitances of a NMOS switch in cutoff.

capacitance. The series R_s and C_s circuit can be converted to a parallel equivalent circuit [37]:

$$Q_s = \frac{1}{\omega R_s C_s} \tag{2.34}$$

$$R_p = R_s(1+Q_s^2) \tag{2.35}$$

$$C_p = \frac{Q_s^2}{1+Q_s^2} C_s \tag{2.36}$$

As series resistance increases, Q_s drops so that both the equivalent parallel resistor R_p and capacitor C_p decrease. The decrease of C_p increases the resonant frequency of the VCO, and therefore increases the VCO tuning range. The switch performance indicates that the VCO should be operated with varactor control voltages less than 1.1 V to avoid the excessive loss due to the switches.

In addition to the switch resistances, the CMOS switches also add extra parasitic capacitances to the tank circuit even when in the off state. This is especially problematic for high frequency VCO design since the oscillation frequency is quite sensitive to extra capacitance. The parasitic capacitances of the structure can be understood from Figure 2.15. As the gate voltage is reduced to ground, there are two parasitic paths between the drain and source: one through gate overlap capacitances; the other through drain/source to bulk diode capacitances in series with the bulk resistance. Modern CMOS process use low bulk resistivity ($20\Omega \cdot cm$ to $0.1\Omega \cdot cm$) to mitigate the digital latchup effect. Consequently the resistance between the drain/source to bulk

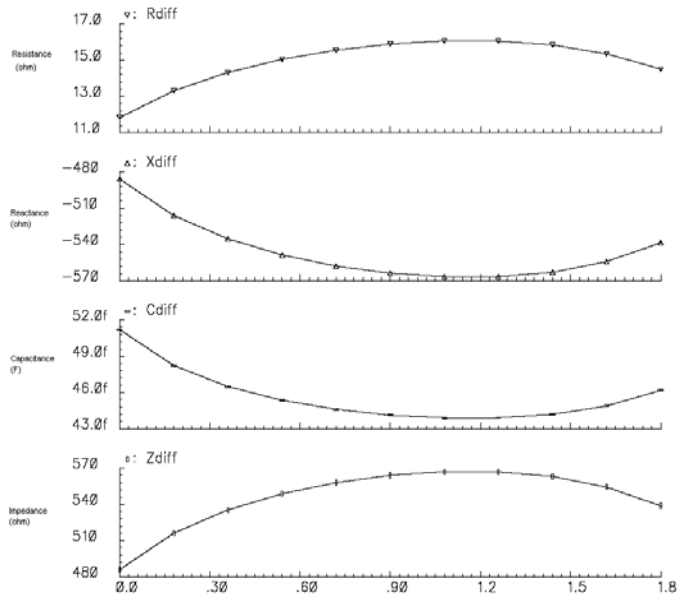


Figure 2.16: SpectreRF simulated equivalent capacitance of an off-state CMOS switch vs. varactor tuning voltage.

capacitance can be quite small, especially for shorter gate length devices. This additional capacitance limits the maximum size of the CMOS switches that can be used without causing the maximum VCO high band frequency to be reduced significantly. S-parameter simulation results with the CMOS switches off are shown in Figure 2.16. An equivalent differential capacitance about 50 fF (two 100 fF capacitances in series) is introduced by the CMOS switch (C_{diff} in Fig. 2.16).

The final designed VCO schematic with tank circuit is shown in Fig. 2.17. The SpectreRF simulations of the switched tank VCO of all three frequency bands are shown in Fig. 2.18. Table 2.1 summarizes the simulated results of the switched tank VCO. Phase noise simulation could not performed due to the custom inductor S-parameter results being in compatible with the Cadence Pnoise simulator.

Ultimately, the on-off performance of this CMOS switch design leaves much to be desired. As discussed above, this problem is caused mainly by the switch resistance dependence on varactor control voltage. One solution to this problem is to segregate the control voltage V_c from the switch DC path by adding two extra blocking capacitors C_b as shown in Figure 2.19.

	f_o (GHz)			Δf	I_{dc} (mA)
HighBand	7.4	7.9	8.3	1.1	3.16
MidBand	5.6	6.6	7.4	1.8	3.95
LowBand	4.2	4.7	6.2	2.0	6.1
$V_{tune}(V)$	0	0.9	1.8		-

Table 2.1: Switched tank VCO design simulated results

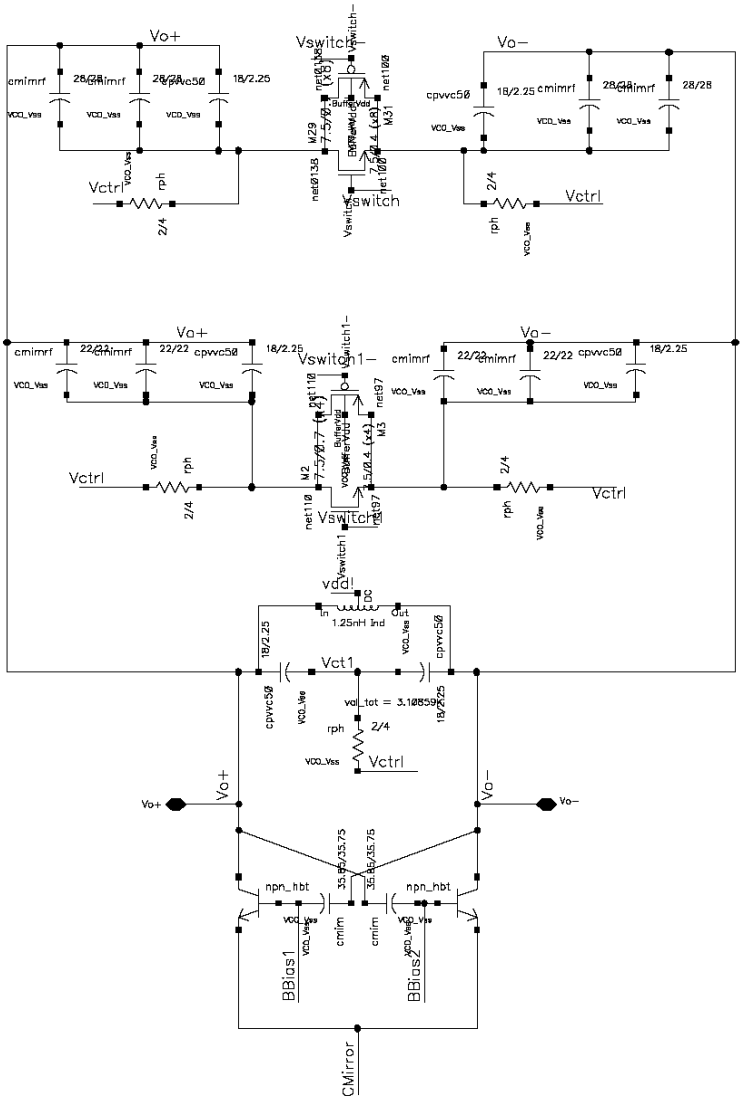


Figure 2.17: Complete Cadence schematic of the designed switched tank VCO circuit.

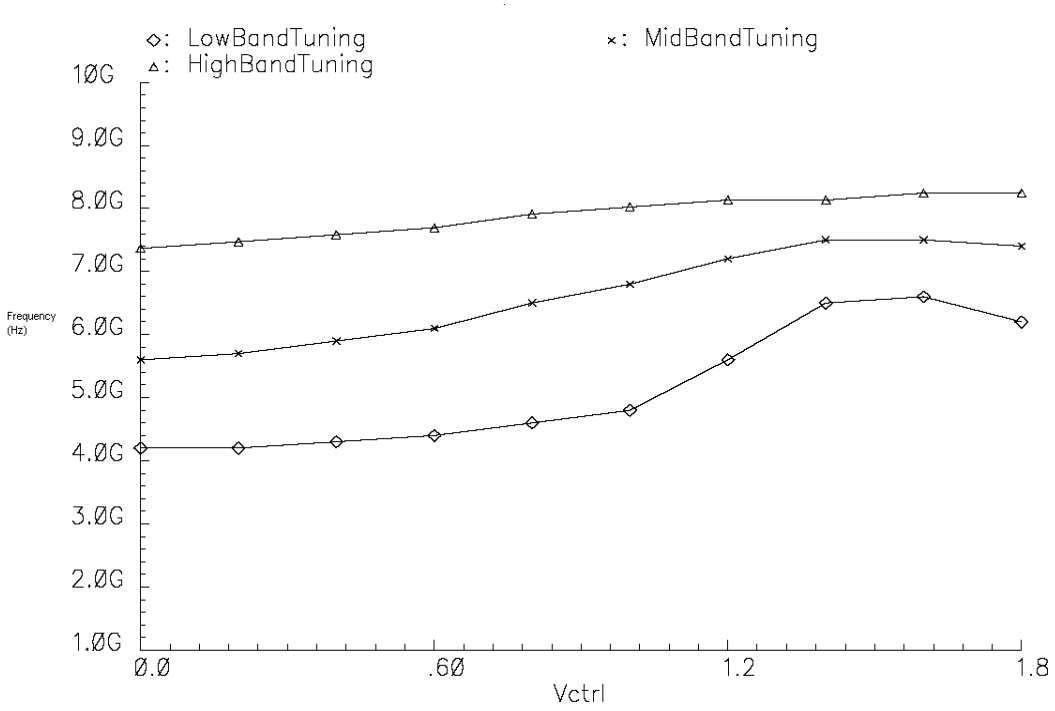


Figure 2.18: SpectreRF simulation of the switched tank VCO circuit (frequency range vs. tuning voltage in V).

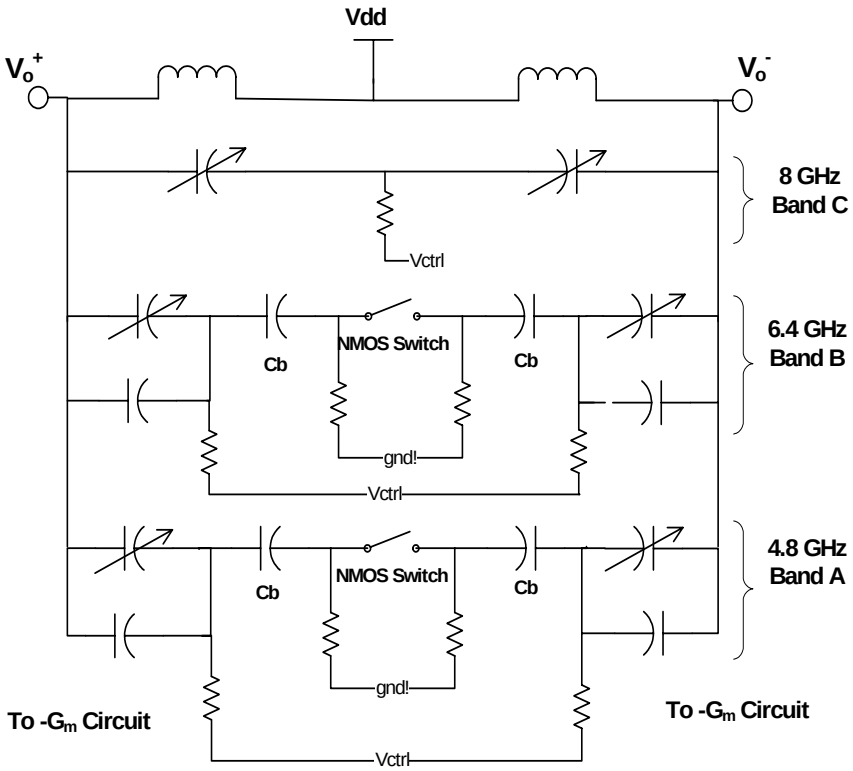


Figure 2.19: An alternative switched tank circuit structure which isolates varactor control voltage from the switched S/D terminals.

	f_o (GHz)			Δf (GHz)	I_{dc} (mA)
$V_{tune}(V)$	0	0.9	1.8		
HighBand	7.8	8.4	8.8	1.0	1.6
MidBand	6.3	6.8	7.2	0.9	4.25
LowBand	4.5	4.9	5.2	0.7	5.8

Table 2.2: Improved switched tank VCO simulated results

In this topology, only NMOS switches are needed since their drain/source nodes are grounded at DC through the large resistors. As the switch is turned on, its gate voltage is 1.8V and since its source voltage is kept close to ground (with only small AC variation), it operates at its deep triode region with small on-resistance. Due to the higher electron mobility, NMOS-only switches can provide smaller switching resistance due to their higher channel mobility while keeping the parasitic capacitances small enough not to affect the high band oscillation frequency. In addition, the noise introduced by the NMOS switch will appear as correlated common mode noise at the differential VCO output, and will not contribute to the differential noise performance. Another advantage of using single NMOS is that the equivalent single ended resistance of is only half of the total resistance due to virtual ground at the center of the device.

The schematic of the improved switched tank VCO circuits is shown Fig. 2.20, and the simulated results in shown in Fig. 2.21. As can be seen, the switching of the each band is quite linear due to the NMOS only switches. Table 2.2 summarizes the simulated results of the improved switched tank VCO. However, due to time limitations for completing the HIP6WRF design tapeout, this switch design modification was not incorporated into the fabricated designs.

2.5 Summary

This chapter has covered the design and simulation of SiGe BiCMOS switched-tank VCO design for the proposed multiband UWB transmitter. To achieve a wide overall tuning range, a switched capacitor tank controlled by CMOS switches was designed. The nonlinearity of the CMOS switches caused by the varactor tuning voltage are discussed and an alternative structure which is not sensitive to the tuning voltage

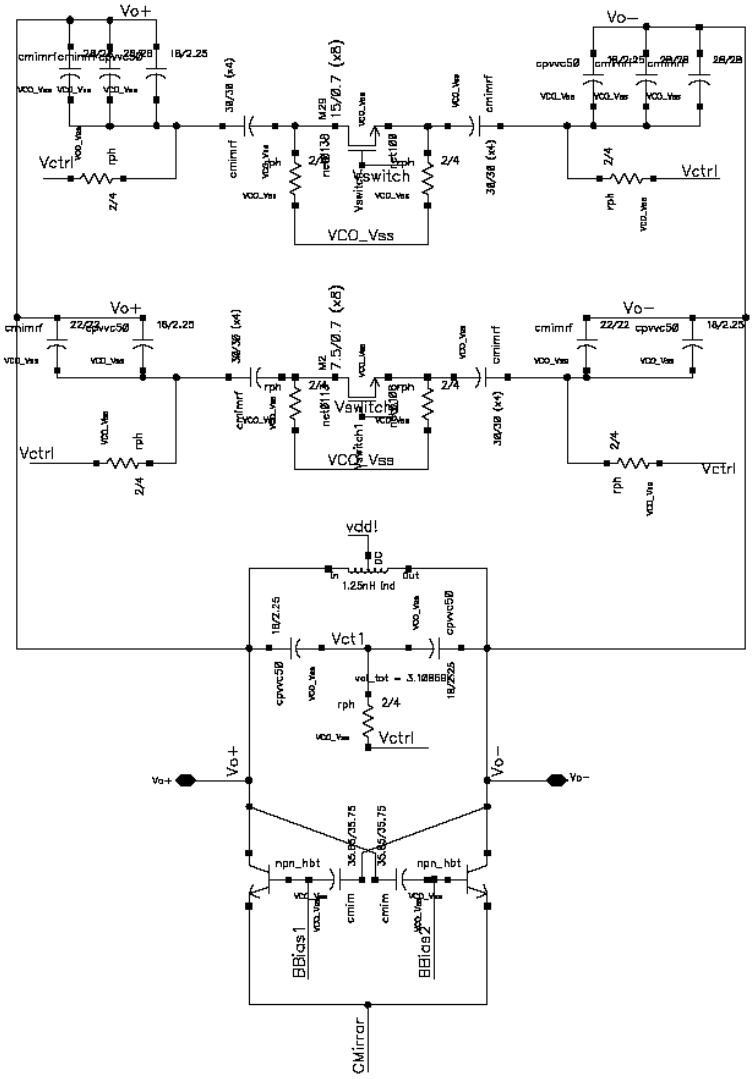


Figure 2.20: Schematic of the improved switched tank VCO circuit.

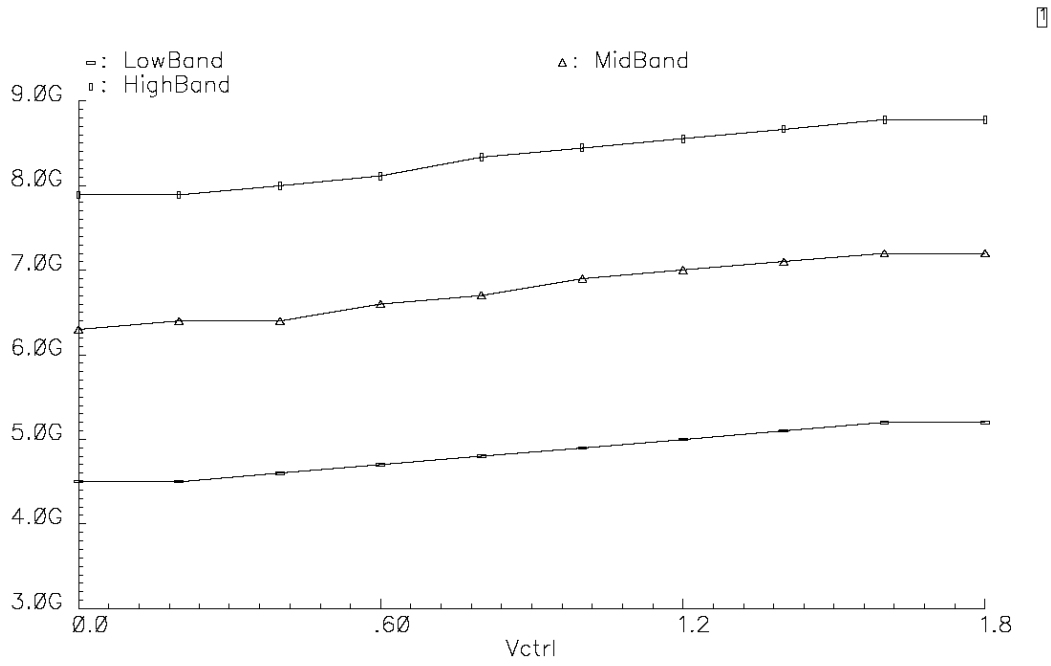


Figure 2.21: SpectreRF simulation of the improved switched tank VCO.

is proposed. The main contribution of the work in this chapter is the design of an adjustable frequency tuning VCO over wide frequency range from 4 GHz to 8 GHz, analysis of the nonlinear switching issues, and the proposed design of a new switched tank VCO with separate AC/DC paths to avoid nonlinear switching issues. With the improved switched tank VCO design, a wide frequency operation and adjustable tuning range can be achieved in future designs.

Chapter 3

SiGe BiCMOS Multi-band UWB transmitter Design

As introduced in Chapter One, a prototype Ultra-Wideband transmitter is designed to operate over three 500 MHz frequency bands centered at 4.8/6.0/8.0 GHz [38]. The transmitter design consists of a fast multiband Phase Locked Loop and a differential wideband pulse generation unit (Fig. 3.1). Baseband modulated digital input bit streams are fed directly to the pulse modulator for transmission. The biphase modulation is obtained by selecting one of the differential outputs from the VCO. The UWB transmitter design is implemented using Freescale's HIP6WRF $0.18\mu m$ BiCMOS process.

The internal charge pump PLL is designed to have a wide bandwidth and a fast lock time ($0.7\mu s$), such that the transmitter can hop over different carrier frequency bands and retransmit without significant delay. An external input signal of 100 MHz is used as the reference for the system. The phase detector compares the reference at 100 MHz with the divided VCO output and generates an error signal. This error signal is then processed, filtered and converted to a voltage control signal by the charge pump and on-chip loop filter. The wideband PLL design also benefits from small on-chip loop filter capacitors, therefore reducing the overall chip size and cost. A two-bit frequency selection code is sent to both the switched capacitor tank VCO and the variable gain divider simultaneously. After receiving the control command, both VCO and divider will switch to the appropriate band/ratio of operation. Each time

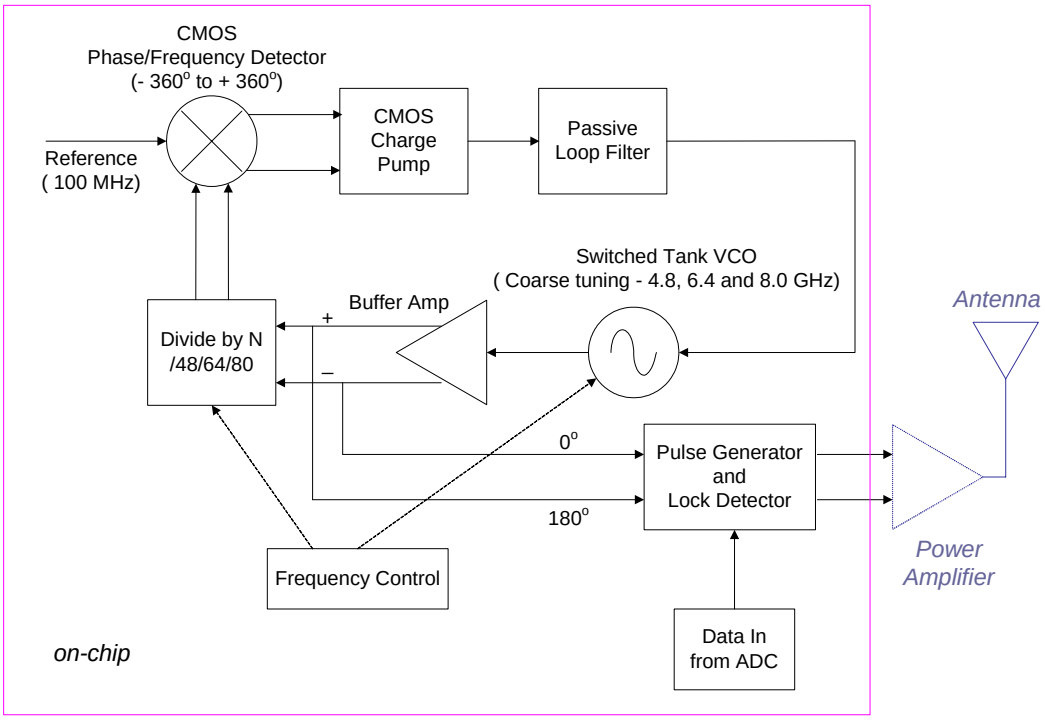


Figure 3.1: Proposed SiGe UWB transmitter architecture.

the transmitter switches frequency bands, the PLL will switch from locked state to acquisition state and then regain lock. Since no information should be transmitted during the nonlinear acquisition phase, a lock detector is integrated to ensure that the system is in stable condition before any transmission. The pulse generator is implemented by a combination of digital logic and delay lines to generate the intended $4ns$ gating pulses.

In PLL design there is a well known trade-off between the loop bandwidth, tracking and jitter [39]: a large loop bandwidth can minimize the phase noise of the internal VCO and achieve the best tracking properties; on the other hand, a small loop bandwidth will minimize the jitter due to the external noise from the charge pump and loop filter. Excessive jitter or phase noise may cause receiver synchronization problems and data errors. In [40], the authors proposed a low jitter PLL operating at 2.4 GHz with a bandwidth of 2 MHz fabricated on $0.12\mu m$ CMOS. In [41], another PLL with a loop bandwidth of 26 MHz and loop settling time of less than 100ns was proposed for UWB OFDM applications.

The initial prototype PLL in this project was designed for a bandwidth of 4 MHz and settling time of 700ns over wide tuning frequencies. It is challenging to keep the PLL performance stable while fast hopping over a wide frequency range. For the highest frequency band, it is important to reduce the circuit sensitivity to parasitics; while for the lowest frequency band, it is important to compensate for the extra tank loss while not contributing additional parasitics in the higher band states.

3.1 Basic Theory of Phase Locked Loops

The Phase Locked Loop (PLL) is a fundamental building block in many modern communication systems. PLLs are widely used in various wireless applications such as FM detection, frequency synthesis, bit synchronization and data detection. A phase-locked loop is fundamentally a nonlinear feedback control system which can be used to control the phase/frequency of the local oscillator. A PLL can synchronize the phase of a VCO to a very stable input reference source, such that the locked VCO is much more stable compared to the free-running VCO. An important feature of PLLs is that they can be configured to provide filtering of noise from either the reference input or the VCO depending on its bandwidth. The noise from the VCO is high-pass filtered, while the noise from the reference path is low-pass filtered. If a PLL has a narrow band loop filter, it tracks the average frequency of the input signal thereby reducing the noise from the reference input; if the bandwidth of the loop filter is wider, then PLL will track the instantaneous input frequency thereby reducing the contribution of the VCO noise.

A basic PLL consists of a phase detector, a loop filter and a voltage-controlled oscillator. The function of the phase detector is to capture the phase difference between the reference source and the VCO output signal. By comparing the phase of the reference source with the VCO, PLL generates an error signal that in turn controls the internal VCO frequency so that it will maintain a constant phase with respect to the reference source. The loop filter is used to remove the unwanted frequency components and adjust the tracking characteristic of the PLL. A frequency synthesizer is a more sophisticated version of a PLL which is designed to provide multiple output frequencies at very specific channel spacings (Fig. 3.2). Such a frequency synthesizer compares the reference frequency divided by M to the VCO frequency divided by N

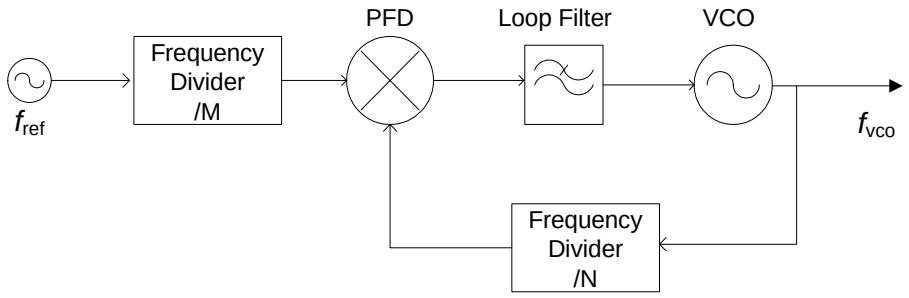


Figure 3.2: A simplified diagram of a frequency synthesizer.

[42]. The resulting output frequency is controlled by the divider ratio N/M:

$$f_{vco} = \frac{N}{M} f_{ref} \tag{3.1}$$

A PLL can be analyzed by using a s-domain mathematical model (Fig. 3.3) [43]. In this model, the phase error φ_e is calculated by subtracting the input phase φ_{in} from the output phase φ_{out}. K_P is the gain of the phase detector in V/rad, K_{LF} is the gain of the loop filter in V/V, $F(s)$ is the filter function, K_V is the gain of the VCO in Hz/V, $u_1(s)$ is the phase detector output and $u_2(s)$ is the loop filter output. The integration term $1/s$ arises because the phase detector of the loop compares the phase (instead of frequency) of the VCO with the phase of the input reference.

If $\varphi_{in} > \varphi_{out}$, we can find that $\varphi_e > 0$, $u_1 > 0$ and $u_2 > 0$. Then, φ_{out} will increase as the VCO frequency increases. As a result, the phase of the VCO output signal will gradually catch the phase of the reference source. On the other hand, if $\varphi_{in} < \varphi_{out}$, the VCO frequency will slow down to meet the reference source. Since the frequency error is the derivative of the phase error, the PLL will respond to a frequency deviation by adjusting the VCO to be in synchronism with the reference source.

The open-loop transfer function $G(s)$ of the basic PLL shown in Fig. 3.3 can be expressed as:

$$G(s) = \frac{K_P \cdot K_{LF} F(s) \cdot K_V}{s} = \frac{KF(s)}{s} \tag{3.2}$$

where K is the open loop gain of the PLL in Hz/rad. The close loop transfer function of the PLL is $H(s)$:

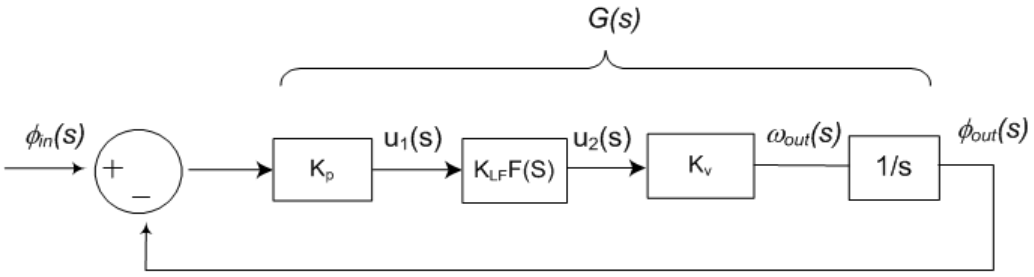


Figure 3.3: A linear mathematical control system model of PLL.

$$\frac{\varphi_{out}(s)}{\varphi_{in}(s)} = H(s) = \frac{G(s)}{1+G(s)} \tag{3.3}$$

In case of a frequency synthesizer, where a divider (variable ratio N) stage is inserted after the VCO, the VCO frequency is controlled by adjusting the divider ratio while keeping the reference frequency fixed. The closed loop transfer function $H(s)$ at the divider output is therefore given by:

$$H_1(s) = \frac{G(s)D(s)}{1+G(s)D(s)} = \frac{\frac{G(s)}{N}}{1+\frac{G(s)}{N}} \tag{3.4}$$

and the closed loop transfer function $H_1(s)$ at the VCO output is

$$H(s) = \frac{G(s)}{1+\frac{G(s)}{N}} \tag{3.5}$$

In a phase locked loop, noise is potentially generated within each loop component. The noise contribution to the output of the PLL due to each component depends on the closed loop transfer function at the point of noise injected. The total phase noise at the output of the PLL can be calculated as (assuming all noise sources are

uncorrelated) [44]:

$$\begin{aligned} |\overline{n_{PLL}}|^2 &= N^2 |H_1(s)|^2 |\overline{n_{ref}}|^2 + \frac{N^2 |H_1(s)|^2}{K_p^2} |\overline{n_{\det}}|^2 + \frac{N^2 |H_1(s)|^2}{K_p^2 |F(s)|^2} |\overline{n_{filter}}|^2 \\ &\quad +(1 - |H_1(s)|^2) |\overline{n_{VCO}}|^2 + N^2 |H_1(s)|^2 |\overline{n_{\mathrm{div}}}|^2 \end{aligned} \tag{3.6}$$

Since the closed loop function $H_1(s)$ has a low-pass frequency response, the VCO noise experiences high pass filtering $(1 - |H_1(s)|^2)$ while the rest of the loop noise components experience low pass filtering $(|H_1(s)|^2)$.

There are two terms generally used to classify different PLLs: the *order* is determined by the number of poles in the open-loop transfer function $G(s)$; the *type* is determined by the number of poles at the origin [43][44]. A first order PLL has only one parameter: its gain. The bandwidth of a first order PLL is proportional to its gain. First order PLLs are not frequently used since any practical VCO has limited bandwidth. A second order PLL uses either passive or active loop filters, and both their gain and bandwidth can be controlled separately. Second order PLLs are widely used in practice.

There are three tuning ranges commonly used to describe PLL operation: seize range Ω_S, pull-in range Ω_{PI} and hold-in range Ω_{HI} (Fig. 3.4). Within the range Ω_S, the PLL is able to lock to the input frequency within one cycle; within Ω_{PI}, the PLL will eventually achieve lock, but may take several cycles; within Ω_{HI}, the PLL is able to maintain lock but not necessarily acquire lock.

Lock-in time is an important parameter describing how fast the PLL can achieve lock after the loop is closed. A number of fast lock techniques have been proposed recently. In [45], an on-chip passive discrete loop filter is used instead of an RC loop filter. By removing an integrator from the feedback loop, the PLL achieves fast lock time of $\sim 30\mu s$. Another technique is to implement two sets of loop parameters [46], which are used to coarse and fine tune the PLL respectively. The PLL settling time can be improved by using a wider bandwidth to achieve lock, and then switching to the smaller bandwidth to maintain lock. In [47], a feed forward technique implemented on a DSP chip is used to pretune the VCO to the desired the frequency. Then the regular PLL takes the frequency to lock. In case of the prototype design in this work, a wideband charge pump PLL is used to achieve fast lock (on the order of a few ns).

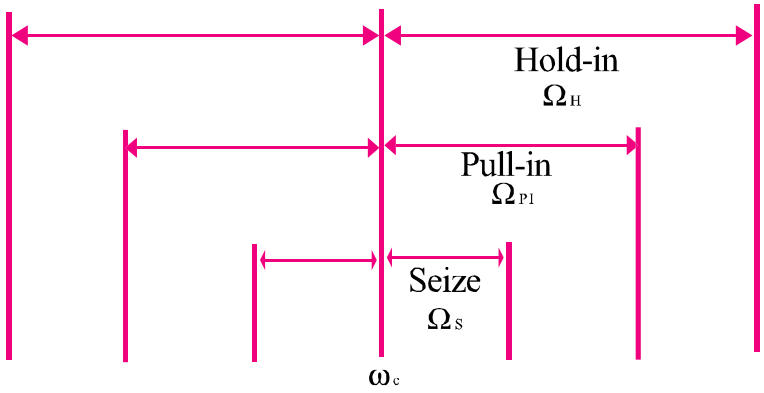


Figure 3.4: Three PLL tuning ranges.

3.2 Phase Detectors

A phase detector in a PLL generates a phase error output by comparing a reference input phase (normally a temperature stable, low jitter source such as a crystal oscillator) and the output phase of a VCO. Types of phase detectors include multiplier, exclusive-or gate, and phase frequency detector (PFD) [43]. On the other hand, the PLL in this work uses a PFD for its ability to track phase and frequency simultaneously.

A phase frequency detector generates either an up or a down output signal depending on the relative phase between the reference and the VCO output. If the reference input is leading the VCO output, then an up pulse is generated, and vice versa. The actual phase error information is embedded in the duration of the PFD output pulses. The PFD output is first converted to a current signal through a charge pump circuit (Fig. 3.5). Then a trans-resistance low pass filter following the charge pump converts the current signal to a voltage control signal for the VCO while filtering out unwanted frequency components. By generating both up and down outputs, a PFD is able to track a wider phase error range than other techniques mentioned — from $\{-2\pi,\ 2\pi\}$ — while tracking frequency simultaneously (Fig. 3.6).

The phase frequency detector in the prototype PLL here is constructed using two D flip-flops and an AND gate [Fig. 3.7(a)]. The reference frequency input and the VCO frequency input to the PFD are delivered to the clock input of each D register

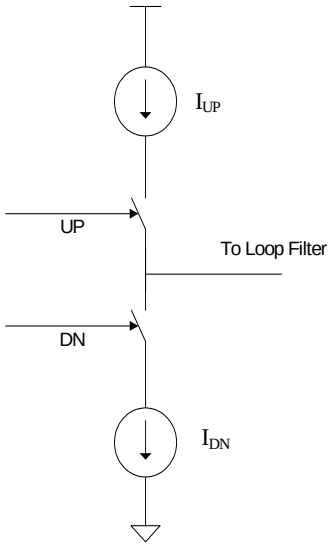


Figure 3.5: A simplified diagram of a charge pump circuit.

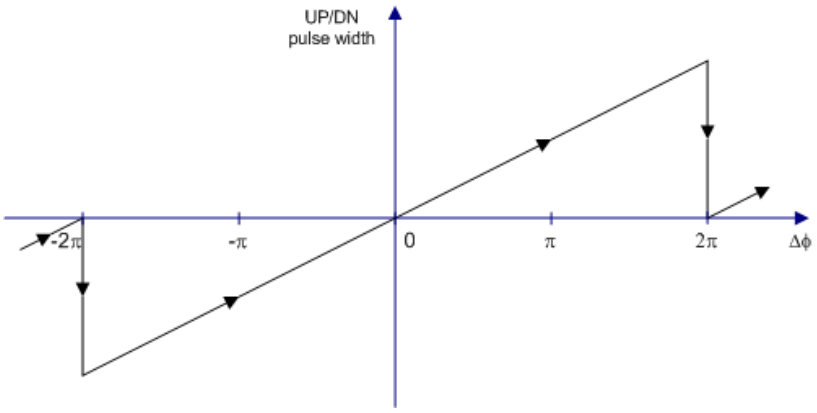


Figure 3.6: A phase frequency detector output vs. phase error.

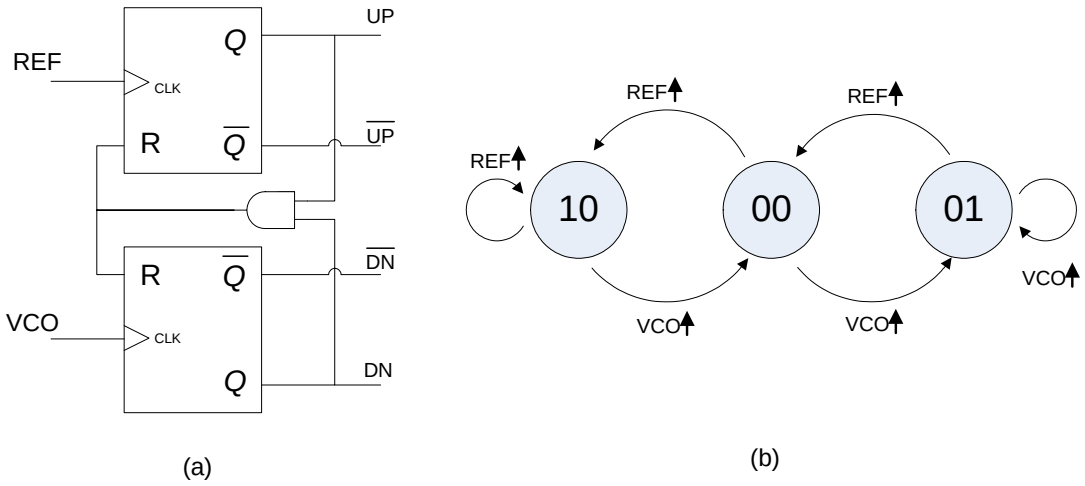


Figure 3.7: Phase frequency detector (a) schematic and (b) state transition diagram.

respectively. The PFD operation can be analyzed using a two bit state diagram with each bit representing the current state of a register. A pair of complementary outputs $UP/\overline{UP}$ and $DN/\overline{DN}$ are read out from the two D registers and are used as control signals for the charge pump switch. Each time there is a rising edge of clock at a D register, the state of the PFD will be re-configured as described by the state diagram in 3.7(b).

Theoretically, there can be only three states (00, 01, 10) since the (11) state will immediately reset both D registers. However in reality, due to delays through the digital logic, a 11 state can exist for a very short period of time. The time duration for a (11) stage ensures that the charge pump will be turned on briefly even a the system is in lock; this helps to remove the dead zone of the PFD [39]. At every rising edge of the reference input, the current state will shift one state to the left [Fig. 3.7(b)]. On the other hand, at every rising edge of the VCO input the current state will shift one state to the right [48]. If the reference input is leading the VCO input, an UP pulse will be created with its width proportional to the phase difference while the DN pulse remains low, and vice versa when the reference input is lagging the VCO input.

The phase frequency detector is capable of detecting both phase and frequency offset from the reference input. Figure 3.8 shows a particular case where the reference is at a lower frequency, but leads the VCO in phase. Initially, the PFD generates UP pulses,

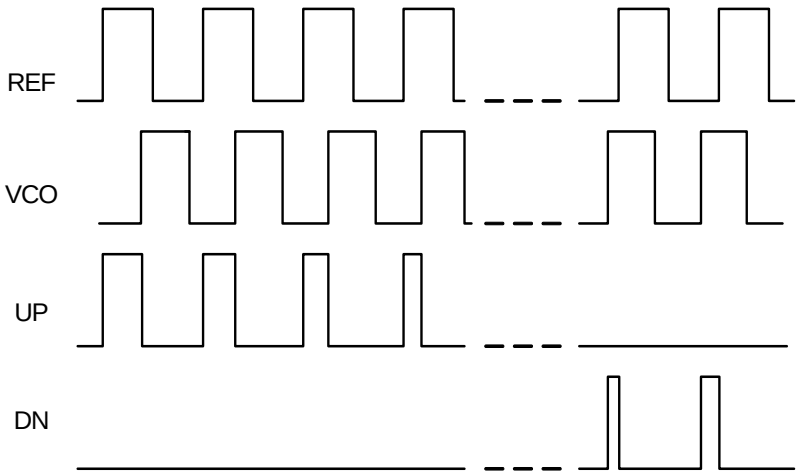


Figure 3.8: PFD can track the frequency as well as phase error.

which speeds up the VCO frequency and increases the frequency offset. However, after several cycles, the VCO phase catches up and starts to lead the reference. After that, the PFD generates DN pulses to slow down the VCO frequency. Eventually both the phase and frequency differences between the reference and VCO reduce to zero and the PLL achieves a locked state.

The flip-flop used in the PFD in this work is a modified version of a True Single Phase Clock (TSPC) flip-flop (Fig. 3.9) [49]. It uses fewer transistors and therefore has a faster response time, which makes it a good candidate for high frequency phase detection. This flip-flop is positive level triggered by the clock input CLK. The reset input R becomes logic high when both UP and DN go high, and transistor N1 is turned on establishing the voltage at the gate of $P3/N3$ high. $\bar{Q}$ goes high which in turn forces output Q to be low, therefore resetting the flip-flop. When the reset R is logic low, transistor $P2$ is on and $M1$ is off. A rising edge of CLK will set Q to be high by first charging the gate of $P3/N3$ to logic high and then turning on $N2$ to discharge $\overline{Q}$ to logic low. A falling edge of CLK after reset will not change the output Q.

When the PLL is in lock, the PFD will continually generate very short UP and DN pulses due to mismatches in the charge pump. This results in spikes in the VCO tuning voltage at the same frequency as the reference input, which in turn generates spurs at the PLL output by frequency modulating the VCO. The spurs will be at

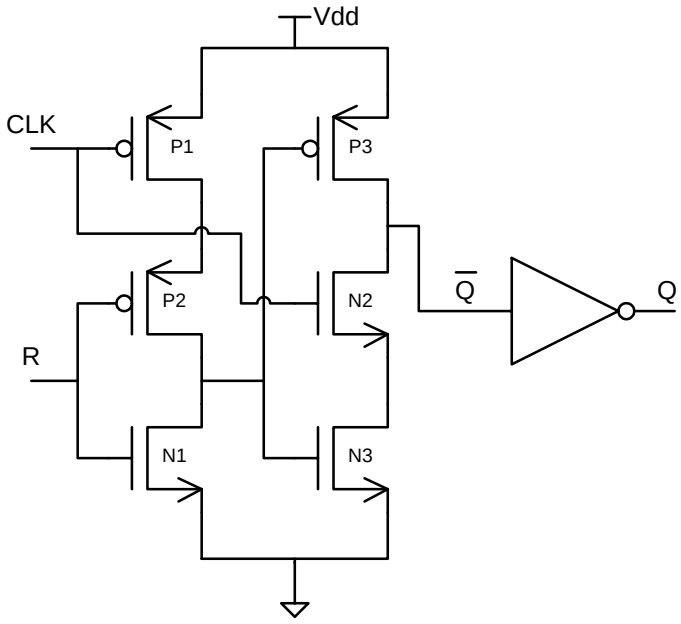


Figure 3.9: A modified TSPC flipflop for PFD.

multiples of the reference frequency on either side of the VCO output frequency.

3.3 Charge pump

A charge pump is a device which converts voltage inputs from the PFD to current output pulses. Since the PFD output is either an up or a down signal depending on the phase error information, the charge pump sources/sinks current to/from the trans-resistance loop filter with timing control related to the phase error (Fig. 3.10). The switches in the charge pump circuit need to have fast response time and good sensitivity to the UP/DN pulses from the PFD, since excess delays during the on/off instant may result in unwanted extra current flow or no current flow at all (for very short control pulses from PFD).

One method of implementing a charge pump circuit is to insert switches below/above UP/DN current sources to turn on/off either UP or DN current; however this tends to reduces the voltage swing headroom and introduces additional parasitics. Alternatively a charge pump circuit design with wide swing current sources [50] is adopted

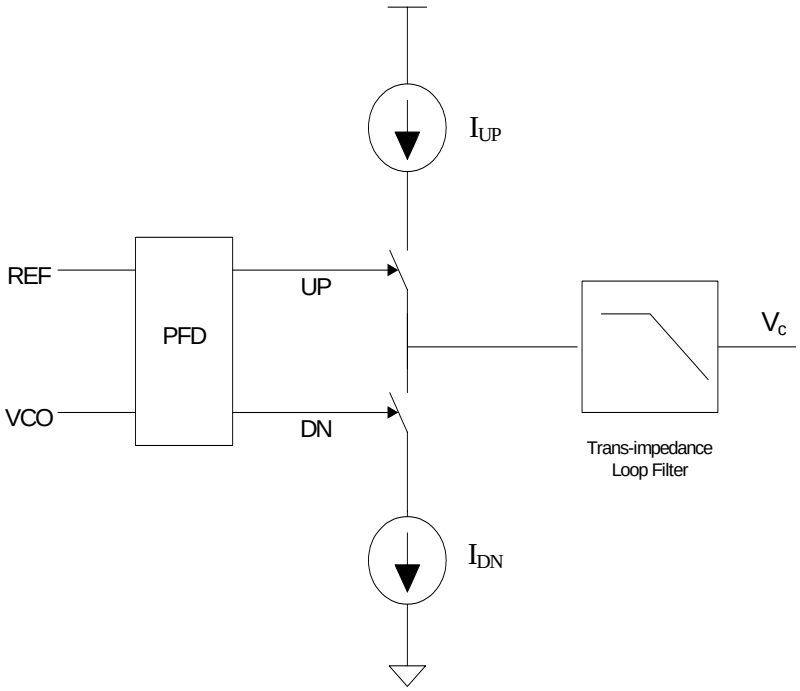


Figure 3.10: A simplified diagram of phase detector, charge pump and loop filter converting phase error to a control voltage.

in this work. As shown in Fig. 3.11, this charge pump has a pull-up half and a pull-down half using PMOS and NMOS current mirrors. The transistors in the pull-up half are denoted as $N_{up}(P_{up})$, while the ones in the pull-down half are denoted as $N_{dn}(P_{dn})$. When an UP pulse is presented to the input of the charge pump, the up current source I_1 is connected to I_{out} while the down current source I_2 is bypassed to ground. The opposite happens when a DN pulse is presented at the input. A pair of current sources I_{1a} and I_{2a} are employed to aid the speed of the transition. These sources have lower current values than I_1 and I_2. For example, for the pull-up half, the current mirror circuit including I_{1b}, $P3_{up}$ and $P4_{up}$ pulls up the gate voltage of $P1_{up}$ and $P2_{up}$ when the control is switched from UP to DN. As the charge pump switches from up to down, $N2_{up}$ is turned off immediately and leaves the gates of $P1_{up}$ and $P2_{up}$ floating if the pull-up mirror circuit is not used. The residual voltage at the gate of $P2_{up}$ will slow down, shutting off the pull up current. By connecting current output $P3_{up}$ to the gates of $P1_{up}$ and $P2_{up}$, the gate voltage of $P2_{up}$ is pulled up promptly after the switching, therefore shutting down the pull up current rapidly. The pull-down half operates in a similar manner, with $NMOS$ current sources instead of $PMOS$ current sources as the only exception.

Transistor-level simulation results of the PFD and charge pump circuit using Cadence SpectreRF are shown in Fig. 3.12. To show the phase and frequency tracking capability, the VCO output is intentionally set to a higher frequency than the reference with initial phase lag relative to the reference input. Initially, the phase and frequency of VCO undergo separate direction shifts with respect to the reference: phase error is getting smaller while frequency error is getting larger. As expected, the PFD initially finds the VCO phase is lagging the reference input, so it sends out UP pulses corresponding the delay time (phase error). The UP pulses turn on the charging current which increases the VCO control voltage V_c. The UP pulses become shorter by each pulse as the VCO output catches up, while VCO frequency becomes even higher than the reference. After about 7 cycles, the VCO output leads the reference input; this turns on the DN pulses, which starts to discharge the loop filter, reducing the VCO control voltage V_c. From this point on, both VCO frequency and phase are converging to the reference simultaneously.

Note that there are very short pulses of the UP/DN signal even if the phase error is almost zero. This is due to the finite delay time of the PFD resetting circuitry.

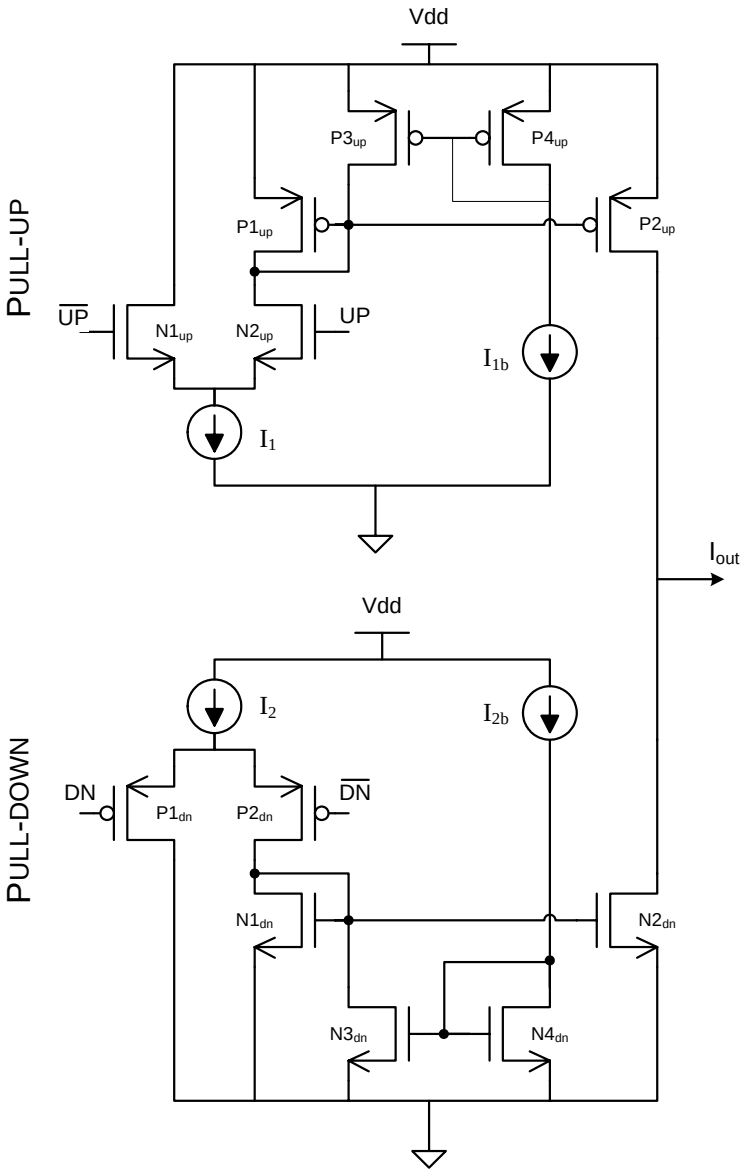


Figure 3.11: A charge pump consists of a pull-up and a pull-down current sources controlled by the PFD output.

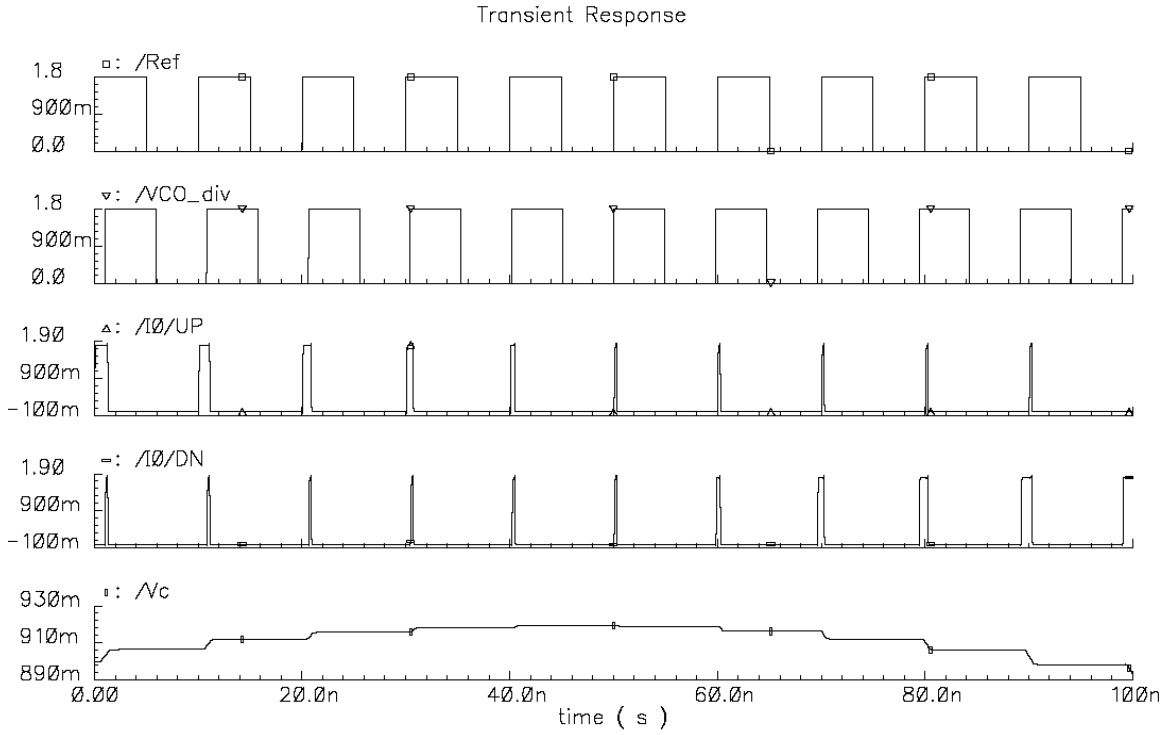


Figure 3.12: Simulation results of the PFD and charge pump circuit.

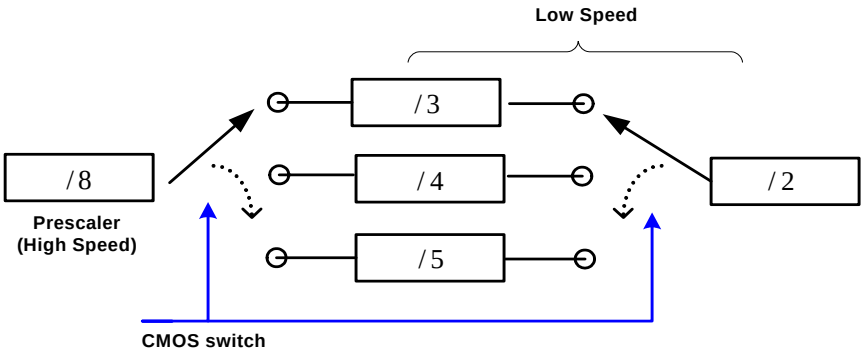


Figure 3.13: Simplified diagram of a variable (48/64/80) frequency divider.

However, these finite delay times ensure that both flip-flops in the PFD reset correctly. The finite delay also turns on the charge pump switches even when both inputs to the PFD are perfectly in phase, which removes the dead zone from the PFD response curve [39][51].

3.4 Prescaler and Variable Frequency Dividers

As discussed above, the prototype PLL is designed to switch between three frequency bands 4.8/6.4/8.0 GHz as controlled by a two bit code. Since the reference frequency is selected to be 100 MHz, the three frequency bands need to be divided down to the proximity of this value. This is done through a variable frequency divider with the dividing ratios of 48/64/80. The variable divider consists of a high speed divide-by-8 prescaler and a low speed variable divide-by-6/8/10 divider (Fig. 3.13).

3.4.1 High Frequency Divider

The high frequency divide-by-8 prescaler consists of three identical divide-by-2 Master-Slave Flip-flop stages (Fig. 3.14). Each D flip-flop inside the divider is designed using modified source coupled logic (SCL) [52]. In the modified SCL structure, the current source is removed and an external control bias voltage V_{bias} is added and applied to the gates of the PMOS pair (Fig. 3.15). Therefore, the current flow into the D flip-flop can be controlled during the measurement and the prescaler speed can be

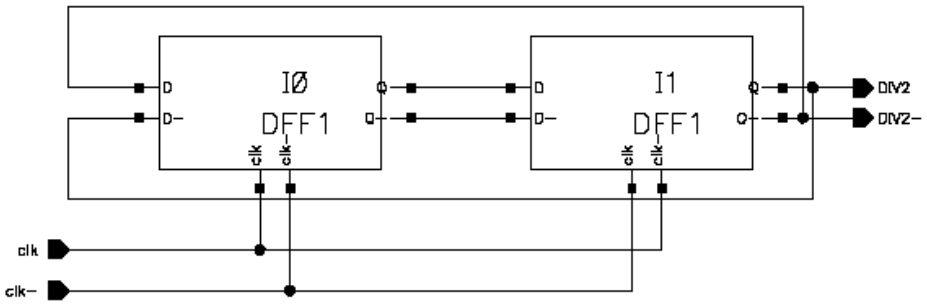


Figure 3.14: A divide-by-2 high speed prescaler. The divide-by-8 prescaler is composed of 3 identical versions of this stage.

adjusted. When CLK is high, the differential pair $M3/M4$ takes the input D; as the CLK goes low, the data input D is then stored in the cross coupled latch $M5/M6$.

The PMOS devices $M7/M8$ basically act as voltage controlled resistors for adjusting the time constant that determines the switching speed. $M7/M8$ operate in triode region, with an on-resistance given by (long channel approximation):

$$R_{M7} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)} \tag{3.7}$$

The capacitance at the node $\overline{Q}$ is a parallel combination of drain gate capacitances:

$$C_{M7} = C_{d7} \parallel C_{d3} \parallel C_{d5} \parallel C_{g6} \tag{3.8}$$

The resulting time constant is $\tau = R_{M7} \cdot C_{M7}$. By reducing the gate control voltage of $M7$, the time constant of the D flip-flop is reduced, enabling it to operate at a higher speed. The downside of this approach is additional current consumption through the devices. On the other hand, since the current source is removed from the source of the clocking transistor pair, the output swing range is increased.

A simulation result for a single Master-Slave stage divide-by-2 prescaler with an input frequency of 8 GHz is shown in Figure 3.16. The simulated maximum operating speed for the D flip-flop is at least $12GHz$ (Fig. 3.17) which is sufficient for the frequencies of interest in this work. A Cadence Periodic Steady State simulation shows that the divider is capable of outputting up to 6 GHz with an input frequency of 12 GHz.

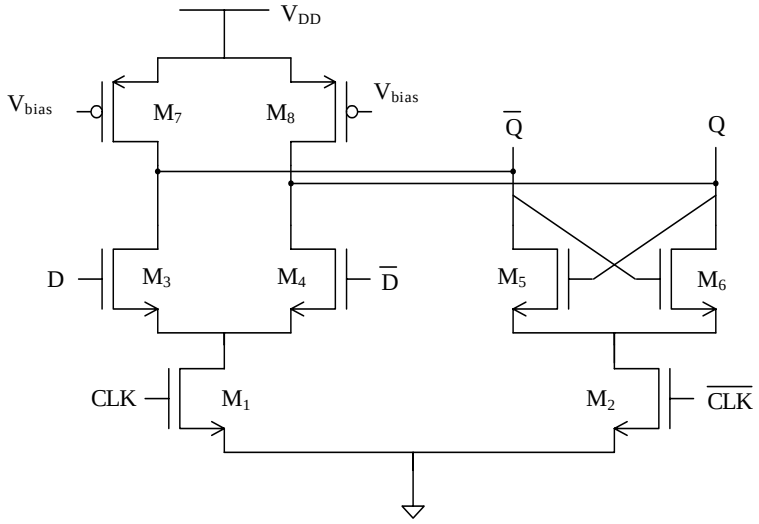


Figure 3.15: Modified source coupled logic D flip-flop.

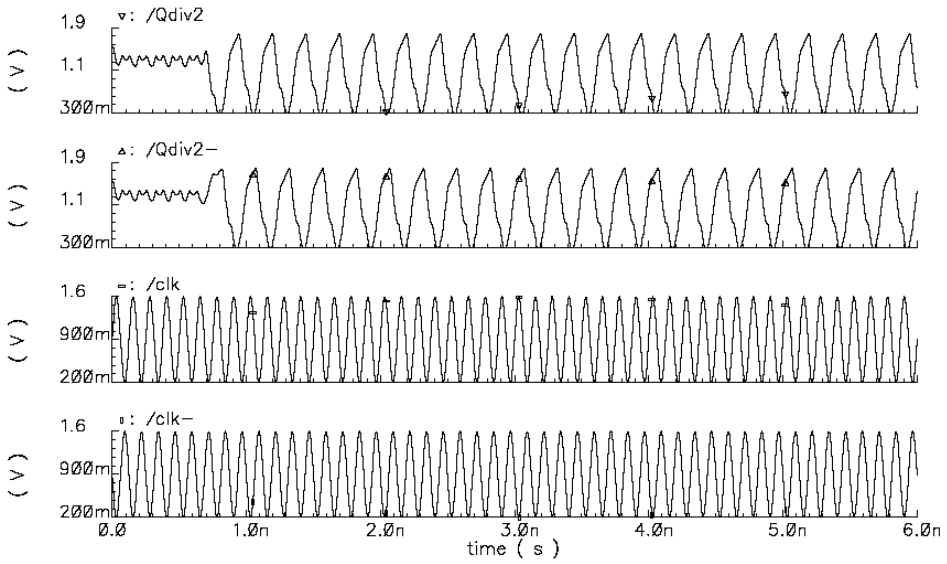


Figure 3.16: SpectreRF simulation results of a high speed prescaler (first divide-by-2 stage) with an 8 GHz input clock.

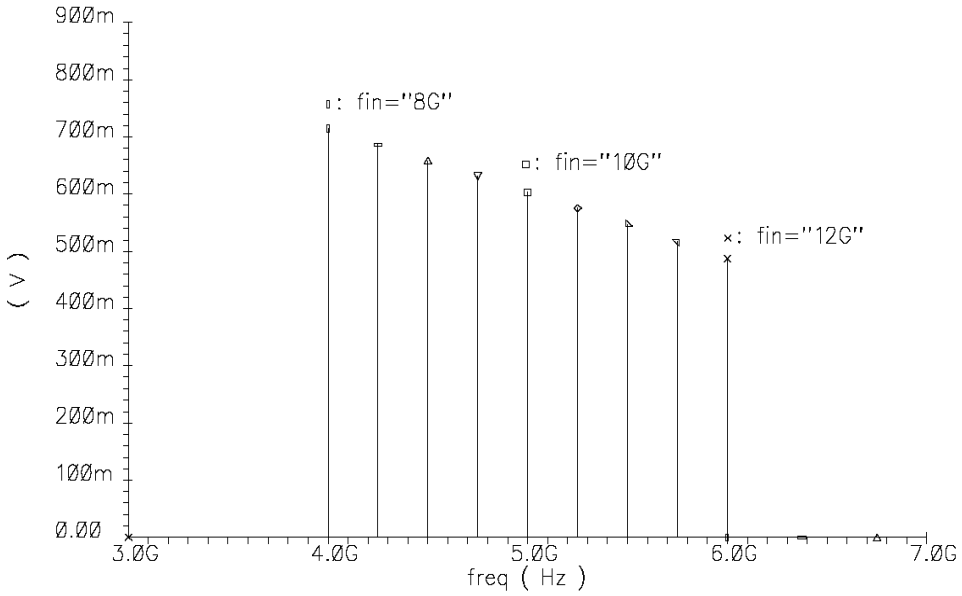


Figure 3.17: Cadence PSS simulation of the divide-by-2 prescaler.

Beyond the 12 GHz input frequency, the simulator is unable to find a solution. The transient simulation also indicates that the divider stops functioning beyond 12 GHz. To reduce the power consumption of the prescaler, the second and third divide-by-2 stages can be biased to use less current and still operate normally.

3.4.2 Low Frequency Adjustable Divider

The divide-by-3 low frequency divider is constructed using two JK flip-flops with clear control (Fig. 3.18) [53]. The operation of the divider can be easily described using a state transition diagram. Since two JK flip-flops are used to for the divider, their current state can be expressed using a two bit binary code where each bit represents the Q value of one JK flip-flop. At the beginning of each operation, the current state status is initialized to be 00. At the first rising edge of the clock, the first JK flip-flop will toggle states while the second JK flip-flop will be reset to zero. The state changes from 00 to 10. At the second rising edge of the clock, the first flip-flop will toggle its current state while the second JK flip-flop will be set to one. The state changes from 10 to 01. At the third rising edge of the clock, the first flip-flop will remain at the

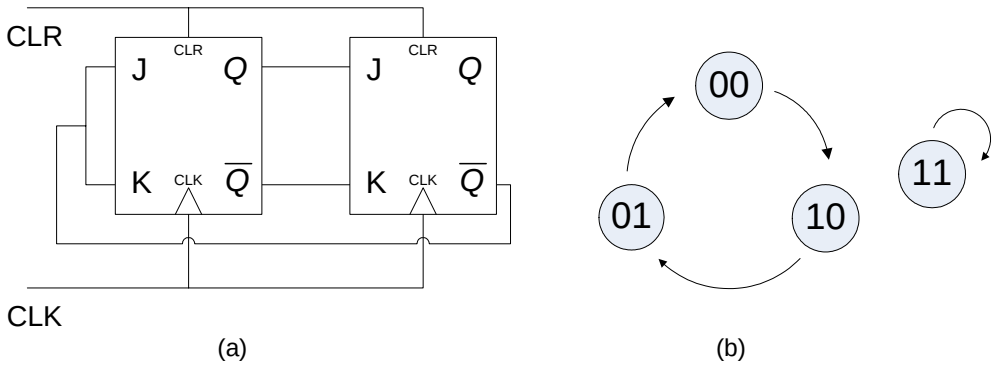


Figure 3.18: Low frequency divide-by-3 stage. (a) Schematic. (b) State transition diagram.

current state while the second JK flip-flop will be reset to zero. The state changes from 10 to 00. The transition will repeat the three states during each cycle. The output is taken from Q of the second JK flip-flop. The output waveform has a period of three times the input clock period with a duty cycle of *1/3*. Note that if for any reason during operation the divider state is changed to 11, it will remain at 11 and no longer function as a divide-by-3 divider. Therefore, the divider needs to be reset to 00 at the beginning of each operation.

The divide-by-4/5 low frequency dividers are constructed using three D flip-flops with clear control (Fig. 3.19). A mode control signal is inserted before the third D flip-flop. When mode is zero, the divider ratio is four; when mode is one, the divider ratio is five. The output of the divider is taken from $\overline{Q}$ of the first D flip-flop. The state diagram clearly shows that there are two separate closed paths with four and five states in each transition circle respectively (Fig. 3.20). The mode control will direct the operation into one of the two closed paths resulting in divide-by-4 and divide-by-5 ratios, respectively. It is worth mentioning that no matter what the initial state is, the operation will eventually fall into the intended closed path after several clock cycles. Unlike the case for the divide-by-3 stage, the divide-by-4/5 stage will not become trapped in an isolated state.

Figures 3.21 and 3.22 provide the schematic and simulated results of the complete variable ratio divider. A two bit selection code $SEL3/SEL4$ sets the desired dividing ratios. The output of the divider F_{out} is then fed to input the of the phase frequency detector and Figure 3.22 shows the corresponding time domain output for divider

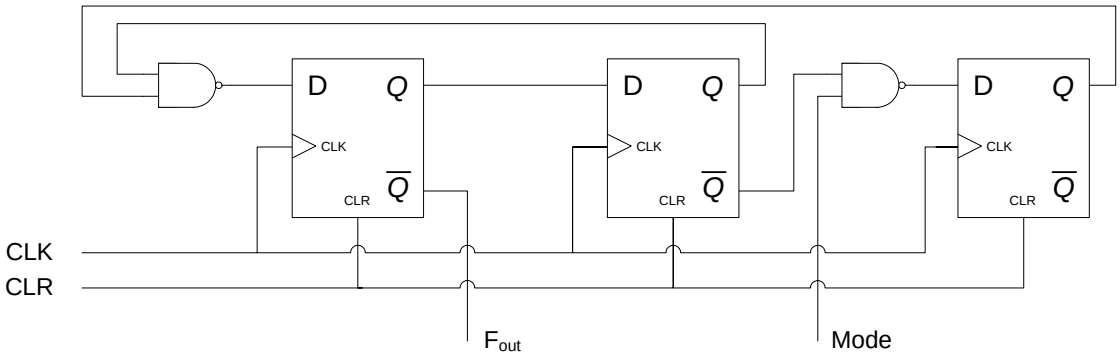


Figure 3.19: Schematic of the low frequency divide-by-4/5 stage.

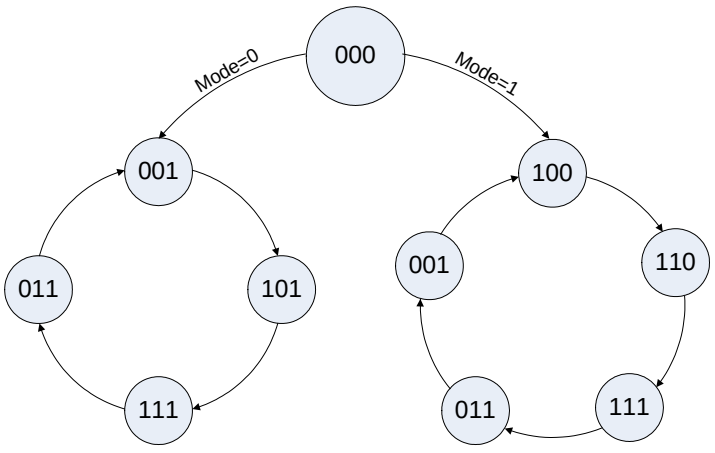


Figure 3.20: State transition diagram of the low frequency divide-by-4/5 stage.

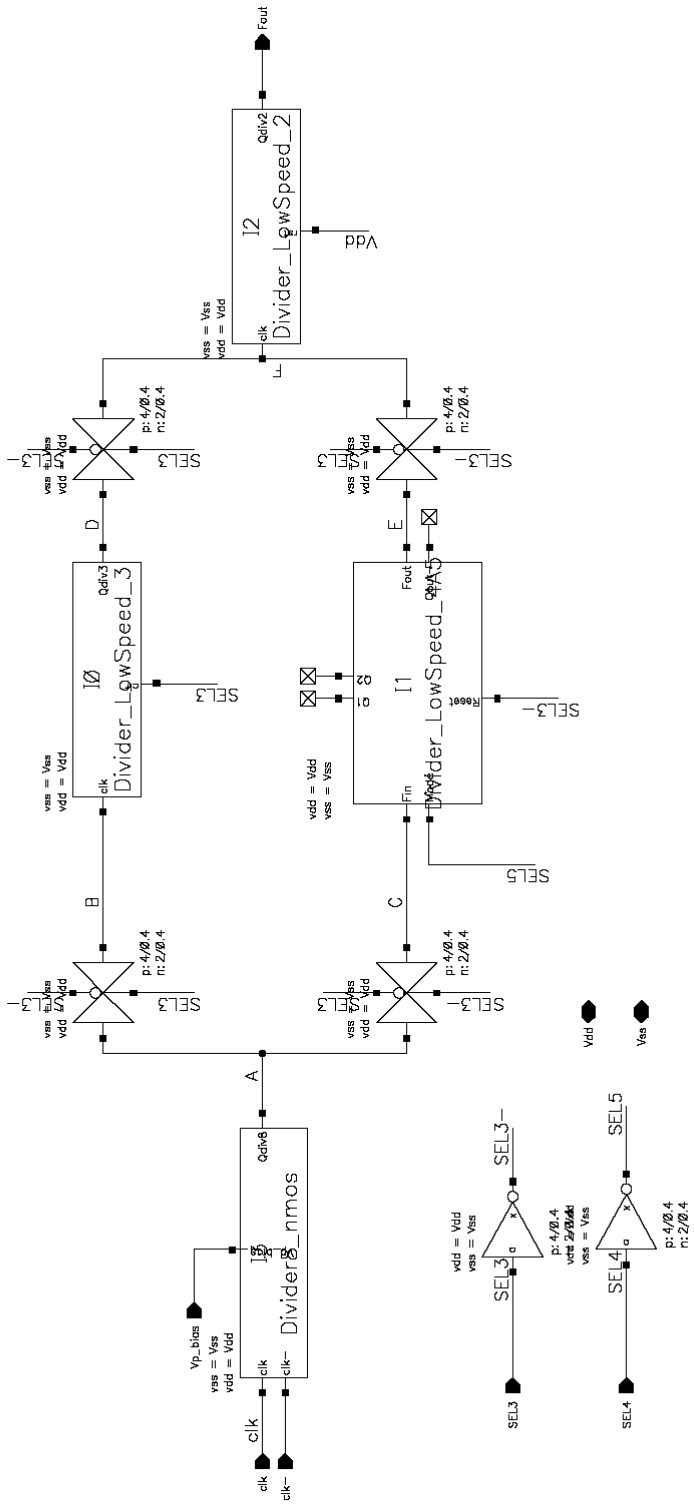


Figure 3.21: Schematic of the designed 48/64/80 divider.

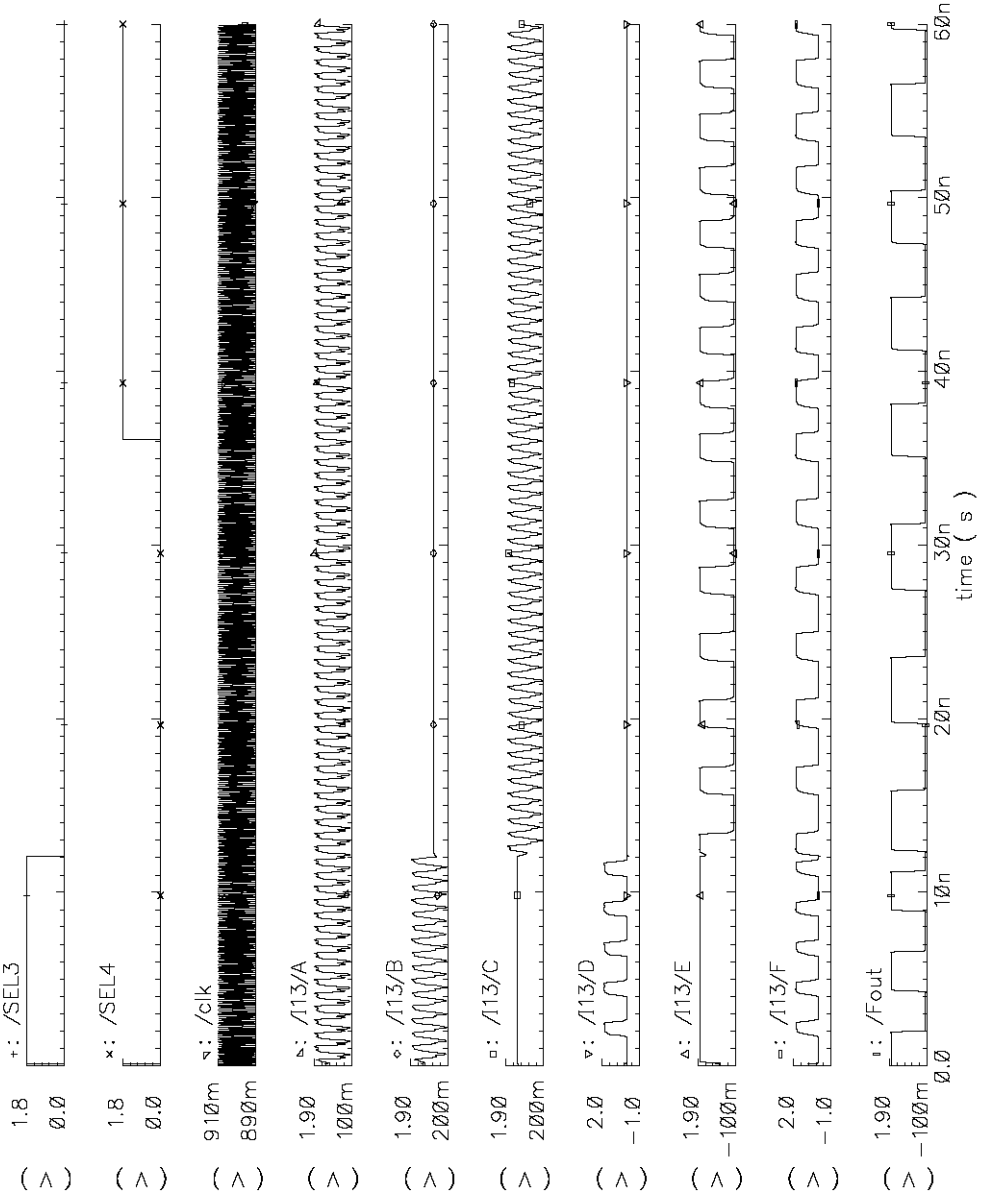


Figure 3.22: Simulation results of the divider with different ratios (48/64/80).

Divider Ratio	48	64	80
SEL3	1	0	0
SEL4	-	1	0

Table 3.1: Logic control table for variable 48/64/80 divider.

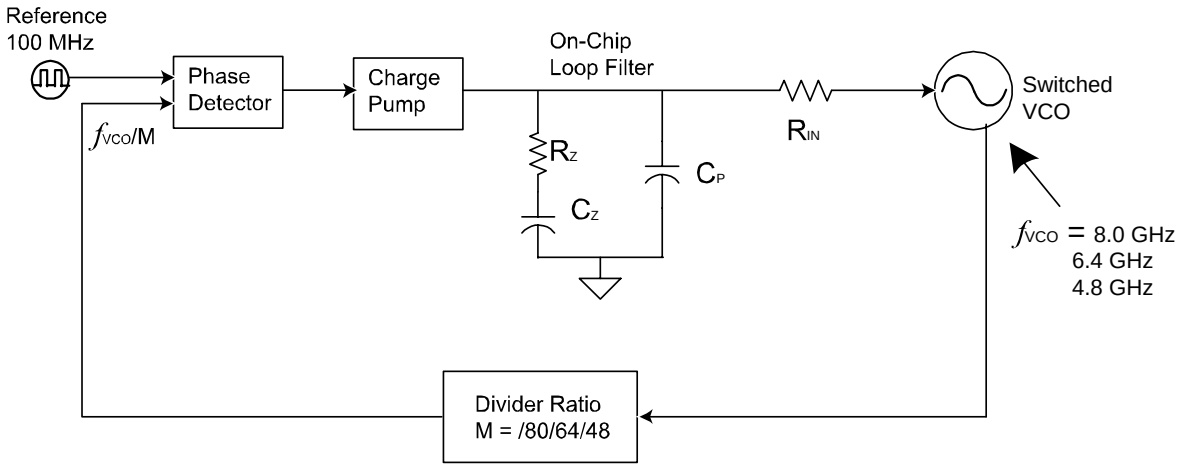


Figure 3.23: The proposed charge-pump PLL with variable divider ratio.

ratios of 48/64/80 respectively. Table 3.1 displays the divider control switch states and corresponding divider ratio.

3.5 Complete Charge Pump PLL Analysis

A charge-pump type PLL has the advantages of low complexity and ease of integration on chip. The prototype PLL in this work consists of: (1) a high-speed CMOS phase/frequency detector (PFD); (2) a CMOS charge pump; (3) a passive, type 2, 3rd order loop filter; (4) a switched tank VCO as described in Chapter Two; and (5) a variable frequency divider (Fig. 3.23) [54]. When locked to the reference frequency, the output of the VCO frequencies are at 8.0, 6.4 and 4.8 GHz, respectively, depending on the tank state. An input frequency of 100 MHz was chosen as the reference source since it is a common divisor of all three frequencies. A variable frequency divider with ratios of 80, 64 and 48 is used to convert the corresponding VCO frequency down to the proximity of input reference frequency.

The charge-pump and phase frequency detector (PFD) convert the input phase error to current which will charge the loop filter. The transfer function of the PFD is:

$$K_{cp} = \frac{I_{cp}}{2\pi} \tag{3.9}$$

where I_{cp} is the charge pump current. The PFD is capable of tracking phase range of $\pm 2\pi$. The passive loop filter inside the PLL consists of a shunt resistor R_z and capacitor C_z pair in parallel with another shunt capacitor C_p. The series RC pair adds a zero in the transfer function to adjust the loop bandwidth and phase margin. The added shunt capacitor C_p provides an extra pole at higher frequencies which will filter out the high frequency noise. The loop filter transfer function is:

$$K_{LP}(s) = \frac{V_{ctrl}(s)}{I_{cp}(s)} = Z_{LP}(s) \tag{3.10}$$

where V_{ctrl} is the output voltage of the loop filter, and I_{cp} is the charge pump current flow into the loop filter. The loop filter transfer function is therefore the impedance of the passive filter:

$$\begin{aligned} Z_{LP}(s) &= sC_p \parallel (R_z + \frac{1}{C_z}) \\ &= \frac{1 + sR_zC_z}{s^2R_zC_zC_p + s(C_z + C_p)} \\ &= \frac{1 + sR_zC_z}{s(C_z + C_p)(1 + sR_z\frac{C_zC_p}{C_z + C_p})} \\ &= \frac{1 + s\tau_z}{s(C_z + C_p)(1 + s\tau_p)} \\ &= \frac{1 + s/\omega_z}{s(C_z + C_p)(1 + s/\omega_p)} \end{aligned} \tag{3.11}$$

where $\tau_z = R_zC_z$, $\tau_p = R_z(C_z^{-1} + C_p^{-1})^{-1}$, $\omega_z = 1/\tau_z$, $\omega_p = 1/\tau_p$.

The open loop function $G(s)$ at the VCO can be calculated as:

$$G(s) = \frac{K_{cp}K_{LF}(s)K_v}{s} \tag{3.12}$$

With the divider ratio of 1/N, the open loop function $G_1(s)$ at the divider output is:

$$\begin{aligned} G_1(s) &= \frac{G_1(s)}{N} = \frac{K_{cp}F_{LF}(s)K_v}{sN} \\ &= \frac{I_{cp}K_v}{2\pi N}\frac{1+s/\omega_z}{s^2(C_z+C_p)(1+s/\omega_p)} \end{aligned} \tag{3.13}$$

The PLL bandwidth ω_0 is a very important design factor, it can be estimated as the frequency where the open loop function $G_1(s)$ equals to one. Assuming $\omega_z \ll \omega_0 \ll \omega_p,\ C_p \ll C_z$:

$$|G_1(s)| \approx \left|\frac{I_{cp}K_v}{2\pi N}\frac{s/\omega_z}{s^2(C_z+C_p)}\right| = 1 \quad when \ \ \omega = \omega_0 \tag{3.14}$$

and the bandwidth of the PLL can be derived as:

$$\omega_0 \approx \frac{I_{cp}K_vR_z}{2\pi N}\frac{C_z}{(C_z+C_p)} \tag{3.15}$$

The open loop function $G_1(s)$ of the designed PLL has three poles, with two at origin and one at ω_p; in addition it has a zero at ω_z. The positions of the pole and zero of $G_1(s)$ are placed to achieve certain bandwidth and phase margin for the entire PLL with the zero placed at a lower frequency to the pole. As frequency increases, $G_1(s)$ initially decreases at -40dB per decade with a phase angle of -180^o due to two poles at the origin. Once the frequency reaches the zero, $G_1(s)$ decreases at a reduced rate of -20dB per decade. The zero also adds 90^o to the phase of $G_1(s)$. At the pole ω_p, $G_1(s)$ starts falling at 40dB per decade again with an additional -90^o to the phase of $G_1(s)$.

A complete transistor level phase locked loop simulation is quite time consuming and should only be used as the last design step to verify the PLL performance. The design process can be divided into three stages (Fig. 3.24). The first stage is a phase domain simulation in Matlab which takes the least time. Once reasonable performance is achieved at this level, a behavioral model such as VerilogA is used to simulate the performance the complete PLL. The VerilogA components are then replaced by the actual circuits. The last step involves simulating the complete transistor level schematic in Cadence in the time domain and can be time consuming.

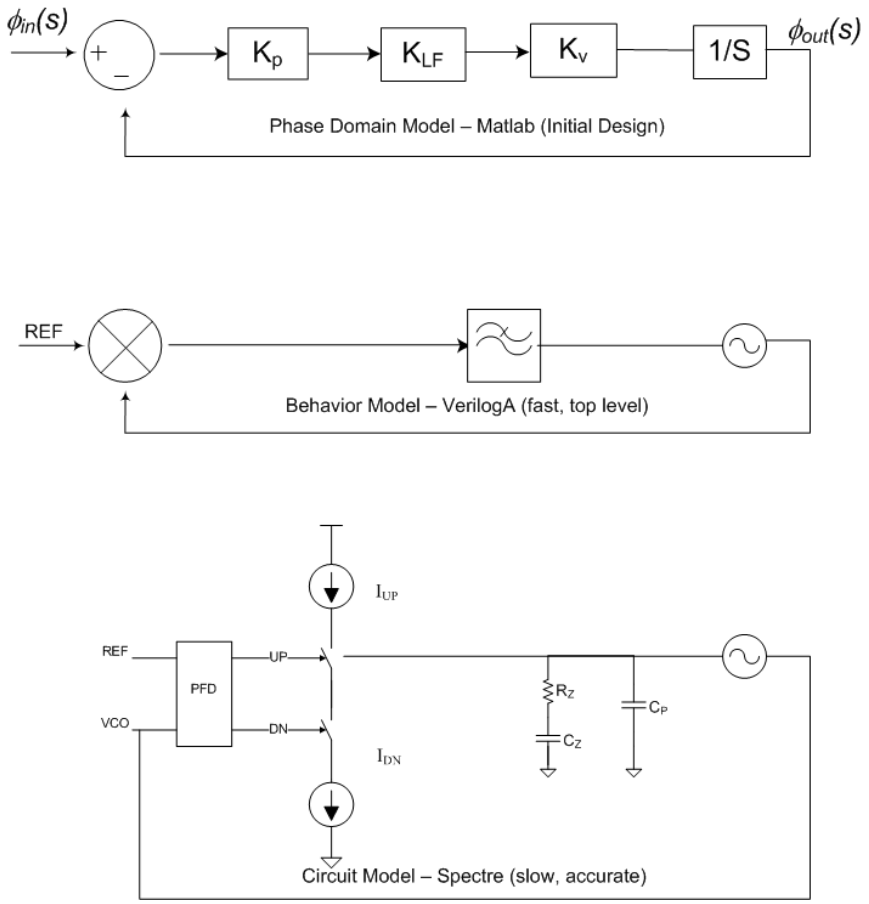


Figure 3.24: Three stage design flow for a PLL.

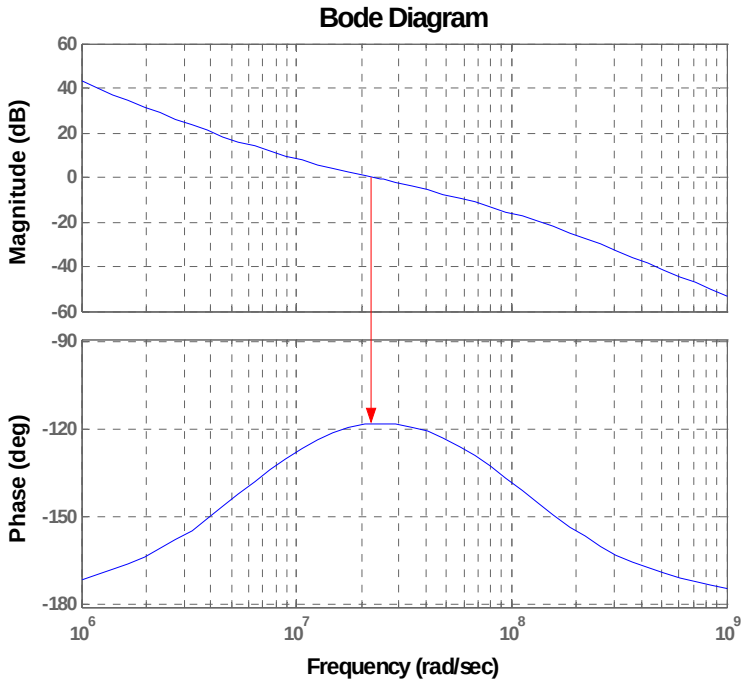


Figure 3.25: Bode plot the of the PLL open loop function $G_1(s)$

The phase locked loop is initially designed using Matlab for the open loop gain and phase margins. The PLL in this project is designed to have wide bandwidth ($\sim$3.7 MHz), short lock-in time, and near critical damping with a damping factor of $\sim$1 (Fig. 3.25). A damping factor close to one indicates that the loop will reach lock in one cycle inside of skipping cycles. The zero is located at 1 MHz and the pole is located 16 MHz. Their relative locations affect the phase margin and damping factor. The target phase margin is over 60^o so that the loop will be unconditionally stable.

The closed loop function and error function of the loop are plotted in 3.26. The closed loop function starts at one, and starts to drop at 40 dB per decade once the frequency is out of the loop bandwidth. The error function $H_e(s)$ increases at 40 dB per decade before it reaches the loop bandwidth, then it approaches one. The VCO noise inside of the loop bandwidth is attenuated by the error function $H_e(s)$, while the noise from reference outside of the loop bandwidth is attenuated by the closed loop function $H_1(s)$.

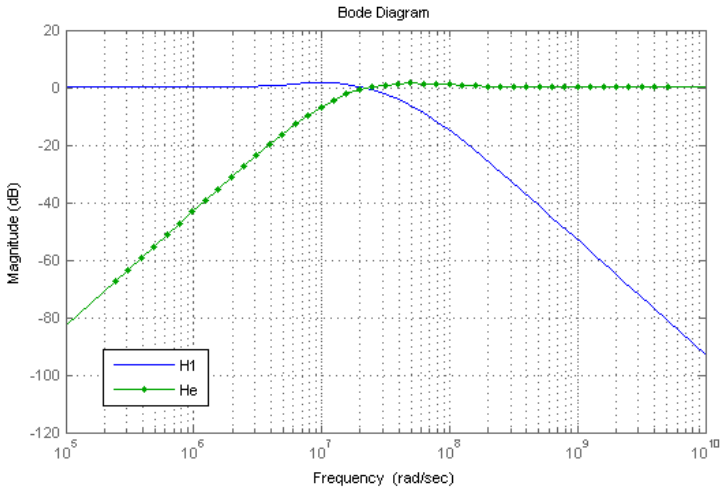


Figure 3.26: Bode plot the of the PLL closed loop function $H_1(s)$, and error function $H_e(s)$.

Finally, the PLL circuit was designed and simulated using Cadence version 4.4.6. VerilogA simulation blocks are replaced by transistor level RF circuit blocks. Simulation results show that the PLL locks within $0.7\mu s$ while switching over the three-frequency bands. The PLL is designed to be close to critical damping, which is also supported by the simulation results (Fig. 3.27); the VCO control voltage takes about one cycle to acquire lock.

3.6 Pulse Generator

The pulse generator was designed to generate DPSK modulated signals complying with the required FCC UWB spectrum mask [23] [55]. Unlike the carrier-less pulse generator where the energy is spread from $\sim$ DC to several GHz, the proposed pulsed binary modulation is based on a carrier frequency approach, and the majority of transmission energy is concentrated around the carrier to comply with the FCC rules.

Various UWB pulse generation methods have been proposed recently. One of the proposed methods generates Gaussian monocycle pulses using a delay block, digital logic and an RLC Band pass filter [56]. Another example uses step recovery diodes and a tunable transmission line to realize tunable duration pulses [57]. Some of those

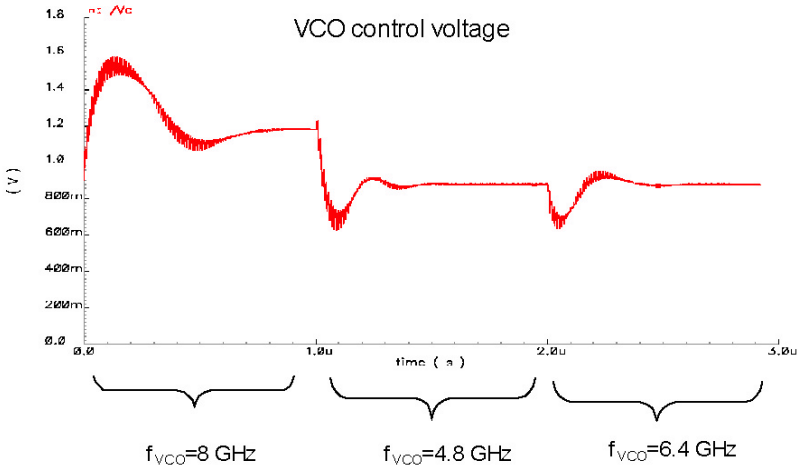


Figure 3.27: Simulated VCO control voltage of PLL when switched between the three-frequency bands.

proposed pulse generators are difficult to be integrated on a chip; others have their energy extending to the low GHz frequency range which could create interference with transmissions such as GPS. In this work, a low power fully integrated digitally-based pulse generator is implemented in CMOS. The design is capable of multi-band operation and controllable bandwidth. Since the pulse generator is part of the PLL based transmitter, it has a precise center frequency.

3.6.1 Prototype Pulse Generator

A prototype pulse generator was designed both to create the short pulses needed for Ultra-Wideband transmission and to DPSK/BPSK modulate data onto the pulses. The bi-phase modulation is realized simply using circuitry which selects either in-phase or 180° out-of-phase signals from a differential VCO output according to the binary data input. The design transmits a bi-phase modulated train of pulses with 500 MHz of bandwidth centered on the PLL frequency. It will transmit an in-phase signal with a data input of 0 and out-of-phase signal with a data input of 1.

The pulse generator can be divided into two parts (Fig. 3.28): (1) a pair of CMOS transmission gate switches controlled by a decoder; and (2) a control circuit generating 4-ns on-time square pulses from the 100 MHz frequency reference (40% duty

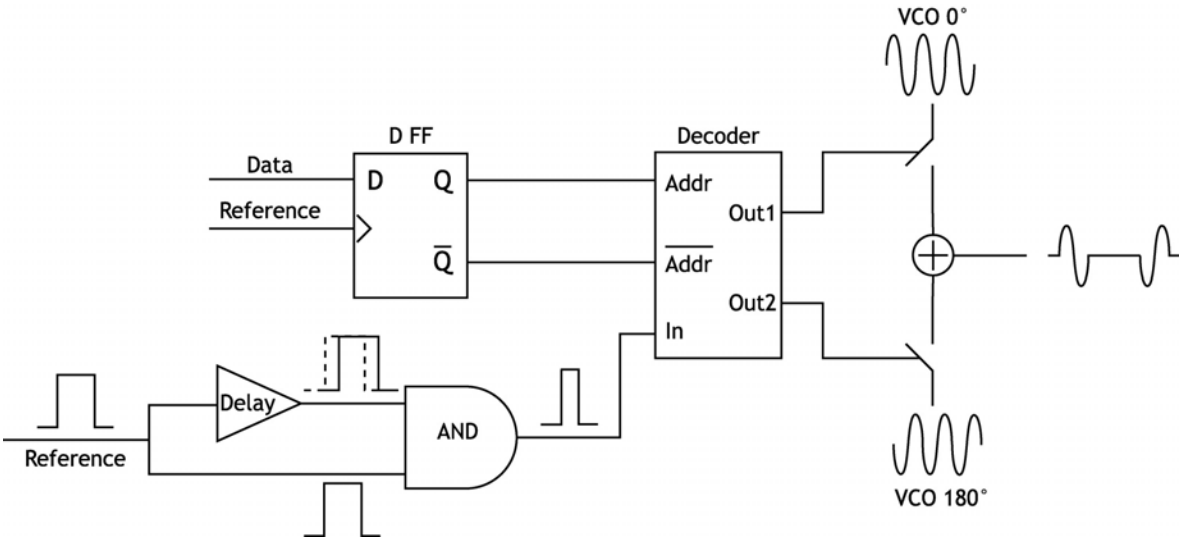


Figure 3.28: Simplified diagram of pulse generation circuit.

cycle). The on-resistance of CMOS switches depends on the size of the transistors; the insertion loss due to the switches decreases with increasing transistor size. However, larger transistors will reduce the isolation while the switch is off. Therefore, the transistor size is a compromise between the insertion loss and isolation.

The transmission gate control circuit utilizes a combination of AND and DELAY circuits to created the desired 40% duty cycle gated pulses. The reference square wave at 100 MHz is passed through the delay line designed to be 6 ns; the delayed reference signal is then ANDed with the original reference signal. This ideally results in a square pulse 4ns in width with a repetition frequency of 100 MHz. At the same time, the digital data to be encoded on BPSK pulses passes through a D flip-flop clocked by the reference frequency of 100MHz. The output from the D flip-flop changes to the next digital data value each reference period of 10ns and then selects either (+) or (-) RF outputs of VCO at the decoder circuit. The decoder circuit sends the 4ns gating pulse to the gates of the transmission gates to create pulsed bi-phase output of 40% duty cycle and a first null bandwidth of 500 MHz. Figure 3.29 shows both the time domain and frequency domain pulse generator outputs. Note that the pulses at different frequencies are actually generated from separate simulations but are displayed on the same graph for ease of comparison.

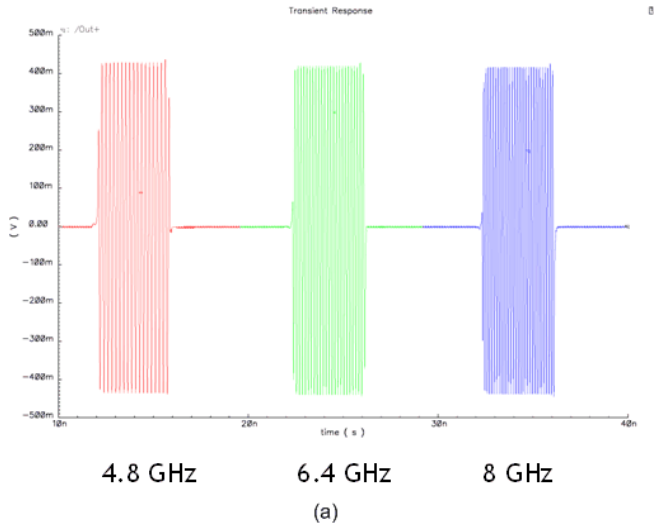


Figure 3.29: Pulsed DBPSK signal at the output of the pulse generator in the (a) time domain; and (b) frequency domain.

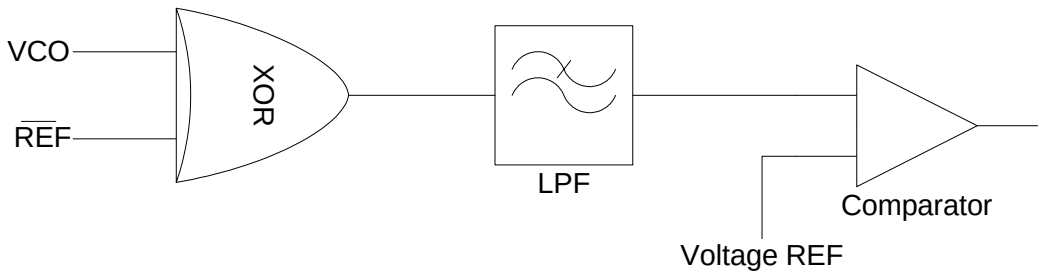


Figure 3.30: A simplified diagram of the lock detector.

3.6.2 Lock Detector

The multiband transmitter is designed to hop to different carrier frequencies controlled by a two bit code. If transmissions start before the phase locked loop settles, excessive bit errors and undesired out-of-band spurs will result. Therefore, a lock detector circuit is designed to ensure that transmitter will only operate under stable PLL conditions. The lock detector is composed of an exclusive OR gate, a low pass filter and a comparator (Fig. 3.30). The XOR is basically acting as a phase detector; it generates an error output by comparing the phase relationship between the two inputs. The low pass filter after the XOR is used to filter out the high frequency components. As the VCO and reference phase are pulled together by the phase locked loop, the filtered XOR output becomes closer to high logic level (VDD). This output is then sent to a comparator with one input set by a predetermined voltage reference level. A high output is generated at the output of the comparator, which declares lock for the transmitter and subsequently allows transmitting signals. A simulation result for the lock detector is shown in Figure 3.31.

3.7 Summary

The proposed SiGe multiband carrier based UWB transmitter design is covered in the this chapter. The main design issues associated with an integrated charge pump phase locked loop are discussed in detail as well as major components of the PLL including phase detector, charge pump, loop filter and variable ratio dividers. Since the PLL is required to operate with fast locking speed, a wide bandwidth of the loop is

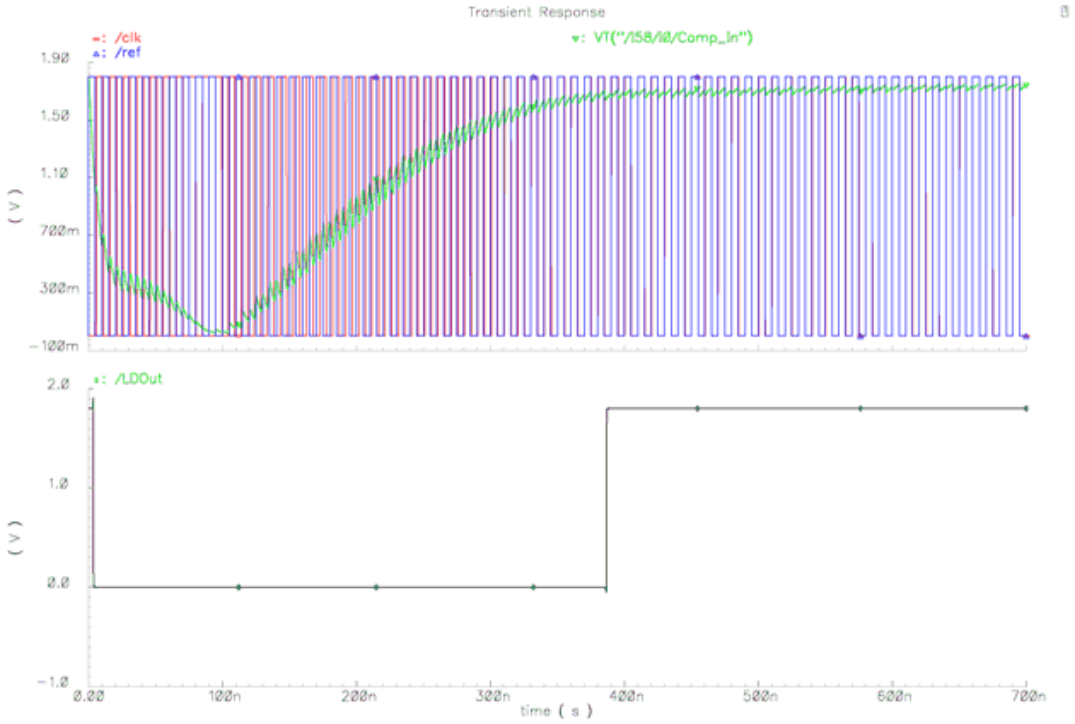


Figure 3.31: Simulated output of a lock detector.

needed. A high reference frequency is also needed to keep the PLL stable and achieve fast lock speed. Because the circuit parasitics change significantly over the wide bandwidth, it is important to design the highest frequency band to perform correctly since it is most sensitive to this parasitics. Matlab is used to simulate the initial design of the PLL in the phase domain. VerilogA models of various loop components are then used to accelerate the simulations in the time domain which is followed by circuit level simulation using Cadence SpectreRF. A CMOS pulse generator using delay lines to generate the desired pulses are deigned as part of the transmitter. The pulse generator provides a simple but efficient way to generate bi-phase UWB pulses. In order to ensure that the PLL is in lock before transmission can occur, a lock detector circuit is also implemented in the transmitter design.

Chapter 4

SiGe UWB Transmitter Layout and Performance Measurements

The complete prototype UWB transmitter discussed in Chapter 3 was designed and fabricated in Freescale's $HIP6WRF$ $0.18\mu m$ BiCMOS process. The layout tool used was Cadence Virtuoso; verification was completed using Assura. The complete transmitter chip occupies a die area of 1mm×1.5mm, and was mounted on a 28-pin 5mm×5mm Amkor MicroLeadFrame[1] [58] package for measurements. A test board for the prototype UWB transmitter was fabricated on a custom-designed four layer FR4 board. In addition, a separate breakout version of the switched tank VCO discussed in Chapter 2 was also fabricated with pads configured for on-wafer probe testing.

The layout at RF frequencies is quite different from that for digital circuits. Since the designed transmitter circuit is to be operating up to above 8 GHz, layout of the complete circuit must be carefully planned. The critical RF paths need to be kept at minimum length while maintaining symmetry for different classes of signals. Parasitics are quite significant at RF frequencies and this makes layout a critical part of the design process. Since the complete transmitter includes both digital and RF circuits on the same die, it is an important yet difficult task to prevent the digital switching noise from coupling into the RF circuit.

[1] MLF – Amkor version of the QFN (Quad Flat No-Lead) package

The breakout VCO was designed to be measured on-wafer on a Cascade probe station. Both frequency and time domain performances were characterized. The complete transmitter design was measured at board level. The pulse generator was measured in both time and frequency domain. Various design issues were identified during the measurements, such as the accuracy of the pulse generator, that led to design improvements to be described in subsequent chapters.

4.1 Layout

The UWB transmitter presents significant layout challenges since it is a mixed-signal part with both analog and digital components integrated on the same chip. The digital noise coupled through the low resistivity silicon substrate can be coupled into sensitive analog and RF components and potentially degrade the overall chip performance. Therefore the layout is carefully planned to reduce possible interference between the digital and RF sections by maximizing the distance between them, while maintaining a small footprint for the overall chip. In addition, ground walls are employed to segregate the sensitive RF components from the rest of the chip (Fig. 4.1); the ground wall has its own ground pin separate from the system ground in order to decouple digital noise from the RF components. By providing a low impedance path through the ground wall, interference coupling between the analog/digital and RF circuit is substantially reduced.

4.1.1 Breakout VCO layout

The switched tank VCO occupies a die area of 1mm×0.8mm including probe pads (Fig. 4.2). The VCO core is identical to that implemented in the overall UWB transmitter circuit. The breakout VCO layout has a total of 13 probe pads for biasing, control, and RF measurement purposes (Table 4.1). All pads have dimensions of $100\times75\mu m$, and a pitch of $150\mu m$ to accommodate available RF and DC probes. The RF pads are placed over an isolated nwell to shield them from substrate noise, while DC pads are placed directly over P substrate. The isolation nwells are connected to V_{DD} forming a reverse biased PN junction. The V_{DD} connection to nwells also provides a low impedance path for noise coupled to the nwell from the substrate,

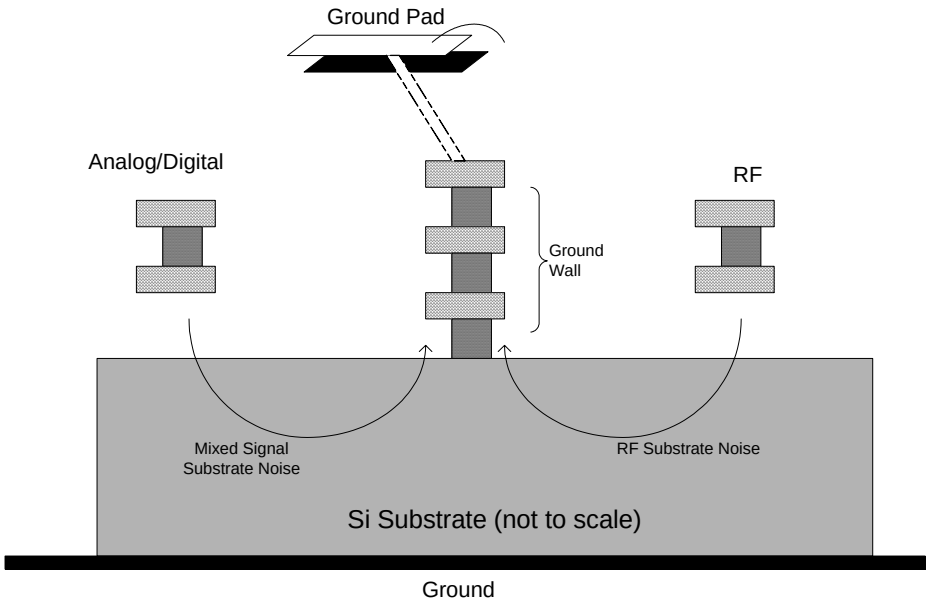


Figure 4.1: Vertical view of metal to substrate layers with ground wall connection.

Pin Name	Function	Pad Type
V_o+	RF output (positive)	RF
V_o-	RF output (negative)	RF
$SW1$	Tank 1 control	DC
$SW2$	Tank 2 control	DC
$V\_control$	Tuning voltage	DC
CM_V_{DD}	Bias control	DC
$Buffer\_V_{DD}$	Buffer bias control	DC

Table 4.1: Breakout switched tank VCO pin assignment.

minimizing noise reaching the RF signal pads.

The differential VCO output signal V_o+/V_o- is coupled out through GSSG (Ground-Signal-Signal-Ground) probe pads, shown in Fig. 4.2 at the top of the layout. DC supply voltages for the output buffer and current mirror of the VCO are provided via the GSSG probe pads on the left side of the layout. The DC supply voltage (V_{DD}) for the VCO is provided via a single pad at the bottom of the layout. A 4-pin DC probe provides control signals SW1/SW2 for selecting the different VCO frequency bands, as well as the VCO varactor control voltage.

Post layout extraction of the VCO circuit was performed using Assura excluding

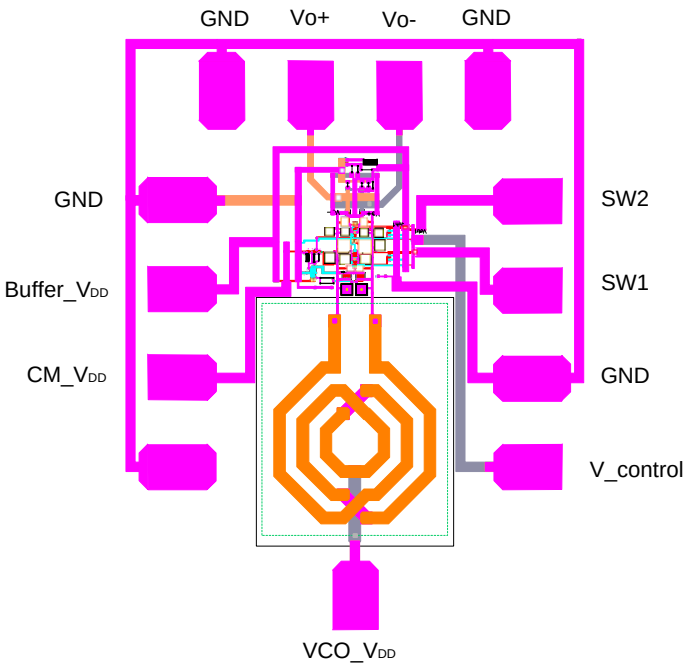


Figure 4.2: Layout of the breakout switched tank VCO. (die area = 1mm×0.8mm including pads)

the custom designed octagonal differential inductor. The VCO design was then re-simulated including the extracted parasitics, which reduced the resonant frequency. The tank capacitors were then reduced in size accordingly to restore the desired design resonant frequency.

4.1.2 UWB Transmitter Layout and Packaging Plan

The chip layout of the complete UWB transmitter design is shown in Fig. 4.3. The UWB transmitter occupies a chip area of 1mm × 1.5mm, including the three major parts: multiband PLL, switched capacitor tank VCO, and pulse generator. The PLL part includes the variable frequency divider, phase detector with charge pump, and on-chip loop filter. The pulse generator includes the pulse shaping circuit and lock detector.

The chip was designed to be packaged in a QFN 28pin $5mm \times 5mm$ package. The ground pins are intended to be downbonded to the package "die flag" directly to

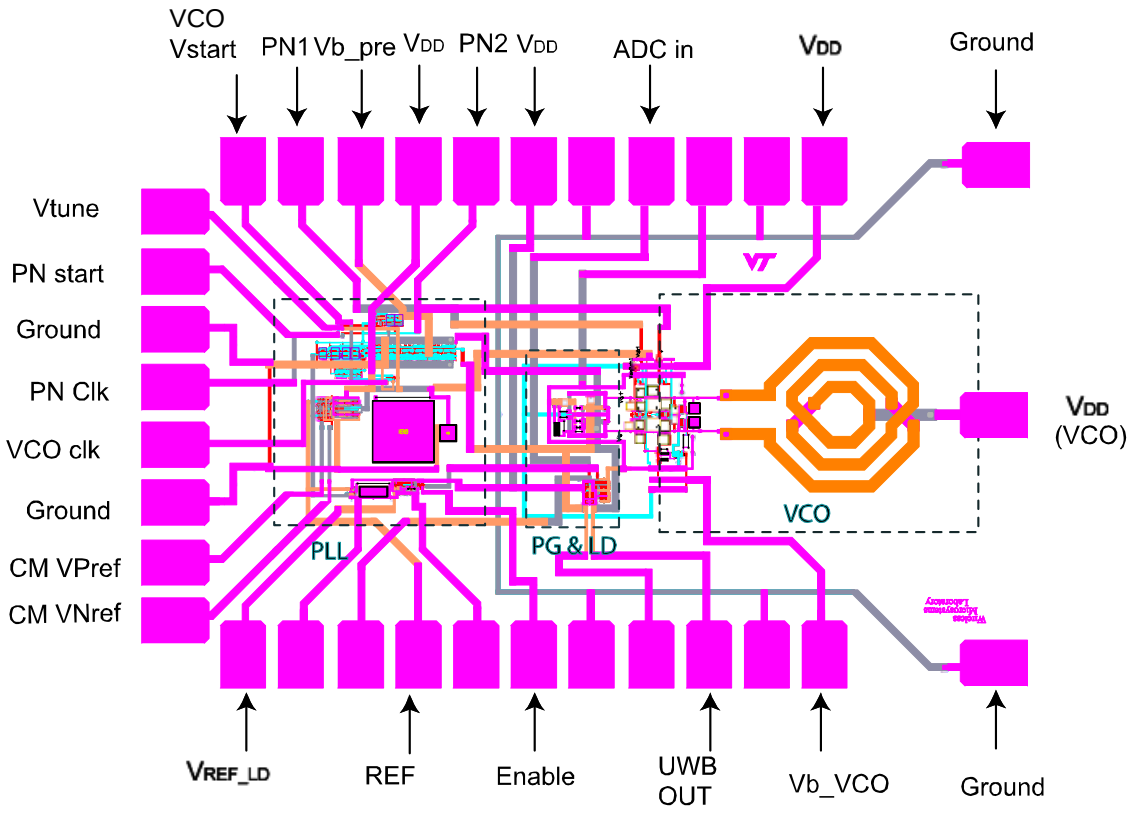


Figure 4.3: Layout of the UWB transmitter including PLL, VCO and pulse generator (die area = 1mm × 1.5 mm)

Pin Name	Function	Pad Type
$UWB\ OUT$	Differential UWB pulse output	RF
REF	100 MHz reference clock	RF
$ADC\ in$	Base Band Data Input	RF
$PN1(PN2)$	UWB band selection code	DC
$Vtune$	VCO Tuning voltage	DC
$CM\ VP(N)\ ref$	Charge pump reference voltage	DC
V_b_pre	Prescaler bias voltage	DC
V_b_VCO	VCO bias voltage	DC
$Enable$	Pulse Generator Enable	DC
$Lock\ Det\ Vref$	Lock detector comparator reference voltage	RF

Table 4.2: Complete transmitter chip pin assignment.

reduce their lengths. However, these bondwires still each present a finite inductance of $\sim 0.4nH$. This translates to an impedance magnitude of 20Ω at 8 GHz. If the digital and RF grounds were to be tied together, noise from the digital part could easily be coupled to RF parts due the imperfect grounding on chip. Therefore, the power supplies and grounds for different sections of the chip were separated by connection to different pads. This measure also helps in diagnosis of problems when measuring the chip, allowing different components of the design to be powered up and characterized individually. Table 4.2 shows the the major pin allocations of the UWB chip. The connections to the package pins from the chip pads are shown in Fig. 4.4.

To further reduce the interference between different parts of the chip, especially between digital and analog parts, a ground wall is built between the RF VCO circuitry and the analog/digital circuitry as discussed in Sec. 4.1.1. This ground wall is built from metal 3 all the way down to the bottom metal (Metal1) which is then connected to the substrate through contact vias (Fig. 4.1). This ground structure is then connected to a separate pad which is grounded directly to the "die flag".

4.1.3 Test Board Design

A custom test board was designed to support the UWB transmitter package for the purpose of performing board-level measurements of the phase-locked loop and the transmitter circuitry. The test board is a four metal layer FR-4 material with the following parameters: ε_r=4.3, $\tan\delta = 0.012$, $\sigma = 4.1\times10^7\ S/m$, roughness = 0.1 mil

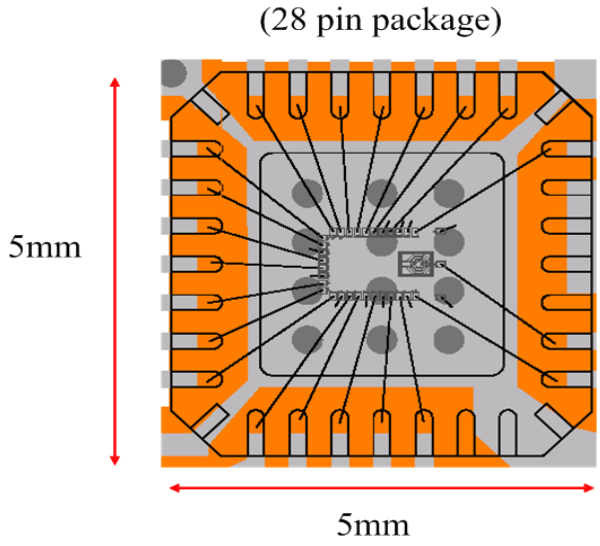


Figure 4.4: 28-pin QFN package diagram of the complete UWB transmitter chip.

(2.54 μm) (Fig. 4.5). The dielectric layer thickness between the top two layers is 10 mil (0.254 mm) which is the most critical design dimension since it dictates the microstrip line impedance.

In the board design, the top metal layer was used primarily for RF signal paths. Most of the DC supply connections are wired to the second metal layer to avoid crossing RF signal lines and reducing coupling between RF and low frequency signal and supply voltages. The remaining two layers were strapped together and served as solid ground through grounding vias. Grounding vias were laid out liberally along the signal paths and around the chip to help reduce cross-talk.

The layout of the test board is shown in Figure 4.6. The overall test board dimensions are 1.8 inch (45.72mm) wide, 0.9 inch (22.86mm) long and 62 mils (1.57mm) thick. The RF and DC feed lines on the board must be properly routed to each pin of the QFN 28pin package. Edge mount SMA connectors were selected for the RF and medium frequency signals, while a single row of pin strip connectors was chosen for the DC to low frequency signals. Surface mount bypass capacitors of value $1\mu F$ are placed between ground and the DC supply lines to filter out unwanted supply interference.

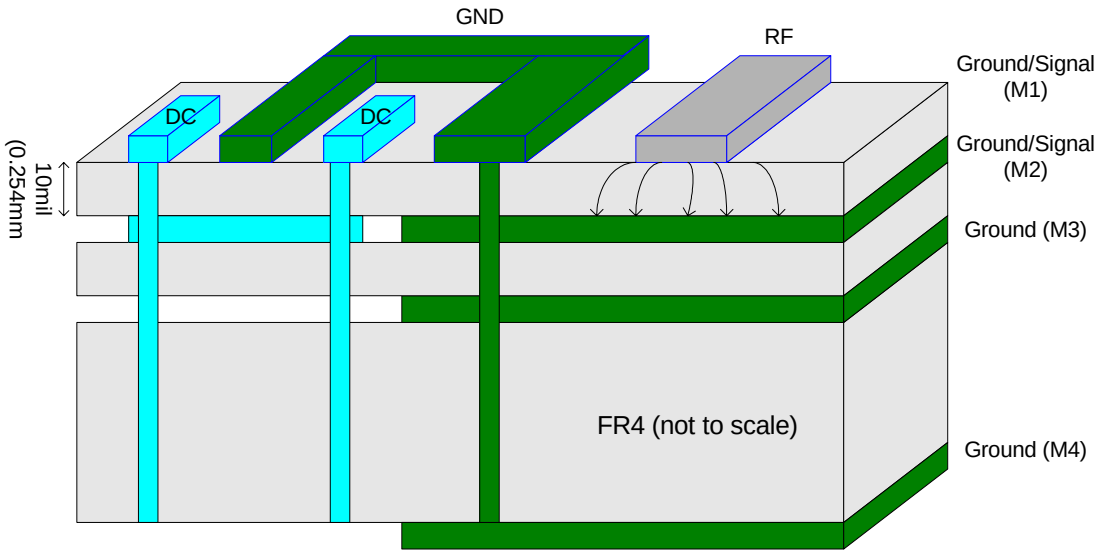


Figure 4.5: Test board material layer assignment.

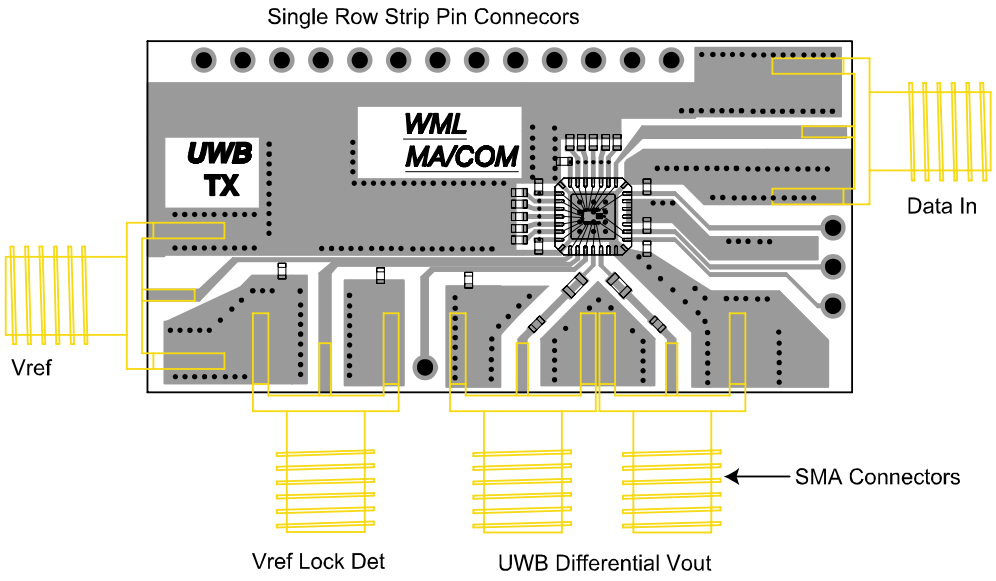


Figure 4.6: Layout of the custom testing board for the UWB Tx design.

Frequency Control	8 GHz Band	6.4 GHz Band	4.8 GHz Band
$SW1\ (V)$	0	1.8	0
$SW2\ (V)$	0	0	1.8

Table 4.3: Breakout switched tank VCO frequency control.

4.2 Test Setup and Measurement Results

The fabricated prototype UWB transmitter and breakout VCO dies were diced into separate chips for packaging and on-wafer measurements, respectively. The breakout VCO was measured on-wafer for its output power spectrum and tuning range in all three frequency bands. Both time and frequency domain results of the locked PLL were measured. The time domain and frequency domain output of the pulse generator was also measured.

4.2.1 VCO Test Setup and Measurement Results

The breakout switched tank VCO die were mounted on a metal carrier substrate using conductive epoxy so they could be easily handled on the probe station. The carrier substrates are placed on the probe station chuck and secured in position by vacuum. The complete setup for the on-wafer measurement of the switched-tank VCO is shown in Fig. 4.7. The equipment includes the Cascade probe station and GSG/GSSG/DC probes, Agilent 34401A multimeter, Agilent E3631A DC supply and HP 8563E spectrum analyzer. The DC supply voltage provided to the VCO V_{DD} pin is 1.8 V. The HPVEE software is used to automatically configure the equipment and acquire data.

As discussed in Section 2.4, the switched capacitor tank VCO operates at three different frequency bands based on the setting of the Switch 1 and Switch 2 control pins (Table 4.3). The VCO operates at (1) high frequency band when both Switch 1 and Switch 2 control are set to 0 V; (2) mid frequency band when switch 1 = 1.8 V and switch 2 = 0 V; (3) low frequency band when switch 1 = 0 V and switch 2 = 1.8 V. One output from the VCO V_o+ is fed to the 8563E spectrum analyzer for measuring the VCO spectrum, while the other is terminated in 50Ω. A photo of the actual equipment setup on the probe station vibration table is shown in Fig. 4.8. A

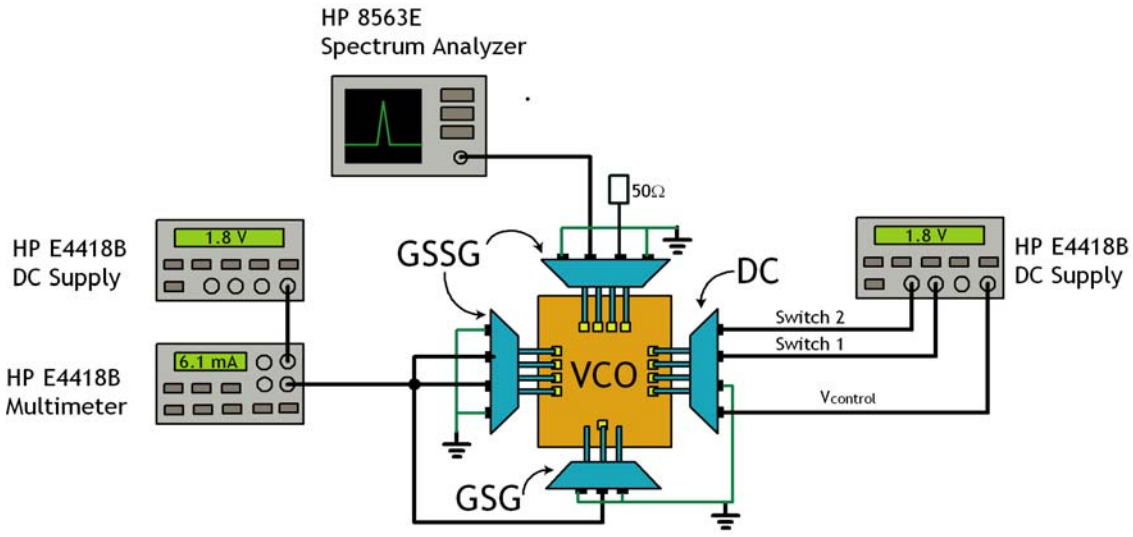


Figure 4.7: Setup of breakout switched VCO on-wafer measurement while mounted on the Cascade probe station

Tuning Range (GHz)	Band1	Band2	Band3
Simulated(parasitic extraction)	1.1(7.4-8.3)	1.8(5.6-7.4)	2.0(4.2-6.2)
Measured	0.89(6.17-7.05)	1.46(5.20-6.66)	2.24(3.72-5.96)

Table 4.4: Simulated and measured VCO tuning range.

micrograph of the VCO die with probes in contact is shown in Fig. 4.9.

The free-running VCO output power level, frequency spectrum and tuning range were measured on-wafer. VCO tuning curves of all three frequency bands (Fig. 4.10) were taken by sweeping the varactor control voltage. The measured VCO resonant frequencies are very close to the simulated results except for the high frequency band which is about 1.2 GHz lower compared to the simulation results (Table 4.4). This is mainly due to the fact that the VCO is very sensitive to even small parasitics at higher frequencies. Note the small hump in the tuning curve in the lower band at a control voltage of $\sim 1.25V$; this is due to the fact that the resistance of the CMOS switches varies as the varactor control voltage changes. As a result, the resonant frequency becomes significantly higher with high switch resistance (see Section 2.4). The peak output power level of the VCO is measured to be $\sim -12dBm$ using the 8563E spectrum analyzer; the low level of the output power may due to the VCO buffer circuit, which was measured to be consuming less DC current than expected.

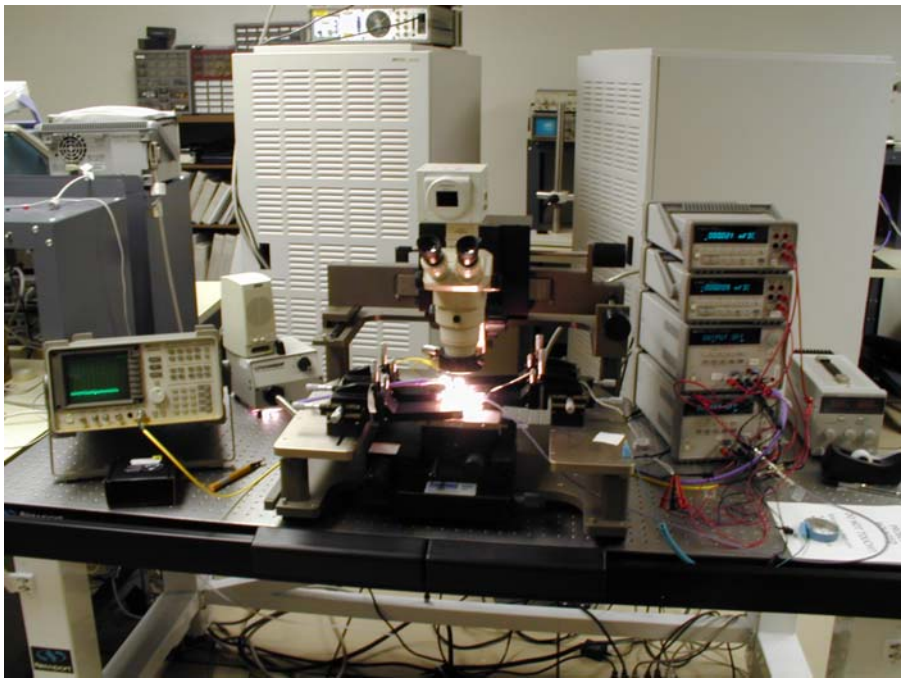


Figure 4.8: Photo of complete equipment setup on the probe station vibration table for VCO on-wafer measurement.

The spectrum taken during on-wafer measurements for the VCO operating in the high frequency band with a varactor tuning voltage of $1.8V$ shows unwanted sidebands. (Fig. 4.11) This is due to an interference signal coupled through probe station of a nearby AM radio station (WKEX) at 1.430 MHz. In order to reduce the sidebands in the VCO spectrum, on-board measurements of the VCO within the PLL circuit were subsequently attempted with the PLL disabled.

4.2.2 UWB Transmitter Measurement Results

The complete fabricated UWB transmitter die (Fig. 4.12) was packaged inside of a QFN 28-pin $5mm \times 5mm$ open top package (Fig. 4.13) through MA/COM, Roanoke, VA. The packaged die was then mounted to custom built testing boards for measurement (Fig. 4.14). In order to reduce the interference coupled through the power rails, $1\mu F$ surface mount bypass capacitors were placed along the power supply traces.

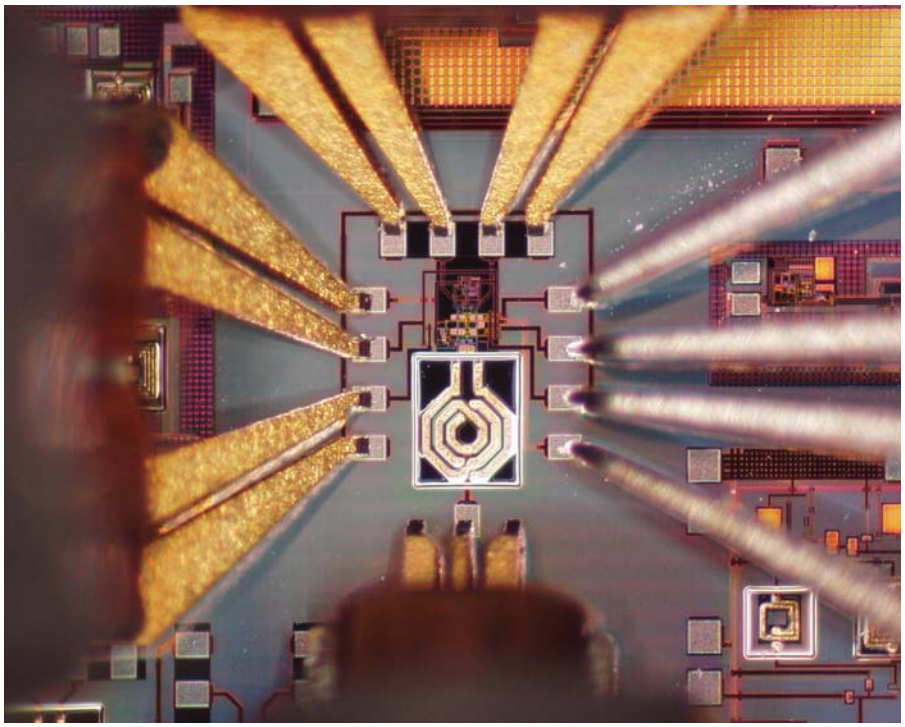


Figure 4.9: Micrograph of the VCO with probe tips in contact with the pads.

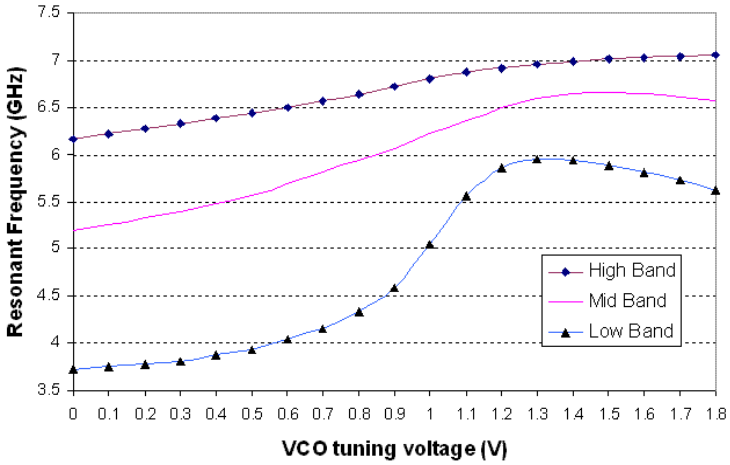


Figure 4.10: VCO tuning curve vs. varactor control voltage for all frequency bands

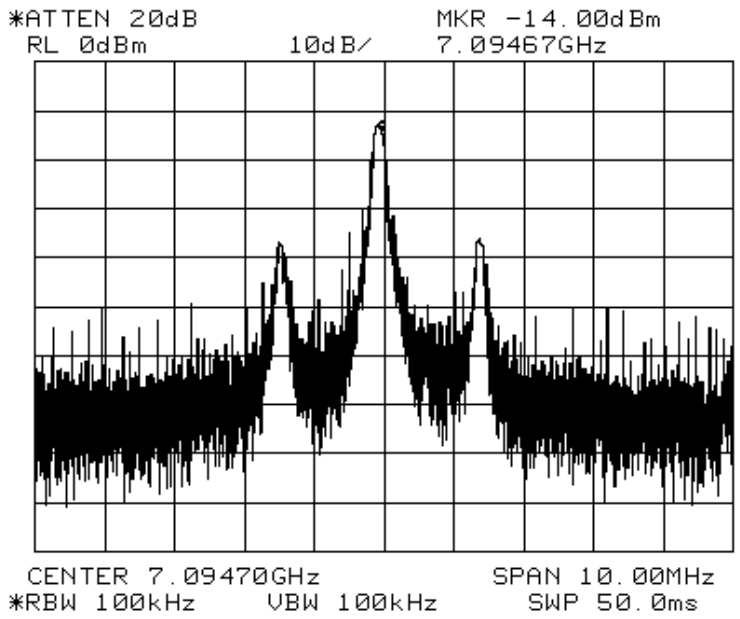


Figure 4.11: VCO spectrum of the high frequency band with varactor control voltage = 1.8 V during on-wafer measurement. Sidebands are located at 1.4 MHz offset.

Phase-locked loop testing setup

The equipment setup for the phase-locked loop measurement is shown in Fig. 4.15. The DC supply and bias network are not shown in the figure for clarity. In order to characterize the phase-locked loop performance, only those parts of the UWB transmitter chip related to the phase-locked loop were powered up. These include the phase detector, charge pump, loop filter, switched VCO, high frequency prescaler and variable ratio low frequency divider. The pulse generator remained off such that the resulting output spectrum is a continuous spectrum instead of a pulsed output.

As in the VCO measurement, DC bias voltages were supplied from the Agilent E3631A and the current was measured using the Agilent 34401A. Because the high frequency band was actually about 1 GHz lower than the simulated results, a reference frequency of ∼80 MHz was used instead of the designed ∼100 MHz. With a reference frequency of 80 MHz and the designed divider ratio in the high-band setting of 80, the phase-locked loop was expected to be able to lock at 6.4 GHz, which is close to the lower end of the high-band tuning curve. The reference frequency was provided from an HP83620B Swept Signal Generator source with a sinusoidal output. In general, it is

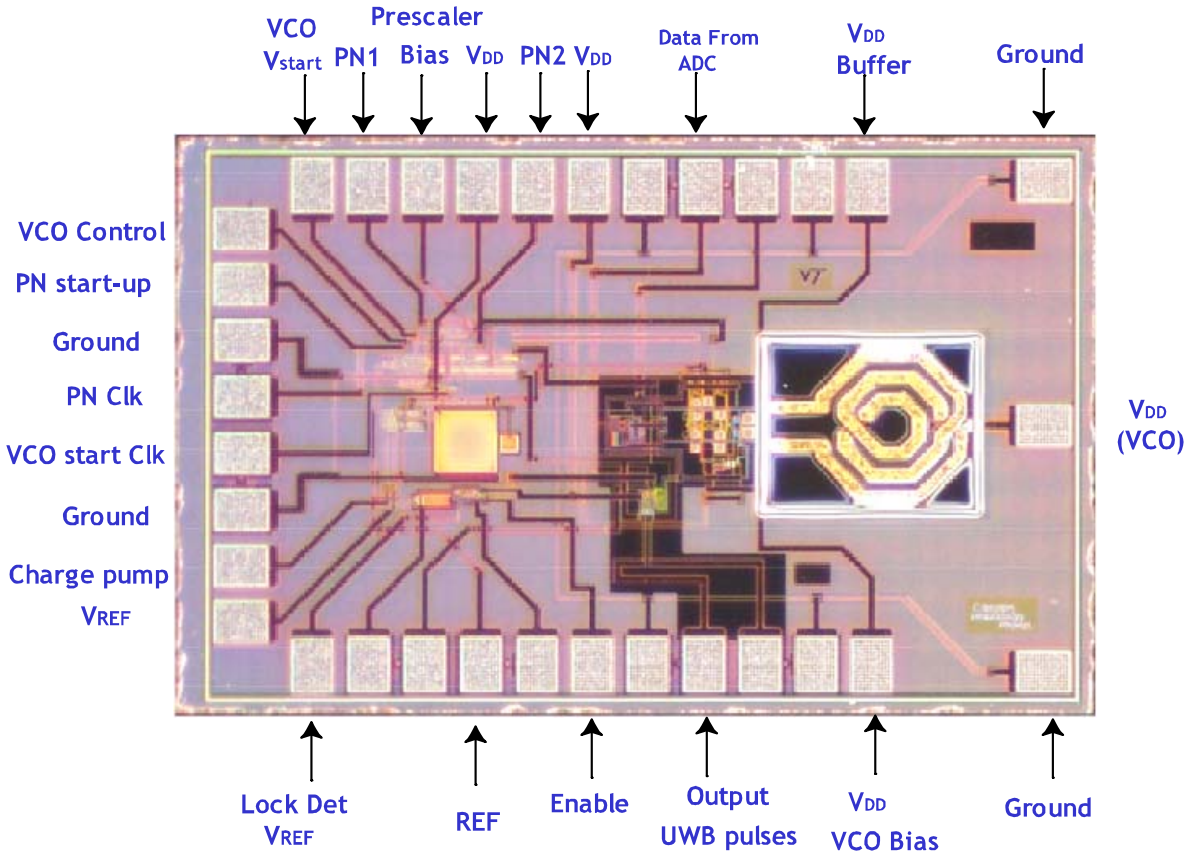
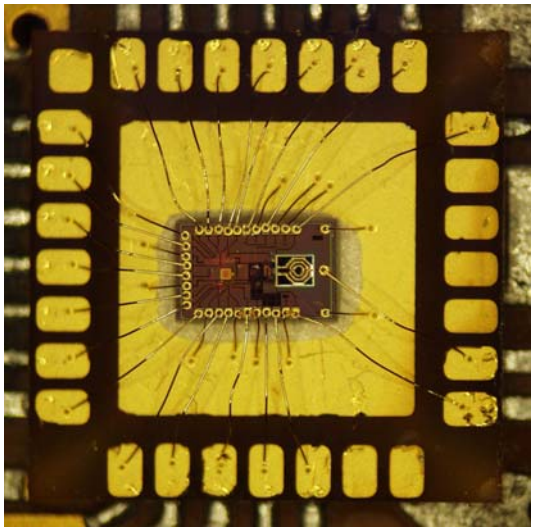
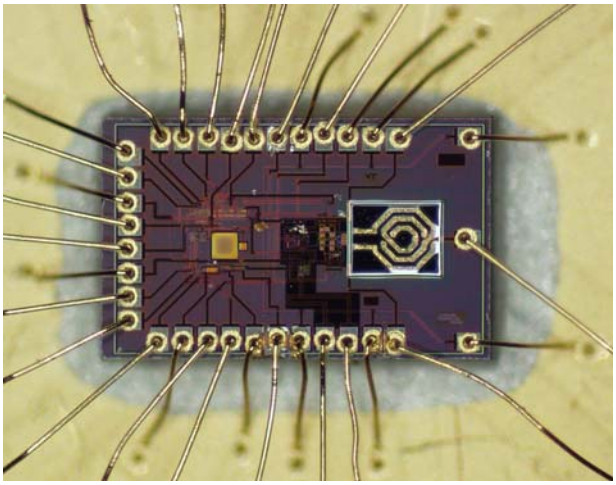


Figure 4.12: Micrograph of the UWB transmitter die (size 1mm x 1.5mm)



(a)



(b)

Figure 4.13: Micrograph of the UWB transmitter die mounted into a QFN 28-pin open top package: (a) die wire-bonded in the package (b) close-up view.

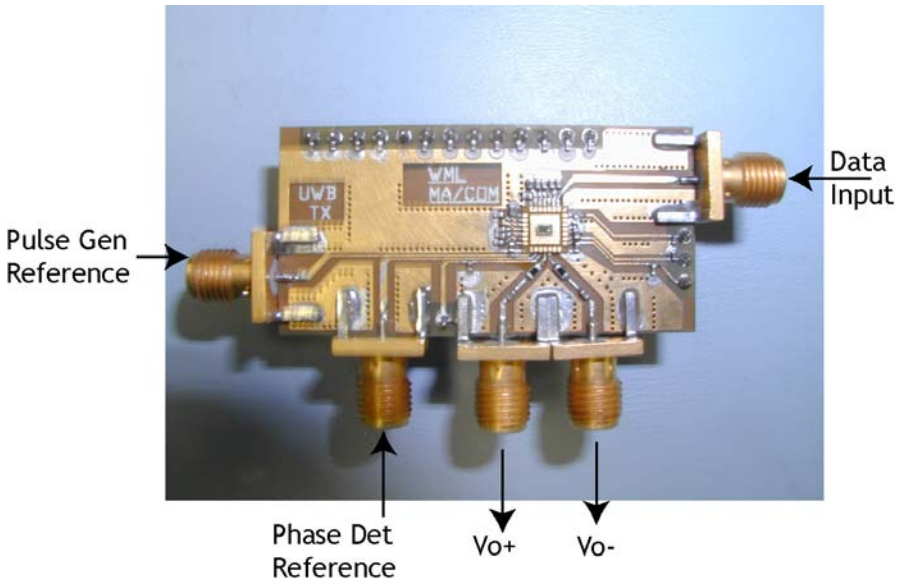


Figure 4.14: Packaged UWB transmitter die mounted on the custom testing board.

preferred to have a square wave reference frequency input since the VCO output after the divider will be close to a square wave. However, a stable square wave generator was not available at the required frequency. In this case, a high sinusoidal signal source amplitude was required to emulate a square wave and switch on the digital phase frequency detector.

The 80 MHz reference source from HP8360B was fed via a Mini-Circuit four-way power divider. Two outputs from the power divider were then connected to the UWB transmitter testing board, one for phase detector and the other for lock detector. The third output from the power divider was fed to the Tektronix CSA8000B Signal Analyzer as the trigger signal. The fourth output was not used and was terminated by a 50Ω SMA load. The differential outputs from the UWB transmitter V_o+/V_o- were connected to the spectrum analyzer and signal analyzer, respectively, for simultaneous frequency and time domain measurement. The varactor control voltage was measured on the Agilent 54264A oscilloscope so that it could be used to monitor the PLL locking performance.

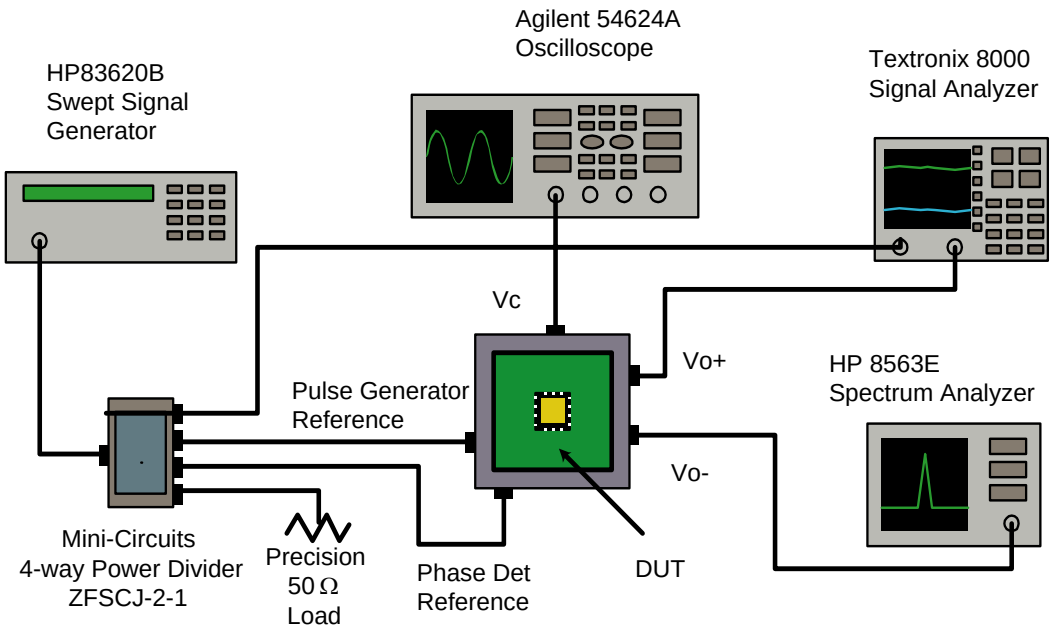


Figure 4.15: Test setup for the phase-locked loop (DC supply and bias network is not shown)

On-board VCO spectrum

The on-board VCO spectrum was measured by only providing DC supply voltage to the VCO related pins on the UWB transmitter chip such that the other parts of the UWB transmitter (PLL, etc.) are turned off. Since the outputs of the VCO are passed through the pulse generator, the measured spectrum in this case is the VCO output leaking through the pulse generator switches. As a result, the peak spectrum is about 20 dB lower than the on-wafer measurement values due to the isolation of CMOS switches in their off-state. The on-board measured spectrum for the higher band with varactor control voltage set to $1.8V$ is shown in Fig. 4.16. The spectrum of on-board VCO measurement does not show the sideband at 1.4 MHz present in the on-wafer results since the parts were more shielded in this case. The peak power spectrum level is $\sim$-38 dBm, which is $\sim$26 dB less than the on-wafer results, as expected.

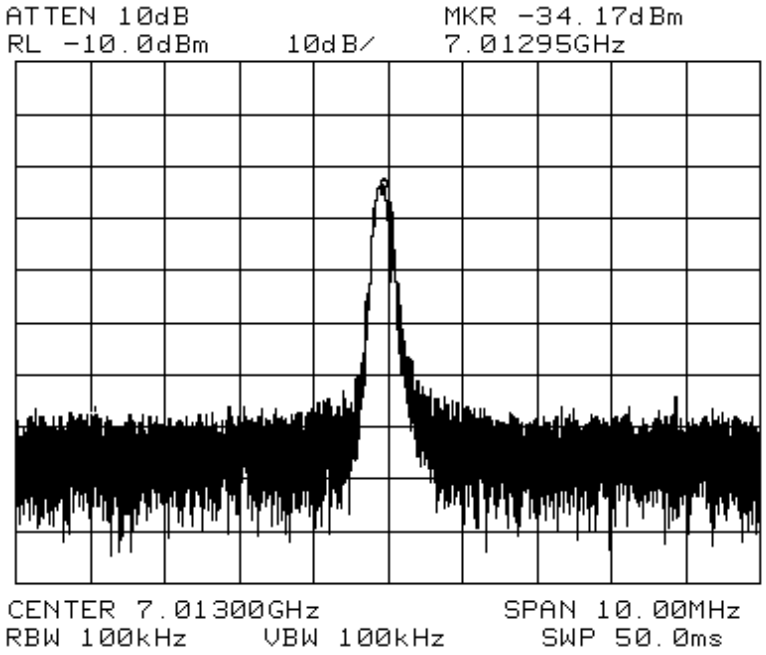


Figure 4.16: On board measurement of the VCO spectrum operating in the high frequency band with varactor control voltage = 1.8 V.

Phase-locked loop measurement results

The phase locked loop was able to lock in the 8.0 GHz band with a designed divider ratio of 80. Several phase-locked loop performance parameters; such as pull in range, hold in range, divider ratio and spectrum, were characterized. The procedure to measure the PLL circuit pull-in range is as follows: (1) set all the DC supply and bias voltages to the designed values; (2) set the power level of the reference signal source to 25 dBm and frequency to about 70 MHz; (3) adjust the input reference frequency slowly from 70 MHz and observe the VCO control voltage on the oscilloscope and the output spectrum on the spectrum analyzer until the phase-locked loop is in lock.

To observe the phase-locked performance, the reference frequency signal source had its output level adjusted to $\sim 25dBm$, and the prescaler PMOS load resistor was biased at $0.1V$ in its triode region. The power supply voltage for the phase-locked loop circuitry is set to the designed 1.8 V. The measured current consumption was $\sim 5.85\ mA$ for the switched VCO circuit block, and $\sim 11\ mA$ for the prescaler/divider circuit blocks. The phase detector and charge pump circuit block power consumptions

Hold-in/pull-in Frequencies	Reference (MHz)	VCO (GHz)	Ratio
Low end	74.07	5.9259	80.004
High end	82.00	6.5578	79.973

Table 4.5: PLL pull in and hold in frequencies.

are negligible.

While the reference frequency is much lower than the lower pull in frequency, the varactor control voltage should remain at the lowest supply voltage rail. While the reference frequency is above the hold in range, the varactor control voltage should remain at the highest supply voltage rail ($1.8V$) as the VCO is always trying to meet the higher reference frequency. As the reference frequency approaches the pull in range, the varactor control voltage starts to fluctuate as the loop tries to obtain lock. When the reference frequency is within the pull in range, the varactor voltage reaches constant value between 0 and $1.8V$ corresponding to the current input reference frequency. As the reference frequency moves inside the hold in range, the varactor control voltage changes correspondingly as the loop is trying to maintain lock. The VCO oscillation frequency also follows the control voltage so that the ratio of 80 between the reference frequency and PLL output frequency is maintained. Both the high-end and the low-end of the pull in range of the PLL were measured.

The measured hold-in/pull-in ranges are the same ($\Omega = \Omega_{HI} = \Omega_{PI}$) and cannot be differentiated during experiments. The measured VCO output spectra for the low-end and high-end pull-in/hold-in ranges are shown in Fig. 4.17 - Fig. 4.18. Note that the current injection of the charge pump ($\sim 80MHz$) leaks through loop filter circuit to the VCO output resulting in the sideband spurs adjacent the VCO resonant frequency. The sideband power levels measured on the spectrum analyzer are $\sim -27dBc$ at the lower edge and $\sim -35dBc$ at the higher edge of the pull-in range. Both the reference frequency and VCO output frequency for the pull-in/hold-in/lock-in ranges are summarized in Table 4.5. The pull-in/hold-in ranges are calculated to be:

$$\Omega = \Omega_{HI} = \Omega_{PI} = \frac{6.5578 - 5.9259}{2} = 0.315\,95GHz \tag{4.1}$$

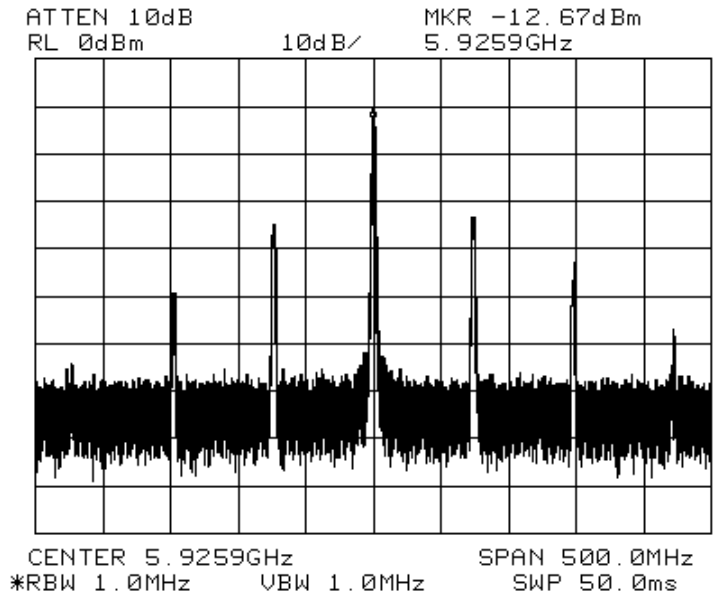


Figure 4.17: Phase locked VCO output spectrum at low end of its pull-in/hold-in range (f_{ref}=74.07 MHz, f_{VCO}=5.9259 GHz, Ratio = 80.004).

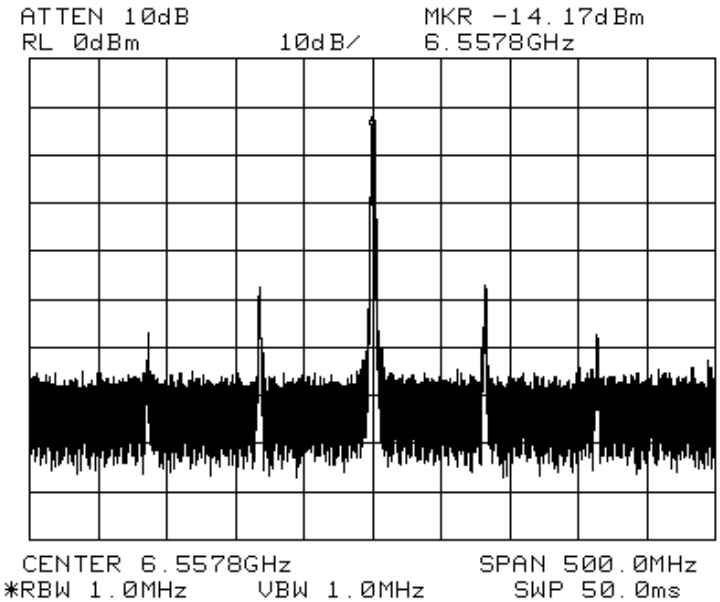


Figure 4.18: Phase locked VCO output spectrum at high end of its pull-in/hold-in range (f_{ref}=82.00 MHz, f_{VCO}=6.5578 GHz, Ratio = 79.973).

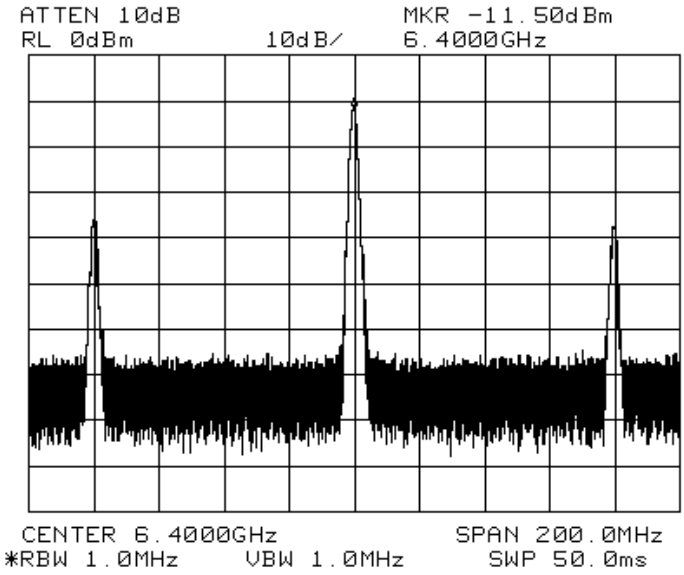


Figure 4.19: Phase-Locked VCO output spectrum with a center frequency of 6.4 GHz ($f_{ref} = 80MHz$, sideband at $\pm f_{ref}$).

Phase Locked VCO Spectrum The VCO output spectrum while loop is in lock is measured at a reference frequency of 80 MHz (Fig. 4.19) with frequency span of 200 MHz and band width resolution of 1 MHz. The VCO center frequency is at 6.4GHz (80MHz $\times$80) due to the divider ratio of 80. Spur levels may be reduced by employing larger capacitor after the charge pump circuit and reducing the bandwidth of PLL. As expected, the output spectra are much more stable compared to free-running VCO spectrum shown in Fig. 4.16 (Section 4.2.2). There are additional noise contributions from the phase detector/charge pump/loop filter/divider circuits. However, phase noise is much less problematic in the wide band system compared to the narrow band system. The total power consumption of the PLL is $30mW$.

Time Domain Phase-Locked VCO Measurement The time domain VCO output waveform is measured using Tektronix CSA8000 Signal Analyzer. The CSA8000 is a sub-sampling scope and takes samples of the signal during several periods to construct the actual waveform. Therefore, the trigger signal needs to have a phase relationship with the testing signal in order for the signal to be sampled correctly. This is the case when the phase-locked loop is in lock, where the VCO output is in

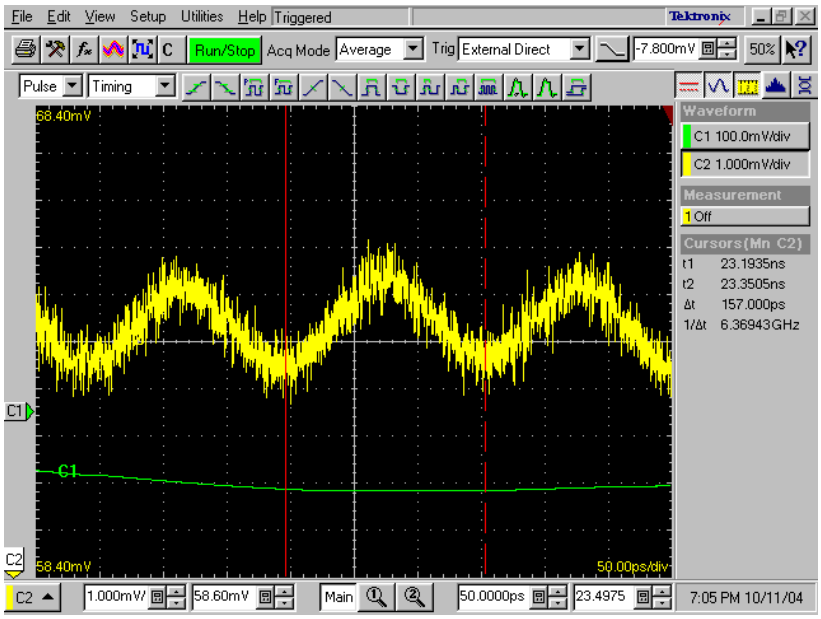


Figure 4.20: Time measurement of locked PLL using Tektronix CSA8000 Signal Analyzer (VCO is locked to 6.4 GHz, Time scale = 50ps/div Avg = 512).

phase with the reference input signal. Again, the frequency of 80 MHz is selected as the reference. In order to increase the signal visibility, averaging of 512 samples is selected in the signal analyzer so that noise due to jitters may be reduced. Note that if there is no fixed phase relationship between the trigger (reference frequency) and the testing signal (VCO output), averaging the signal will reduce the output to zero. Fig. 4.20 shows the VCO output signal in the time domain; the curve below is the reference frequency of 80 MHz. The waveform appears noisy since it is an overlap of multiple waveforms at different sampling time over a period of 256 ns.

4.2.3 Prototype Pulse Generator Measurements

The time domain VCO output waveform (with an input reference frequency of 80 MHz) was measured using an Agilent Infiniium DSO8124A real-time oscilloscope (Fig. 4.21). The measurement results show that the pulse duration is about ~6 ns, this corresponds to a bandwidth of > 300 MHz. The pulse duration is different from the design value of 4ns due to the fact that the reference frequency used in measurement is lower than the designed 100 MHz. Also the delay line used in the

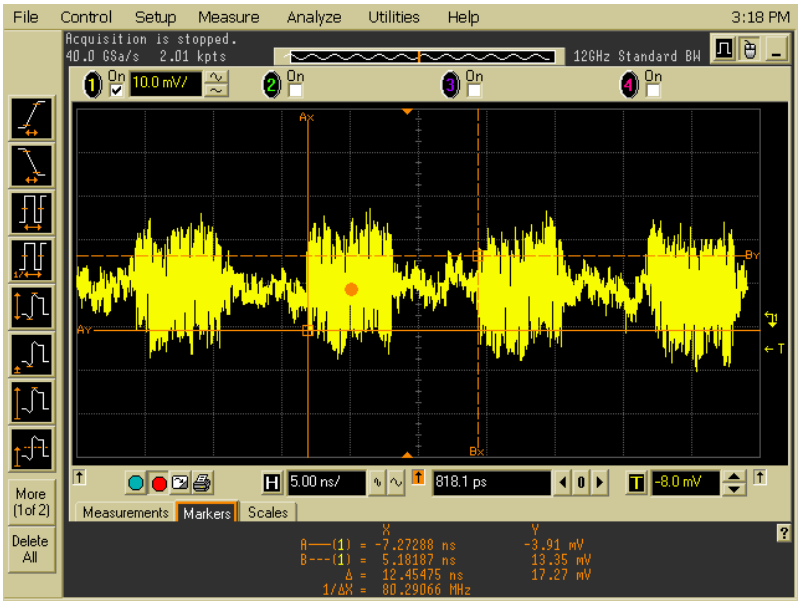


Figure 4.21: Measured gated output from the pulse generator in time domain (Pulse repetition frequency = 80 MHz) using real-time oscilloscope.

pulse generator is somewhat sensitive to process variations. This can be improved by using a digital logic based circuit to generate the desired pulse width as will be discussed in Chapter Five.

The pulse generator is designed to deliver the output pulse to a high input impedance transmit amplifier. This results in low amplitude in the measurement when the 50 Ω impedance from available test equipment is presented to the output of pulse generator. This impedance mismatch also loads the buffer amplifier of the VCO, further reducing the output power. The frequency domain measurement of the pulse generator with a constant data input is shown in Fig. 4.22. As expected discrete spectral lines are observed instead of continuous spectrum. An estimate of the first null bandwidth from Fig. 4.22 is about 320 MHz.

Table 4.6 compares the multiband PLL design with some recently published PLLs. This work implemented a PLL with wide tuning range from 4.8 to 8.0 GHz while remain relatively low power consumptions. The spur level due to the imperfect charge pump switching and possibly substrate coupling, this can be improved by careful well-matched design of the charge pump and layout. Table 4.7 compares the pulse generator design with some recently published pulse generators. The gated pulse

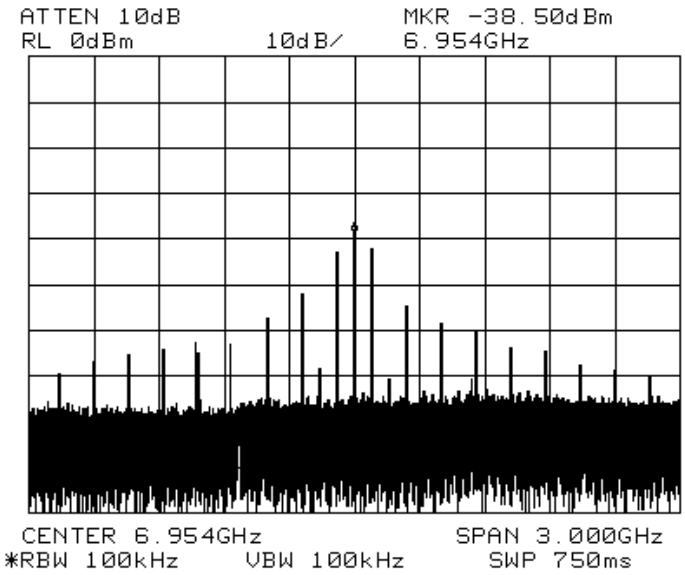


Figure 4.22: Measured gated output from the pulse generator in frequency domain (Pulse repetition frequency = 80 MHz).

PLL	Frequency	Spurs	Bandwidth	Tracking Range	Power
Herzel[59]	4.3 GHz	-43 dBc	-	600 MHz	50 mW
Craninckx[54]	1.8 GHz	-	45 KHz	-	51 mW
Tak[41]	6.3-9 GHz	-52 dBc	26 MHz	2.9 GHz	58 mW
This work	4.8-8.0 GHz	-27 dBc	3.76 MHz	316 MHz	34 mW

Table 4.6: Comparison to recently published PLLs.

approach has been used in various applications. In this work, it was intended for a proposed UWB transmitter architecture for wireless sensor networks where precise position location is a desired feature.

4.3 Summary

In this chapter, the layout and measurement results of the fabricated VCO and PLL are presented. The fabricated switched tank VCO design is capable of switching into the designed three frequency bands, with reasonable agreement with the simulations. The VCO tuning range is somewhat nonlinear and can be improved by an alternative switch structure as proposed in Section 2.4. The PLL is able to lock at the high

Pulse Generator	Type	Bandwidth	Technology
Han[57]	Impulse (300-800ps)	-	SRD/MESFET
Jeong[56]	Impulse (Mono Gaussian)	3.34 GHz (-3dB)	0.18μ CMOS
Gresham[60]	Gated (1n)	1.4 GHz (-10dB)	SiGe BiCMOS
This work	Gated (4n)	500MHz(null)	0.18μ BiCMOS

Table 4.7: Comparison to recently published pulse generators.

frequency band with an hold-in range of 316 MHz. The spur level of the PLL is about -30 dBc; this is due to the low-passed reference input through charge pump, or due to substrate coupling. However, given the extremely low emission mask of UWB transmitter required by FCC, this -30 dBc spur may not be an issue for UWB applications. The pulse generator measurement shows that a nanosecond-range pulsed UWB output is generated; however the pulse width is not accurate due to the delay line timing control circuit. This issue is addressed in an improved pulse generator design to be described in the next chapter. The contribution of this chapter is to provide detailed characterization of the designed prototype UWB transmitter and pulse generator architecture. This serves as the foundation for new design and improvements in the following chapters.

Chapter 5

A Modified RF CMOS UWB Transmitter

As discussed in Chapter Two, the originally proposed transmitter design employed a switched-tank VCO to realize multiband switching operation. Alternatively, the multiband operation of the UWB transmitter can also be realized by employing combinations of single sideband mixers, and possibly frequency dividers, driven by a fixed frequency PLL system. One such method of generating multiple carrier frequencies for MBOA UWB systems is shown in Figure 5.1 (as proposed in [61]). The three MBOA Band group one carrier frequencies are generated using two PLLs and one SSB Mixer. In this work, an alternative different multiband UWB transmitter also makes use of a SSB mixer and frequency dividers to generate the desired carrier frequencies [61][62][63]. Compared to the band switching PLL based multiband system, a SSB mixer based system is capable of very fast band switching speed, since there is no requirement for the PLL to resettle each time a band charges. In this chapter, the switched-tank VCO discussed previously is replaced by a single state LC tank VCO with improved performance. This single band UWB transmitter utilizes a fixed frequency VCO at 4 GHz as the center frequency (Figure 5.2). Concurrently, a new digital pulse generator is designed and integrated with the fixed frequency PLL circuits.

Another issue was that the high frequency source coupled logic (SCL) divider used in the prototype PLL presented in Chapter Three consumed over 10mA of current

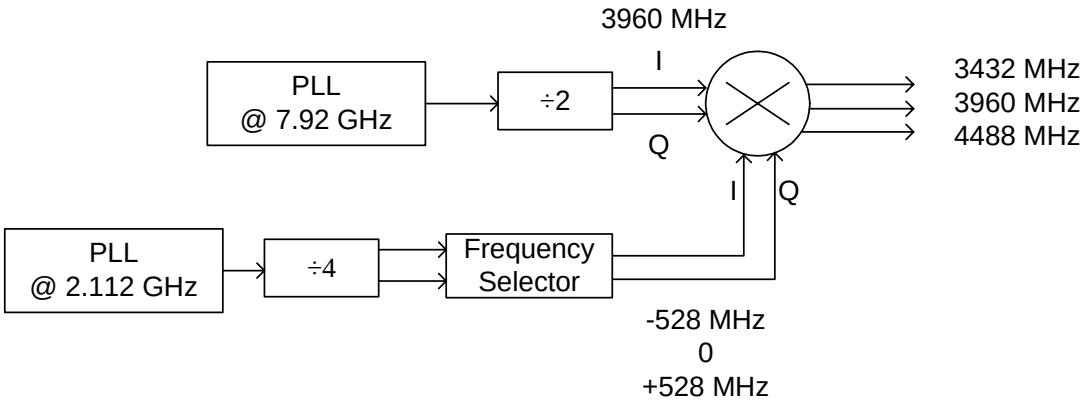


Figure 5.1: Multiple carrier frequency generation for MBOA band group one.

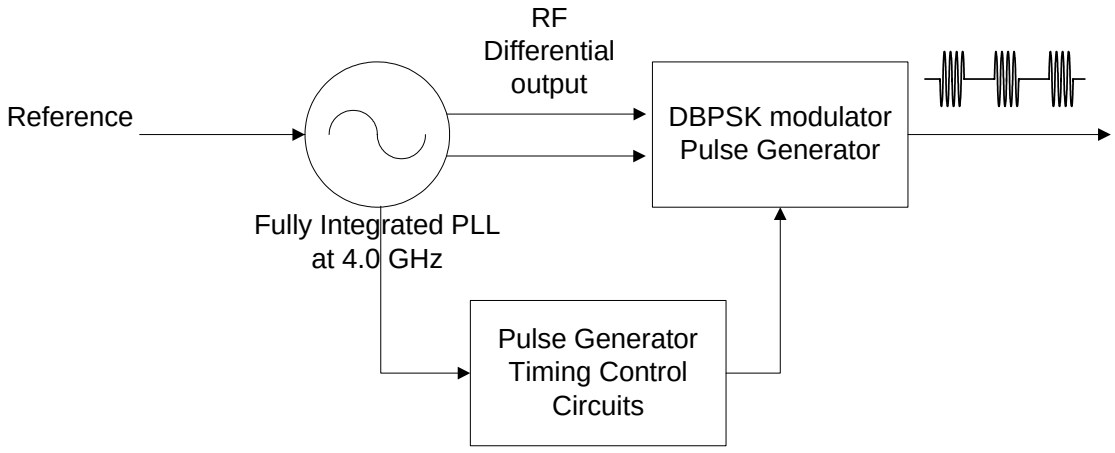


Figure 5.2: Modified UWB transmitter architecture with a fixed PLL center frequency of 4 GHz.

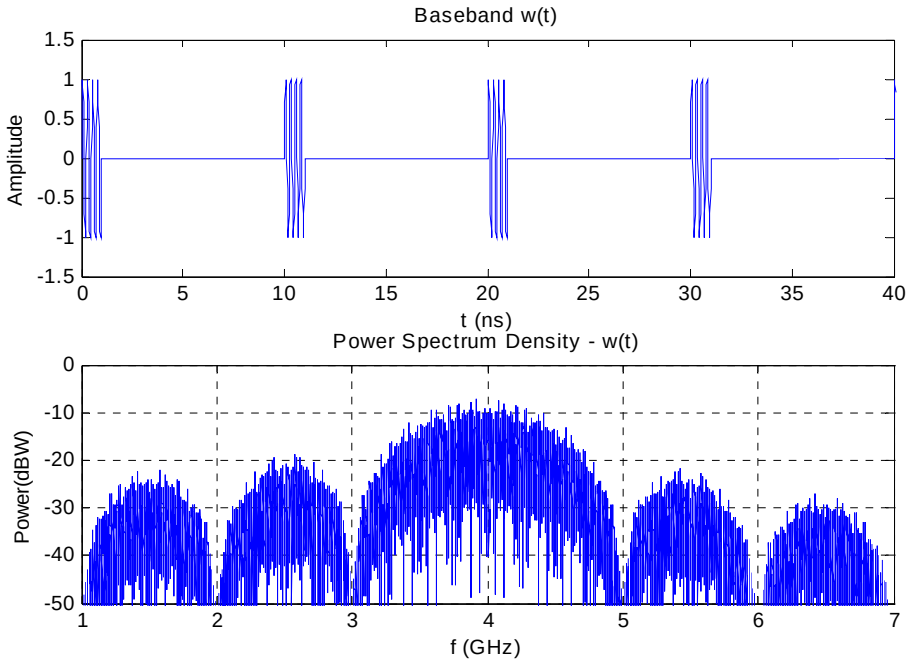


Figure 5.3: Matlab simulations of a transmitted DBPSK/BPSK pulse centered at 4 GHz in both time and frequency domain.

because of static current flow through the circuit. However, CMOS technology scaling has produced higher f_t devices with smaller gate capacitance, enabling high-speed digital dividers, based on, for example, dynamic logic, operating at reasonably high speed but less power. Such digital dividers are used in the PLL design in this chapter to reduce power consumption.

The previous pulse generator design used delay lines to generate the desired $4ns$ pulse width, suffering from timing issues arising from device mismatches. In this chapter, a new pulse generator circuit is developed to realize accurate timing control of the transmitted pulses. The pulse modulator encodes the DPSK/BPSK input data into short pulses with duration of 1ns. This gated pulse output signal corresponds to a $-10dB$ bandwidth of 1.5 GHz (Fig. 5.3). The next section discusses this new pulse generator design.

5.1 Digital Pulse Generator Design

A digital pulse generator was proposed in [64] to generate accurate timing control signals derived from the integrated VCO oscillating at 4 GHz. This pulse generator is composed of two parts: a CMOS transmission gate and a timing control circuit. The timing control circuit uses digital logic instead of delay lines to generate accurate pulse widths. Figure 5.4(a) shows the schematic diagram of the timing control logic. The $4GHz$ VCO output is first divided by a ratio of 8, down to $500MHz$. Then, the differential square pulses at 500 MHz are divided by 4 [Figure 5.4(b)]. The resulting waveforms at C and D are differential signals at $125MHz$ with a delay of $1ns$ relative to each other. After passing these delayed differential signals though an AND gate, a square pulse of $1ns$ pulse width and $8ns$ period is generated. Since the phase lock loop will stabilize the VCO output at $4.0GHz$, the pulse width of $1ns$ generated by the timing circuit will be very accurate and will result in precise UWB bandwidth control, insensitive to process, temperature and voltage variations.

Figure 5.5 shows the simulated timing control signal and transmitter output of the digital pulse generator. This all digital pulse generator consumes a power of only 0.6mW. To test the sensitivity of the digital pulse generator to device mismatches, the gate width of the devices are varied by $\pm 10\%$. As shown in Figure 5.6, this mismatch causes little change in the pulse timing control signals.To further evaluate the timing control pulse accuracy over the process variations and device mismatches, a Monte Carlo simulation was performed on the digital pulse generator circuit. The pulse widths taken between the falling and rising edges are calculated and plotted in Fig. 5.7. This result shows that the generated pulse widths are distributed around two centers: one located at 0.98ns with $\sim 70\%$ probability, and the other located at 0.89ns with $\sim 30\%$ probability.

This bimodal distribution is mainly due to the reset timing relative to the rising/falling edge of the waveform at Node A(B) in Fig. 5.4. Considering Fig. 5.8 two cases can be seen: (i) if reset is switched off *before* a rising edge at Node A, then waveform at Node C toggles its state before Node D which toggles at the rising edge of B. The pulse generator output is at Node E; (ii) if reset is switched off *after* a rising edge at Node A, then Node D toggles its state before Node C, and the waveform is shown as C′ to E′. If the two paths in Fig. 5.4 are perfect symmetrical, then this is

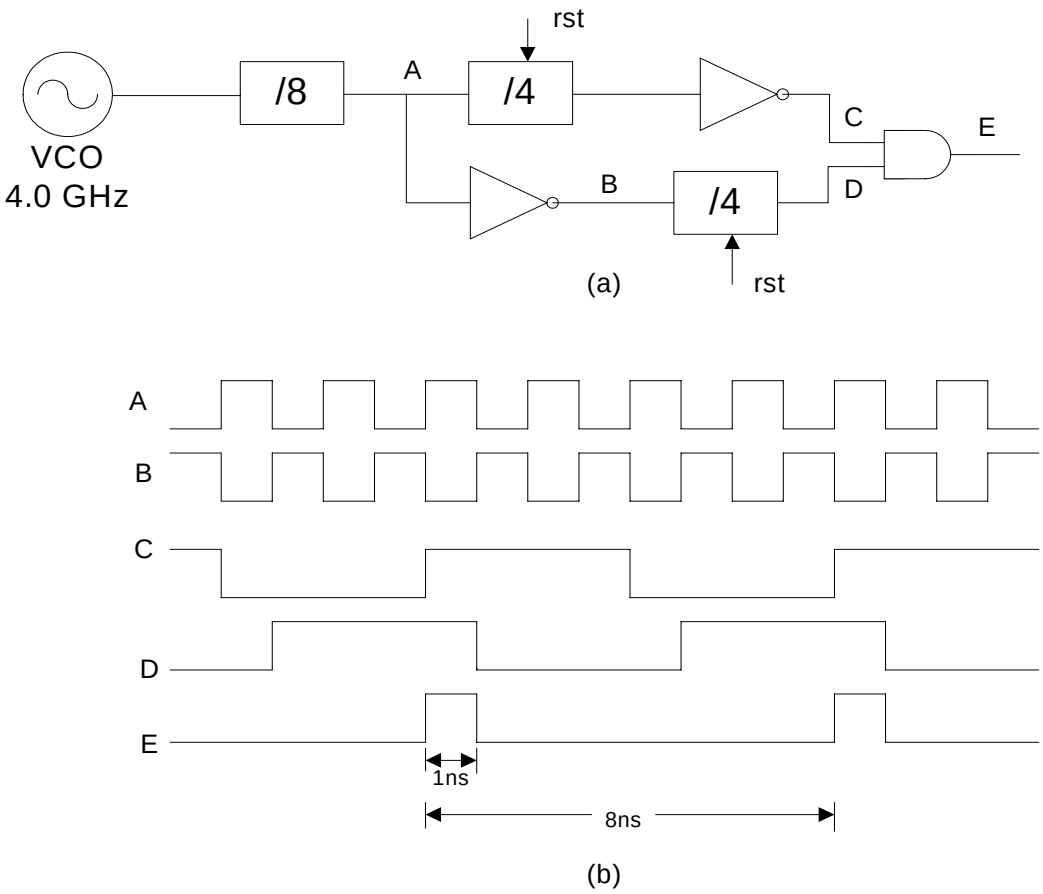


Figure 5.4: Pulse generator timing control unit (a) Schematic diagram of the control logic (b) timing sequence of the control logic.

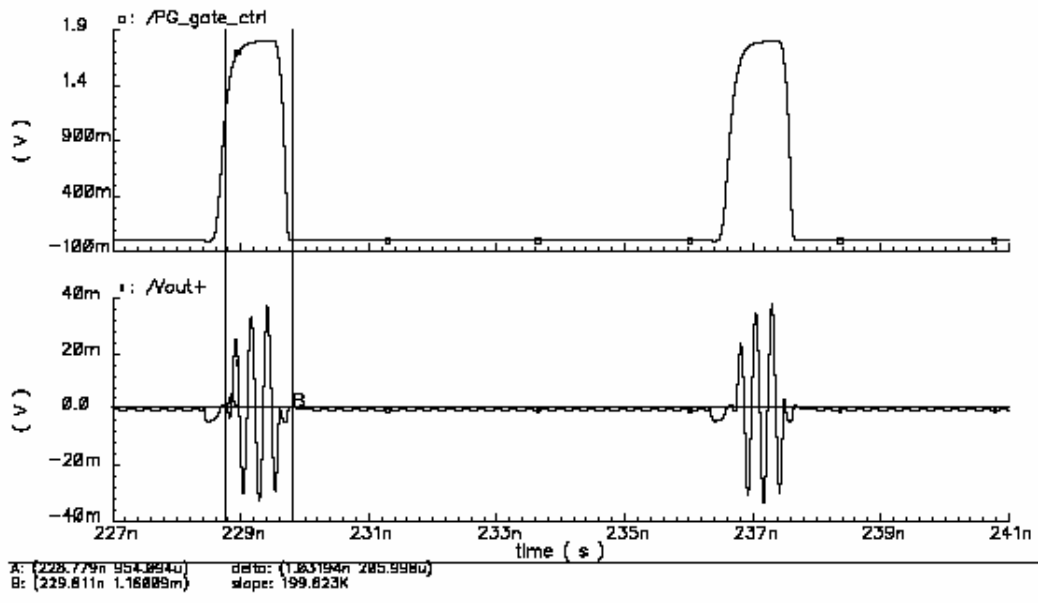


Figure 5.5: Simulated pulse generator timing control signal and transmitter output signal.

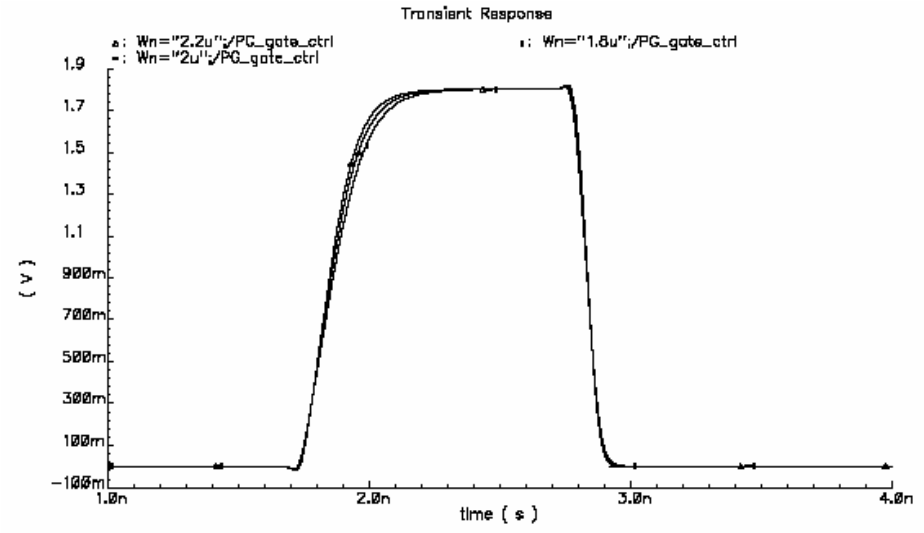


Figure 5.6: Timing control pulse of the all digital pulse generator with device width mismatches.

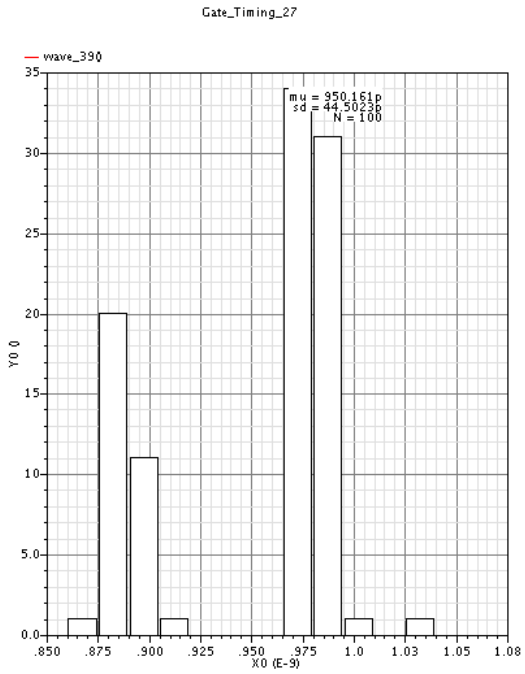


Figure 5.7: Monte Carlo simulation results of the digital pulse generator plotted as a histogram.

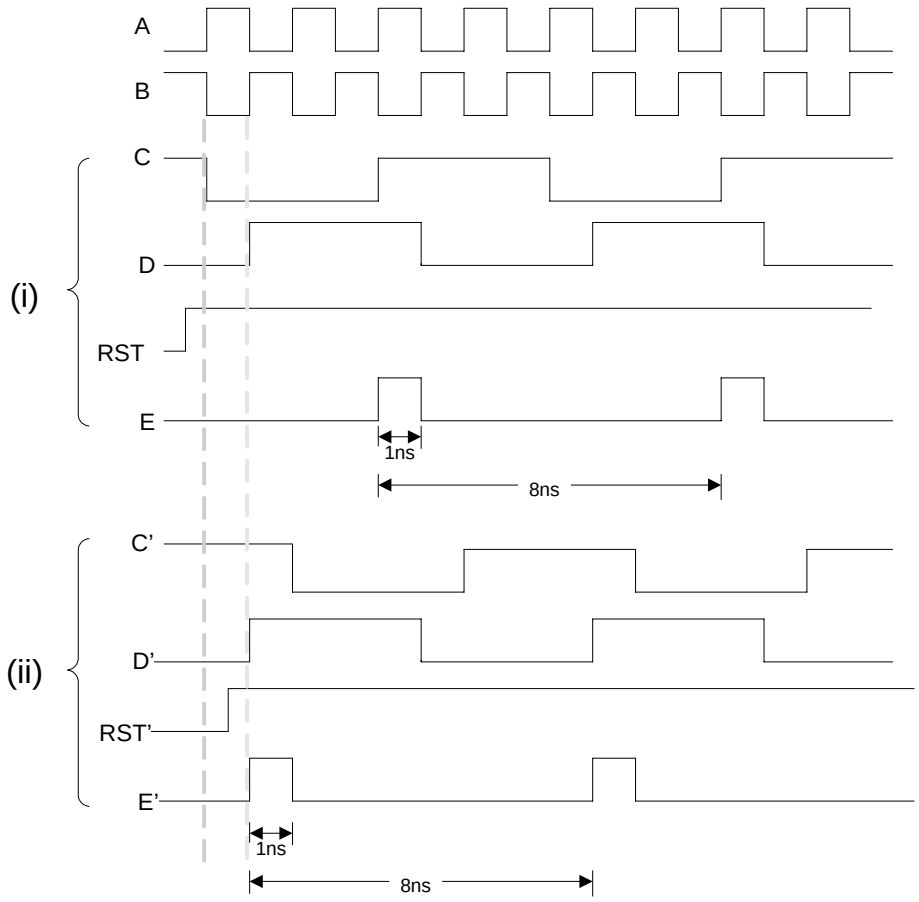


Figure 5.8: Two possible scenarios of the pulse generator output due to reset timing: (i) Reset before rising edge, (ii) Reset after rising edge.

not a problem since 1ns pulse timing control signal is generated with arbitrary start timing. However, due to the mismatch between the two signal paths, the pulse width generated can be slightly different as observed in Fig. 5.7.

The pulse width difference due to the reset timing can be solved by adding a detection circuit in the reset path to the dividers. Before the reset is switched off for both dividers in the two paths, an edge detection circuit is engaged to ensure that reset to the dividers is only turned off after a rising edge. This edge detection circuit is built using edge triggered flip flips. With this edge detection circuit, the pulse generator is resimulated using Monte Carlo in Cadence. The results show that by ensuring that the pulse generator is operated as C′-E′ in Fig. 5.8, the pulse widths can be maintained in a tight range around 0.98 ns (Fig. 5.9).

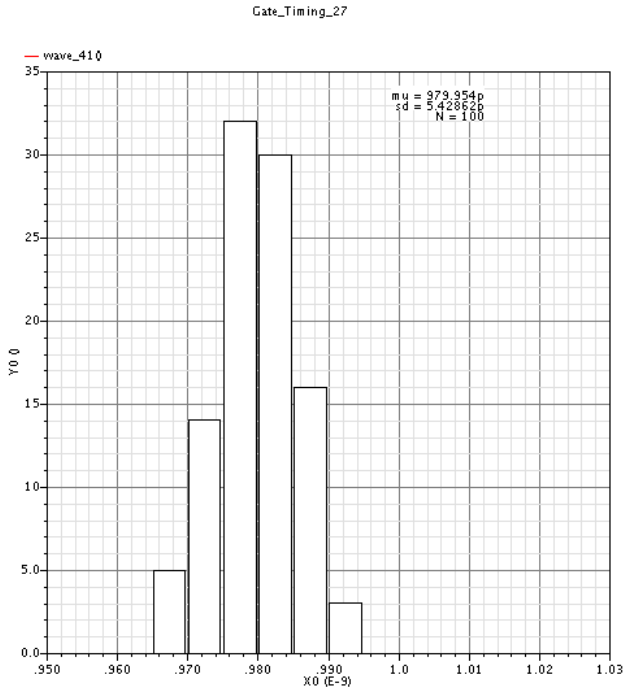


Figure 5.9: Monte Carlo simulation results of the digital pulse generator with edge detection circuit plotted as a histogram.

5.2 4 GHz Carrier Frequency Generation

The 4GHz carrier frequency is generated by a negative G_m VCO in a phase locked loop. As with the previous design in Chapter 3, this Type 2, 3rd order PLL consists of a high-speed CMOS phase/frequency detector (PFD), a CMOS charge pump, and a passive loop filter. A frequency of 31.25 MHz was chosen as the input reference. A schematic of this PLL is shown in Figure 5.10. Since the loop filter generally occupies a large amount of the chip area, the PLL is designed to have a wide loop bandwidth so as to minimize the loop filter capacitance. A large loop bandwidth helps filter out the VCO noise, but passes more input noise. A frequency divider with a ratio of 128 converts the VCO output frequency to the proximity of the input reference frequency (31.25 MHz) and thus aids in acquisition of the PLL. A negative -G_m VCO, based on NMOS devices for the active circuit, generates the center frequency of 4 GHz. As mentioned in Chapter 3, the phase noise requirement of the VCO design here can be relaxed due to the fact that VCO phase noise below the loop bandwidth is significantly attenuated by the PLL. Therefore, the main effort for the VCO design is to reduce its power consumption while maintaining reasonable amplitude so as to drive a subsequent prescaler. The output from the VCO is coupled out via a differential source-follower buffer stage to divider and pulse generator. The buffer isolates the VCO from subsequent stage loading as well as level shifting the DC level from 1.8V to 0.9V for the prescaler input. The differential outputs of the VCO pass through transmission gate switches controlled by the digital pulse generator timing control circuit. The designed transmitter output is a 1ns gated differential signal at a 4 GHz carrier frequency.

5.2.1 Frequency Dividers

There are different types of prescalers prevalent in the literature including source coupled logic[65], true single phase clock logic[66], and dynamic logic[65]. Of these options TSPC logic does not consume static current, so it has the lowest power consumption, but a lower maximum operating frequency. However, a TSPC logic divider can operate up to several GHz when optimized with technology scaling. The SCL logic used in the previous design (in Chapter 3) is the fastest divider, and it does not require input to be full swing since it is able to detect differential input signals,

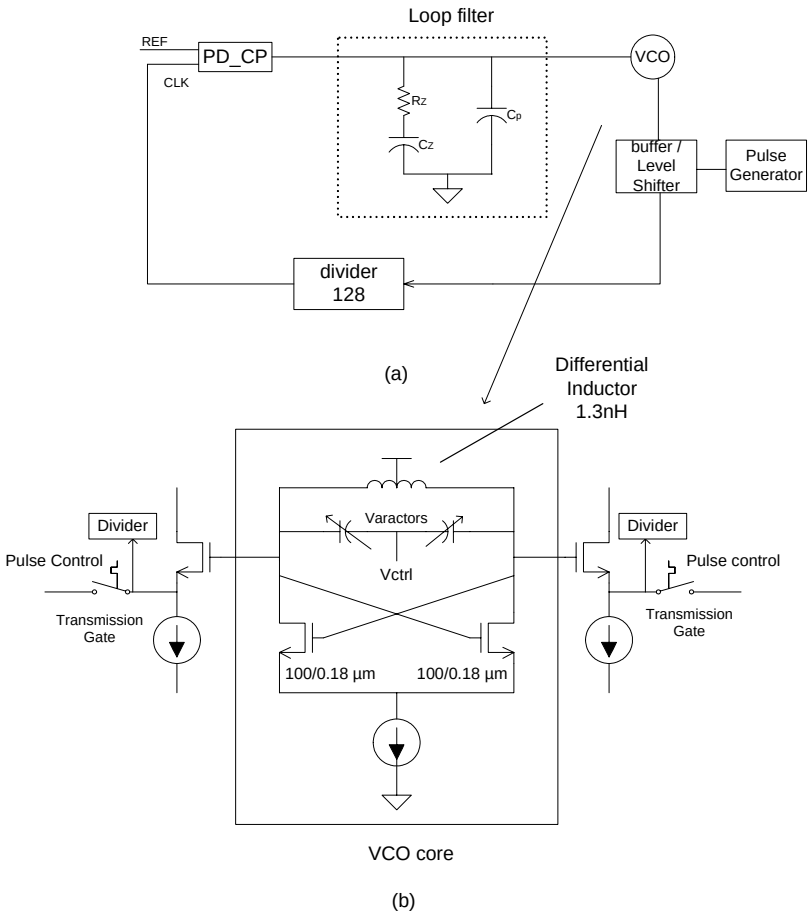


Figure 5.10: Conceptual schematic of the proposed (a) PLL and (b) VCO core.

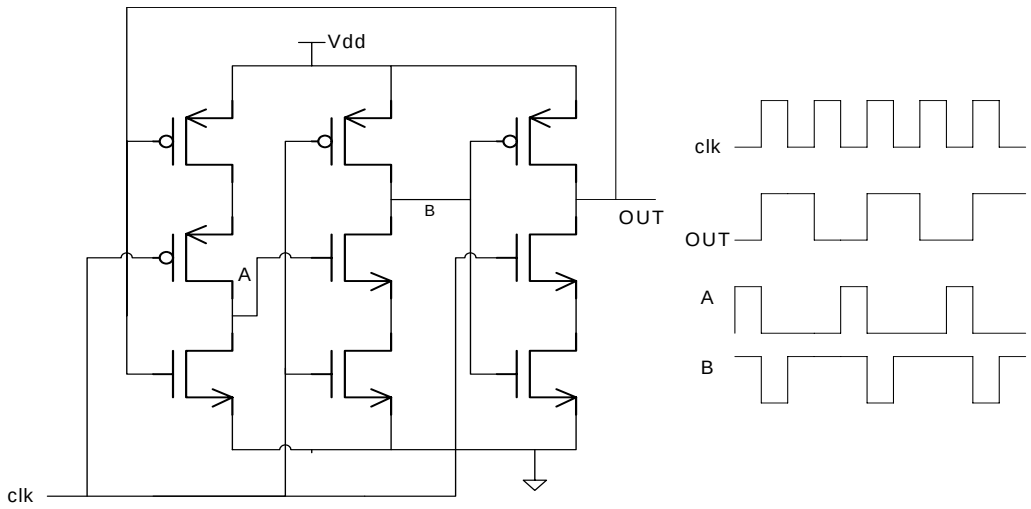


Figure 5.11: TSPC logic prescaler (a) Schematic diagram; (b) timing diagram.

but it requires significantly more current.

The modified CMOS UWB transmitter design in this chapter utilizes the TSPC logic in the PLL prescaler and the pulse generator circuit (Fig. 5.11). The TSPC logic prescaler in this design has a total of 9 transistors [Figure 5.11 (a)]. Three of these TSPC stages are connected sequentially to have a divider ratio of 8. The simulated results show that the TSPC prescaler is capable of operating up to 6 GHz while consuming a current of $\sim 0.25mA$ (each stage). The power consumption is mainly due to the dynamic power dissipation when transistors switch states. Only single ended inputs are required for TSPC logic, and the swing level should be relatively high such that logic is functional.

The TSPC logic divider has three inverters controlled by an input clock. The operation of the TSPC is shown in Figure 5.12. To simplify the analysis of the circuit, the clock controlled transistors are replaced by either short or open circuits. At clock low, the node B is precharged to high state, node OUT stays at its previous value, and node A is the inverted value of node OUT. At clock high, there are two different outcomes: if node A is high, then node B switches low and node OUT is charged to high which in turn grounds node A to low; if node A if low, node B stays high and node OUT is grounded to low while node A remain its previous value. Since node A only switches the state of node B once every two clock rising transitions, the

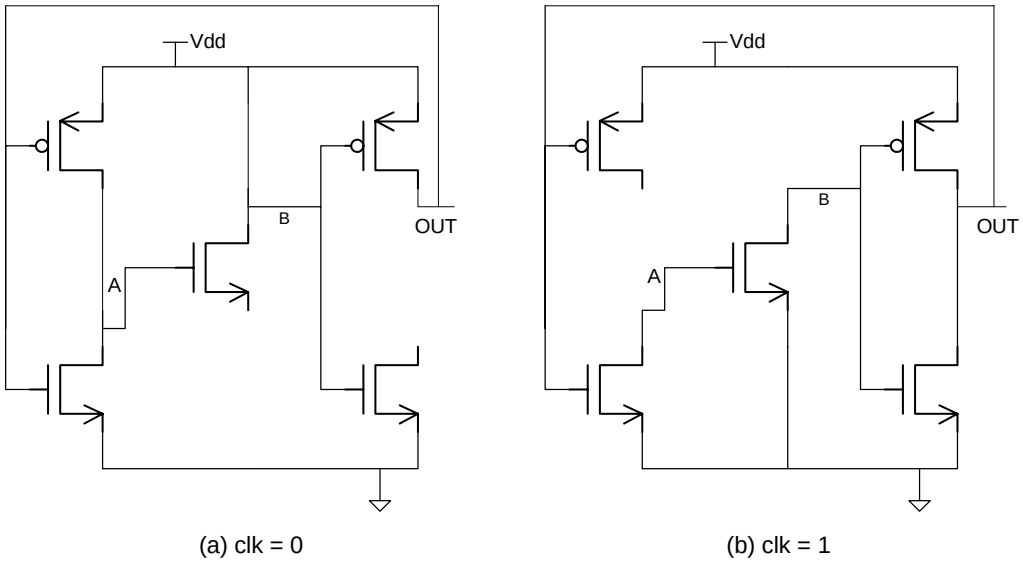


Figure 5.12: Detailed operation of a TSPC divider. Clock controlled transistors are replaced by either short or open circuits.

divide-by-2 operation is realized at node OUT.

As the input frequency increases, the delays at A in Figure 5.11 (b) become significant and the transistors do not have enough time to switch. Simulation results show that the divider design is capable of operating only up to 6.4 GHz; however, this leaves sufficient room for operation with 4 GHz input. The simulated output of a TSPC divide-by-2 divider is shown in Figure 5.13. The top graph shows the input clock at 4 GHz and divider output at 2 GHz. The divider remains functional as the input amplitude to the divider is varied from 0.1V to 0.5V. The bottom graph in Figure 5.13 shows the harmonics (4 GHz and 2 GHz) at the divider output. As the input amplitude increases, the amplitude of the frequency component at 2 GHz increases slightly while the feed through of the 4 GHz clock input drops slightly. This indicates that the divider output is not that sensitive to the input voltage amplitude variations, and an input level of 100mV is sufficient for the divider to function correctly.

5.2.2 Negative - G_m VCO

The simulated quality factor of the varactor ranges from 24 to 80 for its full tuning range. These values are significantly higher than the available on-chip inductors

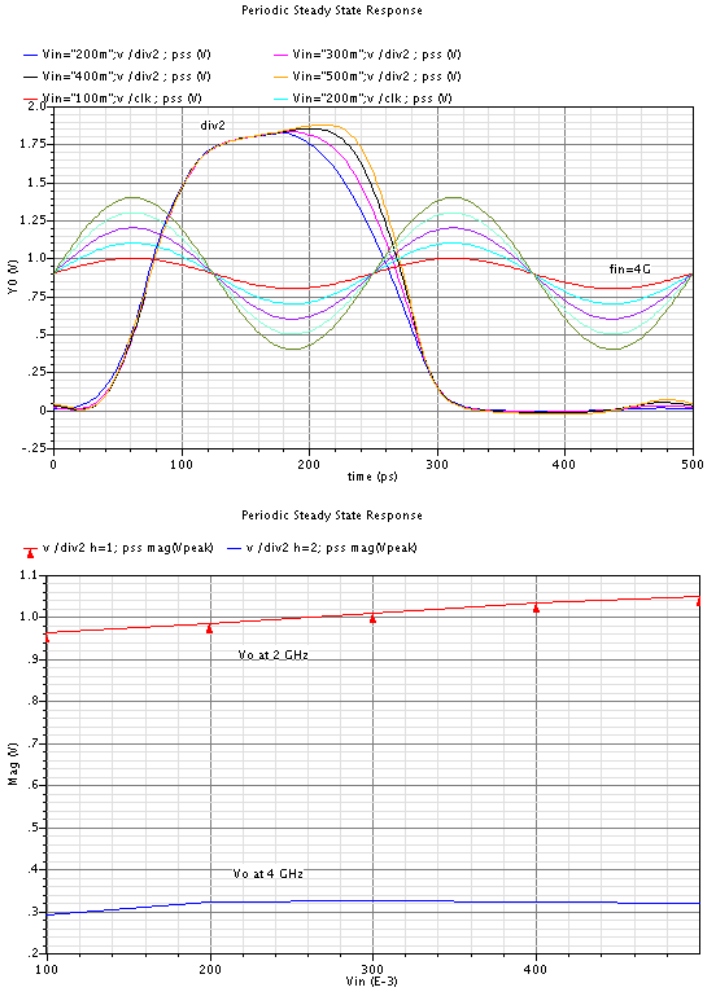


Figure 5.13: Simulated output of the TSPC prescaler at an input of 4 GHz.

at the frequencies of interest. A capacitor value of 0.78pF with Q of 30 gives an parallel equivalent resistor value of 1.5kΩ. Since there are two back-to-back varactors connected between the differential outputs of the VCO, the equivalent differential resistance of the varactors is about 3kΩ. Meanwhile, the differential inductor used in the design has a simulated differential inductance of 2.5nH with a Q of 8.5 at 4 GHz. Its equivalent series resistance 7.5Ω, and its equivalent parallel resistance is approximately 550Ω. Therefore, the loss of the VCO LC tank is dominated the lower-Q inductor. The differential MOSFET pair has a transconductance value of 12mS, which is converted to a negative resistance of -167Ω. This is sufficient to ensure VCO start up. The simulated results in Figure 5.14 show the DC bias current of the VCO (top graph) and differential output amplitude (bottom graph). The output of the VCO can be approximated as $V \sim I_{dc}R_p$. Because the designed frequency divider requires a voltage of about 100mV to function correctly, a bias current of 1.6mA is chosen for the VCO, corresponding to an output amplitude of $\sim 300mV$. The VCO output spectrum and phase noise simulation results when biased at 1.6mA are shown in Figure 5.15. The phase noise is not optimized since it is not as critical for a wideband system as narrow band systems, besides the VCO phase noise is high pass filtered by the wideband PLL. Instead, the design has low current consumptions without compromising VCO performance.

The buffer amplifier for the VCO output is built using source follower [Fig. 5.10 (b)], which provides high input impedance, low output impedance and near-unity gain. The buffer also serves as level shifter that convert the VCO output DC level from 1.8V down to 0.9V for the prescaler input. The size of the buffers are estimated using $MOS\ I-V$ equation and determined through simulation.

5.2.3 Complete Transmitter Simulation

The initial design of the PLL was again based on Matlab phase domain simulation. The PLL has a simulated bandwidth of 1.6 MHz and damping factor of 0.7. The Cadence circuit schematic is shown in Fig. 5.16. The SpectreRF simulation of the modified 4 GHz PLL is shown in Figure 5.17. The simulation of PFD inputs and outputs, plus the VCO control voltage, are displayed in the transient simulation results. The lock time is not as critical since the PLL does not need to retune;

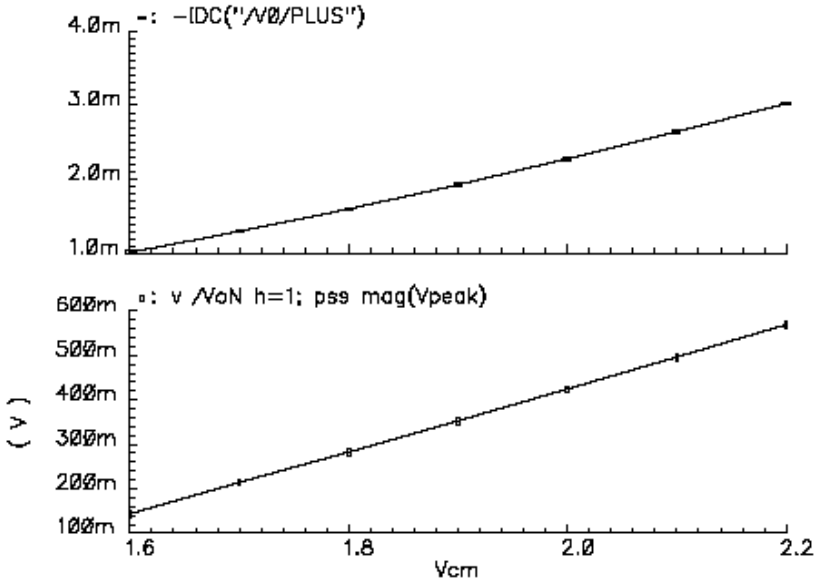


Figure 5.14: Simulated DC bias current and output amplitude of the VCO (V_{cm} is the bias control voltage).

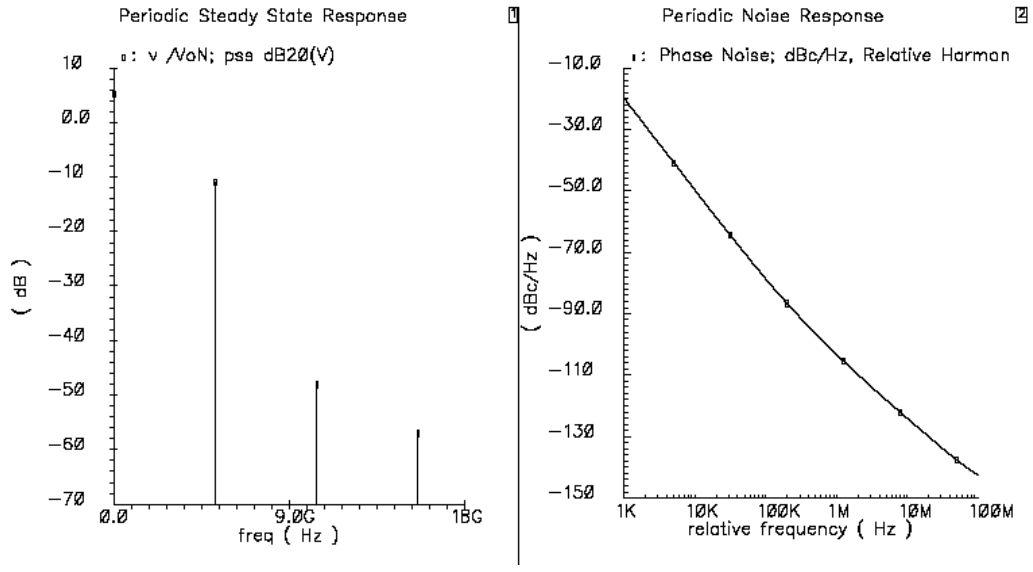


Figure 5.15: Simulated results of VCO output spectrum and phase noise.

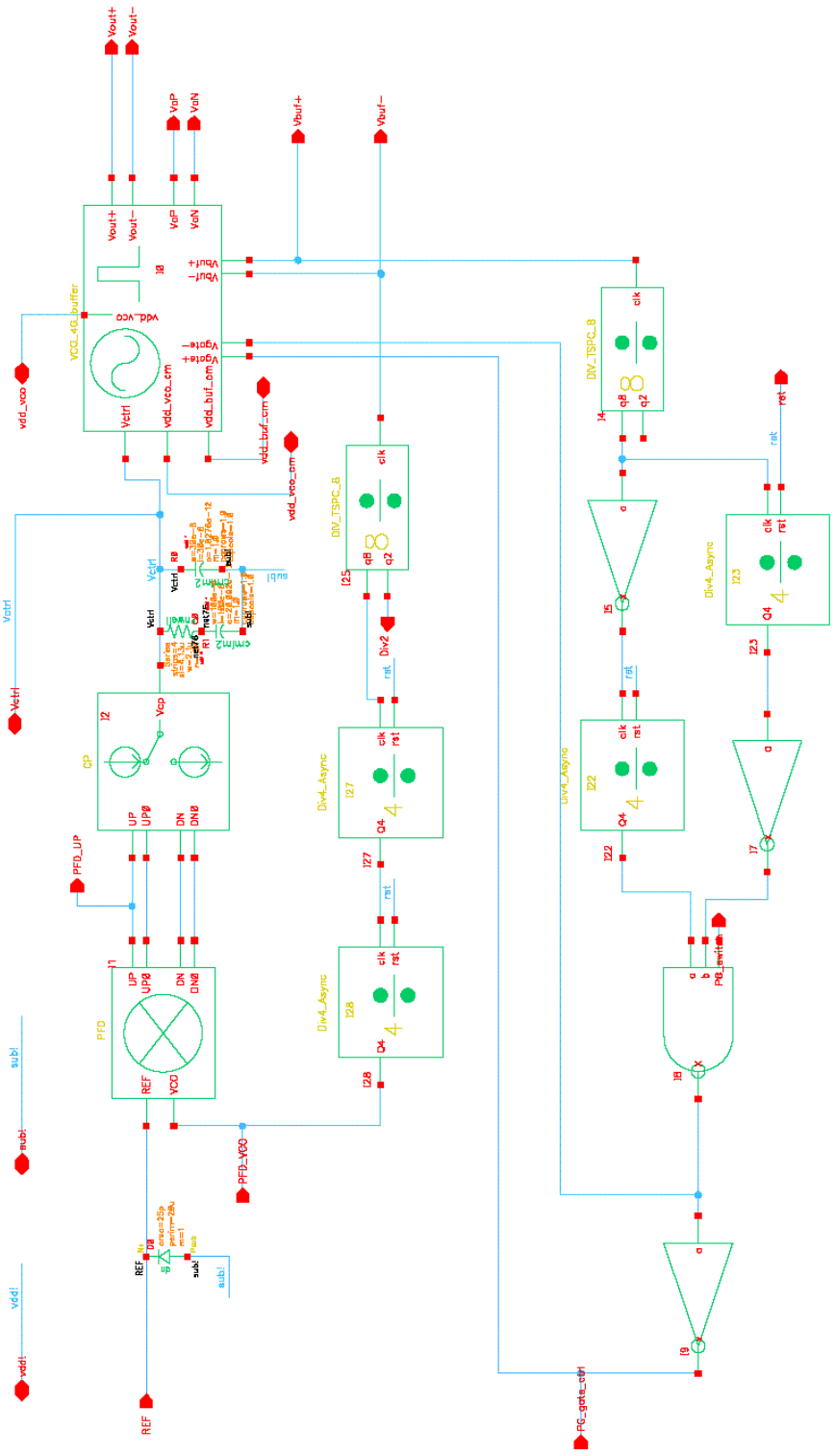


Figure 5.16: Schematic of the 4 GHz transmitter with novel pulse generator.

Pin Name	Function	Pad Type
$V_o(+/-)$	Differential VCO output	RF
$V_{pulse}(+/-)$	Differential pulse output	RF
$DIV2$	Divider output	RF
REF	Reference frequency input	RF
$PFD\_{}_{VCO}$	Divided VCO output	RF
$PFD\_{}_{UP}$	Phase detector output	RF
$PG\_{}_{gate}$	Pulse generator timing control	RF
V_{ctrl}	VCO tuning voltage	RF
$V_{dd\_vco\_cm}$	VCO bias control	DC
$V_{dd\_buf\_cm}$	Buffer bias control	DC
rst	Digital reset	DC
V_{dd}	Digital supply voltage	DC
PG_sw	Pulse generator switch	DC
V_{dd_vco}	VCO supply voltage	DC

Table 5.1: Complete transmitter pin assignment.

nonetheless, the simulation shows that the PLL takes $\sim 1.0\ \mu s$ to acquire lock.

The simulated UWB transmitter time domain output waveform is shown in Figure 5.18. This figure displays the pulse generator control signal, the divider output, the VCO output and the transmitter output. The VCO has an output swing of 300 mV. The simulated pulse generator outputs a 1 ns gated pulse every 8 ns, as intended.

5.3 Layout and Measurements

The modified UWB transmitter was designed using Jazz Semiconductor's $0.18\mu m$ $CMOS\ CA18HR$ process. The complete layout of the 4 GHz UWB transmitter occupies an area of $1.020mm \times 0.940mm$ including pads (Fig. 5.19). The fabricated die is intended to fit a $3\times3mm^2$ 16 pin QFN package. There are a total 18 wirebonding pads with standard pitch of $150\mu m$. Two of the pads are used for ground connections and are down bonded to the package die flag. Of the remaining 16 pads: 6 pads are used for DC power supply and control signal; 4 pads are used for RF output signals; 5 pads are used for low-to-medium frequency probing; and 1 pad is used for reference signal input. Table 5.1 lists the pads with their types and functions.

The die photo of the UWB transmitter is shown in Figure 5.20. It is packaged in an

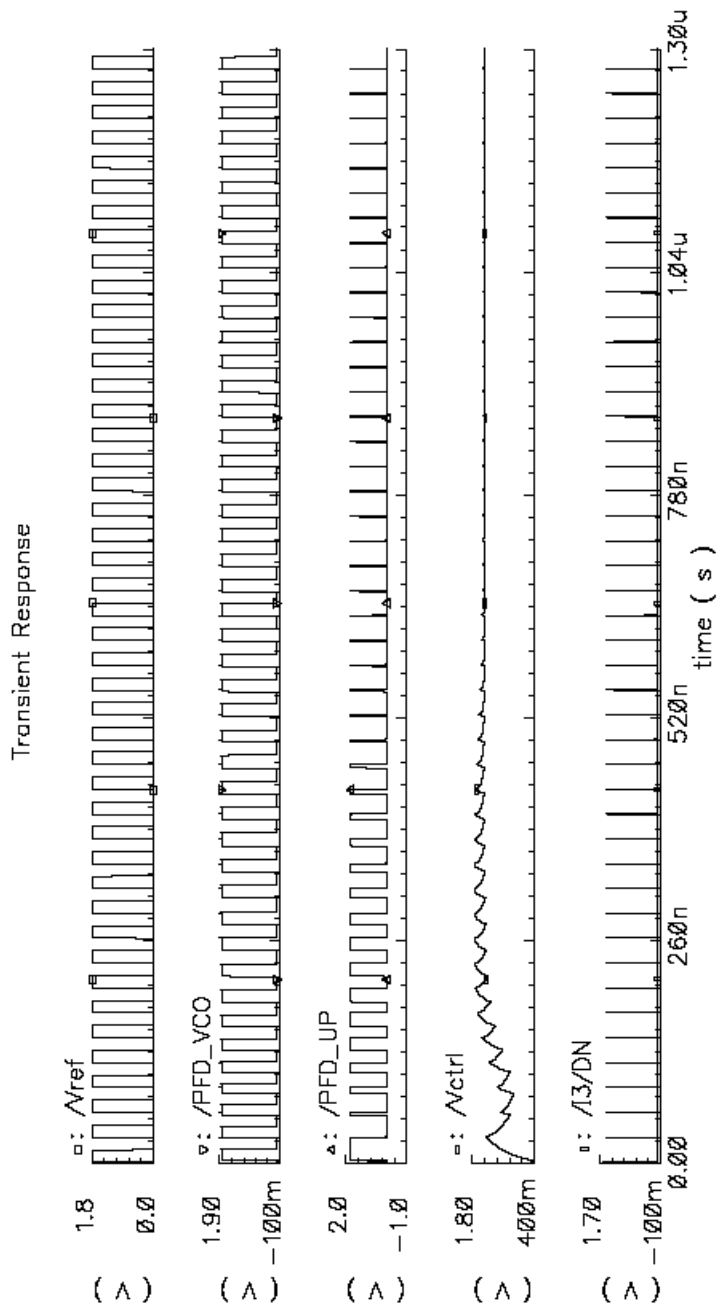


Figure 5.17: Simulated output waveforms of VCO control signal and phase detector inputs from 4 GHz PLL.

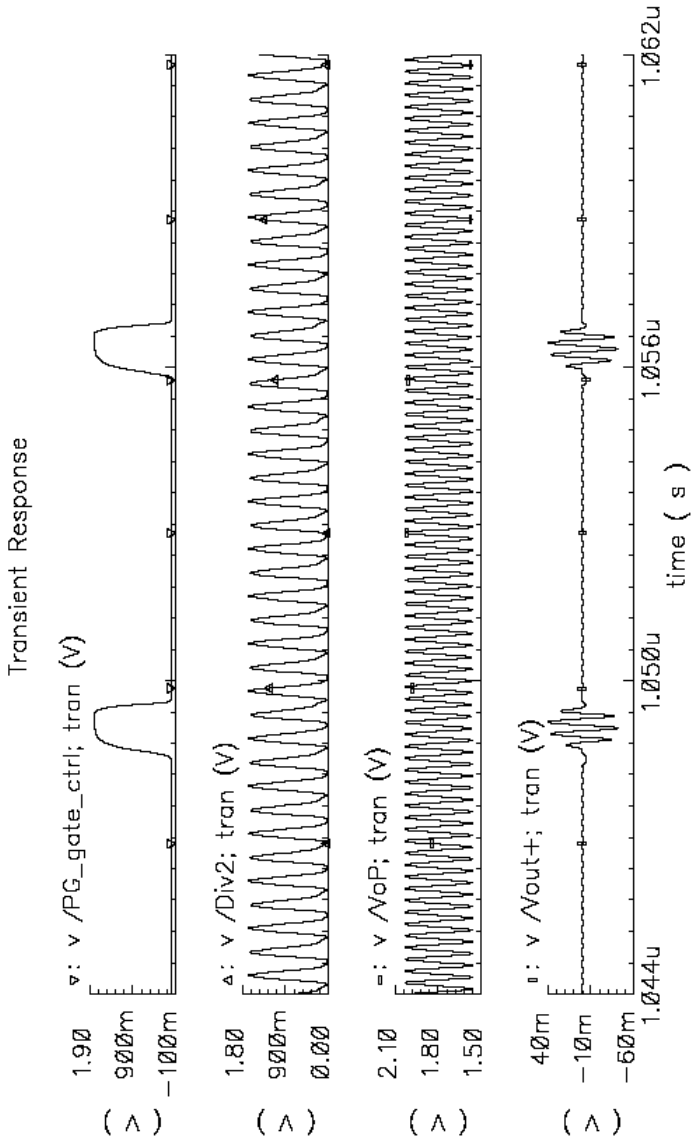


Figure 5.18: Simulated time domain waveforms of VCO output, divider, and pulse generator output from the 4 GHz UWB transmitter.

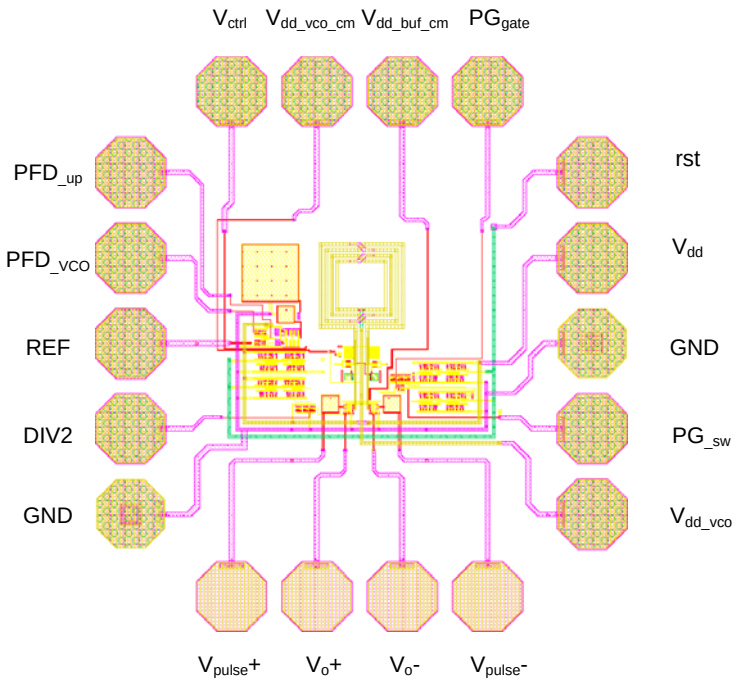


Figure 5.19: Layout of Modified UWB transmitter with 4 GHz fixed PLL.

open QFN package (16 pins, $3{\times}3mm^2$), and then mounted on a custom built testing board (Fig. 5.21) This board has a dimension of 3.51 inch (89 mm) $\times$ 2.48 inch (63 mm). The measured VCO output spectrum at the high end of its tuning range is shown in Figure 5.22. The VCO has an output power of -6.5 dBm at 5.0 GHz which is in the operating range of the prescaler.

The time domain pulse generator control circuit output waveform while the VCO is oscillating at 4.05 GHz (close to its low frequency end) was measured using an Agilent Infiniium DSO8124A real-time oscilloscope. The measured output waveform from the pulse generator timing control circuit and the gated pulse output (Figure 5.23) confirm the designed 1ns gating pulse is generated by the digital logic. Figure 5.24 shows the differential output gated pulses. The measured gated pulse width is indeed $\sim 1ns$, with a PRF of $\sim 8ns$. Note that the pulse starts with the same phase as that of the VCO for each cycle. The apparent VCO feed-through at the pulse generator output may possibly be due to coupling through the area fill tiles and the substrate. This could potentially be reduced by placing the critical components inside an isolated well and removing the area fill tiles above them.

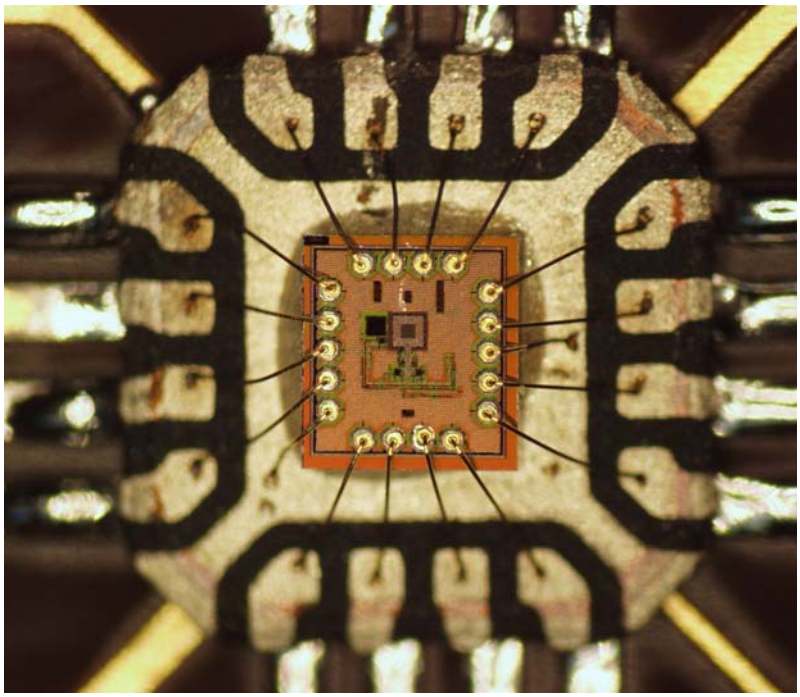


Figure 5.20: Die photo of the CMOS UWB transmitter.

The pulse generator control voltage in Figure 5.23 is distorted from an ideal square wave shape. This is due to loading effect at the output of the pulse generator, rather than mismatches inside of the digital pulse generator. A measurements of the pulse generator gate control signal (after an inverter) without loading switches is shown in Fig. 5.25. The gated signal is the pulse generator control and the other waveform is the VCO output. As can be seen, the pulse generator control signal without loading is very close to square wave form. To improve the pulse generator gating control waveform in the presence of loading, a buffer stage should be inserted between its output and the load.

5.4 Summary

This chapter presents an improved the UWB transmitter circuit with a new digital pulse generator capable of highly accurate $1ns$ pulses. Since the timing control information is designed to be derived from a phase locked VCO, it is not sensitive to

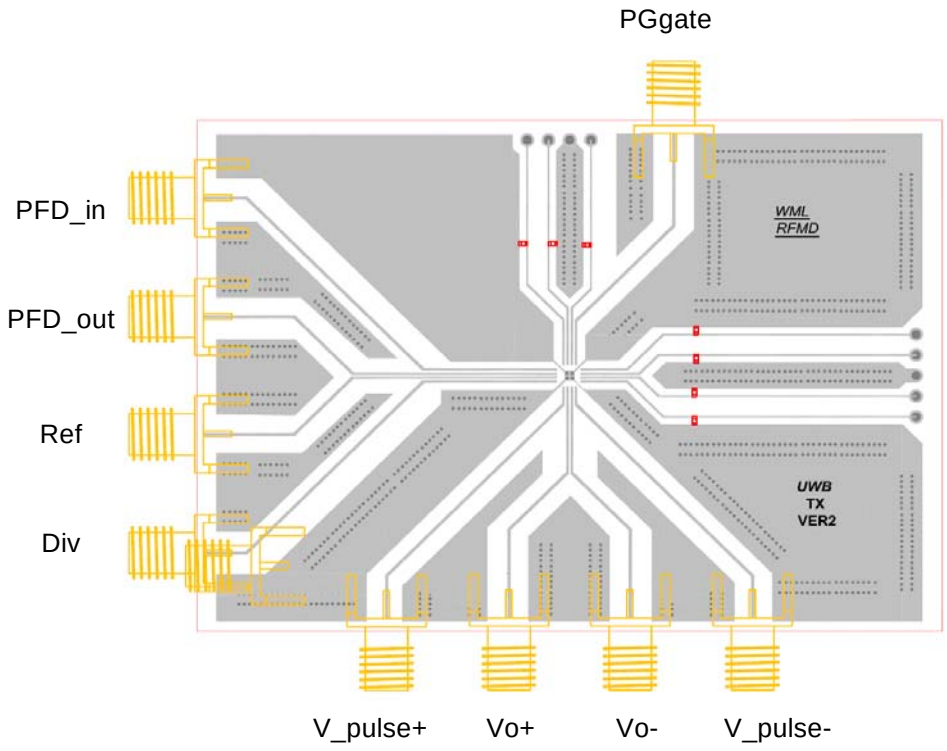


Figure 5.21: Layout of the custom testing board for the modified UWB Tx design.

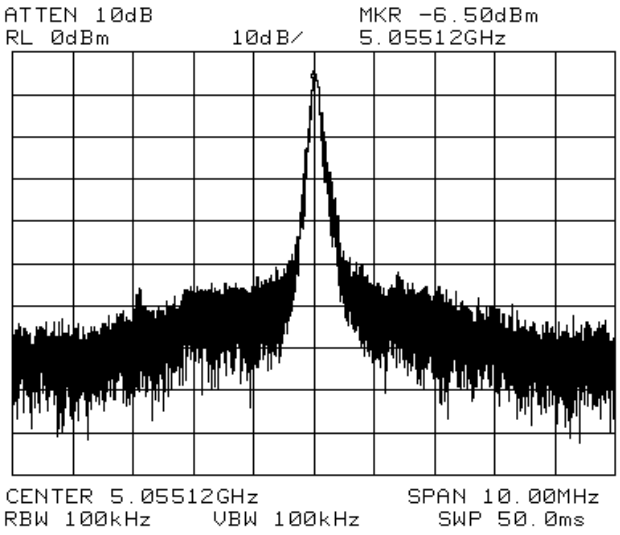


Figure 5.22: Measured VCO output spectrum at its high end of the tuning range.

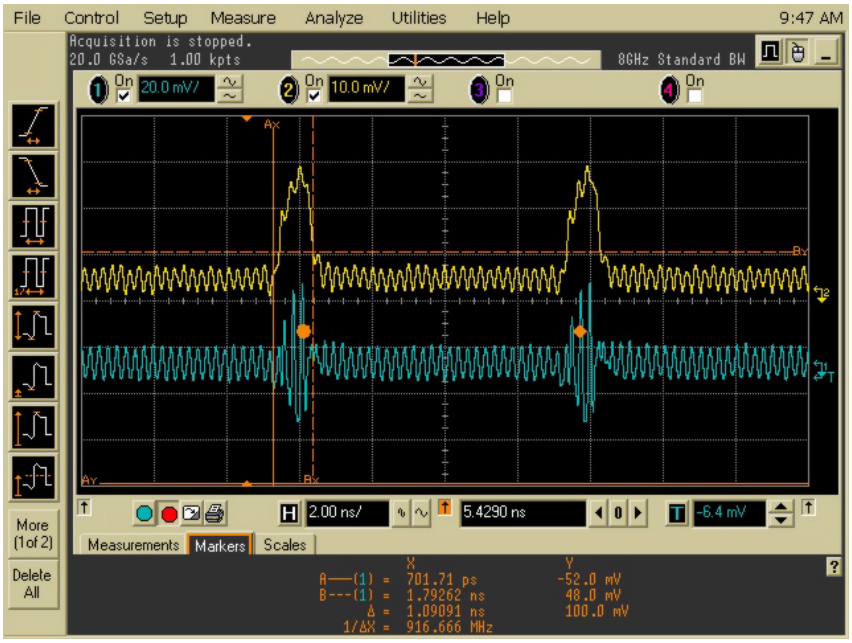


Figure 5.23: Gated VCO time domain output waveform at 4.05 GHz (low tuning end). The pulse generator control output has a measured pulse width of ∼1 ns and PRF of ∼8 ns.

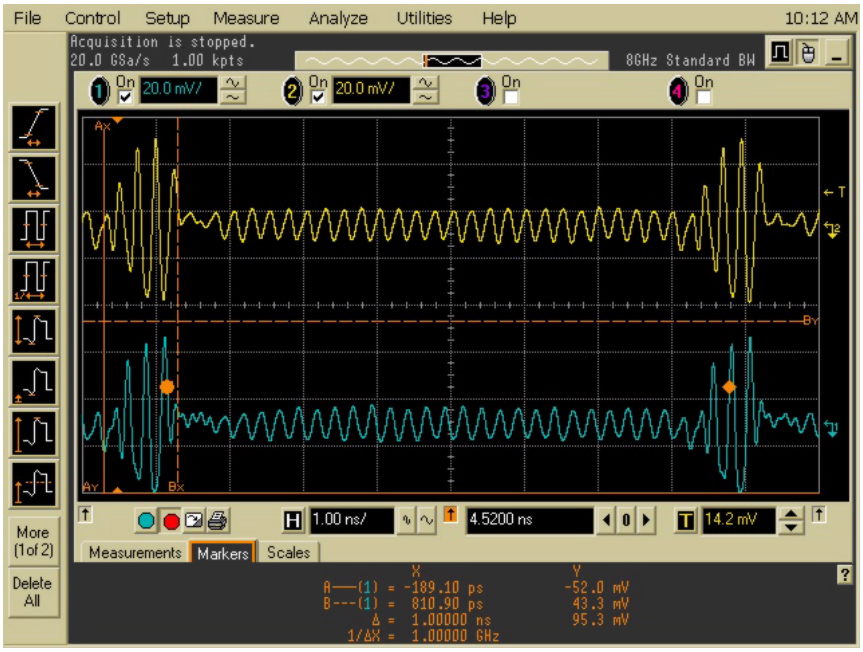


Figure 5.24: Differential gated pulses of 1 ns pulse width.

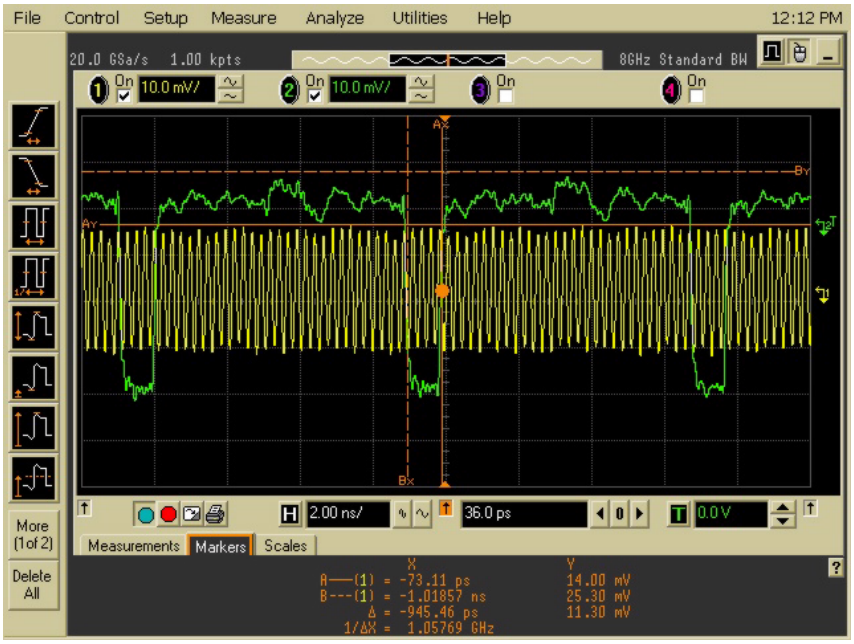


Figure 5.25: The pulse generator control output without loading has a measured pulse width of ∼1 ns and PRF of ∼8 ns.

process variations. Also since there is a correlation between the VCO and the pulse timing control signal, the transmitted pulses have a stable starting phase. With the modified reset signal, the pulse generator shows very stable and accurate timing operation over device mismatches and process variations. The VCO is designed to operate with a fixed center frequency of 4 GHz and consumes a current of 1.6 mA, of which the divider circuit consumption is less than $1mA$. The divider is able to operate up to 6.4 GHz. With technology scaling to smaller gate lengths, this maximum frequency of operation can be further improved. The contribution of this chapter includes the detailed analysis and implementation of the new improved UWB pulse generator, reduced power consumption dividers and smaller die size.

Chapter 6

Linear (Resistive) MOS Double Balanced Mixers

As introduced in Chapter Five (Fig. 5.1), multiband operation for the UWB transmitter can be realized by using a fixed PLL, frequency dividers and SSB mixers. However, mixers generate harmonic and intermodulation products from input frequencies through nonlinear mixing. Such products could corrupt the transmitted spectrum. Therefore, it is critical for a mixer to have high linearity to minimize the level of these unwanted frequencies. In this chapter, a new resistive mixer design with high linearity is discussed in detail, and is subsequently implemented in a multiband transmitter in Chapter Seven. In addition to linearity, the proposed resistive mixer also has negligible DC current consumption, which is desirable for low power systems.

6.1 Overview of Basic mixer operation

The basic function of a mixer is to multiply two input signals at frequencies ω_1 and ω_2, respectively, and generate output signals at the sum $(\omega_1 + \omega_2)$ and difference $(\omega_1 - \omega_2)$ of the input frequencies:

$$\cos(\omega_1 t)\cos(\omega_2 t) = \cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t \tag{6.1}$$

An upconversion mixer converts a intermediate frequency IF to a radio frequency RF ($\omega_{IF} + \omega_{LO}$) by mixing IF with a local oscillator LO; while a downconversion mixer converts RF to IF ($\omega_{RF} - \omega_{LO}$) by mixing RF with LO. Mixers realize frequency translation through either device nonlinearity or a time-variant (switching) process. Ideally, a mixer should only generate the above sum and difference frequencies. However, in the real world, mixers also produce other harmonic and intermodulation frequency terms in addition to the sum and difference terms. It is a very important and challenging task to sufficiently suppress these unwanted frequencies.

Mixers have different requirements depending on whether they are to be used in the receive or the transmit paths. In the receive path, the signal to noise ratio may be very low and there may also be nearby in-band interferences; therefore a down-conversion mixer requires low noise figure and high linearity. For an up-conversion mixer, noise figure is generally not a concern due to the fact that the input signal level is well above the noise floor; however, it is very important to have high linearity in order to suppress unwanted higher order harmonics.

Mixing functions can be implemented with different devices or circuit topologies, for example (Figure 6.1): a diode mixer employing an exponential I-V relation; a FET mixer employing the square law I-V characteristic in the saturation region; and a commutating-type mixer which multiplies the input with a square wave switching function.

A series expansion of the diode exponential equation reveals a second order term that generates the desired mixing products:

$$I = I_s e^{\frac{V_j}{V_T}} = I_s \left[1 + \frac{V_j}{V_T} + \frac{1}{2!}\left(\frac{V_j}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{V_j}{V_T}\right)^3 \quad ... \right] \tag{6.2}$$

where V_j is the diode junction voltage. Nonlinearities arise from the cubic and higher order terms in the expansion. On the other hand, a FET mixer makes use of the square law characteristic of a FET device in its saturation region:

$$\begin{aligned} I &= k(V_{gs} - V_t)^2 \\ &= k(V_{gs}^2 - 2V_{gs}V_t + V_t^2) \end{aligned} \tag{6.3}$$

The desired mixing product is generated by applying an input voltage of $V_{gs} =$

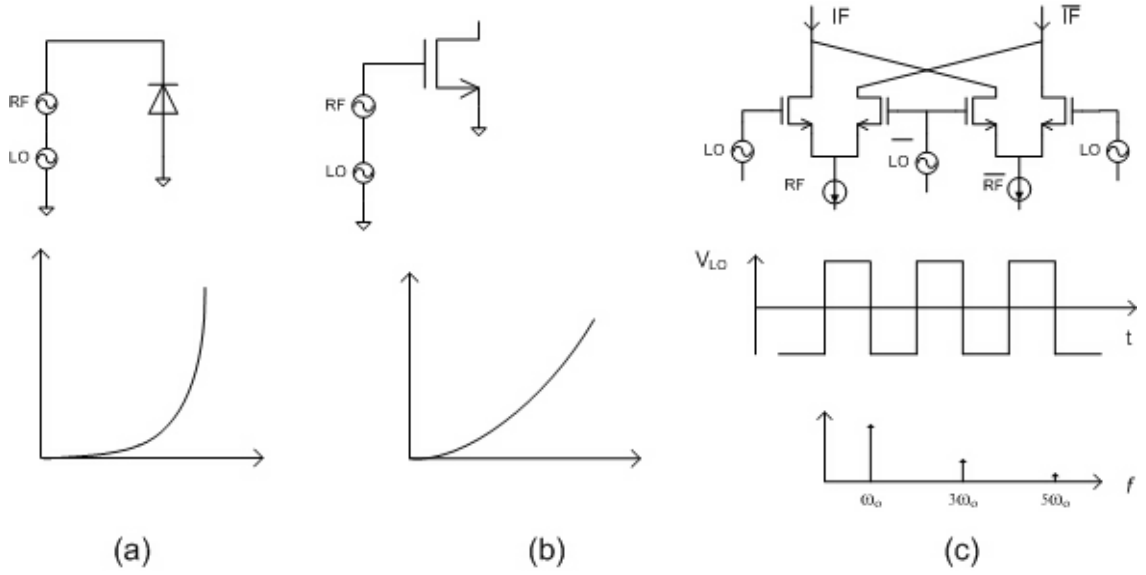


Figure 6.1: Various types of mixers with their nonlinear generating functions: (a) diode mixer; (b) FET mixer; (c) commutating mixer.

$V_{RF} + V_{LO} + V_{bias}$ to the gate of the FET, where the large signal LO modulates the transconductance $[g_m = 2k(V_{gs} - V_t) \sim 2k \cdot (V_{LO} + V_{bias} - V_t)]$ of the FET. An ideal FET I-V equation only contains the square term, such that the output will not contain any higher harmonics and cross products. However, secondary effects such as channel length modulation and short channel effects cause the FET I-V curve to deviate from the pure square law relationship, resulting in higher order harmonics and intermodulation products in the FET mixer output.

Another widely used type of mixer is the commutating-type mixer; the popular double balanced *Gilbert cell* mixer (with the addition of V-I conversion in the RF path) falls into this category. The *Gilbert cell* mixer converts an RF input voltage to a current; then uses a current steering stage controlled by the LO signal to impose a near square wave on the converted RF current. The LO switching waveform is given by:

$$Sq(\omega_{LO}t) = \frac{4}{\pi} \cdot [\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) - \frac{1}{7}\cos(7\omega_{LO}t) + ...], \quad (6.4)$$

which contains a fundamental LO frequency and its odd higher order harmonics (square wave only contains odd integer harmonics). The desired mixing product is

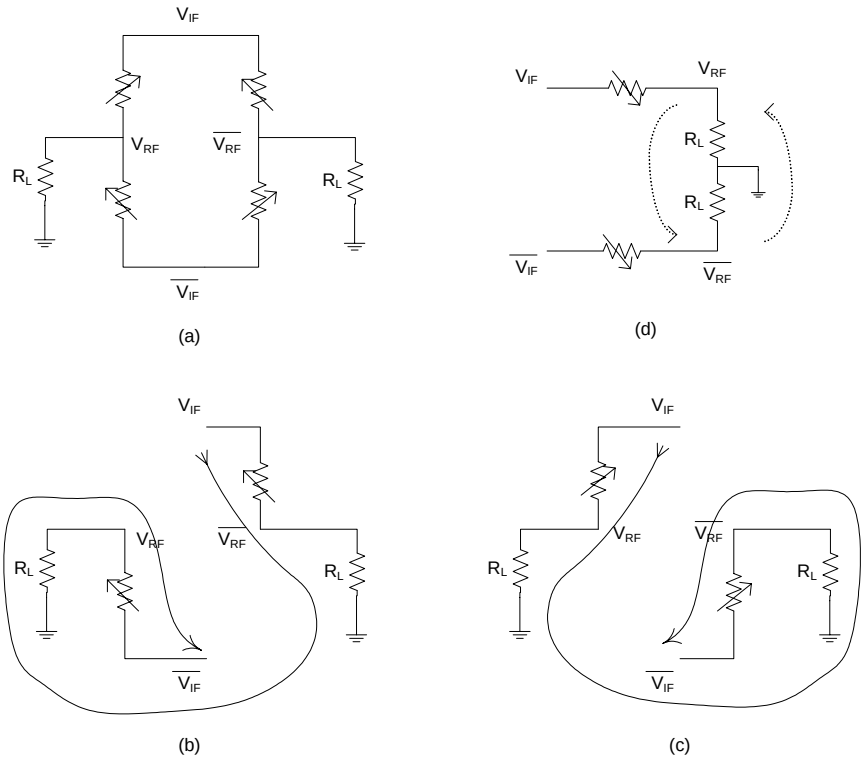


Figure 6.2: Operation of a switched type double balanced mixer.

the product of the RF with the *fundamental* LO component in Eq. 6.4:

$$I_{mix} \sim \frac{4}{\pi} \cdot I_{RF} \cdot \cos(\omega_{LO} t) \sim \frac{4}{\pi} \cdot |I_{RF}| \cdot \cos(\omega_{RF} t) \cos(\omega_{LO} t) \tag{6.5}$$

Traditionally, at high RF frequencies where square wave functions are difficult to realize, a large LO drive is required to increase the conversion efficiency. If the V-I conversion stage is not used, a passive commutating-type mixer can be realized.

The operation of a passive double balanced switching-type mixer (upconversion) can be explained as shown in Fig. 6.2. During each LO cycle, the switches change polarity twice [Fig. 6.2 (b)-(c)]. The mixing operation is realized as the direction of IF current flowing into $RF/\overline{RF}$ nodes being switched twice each LO cycle [Fig.6.2 (d)]. This same operation also creates the IF virtual ground at the RF port. From an IF input impedance point of view, the toggling of $RF/\overline{RF}$ port does not affect

its input impedance. Therefore the equivalent differential IF input resistance is

$$R_{if\_diff} = 2R_L + 2R_{sw} \tag{6.6}$$

where R_L is the load resistance and R_{sw} is the switch resistance. To optimize the conversion gain, the switch resistance should be kept as small as possible. As the switch is driven very hard, its resistance becomes negligible compared to the load resistance. The maximum conversion efficiency is realized by a square wave switching waveform. In this case, the RF output waveform is given by:

$$V_{RF} = V_{IF} \cdot \frac{4}{\pi} \cdot \left[\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) - \frac{1}{7}\cos(7\omega_{LO}t) + ...\right] \tag{6.7}$$

and therefore the conversion gain for one side band is (both side band have equal amplitudes, resulting a factor of 0.5 for each):

$$G_c = 20 \cdot \log\left(0.5 \cdot \frac{4}{\pi}\right) = -3.9dB \tag{6.8}$$

An alternative to the passive switched mixer is the *resistive* mixer, which will be detailed in the next section.

6.2 Resistive Mixers

In contrast to the above approaches, resistive mixing uses FET transistors operating in the triode region, and are capable of very low distortion [67]. In this work, CMOS technology is used, but other types of FETs can be used as well [68][69]. A MOSFET operating in its deep triode region is approximately a linear voltage controlled conductor, generating a current proportional to its drain-source voltage (assuming long channel device here):

$$\begin{aligned} I &= \mu_n C_{ox}\frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{1}{2}(V_{ds})^2\right] \\ &\simeq \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_t)V_{ds} = kV_{eff}V_{ds} \end{aligned} \tag{6.9}$$

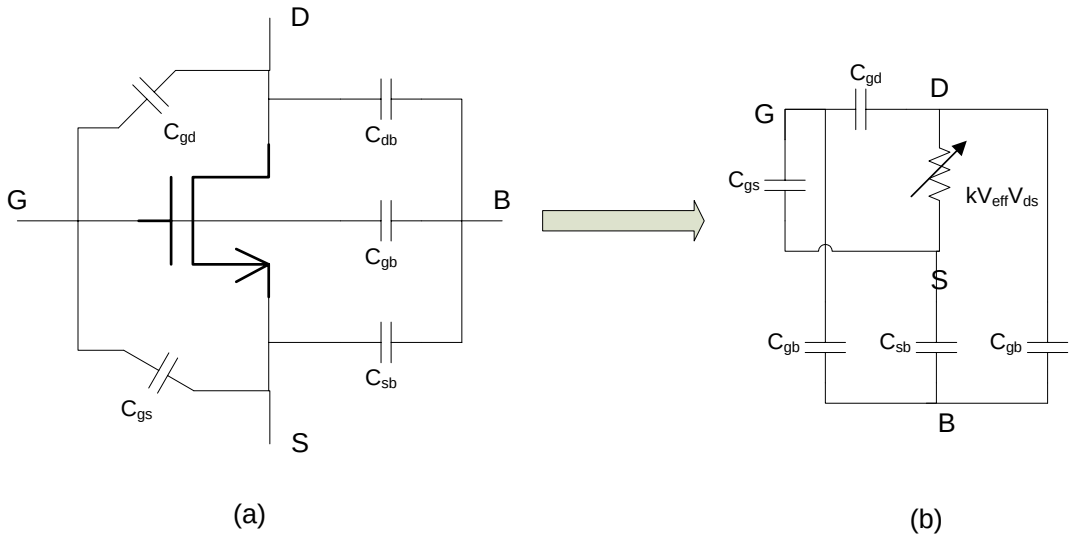


Figure 6.3: An equivalent model of a FET transistor operating in its deep triode region.

given the condition that $V_{gs} - V_t >> V_{ds}$. A simplified high frequency model, including parasitics of the MOSFET operating in the linear (triode) region is shown in Figure 6.3 [70]. In linear operation mode, the gate-to-drain and gate-to-source capacitance is approximated by $C_{gs} = C_{gd} = \frac{1}{2}C_{ox}WL + C_{ov}$. Here C_{ov} is the first order gate to source/drain overlap capacitance ($\frac{\epsilon_{ox}}{t_{ox}}WL_{ov}$). For an NMOS device with dimensions of $50\mu m/0.18\mu m$, C_{gs} and C_{gd} are around $80fF$. The capacitance between the drain and source of a MOSFET is often neglected due to the isolation between the drain and source. The drain/source to bulk capacitances are due to the reverse biased PN diodes at the junctions, and their values are dependent on the drain/source to bulk voltage.

The MOSFET drain current in the deep triode region can be expressed as the product of its drain-to-source voltage V_{ds}, and a voltage controlled conductance G_{triode} (the inverse of the voltage controlled resistance R_{triode}):

$$R_{triode}(V_{gs}) = \begin{cases} \frac{1}{\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)} = \frac{1}{k(V_{gs}-V_t)} & V_{gs} > V_t \\ \infty & V_{gs} < V_t \end{cases} \tag{6.10}$$

$$G_{triode}(V_{gs}) = \begin{cases} \mu C_{ox}\frac{W}{L}(V_{gs} - V_t) = k \cdot (V_{gs} - V_t) & V_{gs} > V_t \\ 0 & V_{gs} < V_t \end{cases} \tag{6.11}$$

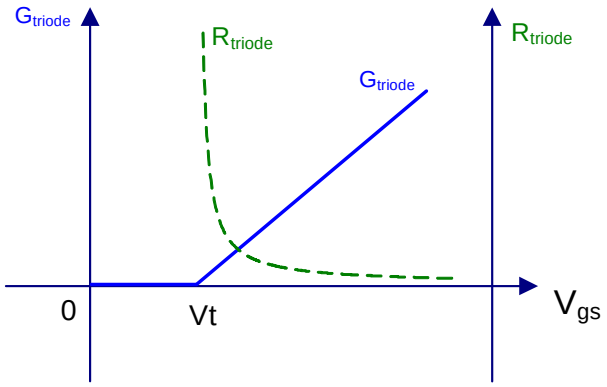


Figure 6.4: FET conductance and resistance in deep triode region (long channel approximation, G and R are not shown to the same scale).

where $k = \mu C_{ox}\frac{W}{L}$ can be seen to be the slope of the G_{triode} vs. V_{gs} curve. As V_{gs} increases above the threshold voltage V_t, the conductance of the FET starts to increase linearly with $(V_{gs} - V_t)$ from zero; at the same time the resistance decreases inversely with the effective voltage $(V_{gs} - V_t)$ from infinity towards zero, as shown in Figure 6.4.

Note that in order to take advantage of the linear characteristic of a FET, it must function as a linear voltage controlled *conductor* instead of a nonlinear voltage controlled resistor. The transistor converts the input voltage to a mixing current, which is used to drive the load. Functioning as a current source, the FET device must have a reasonable output impedance larger than, or comparable to, the load impedance.

Consider the voltage controlled FET conductance G_{triode} assuming the gate-to-source voltage V_{gs} is above the threshold V_t during the entire cycle. Assuming the gate DC bias voltage is V_B, a sinusoidal local oscillator control $V_{lo} = A_{lo}\cos(\omega_{lo}t)$ is applied to the gate with $V_B - V_t > A_{lo}$ so that the MOSFET never enters its cutoff region. The conductance of the transistor can then be written as (Fig. 6.5):

$$G_{triode} = \mu C_{ox}\frac{W}{L}(V_B - V_t) + \mu C_{ox}\frac{W}{L}V_{lo} \tag{6.12}$$

Consequently, the voltage controlled conductance G_{triode} can be separated into two parts — a constant conductance g_{dc} and a variable conductance g_{ac}, given by (Figure

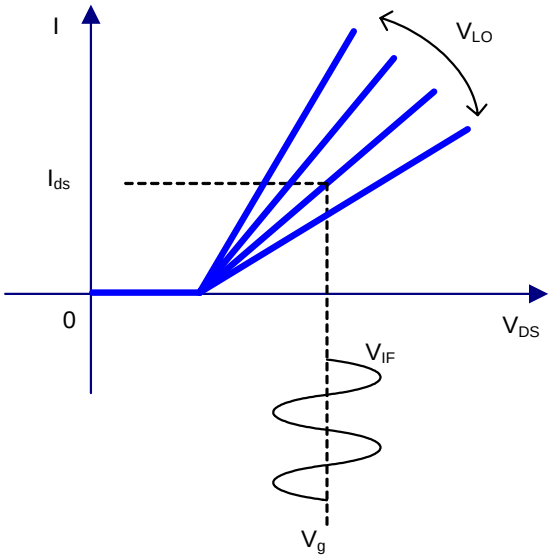


Figure 6.5: Drain current of a FET vs. V_{gs} with LO modulation in the deep triode region.

6.6):

$$\begin{aligned} g_{dc} &= \mu C_{ox}\frac{W}{L}(V_B - V_t) \\ g_{ac} &= \mu C_{ox}\frac{W}{L}V_{lo} = \mu C_{ox}\frac{W}{L}A_{lo}\cos(\omega_{lo}t) \end{aligned} \tag{6.13}$$

The variable conductance g_{ac} is controlled by the AC component of the gate bias. Considering the transmit (upconversion) mode application, with an input IF voltage $V_{if} = A_{if}\cos(\omega_{if}t)$ applied at the drain of the FET, the transistor drain current can be expressed by two terms: (1) $I_{if} = V_{if}Y_{dc}$, which is the product of the IF input and g_{dc}; (2) $I_{mix} = V_{if}g_{ac}$, which is the mixing product between the IF input and LO. While the first term generates an IF current, the second term generates an RF current with first order components at $\omega_{lo} + \omega_{if}$ and $\omega_{lo} - \omega_{if}$. The total transistor

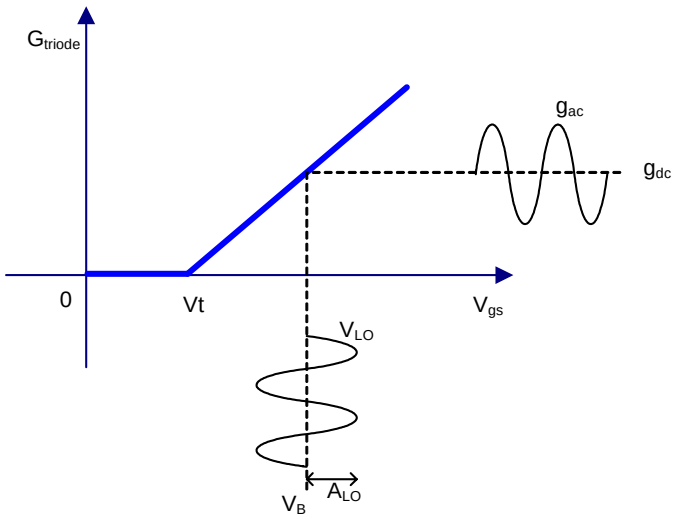


Figure 6.6: Conductance G_{triode} of a FET vs. V_{gs} in the deep triode region.

current I_d (assuming currents other than IF are shorted) is therefore:

$$\begin{aligned} I_d &= I_{if} + I_{mix} \\ &= g_{dc}V_{if} + g_{ac}V_{if} \\ &= A_{if} \cdot \mu C_{ox}\frac{W}{L}(V_b - V_t) \cdot \cos(\omega_{if}t) \\ &\quad + \frac{1}{2}A_{if} \cdot \mu C_{ox}\frac{W}{L}A_{lo} \cdot \cos(\omega_{lo} + \omega_{if})t \\ &\quad + \frac{1}{2}A_{if} \cdot \mu C_{ox}\frac{W}{L}A_{lo} \cdot \cos(\omega_{lo} - \omega_{if})t \end{aligned} \tag{6.14}$$

The constant conductance g_{dc} is the term generating a current at the IF frequency when a IF voltage is applied since no frequency conversion is involved; therefore g_{dc} contributes to the IF input impedance. This can be viewed as a voltage source at the IF frequency applied to the mixer and only an IF current is generated by the Z_{if} of the input port with the output shorted. On the other hand, the variable conductance g_{ac} functions as a frequency converter which generates both upper and lower RF sidebands around the LO input frequency from the input IF voltage. If only one sideband is selected in a single side band mixer, the IF voltage to RF current conversion transconductance can be written as:

$$g_{c\_SSB} = \frac{1}{2}\mu C_{ox}\frac{W}{L}A_{lo} \tag{6.15}$$

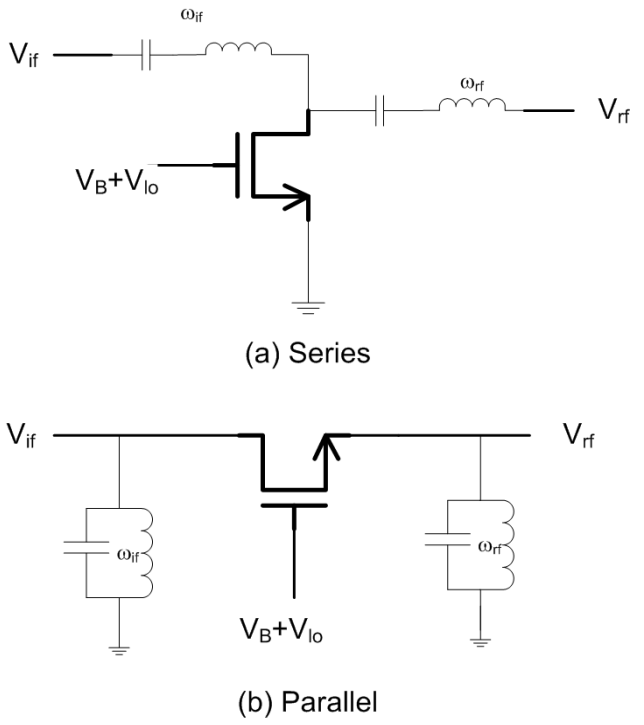


Figure 6.7: Two basic single resistive mixer configurations: (a) Series (b) Parallel.

A single MOSFET resistive mixer can be implemented using either series resonant circuits, as shown in Fig. 6.7 (a) [67], or parallel resonant circuits, as shown in 6.7 (b) [71]. In the series resonant configuration, the MOSFET is grounded at its source terminal. Here the IF input is applied to the drain node through a series LC network resonant at ω_{if}, which ideally passes only the IF frequency and blocks all other frequencies. The RF output is taken from the drain node through a series LC circuit resonant at ω_{rf}, which ideally passes only the RF frequency and blocks all other frequencies. For the series configured resistive mixer, the FET gate-to-source voltage is kept at V_{lo} since both IF and RF voltage are at the the drain node while the source is grounded. In this case, for the IF input signal (assume the RF port is shorted), a current is generated (note that the mixed RF current is flowing out of

RF port):

$$\begin{aligned} I &= V_{if} \cdot g \\ &= A_{if}\cos(\omega_{if}t) \cdot k(V_b - V_t + V_{lo}) \qquad (6.16) \\ &= A_{if}\cos(\omega_{if}t) \cdot k(V_b - V_t) + A_{if}\cos(\omega_{if}t) \cdot kA_{lo}\cos(\omega_{lo}t)) \\ &= A_{if}\cos(\omega_{if}t) \cdot k(V_b - V_t) \qquad (6.17) \\ &\quad + \frac{1}{2}A_{if} \cdot kA_{lo} \cdot \cos(\omega_{rf})t + \frac{1}{2}A_{if} \cdot kA_{lo} \cdot \cos(\omega_{rf\_im})t \qquad (6.18) \end{aligned}$$

where $k = \mu C_{ox}\frac{W}{L}$. If a voltage at RF frequency is present at the drain, a current is generated (in this case the IF port is shorted) :

$$\begin{aligned} I &= V_{rf} \cdot g \\ &= A_{rf}\cos(\omega_{rf}t) \cdot k(V_b - V_t + V_{lo}) \qquad (6.19) \\ &= A_{rf}\cos(\omega_{rf}t) \cdot k(V_b - V_t) + A_{rf}\cos(\omega_{rf}t) \cdot kA_{lo}\cos(\omega_{lo}t)) \\ &= A_{rf}\cos(\omega_{rf}t) \cdot k(V_b - V_t) \\ &\quad + \frac{1}{2}A_{rf} \cdot kA_{lo} \cdot \cos(\omega_{if\_im})t + \frac{1}{2}A_{rf} \cdot kA_{lo} \cdot \cos(\omega_{if})t \qquad (6.20) \end{aligned}$$

$$g_{if} = g_{rf} = k(V_b - V_t + V_{lo}) \qquad (6.21)$$

The second resistive mixer configuration uses parallel resonant LC tanks at the IF input and RF output as shown in Fig. 6.7 (b). A parallel LC tank appears as an open circuit at its resonant frequency, and very low impedance at other frequencies away from its resonant frequency. At the RF output node, the parallel LC network is designed to be resonant at ω_{rf}, passing the RF signal. Ideally, the IF and LO frequencies will see a very low impedances (shorts) and will be rejected. Meanwhile, at the IF input port, the RF and LO signals see very low impedances, and the IF signal is passed.

For the parallel configured resistive mixer, the gate-to-source voltage is different depending on choice of input port. For an IF input voltage, V_{gs} is $V_g - V_{rf}$; for an RF input voltage, V_{gs} is $V_g - V_{if}$. For an input signal at the IF port, the variable

conductance is (note that the mixer RF current is flowing to the RF port):

$$\begin{aligned} g_{if} &= k(V_b - V_t) + kV_{lo} - kV_{rf} \\ &= k(V_b - V_t + V_{lo}) \qquad RF\ port\ shorted \end{aligned} \tag{6.22}$$

For an input signal at the RF port, the variable conductance is:

$$g_{rf} = k(V_b - V_t) + kV_{lo} - kV_{if} \tag{6.23}$$

$$= k(V_b - V_t + V_{lo}) \qquad IF\ port\ shorted \tag{6.24}$$

The IF and RF transconductance are equal for both series or parallel configured resistive mixers (Eq. 6.21-6.23). It can be expressed as a DC conductance and AC conductance:

$$\begin{aligned} g &= k(V_b - V_t) + kV_{lo} \\ &= g_{dc} + g_{ac} \end{aligned} \tag{6.25}$$

where g_{dc} is connected to a current with no frequency change, while g_{dc} will result in a mixer term.

The resistive mixer is "reversible" in that frequency translation can be performed from either the IF side or the RF side. At the RF port, the DC conductance g_{dc} generates current at RF frequency, while at the IF port, the AC transconductance g_{ac} generates current at IF frequency (both side band). It can be shown that the RF output conductance is equal to the IF input impedance when the load and source resistances are equal.

A simplified two port equivalent circuit of a single FET resistive mixer with parallel matching networks is shown in Figure 6.8. Note that the IF and RF circuits are decoupled from each other due to the presence of the LC resonant tanks at both input and output ports. The parallel configured resistive mixer in Figure 6.7(b) has its RF current flowing out of its source node, such that the current source in Figure 6.8 is pointing upward. On the other hand, the series configured resistive mixer in Figure 6.7(a) has its RF current flowing out of its drain node; therefore the equivalent two port for this type should have its conversion transconductance current source pointing downward.

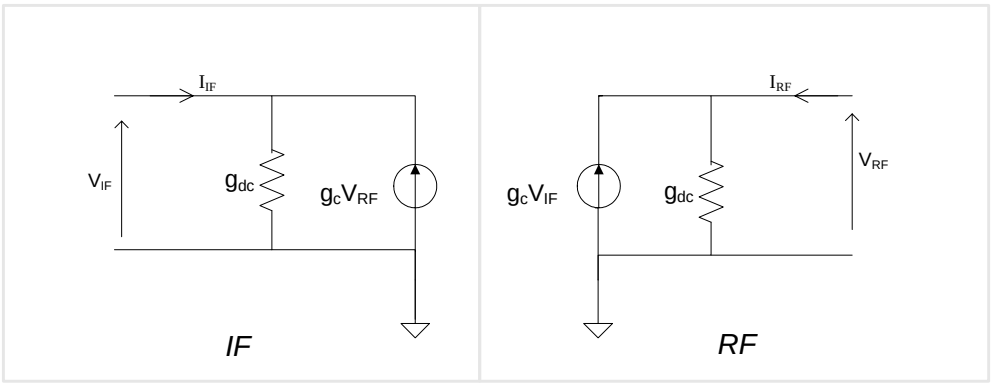


Figure 6.8: An equivalent 2-port circuit of a single FET resistive mixer with parallel IF/RF resonant LC circuit.

The two port current equations of a parallel configured resistive mixer are:

$$\begin{aligned} I_{IF} &= g_{dc}V_{IF} - g_cV_{RF} \\ I_{RF} &= -g_cV_{IF} + g_{dc}V_{RF} \end{aligned} \tag{6.26}$$

where gc is half of g_{ac} (one side band). The two port current equations of a series configured resistive mixer are:

$$\begin{aligned} I_{IF} &= g_{dc}V_{IF} + g_cV_{RF} \\ I_{RF} &= +g_cV_{IF} + g_{dc}V_{RF} \end{aligned} \tag{6.27}$$

Therefore, the equivalent two port Y parameter matrix (without parasitic capacitances) of a parallel configured resistive mixer is [72]:

$$[Y_{2\times 2}] = \begin{bmatrix} g_{dc} & -g_c \\ -g_c & g_{dc} \end{bmatrix} \tag{6.28}$$

The IF input resistance, RF output resistance, and available power gain can be calculated in the presence of source and load impedances connected to the two port equivalent circuit (Figure 6.9). The total voltage equations for the input and output

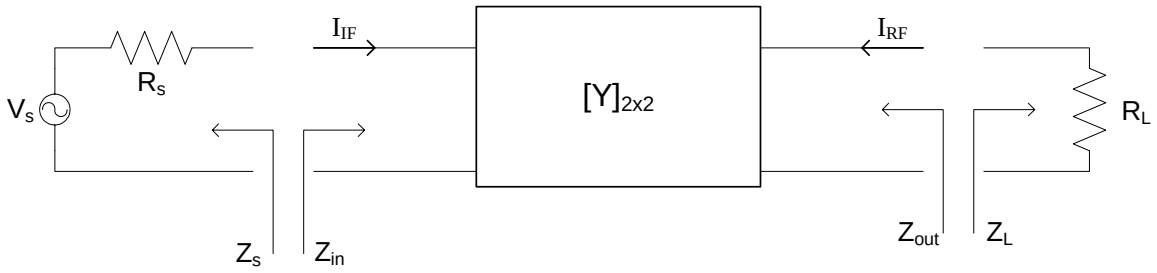


Figure 6.9: A two port model of mixer is connected to a source and a load.

are:

$$V_s = I_{IF}R_s + V_{IF} \tag{6.29}$$

$$V_{RF} = -I_{RF}R_L \tag{6.30}$$

It is convenient to use the current equations at the source and load to calculate the input and output conductance with the two port Y-parameters $[Y_{2\times2}]$:

$$I_{IF}R_s = g_s(V_s - V_{IF}) \tag{6.31}$$

$$I_{RF} = -g_L V_{RF} \tag{6.32}$$

Then, the IF input conductance can be calculated using Equations 6.26, 6.31 and 6.32:

$$g_{in,IF} = \frac{I_{IF}}{V_{IF}} = \frac{g_{dc}(g_L + g_{dc}) - g_c^2}{g_L + g_{dc}} \tag{6.33}$$

The RF output conductance is calculated by shorting the input voltage source V_s using Equation 6.26, 6.31 and 6.31:

$$g_{out,RF} = \frac{I_{RF}}{V_{RF}} = \frac{g_{dc}(g_s + g_{dc}) - g_c^2}{g_s + g_{dc}} \tag{6.34}$$

The maximum available power transfer at both input and output occurs when both input and output are matched, as stated by the following condition:

$$g_s = g_{in} = g_L = g_{out} \tag{6.35}$$

Therefore, the input and output conductances for the matched condition are given

by [72]:

$$g_{in} = g_{out} = g_{dc}\sqrt{1 - \left(\frac{g_c}{g_{dc}}\right)^2} \tag{6.36}$$

For the special case where the output is shorted ($g_L = \infty$), the input conductance is $g_{in} = g_{dc}$. In other words, the conversion conductance reduces the overall input conductance when an nonzero load is applied at the output. The ratio $\frac{g_c}{g_{dc}}$ is equal to or less than unity according to the Fourier analysis of conductance later in this section.

The available input power from the source P_{avs} is that power that a voltage source will deliver to a conjugate matched input. For the case of the IF input of the parallel conjugate matched mixer:

$$P_{if\_avs} = \frac{1}{2}\frac{(\frac{1}{2}V_s)^2}{R_s} = \frac{V_s^2}{8R_s} = \frac{1}{8}V_s^2 g_s \ . \tag{6.37}$$

The output power delivered to the load is

$$P_{rf\_out} = \frac{1}{2}\frac{(V_{RF})^2}{R_L} = \frac{1}{2}V_{RF}^2 g_L \ . \tag{6.38}$$

The available power gain is the ratio between the delivered power and the available power from the source:

$$\begin{aligned} G_a &= \frac{P_{rf\_out}}{P_{if\_avs}} = 4\frac{V_{RF}^2 g_L}{V_s^2 g_s} \\ &= 4A_v^2\frac{g_L}{g_s} \end{aligned} \tag{6.39}$$

The voltage gain from source to load is A_v which can be calculated from Equations 6.26, 6.31 and 6.32:

$$\begin{aligned} A_v &= \frac{V_{RF}}{V_s} \\ &= \frac{g_c g_s}{(g_{dc} + g_L)(g_{dc} + g_s) - g_c^2} \end{aligned} \tag{6.40}$$

The available power gain is therefore:

$$
\begin{aligned}
G_a &= 4A_v^2 \frac{g_L}{g_s} \\
&= 4 \frac{g_c^2 g_s g_L}{\left[(g_{dc} + g_L)(g_{dc} + g_s) - g_c^2 \right]^2}
\end{aligned} \tag{6.41}
$$

The *maximum* available power gain is defined for the case when both input and output ports are conjugate matched [72]:

$$
\begin{aligned}
G_{MAG} &= 4 \frac{g_c^2 g_L^2}{\left[(g_{dc} + g_L)^2 - g_c^2 \right]^2} \\
&= \frac{\left(\frac{g_c}{g_{dc}} \right)^2}{\left[1 + \sqrt{1 - \left(\frac{g_c}{g_{dc}} \right)^2} \right]^2} \\
&= \frac{\beta^2}{\left[1 + \sqrt{1 - \beta^2} \right]^2}
\end{aligned} \tag{6.42}
$$

where the conversion factor β is defined as the ratio of g_c and g_{dc}. Fig. 6.10 shows the maximum conversion gain vs. conversion factor. As the conversion factor approaches one, the conversion gain approaches 0 dB. (Since this is a passive mixer, conversion gain cannot be > 1.)

From Eq. 6.42, we can gain some insight on how to increase the power conversion efficiency. As V_{gs} is above threshold during the entire cycle, the voltage controlled conductance does not compress as the LO voltage swings to its negative half cycle. The conversion gain G_a may be increased by increasing magnitude A_{lo} until it reaches the value of $|V_b - V_t|$ (Fig. 6.4). At this point, the DC and conversion transconductance are given by:

$$
g_{dc} = k(V_B - V_t) = kA_{lo} \tag{6.43}
$$

$$
g_c = \frac{1}{2} kA_{lo} \tag{6.44}
$$

and the conversion factor β is therefore 0.5. Therefore the MAG is $G_{a\_\max} = 0.071 = -11.4dB$. Further increasing A_{lo} will result in clipping of the conductance waveform during portions of the conduction cycle when V_{LO} swings below V_t. In this case,

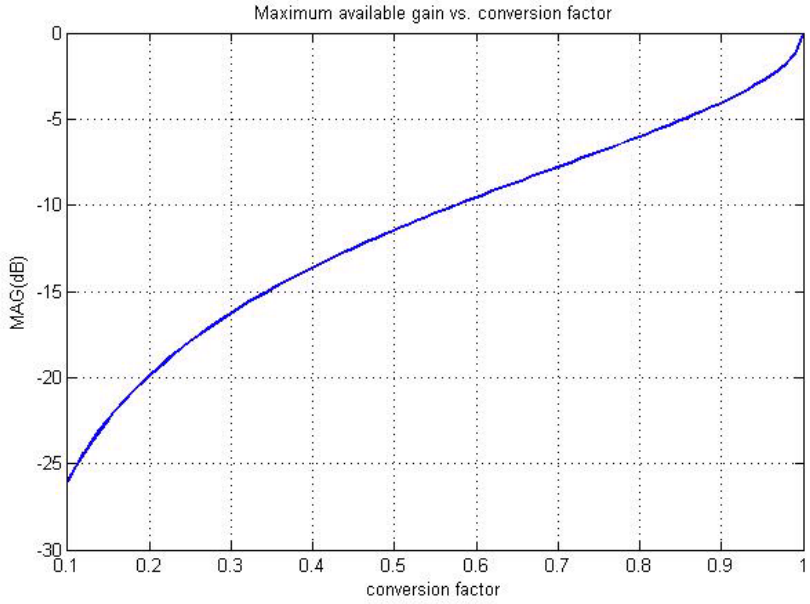


Figure 6.10: Maximum available conversion gain of a Resistive mixer vs. conversion factor.

the conductance will contain not only DC and the LO fundamental frequencies, but also higher harmonic components which are not completely suppressed by the filters. Increasing A_{lo} will increase the conversion factor β (due to increase of g_c), therefore increasing the conversion gain of the mixer.

Alternatively, the DC bias voltage at the gate can be reduced to reduce g_{dc}. The DC conductance is the average value of the transconductance, while the conversion conductance g_c is half of the AC transconductance g_{ac}. By reducing the DC bias voltage at the gate V_B, the FET conduction angle is reduced from 2π. Therefore, instead of a continuous sinusoidal conductance, a partially rectified sine wave conductance will arise (Figure 6.11). It is known that a train of sine-wave tips can be expressed using a Fourier series. With the conduction angle defined as 2ϕ,

$$\phi = \cos^{-1} \frac{(V_b - V_t)}{A_{lo}} \tag{6.45}$$

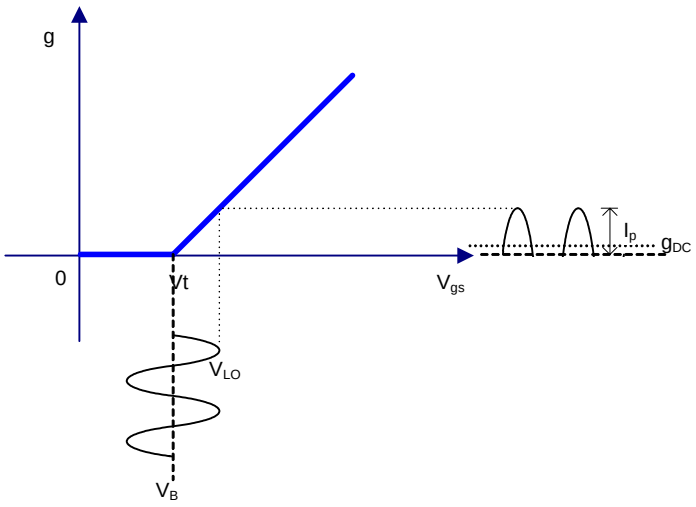


Figure 6.11: Conductance vs V_{gs} curve as the gate bias voltage reduces threshold voltage

The conductance can be expressed by its Fourier expansion [73]:

$$Y_1 = \sum_{n=0}^{\infty} I_n \cos n\omega t \tag{6.46}$$

where I_n are the Fourier coefficients given by

$$I_o = \frac{I_p}{\pi} \frac{\sin\phi - \phi\cos\phi}{1-\cos\phi} \tag{6.47}$$

$$I_1 = \frac{I_p}{\pi} \frac{\phi - \cos\phi\sin\phi}{1-\cos\phi} \tag{6.48}$$

$$I_{n\geq 2} = \frac{2I_p}{\pi} \frac{\cos\phi\sin n\phi - n\sin\phi\cos n\phi}{n\left(n^2-1\right)\left(1-\cos\phi\right)} \tag{6.49}$$

Fig. 6.12 plots the first four Fourier coefficients vs. conduction angle. The conversion factor β is $\frac{1}{2}\frac{I_1}{I_o}$ and is plotted in Figure 6.13. As the conduction angle decreases towards zero, the conversion factor increases towards one. However, unwanted harmonics decrease at a slower rate, therefore increasing their ratio to the fundamental.

Since the IF input resistance and RF output resistance are directly related to the DC conductance, it is desirable to reduce the DC conductance so as to reduce the relative IF drive requirement and increase the RF driving capability while not increasing harmonics significantly. If the mixer is biased at its threshold voltage, this

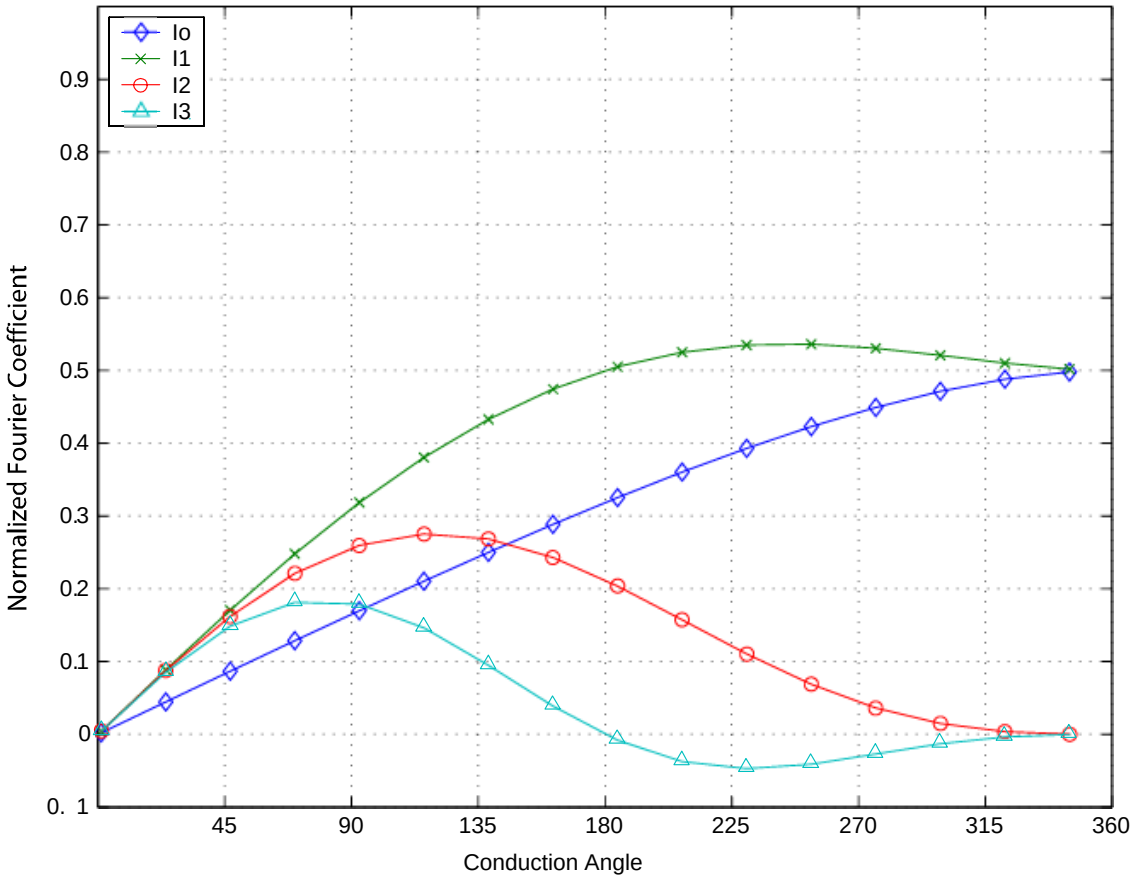


Figure 6.12: Fourier coefficients of a sine-tip pulse trains vs. conduction angle (up to the 3rd harmonic).

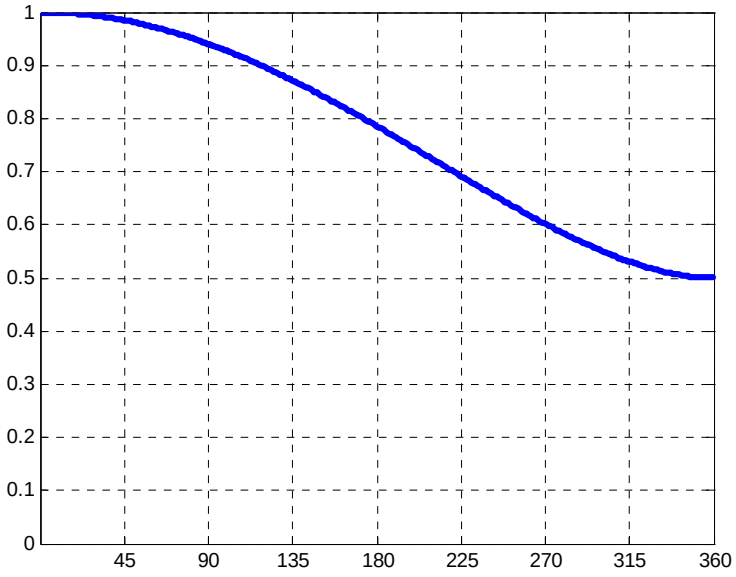


Figure 6.13: Conversion factor of a sine-wave tip pulse trains vs. conduction angle.

corresponds to a conduction angle of 180^o. This operating point provides a good compromise between the conversion factor and unwanted harmonic levels. Under the above operating condition with conduction angle of 180^o, the fundamental frequency has a Fourier coefficient I_1 of 0.5, the DC term I_o has a Fourier coefficient of $1/\pi$, and all the higher order *odd* harmonics have Fourier coefficients of 0 (Fig. 6.12). All the even harmonics are to be cancelled through the balanced mixer design in the next section.

$$\begin{aligned} g_{dc} &= \frac{1}{\pi} k A_{lo} \\ g_c &= \frac{1}{4} k A_{lo} \end{aligned} \tag{6.50}$$

The conversion factor is $\pi/4$, and the corresponding MAG is $G_a = 0.234 = -6.3dB$. As the conduction angle is further reduced, the conversion ratio β keeps increasing to unity. This leads to an ideal maximum available conversion gain of 0 dB, but with no power output, which is similar to the case of a Class C power amplifier.

6.3 Single Balanced Resistive FET Mixer

To remove the even harmonics, a *single balanced* (differential LO input) resistive mixer can be constructed using two single ended resistive mixers biased at their threshold voltages (Figure 6.14). The two FETs are pumped by differential LO inputs, and IF inputs are also connected to the the two FETs differentially. Due to the fact that the two FETs are biased at their threshold voltages with differential AC inputs, each will conduct for 50% of the LO duty cycle. Assuming, in the ideal case, that each FET will be completely on at its positive LO swing and completely off during its negative LO swing. The corresponding conductance waveforms Y_1 and Y_2 are shown in Figure 6.14. During the positive LO cycle, the top FET $M1$ conducts and the current flows from positive RF to IF load; during the negative LO cycle, the bottom FET $M2$ conducts and the current flows from RF to negative IF terminal. Therefore, we can reconstruct a combined conductance curve of the two FETs from the positive and negative parts of the sine-wave conductance with respect to the RF node:

$$\begin{aligned} g_{ac+} &= \sum_{n=0}^{\infty} I_n \cos n(\omega t) \\ &= I_o + I_1 \cos(\omega t) + I_2 \cos(2\omega t) + I_3 \cos(3\omega t) + \quad ... \end{aligned} \tag{6.51}$$

and

$$\begin{aligned} g_{ac-} &= -Y_{ac+}(\omega t + \pi) \\ &= -I_o + I_1 \cos(\omega t) - I_2 \cos(2\omega t) + I_3 \cos(3\omega t) - \quad ... \end{aligned} \tag{6.52}$$

The minus sign is due to the reverse direction of current during the negative LO cycle. The total conductance g_{ac_sb} (single balanced) with respect to differential V_{if} to RF conversion is reconstructed by combining the two linear FET conductances:

$$g_{ac\_sb} = g_{ac+} + g_{ac-} \tag{6.53}$$

If the two portions of the conductance waveforms have the same conduction angle and symmetry, then the even harmonics will cancel each other, while the odd harmonics

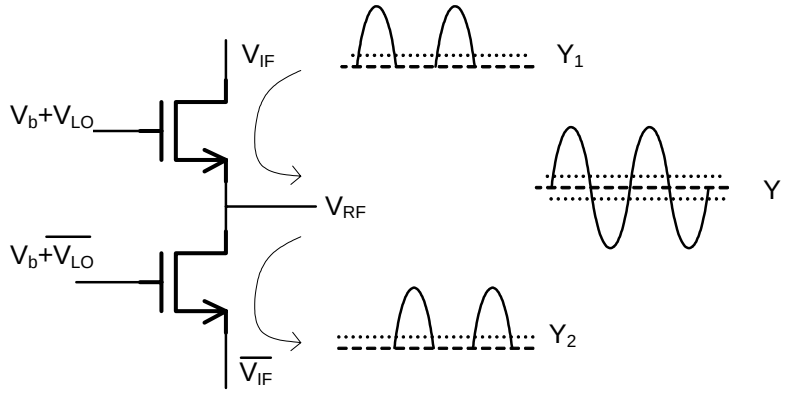


Figure 6.14: Operation of single balanced resistive mixer.

will add in phase, resulting in:

$$g_{ac\_sb} = 2I_1 \cos(\omega t) + 2I_3 \cos(3\omega t) + ... \tag{6.54}$$

From Figure 6.12, if the two FETs are biased at their own threshold voltages, the voltage controlled conductances contain zero odd LO harmonics. It therefore follows that the two sine-wave tip trains with 180^o conduction angle can be added together to reconstruct the sine-wave. In this case, the two FET conductance pulse trains are 180^o out of phase; while current flowing into the two FETs from the opposite directions (current flows from IF to RF through one FET, while flows from RF to IF through the other FET). With a differential LO signal applied at the gates of the FET pair, two rectified sine-wave pulse train conductances are generated by the FET pair. Since the IF input is differential, the conductance sine-wave tip train of the FET with negative IF input voltage can be viewed as negative and added to that of the first FET to reconstruct the complete sine-wave conductance.

For a conduction angle of 2ϕ (180^o), the first five Fourier coefficients of the sine-wave tip pulse trains are shown in Table 6.1. The even harmonics of the two sine-wave tip waveforms will cancel each other, while the odd harmonics are zero at 180^o conduction angle. Therefore, a pure sine-wave conduction waveform g_{ac_sb} results with ideally no higher order harmonics. Even though the even order harmonics and the DC term of the conductance cancel, this does *not* imply that there is no IF current consumption (and therefore infinite input impedance). What actually happens is that the positive

Even order harmonics	Ratio	Odd order harmonics	Ratio
$\frac{I_o}{I_p}$	0.3183	$\frac{I_1}{I_p}$	0.5
$\frac{I_2}{I_p}$	0.2122	$\frac{I_3}{I_p}$	0
$\frac{I_4}{I_p}$	-0.0424	$\frac{I_5}{I_p}$	0

Table 6.1: Fourier coefficient of sine-tip function with conduction angle of 180^o.

and negative terminals of the IF source will each conduct at half of the cycle. In this case, the DC conductance will be the average conductance at each half period. This can be viewed as the RF port being at a virtual ground with respect to the IF differential input with even order harmonic conductance. The resulting ac and dc conductance components of the single sideband mixer are:

$$\begin{aligned} g_{dc\_sb} &= I_o = I_p \cdot \frac{1}{\pi} \\ &= k \cdot (V_b + A_{lo} - V_t) \cdot \frac{1}{\pi} \\ &= k \cdot A_{lo} \cdot \frac{1}{\pi} \end{aligned} \tag{6.55}$$

$$\begin{aligned} g_{ac\_sb} &= \frac{1}{2} \cdot I_p \cos(\omega_{lo} t) \\ &= \frac{1}{2} k \cdot A_{lo}(\omega_{lo} t) \end{aligned} \tag{6.56}$$

Note that the DC conductance g_{dc} is referenced to the input IF.

6.4 Double Balanced Resistive FET Mixer

The single balanced mixer provides good isolation from IF to RF port since RF port is virtual ground for IF; employing a double balanced mixer additionally improves the RF to IF isolation and LO to IF isolation. A double balanced resistive mixer can be constructed using two single balanced resistive mixers with LO drive phase complementary to each other (Figure 6.15). The FETs diagonal to each other have the same phase LO inputs applied to their gates. The differential AC transconductance of the double balanced mixer g_{ac_db} generated by the two single balanced mixers is

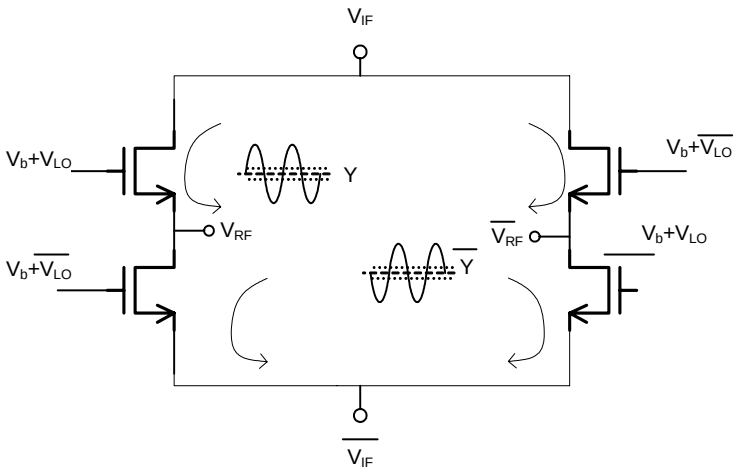


Figure 6.15: Double balanced resistive mixer.

given by

$$\begin{aligned} g_{ac\_db} &= g_{ac\_sb} - \overline{g_{c\_sb}} \\ &= k \cdot A_{lo}(\omega_{lo}t) \ , \end{aligned} \tag{6.57}$$

and the DC differential conductance and conversion conductance are given by

$$g_{dc\_db} = \frac{2}{\pi} \cdot k \cdot A_{lo} \tag{6.58}$$

$$g_{c\_db} = \frac{1}{2}\, g_{ac\_db} = \frac{1}{2} k \cdot A_{lo}(\omega_{lo}t) \tag{6.59}$$

By generating a differential output at the RF port, the differential IF input port now is a virtual ground for both the RF and LO frequencies. As the double balanced resistive mixer is biased at a conduction angle of 180^o (at the threshold voltage), the odd order harmonics in the conductance reduce to zero while the even odd harmonics cancels each other, leaving the conductance term with only the fundamental LO term. This greatly improves the linearity of the mixer since no higher order LO components arise inside of the mixer. However, due to the nonideal nature of the FET DC characteristics, LO harmonics can not be completely removed.

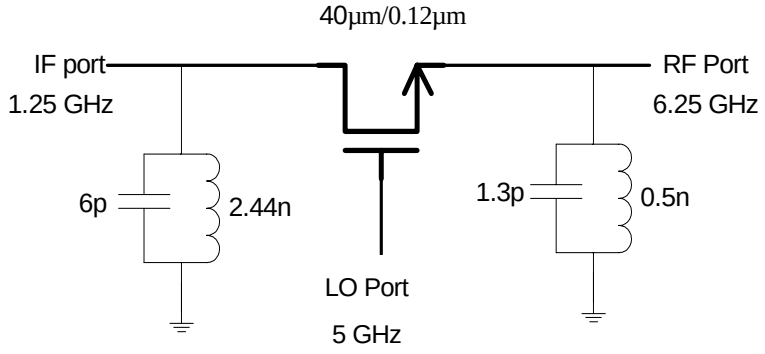


Figure 6.16: Single FET resistive mixer with input and output port parallel tank.

6.5 Resistive Mixer Simulations

First, a parallel configured resistive mixer was designed in the Jazz CA13 130nm RF CMOS process (Fig. 6.16). The input parallel tank was initially implemented using ideal LC components so as to understand the operation of the mixer and validate the theory derived in the previous sections. The simulated available conversion gain vs. LO amplitude is shown in Fig. 6.17. With the LO biased at the transistor threshold voltage of 0.3V, the simulations indicate that the maximum power conversion gain is $-7.1\ dB$. This mixer has an input (IF) 1 dB conversion point of 6.5 dBm with an LO input level of 5 dBm.

The LO DC bias level is an important factor for the conversion gain. As LO bias decreases, the conversion gain increases due to rising conversion factor. Figure 6.18 displays the simulated conversion gain at different LO bias levels. The conversion gain reaches its maximum value of $-6.8\ dB$ when the LO is biased at zero DC voltage, and decreases as the LO bias voltage increases. So if maximum conversion gain is the goal, the LO should be biased at the lowest possible DC voltage. However, linearity starts to degrade when a bias voltage lower than the threshold is used, while the LO drive level requirement is increasing at the same time. To achieve a balance between conversion gain, LO drive level and linearity, the bias voltage should be close to the threshold voltage.

A double balanced resistive mixer with real on-chip LC resonant networks is shown in Figure 6.19; for the double balanced FET resistive mixer, all ports are differential.

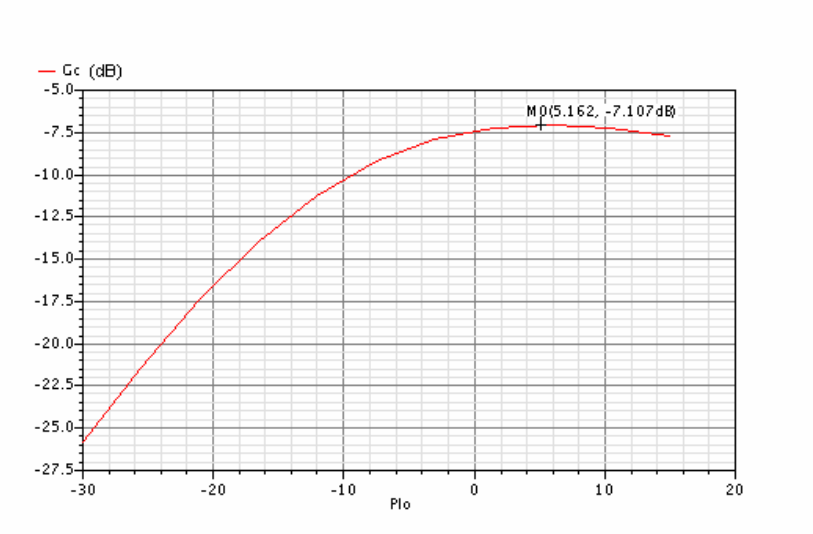


Figure 6.17: Simulated conversion gain vs. LO amplitude for a parallel configured resistive mixer based at the threshold voltage.

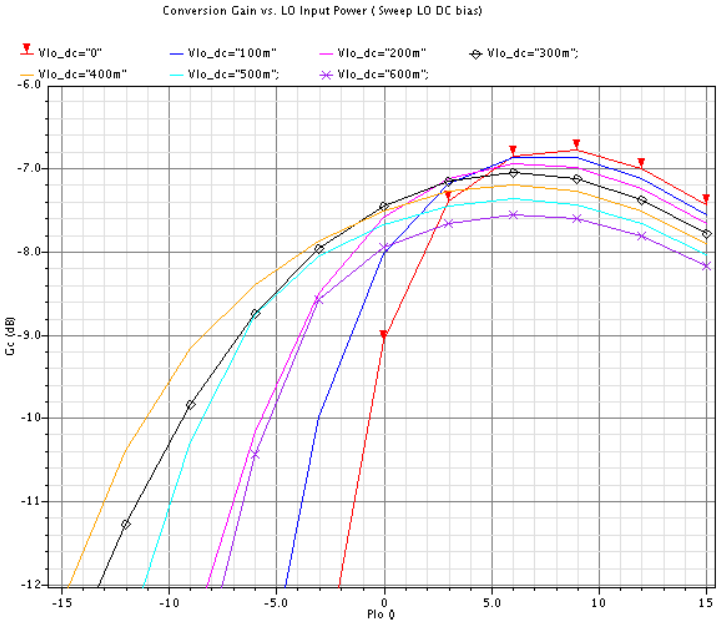


Figure 6.18: Conversion gain vs. *LO* input level while sweeping *LO* bias voltage.

Therefore, the four parallel tanks at differential outputs can be combined into two resonant tanks as shown in Figure 6.19. The simulated results (Fig. 6.20) show a maximum conversion gain of -10dB with an excellent input 1-dB compression point of 9.6 dBm with LO power of 5 dBm. (As a point of comparison: in [74], an input 1-dB compression point of -5dBm was measured with LO power of -3.5 dBm; in [71], a IIP3 of 12.3 dBm was reported with an LO power of 0 dBm) The extra loss compared to the resistive mixer with ideal LC tank is mainly due to the finite Q factor of the on-chip inductors.

6.6 Summary

This chapter provided a detailed analysis of resistive mixers which are used to design a single side band mixer to be implemented in a new multiband UWB transmitter. A resistive mixer has the advantage of near-zero DC power consumption and high linearity. By biasing the resistive mixer at its threshold voltage, the higher order odd harmonics vanish mathematically. The required buffer current may also be reduced by designing the mixer with high input and output impedances. Optimization of gain and linearity for UWB transmitter applications will discussed in the next chapter. The contribution of this chapter includes a detailed analysis of resistive mixer operation, and the evolution from single FET resistive mixers to double balanced resistive mixer. The optimum operating conditions are derived to serve as design guidelines for the transmitter implementation in the next chapter.

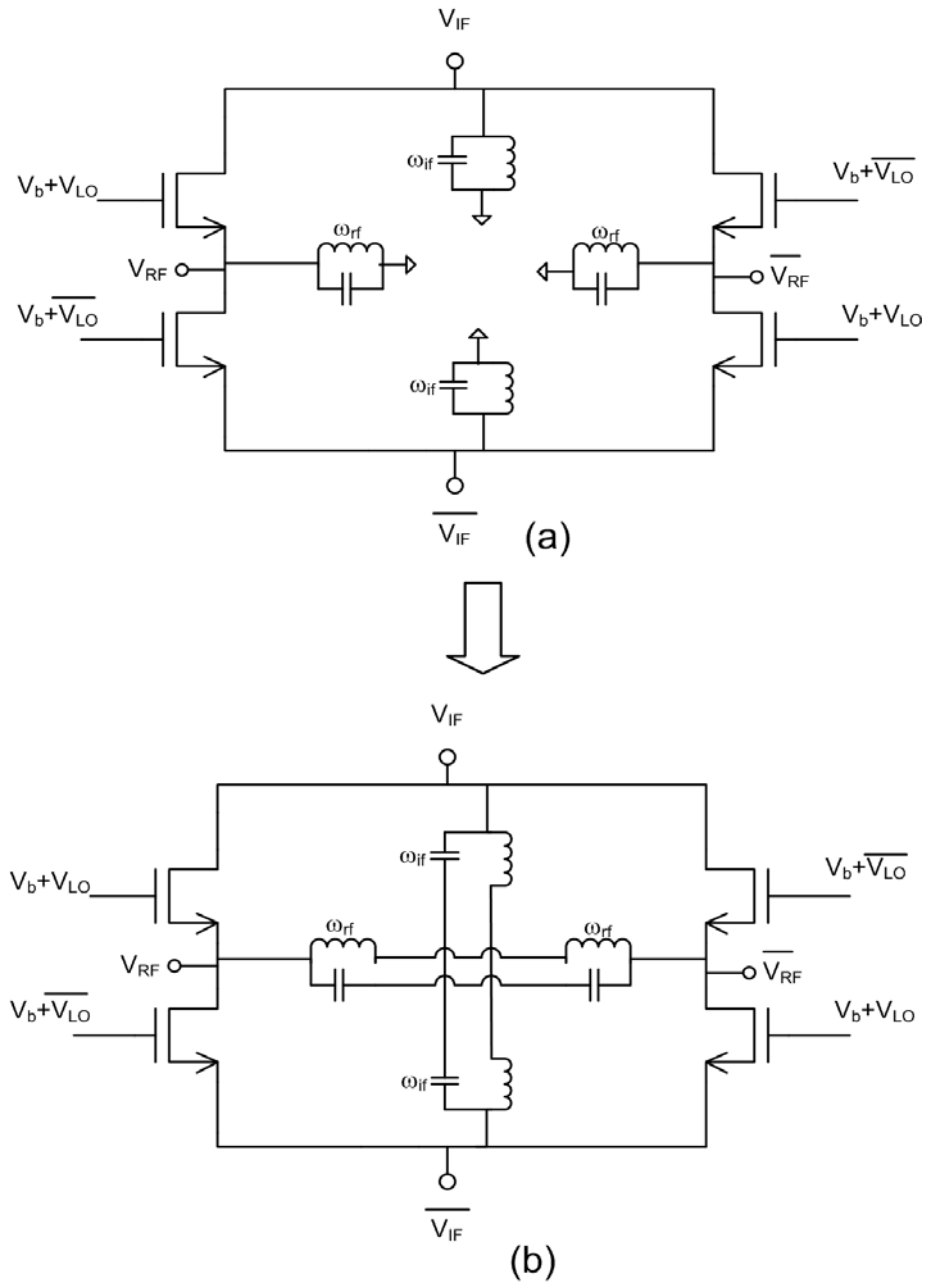


Figure 6.19: A double balanced resistive mixer with parallel resonant tank in RF/IF port.

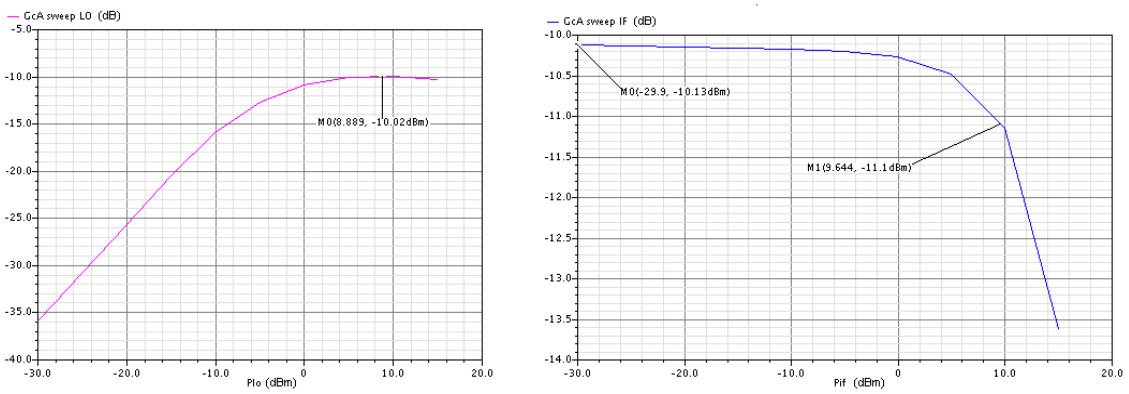


Figure 6.20: Simulated conversion gain and 1-dB compression curve of a double balanced mixer.

Chapter 7

RF CMOS Multiband UWB Transmitter Design and Implementation

In this chapter, a new multiband UWB transmitter design is presented, based on the high-linearity resistive Single Side Band (SSB) mixers discussed in the previous chapter. The SSB mixer design is based on principle of I/Q mixing and image cancellation, so quadrature LO and IF inputs to the mixer are needed. This multiband UWB transmitter approach has several merits: (1) it offers a very fast band switching times in the ns range; (2) the VCO/PLL only needs to operate at a fixed frequency, reducing complexity and enabling higher VCO performance; (3) the digital pulse generator proposed in Chapter Five can achieve very accurate pulse widths at any UWB band carrier frequency since its timing is referenced to the fixed LO frequency. On the other hand, this approach requires SSB mixer and quadrature signals which increase the complexity, and possibly power consumption, of the overall circuit. The proposed design is implemented in JAZZ CA13 $0.13\mu m$ RF CMOS technology.

In the prototype design, the VCO is locked at a fixed frequency of 5 GHz, and the output is mixed with a divided down VCO product to achieve the target carrier frequencies for proof-of-concept [Fig. 7.1 (a)]. As shown, using a divided-by-4 output (1.25 GHz), the single sideband mixer generates sidebands at 3.75 GHz and 6.25 GHz, respectively. Power consumption can be reduced if operating in the 5 GHz

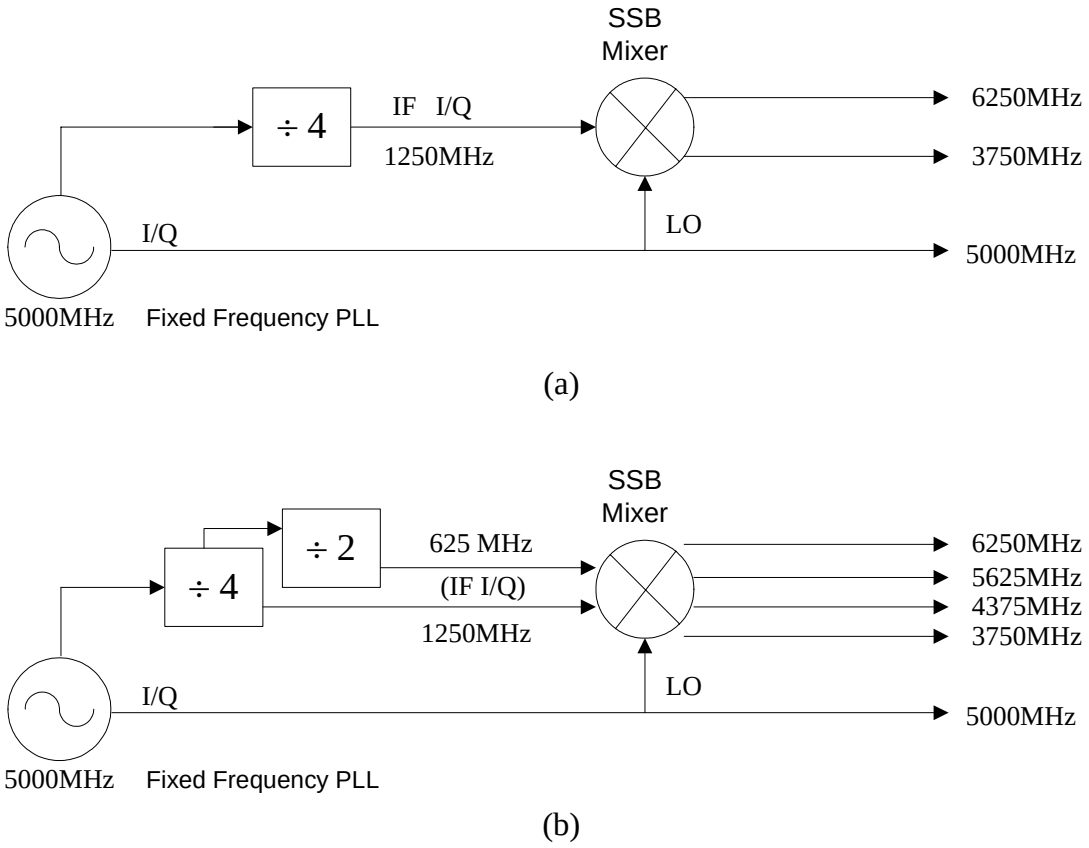


Figure 7.1: The prototype multiband UWB transmitter design: (a) uses a PLL with center frequency of 5 GHz to generate bands at 3.75, 5 and 6.25 GHz; (b) additional bands can be generated with an extra divider.

band by turning off the divider and SSB path. Additional bands at 4375 MHz and 5625 MHz can be generated by adding an extra divided-by-2 divider at the IF output and mixing its output at 625 MHz with the LO at 5000MHz [Fig. 7.1 (b)].

7.1 Single Sideband Mixer

A pair of the double balanced resistive mixers discussed in the previous chapter can be combined to form a single side band mixer, given in-phase and quadrature IF and LO inputs, as shown in Fig. 7.2. Recall that the resistive mixer outputs are RF currents in the transmit mode application. At the output of the SSB mixer, there are two frequency mixing components located at USB and LSB, respectively, from both the I

and Q mixers. If LSB conversion is selected, the LSB currents are in phase, while the USB currents are 180^o out of phase; in other words, when the I-mixer and Q-mixer output frequency components are combined together, the USB currents cancel while the LSB currents reinforce at the output. Since the resistive mixers are functioning as a output current source instead of a switch, the output currents from two mixers may be combined directly at a node, so summing amplifiers are not needed.

For convenience, the mixer with LO_I input is called the $I - mixer$ and the one with LO_Q input is called the $Q - mixer$. If IF_I is mixed with LO_I in the $I - mixer$, and IF_Q is mixed with LO_Q in the $Q - mixer$, the lower sideband (LSB) output is generated:

$$\cos(\omega_{LO} \cdot t) \times \cos(\omega_{IF} \cdot t) + \sin(\omega_{LO} \cdot t) \times \sin(\omega_{IF} \cdot t) = \cos\left[(\omega_{LO} - \omega_{IF})\ t\right] \quad (7.1)$$

On the other hand, if IF_Q is mixed with LO_I and IF_I is mixed with LO_Q, the upper sideband (USB) output is generated:

$$\cos(\omega_{LO} \cdot t) \times \sin(\omega_{IF} \cdot t) + \sin(\omega_{LO} \cdot t) \times \cos(\omega_{IF} \cdot t) = \sin\left[(\omega_{LO} + \omega_{IF})\ t\right] \quad (7.2)$$

By switching the in-phase and in-quadrature components of the input IF applied to the mixer pair (as in Equation 7.1-7.2), either upper sideband or lower sideband operation may be selected. The switching function is through four transmission gate switches shown in Fig. 7.13.

In principle, one sideband may be cancelled completely by the operation of the SSB mixer. However, due to amplitude and phase mismatches at the SSB mixer inputs, the undesired sideband will not be completely cancelled. In addition to the input signal mismatches, device mismatches inside the SSB mixer itself also degrade the sideband cancellation.

A important parameter for a SSB mixer is the image rejection ratio (IRR):

$$IRR = 10\log(\frac{P_{image}}{P_{sig}}) \quad (7.3)$$

To evaluate the impact of the phase and amplitude error, a error input can be introduced into Eq. 7.1 (LSB generation). First, a phase error $\Delta\phi$ (radians) is introduced into the IF input, with zero phase/amplitude error assumed for the LO input and

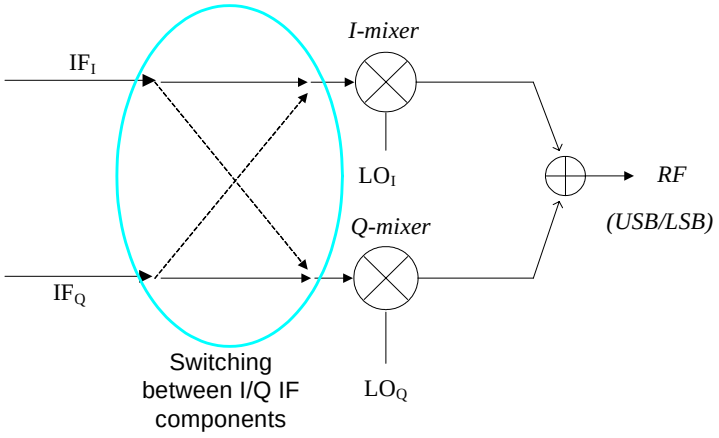


Figure 7.2: A single side band upconversion mixer constructed with two double balanced mixers.

zero amplitude error for the IF input:

$$\begin{aligned}
& \cos(\omega_{LO}\cdot t)\times\cos(\omega_{IF}\cdot t)+\sin(\omega_{LO}\cdot t)\times\sin(\omega_{IF}\cdot t+\Delta\phi) \\
= \;& \cos\left[(\omega_{LO}-\omega_{IF})t\right]-\sin(\omega_{LO}\cdot t)\times\sin(\omega_{IF}\cdot t)\times\left[1-\cos(\Delta\phi)\right] \\
& +\sin(\omega_{LO}\cdot t)\times\cos(\omega_{IF}\cdot t)\times\sin(\Delta\phi) \\
= \;& \cos\left[(\omega_{LO}-\omega_{IF})t\right]-\sin(\omega_{LO}\cdot t)\times\sin(\omega_{IF}\cdot t)\times\left[1-\cos(\Delta\phi)\right] \\
& +\sin(\omega_{LO}\cdot t)\times\cos(\omega_{IF}\cdot t)\times\sin(\Delta\phi) \\
= \;& \cos\left[(\omega_{LO}-\omega_{IF})t\right]-\frac{(\Delta\phi)^2}{4}\cos\left[(\omega_{LO}-\omega_{IF})t\right]+\frac{\Delta\phi}{2}\sin(\omega_{LO}-\omega_{IF})t \\
& +\frac{(\Delta\phi)^2}{4}\cos(\omega_{LO}+\omega_{IF})t+\frac{\Delta\phi}{2}\sin\left[(\omega_{LO}+\omega_{IF})t\right] \qquad (7.4)
\end{aligned}$$

The above derivation assumes that, for small phase error $\Delta\phi$, $\cos(\Delta\phi)\cong 1-\frac{(\Delta\phi)^2}{2}$ and $\sin(\Delta\phi)\cong\Delta\phi$. The squared signal and image amplitudes A^2 and A^2_{imag}, respectively, can then be expressed as:

$$A^2 = \left[1-\frac{(\Delta\phi)^2}{4}\right]^2+\left(\frac{\Delta\phi}{2}\right)^2\approx 1-\left(\frac{\Delta\phi}{2}\right)^2\approx 1 \qquad (7.5)$$

$$A^2_{imag} = \left[\frac{(\Delta\phi)^2}{4}\right]^2+\left(\frac{\Delta\phi}{2}\right)^2\approx\left(\frac{\Delta\phi}{2}\right)^2 \qquad (7.6)$$

The image rejection ratio is given by

$$IRR = 10\log\frac{A_{imag}^2}{A^2} = \left(\frac{\Delta\phi}{2}\right)^2 , \tag{7.7}$$

assuming that both image and signal see the same load impedances.

Next, an amplitude error ΔA is introduced into the IF input in Eq. 7.1 with zero phase/amplitude error assumed for the LO input and zero phase error for the IF input:

$$\begin{aligned} & \cos(\omega_{LO}\cdot t)\times\cos(\omega_{IF}\cdot t) + (1+\Delta A)\sin(\omega_{LO}\cdot t)\times\sin(\omega_{IF}\cdot t) \\ = \;& \cos\left[(\omega_{LO}-\omega_{IF})t\right] + \frac{\Delta A}{2}\left\{\cos\left[(\omega_{LO}-\omega_{IF})t\right] - \cos\left[(\omega_{LO}+\omega_{IF})t\right]\right\} \\ = \;& (1+\frac{\Delta A}{2})\cos\left[(\omega_{LO}-\omega_{IF})t\right] - \frac{\Delta A}{2}\cos\left[(\omega_{LO}+\omega_{IF})t\right] \end{aligned} \tag{7.8}$$

In this case, the image rejection ratio is given by:

$$IRR = \frac{\left(\frac{\Delta A}{2}\right)^2}{\left(1+\frac{\Delta A}{2}\right)^2} \tag{7.9}$$

The image rejection ratios vs. phase and amplitude errors given by equations 7.7 and 7.9 are plotted in Fig.7.3. For an image rejection ratio of greater than 30dB, the IF phase error needs to be less than 3.5^o or amplitude error to be less than 6.5%. The above calculation only considers mismatches from the input source to the mixer. In the designed SSB mixer, there are differential IF inputs (both I and Q) and differential LO inputs (both I and Q); each additional input mismatch further reduces image rejection ratio. In addition, the device mismatches within the SSB mixer introduce additional phase/amplitude errors.

For UWB multiband transmitter applications, a resistive SSB mixer is implemented using two resistive double balanced mixers connected together at the output, with in-phase and quadrature differential input signals applied to their respective ports (Fig. 7.4). Since a resistive mixer functions as a current source at its output, the current outputs of the two mixers can be combined directly to avoid any additional circuits. For the resistive SSB mixer implemented with on-chip inductors and capacitors, the simulated results show a maximum conversion gain of -9.8 dB and an input 1-dB

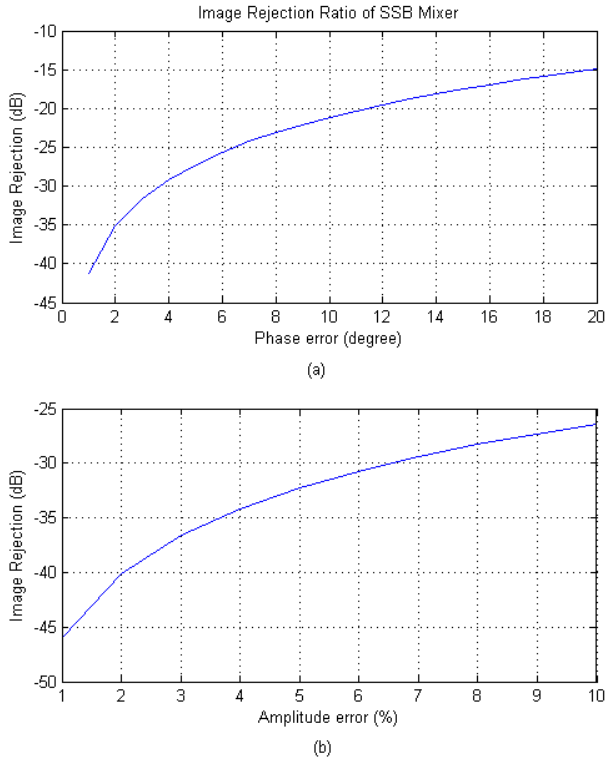


Figure 7.3: Image rejection of SSB (a) phase error $\Delta\phi$; (b) amplitude error ΔA.

compression point of 5.6 dBm. The increase in loss is due to the finite Q factor of the on-chip inductors.

7.2 I/Q Generation

The multiband carrier generation circuit with resistive SSB mixer shown in Fig. 7.1 is implemented in a single chip in $0.13\mu m$ RF CMOS technology along with Quadrature LO source and frequency dividers [75]. The LO I/Q input of the mixer is from a differential quadrature VCO output, while the IF I/Q input to the mixer is from the I/Q output from a divider (Fig. 7.6). The second divide-by-2 divider serves the purpose of both frequency division and I/Q generation.

7.2.1 LO I/Q Generation

There are various methods for I/Q LO generation: one method is using dividers with I/Q outputs; another method is to use a VCO generating the I/Q phase by using two coupled VCOs [76]. One example of the latter case, the parallel coupled QVCO (P-QVCO), generates I/Q signals from two cross-coupled LC-VCOs. In this work, a P-QVCO is implemented for the LO I/Q generation in light of its good I/Q phase balance and phase noise performance [77][78].

The P-QVCO consists two identical VCO cells [Fig. 7.7 (a)] connected in such a way that the first stage output is cross-coupled to the second stage input, and the second-stage output is cross-coupled to the first stage input [Fig. 7.7 (b)]. Inside the individual VCO cores, the cross-coupled transistors provide the -G_m to cancel the tank loss and sustain oscillation. A 90^o phase shift is achieved between the outputs of two VCOs. This is achieved through the combination of differential VCO outputs and cross coupling the second VCO outputs to first VCO inputs. Assume perfect symmetry and equal phase shift θ inside both VCOs with a phase of 0^o at $V_I +$. The output at V_I+ passes through two equal phase shift (2θ) and become V_I- with a phase of 180^o. This leads to a phase shift of 90^o inside of the each VCO. Both cross-coupled PMOS and NMOS pairs are implemented in the VCO core in order to re-use the bias current, providing higher negative resistance at the given current.

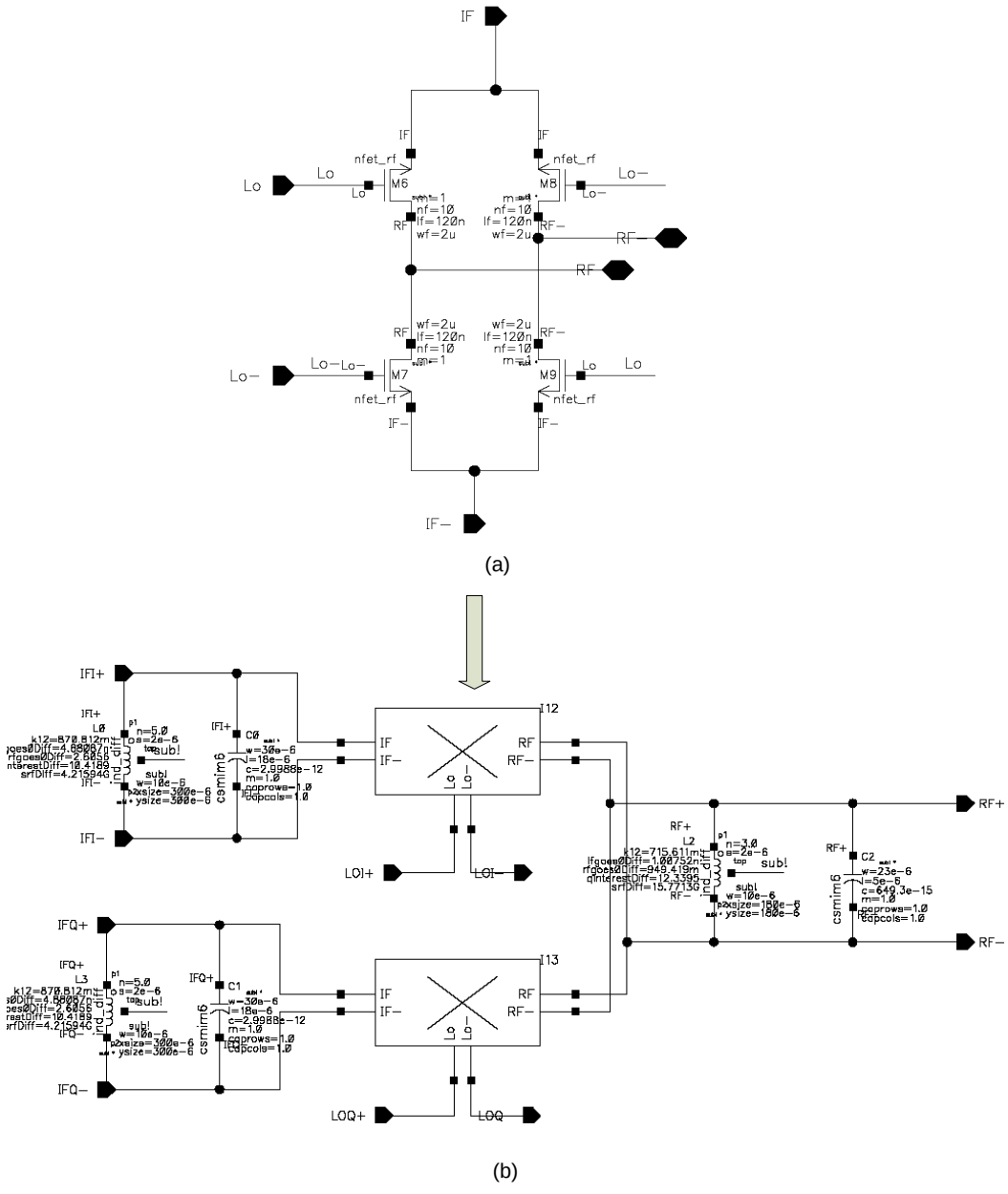


Figure 7.4: Resistive SSB mixer: (a) Mixer core (b)Mixer schematic with current combining at RF output.

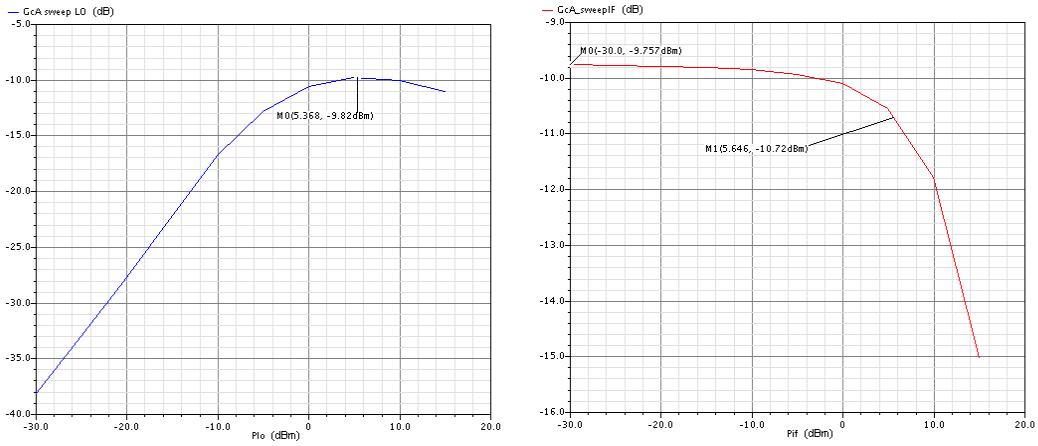


Figure 7.5: Simulated conversion gain 1-dB compression curve of a SSB mixer implemented with real LC tank circuits.

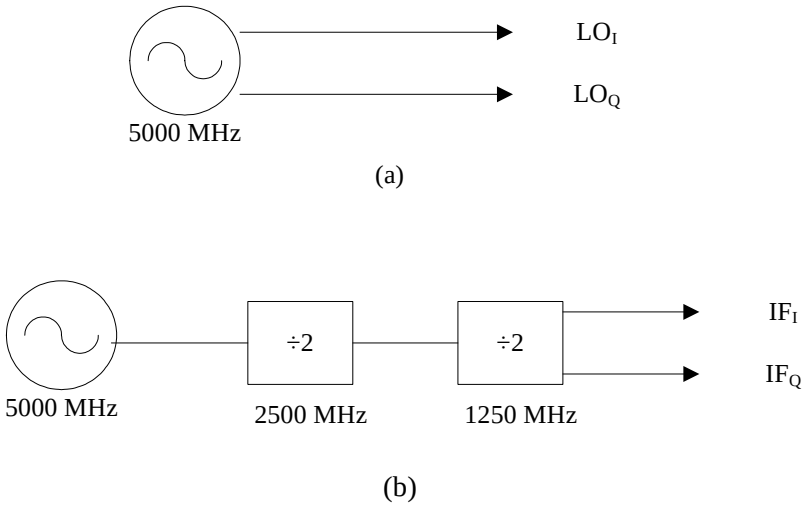
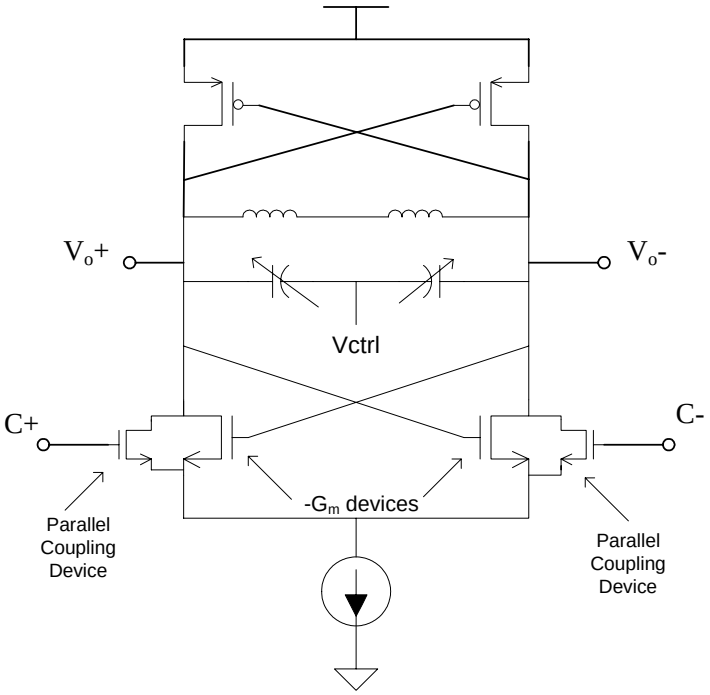
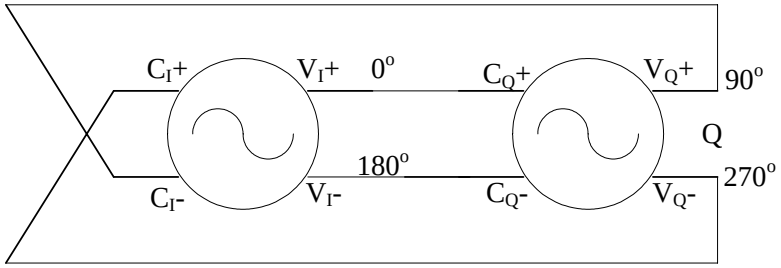


Figure 7.6: I/Q signal generation for both (a) LO and (b) IF inputs.



(a) VCO core



(b) QVCO

Figure 7.7: Simplified schematic of a QVCO: (a) a $-G_m$ VCO cell with parallel coupling devices; (b) connections and relative phases between the two VCOs cores.

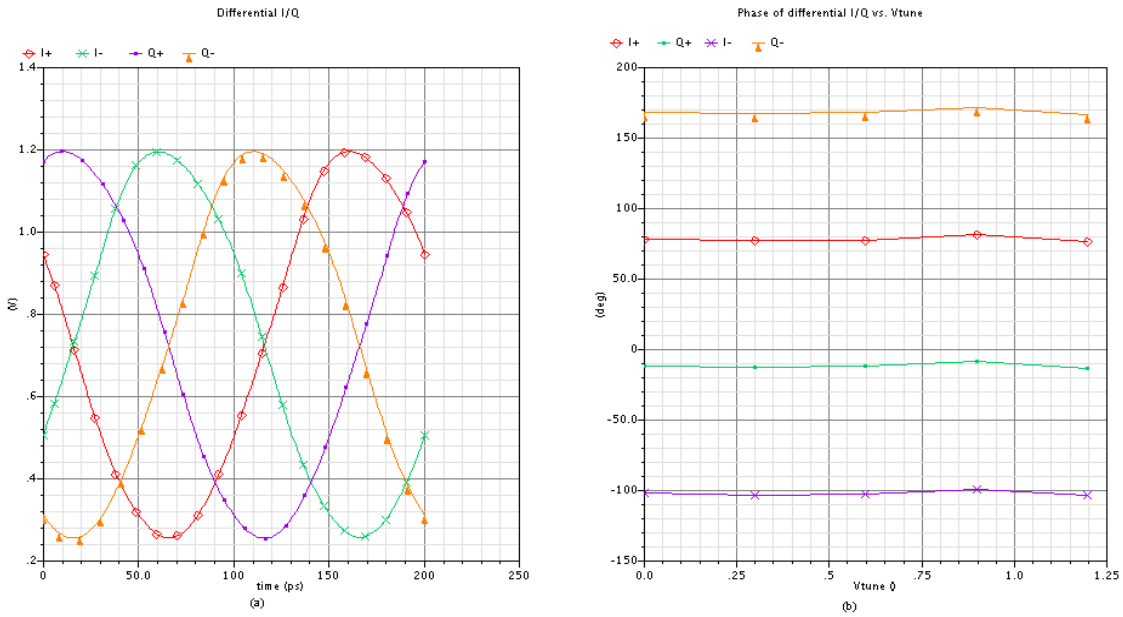


Figure 7.8: RF simulation results of a QVCO in (a) I/Q differential outputs with equal amplitudes; (b) I/Q differential outputs phases of 90^o to each other.

For a parallel QVCO, the phase error is inversely proportional to the coupling coefficient α [77]

$$\alpha = \frac{W_c}{W_{sw}} \tag{7.10}$$

where W_c is the width of the coupling transistor and W_{sw} is the width of the $-G_m$ transistors. To achieve reduced I/Q phase error, α should be made large; however, doing this may increase the phase noise contribution from the coupling devices. A reasonable range of α values, which represents a compromise between the phase error and phase noise, is $1/2 - 1/3$ [77]. In this work, a coupling ratio close to 1/3 is used. The simulated QVCO outputs are shown in Fig. 7.8, and demonstrate very good amplitude and phase matching: Figure 7.8 (a) displays the differential I/Q output from the QVCO in time domain; Figure 7.8 (b) displays the phase of differential the I/Q signal vs. tuning voltage [Vctrl in Fig. 7.7(a)].

Another important factor that must be considered is the current consumption. The simulation results show that overall VCO amplitude decreases as the bias current drops, since its amplitude is proportional to the product of the bias current and equivalent tank parallel resistance. The total bias current is 1.6 mA for the QVCO

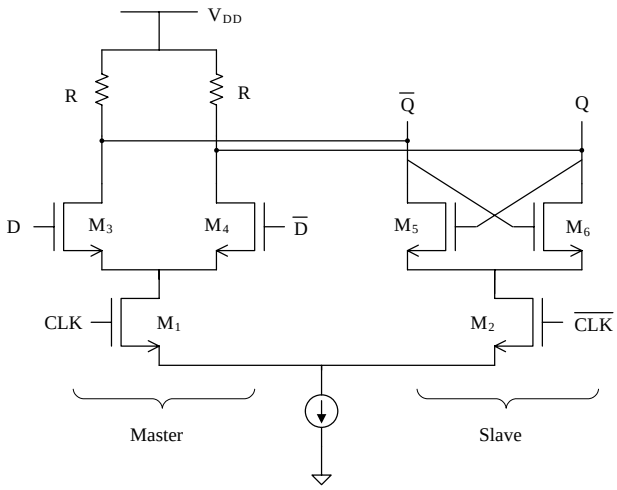


Figure 7.9: Simplified schematic of a source coupled logic cell for the divide-by-2 frequency divider.

with output amplitude of 400mV. The designed QVCO has a voltage supply of 1.2 V.

7.2.2 IF I/Q Generation

The IF input frequency for the SSB mixer is derived from the locked VCO frequency (5 GHz) using two cascaded divide-by-2 dividers. The first divider has its input at 5 GHz and its output at 2.5 GHz. The subsequent divider has two functions: (1) generation of an output frequency at 1.25 GHz from an input of 2.5 GHz; (2) generation of a differential *quadrature* phase output.

Source Coupled Logic (SCL) is used in the divider design (Fig. 7.9) [65]. The SCL takes the differential LO input and generates a differential outputs with a 90^o phase shift between its I/Q outputs with very small phase error. A simplified diagram of the designed source coupled logic frequency divider is shown in Fig. 7.10. It is composed of two master-slave cells (Figure 7.9) controlled by *clock* and $\overline{clock}$, which are the differential LO signal.

The output voltage range of the source coupled logic is $(V_{dd} - IR, V_{dd})$, where I is the bias current, and R is the load resistor (Fig. 7.9). The design of this logic is a trade-off between three factors: the load resistor R, the device size ($M_1 - M_6$ in Fig.

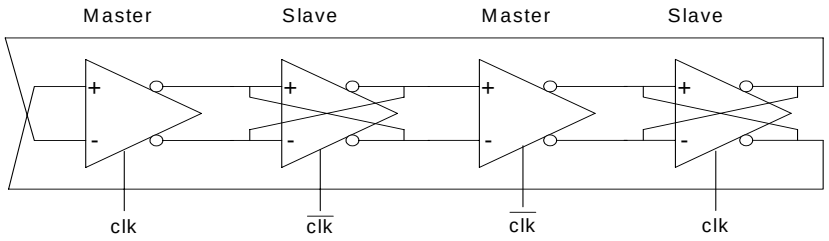


Figure 7.10: Simplified diagram of the common mode frequency divider.

7.9), and the bias current I. The minimum drop across the resistor is determined by the minimum input voltage of the differential pair to switch the current through one of the transistors, which is $\sqrt{\frac{2I}{\mu C_{ox} W/L}}$ (first order approximation). The maximum switching speed is determined by the time constant associated with the resistor value R and the parasitic capacitance at its nodes (Q an $\overline{Q}$). Since power consumption should be minimized, it is desirable to use the minimum possible bias current. At a fixed bias current, a large R will cause the switch to be too slow, while a small R will result in small voltage swing which may not able to toggle the states. Increasing the device size will cause the parasitic capacitance to increase linearly, while the required switching voltage decreases proportional to the square root of device sizes. In this design, a voltage controlled $PMOS$ resistor is used so that the divider speed can be adjusted externally.

The simulated differential I/Q divider time domain output voltage at 1.25 GHz and relative phases are shown in Fig. 7.11. The simulation results show that the phase error of the I/Q output from the divider is quite small (less than 1^o). The two dividers including bias circuit consumes a static current of only 1.06 mA from a 1.2 V voltage supply. This is a significant improvement over the early divider designs presented in Chapter Three.

7.3 Implementation of the Multiband Transmitter

The complete CMOS multiband transmitter design is implemented as shown in Fig. 7.12. The 5 GHz phase locked QVCO provides the reference frequency and I/Q inputs to the LO port of the SSB mixer. The IF I/Q input to the SSB mixer is derived

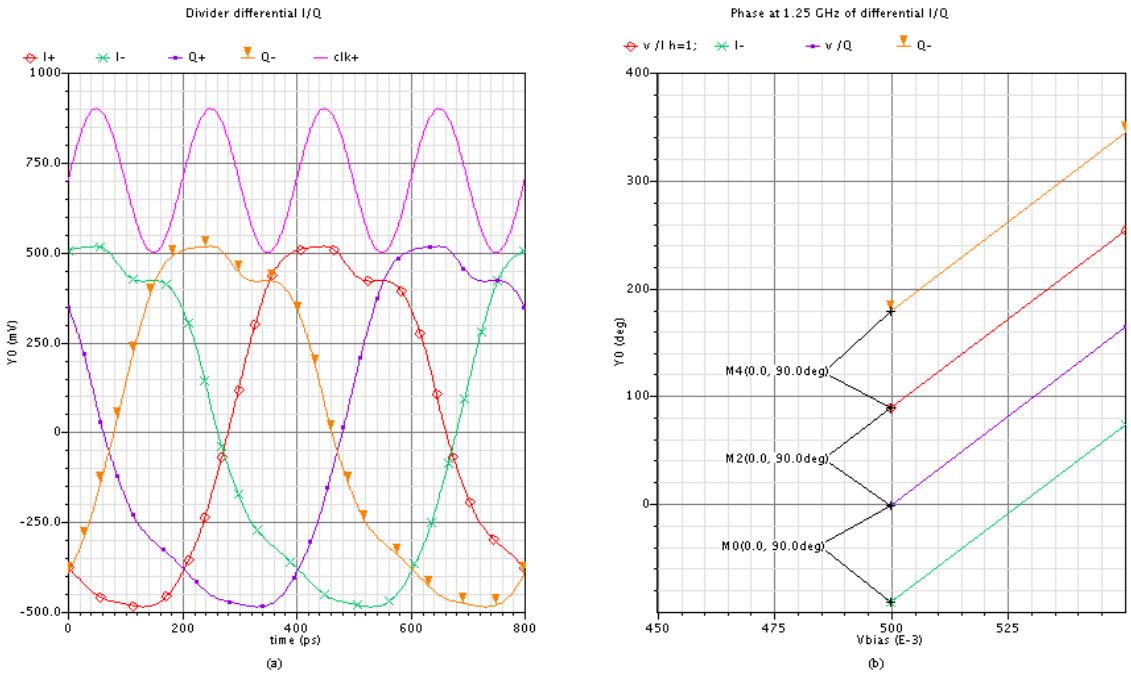


Figure 7.11: SpectreRF simulation of the divider: (a) I/Q differential outputs in time domain; (b)I/Q differential output with 90^o phase relative to each other.

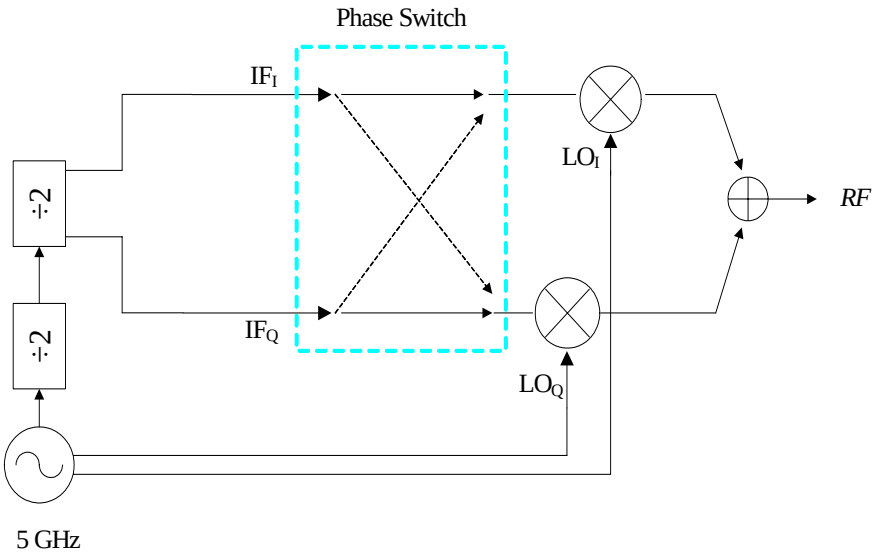


Figure 7.12: Conceptual view of the multiband carrier generation circuit.

from the divider circuit which divides down the frequency from 5 GHz to 1.25 GHz. A switch box (Fig. 7.13) at the IF input of the SSB mixer switches the I/Q phase inputs of the mixer to select either the upper or lower band of the mixer output at 3.75 GHz and 6.25 GHz respectively. At SW high, the I/Q inputs are routed to I/Q outputs; at SW low, the I/Q inputs are switched and routed to Q/I outputs. The complete circuit in Fig. 7.14 is simulated in Cadence SpectreRF. Both upper side band and lower side band outputs are shown in Fig. 7.15. By switching the I/Q phase of the IF input, the transmitter is able to select either upper sideband (6.25 GHz) or lower sideband (3.75 GHz). The simulated results show a image rejection of better than 40 dB for both cases. The results also show good LO level rejection (45 dB); this is very important since the LO is actually one of the possible transmitted bands. The complete circuit consumes a total current of 12mA from a 1.2V supply, dominated by VCOs and buffers.

The new transmitter design based on resistive SSB mixers provide several advantages: it does not require active mixer which constantly consumes power; the system has improved linearity arising from the resistive SSB mixer approach, therefore less harmonic mixing products are generated; the output power level can also be conveniently controlled by the buffers, this results in less power consumption from the buffers .

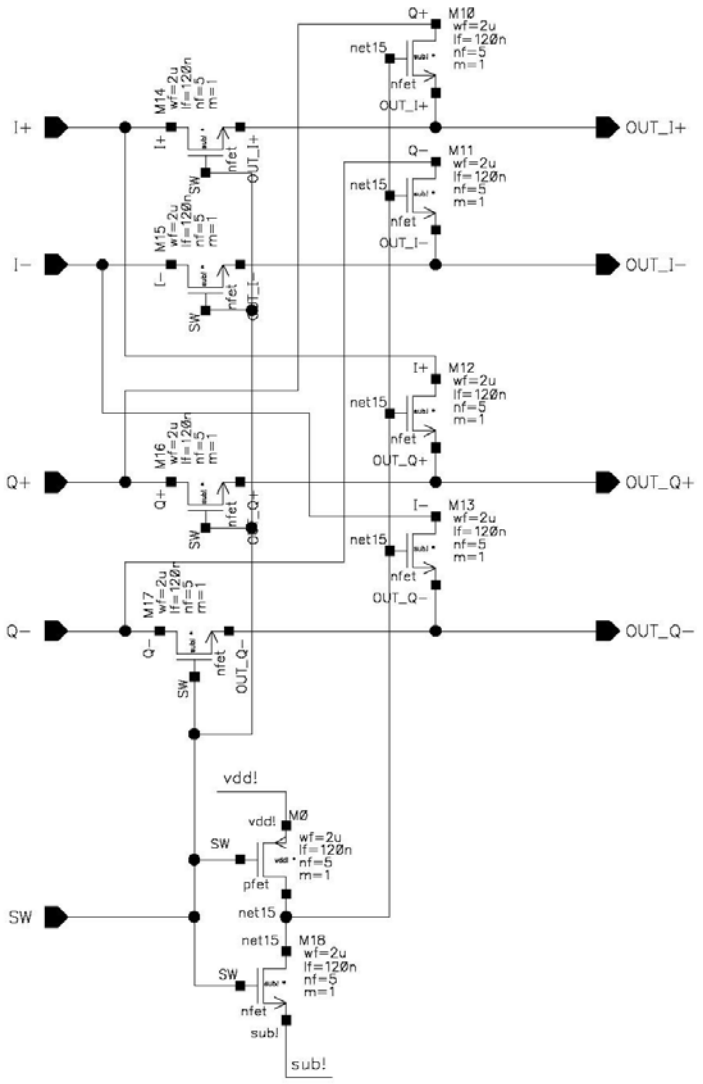


Figure 7.13: Switch "box" for selecting IF I/Q input to the mixer for USB or LSB mixing.

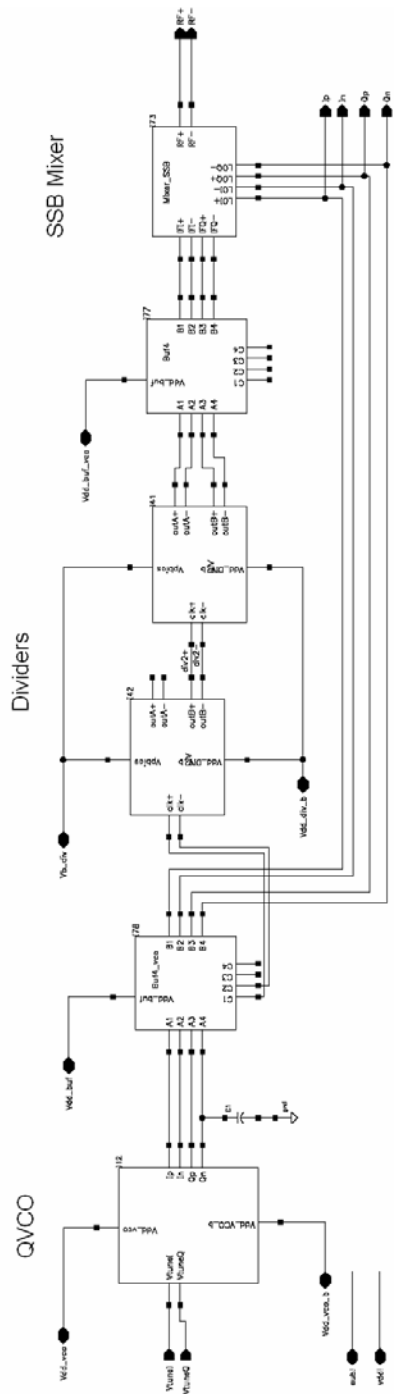


Figure 7.14: Schematic of the complete transmitter design including QVCO (Fig. 7.7), dividers (Fig. 7.10) and resistive SSB mixer (Fig. 7.4).

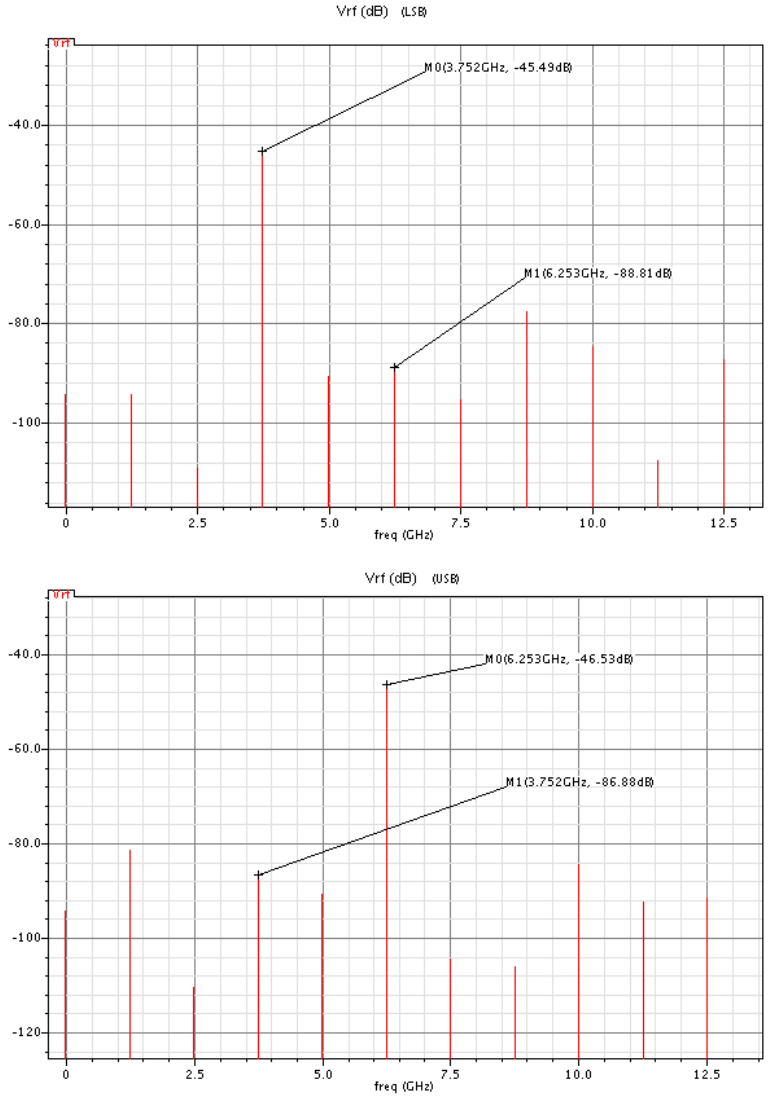


Figure 7.15: Simulated (a) upper and (b) lower side band output spectra of the multiband UWB transmitter.

Pin Name	Function	Pad Type
$RF(+/-)$	SSB Mixer differential output	RF
I_n/I_p	Differential VCO in phase output	RF
Q_n/Q_p	Differential VCO in quadrature output	RF
IP/IN	Differential in phase input	RF
QP/QN	Differential in quadrature input	RF
$V_{tune\_I/Q}$	VCO Phase Control	DC
$V_{b\_\,\mathrm{div}}$	Divider control	DC
V_{dd}	VCO/buffer Power supplies	DC
SW	Band Selection	DC

Table 7.1: Complete transmitter pin assignment.

7.4 Layout

The multiband UWB transmitter has been implemented using Jazz Semiconductor's $0.13\mu m$ RF CMOS $CA13HA$ process. For evaluation purposes, a total of 4 different layouts with similar die area were fabricated (Fig. 7.16): (a) Single sideband generation transmitter (Fig. 7.7, 7.10 and 7.4); (b) Multiband generation transmitter (Fig. 7.7, 7.10, 7.13 and 7.4); (c) SSB mixer with divider (Fig. 7.4 and 7.10); (d) SSB mixer (Fig. 7.4). All four variants are designed to use the same $4mm \times 4mm$ 24 pin QFN package (Fig. 7.17). The complete layout of the multiband UWB transmitter occupies an area of $1.58mm \times 1.17mm$ including pads. Table 7.1 lists all the pads and their functions.

7.5 Summary

This chapters has covered the implementation of a prototype multiband UWB transmitter based on a resistive SSB mixer. The I/Q input generation circuits include a QVCO for the LO and source coupled logic divider for the I/Q IF. The SSB mixer is implemented with two double balanced resistive mixers. An on-chip LC network is implemented to filter out unwanted frequency components. Both upper and lower sideband can be generated by switching the phase of IF inputs. The complete design has been fabricated in JAZZ 130 nm CMOS process. The contribution of this chapter is integrating the resistive SSB mixer concepts developed in Chapter Six into a

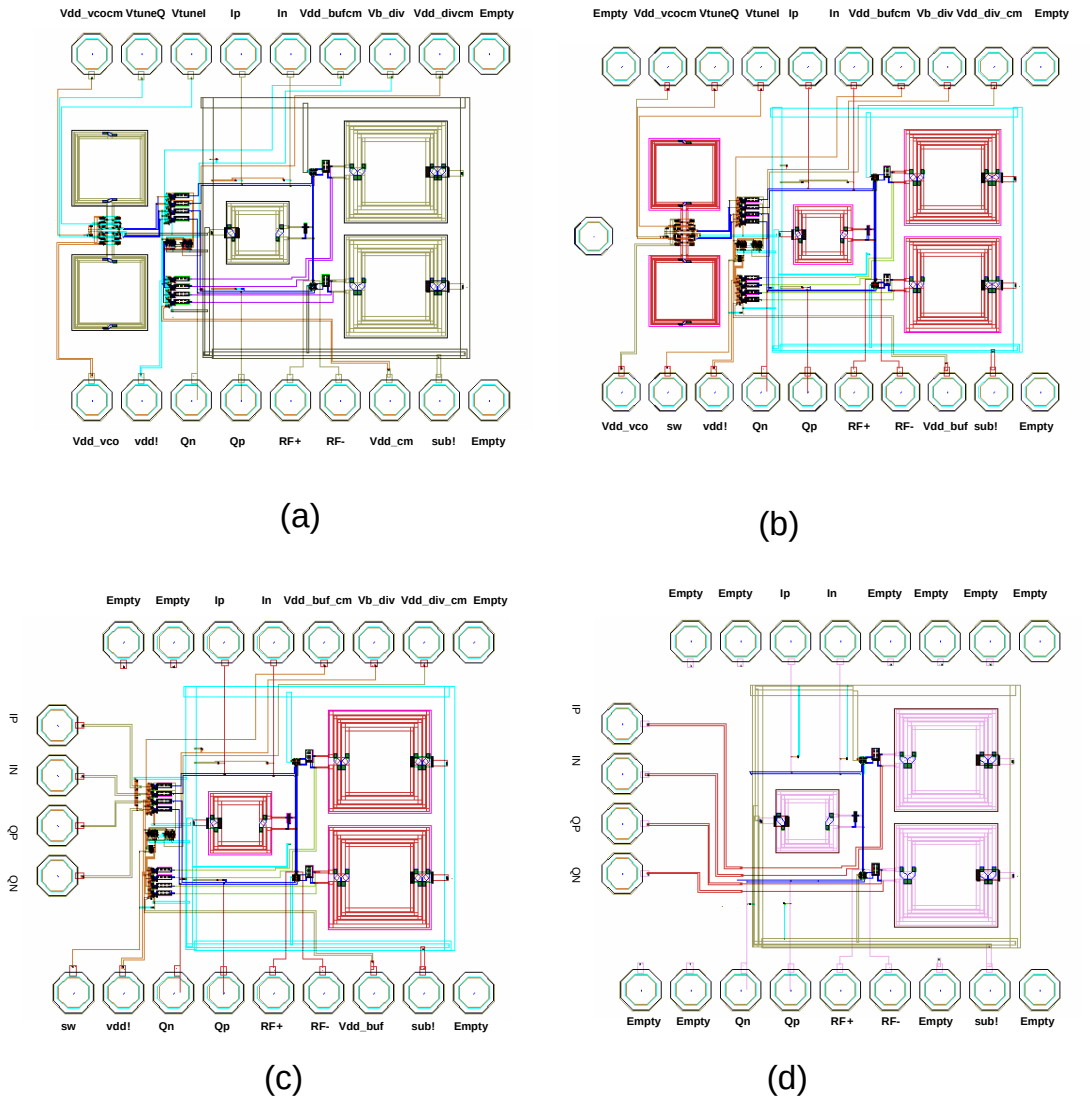


Figure 7.16: Layouts of four multiband UWB transmitter test chips, each chip consists of (a) VCO, divider and SSB mixer; (b) VCO, divider, switch and SSB mixer; (c)SSB mixer with divider; (d) SSB mixer.

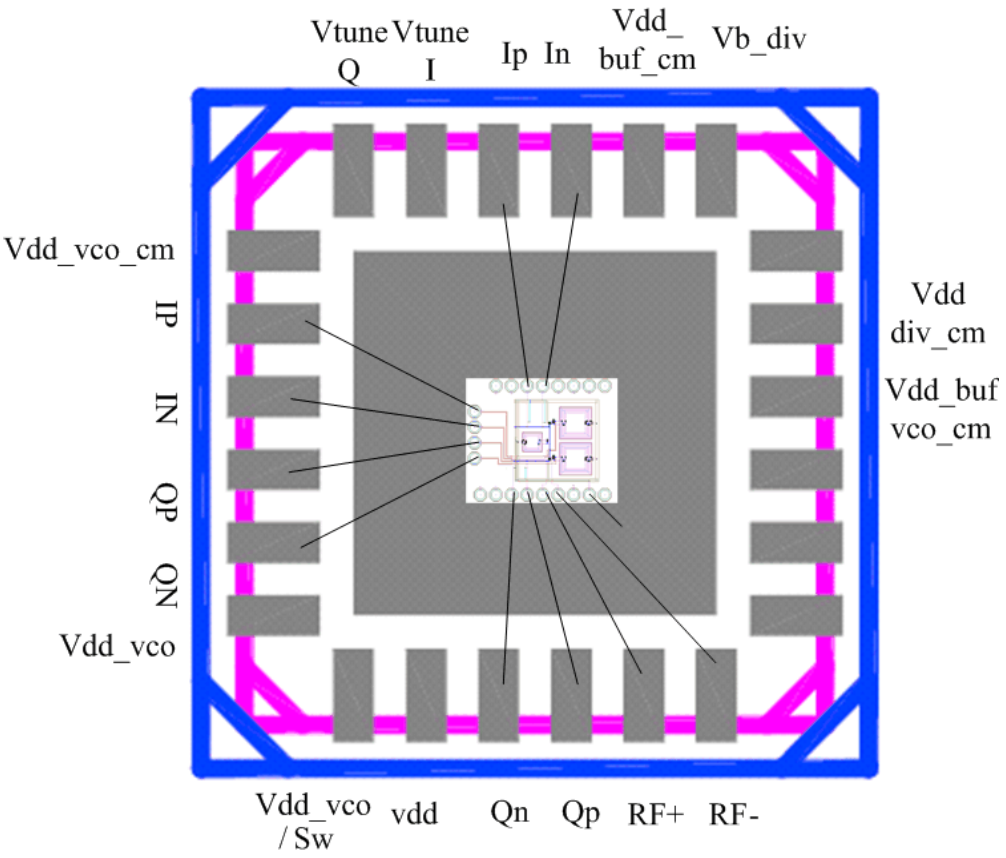


Figure 7.17: A 24 pin QFN package with pin allocations shared by 4 different circuits [one of the four variations is shown (Fig. 7.16(d)].

complete transmitter architecture. This transmitter is different from a conventional Gilbert cell mixer based transmitter[61][63] since it utilizes the linear performance and direct current combining capability of the SSB resistive mixer. It can achieve lower overall power consumption, flexible power control, and excellent linearity.

Chapter 8

Conclusions and Future Work

The main focus of this dissertation has been the development of Si-based UWB transmitters targeting wireless sensor networks and communications applications. The proposed UWB transmitter IC designs may be adapted for use in RF front ends to meet the IEEE 802.15.4a task group requirement for low rate WPAN application with high precision ranging/location capabilities. The multiband carrier generation IC based on SSB mixers, dividers and quadrature VCO may also be adapted to meet the WiMedia MBOA high data rate standard.

8.1 Conclusions

In this work, a SiGe BiCMOS multiband UWB transmitter featuring a switched capacitor tank VCO core was first designed and fabricated using Freescale's HIP6WRF $0.18\mu m$ BiCMOS process. The VCO demonstrated a wide measured tuning range from 3.72 to 7.05 GHz and consumed 5.9mA current at the high frequency band. The VCO tuning curve was not linear due to the nonlinearity of the tank switches, which was eliminated in a subsequent design revision with improved switched tank design. The prescaler circuit of the PLL was designed using common mode logic for its fast switching capability; however the design consumed an excessive 11mA of current. This may be alleviated by designing the 2nd and 3rd stage divider in the prescaler with reduced DC current since they are operating at lower speed. The integrated phase locked loop was demonstrated to lock at its high frequency band with the de-

signed divider ratio of 80. A pulse generator using delay lines for gated timing control of 4ns was also integrated in this transmitter to generate the target 500 MHz first null bandwidth. However, the measured results showed an actual pulse width of 6 ns generated by the pulse generator circuit. This timing inaccuracy is attributed to the device mismatches and process variations, and motivated the design of a new digital pulse generator circuit approach. In addition, current consumption and switching time issues were to be mitigated by using a fixed frequency source and SSB mixer approach for multiband generation.

Subsequently, an improved UWB transmitter employing a fixed center frequency PLL at 4 GHz, reduced power consumption, and improved mismatch-insensitive pulse generator was designed and fabricated in the Jazz CA18HR 0.18μm CMOS process. The VCO has a measured output level of -6.5 dBm with simulated phase noise of -104dBc/Hz at 1MHz offset. The divider circuits were designed using lower power consumption TSPC logic and drew less than 1mA total current. The novel pulse generator design featured all digital logic and derived its timing from the fixed VCO frequency at 4 GHz, therefore generating precise 1ns pulses at the transmitter output.

A new multiband UWB transmitter was also designed employing a fixed frequency VCO (PLL). Multiband operation is achieved using an integrated resistive SSB-mixer with excellent linearity and frequency dividers; the frequency of operation is switched among three frequency bands by switching the I/Q inputs of the SSB mixer. The design uses dividers and a quadrature VCO to generate I/Q IF and LO inputs to the SSB mixer for selecting either the USB or the LSB frequency component. This circuit was designed and fabricated in Jazz CA13HA 0.13μm CMOS process. It has a chip area of 1.6mm x 1.2 mm and consumes 12mA current total from a 1.2V power supply. The simulated SSB mixer design has a maximum conversion gain of -8.5 dB and input 1-dB compression point of 6 dBm which is excellent compared to existing mixer approaches. The simulated image rejection ratio of the entire multiband generation circuit is better than 40 dB. Various configurations of the multiband transmitter including standalone mixer have been fabricated and await testing.

This work has laid the ground work for single-chip RFIC transmitters for emerging UWB applications. Various components of the transmitter design, including switched tank VCO, phase locked loop, pulse generator, and resistive single side band mixer have been thoroughly investigated and researched. During the design process, various

problems surfaced, such as pulse generator timing control accuracy and switched tank VCO switching control issues; solutions to those problems were proposed and realized through subsequent design efforts.

The major contributions of this work include: implementation of a fully integrated multiband UWB transmitter with embedded phase-locked switched-tank VCO capable of wide frequency tuning; demonstration of an all digital pulse generator capable of generating accurate one-nanosecond pulse trains in the presence of various mismatches; investigation of resistive SSB mixer topologies and implementation in an improved UWB multiband generation architecture.

8.2 Future Work

Future work following from this dissertation effort includes:

- Complete characterization of the $0.13\mu m$ RFCMOS SSB mixer and UWB multiband generation circuit designed in Chapter 7.

  The fabricated chips are shown in Fig. 8.1 (corresponding to the layouts shown in Fig. 7.16). All four different dies are to mounted on 24 pin QFN packages and shared same testing board. Measurements of the all fabricated chips are to be completed in the near future.

- Integration of T/R switches and LNA down-conversion mixers to realize fully integrated UWB transceiver frontends.

- Modification of the pulse generator circuit to potentially implement pulse positioning modulation techniques (Fig. 8.2). By adding a NOR gate at the output of the pulse generator, the pulse location can be varied and used for binary coding.

- Implementation of UWB position location system for wireless sensor network applications based on the complete transceiver design (Fig. 1.8).

The prototype UWB transmitter developed in this work can be adapted and implemented in various wireless sensor network environments including video sensor,

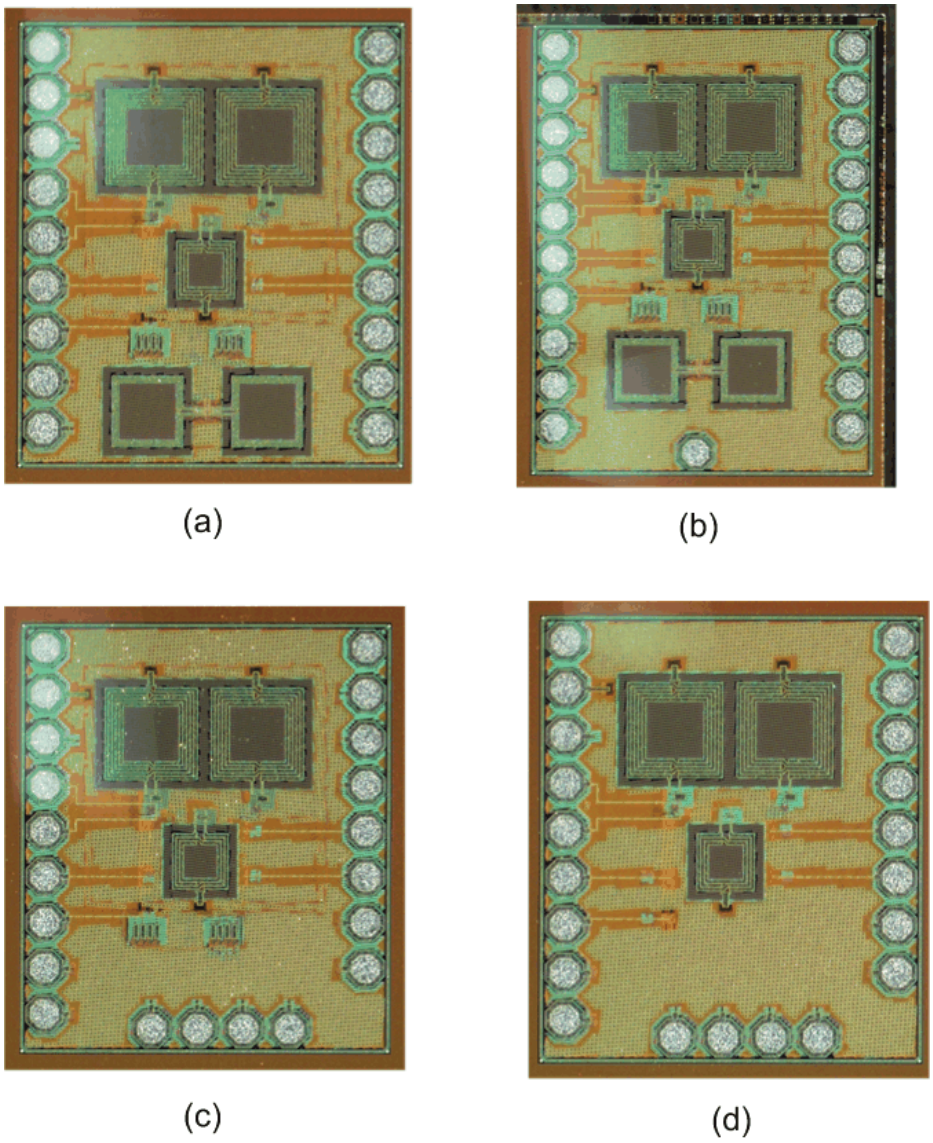


Figure 8.1: A die micrograph of the multiband UWB generation circuit.

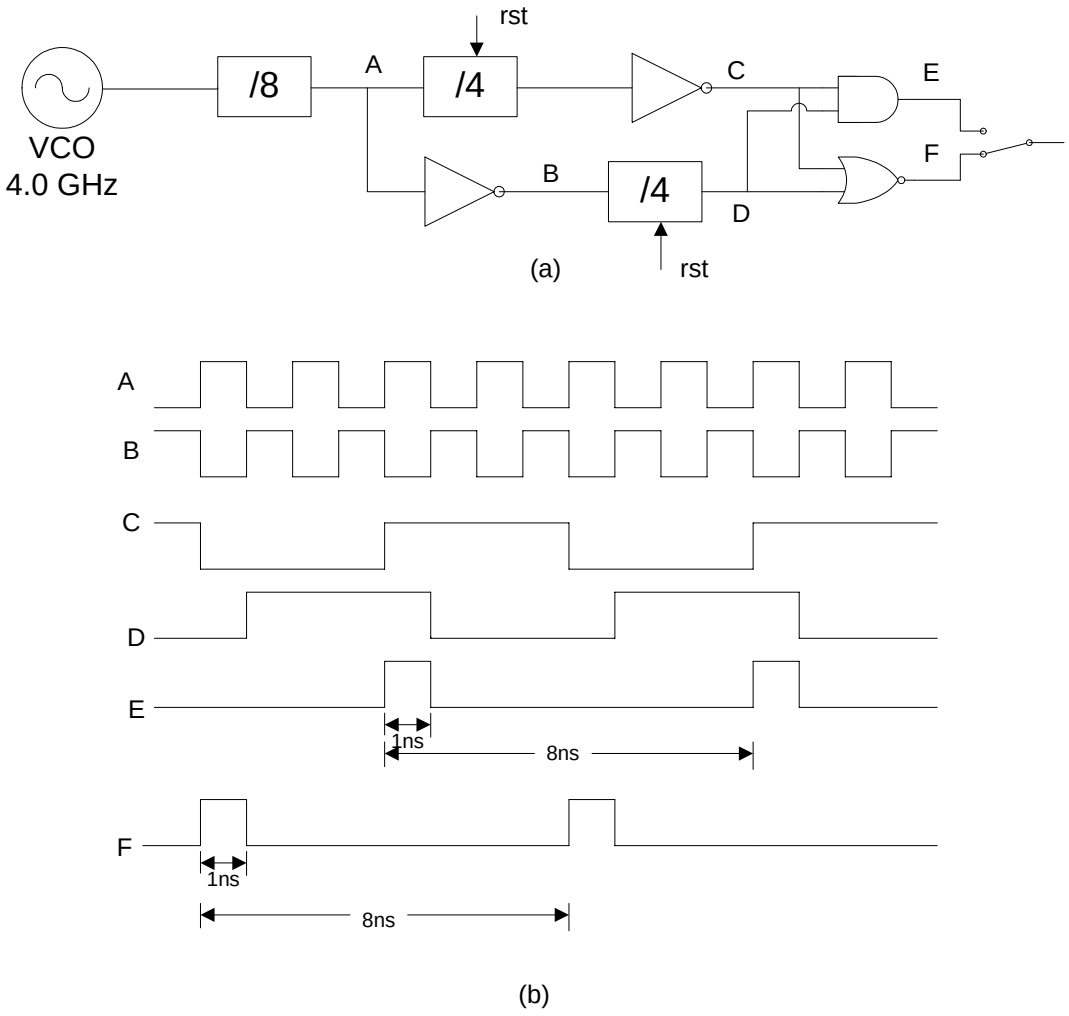


Figure 8.2: Modified digital pulse generator for binary pulse position modulation.

RFIDs, monitoring sensors etc. With additional functions such as RF front end receiver and position location capability, this work can be implemented to even broader applications like intelligent sensor nodes. The SSB mixer in this work has the potential to provide single side band mixing and rejecting image frequency, while provide high linearity and consume no DC power. A resistive based SSB mixer has the potential for UWB transmitters and 60 GHz transceiver applications.

Appendix A

Pulsed DPSK Modulation

The modulation technique selected for the impulse radio based sensor network is Differential Binary Phase Shift Keying (DPSK) [79]. A DPSK modulated signal $b(t)$ with a chip rate of 100 Mbps and carrier frequency ω_0 is:

$$b(t) = A_1 \cos[\omega_0 t + D_p m(t)] \tag{A.1}$$

where A_1 is the amplitude, ω_0 is the carrier frequency, D_p is the phase change between each symbol, $m(t)$ is a random chip [+1,-1] with chip rate of $100Mbps$. Assuming perfect square wave shaping, this DPSK signal has a first null bandwidth of 200 MHz in the passband.

To generate the mandated 500 MHz bandwidth, square-pulse-train shaping function $r(t)$, with an on-state of 4ns and an off-state of 6ns, are generated to shape the DPSK modulated signal:

$$r(t) = \begin{cases} A_2 & 10N < t < 10N + 4 \ (ns) \\ 0 & 10N + 4 < t < 10N + 10 \ (ns) \end{cases} \quad N \in (0, \infty) \tag{A.2}$$

where A_2 is the amplitude, N is the number of period. The first null bandwidth of the pulsed DPSK signal is 500 MHz controlled by pulse width of $r(t)$. Every bit is sent as a short pulse of 4ns with a period of 10ns. This results in a 40% duty cycle of the transmitted signal. Each data pulse is either in-phase (0^o) or out-of-phase (180^o)

with respect to each other. The pulse shaped DPSK signal $w(t)$ can be expressed as:

$$\begin{aligned} w(t) &= b(t) \cdot r(t) \\ &= A\cos[\omega_0 t + D_p m(t)]r(t) \\ &= Ar(t)\cos(\omega_0 t)\cos[D_p m(t)] - Ar(t)\sin(\omega_0 t)\sin[D_p m(t)] \\ &= -Am(t)r(t)\sin(\omega_0 t) \end{aligned} \tag{A.3}$$

where $D_p = \frac{\pi}{2}$ for DPSK modulation, and $w(t)$ can be expressed as the real part of a complex function:

$$w(t) = \text{real}(jAm(t)r(t)e^{j\omega_0 t}) \tag{A.4}$$

$$g(t) = jAm(t)r(t) \tag{A.5}$$

and $g(t)$ is the complex envelope of $w(t)$. The power spectral density function (PSD) for $w(t)$ is the convolution of the PSDs of $m(t)$ and $r(t)$:

$$P_g(f) = P_m(f) * P_r(f) \tag{A.6}$$

where $P_m(f)$ and $P_r(f)$ are the power spectrum density function of $m(t)$ and $r(t)$, respectively. Without pulse shaping, the PSD of BPSK signal is therefore:

$$P_m(f) = A^2 T_b(\frac{\sin \pi f T_b}{\pi f T_b})^2 \tag{A.7}$$

where T_b is the bit period of baseband signal. $P_m(f)$ has a first null bandwidth of 200 MHz (Fig. A.1).

As described above, the pulse shaping control signal $r(t)$ have a periodic rectangular pulse with a 40% duty cycle. This can be expressed using a Fourier series:

$$r(t) = \sum_{-\infty}^{+\infty} c_n e^{jn\omega_0 t} \tag{A.8}$$

$$\begin{aligned} c_n &= \frac{1}{T_0}\int_a^{a+T_1} w(t)e^{-jn\omega_0 t}dt \\ &= \frac{jA}{2\pi n}(e^{-jn\cdot 0.8\pi} - 1) \end{aligned} \tag{A.9}$$

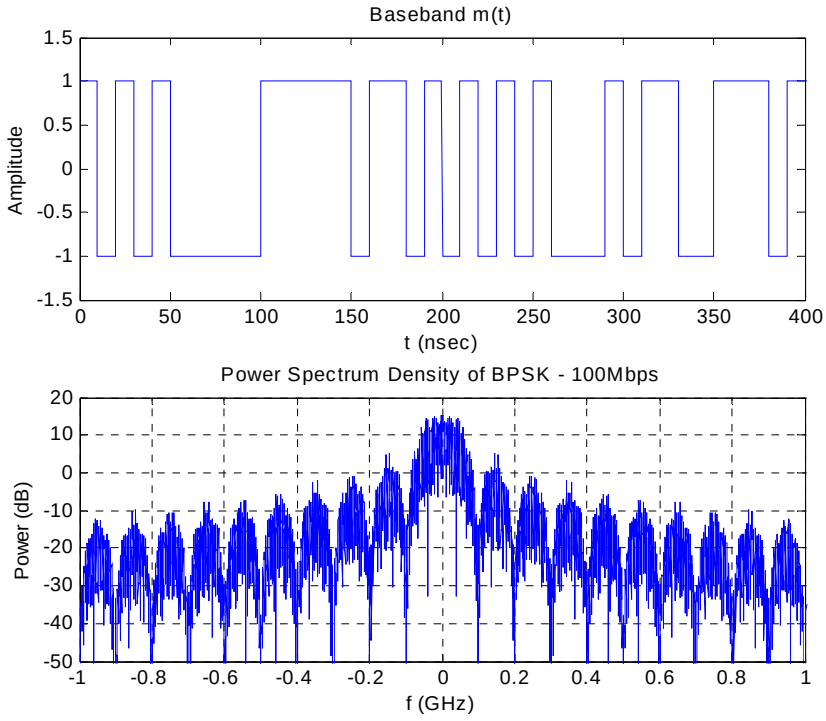


Figure A.1: Power spectral density simulated using Matlab of a random baseband input m(t) at 100 Mbps (200 MHz first null bandwidth).

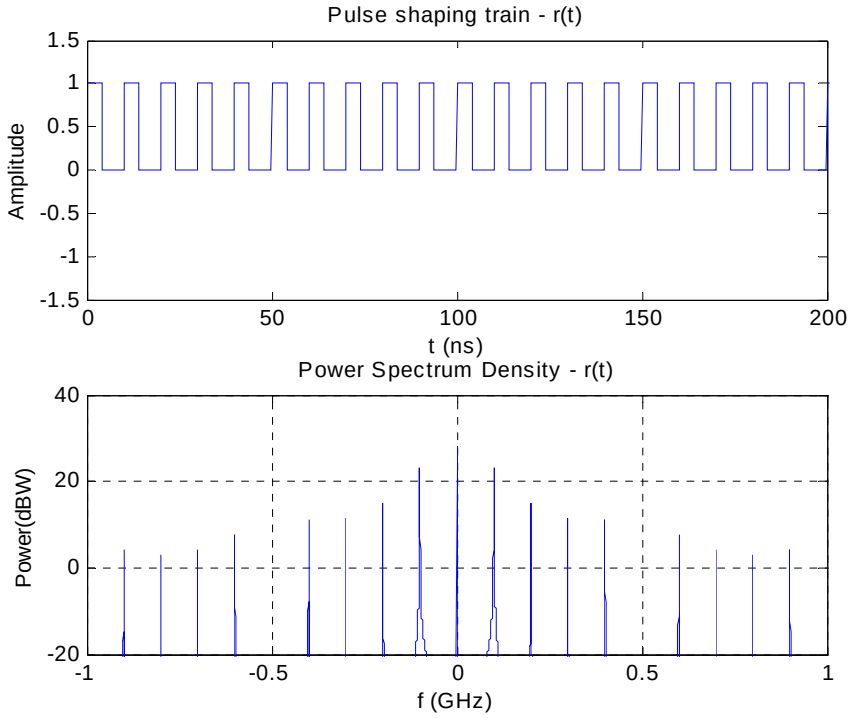


Figure A.2: Power spectrum density of pulse shaping signal r(t), pulse width is 4ns and period is 10ns.

where c_n is the Fourier coefficient of the n^{th} harmonic, T_0 is the pulse repetition period ($10ns$), ω_0 is the fundamental frequency $2\pi/T_0$, and T_1 is the pulse on-state time ($4ns$). The power spectrum of the pulse shaping signal $r(t)$ has discrete lines separated by ω_o, which the frequency of the pulse train. The first null frequency should appear when n equals 2.5 from equation A.9. However, since n can only be an integer number, the first null appears at n equals 5 (Fig. A.2). The spectral density function of the baseband signal $g(t)$ is the convolution of the two spectrums of $m(t)$ and $r(t)$. The baseband spectrum has the expected first null bandwidth of 500 MHz (Fig. A.3).

The transmitted passband signal power spectral density $P_s(f)$ is simply the baseband spectrum shifted by $\pm f_c$, where f_c is the carrier frequency.

$$P_s(f) = \frac{1}{4}[(P_g(f - f_c) + P_g(f + f_c)] \tag{A.10}$$

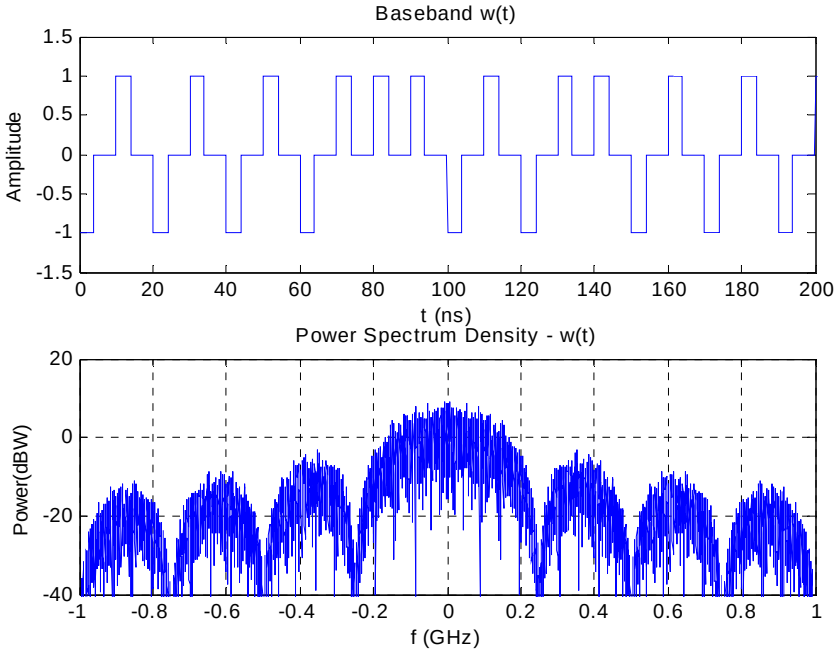


Figure A.3: Power spectral density of pulse shaped BPSK at 100 Mbps.

The power spectrum shown in Fig. A.3 requires that the data input $m(t)$ to be random. If $m(t)$ is a constant or slow varying input, then it can be approximated as constant in equation A.5. Therefore, the complex envelope function is:

$$g(t) = jAr(t) \tag{A.11}$$

As a result, the baseband spectrum will only show discrete frequency lines separated by 100 MHz. The transmitted signal spectrum is then simply that of Fig. A.2 shifted by the carrier frequency. The first null frequency $\pm 250MHz$ is not present in the spectrum due to the $100MHz$ discrete frequency lines. Instead, the first null frequency appears at the 5^{th} harmonic with $\pm 500MHz$. Matlab simulations (Fig. 1.12) with random data inputs show the expected 500 MHz first null bandwidth.

Appendix B

PLL for 8 GHz

A modified transmitter based on phased locked VCO at 8 GHz with the digital pulse generator is designed and fabricated. Due to the speed limitations of the TSPC logic used in 4GHz transmitter design, another prescaler proposed by Razavi is used in the 8 GHz UWB transmitter (Figure B.1). This prescaler requires two differential inputs with relatively high swing levels. The outputs of the prescaler are four signals with 90^o phase difference to each other (Figure B.2). At any given time, only one of the four outputs can be high. As clk or clk- goes low, one of the outputs will go high and the other output will be pulled down by the previous high output. Due to the static pull current, this prescaler consumes $1.5mA$ current, more than the TSPC logic. However, it is significantly less than the SCL since only two NMOS transistors are on at any given time. The outputs have a period of two times the clock period and a duty cycle of 1/4.

The modified 8 GHz PLL has a simulated lock in time $\sim$ 1.6 μs (Figure B.3) and a bandwidth close to the 4 GHz PLL. By designing a PLL with large bandwidth, the loop filter inside the PLL can use relatively small capacitors for small size and ease of integration.

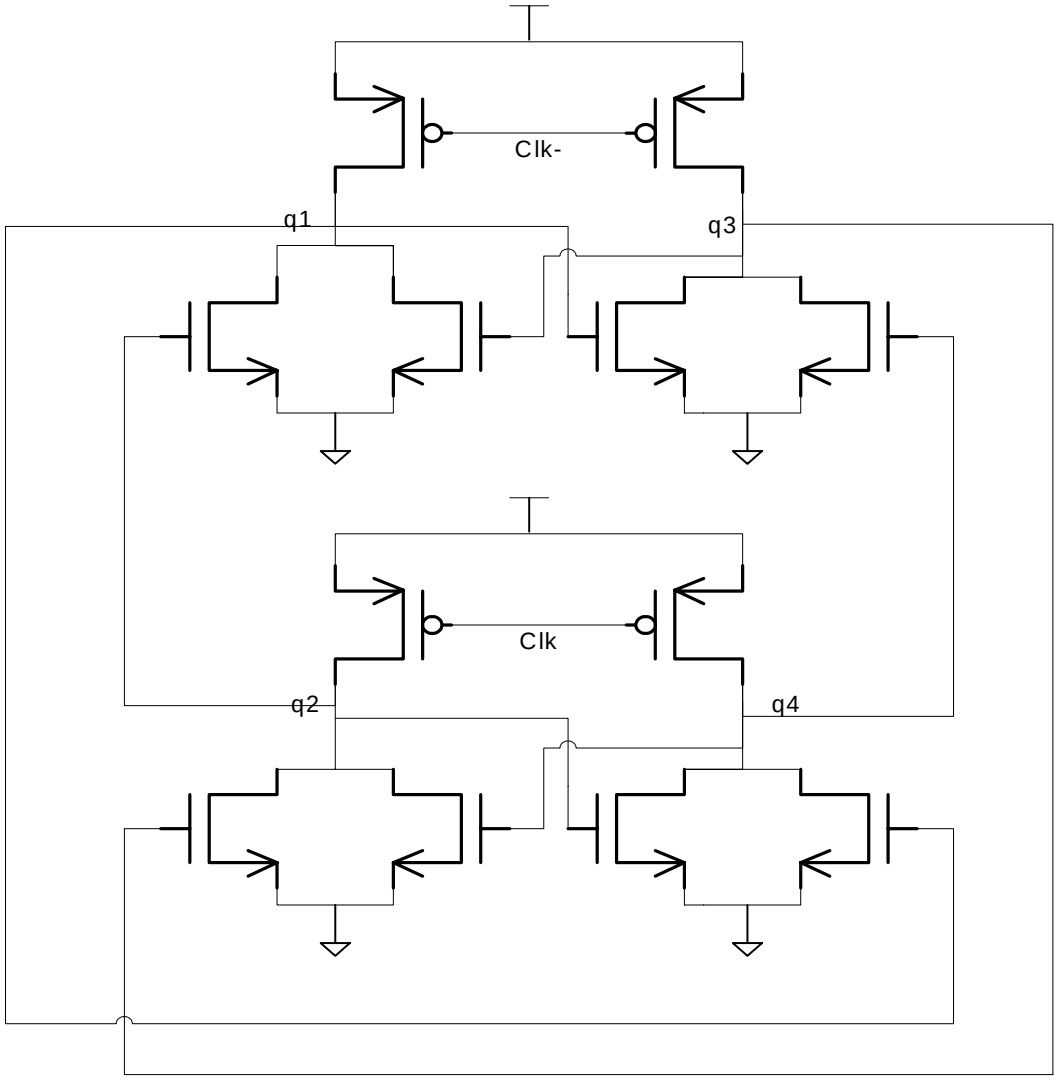


Figure B.1: Schematic diagram of the quadrature prescaler.

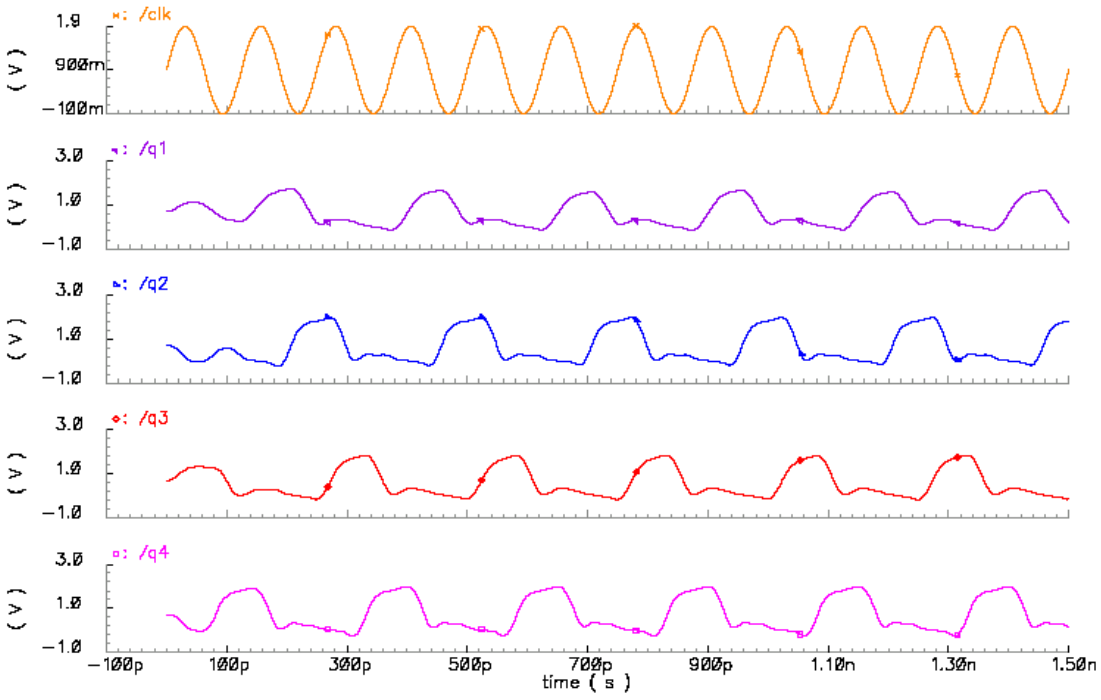


Figure B.2: Simulated quadrature outputs of prescaler.

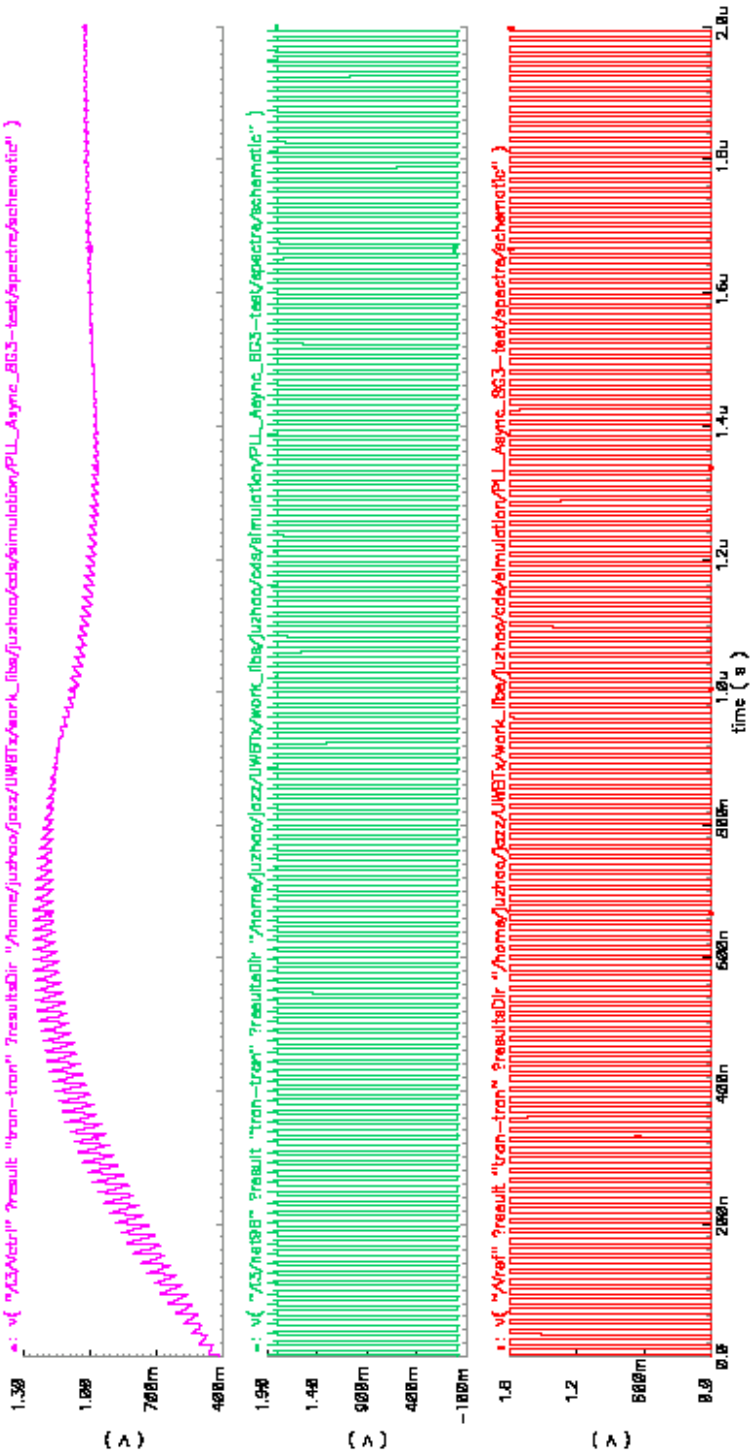


Figure B.3: Simulated output waveforms of control signal and phase detector inputs from 8GHz PLL.

Appendix C

Two Stage OPAMP

The operational amplifier used in the capacitor to voltage converter is implemented utilizing the two stage topology (Fig. C.1) [80]. The first stage is a differential input amplifier $M1 - M2$ driving the active load $M3 - M4$. The active load $M3 - M4$ not only provides high load resistance to the output of the differential pair, but also converts the differential output voltage from $M1 - M2$ to signal ended voltage V_o. The second stage is a common source amplifier $M5$ biased by a current mirror. The bias transistor $M6$ also presents a high resistance to the output of $M5$. To improve the stability of the operational amplifier, a parallel feedback is implemented at the second stage by a series RC circuit connecting the OPAMP output to its input.

The small signal equivalent model of the differential stage is shown in Fig. C.2. The voltage and current of $M4$ can be calculated:

$$V_{gs4} = -\frac{g_{m1}}{g_{m3}}\frac{V_{in}}{2} \tag{C.1}$$

$$I_{d4} = g_{m4}V_{gs4} = -g_{m1}\frac{V_{in}}{2} \tag{C.2}$$

$$I_{d2} = -g_{m1}\frac{V_{in}}{2} \tag{C.3}$$

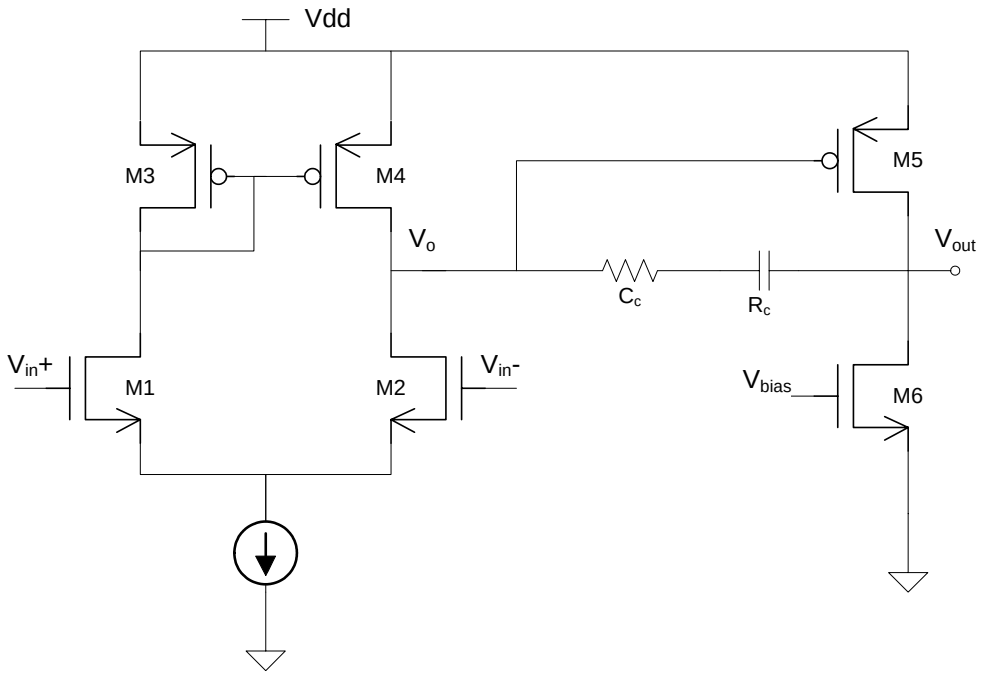


Figure C.1: Schematic of two stage opamp for capacitor to voltage conversion circuit.

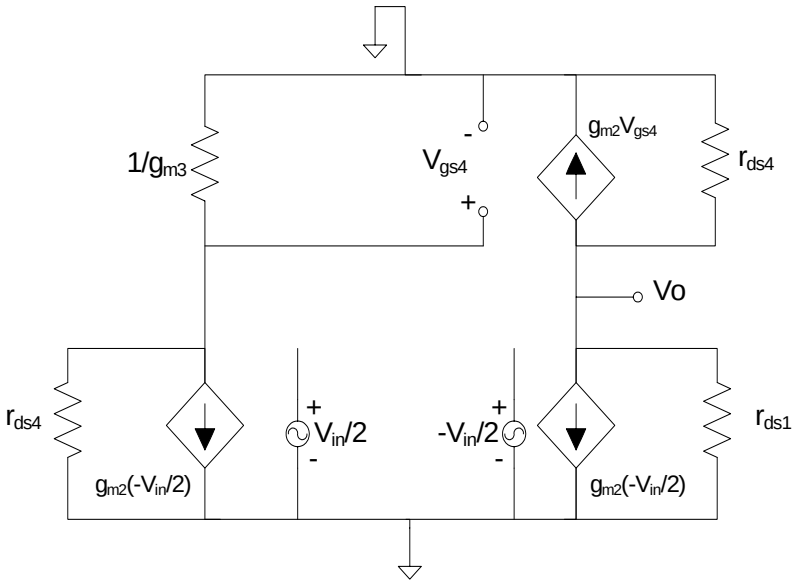


Figure C.2: Differential small signal model of the differential stage.

So the small signal output voltage of the first stage is

$$V_o = -(I_{d4} + I_{d2})(r_{ds2} \parallel r_{ds4}) \tag{C.4}$$
$$= g_m V_{in}(r_{ds2} \parallel r_{ds4}) \tag{C.5}$$

To observe the symmetry of the differential input stage, $M1 - M2$ have the same size and $M2 - M4$ have the same size. The low frequency gain for the differential stage $M1 - M4$ is:

$$A_1 = -g_{m2}(r_{ds2} \parallel r_{ds4}) \tag{C.6}$$

where g_m is small signal transconductance of $M1 - M2$, r_{ds2} and r_{ds4} are the output resistance of $M2$ and $M4$ respectively. The low frequency gain of the second stage is:

$$A_2 = -g_{m5}(r_{ds5} \parallel r_{ds5}) \tag{C.7}$$

where g_{m5} is the small signal transconductance of $M5$, r_{ds5} and r_{ds6} are the output resistance of $M5$ and $M6$ respectively. The overall low frequency gain is

$$A_0 = A_1 A_2 = g_{m2} g_{m5}(r_{ds2} \parallel r_{ds4})(r_{ds5} \parallel r_{ds5}) \tag{C.8}$$

C.1 Compensation

In order to calculate the high frequency performance with the compensation capacitor, a small signal model is shown in Fig. C.3.

The overall high frequency gain is:

$$A_v = g_{m1} g_{m2} r_{o1} r_{o1} \frac{1 - s \cdot c_c(R_c - 1/g_{m2})}{1 + s \cdot X + s^2 \cdot Y + s^3 Z} \tag{C.9}$$

$$X = g_{m2} r_{o1} r_{o2} C_c + C_c(R_c + r_{o1} + r_{o2}) + r_{o1} C_1 + r_{o2} C_2 \tag{C.10}$$

$$Y = r_{o1} r_{o2}(C_c C_1 + C_c C_2 + C_1 C_2) + R_c C_c(r_{o1} C_1 + r_{o2} C_2) \tag{C.11}$$

$$Z = R_c r_{o1} r_{o2} C_c C_1 C_2 \tag{C.12}$$

Equation C.9 can be used to generate the Bode plot in Matlab for analyzing the phase margin. It is oblivious that there are one zero and three poles in the overall

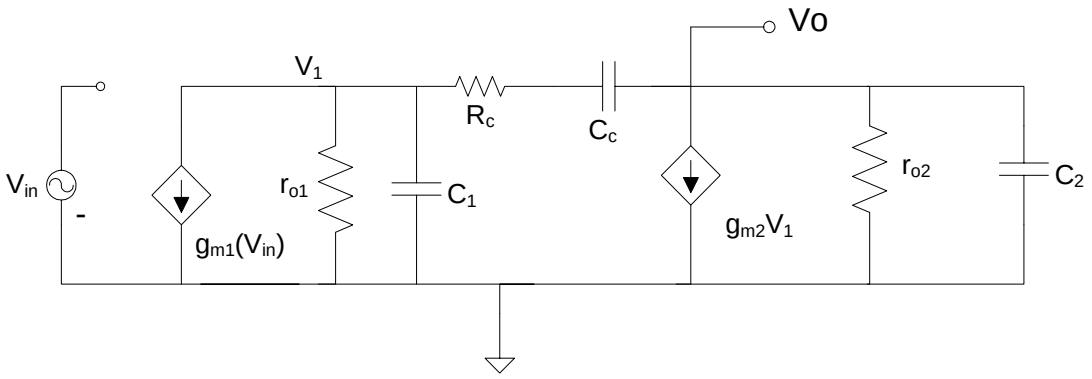


Figure C.3: Small signal model of the opamp output stage.

gain response. To get more insight to the frequency response, the gain equation can be re-written as a function of its zeros and poles:

$$A_v = A_0 \frac{1 - (s/\omega_z)}{(1 + s/\omega_{p_1})(1 + s/\omega_{p_2})(1 + s/\omega_{p_3})} \tag{C.13}$$

where ω_z is a zero generated by the series R_c and C_c feedback circuit.

$$\omega_z = \frac{1}{C_c(R_c - 1/g_{m5})} \tag{C.14}$$

By varying the R_c and C_c values, the zero can be adjusted to make the amplifier more stable. There are total three poles with the relation $\omega_{p1} \ll \omega_{p2} \ll \omega_{p2}$. Furthermore, we can in general assume $C_c \gg C_1$ *or* C_2 and $R_c \ll r_{o1}$ *or* r_{o2}. The three poles can then be solved with their approximation values with ω_{p1} as the dominate pole:

$$\omega_{p1} \approx \frac{1}{g_{m2} r_{o1} r_{o2} C_c} \tag{C.15}$$

$$\omega_{p2} \approx \frac{g_{m5}}{C_1 + C_2} \tag{C.16}$$

$$\omega_{p3} \approx \frac{1}{R_c(C_1 \parallel C_2)} \tag{C.17}$$

Appendix D

Sensor Interface

The ultra wide band transmitter in this work is designed for wireless sensor network applications. Sensor interface circuits are essential parts of the individual sensor nodes, serving as the bridge between the specific sensor and the transmitter. In general, analog sensor outputs can take various forms, such as capacitance, charge, voltage etc.; these analog signals must be converted to digital data before they can be modulated for transmission. Even though the UWB transmitter is designed to ultimately provide a generic wireless communication function, the sensor interface focuses on a specific sensor application.

In the initial prototype design, the target sensor application is an accelerometer, which senses the acceleration and converts it to capacitances [81]. The sensor interface circuit includes a capacitance voltage converter (CVC) and an analog-to-digital converter (ADC). The CVC first converts the sensor output to voltage, then feed this voltage to the ADC. The operational amplifier is discussed in Appendix C.

D.1 Overview of Analog-to-digital Converters

The voltage output from the capacitor-to-voltage converter circuit is passed to an analog-to-digital converter (ADC). ADCs are critical components in virtually all modern electronic systems in which data processing is required. Driven by the technology advances of IC scaling, more and more analog circuit can be replaced by their digital

Type of ADC	Speed	Resolution	Complexity
Slope	slow	high	low
Counter-Ramp	slow	high	low
Successive Approximation	medium	medium	medium
Pipeline	fast	medium	high
Cyclic	medium	medium	medium
Parallel/Flash	very fast	low	very high
Folding	fast	medium	high
Multi-step	very fast	medium	high
$\Sigma - \Delta$	medium	high	high

Table D.1: Comparison of common type of ADCs.

counterparts. Yet most information in the physical world is fundamentally analog, which mandates conversion to digital signals by the ADCs [82]. In wireless sensor applications, the input data needs to be digitized before it can be sent by the transmitter.

A variety of ADC architectures has been demonstrated over the years (Table D.1). ADCs may be classified by their speed: low speed ADCs include slope-type and counter-ramp; medium speed ADCs include sigma-delta (Σ-Δ), successive approximation (SAR) and cyclic; high speed ADCs include flash, folding and multi-step [83][84] .

ADC converts an analog input V_A to its digital approximation. For an analog input voltage with amplitude of V_A at an instant of time t, where $0 < V_A < V_{ref}$, the digital output of an n-bit ADC is $D = (B_{n-1}, B_{n-2}, ...B_0)$. The digital voltage output is

$$V_D = D \cdot \frac{V_{ref}}{2^n} = (B_{n-1}2^{n-1} + B_{n-2}2^{n-2} + \ldots B_1 2^1 + B_0 2^0) \cdot LSB \tag{D.1}$$

where LSB is the least significant bit. The random error between the analog input and digital output due to the finite resolution of ADC is also called *quantization noise*, which is less than the one LSB.

$$|V_A - V_D| < \frac{1}{2} LSB \tag{D.2}$$

From the above equation, it can be shown that the higher the resolution of ADC, the less its quantization noise. The signal-to-noise ratio (SNR) is the ratio between the

voltage input and the quantization noise, which increases with the resolution:

$$SNR = 1.5 \times 2^{2n} \approx 6.02n + 1.76(dB) \tag{D.3}$$

There is a trade-off between the resolution and speed of an ADC. Generally, the higher the resolution, the lower the maximum speed of an ADC. The linearity of ADC is another importance parameter. It is generally measured in the form of differential nonlinearity (DNL) and integral nonlinearity (INL). The DNL is defined as the deviation of the actual ADC step from the ideal step of one LSB. The INL is defined as the deviation of ADC output from the ideal straight line between two end points of the transfer curve [83]. successive approximation register ADCs have medium speed/resolution and consume relatively low power, which make them good candidates for sensor applications.

D.2 Successive Approximation ADC

In this project, an 8-bit 2-MHz charge-redistribution successive approximation register (SAR) ADC was selected to interface between the sensor and the transmitter. The SAR ADC is a medium speed ADC which represents a trade-off between speed, accuracy and power consumption. The charge-redistribution SAR ADC consists of a capacitor network, a SAR, a comparator array, and switching networks (Fig. D.1) [85]. Within each sampling cycle, the SAR needs to completely scan all the output bits. Therefore, the SAR must operate at a much higher speed than the sampling frequency depending on the total number of bits. In this design, the SAR has an internal clock rate of 20MHz. After the SAR completes data acquisition, the 8-bit parallel output of the ADC is converted to serial data stream. The detailed operation of the SAR ADC design is described in the following subsections.

D.2.1 Successive Approximation Register

The operation of an 8-bit successive approximation register (SAR) is illustrated in Table D.2. The eight register output bits $b_7 - b_0$ are reset at the beginning of each analog-to-digital conversion cycle. Starting from the highest significant bit, the ADC

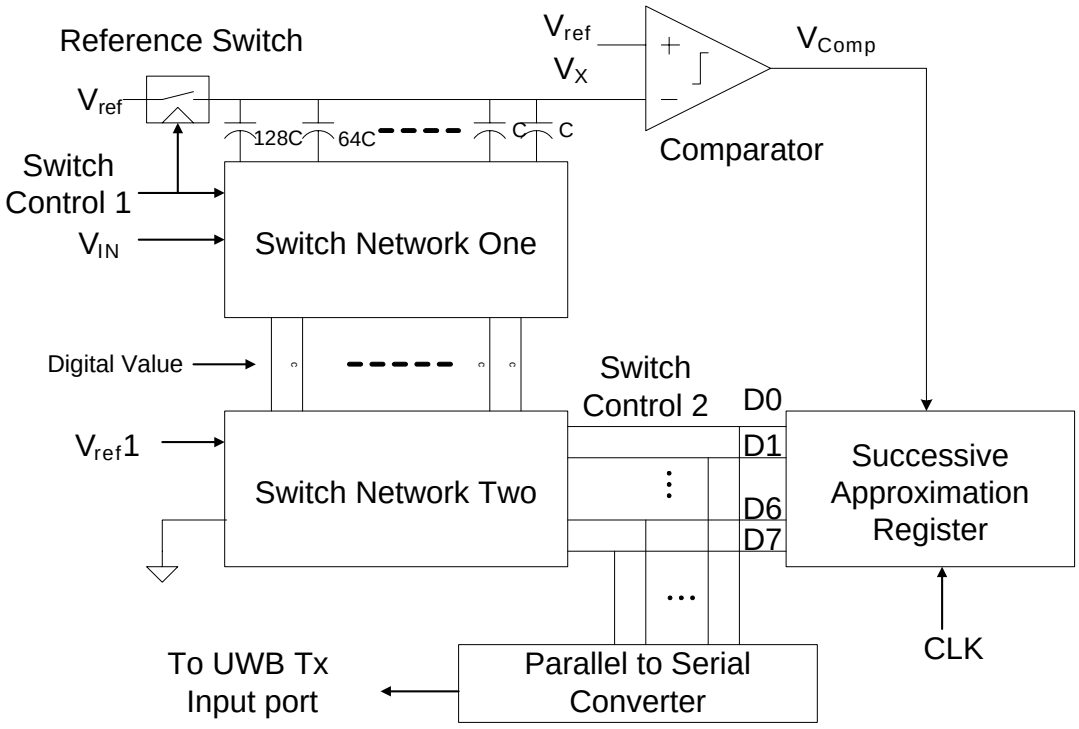


Figure D.1: Simplified diagram of a successive approximation ADC.

Clock	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	Comparator Output
0	0	0	0	0	0	0	0	0	–
1	1	0	0	0	0	0	0	0	c_7
2	c_7	1	0	0	0	0	0	0	c_6
3	c_7	c_6	1	0	0	0	0	0	c_5
4	c_7	c_6	c_5	1	0	0	0	0	c_4
5	c_7	c_6	c_5	c_4	1	0	0	0	c_3
6	c_7	c_6	c_5	c_4	c_3	1	0	0	c_2
7	c_7	c_6	c_5	c_4	c_3	c_2	1	0	c_1
8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	1	c_0
Result	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0	–

Table D.2: Basic SAR ADC operations: one bit will be resolved at each step.

converts one bit during each clock period. It takes a total of 8 clock cycles to finish one 8-bit conversion. At the beginning of each step, the current bit to be resolved will be first set to one. Then an 8-bit internal digital-to-analog converter (DAC) converts the register bits $b_7 - b_0$ to analog voltage. This DAC output voltage is then compared to the analog input voltage. The result from the comparison c_n is stored in the current bit register. This procedure is repeated until the LSB is resolved. As a result, the time for each sample conversion equals the product of number of bits and the conversion time for each bit [86].

The register mentioned in the above operation is a 8-bit SAR constructed using a total of 18 D flip-flops (Fig. D.2). There are two primary sub components in the 8-bit SAR: a 8-bit shift register composed of eight D flip-flops ($R7a - R0a$) and an 8-bit data register composed of another eight D flip-flops ($R7b - R0b$). The two additional D flip-flops RXa and RXb are used to clock in the last comparator output to bit b_0 during the last clock cycle. The 8-bit shift register can only have one bit set at 1 at any time, and the 1 moves from the highest bit ($R7a$) to the lowest bit ($R0a$). The shift register with output of $a_n = 1$ will then set the Q of the corresponding data register output b_n to be 1. Since b_n is also fed to the clock input of the previous bit data register, it will trigger the higher bit b_{n+1} to be stored. The value of bit b_{n+1} is the comparator output when b_n rises from 0 to 1.

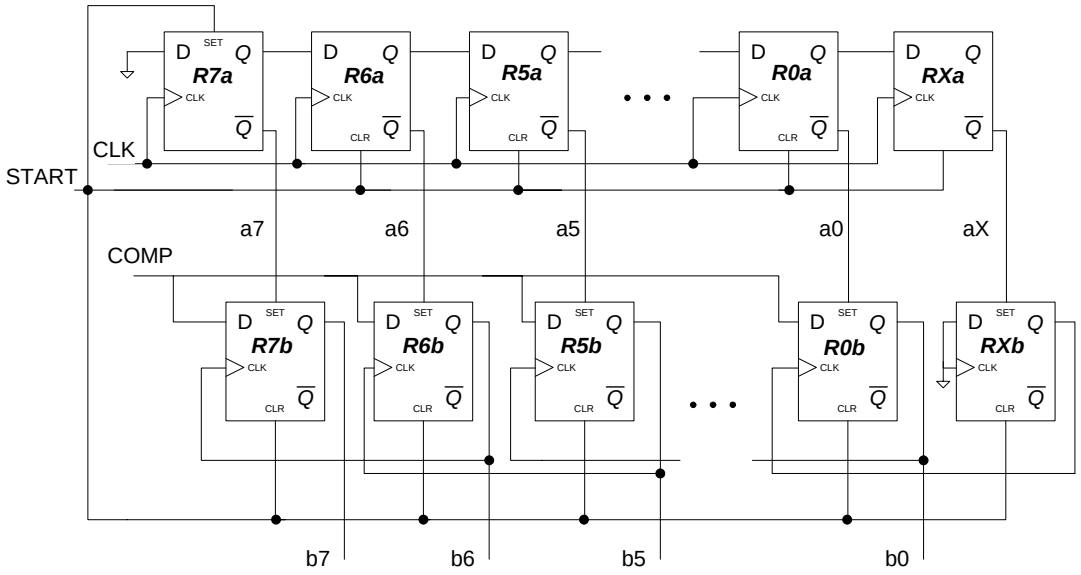


Figure D.2: An 8-bit successive approximation register.

D.2.2 Charge-Redistribution Network

The charge-redistribution network is composed of an array of capacitors controlled by a switching network. It is essentially a part of the internal DAC. The charge-redistribution network is connected to the input voltage and reference voltage through the switching networks (Fig. D.1). By controlling on/off the switching network, the charge-redistribution network realizes the operation of subtracting the DAC output from the sensed input voltage. This operation is illustrated in Fig. D.3 [87].

The positive input of the comparator is connected to the reference voltage V_{ref}. The negative input of the comparator is connected to the capacitor redistribution network. The capacitors in the charge redistribution network are assigned to have binary values. The minimum capacitor value is C_0 which is determined by a trade-off between speed and accuracy. The other capacitor values are sequential doubled according to $C_n = 2^{n-1}C_0$ where n is the bit number.

The top plates of the capacitors is always connected to the negative comparator input. The operation of the charge redistribution network can be divided into three steps. First, all the capacitors are connected in parallel with their top plates to V_{ref} and their bottom plates to V_{in} [Fig. D.3(a)] [87][85]. The total charge on the top plates

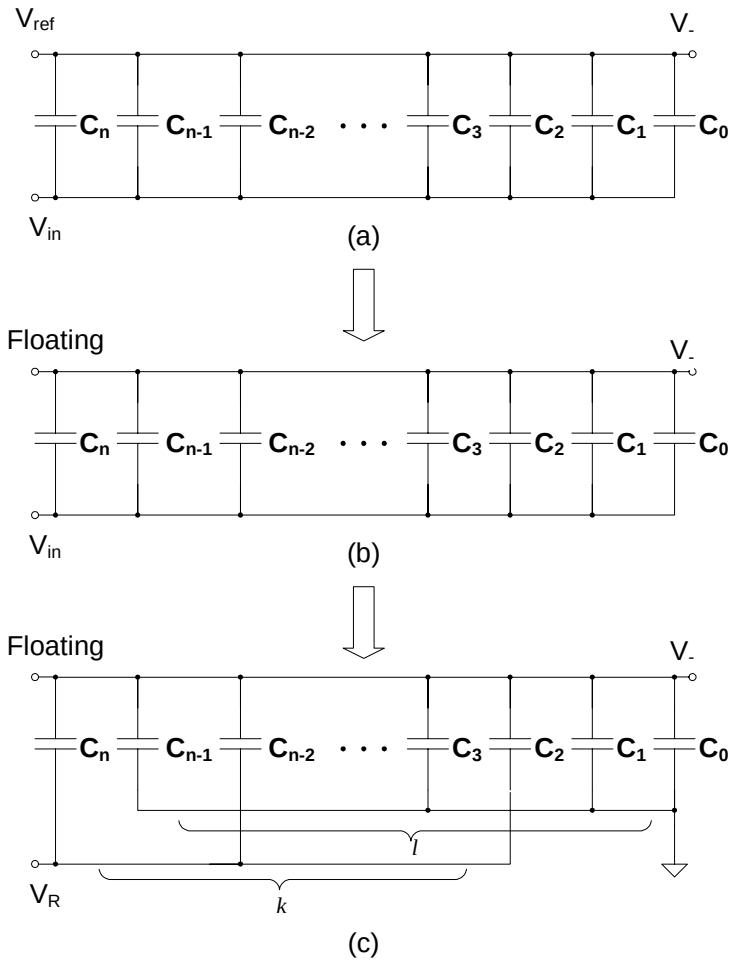


Figure D.3: Basic operation of the charge redistribution network.

connected to the negative comparator input (V_-) is:

$$Q_0 = (V_{ref} - V_{in}) \sum_{n=0}^{N} C_n \tag{D.4}$$

where N is the total number of capacitors. Next, the input V_{ref} is disconnected from capacitor top plates such that the stored charge Q_0 at V_- remains unchanged [Fig. D.3(b)]. The conservation of charge Q_0 is the key concept here, as we shall see below. Finally, the input voltage V_{in} is disconnected from the bottom plates of the capacitor array [Fig. D.3(c)]. Then, controlled by the successive approximation register, certain k capacitors, C_k, have their bottom plates connected to a reference voltage V_R, while the remaining l capacitors, C_l, have their bottom plates connected to the ground. The total charge Q_1 relocated to the top plates of the k capacitors is:

$$Q_1 = -(V_R - V_-) \sum_{k} C_k, \tag{D.5}$$

where k is number of the capacitors connected to V_R. The total charge Q_2 relocated to the top plates of the l capacitors is:

$$Q_2 = V_- \sum_{l} C_l, \tag{D.6}$$

where l is the number of capacitors connected to ground. Since no voltage source is connected to node V_-, the total charge at V_- is conserved and equals to Q_0:

$$Q_0 = Q_1 + Q_2 \tag{D.7}$$

Substituting equations D.5-D.6 into equation D.7, the node V_- voltage can be solved

for as follows:

$$
\begin{aligned}
\Longrightarrow \quad & -(V_R - V_-)\sum_k C_k + V_- \sum_l C_l = (V_{ref} - V_{in})\sum_{n=0}^{N} C_n \\
\Longrightarrow \quad & V_- \sum_{n=0}^{N} C_n = (V_{ref} - V_{in})\sum_{n=0}^{N} C_n + V_R \sum_k C_k \\
\Longrightarrow \quad & V_- = (V_{ref} - V_{in}) + V_R \frac{\sum\limits_k C_k}{\sum\limits_{n=0}^{N} C_n} \\
\Longrightarrow \quad & V_- = (V_{ref} - V_{in}) + V_R \frac{\sum\limits_k 2^{k-1}}{\sum\limits_{n=0}^{N} 2^{n-1}}
\end{aligned}
\tag{D.8}
$$

The difference voltage ΔV at the input of the comparator can be then found:

$$
\Delta V = V_+ - V_- = V_{in} - V_R \frac{\sum\limits_k 2^{k-1}}{\sum\limits_{n=0}^{N} 2^{n-1}} \tag{D.9}
$$

The comparator differential input voltage ΔV essentially compares the input voltage V_{in} and the binary DAC output voltage controlled by the successive approximation register. The comparator output the current bit to be resolved at the successive approximation register.

D.2.3 Comparator

The comparator of the ADC compares its input only at the rising edge of its reset clock. The result of the comparison is then stored in a latch as long as the reset voltage is inactive. This comparator is constructed using a differential NMOS input $M1 - M2$ and a cross coupled PMOS load $M3 - M4$ (Fig. D.4) [85]. Another pair of PMOS transistors $M5 - M6$ was added to reset the comparator.

A low RST tunes on PMOS pair $M5 - M6$ and resets differential outputs V_o+ and V_o-. After RST switches from low to high, $M5 - M6$ are turned off. The error of differential input $V+$ and $V-$ will be amplified by the differential pair $M1 - M2$

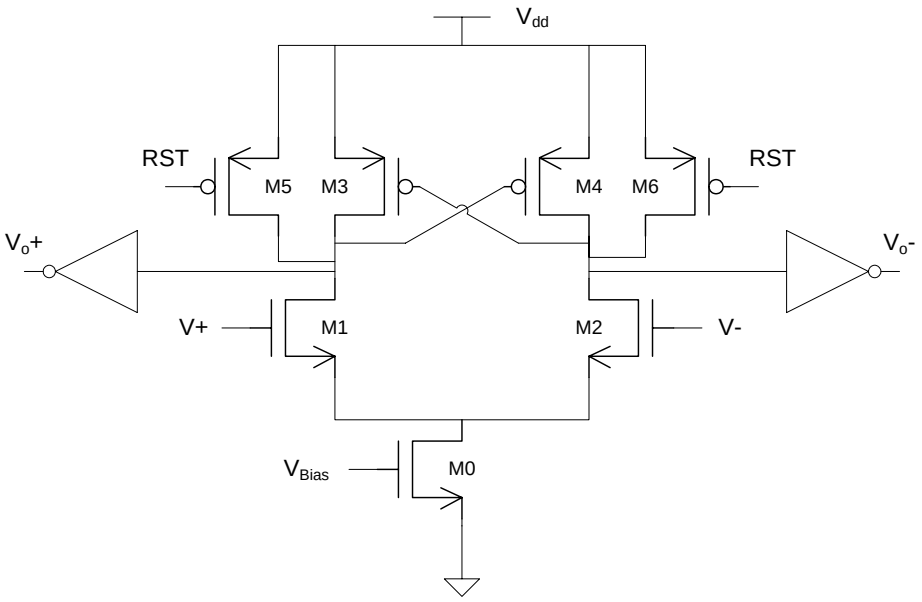


Figure D.4: Simplified schematic of the comparator.

and aided by the cross-coupled PMOS pair $M3 - M4$. As a result, the drain voltage of $M1 - M2$ will be quickly be pulled to the opposite polarity. The comparator output for this clock cycle is then available to be fed to the register. The PMOS pair $M5 - M6$ used for the reset need to be large enough compared to M3-M4 in order to reset at the beginning of the next clock cycle.

D.3 Parallel to Serial Conversion Network

After the analog input is converted to parallel n-bit digital data by the analog-to-digital converter, the parallel data must be translated to n-bit serial data in order to pass it to the transmitter. A n-bit parallel-to-serial converter is constructed for this purpose using an n-bit shift register (Fig. D.5). Each bit of the shift register is composed of a D flip-flop and a Double-Pole-Single-Throw (DPST) switch, which is controlled by an input signal SEL. The entire parallel-to-serial conversion of a single data symbol may be divided into two separate steps governed by the control bit SEL. A the beginning of each data symbol conversion, all the registers output of the parallel-to-serial converted are cleared to be low. The control bit SEL is high at the first clock rising edge, so that the DPST switch is connecting parallel data $B_0 - B_n$

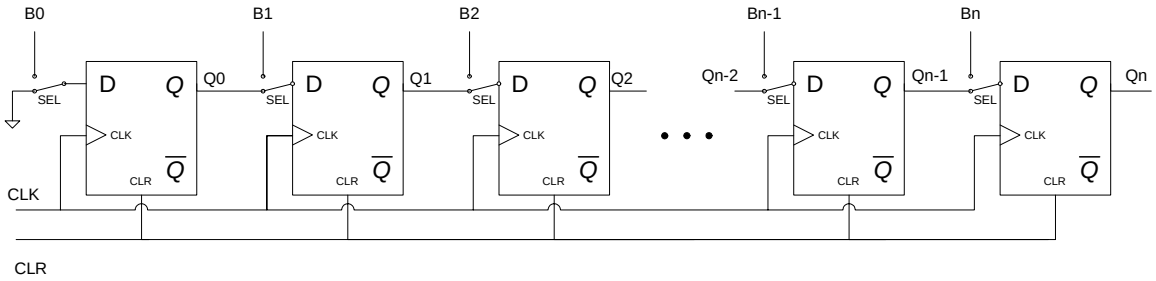


Figure D.5: The parallel-to-serial conversion network composed of n-bit registers.

input to the input of each D flip-flop. Therefore, the data is clocked into the register after the first clock and the highest bit B_n is taken out from last register output Q_n. In the next $n-1$ clock, the control bit SEL is low and the parallel-to-serial converter enters shift mode. From high to low in order, each bit is shifted to the output of the last register Q_n. It takes a total of n clocks to complete each symbol conversion.

D.4 UWB Transmitter with Sensor Interface Layout

A sensor interface circuitry including a successive analog to digital converter and capacitor to voltage converter is added to complete the initial prototype UWB transmitter design. The complete chip occupies a die area = 1mm×2.5mm (Fig. D.6). The different component of the die is also separated using ground walls and powered through separate power supplies as in the previous version. This design is not being fabricated due to the phaseout of the HIP6WRF technology.

D.5 Summary

Appendix D covers the design and operation of a charge redistribution successive approximation ADC. The ADC is composed of several key components: a successive approximation register, a charge-redistribution network and a compactor. The SAR ADC represents a compromise between speed and resolution. It has relatively low

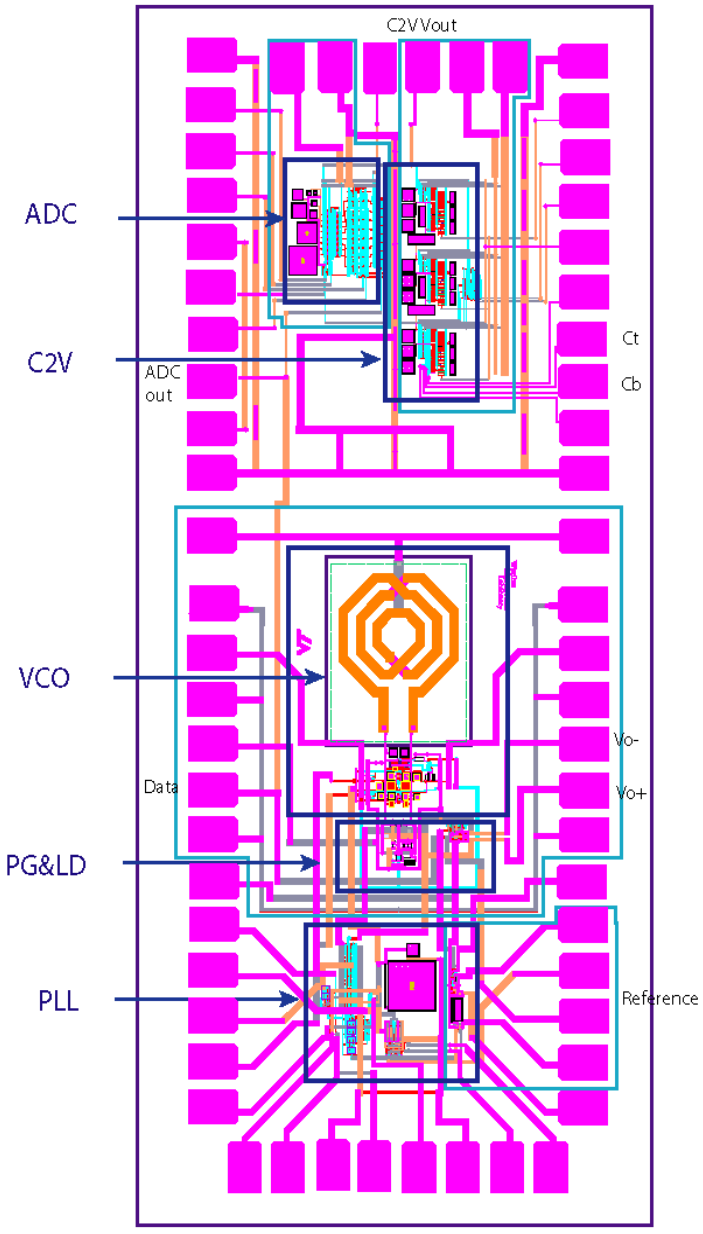


Figure D.6: Layout of the complete UWB transmitter including sensor interface circuit. (CV converter and ADC)

complexity and power consumption, therefore is an ideal candidate to moderate speed wireless sensor node applications.

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