Improved Renewable Energy Power System using a Generalized Control Structure for Two-Stage Power Converters

Rae-Young Kim

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Jih-Sheng Lai, Committee Chair
Douglas K. Lindner
Yilu Liu
Kathleen Meehan
Douglas J. Nelson

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ABSTRACT

The dissertation presents a generalized control structure for two-stage power converters operated in a renewable energy power system for smart grid and micro grid systems. The generalized control structure is based on the two-loop average-mode-control technique, and created by reconstructing the conventional control structure and feedback configuration. It is broadly used for both dc-dc and dc-ac power conversion based on the two-stage converter architecture, while offering several functionalities required for renewable energy power systems. The generalized control structure improves the performance and reliability of renewable energy power systems with multiple functionalities required for consistent and reliable distributed power sources in the applications of the smart grid and micro grid system.

The dissertation also presents a new modeling approach based on a modification of the subsystem-integration approach. The approach provides continuous-time small-signal models for all of two-stage power converters in a unified way. As a result, a modeling procedure is significantly reduced by treating a two-stage power converter as a single-stage with current sinking or sourcing. The difficulty of linearization caused by time-varying state variables is avoided with the use of the quasi-steady state concept.

The generalized control structure and modeling approach are demonstrated using the two-stage dc-dc and dc-ac power conversion systems. A battery energy storage

system with a thermoelectric source and a grid-connected power system with a photovoltaic source are examined. The large-signal averaged model and small-signal model are developed for the two demonstrated examples, respectively. Based on the modeling results, the control loops are designed by using frequency domain analysis. Various simulations and experimental tests are carried out to verify the compensator designs and to evaluate the generalized control structure performance.

From the simulation and experimental results, it is clearly seen that the generalized control structure improves the performance of a battery energy storage system due to the unified control concept. The unified control concept eliminates transient over-voltage or over-current, extra energy losses, power quality issues, and complicated decision processes for multiple-mode control. It is also seen that the generalized control structure improves the performance of a single-phase grid-connected system through increased voltage control loop bandwidth of the active ripple current reduction scheme. As a result of the increased loop bandwidth, the transient overshoot or undershoot of the dc-link voltage are significantly reduced during dynamic load changes.

To my parents

Deuk-Soo Kim and Hae-Sook Wee

To my wife, son, and daughter

Sok-Hyo Kang, Daniel J. Kim, and Claire R. Kim

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Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

In recent decades, renewable energy sources used in distributed power systems have shown dramatic progress and promising potential for viable utilization in smart grid and micro grid systems [1]-[4]. These sources include hydro power, biomass, wind, thermoelectricity, photovoltaic, and fuel cell. However, most renewable energy sources are uncontrollable. As a result of the sources' uncontrollability, renewable energy sources are difficult to operate consistently and reliably for smart grid's and micro grid's power systems. To utilize most of those renewable energy sources, especially those generating dc electricity, power electronics has been used as the "enabling technology" [5]-[8]. One of the promising utilizations, for example, is the use of storage devices, such as lead acid, lithium, and nickel with the renewable energy sources. In this utilization, a power converter needs to accommodate two major tasks: 1) uncontrollability of the renewable energy sources and 2) management of the state-of-charge of batteries. The other utilization is electrical grid interconnection. For this, a power converter needs to tolerate the abnormal grid disturbances and to comply with the standards given by the utility

companies, such as IEC 61000-3-2 [9], IEEE1547 [10], and the U.S. NEC690 [11]. In particular, single-phase power converters reveal more challenges for these requirements, because instantaneous power is inherently pulsated with double-fundamental frequency. The pulsated instantaneous power injects a large amount of current ripple to the energy sources, which causes several issues such as reducing durability and degrading source utilization.

In recent decades, power electronics has undergone fast development, mainly driven by maturation of semiconductor devices and real-time computer controllers. This development has led to the emergence of several power electronics topologies for renewable energy sources. Most topologies may be categorized in two groups, single-stage architecture and two-stage architecture, depending on the number of power processing stages. With decreasing converter prices, the two-stage power converter architecture is becoming more popular since it is versatile, high performance, and easily adapted for most renewable energy sources [3]-[5], [12]-[13]. The two-stage power converter requires a new control strategy to manage more control variables and feedback signals due to the increased complexity of the power stage. Even though several papers on the subject of two-stage power converter control have been published so far, their contributions have primarily focused on the new development of control rules or compromise strategies [14]-[20]. Research efforts to develop a more appropriate control structure for two-stage power converters have not been reported until recently.

The purpose of the research presented here is to propose a new control structure and theoretical rationale based modeling approach for the two-stage power converter when it is operated in renewable energy power systems in the smart grid and micro grid. The

proposed control structure and modeling approach are applicable to various two-stage power converters for a typical renewable energy. As a result, the performance and reliability are significantly improved with multiple auxiliary functionalities for a distributed power system in the applications of smart grid and micro grid systems.

1.2 Overview of power electronics for renewable energy system

Electricity extracted from renewable energy sources requires an efficient power conversion process to transform it into a useable form of electricity. For efficient power conversion, various power converter topologies have been developed and implemented. Most of the existing power converter topologies are classified into two major architectures: a single-stage with or without isolation and a two-stage with or without isolation [5]-[6]. In general, due to its simple structure, the single-stage architecture has the advantages over the two-stage architecture, which include reduced size, weight and cost and realized high efficiency. However, the operating performances such as source utilization, safety, and versatility are extremely limited. For example, the power converter in a grid-interconnected photovoltaic system cannot operate under clouded or shaded conditions because of insufficient input voltage, which causes the reduction of the source utilization. The safety issue may be addressed with using a line-frequency transformer, but system size, weight, and cost issues rise due to the transformer [11]. Even though the cost of two-stage architecture is generally higher, the two-stage power converter is an attractive solution from the viewpoint of performance, design flexible, and power capability, thanks to additional functionalities on each individual power processing stage.

Figure 1.1 illustrates a typical configuration of a two-stage power converter operated for a renewable energy power system. The first-stage converter is commonly a step-up dc-dc power converter in order to boost the voltage. Using the step-up converter allows a sufficiently high dc bus voltage to be maintained even if renewable energy sources drop to low voltage levels. Therefore, a wide range of input voltage is accepted and source utilization is maximized. The higher voltage dc bus also helps improve power conversion efficiency by reducing conduction losses. Moreover, the high frequency transformer is easily incorporated into dc-dc converter topologies when the electrical safety or high voltage conversion ratio is required [21]-[24]. In general, flyback converters are widely used for power levels under 200W. Forward or push-pull converters are used for the power range of 200-1000W. When power requirements are greater than 1kW, half-bridge or full-bridge converters are preferred. In order to increase energy storage, capacitive energy storage devices such as electric double layer capacitors and super capacitors may be substituted for dc bus capacitors [25]-[27]. Second stage power converter topology selection is determined by the application. For battery storage applications, dc electricity regulated by dc-dc converters is required. For the interconnection to existing ac electrical grids, dc-ac inverters are required. The flexibility of the second-stage converter selection allows the two-stage power converter architecture to serve as a general-purpose power electronics building block for various renewable energy sources and applications. Low efficiency could be considered as one major disadvantage for a two-stage power converter architecture, but efficiency may be improved by many advanced power conversion techniques such as resonant or soft-switching [28]-[29].

Several control schemes for two-stage power converter architectures are

summarized in the paper [19]. As shown in Figure 1.2, the control tasks for two-stage power converters are summarized into two major parts. The major task of the first-stage controller is to maximize harvested power. To do this, the design of the first stage controller requires the analysis of the energy source's characteristics. For example, a photovoltaic or thermoelectric energy source requires maximum power point tracking [30]-[41], while a fuel cell power system requires a maximum allowable power control scheme which is usually achieved by communication with the balance of plant (BOP) [11], [13]. The second-stage controller is responsible for managing the output power quality injected into electrical loads. Typical electrical loads include existing electrical grids, passive and active electrical loads, and energy storage systems. The form of electric loads determines the type of control, such as the battery management control, grid connection control, and standalone control. Sometimes additional controllers for ancillary services, such as local voltage and frequency regulation, voltage harmonic compensation, or active filtering, may be required by electrical consumers [42]-[44].

The realization of these control tasks is usually achieved by a cascaded two loop structure composed of internal loop and external loop [19]. In this structure, the internal loop regulates the current with over current protection. The internal current loop is typically designed to have a fast dynamic response. For the external loop, which drives the internal current loop, several control schemes are possible depending on the power converter stage, energy source, load system, or system utilization.

Some renewable energy sources, such as thermoelectric and photovoltaic, exhibit nonlinear voltage-current characteristics, usually having only one maximum power point with given operational or environmental conditions [30]-[39]. Several control schemes,

which are often referred to as maximum power point tracking control, have been proposed to extract as much electrical energy as possible from the renewable energy sources by the power electronics converter. The most popular scheme is perturbation-and-observation, also known as hill climbing. This scheme involves a small perturbation in the operating current or voltage of the renewable energy sources. If an increase in output power is detected, the control scheme drives the subsequent perturbation in the same direction. If a decrease in output power is detected, the control scheme changes the perturbation direction [30]-[33].

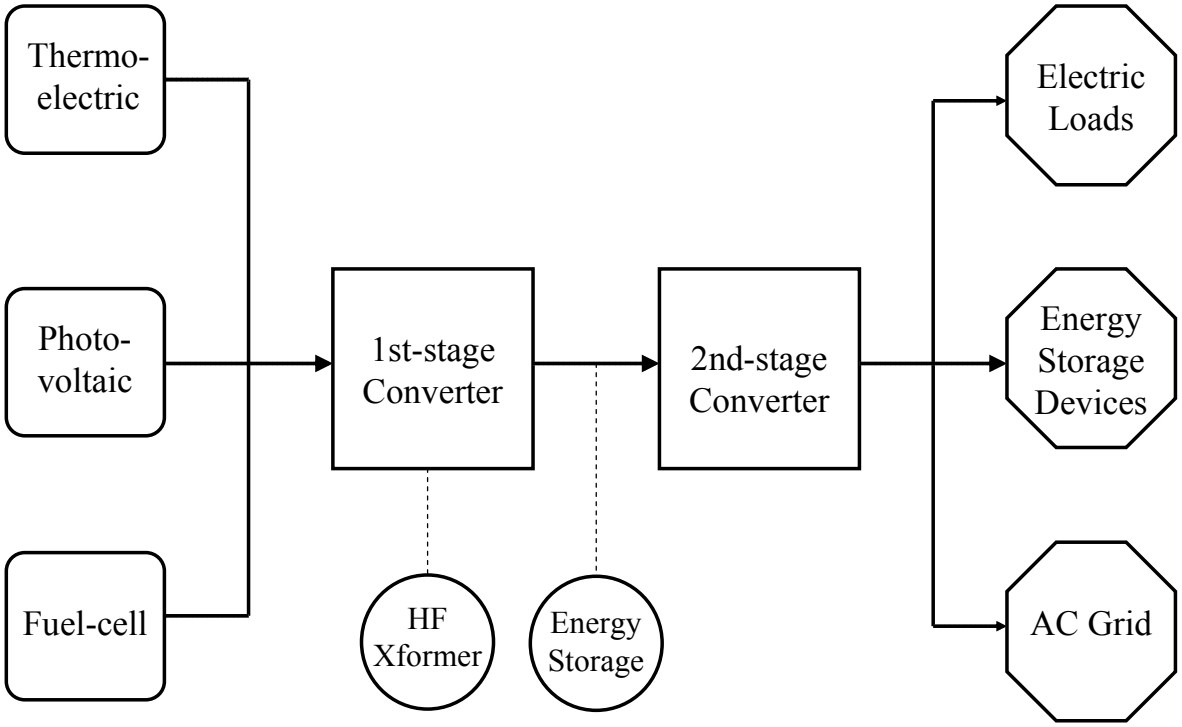


Figure 1.1 Two-stage power converter configuration for renewable energy source.

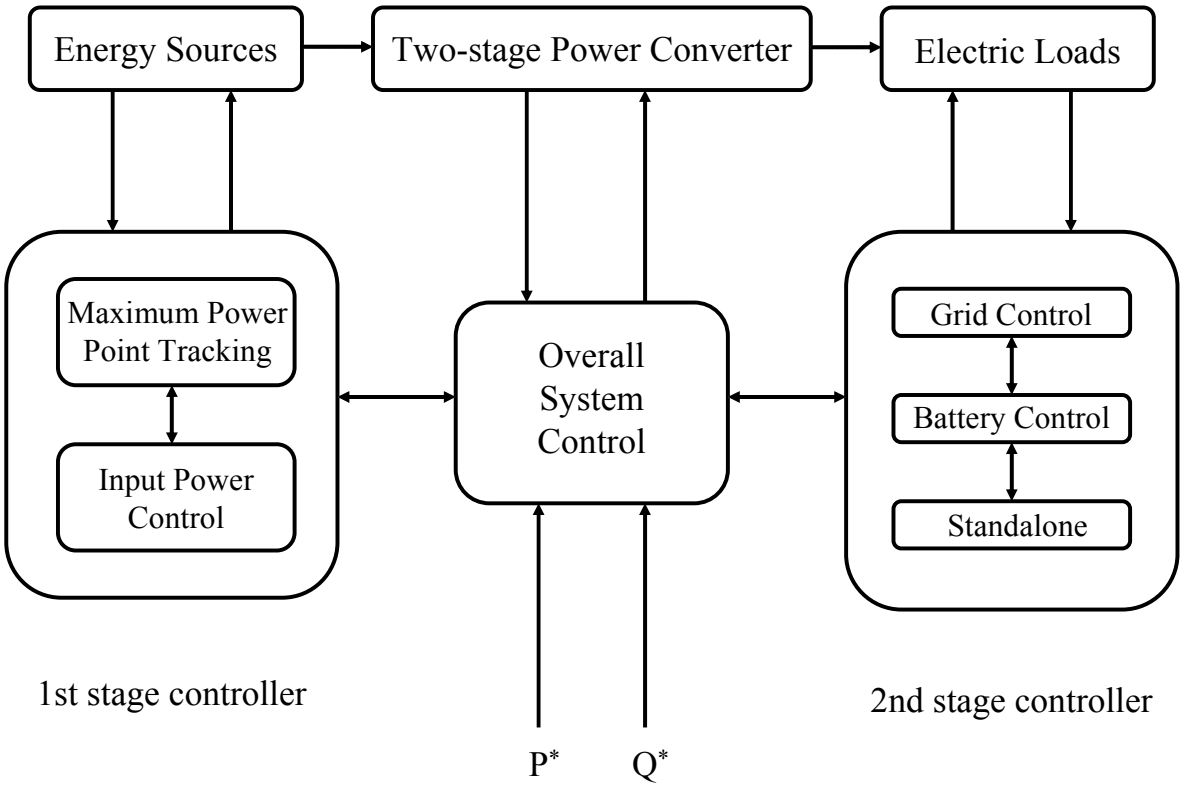


Figure 1.2 Control scheme for two-stage power converter.

Figure 1.3 shows a typical perturbation-and-observation scheme in the flowchart. Even though this method has been widely used because of simplicity and easy implementation, it often struggles with steady-state oscillation and failure under rapidly environmental conditions. The oscillation can be minimized by using variable perturbation size. The step size becomes smaller as output power approaches its maximum power point (MPP). Several schemes, such as incremental conductance, ripple correlation, and power derivative feedback [34]-[36], have been proposed. They use a different control rule in order to meet specific requirements. Incremental conductance scheme is based on the fact that the sum of the instantaneous conductance (I/V) and incremental conductance ($\Delta I/\Delta V$) is zero at the MPP. Unlike the perturbation-and-observation scheme, incremental conductance scheme has a stable operation at the MPP without oscillation. Power derivative feedback scheme computes the derivative of the power with respect to time for every sampling period, and feed it back to the power converter to drive it to zero. Several ways for computing the power derivative computation have been proposed to improve the performances of tracking accuracy and speed. Furthermore, the microcontroller adapted schemes, such as fuzzy logic [37], a neural network [38], and a state-space model [39], have been proposed.

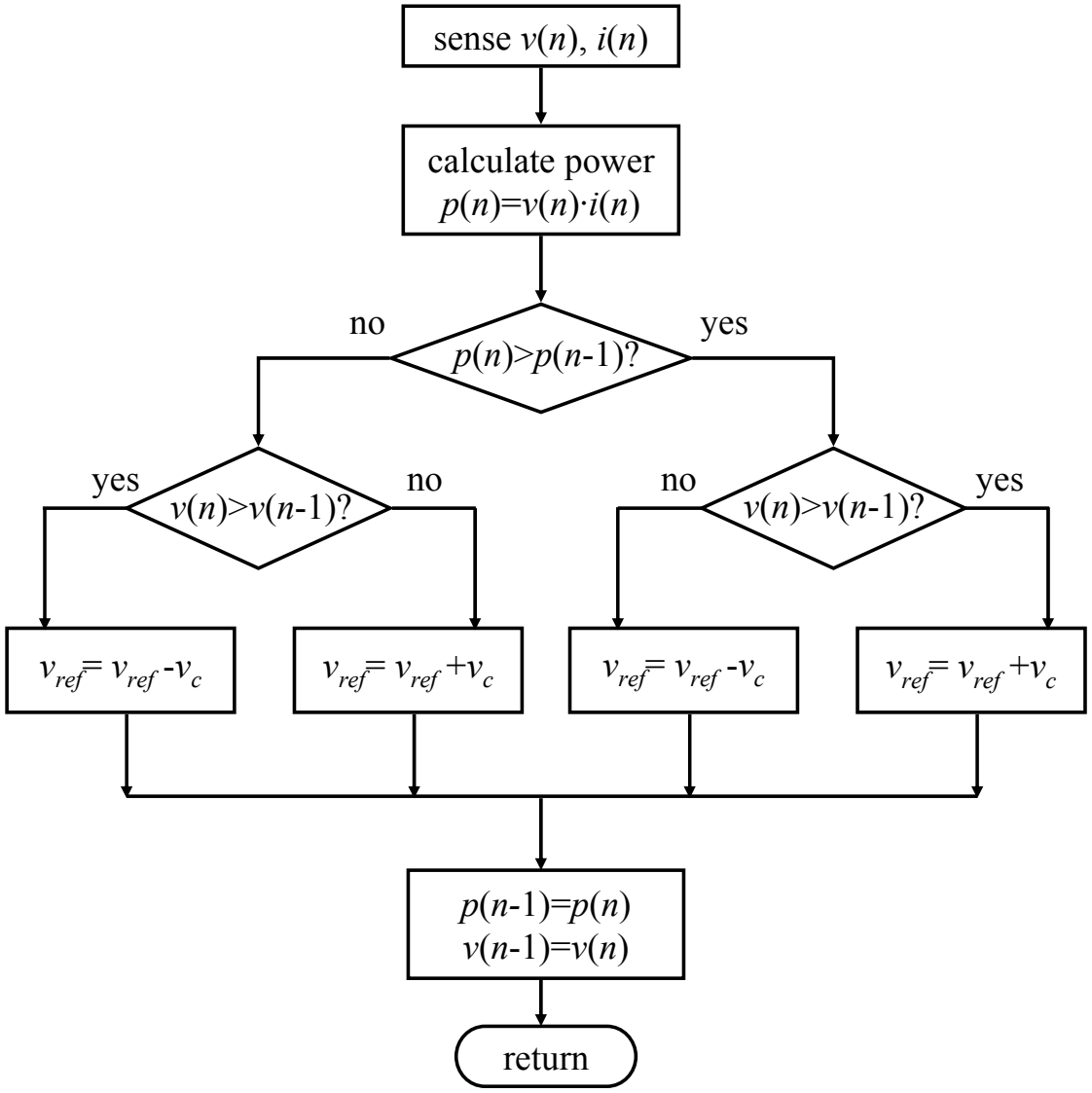


Figure 1.3 Program flowchart of perturbation-and-observation MPPT scheme.

1.3 State-of-the-art of two-stage power converter modeling

The dynamic behaviors of existing power converters are governed by low pass filters. The average concept based on these behaviors was established by Middlebrook in 1973 [45], since then, several modeling methods using the average concept have been proposed. One of the popular approaches is the state-space averaging method. This method is successfully extended to two-stage power converters. Moreover, the averaged pulse-width-modulation (PWM) switch model proposed by Vorperian can lead to simplification of the analysis of the state-space averaging method [46].

When the state-space averaging method is employed for a two-stage power converter, however, two major problems arise: 1) modeling works associated with the analysis of the state-space averaging method are significantly increased due to a large number of elements and control variables, and 2) linearization based on Taylor series breaks down when a dc-ac inverter is employed for a grid connected system, because some of the state variables do not have a dc operating point but strongly oscillate with the fundamental frequency of the utility grid. Several modeling approaches with the goal of overcoming these issues have been proposed. Some major approaches are briefly presented in this chapter.

1.3.1 Modeling approaches for multiple stage converters

A subsystem-integration approach is quite straightforward [47]-[50]. This approach analyzes and designs each converter under a standalone operation condition, and

then integrates together by using two-port network parameters. Since the concept of impedance criterion for checking small-signal system stability was first proposed, many kinds of method have been developed to pursue a more accurate and practical prediction of the system interaction [48]-[50].

The subsystem-integration approach is attractive from the viewpoint that the design work becomes extremely simplified with guaranteed converter stability. However, it exhibits several limitations associated with analysis, modeling, and design for two-stage power converters. The subsystem-integration approach was originally developed to scale and minimize the influence of subsystem interaction. Thus, it mostly focused on dealing with a stability issue among the multiple load converters in distributed power systems. The fundamental behaviors of dynamics and interactions between the two converters are still hard to be predicted.

Another promising approach is to use the averaged PMW switch model [51]-[54]. The equivalent time-invariant continuous power circuit is obtained by substituting the averaged PWM switch model for the switching cells at each converter. This approach is a type of the averaged circuit models, and thus makes it possible to predict large- and small-signal characteristics of the converters. It is a good approach to see the insight of dynamics and interactions of the two-stage power converter, even though it is more complicated than the subsystem-integration approach. In similar way, the modeling method using an equivalent dc transformer model was also proposed [55].

1.3.2 Modeling approaches under time-varying state variables

Extensive research associated with modeling approaches under time-varying state

variables are undertaken in single-phase power factor correction circuits. A sampled-data modeling approach, which is based on a linear time invariant difference equation with the switching period as the sampling interval, was employed for several power converters [56]-[59]. This approach does not require the linear ripple assumption; therefore, it can be applicable to any kind of power converters. However, this method exhibits some disadvantages, which include complexity in the compensator design and extensive efforts for the execution.

A low frequency modeling approach was proposed in the literature [60]. This approach considers the power factor correction circuit as a dc-to-dc converter with an equivalent dc input that corresponds to the rms value of the rectified line voltage. Under this assumption, the small signal model is only applicable to a frequency range much lower than the oscillation frequency of the time varying state variables, an example being less than 10-30Hz for 120 Hz rectified line voltage in single-phase power factor correction circuits.

A quasi-static analysis, known as a high frequency modeling approach, was proposed in [61]-[65]. This approach treats successively changed operation points in the time-varying state variables as several dc operating points under the assumption of much faster dynamics of a system than the oscillation frequency. Contrary to the low frequency modeling approach, the derived model by this approach is applicable to frequency range much higher than the rectified line voltage, typically higher than 1 kHz for 120 Hz rectified line voltage. In a typical power factor correction circuit, the current loop requires much higher bandwidth than the rectified line voltage, while the voltage loop is designed to have lower. The design requirement of the high current loop bandwidth justifies the use of the

quasi-static modeling approach.

Another systematic approach was proposed by applying the concept of the describing function, which depends on transforming from time domain waveforms into frequency domain using the Fourier series expansion [66]-[68]. The harmonic balance concept is employed to relate the state variable harmonic terms and the describing function terms caused from system nonlinearity, which enables to remove the oscillating terms of time varying state variables. As a result, the linearization issue caused by the oscillating terms can be totally eliminated. This method leads to continuous-time small-signal models in linear time invariant expression, with no other assumptions but the small-signal assumption. Therefore, it provides high accuracy and a good insight for dynamics of power converters. The extended describing function to reduce the complexity of the conventional describing function has been proposed, in which an accurate analysis model for small-signal analysis of resonant converter is derived [69]-[70].

1.4 State-of-the-art of two-stage power converter control strategy

1.4.1 Battery management for battery energy storage system

A battery is the most common device to store energy due to low coast and easy availability. While the battery cost is relatively low compared to the system cost, the lifetime cost is considered to be quite expensive due to its short service time. The most common failure of the battery is overcharging. Overcharging batteries result in excessive temperature, which degrades the chemical composition of the electrolyte. As a result, the

expected life time becomes remarkably shorten [71].

In general, maximizing energy harvesting by the maximum power point tracking control scheme is desirable for the battery energy storage system. The extracting electrical energy supports electrical loads, and then the excessive amount is stored to the battery for future usage. However, the story is totally changed when the battery already is fully charged. The extracting energy still supports electrical loads, but the excessive amount should be reduced to prevent overcharging the battery. Stated differently, the energy balance between the extracted energy and the demanded energy is required to manage charging status of batteries. This scenario needs to involve the additional control scheme, usually referred to as power matching control. Consequently, the battery energy storage system requires the two distinctive operating modes by the maximum power point tracking and power matching control in order to maximize energy harvesting and prevent the battery overcharge [72]-[78].

Two distinctive operating modes are usually achieved based on the stop-and-go concept, which realizes a mode transfer by ceasing one controller and running the other control scheme. Figure 1.4 shows one example of this stop-and-go concept for a single-stage dc-dc converter [74]. The photovoltaic power system charging to a battery is implemented with a two-loop control technique. In this technique, a voltage loop regulates the PV voltage to track a maximum power point, and a current loop regulates the battery charging current. These loops are alternately selected according to battery charging status, which may causes the transient over-voltage or -current associated with the dynamic mode changes, extra energy losses, and power quality issue.

Figure 1.5 shows the case when the stop-and-go scheme is used for a two-stage dc-

dc converter [75]. In this converter, an electric double layer capacitor and battery are used as energy storage devices. This control scheme incorporates two control modes for the first-stage converter and three control modes for the second-stage converter. These control modes are changed based on the state of charge for the double-layer capacitor and the battery. Changing control modes causes the transient issues on the system voltage or current. In addition, this type of the multiple-mode control tends to complicate the design and reduce the system reliability. Sometimes, a decision process of several control modes requires a lot of computations in a high-end digital signal process.

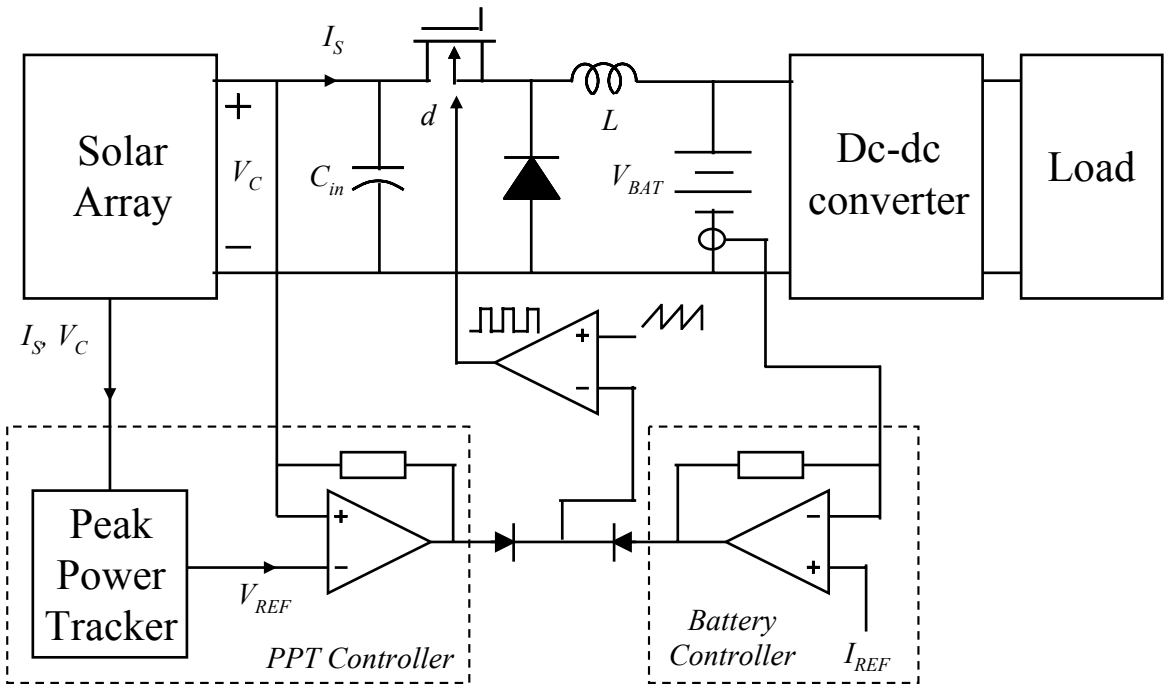


Figure 1.4 Control example of battery energy storage system using stop-and-go scheme.

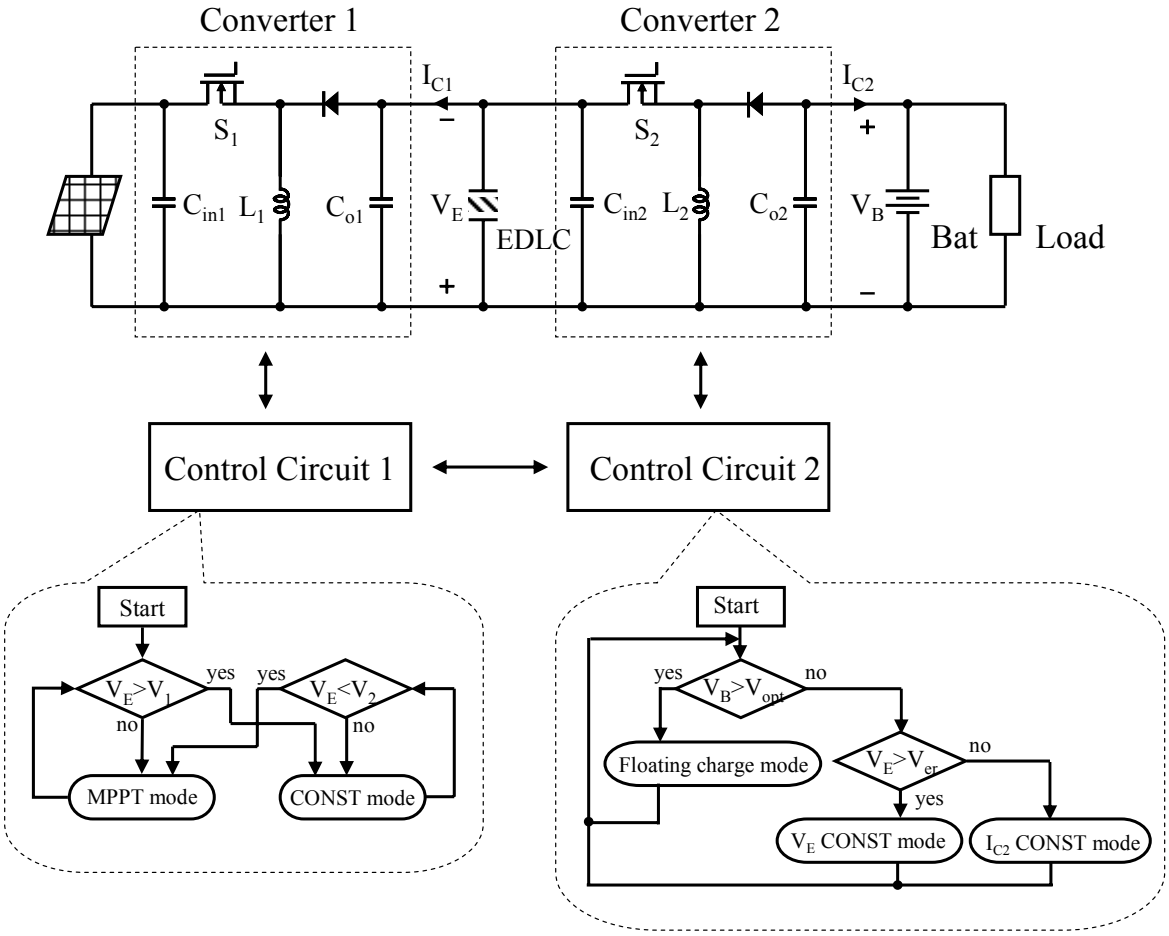


Figure 1.5 Another example of battery energy storage system using stop-and-go scheme.

1.4.2 Power pulsation decoupling for single-phase grid-connected system

In single-phase grid-connected systems, the output power, transferred to the utility grid, is pulsated instantaneously with twice of the utility frequency when the output current is synchronized with the grid voltage. The pulsated output power is propagated upstream toward a renewable energy source, and eventually causes the large double-fundamental frequency current ripple drawn from the energy source. This low frequency current ripple brings forth several drawbacks such as power harvesting deterioration and energy source's life shortening. Thus, the power pulsation decoupling schemes, which prevents to draw the current ripple from the energy source, has been proposed.

A straightforward solution is to use a large decoupling capacitor, usually being electrolytic capacitor in the range of mF, at the energy source terminal. Even though this method is effective and popularly used, it is undesirable because using electrolytic capacitor causes other problems such as decreasing converter reliability and increasing the volume and cost of the converter [79]. The electrolytic capacitor has a very limited expected service time and becomes shorter at the hot temperature of a summer season.

To avoid the electrolytic capacitor, the active compensation solutions using auxiliary power circuits [80]-[83] have been proposed. These approaches have been mostly proposed for single-stage power converter. For example, the flyback-type utility interactive inverter with the power decoupling circuit was proposed by Shimizu [81]. The basic idea is to draw constant current from the energy source, while supplying the current ripple through the small dc capacitor of the power decoupling circuit. Some other topologies, motivated by this circuit, have improved the drawbacks, such as low power efficiency of a maximum 70% or excessive voltage spike [82].

A potential solution, applicable only for two-stage power converter architectures, is to use the existing dc-link capacitor with properly designed control loop [84]. With the use of a control loop, large decoupling capacitors may be avoided. The method shows the advantages of not having extra components and power conversion losses. However, the control loop should be designed carefully to have a sufficient gain at the utility frequency. Otherwise, the output current, which is injected to the utility grid, is heavily distorted due to the large dc-link voltage ripple caused by the power pulsation with the double-fundamental frequency. Moreover, the dc-link voltage experiences a large overshoot or undershoots because of requirement of very slow bandwidth of control loop.

The feed forward compensation scheme was also proposed to generate a voltage ripple on the dc-link capacitor purposely, therefore supplying pulsated output power [85]. Based on the correlation between the instantaneous output power and instantaneous dc-link capacitor, a ripple cancellation duty ratio is obtained and fed forward to the dc-link voltage control. To further reduce the ripple current, the simple proportional control is introduced to compensate the error of the ripple cancellation duty ratio. Moreover, the active power filter [85]-[86] or the modulation index compensation method [87] has been reported.

1.5 Major contributions and dissertation outline

This dissertation makes an effort to develop a generalized control structure for two-stage power converter architecture operated in a renewable energy power system. The generalized control structure is based on the two-loop average-mode-control technique and created by reconstructing the conventional control structure and feedback configuration.

It can be broadly used for both dc-dc and dc-ac power conversion being subject to two-stage power converter architecture while offering several functionalities required for renewable energy power system.

The generalized control structure improves the performance of a battery energy storage system by providing a new control platform to apply the unified control concept. The unified control concept enables the converters to operate under a smooth and continuous mode changes, while performing the two distinctive control objectives of maximum power harness and battery overcharge protection. Thanks to the smooth mode transfer, the disadvantages of the conventional stop-and-go concept, such as the transient over-voltage or –current, extra energy losses, power quality issue, and complicated decision process associated with multiple-mode control, are totally eliminated.

The generalized control structure also improves the performance of single-phase grid-connected systems, compared with the traditional control structure. The generalized control structure allows a fast voltage control loop bandwidth for the active ripple current reduction scheme using two control loops. As a result, the transient overshoots or undershoots at the dc-link voltage are significantly reduced during dynamic load changes.

This dissertation includes the development of a new modeling approach, which is named the general aggregated modeling method. This method is based on the modification of the subsystem-integration approach to provide continuous-time small-signal models for all of the two-stage power converters in a unified way. It significantly reduces the modeling procedure by treating a two-stage power converter as a single-stage power converter with current sinking or sourcing. The difficulty of a linearization caused by time-varying state variables is avoided by using the quasi-steady state concept [61]-[65].

The modeling technique is demonstrated by using examples of the two-stage dc-dc and dc-ac power conversions for a battery energy storage system and grid-connected power system which employs the thermoelectric and photovoltaic energy source respectively. The dynamic behavior of these two-stage converters is analyzed with the consideration of modeling accuracy associated with the perturbed frequency and its impact on the control design. Consequently, the compensators used for the generalized control structure are properly designed by the frequency domain technique.

This dissertation consists of five chapters, organized in the following manner. Chapter 2 of this dissertation describes the battery energy storage system using a thermoelectric generator and its modeling. A thermoelectric generator is characterized, and requirements of a power converter are addressed. To achieve the efficiency target of 95%, the existing design technologies are evaluated by exploring simulations and experiments. Also, the integration modeling approach is established at the basis of theoretical rationale. Converter dynamics is analyzed and the modeling accuracy is discussed.

Chapter 3 establishes the generalized control structure and discusses a close-loop control design using the continuous-time small-signal model. The existing conventional control structure is reviewed first. A unified control concept which allows a smooth mode transition is presented. Simulation and experiments are performed to support the unified control concept and verify the performance improvements.

In Chapter 4, efforts are made to extend the research works for a single-phase grid-connected system using a photovoltaic. First, the proposed aggregated modeling approach is generalized. After which, the simplified assumption and related limitation of the

aggregated modeling are addressed. The detailed and theoretical derivation is presented to generalize it. The small-signal model of a two-stage dc-ac power converter is given, and some aspects that impact the control design are highlighted. The novel active ripple compensation scheme is proposed to attenuate the low frequency input current, based on the generalized control structure, and the compensator designs are detailed. The issues of the conventional control structure associated with a ripple current reduction are also investigated. Simulations of the proposed active scheme provide to see the improved ripple reduction. The experimental results support the effectiveness of the proposed active scheme as well.

Conclusion of this dissertation is presented in Chapter 5. Future work is summarized for the further development of two-stage power converter control operated for renewable energy power systems.

Chapter 2

Battery Energy Storage System and Aggregated Modeling Approach

2.1 Introduction

A thermoelectric generator is a unique solid-state device for converting heat energy to electricity. It is clean, independent, and environmentally friendly energy source, and very reliable and silent because of a lack of moving parts. In some areas where a considerable amount of energy is unused or wasted in the form of exhaust heat, the application of a thermoelectric-based recovery system has led to reported improvements in overall system efficiency. Examples of this effect have been observed in automobiles, steam-based power stations, and subsea wellheads [88]-[94].

Thermoelectric generators mostly work with battery energy storage devices, such as lead acid, lithium, and nickel batteries or super capacitors. Automotive thermoelectric exhaust heat recovery system sets a good example of a battery energy storage system. The internal combustion engine used in vehicles is highly inefficient, and much of the energy is transformed into waste heat which dissipates to the air. According to Yang [95], from

100% of energy produced by an internal combustion engine, about 40% of the energy is dissipated through exhaust. The U.S. Department of Energy's (DOE) Energy Efficiency and Renewable Energy Laboratory expects 10% improvement of the energy efficiency by using thermoelectric exhausted heat recovery system without increased emissions [96].

In this chapter, we will provide the basic principles and the electrical characteristics of the thermoelectric generator. Power converter requirements will be addressed, and the design process of a two-stage power converter will be detailed. Later, a novel aggregated modeling approach will be proposed for the converter. Based on the modeling approach, analysis of the converter dynamics of stage converters occurs, with justification of its accuracy later in the chapter.

2.2 Thermoelectric effects and characteristics

The basic thermoelectric device is based on the fact that a temperature difference between two points in a conductor or semiconductor results in a voltage difference between these two points [96]. In other words, a temperature gradient in a conductor or a semiconductor gives rise to a built-in electric field. This phenomenon, known as the "Seebeck effect", was discovered by Thomas Johann Seebeck in 1826. The Seebeck coefficient (α) is defined to gauge the magnitude of this effect as the potential difference (dE) developed per temperature difference (dT) and can be expressed in (2.1).

$$\alpha = \frac{dE}{dT} \tag{2.1}$$

In a thermoelectric device, a thermocouple is made of n-type and p-type semiconductor materials as shown in figure 2.1. The semiconductor materials are connected electrically in series with highly conductive metal bars and are stacked between thermally conducting and electrically insulating ceramic plates. Hot fluids flow on the one side of the ceramic plates, and cold fluids flows on the other side, as temperature differences build up between the two ceramic plates. The majority carriers: the electrons in the n-type semiconductor and the holes in the p-type semiconductor, near the hot plate are more energetic, and therefore, have faster velocities than those near the cold plate. Consequently, it causes the diffusion of the majority carriers, from the hot plate to the cold plate. The diffused of majority carriers causes the buildup of opposing charger from the hot plate to the cold plate. The charges buildup near each place until the electric field between two plates prevents additional diffusion of the excess majority carriers. This leads to the thermoelectric electromotive force, which corresponds to electric potential for power generation.

The electromotive force of the thermoelectric couple (e_{tem}) is expressed in (2.2); where, T_{hj} and T_{cj} are the temperature of corresponding junctions, ΔT is the temperature gradient, and α_p and α_n are the Seeback coefficients of the specified semiconductor materials.

$$e_{tem} = \left(\alpha_p - \alpha_n\right)\left(T_{hj} - T_{cj}\right) = \alpha_{pn}\Delta T \tag{2.2}$$

When connecting a load resistance (R_L) to the thermoelectric couple, the thermoelectric couple generates the current (i_{tem}) and the voltage (v_{tem}), which are represented by (2.3) and (2.4) where R_{tem} is the internal electrical resistance of the couple.

$$i_{tem} = \frac{e_{tem}}{R_{tem} + R_L} \tag{2.3}$$

$$v_{tem} = e_{tem} - R_{tem} i_{tem} \tag{2.4}$$

A typical thermocouple unit generates around 1.0 ~ 5.0 mV of the electromotive force depending on its material and structure. To obtain a reasonable power and voltage, several thermoelectric couples are electrically connected in a series-parallel arrangement. Considering a thermoelectric generator of a number (N_s) in series and (N_p) in parallel, the internal resistance (R_{tem}) needs to be multiplied by (N_s / N_p) to represent the electrical resistance of the entire thermoelectric generator. Moreover, the electromotive force (e_{teg}) and output current (i_{teg}) generated by the thermoelectric generator becomes, respectively, (N_s) and (N_p) times greater than those for the thermoelectric couple. As a consequence, the relevant equations for the thermoelectric generator composed by (N_s) thermocouples in series and (N_p) in parallel are given as follows.

$$R_{teg} = \frac{N_s}{N_p} R_{tem} \tag{2.5}$$

$$e_{teg} = N_s \alpha_{pn} \Delta T \tag{2.6}$$

$$i_{teg} = N_p I_{teg} \tag{2.7}$$

$$v_{teg} = N_s \alpha_{pn} \Delta T - \frac{N_s}{N_p} R_{tem} i_{teg} \tag{2.8}$$

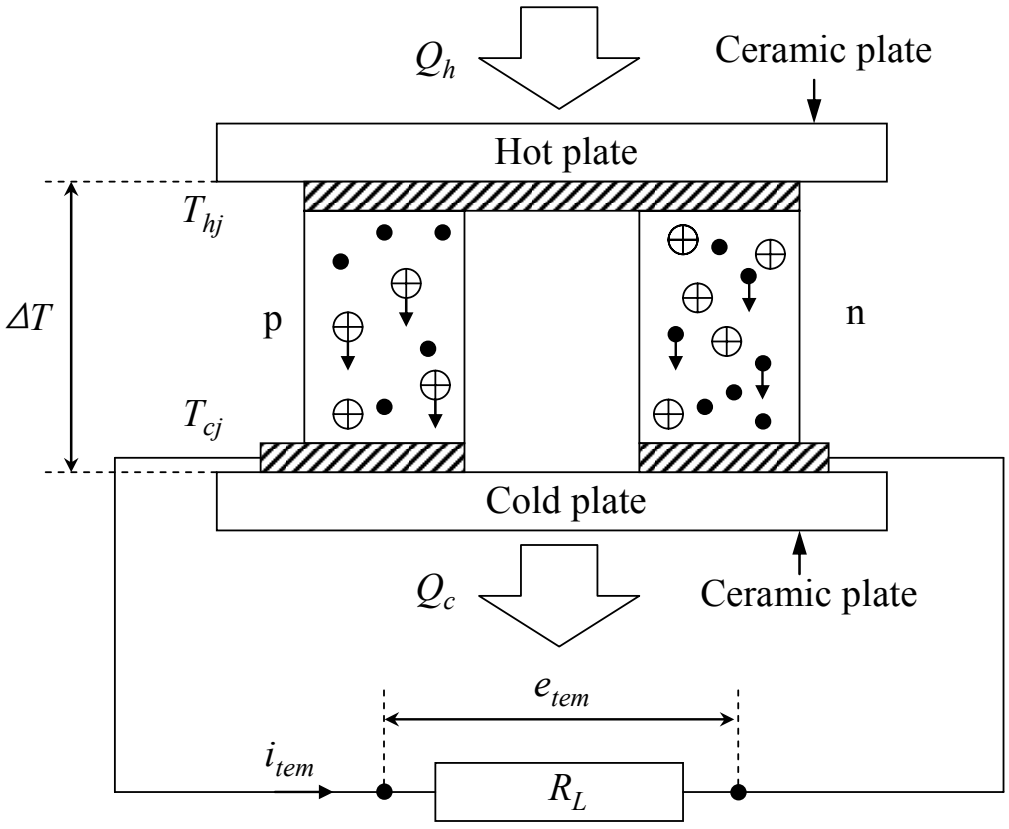


Figure 2.1 Basic structure of semiconductor thermoelectric couple.

The output power (p_{teg}) delivered by the thermoelectric generator to the load (R_L) can be given by the product of the output voltage (v_{teg}) and the current (i_{teg}), i.e.,

$$p_{teg} = N_s \alpha_{pn} \Delta T I_{teg} - \frac{N_s}{N_p} R_{tem} {I_{teg}}^2 \tag{2.9}$$

Consider the thermoelectric generator composed by the specified number of thermocouples ((N_S) in series and (N_P) in parallel with a given internal resistance (R_{TEM})). According to (2.8) and (2.9), the output voltage and power are determined by the temperature gradient and the current (i_{teg}) flowing in the load. The output voltage (v_{teg}) proportionally decreases with the increase of the current (i_{teg}). The open-circuit output voltage, i.e. the electromotive force (e_{teg}) of the thermoelectric generator, increases with rising temperature gradient. As a result, the output power has a parabola-shaped curve.

Figure 2.2 illustrates actual measurements of the output voltage vs. output current and the output power vs. output current under three different temperature gradients. They are often referred to as voltage-current or power-current characteristics. It is clearly seen that the equations of (2.8) and (2.9) are well matched with the actual measurements. Note that the point, at the intersection of the dashed line with the individual power curve, specifies the maximum power point of that given temperature gradient.

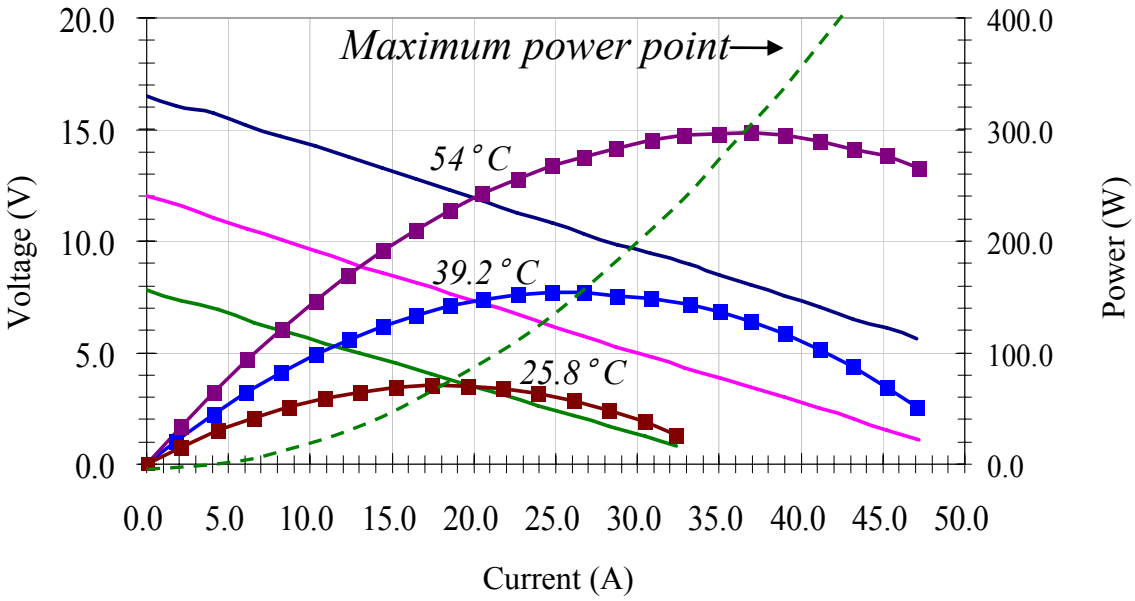


Figure 2.2 Electrical characteristics of thermoelectric generator.

2.3 Requirements and selection of power converter

Even though the output voltage of a thermoelectric generator can be increased by stacking several thermoelectric couples in series, most thermoelectric generators currently available produce a low output voltage, because of the fabrication problems associated with stacking many modules in series; such as, seals, temperature distribution and other packaging issues. Moreover, as seen in Figure 2.2, the low output voltage varies dynamically in wide ranges in accordance with the temperature gradient and the output current. The temperature gradient varies because the working fluid's temperature and mass flow rates fluctuate at the hot and cold plates.

These properties of a thermoelectric generator require a power conditioning circuit to incorporate the battery energy storage devices. More often, the thermoelectric generator, which generates low, inconsistent dc voltage, is connected to a battery storage device by using a dc/dc converter capable of step-up and -down conversion to manage the electrical output voltage [97].

For the step-up/-down, dc-dc converter, various topologies have been proposed to satisfy the specific performances and requirements. The topology review of the step-up/-down, dc-dc converters indicate that the two-stage boost-buck converter is most suitable for the thermoelectric generator. The two-stage boost-buck converter consists of two basic topology dc/dc converters. A boost topology converter is used as the front-end side converter and a buck as the back-end. The boost converter regulates the dc bus voltage in order for it to be greater than the input voltage, and the buck converter regulates the output voltage. Compared to the non-inverting buck or boost converter presented in [99], this

topology requires more inductors and capacitors. However, the complementary switching pattern and the control strategies used for general converters are applied without any modifications. It benefits from the well-matured technologies associated with circuit analysis, control, and practical implementation. Moreover, this converter is capable of allowing more flexibility for energy storage, when the dc-bus capacitor is replaced by additional energy storage devices.

Control aspects make the two-stage boost-buck converter more attractive since the converter's performance can be improved with a flexible control structure. As reviewed in Chapter 1, the thermoelectric battery energy storage system requires two different control schemes. Maximum power point tracking scheme is required to maximize energy harvesting while power matching scheme is necessary to manage the battery state-of-charge. The flexible control structure produced by two-stage converters allows the easy accommodation of two different control schemes. Figure 2.3 shows the two-stage boost-buck circuit topology, which will be employed for the thermoelectric battery energy storage system.

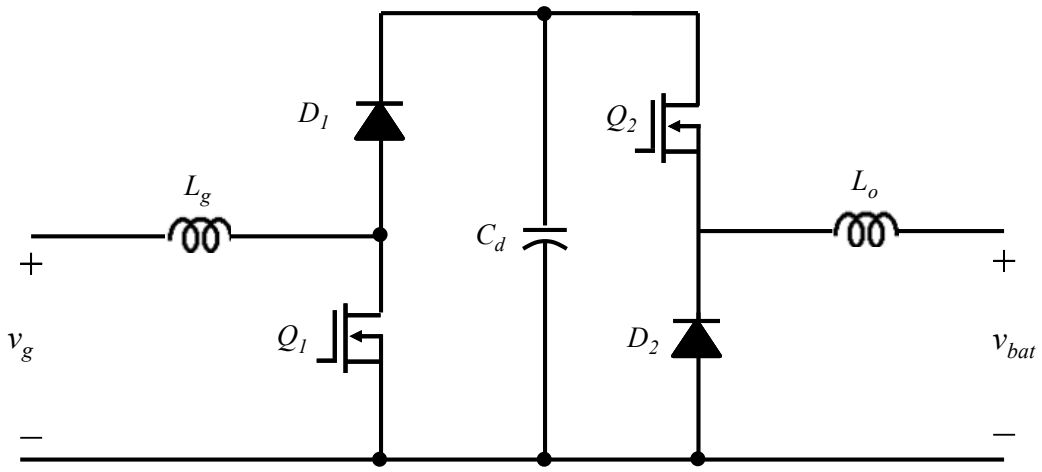


Figure 2.3 Two-stage boost-buck circuit topology for thermoelectric battery energy storage system.

2.4 Two-stage boost-buck converter design

According to literature surveys, typical battery energy storage systems operate with a power higher than 1KW [71]-[78]. For such a power level, the two-stage boost-buck converter requires a large current capability because of the low operating voltage of the thermoelectric generator. The large current brings forth significant conduction losses and the conduction losses overcome switching losses to become dominant. Therefore, it is important to increase circuit conductivity which leads to higher efficiency.

In this design, three existing design techniques are evaluated to increase current capability and circuit conductivity. These techniques include synchronous rectification, multiple switches, and multiple phases. For a reasonable evaluation, the nominal power of thermoelectric generator would be set to 1.5kW. Input voltage of the converter is from 7.5 to 25V, and the output voltage is from 12.3 to 16.5V. Dc link voltage is fixed to 30V. The maximum allowable input current is set to 120A.

2.4.1 Diode rectification vs. synchronous rectification

Synchronous rectification is the technique in which a power diode is replaced with an auxiliary metal-oxide-semiconductor-field-effect-transistor (MOSFET) in the standard converter topologies which has the complimentary PWM signal to the main MOSFET. The auxiliary MOSFET is referred to as the synchronous rectifier. Whenever the power diode would normally conduct, the synchronous rectifier conducts by the gate turn-on of the complimentary PWM signal. The conduction losses would be reduced when the synchronous rectifier has a lower on-resistance ($R_{ds\text{-}on}$). To avoid a shorted circuit, dead-

time is necessary between the main MOSFET and the synchronous rectifier. Losses of the conventional diode rectification and synchronous rectification are determined using (2.10) and (2.11), where v_{ak} is the diode forward voltage drop between anode and cathode, and R_{on} is the diode on-resistance. The e_{on} and e_{off} are MOSFET switching energies of turn-on and turn-off, f_{sw} is switching frequency, and i_b is base current flowing through.

$$p_{diode} = v_{ak} \cdot i_b + R_{on} \cdot i_b^{\,2} \tag{2.10}$$

$$p_{mosfet} = R_{ds-on} \cdot i_b^{\,2} + \left(e_{off} + e_{on}\right) \cdot f_{sw} \tag{2.11}$$

Contrary to expectation, the synchronous rectification shows 0.5% lower efficiency than that of a conventional diode rectifier in PSPICE simulation. The power MOSFET model used in the simulation is an IRFP2907 from International Rectifier. It has a 209A current rating and $R_{ds\text{-}on}$ is 4.5mΩ when the junction temperature is 25°C. The diode model is Schottky CPT20145 from Microsemi with v_{ak} = 0.16V, and R_{on} = 3.4mΩ. The efficiency drop comes from the additional switching losses of a synchronous rectifier. For large current applications, it is necessary to select a sufficiently low $R_{ds\text{-}on}$ MOSFET or to configure multiple synchronous rectifiers in parallel.

2.4.2 Single-switch vs. multiple-switch

A MOSFET is a channel based device which permits a high switching speed. When it conducts current by the gate turn-on, the drain-to-source voltage becomes linearly proportional to both the current and the on-resistance. Paralleling multiple MOSFETs reduces the total on-resistance and the condition losses while the switching losses are not significantly affected. Conduction losses of multiple-MOSFETs are calculated by (2.12), where N_m is the number of MOSFETs in parallel. The total turn-on and turn-off losses are not significantly affected by multiple-MOSFETs.

$$p_{mosfet,cond} = \left(\frac{R_{ds-on}}{N_m} \right) \cdot i_b^{\,2} \tag{2.12}$$

Simulation results using multiple-MOSFETs are summarized in Table 2.1. It is clear that efficiency is improved significantly in comparison to a single-MOSFET. This improvement is more effective at the lower input voltage condition due to larger current under the same power level.

TABLE 2-1 EFFICIENCY EVALUATION OF SINGLE-PHASE MULTIPLE MOSFETS.

Voltage condition	Single MOSFET (%)		Two MOSFETs (%)		Three MOSFETs (%)	
	SR*	No SR*	SR	No SR*	SR*	No SR*
Input 7.5V, Output 12.3V	83.8	83.6	87.1	88.2	88.1	89.5
Input 16.5V, Output 16.5V	91.5	91.3	92.6	93.4	92.9	94.0
Input 25.0V, Output 16.5V	93.8	93.6	94.4	95.0	94.6	95.3

SR* = Synchronous Rectification.

2.4.3 Single-phase vs. multiple-phase

Most discrete semiconductors have a limitation on their pin-outs at 70A due to the thermal constraint. Current limit and converter efficiency are factors to consider in determining an optimum number of phases. Multiple-phases split the base current flow through both the MOSFET and diode. Conduction losses are reduced by the square of the current as shown in (2.13) and (2.14). Moreover, reduced base current saves parasitic resistive losses: such as, wire loss, printed-circuit-board (PCB) copper loss, and electrical contactor loss.

$$p_{mosfet,cond} = R_{ds-on} \cdot \left(\frac{i_b}{n_{ph}} \right)^2 \tag{2.13}$$

$$p_{diode} = v_{ak} \cdot \left(\frac{i_b}{n_{ph}} \right) + R_{on} \cdot \left(\frac{i_b}{n_{ph}} \right)^2 \tag{2.14}$$

The resulting efficiencies from using multiple-switches with two-phases are shown in Table 2.2. Efficiencies with three-phase circuits are summarized in Table 2.3. The effect of three-phases on efficiency is most noticeable at the low voltage level. The maximum efficiency is expected to be at 95.8 percent at input 25V and output 16.5V. Minimum efficiency is 88.6 percent at input 7.5V and output 12.3V for two-phase, single MOSFET, and no synchronous rectification.

TABLE 2-2 EFFICIENCY EVALUATION OF TWO-PHASE MULTIPLE MOSFETS.

Voltage condition	Single MOSFET (%)		Two MOSFET (%)	
	SR*	No SR*	SR*	No SR*
Input 7.5 V, Output 12.3 V	88.7	88.6	90.3	90.6
Input 16.5 V, Output 16.5 V	93.7	93.7	94.2	94.5
Input 25.0 V, Output 16.5 V	95.3	95.3	95.6	95.7

SR* = Synchronous Rectification.

TABLE 2-3 EFFICIENCY EVALUATION OF THREE-PHASE MULTIPLE MOSFETS

Voltage condition	Single MOSFET (%)		Two MOSFET (%)	
	SR*	No SR*	SR*	No SR*
Input 7.5 V, Output 12.3 V	90.1	89.9	90.3	90.6
Input 16.5 V, Output 16.5 V	94.3	94.3	94.5	94.6
Input 25.0 V, Output 16.5 V	95.8	95.7	95.8	95.8

SR* = Synchronous Rectification.

2.4.4 Three-phase interleaved synchronous boost-buck converter

Based on the simulation results of the techniques explained above, efficiency evaluation is summarized in Figure 2.4. The best efficiency is observed at Case G, which uses two-switches, three-phases, and synchronous rectification. This is an understandable result; less current through each MOSFET should show better efficiency. However, other considerations must be made. Each additional MOSFET increases auxiliary and parasitic losses, circuit complexity, size, and price. Therefore, the number of power MOSFET should be minimized as long as the efficiency is acceptable. Cases E, F, G are likely to show the reasonable efficiency of 95 percent, but Case F is preferred because it uses less switches. For Case F, only six MOSFETs would be needed for the design, reducing parasitic and auxiliary losses. To further reduce the number of MOSFETs, a Schottky diode would be considered as a possible option to replace synchronous rectifiers. However, for high current capability, the Schottky diode becomes less attractive due to much larger the larger physical size than the MOSFET.

Figure 2.5 shows the proposed converter. The stage converters consist of three-phases. In each phase, a synchronous rectifier is employed and operates with a complementary gating signal with a prefixed dead-time. A small Schottky diode is paralleled with the synchronous rectifier to prevent excessive body diode reverse recovery current during the dead-time. A thermoelectric generator is placed on the converter input, and battery or other energy storage device is placed on the output.

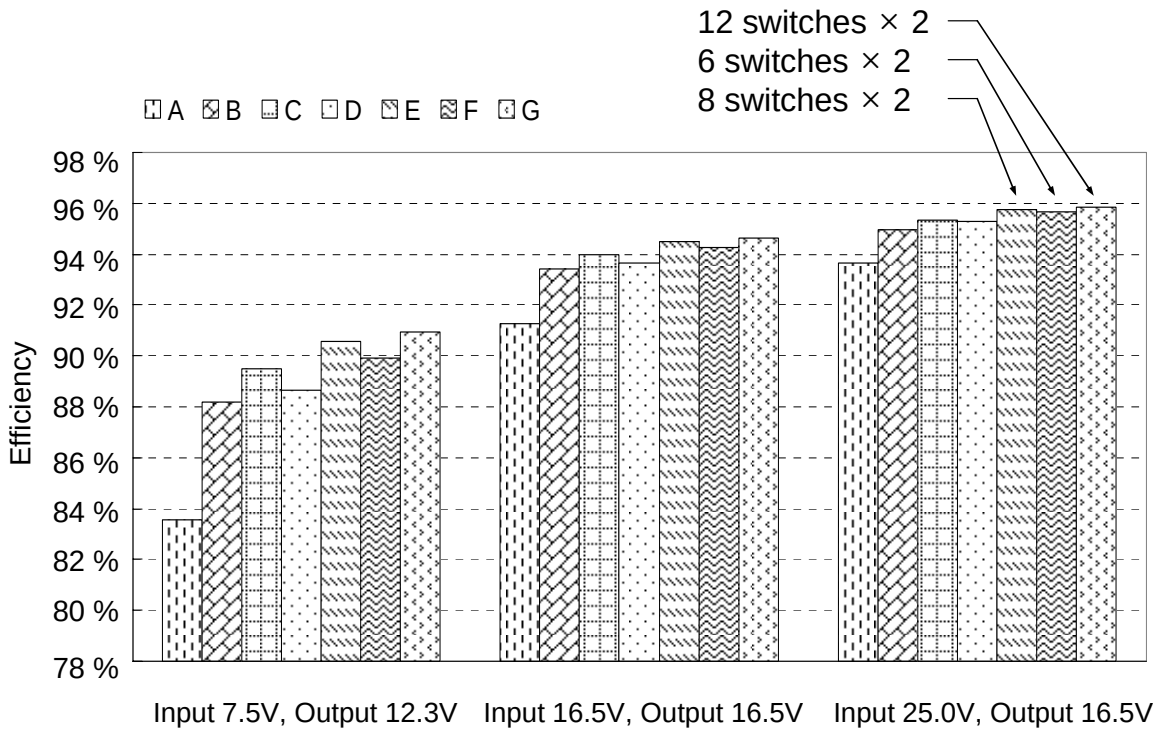


Figure 2.4 Efficiency evaluation of two-stage boost-buck converter using multiple-switch, multiple-phase, and synchronous rectification.

To attenuate the high-frequency current caused by converter switching action, high-frequency capacitors are added on the converter input and the output. To further reduce the switching ripple, the three-phases operates with a 120-degree phase shift from each other which is also known as interleaved operation. The switching ripple on the total current is canceled out by this operation. The dc-link capacitor serves as an energy buffer to compensate an unbalance between the stage converters. The thermoelectric generator is placed on the converter input, and the battery is on the output along with the standalone electrical load. For simplicity, the standalone electrical load is represented as a resistive load in this research.

Figure 2.6 illustrates the assembly of the prototype stage power converter where the first stage and the second stage power circuit configurations are essentially identical. It consists of four major parts: a three-phase power circuit, a digital and analog control circuitry, a set of auxiliary power supplies, and a set of three inductors. In this test unit, the current and voltage commands, and operation signals, such as run, stop, and emergency stop, are supplied by external digital circuitry.

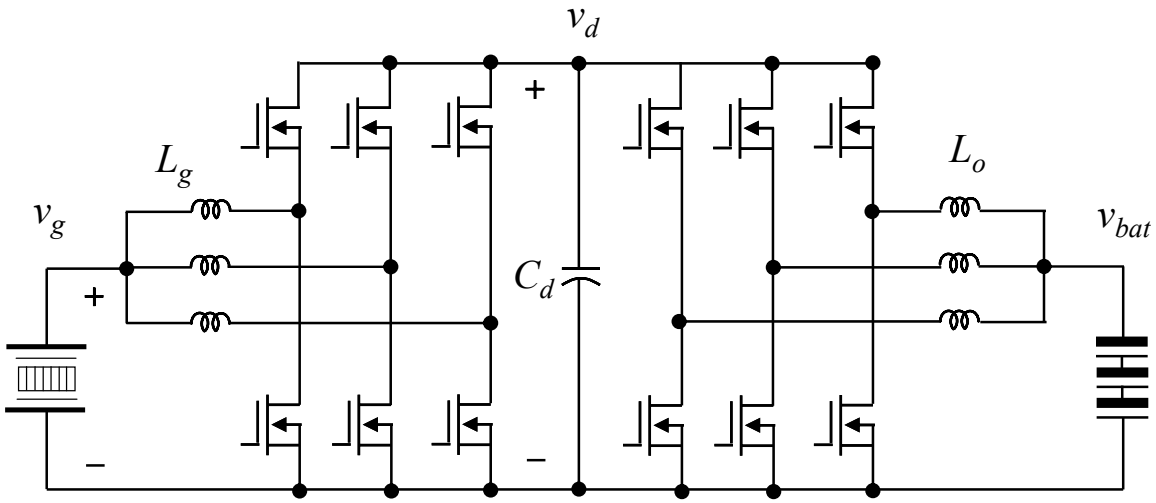


Figure 2.5 Proposed three-phase interleaved two-stage dc-dc converter topology.

The three-phase interleaved inductor current, the total current and the corresponding output voltage waveforms are shown in Figure 2.7. As mentioned before, the interleaved operation for three-phase significantly reduces the high frequency ripples related to device switching. With interleaved control, it is seen that the total current ripple and the output voltage ripple frequency is three times of switching frequency. The ripple amplitude becomes lowered even with a smaller value of capacitor.

Figure 2.8 shows the comparison of experimental efficiency and calculated efficiency of the two-stage boost-buck converter at different power levels, under 16.5V as both input and output voltages and a 40V dc link voltage. Both the calculated and experimental peak efficiencies are found to be around 96% at the light load condition. The peak at the light load implies that the conduction losses are the major contributor in the loss distribution.

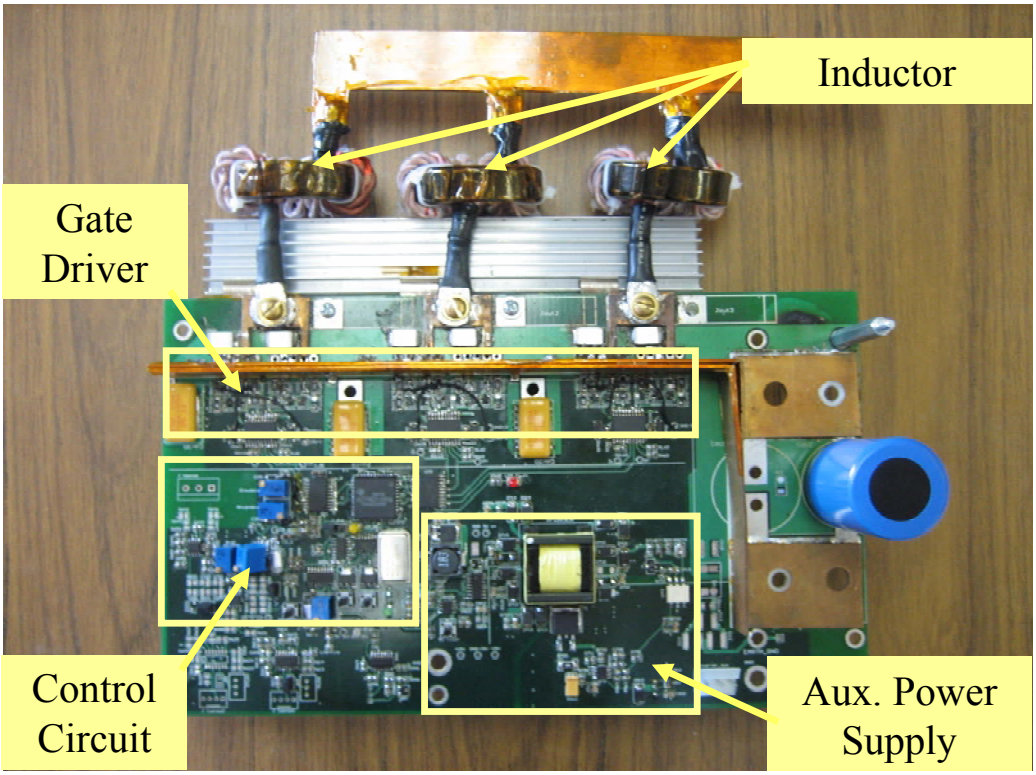


Figure 2.6 Hardware prototype unit of proposed three-phase interleaved stage converter.

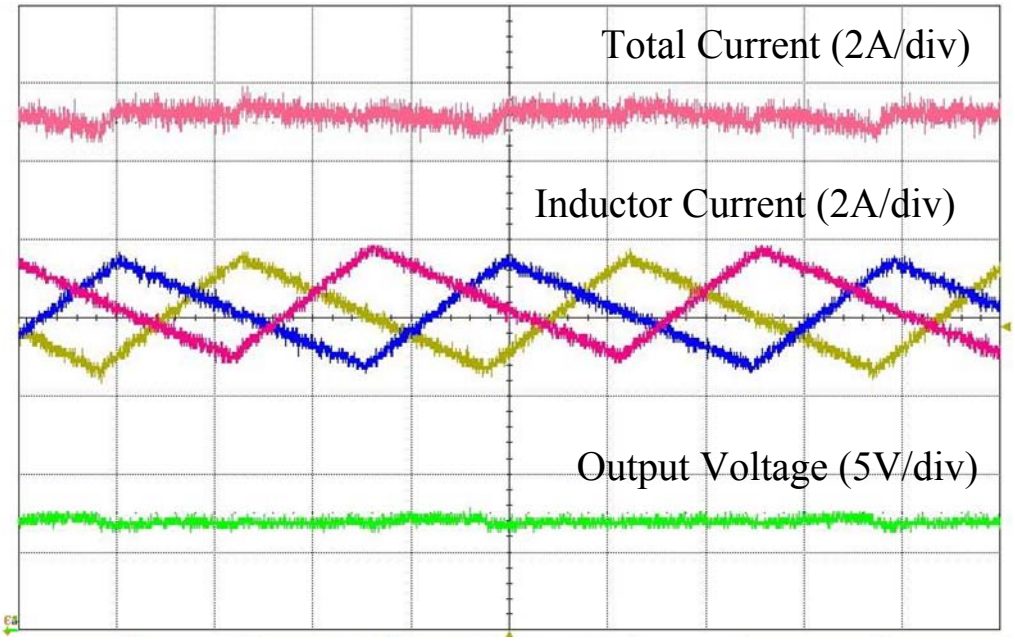


Figure 2.7 Experimental waveform of proposed three-phase interleaved stage converter.

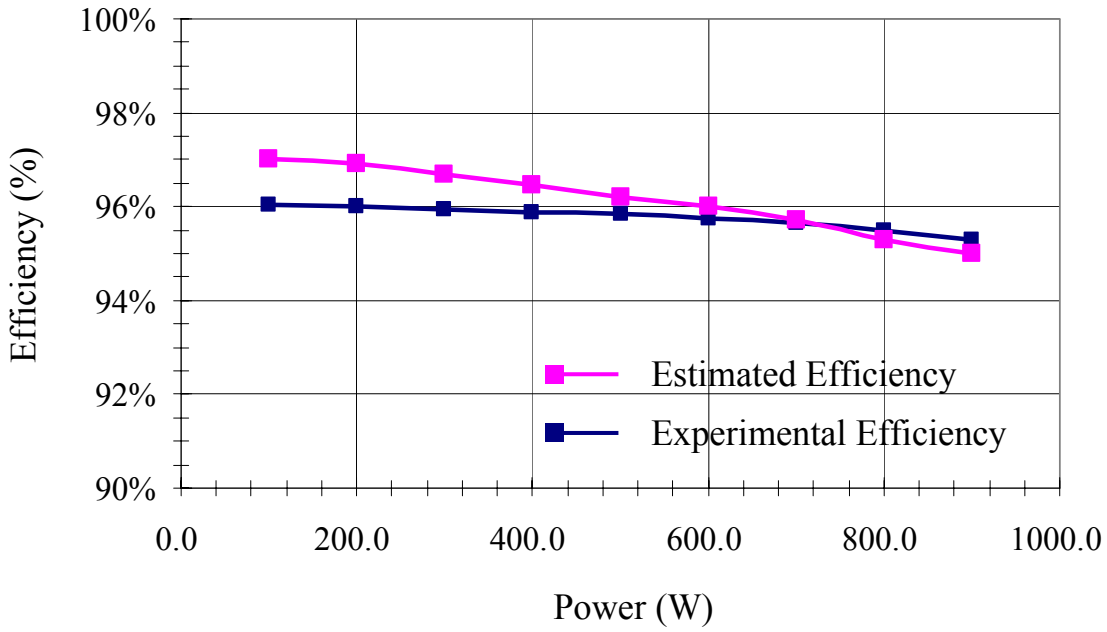


Figure 2.8 Experimental efficiency of stage-converter with estimated efficiency.

2.5 Aggregated modeling approach and modeling

The topology selection and the high efficiency design of the power converter were discussed in Section 2.4. In this section, the two-stage power converter modeling will be described. A two-stage converter architecture with a common dc link capacitor increases modeling complexity when utilizing the state-space averaging method. This difficulty will be simplified by the new modeling approach which applies the subsystem-integration approach. We will first start a simple discussion in which the three-phase interleaved synchronous boost-buck converter can be simplified as a single-phase equivalent circuit model.

2.5.1 Single-phase equivalent circuit model

The state-space averaging method is the most commonly used approach for deriving a power converter model. For a general synchronous boost converter shown in Figure 2.9 (a), the switching of the active device creates two distinctive sub-circuits when it conducts current and when it does not. Based on time averaging, these sub-circuits are converted to the averaged circuit model shown in Figure 2.9 (b). The controlled voltage source and current source in Figure 2.9 (b) are given as follows, where *d* denotes duty cycle.

$$v_c = v_o \cdot (1-d) \tag{2.15}$$

$$i_d = i_L \cdot (1-d) \tag{2.16}$$

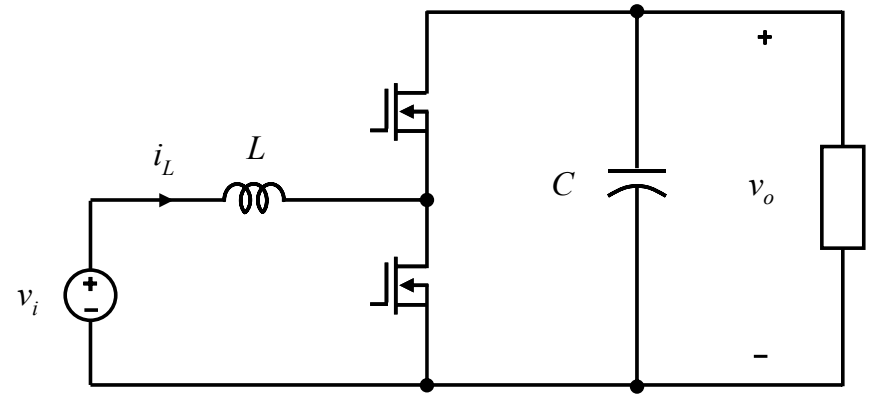
For a three-phase interleaved boost converter, the input and output voltages are commonly connected to each other, as shown in Figure 2.10. The control duty cycle (d) is the same, because there is only one feedback control loop. Thus, the controlled voltage sources in the three-phase converter are the same and can be represented by a single voltage source. The current source also can be represented by a single current source with a total inductor current, which is the same as an input current. As a result, the inductors for different phases are configured in parallel, and thus it can be replaced by a single equivalent inductance ($L_{eq.}$). For symmetric inductance in each phase (L_1=L_2=L_3=L), the equivalent inductance is the simple inductance in parallel as shown in (2.17).

For a three-phase interleaved buck converter, the same derivation can be presented. As a result, the average circuit model of the three-phase interleaved synchronous boost-buck converter can be simplified as a single-phase equivalent boost-buck converter, as shown in Figure 2.11. The equivalent inductance has one third of the each phase inductance, where L_{geq} denotes input equivalent inductance, and L_{oeq} denotes output equivalent inductance.

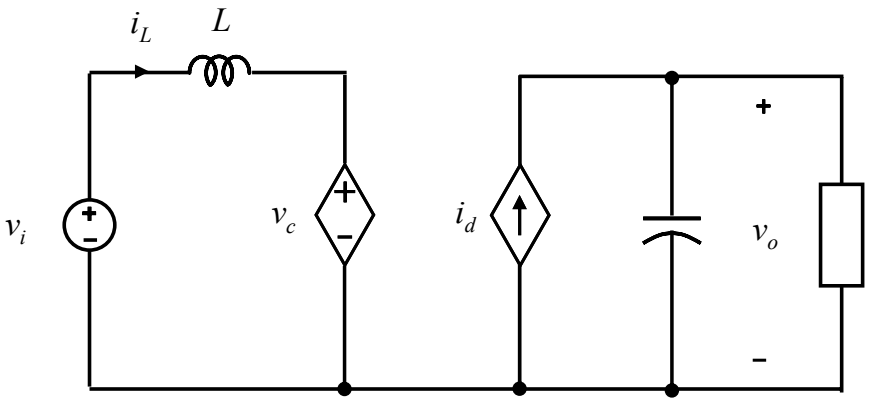
$$L_{eq} = \frac{L}{3} \tag{2.17}$$

$$L_{geq} = \frac{L_g}{3} \tag{2.18}$$

$$L_{oeq} = \frac{L_o}{3} \tag{2.19}$$



(a)



(b)

Figure 2.9 Equivalent circuit model of synchronous boost converter; (a) typical synchronous power converter and (b) equivalent circuit model.

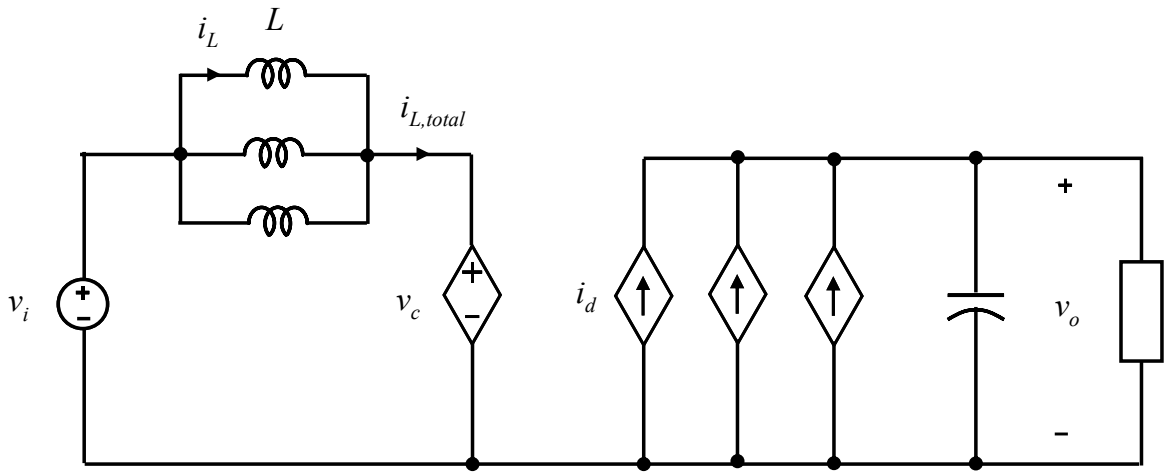


Figure 2.10 Equivalent circuit model of three-phase interleaved boost converter.

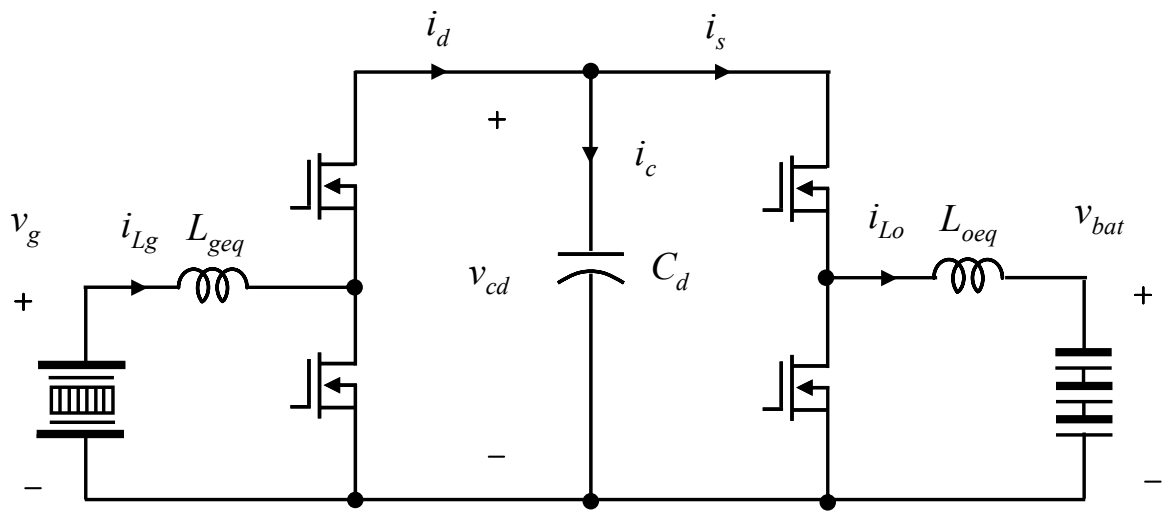


Figure 2.11 Equivalent circuit model of three-phase interleaved synchronous boost-buck converter.

2.5.2 Aggregated modeling approach and implementation

As discussed in Chapter 1, the subsystem-integration approach uses the modeling of the sub-converters under a standalone condition. Dynamics among the sub-converters are indirectly represented by using two-port parameters without any considerations. This simplification is the major reason behind the unclear insight for dynamics. For better dynamics representation, the fundamental behaviors of the state variables are required (i.e. inductor currents and capacitor voltages, among the sub-converters).

For the first-stage converter shown in Figure 2.11, the inductor current (i_{Lg}) during device switching is shown in Figure 2.12 (a). The current of the synchronous rectifier, denoted as i_d, is shown in Figure 2.12 (b). In those figures, T_s designates switching period, "–" designates averaged value over one switching period, and d_g is duty cycle of the first-stage converter. For the steady-state condition, the averaged synchronous rectifier current of the first-stage converter can be represented as (2.20). In similar way, Figure 2.13 (a) shows the second-stage inductor current (i_{Lo}). The current of the synchronous rectifier (i_s) is illustrated in Figure 2.13 (b), where d_o is duty cycle of the second-stage converter. The averaged synchronous rectifier current of the second-stage converter can be represented as (2.21).

$$\bar{i}_d = \bar{i}_{Lg} \cdot \left(1 - d_g\right) \tag{2.20}$$

$$\bar{i}_s = \bar{i}_{Lo} \cdot d_o \tag{2.21}$$

Next, the current flowing into the dc link capacitor in Figure 2.11 (denoted as i_c) is obtained by subtracting i_d from i_s. Substituting the capacitor voltage (v_{cd}) for i_c, we can derive:

$$C_d \frac{dv_{cd}}{dt} = i_d - i_s \tag{2.22}$$

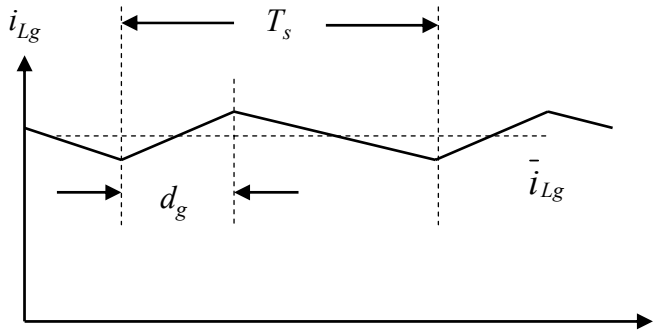
Averaging (2.22) over one switching cycle, and substituting (2.20) or (2.21) into (2.22) gives the following equations.

$$C_d \frac{d\bar{v}_{cd}}{dt} = \bar{i}_{Lg} \cdot \left(1 - d_g\right) - \bar{i}_s \tag{2.23}$$

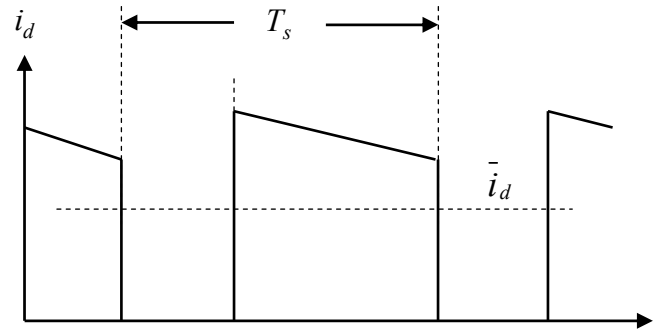
$$C_d \frac{d\bar{v}_{cd}}{dt} = \bar{i}_d - \bar{i}_{Lo} \cdot d_o \tag{2.24}$$

Now we can represent the equations of (2.23) and (2.24) by equivalent circuit models shown in Figure 2.14. The equivalent circuits are a simple form of the stage-converter and the controlled current source. The controlled current sources are used to represent the dynamics between the stage-converters. This idea is similar to a conventional subsystem-integration approach in the sense that each converter is modeled

under a standalone operation, but the controlled currents are used instead of the two-port parameters. This is in order to represent dynamics between the stage-converters. This idea can be extended further to the arbitrary multiple-stage power converter.

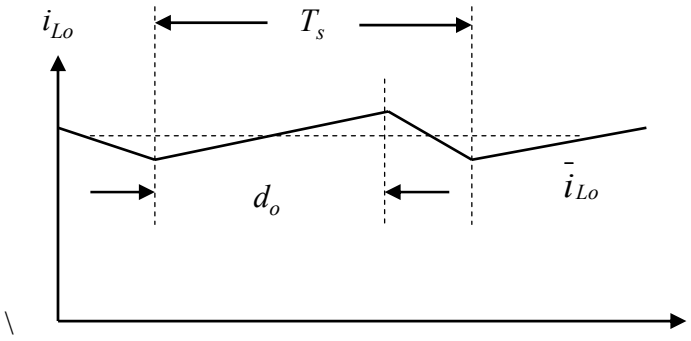


(a)

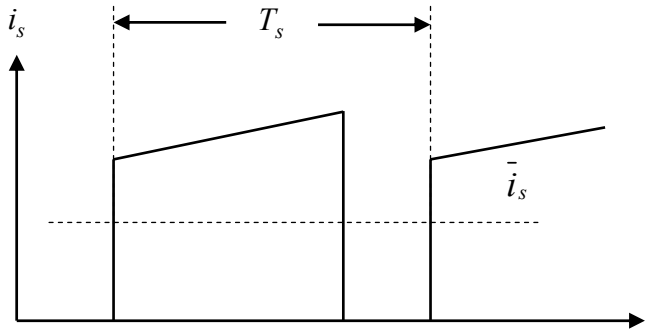


(b)

Figure 2.12 Instantaneous current waveform of first-stage converter; (a) inductor currents and (b) synchronous switch current.



(a)



(b)

Figure 2.13 Instantaneous current waveform of second-stage converter; (a) inductor currents and (b) synchronous switch current.

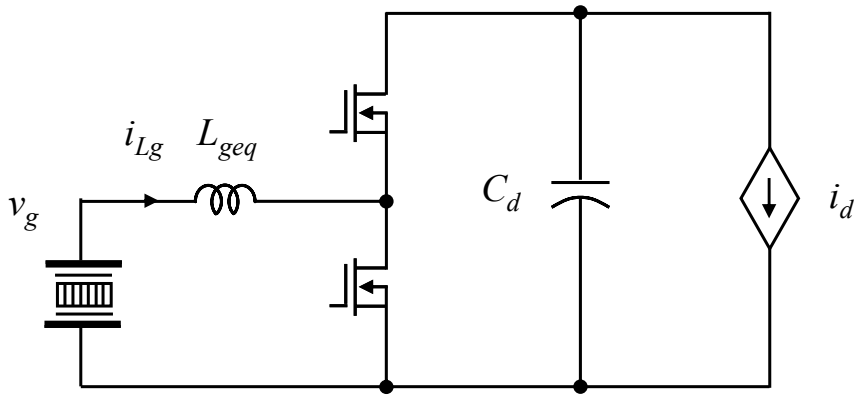
Based on the idea discussed above, a novel modeling approach, named aggregated modeling approach, is proposed for multiple-stage power converters. It gives intuitive and clear insight for the dynamics, while simplifying the modeling efforts significantly. The modeling processes to implement the aggregated modeling approach are as follows:

1) The multiple -stage power converter is first decomposed into multiple subsets of the converter. The subset converters consist of the stage-converter and the controlled current source. The dc link capacitor is treated as an output capacitor or input capacitor, which is included in multiple subsets of the converter.

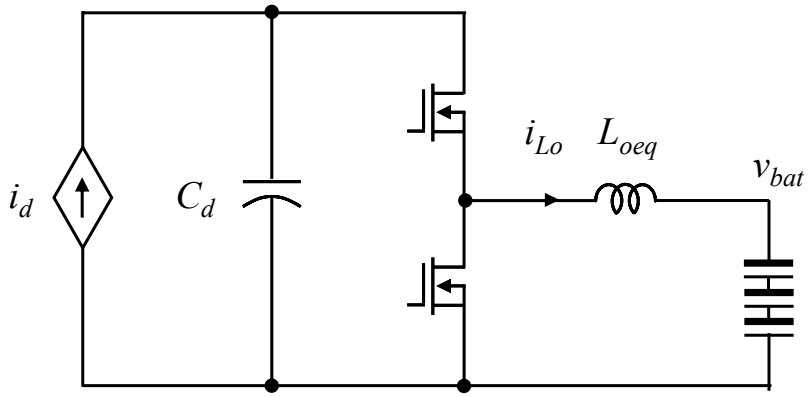
2) The next step is to derive the state-space averaging equations for multiple subsets of the converter, respectively. The currents flowing out or into the stage-converter are averaged, and then represented by the state-space variables. The subset converter has only a single inductor and a single capacitor, as basic converters. Therefore, the state-space averaging equations are simply obtained by conventional ways.

3) The state-space equations derived in step 2) are aggregated. The controlled current source terms are substituted by the state-space variables, which are derived from the averaged currents flowing out or into the stage-converter. The resultant equations predict the large-signal characteristics of the two-stage converters.

4) To complete this model, the aggregated state-space equations are finally linearized by introducing the small perturbations. As a result, small-signal averaged state-space equations are obtained with having linear time invariant expressions. The resultant equations predict the small-signal characteristics of the two-stage converters. Thus, major control-to-output transfer functions are derived.



(a)



(b)

Figure 2.14 Subset converter of two-stage boost-buck circuit with current sources; (a) first-stage converter and (b) second-stage converter.

2.5.3 Thermoelectric energy storage system modeling

As discussed in Section 2.4.1, it is seen that that modeling of the three-phase interleaved converter is simplified by using the singe-phase equivalent circuit. On the other hand, equation (2.4) provides the electrical equivalent circuit of the thermoelectric generator, which is characterized with an electromotive force (e_{teg}) and an internal electrical resistance (R_{teg}) [99]. The short-term output characteristic of the battery can be modeled by a first order linear electrical model [100]-[101]. As a result, the equivalent circuit model of an overall battery energy storage system is shown in Figure 2.15, where the dc-link capacitor includes its Equivalent Series Resistance (ESR).

Deriving the large-signal and small-signal state-space equations begins with decomposing the equivalent electrical circuit model of Figure 2.15 into two subsets of the converter shown in Figure 2.16. Based on the subinterval analysis associated with their turn-on and -off, the state-space averaging equations for two subset circuits are obtained as (2.25) and (2.26).

Aggregating the state-space averaging equations of (2.25) and (2.26), the large-signal averaged equations are obtained in a form of the state-space representative expressed in (2.27) and (2.28). The corresponding large-signal equivalent circuit model is shown in Figure 2.17.

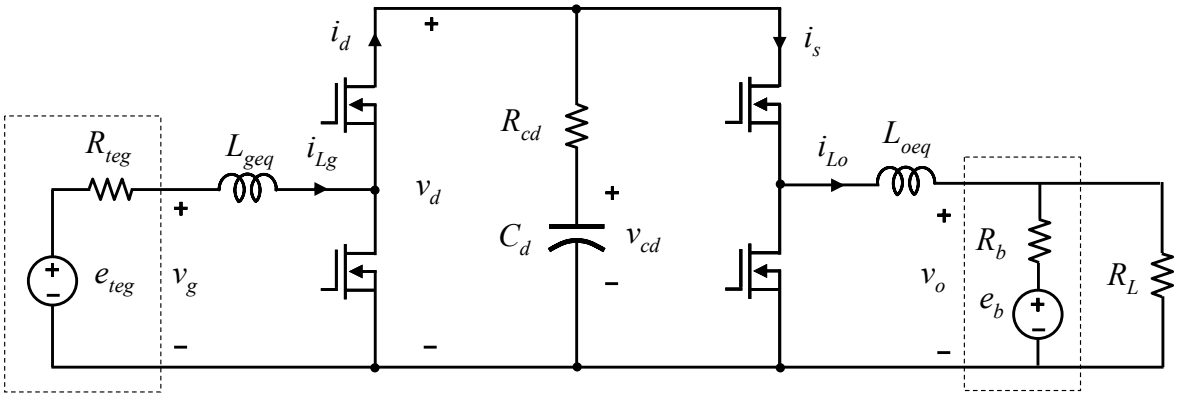
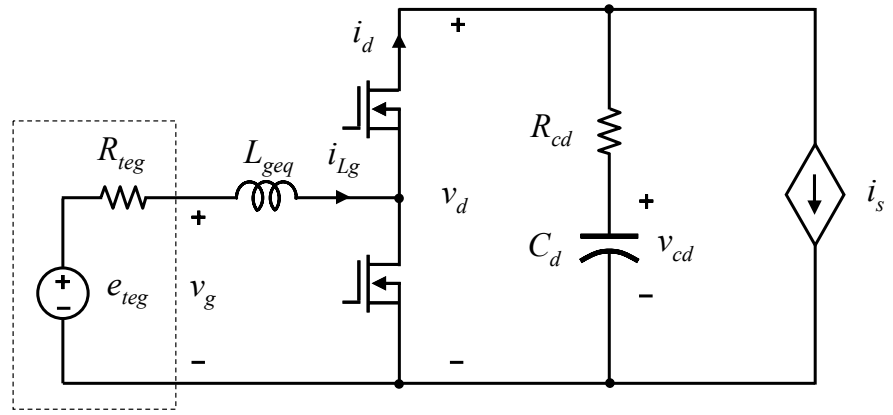
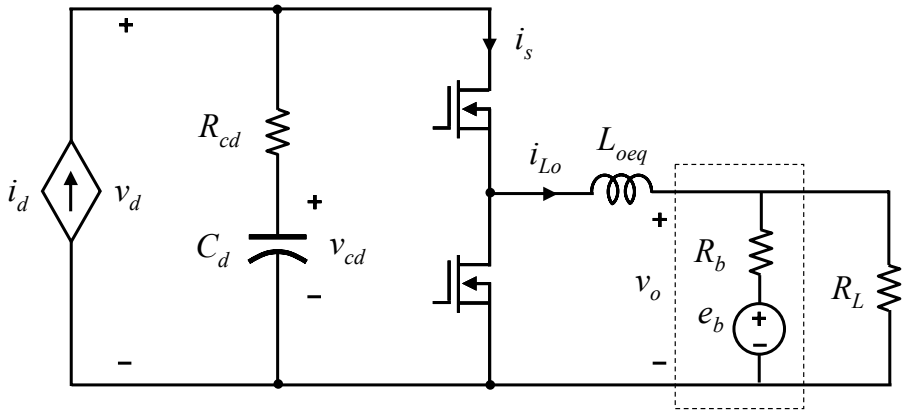


Figure 2.15 Hardware prototype unit of proposed three-phase interleaved stage converter.



(a)



(b)

Figure 2.16 Two subsets of converter of thermoelectric energy storage system: (a) first-stage converter with current sinking and (b) second-stage converter with current sourcing.

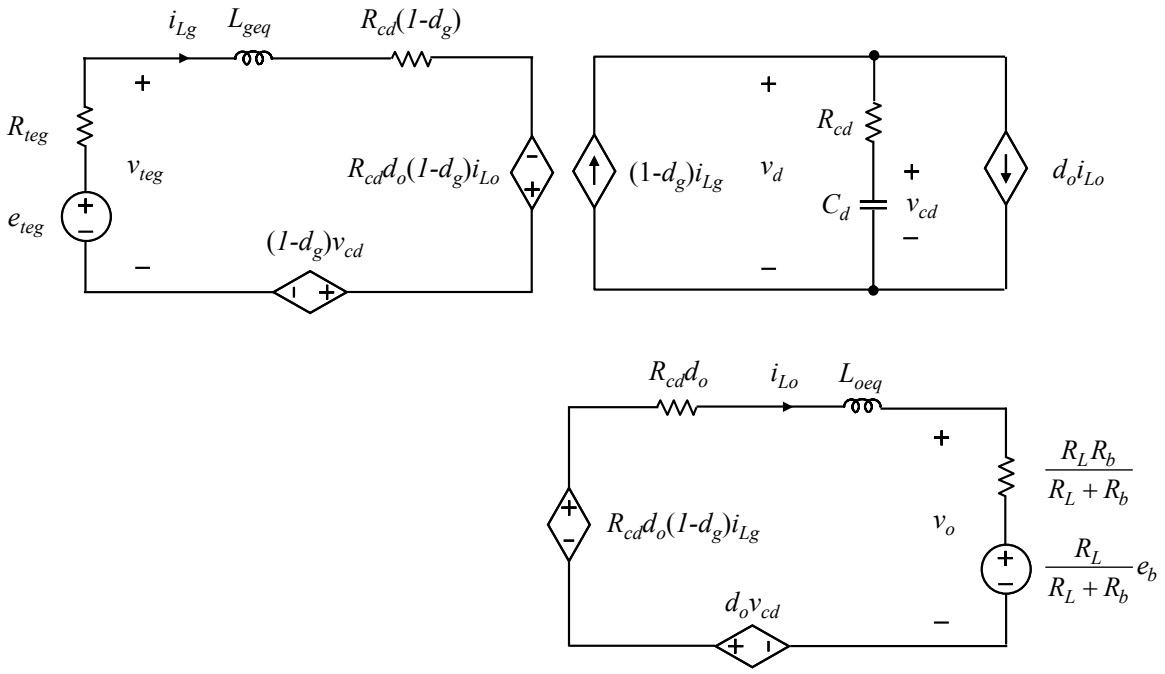


Figure 2.17 Large-signal equivalent circuit model of thermoelectric battery energy storage system.

$$
\begin{cases}
L_{geq}\dfrac{d\bar{i}_{Lg}}{dt}=e_{teg}-R_{teg}\bar{i}_{Lg}-\left[\bar{v}_{cd}+R_{cd}\left(\bar{i}_{Lg}-\bar{i}_{s}\right)\right]\left(1-d_{g}\right)\\
C_{d}\dfrac{d\bar{v}_{cd}}{dt}=\bar{i}_{Lg}\left(1-d_{g}\right)-\bar{i}_{s}\\
\bar{i}_{d}=\bar{i}_{Lg}\left(1-d_{g}\right)\\
\bar{v}_{g}=\bar{e}_{teg}-R_{teg}\bar{i}_{Lg}\\
\bar{v}_{d}=\bar{v}_{cd}+R_{cd}\left[\bar{i}_{Lg}\left(1-d_{g}\right)-\bar{i}_{s}\right]
\end{cases}
\tag{2.25}
$$

$$
\begin{cases}
L_{oeq}\dfrac{d\bar{i}_{Lo}}{dt}=\left[\bar{v}_{cd}+R_{cd}\left(\bar{i}_{d}-\bar{i}_{Lo}\right)\right]d_{o}-\dfrac{R_{L}}{R_{L}+R_{b}}\bar{e}_{b}-\dfrac{R_{L}R_{b}}{R_{L}+R_{b}}\bar{i}_{Lo}\\
C_{d}\dfrac{d\bar{v}_{cd}}{dt}=\bar{i}_{d}-\bar{i}_{Lo}d_{o}\\
\bar{i}_{s}=\bar{i}_{Lo}d_{o}\\
\bar{v}_{o}=\dfrac{R_{L}}{R_{L}+R_{b}}\bar{e}_{b}+\dfrac{R_{L}R_{b}}{R_{L}+R_{b}}\bar{i}_{Lo}\\
\bar{v}_{d}=\bar{v}_{cd}+R_{cd}\left(\bar{i}_{d}-\bar{i}_{Lo}d_{o}\right)
\end{cases}
\tag{2.26}
$$

$$\frac{d}{dt}\begin{bmatrix} i_{Lg} \\ i_{Lo} \\ v_{cd} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_{teg}+R_{cd}\left(1-d_g\right)}{L_{geq}} & \dfrac{R_{cd}d_o\left(1-d_g\right)}{L_{geq}} & -\dfrac{1-d_g}{L_{geq}} \\ \dfrac{R_{cd}d_o(1-d_g)}{L_{oeq}} & -\dfrac{1}{L_{oeq}}\left[\dfrac{R_L R_b}{R_L+R_b}+R_{cd}d_o\right] & \dfrac{d_o}{L_{oeq}} \\ \dfrac{1-d_g}{C_d} & -\dfrac{d_o}{C_d} & 0 \end{bmatrix}\begin{bmatrix} i_{Lg} \\ i_{Lo} \\ v_{cd} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_{geq}} & 0 \\ 0 & -\dfrac{R_L}{L_{oeq}\left(R_L+R_b\right)} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} e_{teg} \\ e_b \end{bmatrix} \tag{2.27}$$

$$\begin{bmatrix} v_g \\ v_d \\ v_o \end{bmatrix} = \begin{bmatrix} -R_{teg} & 0 & 0 \\ R_{cd}(1-d_g) & -R_{cd}d_o & 1 \\ 0 & \dfrac{R_L R_b}{R_L+R_b} & 0 \end{bmatrix}\begin{bmatrix} i_{Lg} \\ i_{Lo} \\ v_{cd} \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & \dfrac{R_L}{R_L+R_b} \end{bmatrix}\begin{bmatrix} e_{teg} \\ e_b \end{bmatrix} \tag{2.28}$$

The small-signal averaged equations can be derived as follows. Assuming the battery energy storage system operates in equilibrium point, the state variables (i_{Lg}, i_{Lo} and v_{cd}), input variables (e_t and e_b), output variables (v_g, v_d and v_o), and duty ratios (d_g and d_o) are expressed as quiescent variables and small ac variations, as shown in (2.29)–(2.32).

$$\begin{bmatrix} i_{Lg} \\ i_{Lo} \\ v_{cd} \end{bmatrix} = \begin{bmatrix} I_{Lg} \\ I_{Lo} \\ V_{cd} \end{bmatrix} + \begin{bmatrix} \hat{i}_{Lg} \\ \hat{i}_{Lo} \\ \hat{v}_{cd} \end{bmatrix} \tag{2.29}$$

$$\begin{bmatrix} e_{teg} \\ e_b \end{bmatrix} = \begin{bmatrix} E_{teg} \\ E_b \end{bmatrix} + \begin{bmatrix} \hat{e}_{teg} \\ \hat{e}_b \end{bmatrix} \tag{2.30}$$

$$\begin{bmatrix} v_g \\ v_d \\ v_o \end{bmatrix} = \begin{bmatrix} V_g \\ V_d \\ V_o \end{bmatrix} + \begin{bmatrix} \hat{v}_g \\ \hat{v}_d \\ \hat{v}_o \end{bmatrix} \tag{2.31}$$

$$\begin{bmatrix} d_g \\ d_o \end{bmatrix} = \begin{bmatrix} D_g \\ D_o \end{bmatrix} + \begin{bmatrix} \hat{d}_g \\ \hat{d}_o \end{bmatrix} \tag{2.32}$$

When the equations of (2.29)–(2.32) are substituted into (2.27) and (2.28), the linearized small-signal averaged equations are derived with the assumption that the nonlinear or second-order terms are negligible under sufficiently small variations. Figure 2.18 illustrates the resultant small-signal equivalent circuit model of the thermoelectric battery energy storage system, where $R_{eq} = R_L R_b / (R_L + R_b)$, $D_g^p = 1 - D_g$. Upper-case

letters denote the quiescent values, and the math accent "^" denotes the small ac variations from the quiescent values.

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{Lg}\\ \hat{i}_{Lo}\\ \hat{v}_{cd}\end{bmatrix} = \boldsymbol{A}\cdot\begin{bmatrix}\hat{i}_{Lg}\\ \hat{i}_{Lo}\\ \hat{v}_{cd}\end{bmatrix} + \boldsymbol{B}\cdot\begin{bmatrix}\hat{e}_{teg}\\ \hat{e}_{b}\end{bmatrix} + \boldsymbol{C}\cdot\begin{bmatrix}\hat{d}_{g}\\ \hat{d}_{o}\end{bmatrix} \tag{2.33}$$

$$\boldsymbol{A} = \begin{bmatrix} -\dfrac{R_{teg}+R_{cd}\left(1-D_g\right)}{L_{geq}} & \dfrac{R_{cd}D_o\left(1-D_g\right)}{L_{geq}} & -\dfrac{1-D_g}{L_{geq}} \\ \dfrac{R_{cd}D_o\left(1-D_g\right)}{L_{oeq}} & -\dfrac{1}{L_{oeq}}\left(\dfrac{R_L R_b}{R_L+R_b}+R_{cd}D_o\right) & \dfrac{D_o}{L_{oeq}} \\ \dfrac{1-D_g}{C_d} & -\dfrac{D_o}{C_d} & 0 \end{bmatrix}$$

$$\boldsymbol{B} = \begin{bmatrix} \dfrac{1}{L_{geq}} & 0 \\ 0 & -\dfrac{R_L}{L_{oeq}\left(R_L+R_b\right)} \\ 0 & 0 \end{bmatrix}$$

$$\boldsymbol{C} = \begin{bmatrix} \dfrac{V_{cd} + R_{cd}\left(I_{Lg} - I_{Lo}D_o\right)}{L_{geq}} & \dfrac{R_{cd}I_{Lo}\left(1-D_g\right)}{L_{geq}} \\ -\dfrac{R_{cd}I_{Lg}D_o}{L_{oeq}} & \dfrac{V_{cd} + R_{cd}\left[I_{Lg}\left(1-D_g\right) - I_{Lo}\right]}{L_{oeq}} \\ -\dfrac{I_{Lg}}{C_d} & -\dfrac{I_{Lo}}{C_d} \end{bmatrix}$$

$$\begin{bmatrix} \hat{v}_g \\ \hat{v}_d \\ \hat{v}_o \end{bmatrix} = \boldsymbol{D} \cdot \begin{bmatrix} \hat{i}_{Lg} \\ \hat{i}_{Lo} \\ \hat{v}_{cd} \end{bmatrix} + \boldsymbol{E} \cdot \begin{bmatrix} \hat{e}_{teg} \\ \hat{e}_b \end{bmatrix} + \boldsymbol{F} \cdot \begin{bmatrix} \hat{d}_g \\ \hat{d}_o \end{bmatrix} \tag{2.34}$$

$$\boldsymbol{D} = \begin{bmatrix} -R_{teg} & 0 & 0 \\ R_{cd}\left(1-D_g\right) & -R_{cd}D_o & 1 \\ 0 & \dfrac{R_L R_b}{R_L + R_b} & 0 \end{bmatrix}$$

$$\boldsymbol{E} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & \dfrac{R_L}{R_L + R_b} \end{bmatrix}$$

$$\boldsymbol{F} = \begin{bmatrix} 0 & 0 \\ -R_{cd}I_{Lg} & -R_{cd}I_{Lo} \\ 0 & 0 \end{bmatrix}$$

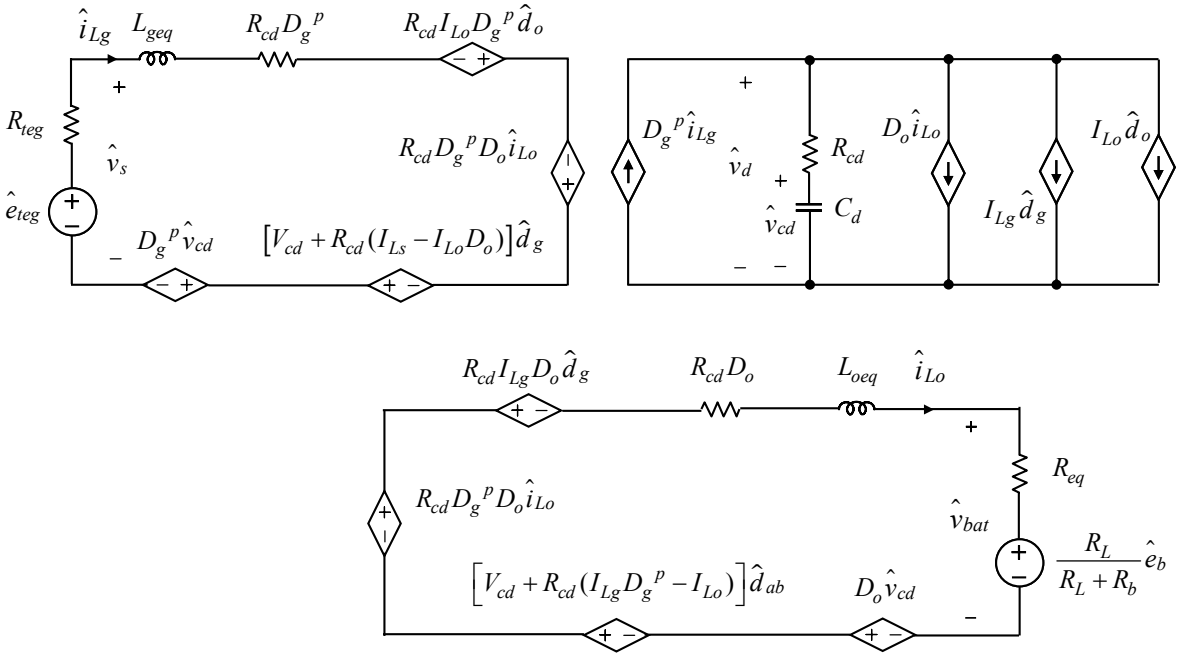


Figure 2.18 Small-signal equivalent circuit model of thermoelectric battery energy storage system.

The major transfer functions are obtained as expressed in (2.35)–(2.38), when G_{idg} and G_{vdg} are the duty-to-current and the duty-to-output transfer functions of the first-stage converter, and G_{ido} and G_{vdo} are the duty-to-current and the duty-to-link transfer functions of the second-stage converter, respectively. In the equations, the K terms represent gain, the z terms represent the zeros, and the p terms represent the poles. The transfer functions reveal third-order dynamics with one real pole and one pair of complex conjugate poles. Note that G_{vdo} in (2.38) has a negative dc gain.

$$G_{idg}(s) = \frac{\hat{i}_{Lg}}{\hat{d}_g} = K_{idg} \cdot \frac{\left(1 + s / z_{idg1}\right) \cdot \left(1 + s / z_{idg2}\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2^*\right)} \tag{2.35}$$

$$G_{vdg}(s) = \frac{\hat{v}_o}{\hat{d}_g} = K_{vdg} \cdot \frac{\left(1 + s / z_{vdg1}\right) \cdot \left(1 - s / z_{vdg2}\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2^*\right)} \tag{2.36}$$

$$G_{ido}(s) = \frac{\hat{i}_{Lo}}{\hat{d}_o} = K_{ido} \cdot \frac{\left(1 + s / z_{ido1}\right) \cdot \left(1 + s / z_{ido2}\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2^*\right)} \tag{2.37}$$

$$G_{vdo}(s) = \frac{\hat{v}_d}{\hat{d}_o} = -K_{vdo} \cdot \frac{\left(1 + s / z_{vdo1}\right) \cdot \left(1 + s / z_{vdo2}\right) \cdot \left(1 + s / z_{vdo3}\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2^*\right)} \tag{2.38}$$

2.6 Modeling verification and discussion

An introduction of the modeling tool has occurred thus far, and a computer simulations are used to verify the modeling approach. Saber Designer and Simplis™ simulation softwares are used to provide the time-domain and frequency domain responses. Simplis™ generates the small-signal gain/phase plots by a frequency sweep which imitates the real hardware frequency analyzer to calculate the small-signal response. Therefore, the precise frequency response can be obtained under a non-linear power switching circuit. The parameter values of the thermoelectric energy storage system used for this computer simulation are:

e_{teg} = 15V R_{teg} = 50mΩ

L_{geq} = 5uH C_d = 500uF R_{cd} = 10mΩ L_{oeq}=3.3uH

e_b= 12V R_b = 10mΩ R_L = 1Ω

2.6.1 Large-signal model verification

The time-domain simulation of the single-phase switching circuit model shown in Figure 2.15 is compared with the large-signal equivalent circuit model shown in Figure 2.17. Figure 2.19 shows the simulated converter waveforms of the first-stage inductor

current (i_{Lg}), second-stage inductor current (i_{Lo}), and dc link voltage (v_d) when the first stage duty cycle (d_g) increases from 0.6 to 0.9 after reaching the steady-state. The waveforms of the large-signal circuit model match the corresponding waveforms of the switching circuit model well.

Figure 2.20 shows the simulation waveforms when the second stage duty cycle d_o increases from 0.6 to 0.9, while the d_g remains at the constant value of 0.6. The waveforms of the averaged model also agree with its counterpart in the switching model. These time domain simulation results support the effectiveness of the large-signal averaged equations and equivalent circuit model derived by the aggregated modeling approach.

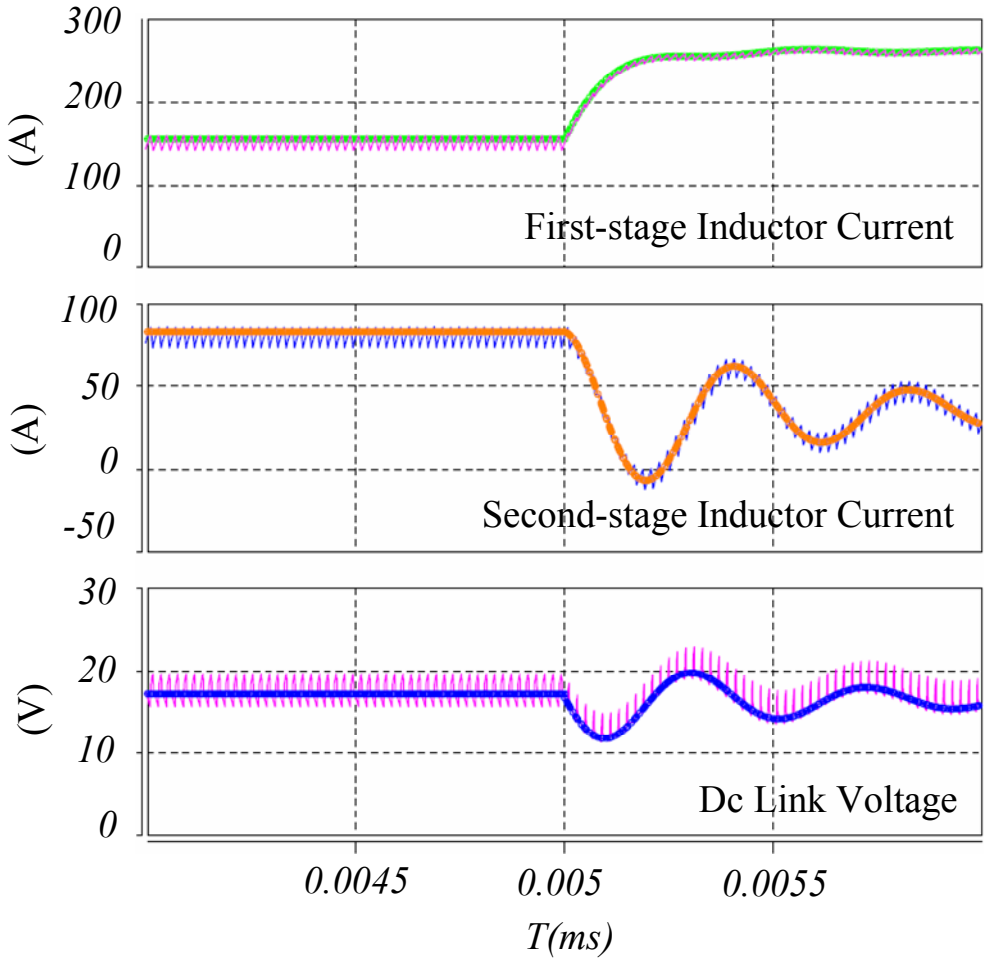


Figure 2.19 Simulation waveform of switching model and averaged model under increased first-stage duty cycle (from 0.6 to 0.9).

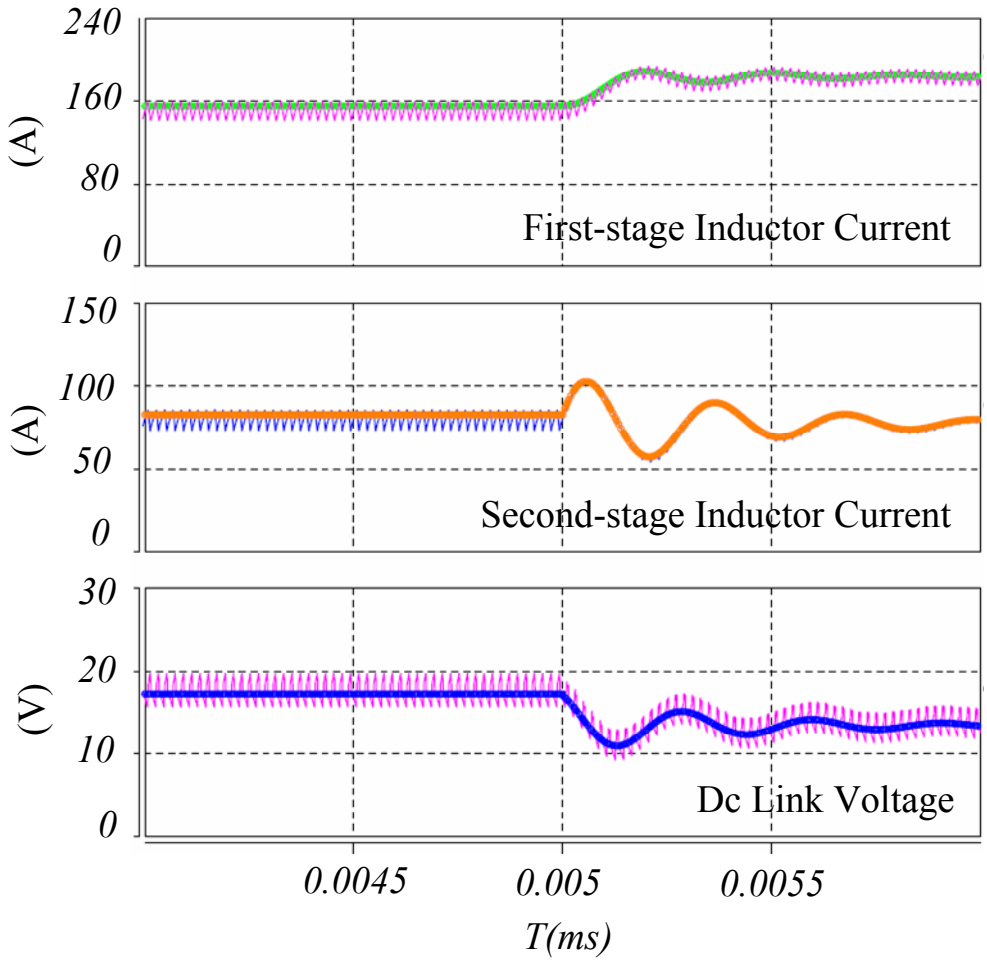
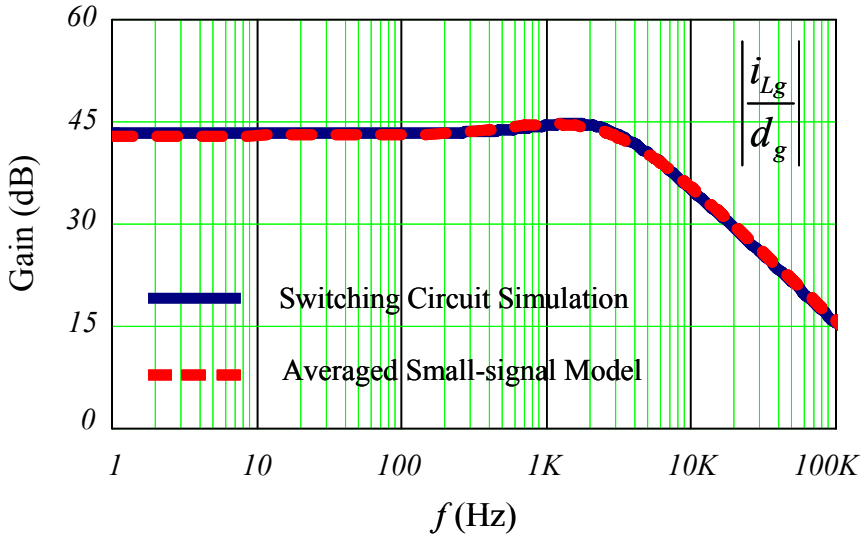


Figure 2.20 Simulation waveform of switching model and averaged model under increased second-stage duty cycle (from 0.6 to 0.9).

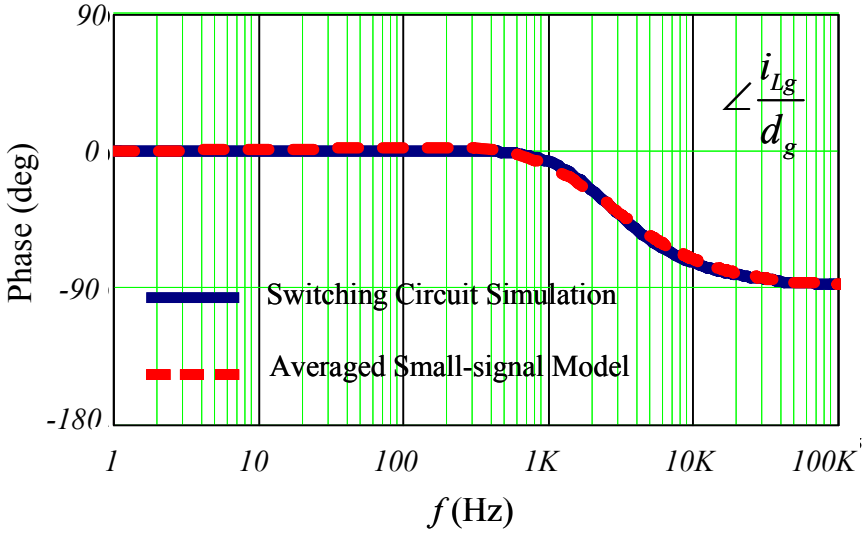
2.6.2 Small-signal model verification

The Simplis^{TM} simulation software runs the ac analysis mode using once again the single-phase switching circuit model shown in Figure 2.15. The resultant frequency responses are imported into MathCAD in order to compare with duty-to-current transfer functions of the first-stage and second-stage converter. In the simulation, a 200 kHz switching frequency is used.

Figure 2.21 shows the gain/phase plots of the duty-to-current transfer function (G_{idg}) of (2.35), where the solid line represents the ac analysis result by the Simplis^{TM} simulation and the dashed line is the transfer function provided from by aggregated small-signal modeling. It is clear that the modeling predictions match the simulation result well. Figure 2.22 also shows that the small-signal models are valid for the second-stage converter's duty-to-current transfer function (G_{ido}) of (2.37). In these figures, it can be seen that the converter dynamics are correctly predicted at the low frequency and the high frequency region up to the Nyquist frequency or one-half of the switching frequency. These comparison results support that the small-signal models provided by the aggregated modeling approach can predict the system dynamics accurately.

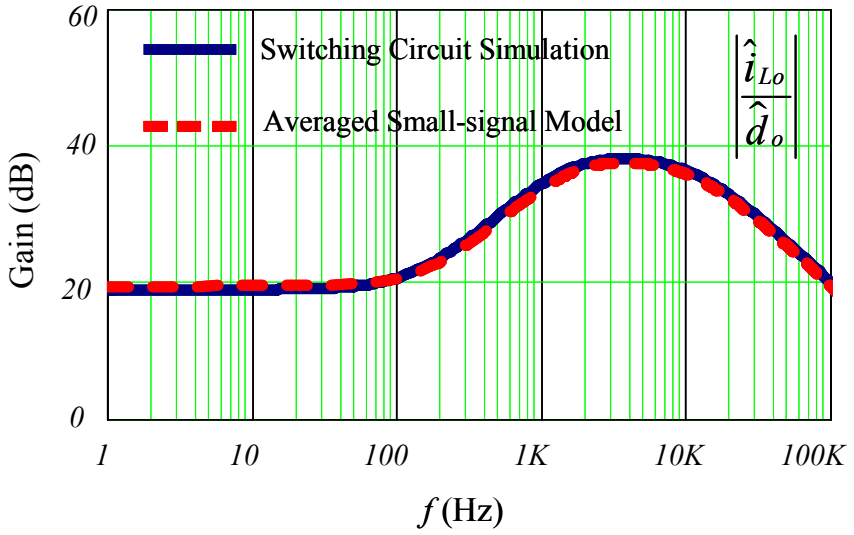


(a)

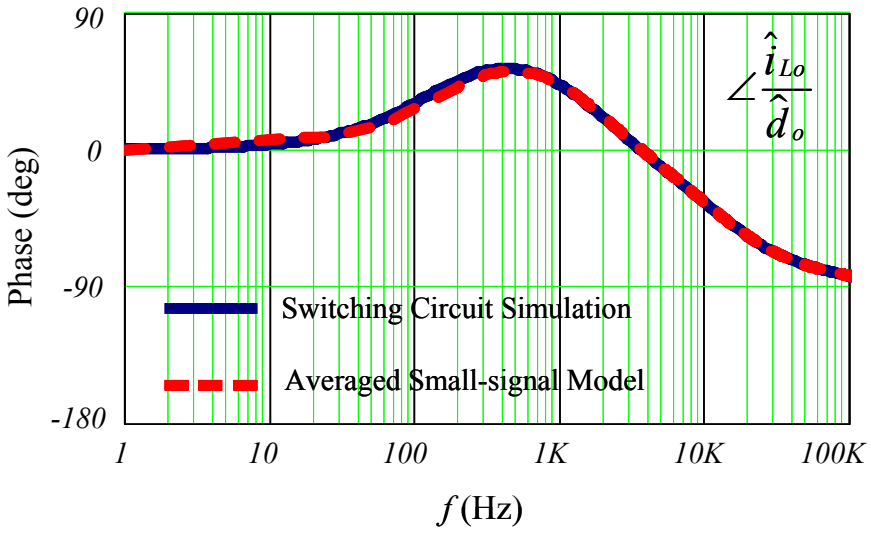


(b)

Figure 2.21 Gain/phase plot of duty-to-current transfer function in first-stage converter G_{idg} under d_g=0.5 and d_o=0.72: (a) Gain plot, (b) Phase plot.



(a)



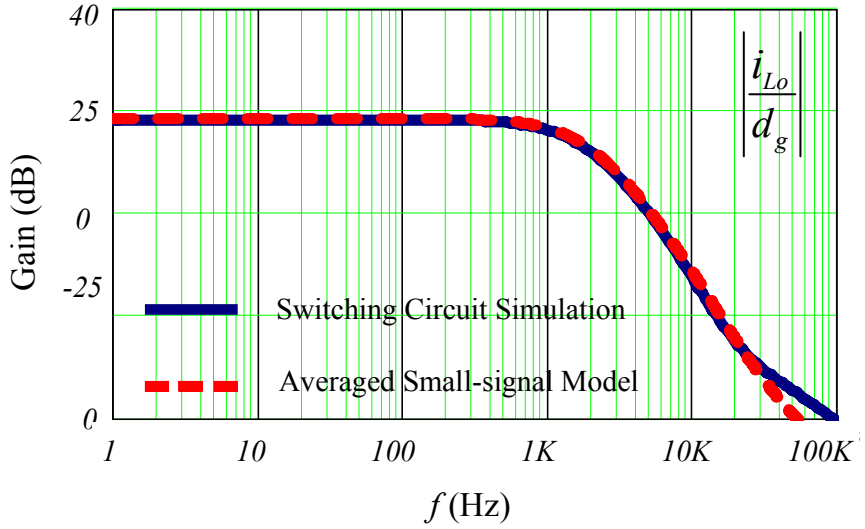
(b)

Figure 2.22 Gain/phase plot of duty-to-current transfer function in second-stage converter G_{ido} under d_g=0.5 and d_o=0.72: (a) Gain plot, (b) Phase plot.

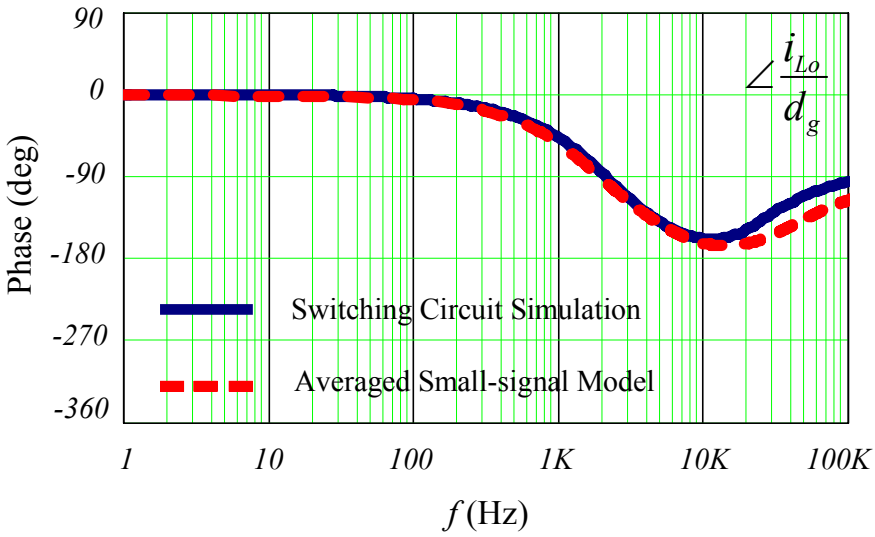
2.6.3 Stage-converter interaction verification

Figures 2.23 and 2.24 illustrate the predicted and simulated dynamics between the stage converters. Figure 2.23 demonstrates the dynamics of the second-stage current impacted by the first-stage duty cycle, while Figure 2.24 shows the impact of the second-stage duty cycle on the first-stage current. It is seen that the low-frequency dynamics are predicted well, but the high frequency dynamics are not. This is the high frequency limitation of the aggregated modeling approach. The controlled current source, which is introduced to represent dynamics between the stage-converters, requires averaging over one switching period, as shown in (2.22) or (2.23). When the frequency moves close to the switching frequency, the averaging is deteriorated, and the error increases accordingly.

From the control design point of view, inaccuracy at the high frequency range (close to the switching frequency) is acceptable, because the crucial frequency range is much lower than the switching frequency (usually, 5~10 times lower). Therefore, these modeling results are still effective to predict dynamics between the stage converters. To summarize, the modeling approach provides a fairly comprehensive and automatic way to perform the small-signal analysis. The procedure is straightforward and all of the dynamics and steady-state information of the converter can be provided. In addition, the methodology is generally applicable to multiple-stage converters. All of these features make the aggregated modeling approach a valuable tool for practical analysis and design.

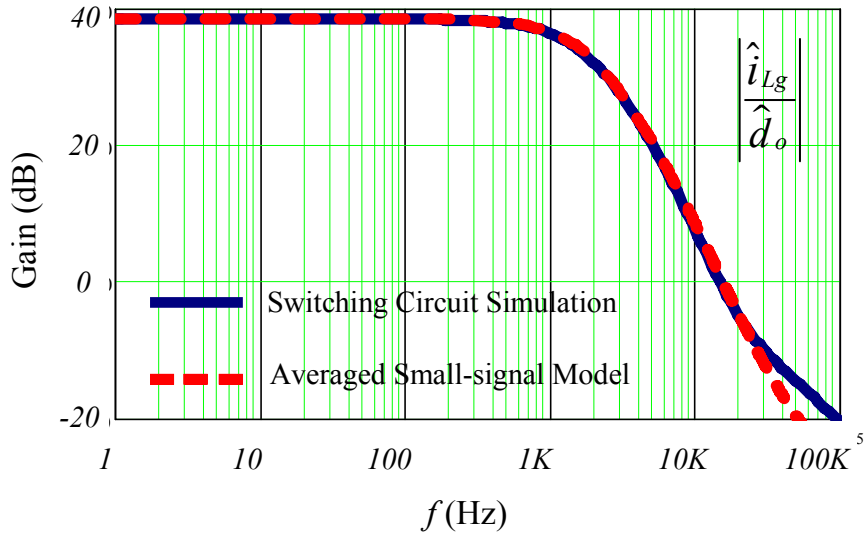


(a)

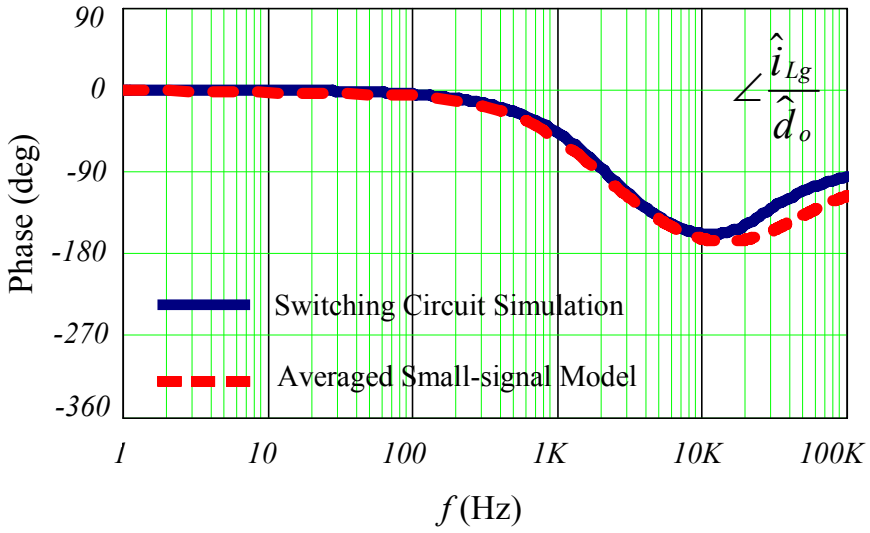


(b)

Figure 2.23 Gain/phase plot of system interaction impacted by first-stage duty cycle: (a) Gain plot, (b) Phase plot.



(a)



(b)

Figure 2.24 Gain/phase plot of system interaction impacted by second-stage duty cycle: (a) Gain plot, (b) Phase plot.

2.7 Summary

In this chapter, thermoelectric generator features and characteristics were discussed, along with the requirement of a step-up/-down power convertor. The three-phase interleaved synchronous boost-buck converter was proposed and designed for the thermoelectric battery energy storage system. The predicted and experimental efficiency was 95%. The aggregated modeling approach was proposed as a general modeling tool for multiple-stage converters based on the modification of the conventional approach. The approach reduces modeling work while giving more intuitive and clear insight for the dynamics. The thermoelectric battery energy storage system is demonstrated for systematic implementation for the aggregated modeling approach. As a result, the large-signal and small-signal models were derived along with the major transfer functions. Simulations were performed to check the modeling validation for the large-signal model, the small-signal model, and the transfer functions. The modeling results agree with the simulation results very well: and thus, they validate the aggregated modeling approach.

Chapter 3

Proposal of Generalized Control Structure, Compensator Design and Performance Evaluations

3.1 Introduction

In this chapter, we will perform analysis and design of the controller for a thermoelectric battery stage system. As mentioned in Chapter 1, the thermoelectric battery stage system operates in two distinctive modes. Achievement of the two-mode operation occurs mainly through the stop-and-go concept. The issues caused by this concept will be addressed with an experimental result. After which, a novel control structure will be proposed. Based on the novel control structure, a single, unified control scheme will be presented which is capable to achieve two distinctive modes by the unified control scheme. The implementation of the unified controller will be detailed with compensator designs based on frequency domain information. The experimental results support the superiorities of the unified control concept established by the novel control structure.

3.2 Generalized control structure and unified control scheme

3.2.1 Issues of stop-and-go concept

In two-stage power converters, the dc link voltage is normally controlled by the first-stage converter. The second-stage power converter controls the output. This is the basic operation of the conventional control structure for two-stage power converters (illustrated in Figure 3.1). The stop-and-go concept is easily adapted to the conventional control structure without any break-down.

Figure 3.2 shows one possible implementation with basis of the conventional control structure. In this control structure, the maximum power point tacking control takes care of maximizing the power harvest, while power matching control prevents the battery overcharge. As shown in Figure 3.2, the first-stage converter contains two controller, the maximum power point tracking controller (denoted as *MPPT*) and dc link voltage controller (denoted as *DCC*). The two controllers of the first-stage converter are alternatively selected by the hysteresis comparator. The dc link voltage is used to make a stop-and-go decision. In nominal condition, the maximum power point tracking control is performed. When the dc link voltage exceeds the prefixed voltage (denoted as v_d^+), the dc link voltage control is activated to stabilize it. The operation returns to the maximum power point tracking control when the dc link voltage becomes lower than the other prefixed voltage (denoted as v_d^-), and this operation keeps to be iterated. The second-stage converter is dedicated to regulate the battery voltage.

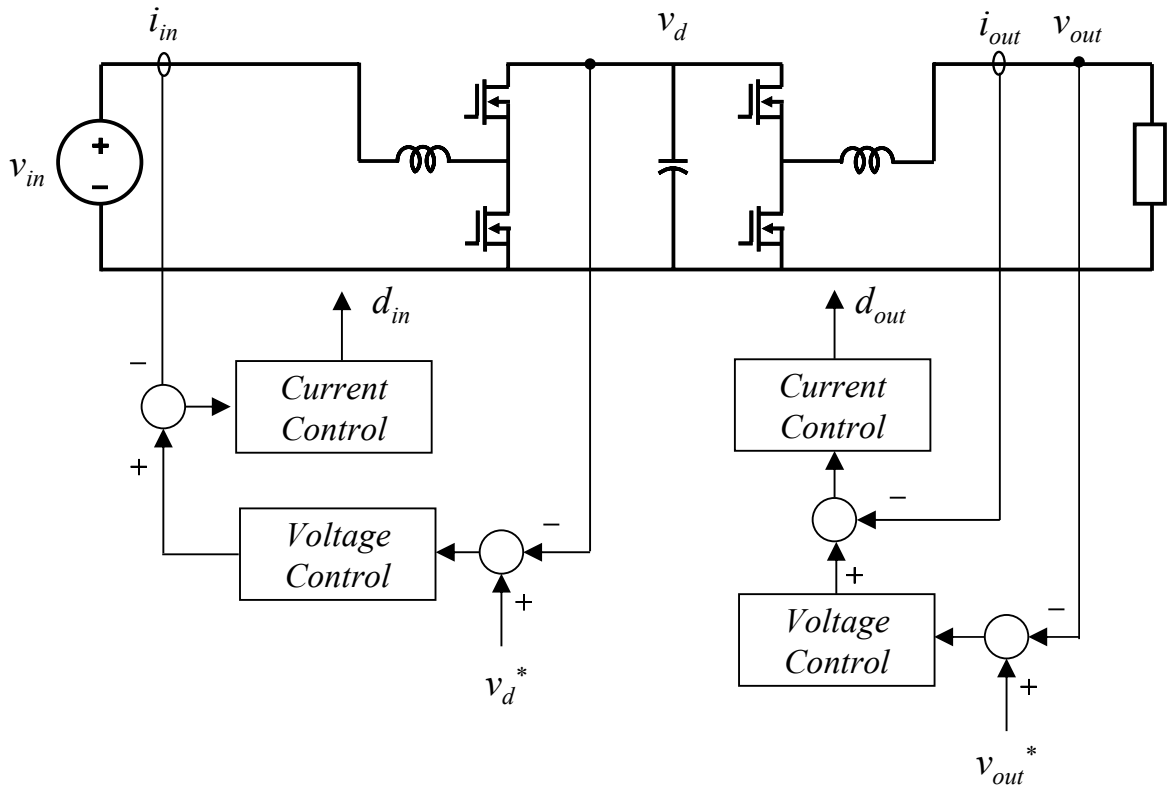


Figure 3.1 Conventional control structure for two-stage converter.

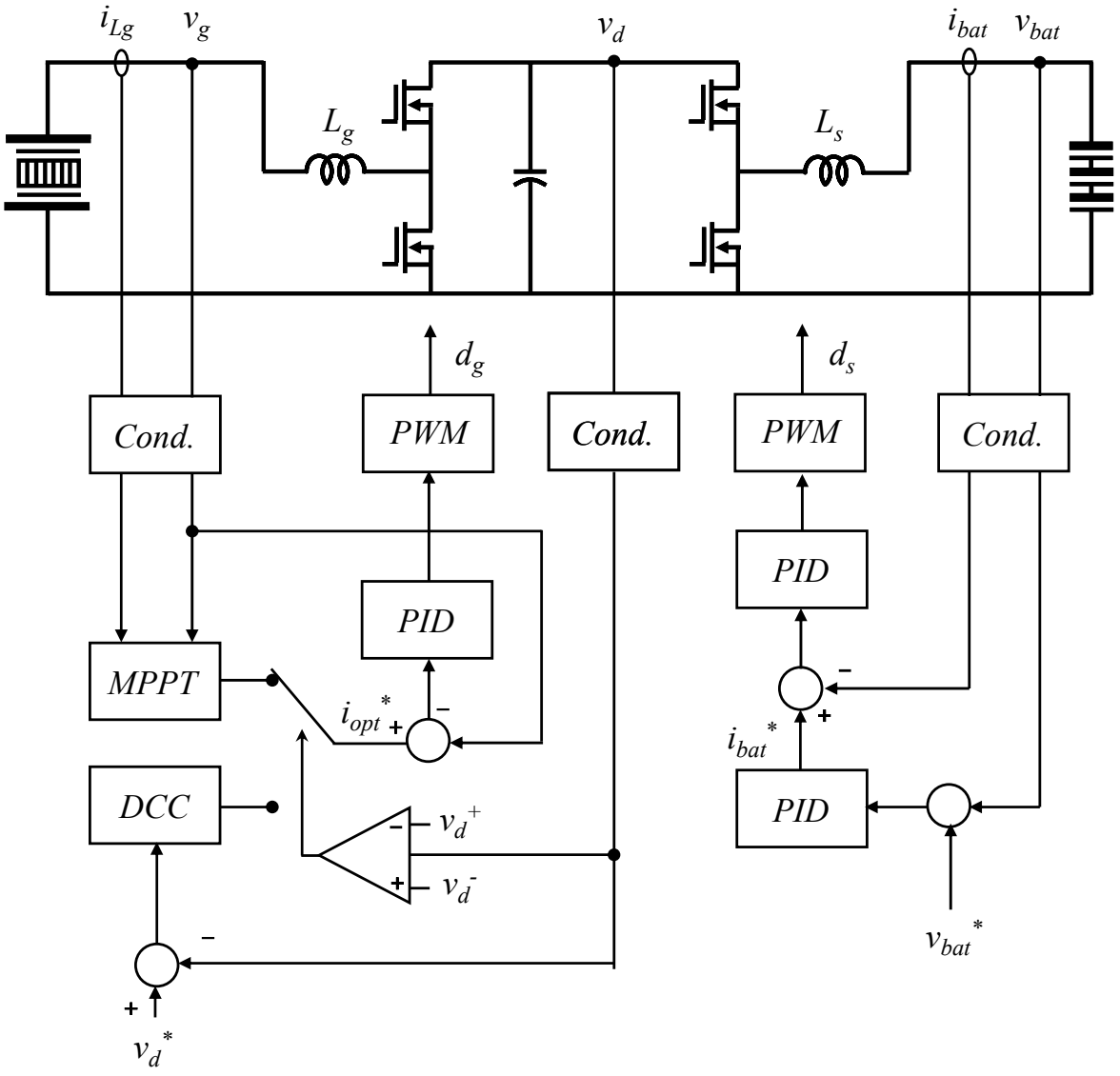


Figure 3.2 Control structure using stop-and-go concept of two-stage dc-dc converter for battery energy storage system.

Figure 3.3 shows the experimental waveforms of the stop-and-go implementation explained above. As expected, the second-stage converter regulates the battery voltage consistently without any overcharging. However, the dc link voltage suffers from the low frequency oscillation in the prefixed voltage range of the hysteresis comparator. Apparently, the low frequency oscillation originates from the repeated mode transient of the stop-and-go concept. Input power increases when the maximum power point tracking controller is activated, and then, the dc link voltage starts to go up. The dc link voltage keeps going up, because the demanded output power is almost constant and eventually hits the upper hysteresis limitation. Activation of the dc link voltage controller then decreases the input power. Consequently, input power oscillates at a low frequency, and thus, the thermoelectric generator experiences low frequency current ripple as shown in Figure 3.3. The low frequency current ripple causes almost 20% higher current handling capability and limits thermoelectric generator's deliverable power capability. Operating the thermoelectric generator under the de-rated power condition is highly undesirable due to underutilization of the source. The power converter also requires higher current handling capability to deal with current ripple and conversion efficiency is dropped due to increasing conduction losses. As a result, the performance and reliability of thermoelectric battery energy storage is dramatically degraded.

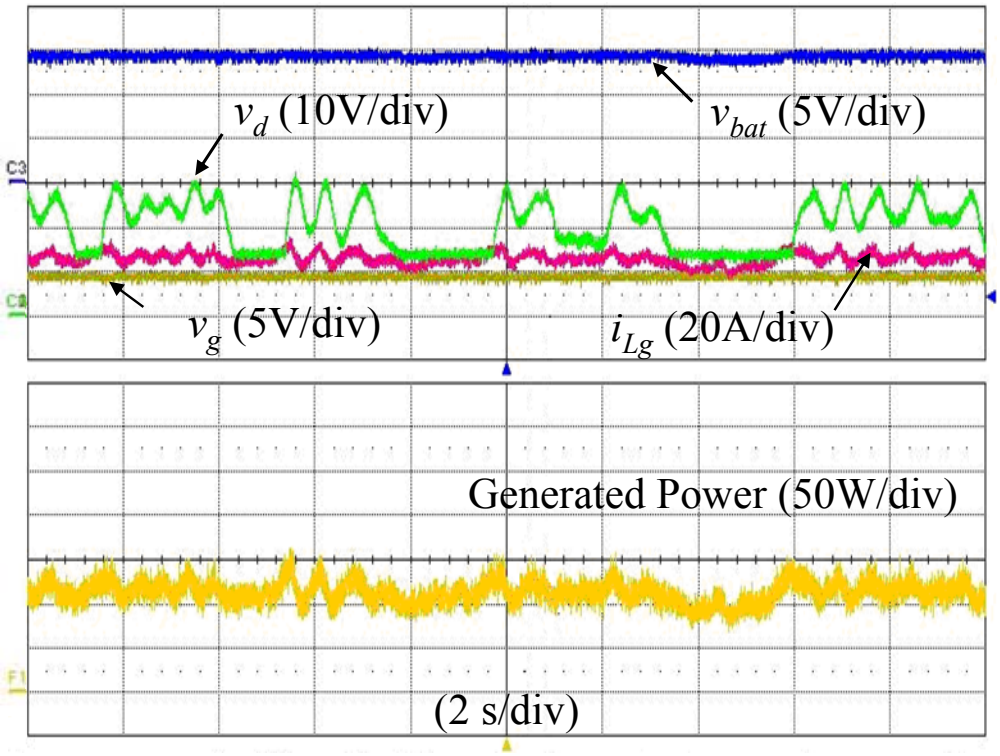


Figure 3.3 Experimental waveform under stop-and-go concept in two-stage dc-dc power converter.

3.2.2 Proposal of generalized control structure

The input power and battery voltage are the major control variables in the battery energy storage system. These variables, in the conventional control structure, are managed independently by the stage converters without any collaboration. The lack of the mutual cooperation of the isolated control structure causes the collision at the dc link capacitor. As a result, the dc-link voltage oscillates, and thus the input power pulsates accordingly. It is more reasonable to manage the major control variables by reconfiguring control structure, in order to eliminate this issue.

The other critical issue of the conventional control structure is intermittent dc link voltage regulation. In the conventional control structure, the first-stage converter takes care of regulating the dc link voltage. In addition, the maximum power point tracking is also achieved by the first-stage converter. These overlapped control tasks degrade the dc link voltage regulation. While the converter operates in maximum power point tracking mode, the dc link voltage control is disabled. Then, the dc-link voltage is left to be uncontrollable. Sometimes this undesirable operation results in a high voltage spike at the dc link capacitor which requires the immediate shut-down, in order to protect the power converter. Alternative solution is made through reconfiguring control structure. The second-stage power converter undertakes the dc link voltage regulation.

Based on these ideas, the novel control structure, named generalized control structure, is established as shown in Figure 3.4. Different from the conventional control structure shown in Figure 3.1, the input power (or input voltage and current) and the battery voltage are fed to the first-stage converter. As a consequence, two major control variables can be easily managed by the single stage-converter. This feature of the generalized

control structure provides more appropriate control platform for the unified control scheme. Moreover, in this control structure, the dc link voltage can be continuously regulated by the second-stage converter without any interruption associated with the operation modes.

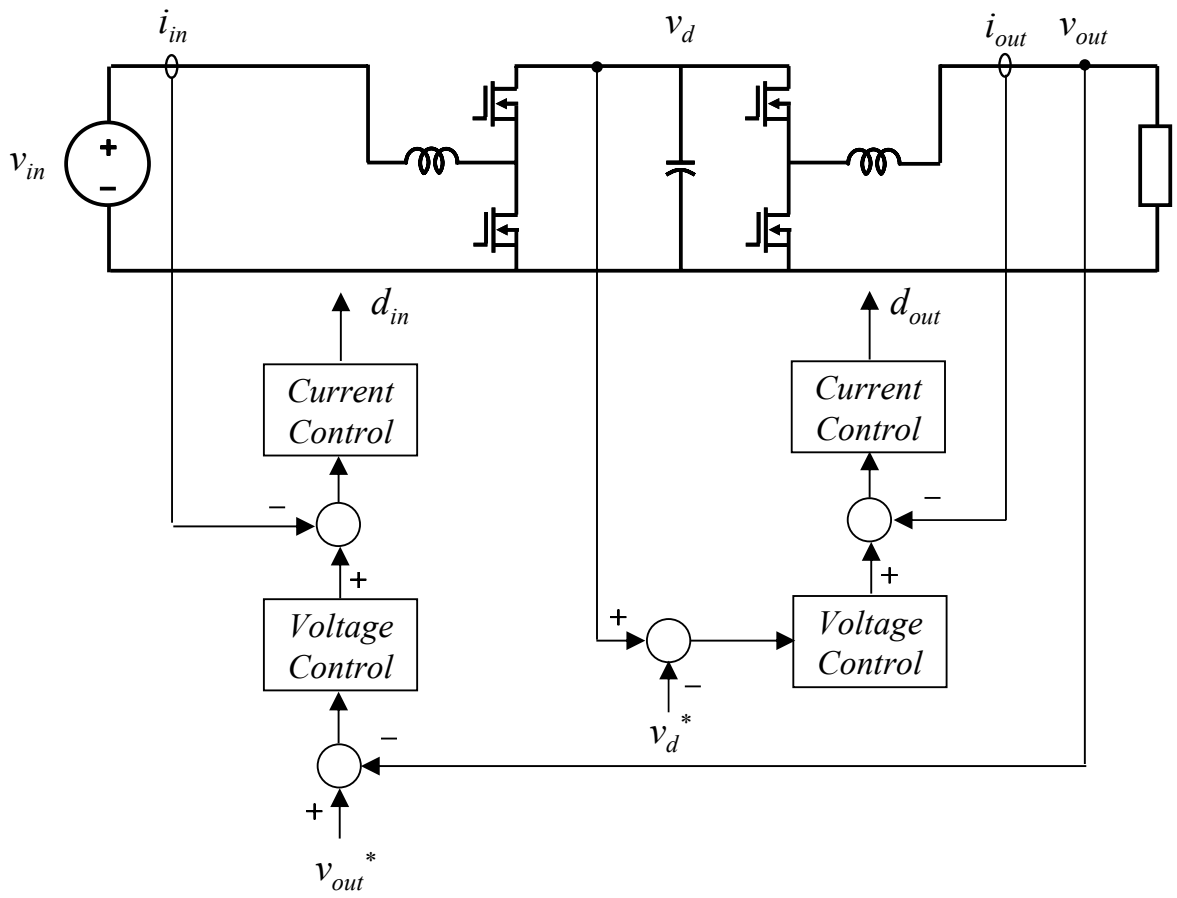


Figure 3.4 Generalized control structure for two-stage converter.

Now we can conclude the basic formulation of the generalized control structure:

1) The generalized control structure is composed by two control loops which have the different designated feedback signals. The first-stage converter loop feeds back the input voltage, input current, and output voltage signals, while the second-stage converter loop feeds back the dc link voltage and output current signals;
2) Based on the feedback signals explained above, the first-stage converter usually regulates the input power (sometimes current or voltage) or output voltage. The second-stage usually controls the dc link voltage or output current.
3) For a battery energy storage system, unified control scheme could be easily implemented by dealing with the input power and battery voltage in the first-stage converter side.
4) In the generalized control structure, the dc link voltage is regulated by the second-stage converter. This feature provides the continuous dc link voltage regulation for a battery energy storage system, regardless of the operation modes.

Figure 3.5 shows the practical implementation of the generalized control structure for the thermoelectric battery storage system. In the figure, the first-stage converter loop, denoted as the dotted lines, is responsible for the maximum power point tracking control or power matching control. The unified control scheme (C_{vg}), which will be detailed in the next section, continuously loops back the input voltage (v_g), the input current (i_{Lg}) and the battery voltage (v_{bat}). Based on these inputs, the unified control scheme determines the operation mode and outputs the optimal command of the input current (i_{opt}^*). After comparing the optimal input current command (i_{opt}^*) with the actual input current (i_{Lg}), the error is fed into the current compensator (C_{ig}) to generate the control voltage (v_{cg}). The v_{cg}

is converted to the duty cycle (d_g) for the first-stage converter by the PWM circuit.

The second-stage converter loop, denoted as the solid lines, is responsible for regulating the dc-link voltage (v_d). The current compensator (C_{io}) regulates the output current (i_{Lo}) to match the output current command (i_{Lo}^*), and the voltage compensator (C_{vo}) regulates the actual dc link voltage (v_d) according to the given voltage command (v_d^*).

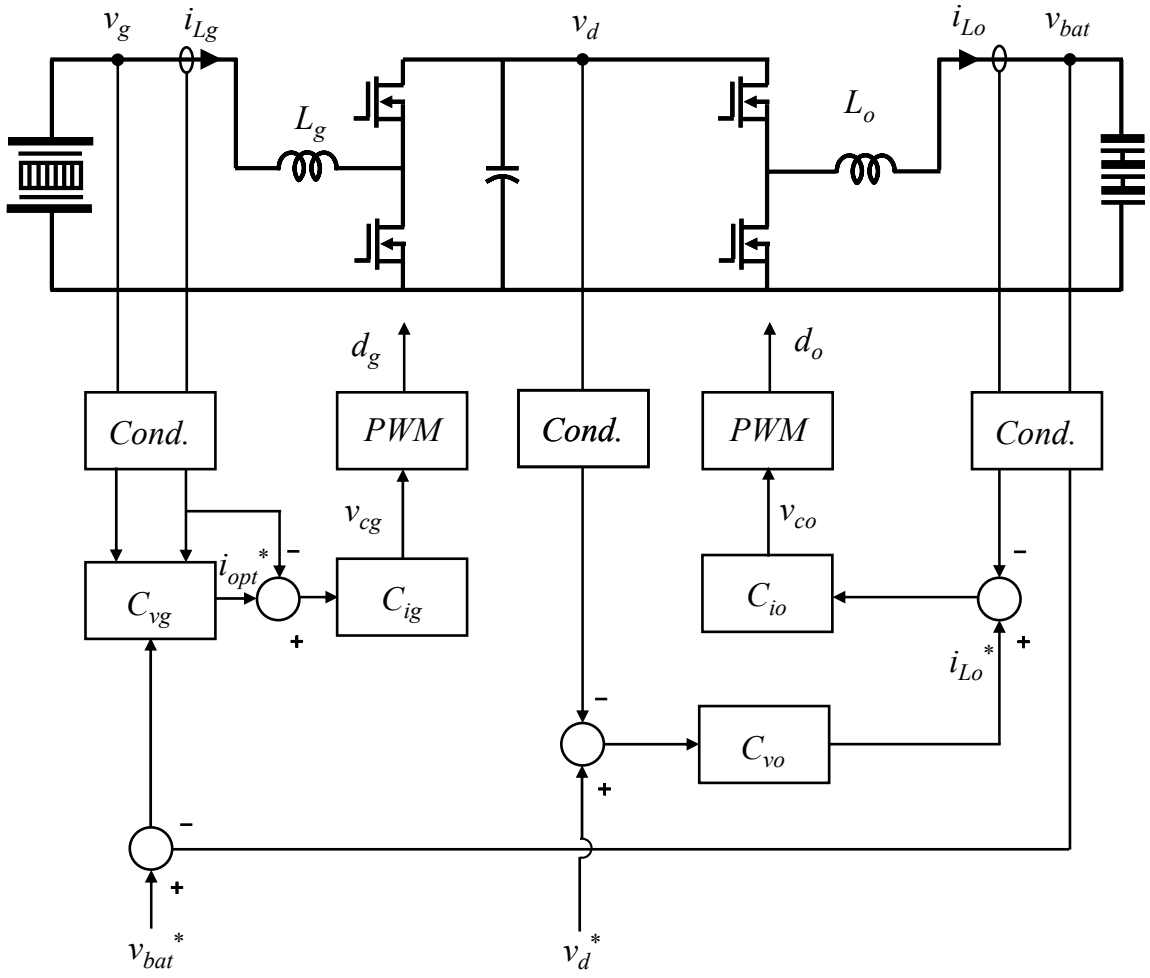


Figure 3.5 Control implementation based on generalized control structure of two-stage dc-dc converter for battery energy storage system.

3.2.3 Unified control scheme and modeling

The objective of the unified control scheme is to perform the maximum power point tracking control or the power matching control, depending on a battery state-of-charge. Before incorporating these controls into a single control scheme, we need to review the fundamentals of a maximum power point tracking scheme. As discussed in Chapter 1, the governing rule of most maximum-power-point-tacking schemes is to move operating current (sometimes voltage) of a renewable energy source toward the maximum power point. When the operating point doesn't reach the maximum power point yet, the working current needs to be further increased. For this case, the derivative of power-current characteristics has a positive value. On the other hand, passing the maximum power point requires the working current reduced. The derivative of power-current characteristics has a negative value for this case. According to the correlations, we easily determine the desirable current movement by getting the derivative of power-current characteristics.

Now, we consider another desirable current movement when the battery is already fully charged, and thus, the battery voltage exceeds the nominal working voltage. For this case, operating current should be moved toward the direction to reduce the input power. Consequently, the desirable current movement becomes opposite to the derivative of power-current characteristics. This operation reduces the input power, and therefore, the battery voltage decreases accordingly. When it becomes equal to the nominal working voltage, the operating current is preserved to balance the power between the input and output side.

To summarize, the operating rules of the unified control scheme are as follows:

1) When the battery voltage is lower than its nominal voltage, the maximum power point

tracking control is activated to harvest as much electrical energy as possible from the thermoelectric generator. In this case, the operating current movement has the same direction as the derivative of power-current characteristics.

2) When the battery voltage is higher than the nominal voltage, the power matching control is triggered to reduce the power production. The operating current movement becomes the opposite to the derivative of power-current characteristics.

3) When the battery voltage equals the nominal, the operating current settles down and remains unchanged.

Based on the operating rules summarized above, the governing equation of the unified control scheme is written as (3.1), where a simple integral compensator with the defined error (e_{vo}) and the constant gain (K_p) are used. Shown in (3.2), the e_{vo} is defined as the scalar product of the derivative sign of power-current characteristics (denoted as sgn[ ]), and the error between the prefixed nominal working voltage of a battery v^*_{bat} and its terminal voltage (v_{bat}). The $v_{bat}{}^*$ is usually given by the battery manufacturers. The K_p affects a tracking speed and stability, and thus needs to be designed carefully.

$$i_{opt}{}^*(t) = K_p \cdot \int e_{vo}(t) \tag{3.1}$$

$$e_{vo}(t) = \mathrm{sgn}\left(\frac{d\left[v_g(t) \cdot i_{Lg}(t) \right]}{di_{Lg}(t)} \right) \cdot \left(v_{bat}{}^*(t) - v_{bat}(t) \right) \tag{3.2}$$

Applying the forward Euler method, the discrete-time expression of the unified

control scheme is represented as (3.3)-(3.5), where [n+1], [n], and [n-1] represent the quantized values at the (n+1)th, n^{th}, and (n-1)th sampling interval, respectively.

$$i_{opt}{}^{*}[n+1] = i_{opt}{}^{*}[n] + K_p \cdot e_{vo}[n] \tag{3.3}$$

$$e_{vo}[n] = \mathrm{sgn}\left(\frac{\Delta P_g[n]}{\Delta i_{Lg}[n]}\right) \cdot \left(v_{bat}{}^{*}[n] - v_{bat}[n]\right) \tag{3.4}$$

$$\frac{\Delta P_g[n]}{\Delta i_{Lg}[n]} = \frac{v_g[n] \cdot i_{Lg}[n] - v_g[n-1] \cdot i_{Lg}[n-1]}{i_{Lg}[n] - i_{Lg}[n-1]} \tag{3.5}$$

Figure 3.6 illustrates the block diagram of the unified control scheme in z-domain with the sampler and zero-order-hold (ZOH).

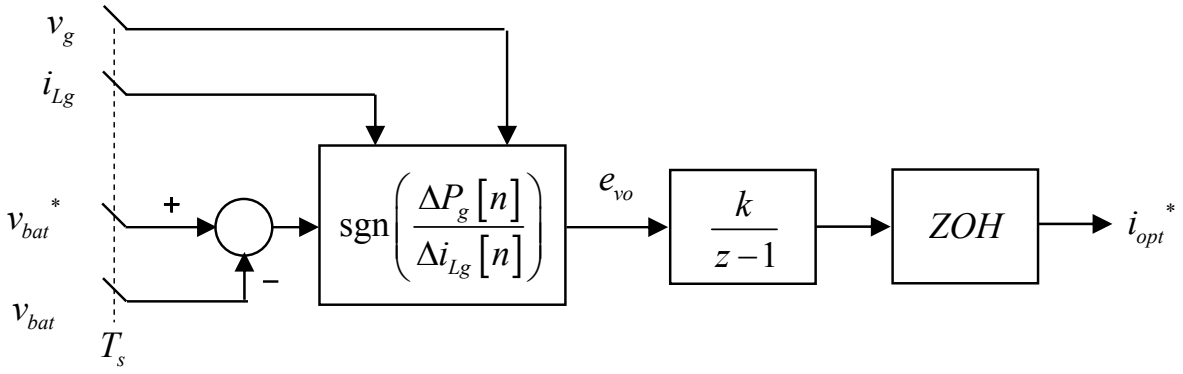


Figure 3.6 Block diagram of unified control scheme.

Some practical considerations need to be taken into account, in order to improve the performance of the unified control scheme. According to (3.3), the step size of maximum-power-point tracking control is adjusted by the defined error $e_{vo.}$ When we have too large e_{vo}, the operation of the unified control scheme could cause oscillation due to excessively big step size. To avoid the oscillation, the e_{vo} should be limited within proper ranges. The other consideration is needed when the power matching control is activated. According to the operating rule, the current needs to be increased when the operating point has passed the maximum power point. However, in practice, this operation is not desirable, because a power converter may experience large conduction losses. Therefore, some modifications are needed to prevent this situation, so that the power matching control always operates in the right side of the maximum power point.

The error-to-current transfer function (C_{vg}) is derived as follows. In Figure 3.8, the relation between the e_{vo} and i_{opt}^{*} is represented in the z-domain, as shown in the following equation.

$$i^{*}_{opt}(z) = K_p \cdot \frac{1}{1-z} e_{vo}(z) \tag{3.6}$$

The continuous-time expression of G_{vg} is given by substituting $z = e^{s \cdot Ts}$ into (3.6) and then multiplying by $(1\text{-}e^{-sTs})/(s \cdot T_s)$ [102] in order to represent the ZOH effect as (3.7) where T_s presents the sampling interval. Note that the C_{vg} has the inherent pole at the origin, and thus the zero steady-state error is achieved without an additional compensator.

$$C_{vg}(s) = \frac{\hat{i}_{opt}^{*}}{\hat{e}_{vo}} = \frac{K_p}{T_s} \cdot \frac{1}{s \cdot e^{s \cdot Ts}} \tag{3.7}$$

3.3 Compensator design for thermoelectric battery energy storage system

The design of the control of thermoelectric battery energy storage system is based on the major transfer function derived in Chapter 2. A proportional-integral-derivative (PID) compensator has been prevailed in the industry. It will be employed here to control the thermoelectric battery energy storage system. The most popular PID compensator types are the two-pole and one-zero compensator (often referred as type 2) and the three-pole and two-zero compensator (type 3).

The type 2 compensator is easy to implement and provides no steady-state error with the pole at the origin. The other pole and zero are used to improve system dynamics while retaining stability, by reshaping system loop gain curve. The type 3 compensator provides better performance when the type 2 compensator can not meet the system control requirement. The additional pole and zero enables to further reshape system loop gain curve.

A typical design procedure using the PID compensator is given as,

1) Draw gain/phase plot of the loop gain which contains the PID compensator.
2) Place the first pole at the origin to achieve no steady-state error
3) Place the second pole around the lowest zero of the plant; usually caused from the

equivalent series resistance (ESR) of a capacitor in a power stage.

4) Place the third pole (if applicable) at the high frequency range to get maximum attenuation.
5) Place the first zero around the resonant pole of the plant to damp the overshoot.
6) Place the second zero (if applicable) below the resonant pole of the plant to compensate conditional instability caused from parameter uncertainty or variation.
7) Set the loop gain crossover frequency below the Nyquist frequency or one-half of the switching frequency; typically one decade less than the switching frequency.
8) Determine a dc gain with a sufficient phase margin.

The circuit parameter values of the thermoelectric energy storage used for the control design are shown below where two cases of R_L are used for light-load (80W) and heavy-load (400W) condition. The switching frequency f_{sw} (or $1/T_{sw}$) is 50 kHz, and sampling frequency f_s (or $1/T_s$) is 10 kHz.

e_{teg} = 15V R_{teg} = 100mΩ

L_{geq} = 5uH C_d = 500uF R_{cd} = 10mΩ L_{oeq}=3.3uH

e_b = 12V R_b = 10mΩ R_L = 2.5Ω or 0.5Ω

v_d = 20V v_{bat} = 14.4V

3.3.1 First-stage control loop design

From the generalized control structure shown in Figure 3.5, the closed-loop compensator diagram of the first-stage control loop can be obtained. It is represented in Figure 3.7 by using transfer function blocks: G_{ig} — duty-to-current transfer function, G_{voig} — current-to-output transfer function, C_{ig} — inner current loop compensator, C_{vg} —unified control scheme transfer function, H_{vg} — voltage conditioning circuit transfer function, H_{ig} — current conditioning circuit transfer function, and F_{mg} — PWM gain. The current-to-output transfer function (G_{voig}) can be derived by using duty-to-current transfer function (G_{ig}) of (2.33) and duty-to-output transfer function (G_{vg}) of (2.34).

$$G_{voig}(s) = \frac{\hat{i}_{Lg}}{\hat{v}_{bat}} = \frac{\hat{i}_{Lg}}{\hat{d}_g} \cdot \frac{\hat{d}_g}{\hat{v}_{bat}} = G_{ig}(s) \cdot \frac{1}{G_{vg}(s)} \tag{3.8}$$

From Figure 3.7, the loop gain of inner current loop (T_{ig}) given as (3.9). The type 3, three-pole and two-zero compensator is employed to regulate current in the first-stage control loop, as written in (3.10).

$$T_{ig}(s) = C_{ig}(s) \cdot F_{mg} \cdot G_{ig}(s) \cdot H_{ig}(s) \tag{3.9}$$

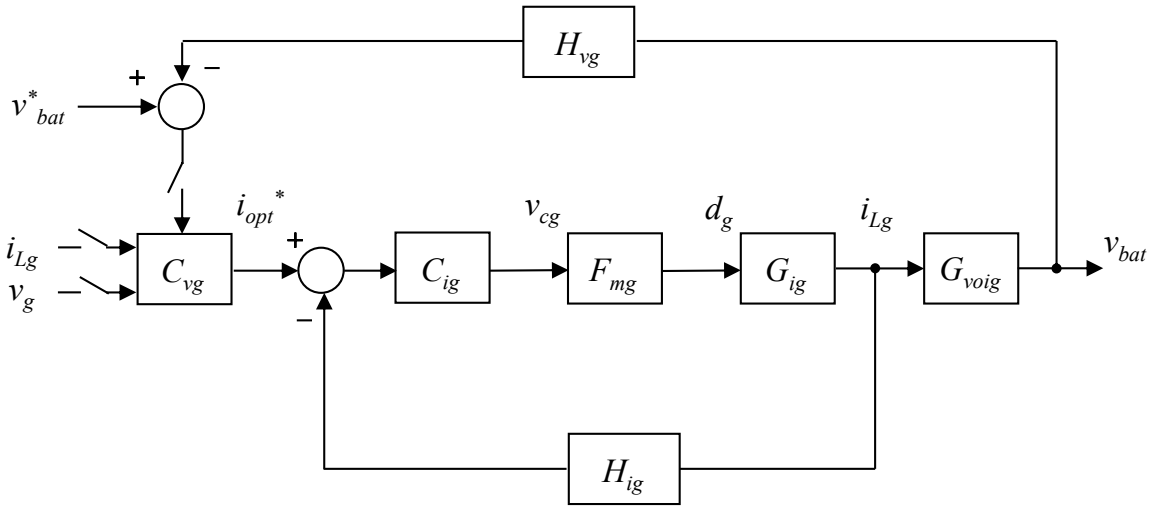


Figure 3.7 Block diagram of closed-loop control of first-stage converter.

$$C_{ig}(s) = C_{ig}(0)\frac{\left(1+\frac{s}{2\pi f_{ig,z1}}\right)\cdot\left(1+\frac{s}{2\pi f_{ig,z2}}\right)}{s\cdot\left(1+\frac{s}{2\pi f_{ig,p1}}\right)\cdot\left(1+\frac{s}{2\pi f_{ig,p1}}\right)} \tag{3.10}$$

Following the design procedure detailed above, a compensator is designed using the circuit parameter values shown above, under both a light-load and a heavy-load condition. The compensator parameters are designed as; $C_{ig}(0)$=74900, $f_{ig,z1}$ = 2.0kHz, $f_{ig,z2}$ = 2.7kHz, and $f_{ig,p1} = f_{ig,p1}$ = 19kHz. This design results in a phase margin greater than 130° and gain margin of greater than 17dB, with the cross-over frequency from 600Hz to 3kHz. Figure 3.8 illustrates the gain/phase plot of the loop gain (T_{ig}) with/without the compensator C_{ig}, under light-load and heavy-load condition. The observed parameters matched the design results well. The designed compensator is valid for the first-stage control loop.

The outer loop design depends on the inner current loop design. From 3.7, the loop gain of the outer loop (T_{vg}) can be written as (3.11), where T_{icl} is the closed-loop transfer function of the inner current loop.

$$T_{vg}(s) = C_v(s)\cdot T_{igcl}(s)\cdot G_{igvo}(s)\cdot H_{vg}(s) \tag{3.11}$$

$$T_{igcl}(s) = \frac{\hat{i}_{Lg}}{\hat{i}_{opt}^{*}} = \frac{1}{H_i(s)} \cdot \frac{T_{ig}(s)}{1 + T_{ig}(s)} \tag{3.12}$$

As written in (3.13), the transfer function of the unified control scheme (C_{vg}) has the constant gain (K_p), which should be designed to provide a proper phase margin and gain margin for the loop gain of the outer loop (T_{vg}). Its cross-over frequency also needs to be much lower than that of the inner current closed-loop control (typically one decade less than), so that the interaction between two closed-loop controls is reduced.

$$G_{vg}(s) = \frac{\hat{i}_{opt}^{*}}{\hat{e}_{vo}} = \frac{K_p}{T_s} \cdot \frac{1}{s \cdot e^{s \cdot Ts}} \tag{3.13}$$

Considering these design requirements, K_p is selected to be 0.02. Consequently, the loop gain (T_{vg}) exhibits a phase margin greater than 80° and a gain margin of greater than 40dB, with a cross-over frequency between 70Hz and 300Hz. Figure 3.9 illustrates the gain/phase plot for open- and closed-loop cases, under light-load and heavy-load condition. One noticeable thing is the abrupt phase drop beyond the half of the sample frequency or $f_{sw}/2$. It comes from the digital sampling effect, and it is interpreted by the delay term in (3.13).

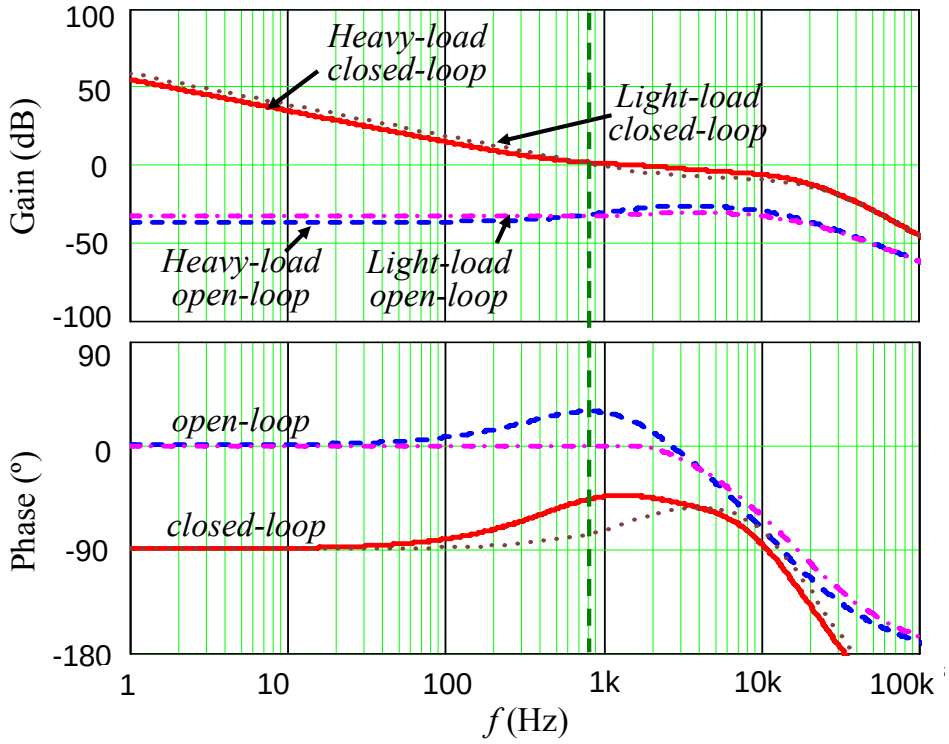


Figure 3.8 Gain/phase plots of first-stage current loop gain with/without compensator.

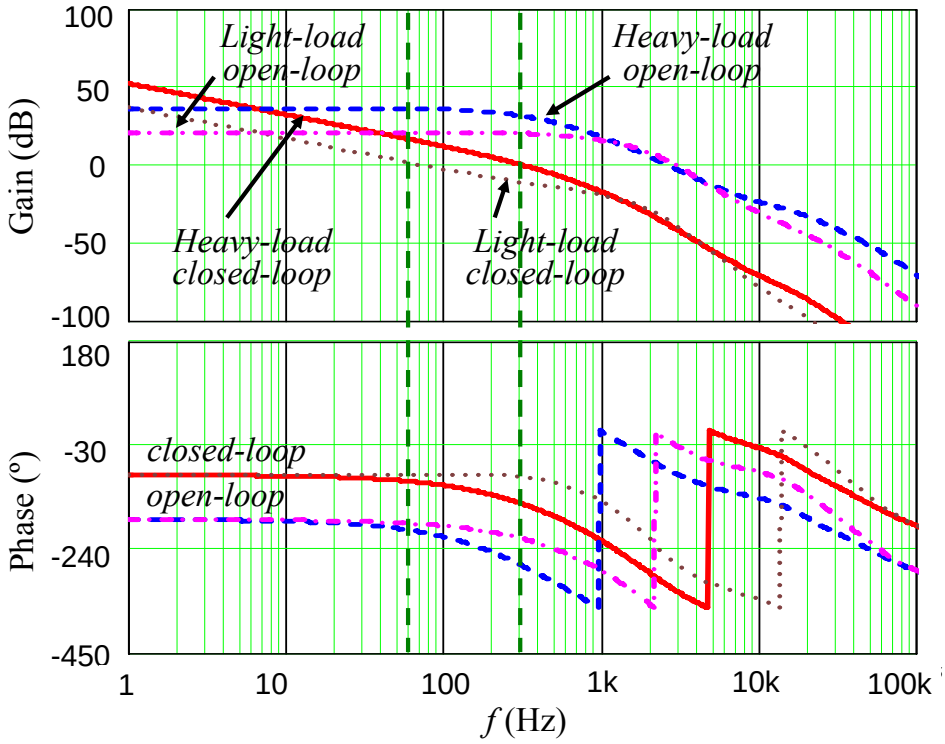


Figure 3.9 Gain/phase plots of first-stage voltage loop gain with/without compensator.

3.3.2 Second-stage control loop design

Illustrated in Figure 3.10, the closed-loop compensator diagram of the second-stage control loop can be defined where: G_{io} — duty-to-current transfer function, G_{vdio} — current-to-link transfer function, C_{io} — inner current loop compensator, C_{vo} — outer dc link voltage compensator, H_{vo} — voltage conditioning circuit transfer function, H_{io} — current conditioning circuit transfer function, and F_{mo} — PWM gain. In similar way, the current-to-link transfer function (G_{vdio}) and the loop gain (T_{io}) are given as:

$$G_{vdio}(s) = \frac{\hat{v}_d}{\hat{i}_{Lo}} = \frac{\hat{v}_d}{\hat{d}_o} \cdot \frac{\hat{d}_o}{\hat{i}_{Lo}} = G_{vo}(s) \cdot \frac{1}{G_{io}(s)} \tag{3.14}$$

$$T_{io}(s) = C_{io}(s) \cdot F_{mo} \cdot G_{io}(s) \cdot H_{io}(s) \tag{3.15}$$

Similarly, the inner current loop is designed with a type 3, two-zero and three-pole compensator, as shown in (3.15). The above design procedure can also be applied here.

$$C_{ig}(s) = C_{io}(0) \frac{\left(1 + \frac{s}{2\pi f_{io,z1}}\right) \cdot \left(1 + \frac{s}{2\pi f_{io,z2}}\right)}{s \cdot \left(1 + \frac{s}{2\pi f_{io,p1}}\right) \cdot \left(1 + \frac{s}{2\pi f_{io,p1}}\right)} \tag{3.16}$$

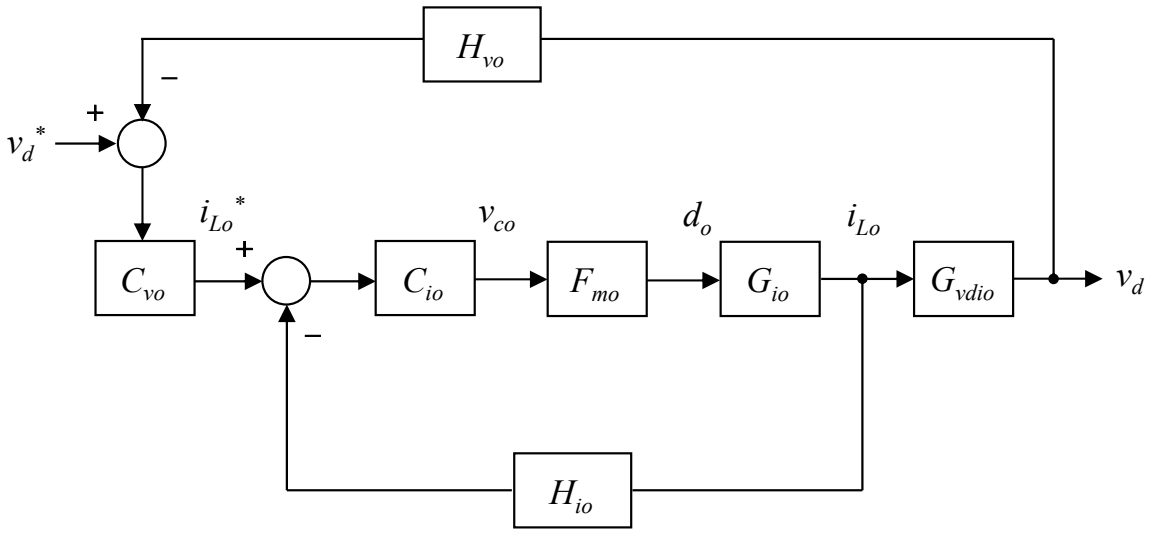


Figure 3.10 Block diagram of closed-loop control of second-stage converter.

Following the design procedure detailed above, the compensator with $C_{io}(0)$=10000, $f_{io,z1}$ = 4.7kHz, $f_{io,z2}$ = 5.5kHz, $f_{io,p1}$ = 20kHz, and $f_{io,p2}$ = 23kHz can be adopted for the inner current loop. Eventually, this design gives us the T_{io} with a phase margin greater than 100° and a gain margin of greater than 20dB with a cross-over frequency of approximately 800Hz. These design results are also verified by the gain/phase plot of the loop gain (T_{ig}) with/without the compensator (C_{ig}), under light-load and heavy-load condition, shown in Figure 3.11.

Now, the outer loop design becomes a routine. The loop gain of the outer loop (T_{vo}) and the closed-loop transfer function of the inner loop (T_{iocl}) are seen below,

$$T_{vo}(s) = C_{vo}(s) \cdot T_{iocl}(s) \cdot G_{iovd}(s) \cdot H_{vo}(s) \tag{3.17}$$

$$T_{iocl}(s) = \frac{\hat{i}_{Lo}}{\hat{i}_{Lo}^{*}} = \frac{1}{H_{io}(s)} \cdot \frac{T_{io}(s)}{1 + T_{io}(s)} \tag{3.18}$$

Most of the time, for the outer loop control, a type 2, one-zero and two-pole compensator can satisfy the system performance requirement. This is because dynamics of the plant can be easily approximated by simple first-order system using the effect of the inner current loop control.

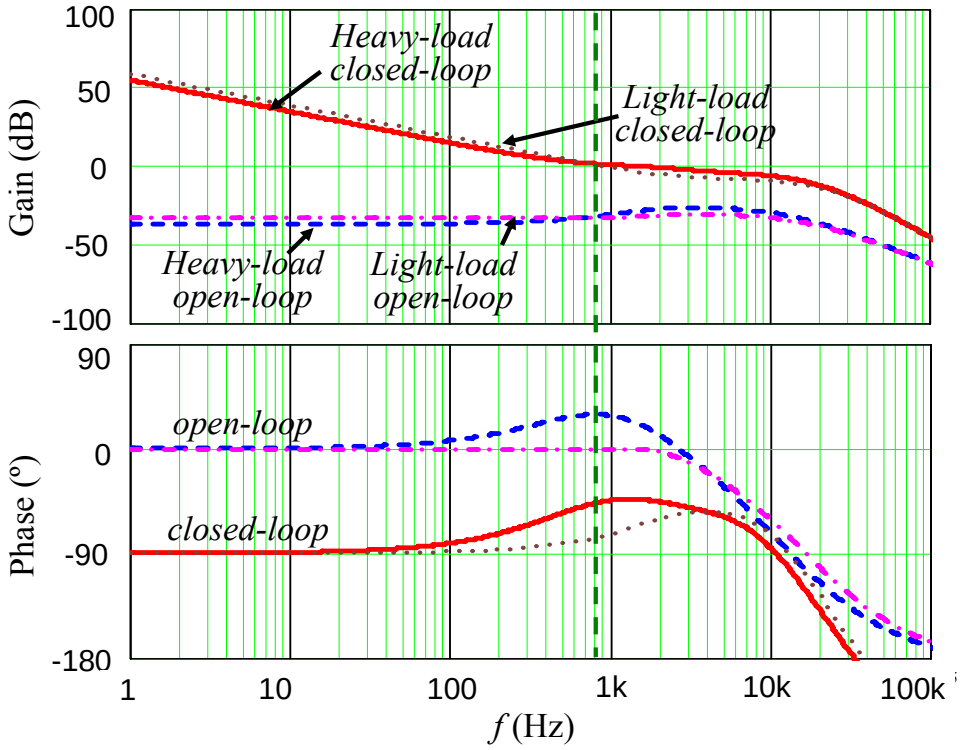


Figure 3.11 Gain/phase plots of second-stage current loop gain with/without compensator.

$$C_{vo}(s) = C_{vo}(0)\frac{\left(1+\frac{s}{2\pi f_{vo,z}}\right)}{s\cdot\left(1+\frac{s}{2\pi f_{vo,p}}\right)} \tag{3.19}$$

Based on the design procedure above, a design example of the outer loop compensator would be given as: $C_{vo}(0)$ = -282, $f_{vo,z}$ = 350Hz, and $f_{vo,p}$ = 2.5kHz. Note that the compensator requires a negative gain because the loop gain (T_{vo}) is already a negative value, which originates from a negative dc gain of the $G_{vo}(s)$ in (1.36). The gain/phase plot of the loop gain (T_{ig}) verifies the design results in Figure 3.12.

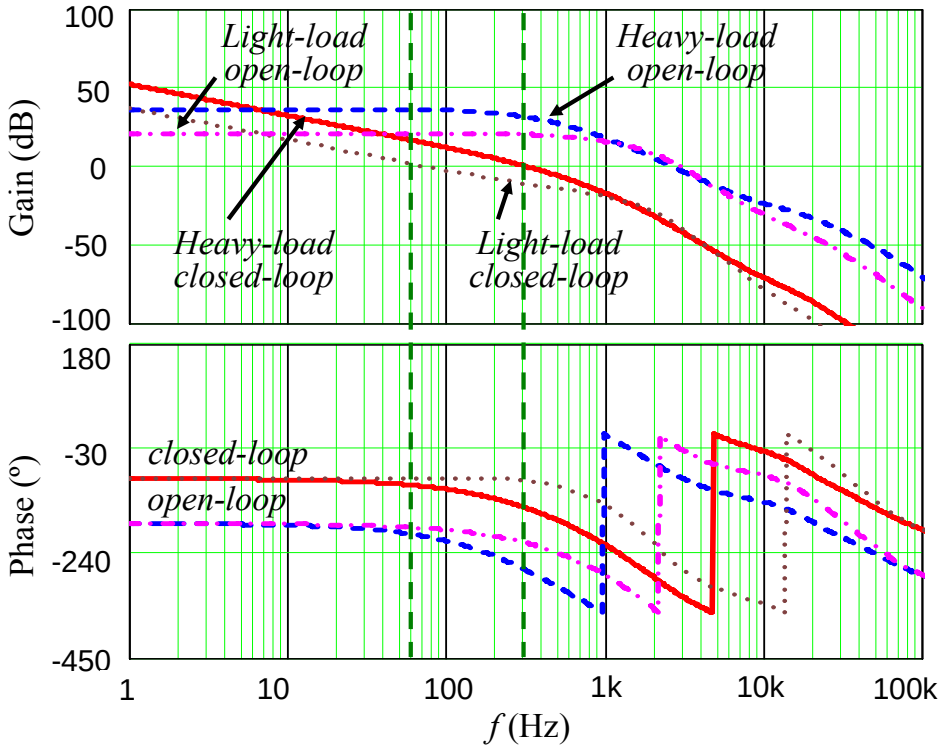


Figure 3.12 Gain/phase plots of second-stage voltage loop gain with/without compensator.

3.4 Performance evaluation of generalized control structure

A well-designed compensator must guarantee system stability under all the operating circumstances. Applying the compensators that were designed in Section 3.3 to the generalized control structure, a hardware prototype is built to verify the compensator design. System performance is evaluated to achieve two distinctive control objectives of maximum power harness and battery management under the generalized control structure employing the unified control scheme.

Figure 3.13 shows the hardware prototype of the thermoelectric generator battery storage system. It consists of four major parts: an adjustable power supply with a series resistor (in order to mimic the thermoelectric generator), a three-phase interleaved synchronous boost-buck converter, a microprocessor implementing the compensators associated with the generalized control structure, and a lead-acid battery with a variable resistor bank.

For all experimental tests in this section, the adjustable power supply is set to 14.9V output. This output voltage corresponds to the electromotive force (e_{teg}) of the actual thermoelectric generator. The three-phase boost-buck converter is composed of two stacked power boards, where the inner current control loops are implemented on the power board by using the analog circuitry. The lead-acid battery shows 14.4 V nominal working voltage when it is fully charged. This working voltage is preset in the microprocessor for the unified control scheme.

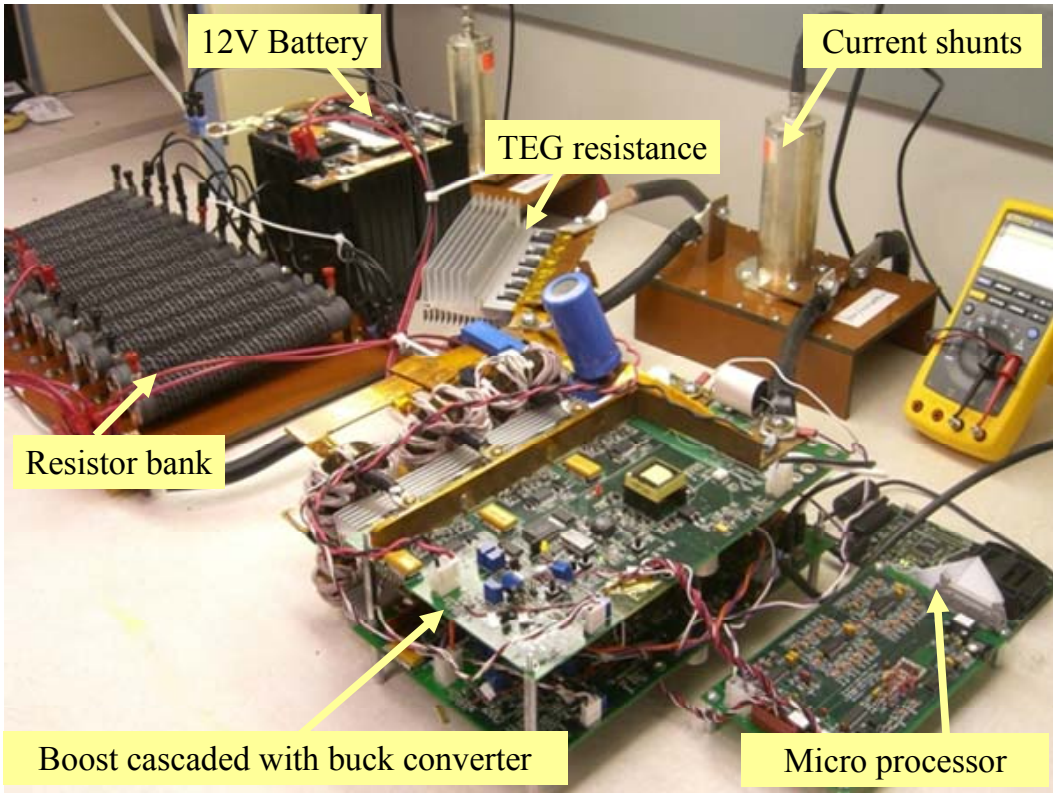


Figure 3.13 Test setup of thermoelectric generator power conversion system.

3.4.1 Evaluation of achieving two distinctive modes

First, the thermoelectric battery energy storage system is operated alternatively in two distinctive modes to evaluate the transient- and steady-state performance. Mode transfer between the two control modes is tested based on the variable resistor bank. The series resistor of the adjustable power supply is set to 0.21 Ω.

Figure 3.14 shows the experimental waveforms when the system is transferred from the maximum power point tacking control to power matching control. To trigger mode transfer, the demanded power is reduced by increasing the variable resistor bank from 0.5Ω to 1Ω. At the beginning, the battery is discharged to support too much demanded power, and the battery voltage is less than its fully charged voltage (14.4V). Therefore, the energy storage system is operated in the maximum power point tacking control close to its analytical maximum power point (264.3W) and its corresponding optimal current (35.5A) in order to harvest as much power as possible. When the demanded power is reduced, the battery begins charging, due to the presence of excessive power by decreasing demanded power. Accordingly, the battery voltage increases to its nominal working voltage and eventually fully charges. The energy storage system now is transferred to the power matching control, and the unified control scheme starts to reduce the current gradually. Accordingly, input power is slowly reduced. Eventually, the power balance is achieved between the input and output, and the current settles down and remains unchanged.

The experimental observation illustrates that transferring between two control modes under the generalized control structure employing the unified control scheme is achieved smoothly, continuously and seamlessly. Compare with Figure 3.2, it is seen that

the dc link voltage oscillation at the low frequency is almost eliminated. Meanwhile, it is tightly regulated at the constant value even under mode transfer and demanded power change. The mitigation of this voltage oscillation enables smooth input power and current oscillation at the low frequency. As a result, the issues caused by the existing stop-and-go concept under the conventional control structure, such as higher current handling capability requirement, derated power operation, and increased conduction losses, are totally eliminated. This experimental test supports that the generalized control structure improves the performance and reliability of a battery energy storage system.

Figure 3.15 shows the experimental waveforms when the system returns the maximum power point tacking control from power matching control. The control mode changes when the variable resistor bank decreases (1Ω to 0.5Ω). When the variable resistor bank is reduced to 0.5 Ω, the battery is discharged again. The battery voltage drops to less than its nominal working voltage. As a result, the energy storage system returns the maximum power point tacking control. The current start to increase again, and the input power approaches its analytical maximum power point (264.3W) again. The mode transfer is then completed. Note that dc link voltage is well maintained at the commanded reference of 20V.

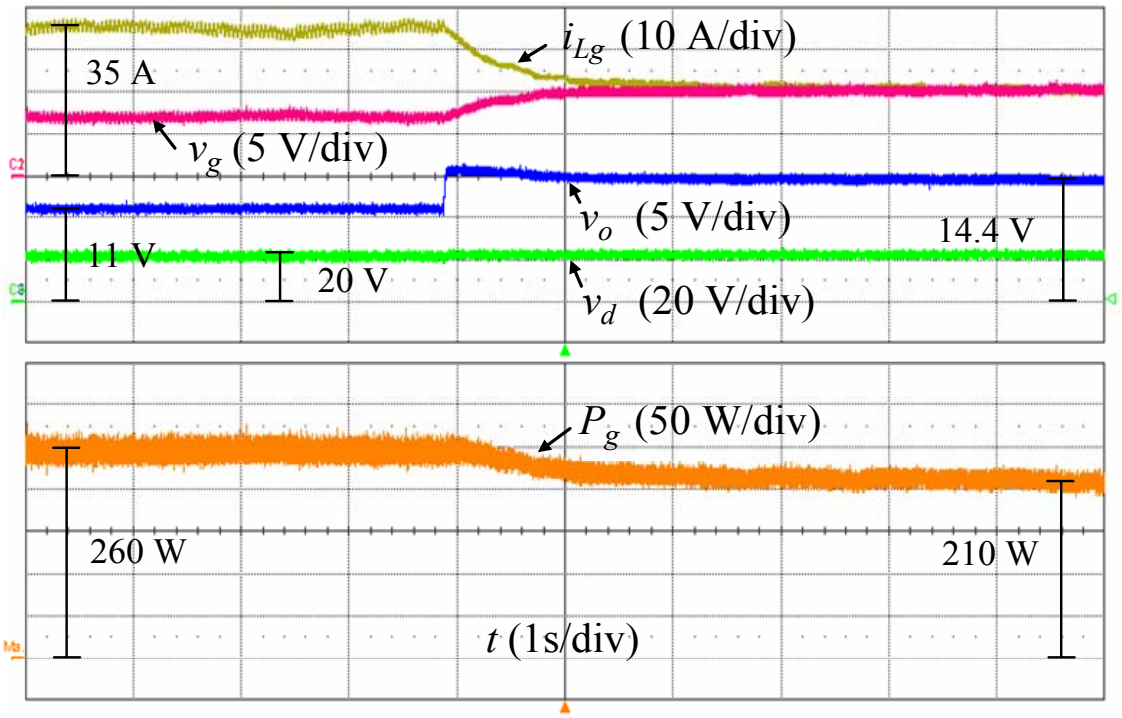


Figure 3.14 Experimental waveform of mode transfer test from maximum power point tracking mode to power matching mode (1 sec/div).

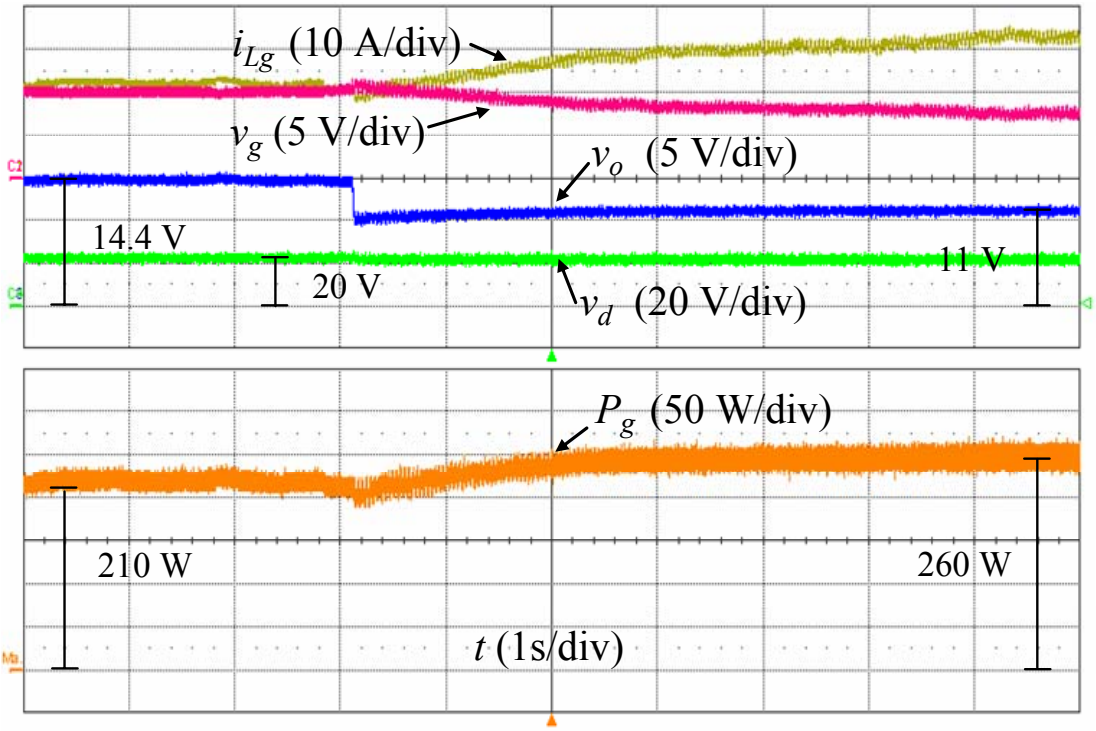


Figure 3.15 Experimental waveform of mode transfer test from power matching mode to maximum power point tracking mode (1 sec/div).

3.4.2 Evaluation of maximum-power-point tracking accuracy

To evaluate the maximum power point tracking accuracy of the unified control scheme, the series resistor of the adjustable power supply is dynamically adjusted from 0.21Ω to 0.26Ω and vice versa, while the variable resistor bank is set to 0.5. Figure 3.16 illustrates experimental waveforms when the series resistor is increased to 0.26Ω. By increasing the series resistor, the unified control scheme reduces the operating current slowly, and input power starts to increase, accordingly. Eventually, the unified control scheme settles down to the new maximum power point, close to its analytical maximum power point 191.4W and its corresponding optimal current (25.6A).

Figure 3.17 illustrates experimental waveforms when the series resistor is reduced to 0.21 Ω. When reduced, the unified control scheme detects the change of the maximum power point. Therefore, it moves the operating point toward new maxim power point by increasing the operating current. Accordingly, the input power starts to increase, and it eventually reaches the new maximum power point, where the analytical maximum power point is 264.3W at optimal current (35.5A). The battery voltage is increased as the operating point move close to its maximum power point.

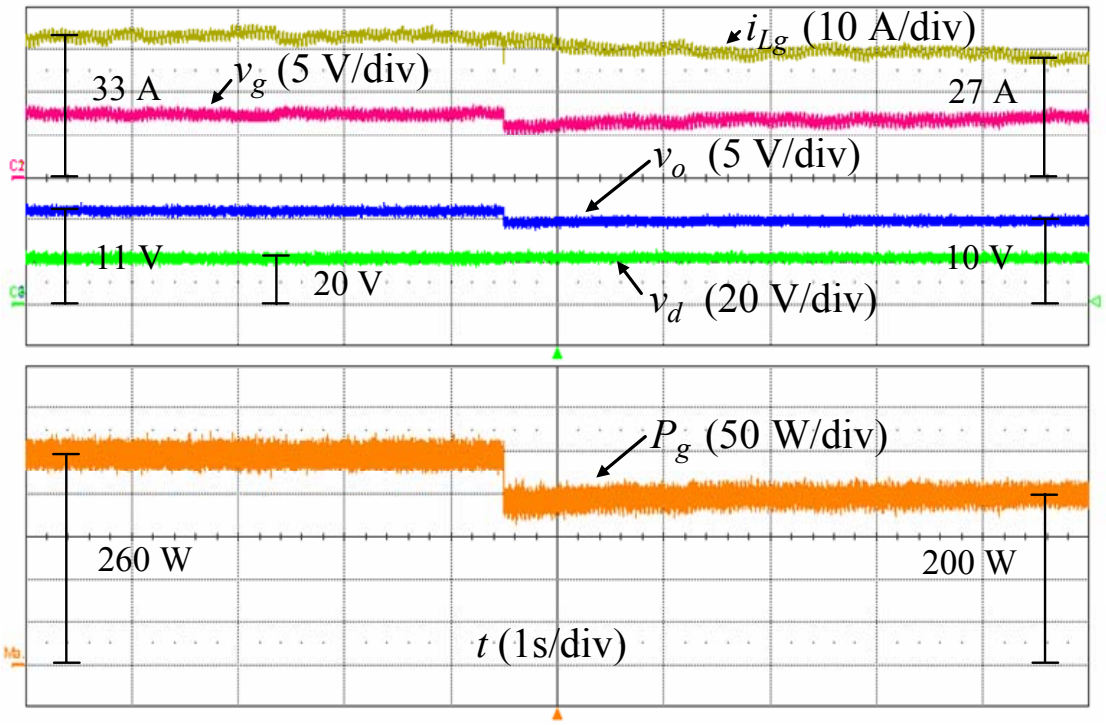


Figure 3.16 Experimental waveform when internal resistance is changed from small resistance to large resistance (1 sec/div).

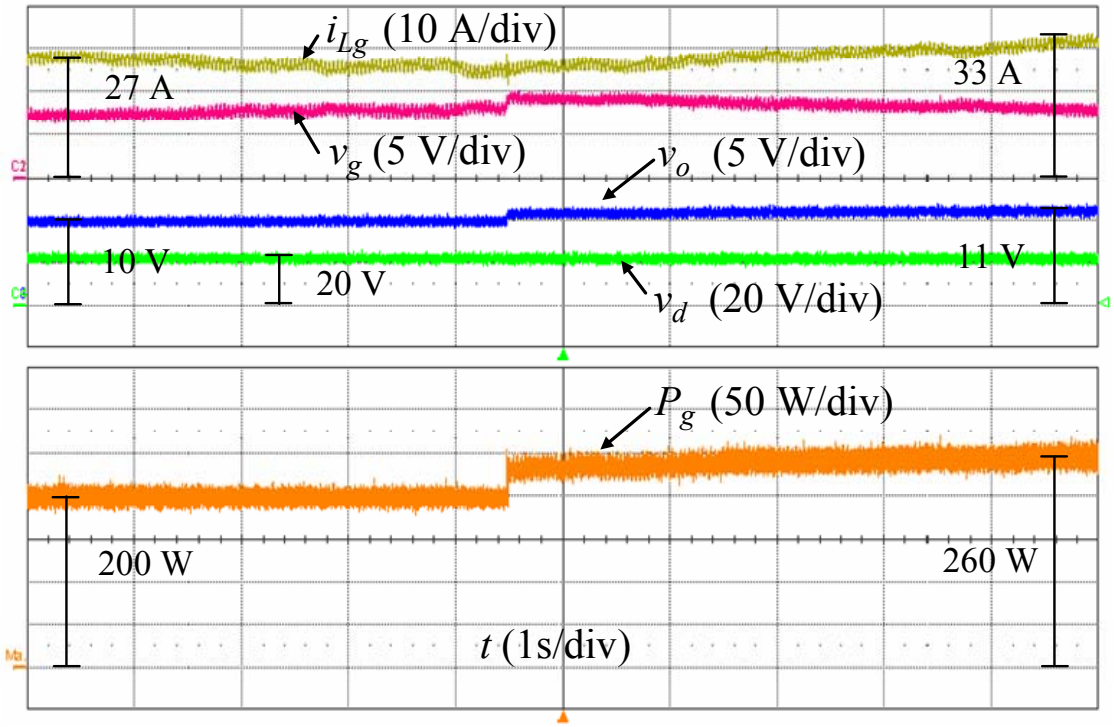


Figure 3.17 Experimental waveform when internal resistance is changed from large resistance to small resistance (1 sec/div).

3.4.3 Evaluation of dc link voltage regulation

Improving the dc link voltage regulation is another unique feature of the generalized control structure. In this control structure, the dc-link voltage (v_d) can be regulated at any given command. This feature allows more flexibility of energy harnessing when the dc-link capacitor is replaced with an electric double-layer capacitor.

Figure 3.18 illustrates the experimental waveforms regulating the dc link voltage while periodically changing the reference from 20V to 30V and vice versa. It is clear that the dc link voltage follows the reference very well, while the battery voltage and input power are not affected by this variation. Based on experimental tests shown so far, we also can conclude the effectiveness of the compensator design discussed in section 3.3 is verified. The thermoelectric battery energy storage system operates well without any stability issue.

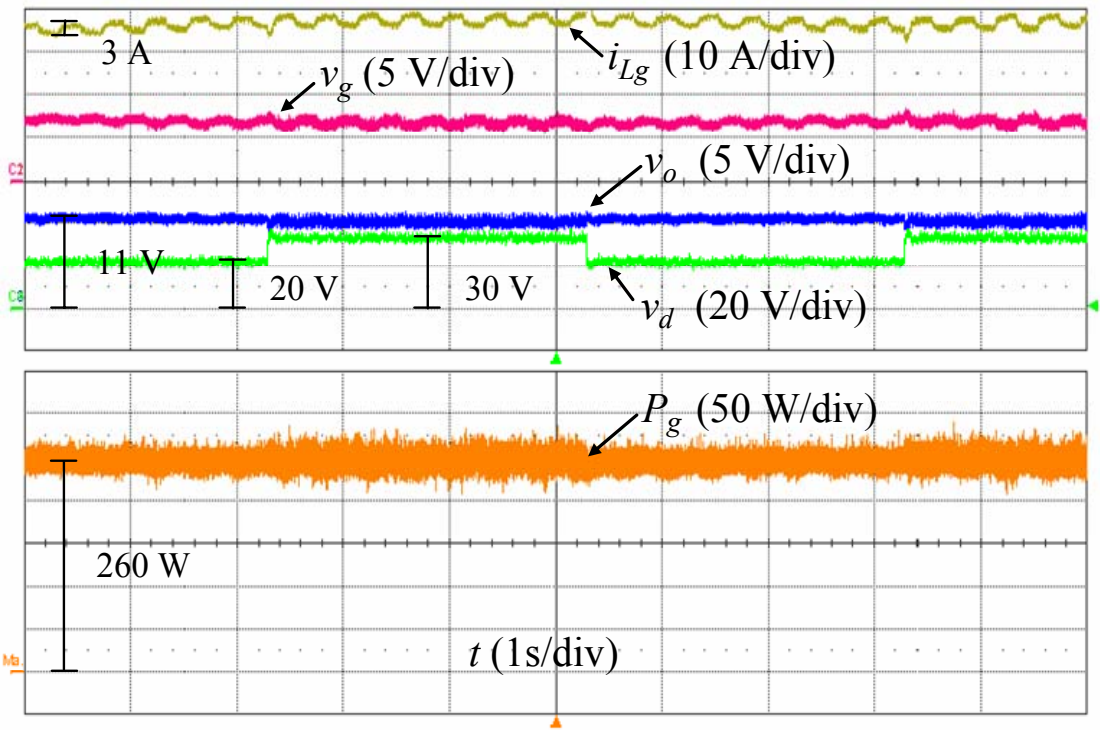


Figure 3.18 Experimental waveform of dc-link voltage regulation (1 sec/div).

3.5 Summary

In this chapter, issues of the conventional control structure have been discussed. The particular issues arise when the conventional control is utilized for the stop-and-go concept to achieve two distinctive control modes. The major reason for these issues was analyzed. Based on the analysis, the generalized control structure was proposed with its implementation for a battery energy storage system. A unified control scheme was proposed along with its small-signal transfer function for a rational design. Design of proportional-integral-derivative compensators for first-stage control loop and second-stage control loop occurred. The experimental tests were carried out to verify the compensator design and to evaluate the generalized control structure's performance. From experimental results, the superiority of the generalized control structure was proven under: 1) achieving two distinctive modes, 2) maximum power point tracking accuracy, and 3) dc link voltage regulation.

Chapter 4

Research Extension to Single-Phase Grid-Connected System

4.1 Introduction

For a better utilization of renewable energy sources, the single-phase grid-connected power system has been another promising solution for the last decade [3]-[6]. In this chapter, we will apply our research works to the single-phase grid-connected power system based on a two-stage power converter employing a photovoltaic source. The basic principle and electric characteristics of a photovoltaic source will be briefly presented first. Then, the single-phase grid-connected power system using a two-stage dc-ac power converter will be introduced.

For the single-phase grid-connected power system, modeling works become more complicated. This is due to the presence of time-varying state variables which originate from the connected electrical grid. In order to cope with the time-varying state variables, the quasi-steady state concept will be employed for the aggregated modeling approach. Its modeling results will be shown with some major transfer functions. Finally, a new active

ripple compensation scheme based on the generalized control structure will be proposed, in order to attenuate the low frequency ripple current drawn from the photovoltaic source. Its control loop design will be detailed, and the simulation and experimental results will be provided to support its effectiveness and improvement.

4.2 Photovoltaic single-phase grid-connected system

A photovoltaic is a type of technology that generates direct current electrical power from solid state P-N junction semiconductors when it is illuminated by photons. Since Edmund Becquerel discovered the photovoltaic effect in 1839, photovoltaic technology has rapidly been developed and has established itself as one of the most promising energy sources in virtually unlimited areas, from small consumer electronics to large utility power generation. In particular, this technology attracts lots of interests as a medium power distributed generation system. It allows energy efficient power generation on customer sites by being connected to the existing utility grid.

4.2.1 Fundamental of photovoltaic and its electrical characteristics

A photovoltaic cell is simply considered as a semiconductor diode that has been carefully designed and constructed to efficiently absorb and convert light energy from the sun into electrical energy. In general, a semiconductor has the capacity to absorb light and to deliver a portion of the absorbed light energy to carriers of electrical current, i.e., electrons and holes. This phenomenon is known as the photovoltaic effect – discovered by Edmund Becquerel during his experiments with an electrolytic cell made up of two metal electrodes. A typical photovoltaic cell structure is depicted in Figure 4.1. The

sunlight strikes the photovoltaic panels, from the top on the front of the photovoltaic cell. A metallic grid, which electrically contacts the one side of the photovoltaic cell, allows light to fall on the surface of the semiconductor through the grid lines. An anti-reflective layer between the grid lines increases the amount of sunlight transmitted to the semiconductor. As a result, photons, particles or packets composing light, are absorbed into the n-type and p-type semiconductor materials.

The n-type and p-type semiconductor materials in the photovoltaic cell have weakly bonded majority carriers, electrons in the n-type semiconductor and holes in the p-type, occupying a band of energy called the valence band. When the energy of a photon, exceeding a certain threshold (often called the band gap), is transferred to valence carriers by striking the atom, the bonds grapping the majority carriers are broken. These carriers become almost free to move around in a new energy band, called the conduction band. They are now subject to the classic processes of drift and diffusion, similar to a thermoelectric device.

Consequently, the electric field is built-up to balance the diffusion carriers and drift carriers in equilibrium steady state, which is electric potential for power generation. Since the fundamental of photovoltaic cell is based on a semiconductor diode, its electrical characteristics are given by solving the minority-carrier diffusion equation with appropriate boundary condition, similar to a semiconductor diode. The resultant equations are shown in (4.1)-(4.3), when the internal shunt resistance is not considered. The generated current (i_g) and saturation current (i_{sat}) are given in (4.2) and (4.3), respectively.

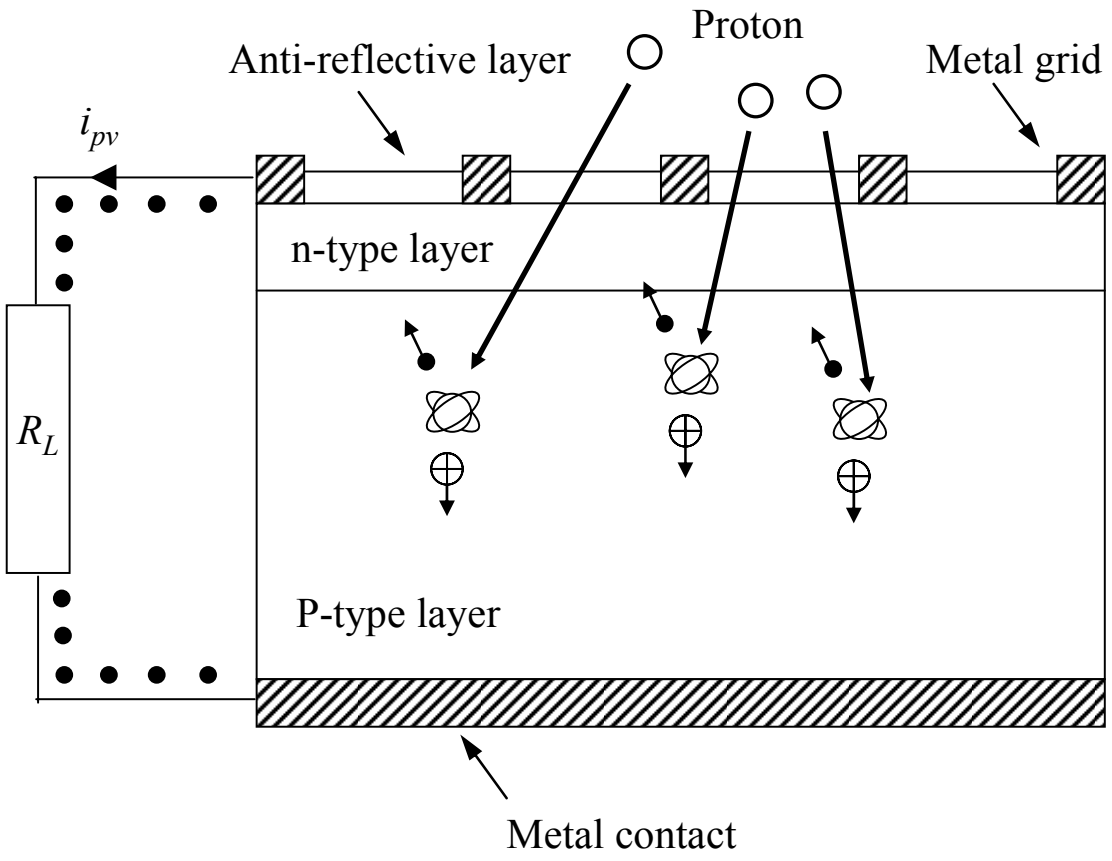


Figure 4.1 Basic structure of typical photovoltaic cell.

$$i_{pv} = i_g - i_{sat} \cdot \left[\exp\left(\frac{q}{AKT} v_{pv} \right) - 1 \right] \tag{4.1}$$

$$i_g = \left[i_{sc} + K_I \left(T_c - 25 \right) \right] \frac{\lambda}{100} \tag{4.2}$$

$$i_{sat} = i_{or} \cdot \exp\left[\frac{qE_{go}}{KT} \left(\frac{1}{T_r} - \frac{1}{T} \right) \right] \cdot \left(\frac{T}{T_r} \right)^{\frac{X_T}{A}} \tag{4.3}$$

All the symbols in (4.1)-(4.3) are defined as follows;

i_{pv}	Photovoltaic output current
v_{pv}	Photovoltaic output voltage
i_g	Generated current under a given insulation
i_{sat}	Reverse saturation current,
q	Charge of an electron; 1.602×10^{-19} C (coulombs)
A	Ideality factor for the given p-n junction (usually given 1 to 5)
K	Boltzmann's constant; 8.62×10^{-5} eV/K
T	Photovoltaic temperature in K (Kelvin)
I_{sc}	Photovoltaic short circuit current at 28°C and 100 mW/cm^2
K_I	Temperature coefficient of short circuit current; 0.0017 A/°C
T_c	Photovoltaic temperature in °C (Celsius)
λ	Photovoltaic illumination (mW/cm^2)

T_r Reference temperature; 301.18 K

i_{or} Saturation current at T_r; 19.97×10^{-6} A

E_{go} Band gap energy (1.12 eV for silicon)

X_T Temperature exponent of saturation current (3 for p-n junction)

Considering intrinsic shunt resistance (R_p) and series resistance (R_s), the equivalent circuit model of the photovoltaic cell can be illustrated as Figure 4.2. Shown in Figure 4.2, the equivalent circuit is composed of the current source, varied with sunlight illumination and temperature, and of the diode, whose reverse saturation current is also varied by temperature. The output voltage of the photovoltaic is explained by the diode forward voltage drop caused by the difference between the current source and photovoltaic output current. According to (4.2), the magnitude of the current source is proportional to the strength of sunlight illumination. When illumination is intensified, the diode voltage drop is raised under the constant photovoltaic output current, due to the larger current source. Therefore, output voltage of the photovoltaic increases.

On the other hand, higher temperature increases the saturation current (i_{sat}), as seen from (4.3). This increasing saturation current, in the equivalent circuit model of the photovoltaic cell, can be understood to replace the existing diode to the new diode, which has more heavily doped n-type and p-type semiconductor materials. Increase of doping concentration in a semiconductor diode, in general, leads to small forward voltage drop under same current conduction. Consequently, the equivalent circuit shows that the output voltage of the photovoltaic is reduced when temperature is increased. Note that,

according to (4.2), higher temperature also increases the current source, but this impact is negligible when compared to the effect of the saturation current.

Figure 4.3 shows actual measurements of the voltage-current characteristics and its corresponding power-current characteristics under four different intensities of light illumination, where high concentration type photovoltaic (also known as HCPV) are used with four in series and ten in parallel configuration. These actual measurements are well matched with the behaviors of the equivalent circuit shown in Figure 4.2. As seen in the figures, the photovoltaic characteristics exhibit nonlinear properties with varying the maximum power point. These nonlinearities of a photovoltaic system require some type of power converter in order to achieve efficient and reliable operation.

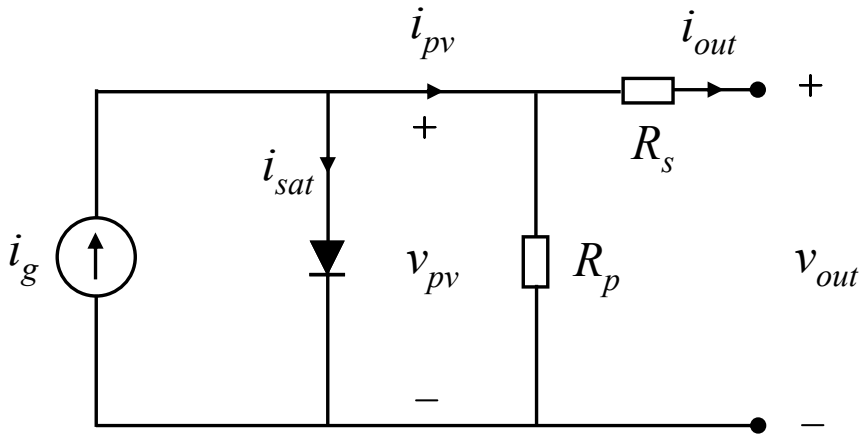
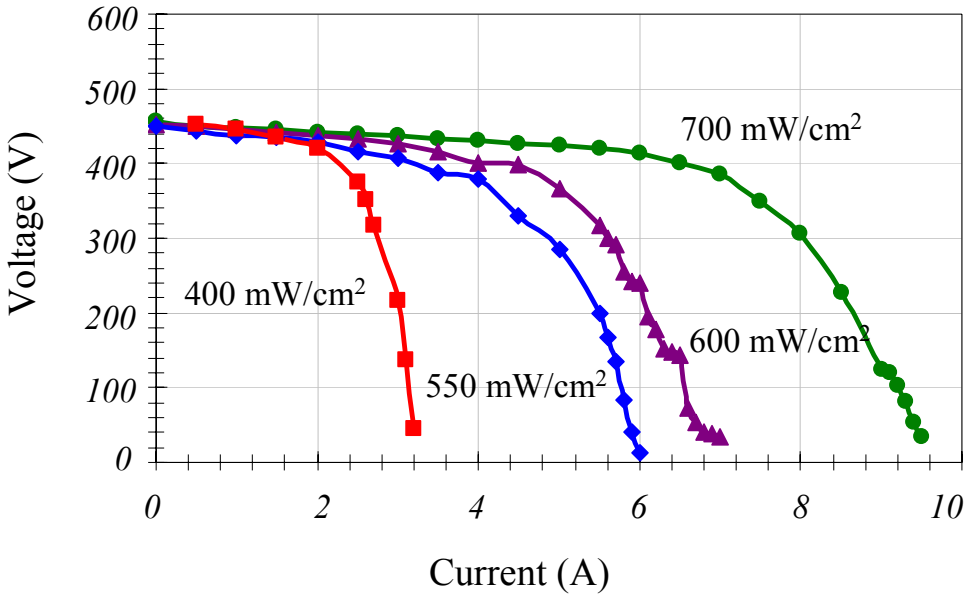
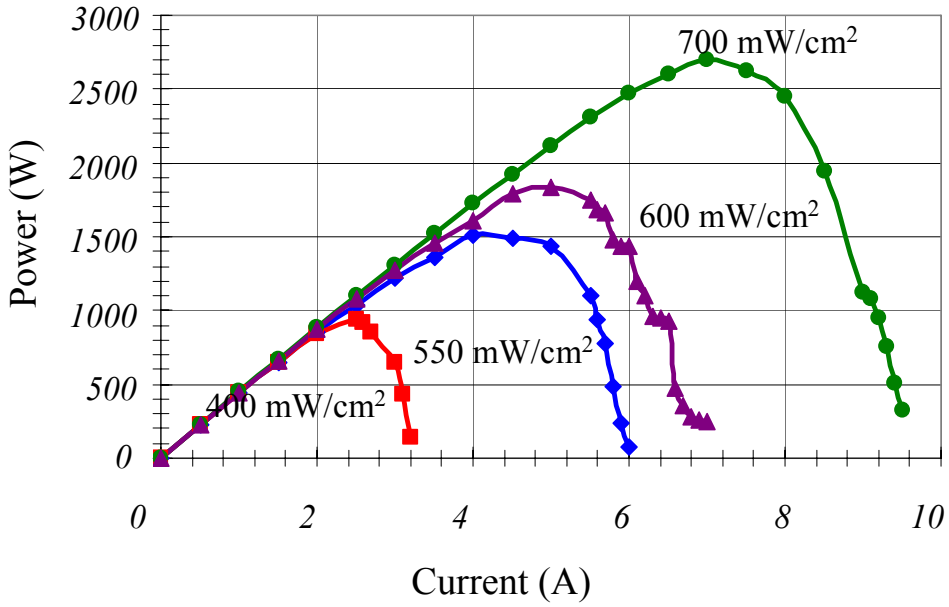


Figure 4.2 Equivalent circuit of photovoltaic cell.



(a)



(b)

Figure 4.3 Electrical characteristics of photovoltaic cell; (a) current-to-voltage curve and (b) current-to-power curve.

4.2.2 Two-stage dc-ac power converter for photovoltaic grid-connected system

Figure 4.4 illustrates the proposed converter, composed of the first-stage and second-stage converter. For the first-stage converter, a non-isolated type boost converter topology is employed along with a four-phase interleaved scheme operated with 90-degree phase shift. The four-phase interleaved scheme helps to increase power conversion efficiency and to reduce switching ripple current. Inversely coupled inductors are adapted between the two phases which have a 180-degree phase shift. The coupled inductor shares the center leg in the EE core and cancels the magnetic flux inside the center leg. Using the coupled inductor reduces the core losses effectively, in particularly, when the inductor current shows the large magnitude of ripple components in high frequency range, and consequently, power conversion efficiency is further improved.

Thanks to ripple current cancellation by four-phase interleaved scheme, each inductor can be designed with small inductance, which enables the converter to achieve zero voltage switching (ZVS) operation with the synchronous rectifiers. The ZVS operation permits not only reduced turn-on losses and EMI noises but also the utilization of MOSFET rather than insulated gate bipolar transistor (IGBT), even at high voltage. Based on ZVS operation, MOSFET failure is avoided by eliminating the excessive reverse recovery current caused by its body diode. In this circuit, the recently developed superjunction MOSFET (sometimes referred as the CoolMOS^{TM} from Infineon) is utilized, where this MOSFET provides much smaller on-resistance when compared with the existing IGBT, almost by a factor of 1/5. All the features of this circuit improve the power conversion efficiency incredibly. As a result, the experimental results show high efficiency close to 99% as shown in Figure 4.5.

A single-phase full-bridge inverter topology is employed for the second-stage converter with the output inductor serving as the energy buffer between the two voltage sources, the dc link voltage and the existing utility grid. The IGBT is utilized in this circuit, with the top IGBT and bottom IGBT in the same phase operating in a complimentary pattern. The switching ripple of the output current is attenuated by adapting the unipolar PWM scheme. This effectively doubles the switching frequency.

The input side of the first-stage converter connects to a photovoltaic source. The output side of the second-stage converter is then connected to the existing utility grid. To reduce high-frequency current, small high-frequency capacitors may be placed in the input of the first-stage. Figure 4.6 illustrates the assembly of the proposed power converter, where the converter of each stage is operated by its own digital signal processor (DSP) control circuit. This assembly of the converter is expected to meet the electrical specifications at a nominal operation as: input voltage v_{pv} — 50 ~ 250V, dc link voltage v_d — 400V, interconnected grid voltage v_s — 220V, maximum output power p_{out} — 4KW, and maximum input current — 16A. The electrical parameters of the power converter built in are: input inductor L_{pv} — 180uH, dc link capacitor C_d — 1100u, and output inductor L_s — 2mH.

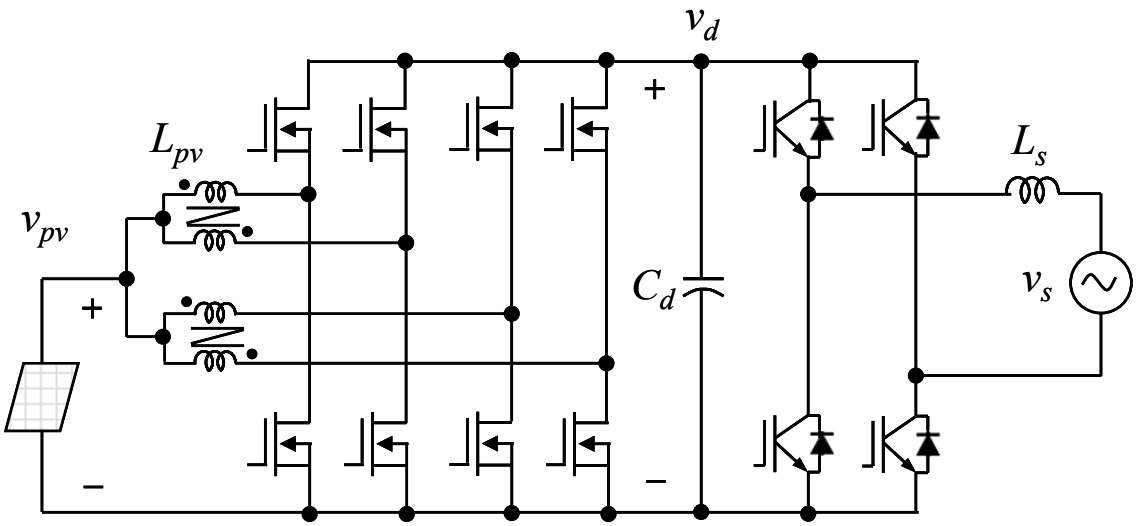


Figure 4.4 Proposed four-phase interleaved synchronous ZVS dc-ac power converter topology for photovoltaic single-phase grid-connected power system.

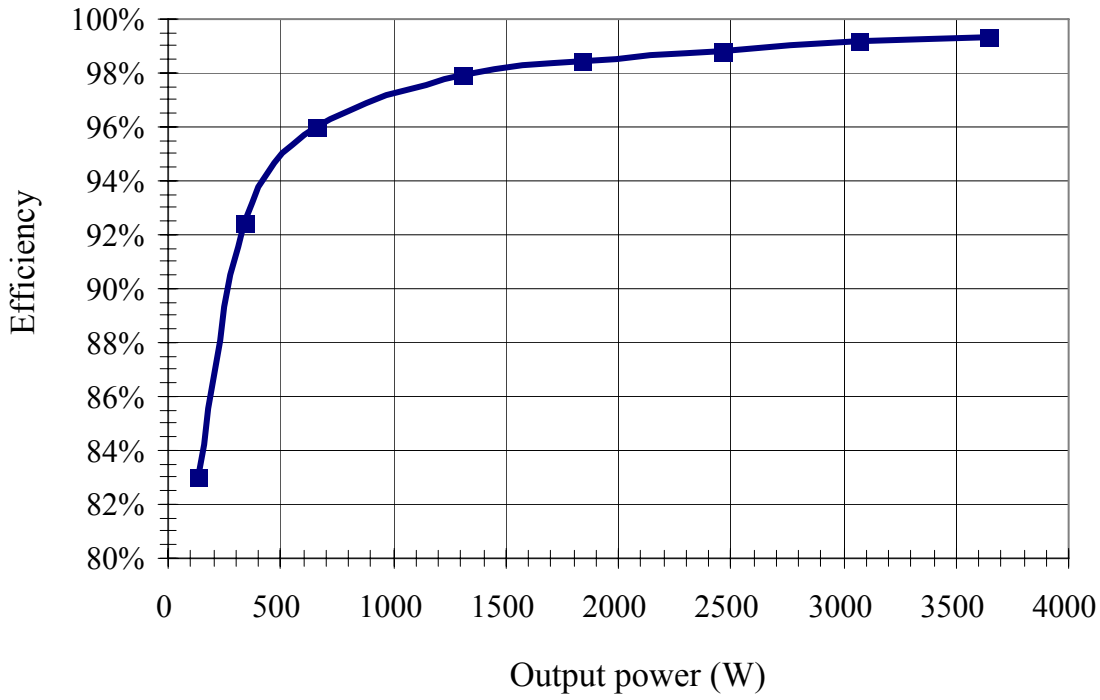


Figure 4.5 Experimental efficiency of four-phase interleaved synchronous ZVS first-stage power converter under 250V input voltage and 400V output voltage.

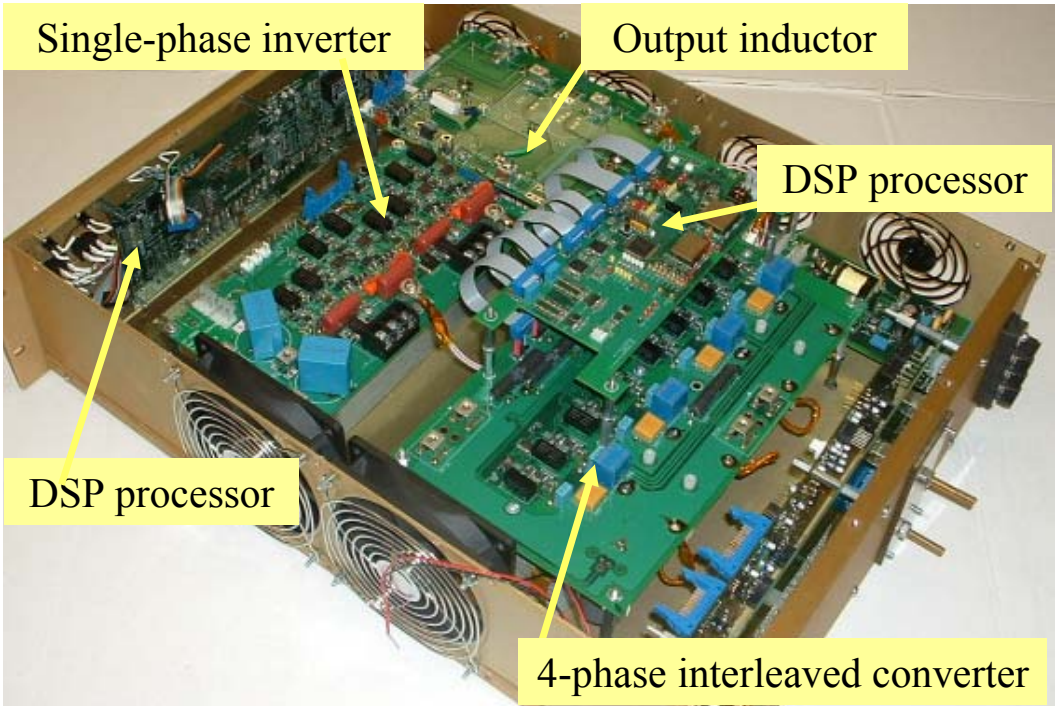


Figure 4.6 Hardware prototype unit of proposed two-stage dc-ac power converter.

4.3 Generalization of aggregated modeling approach and modeling

The existing utility grid transmits electricity in the form of alternating current (ac), in which current and voltage change constantly in their amplitude and regularly change their polarity. Therefore, the photovoltaic, grid-interconnected power system requires dealing with ac electricity in order to cooperate with the existing utility grid on sending generated power smoothly. However, this ac electricity causes a complicated issue in the aggregated modeling approach proposed in chapter 2. The linearizing process to derive the small-signal averaged equations, by introducing the small perturbations, collapses, because of the non-existence of the equilibrium point for ac voltage and/or current. They are the time varying state variables. In this section, we demonstrate how this issue can be overcome in the aggregated modeling approach, and show the generalization of the aggregated modeling approach for all kinds of the two-stage power converters in a unified way.

4.3.1 Large-signal averaged equations and equivalent circuit

Figure 4.7 shows the equivalent circuit model of the photovoltaic single-phase grid-interconnected power system. Discussed in Section 2.4, modeling of the four-phase interleaved boost converter is simplified by using the singe-phase equivalent circuit with the equivalent inductance, which is factored by (1/4) of the each phase inductance, as written in (4.4). The photovoltaic is modeled by a simple voltage source.

$$L_{pveq} = \frac{1}{4} L_{pv} \tag{4.4}$$

The equivalent circuit of Figure 4.7 is composed of three switching legs, all operated by using complementary gate signals. Therefore, each of them can be considered as a single power converter. The equivalent circuit is thus decomposed into three subsets of the converter shown in Figure 4.8. Analyzing the subinterval of each subset converter in accordance to its switching actions and averaging them over one switching period results in the state-space averaging equations as (4.5) - (4.7).

$$\begin{cases} L_{pveq} \dfrac{d\bar{i}_{pv}}{dt} = v_{pv} - \left[\bar{v}_{cd} + R_{cd} \left(\bar{i}_{pv} - \bar{i}_a - \bar{i}_b \right) \right] \left(1 - d_g \right) \\ C_d \dfrac{d\bar{v}_{cd}}{dt} = \bar{i}_{pv} \left(1 - d_g \right) - \bar{i}_a - \bar{i}_b \\ \bar{i}_d = \bar{i}_{pv} \left(1 - d_g \right) \\ v_d = v_{cd} + R_{cd} \left[i_{pv} \left(1 - d_g \right) - i_a - i_b \right] \end{cases} \tag{4.5}$$

$$
\begin{cases}
L_s \dfrac{d\bar{i}_s}{dt} = -\bar{v}_s - \bar{v}_b + \left[\bar{v}_{cd} + R_{cd}\left(\bar{i}_d - \bar{i}_b - \bar{i}_s\right)\right] d_a \\
C_d \dfrac{d\bar{v}_{cd}}{dt} = \bar{i}_d - \bar{i}_b - \bar{i}_s d_a \\
\bar{i}_a = \bar{i}_s d_a \\
\bar{v}_a = \left[\bar{v}_{cd} + R_{cd}\left(\bar{i}_d - \bar{i}_b - \bar{i}_s\right)\right] d_a \\
\bar{v}_d = \bar{v}_{cd} + R_{cd}\left(\bar{i}_d - \bar{i}_b - \bar{i}_s d_a\right)
\end{cases}
\tag{4.6}
$$

$$
\begin{cases}
L_s \dfrac{d\bar{i}_s}{dt} = -\bar{v}_s + \bar{v}_a - \left[\bar{v}_{cd} + R_{cd}\left(\bar{i}_d - \bar{i}_a + \bar{i}_s\right)\right] d_b \\
C_d \dfrac{d\bar{v}_{cd}}{dt} = \bar{i}_d - \bar{i}_a + \bar{i}_s d_b \\
\bar{i}_b = -\bar{i}_s d_b \\
\bar{v}_b = \left[\bar{v}_{cd} + R_{cd}\left(\bar{i}_d - \bar{i}_a + \bar{i}_s\right)\right] d_b \\
\bar{v}_d = \bar{v}_{cd} + R_{cd}\left(\bar{i}_d - \bar{i}_a + \bar{i}_s d_b\right)
\end{cases}
\tag{4.7}
$$

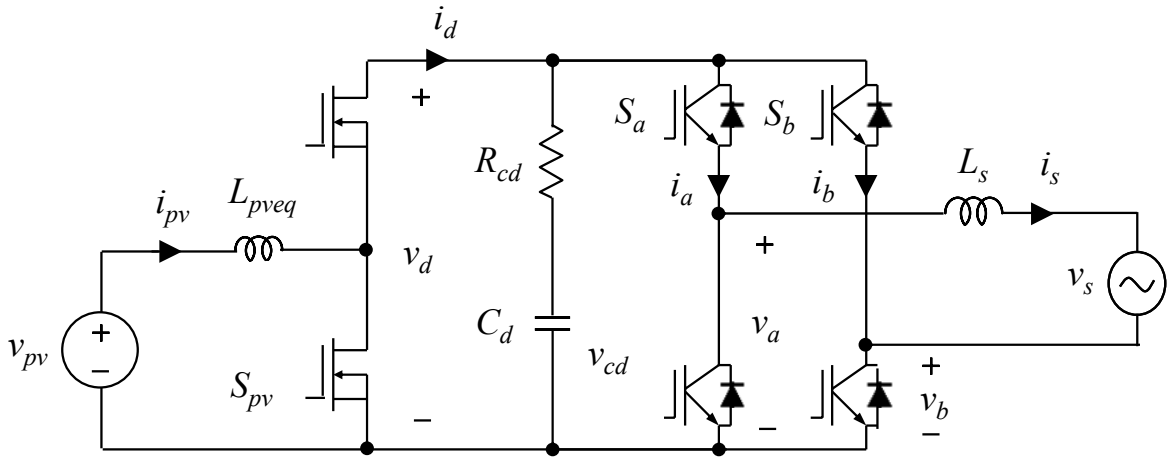
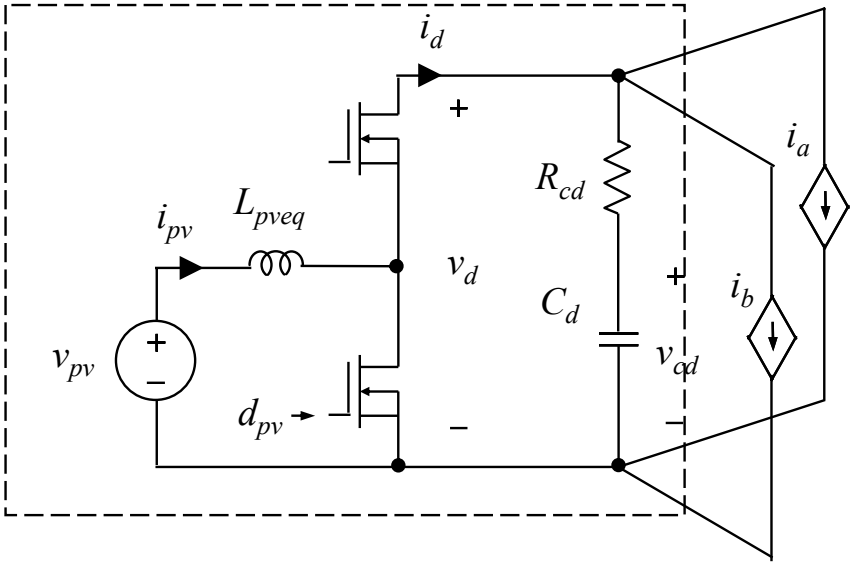
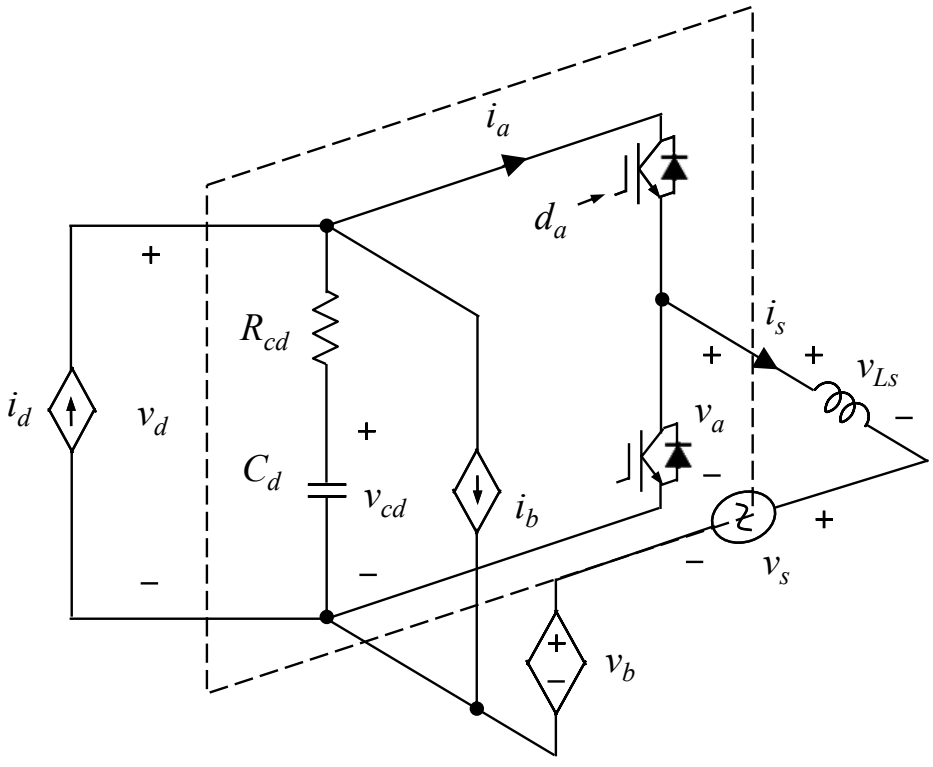


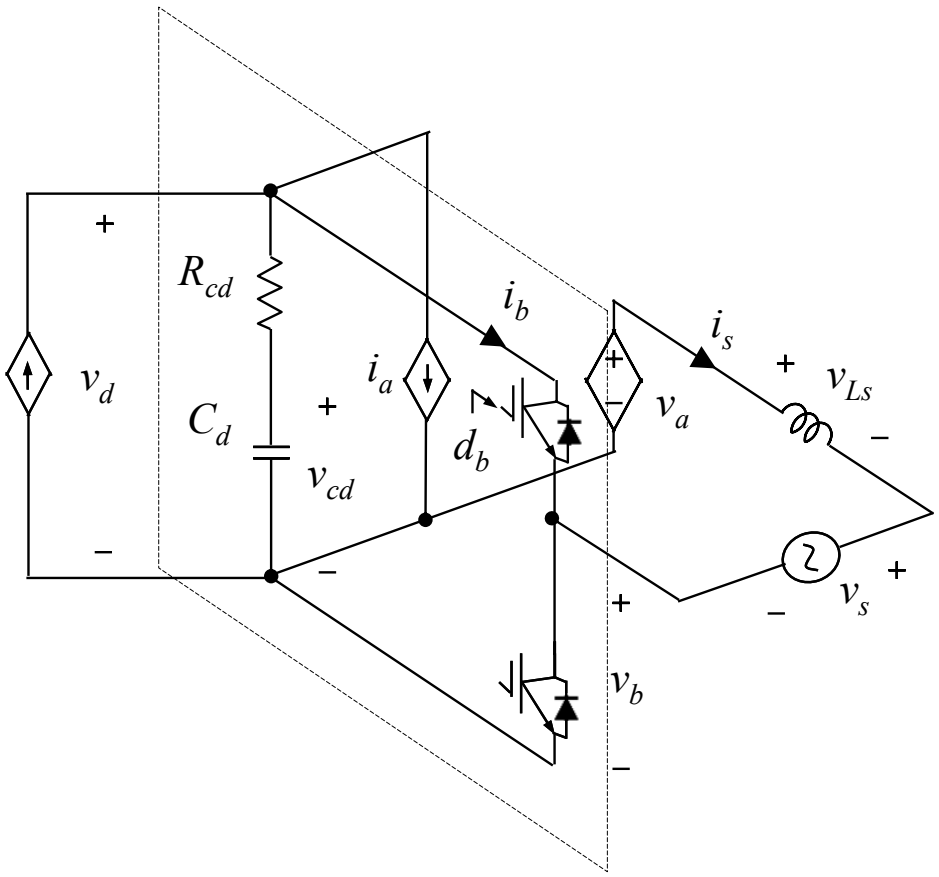
Figure 4.7 Equivalent circuit model of photovoltaic single-phase grid-connected power system.


i_d
+
i_a
R_{cd}
i_{pv}
L_{pveq}
v_d
C_d
+
i_b
v_{pv}
+
–
v_{cd}
d_{pv}
–
–

(a)


i_a
d_a
+
R_{cd}
i_s
+
+
v_{Ls}
i_d
v_d
+
v_a
–
C_d
v_{cd}
i_b
–
+
–
v_s
+
–
v_b

(b)



(c)

Figure 4.8 Three subsets of converter of photovoltaic single-phase grid-connected power system; (a) first-subset, (b) second-subset, and (c) third-subset converter with current sourcing.

The large-signal averaged equations are derived by aggregating the state-space averaging equations of (4.5)-(4.7). Assuming that the unipolar PWM scheme is in use for the second-stage inverter, the resultant equations of the state-space representative are shown in (4.8) and (4.9). The corresponding large-signal equivalent circuit model is shown in Figure 4.9, where d_a^p is defined as (1 - d_g) and d_{ab} is defined as (d_a - d_b). Note that the unipolar PWM scheme always satisfies (d_a + d_b) = 0.

$$\frac{d}{dt}\begin{bmatrix} i_{pv} \\ i_s \\ v_{cd} \end{bmatrix} = \begin{bmatrix} -\frac{R_{cd} d_g{}^p}{L_{pveq}} & \frac{R_{cd} d_g{}^p d_{ab}}{L_{pveq}} & -\frac{d_g{}^p}{L_{pveq}} \\ \frac{R_{cd} d_g{}^p d_{ab}}{L_s} & -\frac{1}{2}\frac{R_{cd}\left(1+d_{ab}{}^2\right)}{L_s} & \frac{d_{ab}}{L_s} \\ \frac{d_g{}^p}{C_d} & -\frac{d_{ab}}{C_d} & 0 \end{bmatrix} \begin{bmatrix} i_{pv} \\ i_s \\ v_{cd} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{pveq}} & 0 \\ 0 & -\frac{1}{L_s} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{pv} \\ v_s \end{bmatrix} \quad (4.8)$$

$$v_d = \begin{bmatrix} R_{cd} d_g{}^p & -R_{cd} d_{ab} & 1 \end{bmatrix} \begin{bmatrix} i_{pv} \\ i_s \\ v_{cd} \end{bmatrix} \quad (4.9)$$

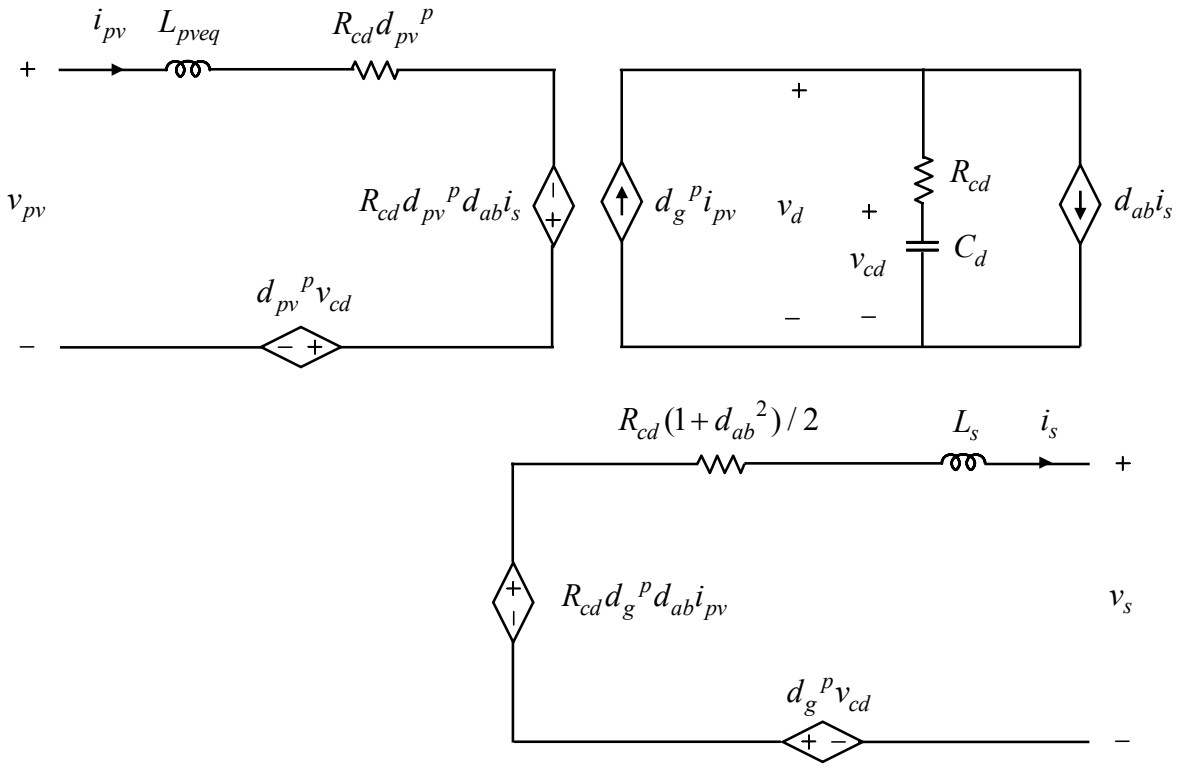


Figure 4.9 Large-signal equivalent circuit model of photovoltaic single-phase grid-connected power system.

4.3.2 Quasi-static analysis and small-signal averaged equation

Deriving small-signal averaged equations in the aggregated modeling approach requires the assumption that the system operates in the equilibrium point, in which all variables in the large-signal averaged equations can be expressed as quiescent values and small ac variables. This is shown in (2.27)-(2.30). However, this assumption can not be applicable to (4.8) and (4.9) anymore. The i_s and v_s are the sinusoidal waveforms oscillated with the fundamental frequency of the utility grid (50 or 60Hz), and thus the equilibrium point does not exist.

This fundamental difficulty can be overcome by using quasi-steady analysis. In this analysis, the i_s and v_s are assumed to oscillate at relatively slow speed when compared to dynamics of system and small ac variations. Under this assumption, their sinusoidal steady-state operation point is considered as the sequence of the several "quasi" equilibrium points (even if changed slowly and successively). Therefore, large-signal averaged equations can be linearized by using the conventional small-signal techniques at these quasi-equilibrium points along with their steady-state operation point. This results in several sets of small-signal averaged equations being valid around the corresponding steady-state operation point. The quasi-steady analysis generalizes the aggregated modeling approach for all kinds of the two-stage power converters, regardless of the form of electricity (alternating current or direct current).

The first step of the quasi-steady analysis is to obtain the steady-state operations. These present the quasi-equilibrium points. Assume that the power converter draws the dc voltage and dc current from the photovoltaic and transmits a nearly sinusoidal current into the utility grid in phase with the grid voltage. The steady state operations are expressed as

(4.10)-(4.13), where V_{pv} and I_{pv} represent dc voltage and current of the photovoltaic side, V_s and I_s represent rms voltage and current of utility side, and ω represents the fundamental frequency of the utility grid. For the steady-state operation, power between the input and output side is balanced with the assumption that the power converter has zero losses.

$$v_{pv} = V_{pv} \tag{4.10}$$

$$i_{pv} = I_{pv} \tag{4.11}$$

$$v_s = \sqrt{2}V_s \cos(\omega t) \tag{4.12}$$

$$i_s = \sqrt{2}I_s \cos(\omega t) \tag{4.13}$$

Substituting (4.10)-(4.13) into (4.8), the first-order simultaneous nonlinear equations are obtained as follows:

$$0 = -R_{cd} d_g{}^p I_{pv} + R_{cd}\left(1 - d_g{}^p\right) d_{ab}\sqrt{2}I_s \cos(\omega t) - d_g{}^p v_{cd} + V_{pv} \tag{4.14}$$

$$-\omega L_s \sqrt{2} I_s \sin \omega t = R_{cd}\left(d_g - 1\right) d_{ab} I_{pv} - \frac{1}{2} R_{cd} d_{ab}{}^2 \sqrt{2} I_s \cos \omega t + d_{ab} v_{cd} - \sqrt{2} V_s \cos \omega t \tag{4.15}$$

$$C_d \frac{dv_{cd}(t)}{dt} = d_g{}^p I_{pv} - d_{ab}\sqrt{2}I_s \cos \omega t \tag{4.16}$$

These equations are not solved analytically. Due to this factor, it is possible to use numerical methods, such as Euler method, Newton-Raphson method, Runge-Kutta method, with approximation to the solution. However, it is somewhat time-consuming. Neglecting the equivalent series resistance of the dc link capacitor under assuming it has an insignificant impact on the steady-state operation, these equations are represented as (4.17)-(4.19).

$$0 = -d_g{}^p v_{cd} + V_{pv} \tag{4.17}$$

$$-\omega L_s \sqrt{2} I_s \sin \omega t = d_{ab} v_{cd} - \sqrt{2} V_s \cos \omega t \tag{4.18}$$

$$C_d \frac{dv_{cd}(t)}{dt} = d_g{}^p I_{pv} - d_{ab} \sqrt{2} I_s \cos \omega t \tag{4.19}$$

Substituting (4.17) and (4.18) into (4.19) for d_g^p and d_{ab}, the dc link capacitor expression (4.19) can be written in an explicit representation known as the Bernoulli differential equation. This can be solved analytically. The resulting solutions are given as,

$$v_{cd}(t) = \sqrt{\frac{VA_o}{\omega C_d}\left(\cos\varphi - \cos\left(2\omega t - \varphi\right)\right) + V_{cd}{}^2} \tag{4.20}$$

$$d_g{}^p(t) = \frac{V_{pv}}{v_{cd}(t)} \tag{4.21}$$

$$d_{ab}(t) = -\frac{\sqrt{2} \cdot V_o}{v_{cd}(t)} \sin\left(\omega t - \varphi\right) \tag{4.22}$$

All the symbols in (4.20) - (4.22) are defined as follows;

VA_o Apparent converter power; $\sqrt{\left(V_s I_s\right)^2 + \left(\omega L_s I_s \cdot I_s\right)^2}$

φ Phase between converter voltage and current; $\tan^{-1}\left(\frac{V_s}{\omega L_s I_s}\right)$

V_o Output voltage of converter; $\sqrt{V_s^2 + \left(\omega L_s I_s\right)^2}$

The time-domain simulation, using the Saber Designer, is performed to verify the steady-state solutions, which is shown in Figure 4.10. The equivalent circuit model shown in Figure 4.7 is employed with the following parameters as: V_{pv} —50V, I_{pv} — 10A, V_{dc} — 200V, L_{pveq} — 45uH, C_d — 1100uF, L_s — 2mH, V_s — 100V, and I_s — 5A. Figure 4.10 illustrates the simulated converter waveforms for the following: the converter input voltage (v_{pv}) and current (i_{pv}), the dc link voltage (v_d), and the output voltage (v_s) and current (i_s) when the duty cycles (d_g) and (d_{ab}) are changed along with (4.21) and (4.22).

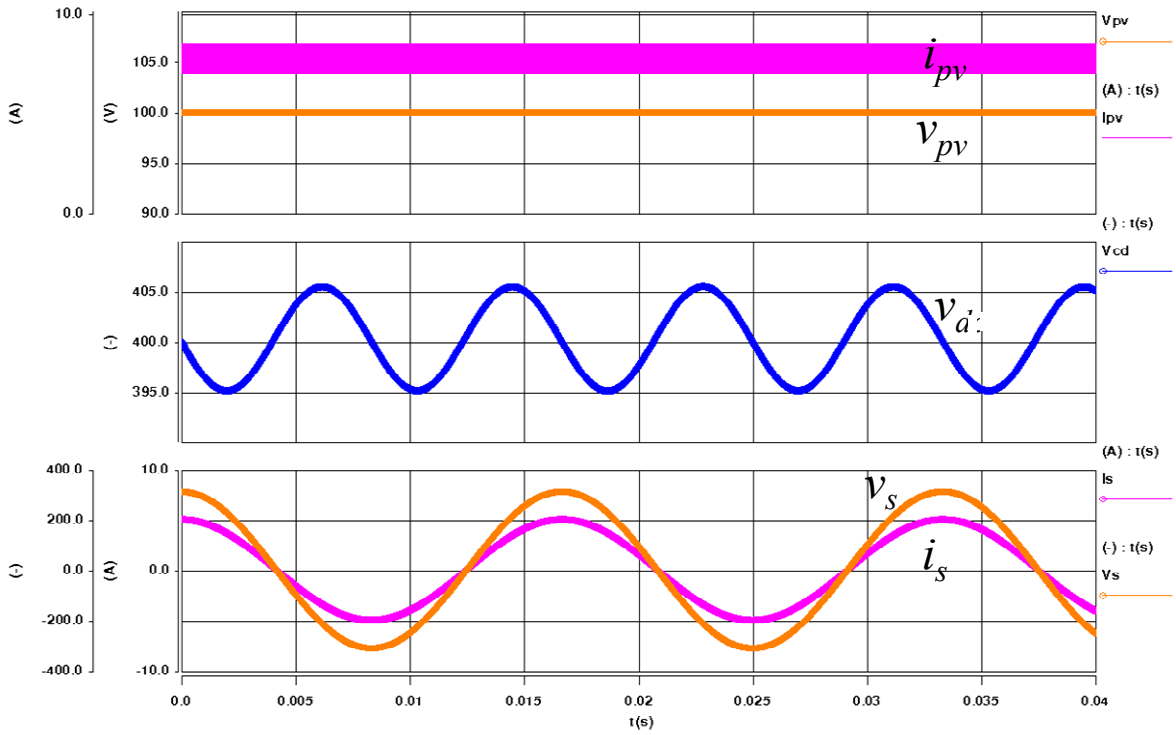


Figure 4.10 Simulated sinusoidal steady-state solution under single-phase grid-connection.

The simulated waveforms show that the input side operates in the dc electricity, while the output has nearly sinusoidal ac current in phase with the grid voltage. In the dc link voltage, a sinusoidal ac component with double the fundamental frequency is observed just as expected in (4.20). These waveforms support the effectiveness of the analytical steady-state solutions very well.

Deriving small-signal averaged equations along with the steady-state solutions (often called the quasi-equilibrium points), follows the exact approach of the conventional small-signal technique discussed in Chapter 2. The state variables (i_{pv}, i_s, and v_{cd}), input variables (v_{pv} and v_s), output variables (v_d), and duty ratios (d_{pv} and d_s) are decomposed into the quiescent values and small ac variation once again, where the quiescent values will be replaced by the steady-state solutions obtained above.

$$\begin{bmatrix} i_{pv} \\ i_s \\ v_{cd} \end{bmatrix} = \begin{bmatrix} I_{pv} \\ I_s \\ V_{cd} \end{bmatrix} + \begin{bmatrix} \hat{i}_{pv} \\ \hat{i}_s \\ \hat{v}_{cd} \end{bmatrix} \tag{4.23}$$

$$\begin{bmatrix} v_{pv} \\ v_s \end{bmatrix} = \begin{bmatrix} V_{pv} \\ V_s \end{bmatrix} + \begin{bmatrix} \hat{v}_{pv} \\ \hat{v}_s \end{bmatrix} \tag{4.24}$$

$$v_d = V_d + \hat{v}_d \tag{4.25}$$

$$\begin{bmatrix} d_{pv} \\ d_s \end{bmatrix} = \begin{bmatrix} D_{pv} \\ D_s \end{bmatrix} + \begin{bmatrix} \hat{d}_{pv} \\ \hat{d}_s \end{bmatrix} \tag{4.26}$$

Substituting (4.23)-(4.26) into (4.8) and (4.9) and retaining only the linear terms gives the small-signal equations as (4.27) and (4.28). Its corresponding small-signal equivalent circuit models are illustrated in Figure 4.11.

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{pv}\\ \hat{i}_{s}\\ \hat{v}_{cd}\end{bmatrix}=\boldsymbol{A}\begin{bmatrix}\hat{i}_{pv}\\ \hat{i}_{s}\\ \hat{v}_{cd}\end{bmatrix}+\boldsymbol{B}\begin{bmatrix}\hat{v}_{pv}\\ \hat{v}_{s}\end{bmatrix}+\boldsymbol{C}\begin{bmatrix}\hat{d}_{g}\\ \hat{d}_{ab}\end{bmatrix} \tag{4.27}$$

$$\boldsymbol{A}=\begin{bmatrix}-\frac{R_{cd}D_g{}^{p}}{L_{pveq}} & \frac{R_{cd}D_g{}^{p}D_{ab}}{L_{pveq}} & -\frac{D_g{}^{p}}{L_{pveq}}\\ \frac{R_{cd}D_g{}^{p}D_{ab}}{L_s} & -\frac{1}{2}\frac{R_{cd}\left(1+D_{ab}{}^{2}\right)}{L_s} & \frac{D_{ab}}{L_s}\\ \frac{D_g{}^{p}}{C_d} & -\frac{D_{ab}}{C_d} & 0\end{bmatrix}$$

$$\boldsymbol{B}=\begin{bmatrix}\frac{1}{L_{pveq}} & 0\\ 0 & -\frac{1}{L_s}\\ 0 & 0\end{bmatrix}$$

$$\boldsymbol{C} = \begin{bmatrix} \dfrac{R_{cd}(I_{pv} - I_s D_{ab}) + V_{cd}}{L_{pveq}} & \dfrac{R_{cd} I_s D_g{}^p}{L_{pveq}} \\ -\dfrac{R_{cd} I_{pv} D_{ab}}{L_s} & \dfrac{R_{cd}(I_{pv} D_g{}^p - I_s D_{ab}) + V_{cd}}{L_s} \\ -\dfrac{I_{pv}}{C_d} & -\dfrac{I_s}{C_d} \end{bmatrix}$$

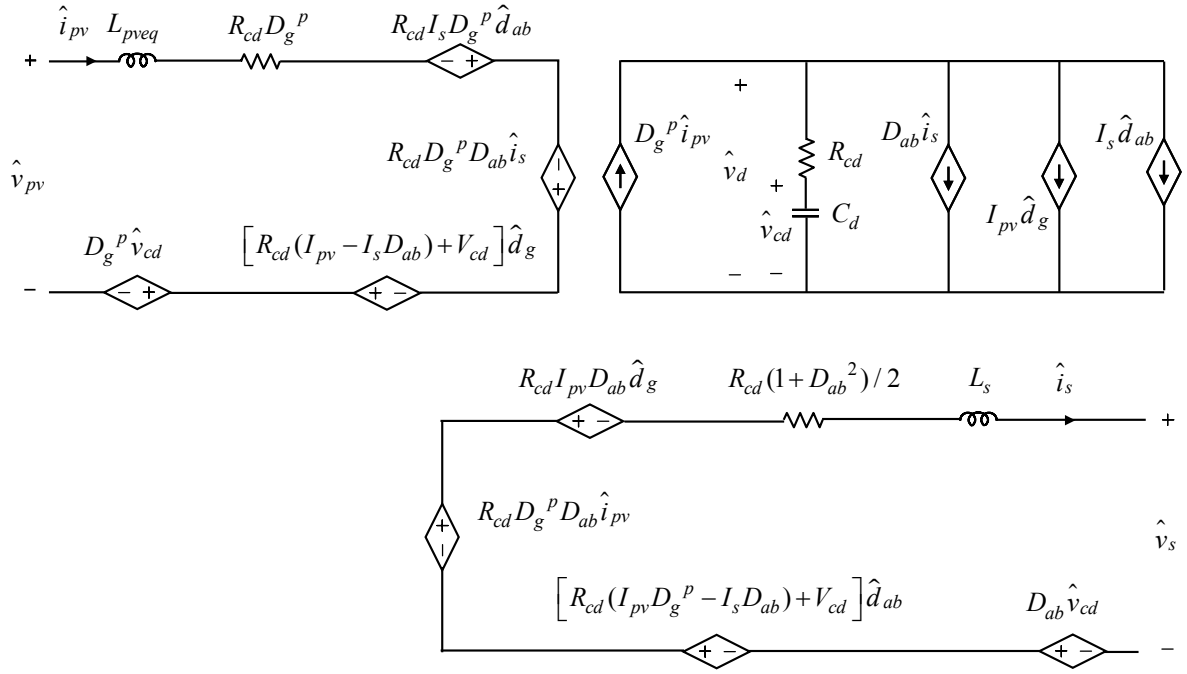


Figure 4.11 Small-signal equivalent circuit model of photovoltaic single-phase grid-connected power system.

$$\hat{v}_d = \begin{bmatrix} R_{cd}D_g{}^p & -R_{cd}D_{ab} & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{pv} \\ \hat{i}_s \\ \hat{v}_{cd} \end{bmatrix} + \begin{bmatrix} -R_{cd}I_{pv} & -R_{cd}I_s \end{bmatrix} \begin{bmatrix} \hat{d}_g \\ \hat{d}_{ab} \end{bmatrix} \tag{4.28}$$

Finally, the continuous-time expressions of small-signal averaged equations, which move along with their steady-state operation point, are derived by substituting the steady-state solutions of (4.20)-(4.22) into the quiescent values V_{cd}, $D_g{}^p$, and D_{ab} of (4.27) and (4.28). From the resulting expressions, the major control-to-output transfer functions are also obtained as shown in (4.29)-(4.31). The transfer functions are presented as a third-order dynamics with one real pole and one pair of complex conjugate poles. Note that the sign of the G_{vsd} is dependant on the polarity of the utility grid voltage v_s.

$$G_{ipv}(s) = \frac{\hat{i}_{pv}}{\hat{d}_{pv}} = K_{idpv} \cdot \frac{\left(1 + s / z_{idpv1}\right) \cdot \left(1 + s / z_{idpv1}{}^*\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2{}^*\right)} \tag{4.29}$$

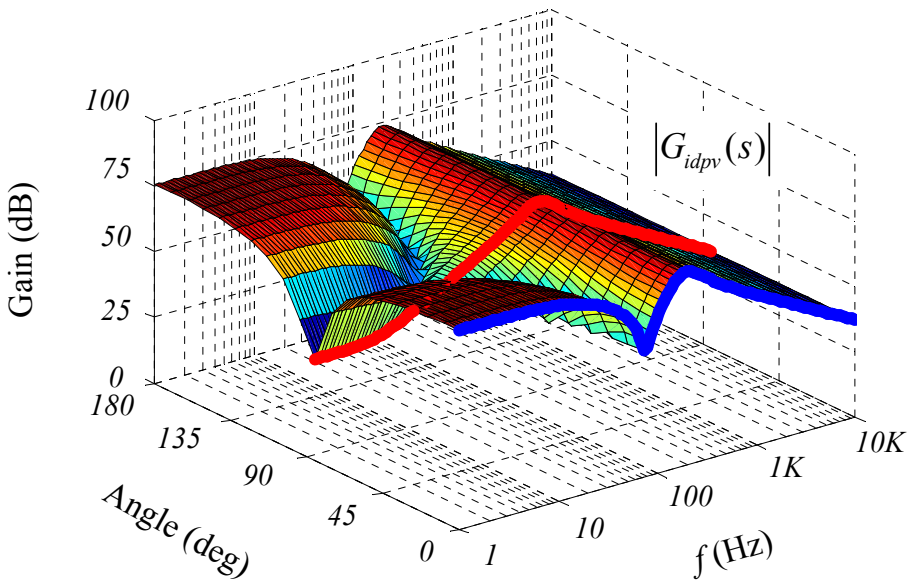
$$G_{is}(s) = \frac{\hat{i}_s}{\hat{d}_s} = K_{ids} \cdot \frac{\left(1 + s / z_{ids1}\right) \cdot \left(1 + s / z_{ids1}{}^*\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2{}^*\right)} \tag{4.30}$$

$$G_{vs}(s) = \frac{\hat{v}_d}{\hat{d}_s} = K_{vds} \cdot \frac{\left(1 + s / z_{vds1}\right) \cdot \left(1 + s / z_{vds2}\right) \cdot \left(1 + s / z_{vds3}\right)}{\left(1 + s / p_1\right) \cdot \left(1 + s / p_2\right) \cdot \left(1 + s / p_2{}^*\right)} \tag{4.31}$$

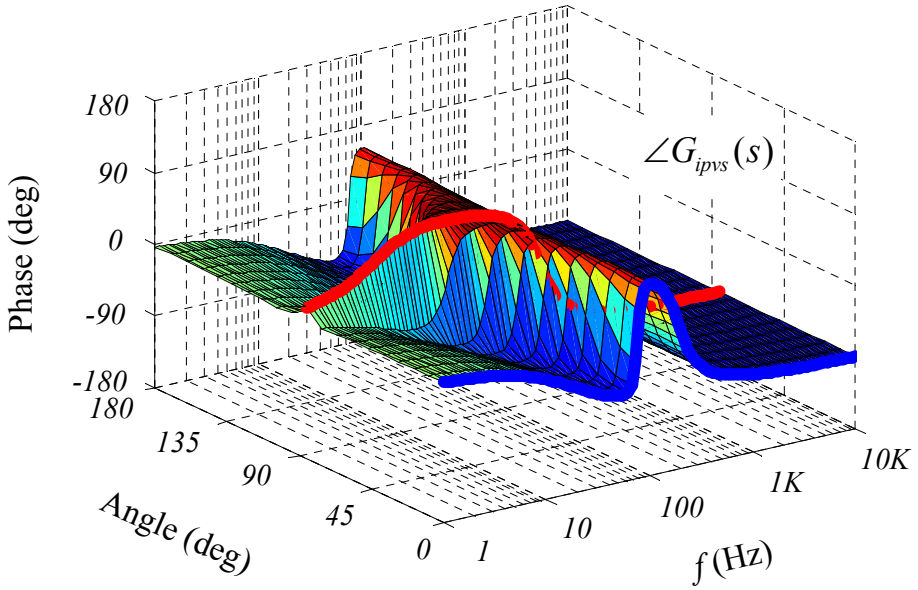
$$\text{where} \begin{cases} k_{vds} < 0 & \text{when } v_s > 0 \\ k_{vds} > 0 & \text{when } v_s < 0 \end{cases}$$

The transfer functions of (4.29)-(4.31) are periodically changed as a function of phase angle in the grid voltage. Thus, the three dimensional Bode plots are obtained by using the Matlab®, as shown in Figure 4.12 - Figure 4.14. From there, we can see that the gain and phase of the G_{ipv} have dynamically changed along with the steady-state operation point, while the G_{is} and G_{vs} are not impacted much. The variation of the G_{ipv} aggravates the current loop design for the first-stage converter and needs to be confirmed by two boundary transfer functions in order to guarantee stability. These boundary transfer functions are observed at the phase angle of 0 degree and 90 degree, which are denoted as the thick solid lines of Figure 4.12.

Figure 4.14 (b) shows the phase plot of the G_{vs}, where the abrupt discontinuous transition is observed at 90 degree. This discontinuity results from the changed gain of the G_{vds} according to the polarity of the grid voltage (v_s), as expressed in (4.31). In order to secure stability, the gain of control loop also needs to be changed every transition, which is generally compensated by detecting the phase angle of the utility grid voltage (v_s).

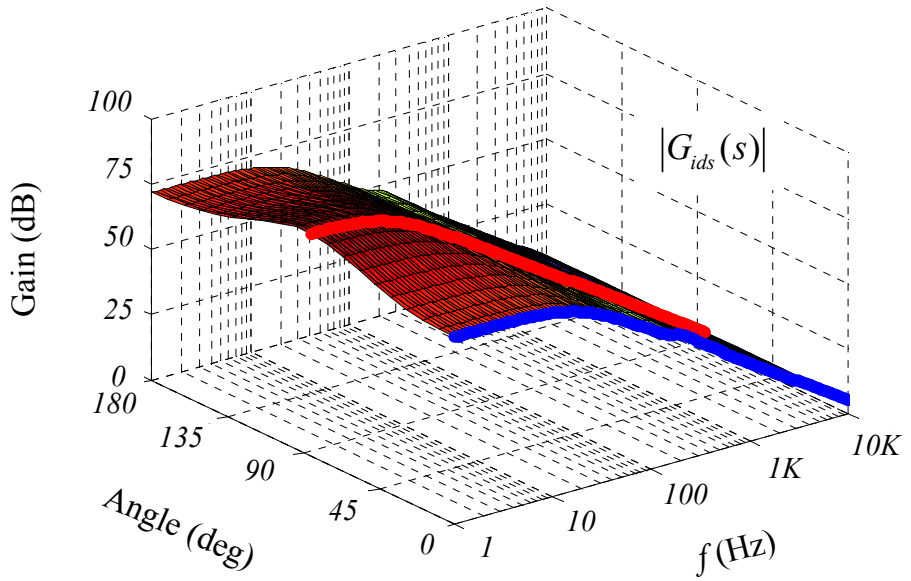


(a)

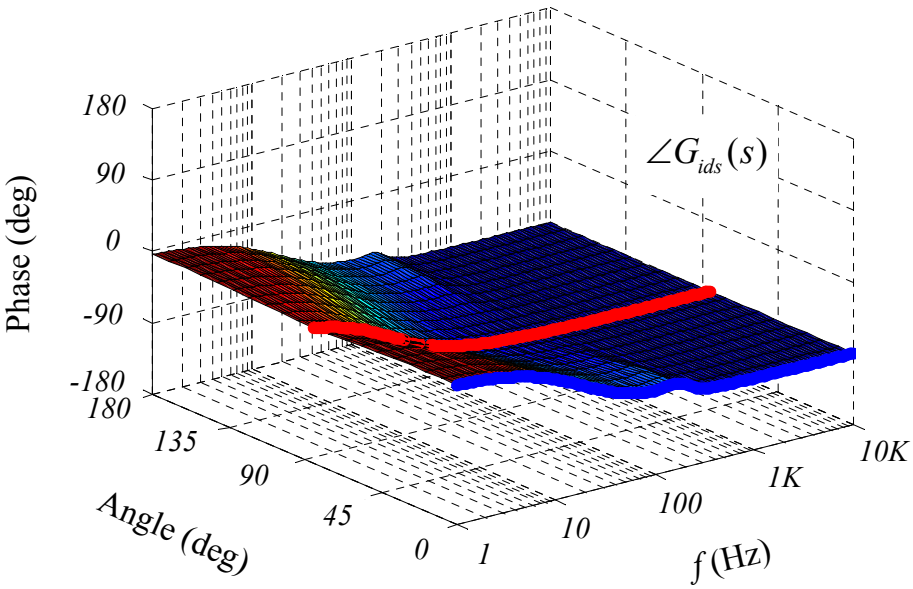


(b)

Figure 4.12 Control-to-current transfer function of first-stage converter; (a) gain and (b) phase plots.

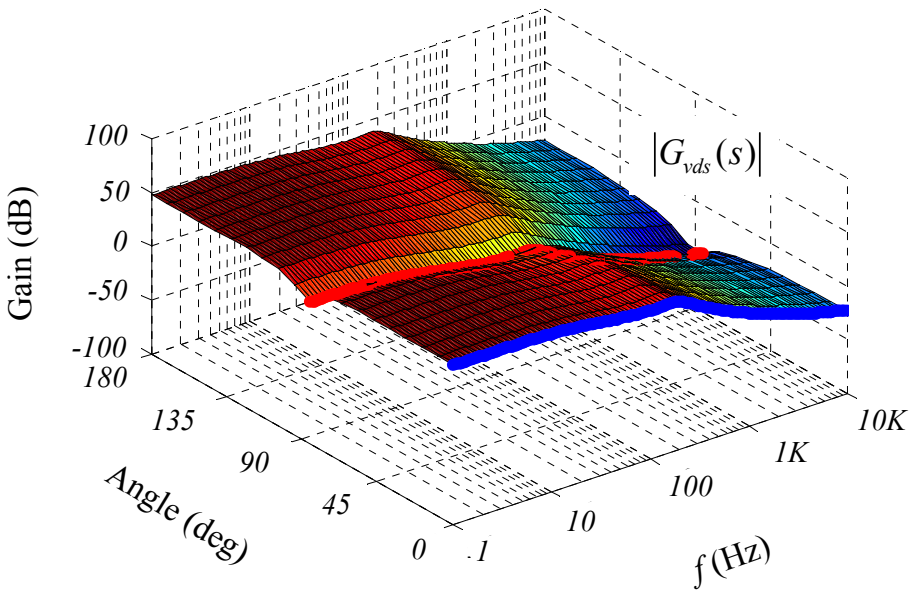


(a)

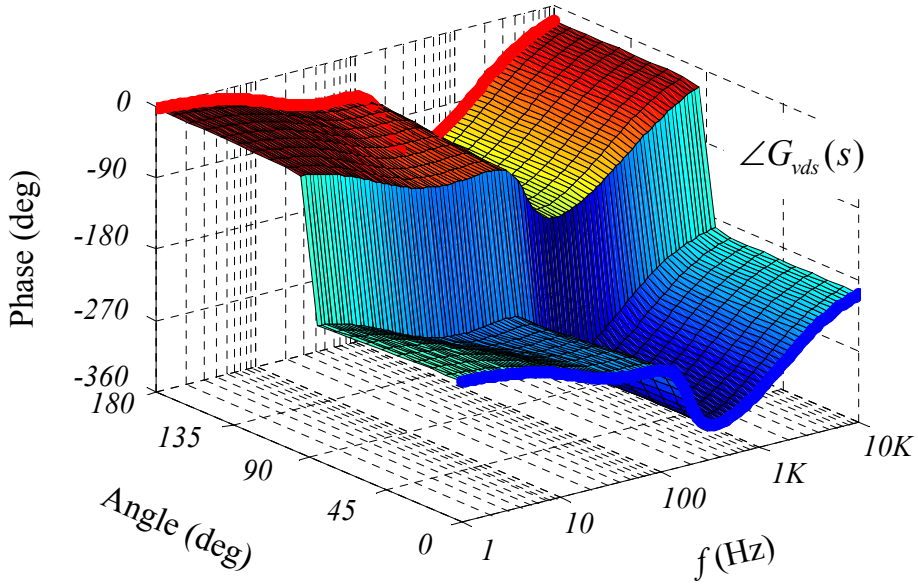


(b)

Figure 4.13 Control-to-current transfer function of second-stage converter; (a) gain and (b) phase plots.



(a)



(b)

Figure 4.14 Control-to-voltage transfer function of second-stage converter; (a) gain and (b) phase plots.

4.4 Novel active ripple compensation scheme and its control loop design

One of widely known issues for a single-phase grid-connected system is the instantaneous power pulsation with twice that of the utility grid frequency. As discussed in Chapter 1, the power pulsation is propagated to the upstream input side of the converter. It eventually draws the low frequency current ripple with same frequency of the power pulsation from the energy source. In particular, for the photovoltaic applications, this low frequency current ripple deteriorates the power harvest performance.

4.4.1 Impact of low frequency ac ripple on power harvest

The power harvest performance is impacted by the magnitude of the low frequency current ripple and depends on the input capacitor. Questions on this issue have arisen, including how much current ripple is allowable to achieve a reasonable power harvest performance, and how large of a capacitor is needed for it. These questions are easily investigated based on the low frequency ac model proposed in [83].

Figure 4.15 presents the simplified single-phase grid-connected system. The photovoltaic source is modeled by using a voltage source along with series impedance, in which the photovoltaic current consists of the dc current (I_{dcpv}) and low frequency ac ripple (I_{acpv}). The second-stage converter and the connected utility grid are represented by two output current sources, dc current (I_{dcout}) and low frequency ac ripple (I_{acout}). The input and dc link capacitors (C_{in}) and (C_{out}) are included to consider their impact on the (I_{acout}).

The switching phase of Figure 4.15 can be represented by an equivalent dc/dc transformer model with (d_{pv}^{p} : 1) turns ratio, where $d_{pv}^{p} = (1 - d_{pv})$. Figure 4.15, therefore, can be redrawn to Figure 4.16 by using the dc/dc transformer model, where the transformer primary side parameters are reflected to secondary side for easy calculations.

Now we assume that output current (i_s) is regulated in phase with the grid voltage (v_s) as,

$$v_s = \sqrt{2} V_{rms} \cos(\omega t) \tag{4.32}$$

$$i_s = \sqrt{2} I_{rms} \cos(\omega t) \tag{4.33}$$

Assuming the constant dc link voltage (V_{dc}), the output current sources (I_{dcout} and I_{acout}) are approximated as,

$$I_{dcout} \approx \frac{V_{rms} I_{rms}}{V_{dc}} \tag{4.34}$$

$$I_{acout} \approx \frac{V_{rms} I_{rms}}{V_{dc}} \cos(2\omega t) \tag{4.35}$$

By using the linear circuit superposition, Figure 4.16 is decomposed into the dc signal and ac signal equivalent circuits with the dc current (I_{dcpv}) and low frequency ac ripple (I_{acpv}), which are illustrated in Figure 4.17. The circuit analysis of Figure 4.17 gives the following equations,

$$I_{dcpv} = \frac{V_{rms} I_{rms}}{d_{pv}{}^{p} V_{dc}} \tag{4.36}$$

$$I_{acpv} = \frac{d_{pv}{}^{p} V_{rms} I_{rms} \cos(2\omega t)}{V_{dc}\left[d_{pv}{}^{p2} + s(C_{in} d_{pv}{}^{p2} + C_d) z_s + s^2 C_d L_s + s^3 C_{in} C_d L_{pveq} R_s \right]} \tag{4.37}$$

Since the low frequency ac ripple (I_{acpv}) has no contribution for real power delivery, the power harvest performance of the power system is simply gauged by the utilization ratio (K_{pv}), defined as (4.38), where I_{pvmag} is maximum magnitude of current from the photovoltaic and $I_{acpvmag}$ is the magnitude of the low frequency ac ripple (I_{acpv}) of (4.37).

$$k_{pv} = \frac{I_{dcpv}}{I_{pvmag}} = \frac{I_{dcpv}}{I_{dcpv} + I_{acpvmag}} \tag{4.38}$$

Substituting (4.36) and (4.37) into (4.38), the resultant expression is given as,

$$k_{pv} = \frac{{d_{pv}}^{p2} + s(C_{in}{d_{pv}}^{p2} + C_d)z_s + s^2 C_d L_s + s^3 C_{in} C_d L_{pveq} R_s}{2{d_{pv}}^{p2} + s(C_{in}{d_{pv}}^{p2} + C_d)z_s + s^2 C_d L_s + s^3 C_{in} C_d L_{pveq} R_s} \tag{4.39}$$

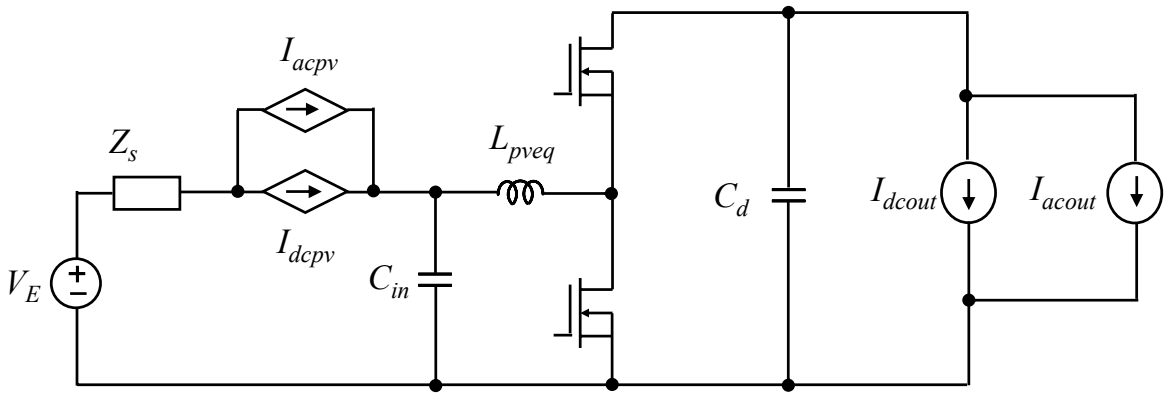


Figure 4.15 Simplified single-phase model with ac load.

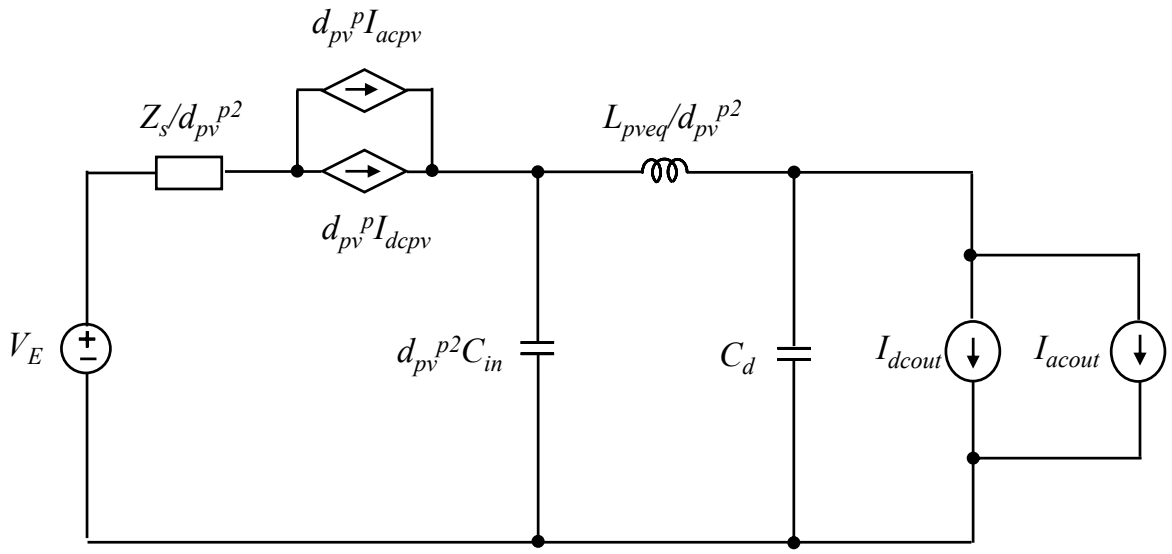
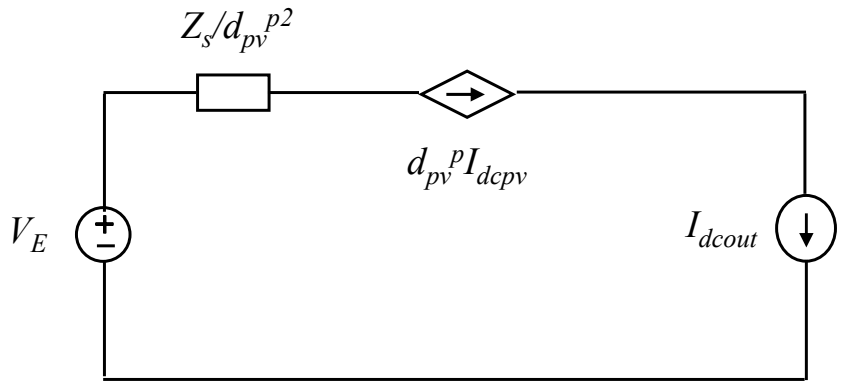
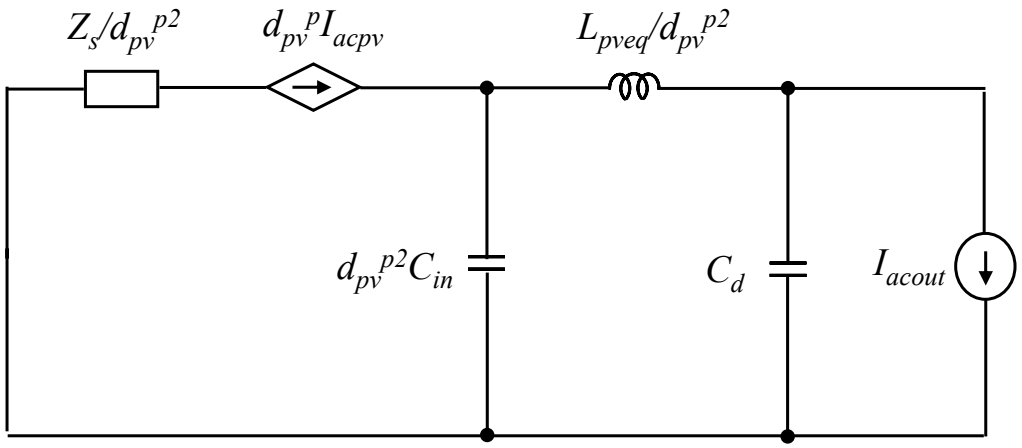


Figure 4.16 Simplified single-phase using equivalent dc/dc transformer model.



(a)



(b)

Figure 4.17 Equivalent single-phase circuit; (a) large-signal dc model and (b) small-signal ac model for converter.

From (4.38), we can see that the relationship between the utilization ratio (K_{pv}) and the low frequency ac ripple. Equation (4.39) describes the impact of the Z_s, C_{in}, and C_{out} on the utilization ratio (K_{pv}). Assuming no capacitors of the input and dc link at all, the calculation by (4.39), for example, results in the k_{pv} of 0.5, meaning that the delivered power to the utility grid is only 50% of total available power.

According to (4.38), the low frequency ac current ripple (I_{acpv}) should be below 2% of the dc current (I_{dcpv}), in order to reach a utilization ratio of 98%. Assuming the photovoltaic dc source impedance (Z_s) is 0.3Ω. Using the circuit parameters presented in section 4.3.2, V_{pv} —50V, V_{dc} — 400V L_{pveq} — 45uH, C_d — 1100uF, and L_s — 2mH, the required size of the input capacitor is given by (4.29). The result indicates that the input capacitor needs to be designed with the higher capacitance than 5000uH.

4.4.2 Active ripple compensation scheme based on generalized control structure

In prior scholarship, some active ripple compensation schemes have been proposed to attenuate the low frequency ac current ripple, mostly adapted in the conventional control structure [83]-[84], [87]. As an example, the scheme proposed for a phase-shift controlled dc-dc converter [83] is cited in the dissertation. Shown in Figure 4.18, this scheme uses two control loops; a voltage loop is served for the outer loop and a current loop for the inner loop. Here, the inner current loop is designed to have a fast dynamics to attenuate the current ripple, while the crossover frequency for the outer voltage loop is designed to be very low (2Hz is used to 120Hz ac current ripple attenuation). This is compared to the double-fundamental frequency, which permits the dc-link voltage ripple.

The inherent issue with this method is the slow transient response of the dc-link voltage, which causes large overshoot or undershoots during load transient. Apparently, this issue originates from inadequate feedback configurations of the conventional control structure, in which the voltage and current loop fight each other, and consequently a faster voltage loop hurts current loop performance. In this configuration, the current loop is driven by the voltage loop's output. Unless it is implemented with strong attenuation, the voltage loop is easily affected by its feedback signal of dc link voltage, which contains low frequency ripple components.

As a result, the current loop is regulated along with its reference contaminated by the low frequency ripple components. Consequently, the low frequency ripple can not be totally eliminated in the input current. It is the main reason to require a low bandwidth in the outer voltage loop. However, the generalized control structure doesn't suffer from this issue. Thus, it provides more favorable control platform to achieve relatively fast dynamic of the dc link voltage loop, while providing active ripple compensation.

Figure 4.19 shows a novel active ripple compensation scheme using the generalized control structure. In the first-stage converter loop, the current compensator (C_{ipv}) regulates the input current (i_{pv}) along with its reference (i_{pv}). The maximum power point tracking scheme can be implemented to determine the i_{pv} as needed. In the second-stage converter loop, the current compensator (C_{is}) regulates the output current (i_s) to follow its reference (i_s^*), which is obtained by multiplying the magnitude of the output current (i_{sm}) to the phase information of the grid voltage $cos(\omega t)$, which is detected by the phase-lock-loop (PLL). The voltage compensator (C_{vs}) regulates the dc link voltage (v_d) according to the given voltage command (v_d^*).

The input current is regulated by the first-stage converter loop, which is governed by the external reference. The dc link voltage is fed to the outer voltage loop of the second-stage converter. Eventually it determines the magnitude of the output current flowing into the connected utility grid. Such an independent control structure between the input current and dc link voltage helps to reduce the interference of low frequency ripple on the input current regulation, and to increase crossover frequency in the dc link voltage loop. However, the outer voltage loop still requires relatively low crossover frequency, in comparison to the double-fundamental frequency, in order to permit the dc-link voltage ac ripple. This low crossover frequency requirement is alleviated by introducing a quasi-notch filter. This will be detailed in the next section.

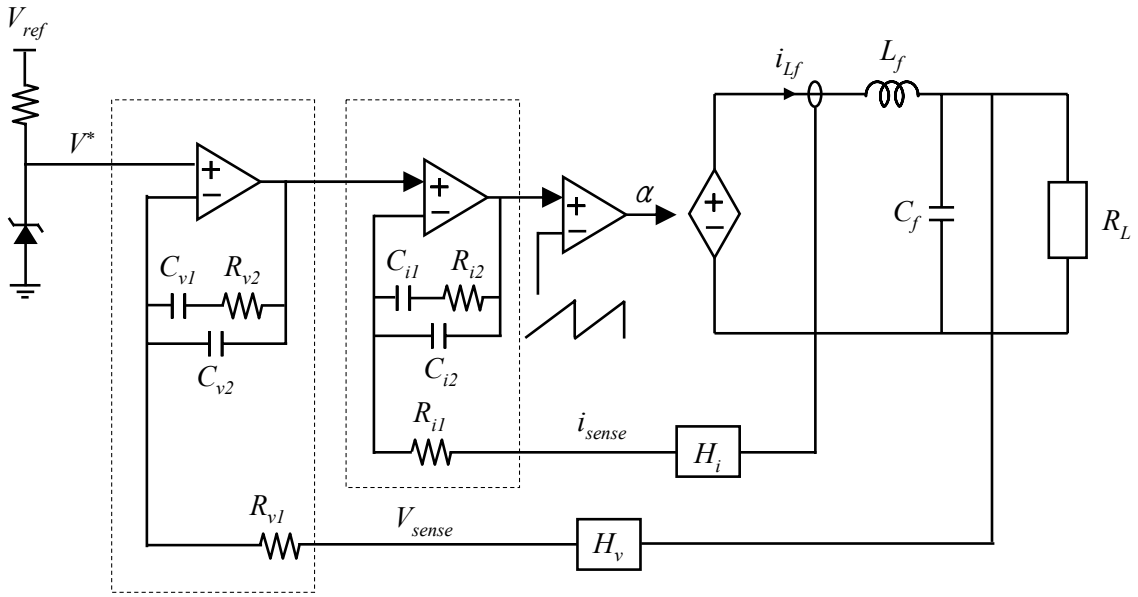


Figure 4.18 Active ripple current reduction scheme with two control loops.

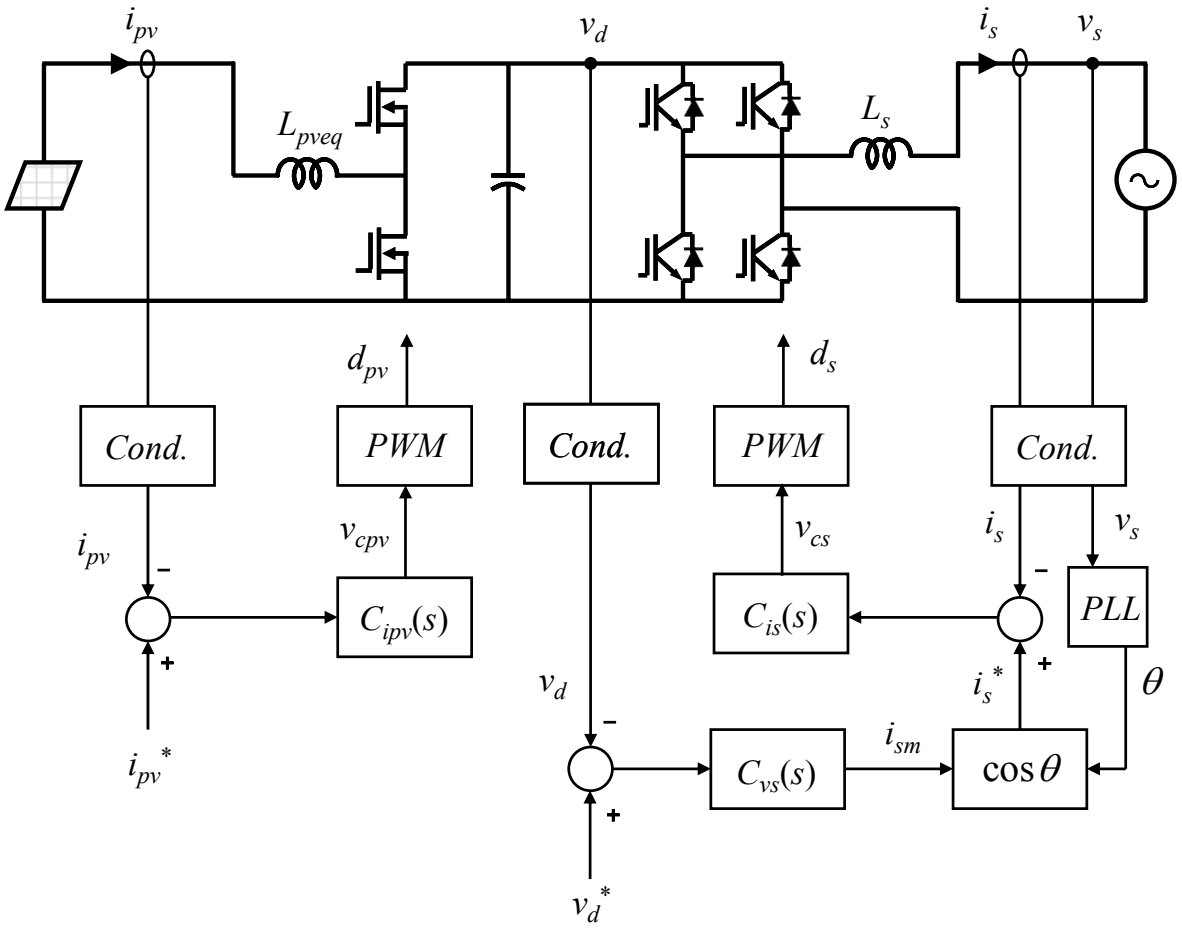


Figure 4.19 Novel active ripple compensation scheme based on generalized control structure.

4.4.3 Compensators design for novel ripple condensation scheme

In this section, the compensators shown in Figure 4.19 are designed, based on the frequency domain analysis. The circuit parameter values used for this compensator design, where two cases of load are picked up as light-load (50W) and heavy-load (500W) condition, are as follows:

$V_{pv} = 25 \sim 50\text{V}$ $V_d = 200\text{V}$ $V_s = 100\text{V}$

$L_{pveq} = 45\text{uH}$ $C_d = 1100\text{uF}$ $L_s = 2\text{mH}$

Figure 4.20 shows the closed-loop compensator diagram of the first-stage control loop, using transfer function blocks: G_{ipv} — duty-to-current transfer function, C_{ipv} — current loop compensator, H_{ipv} — current conditioning circuit transfer function, and F_{mpv} — PWM gain. In the figure, the current loop gain (T_{ipv}) is,

$$T_{ipv}(s) = C_{ipv}(s) \cdot F_{mpv} \cdot G_{ipv}(s) \cdot H_{ipv}(s) \tag{4.40}$$

The type 2, two-pole and one-zero compensator discussed in chapter 3 can satisfy the system performance requirement to regulate the input current. The compensator is written as (4.41).

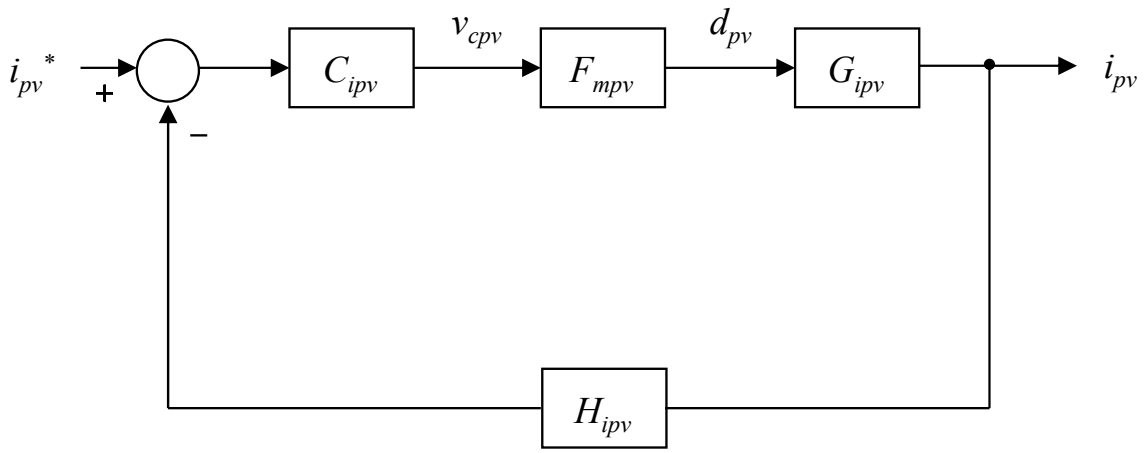


Figure 4.20 Block diagram of closed-loop control for first-stage converter.

$$C_{ipv}(s) = C_{ipv}(0) \cdot \frac{\left(1 + \frac{s}{2\pi f_{ipv,z}}\right)}{s \cdot \left(1 + \frac{s}{2\pi f_{ipv,p}}\right)} \tag{4.41}$$

Using the design procedure discussed in Chapter 3, the compensator is designed under low line-light load and high line-heavy load conditions. Note that the G_{ipv} is heavily dependant on the steady-state operation points, and thus compensator design needs to verify its stability by using boundary transfer function at 0 degree and 90 degree of the grid voltage angle. Figure 4.21 illustrates the gain/phase plots of the loop gain T_{ipv} with/without the compensator C_{ig} under boundary transfer points; 0 degree and 90 degree of grid voltage angle. The resultant design gives a phase margin of approximately 90° and gain margin of larger than 20dB. The crossover frequency is widely varied in the range of 300Hz ~ 3kHz. The designed compensator parameters include: $C_{ipv}(0)$ = 1630, $f_{ipv,z}$ = 55Hz, , and $f_{ipv,p}$ = 10kHz

The current control loop of the second-stage converter deals with the time-varying control variable of the output current. It is sinusoidal waveform oscillated with the fundamental frequency of the utility grid (50 or 60Hz). The PID type compensators, for this case, encounter difficulties in removing the steady-state error, because of a limited gain at the fundamental frequency. The proportional-resonant (PR) type compensator, as a promising alterative, has been proposed, and in the time since, has gained a large popularity [19]. The compensator provides high gain at the fundamental frequency, thus eliminating

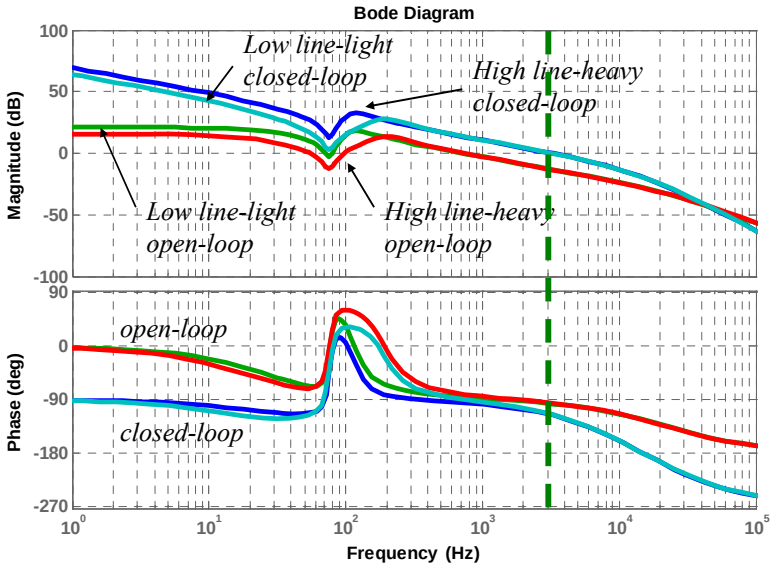
the steady-state error when the control variables are sinusoidal waveforms oscillated at the fundamental frequency. The transfer function of proportional-resonant compensator is defined as (4.42), where k_p is proportional gain, k_r is resonant gain, ω_c is equivalent bandwidth, and ω_o is resonant frequency of the resonant controller.

$$C_{PR}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_o{}^2} \tag{4.42}$$

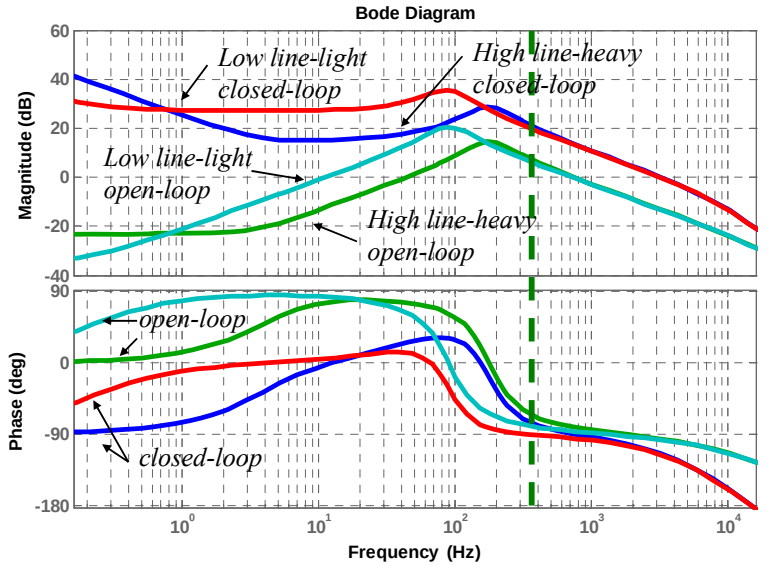
Figure 4.22 illustrates the second-stage closed-loop compensator diagram, where G_{is} — duty-to-current transfer function, G_{vdis} — current-to-link transfer function, C_{is} — inner current loop compensator, C_{vs} — outer dc link voltage compensator, H_{vs} — voltage conditioning circuit transfer function, H_{is} — current conditioning circuit transfer function, and F_{ms} — PWM gain.

The K_{cos} represents small-signal transfer function of $cos(\omega t)$ to determine the phase of output current i_s, as shown in Figure 4.19. From the fast small ac variations point of view, $cos(\omega t)$ moves very slowly. In other words, it is seen as a quasi-steady state value without any dynamics. Therefore, the K_{cos} can be treated as a simple unity gain block, but its sign is reversed whenever the polarity of the grid voltage (v_s) is changed.

$$k_{cos} = \begin{cases} 1 & \text{when } v_s > 0 \\ -1 & \text{when } v_s < 0 \end{cases} \tag{4.43}$$



(a)



(b)

Figure 4.21 Gain/phase plots of first-stage current loop gain with/without compensator under boundary transfer function at; (a) 0 degree and (b) 90 degree.

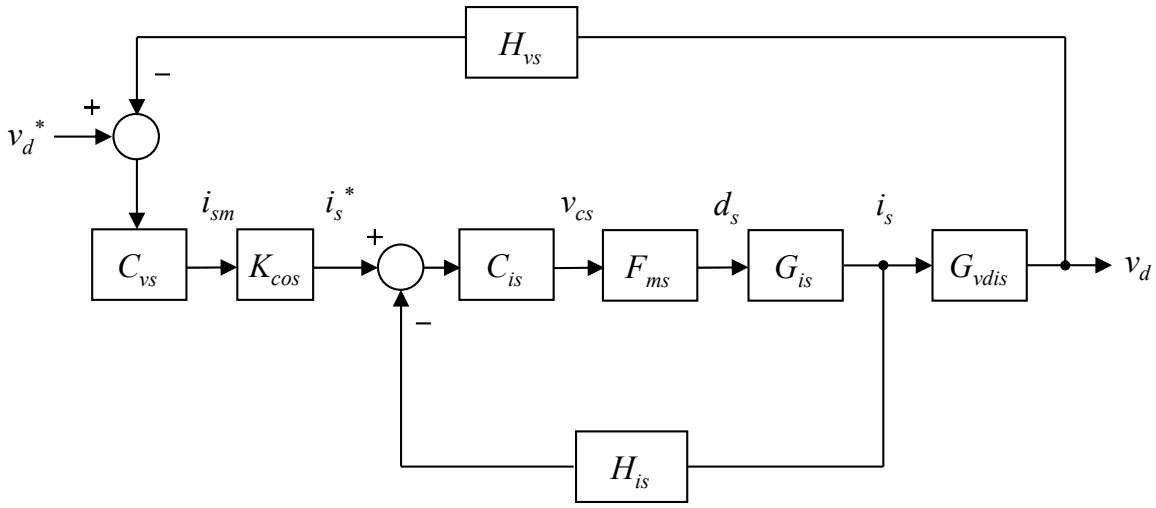


Figure 4.22 Block diagram of closed-loop control for second-stage converter.

The current-to-link transfer function (G_{vdis}) and the loop gain (T_{io}) are obtained as,

$$C_{vdis}(s) = \frac{\hat{v}_d}{\hat{i}_s} = \frac{\hat{v}_d}{\hat{d}_s} \cdot \frac{\hat{d}_s}{\hat{i}_s} = G_{vs}(s) \cdot \frac{1}{G_{is}(s)} \tag{4.44}$$

$$T_{is}(s) = C_{is}(s) \cdot F_{ms}(s) \cdot G_{is}(s) \cdot H_{is}(s) \tag{4.45}$$

The PR compensator is employed to regulate ac output current in the second-stage control loop, as written in (4.46) again.

$$C_{is}(s) = k_{pis} + \frac{2k_{ris}\omega_{cis}s}{s^2 + 2\omega_{cis}s + \omega_{ois}{}^2} \tag{4.46}$$

The compensator is carefully designed using the circuit parameter values in the beginning of the section. The compensator parameters are designed as: k_{pis} = 50, k_{ris} = 2000, ω_{cis} = 5 rad/sec, and ω_{ois} = 376.99 rad/sec. This design results in a phase margin of greater than 80° and gain margin of greater than 30dB, with cross-over frequency at 1kHz. Figure 4.23 illustrates the gain/phase plot of the loop gain (T_{is}) with/without the compensator (C_{is}), under low line-light load and high line-heavy load. The designed compensator is valid and very well matched with the design results.

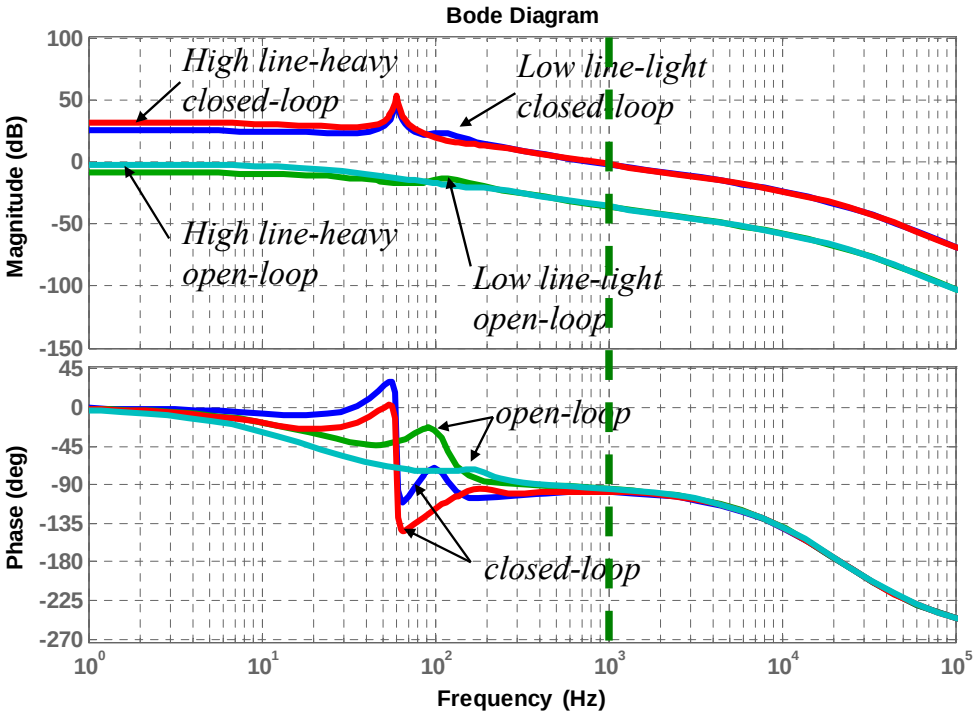


Figure 4.23 Gain/phase plots of second-stage current loop gain with/without the compensator.

From Figure 4.21, the loop gain of the outer loop (T_{vs}) can be written as (4.47), and the closed-loop transfer function of the inner current loop (T_{icl}) is given as (4.48).

$$T_{vs}(s) = C_{vs}(s) \cdot k_{cos} \cdot T_{iscl}(s) \cdot G_{vdis}(s) \cdot H_{vs}(s) \tag{4.47}$$

$$T_{iscl}(s) = \frac{\hat{i}_{is}}{\hat{i}_{is}^{*}} = \frac{1}{H_{is}(s)} \cdot \frac{T_{is}(s)}{1 + T_{is}(s)} \tag{4.48}$$

Similar to previous control loop designs, the outer voltage loop compensator employs a type 2, one-zero and two-pole compensator. For the purpose of ac ripple current reduction, however, the designed loop gain curve should be able to provide sufficient attenuation (suggested 20dB, but preferred more than 40dB) at the ac ripple frequency (120Hz in this application). The conventional approach for this is to design well-separated the crossover frequency from 120 Hz, at least a half decade of separation, at the expense of compensator dynamics. In practice, a 2Hz crossover frequency is reported to get 37dB attenuation at 120Hz [83].

In this research, as an alternative approach, a quasi-notch filter is proposed to provide sufficient attenuation without the sacrifice of dynamics. The quasi-notch filter is composed of one set of a resonant pole and one set of a resonant zero with different quality factor. Similar to a standard notch filter, the quasi-notch filter provides attenuation in a specific frequency range. However, its phase drop at the specific frequency is determined

by the strength of attenuation, while a standard notch filter shows a fixed phase drop of 90 degree at the band-reject frequency. This adjustable phase drop of the quasi-notch filter provides the flexibility compensator design, and thus, helps to increase the crossover frequency even beyond the ac ripple frequency as needed. The transfer function of the quasi-notch filter is defined as (4.49), where Q_z is the quality factor of the resonant zero, Q_p is the quality factor of the resonant pole, and ω_o is the resonant frequency of the quasi-notch filter. The attenuation level (Q) in dB is given as (4.50). By choosing Q_p = 10 with several Q_z, the frequency response of the quasi-notch filter is illustrated in Figure 4.24.

$$C_{QRF}(s) = \frac{s^2 + \frac{\omega_o}{Q_z} s + {\omega_o}^2}{s^2 + \frac{\omega_o}{Q_p} s + {\omega_o}^2} \tag{4.49}$$

$$\left|Q\right|_{dB} = \left|Q_p\right|_{dB} - \left|Q_z\right|_{dB} \tag{4.50}$$

The resulting compensator of the outer voltage loop compensator is composed of the type 2, one-zero and two-pole PID compensator and the quasi-notch filter, as shown in (4.51). A design example of voltage loop compensation would be given as: $C_{vs}(0)$ = -500, $f_{vs,z}$ = 30Hz, fvs,p = 480Hz, Q_z = 500, Q_p = 10, and ω_o = 753.98 rad/sec. Note that the C_{vs} requires no alternating gain, even if the plant (G_{vs}) shows reversed gain according to the polarity of the grid voltage (v_s). The K_{cos} inherently alternates its sign, as shown in (4.43). This alternating sign naturally compensates the reversed gain of the G_{vds}.

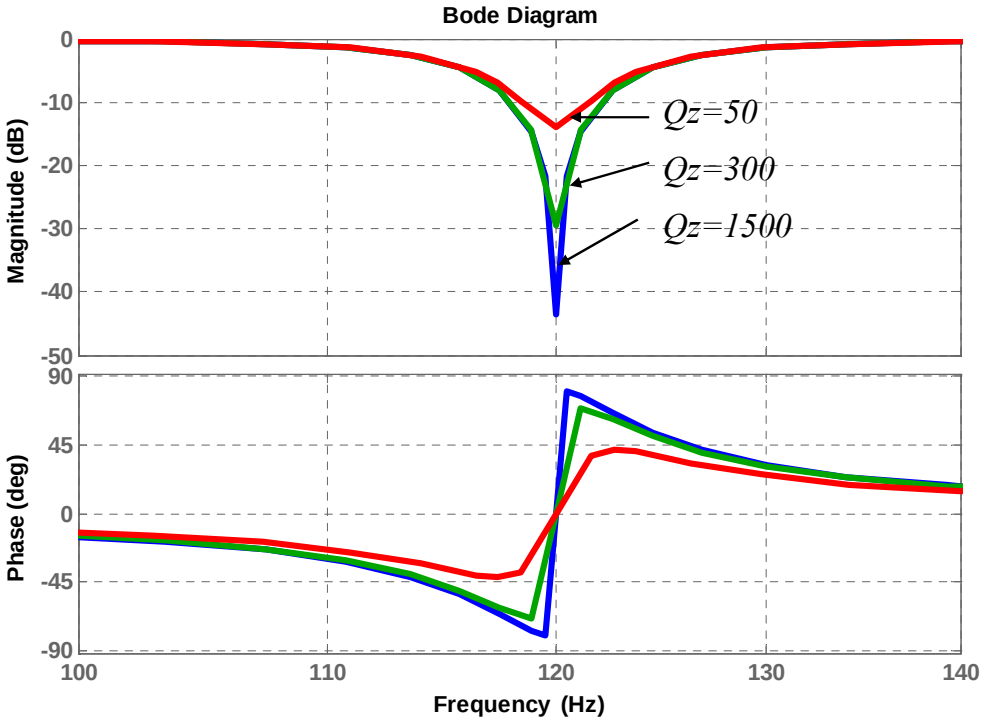


Figure 4.24 Gain/phase plots of quasi-notch filter under varying quality factor of resonant zero with fixed quality factor of resonant pole.

$$C_{vs}(s) = C_{vs}(0) \cdot \frac{\left(1 + \frac{s}{2\pi f_{vs,z}}\right)\left(s^2 + \frac{\omega_o}{Q_z}s + {\omega_o}^2\right)}{s \cdot \left(1 + \frac{s}{2\pi f_{vs,p}}\right)\left(s^2 + \frac{\omega_o}{Q_p}s + {\omega_o}^2\right)} \tag{4.51}$$

Figure 4.25 illustrates the resultant gain/phase plots of the loop gain (T_{vs}) with/without the compensator (C_{vs}) under low line-light load and high line-heavy load. We can clearly see the attenuation more than -20dB at the ac ripple frequency of 120Hz. The plots indicate a phase margin of approximated 50° and gain margin of larger than 15dB, with crossover frequency at 300 Hz. Based on the gain/phase plot of the loop gain (T_{vs}), the effectiveness of the quasi-notch filter is verified, having provided sufficient attenuation without expense of slow dynamics.

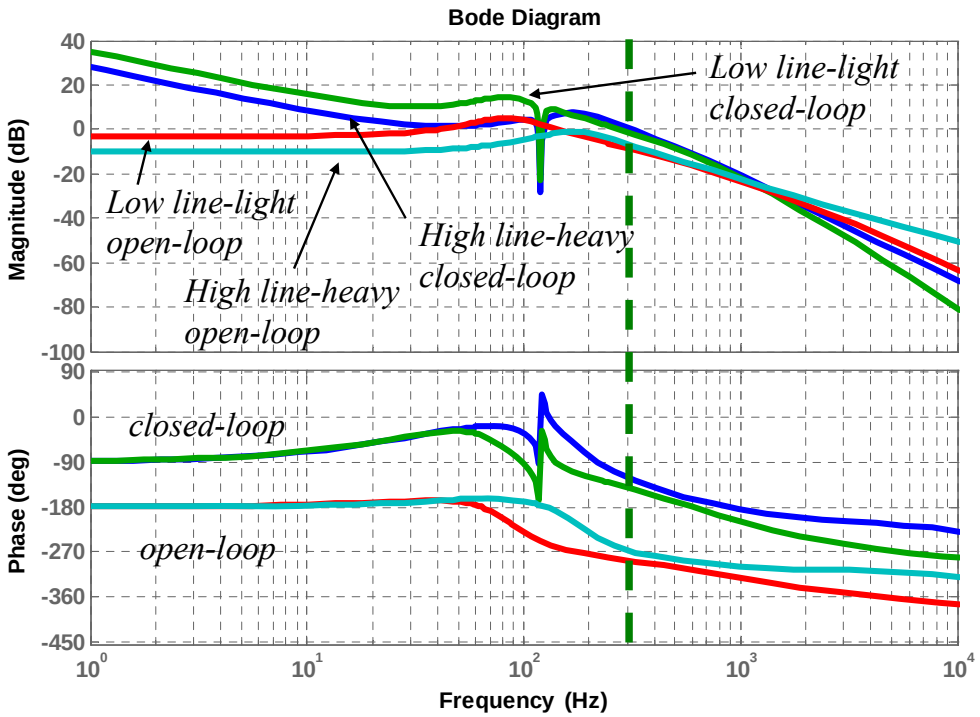


Figure 4.25 Gain/phase plots of second-stage voltage loop gain with/without compensator.

4.5 Performance evaluation of active ripple compensation scheme

4.5.1 Simulation verification

Figure 4.26 shows the simulation results based on the conventional control structure with very low crossover frequency of voltage control loop around 2 Hz. The current control loop is designed with 3kHz crossover frequency. As expected, the input current is regulated with almost dc current without ac ripple, while the dc link voltage exhibits 120Hz ac ripple components. However, during the load transient, the excessive voltage overshoot or undershoot (almost reaches to 100V) is observed in the dc link and illustrated in Figure 4.27.

Figure 4.28 shows the case of higher crossover frequency at 16 Hz. The small ac ripple component is observed in the input current, while dc link voltage exhibit 120Hz ac ripple components as well. Under same crossover frequency of the voltage control loop, the novel active ac ripple scheme is simulated. Figure 4.29 shows the simulation result. Even if the same crossover frequency at 16 Hz is used for the voltage control loop, the input current still has much smaller ac ripple. Output current is regulated well under dc link voltage fluctuated by the ac ripple components. Figure 4.30 shows the dc link voltage during load transient. It is clearly seen that voltage transient is reduced a lot compared to Figure 4.26, due to the higher crossover frequency in the voltage loop.

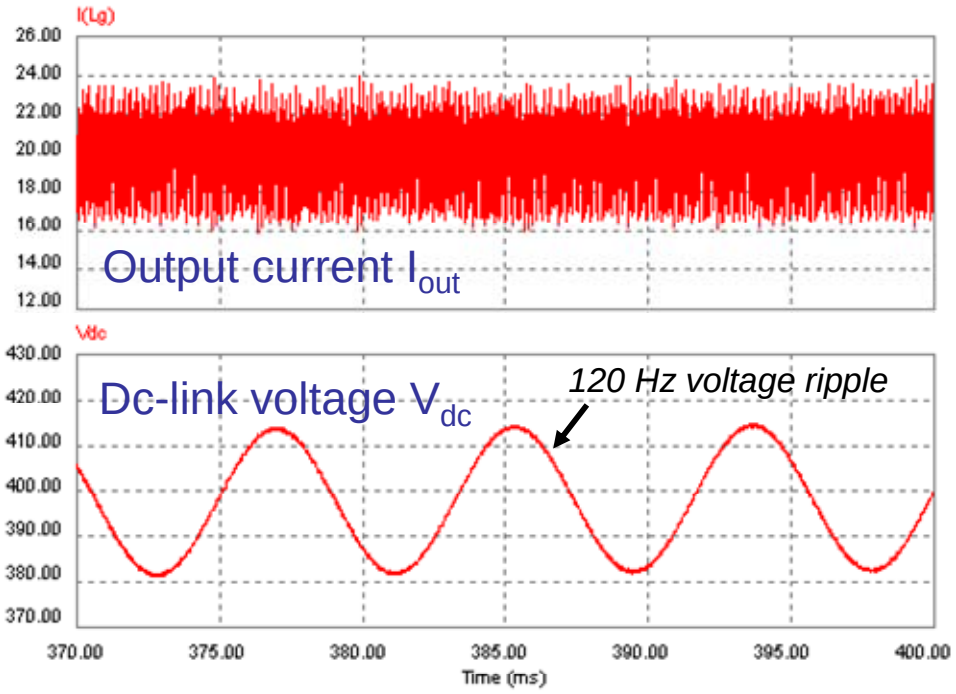


Figure 4.26 Simulation waveforms of conventional control structure with 3kHz current loop and 2Hz voltage loop.

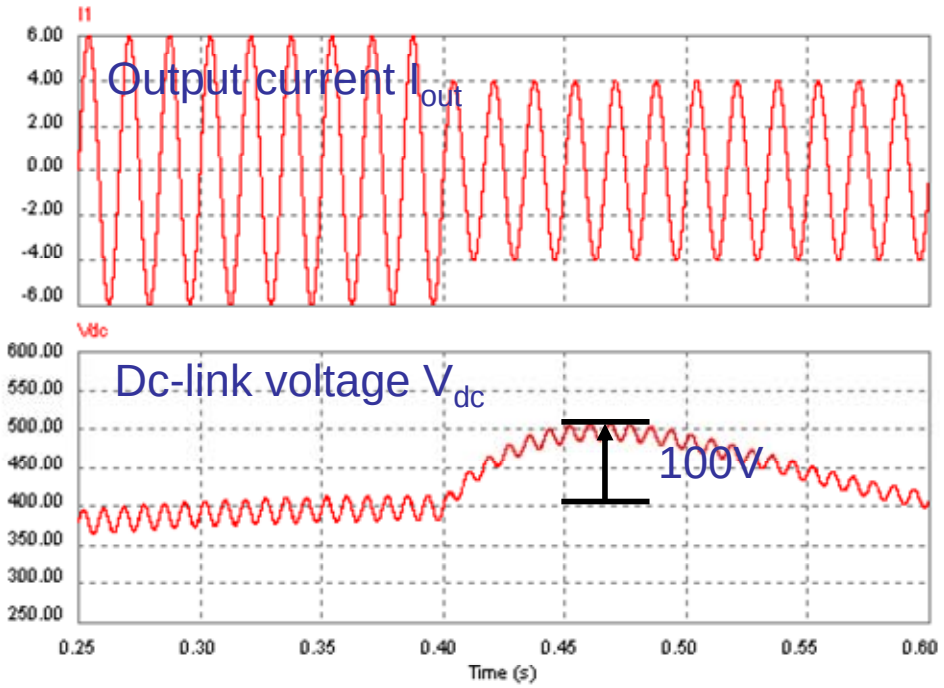


Figure 4.27 Simulation waveforms during load transient.

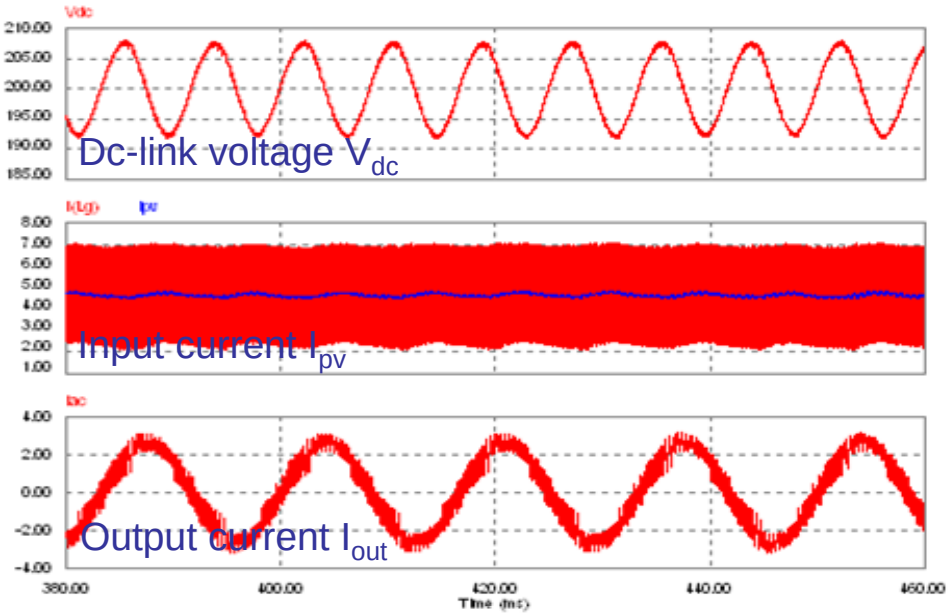


Figure 4.28 Simulation waveforms of conventional control structure with 16Hz voltage loop crossover frequency.

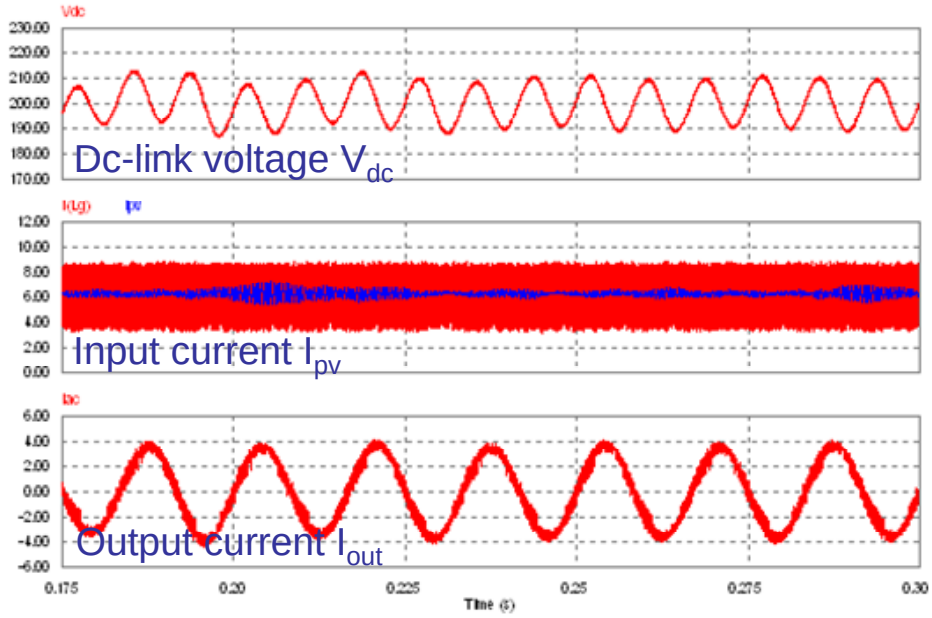


Figure 4.29 Simulation waveforms of novel active ripple compensation with 16Hz voltage loop crossover frequency.

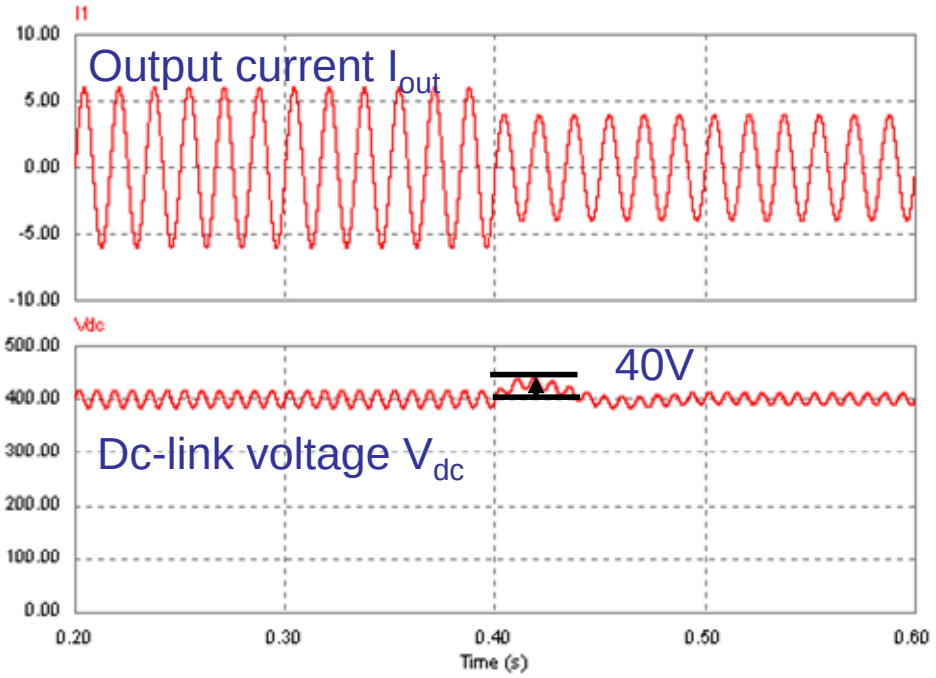


Figure 4.30 Simulation waveforms of novel active ripple compensation during load transient.

4.5.2 Experimental verification

The novel active ripple compensation scheme is applied to the hardware prototype of the single-phase grid-connected power system based on the two-stage dc-ac converter. The compensators designed in Section 4.4 are implemented to a digital signal processor (DSP) circuit. The power circuit parameters discussed in Section 4.3 are also used.

First, the steady-state operation performance of the compensator loops, based on the generalized control structure, is tested. Figure 4.31 shows the steady-state waveforms with a zero input current command under a grid-connected operation. It is seen that the input current is regulated to be zero with its command. Accordingly, no power is transmitted into the utility grid. The dc link voltage is regulated to 250V, as commanded.

Figure 4.32 is the steady-state operation waveforms when the input current command is increased to 7A. In the experiment, the outer voltage loop of the second-stage converter is designed with a high frequency crossover frequency of 500 Hz. The quasi-notch filter is not applied. After increasing the input current command, it is seen that the input current is regulated to be approximated 7A, and henceforth, the corresponding output current is transmitted into the utility grid as being nearly sinusoidal waveform. In this experiment, due to its fast crossover frequency, the dc link voltage is tightly regulated without any ripple components. As a result, the input current oscillates with a low frequency ripple component, in order to supply 120Hz instantaneous ac power.

Figure 4.33 (a) shows the steady-state waveforms captured in the experiment using the same hardware prototype operation of Figure 4.32. The outer voltage loop crossover frequency of the second-stage converter is set to 20 Hz. Note that the quasi-notch filter is not applied here. It can be seen that the input current has reduced the ripple component

more than with the input current of Figure 4.32, while dc link voltage takes over some parts of the ripple component.

The 20Hz voltage loop crossover frequency means that the voltage loop is slow. Therefore, the voltage loop permits greater 120Hz voltage ripple components. The slow voltage loop is able to reduce low frequency current ripple but sacrifices transient voltage performance, as discussed before.

Figure 4.33 (b) illustrates the steady-state waveform's application of the quasi-notch filter to the outer voltage loop of the second-stage converter, with same crossover frequency of 16Hz. From Figure (b), the further attenuation of the quasi-notch filter takes over most of ripple components in the dc link voltage. This achieves almost ripple free input current. However, it is observed that the output current becomes a little distorted. This distortion can be explained from the control configuration of the generalized control structure, in which the dc link voltage loop drives the output current loop. Some of the ripple components dwelling at dc link voltage still penetrate the dc link voltage loop, even though the quasi-notch filter is designed to have a strong attenuation. Consequently, this impacts the output current control loop. Therefore, there is a design trade-off between the sinusoidal output current regulation and low frequency ripple reduction effect.

Finally, the improvement of the novel active ripple compensation scheme on transient performance is addressed in Figure 4.34, in comparison with the conventional approach using voltage loop crossover frequency. Figure 4.34 (a) shows the waveforms under the conventional scheme under 2 Hz cross-over frequency, while Figure 4.34 (b) is the captured waveforms under the novel scheme under faster 16Hz cross-over frequency with the quasi-notch filter. It is clearly seen that the proposed active ripple compensation

of Figure 4.34 (b) causes a lot of improvement on transient response, and thus results in small overshoot voltage and fast settling time.

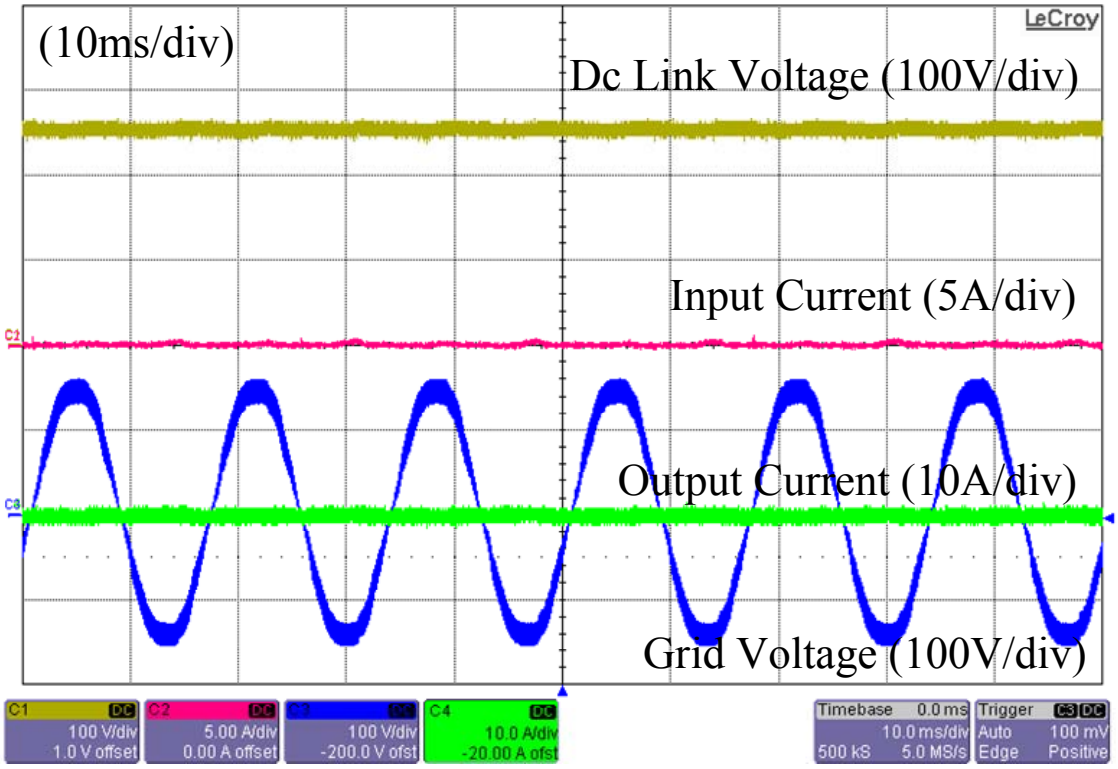


Figure 4.31 Experimental waveform of single-phase grid-connected power system under zero input current command (10 ms/div).

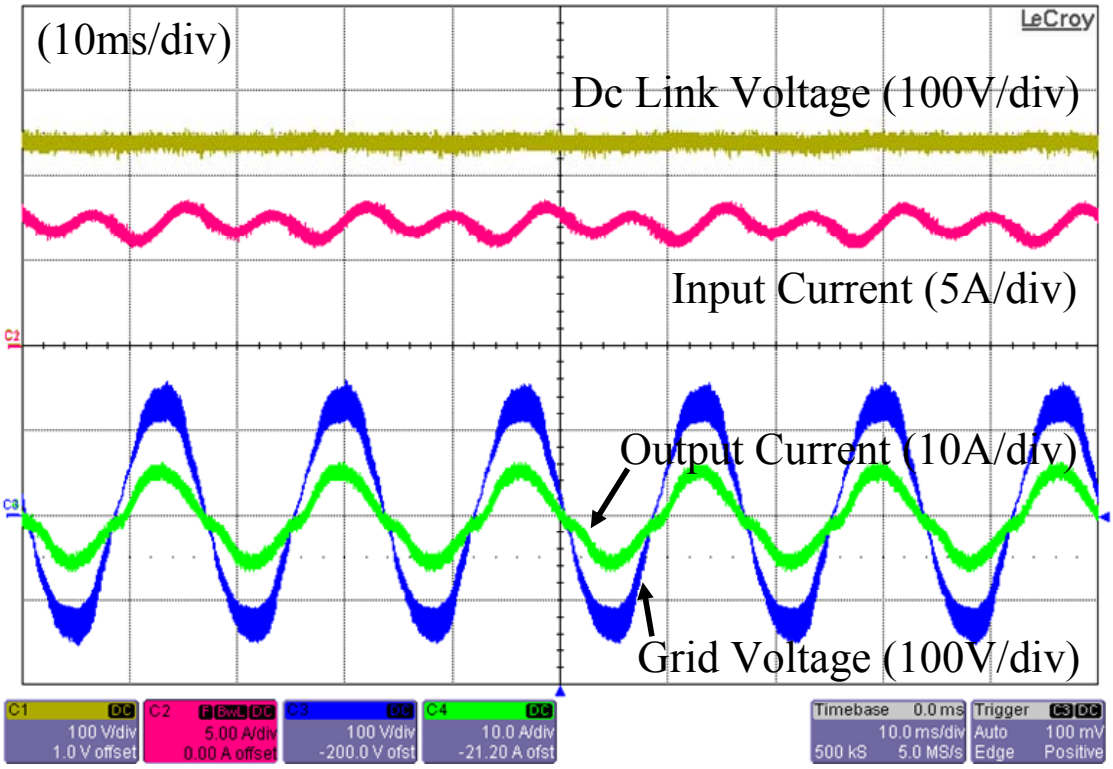
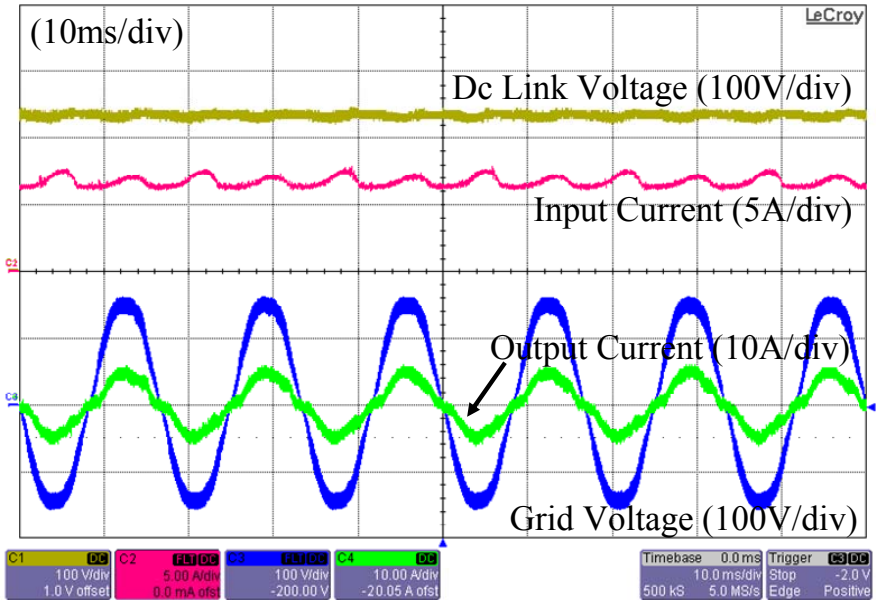
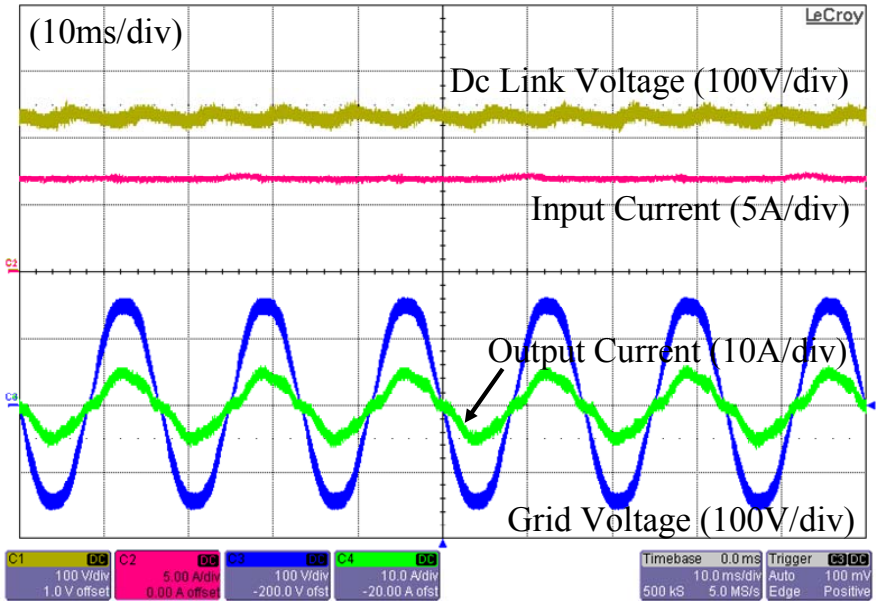


Figure 4.32 Experimental waveform of single-phase grid-connected power system under 7A input current command (10 ms/div).

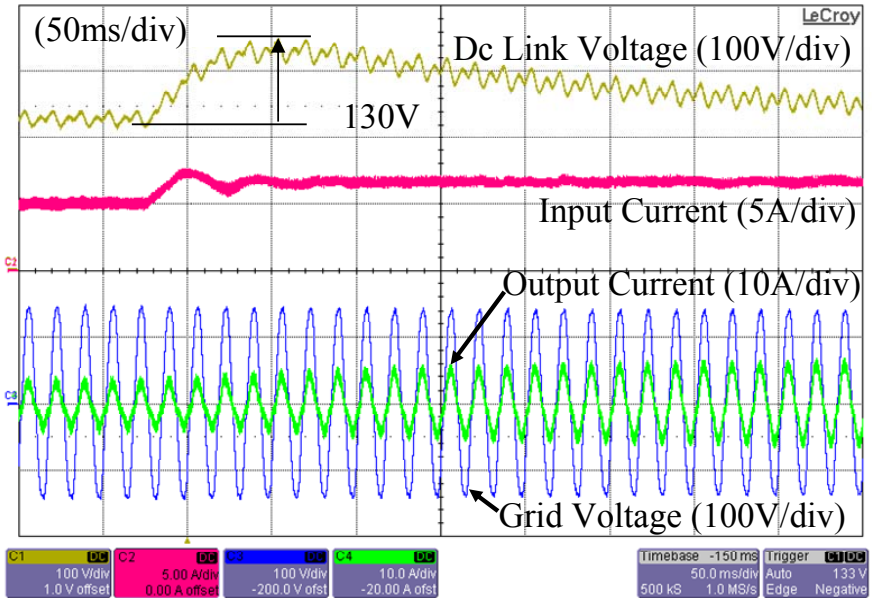


(a)

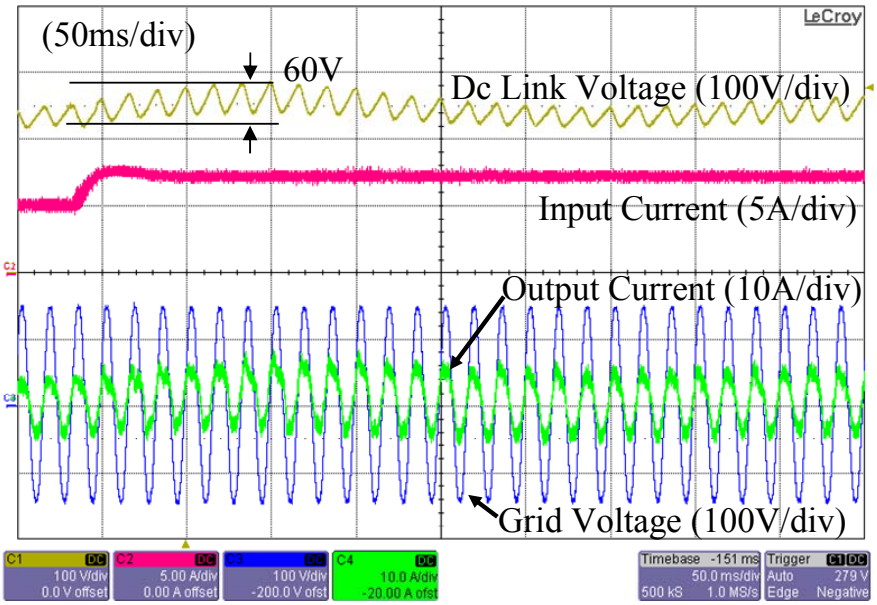


(b)

Figure 4.33 Experimental waveform using 16 Hz voltage loop crossover frequency; (a) without and (b) with quasi-notch filter (10 ms/div).



(a)



(b)

Figure 4.34 Experimental waveform of dynamic transient under increasing input current; (a) conventional scheme with 2Hz crossover frequency and (b) novel scheme with 16Hz crossover frequency and quasi-notch filter (50 ms/div).

4.6 Summary

This chapter presents the extension of the previous research works, regarding two-stage control, to a single-phase grid-connected power system adapting photovoltaic energy sources. The basic principle and electrical characteristics, such as variation with illumination and temperature, of photovoltaic energy sources were addressed. The time-varying state variables in the single-phase grid-interconnected power system were modeled using the quasi-steady state concept, which approximates sinusoidal steady-state operation point as the sequence of the several "quasi" equilibrium points. The disadvantages of active ripple reduction schemes based on the conventional control structure were analyzed. It is shown that the generalized control structure can solve these issues.

Moreover, to avoid poor transient performance of the dc link voltage control loop, the quasi-notch filter was incorporated into the voltage loop. This attenuates the ac low frequency harmonic components strongly, while providing design flexibility for higher crossover frequency. Using the small-signal model derived by aggregated modeling approach based on the quasi-steady state concept, both the first-stage and second-stage converter's control loop were designed on frequency domain analysis. The simulation results and experimental results were provided to verify the effectiveness and improvement of the proposed active compensation scheme.

Chapter 5

Conclusion and Future Works

5.1 Summary and major results of this dissertation

This dissertation summarizes research work that develops the generalized control structure and modeling approach of the two-stage power converters in a unified way. As a result, the performance and reliability of a energy storage system employing two-stage power converter is significantly improved with multiple functionalities required for a consistent and reliable independent power system.

The initial research explores based on the two-stage dc-dc architecture which converts dc electricity extracted from a thermoelectric generator to regulated dc electricity in order to store it into a battery storage device. The conventional control structure is demonstrated. Also, issues associated with achieving two distinctive control modes are addressed. Based on the analysis of the issues, the novel control structure is proposed. The generalized modeling approach for the two-stage power converter allows for design of the novel control structure based on the frequency domain information. As a result of this research, the performance and reliability of the thermoelectric battery energy storage system is improved with the functionality of managing the state-of-charge of batteries.

Later, the generalized control structure and modeling approaches extend to the two-stage dc-ac architecture in order to connect dc electricity into the existing single-phase power grid for a photovoltaic power system. The performance and reliability of the photovoltaic single-phase grid-connected power system is improved by the advanced active ripple compensation scheme of double-fundamental frequency to increase source utilization.

Overall, the major results of this dissertation work are:

1) Proposing a novel control structure based on two-loop average-mode-control technique, and created by reconstructing the conventional control structure and the different designated feedback signals; the first-stage converter loop designates input voltage, input current, and output voltage feedback signals, while the second-stage converter loop designates dc link voltage and output current feedback signals.
2) Developing a new modeling approach with basis on the modification of the subsystem-integration approach and employment of the quasi-steady state concept. Modeling works are significantly reduced by treating a two-stage power converter as a single-stage power converter having current sinking or sourcing.
3) Identifying system level issues, such as the control mode transfer and low frequency ac ripple reduction, for the two most promising applications, battery energy storage and single-phase grid connected power system, when renewable energy sources are utilized. The solutions of these issues are proposed by using the novel control structure. Design examples are illustrated. The simulation and experimental evaluations of the proposed solutions are presented and support their effectiveness.

5.2 Future works

1) The quasi-steady state analysis dealing with time varying state variables of ac electricity is usually effective to design a control loop. However, it is not sufficient to be a systematic modeling approach because of the assumption that the oscillatory of time varying state variables should be much slower than both dynamics of the system and small ac variations. The assumption leads to controversial uncertainty of modeling validation at the low frequency range, and thus more research is needed.
2) The generalized control structure requires system level operation scheme to improve the performance of renewable energy power system. Further research on the power management strategy is necessary.

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