Chapter 1

Introduction

Significant progress in ferroelectric random access memory (FRAM) technology has been realized during the last decade, but the integration of a commercial FRAM device is still restricted by several process problems. In this chapter, three types of major process-induced damage which hampers the realization of a FRAM device are briefly discussed, dry etching induced damage, hydrogen-induced degradation, and stress effects. A brief introduction on the recent development of ferroelectric capacitors are also included.

§1. BACKGROUND OF FERROELECTRIC CAPACITORS

The fabrication of memory devices using ferroelectric materials was intensively studied between 1950’s and 1970’s by many market-leading companies such as IBM, RCA, Bell Laboratories and Westinghouse. Due to the incompatibility with the silicon process, the research was almost abandoned after 1975. However, since 1986, it has exploded as a result of the improvements in thin film technology, especially Pb(ZrxTi1-x)O3 (PZT) sol-gel and sputtering deposition techniques [1]. Ferroelectric memories have been investigated by many semiconductor memory industries as well as by the defense industries, because of the nonvolatility, radiation hardness, high speed, low power, and compatibility with silicon process [2-5].

In general, there are two major applications of ferroelectric materials for memory devices. Firstly, ferroelectric materials could be utilized for dynamic random access memory (DRAM). Secondly, they are applicable for FRAM. Because ferroelectric materials generally have high dielectric constants, ferroelectric thin films have been considered to be a fungible capacitor material for high-density DRAM. As the integration
density of DRAM reaches 4 Gbit, the device size is tremendously decreased. As a result, current silicon-based dielectric materials, namely SiO$_2$ and Si$_3$N$_4$, have proved to be rather inadequate, due to their low dielectric constants. Considerable effort has been made to overcome the low dielectric constant problem by geometric methods such as developing a trench or stack structure, providing wider surface area to increase the capacitance values. Figure 1-1 shows the current method for expanding surface area. HSG (hemispherical grain) and double-cylindrical structures are shown in figure 1-1(a) and 1-1(b) respectively [6]. Both methods represent ultimate technology in current silicon process, and have been applied to the fabrication of 1 Gbit DRAM devices. However, this geometric complexity made the integration process inevitably difficult and thus could not be applied to 4 Gbit DRAM and beyond. Capacitance, by definition, could be improved by expanding the area, increasing the dielectric constant, or decreasing the thickness of dielectric layer. In fact, the thickness of dielectric layer has been already minimized to barely block tunneling current, which is below 100Å. The remaining choice, then, is to look for dielectric materials that have considerably higher dielectric constant. Ferroelectric thin films, which are known to have dielectric constant about two orders higher than that of SiO$_2$, were selected as capacitor materials in 4 Gbit DRAM and beyond.

Along with the high dielectric constant, ferroelectric materials also exhibit characteristic polarization responses to an applied electric field, which makes them potential candidate materials for nonvolatile memory devices. In case of current DRAM, the data is stored as a form of charge in a linear capacitor. In order to safely maintain the stored data, it is necessary to supply constant voltage to the capacitors, which are recharged hundreds times per second by refresh circuitry. If the power is interrupted, DRAM loses all data stored in it, that is to say DRAM is volatile. In contrast, data in a ferroelectric capacitor is stored as a remnant polarization state of the ferroelectric material itself. The ferroelectric capacitor has a nonlinear dielectric property with permanent charge retention capabilities after the voltage application. Therefore, the stored data does not disappear, even though the power is turned off, that is, FRAM is nonvolatile. The principal advantages of FRAM over other nonvolatile memories are fast write/erase access times at
the nanoseconds level, low operating voltage below 5V, high endurance on read/write repeating cycle, and high radiation hardness which is especially required for military and space applications. In principle, FRAM could replace EPROM (erasable programmable read only memory), EEPROM (electronically erasable programmable ROM), SRAM (static RAM), and DRAM. Furthermore, if high density FRAM could be developed and the production cost could be reduced down to the level of magnetic core, then FRAM could also replace the hard disk as the mass storage device, because of its faster access speed and the absence of mechanical wear problems. Actually, low density FRAM, such as 4 K, 16 K, and 64 K FRAM, have been manufactured by some semiconductor industries, such as Ramtron, Rohm, and Hitachi. Such a low density FRAM is replacing EPROM and EEPROM in some areas such as game machines and smart cards. Matzushita, the largest consumer-electronics firm in the world, expects the market for FRAM to amount to ¥100 billion ($690 million) a year by 2005. Explosive demands in video games, cellular phones, portable computers and other portable electronic goods, indicate that annual sales of those speedy nonvolatile memories could amount to more than ¥3 trillion ($20.7 billion) by 2010 [7]. The trend of ferroelectric capacitor technology is schematically shown in figure 1-2 in terms of memory density. Low density FRAM comprising CUB (capacitor under bit-line) structure is already available in the market, but high density FRAM is still in the development stage with COB (capacitor over bit-line) structure. Both cross-sectional view of real FRAM device is shown in figure 1-3 and 1-4 [3,9]. The ferroelectric capacitor for Gbit density devices, a current hot issue of DRAM makers, aims to develop 1 G DRAM and beyond by replacing silicon oxide with Ba$_x$Sr$_{1-x}$TiO$_3$ (BST) film.

With such promising properties, however, FRAM has failed to attract a market share due to high production cost, poor reliability and lack of high-density fabrication technology. Several attempts to integrate such devices on a scale larger than 1 Mbit by using a advanced silicon ultra large scale integration (ULSI) technologies, have been reported using PZT or SrBi$_2$Ta$_2$O$_9$ (SBT or Y1) ferroelectric thin films. However, there are still several issues concerning the integration to be solved for the realization of high-density FRAM. Such process issues will be individually discussed in this chapter.
§2. Ferroelectric Materials Issue

The recent surge in FRAM technology can be traced to the development of thin film technology in 1980’s, which permits the fabrication of thin films at temperatures compatible with the silicon process. For the purpose of the DRAM capacitor material, only BST thin films have been focused these days because of high dielectric constant (300 - 700) and process compatibility with silicon technology. However, many ferroelectric materials have received attention for FRAM materials, including PZT, SBT, Bi$_4$Ti$_3$O$_{12}$, LiNbO$_3$ and BaMgF$_4$. Among those, PZT and SBT films have been the focus of investigation because of their large polarization values and process feasibility.

An ideal material for use as a FRAM capacitor should have high remnant polarization, low coercive voltage, and a reasonable Curie temperature (much higher than the device operating temperature and lower than the film formation temperature). Inherent switching speed should be in the nanoseconds level, and the ferroelectric capacitor should have good retention, imprint, and endurance characteristics. Radiation hardness is another desirable property for military and space application. The process burden required to prepare ferroelectric thin film must not have a detrimental effect on the underlying pattern structure. Two families of materials, PZT and SBT, have been widely investigated for memory application. Although their electrical characteristics can be modified by dopant addition (PLZT, PNZT: La or Nb doped PZT, SBTN: Ta doped SBT), the advantages and disadvantages of both materials are listed as shown in table 1-1. The PZT films grown on a Pt electrode, a typical electrode for ferroelectric film growth, show fatigue problems, that is, the remnant polarization value decreases with read/write repeating cycles [8]. This problem can be avoided by replacing the metallic Pt electrode with a metal oxide electrode such as RuO$_2$, IrO$_2$ and La$_{0.5}$Sr$_{0.5}$CoO$_9$ or with multi-electrode like RuO$_2$/Pt. Practically, IrO$_2$/Pt and IrO$_2$/Ir multi-electrode system is being used in FRAM industries [9]. The bismuth layer structure SBT films are attractive because of their good fatigue properties. Therefore we can simplify the integration process by using SBT films instead of PZT films. However the
process temperatures are high in relation to the standard silicon process, and therefore SBT films are not applicable for high density FRAM fabrication at present. Many efforts have been paid to reduce the formation temperature in terms of process optimization, precursor system, and solid-solution method [10].

In this study, PZT thin films were selected as ferroelectric materials for capacitors for the three main reasons below:

- Remnant polarization ($P_r$) values in PZT capacitors are larger than SBT capacitors.
- The formation temperature of a PZT film is considerably lower than that of an SBT film.
- PZT films show relatively stronger endurance against hydrogen-induced damage compared with that of SBT films [11,24].

Table 1-1. Thin film properties of PZT and SBT families.

<table>
<thead>
<tr>
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<th>PZT families</th>
<th>SBT families</th>
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<tbody>
<tr>
<td>Crystal Structure</td>
<td>ABO3 type perovskite</td>
<td>Bi layered structure</td>
</tr>
<tr>
<td>Formation temperature ($^\circ$C)</td>
<td>600 – 700</td>
<td>750 – 850</td>
</tr>
<tr>
<td>Switching polarization ($\mu$C/cm$^2$)</td>
<td>30 – 60</td>
<td>10 – 30</td>
</tr>
<tr>
<td>Coercive field (kV/cm)</td>
<td>50 – 70</td>
<td>30 – 50</td>
</tr>
<tr>
<td>Dopants</td>
<td>Nb, La</td>
<td>Nb</td>
</tr>
<tr>
<td>Dielectric constants</td>
<td>400 – 1500</td>
<td>200 – 300</td>
</tr>
<tr>
<td>Fatigue (Pt electrode)</td>
<td>Poor (oxide needed)</td>
<td>Good</td>
</tr>
<tr>
<td>Curie temperature ($^\circ$C)</td>
<td>400 – 500</td>
<td>~ 310</td>
</tr>
</tbody>
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§3. **Damages Induced During Dry Etching Process**

There are several problems that should be overcome in order to realize the integration of ferroelectric thin films to semiconductor devices. One of the associated issues is to establish a dry etching process without plasma damage. Due to the low vapor
pressure of etched products of ferroelectric films and electrode materials (typically Pt, Ru and Ir), physical sputtering should be incorporated into the etching process. In general, chlorine and fluorine containing gases are used for the etching of PZT thin films. Energetic ion bombardment during dry etching was found to be essential in the enhancement of etch rate by inducing surface damage [12,13]. In dry etching, reactive free radicals and ions in the plasma may change the physical and electrical properties of the etched films, which is called as the etching damage. The etching damage can be categorized into two types. First, the suppression of polarization is observed. This can be attributed to the impingement of charged particles, because domain switching is hampered by charges nearby. We could diminish this effect up to nearly the virgin state simply by the annealing above the Curie temperature ($T_c$) as shown in figure 1-5, because phase transitions to the paraelectric phase can expel all charged particles by the rearrangement of atomic structure. Second, bombardment with high energetic atoms usually produces a plasma-damaged layer on the surface of PZT film [14,15]. In addition, it is generally thought that the damaged layer in the ferroelectric capacitor is likely to play a parasitic role, which affects the performance of a device. Recently, Torii et al. reported an improved leakage current property by applying the rf oxygen plasma treatment to reduce etching damage. However, the plasma damage was not completely recovered by the plasma treatment. Thus it would be expected that the fabrication of higher density FRAM might be impossible because of this etching damaged layer [14]. To date, it is not easy to formulate a recipe without the plasma damage during the dry etching process. In this study, therefore, a wet cleaning approach was attempted as a method for the elimination of the etching damaged layer. The detrimental effect of this etching damaged layer was evaluated in terms of the electrical properties and process endurance.

§4. HYDROGEN-INDUCED DAMAGE

Another problem that PZT ferroelectric capacitors suffer from during integration is the loss of hysteresis characteristics in an atmosphere that contains hydrogen, which is
dissociated from the precursor material. Such a phenomenon occurs during the process of silicon oxide deposition (inter-layer dielectric [ILD] and inter-metallic dielectric [IMD] process) and forming gas anneal, and this degradation is generally referred to as hydrogen-induced damage, hydrogen damage or hydrogen attack. Hydrogen-induced damage can deteriorate not only the electrical properties including ferroelectric characteristics but also the mechanical properties. Three types of degradations are observed in general: decrement of the remnant polarization, increment of the leakage current, and delamination of electrodes. Figure 1-6 clearly demonstrates the degradation of hysteresis loops after ILD deposition.

It is well known that the degradation of a PZT capacitor is closely related to the electrode materials, especially the top electrodes [16-18]. It has been suggested that the catalytic activity of the top electrode, the dissociation of molecular hydrogen into atomic hydrogen, plays a critical role in the degradation of PZT capacitors. The group 10 (Ni, Pd, Pt), metals have strong catalytic activity compared to group 9 (Ir, Rh) and 11 (Ag, Au) metals. In the case of Pt, a typical electrode material for ferroelectric capacitor due to its chemical inertness, catalytic activity is so high that hydrogen molecules would dissociate and be adsorbed chemically at low temperatures, even 150 K, and migrate freely without an energy barrier [19,20] Without the top electrode, a bare PZT film starts to show degraded polarization values from above 400°C by forming gas annealing. However, when the Pt top electrode is deposited, Pt/PZT/Pt capacitor begin to degrade at below 150°C.

Miki et al. suggested an interfacial reduction model, which explains the degradation of electrical properties most reasonably up to the present [21]. In this model, activated hydrogen, protons or radicals, penetrate the Pt electrode into PZT, and react to reduce PZT at the Pt/PZT interface. As a result, oxygen vacancies which produce positively charged centers, could occur, damaging the interface. These defects pile up at the Pt/PZT interface and act as a heavily doped semi-conductive layer, resulting in a positive space charge and voltage drop. This model provides a reasonable explanation of the increase of leakage current, and the asymmetric I-V breakdown behavior when the top electrode is negatively biased. However, there still is no model so far which can elucidate.
the degradation in view of ferroelectric material itself.

The changes in PZT crystal structures caused by hydrogen-induced damage have not yet been fully revealed. Only two papers have been published relative to this issue. Ikarashi detected phase changes near the PZT/Pt interface by transmission electron microscopy (TEM) analysis, and concluded that the decrease in Pb composition, and distortion of Ti-O coordination were caused by forming gas annealing [22]. Aggarwal reported that hydroxyl bonds (OH) were formed in PZT films by forming gas annealing, and proposed that bonded hydrogen prevents the Ti (or Zr) ion from switching [23]. Surprisingly, despite the many results on the degradation of ferroelectric properties, PZT films still exhibited unchanged properties after forming gas annealing such as, for example, XRD patterns. On the contrary, it was reported that SBT film, rival of PZT, lost their crystal structure by forming gas annealing [11,24].

In this study, process parameters such as Zr/Ti ratio, PbTiO₃ seeding layer and excess Pb amount in PZT film on hydrogen-induced damage were investigated and optimized. A variety of PZT capacitor modules including TiO₂ barrier layer were compared in terms of the polarization degradation.

§5. Effect of Stress

In general changes in polarization are expected when PZT films are exposed to external or internal stress, because lattice constants should vary according to the stress applied. The stress may hinder the switching of an area or cause an undesirable switching of neighboring areas, thereby losing the information stored in ferroelectric capacitors. For a FRAM device, stress-induced distortion may be disadvantageous even in very small areas because of the need for high storage densities.

Numerous studies have revealed that ferroelectric films exhibited changes in hysteretic properties, such as remnant polarization, coercive voltage, and Curie temperature according to the imposing stress intensity [25]. The stress can originate from the substrate materials [26], deposition parameters of ferroelectric film [27], and interconnect layer [28].
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Theoretical calculation also indicates that hysteretic properties should vary with the induced stress [29,30]. Surprisingly, the results of many experiments are not consistent with these assumptions. In some case Pr increases monotonously and in the other case Pr decreases monotonously as compressive stress develops in a ferroelectric layer. This can be attributed to the art effect of thin film process. The most credible experiment was performed by Kumazawa et al., which avoids possible process-induced art effects, and extracts a pure stress effect [31]. They observed 0.6% of Pr reduction per 100 MPa tensile stress, and 3.4% of Pr increment per 100 MPa compressive stress in Pt/PZT/Pt capacitors (figure 1-7). In general, the maximum stress of a PZT film is expected to be about 1 GPa of the tensile stress, in the case of PZT films which are grown by CSD (chemical solution deposition) method. About a maximum 6% of Pr attenuation would be expected, at most, in this case. It would be expected that PZT film stress can be minimized by controlling stresses of ferroelectric capacitor module, and layers deposited above it such as ILD or interconnect layer. Actually NEC, Japanese chip maker, deposit Ir/IrO2 layer onto the ILD layer to attenuate the stress imposed on PZT film, thus improving hysteretic properties.

In this study, the effect of stress developed by the ILD layer was investigated in chapter 7.

§6. Objectives of Research

The objectives of this research are outlined as follows:

1. Characterization of physical and chemical properties of the damaged layer formed during dry etching process.
2. Preparation of the cleaning solution for the elimination of the etching damaged layer.
3. Cleaning process setup using PZT cleaning solution.
4. Investigation of the process parameters in view of hydrogen-induced damage to optimize PZT capacitor structure.
5. Investigation of the blister formation mechanism in Pt/PZT/Pt capacitors.

§7. REFERENCES

[31] Tetsuo Kumazawa, Yukihiro Kumagai, Hideo Miura, and Makoto Kitano, and Keiko
Figure 1-1. SEM Pictures of capacitor nodes for 1 Gbit DRAM device. (a) Hemispherical grain (HSG) method and (b) double-cylindrical structure [6].
Figure 1-2. Trend of ferroelectric capacitor technology
Figure 1-3. Cross-sectional SEM pictures of 64K FRAM fabricated by Samsung Electronics. Design Rule 1.2µm, Double Metal, 1T/1C architecture [3].
Figure 1-4. Cross-sectional SEM pictures of 4M FRAM fabricated by Samsung Electronics. Design Rule 0.6μm, triple Metal, 1T/1C architecture [8].
Figure 1-5. Suppression of the hysteretic properties due to the dry etching process. (a) Polarization recovery by the annealing, (b) hysteresis loops before and after recovery annealing.
Figure 1-6. Degradation of the hysteretic properties due to hydrogen-induced damage. Loops were measured from the 100 capacitors after ILD deposition. The effect of hydrogen-induced damage is more serious as the size is smaller. The structure of the capacitor is Ir/IrO$_2$/PZT/Pt/IrO$_2$. 
Figure 1-7. Remnant polarization values with a variation of stress applied to a PZT thin film. (a) Tensile stress, (b) compressive stress [30].