SPACE VECTOR MODULATION AND CONTROL OF MULTILEVEL CONVERTERS

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(ABSTRACT)

This dissertation is the result of the research and development of a power conditioning system for superconductive magnetic energy storage systems (SMES). The dominant challenge of this research was to develop a power conditioning system that can match slowly varying dc voltages and dc currents on the superconductive magnet side with the ac voltages and ac currents on the utility side. At the same time, the power conditioning system was required to provide a bi-directional power flow to the superconductive magnet.

The focus of this dissertation is a three-level diode-clamped dc/ac converter, which is a principle part of the power conditioning system. Accordingly, this dissertation deals with the space vector modulation (SVM) of three-level converters and introduces a computationally very efficient three-level SVM algorithm that is experimentally verified.

Furthermore, the proposed SVM algorithm is successfully generalized to allow equally efficient, real-time implementation of SVM to dc/ac converters with virtually any number of levels. The most important advantage of the proposed concept is that the number of instructions required to implement the algorithm is almost independent from the number of levels in a multilevel converter.

More on the side of the control of multilevel converters, particular attention in this dissertation is paid to the problem of charge balance in the split dc-link capacitors of three-level neutral-point-clamped converters. It is a known fact that although the charge balance in the neutral point (NP) can be maintained on a line cycle level, a significant third harmonic current

flows into the NP for certain loading conditions, causing the neutral-point voltage ripple. The logical consequence of that ripple is the deteriorated quality of the output voltage waveforms as well as the increased voltage stress on the switching devices.

This was the motivation to more carefully explore the loading conditions that cause the imbalance, as well as to study the fundamental limitations of dc-link capacitor charge balancing algorithms. As part of this work, a new model of the neutral-point current in the rotating coordinate frame is developed as a tool for the investigation of theoretical limitations and in order to provide some insight into the problem. Additionally, the low-frequency ripple is quantified and guidelines are offered that can help determine the correct size for the dc-link capacitors.

Because the study of the neutral-point balance identified the loading conditions that (under some possible system constraints) cause an unavoidable neutral-point voltage ripple, a feed-forward type of control method is developed next. The proposed feed-forward algorithm can effectively prevent the neutral-point voltage ripple from creating distortions in the converter output voltage under all loading conditions and without causing additional disturbance in the neutral-point voltage. The feed-forward method is developed for a sine triangle as well as for the SVM type PWM algorithm.

The simulation results that include the full dynamic model of the converter and load system validate the feed-forward approach and prove that the feed-forward algorithm can effectively compensate for the effect of the neutral-point voltage ripple. The simulation results are then experimentally verified.

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To my parents

Table of Contents

List of Figures

List of Tables

1 INTRODUCTION

1.1 Motivation and Objectives

In recent years, there has been increased interest in renewable energy sources on one side, while on the other, the initiative for deregulation of the utilities increased the interest in systems that can increase their flexibility. Both these developments recognize power electronics systems as a core enabling technology.

For example, renewable and/or clean energy sources such as wind turbine, solar power, fuel cells and micro turbines all require power-conditioning systems. While these power-conditioning systems provide the necessary interface to the utility, they also match the electrical characteristics of the sources with the electrical requirements of the loads and/or the utility. Similar to the renewable sources, energy storage systems (viewed as key components of the envisioned flexible utilities) also require power conditioning systems that can match the electrical characteristics of the energy storage systems with those of the utility.

What makes power electronics solutions unique in both these cases is that they are fundamentally multifunctional and can provide not only their principle interfacing function but various utility functions as well. This is particularly true of energy storage systems, which are potentially well suited to provide a host of additional functions on the utility level. Some of these functions are load leveling, utility stabilization, static var compensation, harmonic compensation and active filtering. In addition, they can also be used as uninteruptible power

supply (UPS) systems at various power levels, and can be designed to provide a pulse power capability that is of interest for certain military applications as well as for some high-energy physics experiments.

One of the practical energy storage technologies is superconductive magnetic energy storage (SMES). The design of a power conditioning system for a SMES system was one of the primary objectives of the work that will be presented in this dissertation. However, some of the insight gained from the development of a SMES power conditioning system is readily applicable to power conditioning systems for batteries, fuel cells, flywheels, super capacitors and other energy storage technologies.

What makes this power conditioning system (PCS) design even more interesting is that it was built using multilevel converters, which allowed a research into the issues, and tradeoffs involved with multilevel power converter technology in general. Therefore this work followed a trend in the power electronics community to shift towards multilevel power electronics converter topologies that seem to offer significant advantages for utility applications over the more conventional two-level topologies. This is the principle reason why this work concentrates on some important aspects of multilevel topologies that are directly applicable to a wide range of multilevel converters.

For example, together with the wider introduction of multilevel converter topologies, there is a strong tendency to modularize the hardware design in order to reduce the prices, simplify converter design and potentially increase the availability of multilevel converters. However, with the increased number of levels, the number of allowable switching states in the converters is also rapidly increasing. This situation places significant computational challenges in front of the PWM modulator, which is typically implemented in software and operating in real time and for high switching speed.

This problem is addressed with a new and general multilevel algorithm. The algorithm very efficiently performs a switching vector identification and duty cycle computation; even more

importantly, the number of steps involved in the computation is almost independent of the number of levels in the converter.

Secondly, with respect to the voltage balancing problem of the three-level neutral-point-clamped converter, which is currently perhaps the most widespread multilevel topology, a problem of split dc-link capacitors' charge balancing is explored in a comprehensive way. This is accomplished using the new model of the neutral point (NP) current in the rotating dq reference frame. The study resulted in the identification the loading conditions that result in the low-frequency ripple, the quantification of the size of the ripple, and the ability to make recommendations for the size of the dc-link capacitors for any given operating point as well as the NP ripple specification.

And thirdly, because the study of the NP balance identified the loading conditions under which certain system constraints cause an unavoidable NP voltage ripple, a feed-forward control method is developed. It is the objective of this dissertation to investigate the effects of the feed-forward algorithm on the quality of the output waveforms as well as on the control authority over the charge balance in the split dc-link capacitors.

1.2 Review of Previous Research

When designing a system, particularly a relatively complex system such as the SMES power conditioning system, there are many important considerations, in areas ranging from the device's physics and soft switching all the way to the mathematical abstractions used for modeling and control. Because of the overwhelming breadth of published material on these topics, this literature review will be limited to multilevel topologies, multilevel modulations and the control of multilevel converters, because these topics are closely related to the work in this dissertation.

At this time, the area of multilevel power conversion can still be considered young. In 1980, early interest in multilevel power conversion technology was triggered by the work of Nabae, et al., who introduced the neutral-point-clamped (NPC) inverter topology [B1]. It was immediately

realized that this new converter had many advantages over the more conventional two-level inverter. Subsequently, in the early nineties the concept of the three-level converter was extended further and some new multilevel topologies were proposed.

At the present time, the majority of research and development effort seems to concentrate on the development of three classes of converters: the diode-clamped multilevel converter, the multilevel converter with cascaded single-phase H-bridge inverters, and the multilevel converter known as the flying capacitor converter, or sometimes as the imbricated cells multilevel converter. The two remaining configurations, namely the multilevel converter with bi-directional switch interconnections [A1] and the multilevel converter with multiple three-phase inverters are receiving less attention at the present time and will not be discussed further.

As mentioned, the three-level NPC converter was the first widely popular multilevel topology. A significant amount of research effort was invested in the development of this family of converters [B], which resulted in the fact that today this topology probably represents the state-of-the-art multilevel converter technology. This is in part because the converters of this type are currently in the phase of rapid market introduction by several world-renowned manufacturers [B20, B22].

Soon after the introduction of the NPC converter, the original topology was extended to a higher number of levels using the same principle of diode-clamped intermediate voltage levels [C1]. The back-to-back connection of two converters of this type [A7, A8, C4, C5] enables bi-directional power flow, facilitates balancing of the intermediate capacitor levels and has a very "clean" utility interface. The main disadvantage of this topology is that the required blocking voltage of the clamping diodes is proportional to the level for which they are used to employ clamping action. Consequently, series connection of the diodes may be required. In addition, because of the high switching speed of today's switching devices, mainly IGBTs and IGCTs, the clamping diodes can be subject to severe reverse-recovery stress, which challenges this technology.

An alternative to the diode-clamped converter, the flying capacitor topology does not have issues with clamping diodes. First proposed in 1992 [E1], this approach has the advantage of a larger number of redundant switching states, which allows more freedom in balancing the clamping capacitors' voltages. The main disadvantage is the potential for parasitic resonance between the decoupling capacitors; this is made even worse by the high number of capacitors, which complicates packaging for small inductance. In addition, there are issues with voltage redistribution in the case of voltage surges. Nevertheless, the flying capacitor topology seems very promising.

Finally, the multilevel configuration with cascaded H-bridge inverters presents another alternative in the design of multilevel converters. One of the earlier applications of this topology was for plasma stabilization [D1]; it was then extended for three-phase applications [D3]. A primary advantage of this topology is that it provides the flexibility to increase the number of levels without introducing complexity into the power stage. Also, this topology requires the same number of primary switches as the diode-clamped topology, but does not require the clamping diode. However, this configuration uses multiple dedicated dc-busses and often a complicated and expensive line transformer, which makes this a rather expensive solution. In addition, bi-directional operation is somewhat difficult (although not impossible) to achieve [D10].

Perhaps the most important improvement in cascaded converter topologies is the hybrid multilevel topology [D7]. The main strength of this approach is its combination of the high voltage capacity of the relatively slow GTO devices with the high switching frequency of the lower voltage capacity IGBT devices. At the same time, the different voltage levels of the IGBT and GTO bridges create an additional voltage level without any additional complexity.

Modulation techniques in multilevel converters for utility applications were originally restricted to the synthesis of stepped waveforms [A4]. This strategy can be interpreted as a quantization process in which the reference sinusoidal voltage is approximated by discrete levels of voltage available at the dc-bus. The implementation of this type of modulation is relatively simple and does not require high switching speed, which makes it suitable for converters realized

with GTO thyristors. However, the spectral performance is not very good and a variable dc-bus voltage is required in order to obtain variable voltage at the output.

Far more popular, especially for the converters with faster switching devices, are the so-called sinusoidal PWM techniques. These methods have been extensively studied and are among the most popular in industrial applications. These methods involve a comparison of the reference signal with a triangular carrier waveform and the detection of cross-over instances to determine switching events. The variations of these methods are essentially in the polarity and shape of the carrier waveforms. Although there are slight differences in spectral performance [C16], for the high-enough frequency ratio between the carrier and the reference waveforms, there is no substantial difference between them.

Another very interesting method is based on multiple reference waveforms. It is also sometimes referred to as dipolar modulation [C17]. This method uses a single triangular carrier and two sinusoidal reference waves to modulate three-level inverters. The sinusoidal reference waves are usually obtained by adding positive and negative offsets to the conventional reference signal. The principal reason to introduce the offset is to always interrupt the switching between the outermost levels and the middle level, as well as to avoid any minimum pulse width problems for low modulation indexes.

Perhaps one of the most popular modulation approaches for two-level converters is space vector modulation (SVM), which is now being used more and more in the control of multilevel converters. The concept of space voltage vectors corresponding to various switching states has been applied to study the impact of various switching states on the capacitor charge balancing in almost every paper discussing the SVM approach [B6, B10-11]. An advantage of the SVM is the instantaneous control of switching states and the freedom to select vectors in order to balance the NP. Additionally, one can realize output voltages with almost any average value by using the nearest three vectors, which is the method that results in the best spectral performance.

The primary constraint in devising SVM (as is the case with in most multilevel modulation techniques) involves minimizing the harmonic content of the output PWM waveform while at

the same time maintaining the capacitor charge balance. This is the basic tradeoff of three-level SVM, because the tight regulation of the capacitor charge balance can always be achieved at the expense of increased switching losses and poorer harmonic performance.

Another typical design problem particularly important for the converters built with the slower-switching GTO thyristor devices is the minimum pulse width. This problem is present whenever the reference vector is close in phase and magnitude to any of the switching state vectors. One way of dealing with this problem is to change from the nearest three vector approach (NTV) to nearest four vector approach. Thus a narrow pulse problem can be solved at the expense of increased switching stress and somewhat increased harmonic content. Perhaps a better (but not necessarily more practical) alternative involves the division of the sixty-degree regions into fourteen sub-regions with their switching sequence optimized in order to avoid the narrow pulses [B9].

Finally, it is accepted as conventional wisdom that SVM methods (although very powerful in reducing harmonics) become computationally very demanding and all but impractical as the number of levels increases.

With respect to modeling and control of three- and higher- level converters, the dominant approach is to divide and conquer. What this means in practice is that phase legs are treated essentially as voltage sources (as is the case in two-level converters), while the charge balance becomes part of the modulator, which selects between the redundant switching states in order to maintain the charge balance in the split dc-link capacitors.

This approach makes the charge balance controller relatively simple. For sine-triangle modulated converters, this amounts to control of the modulating signal's zero sequence for the three-level converter [B2, B3], or the manipulation of the redundant small vectors [B4].

Building a model that can describe the behavior of the NP voltage balance is quite difficult because the NP current as well as NP "duty cycles" are piece-wise nonlinear functions. In addition, the steady-state response usually has a strong third harmonic component. Taking all

this into account, perhaps the best approach is to average the NP current across the whole line cycle [B14]. Although this approach can not determine either the size or the shape of the voltage ripple, it does show the trends and the overall stability of the dc-link voltage, and can be linearized and used to design a NP voltage controller.

Perhaps the first comprehensive approach to modeling three-phase PWM converters was presented by Ngo, et al. [F14]. The modeling was performed in four steps: development of the switching model, averaging, transformation in the rotating coordinates, and linearization. The converter models published thereafter [F2, F4, F15, F16] mainly followed the same steps and resulted converter models that describe the low-frequency dynamic behavior of currents and voltages of multilevel converters as well. Naturally, they do not describe the effects of the split dc-link capacitors, but under the usually valid assumption that the NP voltages can be controlled by the modulator and that the ripple is sufficiently small, they do accurately describe the low-frequency dynamic behavior.

Finally, it is important to mention an attempt to make a unified dynamic model [F8, F13] of a three-level converter that included the NP voltage dynamics together with all the other voltages and currents. The model was developed using the usual steps of developing the switching model first, than averaging, transforming into the rotating frame, and linearizing.

Unfortunately, in order to include the dynamics of the split dc-link capacitors, the switching model had to be developed using the phase instead of the line-to-line switching functions. This resulted in a large number of duty cycles to be controlled, altogether six for a three-phase converter. The linear model was than obtained by linearizing the average model in a rotating coordinate frame around the operating point. Clearly, the steady-state solutions of the linear model are constant duty cycles, which is only one of the infinite number of functions that steady-state duty cycles of the average (nonlinear) model can have. Essentially, in this case, the coordinate transformation and linearization reduces the number of possible solutions from infinity to one sub-optimal solution, thus taking away most of the freedom to optimize the switching patterns.

Therefore, although interesting from the theoretical point of view, by controlling good part of the modulation itself, this method effectively limits the freedom to optimize the switching patterns without offering additional insight into converter operation.

1.3 Dissertation Outline and Major Results

The work in this dissertation is divided into the following major parts.

Three-Level Diode-Clamped Converter. This chapter is, in a sense, an extended introduction that discusses the requirements that an effective power conditioning system for SMES needs to satisfy. At the same time, this chapter covers the topological, control design and modeling issues unique to the approach that was taken in the design of the prototype power processing converter that was designed as a part of this dissertation work. In addition, there is a discussion of how this approach compares with other available converter technologies, as well as the problems that were encountered and the original solutions that were proposed.

Implementation of a Three-Level Converter in a SMES Power Conditioning System. Finally, an approach to modeling and implementing a control system for a three-level NP-clamped converter for the application in the SMES system is presented. The control design enables the dc/ac converter of the power processing system to operate as a rectifier when the magnet is being charged, and as a utility inverter when the magnet is being discharged. The control design is based on a two-level dc/ac converter model that is experimentally proven to closely match the dynamic behavior of a three-level converter. Finally, specific requirements for the control of a dc/ac converter operating in an environment with frequent demands for changes in operating mode and power flow direction are discussed.

A fast SVM Algorithm for Multilevel Converters. This chapter introduces an original SVM algorithm for n-level three-phase converters. This algorithm is computationally extremely efficient and is almost independent of the number of levels of the converter. At the same time, it provides excellent insight into the operation of multilevel converters. In addition, the

experimental results from the operation of the prototype power conditioning converter are included as is the discussion of the algorithm's strengths compared with SVM algorithms. This chapter also covers the details of the real-time algorithm's implementation on the DSP processor using the example of a three-level space vector modulator.

Neutral Point Balancing Problem in Three-Level NP-Clamped Converters. It is known that under certain loading conditions and for certain output voltages a charge balance in the three-level converter can not be maintained on the switching cycle level. This results in the low-frequency voltage ripple in the NP, which is the point between the two dc-link capacitors. This chapter explores the fundamental limitations of the NP voltage balancing problem for different loading conditions of three-level voltage source converters. A new model in dq coordinate frame (utilizing current switching functions) is developed as a means to investigate theoretical limitations and lend to more insight into the problem. The low-frequency ripple of the NP (caused by certain loading conditions) is observed and quantified. The theoretical results are then experimentally verified and guidelines for choosing the dc-link capacitor size are given.

Feed-Forward Control of Three-Level Diode-Clamped-Converters. The results from the previous chapter indicate that under certain loading conditions, the low-frequency voltage ripple in the NP of the dc-link capacitors is to be expected. In this chapter, a feed-forward control strategy to compensate this ripple is presented for two modulation algorithms: a sine triangle and a space vector PWM algorithm. A full dynamic model is developed to help better understand the effect of the feed-forward algorithm on the quality of output waveforms as well as its effect on the control authority over the charge balance of the dc-link capacitors. Interestingly, the proposed algorithm seems to effectively compensate for the disturbance in the output voltage created by the voltage ripple in the NP, while simultaneously improving the control authority over the capacitor charge balance. Some of the theoretical results are experimentally verified.

2 MULTILEVEL CONVERTERS' MODULATION AND CONTROL

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive applications of this technology are in the medium- to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications.

In general, multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occur in series-connected devices.
- Spectral performance of multilevel waveforms is superior to that of their two-level counterparts.
- Multilevel waveforms naturally limit the problems of large voltage transients that occur due to the reflections on cables, which can damage the motor windings and cause other problems.

The selection of the best multilevel topology and the best control strategy for each given application is often not clear and is subject to various engineering tradeoffs. By narrowing this

study to the DC/AC multilevel power conversion technologies that do not require power regeneration, several attractive topological, modulation and power semiconductor device choices present themselves. The most actively developed of these multilevel topologies are listed in Figure 2.1.

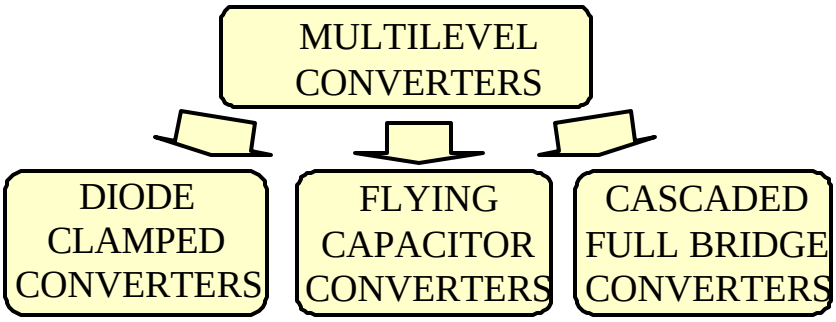

Figure 2.1. Multilevel converter topologies.

Similarly, the modulation strategies, with their rich variety of techniques, can be roughly divided, as shown in Figure 2.2.

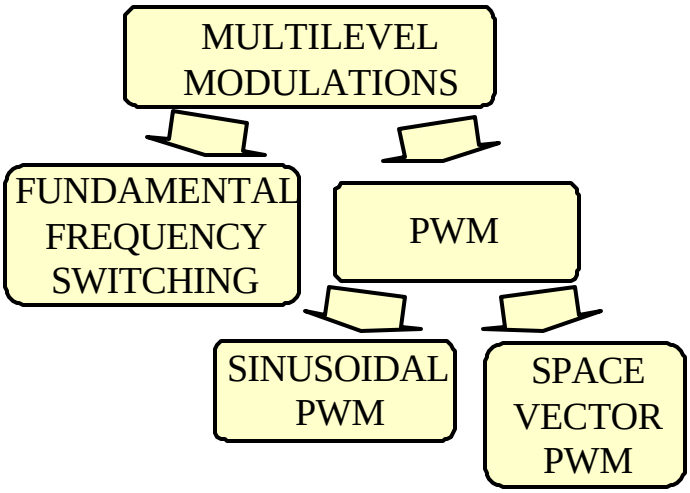

Figure 2.2. Multilevel modulation techniques.

2.1 Multilevel Topologies

Although definitions may vary, in this document the multilevel converter has three- or more levels. The intention is to give a brief review of the three basic topologies and their most promising derivatives. Although this section is by no means a complete review of all the multilevel topologies, it does cover the ones that are presently receiving the most attention.

2.1.1 Diode-Clamped Multilevel Topology

The first practical (and still widely studied) multilevel topology is the neutral-point-clamped (NPC) PWM topology first introduced by Nabae, et al., in 1980 [B1]. The three-level version of this topology, shown in Figure 2.3, has several distinct advantages over the two-level topology.

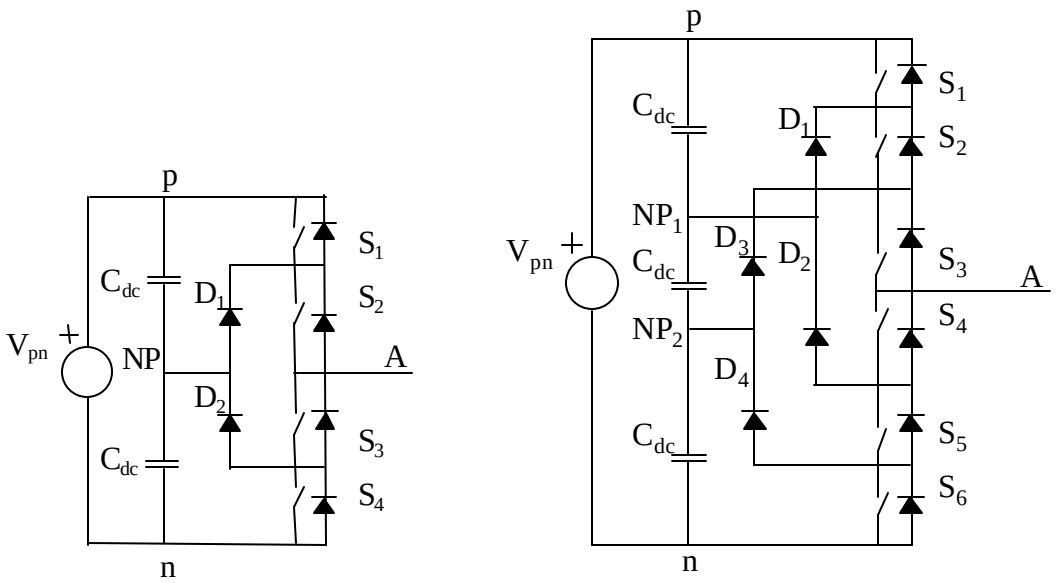

Figure 2.3. The three- and four-level neutral-point-clamped phase leg.

The advantages are:

- Voltages across the switches are only half of the dc-link voltage.
- The first group of voltage harmonics is centered around twice the switching frequency.

- This topology can be generalized, and the principles used in the basic three-level topology can be extended for use in topologies with any number of levels.

However, practical experience with this topology revealed several technical difficulties that complicate its application for-high power converters. These are as follows:

- This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress. Although measures to alleviate this problem can be applied, this remains a serious consideration.
- For topologies with more than three levels the clamping diodes are subject to increased voltage stress equal to $V_{pn}\cdot(n-1)/n$. Therefore, series connection of diodes might be required. This complicates the design and raises reliability and cost concerns.
- The issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three-levels. Although the three-level NPC topology works well with high power factor loads, NPC topologies with more than three levels are mostly used for static var compensation circuits. This may be due to the capacitor balancing issues if the nearest three vector (NTV) modulation is used (which is the modulation scheme with the least amount of stress and superior spectral performance, and which is therefore preferred over other possibilities).

2.1.2 Flying Capacitor Multilevel Topology

The flying capacitor multilevel topology from Figure 2.4, was first proposed in 1992, and is considered to be the most serious alternative to the diode-clamped topology.

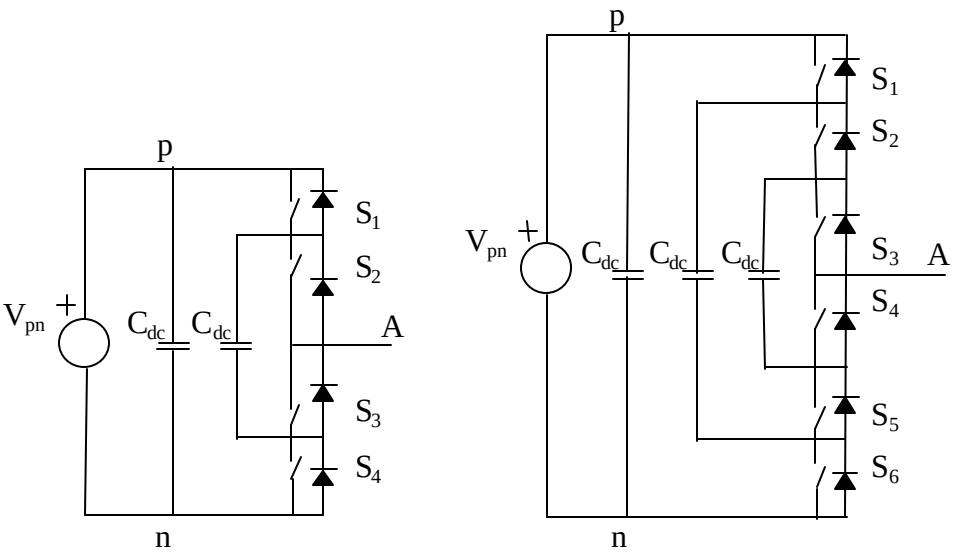

Figure 2.4. Three- and four-level flying capacitor phase leg.

The significant advantage of this topology is that it eliminates the clamping diode problems present in the diode-clamped multilevel topologies. Additionally, this topology naturally limits the dV/dt stress across the devices and introduces additional switching states that can be used to help maintain the charge balance in the capacitors. Unlike the diode-clamped converter, the flying capacitor topology has enough switching states to control the charge balance in the single isolated leg with converters having any number of levels, even if the phase current is unidirectional. This makes this topology attractive even for the dc/dc converters.

At the present time it seems that this topology has few disadvantages. Nevertheless, some possible "weak points" that still need to be explored are:

- The dc-link capacitor charge controller adds complexity to the control of the whole circuit.
- The flying capacitor topology might require more capacitance than the equivalent diode clamped topology. In addition, it is obvious that rather large rms currents will flow through these capacitors. A study of the tradeoffs involved is not described in the available literature.
- There is a potential for parasitic resonance between decoupling capacitors.

2.1.3 Multilevel Configurations with Cascaded Two-Level Full-Bridge Inverters

One of the early applications of the series connection of single-phase full-bridge inverter topology was for plasma stabilization in 1988 [13]. This modular approach has since been extended to include three-phase systems as well, and is probably most successfully applied by Robicon, with their line of medium-voltage drives, which reportedly have an excellent field record.

Arguably, the overall complications and cost of the isolated sources for each full bridge is overall not too serious a drawback and is offset by the advantages of modular construction. The modularity of this structure allows easier maintenance and provides a very convenient way to add redundancy into the system [20]. The five-level phase leg of the cascaded two-level full-bridge converter is given in Figure 2.5.

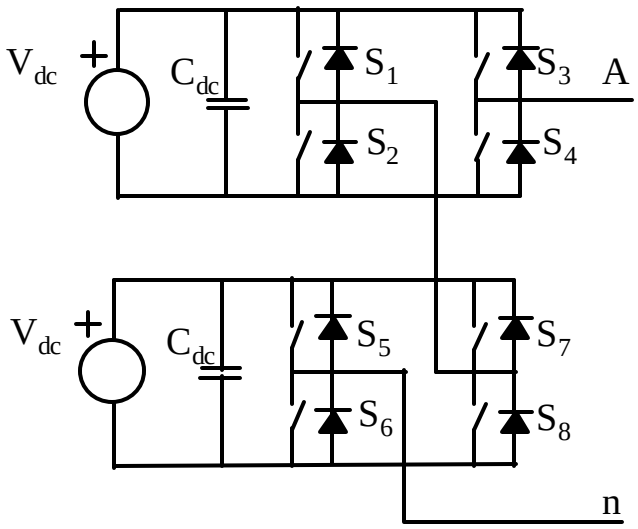

Figure 2.5. Phase leg of a cascaded five-level full-bridge inverter.

One major advantage of this hybrid approach is that the number of output can be further increased without addition of any new components, requiring only the dc sources with different voltage levels [D9]. Probably the most advantageous uses the dc-sources with two different voltage levels, V_{dc} and $2 \cdot V_{dc}$, as shown in Figure 2.6.

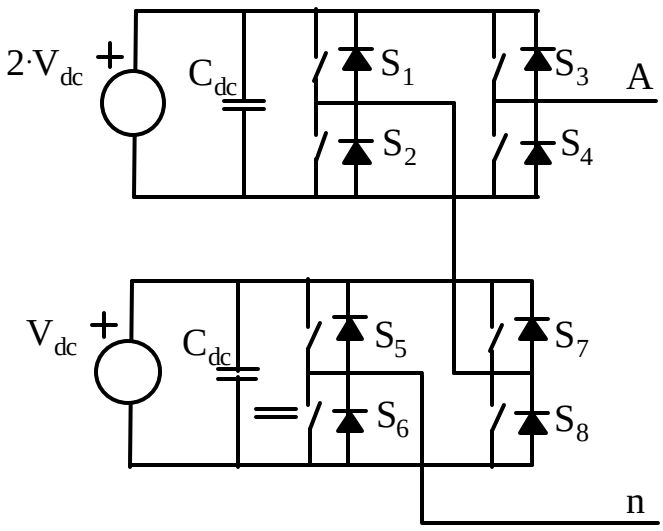

Figure 2.6. Phase leg of a cascaded full bridge seven-level converter.

This approach can then be implemented using hybrid device technology [D9]. In that arrangement, the slower, higher-voltage devices can be used to change the output voltage level (S_1, S_2, S_3, S_4), while the faster, lower-voltage devices can provide the full PWM capability between levels (S_5, S_6, S_7, S_8). This arrangement can generate seven-level (0,+/-V_{dc},+/-2·V_{dc},+/-3·V_{dc}) fully pulse width modulated output voltage.

2.1.4 Additional Full-Bridge Topologies

Compared to cascaded full-bridge inverters, some savings on isolation of dc power supplies can potentially be achieved using full-bridge multilevel topologies. GE already successfully applied this approach in their medium-voltage (4160V) drive product. They relied on well-understood three-level NPC topology to build the full-bridge five-level phase leg. This topology has enough redundant switching states to allow the charge balancing of the dc-link capacitors on a switching cycle level for all line/load conditions. However the difficulties with the clamping diodes still remain, as does the need for isolated dc-voltage source for every phase.

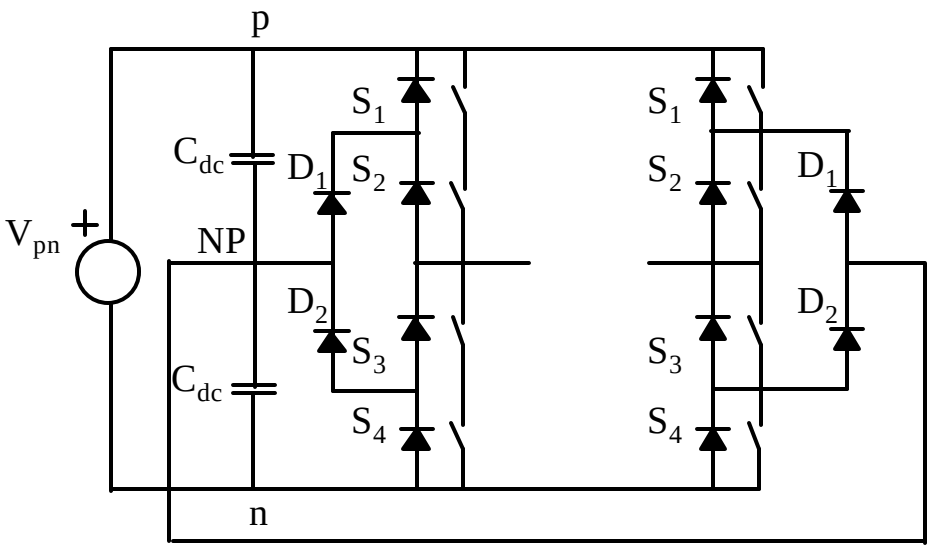

Figure 2.7. Diode clamped full bridge five-level topology.

Using the same philosophy, a full-bridge five-level phase leg can be built, based on the flying capacitor topology, as shown in Figure 2.8. Very similar to the flying capacitor half-bridge topology, this approach alleviates the clamping diode issues, but introduces the issues of clamping capacitors instead. Both these multilevel design approaches have yet to be proven in real-life applications.

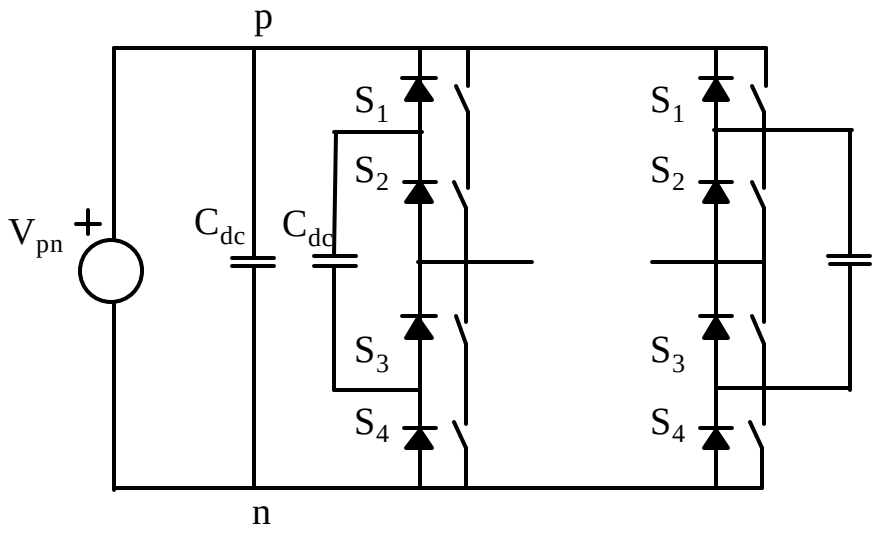

Figure 2.8. Flying capacitor full-bridge five-level topology.

2.2 Multilevel Digital Control Hardware

The complexities of the multilevel converters' systems, together with the increase in power, performance and availability (as well as the decrease in price) of digital control hardware, result in almost exclusive application of digital control hardware for the majority of modern multilevel converters and converter systems. In addition, the versatility of modern microprocessors allows them to be used for the control of any type of converter, and allows implementation of any type of modulation algorithm. At the same time, the ever-increasing processing power of microprocessors allows for much more user-friendly development tools that can accept input from higher programming languages such as C and (increasingly) Matlab.

2.2.1 Overview of the Architecture of Digital Control Hardware

Regardless of the topological differences, the direction of power flow, or its application in almost every power electronics system, has few main components, such as the switching network with filter components on both input and output, the sensors subsystem, the power terminals and a (digital) control subsystem.

Similarly, the architecture of modern digital controllers can be subdivided into several major functional blocks from Figure 2.10. The central element is the processor (or a combination of several processors) usually accompanied by some kind of programmable logic devices to implement the PWM (if this capability is not already provided on the processor). In addition, programmable logic devices provide the simplest way to implement some specific protection functions that require very fast response speed as well as any "glue" logic required to interface the processor with other components on the control board.

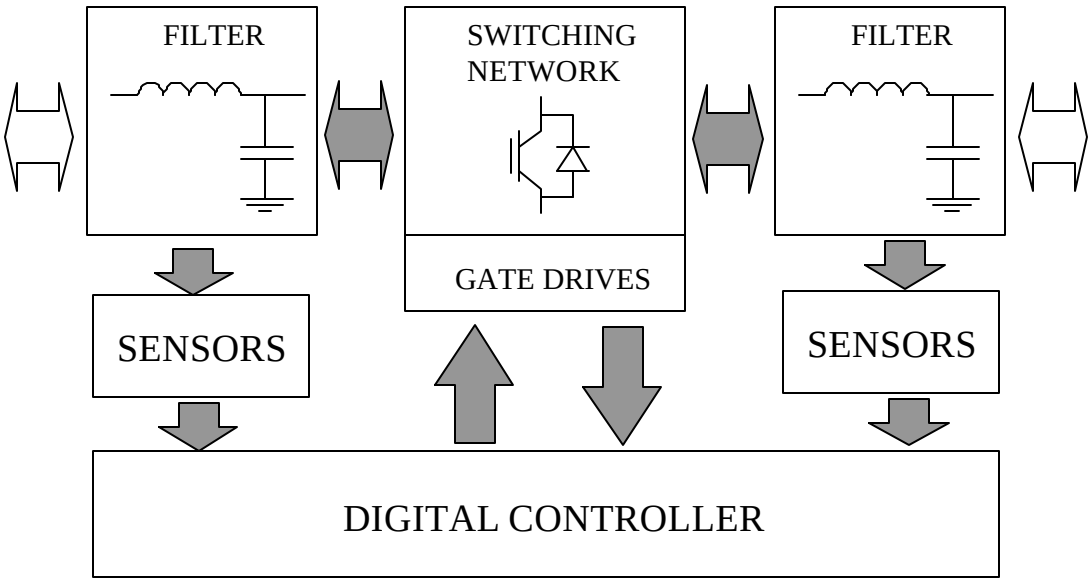

Figure 2.9. Power electronics system overview.

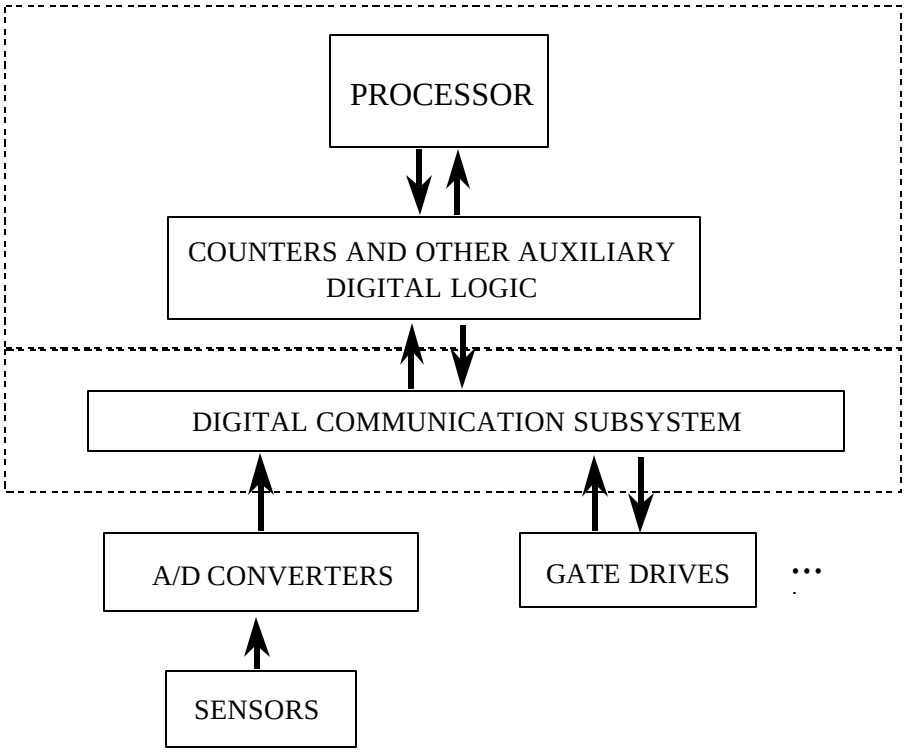

Figure 2.10. Architecture of the digital controller for power electronics systems.

This traditional structure of the controller is being challenged as part of the development of the power electronic building block concept and the introduction of the digital communication subsystem. Such a subsystem (although still in the development phase, and with uncertain future), has the potential to standardize the signal distribution network across the whole range of power electronics products from different manufacturers. Although different implementations have been proposed the main idea is to establish a standardized communication protocol, most likely through a serial fiber optic link [F17, F18]. If accepted the standardized protocol would allow any processor to control and communicate with all elements of the power electronic system, regardless of their manufacturer, as long as they support the same protocol. The elements considered for communication upgrade range from single switches or phase legs with integrated sensors, remote sensors, or the whole converters. In addition, such a system would be easy to service/upgrade by adding or replacing various modules.

2.2.2 Components of the Digital Controller for SMES Power Conditioning System

The digital controller hardware partially developed for the control of the SMES PCS consists of the digital signal processor, boot memory, erasable programmable logic device (EPLD), analog-to-digital (A/D) converter, and digital-to-analog (D/A) converter. Since most of the feedback transducers generate analog signals, A/D converters are required to convert those signals to the digital format, which is suitable for the processor. The EPLD can be programmed to perform any digital operation. This allows a part of the control logic to be implemented in hardware. The D/A converters are very useful for system debugging and measurement of the variables internal to the processor. The design and choice of components for the SMES digital controller are listed as follows.

Processor

The present system is based on the Analog Devices ADSP 21062 (SHARC) processor. It is a 32-bit floating point processor with a throughput of 40 MIPS. It has a 1M bit of on-chip program memory and a 1M bit of on chip data memory. This powerful processor is a perforce

requirement for power electronics control systems that execute sophisticated algorithms at high sampling rates.

Programmable Logic Device

The EPLD can be electrically programmed to implement any logic functions. The most important selection criteria for the EPLD are the speed, number of flip-flops and usable gates as well as the number of I/O pins that can be configured. This limits the maximum size of the logic circuitry that can be implemented with any given EPLD. At the time of the board development two, FLEX 8820 chips from ALTERA looked like a very good choice. Each chip has 8000 usable gates, 820 flip-flops and 152 pins that can be user defined as input, output or input/output.

Analog to Digital Converter

The processor acquires the analog feedback signals from the plant through A/D converters. The most important selection criteria for the A/D converters are the conversion time, and the resolution. In the present design, the AD876, 10-bit 20 MSPS A/D converters from Analog Devices were used.

Digital to Analog Converter

In PWM-based systems, D/A converters are mostly used for debugging and transfer function measurement, so their performance is not critical. We have chosen Quad, 12-bit DAC8412 converters from Analog Devices, with 180ns write cycle time.

2.2.3 Controller Architecture

Figure 2.11 shows the block diagram of the DSP-based controller. It can be divided into three functional subsystems, implemented on separate printed circuit boards:

- DSP subsystem
- Digital interface subsystem with flex EPLDs
- Analog interface subsystem with A/D and D/A converters

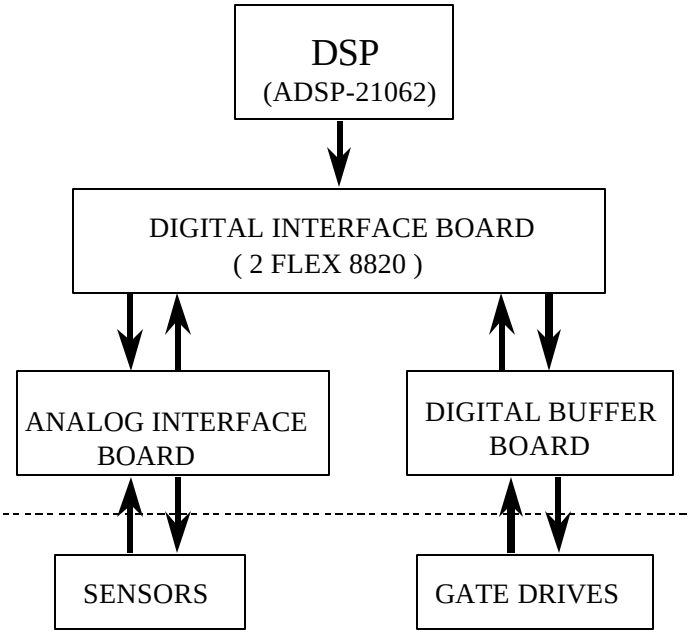

Figure 2.11. Architecture of the SMES digital controller board.

DSP Processor Board

The ADSP-21062 EZ-LAB from Analog Devices, used in this project is a complete development system based on the ADSP 21062 (SHARC) processor. It allows the use of EZ-ICE In-Circuit Emulator and facilitates communication with additional modules through the SHARCPAC expansion connectors, that let the user add additional memory and/or SHARC processors. In the present design the SHARCPAC expansion connectors are used to interface with digital interface board.

Digital Interface Board

The digital interface board from Figure 2.12 consists of two back-to-back connected EPLDs. These EPLDs share the address/data and control lines with the processor. The EPLDs can be programmed using a serial cable from a personal computer (PC) or using the programmable read only memories (PROMs). This board performs the majority of the PWM generation and system protection tasks such as shutdown at repeated fault signal from gate drives, watch dog timer function and shoot through protection.

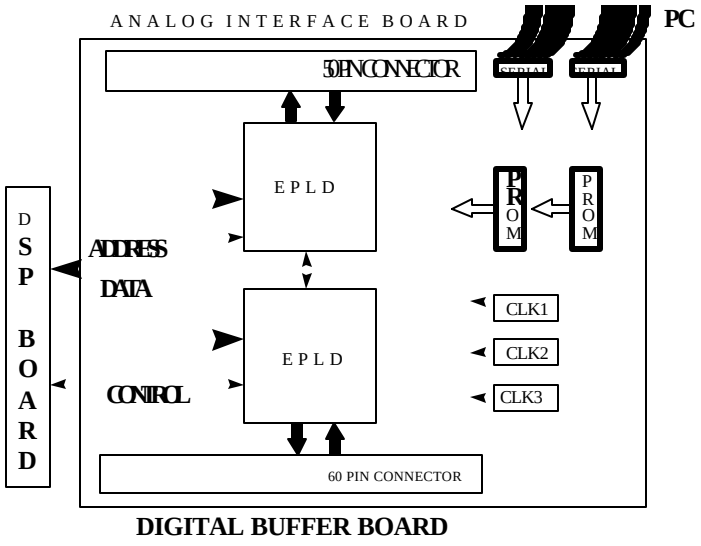

Figure 2.12. Digital interface board.

Analog Interface Board

Figure 2.13 shows the functional block diagram of the analog interface board. Sixteen analog input channels are being level-shifted, inverted and filtered, and then fed to two analog multiplexers (both 2 x 4-to-1). The outputs of the multiplexers are routed to four A/D converters, which are all connected to the digital interface board via common data lines. The main consideration in the choice of architecture was not so much the throughput as it was the

nearly instantaneous sampling, which can not be achieved using a single converter with multiplexed input (the limitation primarily lies in the speed of the multiplexers). The analog interface board also has 8 analog outputs, all of which are buffered using voltage followers, and two of which drive the current transmitters that can be used to feed long cables.

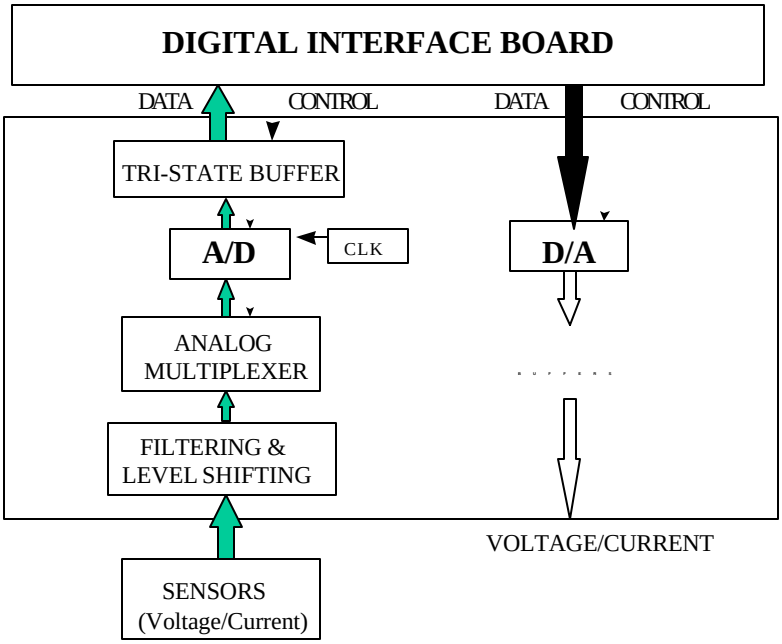

Figure 2.13. Analog interface board.

2.2.4 Control Algorithm

The primary tasks of any controller are regulation and pulse width modulation. The block diagram of the control structure is shown in Figure 2.14. The process begins with the sensing of output voltages and line currents (INPUT). These are then transformed from stationary three-phase (abc) to rotating three-phase (dqo) coordinates and compared with reference values to generate errors. The error signals are processed in a compensator and the result is transformed back to abc coordinates (T-1). Then the modulator takes over and selects the switching states and duty cycles that implement the commanded reference vector from the compensators. Up to this point the complete algorithm is implemented in software.

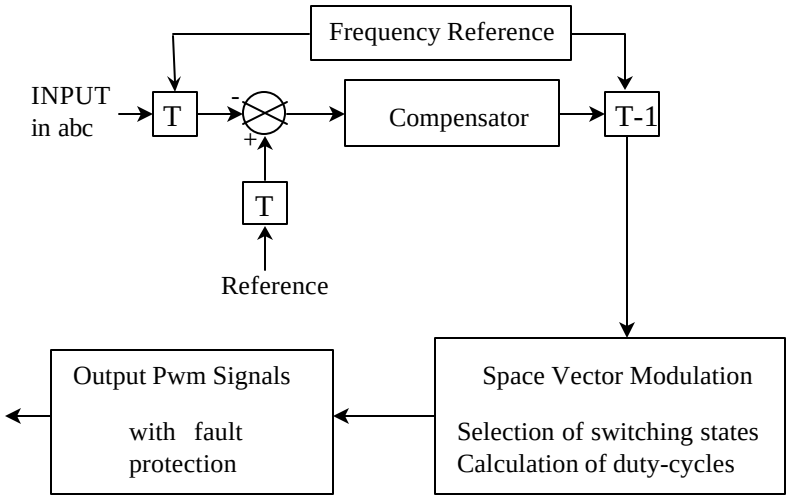

Figure 2.14. Control overview.

Finally the PWM generation is implemented in hardware requires many timers to keep track of the time elapsed (duty cycles) and some combinatorial logic to change between the switching states.

2.2.5 Functions of the EPLD

The main function of the EPLD is to generate the PWM signals that are fed into the inverter gate drives, based on the data received from the DSP. A functional block diagram of the EPLD logic responsible for generating the PWM signals is shown in Figure 2.15.

The DSP receives periodic interrupt requests (IRQ) from the EPLD at switching frequency ($1/T_S$), which is equal to the control sampling frequency. After receiving an IRQ, the processor reads the feedback variables from the A/D converters and calculates the switching states and their duty cycles according to the algorithm described in the previous section. These are then loaded into the double-buffered register bank in the EPLD to be used in the following switching cycle. The processor then enters the idle state until receiving new IRQ.

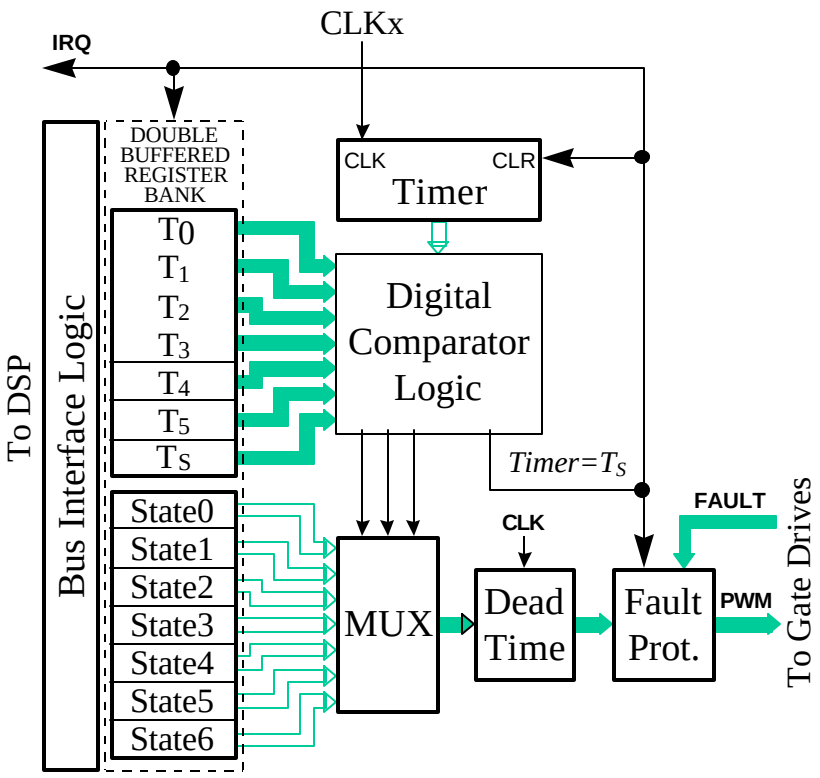

Figure 2.15. PWM signal generation logic within the EPLD.

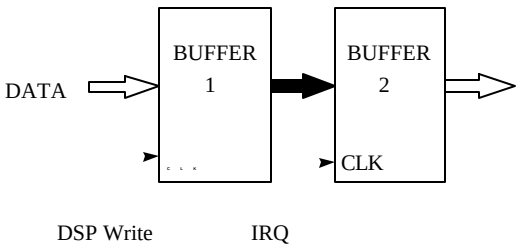

Figure 2.16. A double-buffered register bank inside the EPLD.

The double-buffered register bank consists of timer registers and state registers, the numbers of which vary for different applications. Each register is double-buffered, as shown in Figure 2.16, so that the PWM data used in the current switching cycle (BUFFER 2) is not affected by

the asynchronous DSP write into BUFFER 1. The fresh data is loaded into BUFFER 2 by an IRQ signal at the beginning of each switching cycle.

The state registers contain those switching-state codes which are used for PWM in the current switching cycle, ordered in the sequence in which they will be applied. The timer registers contain the duty-cycle information, *i.e.,* the times from the beginning of the switching cycle (measured in the units of EPLD CLK period) when the corresponding switching state ends.

Generation of PWM Signals

The timer in Figure 2.15 is a free-running counter with the same length as the timer registers in the register bank. It can be fed by any of the three clock signals available on the digital interface board (CLK1, CLK2, CLK3 in Figure 2.12). The counter is cleared by the IRQ signal at the beginning of each switching cycle. The Digital Comparator Logic and MUX in Figure 2.15 sequentially output the switching states using the current data in the double-buffered register bank. After the timer reaches T_S, digital comparator logic generates the IRQ signal which starts a new switching cycle by interrupting the processor, loading the new data into the double-buffered register bank, and clearing the timer counter.

Dead-Time Protection

Dead-time protection is provided to avoid any shoot through of the inverter legs. This is done by delaying the rising edges of all the signals by a particular number of clock cycles, as shown in Figure 2.17.

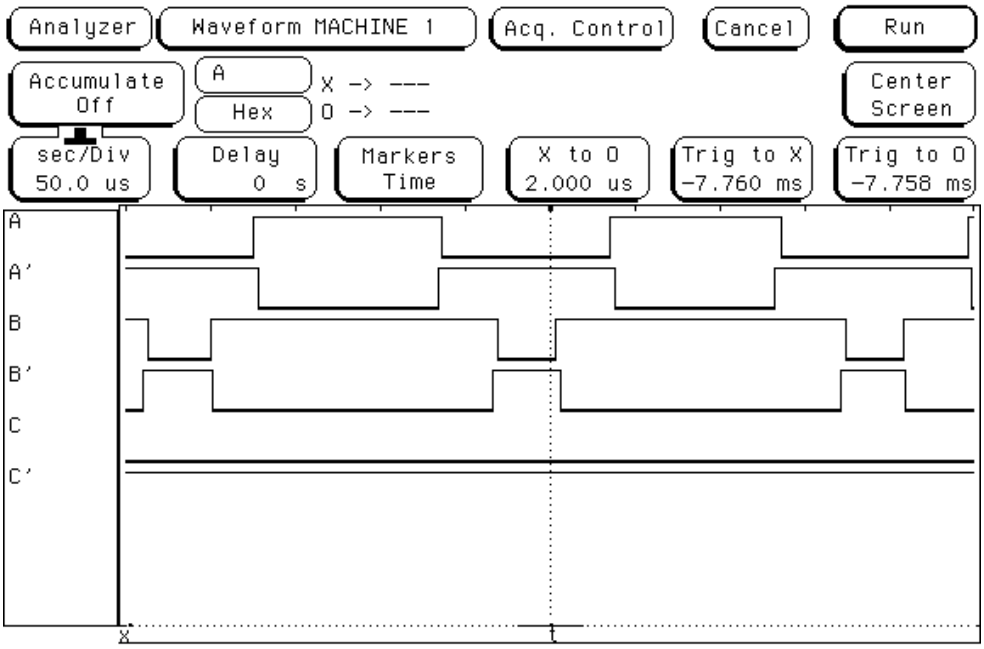

Figure 2.17. Inverted gate drive signals with dead-time.

Fault Protection

In the event of a fault, the PWM signals are shut down to save the power stage. Two kinds of fault protection have been provided: internal and external. If for some reason the PWM signals received from the dead-time block are such that they turn on the top and bottom switches of a given phase leg, then a fault signal is generated inside the EPLD (internal fault) and the PWM pulses are shut down. The internal fault can also be generated by the watchdog timer. These conditions should not occur under normal operating conditions. They are a protection against software failure.

External fault protection is activated when a gate driver senses an over-current through the power device and sends a fault signal to the digital buffer board. This fault signal is passed to the EPLD where it enables an IRQ counter. If the fault persists for a particular number of switching cycles (this number can be programmed into the IRQ counter), the PWM signals are shut down. In this way, the complete inverter is not shut down if the over-current condition happens in only

a couple switching cycles, which is acceptable because the gate drives automatically turn off the switch whenever over-current is detected.

Other EPLD Functions

The analog interface board has four A/D converters and two D/A converters that all communicate through the same 12-bit data bus. In addition, the processor and A/D converters have different frequency clocks that are not synchronized. Therefore, to insure proper operation of the board, the timing of the control signals is critical. The logic that receives signals from the analog interface board and takes care of synchronization is implemented inside the EPLD. In addition, the system watchdog timer and the address decoding of the input and output ports are also implemented in the EPLD.

2.3 Multilevel Power Conditioning System as a Power Controller for a Superconducting Magnetic Energy Storage System

Historically, most of the interest in SMES systems seems to have been shown for utility type applications. The main motive was to combine the flexibility of an energy storage system with the ease of control provided by power electronics. In fact, by providing a buffer between the power generation and load consumption, the ease of control and operational flexibility of power systems could be greatly increased. There are certainly other utility-type applications to which SMES systems could be applied, such as active filtering, supplying pulse power load and UPS applications.

The main challenge in developing such a PCS is to match the constant ac voltage and variable current operation of the utility with the slowly varying current and varying voltage of the magnet, while at the same time providing bi-directional power flow.

In addition, there is one rather unique characteristic of SMES systems: both dc voltage and dc current vary over a large range. This feature implies that the PCS must be overrated relative to the designed power transfer levels by a factor of three to four, or even more. This feature is one of the main reasons why the current source inverter is not a preferred way to design a SMES PCS while the series connection of a dc/dc chopper and ac/dc voltage source inverter (VSI) is. Clearly the later approach can have significant cost advantage because the whole system does not have to be overrated (only dc/dc converter).

2.3.1 Power Conditioning System Design approach

Consistent with the preceding discussion, the PCS that was studied in this dissertation is implemented using a combined chopper/VSI approach. Considering the various tradeoffs (already mentioned), the three-level diode-clamped topology was chosen. Figure 2.18 shows the topology of the prototype PCS. Some of the advanced features of the system include the zero-current-transition (ZCT), soft switching technique, which allows the system to be rated at 250kVA, while switching with the 20kHz switching frequency. The details of the power stage and the intricacies of the soft-switching design and control are the part of the doctoral research of Dr. Dong-Ho Lee, and are described in detail in his work [G9].

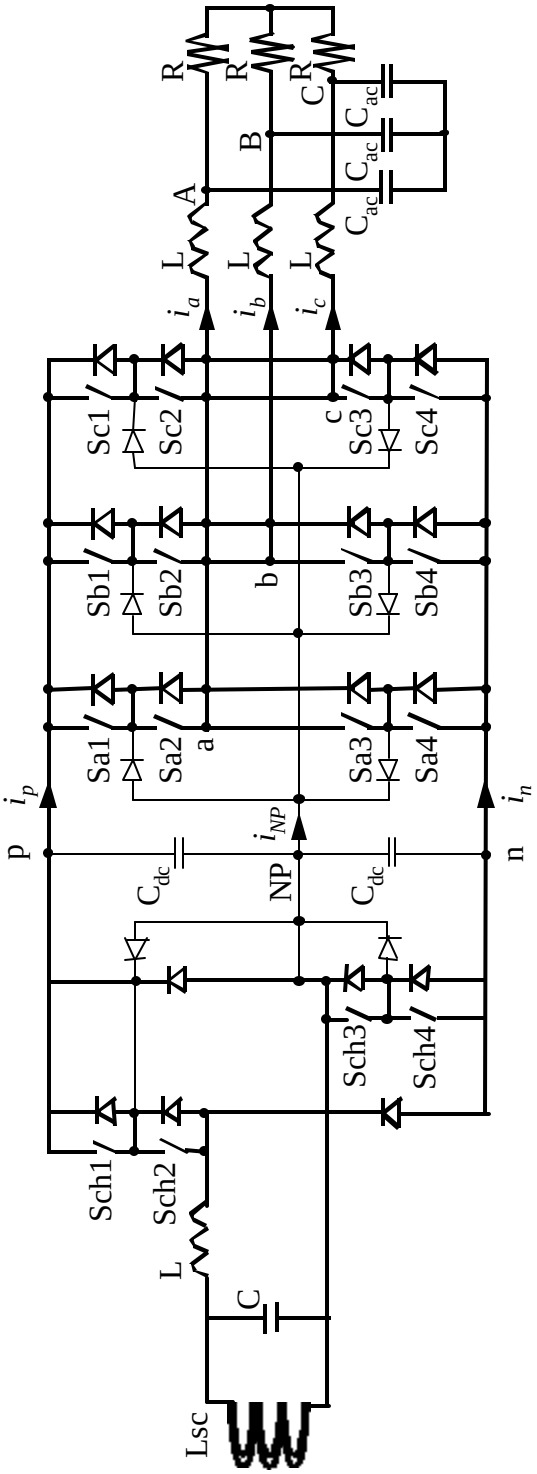

Figure 2.18. Power conditioning system for SMES.

2.3.2 Modeling and Control of the Chopper

A functional diagram of the three-level chopper is given in Figure 2.19. The task of the chopper is to control the power flow to and from the superconductive coil (SC). The circuit is bi-directional and, to avoid confusion, the SC side of the circuit is defined as the output side, while the side interfacing with the inverter is defined as the input side. Current direction in the SC is always the same so that the voltage on the filter capacitor, V_{sc}, determines the power flow.

Fig. 2.20 shows the output voltages given in the form of space voltage vectors that are produced with different switching combinations of the Chopper. Although the space vector notation is not common for the dc/dc converters, such as in this case chopper, it is adopted here because it is consistent with the space vector notation introduced for the VSI in Section 2.3.4

The voltage vectors in Fig. 2.20 are named according to the switching combinations used to produce them. For example, if in Figure 2.19, switch S_x is connected to the p-rail and switch S_y is connected to the NP, the output voltage vector is **po**. There are nine vectors in all: two large vectors (**pn**, **np**) that produce output voltages of opposite polarity with the magnitude equal to the dc-link voltage, V_{pn}; four small vectors (**po**, **on**, **no**, **op**) with magnitude equal to $V_{pn}/2$; and three zero-voltage vectors (**pp**, **oo**, **nn**).

The task of the chopper modulator is to synthesize the voltage reference vector, V_{xyREF}, which is a dc voltage and is always located on the V_{DC} axis shown in Fig. 2.20. The modulation scheme in which the reference vector V_{xyREF} is synthesized from the two closest vectors is adopted and will be discussed here. The advantage of this scheme is that it minimizes the voltage ripple on the SC and allows for effective control of the NP voltage balance.

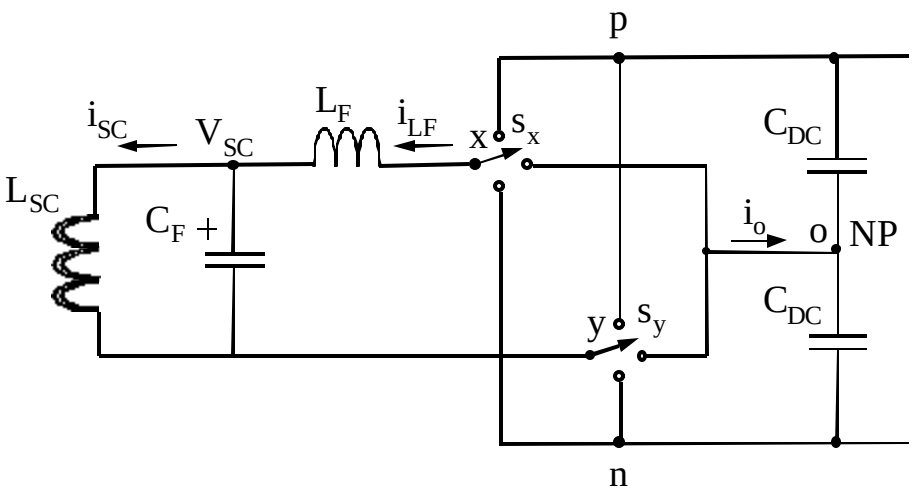

Figure 2.19. Equivalent switching model of three-level chopper.

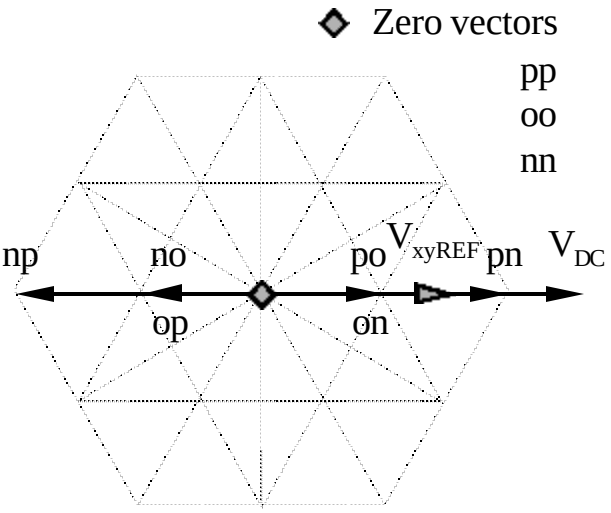

Fig. 2.20. Space voltage vectors of the chopper.

If we define the duty cycle as $d = \left| V_{xyREF} / V_{pn} \right|$, where $d \in [0,1]$, then for $d \in [0,0.5]$, the duty cycles of large, small and zero vectors are given by

(2-1) $d_L = 0$,

(2-2) $d_S = 2 \cdot d$ and

(2-3) $d_0 = 1 - 2 \cdot d$,

respectively, where small vectors **po** or **on** should be used for $V_{xyREF} > 0$, and **no** or **op** for $V_{xyREF} < 0$. For $d \in (0.5,1]$ duty cycles are given by

(2-4) $d_L = 2d - 1$,

(2-5) $d_S = 2 - 2d$ and

(2-6) $d_0 = 0$,

where vectors **pn**, **po** and **on** are used for $V_{xyREF} > 0$, while **np**, **no** and **op** are used for $V_{xyREF} < 0$.

Large vectors and zero vectors do not produce any NP current, i_{NP}, and hence do not affect the NP voltage. Small vectors come in pairs. Both vectors in a pair generate the same output voltage, but they produce the current i_{NP} in opposite directions, as shown inTable 2-I. The vectors resulting in $i_{NP} = i_{LF}$ are referred to as positive small vectors, while the vectors resulting in $i_{NP} = -i_{LF}$ are called negative small vectors. The task of the NP voltage controller is to select from the redundant small vectors in

, with the objective of minimizing the NP current and maintaining the NP voltage as close as possible to one-half of the dc-link voltage.

Table 2-I Neutral-point current i_{NP} for different small vectors.

V_{xy}	Positive Small Vectors	i_o	Negative Small Vectors	i_o
$V_{np}/2$	**po**	i_{LF}	**on**	$-i_{LF}$
$-V_{np}/2$	**no**	i_{LF}	**op**	$-i_{LF}$

Neutral-point control issues notwithstanding, the average model of the rectifier is not different from the average model of a bi-directional two-level converter from Figure 2.21. The modulation index is defined as $m = V_{xyREF}/V_{pn}$. Clearly, the duty cycle is then given by $d = |m|$ and the switch duty cycles can be easily calculated from (2-1)-(2-6).

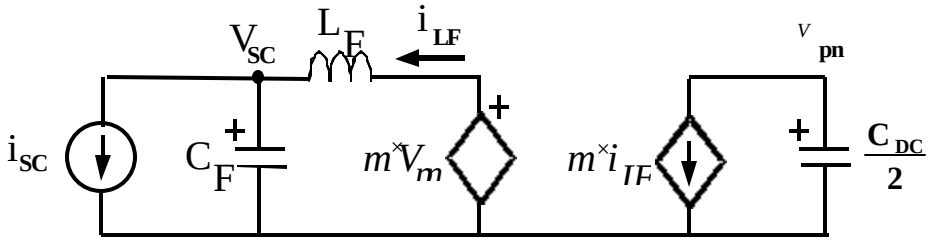

Figure 2.21. Average model of the chopper.

The average model is similar for both modes of operation; there is only a slight difference in the control design. In the charging mode, the chopper operates as a buck dc/dc converter with the inner current loop and the outer voltage loop, Figure 2.22. In the discharging mode, the chopper operates as a boost dc/dc converter, Figure 2.23.

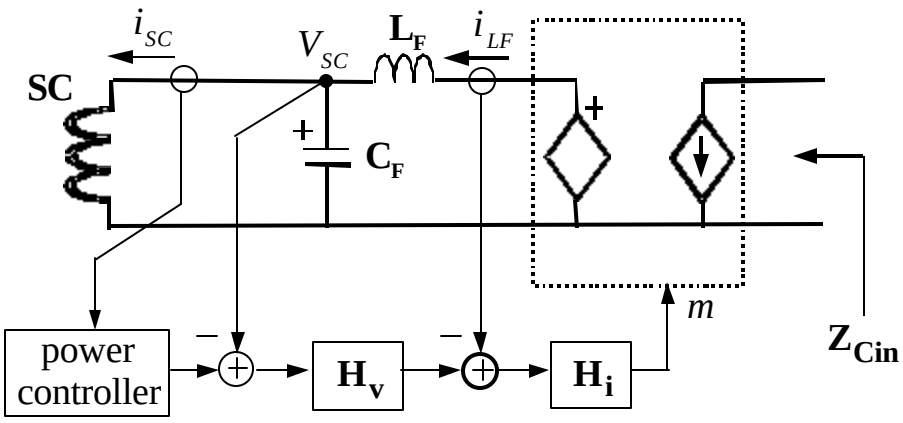

Figure 2.22. Buck mode control of the chopper (charging the SC).

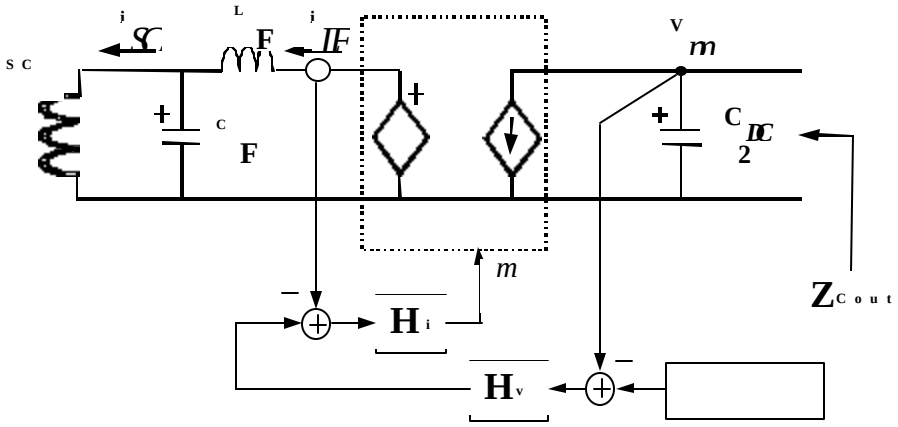

Figure 2.23. Boost mode control of the chopper (discharging the SC).

2.3.3 Modeling of a Three-Level Voltage Source Inverter

A functional diagram of a three-level VSI switching network is given in Figure 2.24. The subsequent analysis will reveal a few important properties of this type of converter. It will show that the error in the NP, Δv_{pn}, does not dynamically influence the output voltages V_{ab}, V_{bc}, V_{ca}, but rather in a static way determined by the type of modulation and the NP-balancing method applied. This result justifies application of the static method for the study of the NP-balancing problem, such as the one described in [B20]. Additionally, it will be shown that the error in NP, Δv_{pn}, depends only on the NP current i_o and is not directly influenced by any other circuit parameters.

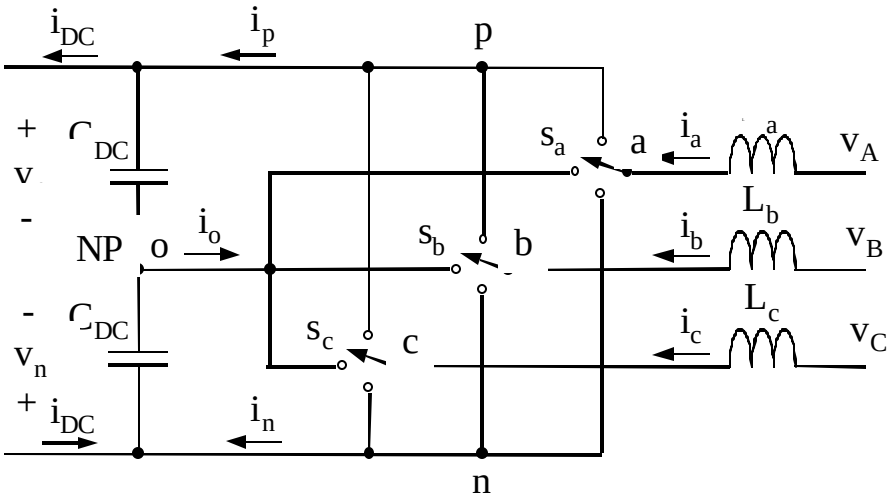

Figure 2.24. Switching network of a three-level VSI

Equation (2-7) shows the definition of the switching functions that are used in (2-8) to write the switching network voltages referenced to the NP.

$$\sum_{\substack{i\in\{a,b,c\}\\ j\in\{p,o,n\}}} s_{i,j} = 1, \quad where \quad s_{i,j} = \begin{cases} 1 & if\ i\ is\ connected\ to\ j \\ 0 & otherwise \end{cases} \tag{2-7}$$

(2-8)
$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} s_{ap} & s_{an} \\ s_{bp} & s_{bn} \\ s_{cp} & s_{cn} \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \end{bmatrix}$$

From the definitions in (2-7) and (2-8) and by inspection of the switching network in Figure 2.24, line-to-line voltages can be written (2-9) as follows:

(2-9)
$$\mathbf{v_{sn}} = \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} s_{abp} & s_{abn} \\ s_{bcp} & s_{bcn} \\ s_{cap} & s_{can} \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \end{bmatrix}$$
$$where: \; s_{abp} = s_{ap} - s_{bp} \quad s_{abn} = s_{an} - s_{bn} \ldots$$

By rewriting the voltages of the top and bottom dc-link capacitor in terms of the full dc link voltage and the NP error voltage (2-10), additional insight can be gained into the effect of the NP voltage error, Δv_{pn}.

(2-10)
$$v_p = \frac{v_{pn}}{2} + Dv_{pn}, \; v_n = -\frac{v_{pn}}{2} + Dv_{pn}$$

By substituting (2-10) into (2-9), as in (2-11), it becomes clear that the line-to-line voltage depends on the DC-link voltage and the error of the NP, and there is no dynamic coupling between the two.

(2-11)
$$\mathbf{v_{sn}} = \begin{bmatrix} s_{abp} - s_{abn} \\ s_{bcp} - s_{bcn} \\ s_{cap} - s_{can} \end{bmatrix} \cdot \frac{v_{pn}}{2} + \begin{bmatrix} s_{abp} + s_{abn} \\ s_{bcp} + s_{bcn} \\ s_{cap} + s_{can} \end{bmatrix} \cdot Dv_{pn} =$$
$$= \mathbf{S} \cdot \frac{v_{pn}}{2} + \mathbf{S_{np}} \cdot Dv_{pn}$$

Defining the current vector as in (2-11), (2-12) and (2-13) can be written. Note that the vector $\mathbf{i_{sn}}$ influences the NP current i_o through the same matrix of switching functions as the error of the NP voltage, and that there is no dynamic relationship between these two either.

(2-12) $$\mathbf{i_{sn}} = \frac{1}{3} \cdot \begin{bmatrix} i_a - i_b \\ i_b - i_c \\ i_c - i_a \end{bmatrix}$$

(2-13) $$\begin{bmatrix} i_p \\ i_n \end{bmatrix} = \begin{bmatrix} s_{abp} & s_{bcp} & s_{cap} \\ s_{abn} & s_{bcn} & s_{can} \end{bmatrix} \cdot \mathbf{i_{sn}}$$

(2-14) $$i_o = i_p + i_n = \left[\mathbf{S_{np}}\right]^T \cdot \mathbf{i_{sn}}$$

At last we can derive equation, (2-15), which describes the dynamic relationship between the NP current i_o and the voltage error of the NP, Dv_{pn}. This equation completely describes the dynamics of the voltage error in the NP and will be included in the complete state-space model of the switching network.

(2-15) $$\begin{aligned} i_o &= \left(i_{DC} + C_{DC} \cdot \frac{dv_p}{dt} \right) + \left(-i_{DC} + C_{DC} \cdot \frac{dv_n}{dt} \right) = \\ &= C_{DC} \cdot \frac{d}{dt}\left(\frac{v_{pn}}{2} + Dv_{pn} \right) + C_{DC} \cdot \frac{d}{dt}\left(-\frac{v_{pn}}{2} + Dv_{pn} \right) = \\ &= 2 \cdot C_{DC} \cdot \frac{d}{dt}\left(Dv_{pn} \right) \end{aligned}$$

Finally, from Kirchof's current and voltage laws and the definitions given, a dynamic relationship between input and output quantities of the three-level switching network can be obtained (2-16), (2-17). Combining these equations with the result of the derivation in (2-15), a full set of dynamic equations describing the three-level switching network is developed. This model is general, complete and makes no assumptions.

(2-16)
$$\frac{d}{dt}\left(\mathbf{i_{sn}}\right)=\frac{1}{3\cdot L}\cdot\mathbf{v_u}-\frac{1}{3\cdot L}\cdot\left[\mathbf{S}\right]^T\cdot\frac{v_{pn}}{2}+\\+\frac{1}{3\cdot L}\cdot\left[\mathbf{S_{np}}\right]^T\cdot Dv_{pn}$$

(2-17)
$$\frac{d}{dt}\left(v_{pn}\right)=\frac{1}{C_{DC}}\left[\mathbf{S}\right]^T\cdot\mathbf{i_{sn}}-\frac{2}{C_{DC}}\cdot i_{DC}$$

(2-18)
$$\frac{d}{dt}\left(Dv_{pn}\right)=\frac{1}{2\cdot C_{DC}}\cdot\left[\mathbf{S_{np}}\right]^T\cdot\mathbf{i_{sn}}$$

Different switching matrices **S** and $\mathbf{S_{np}}$ correspond to each position of the switches s_a, s_b and s_c. These allowable combinations of the switches are called voltage space vectors. The switching matrices are changed as the modulator selects new voltage space vectors. Averaging the switching matrices using the averaging operator (2-19), the small signal model is obtained.

(2-19)
$$\overline{z(t)}=\frac{1}{T_s}\cdot\int_{t-T_s}^{T_s}z(t)\cdot dt$$

Under the assumption that Δv_{pn} is small, Equation (2-18) can be neglected as, can the last term in the equation (2-16). What remains is the well-known, average state-space model of a two level inverter.

2.3.4 Control of the Inverter in Rotating Coordinates

In order to facilitate control design, three-phase variables can be transformed into a rotating d-q reference frame. By transforming Equations (2-10) and (2-11), a new model in rotating refernce frame is obtained, Figure 2.25. The control inputs into the system are d_d and d_q. They are computed by the d and q channel controller.

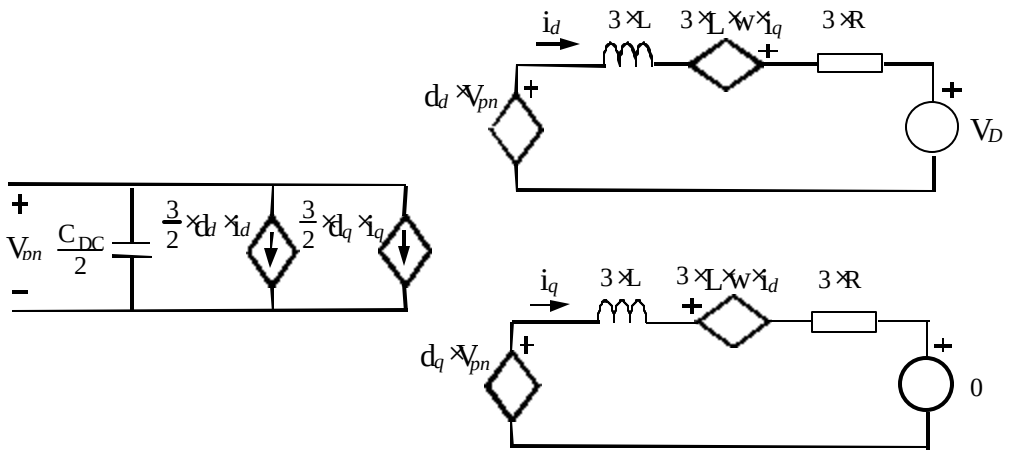

Figure 2.25. Inverter average model in rotating d-q coordinate frame.

The d-axis of the rotating reference frame is aligned with the utility line voltage space vector, $\mathbf{V_{ABC}}$, as shown in Figure 2.26. The control inputs are the line-to-line duty cycles, d_d and d_q, transformed into the synchronous frame. Their relationship to the voltage reference vector in Figure 2.28 is

$$d_d = \frac{|\mathbf{V_{REF}}|}{V_{pn}} \cdot \cos\theta \quad , \quad d_q = \frac{|\mathbf{V_{REF}}|}{V_{pn}} \cdot \sin\theta \quad . \tag{2-20}$$

The control inputs are obtained from a closed loop-controller, and the reference voltage vector is then calculated from (2-20). Finally, the modulator generates the corresponding duty cycles.

During the period of SC's discharging, the inverter operates in the utility inverter mode. The task of the inverter is to control the magnitude and phase angle of the three-phase output currents, thereby controlling the amount of active and reactive power supplied to the utility, as shown in Figure 2.26. The design of the current controllers can follow a standard procedure for VSIs; conventional PI regulators were used in the implementation described here.

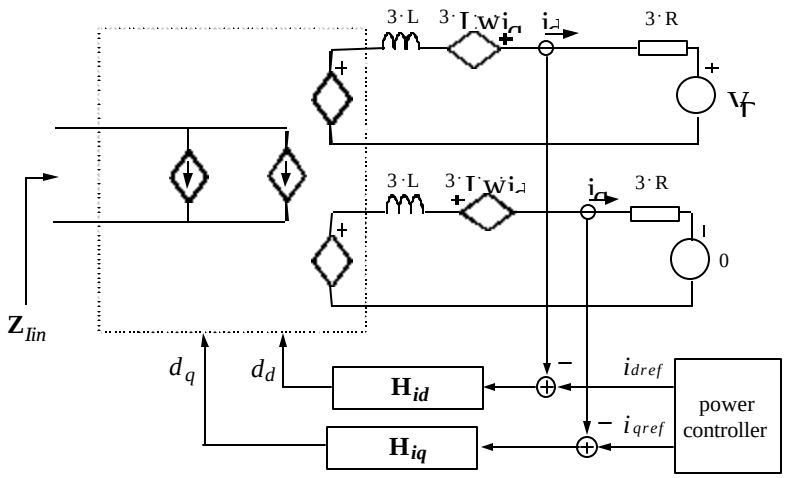

Figure 2.26. Inverter control in the utility mode (charging the SC).

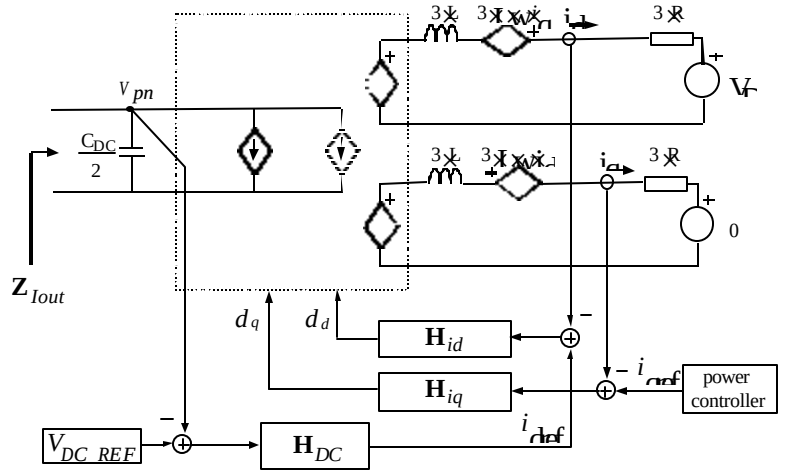

Figure 2.27. Inverter control in rectifier mode (discharging the SC).

In the SC charging mode, the inverter is operates as a three-phase boost rectifier with the objective of controlling the voltage on the dc-link, as shown in Figure 2.27. The active power flow is controlled by the chopper, while the inverter still independently controls the reactive ac power depending on the utility requirements.

The outputs of the controllers can not be implemented directly by the power stage. Instead, the voltage reference vector V_{REF} (as computed by the controller in the rotating reference frame) needs to be converted back to the stationary reference frame and implemented by the modulator.

The inverter output line-to-line voltages, V_{ab}, V_{bc} and V_{ca} (produced by available switching combinations) can be represented as space voltage vectors in one plane, as shown in Figure 2.26. The vector names represent the allowable states of the switches; e.g., **pon** represents the state in which switch S_a is connected to the positive dc rail, S_b to the NP, and S_c to the negative dc rail. . There are 27 switching-state vectors: six large vectors with the magnitudes equal to $2 \cdot V_{pn} / \sqrt{3}$; six medium vectors with magnitudes equal to V_{pn}; twelve small vectors with magnitudes equal to $V_{pn} / \sqrt{3}$, and three zero-voltage vectors.

The task of the VSI modulator is to synthesize the reference line voltage space vector, $\boldsymbol{V_{REF}}$, by PWM of the available voltage space vectors. The space vector modulation (SVM) implemented in this system switches the three vectors nearest to the voltage reference vector. The duty cycles of the vectors are found as a vector decomposition of the reference vector to the nearest three vectors. Details of the modulation process will be studied in Chapter 3.

Large vectors and zero vectors do not produce any NP current, i_{NP} and hence do not affect the NP voltage. Medium and small vectors affect the NP balance, but only the small vectors come in pairs. Both vectors in a pair produce the same line-to-line voltage, but produce the NP current in opposite directions. Consequently, the effect of the small vectors alone could be balanced in a way similar to that used in the chopper case, but the effect of the middle vectors cannot be directly controlled. This may produce a low-frequency voltage ripple of the NP, the extent of which depends on the magnitude of the voltage reference vector, the magnitude and phase angle of the output phase current, the NP control method, and the size of the dc-link capacitors. This

issue will be addressed in Chapter 4, where it will be shown that the worst case scenario is when the VSI supplies a purely reactive power at the full current capacity. In such a case, large a NP ripple can be expected and active compensation with the chopper may be essential.

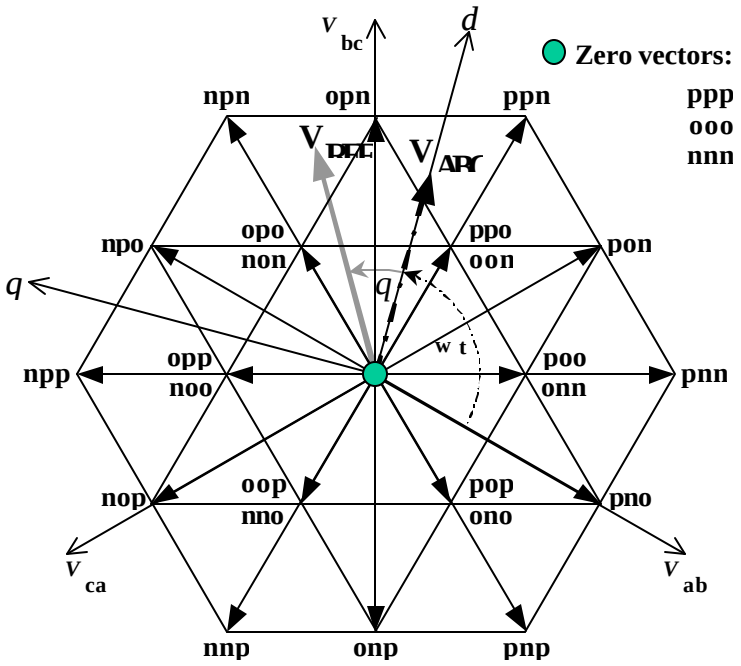

Figure 2.28. Voltage space vectors of a three-level inverter.

2.3.5 Simulation and Experimental Results

The average model simulation results were validated on the experimental setup shown in Figure 2.29. The system in the picture is rated at 250kW, with a dc-link voltage of 1800V, the dc-link current of 150A, and operates with 20kHz switching frequency. Simulations and the experiments were performed with the inverter operating alone in the rectifier mode at 28kW power level. The three-phase utility line voltage was 208V with the 77A phase rms current. This produced 600V on the dc link that was loaded with 13Ω resistive load.

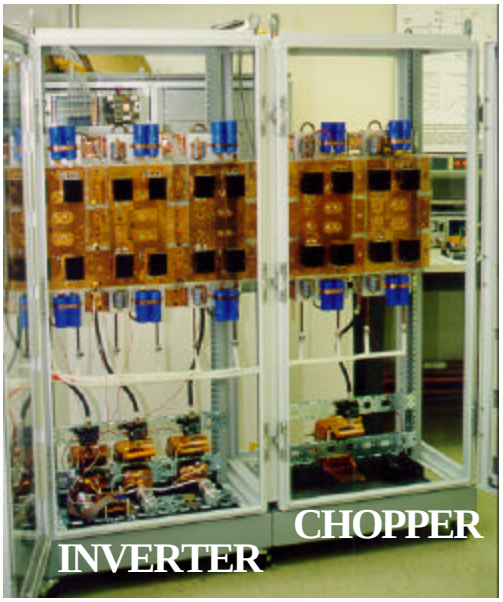

Figure 2.29. Experimental SMES PCS system.

The simulated and measured current loop gain in the d channel is given in Figure 2.30. The PI regulators $\boldsymbol{H_{id}}$ and $\boldsymbol{H_{aq}}$ were designed using the model in Figure 2.27 for the current loop-gain crossover frequency of 1kHz. The results in Figure 2.30 show good agreement between the design predictions, simulations and experiments. The achieved wide current-loop bandwidth confirms the feasibility of using the system for power quality applications, including the active filtering of loads with high harmonic contents.

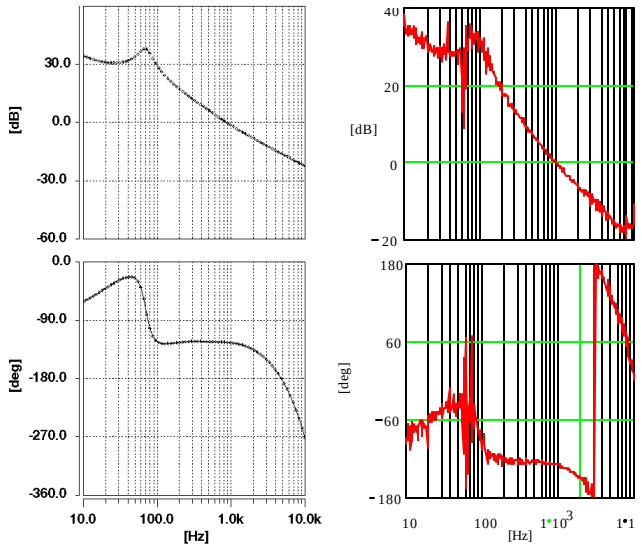

Figure 2.30. Simulated and measured rectifier current loop gain.

The voltage regulator, $\mathbf{H_{DC}}$, was designed for the loop gain crossover at 20Hz. The simulated and experimental measurements of the voltage loop-gain are shown in Figure 2.31. Again, the results demonstrate the good agreement between simulations and measurement.

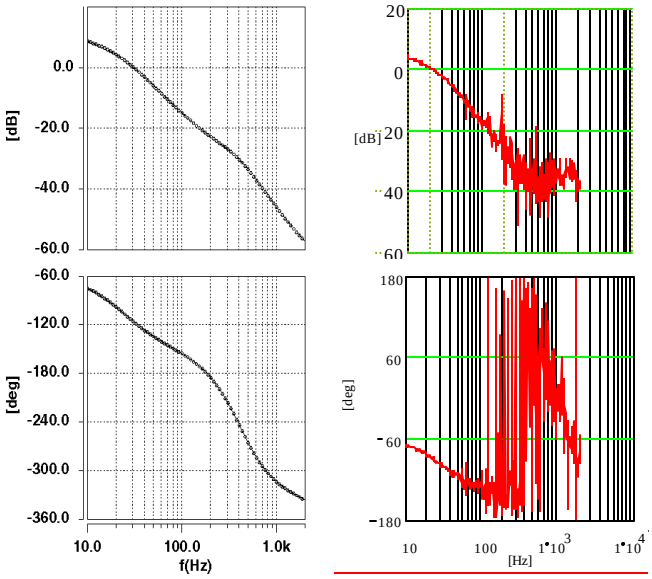

Figure 2.31. Simulated and measured rectifier voltage loopgain.

The response of the rectifier to the step change in current command with the voltage loop disabled is shown in Figure 2.32; this shows the performance of the rectifier inner current loop.

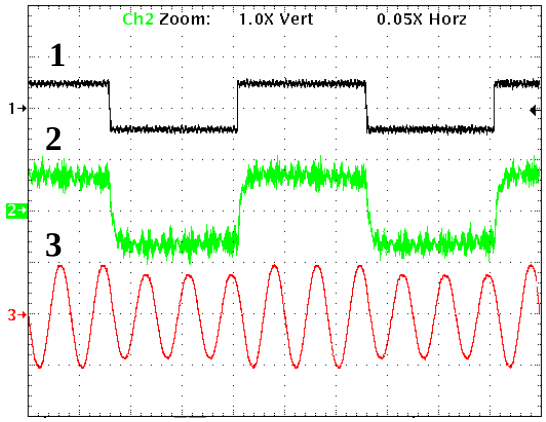

Figure 2.32. Rectifier response to change in current command: 1) current command (20ms/div); 2) d-channel current, i_d; and 3) rectifier phase current (100 A/div).

2.4 Modeling and Control Approach and Problem Formulation

The principle research and development effort in this dissertation was to better understand how to control and model three- and more level, three-phase converters for use in SMES power conditioning systems as well as in other applications. The approach was really bottom up. Important modeling and control concepts were first understood, then analyzed, and finally generalized when possible. Only than was the understanding of the fundamental concepts applied in the design of the system as a whole.

It was already mentioned that one of the important problems of multilevel converters is the modulator design (implementation). The SVM approach is perhaps the most powerful, because it allows more freedom to control and optimize the switching patterns than any other modulation approach; at the same time, for converters with higher number of levels it becomes too cumbersome for real-time implementation. Therefore, the first big task in this work was to simplify and generalize the implementation of a SVM for converters with any number of levels.

This goal was successfully achieved through the geometric analysis of the space vector diagrams, and through implementation of linear transformations that transform the switching vectors from a space where the algorithm is difficult to implement to a space where implementation of the algorithm becomes almost trivial.

The second problem that was analyzed is perhaps less general, in the sense that it directly applies to the problem of charge balancing in the dc-link capacitors of a three-level NPC converter. Still, it is currently one of the most popular topologies and was used for the prototype PCS. The idea behind the research was to try to find a mathematical model that could describe the effect of the load on the charge balance as well as to find guidelines for sizing the dc-link capacitors in order to achieve the optimal voltage ripple amplitude for any operating condition.

The modeling approach was geared towards the SVM and is general in the sense that it can model almost any type of SVM. In addition, it offers some intuitive insight into the operation

and the limitations of the charge-balancing algorithms. Finally the theoretical results were verified on the prototype PCS.

Further thinking along the lines of the charge ripple leads almost naturally to the following question: If there are certain operating conditions that cause a significant charge ripple in the dc-link capacitors, is there a way to implement a controller such that it can cancel the effect of that ripple in the output waveform, and therefore allow savings in the size of the dc-link capacitors?

The answer to the above question is positive. By applying a feed-forward controller (proposed in this work), it is possible to compensate for any size of the imbalance in the dc-link capacitors. The properties of the feed-forward algorithm were studied on two different time scales. The initial study included the development line cycle averaging model and its linearization for the purpose of feedback. Than a switching cycle average model was built and simulated in the computer in order to study the system behavior in more detail. Some of the results were verified through the experiment.

2.5 Conclusions

This is an overview chapter that covers a wide range of issues important in the design of a generic three-phase, multilevel power electronics system. The issues range from the selection of the topology and the requirements of the digital control hardware all the way to an overview of the PCS for the SMES application and the formulation of the research problems studied in this dissertation. At the same time, this chapter is an overview of the issues that had to be resolved during the course of the design and implementation of the prototype SMES PCS.

3 A FAST SPACE VECTOR MODULATION ALGORITHM FOR MULTILEVEL CONVERTERS

With the increase of the number of levels, the number of allowable switching states in the converters is also rapidly increasing. This situation places significant computational difficulties in front of the space vector PWM modulator, which is typically implemented in software and operating in real time and for high switching speeds. Figure 3.1 shows the structure of a generic three-phase converter digital control system.

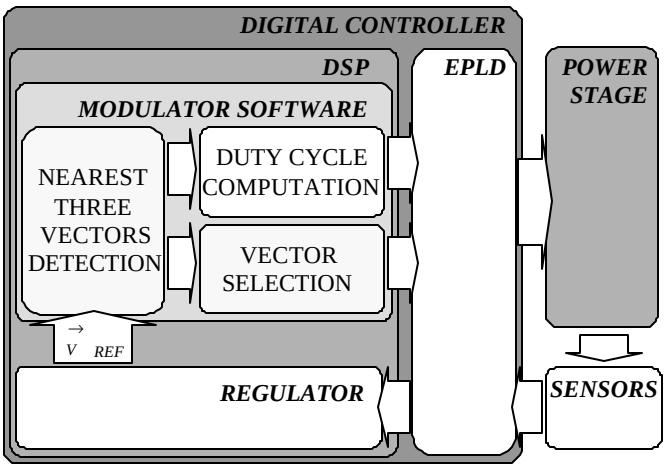

Figure 3.1. Architecture of digital controller for three-phase converters.

3.1 Switching Vectors, Switching States and Reference Vector

In essence, a multilevel converter is a voltage synthesizer that generates its output voltage from many discrete voltage levels. Therefore, without a loss of generality, most recently studied multilevel topologies can be well represented (for the purpose studying SVM), by the functional diagram in Figure 3.2.

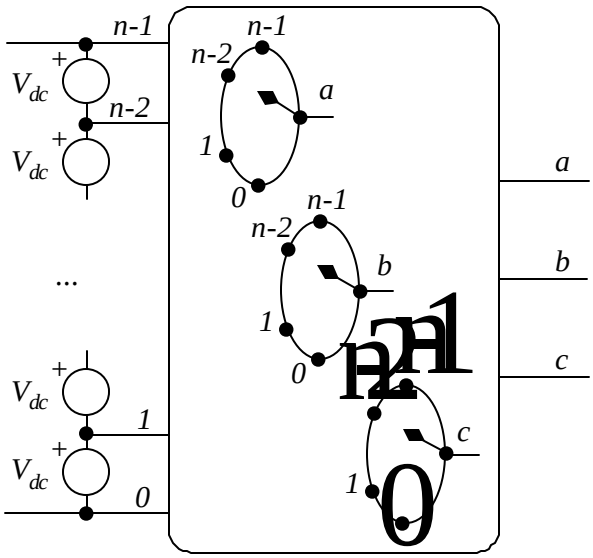

Figure 3.2. Functional diagram of a three-leg n-level converter.

Because the functionality of each phase leg can be represented by a single-pole n-throw switch, it becomes clear that each switching state (combination of phase-leg switches) produces uniquely defined three-phase line voltages (3-1), which can be represented as vectors in a three-dimensional Euclidean vector space[1]:

(3-1) $$\vec{V} = \begin{bmatrix} v_{ab} & v_{bc} & v_{ca} \end{bmatrix}^T .$$

[1] Three-dimensional, Euclidean coordinate space is chosen to present vectors, primarily for the elegance of mathematical description, even though it might not be the most widely accepted way of representing vectors in three-phase systems.

For example, if the location of the equivalent phase switches of the phases a, b and c were in the positions i, j and k, respectively, where $i, j, k \in [0, n-1]$, then that switching state could be represented by the switching vector

(3-2) $$\vec{V}_{(ijk)} = V_{dc} \cdot [i-j \quad j-k \quad k-i]^T .$$

It is somewhat important to make the distinction between switching states and switching vectors, in the sense that different switching vectors can be implemented with a various number of switching states. There are $N_{states} = n^3$ switching states, which make $N_{vectors} = 1 + 6\sum_{i=1}^{n-1} i$ switching vectors. Clearly the number of allowed combinations increases rapidly as the number of levels increases.

On the other hand, the existence of various switching states of some of the switching vectors has some merit. Having a variety of switching states from which to choose provides the important degree of freedom to balance the charge in the split dc-link capacitors and/or optimize the switching pattern. Shown in Figure 3.3 are all the switching vectors of a three-level converter, with their corresponding switching states. The reason to naming the vectors with their corresponding switching states is purely practical, because the converter switches are controlled on a per-phase basis, and a decision must be as to which vector to switch, as well as which switching state to select. On the other hand, representing vectors in the line voltage coordinate space is a nice mathematical abstraction to consistently explain the spatial relations between the switching vectors.

Finally, because of Kirchof's voltage law, the sum of the line-to-line voltages always adds up to zero, which is really an equation of the plane in the line-to-line coordinate system. This means that all the switching vectors of a three-level converter lie in the plane, and that is how they are usually represented.

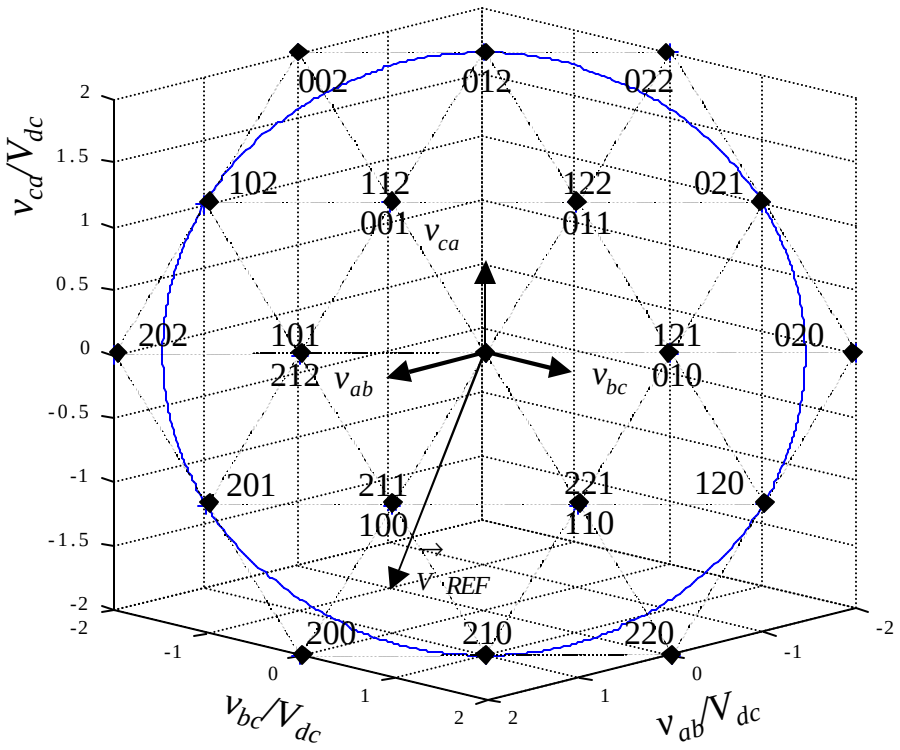

Figure 3.3. Switching states of a three-level converter.

Coming back to the same three-dimensional representation, a voltage reference vector that is to be synthesized with the help of switching vectors can also be represented in vector form, as follows:

(3-3) $$\vec{V}_{REF} = V_{l-l} \cdot \begin{bmatrix} \cos(w \cdot t + j) \\ \cos(w \cdot t - 2 \cdot p/3 + j) \\ \cos(w \cdot t - 4 \cdot p/3 + j) \end{bmatrix},$$

and also has only two degrees of freedom. Using the definition of vector norm, the length of the reference vector is

(3-4) $$\left| \vec{V}_{REF} \right| = \sqrt{\vec{V}_{REF} \cdot \vec{V}_{REF}} = V_{l-l} \cdot \sqrt{\frac{3}{2}},$$

while by the same definition, the length of the longest switching vector is

$$\left|\vec{V}_{\max}\right| = \sqrt{2}\cdot(n-1)\cdot V_{dc}. \tag{3-5}$$

Because the maximum length of the reference vector (3-3) that can be synthesized equals the radius of the largest circle that can be inscribed in the outermost hexagon, the maximum length of the reference vector for a general multilevel converter is

$$\left|\vec{V}_{REF_{\max}}\right| = \left|\vec{V}_{\max}\right|\cdot\cos(\pi/6). \tag{3-6}$$

By substituting (3-4) and (3-5) into (3-6), the maximum amplitude of the undistorted line-to-line voltage that a multilevel converter can synthesize is

$$V_{l-l\max} = (n-1)\cdot V_{dc}. \tag{3-7}$$

3.2 Space Vector Modulation of a Three-Level Converter

It is the task of the modulator to decide which position the switches should assume (switching state), and the duration needed (duty cycle) in order to synthesize the reference voltage vector. In other words, it is the task of the modulator to approximate the reference vector, computed by the controller, using the PWM of several switching vectors. Arguably, the best way to synthesize the voltage reference vector is by using the nearest three vectors

$$\vec{V}_{REF} = \left(d_1\cdot\vec{V}_1 + d_2\cdot\vec{V}_2 + d_3\cdot\vec{V}_3\right), \tag{3-8}$$

with the following additional constraint on the duty cycles:

(3-9) $$d_1 + d_2 + d_3 = 1.$$

It was shown in the previous paragraph that the voltage space vectors of a three-phase converter are always located in the plane, and that is how they are represented in Figure 3.4. In addition, although naming the switching states with the numbers is much more general (and applicable for any number of levels converter), for the three-level converter, equivalent nomenclature in which 2, 1, 0 are named p, o, n is perhaps a little more common; the two will be used interchangeably.

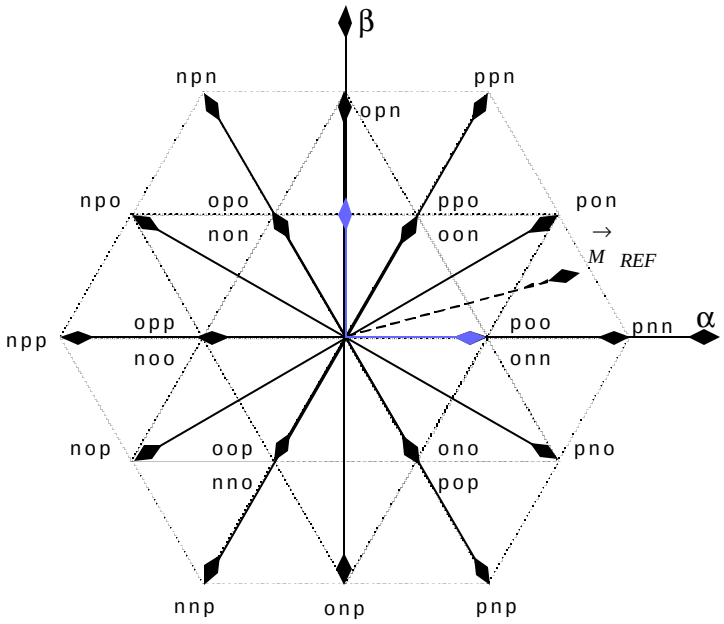

Figure 3.4. Voltage space vectors of a three-level converter.

So far, it has been shown that all the switching state vectors and the reference vector can be represented in a two-dimensional space, and that the goal is to approximate the reference vector using the nearest three vectors (NTVs) that satisfy (3-8) and (3-9). Clearly, there is a certain degree of freedom in choosing the coordinate system in which to represent those vectors. This decision will have important consequences for the rea-time implementation of the modulation algorithm. The two coordinate frames that first come to mind are the rectangular, often called (a, b) and the polar (r, q).

Because the control loops are implemented in the rotating reference frame, and because the conversion from rotating reference frame to the stationary polar reference frame requires computation of the arctangent function to determine the angle q of the reference vector, the a, b reference frame is perhaps a better choice for the real-time implementation[1], if the modulator will operate within the feedback system.

The first step the modulator needs to perform is to identify the NTVs, which is really to determine the small triangle in which the tip of the reference vector, $\vec{V}_{REF}$, is located. The inner triangle is always within a certain sixty-degree region. The small triangle sides are described with simple linear equations in the a, b coordinate system. The small triangle (NTVs) are than found by evaluating the sign of some linear expressions with reference vector coordinates substituted. Finally, when the NTVs are located, then solving the system of three linear equations with the three unknowns given in (3-8) and (3-9) results in the duty cycles.

However, because the derivation of the model describing the charge balance in the NP, (which will be developed in the next chapter) turns out to be easier to develop in polar coordinates, the SVM algorithm in polar coordinates will be presented in more detail. The implementation of the algorithm in polar coordinates follows the same steps already outlined in the previous paragraph.

The first step in detecting the NTVs is to find the sixty-degree region, which in polar coordinates comes naturally, because the angle of the reference vector is known. Then the small triangle has to be located, which requires evaluation of the sign of some non-linear expressions. For example, if the expression

(3-10) $$m - \frac{1}{\sqrt{3} \cdot \cos(q) - \sin(q)} > 0$$

is true (which is really the equation of the line in polar coordinates system that connects the small and the medium vector from Figure 3.5), then the NTVs are located in the outer triangle in Figure 3.5. The three duty cycles can be found by solving the system for one vector (3-11) and one scalar (3-12) equation:

(3-11) $\boldsymbol{V_{REF}}=d_{S0}\,\boldsymbol{V_{S0}} + d_M\,\boldsymbol{V_M} + d_L\,\boldsymbol{V_L}$ and

(3-12) $d_{S0}+d_M+d_L=1$.

The solution for duty cycles d_{S0}, d_M and d_L can be shown to be

(3-13) $$d_{S0} = 2 - m \cdot \left(\sqrt{3} \cdot \cos(q) + \sin(q)\right),$$

(3-14) $$d_M = 2 \cdot m \cdot \sin(q) \text{ and}$$

(3-15) $$d_L = -1 + m \cdot (\sqrt{3}\cos(q) + \sin(q)).$$

[1] In case of the modulator is running open loop there is no need to implement arctangent function to compute the q coordinate since it can be freely incremented depending on the desired line frequency.

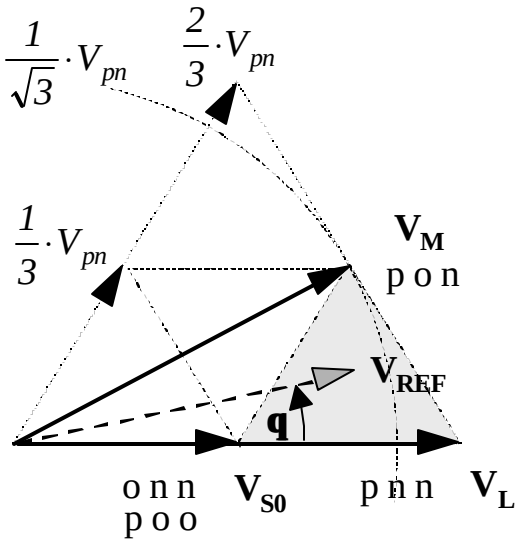

Figure 3.5. Synthesis of $\mathbf{V_{REF}}$ in outer small triangle.

It was already mentioned that the equations for every triangular region are somewhat different; Equations (3-16)-(3-20) give the duty cycles for the middle triangular region from Figure 3.6:

(3-16) $\boldsymbol{V_{REF}} = d_{S0}\,\boldsymbol{V_{S0}} + d_M\,\boldsymbol{V_M} + d_L\,\boldsymbol{V_L}$,

(3-17) $d_{S0} + d_{S1} + d_M = 1$,

(3-18) $d_{S0} = 1 - m \cdot 2 \cdot \sin(\theta)$,

(3-19) $d_{S1} = 1 + m \cdot (\sin(\theta) - \sqrt{3} \cdot \cos(\theta))$ and

(3-20) $d_M = -1 + m \cdot (\sin(\theta) + \sqrt{3} \cdot \cos(\theta))$.

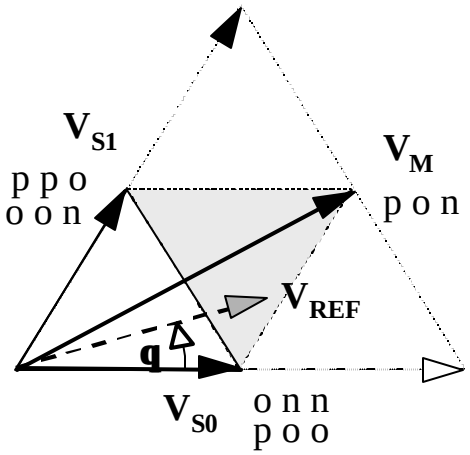

Figure 3.6. Synthesis of $\mathbf{V_{REF}}$ in middle small triangle

Finally, the sign of the left hand side of the Equation (3-21) determines whether the reference vector is located in the inner smaller triangle.

(3-21) $$m - \frac{1}{\sqrt{3} \cdot \cos(q) + \sin(q)} < 0.$$

If the Equation (3-21) is true the vector is in the inner small triangle. Then the duty cycles are found as follows:

(3-22) $$\boldsymbol{V_{REF}} = d_{S0}\,\boldsymbol{V_{S0}} + d_{S1}\,\boldsymbol{V_{S1}},$$

(3-23) $$d_{S0} + d_{S1} + d_Z = 1,$$

(3-24) $$d_{s0} = m \cdot (\sqrt{3}\cos(q) - \sin(q)) \text{ and}$$

(3-25) $$d_{s1} = 2 \cdot m \cdot \sin(q).$$

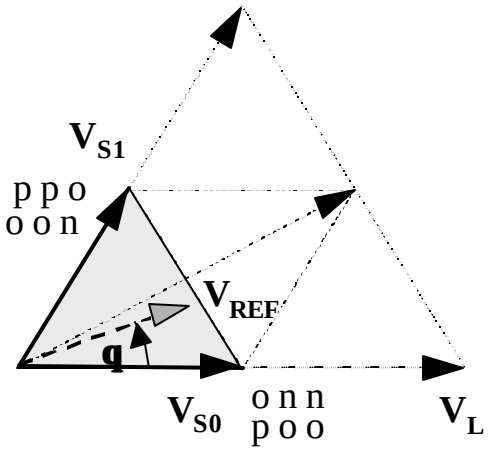

Fig. 3.7. Synthesis of $\mathbf{V_{REF}}$ in inner small triangle.

Finally, it is clear that whether implementing the SVM in the rectangular or the polar coordinate system, the implementation becomes increasingly more complex as the number of levels increases. This is especially true for the implementation of the algorithm in polar coordinates, which requires the division, sine and cosine functions (or corresponding look-up tables), and even the arctangent function for the implementation of the closed-loop system. Fortunately, most of these implementation problems (and more) can be avoided with the new SVM algorithm described next.

3.3 The New Space Vector Modulation Algorithm

Comparing the arrangement of voltage space vectors of a four-level converter (from Figure 3.8) to that of the voltage space vectors from Figure 3.4, a visible pattern can be noticed in their hexagonal structures. In fact, starting with the innermost hexagon that corresponds to the two-level converter, each new level adds one more ring of equilateral triangles to form a new hexagon of voltage space vectors.

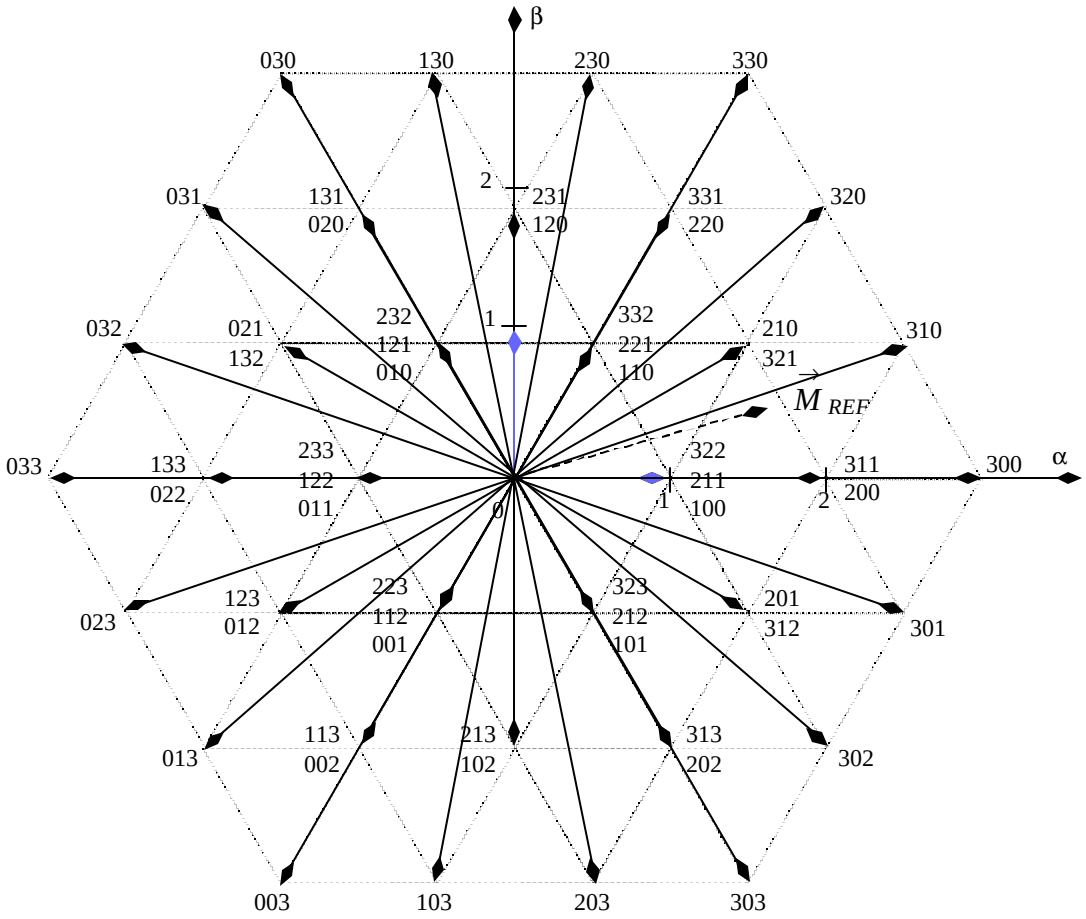

Figure 3.8. The voltage space vectors of a four-level converter.

Fortunately, it turns out that this regularity in the structure of the hexagons can be used to more efficiently represent the vectors in the plane, and can be used to generalize the SVM algorithm. The trick is to use a set of non-orthogonal vectors as a new basis in which to represent the switching vectors and the reference vector. One such basis set is

(3-26)
$$\left\{ \vec{g}_{(v_{ab},v_{bc},v_{ca})}, \vec{h}_{(v_{ab},v_{bc},v_{ca})} \right\} = \left\{ \begin{bmatrix} V_{dc} \\ 0 \\ -V_{dc} \end{bmatrix}, \begin{bmatrix} 0 \\ V_{dc} \\ -V_{dc} \end{bmatrix} \right\}.$$

.

3.3.1 Coordinate Transformation

The first step in the algorithm is to transform the reference vector $\vec{V}_{REF}$ into a two-dimensional coordinate system. This can be achieved using a change-of-basis linear transformation. Naturally the transformation matrix differs depending on the source coordinate system. For example, Matrix (3-28) transforms the reference vector given in the line-to-line coordinate system (3-3) into the *(g,h)* coordinate system, and at the same time normalizes the reference vector with the length of the basis vector.

(3-27) $$\vec{V}_{REF(g,h)} = T \cdot \vec{V}_{REF(v_{ab},v_{bc},v_{ca})}$$

(3-28) $$T = \frac{1}{3 \cdot V_{dc}} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}$$

Because of the normalization, all the switching-state vectors in the $\{\vec{g}, \vec{h}\}$ coordinate system have only integer coordinates.

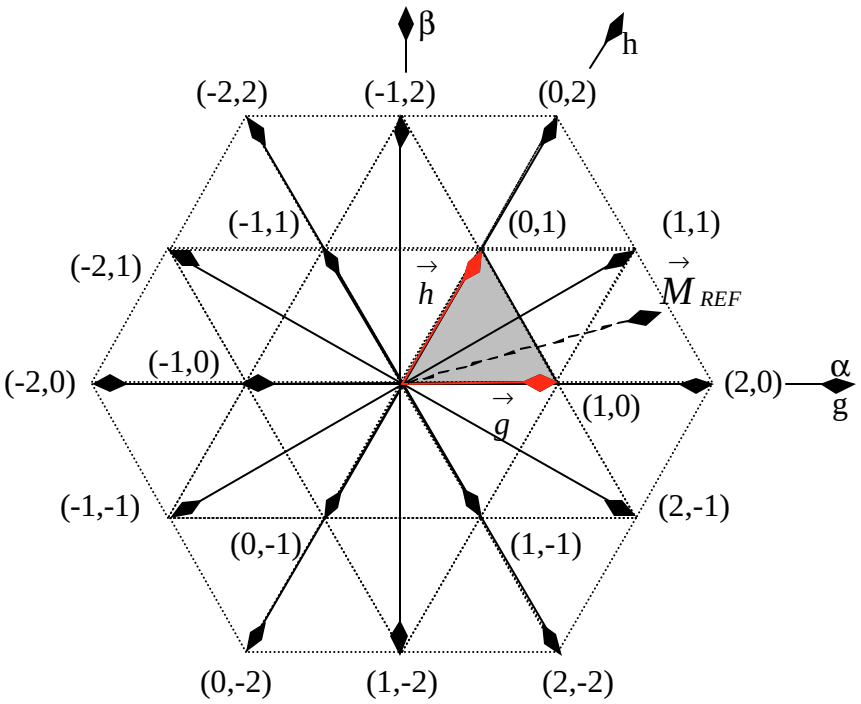

Figure 3.9. Switching-state vectors of a three-level converter in a hexagonal coordinate system.

3.3.2 Detection of Nearest Three Vectors

The fact that all the switching vectors have integer coordinates is advantageous because the four vectors nearest to the reference vector can be identified simply as vectors the coordinates of which are combinations of upper and lower rounded integer values of the reference vector coordinates, as follows:

(3-29)
$$\vec{V}_{u1} = \begin{bmatrix} \lceil V_{REFg} \rceil \\ \lceil V_{REFh} \rceil \end{bmatrix}, \vec{V}_{lu} = \begin{bmatrix} \lfloor V_{REFg} \rfloor \\ \lceil V_{REFh} \rceil \end{bmatrix}$$
$$\vec{V}_{uu} = \begin{bmatrix} \lceil V_{REFg} \rceil \\ \lceil V_{REFh} \rceil \end{bmatrix}, \vec{V}_{ll} = \begin{bmatrix} \lfloor V_{REFg} \rfloor \\ \lfloor V_{REFh} \rfloor \end{bmatrix} .$$

The endpoints of the nearest four vectors form the equal-sided parallelogram that is divided into two equilateral triangles by the diagonal connecting vectors $\vec{V}_{u1}$ and $\vec{V}_{lu}$. The vectors $\vec{V}_{u1}$ and $\vec{V}_{lu}$ are always two of the NTVs. The third nearest vector is one of the remaining two vectors located on the same side of the diagonal,

(3-30) $$g + h = V_{u\,lg} + V_{ulh},$$

as the reference vector. Therefore, the third nearest vector can be found by evaluating the sign of the expression

(3-31) $$V_{REFg} + V_{REFh} - (V_{u\,1g} + V_{ulh}).$$

If the sign is positive, then the vector $\vec{V}_{uu}$ is the third nearest vector; otherwise, vector $\vec{V}_{ll}$ is the third nearest vector. This completes the identification of the NTVs for the n-level converter.

3.3.3 Duty Cycles Computation

Once the NTVs are identified, their corresponding duty cycles can be found by solving (3-8) and (3-9), where $\vec{V}_1 = \vec{V}_{ul}$, $\vec{V}_2 = \vec{V}_{lu}$, and $\vec{V}_3 = \vec{V}_{ll}$ or $\vec{V}_3 = \vec{V}_{uu}$. Fortunately, however, because all switching-state vectors always have integer coordinates, the solutions are essentially the fractional parts of the $\vec{V}_{REF}$ coordinates, or more precisely

(3-32)
$$\begin{aligned} d_{ul} &= V_{REFg} - V_{llg}, \\ d_{lu} &= V_{REFh} - V_{llh} \quad \text{and} \\ d_{ll} &= 1 - d_{ul} - d_{lu}. \end{aligned}$$

if $\vec{V}_3 = \vec{V}_{ll}$, or

(3-33)
$$d_{ul} = -(V_{REFh} - V_{uuh}),$$
$$d_{lu} = -(V_{REFg} - V_{uug}) \text{ and}$$
$$d_{uu} = 1 - d_{ul} - d_{lu}.$$

if $\vec{V}_3 = \vec{V}_{uu}$.

Consider, for example, a three-level converter and reference vector with amplitude $V_{l-l} = 1.8 \cdot V_{dc}$ at the instant $w \cdot t = 50 \cdot \frac{p}{180}$, which can be represented as

(3-34)
$$\vec{V}_{REF} = 1.8 \cdot V_{dc} \cdot \begin{bmatrix} 0.643 \\ 0.342 \\ -0.985 \end{bmatrix}.$$

Using the change-of-basis transformation (3-28), the reference vector in the proposed two-dimensional coordinate system is

(3-35)
$$\begin{bmatrix} V_{REFg} \\ V_{REFh} \end{bmatrix} = T \cdot \begin{bmatrix} V_{REFab} \\ V_{REFbc} \\ V_{REFca} \end{bmatrix} = \begin{bmatrix} 1.157 \\ 0.616 \end{bmatrix}_{g,h}.$$

From there, the nearest four vectors can be found simply as vectors the coordinates of which are the combinations of upper and lower rounded values of the voltage reference vector:

(3-36)
$$\vec{V}_{ul} = \begin{bmatrix} 2 \\ 0 \end{bmatrix}, \vec{V}_{lu} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}, \vec{V}_{uu} = \begin{bmatrix} 2 \\ 1 \end{bmatrix}, \vec{V}_{ll} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}.$$

In order to find the third nearest vector, all that needs to be done is to evaluate the sign of the expression:

(3-37)
$$1.157 + 0.616 - (2 + 0) = -0.16 < 0.$$

Because it is negative, in this example, vector $\vec{V}_{ll}$ is the third nearest vector. Finally, computing the expressions in (16) gives the solution for the duty cycles

$$\begin{aligned} & d_{ul} = 0.157, \\ & d_{lu} = 0.616 \text{ and} \\ & d_{ll} = 0.227. \end{aligned} \tag{3-38}$$

This completes the selection of the vectors and the computation of their corresponding duty cycles. Nevertheless, one more step remains if the modulator is to generate the commands for the equivalent switches from Figure 3.2.

3.3.4 Switching-State Selection

This last step requires a transformation from a two-dimensional coordinate space back to the three-dimensional space of switching combinations. In general, there is no unique solution for this problem, which allows some freedom in optimizing the switching strategy. The first step in choosing the best switching state or states at any given moment is to find all the switching states that make a switching vector in question $\vec{V} = [g,h]^T$. Mathematically, all the switching states of a switching vector satisfy a relationship

$$\begin{bmatrix} k \\ k-g \\ k-g-h \end{bmatrix}, \text{ where } k, k-g, k-g-h \in [0, n-1]. \tag{3-39}$$

For example, in the case of a three-level converter, a vector $[1,0]^T$ transforms into two switching combinations: $[1,0,0]^T$ and $[2,1,1]^T$. Which of the valid switching states to switch, and for what part of their corresponding switching vector duty cycle (in case the balancing algorithm requires use of several small vectors during one switching cycle), usually requires some

additional information. In fact, it depends on the strategy for balancing the dc sources, which usually requires some knowledge of the phase currents and/or dc-link voltages.

Finally, simulated switching waveforms for three-, four- and five-level converters are shown in Figure 3.10.

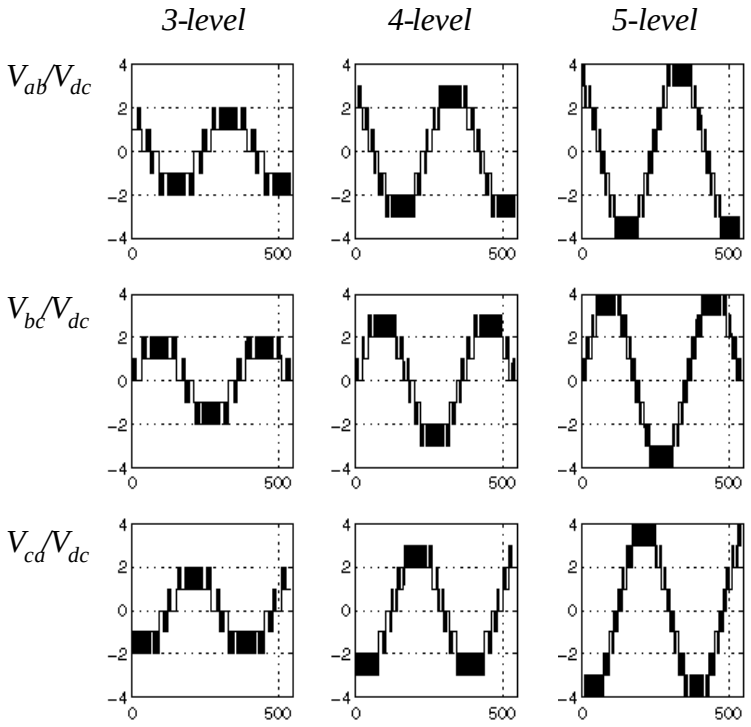

Figure 3.10. Normalized line-to-line PWM voltage waveforms for three-, four- and five-level converters.

3.4 Practical Implementation of The New SVM Algorithm

It was already mentioned that the principal strength of the proposed algorithm is in its ease of implementation. The ease of implementation in this case is augmented by the very small number of instructions and with the suitability for implementation that can run in real time, for high switching frequency, and for converters with any number of levels. The properties of the algorithm can best be explained by presenting the flow chart of the algorithm implemented on

the DSP that controls the prototype SMES PCS. The algorithm can be divided in three steps as shown in Figure 3.11.

The first step in the algorithm is to change into the *(g,h)* coordinate system which is in fact the linear transformation as in (3-28). Other change-of-basis transformations can be constructed to transform the reference vector from the *(d,q)*, the *(a,b)* or any other basis into the *(g,h)* basis.

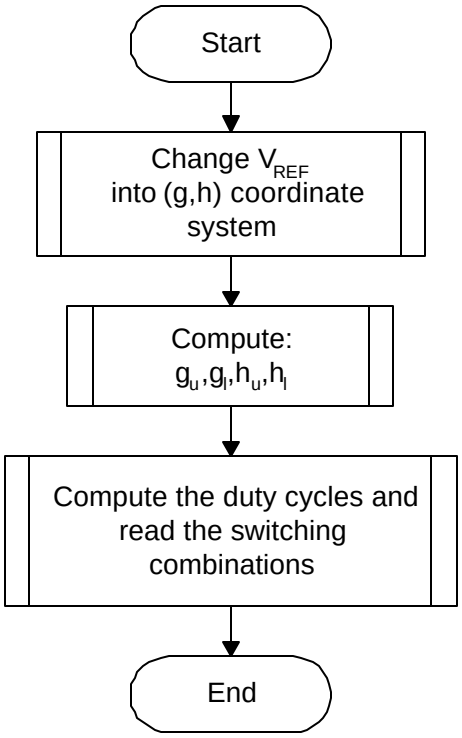

Figure 3.11. Overview of the new SVM algorithm.

The next step in the algorithm is to find the nearest four vectors by computing the upper and lower rounded values of the reference vector's coordinates in the *(g,h)* coordinate system. Figure 3.12 shows how this operation can be conveniently implemented using a truncation function, usually available in most floating-point DSPs.

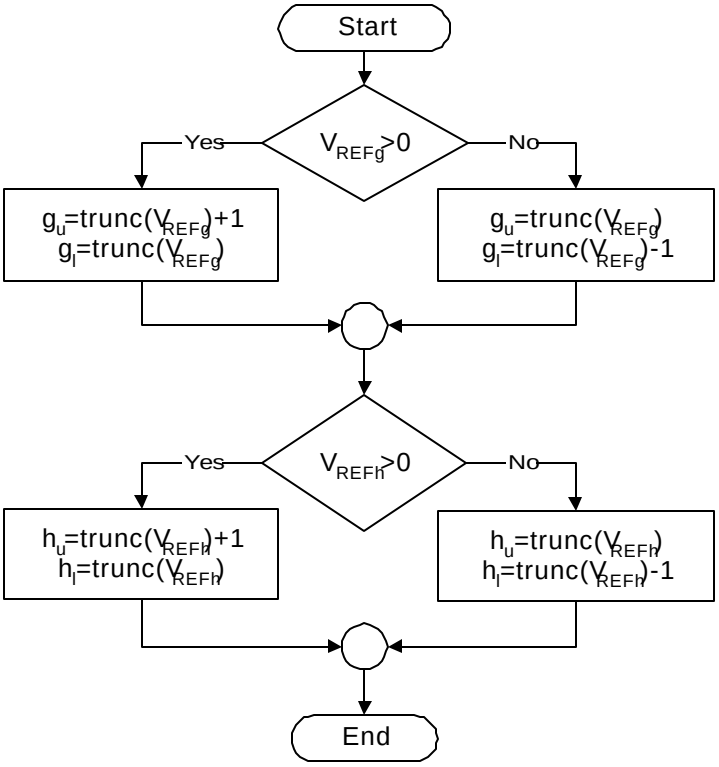

Figure 3.12. Computing the nearest four vectors.

The set of nearest four vectors needs to be reduced to the nearest three vectors, the duty cycles need to be computed and the switching states selected. Figure 3.13 shows one possible implementation approach in which, based on the sign of the expression (3-31), the algorithm branches into two branches. One branch treats the case in which the third nearest vector is $\boldsymbol{V_{ll}}$; the other branch treats the case in which the $\boldsymbol{V_{uu}}$ is the third nearest vector. In both cases, the duty cycles for all three vectors are computed based on the simple linear expressions from (3-32) and (3-33). So far, the algorithm is unique and works for any number of levels converter.

In real implementation, however, one last coordinate transformation still remains. The remaining transformation converts the vectors in the *(g,h)* coordinate system into the switching functions. This transformation is not unique, because it essentially transforms a vector existing

in a two-dimensional space into a switching combination that exists in three-dimensional space (all three single-pole triple-throw switches from Figure 3.2 can be chosen independently).

At the same time, selection of switching combinations affects the charge balance of the dc-link capacitors. A consistent choice of "wrong" switching states leads inevitably to the charge imbalance, loss of converter levels and the over-voltage condition in the devices. In fact, very often, control of the charge balance is performed in this part of the modulator algorithm by selecting the switching states based on the current direction information and based on the error in the dc-link capacitors' charge (voltage) imbalance.

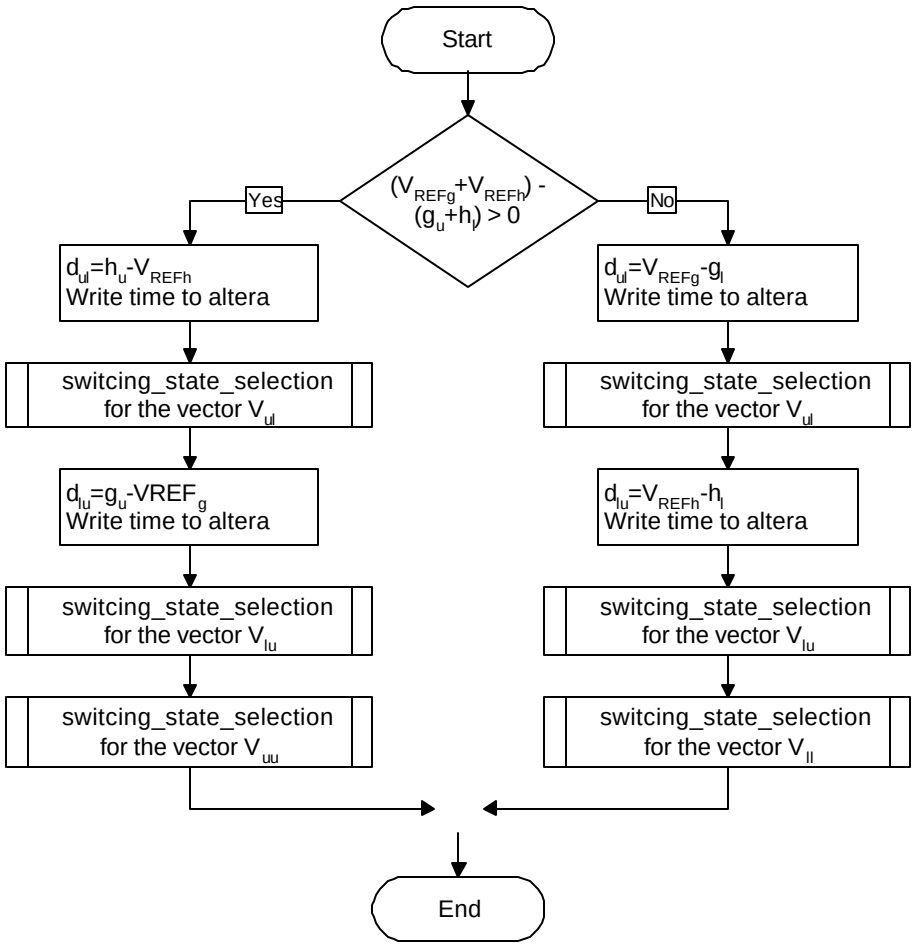

Figure 3.13. Computation of duty cycles and selection of switching states.

Figure 3.14 shows one implementation of the subroutine that selects the switching states based on the *(g,h)* coordinates of the three-level converter. Unfortunately, at this point there does not seem to be a universal algorithm available that can select the appropriate switching states for converters with any number of levels. That is the reason that the three-level modulator for the SMES system was implemented based on the look-up table (

Table 3-I). The switching states are stored as hexadecimal numbers, in which the right-most hexadecimal number is reserved for the location of the right-most phase, or according to representation from Figure 3.2, phase c. The 0 equivalent switch location is coded with *#3*, the 1 location with #6, and finally the 2 switch location is coded with *#C*. The fourth hexadecimal number from right to left is used only for the switching state of the small vectors. That number tells the NP balancing algorithm which phase leg current is connected to the NP. The switching states and how they affect the dc-link capacitors' charge balance in case of three-level converters is studied in detail in Chapter 4.

The core of the algorithm is a simple formula that computes the address of the switching state in

Table 3-I, based on the *(g,h)* coordinate of the switching vector

(3-40) $M8=7*(g+h+2)+(h+2)$.

In case of small vectors that can be implemented with two switching combinations, the other switching combination is located at the address *M8+4*.

After the address is found, based on the measurement of the voltage imbalance and the direction of the phase currents, the charge-balancing algorithm selects the switching state of the small vector that will minimize the charge imbalance. If the variable NP from the algorithm is 0, there is only one choice of the switching state for the given switching vector and that is the switching state from the switching vector selection subroutine. If the NP is not equal to 0, one of the two switching combinations is selected to minimize the charge imbalance.

Finally, a much more in-depth treatment of the NP balancing problem is located in the next three chapters. The main purpose of presenting the new SVM algorithm in this section was to illustrate the simplicity of its implementation in a real-life example

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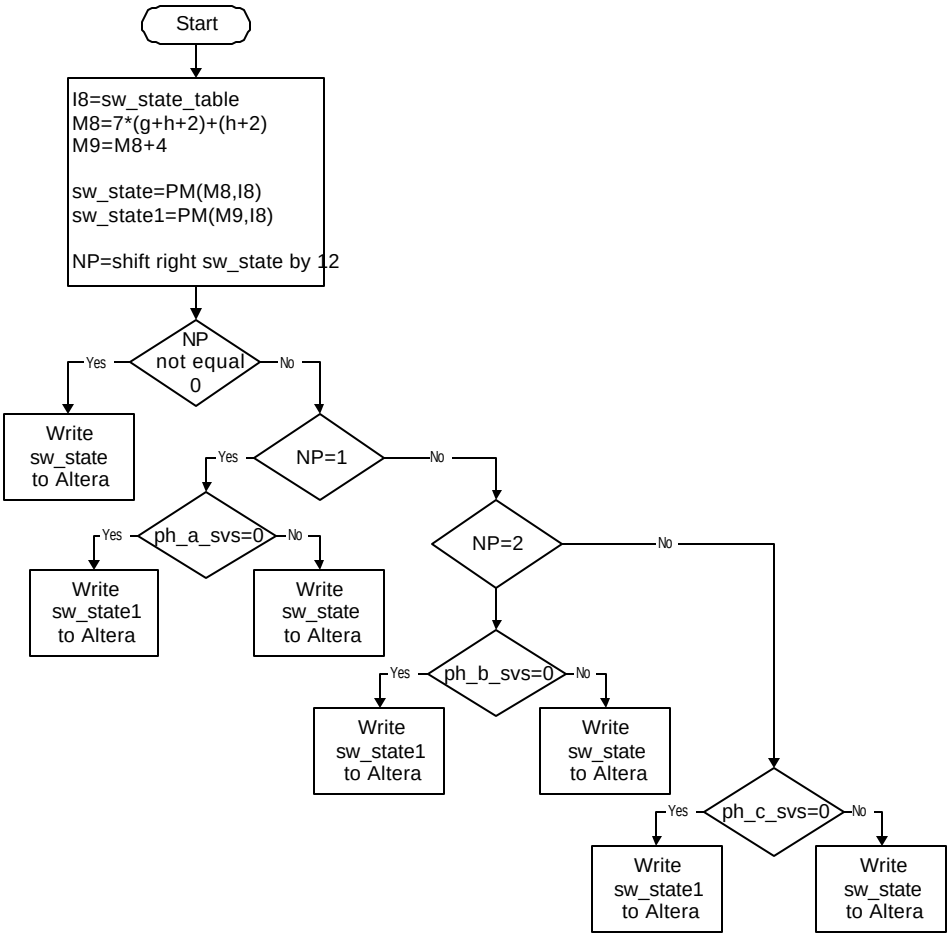

Figure 3.14. Switching-state selection with dc-link capacitor charge control.

Table 3-I The switching-state look-up table.

Switching State Table Location	Switching Vectors, Large & Medium $V_{g,h}$	Small Switching Vectors, $V_{g,h}$	Switching States (per Phase)	Hexadecimal Switching Number	Small Vectors NP Currents
0.	(0,-2)		002	#33C	
1.	(-1,-1)		012	#36C	
2.	(-2,0)		022	#3CC	
3.					
4.					
5.					
6.					
7.	(1,-2)		102	#63C	
8.		(0,-1)	001	#3336	ic
9.		(-1,0)	122	#16CC	ia
10.	(-2,1)		021	#3C6	
11.					
12.		(0,-1)	112	#66C	-ic
13.		(-1,0)	011	#366	-ia
14.	(2,-2)		202	#C3C	
15.		(1,-1)	212	#2C6C	ib
16.					
17.		(-1,1)	010	#2363	ib
18.	(-2,2)		020	#3C3	
19.		(1,-1)	101	#636	-ib
20.					
21.		(-1,1)	121	#6C6	-ib
22.	(2,-1)		201	#C36	
23.		(1,0)	100	#1633	ia
24.		(0,1)	221	#3CC6	ic
25.	(-1,2)		120	#6C3	
26.					
27.		(1,0)	211	#C66	-ia
28.		(0,1)	110	#663	-ic
29.					
30.	(2,0)		200	#C33	
31.	(1,1)		210	#C63	
32.	(0,2)		220	#CC3	

It is difficult to come up with one number that will demonstrate the superiority of this approach, in part because due to its complexity SVM is generally not used for the converters with more than three levels. The other difficulty is the fact that implementation of the algorithm depends heavily on the platform. Thus, it is very hard to compare algorithms implemented on different platforms.

Nevertheless, as an illustration of algorithm's performance, its, real-life implementation on the Analog Devices Shark floating point processor will be discussed next. Table 3-III shows the rough number of instructions for each step of the algorithm. It is a rough number because the implementation does not make use of all the processor resources that can speed up the algorithm execution, while it does include the "house keeping" instructions that communicate with PWM generators. Therefore, substantial savings in the number of instructions can be made with an implementation that makes use of all the available processor resources, such as the use of two instructions per switching cycle and the use of shadow registers to pass the variables. Perhaps as much as two-thirds of the execution time can be saved in an optimized implementation, compared to the execution time in this implementation.

Table 3-III The performance of the algorithm implementation for a three-level converter.

	Number of Instructions
Change of Basis	9
Finding Nearest Four Vectors	25
Duty Cycle Computation	29
Switching State Selection (Worst Case)	3*28
TOTAL NUMBER OF INSTRUCTIONS	147

Even this sub-optimal implementation (listed in the Apendix) executes on the Shark DSP operating at 33 MHz clock speed, in less than 5μs. Therefore, the application of this algorithm we can think of multilevel converters operating at the switching frequencies in excess of 100 kHz, where by increasing the number of levels the algorithm essentially does not change. The switching state table becomes larger, but the speed of execution remains essentially unaffected.

3.5 Conclusions

This chapter introduced the fast new space vector algorithm for multilevel three-phase converters. The algorithm is general and applicable to converters with any number of levels, since the number of steps involved in computation is always the same regardless of the location of the reference voltage vector. In addition, the efficiency and the ease of implementation of this algorithm makes it well suited for simulation on digital computers; it can become a very useful tool in further exploration of the properties of multilevel power converters. The algorithmic description of the real-life implementation shows its simplicity.

4 NP BALANCING PROBLEM IN THREE-LEVEL DIODE-CLAMPED CONVERTERS

Figure 4.1 shows one of the most widespread realizations of a three-level converter, a diode-clamped converter. At this point, it is probably clear that regardless of the implementation, the benefits of using the multilevel topology come with a price. The price, almost as a rule, must be paid in the form of the more complicated, more difficult to make reliable, hardware and software realizations, and in a struggle with multiple dc sources. Three-level diode clamped topology is no exception to this rule.

Since one of the main advantages of this technology is its ability to utilize the switching devices rated for one-half of the dc-link voltage, the NP must be maintained at (or very close to) half of the dc-link voltage. This is one of the critical requirements of the control system. In addition, any disturbance in the dc link will propagate into the output of the converter, and although the disturbance in the dc-link voltage can be compensated for by the control system, a disturbance in the charge balance (NP voltage) can not. At least not without introducing some of the techniques that will be, perhaps for the first time, introduced in the next chapter.

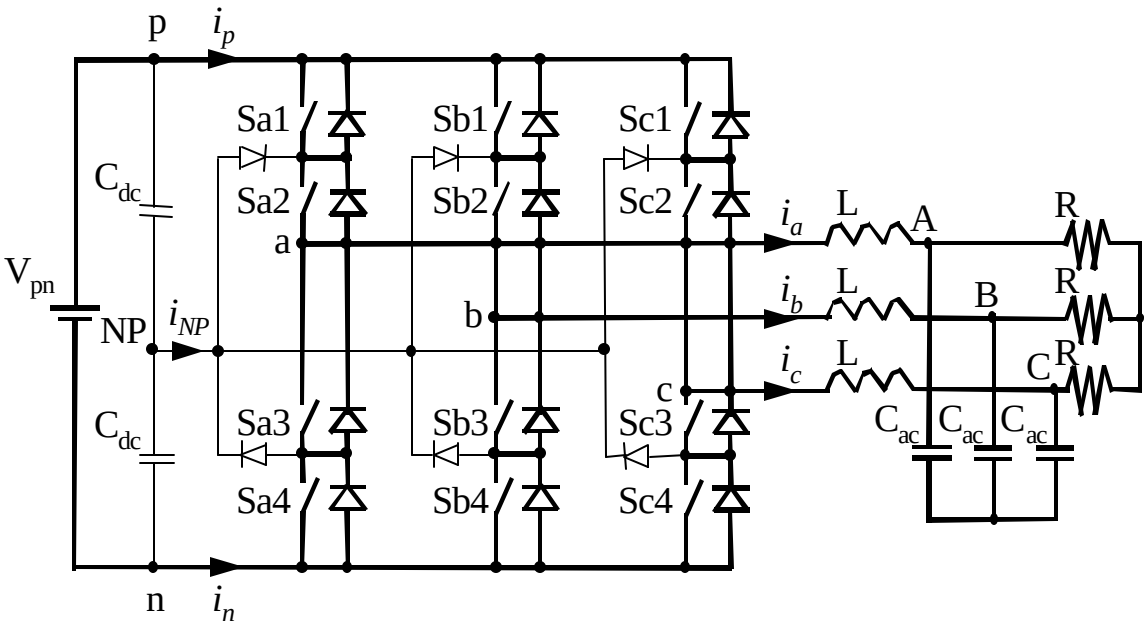

Figure 4.1. Circuit schematic of a three-level VSI.

In this chapter, certain assumptions, are made (that will be relaxed later), in order to help study the properties of NP balancing. Perhaps the most important assumption is the infinite size of the dc-link capacitors. Under this assumption the voltage in the NP will not change from its initial condition, set at one-half the dc-link voltage. In addition, because of this assumption, the output voltage can be assumed ideal in the average sense, which allows the use of ideal current in place of the load.

With all these assumptions in place, this study can concentrate on modeling the properties of SVMs with respect to the current in the NP, which will result in a more intuitive understanding of the NP balancing problem in three-level diode-clamped converters.

4.1 The Effect of Different Switching States on the Current in the NP

Figure 4.2 shows all the available voltage space vectors, and their corresponding switching combinations. As the reference vector rotates 360 degrees, it is continuously being synthesized by applying different switching vectors for the various length of time (duty cycles), as explained in Chapter 3. However, this chapter develops a mathematical apparatus that is general enough to describe the average current in the NP, and to study the contributions of different vectors to the NP current. In addition, the model will try to explain the theoretical limitations of the control authority over the dc-link capacitors charge balance, and include guidelines for sizing the dc-link capacitors.

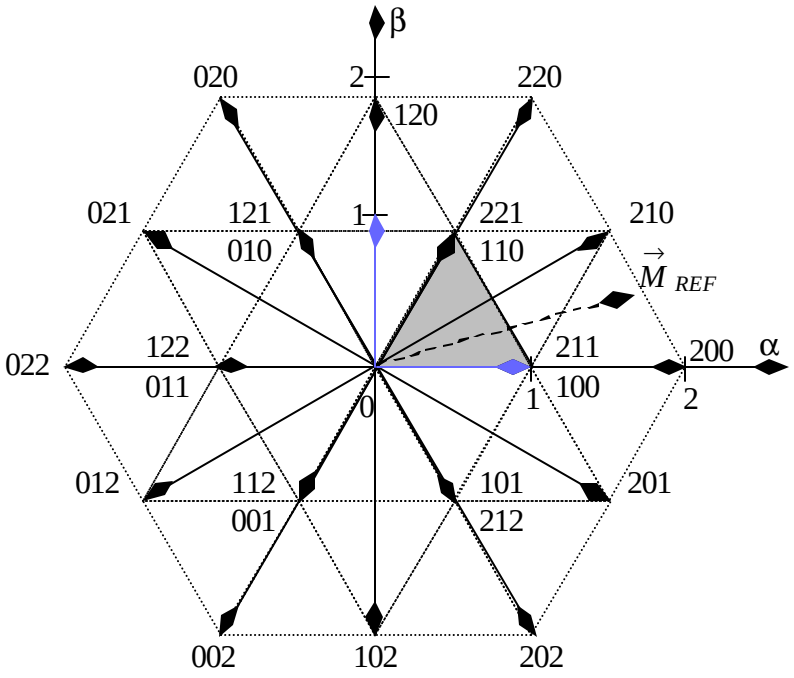

Figure 4.2. Switching-state vectors of the three-level VSI.

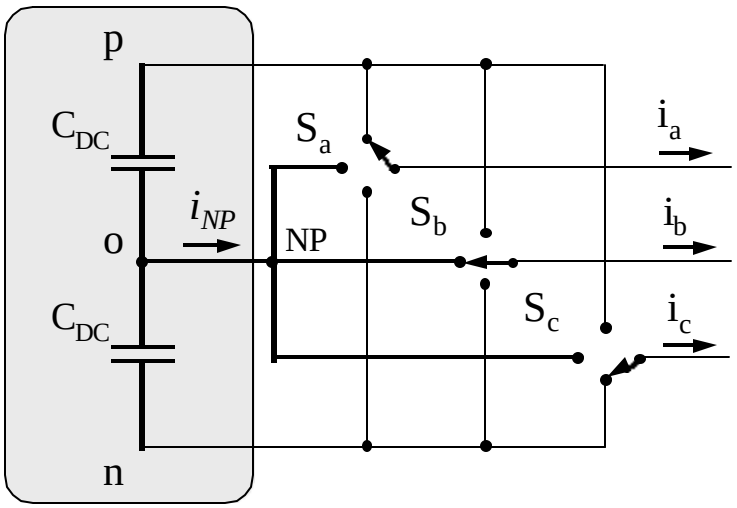

Figure 4.3. The position of equivalent switches for the switching state **pon**.

Table 4-I NP current i_{NP} for different space vectors.

Small Vectors (positive switching state)	i_{NP}	Small Vectors (negative switching state)	i_{NP}	Medium Vectors	i_{NP}
onn	i_a	poo	$-i_a$	pon	i_b
ppo	i_c	oon	$-i_c$	opn	i_a
non	i_b	opo	$-i_b$	npo	i_c
opp	i_a	noo	$-i_a$	nop	i_b
nno	i_c	oop	$-i_c$	onp	i_a
pop	i_b	ono	$-i_b$	pno	i_c

For the purpose of model development, it is convenient to divide the switching vectors into three categories according to their lengths: large, medium and small. This categorization can also be used to explain the effects of these vectors on the charge balance, because vectors from each of the three categories affect the charge balance in a similar way. For example, the large vectors do not affect the NP at all. The medium vectors connect one of the phase currents for the duration of their duty cycles thus causing a charge imbalance. The effect of the medium vectors is not controllable because it depends only on the duty cycle and the load power factor. Figure 4.3 shows how one of the medium vectors, vector **pon** directly connects the phase b to the NP, and as a result, a full-phase current flows into the NP for the duration of its duty cycle.

Finally, every small vector has two realizations: one positive and one negative switching function. Choosing one of the two switching combinations in a pair changes the sign of the phase current that vector connects to the NP. That is the source of the positive and negative atributes. Figure 4.3 shows the NP current for switching combinations of different small and medium vectors.

4.2 Neutral Point Current Modulation

The previous chapter discussed the methods of synthesizing the reference vector. The discussion will now turn to the attempt model the NP current and show its dependence on the load current. The modeling approach to be presented uses the switching functions to model the effect of different small and medium vectors connecting different phase currents to the NP. In order to effectively use the switching functions, it is beneficial to have the reference vector represented in polar coordinates.

In this case, the division into sixty-degree segments with inner, middle and outer small triangles still holds. Accordingly, as explained in

Table 4-I, different NP current flows for different switching combinations. For example, the outer small triangle in Figure 4.4 consists of two components: the non-controllable component from the medium vector and the controllable component from the small vectors.

A controlling effect of the small vectors can be described through the introduction of the new variable called the NP current-modulation index. This index, $m_{S0} \in [-1,1]$, in the case of this particular small triangle, represents the relative duration of the positive (onn) and negative (poo) small vectors within $\boldsymbol{V_{S0}}$.

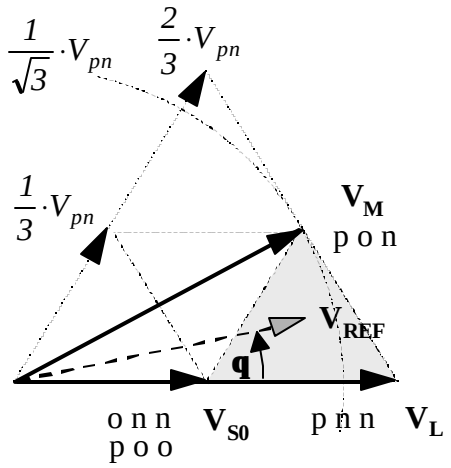

Figure 4.4. Outer small triangle.

In other words, the effective duty cycle of the vector $\boldsymbol{V_{S0}}$ can be expressed, using the current modulation index, with two duty cycles. For example in the outer small triangle of the Figure 4.4, the duty cycle of the positive switching combination (onn) is

(4-1) $$d_{S0\_pos} = (1 + m_{S0}) \cdot d_{S0} / 2,$$

while the duty cycle of the negative switching combination (poo) of the same vector is

(4-2) $$d_{S0\_neg} = (1 - m_{S0}) \cdot d_{S0} / 2.$$

Then in the case of this particular outer triangle the current flowing into the NP is

(4-3) $$i_{NP} = d_M \cdot i_b + m_{S0} \cdot d_{S0} \cdot i_a .$$

Using the same approach, the NP current can be expressed in the other small triangles as well. If the reference vector is within the middle small triangle, there are two small vectors available to aid in the NP balancing, and accordingly, two small vector-modulation indices. The NP current is, in this case:

(4-4) $$i_{NP} = d_M \cdot i_b + \left(m_{S0} \cdot d_{S0} \cdot i_a + m_{S1} \cdot d_{S1} \cdot i_c\right),$$

Finally, as far as maintaining charge in the NP, the most beneficial is the inner triangle region because in the inner triangle region, the reference vector is synthesized from the small vectors only, and is therefore completely controllable:

(4-5) $$i_{NP} = m_{S0} \cdot d_{S0} \cdot i_a + m_{S1} \cdot d_{S1} \cdot i_c .$$

4.3 Analysis and Control of the Neutral Point Voltage Error

A steady state low-frequency ripple in the NP current is caused by a periodic variation of the components in (4-3), (4-4) and (4-5) over the output voltage line cycle. In the steady state, the voltage reference vector has a constant amplitude and rotates with constant angular speed, $w = dq / dt$. As the reference vector sweeps through successive 60-degree sectors, the duty cycles d_{S0}, d_{S1}, d_M, and d_L become periodic functions of time. Due to the selected SVM strategy, these functions have discontinuous first derivatives at the boundaries of the small triangles and their wave shape dependent on the modulation index, m, as shown in Figure 4.5.

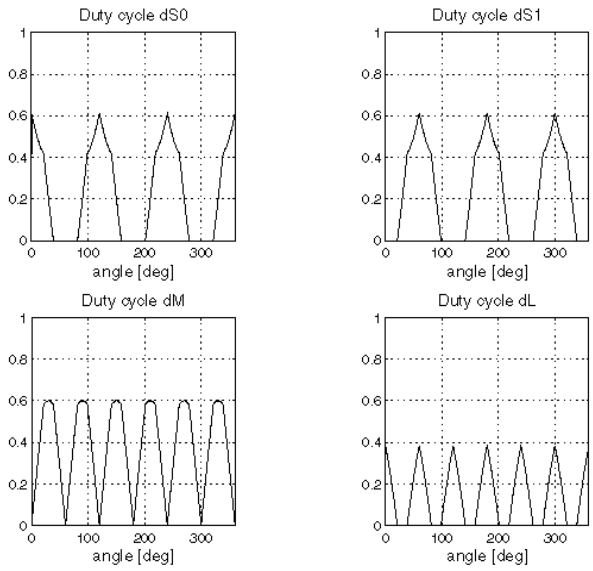

Figure 4.5. Duty cycles of SVM for modulation index m=0.8.

Although the duty cycle functions in Figure 4.5 are continuous functions, they map to different switching-state vectors in different 60-degree sectors. For example, it can be seen from Figure 4.2 that for $0^\circ \le q < 60^\circ$, d_M is the duty cycle of the medium vector **pon,** and for $60^\circ \le q < 120^\circ$, d_M is the duty cycle of the medium vector **opn**. Hence, the contribution of the medium vector to the NP current is $d_M \cdot i_b$ for $0^\circ \le q < 60^\circ$, and $d_M \cdot i_a$ for $60^\circ \le q < 120^\circ$.

Using the switching functions (such as those in Figure 4.6), it is possible to generalize the contribution of the medium vectors to the current in the NP for the full line cycle. In this case, the NP current can be written in the matrix form, as in (4-6). It is important to notice that the SVM algorithm completely determines the switching functions. In other words the switching functions depend solely on the choice of modulation algorithm.

On the contrary, the duty cycle of the medium vector (also shown in Figure 4.5, for one specific modulation index), is determined by the SVM algorithm as well as by the voltage reference vector's angle and magnitude. And finally, there are time-varying load currents (with their phase angle with respect to the voltage reference vector) that also affect the current flowing into the NP as a consequence of switching the medium vector switching states.

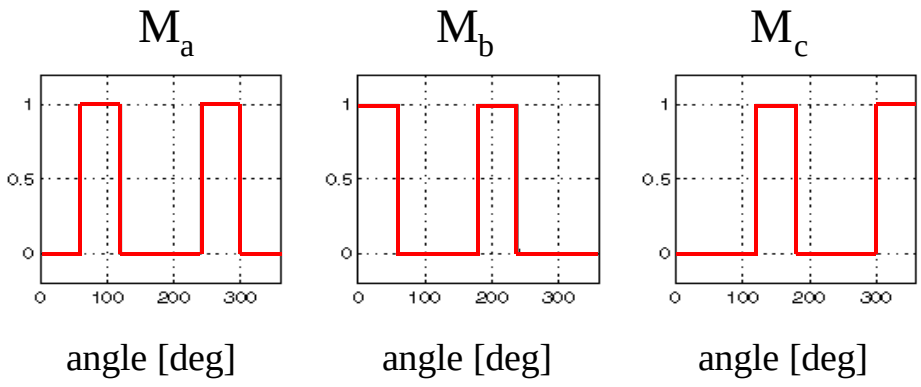

Figure 4.6. Switching functions of the medium vectors.

(4-6)
$$i_{NP\_mediu\_vector} = d_M \cdot \begin{bmatrix} M_a & M_b & M_c \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}.$$

Similar to the method used to select the switching functions of medium vectors (drawn in Figure 4.6 and represented in tabular form in

Table 4-II, mapping functions can also be derived for the small vectors. Using the small vector switching functions in

Table 4-III and

Table 4-IV, a NP current from the small vectors is expressed as

$$i_{NP\_small\_vector} = \begin{bmatrix} m_{S0} & m_{S1} \end{bmatrix} \cdot \begin{bmatrix} d_{S0} & 0 \\ 0 & d_{S1} \end{bmatrix} \cdot \begin{bmatrix} S0_a & S0_b & S0_c \\ S1_a & S1_b & S1_c \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \tag{4-7}$$

Finally, combining Equations (4-6) and (4-7) results in a single expression for the NP current over the full line cycle:

$$i_{NP} = d_M \cdot \begin{bmatrix} M_a & M_b & M_c \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} m_{S0} & m_{S1} \end{bmatrix} \cdot \begin{bmatrix} d_{S0} & 0 \\ 0 & d_{S1} \end{bmatrix} \cdot \begin{bmatrix} S0_a & S0_b & S0_c \\ S1_a & S1_b & S1_c \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \tag{4-8}$$

Expression (4-8), although valid over the full line cycle, does not offer significant insight into the properties of the modulator with respect to the current flowing into the NP. Therefore, in order to facilitate the analysis and control of the NP current for different loading conditions, it is perhaps a good idea to transform Equation (4-8) into the rotating d-q reference frame. Substituting the phase currents with the right hand side of the expression makes the transformation:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ \cos(\theta - 2 \cdot \pi / 3) & \sin(\theta - 2 \cdot \pi / 3) \\ \cos(\theta + 2 \cdot \pi / 3) & \sin(\theta + 2 \cdot \pi / 3) \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix}, \tag{4-9}$$

After multiplying the current-modulation indexes, the matrices of switching functions and the transformation matrix results in a compact expression, as follows:

(4-10)
$$i_{NP} = \begin{bmatrix} d_M \cdot M_d & d_M \cdot M_q \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} m_{S0} \cdot d_{S0} \cdot S0_d & m_{S0} \cdot d_{S0} \cdot S0_q \\ m_{S1} \cdot d_{S1} \cdot S1_d & m_{S1} \cdot d_{S1} \cdot S1_q \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix}.$$

Table 4-II Current-switching function for medium vectors.

Angle θ [deg]	Medium Vector	Switching Function			i_{NP}
		M_a	M_b	M_c	
0-60	pon	0	1	0	i_b
60-120	opn	1	0	0	i_a
120-180	npo	0	0	1	i_c
180-240	noip	0	1	0	i_b
240-300	onp	1	0	0	i_a
300-360	Pno	0	0	1	i_c

Table 4-III Current-switching function for S0 small vectors.

Angle θ [deg]	S0 Small Vector	Current Switching			i_{NP}
		$S0_a$	$S0_b$	$S0_c$	
300-60	onn/poo	1	0	0	ia
60-180	non/opo	0	1	0	i_b
180-300	oop/nno	0	0	1	i_c

Table 4-IV Current-switching function for S1 small vectors.

Angle θ [deg]	S1 Small Vector	Current Switching			i_{NP}
		$S1_a$	$S1_b$	$S1_c$	
0-120	ppo/oon	0	0	1	i_c
120-240	opp/noo	1	0	0	i_a
240-360	pop/ono	0	1	0	i_b

This expression is a little more readable because in steady state, i_d and i_q are constants and represent active and reactive components of the load current, respectively. Note that (4-10) is essentially a composite expression that combines (4-3), (4-4) and (4-5) into one matrix equation that is valid over the full line cycle of the output voltage. The NP current in this formulation still contains non-controllable current produced by the application of the medium vector and the controllable current produced by the small vectors.

NP current resulting from the application of medium vectors can be found by multiplying the direct i_d and quadrature i_q current by the direct, $d_M \cdot M_d$, and quadrature, $d_M \cdot M_q$, weighing factors, respectively. The wave shape of factors is given in Figure 4.7 for the case in which the modulation index $m=0.8$. It is apparent that the quadrature component of the current will be weighed much more heavily, and will produce much larger low-frequency (LF) ripple than does the direct component of current.

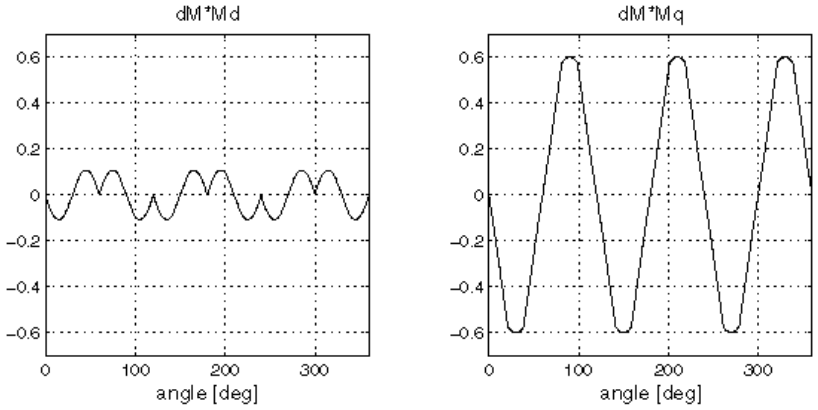

Figure 4.7. Weighing factors for medium vectors with m=0.8.

Similarly, NP current resulting from application of small vectors, depends on direct, and quadrature weighing factors multiplying the direct, i_d, and quadrature, i_q, load currents. Figure 4.8 shows the wave shape of the small vectors weighing factors for modulation index $m=0.8$. These four weighing factors depend not only on the small vectors' duty cycles and the current switching functions that are determined by the type of SVM used, but also on the control inputs m_{S0} and m_{S1}, as defined earlier. Two distinct sets of weighing factors are given in Figure 4.8.

One set of weighing factors used when only positive small vectors are involved (i.e., $m_{S0}=m_{S1}=1$), is given by the solid line; the other set when only negative small vectors are used (i.e. $m_{S0}=m_{S1}=-1$), is given by the dashed line. Between these two extreme cases, the weighing factors can be controlled by adjusting current-modulation indices.

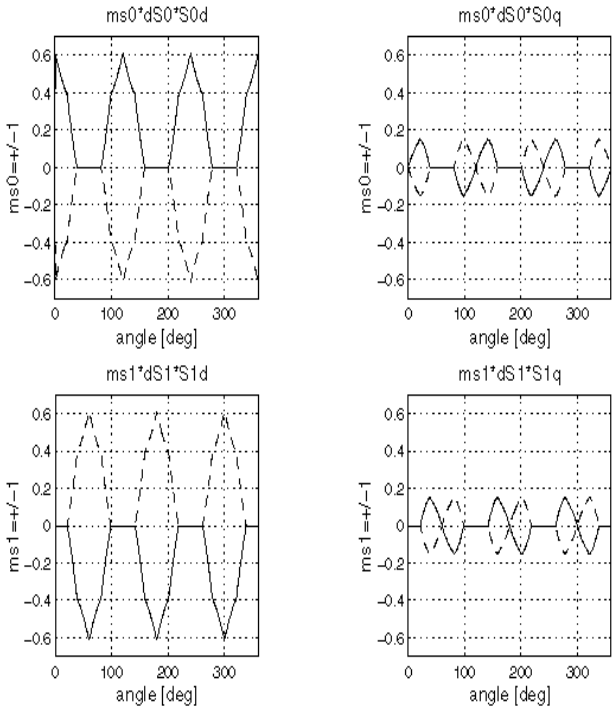

Figure 4.8. Weighing factors for small vectors with m=0.8.

The weighing factors for medium vectors are periodic functions with zero average value over a line cycle. This means that in steady state, at which i_d and i_q currents are constant, the NP current from medium vectors will naturally balance over a line cycle, and the only concern is the size of the LF ripple.

Note that the ratio of active and reactive weighing factor is opposite for medium and small vectors. Large i_d and small i_q means large control authority on the NP current through the manipulation of current-modulation indices of small vectors, and small disturbance from middle vectors. On the other hand, large i_q and small i_d means large disturbance from middle vectors,

with small control authority from small vectors. This means that it will be much easier to suppress the LF ripple from direct current, than it is to suppress them from quadrature current.

These results confirm the fact already proven in practice that accomplishing the NP balance is not very difficult for loads with high power factor. This requirement is usually met for ac-drive applications (except at no-load conditions, when the currents are generally small anyway). It is also true for three-level rectifiers operating at or close to unity power factor. However, for static VAR compensation, this requirement will not be met, meaning that this application will require different design tradeoffs.

Regarding NP balancing control for SVM, with the restriction to use of the NTV method, three distinctive approaches to the control of NP might be:

- Passive control, in which the positive and negative small vectors are selected alternately in each new switching cycle. This method can work only in the case of a perfectly balanced load and a perfectly balanced PWM scheme, which is unlikely to happen in practice. In addition, this method would have difficulties to recovering from line or load transients. Still, this control method can be used to establish a benchmark for NP controller performance. This benchmark can then be used to evaluate the performance of other NP control methods.

- Hysteresis-type control is perhaps the simplest and most popular closed-loop NP control scheme. This method requires knowledge of the current direction in each phase. Based on that information, the small vectors' switching combination that will move the NP voltage in the direction opposite from the direction of imbalance can be selected. The downside of this method is that the current ripple has a strong harmonic component at one half of the switching frequency. One implementation of this method is described in Figure 3.14.

- Active control schemes control the current modulation indices m_{S0} and m_{S1}. In general, these schemes require measurement of the voltage imbalance in the NP, and often require measurement of the amplitudes of the phase currents as well. The benefits of these schemes are that they do not have the ripple at half the switching frequency, and some variations of

these control schemes can balance the NP exactly. Unfortunately, they all increase the switching losses (due to the introduction of additional switching states), and may be less robust than the hysteresis-type control schemes.

Because the resulting NP ripple is low-frequency, the selection of the balancing algorithm (which affects the high-frequency content of the NP current) is not important in determining the size of the dc-link capacitors, and will not be investigated further.

4.4 Limitations of the Neutral-Point Control and Some Design Recommendations

From the analysis in previous sections, it is clear that regardless of control scheme the control authority over the NP current is limited, but that the region in which exact balancing can be achieved in each switching cycle must exist. This region is given as a shaded area in Figure 2.9. Note that the graph is symmetrical, and that the unity power factor load represents the most favorable case, in which the NP voltage can be balanced in every switching cycle for a modulation index as high as m=0.96.

If the operating point exits the shaded region, low-frequency, mainly third-harmonic ripple current flows into the NP. This is a highly undesirable effect because for some converter designs it significantly increases the size of the dc-link capacitors.

Figure 4.10 shows the peak-to-peak value of the low-frequency charge ripple in the NP divided by the amplitude of output phase current. The first graph shows the normalized NP charge ripple for the passive control of NP voltage balance. The second graph shows the best that can be done using feedback control of NP voltage balance. The shaded region represents the same ripple free area as the one in Figure 4.9.

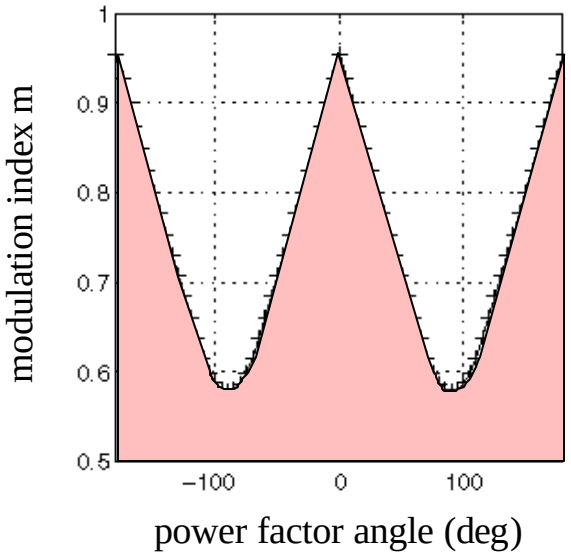

Figure 4.9. Region where LF ripple can be suppressed.

The actual dc-link capacitor size for the specified NP voltage ripple and for any power factor angle and voltage modulation index m, can be computed by multiplying the normalized charge ripple, $Q_{NORM} = Q_{NORM}(m, \phi_{LOAD})$, from Figure 4.10, by the current amplitude, then dividing that by two times the desired size of the NP voltage ripple:

$$c_i = \frac{Q_{NORM} \cdot I_{max}}{2 \cdot DU_{DC\_max}}. \tag{4-11}$$

This should provide sufficient guidelines to size the dc-link capacitors for any expected operation mode and desired NP voltage ripple.

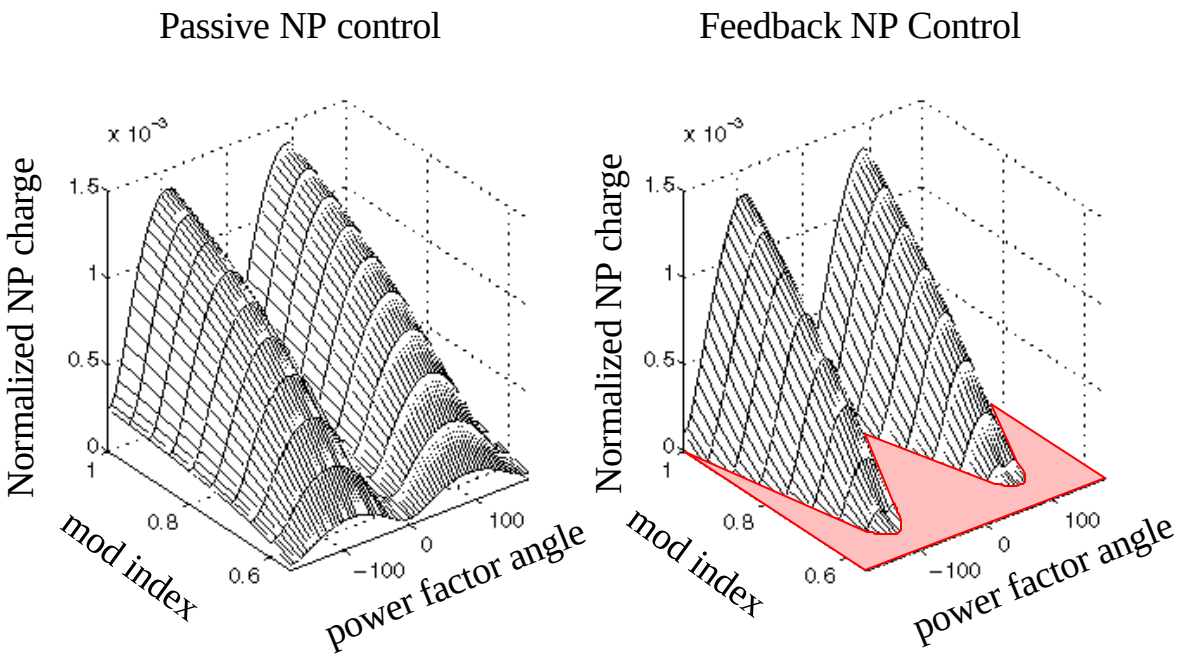

Figure 4.10. Normalized amplitude of the LF charge ripple.

For example, consider the prototype SMES PCS with 1800V dc-link voltage and Imax=200A phase current amplitude, and allow 1% voltage ripple (ΔUdc_max=18 V) in the NP. For modulation index m=0.9, the comparison of capacitor sizes for the feedback NP control and passive NP control is summarized in Figure 4.11. It is clear that the greatest savings in the size of capacitor can be achieved when the inverter is predominantly supplying active power; while for the operation with purely reactive power, the benefits of feedback NP control diminish.

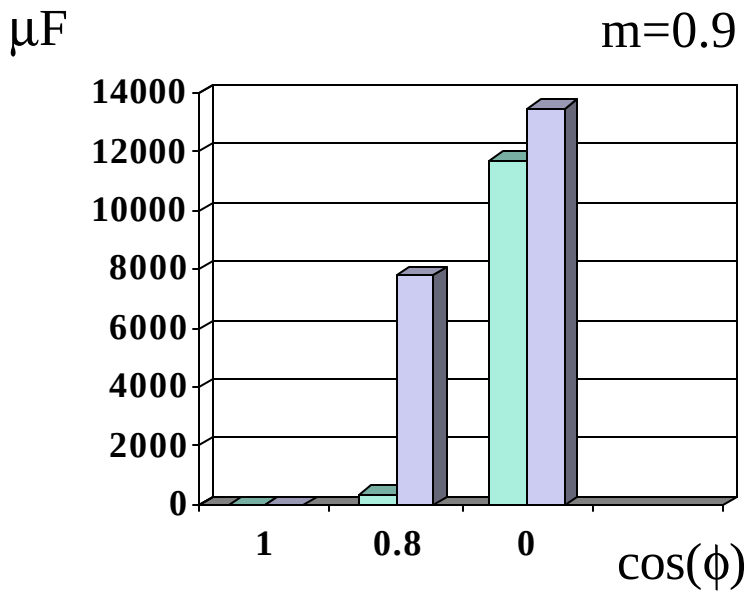

Figure 4.11. Capacitor sizes for specified NP ripple, with and without NP control.

4.5 Experimental Results

A full experimental verification of the results from this chapter requires the converter to operate in all four quadrants and with all possible power factors. In addition, to investigate the situation with the converter as a load (rectifier mode of operation) would require a high-power three-phase current source, and synchronization of that current source with the voltage reference vector. In short, this is a rather difficult requirement, which does not hold the promise of introducing new, and unexpected results[1]. Instead, Figure 4.12 shows the experimental setup used to verify the theoretical results for the inductive loads of three different power factors, namely, 85, 45 and 12 degrees.

[1] Operating a converter in a rectifier mode with the current loop closed and with a high voltage ripple in the NP (due to the low power factor) seemed like a risky experiment.

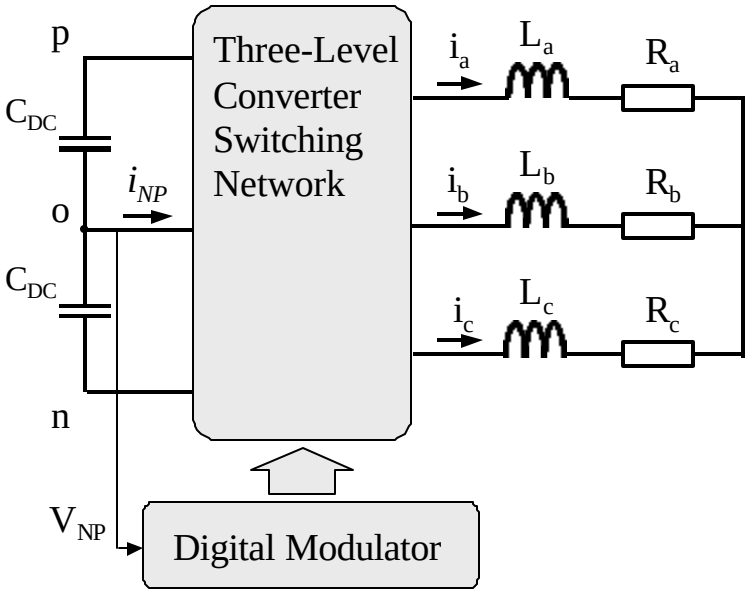

Figure 4.12. Experimental verification of NP voltage ripple properties.

The dc-link voltage was set to 80V. There were three different load conditions. Three, 1.8 mH, inductors in series with three .06Ω resistors were used as 85 degrees reactive power factor load. Three .72Ω resistors in series with the same inductors for the 45 degrees reactive power factor and finally three1Ω resistors in series with three .6mH inductors for 12 degrees inductive load. The experimental results in Figure 4.13 show the ripple in the NP voltage normalized with the amplitude of the phase current, when the load with the power factor angle of 85 degrees is connected to the ac terminals. Finally, the collection of experimental results for different operating points (Figure 4.13) show excellent agreement with the theoretical result from this Chapter.

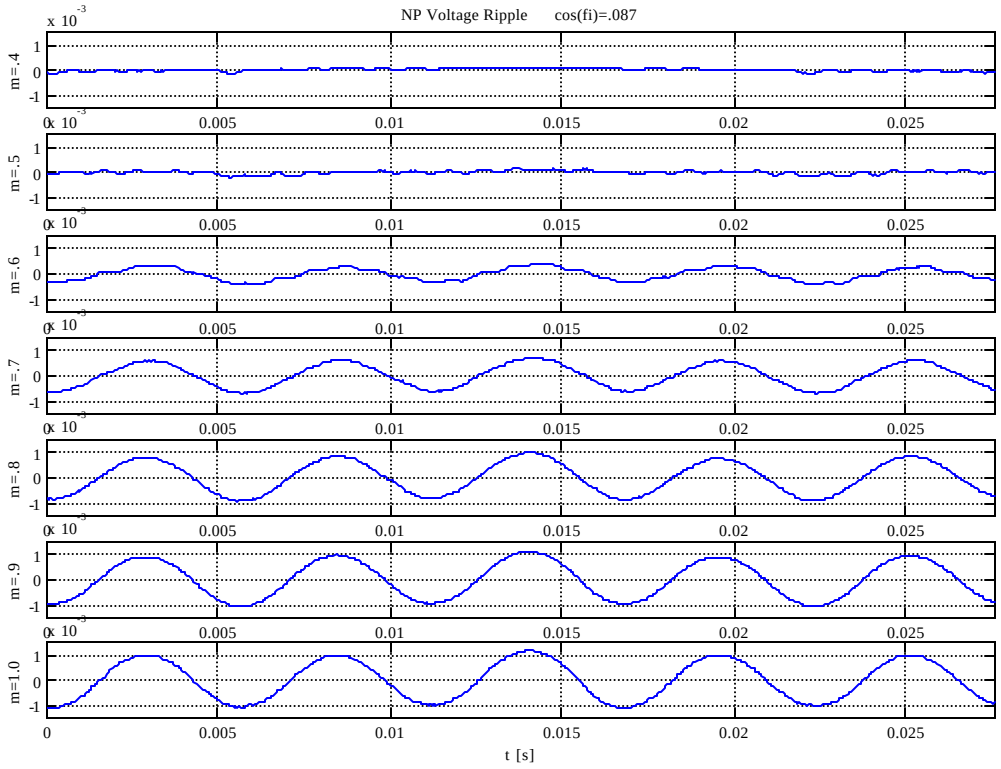

Figure 4.13. Normalized NP voltage for power factor angle of 85 degrees.

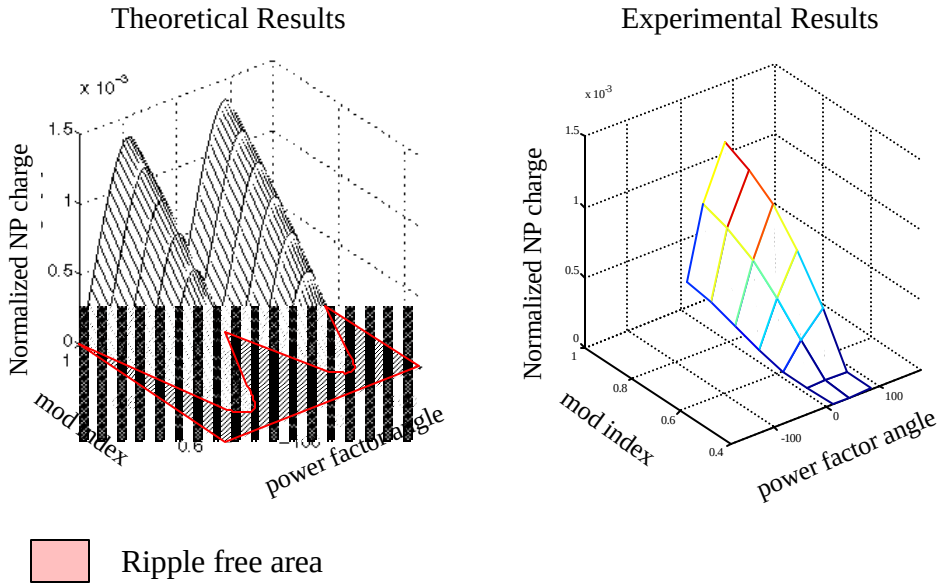

Figure 4.14. Theoretical and experimental normalized NP voltage ripple.

4.6 Conclusions

This chapter introduces a novel approach to modeling the three-level space vector modulator for the purpose of investigating the characteristics of NP balancing. The model is general and can be used to describe any SVM and its effect on the NP.

Using the modeling approach developed in the beginning of the chapter, properties of NP control were studied for one particular SVM. The study identified the region in which the NP can be balanced on a switching cycle level, and offered an intuitive explanation of the origin of the ripple. In addition, a quantitative study of NP balancing offered a normalized size of the dc-link voltage ripple for all possible operating conditions, which is essential information for the design of dc-link capacitors.

Finally, from this study of NP balancing (and from available literature), it is clear that the NP can be balanced in a three-level converter for all possible operating conditions. However, the question of tradeoff between the size of the ripple and the size of the dc-link capacitors remains. Furthermore, through the use of the feed-forward algorithm, introduced in the next chapter, this tradeoff can be extended to include the trade off between the voltage capacity of the switches and the size of the dc-link capacitors.

5 FEED-FORWARD CONTROL OF THREE-LEVEL NEUTRAL-POINT CLAMPED CONVERTERS

From the analysis in the previous chapter, as well as that shown in the many cited references, it becomes clear that the load with the low power factor creates a ripple current in the NP of the three-level converter. Because the majority of the three-level converters used for the drive applications need a significant energy storage in order to compensate for the possible disturbances in the utility line voltage, the low-frequency current ripple often does not determine the size of the dc-link capacitors.

However, if the goal is to design an optimized converter, one that does not have the need for excessive energy storage, then the amplitude of the ripple current flowing into the NP becomes a primary factor in determining the size of the dc-link capacitors. This is the situation for which the results from the previous chapter become important.

Further thinking about capacitor-size optimization leads to the question of whether the size of the dc-link capacitors can be further reduced if a certain amount of the NP ripple can be tolerated. The answer to that question is positive, if two basic requirements are satisfied. The first requirement is that the switches must be able to handle the extra voltage stress, and the second requirement is that an effective feed-forward algorithm must be constructed in order to

compensate for the distortion in the output ac voltage waveforms that occur due to the ripple in the NP voltage.

Therefore if an effective stable algorithm can be found, then allowing a certain amount of voltage ripple can be a good way to save on the capacitor size. Furthermore, the only hardware requirement for the implementation of this algorithm is the dc-link sensors, which are needed for the NP controller as well, and are therefore available almost by default. In addition, such an approach can, with few modifications, be applied to other converter topologies such as the flying capacitor topology or even the cascaded full-bridge converter. For these reasons, this chapter will first propose and than make a detailed study of a feed-forward algorithm that can effectively compensate for the ripple in the NP.

5.1 The Effect of the Capacitor Charge Imbalance on the Voltage Space Vectors

The task of the modulator is to determine the switching sequence of the equivalent switches from Figure 5.1 that will result (in the average sense) in the synthesis of the voltage reference vector commanded by the system controllers. Also (as was already mentioned) every switching state produces well-defined three-phase line voltages, which can be represented as two-dimensional voltage space vectors (as shown in Figure 5.2). The goal at this point is to examine how the error in the NP affects the voltage space vectors. It is convenient to use the definition of the error in the NP voltage given in Figure 5.3.

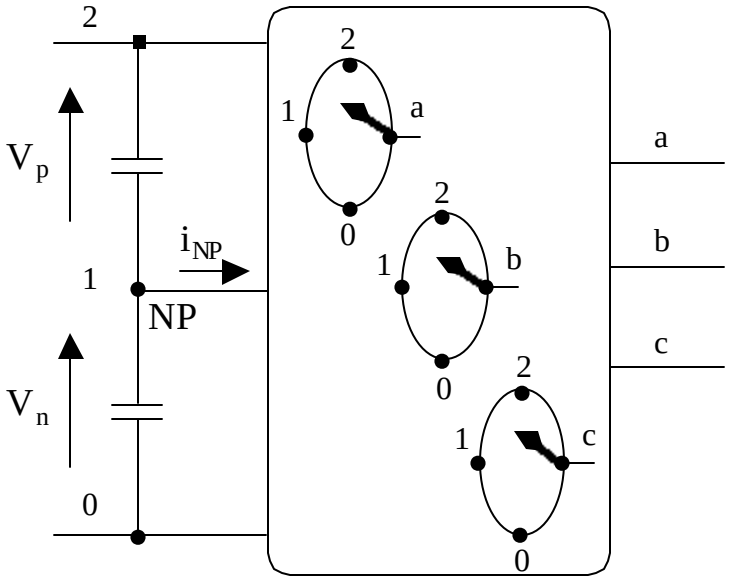

Figure 5.1. Functional diagram of a three-level converter.

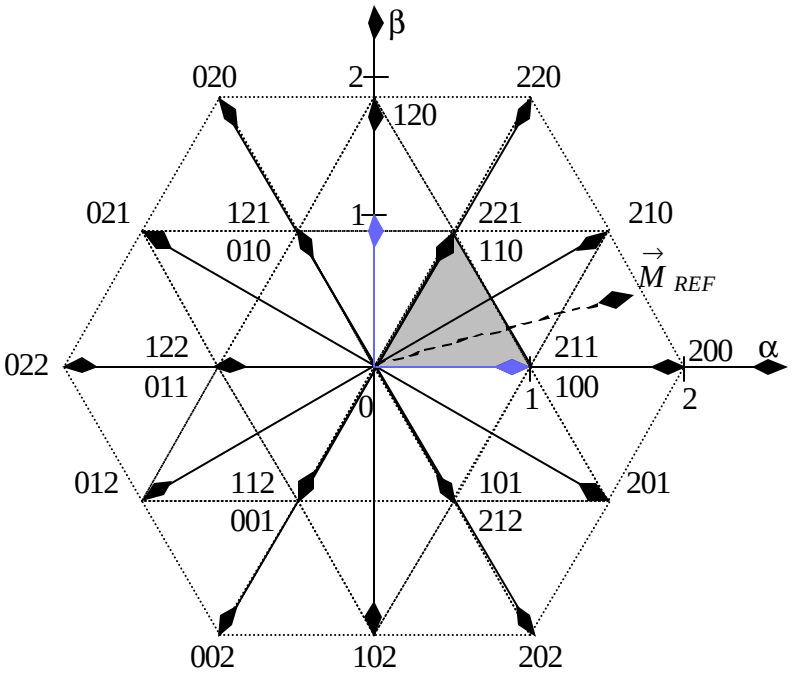

Figure 5.2. Voltage space vectors of a three-level converter.

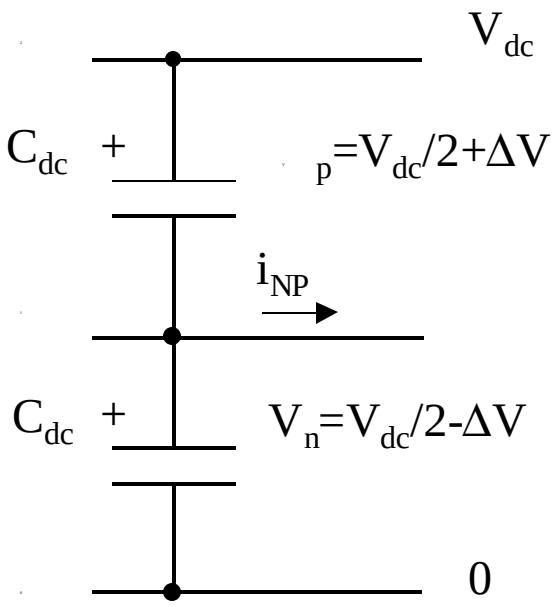

Figure 5.3. The definitions of the dc-link voltages and the voltage error in the NP.

Because the large voltage space vectors do not connect any of the phases to the NP, these vectors remain unaffected by the voltage error in the NP. On the other hand, voltage error in the NP does affect both medium and small voltage vectors. For example, if the NP voltage error, ΔV, is smaller than 0, the medium vectors shift like as shown in Figure 5.4. From the same figure, it is clear that one of the line voltages remains unaffected, which explains why the tip of the medium vectors slides along the outer border of the hexagon. Table 5-I shows how the line-to-line voltages of each medium vector are affected.

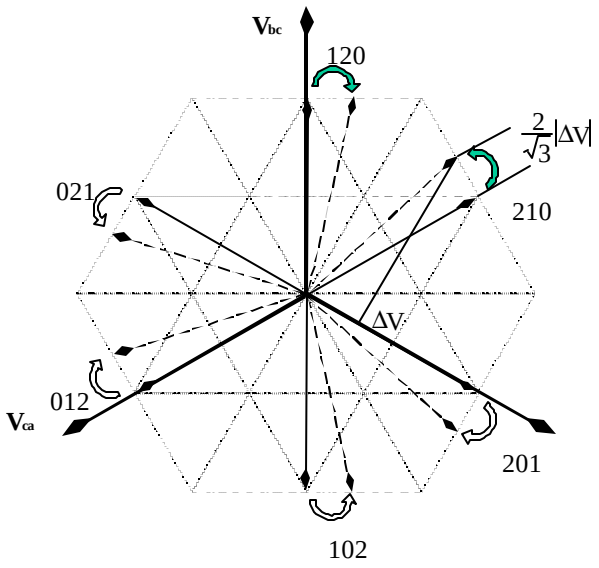

Figure 5.4. Shift of the medium voltage vectors due to the ΔV>0 error in NP voltage.

Table 5-I Effect of the error in NP voltage on the medium voltage vectors.

	210	120	021	012	102	201
V_{ab}	$V_{dc}/2-\Delta V$	$-V_{dc}/2+\Delta V$	$-V_{dc}$	$V_{dc}/2-\Delta V$	$V_{dc}/2+\Delta V$	V_{dc}
V_{bc}	$V_{dc}/2+\Delta V$	V_{dc}	$V_{dc}/2-\Delta V$	$V_{dc}/2-\Delta V$	$-V_{dc}$	$-V_{dc}/2-\Delta V$
V_{ca}	$-V_{dc}$	$-V_{dc}/2-\Delta V$	$V_{dc}/2+\Delta V$	V_{dc}	$V_{dc}/2-\Delta V$	$-V_{dc}/2+\Delta V$

Small vectors are affected by the error in NP in a somewhat different way. While there is no error in the NP voltage, each small vector switching combination has the same magnitude and phase. On the other hand, when there is an error in the NP voltage, each of the switching combinations of a small vector turns into a different small vector. Therefore, the effective "splitting" of the small vectors (shown in Figure 5.5) occurs, and only the magnitude changes while the angle remains unaffected. Again, Table 5-II shows a summary of the small vectors' line voltages.

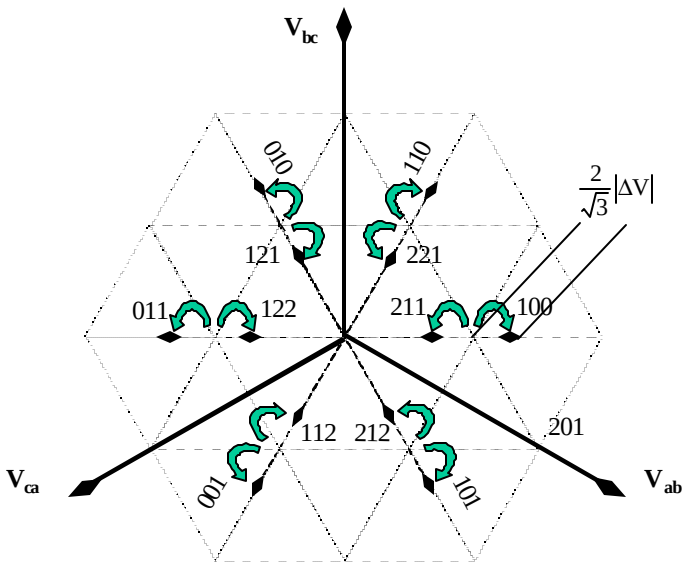

Figure 5.5. "Splitting" of the small voltage vectors due to the $\Delta V>0$ error in NP voltage.

Table 5-II Effect of the error in NP voltage on the small voltage vectors.

	211	221	121	122	112	212
V_{ab}	$V_{dc}/2-\Delta V$	0	$-V_{dc}/2+\Delta V$	$-V_{dc}/2+\Delta V$	0	$V_{dc}/2-\Delta V$
V_{bc}	0	$V_{dc}/2-\Delta V$	$V_{dc}/2-\Delta V$	0	$-V_{dc}/2+\Delta V$	$-V_{dc}/2+\Delta V$
V_{ca}	$-V_{dc}/2+\Delta V$	$-V_{dc}/2+\Delta V$	0	$V_{dc}/2-\Delta V$	$V_{dc}/2-\Delta V$	0
	100	110	010	011	001	101
V_{ab}	$V_{dc}/2+\Delta V$	0	$-V_{dc}/2-\Delta V$	$-V_{dc}/2-\Delta V$	0	$V_{dc}/2+\Delta V$
V_{bc}	0	$V_{dc}/2+\Delta V$	$V_{dc}/2+\Delta V$	0	$-V_{dc}/2-\Delta V$	$-V_{dc}/2-\Delta V$
V_{ca}	$-V_{dc}/2-\Delta V$	$-V_{dc}/2-\Delta V$	0	$V_{dc}/2+\Delta V$	$V_{dc}/2+\Delta V$	0

It is important to note that because the outer boundaries of the hexagon remain unaffected by the error in the NP voltage, the maximum amplitude of the reference vector that can be synthesized remains unaffected by the size of the NP voltage error. This should indicate the feasibility of finding a correction algorithm, and that it should be possible to compensate for the effect of the NP voltage ripple without sacrificing the converter voltage gain. However, a

significant change in the small vectors' amplitude will change their corresponding duty cycles and will ultimately affect their control authority over the NP current. This is only one of the issues discussed in thiscChapter.

5.2 Sine Triangle Modulation for Three-Level Converters

Although SVM is perhaps the most general and unrestricted approach to the generation of PWM signals, and although the sine triangle modulation is basically a subset of SVM[1], it might be the subset that is significantly simpler to model and easier to understand. That is the principle reason why in this chapter it is the sine triangle modulator that will be predominantly studied. Then, with few restrictions, the conclusions can also be used to explain the behavior of the space vector modulator.

5.2.1 PWM Generation with Sine Triangle Modulation

All sine triangle modulations are the same in the sense that that the intersection between the carrier triangular waveform and the modulation signal determines the switching instances. The main variations are in the exact shape of the carrier waveform and/or the modulating signal that can be augmented with the third harmonic for increased voltage gain, and so on.

Then, using the same basic principle, a multilevel modulator can be constructed that will have *n-1* carrier waveforms, where *n* is the number of levels. As an example, Figure 5.6 shows a basic three-level sine triangle modulator.

[1] Historically, sine triangle modulation was the only option when implementing the modulator with discrete components. However when implemented with the processor, the distinction between the two implementations (in terms of versatility and freedom to optimize the PWM signals) diminishes.

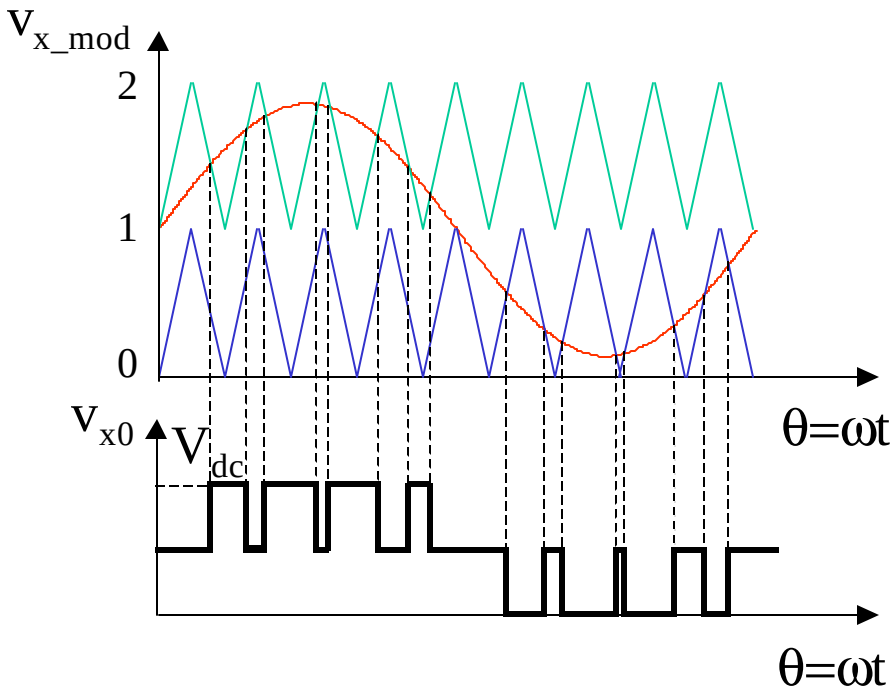

Figure 5.6. Principle of sine triangle modulation for a three-level converter.

5.2.2 NP Control With Sine Triangle Modulation

Adding the zero sequence to the modulating sinusoidal waveform controls the charge balance in the NP. This is really the method used so far throughout this dissertation, because manipulating the switching combinations of small vectors actually manipulates zero sequence.

$$
\begin{aligned}
v_{a\_mod} &= A \cdot \sin(w \cdot t + j) + d + 1 \\
v_{b\_mod} &= A \cdot \sin(w \cdot t + j - 2 \cdot p / 3) + d + 1 \\
v_{c\_mod} &= A \cdot \sin(w \cdot t + j + 2 \cdot p / 3) + d + 1
\end{aligned}
\qquad \text{(5-1)}
$$

Figure 5.7 shows how a constant zero sequence shifts the power transfer to the upper of the split dc-link capacitors, which then (depending on the direction of the power flow) becomes charged or discharged more than the lower dc-link capacitor. Therefore, depending on the

direction of the power flow, a specific amount of zero sequence can be added to correct for the disturbance.

It is important to note, however, that similar to the space vector modulator, this type of control has its limitations. For example, if the modulating sinusoid is too large, there might be little or no room to add the zero sequence. In that case, the size of the ripple current will depend solely on the load impedance and load power factor, which is a limitation that applies to the SVM as well. Despite these limitations, from the modeling point of view, sine triangle modulation has one big advantage. The NP controller needs to supply only one control variable, and does not really require information on the direction of phase current, but only on the direction of power flow. This greatly facilitates writing equations and developing the model.

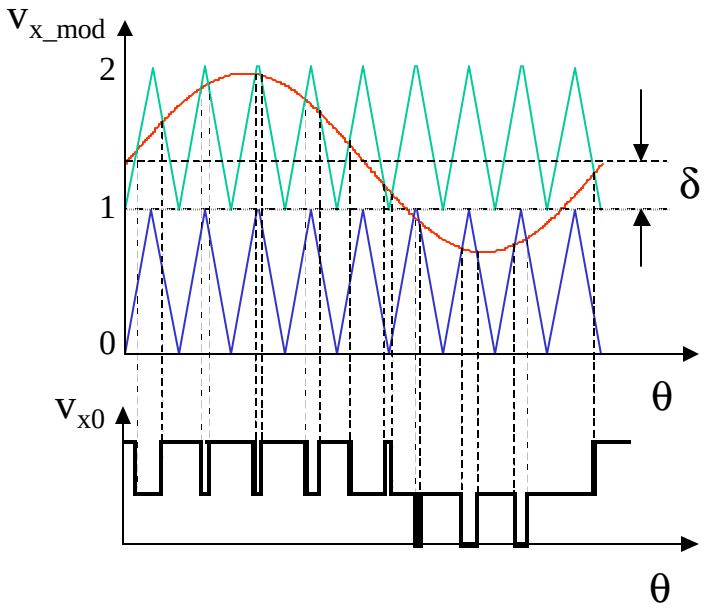

Figure 5.7. Principle of NP control for the three-level converter.

5.2.3 The Average Model of a Sine Triangle Modulator

By magnifying the time scale and looking into the process of computing the duty cycles, there are really two cases to consider. Figure 5.8 shows both cases: one in which the modulating signal

is compared with the upper carrier waveform, and the other in which it is compared to the lower modulating waveform. Because it is advantageous for the utilization of multiple dc voltage levels and because it reduces the switching frequency ripple, it almost goes without saying that all the switching should occur between the two closest levels. Accordingly, from the left-hand side of the illustration in Figure 5.8, the modulator will connect the phase output to the positive rail for time $d_p \cdot T$, where

(5-2) $$d_p = v_x - 1 \qquad x \in \{ a,b,c \}$$

and v_x is the modulating signal for phase x, $x \in \{ a,b,c \}$. The duty cycle for the NP is then,

(5-3) $$d_0 = 1 - d_p = 2 - v_x .$$

When the modulating signal is compared with the bottom carrier waveform the duty cycles for NP and for the negative dc rail are

(5-4) $$d_0 = v_x$$

and

(5-5) $$d_n = 1 - v_x .$$

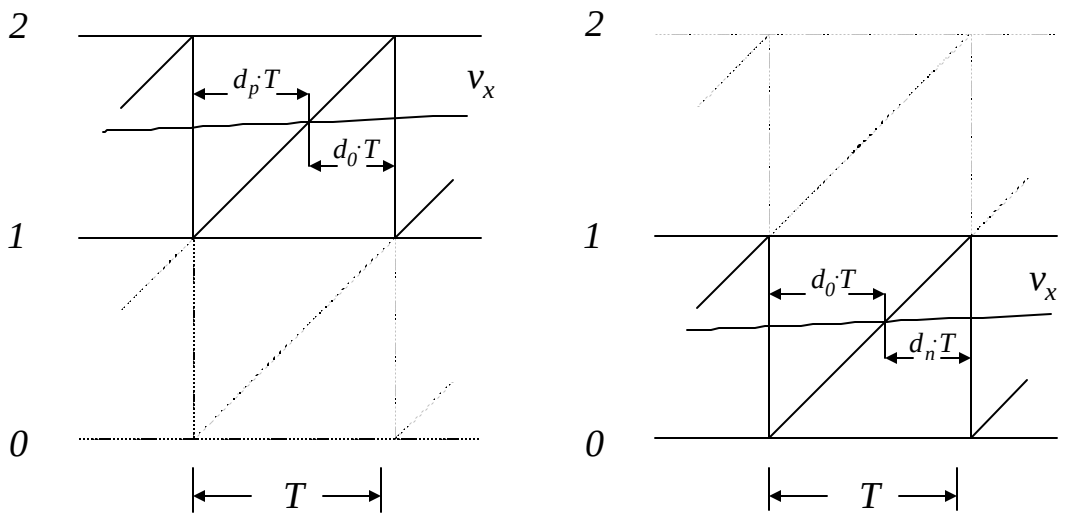

Figure 5.8. Duty cycles for the sine triangle three-level modulation.

Perhaps the most intuitive (and although approximate, quite accurate), is the modeling approach published by Newton and Sumner [B14]. The modeling approach averaged the NP current during the line cycle, which results in the expression that describes the relationship between the zero sequence command, the amplitude of the modulating signal, the load power factor and the NP current that is to be controlled. That expression can then be linearized around an operating point and that model can be used for control design. This chapter will first briefly repeat Newton and Sumner's methodology and main resultsthen extend those results in order to model the sine triangle modulator with feed-forward control.

To find the line cycle average of the current flowing through the NP, it is necessary to first study the duty cycles of one phase leg, as shown in Figure 5.9. Clearly, the phase flows through the NP for the duration of the NP duty cycle d_1. From (5-2) and (5-3), and after substituting the modulating v_{a_mod} from (5-1), the duty cycle of the NP can be expressed as follows:

(5-6) $$d_1 = \begin{cases} 1 - A \cdot \sin(q) & 0 \le q < p \\ 1 + A \cdot \sin(q) & p \le q < 2 \cdot p \end{cases}.$$

Hence the average current flowing in the NP during one line cycle is

$$\overline{i_{NP}} = \frac{1}{2 \cdot p} \cdot \left[\int_{0}^{p} I \cdot \sin(q + j)(1 - A \cdot \sin(q)) \cdot dq + \int_{p}^{2p} I \cdot \sin(q + j)(1 + A \cdot \sin(q)) \cdot dq \right], \tag{5-7}$$

which quite expectedly, turns out to be zero ($\overline{i_{NP}} = 0$) for any power factor angle j. It might be clear (but it is still important to point out) that this analysis does not study the low-frequency, mainly third-harmonic ripple that is present in the NP. All it says is that under ideal conditions, regardless of the power factor angle, the line cycle average of the NP current will be zero.

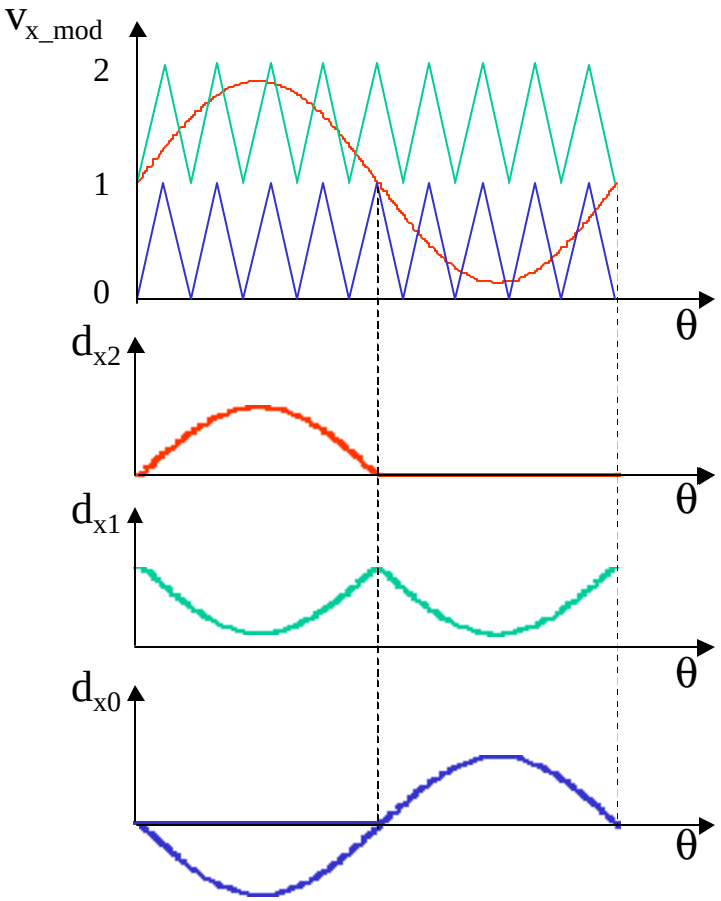

Figure 5.9. Duty cycle of one phase equivalent switch for sine triangle modulation.

However, even though in ideal conditions the NP current is zero, the feedback implementation is required to insure that the capacitor charge can balance during the transients or in the presence of disturbances. In that case, it is important to analyze the average current in the NP for different phase angles in order to determine the control authority of the zero sequence over the NP. The integration is a little more involved in that case because the integration limits that correspond to the zero sequence δ need to bedetermined. From Figure 5.10, it is clear that the first discontinuity in the duty cycles occurs for

(5-8) $$1+\sin(\alpha)+\delta = 1,$$

which sets the first integration limit at

(5-9) $$\alpha = -\sin^{-1}\left(\frac{\delta}{A}\right).$$

From there, the remaining two integration limits are simply

(5-10) $$\beta = \pi - \alpha \text{ and } \gamma = 2\cdot\pi + \alpha .$$

The line cycyle average NP current can be computed from

(5-11) $$\overline{i_{NP}} = \frac{3}{2\cdot\pi}\cdot\left[\int_{\alpha}^{\beta} I\cdot\sin(\theta+\varphi)(1-(A\cdot\sin(\theta)+\delta))\cdot d\theta + \int_{\beta}^{\gamma} I\cdot\sin(\theta+\varphi)(1+(A\cdot\sin(\theta)+\delta))\cdot d\theta\right],$$

resulting in the following expression for the line cycle average of the NP current:

(5-12) $$\overline{i_{NP}} = \frac{-3\cdot I}{A\cdot\pi}\cdot\cos(\varphi)\left[\delta\cdot\sqrt{A^2-\delta^2} + A^2\cdot\sin^{-1}\frac{\delta}{A}\right],$$

valid only for

(5-13) $$A < 1 + d < 2 .$$

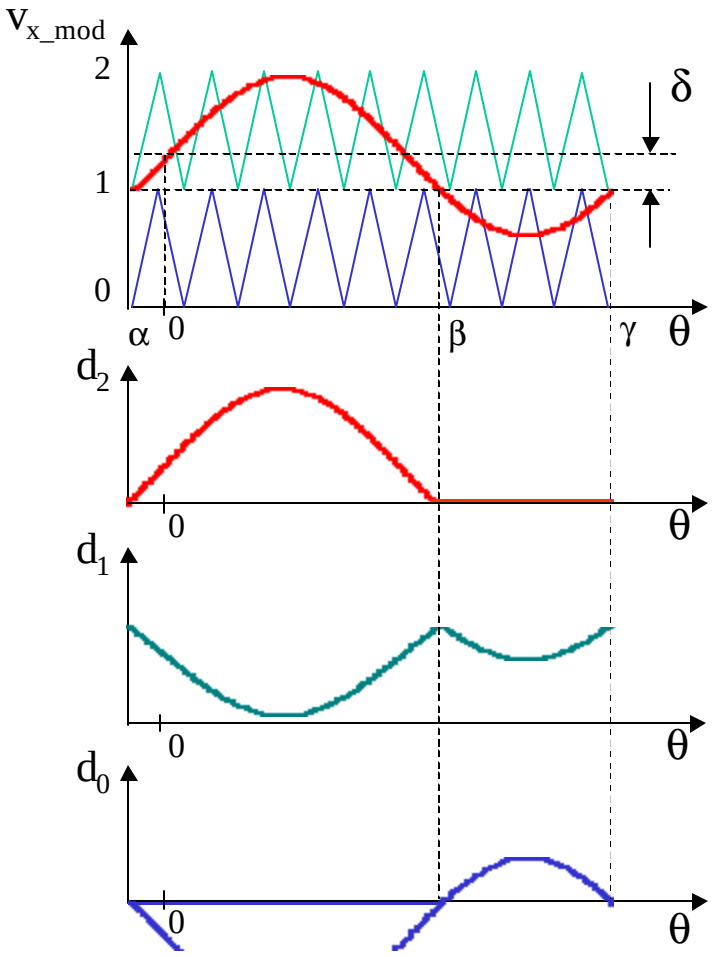

Figure 5.10. Duty cycles of one phase with the zero sequence present.

5.3 Modeling the Feed-Forward Control

If the modulator computes the duty cycles and selects the vectors under the assumption that the charge in the dc-link capacitors is balanced, then the modulator would make an error

whenever the capacitor charge was imbalanced. Most of the modulation algorithm does not take this possibility into account, perhaps because it is assumed that the dc-link capacitors will be able to sufficiently minimize the voltage ripple in the NP.

However, as already mentioned, if a certain amount of ripple in the NP can be tolerated, then that is one way to make significant savings on the size of the dc-link capacitors. In that case, a feed-forward control algorithm that allows the modulator to take into account the ripple in the NP and still produce high-quality sinusoidal output waveforms becomes significant.

5.3.1 The Feed-Forward Algorithm

The idea behind the feed-forward algorithm is to modify the amplitude of the triangular carrier waveforms so that the ratio of upper and lower carrier waveform corresponds to the ratio of upper and lower dc-link capacitor voltage. One way to satisfy this requirement is to control the amplitude of the triangular modulating waveform to make sure that the following condition is always satisfied:

(5-14) $$K_p = \frac{V_p}{V_{dc}/2} \text{ and } K_n = \frac{V_n}{V_{dc}/2},$$

where K_p and K_n are the amplitudes of the top and bottom carrier waveforms, respectively. In that case,

(5-15) $$\frac{K_p}{K_n} = \frac{V_p}{V_n} \text{ and } K_p + K_n = 2$$

also holds true.

From Figure 5.11 (and with the help of a little trigonometry), it turns out that when the modulating signal is larger than K_n, the phase duty cycles are

(5-16) $$d_2 = \frac{v_x - K_n}{K_p} \text{ and } d_1 = \frac{2 - v_x}{K_p},$$

and when the modulating signal is lower than K_n, the duty cycles are

(5-17) $$d_1 = \frac{v_x}{K_n} \text{ and } d_0 = \frac{K_n - v_x}{K_n}.$$

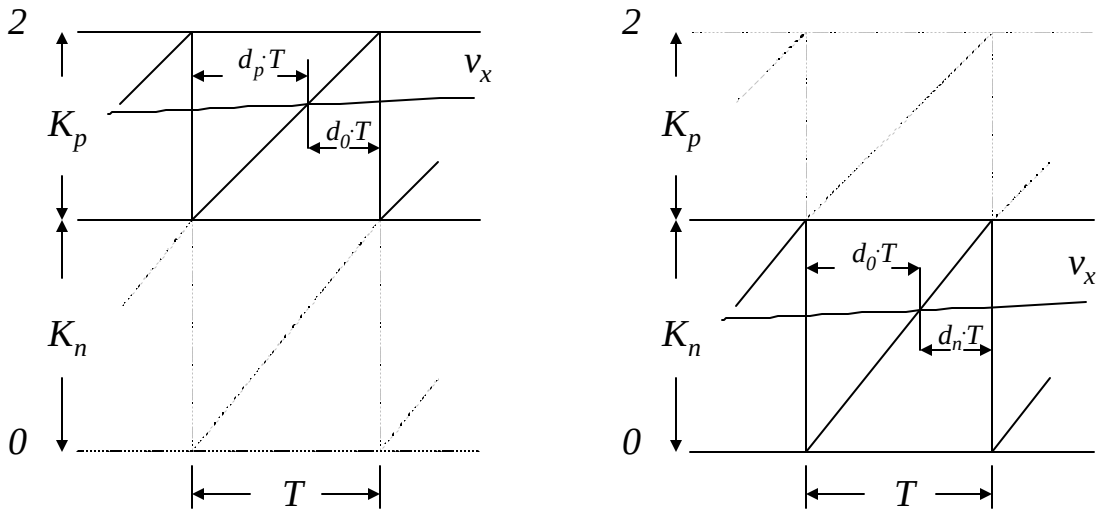

Figure 5.11. Duty cycles for the sine triangle three-level modulation.

5.3.2 Mathematical Basis of the Feed-Forward Algorithm

Even though the development of the feed-forward algorithm is quite intuitive, it might not be at all obvious whether there will be a discontinuity when the modulating signal crosses the "moving" boundary between the upper and lower carrier signals. In order to examine the effects of crossing the boundary, it is probably easiest to write equations for the average output voltage for the case in which the modulating signal $v_x(t) > K_n$, and when the $v_x(t) < K_n$, where

(5-18) $$v_{x\_mod} = A \cdot sin(q) + K_n + d \,,$$

and where

(5-19) $$v_{x\_mod} \in [0,2] \qquad A \in [0,1] \,, A < K_n + d < 2 - A.$$

The output voltage for the case when $v_{x\_mod}(q) > K_n$ is

(5-20) $$v_{x0} = d_p(q) \cdot V_p \ .$$

After substituting equation (5-16), the output voltage can be written as

(5-21) $$v_{x0} = \frac{v_x(q) - K_n}{K_p} \cdot V_p \,,$$

and finally, after substituting the relation from (5-14), the final form of the output voltgae is

(5-22) $$v_{x0} = (v_x(q) - K_n) \cdot \frac{V_{dc}}{2}.$$

Using the same steps, the output voltage of the modulator, for the case when the $v_x(q) < K_n$, turns out to be

(5-23) $$v_{x0}(t) = -d_n(q) \cdot V_n = \frac{K_n - v_x(q)}{K_n} \cdot V_n = (v_x(q) - K_n) \cdot \frac{V_{dc}}{2} \,,$$

which is exactly the same expression as (5-22). Therefore, there are no discontinuities at the boundary of the lower and upper carrier waveform for the feed-forward algorithm (5-14). This ends the proof.

5.3.3 Average Model of the Zero-Sequence NP Control

In terms of NP the switching network in Figure 5.1 (together with any source or the load that might be connected to its ac side) is just a current source like the one in Figure 5.12. What complicates this otherwise simple modeling approach is that there are multiple dependencies of the source that are influenced not only by the phase angle of the load and the feed-forward terms, but also by the zero sequence of the modulating signal. Still, as the experimental results in the next chapter will prove, because of the filtering properties of the dc-link capacitors most of the unmodeled dynamics from the load and the output filters will appear only as a nonlinear gain in the NP controller loop. That is the principle argument for the application of the line-cycle averaging method in the study of NP voltage dynamics.

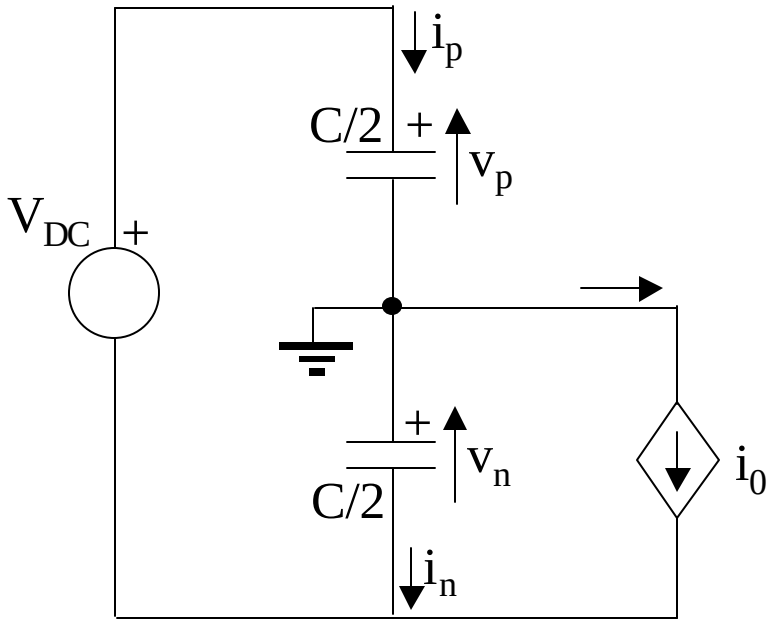

Figure 5.12. The model of the modulator with respect to the NP current.

As shown in Figure 5.12, the voltage in the NP depends on the equivalent NP current, which again depends on the load currents and the NP duty cycle of each phase,

(5-24) $$C\frac{dv_p}{dt} = d_{a0}\cdot i_a + d_{b0}\cdot i_b + d_{c0}\cdot i_c .$$

In order to perform line-cycle averaging, the boundary between the piece-wise linear NP duty cycles needs to be determined. As shown in Figure 5.13, and similar to the equation (5-8), the first discontinuity in the duty cycle comes from the following condition:

(5-25) $$K_n + d + A\cdot sin(\alpha) = K_n .$$

From this equation and Figure 5.13, it becomes clear that the integration boundaries are in fact the same as those in (5-11),

(5-26) $$\alpha = -sin^{-1}\frac{d}{A},\ \beta = \pi - \alpha \text{ and } \gamma = 2\cdot\pi + \alpha .$$

Substituting the modulating signal, defined in Figure 5.13 as $v_x = K_n + d + A\cdot sin(\theta)$, into the expressions for NP duty cycles, d_0 in (5-16) and (5-17), the line-cycle average of the NP current can be found by integrating

(5-27) $$\overline{i_{NP}} = 3\cdot\left[\int_a^b I\,sin(\theta+\varphi)\cdot\left(\frac{2-(K_n+d+A\,sin(\theta))}{K_p}\right)\cdot d\theta + \int_b^g I\,sin(\theta+\varphi)\cdot\left(\frac{K_n+d+A\,sin(\theta)}{K_n}\right)\cdot d\theta\right],$$

which results in the expression

(5-28) $$\overline{i_{NP}} = \frac{-3\cdot I\cdot cos(\varphi)}{4\cdot\pi\cdot A\cdot K_n\cdot K_p}\cdot\left[2\cdot(4\cdot K_n + 2\cdot d - 4)\cdot\sqrt{A^2-d^2} - A^2\cdot\pi\cdot(K_n - K_p) + 2\cdot A^2\cdot(K_p + K_n)\cdot sin^{-1}\left(\frac{d}{A}\right)\right],$$

which is valid for

(5-29) $$A < K_n + d < 2 - A.$$

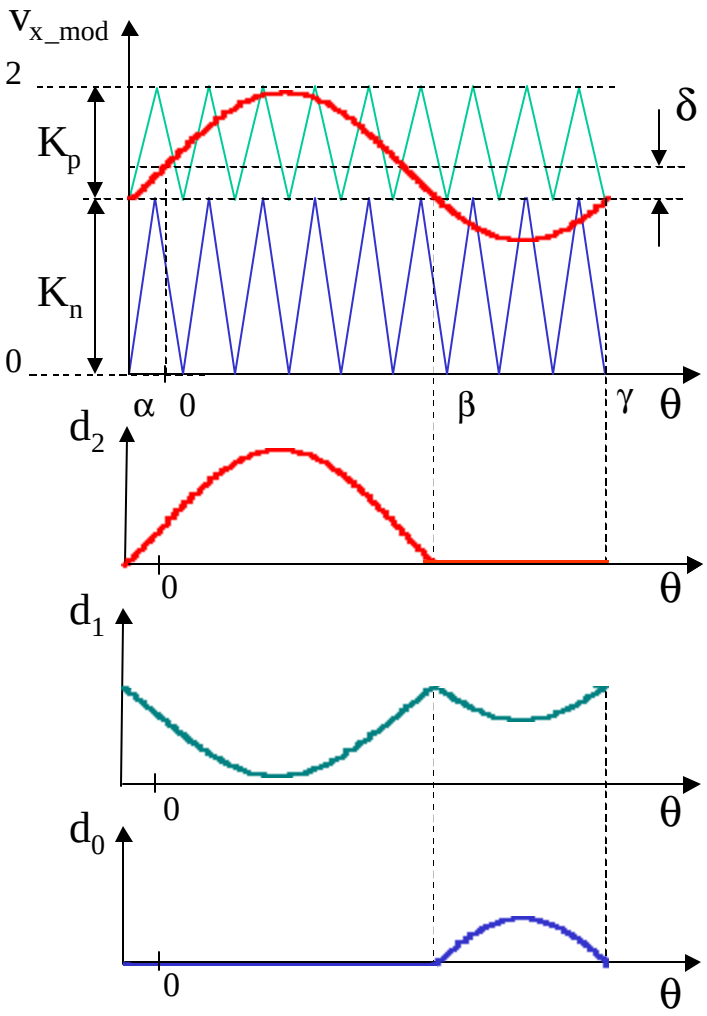

Figure 5.13. The duty cycles of the sine triangle modulator with zero sequence.

Outside the region defined in (5-29), the modulator works in overmodulation mode, which is not covered in this analysis. Otherwise, if the dc-link capacitor charges are balanced ($K_P = K_n = 1$), Equation (5-28) simplifies to the following expression for the average NP current with no feed-forward terms:

(5-30) $$\overline{i_{NP}} = \frac{-3 \cdot I}{\pi \cdot A} \cos(\varphi) \left[d \cdot \sqrt{A^2 - d^2} + A^2 \cdot \sin^{-1} \frac{d}{A} \right]$$

5.3.4 A Small-Signal Model of the Zero-Sequence NP Control

The average model of the zero-sequence control in the NP can be derived by developing the expression for the average current (5-28) into Taylor's series around the operating point $d = 0$, $K_p = K_n = 1$, and then by neglecting the higher-order terms as follows:

(5-31) $$\overline{i_{NP}}(d) = \overline{i_{NP}}(0) + \frac{\partial \overline{i_{NP}}}{\partial d}(0) \cdot d + \frac{\partial^2 \overline{i_{NP}}}{\partial d^2}(0) \cdot d^2 + \ldots$$

The first derivative of the average NP current (with respect to d) is

(5-32) $$\frac{\partial \overline{i_{NP}}}{\partial d} = -\frac{3 \cdot I \cdot \cos(\varphi)}{4 \cdot \pi \cdot K_n \cdot K_p} \cdot \left[(K_n + K_p) \cdot \frac{2 \cdot A}{\sqrt{A^2 - d^2}} - (K_n + K_p) \cdot \frac{2 \cdot d \cdot (2 \cdot K_n + 2 \cdot d)}{A \sqrt{A^2 - d^2}} + \right.$$
$$\left. + \frac{2}{A} (K_n + K_p) \cdot \sqrt{A^2 - d^2} - \frac{8 \cdot d}{A \cdot \sqrt{A^2 - d^2}} \cdot K_n \right].$$

The first derivative of the line-cycle average in the operating point $d = 0, K_p = K_n = 1$, is

(5-33) $$\frac{\partial \overline{i_{NP}}}{\partial d}(d = 0, K_p = K_n = 1) = -\frac{6 \cdot I}{\pi} \cos(\varphi),$$

while the average value of the line-cycle average of the NP current is zero around the operating point

(5-34) $$\overline{i_{NP}}(d=0, K_p = K_n = 1) = 0 .$$

Finally, at the operating point,

(5-35) $$\overline{i_{NP}} = -\frac{6}{p} \cdot I \cdot \cos(f) \cdot d .$$

Therefore, around the operating point, which assumes the balanced charge in the dc-link capacitors, and when the zero-sequence voltage equals zero, the small-signal average current model is the same as the small-signal model for the modulator without the feed-forward control [B14].

5.3.5 The Stability Analysis of the Feed Forward Algorithm

So far, the line cycle average dynamic model of the sine-triangle modulator with and without the feed-forward control has been derived. In addition, through linearization around the operating point, the small-signal dynamic model of the NP control has been derived as the function of the load power factor, the zero-sequence balancing component and the feed-forward term. The feed forward algorithm has also been proven to not introduce any discontinuities in the output waveform and has shown that it can effectively compensate for any size of imbalance.

However, the feed-forward control does change the ratio between the two triangular carrier signals and, by doing so, it effectively introduces a zero-sequence component which influences the NP control. For example, Figure 5.14 shows the situation in which the feed-forward controller compensates for the significantly higher voltage of the upper dc-link capacitor. At the same time, the size of the modulating signal does not allow the freedom to control the zero sequence for the purpose of NP control.

As clearly illustrated in the situation shown in Figure 5.14, the output is switched more often between the positive rail and the NP than between the NP and the negative rail. In addition, in an exaggerated situation with the bottom dc-link capacitor voltage equal to zero, the output of the converter would never be connected to the bottom dc rail; therefore, all the power would flow between the upper capacitor and the load, and there will be no power flow between the load and the bottom capacitor.

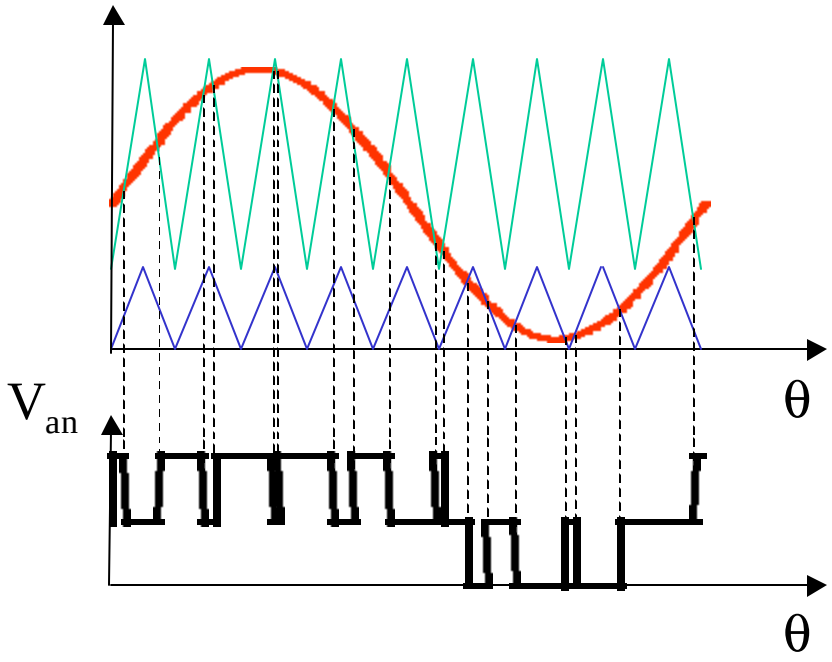

Figure 5.14. The PWM signal with strong feed-forward component.

Evidently, depending on the direction of the power flow, the top capacitor will be either charged or discharged. For example, Figure 5.15 shows the power flow in the inverter mode of operation, with the upper dc-link capacitor at much higher voltage than the bottom and with a high modulation index, as in Figure 5.14. The feed-forward influence will always tend to discharge the capacitor with the higher state of charge, and in that way it exercises a stabilizing influence. Conversely, in the rectifier mode, with the power flowing from the ac to the dc side, the feed-forward algorithm introduces a destabilizing influence by always further charging the capacitor with the higher voltage.

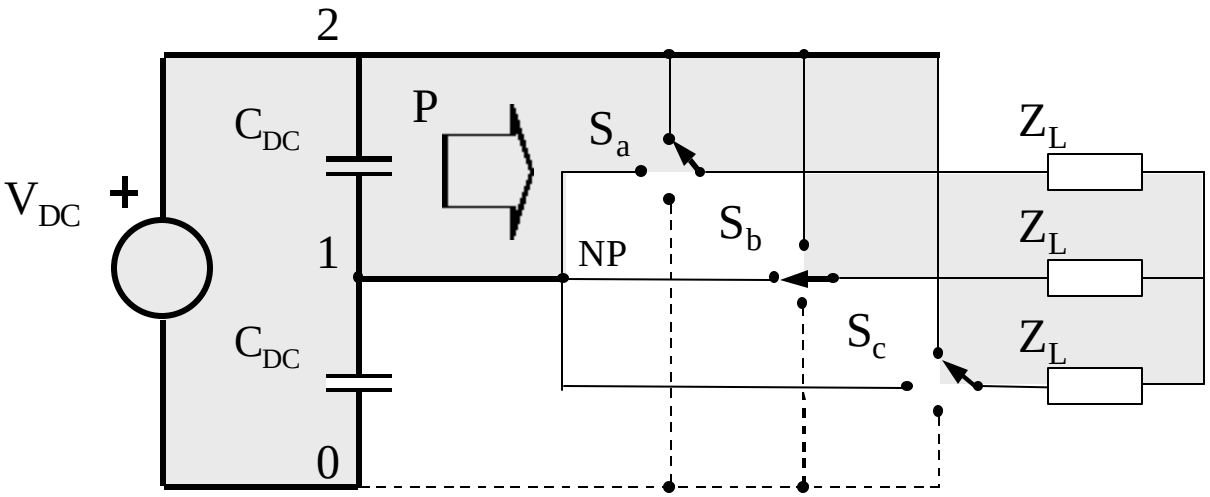

Figure 5.15. Power flow in the inverter mode of operation with large imbalance in NP.

In other words, in the inverter mode of operation, feed-forward control reduces the size of the NP voltage ripple by inherently providing a stabilizing influence. In the rectifier mode of operation however, the feed-forward control still compensates for the disturbance in the line voltage caused by the dc-link capacitor charge imbalance, but it also introduces a destabilizing effect into the NP control. This destabilizing effect can be compensated for with the addition of zero-sequence voltage. Unfortunately, the compensation of the feed forward by the zero sequence limits the maximum amplitude of the modulating signal to $d \in [-min[K_n], min[K_p]]$. Therefore, for the rectifier operation a tradeoff exists between the influence of the feed forward algorithm, the maximum amplitude of the modulating sequence and the maximum ripple that can be allowed in the NP. Still, it is important to point out that this is only a qualitative analysis. In reality, in steady state, the NP voltage has mainly a third-harmonic ripple component, and no fixed dc offset. To exactly determine the wave shape of the voltage in the NP (in order to find the stability boundaries), it would be necessary to solve (5-24) analytically, which is very hard if not impossible, even if the form of the solution is known in advance.

5.4 Implementation of Feed-Forward Algorithm for Space Vector Modulation

The effects of the shift in the NP on the location of the voltage space vectors were discussed earlier in this chapter. The modifications in SVM algorithm that can help compensate for the imbalance will now be discussed. First consider how to synthesize the reference vector located in the sixty-degree region from Figure 5.16.

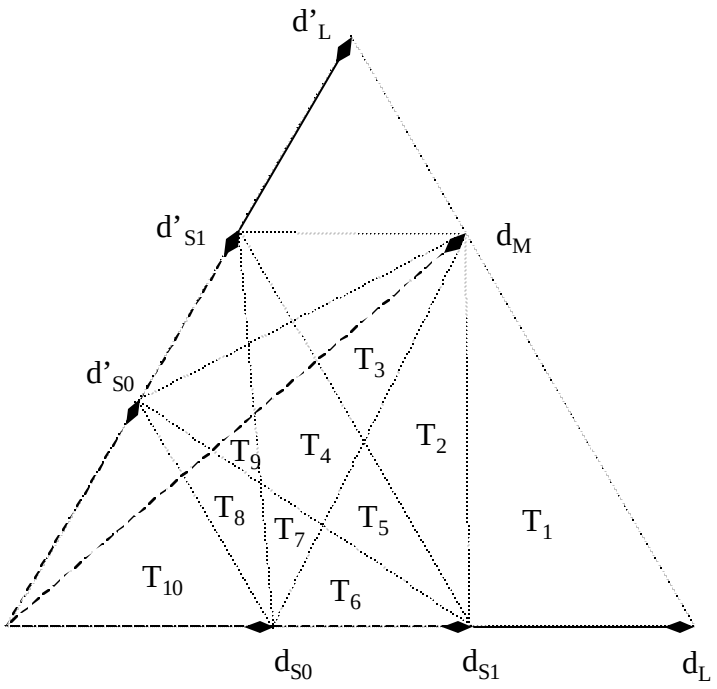

Figure 5.16. The effect of NP unbalance on the boundaries of small triangles.

There are several issues that complicate the implementation of the SVM feed-forward control:

- The boundaries between the small triangles that change as the vector locations change (due to NP ripple). In fact, because of the splitting of the small vectors, there are now ten inner triangular regions within the sixty-degree region, instead of only four.

- Because the vectors change their locations, the fast SVM algorithm can not be used since it relies on the integer values of the voltage space vectors' coordinates. Likewise, the

other algorithms can not rely on the fixed locations of the vectors to simplify the duty cycle calculation.

Perhaps the most troublesome aspect is the identification of the current sector because of the splitting of the small vectors. One way to overcome this problem is based on the virtual small vector approach shown in Figure 5.17. The basic idea of the virtual small vector approach is that the NP controller supplies the ratio between the positive and negative small vectors' switching combinations, therefore determining the amplitude of the equivalent small vector amplitude

(5-36) $$\vec{H} = c \cdot \vec{V}_{S0} + (1-c) \cdot \vec{V}_{S1} \qquad \text{where} \quad c \in [0,1].$$

This method is approximate, because it uses the NP controller command from the previous switching cycle, but from the implementation point of view it might be the most practical implementation. In addition, because the switching frequency is usually very high for the slow dynamics of dc-link capacitors, it is probably more than acceptable to use the previous switching cycle value of the NP controller.

But, for the sake of argument, consider the approach that can both compensate for the disturbance in the NP and maintain the NP current at zero on the switching-cycle level. It is possible to meet both these requirements in the operating region we have identified in the previous chapter. Therefore, in order to both maintain NP current at zero during each switching cycle and to compensate for the disturbance, an iterative approach might be required, due to the troublesome "splitting" of the small vectors.

In fact, in order to select the small triangle, its boundary needs to be known, but the boundary is not known before the duty cycles of the small vectors are selected. However, the duty cycles of the small vectors depend on the boundary as well, and are computed from a different set of equations for each small triangle. This means that the triangular region must be guessed initially, and than all the equations are solved and then checked to be sure the boundary conditions are satisfied. This is hardly a practical approach.

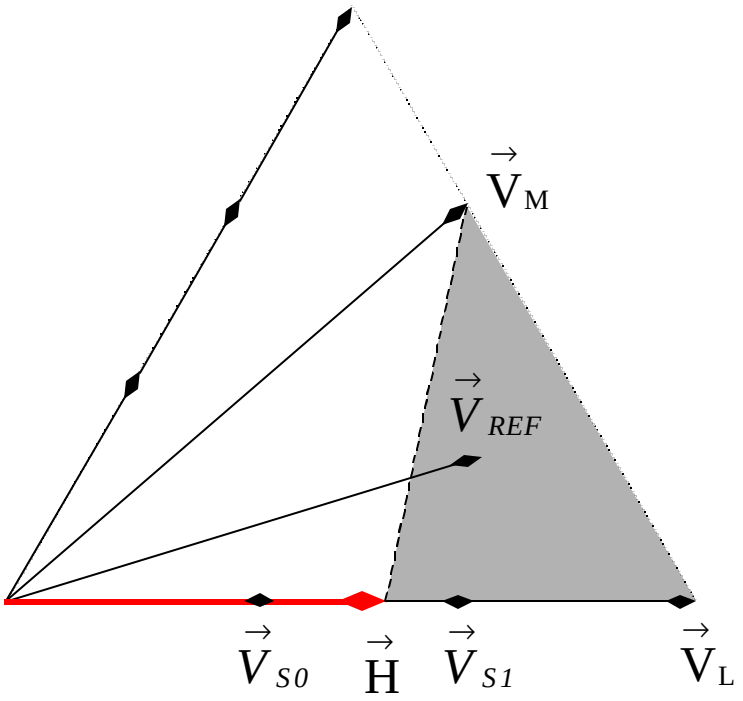

Figure 5.17. The active sector computation based on the home vertex algorithm.

Returning to the approach using the virtual small vector, it is clear that when the location of the small vector is known (or better to say predetermined by the NP controller), then all the small triangle boundaries are known, which allows the duty cycles to be computed, as follows:

(5-37) $$\vec{V}_{REF} = d_H \cdot \vec{H} + d_L \cdot \vec{V}_L + d_M \cdot \vec{V}_M ,$$ where

(5-38) $$d_H + d_L + d_M = 1 .$$

Finally, the small vectors' duty cycles are then easy to find, as follows:

(5-39) $$d_{S0} = c \cdot d_H , \quad d_{S1} = (1 - c) \cdot d_H .$$

This concludes the implementation of the proposed feed-forward algorithm, for the case of the outer triangular region. If vector $\vec{V}^*$ is located in one of the inner triangle region the algorithm remains the same. The only difference is that there are two home vertices to take into account in determining the boundary regions and in duty-cycle computations.

5.5 Conclusions

This chapter introduces and analyzes the feed forward algorithm as a method to successfully compensate for NP voltage ripple of any size and thus allow the tradeoff between the voltage capacity of the switching devices and the size of the dc-link capacitors.

The influence of the new algorithm on the control of the NP is studied using the example of the sine triangle modulator. The influence of the modulator on the NP controller is shown by the average models developed at two different time scales: first at the fast scale (the time scale of the switching frequency); then those results were used to develop an average model on the slow scale (the time scale of the line-cycle average). The line-cycle average model of the sine triangle modulator's influence on the control of the NP is then linearized around the operating point and can be used to design on NP voltage controller.

In addition, the qualitative analysis shows that the feed-forward algorithm introduces an additional stabilizing effect into the NP control in the inverter mode of operation. In the rectifier mode of operation, the same analysis shows that the feed-forward control introduces a destabilizing effect, which can essentially limit the voltage gain of the system.

6 FEED-FORWARD CONTROL OF THREE-LEVEL NEUTRAL-POINT-CLAMPED CONVERTERS—SIMULATION AND EXPERIMENTAL RESULTS

The goal in this chapter is to continue the analysis of the three-level converter modulator with feed-forward control using numeric simulation tools to gain some further insight. As in the previous chapter, the system is analyzed on two time scales by using the line-cycle average and the switching-period average. The general approach is to develop models, verify the models with the experimental results, and then use the models to verify the system operation outside the region of the experimental results.

The full dynamic simulation confirms the qualitative stability analysis from the previous chapter, and proves that the influence of the feed-forward control the rectifier mode causes instability only in extreme cases with unrealistically large voltage ripple and high power factor correction (PFC mode of operation). Furthermore, the danger of instability is lessened by the fact that the higher the power factor, the smaller the ripple in the NP, therefore, the smaller the chance of instability. In addition, in the inverter mode of operation, the feed-forward control has a slight stabilizing effect, and under no circumstances does the loss of NP control occur.

6.1 Analysis and Experimental Verification of the Line Cycle Average Model of the Feed-Forward Algorithm

The line-cycle average method of analysis leaves the impression that the modulator does nothing other than provide a current gain. This might not be at all obvious when the nonlinear and heavily discontinuous NP current is considered. For that reason, it is perhaps best to verify this underlying assumption of the line-cycle averaging method by measuring the loop gain of the NP voltage controller. The experimental hardware is the SMES hardware with the NP controller modified, as shown in Figure 6.1, in order to allow the loop-gain measurements with the network analyzer. The modulator is implemented using the fast SVM algorithm. The converter operates in the inverter mode with 80V dc-link voltage and with a 45-degree power factor inductive load (R=.72Ω, L=1.8mH).

Figure 6.2 shows the controller loop gain for different modulation indexes (output voltage and output current) of the converter. The loop gain measurement results H(s)=A(s)/B(s) show only the first-order response, with the phase slowly increasing with the increase of frequency, which occurs as a consequence of the delay in the control loop. The first-order response can be observed for other power factor loads as well. This proves that the assumption from the previous chapter, that the modulator together with the load is essentially a nonlinear gain (5-12), is correct and can be used for the closed-loop NP controller design.

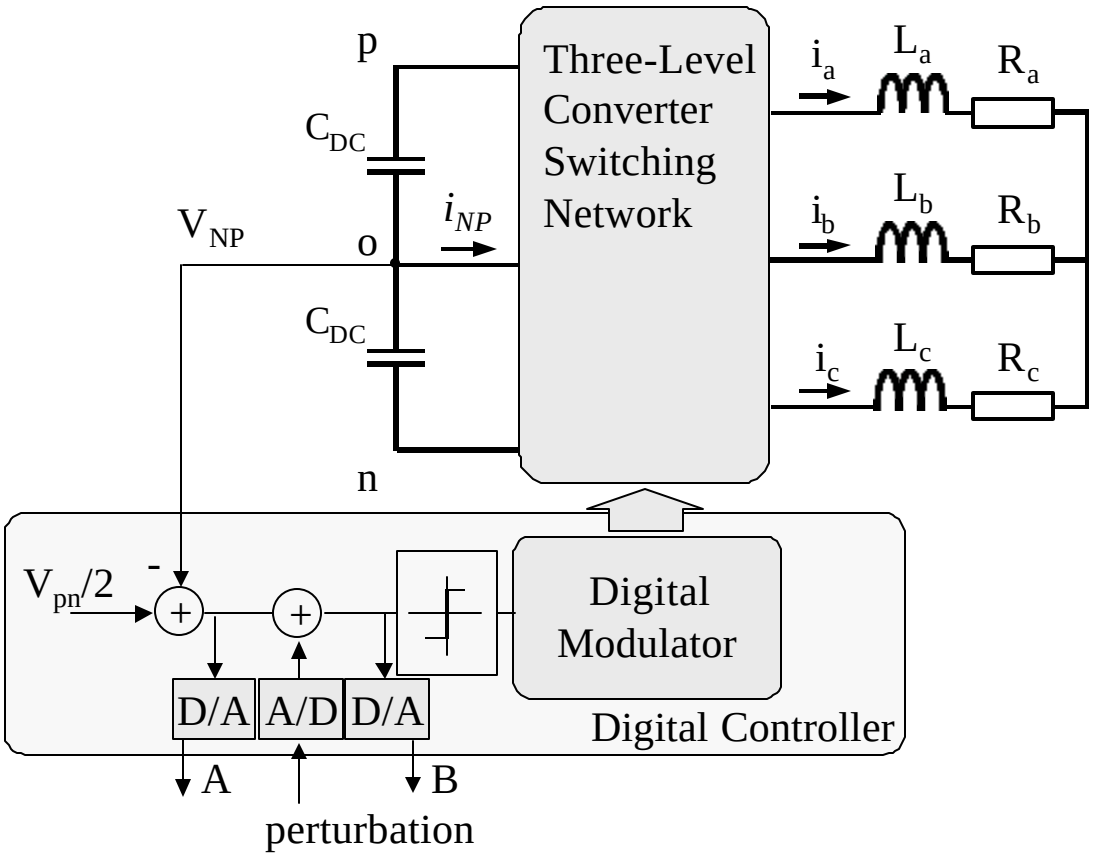

Figure 6.1. Experimental measurement of the loop gain in the NP controller.

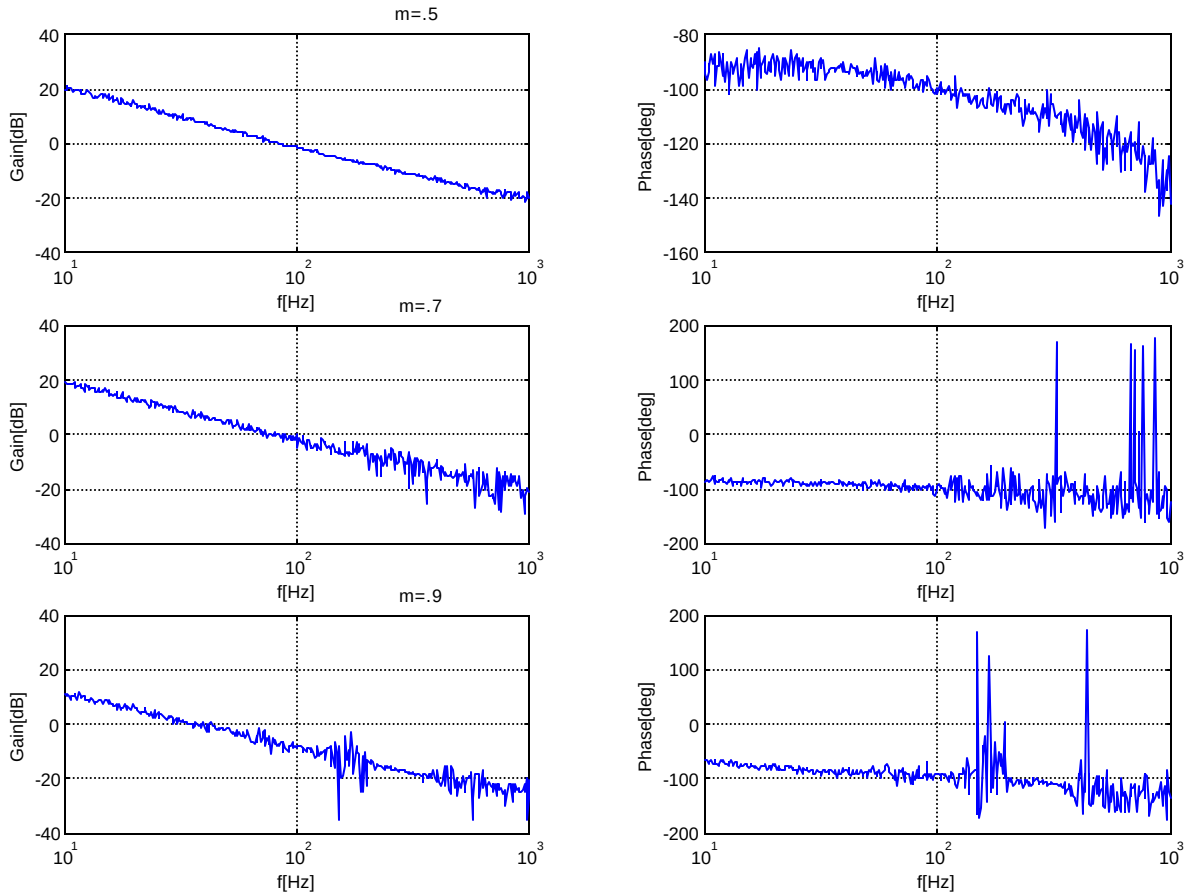

Figure 6.2. Measurement of the NP control loop gain without normalization.

6.1.1 Control Authority Over the NP Current, with and without Feed-Forward Terms

Control authority of the zero-sequence term for the sine triangle modulated converters can best be observed by studying the expressions for line-cycle average currents without (6-1) and with

(6-2) feed-forward correction. Expressions (6-1) and

(6-2) give the average current that flows into the NP under the control of the modulating signal's zero sequence ***d***. Both expressions assume there is either a very small ripple or none at all in the NP. Figure 6.3 shows the line-cycle average of the current flowing into the NP when the dc-link capacitors are balanced. The figure shows the symmety around the zero value of the

zero sequence d. For the small, and large modulation index, A, the current that can be commanded into or out of the NP is rather small, because the difference between the upper and lower duty cycle is small. As the modulation index approaches the point A=.5, the control authority reaches its maximum.

(6-1) $$\overline{i_{NP}} = \frac{-3 \cdot I}{A \cdot \pi} \cdot \cos(f) \left[d \cdot \sqrt{A^2 - d^2} + A^2 \cdot \sin^{-1} \frac{d}{A} \right]$$

The zero sequence's control authority over the NP in the presence of the constant feed-forward terms is as expected not symmetric around zero value of the zero sequence because of the presence of the feed forward terms. The expression for the line cycle average current

(6-2) is plotted for two different feed forward terms in Figure 6.4. Again, the zero sequence exhibits the most control authority over the duty cycle around A=0.5.

(6-2) $$\overline{i_{NP}} = \frac{-3 \cdot I \cdot \cos(f)}{4 \cdot \pi \cdot A \cdot K_n \cdot K_p} \cdot \left[2 \cdot (4 \cdot K_n + 2 \cdot d - 4) \cdot \sqrt{A^2 - d^2} - A^2 \cdot \pi \cdot (K_n - K_p) + \right.$$
$$\left. + 2 \cdot A^2 \cdot (K_p + K_n) \cdot \sin^{-1}\left(\frac{d}{A}\right) \right]$$

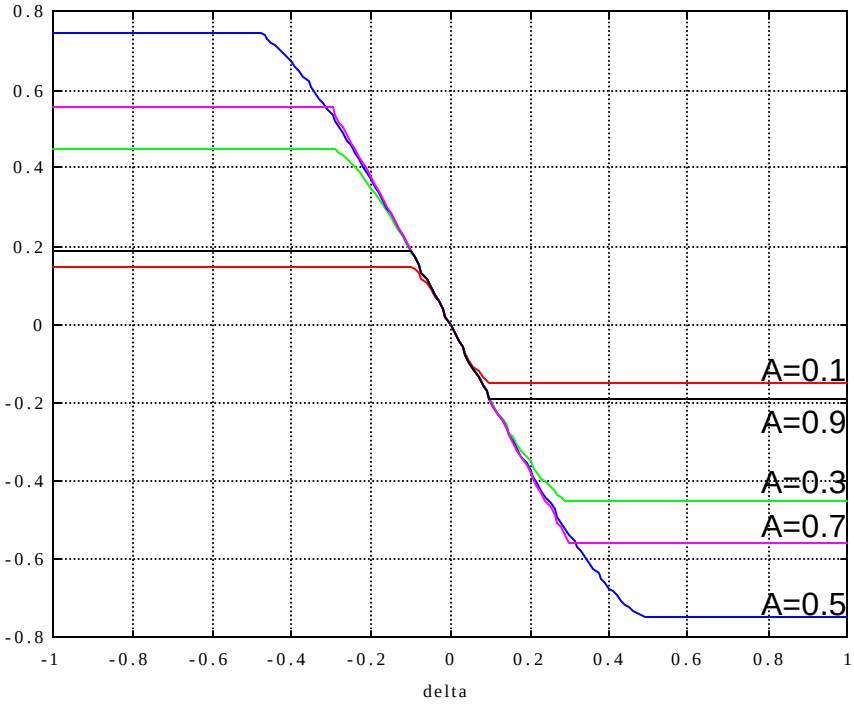

Figure 6.3. The line-cycle average NP current as a function of the zero-sequence component δ.

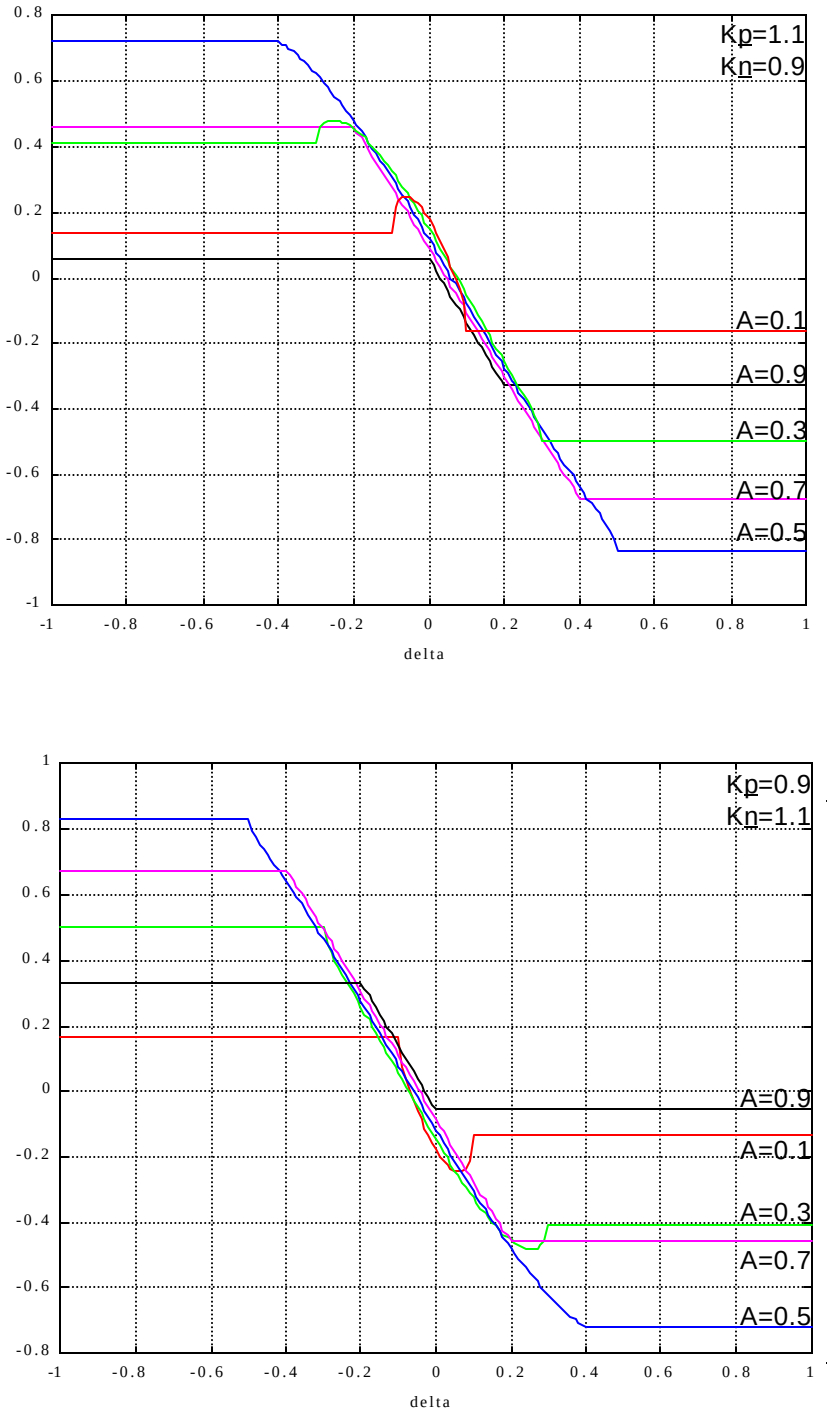

Figure 6.4. The line-cycle average NP current with feed-forward terms included.

6.2 Analysis of the Switching-Cycle Average Model of the Sine Triangle Modulator with the Feed-Forward Algorithm

All the analysis performed so far included one key assumption: that the capacitance of the dc-link capacitors is sufficient to prevent a significant ripple. Thus way, the influence of the possible ripple voltage could be neglected in order to study the limitations of the modulation in the sense of controlling the NP current on the switching-cycle level and on the line-cycle level. The "no ripple" approach was chosen because of the complexity of the modulator and the inherent discontinuities in modulation, which were not only difficult to solve analytically, but were also very hard to explain intuitively. In addition, anything other than a constant zero sequence is just too difficult to include in the analytical expressions for the line-cycle average current.

However, the simplified model has its own limitations, which present themselves mainly in the conservative stability estimate in the case of the analysis of the feed-forward algorithm as well as in the inability to predict the NP ripple's effect on the output line voltage. The full dynamic simulation of the converter and the load will overcome these limitations. Finally, some of the simulation results will be verified experimentally.

6.2.1 Average Model of Three-Level Converter with Sine Triangle Modulator

Figure 6.5 shows the Matlab Simulink average model of the three-phase converter with the R-L load. The only assumption in this model is that the there is an ideal dc-voltage source at the dc link. The model consists of three phase leg average models, a model of load, and an NP controller, which is essentially a comparator that applies maximum positive or maximum negative zero sequence (maximum, so that the modulator is not saturated at any given moment), depending on the sign of the NP voltage error. There are two load models that were used for the simulations: The first model used for the simulations of the inverter mode of operation was a

dynamic model of the balanced three-phase R-L; the second load model used for the rectifier mode of operation was three sinusoidal phase-shifted current sources.

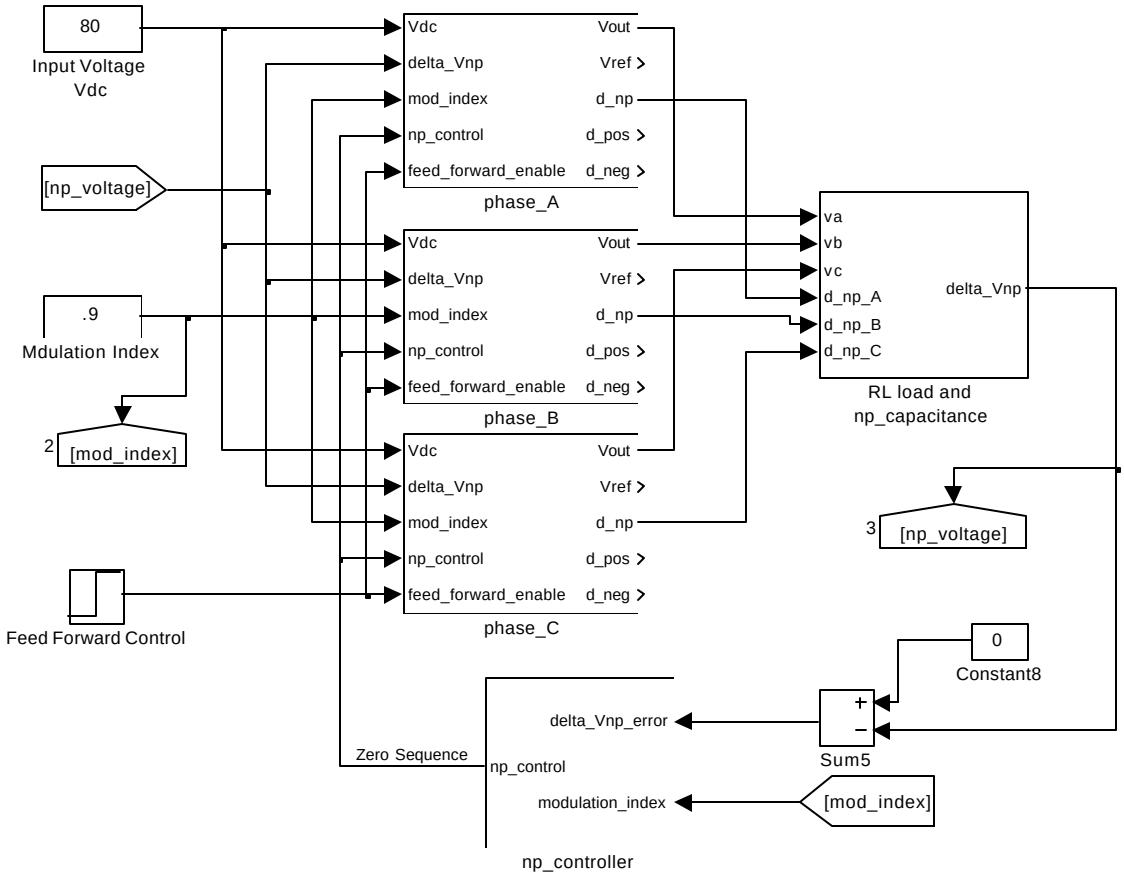

Figure 6.5. Average model of the sine triangle modulator with feed forward.

Figure 6.6 shows the implementation of the average model of the phase leg. Essentially, the modulating sinusoid is scaled with the modulating index, added with the zero sequence, and then the duty cycles and the output voltage are computed from the average equations, as in (5-16) and (5-17).

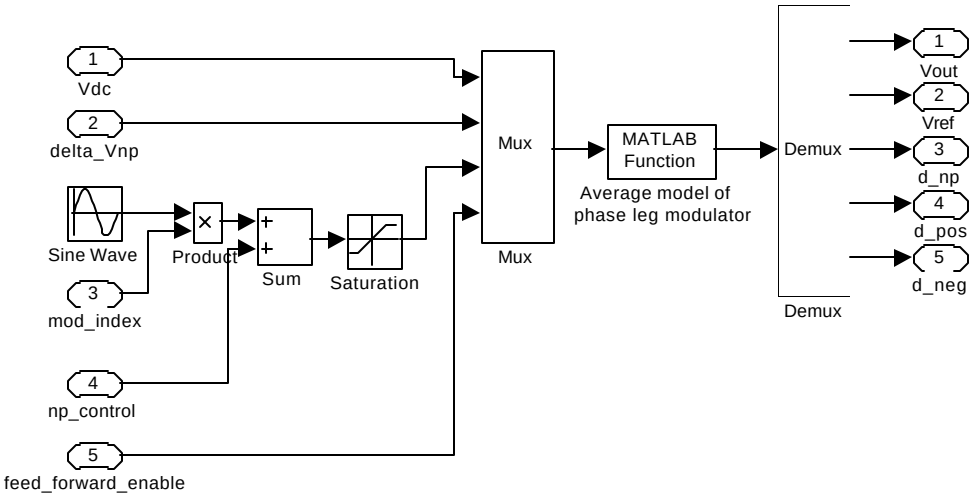

Figure 6.6. Average model of one phase leg sine triangle modulator.

Finally, the bang-bang NP controller is shown in Figure 6.7. This implementation of the controller is probably not optimal; nevertheless, in the case of the average model, the harmonic performance of the converter is not of interest.

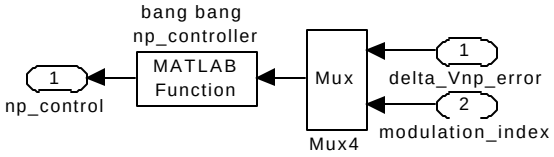

Figure 6.7. Model of NP bang-bang controller.

6.2.2 Performance of Feed-Forward Algorithm, Simulation Results

The qualitative analysis and the expressions for the NP current obtained through the line-cycle averaging indicate that there is a potential to lose control of the NP in the presence of the feed-forward control. This danger exists only in the rectifier mode of operation, in which the converter has the tendency to further charge the capacitor that is already charged to a higher

potential. For this reason the system is simulated in the rectifier mode of operation for different power factors' ac currents.

Figure 6.8 shows the rectifier mode of operation with the 85-degree power factor angle. The amplitude of the phase current is 80A, the dc-link voltage is 80V dc, and the modulation index is unfavorably high at m=0.95. All the parameters closely resemble the system parameters from practical experiments. The first graph is line voltage, the second is the line current, the third the NP voltage and the last is the feed-forward enable command. The effectiveness of the feed-forward algorithm is clear. Not only was the line-voltage waveform dramatically improved and completely cleaned of harmonic components, but the NP ripple size was significantly reduced for this operating point. Furthermore, it is important to notice that the operating conditions are chosen to have an unrealistically large ripple (dc capacitors have a 75% voltage swing) in the NP in order to more clearly demonstrate the effectiveness of the feed-forward algorithm.

As many simulations show, the feed-forward algorithm does not critically affect the stability of the NP. There is a very narrow region with a very high NP ripple, high power factor (mostly active power) and high modulation index (very little zero-sequence control) when the instability may occur. Figure 6.9 shows one boundary for which the feed-forward algorithm causes the loss of NP control. The operating conditions are the same as in previous simulations, except that the power factor angle is 0. The simulation shows that the converter operates with no distortion in the average line voltage, even when the dc link collapses completely.

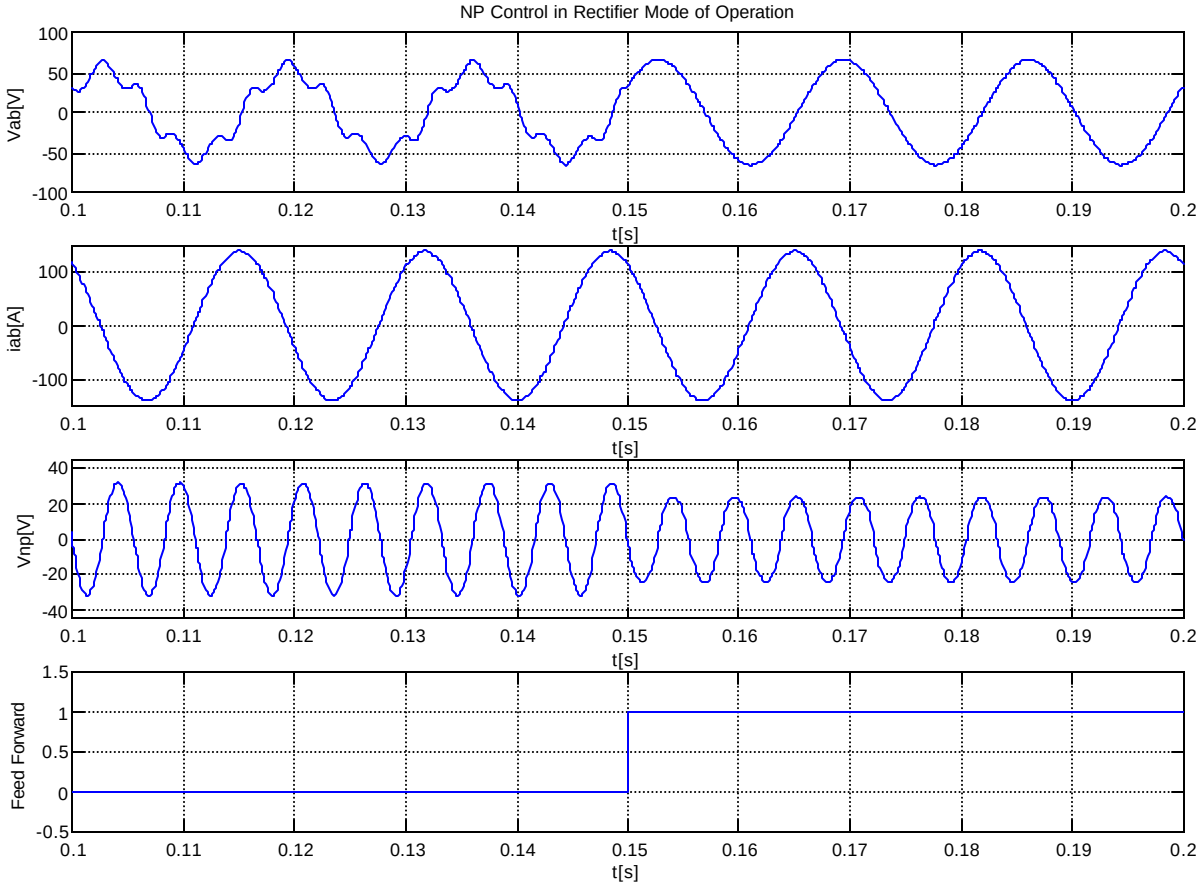

Figure 6.8. Rectifier mode of operation with low power factor.

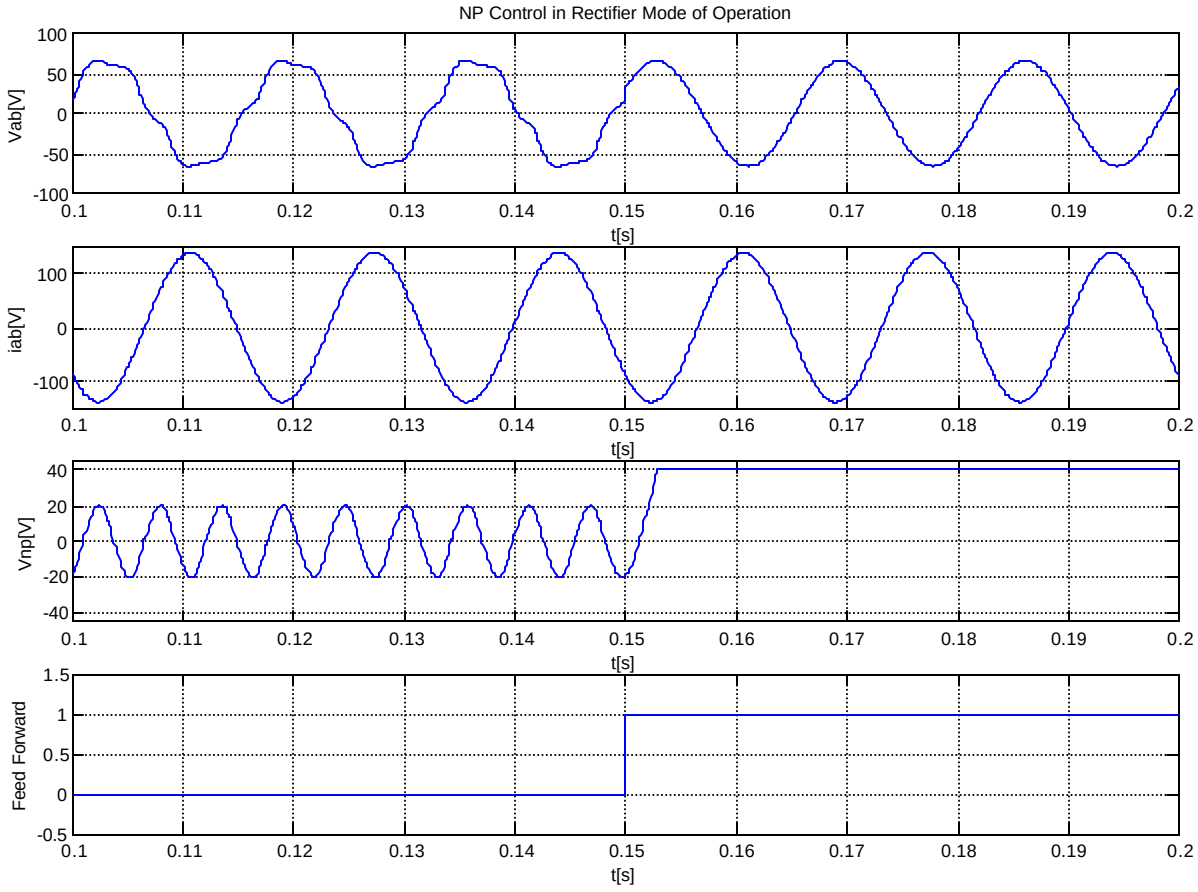

Figure 6.9. Rectifier mode of operation for high power factor.

Finally, the algorithm is simulated in the inverter mode of operation with the dynamic model of R-L load, where R= 0.06Ω, L=1.8 mH (85-degree power factor angle), and with a high modulation index, m=0.95. The simulation results show an improvement in the quality of the line voltage, while the NP voltage remains unaltered.

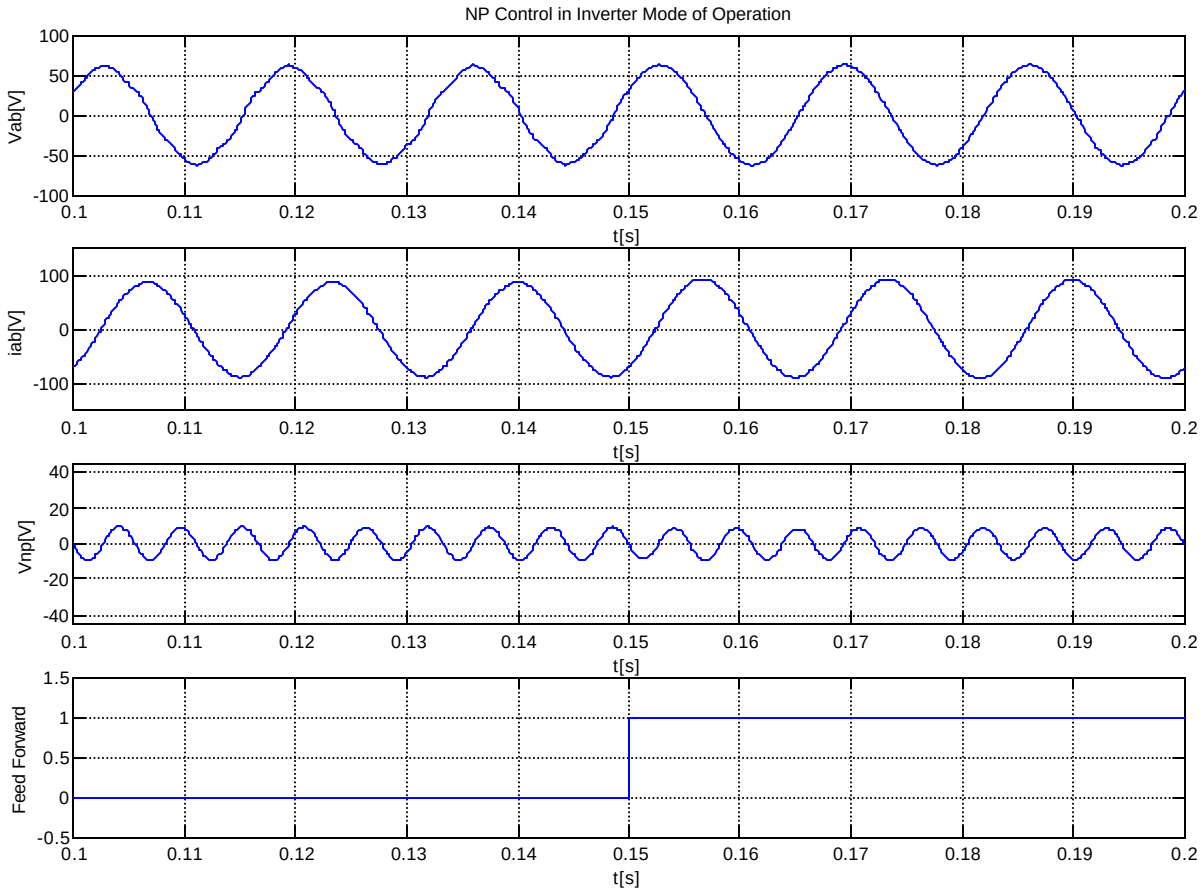

Figure 6.10. The inverter mode of operation with low power factor load.

6.3 Average Model of Fast Space Vector Modulator, Experimental Verification of the Model

Because the simulation results of the average model of three-level converter with the sine triangle modulator did not exactly match the experimental results, the average model of the fast space vector modulator is developed next. It is important to mention that the discrepancy was only to be expected, because the modulator of the experimental system was implemented using SVM with the NP control based on the selection of redundant small vectors and not on control of the zero sequence. This leads to the discrepancy in the zero sequence of the space vector modulated experimental hardware and the sine triangle modulated simulation results.

6.3.1 Average Model of the Three-Level Converter with Fast Space Vector Modulation Algorithm

Figure 6.11 shows the Matlab Simulink model of the average model of the three-phase converter with the R-L load. The difference from the previous model is the modulating technique. In this case, the fast SVM algorithm is implemented. As in the previous model, the main assumption is the constant dc-link voltage. The model implementation is relatively straightforward: there are two essential blocks, the modulator and the load. There is still a coordinate transformation block, which converts the rotating reference vector from the orthogonal to the non-orthogonal (g, h) coordinate system, and the integrator that uses the NP current to compute the NP voltage ripple.

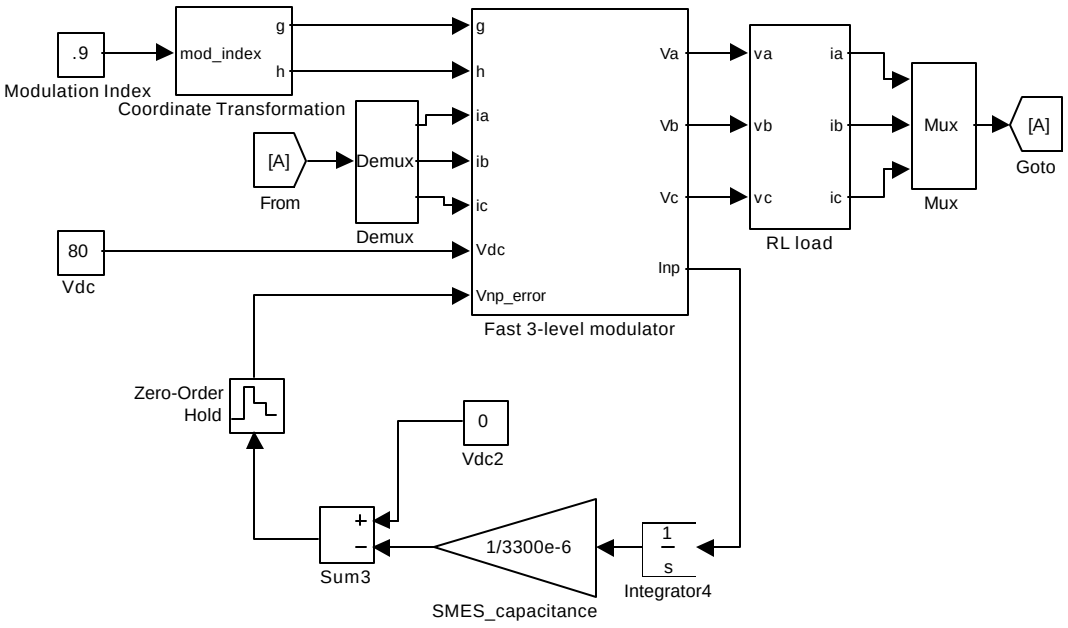

Figure 6.11. Average model of the fast SVM algorithm.

Finally, Figure 6.12 shows some details of the implementation of the fast space vector modulator. There are three functions implemented. The first function finds the nearest three vectors and their corresponding duty cycles, then a switching-state selection function converts

the vectors given in (g, h) coordinates into the switching combination and selects between the redundant vectors in order to balance the NP. Finally, the third and last function adds together the products of duty cycles and voltages to find the average phase voltage and adds the NP currents from the three vectors in order to find the resulting average NP current.

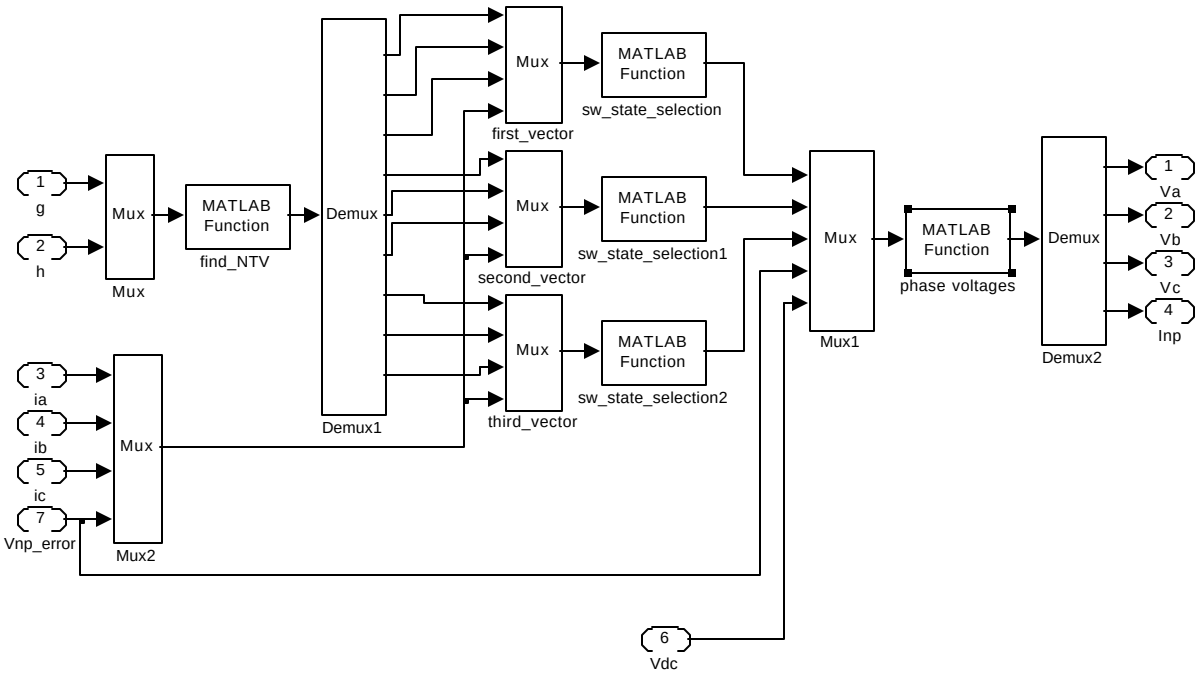

Figure 6.12. Fast three-level space vector modulator.

6.3.2 The Fast Space Vector Modulation Algorithm, Experimental Results

Figure 6.13 shows the NP voltage for several different modulation indexes for the 80V dc-link voltage and for the R-L load, where R=0.06 Ω and L=1.8 mH (making a power factor angle of 85 degrees). The figures in the left column are the measurement results; the figures in the right column are the simulation results with the average model of the space vector modulator. The two columns seem to be in excellent agreement.

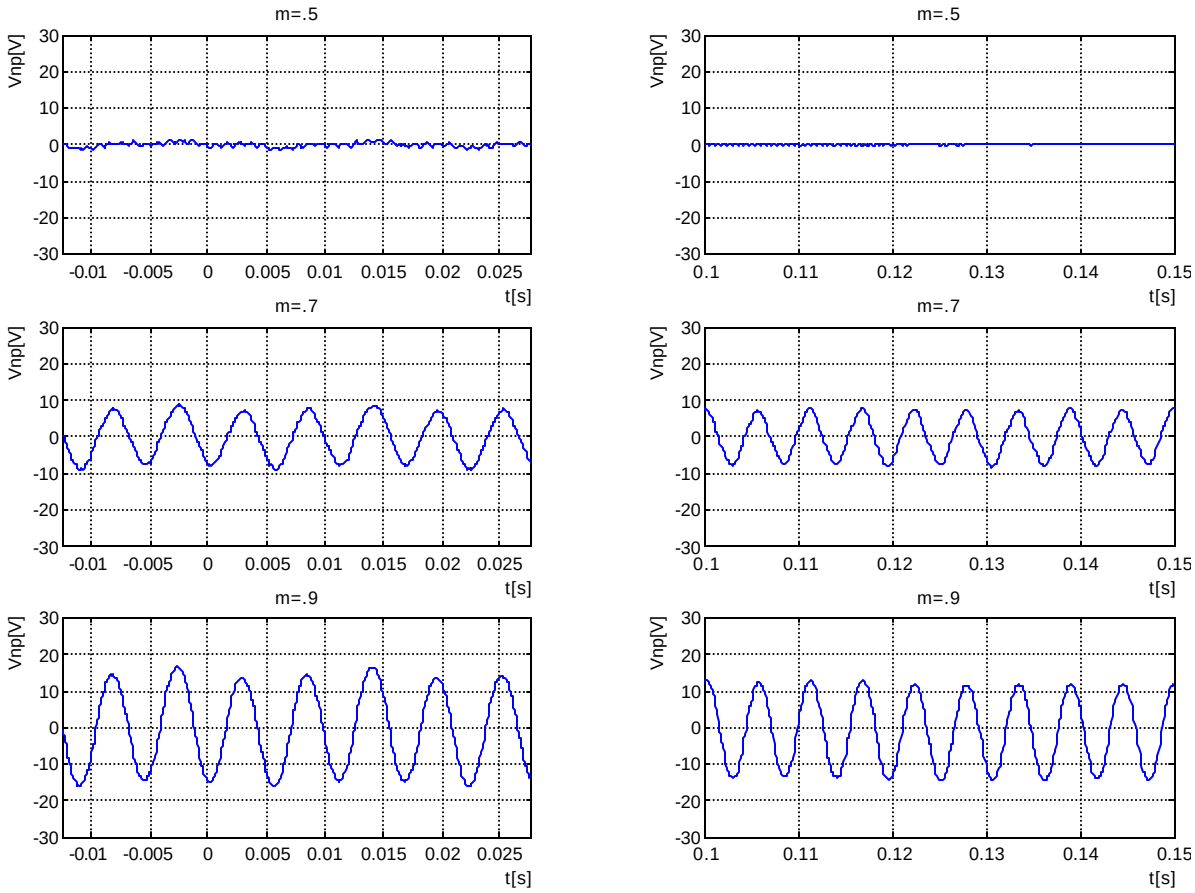

Figure 6.13. Measured and simulated NP ripple of a three-level converter.

Figure 6.14 shows the measured and simulated line-to-line voltage for the same operating point as in the previous figure. It is interesting to observe the strong third-harmonic component in the line-to-line voltage. The strong third harmonic in the line-to-line voltage gets canceled for the balanced load, resulting in nearly perfect phase currents. Figure 6.15 shows simulated line-to-line currents for the same operating condition as in the previous two figures. The measurement results are not shown because they were also nearly perfect sinusoids. This fact points out an interesting new aspect of the design optimization of three-level converters; It might be possible to design three-level converters for certain with requirement for a very low dc-link capacitance applications and very simple controller, which might even operate without the feed-forward algorithm and with only a basic NP-balancing scheme.

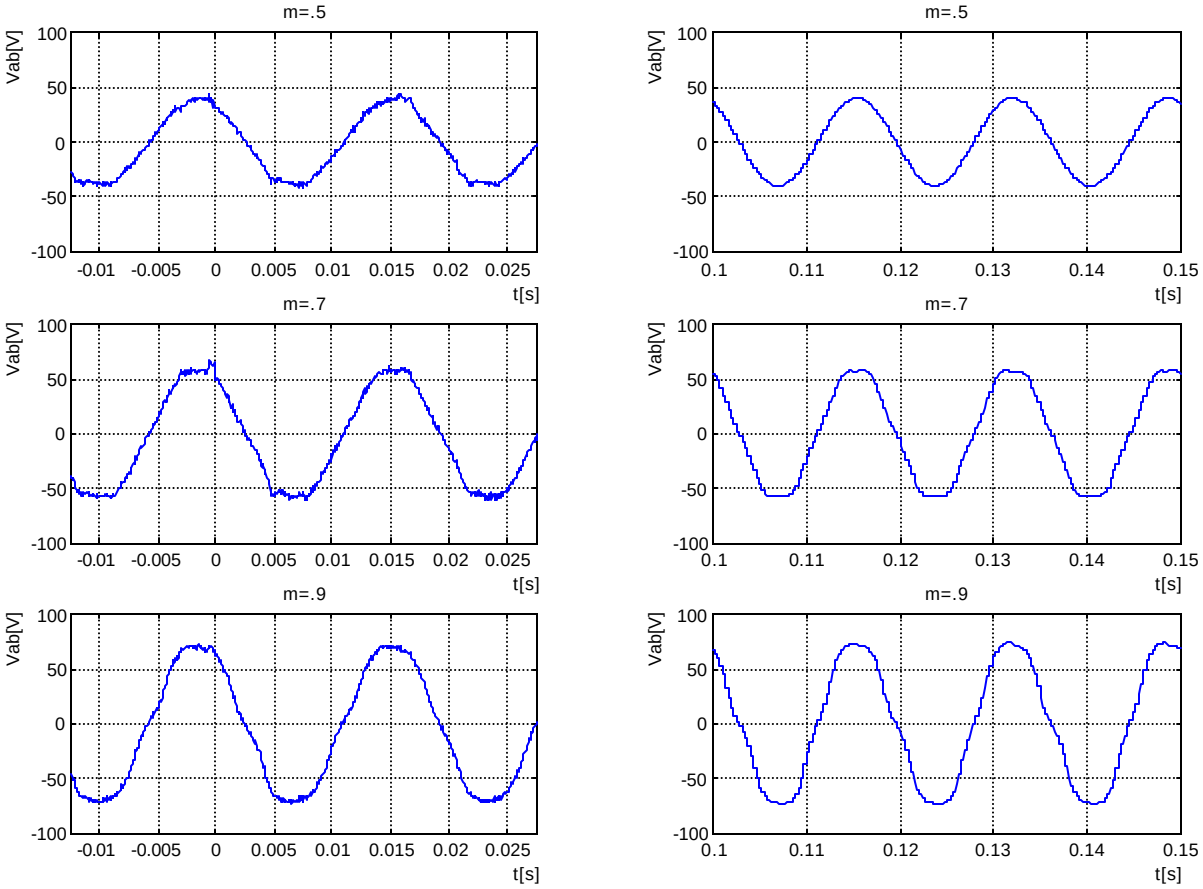

Figure 6.14. Measured and simulated line voltage in the presence of NP ripple.

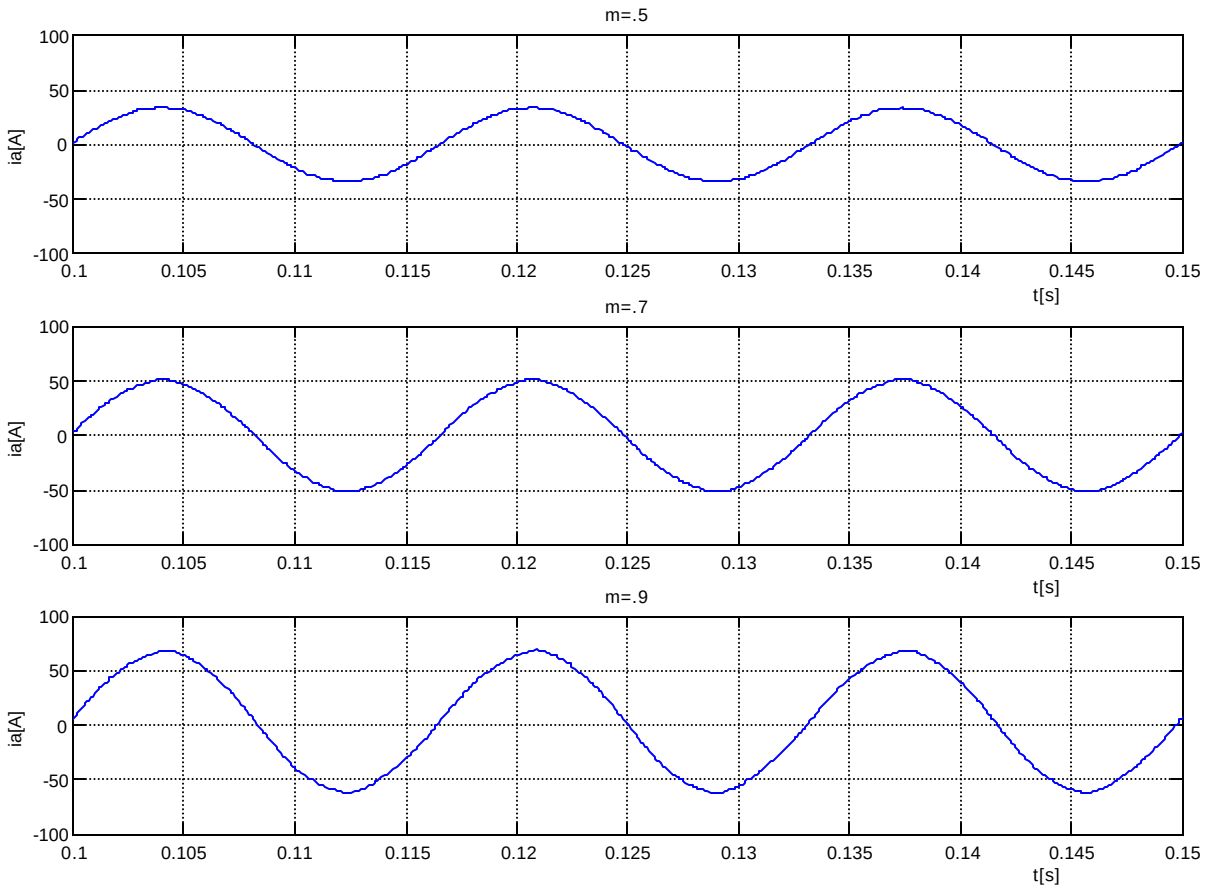

Figure 6.15. Simulated line-to-line currents for balanced and symmetric load.

6.4 Conclusions

This chapter verifies the essential assumption of the line-cycle averaging method through experiment. The experiment proves that for the purpose of NP control the inverter together with the load can be considered a variable-gain current source with no dynamics. With the line-cycle averaging technique experimentally proven, the next step is the stability study based on the expressions for NP current obtained through line-cycle averaging. The expressions for the NP current in the presence of the feed-forward control show that the stability is compromised only in the rectifier mode with a certain amount of voltage error in the NP and for operation with either very low or very high modulation indexes.

Because the expression for line-current averaging assumes a constant dc-link imbalance and a constant zero sequence, it seemed likely that the danger of NP control stability problems was exaggerated. That is the reason why a switching-cycle average model of the converter was implemented and used to study the stability in the presence of a significant voltage ripple in the NP. The full dynamic simulations show not only the excellent performance of the feed-forward algorithm, but also that it is unlikely to have the stability problems in any but the most extreme conditions. The NP control stability problems were observed only with the NP ripple higher than 50% of the nominal split dc-link capacitor voltage, while at the same time the converter operated at high modulation index and in PFC (or near PFC operation).

Finally, although it was expected that the dynamic model of the converter with sine triangle modulator was not going to exactly match the experimental waveforms of the converter with the fast SVM algorithm, a dynamic model of the converter with the space vector modulator was developed as well. The results of the simulations using the space vector modulator almost exactly match the experimental results, and in that way demonstrate the validity of the switching cycle averaging method.

7 CONCLUSIONS

This work discusses space vector modulation and the control of multilevel power electronics converters, and is really the result of generalizations and insights gained from the theoretical study of a practical problem, such as the design of a power conditioning system for superconductive magnetic energy storage. The engineering challenge in designing the power conditioning system (or more precisely, in the design of the digital controller for the power conditioning system) was to enable the power conditioning hardware to control the bi-directional power flow between the magnet and the utility line. In fact, the challenge was to control the power conditioning system in order to provides stable, controllable and high-quality power on both the magnet and utility sides.

The first engineering part of this research shows that a power conditioner based on the three-level converter topology is feasible, and that its control design can provide a stable, high-bandwidth, bi-directional control of the power flow. In addition, the control design approach in which the NP controller was designed separately from the main power stage was theoretically and practically justified.

During the modeling and hardware development phase of the digital controller, two main problems presented themselves as worthwhile research topics. One problem is the excessive complexity of the implementation of the SVM algorithm, particularly for converters with a higher number of levels. The other one is more specific and deals with the issue of controlling

the NP of the three-level converters; This is a very important aspects of the three-level converter design.

Accordingly, Chapter 3 introduces the new SVM algorithm that is computationally very efficient and applicable to converters with any number of levels. The computational efficiency of the algorithm comes from its simplicity, and it is important to mention that not only can the same algorithm used for converters with any number of levels, but the number of steps in the algorithm remains the same regardless of the number of levels in the converter. These features make the new algorithm not only a good design and implementation choice, but also a very good tool for teaching the mathematical basis of multilevel SVM.

The research on NP control and the issues of the imbalance in the NP control are approached from several different angles. The initial approach taken was to develop the model of the space vector modulator for the purpose of investigating the NP current ripple. The developed model is general in the sense that it can describe any SVM, and its effects on the NP. Using the developed model (under the assumption of the infinite dc-link capacitance), the model presents the properties of the NP control in an intuitive way. In addition, a region in which the dc link can be balanced on the switching-cycle level was identified, and a quantitative study of the NP balancing offered as an essential tool in designing the size of the dc-link capacitors. Finally, some of these results were verified experimentally.

The study of the properties of the NP and the ripple in the NP led to the following idea: If there is a way to compensate for the effect of the NP ripple in the control, than it might be possible to allow designers the freedom for a new kind of design tradeoff between the size of the dc-link capacitors and the increased voltage capacity of the switching devices.

The result of this study is a feed-forward algorithm, which can actively compensate for the ripple in the NP so that it does not propagate and affect the output of the converter. The algorithm is proposed for both the carrier-based modulation and for SVM. Subsequent analysis was performed with multiple tools, including line-cycle average, switching-cycle average, and finally, with the dynamic simulation. The study shows that the feed-forward algorithm (although

it affects the NP control) does not require redesign of the NP controllers; it compensates for the effects of the imbalance in the NP, and in some cases reduces the NP ripple itself. Unfortunately, in the rectifier mode of operation and under the most extreme conditions (high modulation index, higher than 50% ripple and high power factor current), there exists the possibility that the NP control algorithm can cause the loss of NP control. In that case the amount of feed-forward action can be adjusted in order to avoid stability problems.

Finally, there are several interesting topics for further research:

- The digital controller for the SMES power conditioning system was built as a centralized controller, while using the power electronics building block (PEBB) approach. In the future, it would be interesting to implement a distributed controller approach into the design of the digital controller like in [F17, F18], thus standardizing the signal distribution network throughout the converter.

- The research in the application of the new fast SVM algorithm still has potentially very interesting research opportunities. Perhaps the most immediate research topic can be found in the attempt to generalize the algorithm to converters with more than three phases by exploiting the hidden symmetries in the higher-dimensional spaces of the more these converters. Another interesting opportunity can be found in the challenge to generalize and organize the conversion of the switching vectors back into the switching states.

- With respect to modeling the space vector modulator for the purpose of NP balancing, the model (although general) does not allow the ripple in the NP. It might be interesting to generalize the modeling approach to include the NP ripple if the dc-link capacitors can not be assumed to be infinitely large.

Finally, with respect to the feed-forward algorithm, it might be interesting to determine how much can really be saved by trading off the increased voltage rating of the switches for the decreased capacitance of the dc-link capacitors. In addition, for the more confident application

of the algorithm, it is important to make a more detailed study of the conditions that cause instability in the rectifier mode of operation.

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