HIGH PERFORMANCE POWER CONVERTER SYSTEMS FOR NONLINEAR AND UNBALANCED LOAD/SOURCE

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(ABSTRACT)

This dissertation covers three levels of issues and solutions dealing with unbalanced and/or nonlinear situations in power electronic systems, namely power converter level, power converter system level, and large-scale power electronics system level.

At power converter level, after review of traditional PWM methods, especially two-dimensional space vector modulation schemes, three-dimensional space vector modulation schemes are proposed for four-legged voltage source converters, including inverters and rectifiers. The four-legged power converters with three-dimensional space vector modulation schemes have a better DC link voltage utilization and result in a low distortion. It is an effective solution to provide the neutral point for a three-phase four-wire system and to handle the neutral current due to unbalanced load or source and nonlinear loads. Comprehensive design guidelines for a four-legged inverter are presented. The four-legged rectifier is also presented which allows not only fault tolerant operation, but also provides the flexibility of equal resistance, equal current, or equal power operation under unbalanced source.

Average large-signal models of four-legged power converters in both the a-b-c and d-q-o coordinates are derived. Small signal models are obtained in the d-q-o rotating coordinates. Voltage control loops are designed in the d-q-o coordinates for a high power utility power supply. Performance is studied under various load conditions.

At the power converter system level, the load conditioner concept is proposed for high power applications. A power converter system structure is proposed which consists of a high-power low-switching frequency main inverter and a low-power high-switching frequency load conditioner. The load conditioner performs multiple functions, such as active filtering, active damping, and active decoupling with a high current control bandwidth. This hybrid approach allows the overall system to achieve high performance with high power and highly nonlinear loads.

At the large-scale power electronics system level, the nonlinear loading effect of load converters is analyzed for a DC distribution system. Two solutions to the nonlinear loading effect are presented. One is to confine the nonlinear load effect with the sub-converter system, the other is to use a DC bus conditioner. The DC bus conditioner is the extension of the load conditioner concept.

To my father and mother,
and Ningling

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Chapter 1 Introduction

1.1Motivations and Objectives

Power electronics has continuously penetrated into more and more applications in the past decades, playing as a key role in energy conversion and consumption. With the deregulation of power industry, it is expected that power electronics will be more active in energy generation and distribution as well. The momentum behind power electronics technologies stems from the high efficiency and compactness of power converters. Therefore, it is deemed the enabling technology.

Nonlinearity is a prevailing phenomenon in a system using power converters. The nonlinearity comes from both the power converters, due to their on/off switching actions, and the load or source of the power converters. Some examples are described below.

In the energy conversion category, power converters have been used extensively for two subcategories — (1) a transforming hub of different electric energy forms, or voltage or current levels, e.g. step-up or step-down voltages or currents; and (2) an interface between different energy forms, for example, a power converter driving a piezo-electric actuator or motor converts electric energy into mechanical energy. The energy conversion using power converters can be divided into four classes. The DC to DC (direct current) conversion, DC to AC (alternative current) conversion, AC to DC conversion, and AC to AC conversion. For a DC/DC converter used for a welding machine, the load profile can be highly nonlinear depending on the characteristics of the generated arc. For a DC/AC converter used for lighting, the fluorescent lamp has nonlinear characteristics. For an AC/DC converter used for silver box in a computer power supply, it is a simple diode rectifier, yet a strong nonlinear load; for an AC/AC converter used for a drive system, the motor is a nonlinear load.

Since the analysis and control method for nonlinear systems are not as well established as that of linear systems, the nonlinearity of the load to the power converters calls for extra attention. Not only the nonlinearity of the load to the power converters is

of concern, but also the power converter itself. Compared with a traditional solution for energy conversion using a linear circuit, a power electronics circuit has a much higher efficiency with a more compact design. However, since it brings more nonlinearity into the system.

A vast body of all the loads consuming electric energy manifests some degree of nonlinearity, except for limited applications such as heaters. All those nonlinear loads draw harmonic currents. Those harmonics cause a lot of problems, such as distorted voltage, voltage flicking, overheated transformer, high torque ripple in the generator, severe EMI noise to communication systems and computer systems. Those problems become more and more severe as more and more nonlinear loads put in use in the field. In order to address the problems caused by nonlinear loads, some standards have been established to limit harmonics produced by nonlinear loads. The most commonly cited standards are IEEE std 519 [A9], IEC 1000-3-2 [A10], and IEC 1000-3-4 [A11].

The IEEE std 519 sets customer/system voltage and current limits at the point of common coupling (PCC). It is mainly for high voltage and high power applications such as arc furnace, paper mills, steel mills, and large drive systems. It is designed to limit harmonic currents flowing back to the power system and affecting other users. For utilities, IEEE std 519 limits the voltage distortion, as shown in Table 1-1. For example, for 69 kV and below, the maximum individual harmonic voltage is limited to 3% and the total harmonic voltage distortion (THD) is limited to 5%. This covers 208/380/480 V utility systems. It also limits the interference with communication circuits. For individual consumers, it limits commutation notch of the distorted current waveform and individual harmonic current percentage. The current distortion limits are developed to meet the voltage distortion limit mentioned above. Therefore, current distortion limits are different for different systems. There are three tables in the IEEE std 519 that set the current distortion limits. For 120 V through 69,000 V, current distortion limits are set for general distribution systems; for 69,001 V through 161,000 V, current distortion limits are set for general subtransmission systems; for larger than 161 kV, current distortion limits are set for general transmission systems including dispersed generation and cogeneration. The current distortion limits for general distribution systems (120 V ~ 69 kV), as shown in

Table 1-2, is of interest of power electronics engineers, where I_{sc}/I_L is the short circuit ratio (SCR), and I_{sc} is the maximum short-circuit current at PCC; I_L is the maximum demand load current (fundamental frequency component) at PCC. It can be seen that the harmonic current limits are more stringent for a distribution system with less short circuit capability. All the power generation equipment is limited to the most stringent current distortion limits (corresponding to SCR < 20) regardless of its actual SCR.

IEC 1000-3-4 sets harmonic current limits for electrical and electronic equipment with a per phase current level higher than 16 A. It applies to equipment for low-voltage AC distribution systems, including 240 V single-phase two or three-wire systems, up to 415 V three-phase three or four-wire systems. IEC 1000-3-4 sets up three consecutive stages of assessment of harmonic current emission, where stage 1 is the most stringent for connection without restrictions, as shown in Table 1-3; stage 2 is for connection under specific conditions having regard to supply characteristics. Stage 2 differentiates between single-phase equipment and unbalanced three-phase equipment, as shown in Table 1-4, and balanced three-phase equipment, as shown in Table 1-5; stage 3 is for connections subject to special conditions and is required for equipment with per phase current higher than 75 A, as shown in Table 1-6.

IEC 1000-3-2 sets harmonic current limits for equipment with a per phase current level up to 16 A. All the equipment is classified into A, B, C and D classes. Class A refers to balanced three-phase equipment and all other equipment, except that stated in one of the other classes; Class B refers to portable tools; Class C refers to lighting equipment, including dimming devices; Class D refers to equipment having an input current with a “special wave shape” and an active input power less than or equal to 600 W. Harmonic current limits for Class A, B, and D equipment are given by absolute harmonic current RMS value, while limits for Class C are given by a percentage of harmonic currents. Harmonic current limits for Classes A and C are summarized in Table 1-7 and Table 1-8, respectively.

All those standards indicate two things. First, power converters used as energy consumers have to comply with the standards by adopting PFC techniques; second,

power converters used in power generation applications have to be able to deal with those nonlinear loads. This dissertation mainly deals with the power generation applications.

Although most of the three-phase applications, such as motor drives, are balanced three-phase systems, unbalanced loads are prevalent for UPS, standalone power generation applications, and for fault-mode operation of a balanced three-phase system as well. Unbalanced three-phase source could also exist due to heavily unbalanced loads. Unbalanced load or source may cause an overheated neutral conductor due to excessive neutral current, large even-order low frequency reactive power, and distorted source. Especially for UPS and standalone power generation applications, there is no limitation to the percentage of unbalance. Unbalanced load condition for each phase can be anything from full load to no load, depending on particular applications and the user's demand.

This dissertation will address the following issues of unbalanced load/source and nonlinear load in power electronics system with special attention to utility power generation applications:

- Power converter topologies for unbalanced load source and nonlinear load
- Pulse width modulation techniques for power converter for unbalanced load
- Modeling and control of power converter for unbalanced and nonlinear load
- Power converter system to handle unbalanced and nonlinear load
- Nonlinearity in large-scale power electronics system

Table 1-1 Voltage Distortion Limits

(IEEE std 519, Recommend Practices for Utilities)

Bus Voltage at PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
69 kV and below	**3.0**	**5.0**
69.001 kV through 161 kV	1.5	2.5
161.001 kV and above	1.0	1.5

Table 1-2 Current Distortion Limits for General Distribution Systems (120 V through 69,000 V)

(IEEE std 519, Recommended Practices for Individual Consumers)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
SCR = I_{sc}/I_L	<11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	35 ≤ h	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above						

Table 1-3 Stage 1 (normative) (IEC 1000-3-4)

Harmonic number n	Admissible harmonic current I_n/I_1	Harmonic number n	Admissible harmonic current I_n/I_1
3	21.6	19	1.1
5	10.7	21	≤ 0.6
7	7.2	23	0.9
9	3.8	25	0.8
11	3.1	27	≤ 0.6
13	2.0	29	0.7
15	0.7	31	0.7
17	1.2	≥ 33	≤ 0.6
Even harmonics: ≤ 8/n or ≤ 0.6			

Table 1-4 Stage 2 (normative) (IEC 1000-3-4)

(Single Phase, Interphase and Unbalanced Three-phase Equipment)

Minimal R_{scc}	Upper limits for harmonic distortion factors		Limits for individual harmonics in % of I_1					
	THD	PWHD	I_3	I_5	I_7	I_9	I_{11}	I_{13}
66	26	26	23	11	9	5	4	3
120	29	29	25	12	10	7	6	5
175	33	33	29	16	11	8	7	6
250	39	39	34	18	12	10	8	7
350	46	46	40	24	15	12	9	8
450	51	51	40	30	20	14	12	10
> 600	57	57	40	30	20	14	12	10

Table 1-5 Stage 2 (normative) (IEC 1000-3-4)

(Balanced Three-phase Equipment)

Minimal R_{scc}	Upper limits for harmonic distortion factors		Limits for individual harmonics in % of I_1			
	THD	PWHD	I_5	I_7	I_{11}	I_{13}
66	17	22	12	10	9	6
120	18	29	15	12	12	8
175	25	33	20	14	12	8
250	35	39	30	18	13	8
350	48	46	40	25	15	10
450	58	51	50	35	20	15
> 600	70	57	60	40	25	18

Table 1-6 Stage 3 (IEEE 1000-3-4)

(For Equipment Exceeding 75 A Input Current Per Phase)

Harmonic number n	Admissible harmonic current I_n/I_1	Harmonic number n	Admissible harmonic current I_n/I_1
3	19	19	1.1
5	9.5	21	≤ 0.6
7	6.5	23	0.9
9	3.8	25	0.8
11	3.1	27	≤ 0.6
13	2.0	29	0.7
15	0.7	31	0.7
17	1.2	≥ 33	≤ 0.6
Even harmonics: ≤ 4/n or ≤ 0.6			

Table 1-7 Limits for Class A Equipment (IEC 1000-3-2)

Harmonic order n	Maximum permissible harmonic current A
Odd harmonic	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$	$0.15\frac{15}{n}$
Even harmonic	
2	1.08
4	0.43
6	0.30
$8 \le n \le 40$	$0.23\frac{8}{n}$

Table 1-8 Limits for Class C Equipment (IEC 1000-3-2)

Harmonic order n	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency %
2	2
3	$30 \cdot \lambda^*$
5	10
7	7
9	5
$11 \le n \le 39$ (odd harmonic only)	3
$^*\lambda$ is the circuit power factor	

1.2 Review of Previous Research

Most of the research work in the three-phase power converter area was for balanced three-phase systems, such as motor drive applications, where three-legged power converters are used. When the neutral connection is needed, typically split DC link capacitors are used. The first four-legged current source thyristor inverter was presented in [E2] in 1979, where the fourth leg was used for commutation of thyristors. A four-legged power inverter was also proposed in [B19] to eliminate the common mode noise. The first voltage source four-legged inverter used for an aircraft power generation application was presented in [E1] in 1993 to provide the neutral connection and to handle the neutral current. Since it is a resonant DC link inverter (RDCL inverter), it is controlled with a pulse density modulation scheme. The same topology was proposed in [G2] in 1992 for active filter applications to deal with a zero-sequence component in a power system. The current source four-legged inverter was also proposed for active filter applications in [G3] in the same year to handle a zero-sequence component. Another

variation of four-legged inverter was proposed in [G23], where the neutral point is still provided by two split capacitors, and the fourth leg is really an active filter independent from the three phase legs. The fourth leg is controlled to nullify the zero-sequence current due to unbalanced load or nonlinear load so that the neutral current does not flow through the DC link capacitors. This approach allows a smaller DC link capacitance to be used for the same voltage ripple, however, it still suffers from insufficient utilization of the DC link voltage. In all the previous research, there are no space vector modulation schemes proposed for four-legged power converters, nor are the modeling and control aspects of four-legged power converters discussed.

Pulse width modulation (PWM) techniques have been widely used in the field since 1960s. With intensive research activities over the last decades, many PWM schemes have been proposed for single-phase and three-phase applications, including sinusoidal PWM, harmonic elimination or optimal PWM [B24-25], hysteresis and bang-bang type modulation [B28-32], random modulation [B33-35], and space vector modulation [B2-B17]. Space vector modulation was first proposed in [B2] in 1982 and became more and more popular due to its merits of high utilization of the DC link voltage, possible optimized output distortion and switching losses, and compatibility with a digital controller. It has been widely used for high performance three-phase drive systems [B3-7] and PFC rectifiers [B8] with success. Several research focuses for space vector modulation can be identified: (1) optimized space vector modulation schemes in terms of harmonic distortion [B13-14] and switching losses [B10-12]; (2) digital implementation of space vector modulation schemes [B4, B14, B16]; (3) overmodulation operation [B9]; and (4) adaptive sequencing schemes for varying modulation index and load power factor [B15, B17]. All the existing space vector modulation schemes are implemented in a two-dimensional space, and are therefore unable to deal with the zero-sequence component caused by unbalanced or nonlinear loads.

Unbalanced source and load have been analyzed extensively in power systems. The symmetrical component representation was proposed by C. L. Fortescue in 1918, and became a textbook method when analyzing unbalance in power systems. By decomposing an arbitrarily unbalanced three-phase variable into three sets of balanced

three-phase variables, namely, positive-sequence, negative-sequence and zero-sequence, not only is the analysis greatly simplified, but also more physical meaning can be obtained from the unbalanced conditions. In power systems, there are several passive means to correct the negative-sequence and zero-sequence components caused by unbalanced load, such as zero-sequence trap [A4], zigzag transformer [A5], and passive balancing network [A6]. In a power electronics system, there are three ways to correct the negative-sequence component caused by a unbalanced load: (1) large passive filter to reduce the 2ω ripple; (2) high bandwidth feedback control so that the disturbance caused by the 2ω ripple can be suppressed; (3) feedforward control to counterbalance the disturbance of the 2ω ripple; or combination of (2) and (3). Using three-legged power converters to deal with unbalanced source has been addressed in [F1-F3]. By engaging a feedforward control, the negative-sequence component caused by an unbalanced source can be canceled out so that the input power becomes a constant and the DC link voltage is free of low frequency even harmonic ripples. The same concept was used for active power filter application in [G1]. However, a three-legged power converter is incapable of dealing with zero-sequence unbalance. To solve the limitation, normally split DC link capacitors are used. The zero-sequence current path is provided by tying the neutral point to the middle point of the two DC link capacitors. [G1] presented a scheme using split DC link capacitors to handle the zero-sequence for active power filter application. The drawback of this scheme is that excessively large DC link capacitors are needed, therefore cost is high especially for high voltage applications. To handle the zero-sequence component, the four-legged inverter proposed in [E1] can substantially reduce the DC link capacitance. Since it is a soft-switching inverter, the correction of unbalance is achieved by a fast feedback control loop with a high switching frequency.

Modeling of three-phase three-legged power converters was presented in [H2] by representing the switching networks with controlled voltage and current sources. The “in-place” circuit averaging method was adopted to derive the average circuit model directly from the switching circuit model. Large-signal and small-signal models are derived in d-q rotating coordinate. The models are convenient for direct analysis and simulation with circuit simulation software. Effects of circuit parasitics are also discussed in [H2]. Due to

three-legged topologies, the zero-sequence component is not revealed in the models. Small-signal models of PWM modulators are also presented in [H1]. It has been shown that a PWM modulator will add additional time delay, and the gain of the PWM modulator could change with respect to the modulation index and the vector position. Both the gain and phase delay of the PWM modulator cannot be expressed in a simple closed form.

Control of three-phase three-legged power converters has been extensively investigated. As with DC/DC converters, control for three-phase power converters can also be classified into voltage mode control and current mode control. Current mode control has been used widely for PFC rectifier, motor drive applications and high performance UPS due to its fast dynamic response and inherent current protection capability. Three independent hysteresis current controllers can provide fast current regulation. However, in unbalanced cases, the performance is degraded due to a continuous fight among the three independent hysteresis controllers. Deadbeat control was proposed to make the controlled variable equal to the reference at the end of each switching cycle so that a response within one discretigation time is obtained. Deadbeat control was used for both single-phase applications [H5] and three-phase applications [H6-8]. It can be applied to both the current control loop and voltage control loop [H7-8].

For hard-switching power converters, a dead time needs to be added for each switching commutation to prevent shoot-through problem. The dead time will cause duty ratio loss, and thus lead to an inaccurate control. The control inaccuracy may greatly degrade performance especially when the ratio of the dead time to the switching period is large. [H14] proposed a method to compensate the duty ratio loss caused by the dead time. It adjusts the pulse width by the amount of dead time according to the load current direction.

As Digital Signal Processor (DSP), microcontroller, and other peripherals such as A/D conversion and D/A conversion become faster and faster, the digital controller becomes more and more popular in power electronics [H9-13] [H22]. A digital controller can easily realize a complicated control algorithm. It is insensible to parameter changes

and temperature variations, and thus more robust. The drawback with a digital controller is an additional time delay caused by sensing, sampling and computation, which is a major limitation for extending control bandwidth. Predictive current control may help to reduce the delay to some extent [B1].

To achieve a high performance with nonlinear load, a low output impedance is needed. The output impedance may be reduced by (1) parallel power converters, or (2) a high control bandwidth. The parallel power converters have to deal with current sharing problem [D5-14]. A high control bandwidth is always desired to achieve a compact and high performance system. The control bandwidth can be extended with a high switching frequency. Soft-switching power converters [C1-14] enable the use of a high switching frequency by reducing switching losses. However, there is a trade-off in using soft-switching power converters. A control inaccuracy may occur due to duty ratio losses caused by interventions of a soft-switching network.

Active filters were investigated in the past decades to deal with nonlinear loads in power systems. The basic principle was first proposed in [G5] in 1971, and was generalized in [G6] in 1976. Active filters can be classified into two categories: shunt (parallel) active filter and series active filter [G7]. Parallel active filters are controlled to be a current source, and used to deal with nonlinear loads with a harmonic current source characteristic; a series active filter is controlled to be a voltage source, and used to deal with nonlinear loads with a harmonic voltage source characteristic [G8]. Active filters can be used not only to handle the harmonics caused by nonlinear loads, but also to handle reactive power [G9-10]. Design aspects of hard switching active filters were discussed in [G14-16], while an example of a soft switching active filter was given in [G17].

There were three hybrid approaches in the active filter applications aiming at a high performance and cost-effective solution. First, a hybrid of a shunt active filter with a passive filter. The shunt active filter compensates low-order harmonic currents, and the passive filter compensates high-order harmonic currents [G7]; second, hybrid of a series active filter with a passive filter [G7][G1-12]. The series active filter does not

compensate harmonic currents, it only isolates the harmonics for the passive filter to handle. This approach can eliminate the sensitivity of the passive filter to the power source impedance, and results in a low cost system; third, a hybrid of a shunt active filter with a series active filter. The so-called universal active can deal with nonlinear loads with both harmonic current and voltage source characteristics [G13].

Harmonic current detection is the major focus in designing an active power filter. Instantaneous reactive power theory was developed in [G19] to extract harmonic currents. Both three-phase voltage and current are sensed. If the three-phase voltage is known, instantaneous reactive power theory is the same as applying d-q transformation to the load current to extract the harmonic currents. Instantaneous reactive power theory is more appropriate for a balanced source. When three-phase systems are unbalanced, [G20] proposed three methods to calculate the current references by using a synchronous detection technique. Under an unbalanced source voltage, the current reference for the active power filter can be given to realize either of the following three: (1) equal power among phases; (2) equal current among phases; (3) equal resistance among phases. The source could be not only unbalanced, it could also be distorted due to heavy nonlinear loads, that makes the harmonic current detection even more difficult. It was also argued in [G21] that when the source voltage is heavily distorted under a heavy nonlinear load, the instantaneous reactive power theory does not give satisfactory results. It could even make the harmonic currents larger. A compensation strategy, which aims at making the nonlinear load/active filter system a constant linear resistor, is concluded to be a better choice in this situation. Another compensation concept suitable for nonlinear voltage and current can be found in [G22], where fictitious power was defined to include reactive power, effect of harmonic voltage and current and subharmonic voltage and current. However, the computation is more complicated.

With the ever faster evolution of power electronics technologies, power converters tend to be connected to form a power converter system. Series and parallel connected power converters are the two basic forms of power converter systems. A series connected AC/DC PFC rectifier and a DC/AC inverter can provide a high performance motor drive system. Multiple power converters in parallel can provide high power

capacity and N+1 redundancy. In recent years, more sophisticated power converter systems have been proposed. Among them, we can find multi-functional power converters, passive circuit combined with active power converter, and active power converter combined with active power converter. One example of a multi-functional power converter was given in [D17], where a three-phase voltage source inverter, used in a battery energy storage system and connected to a utility line, can perform charger, inverter and active filter functions. Hybrid approaches are mostly found in power conditioning applications. A combined system with a shunt passive filter and series active filter was presented in [G11-12] to compensate harmonic currents in power systems. The series active filter isolates the harmonic currents from the power source so that the passive filter can be effective for harmonic currents. The passive-active hybrid system is more effective than a passive filter and practical due to its low cost. An active-active hybrid approach can be found in [G13], where a shunt active filter is combined with a series active filter. Since a shunt active filter is effective in dealing with nonlinear load with harmonic current source characteristics, and a series active filter is effective in dealing with nonlinear loads with a harmonic voltage source characteristics, the hybrid system renders an overall better performance. This kind of active-active power converter system is a hybrid of power converters for different loads. Another kind of active-active power converter system is presented in [D18-20], which partitions the energy flow into two distinguished parts: high-power/low-frequency and low-power/high-frequency, and then handles them separately by two power converters. [D18] presented a high-power magnet power supply, where a low-frequency thyristor rectifier is used to handle the main output power, while a high-frequency PWM converter is in series with the thyristor rectifier to cancel harmonics and compensate for errors. [D19] presented a hybrid system with a similar concept for active power filter application. A GTO high-power low-frequency inverter is combined with a low-power high-frequency IGBT inverter. [D20] was also for power conditioning applications. A high-power multi-step inverter was adopted to handle reactive power, and PWM inverters are adopted for harmonic compensation. The common essential aspect of a power converter system is the control strategy it employs. Since more than one power converter and/or loads are involved, the analysis and control design of the whole system can be extremely difficult. In designing a

power converter system, special attention should also be paid to the circulating current at switching frequency [D1-2] and grounding issue [D16].

Using power converters to perform active damping function was suggested in [H20] and [H21]. A distributed UPS system was presented in [H20]. The loop formed by UPS output filter capacitors and the interconnecting line inductance is highly under-damped. The derivative of the interconnecting current was used as a current reference for each UPS to serve a damping purpose. No active power is processed to perform the damping function since only harmonic currents were included in the derivative. Simulation results showed that active damping can suppress the subharmonic oscillation on the line. However, this approach is noise sensitive due to the derivative. A current type PWM rectifier was presented in [H21] with active damping function. The motivation was to damp harmonic currents amplified by the LC filter of the current type rectifier. There is no prior research on using active damping function for the purpose of extending the control bandwidth of the other power converter.

Large-scale power electronic systems have been analyzed for solar power systems and parallel UPS systems. System stability is of a major concern when many power converters are connected together. The forbidden region concept was developed for test of small-signal stability margin. A large-scale DC distribution power system with PFC rectifier, motor drive, utility power supply, and other power converters, has not been investigated before. There is no large-signal stability issue discussed for this large-scale power electronics system.

1.3Dissertation Outline and Highlights of Contributions

Chapter 2 introduces the characteristics of unbalanced and nonlinear situations in power electronic systems and elaborates on the impacts of nonlinear and/or unbalanced situations to the design of power converters.

Chapter 3 discusses four-legged three-phase power converter topologies and its three-dimensional space vector modulation schemes. The four-legged voltage source

converter can be used in inverter, rectifier and active filter applications. Compared with traditional ways of providing the neutral connection by using split DC link capacitors, zero-sequence trap, or zig-zag transformer, four-legged power converters offer a compact, low cost and high performance solution.

After reviewing different PWM schemes for traditional three-legged power converters, it is concluded that a two-dimensional space vector modulation scheme is an excellent choice for a high-performance digital controlled three-phase three-legged power converter. Unlike a conventional three-phase three-legged power converter, where a balanced load or source is always assumed, the four-legged power converter is used to provide a path for the neutral current due to an unbalanced and/or nonlinear load. Due to the existence of the neutral current, an additional dimension has to be added. Three-dimensional space vector is defined. Three-dimensional space vector modulation scheme is proposed. Different sequencing schemes are given along with the over-modulation in the three-dimensional space.

A comprehensive design example for a four-legged 150 kW inverter is given with special consideration of the unbalanced load specifications.

Chapter 4 addresses the modeling and control issues of four-legged voltage source power converters. The large-signal models of a four-legged inverter are given in both a-b-c stationary coordinate and the d-q-o rotating coordinate. The small signal model is derived in the d-q-o rotating coordinate. The models are verified by measurements. Unbalanced and nonlinear loads are also characterized in the d-q-o rotating coordinate. Their impacts to the control loop designs are analyzed. It is concluded that in general the four-legged power inverter can handle the unbalanced and/or limited nonlinear load with a satisfactory output. However, for high power applications where the control bandwidth is limited by a low switching frequency, the four-legged inverter does not have a high dynamic performance for a strong nonlinear load such as diode rectifier.

Four-legged PFC rectifier is proposed. Its fault tolerant operation capability is demonstrated. It allows ‘equal resistance’ operation under unbalanced source, which is more favorable from the source point of view.

Chapter 5 proposes the concept of multi-functional load conditioner and power converter system. The load conditioner is used to achieve an overall high system performance for a strong nonlinear load. Major power flow in the low frequency range is dealt with by a high power main inverter running at a lower switching frequency, while a small fraction of harmonic power is dealt with by a low power level load conditioner running at a higher switching frequency and designed with a high control bandwidth. The load conditioner assists the main inverter by performing three functions: (1) active filtering; (2) active damping; and (3) decoupling. This power converter system structure offers a low cost and high performance solution to high power applications. The concept can be extended to other applications, such as DC/DC conversion, UPS and high power drive systems. Design aspects of the load conditioner are discussed using the application of a utility power supply as an example. The modeling and control of the load conditioner and the power converter system are presented in d-q-o coordinate. Simulation and experimental results show that the proposed power converter system is very effective for a strong nonlinear load such as a diode rectifier.

Chapter 6 deals with system level issues when the utility power supply, described in Chapter 5, is embedded into a large-scale DC distribution power system. It is found that the utility subsystem behaves like a nonlinear load to the primary DC bus when the utility subsystem is loaded with an unbalanced and/or nonlinear load. This is called the nonlinear loading effect of load converters. The nonlinear loading effect of the utility subsystem to the primary DC bus is pointed out as one of the major large-signal system level issue. It is demonstrated that the nonlinear loading effect has a great impact on the stability of the primary DC bus and performance of source power converter. It is a potential threat to other load converters connected to the same primary DC bus. Two solutions are proposed to eliminate the nonlinear loading effect. One is to modify the load conditioner control scheme such that the nonlinear loading effect is confined within the utility subsystem itself. The other alternative is to use a bus conditioner, which is an extension of the load conditioner concept, to handle the low-frequency ripple power and to provide damping to the primary DC bus and enhance the primary DC bus stability. Both solutions are effective.

Chapter 2 Unbalanced Load/Source and Nonlinear Load

2.1 Introduction

Load condition has profound impacts on the design and performance of power converters, as well as utility line. In most cases, a power converter is designed under the assumption of a balanced load/source. Although unbalanced and/or nonlinear loads and unbalanced sources seem to be abnormal conditions, in the real world unbalanced and/or nonlinear loads and unbalanced sources are prevalent. In this chapter, unbalanced load/source conditions are analyzed based on the symmetrical component theory. They will be used as a design guideline later. Frequency spectrum analysis is used to describe a nonlinear load. In turn, nonlinear loads are modeled as harmonic current sources or harmonic voltage sources. The harmonic load currents will be examined again in the stationary α–β–γ coordinate and the rotating d-q-o coordinate in Chapter 4 and Chapter 5.

2.2 Unbalanced Load/Source and Their Impacts

2.2.1 Definition of Unbalanced Load/Source Based on Power Difference

In a three-phase system, load imbalance could be caused by unevenly distributed single-phase load or by balanced three-phase load running at a fault condition, such as phase open or short fault. The source imbalance may be caused by a large load imbalance and non-uniform source output impedance. An unbalanced load may show up as different load current rms levels among phases, or same load current rms levels but different phase shift, or both. There are several existing ways to define the imbalance. They could be grouped into two methods. The first definition is given in MIL-STD-704E [A12] based on the differences between the maximum per-phase load and the minimum per-phase

load [A12]. A similar definition is also given in NEMA standard MG1-14.24. Another similar definition was adopted in [E1], and expressed as

$$\%\text{UnBal} = \frac{\text{Max(line-to-line load) - Min(line-to-line load)}}{\text{Total Three Phase Load}} \qquad \textbf{(2.1)}$$

The drawback of this definition can be seen from Table 2-1, where I_m is the maximum load current, and I_n is the current through the neutral conductor. Assuming the load power factor varies within [-0.8, +0.8] range, four examples of loading conditions are given in the left column. Load condition ① indicates that only one phase is loaded with the rated power condition; load condition ② indicates that three phases are loaded with the same rms current, however, the power factors are different among phases; load condition ③ indicates that two phases are equally loaded and the third phase is loaded with half of the rated power; load condition ④ indicates that only two phases are loaded. The resulting neutral current is shown in the right column.

Table 2-1 Unbalanced Load and Neutral Current

Load Condition	Neutral Current I_n
① $\lvert I_{LA} \rvert = I_m$; $I_{LB} = I_{LC} = 0$	$\lvert I_n \rvert = I_m$
② $\lvert I_{LA} \rvert = \lvert I_{LB} \rvert = \lvert I_{LC} \rvert = I_m$ $PF_A = 1$; $PF_B = 0.8$; $PF_C = -0.8$	$\lvert I_n \rvert = 1.24\ I_m$
③ $\lvert I_{LA} \rvert = \lvert I_{LB} \rvert = \lvert 2I_{LC} \rvert = I_m$ $PF_A = -0.8$; $PF_B = PF_C = 0.8$	$\lvert I_n \rvert = 1.47\ I_m$
④ $\lvert I_{LA} \rvert = \lvert I_{LB} \rvert = I_m$; $I_C = 0$ $PF_A = -0.8$; $PF_B = 0.8$	$\lvert I_n \rvert = 1.84\ I_m$

Based on the imbalance definition given in (2.1), load condition ④ has a lower percentage of imbalance than load condition ①. However, in terms of the neutral current,

load condition ④ is the worst unbalanced case in that it leads to the largest neutral current.

2.2.2 Definition of Unbalanced Load/Source Based on Symmetrical Component

The difference caused by the magnitude or phase shift of load currents cannot be distinguished by the above-mentioned definition. From a design viewpoint, it is better to use IEC's definition based on symmetrical component representation [A7].

The symmetrical component representation was first proposed by C. L. Fortescue in 1918 and became a textbook method to analyze unbalanced conditions in power systems. It can been seen from the following chapters that symmetrical component representation is not only for the convenience of analysis, but also has it specific physical meaning and provides guideline for the power converter design.

An arbitrarily unbalanced three-phase current (or voltage) is expressed as

$$\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \begin{bmatrix} |I_{LA}|\sin(\omega t + \varphi_{LA}) \\ |I_{LB}|\sin(\omega t + \varphi_{LB}) \\ |I_{LC}|\sin(\omega t + \varphi_{LC}) \end{bmatrix} \quad \textbf{(2.2)}$$

or it can be represented by phasor representation with six variables $|I_{LA}|\angle\varphi_{LA}$, $|I_{LB}|\angle\varphi_{LB}$, $|I_{LC}|\angle\varphi_{LC}$. According to the symmetrical component representation, the six variables can be represented by three sets of balanced three-phase currents – positive sequence currents $I_p = |I_p|\angle\varphi_p$, including I_{LA_p}, I_{LB_p}, and I_{LC_P}; negative sequence currents $I_n = |I_n|\angle\varphi_n$, including I_{LA_n}, I_{LB_n}, and I_{LC_n}; and zero sequence currents $I_0 = I_0\angle\varphi_0$, which is the same for all three phases. The transformation from a-b-c variables to symmetrical components is expressed in (2.3), while the inverse transformation is expressed in (2.4).

$$\begin{bmatrix} I_p \\ I_n \\ I_0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} \quad \textbf{(2.3)}$$

(2.4)
$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_0 \end{bmatrix}$$

where $a=e^{j2\pi/3}$. It is clear that the neutral current equals three times the zero-sequence current. From (2.3) and (2.4), we have

(2.5)
$$\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \begin{bmatrix} I_{LA\_p} + I_{LA\_n} + I_{LA\_0} \\ I_{LB\_p} + I_{LB\_n} + I_{LB\_0} \\ I_{LC\_p} + I_{LC\_n} + I_{LC\_0} \end{bmatrix}$$

An example of the symmetrical component decomposition for an arbitrary unbalanced load current is shown in Figure 2-1;

Based on symmetrical component representation, IEC gives the definition of "degrees of unbalance in a three-phase system" in [A14] as "ratios between the R.M.S. values of the negative sequence [dissymmetry] or zero sequence [assymmetry] co-ordinate and the positive sequence co-ordinate." Based on this definition, an unbalanced load/source can be described by two imbalance factors – negative-sequence unbalance factor Unbal_N%, and zero-sequence unbalance factor Unbal_0%.

The percentage of negative-sequence unbalance is expressed as

(2.6)
$$\text{Unbal\_N\%} = \frac{\text{negative} - \text{sequence} \quad \text{component}}{\text{positive} - \text{sequence} \quad \text{component}} \times 100$$

The percentage of zero-sequence unbalance is expressed as

(2.7)
$$\text{Unbal\_0\%} = \frac{\text{zero} - \text{sequence} \quad \text{component}}{\text{positive} - \text{sequence} \quad \text{component}} \times 100$$

Table 2-2 shows the results of using these two imbalance factors to describe the four cases of unbalanced loads listed in Table 2-1. The Unbal_N% and Unbal_0% may change when the power factors are different.

Table 2-2 Unbalanced Load and Imbalance Factors

Load Condition	Unbal_N%	Unbal_0%
① $\lvert I_{LA} \rvert = I_m$; $I_{LB} = I_{LC} = 0$	100%	100%
② $\lvert I_{LA} \rvert = \lvert I_{LB} \rvert = \lvert I_{LC} \rvert = I_m$ $PF_A = 1$; $PF_B = 0.8$; $PF_C = -0.8$	32.3%	47.7%
③ $\lvert I_{LA} \rvert = \lvert I_{LB} \rvert = \lvert 2I_{LC} \rvert = I_m$ $PF_A = -0.8$; $PF_B = PF_C = 0.8$	35%	72.7%
④ $\lvert I_{LA} \rvert = \lvert I_{LB} \rvert = I_m$; $I_C = 0$ $PF_A = -0.8$; $PF_B = 0.8$	15%	115%

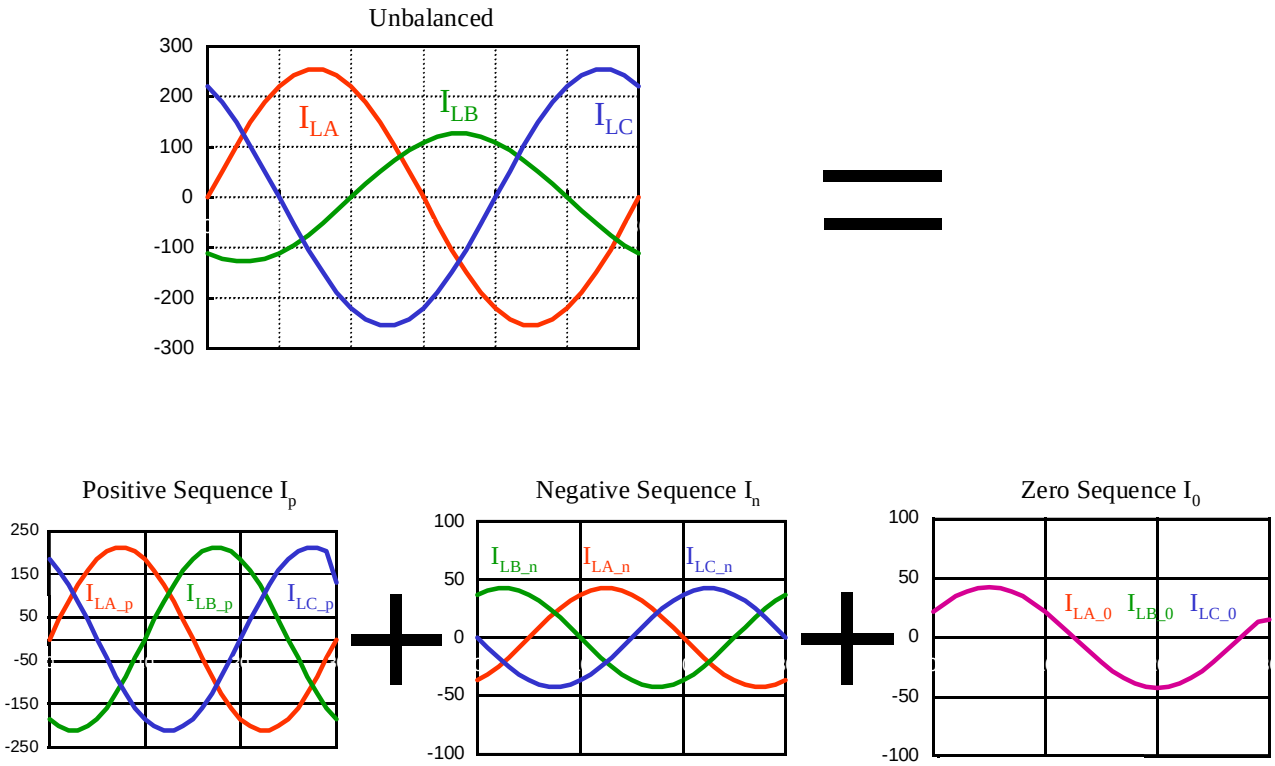


Figure 2-1 Example of symmetrical component decomposition

2.2.3 Impacts of Unbalanced Load/Source

Both the load and the source could be either Δ configuration (three-wire) or Y (four-wire) configuration. Figure 2-2 shows all the four possible connections of the source and load.

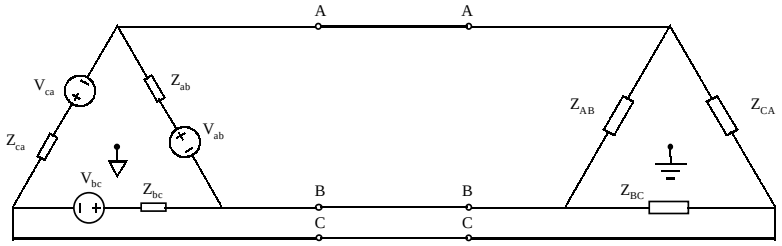
For Δ-Δ connection, both the source and the load have their neutral points floating. When imbalance happens with the load, the line-to-line current will be unbalanced. Flowing through the source impedance, the unbalanced line-to-line current will in turn cause the terminal voltage to be unbalanced. Due to the elimination of the neutral point, the zero-sequence component will be trapped within the source or the load, and it does not exist in the current from the source to the load. The impact of the load imbalance is only reflected by a negative-sequence current from the source to the load. Thus, a ripple power will be circulating between the source and the load at two times the line frequency. Since the neutral points are floating, the voltage potentials of the neutral points will shift according to the unbalanced load. This may cause ground current due to unequal neutral potentials between the source and the load, and more severe EMI problems.

For Δ-Y connection, the situation would be similar to Δ-Δ connection, except that since there is an explicit load neutral point, the load could be malfunctioning due to the shifted voltage potential of the load neutral point. There is no zero-sequence current in the load; however, zero-sequence current could exist in the source.

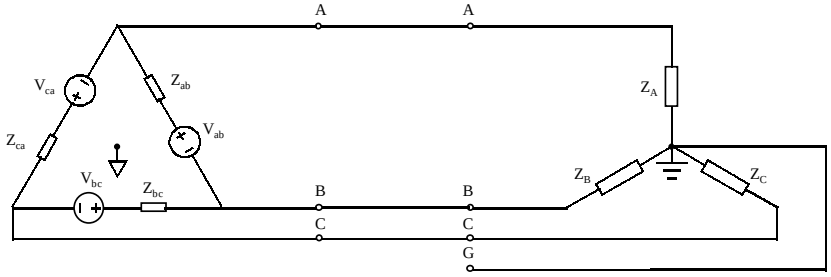
The Y-Δ connection is similar to the Δ-Δ connection, except that there is no zero-sequence current in the source; however, the zero-sequence current could exist in the load.

For Y-Y connection, the source and the load neutral points are tied together. Thus, not only the negative-sequence current circulates between the source and the load at two times the line frequency through the A, B, and C connection, but also the zero-sequence current circulates between the source and the load at the line frequency through the

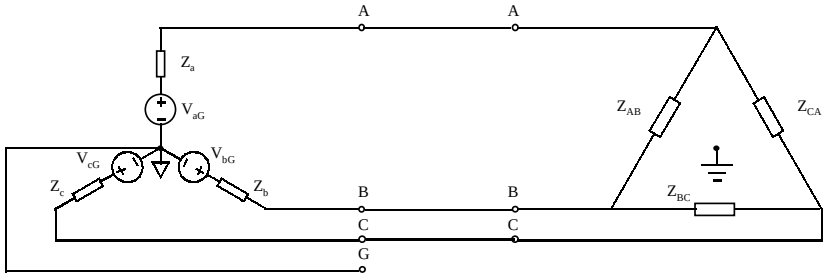
neutral connection G. Since there is no neutral current in a balanced case, normally a neutral conductor is undersized for unbalanced situations. Even worse, a nonlinear load could also cause a large neutral current, which can be seen in Section 2.4.2.



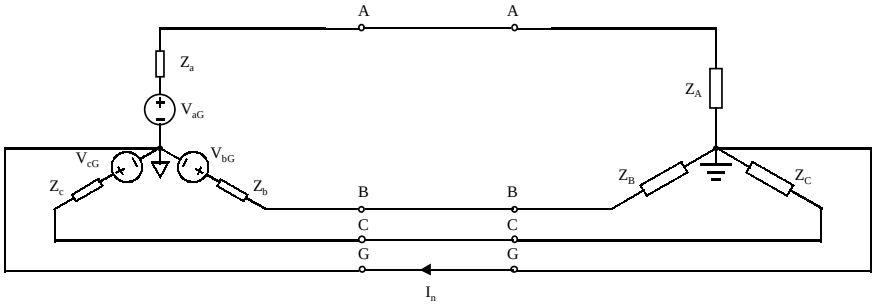
(a) Δ-Δ connection



(b) Δ-Y connection



(c) Y-Δ connection



(d) Y-Y connection

Figure 2-2 Possible source and load connections

2.4 Nonlinear Loads and Their Impacts

2.4.1 Specifications for Nonlinear Loads

The most common linear loads in power electronics system are resistors, inductors and capacitors. The most common nonlinear loads are diode rectifier, thyrisitor chopper, arc furnace, and switching mode power supply. A linear load could be defined as a linear relationship between the voltage across and the current through the load or their derivatives. Although there is no explicit mathematical description for nonlinear loads, they could be described as "a load that draws a non-sinusoidal current wave when supplied by a sinusoidal voltage source" [A9]. Therefore, given a three-phase voltage source, expressed as

$$\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} = V_{ln\_pk} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2}{3}\pi) \\ \sin(\omega t + \frac{2}{3}\pi \end{bmatrix} \quad \textbf{(2.8)}$$

where V_{ln_pk} is the peak of line-to-neutral voltage, the resulting three-phase current through the nonlinear load could be represented by

$$\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \begin{bmatrix} I_1 \sin(\omega t + \varphi_1) + \sum_{k=2}^{\infty} I_{2k\pm1} \sin((2k \pm 1)\omega t + \varphi_{2k\pm1\_A}) \\ I_1 \sin(\omega t + \varphi_1 - \frac{2}{3}\pi) + \sum_{k=2}^{\infty} I_{2k\pm1} \sin((2k \pm 1)\omega t + \varphi_{2k\pm1\_B}) \\ I_1 \sin(\omega t + \varphi_1 + \frac{2}{3}\pi) + \sum_{k=2}^{\infty} I_{2k\pm1} \sin((2k \pm 1)\omega t + \varphi_{2k\pm1\_C}) \end{bmatrix} \quad \textbf{(2.9)}$$

In an ideal case, there is no even order harmonics. Based on (2.9), the load nonlinearity may be compared according to the magnitudes of individual harmonics and the total harmonic distortion (THD), which is defined as

$$\textbf{(2.10)} \qquad \mathrm{THD} = \frac{\sqrt{\sum_{k=2}^{\infty} I_{2k\pm1}^2}}{I_1}$$

Another practical way to depict the characteristics of a nonlinear load is to use crest factor, K_c, which is defined as the ratio between the peak value of the waveform and its rms value. Obviously, a linear load should have a K_c equal to $\sqrt{2}$. Anything other than that would mean a nonlinear load. For a diode rectifier, K_c is normally within the range of 1.5 and 3, depending on the DC link filter design. The harmonic current limitations for nonlinear loads can be found in standards [A9~11].

2.4.2 Impacts of Nonlinear Loads

Several typical diode rectifier loads are studied, including a three-phase diode rectifier without DC link filter, three-phase diode rectifier with only capacitor as the DC link filter, three-phase rectifier with L/C as the DC link filter, and three single-phase rectifiers. Because of their simplicity, reliability and low cost, they are the most popular topologies for front-end AC/DC conversions. All the rectifiers are assumed to have a 277 V (line-to-neutral) three-phase source and an output power of 150 kW with a resistive load. Other nonlinear loads, such as a thyristor rectifier may lead to larger harmonic currents, thus even worse situations. Since a thyristor rectifier is semi-controlled, its waveforms will depend on the regulation requirement. A more complicated analysis needs to be performed. Therefore, they are excluded from this discussion. Simple nonlinear loads, such as rectifiers, are enough to point out the impacts of nonlinear loads.

Case 1: three-phase diode rectifier without DC link filter

A three-phase diode rectifier without a DC link filter is shown in Figure 2-3 (a). It can be seen from Figure 2-3 (b) that the input current is distorted – similar to a quasi-square waveform with two humps on the top. In this case, the crest factor K_c is approximately 1.28, which is less than that of a linear load. The THD is 30%.

Case 2: Three-phase diode rectifier with capacitor DC link filter

A three-phase diode rectifier with a capacitor as the DC link filter is shown in

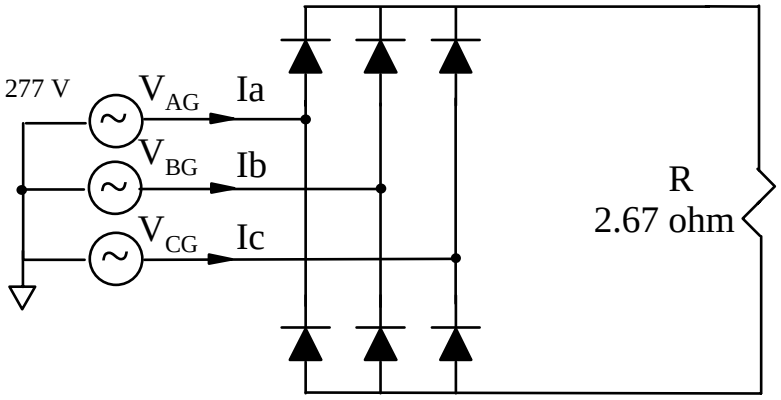
Figure 2-4 (a). A strong pulsating current can be observed in

Figure 2-4 (b). In the studied case, the current THD is 69%; the crest factor K_c is 1.86, which is greater than that of a linear load. The source output impedance, transmission line impedance, ESR of the filter capacitor and its capacitance have a great influence on the current peaking, thus, on the crest factor and THD. The larger the capacitance is, the larger the current peak and THD would be; the larger the source output impedance, transmission line impedance, and ESR of the capacitor are, the smaller the current peak and THD would be.

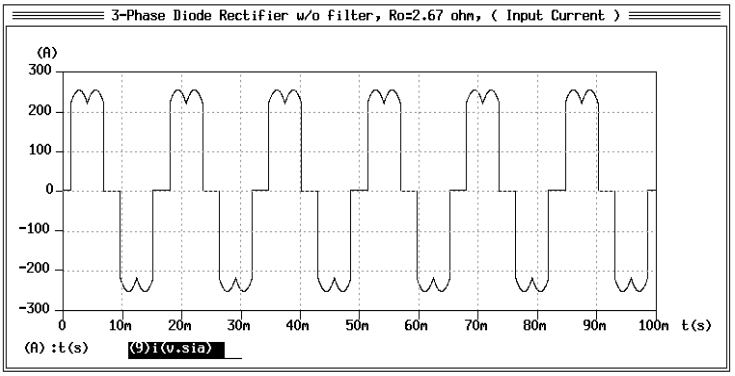
Case 3: Three-phase diode rectifier with L/C DC link filter

A three-phase diode rectifier with L/C DC link filter is shown in Figure 2-5 (a). Due to a relatively large inductor, a quasi-square wave current can be observed in Figure 2-5 (b). The inductor smooths out the pulsating current caused by the capacitor. That results in a less THD of 29%, and a smaller K_c of 1.22, which is similar to Case 1 due to the resemblance between the waveforms.

(a)



(b)



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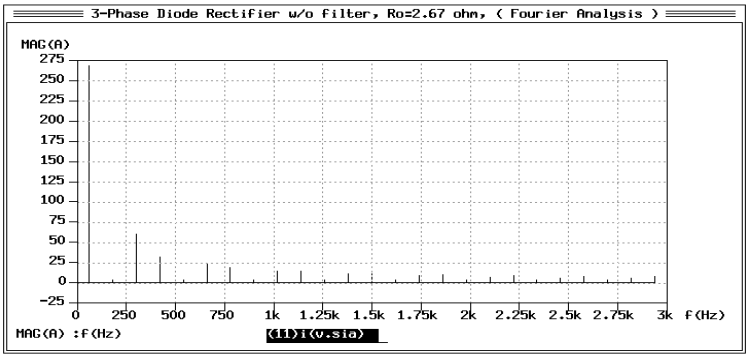
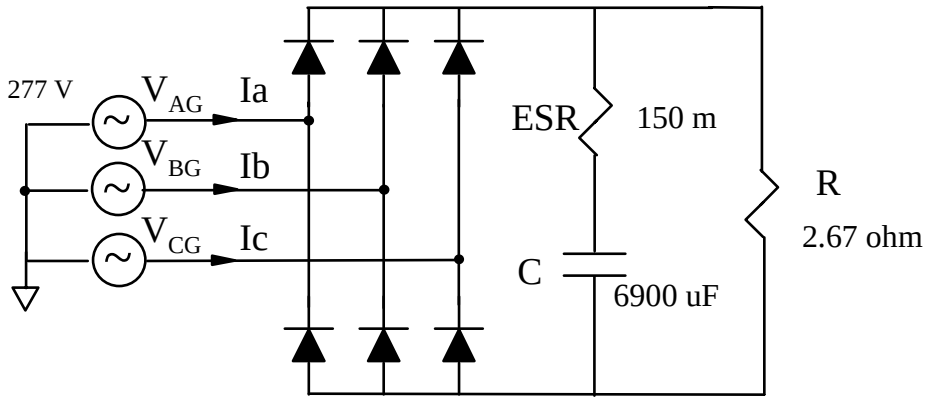


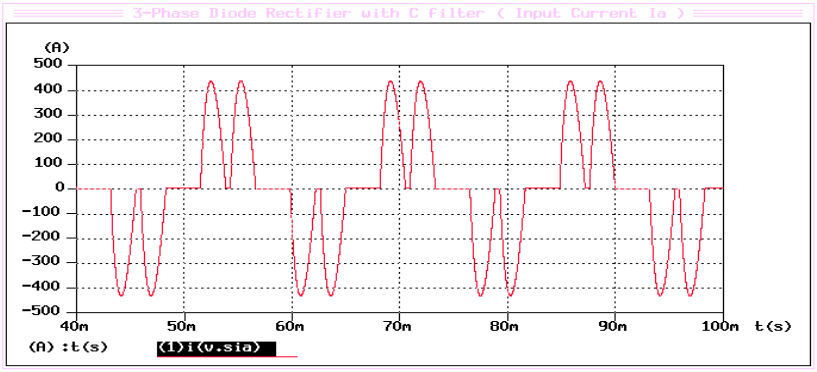
Figure 2-3 Three-phase diode rectifier without DC link filter

(a) power stage; (b) phase A current; (c) frequency spectrum of phase A current

(a)



(b)



(c)

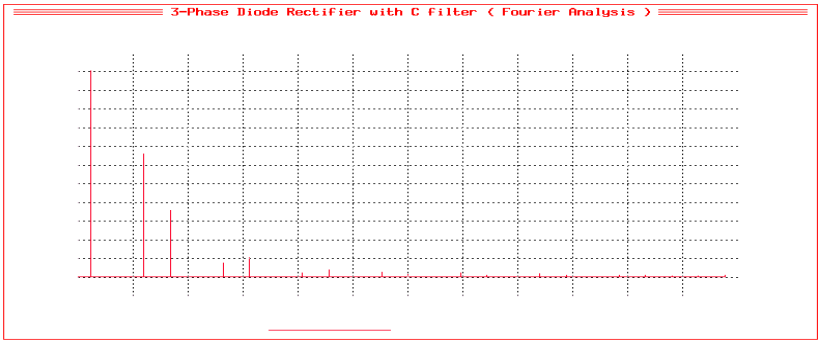
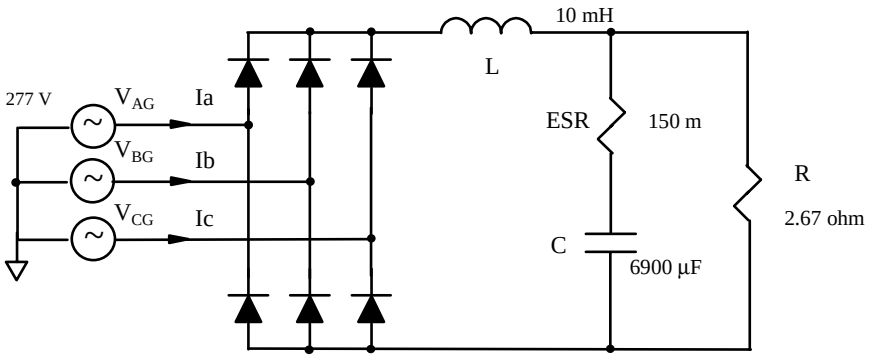


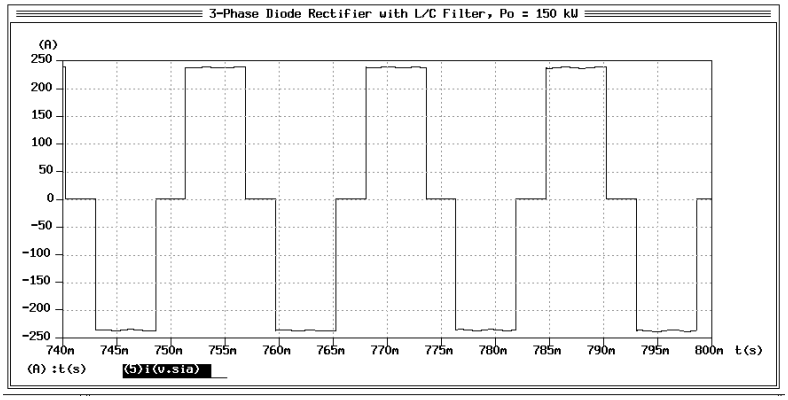
Figure 2-4 Three-phase diode rectifier with capacitor DC link filter

(a) power stage; (b) phase A current; (c) frequency spectrum of phase A current

(a)



(b)



(c)

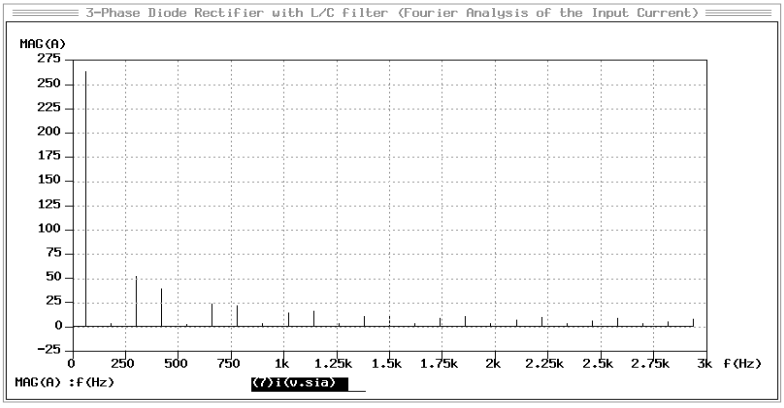


Figure 2-5 Three-phase diode rectifier with L/C DC link filter

(a) power stage; (b) phase A current; (c) frequency spectrum of phase A current

Case 4: Three single-phase diode rectifiers with capacitor filter

The power stage of three identical single-phase diode rectifiers is shown in Figure 2-6. A typical pulsating current for a single-phase diode rectifier can be found in Figure 2-7 (a). From the frequency spectrum shown in Figure 2-7 (b), it can be seen that the crest factor K_c is 2.23, which is much larger than that of a linear load; the phase current THD is 65%.

Despite the fact that the three phases are identically loaded and that currents through each phase have identical waveforms, there is a large amount of third order harmonic current going through the neutral. In this case, the neutral current is 1.7 times the phase current. All the other harmonics are cancelled among phases due to the 120 ° phase shift, and thus, they do not appear on the neutral. The third order harmonic and other triplen harmonics cannot be cancelled because they have the same phase shifts. For an identically loaded single-phase nonlinear loads on the three phases, it can be found that 3k order harmonic are zero-sequence, where k={1,3,5…∞}, e.g. 3^{rd}, 9^{th}, 15^{th}; 3k+1 order harmonics are positive sequence, e.g. 7^{th}, 13^{th}, 19^{th}; and 3k+2 order harmonic currents are negative sequence, e.g. 5^{th}, 11^{th}, 17^{th}, where k={2,4,6…∞}.

The comparison of major harmonic contents with respect to the fundamental component in the four cases is shown in Table 2-3.

Table 2-3 Comparison of Ratios between Major Harmonic Contents and the Fundamental Components

Case	3^{rd} (%)	5^{th} (%)	7^{th} (%)	9^{th} (%)	11^{th} (%)	13^{th} (%)	THD(%)	K_c
1		22	11.7		8.7	6.9	30	1.28
2		60	32		6.6	9.3	69	1.86
3		20	15		8.6	8.2	30	1.22
4	76%	40	8.4	7.1	7.4		65	2.23

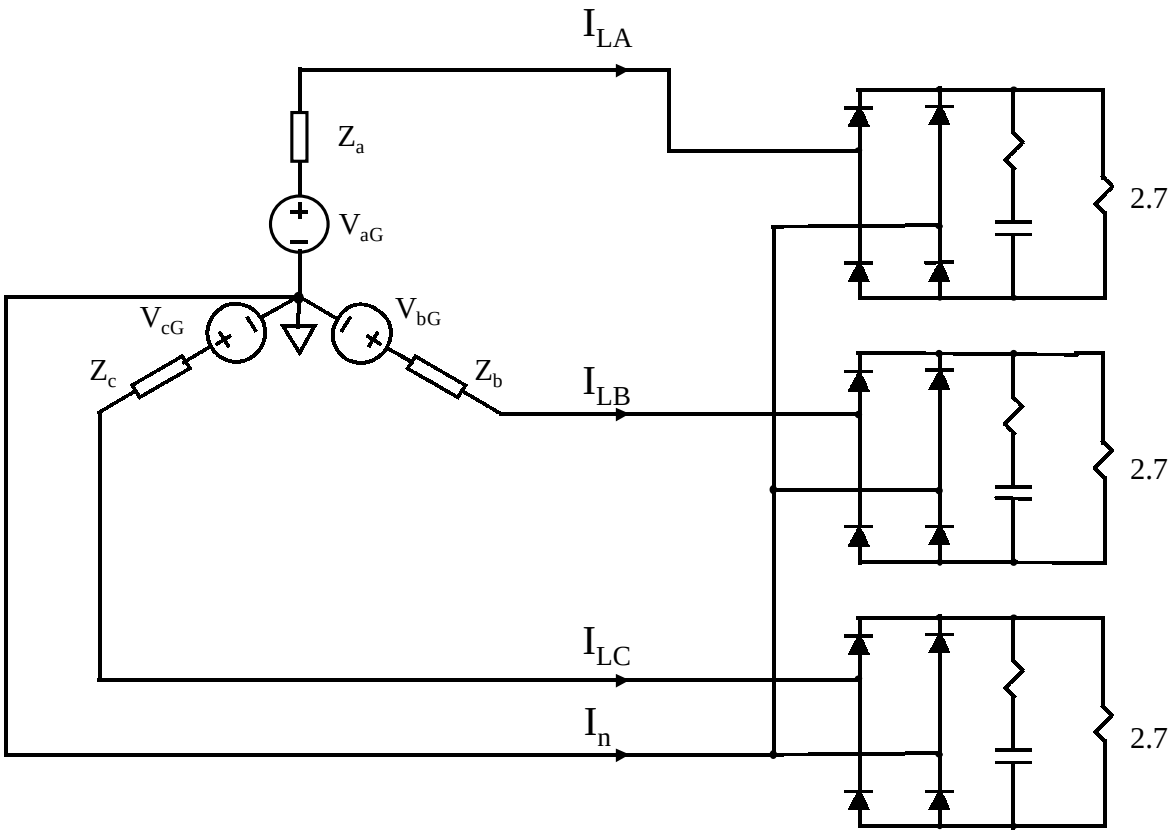
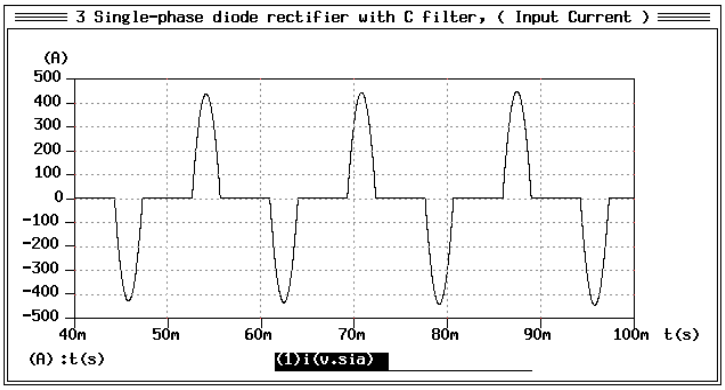
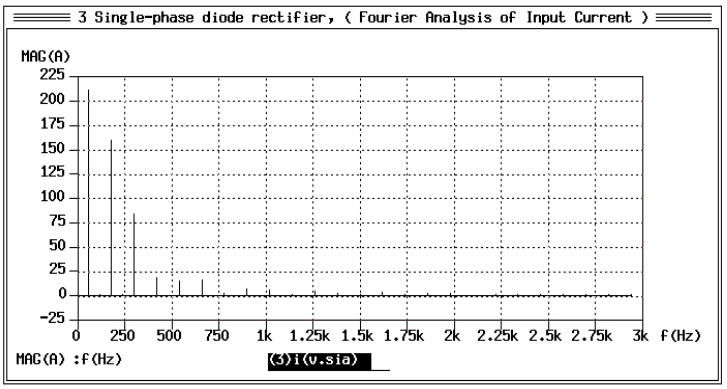


Figure 2-6 Three single-phase diode rectifier with capacitor DC link filter

(a)



(b)



(c)

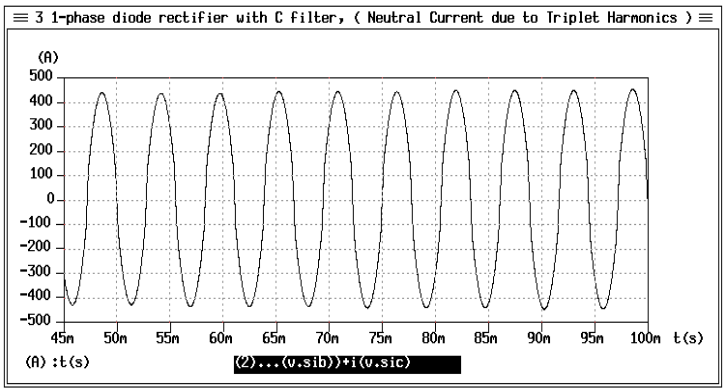


Figure 2-7 Waveforms for three single-phase diode rectifier

(a) phase A current; (b) frequency spectrum of phase A current; (c) neutral current

The harmonics produced by the nonlinear loads have several undesirable impacts on the source and other loads connected to the same source, including:

- Distorted source voltage. Harmonic load current flowing through the source output impedance produces harmonic voltage drop. The effect can be seen as voltage notches and/or distorted sinusoidal at the input voltage terminal. The distorted source voltage will consequently affect the load current distortion.

- Overheating of transformers. Due to skin effect, the conduction losses due to harmonic currents can be excessive. The originally designed transformer for linear load may suffer from overheating problem and incur fire. For a safe operation, a transformer has to be greatly derated.

- System oscillation. The harmonic currents spread over a wide frequency range, which may excite system oscillation at the system natural frequency.

- Mechanical vibrations and acoustic noise in motors and generators. The harmonic currents generate harmonic flux in the electric machines. The ripple torque produced by harmonic flux causes mechanical vibrations and larger acoustic noise.

- Larger conducted and radiated EMI noise. The harmonic currents generate large conducted EMI noise. Travelling through the transmission line, they are also the radiated EMI source. The large EMI noise due to harmonic currents causes performance degradation or malfunction of communication systems and electronic equipment.

- Last but not the least, nonlinear loads, like three single-phase rectifiers, may cause a great amount of neutral current which may be far more severe than an unbalanced load. An overheated neutral conductor is often found with this kind of load. In practice, the transformer may have to be derated up to 50%.

There are several ways to tackle the undesirable impacts of nonlinear load. They can be classified as passive means and active means. Passive harmonic filters can be used to either trap harmonics within the filter or block the harmonic currents from returning to

the source. Passive harmonic filters are normally very bulky. Since they have to be tuned to the specific harmonics, the line impedance has to be known. However, normally it is hard to know the exact line impedance. Passive harmonic filter may even excite system oscillation. Active filter was proposed two decades ago. Active filter is a power converter used to control harmonic currents through the transmission line. It is proven that active filter is an effective way to handle nonlinear loads in power systems.

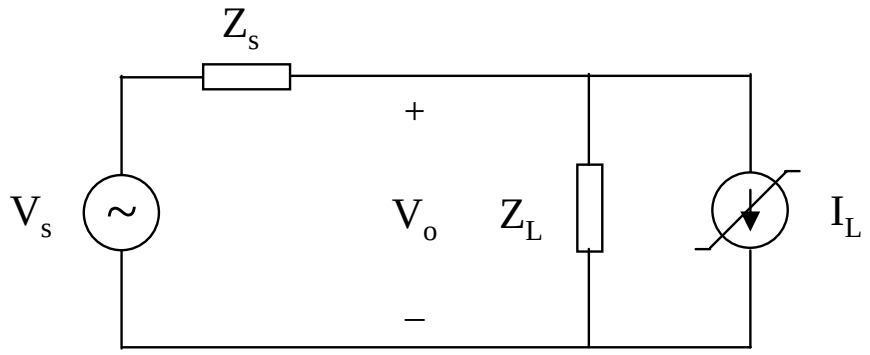
2.4.3 Model of Nonlinear Loads Using Harmonic Sources

A nonlinear load may be modeled by a harmonic current source or harmonic voltage source, depending on the input impedance of the nonlinear load.

A nonlinear load with large input impedance can be modeled as a harmonic current source. The nonlinear load described above as Case 3 is an example of such current-type nonlinear load. The input filter inductor yields a large input impedance. The conduction of the diodes is determined by the source voltage and the current through the inductor. Whenever a diode conducts, the source sees the inductor current. A per phase model is shown in Figure 2-8(a), where Z_s is the source output impedance, and Z_L is the load input impedance. Normally the load impedance of a current-type nonlinear load Z_L is much larger than the source impedance Z_S, therefore, the equivalent circuit can be simplified as shown in Figure 2-8(b). It should be noted that the magnitude of the harmonic current source is not proportional to the load power level in that the terminal voltage V_o also depends on the harmonic currents. Since many applications have a smooth inductor filter or input EMI filter with large impedance, this dissertation will focus on the current-type nonlinear loads. In active filter applications, a shunt active filter is more effective for a current-type nonlinear load [G8].

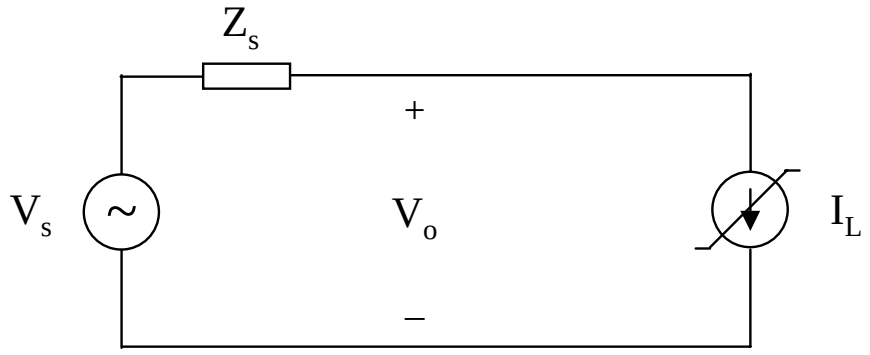
A nonlinear load with small input impedance can be modeled as a harmonic voltage source. The nonlinear load described above as Case 2 and 4 are examples of such voltage-type nonlinear loads. The input filter capacitor yields a small input impedance. The conduction of the diodes is determined by the source voltage and the DC output voltage. Whenever a diode conducts, the source sees the DC output voltage. A per phase

model is shown in Figure 2-9. For active filter applications, a series active filter is more effective for voltage-type nonlinear loads [G8].



(a)

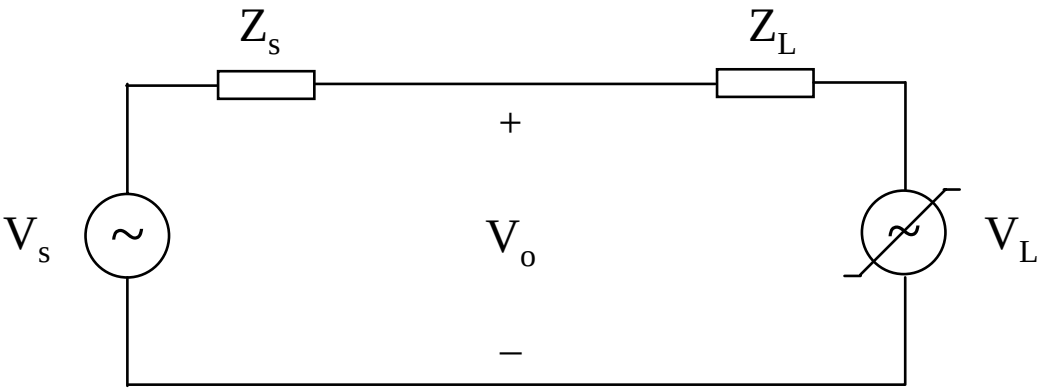
$$I_L = I_1 \sin(\omega t + \varphi_1) + \sum_{k=2}^{\infty} I_{2k\pm1} \sin((2k \pm 1)\omega t + \varphi_{2k\pm1\_A})$$



(b)

Figure 2-8 Current-type nonlinear load – nonlinear load modeled as harmonic current source

(a) Z_s is comparable with Z_L; (b) $Z_s << Z_L$



$$V_L = V_1 \sin(\omega t + \varphi_1) + \sum_{k=2}^{\infty} V_{2k\pm1} \sin((2k \pm 1)\omega t + \varphi_{2k\pm1\_A})$$

Figure 2-9 Voltage-type nonlinear load – nonlinear load modeled as harmonic voltage source

2.5 Conclusions

In this chapter, specifications for unbalanced loads and nonlinear loads are introduced. The symmetrical component representation is used to specify an unbalanced load/source conditions. Harmonic spectrum, THD and the crest factor are adopted to describe a nonlinear load.

An unbalanced load/source could produce negative-sequence current and zero-sequence current in the system depending on the source and load connection. The negative-sequence current draws 2ω ripple power from the source. The zero-sequence current will flow through the neutral conductor.

Nonlinear loads produce harmonic currents under ideal voltage source. Depending on its impedance, they can be modeled as a harmonic current source or harmonic voltage source. For balanced three-phase nonlinear loads, different harmonic contents have different phase sequences, e.g. fundamental, 7^{th}, 13^{th} harmonics are positive-sequence components; 5^{th}, 11^{th} harmonics are negative-sequence components; 3^{rd}, 9^{th} are zero-sequence components and they exist when the source and the load have a Y-Y connection. Nonlinear loads have several undesired impacts on the system. Special efforts, such as passive harmonic trap or active filter, should be made to eliminate harmonic currents in the system.

Chapter 3 Four-Legged Power Converters and Three-Dimensional Space Vector Modulation

3.1 Introduction

In this chapter, voltage source four-legged power converters are described which can operate as a four-legged inverter or PFC boost rectifier. A four-legged voltage source inverter has the ability to handle the ground current due to an unbalanced and/or nonlinear load. The operation of the four-legged power converter is described, which makes clear the advantages of the four-legged power converter over a traditional three-legged power converter. A comprehensive design procedure is given for a four-legged high power inverter.

In the past, much research has been done along the line of pulse width modulation (PWM) control of a power converter. A space vector modulation (SVM) control is deemed advantageous over a sinusoidal pulse width modulation (SPWM) because it has a higher DC bus utilization, less output voltage/current harmonics, less switching loss and is suitable for implementation using a digital controller. For a traditional three-legged power converter, where a balanced case or absence of the zero sequence is always assumed, a space vector is defined in a two-dimensional (2D) plane and a SVM is performed in the two-dimensional plane. For the four-legged power converters, a three-dimensional (3D) space vector has to be defined in this chapter. New three-dimensional space vector modulation schemes are also proposed. The three-dimensional space vector modulation schemes are supersets of, and thus are compatible with, conventional two-dimensional space vector modulation schemes.

Some simulation and experimental results are given based on a 150 kW four-legged power inverter used for a standalone power supply system, and a four-legged PFC rectifier. The operation principle of the four-legged power converter and the three-dimensional space vector modulation is verified.

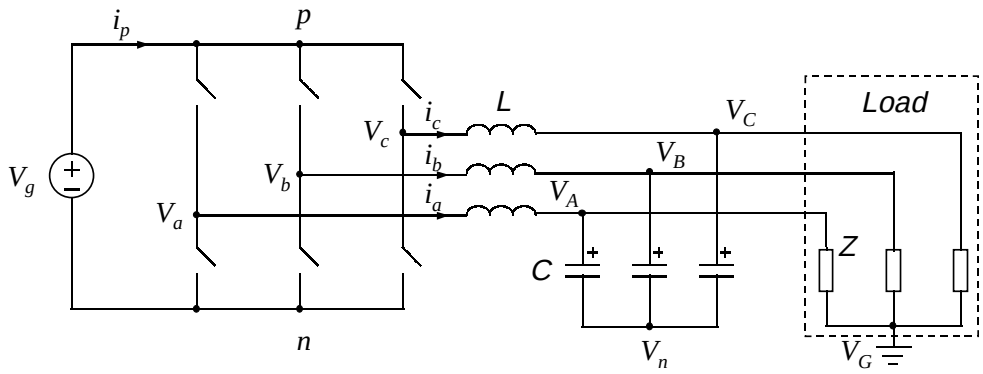
3.2 Three-Legged Power Converters of Its Space Vector Modulation

3.2.1 Three-Legged Voltage Source Power Converters

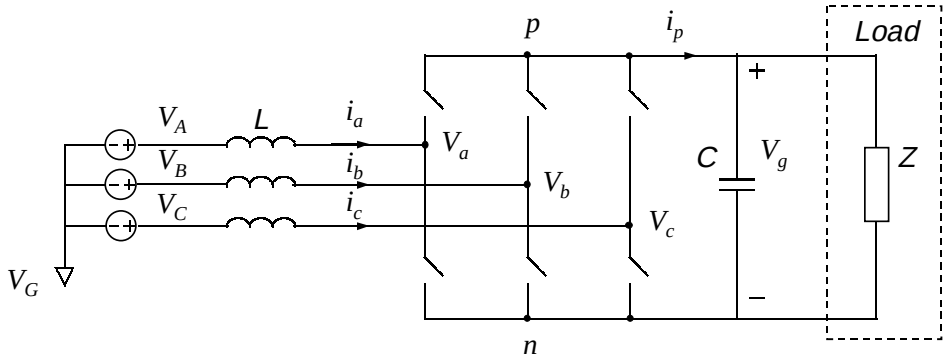
Three-legged voltage source power converters include voltage source inverter (VSI) and boost PWM rectifier, as shown in Figure 3-1. They are the most popular power converter topologies used in motor drive applications and three-phase PFC rectifiers. A common switching network, consisting of six power switches, can be identified in both the voltage source inverter and the boost rectifier, as shown in Figure 3-2. The switching network has DC terminals – p and n, and AC terminals — V_a, V_b, and V_c. To construct a voltage source inverter, an ideal voltage source is connected to the DC terminals, while a balanced three-phase L/C filter is connected to the AC terminals. To construct a boost PWM rectifier, the load is connected to the DC terminals, while three boost inductors are connected to the AC terminals. It is normally assumed the three-phase load is balanced for a three-phase voltage source inverter. Ideally the voltage potential of V_G would be the same as that of V_n, and there would be no ground current incurred. Similarly a well-balanced three-phase AC source is also assumed for the boost PWM rectifier.

The switching network chops energy into chunks and dispatches the energy chunks by on/off actions. Each of the ideal switches in the switching network operates in the first and second quadrant of the V-I plane, and can be realized by a power switch shown in Figure 3-3. Figure 3-4 is a unified representation of a three-legged power converter including an inverter and a rectifier. A modulator controls the switching actions of the switching network. The modulator sends all the gate signals of the power switches. For an inverter used as an UPS, the modulator sends on/off control signals to the switching network such that the output voltage at the energy sink terminal is a three-

phase sinusoidal voltage. For boost rectifier, the modulator sends on/off control signals to the switching network such that the current from the energy source is a three-phase sinusoidal current.



(a)



(b)

Figure 3-1 Three-phase voltage source power converters

(a) voltage source inverter (b) boost PWM rectifier

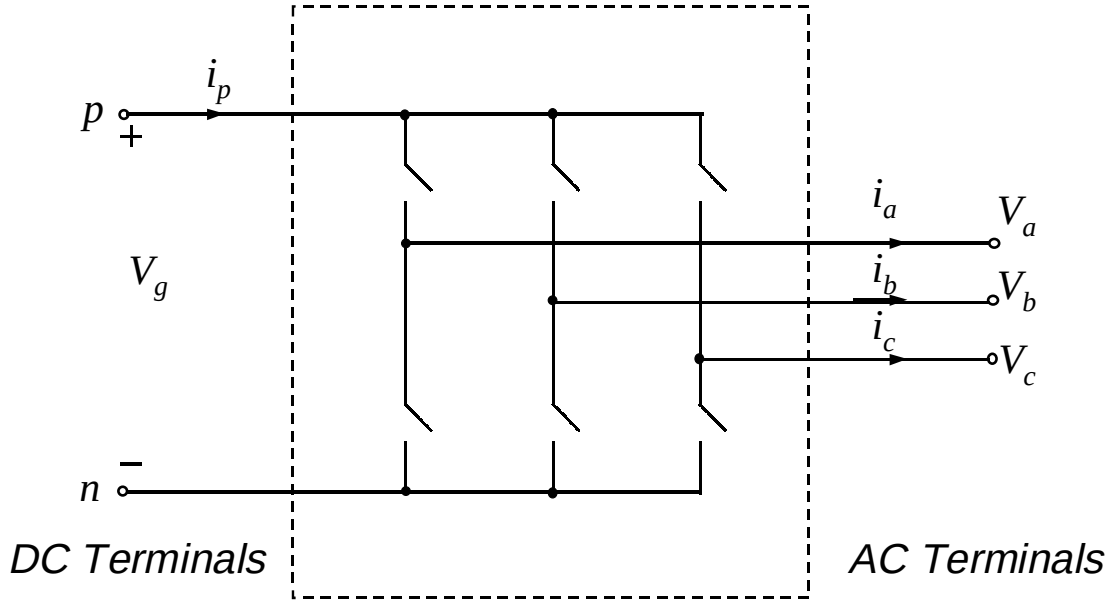


Figure 3-2 Three-legged switching network

Figure 3-3 Power switch realization and its characteristics

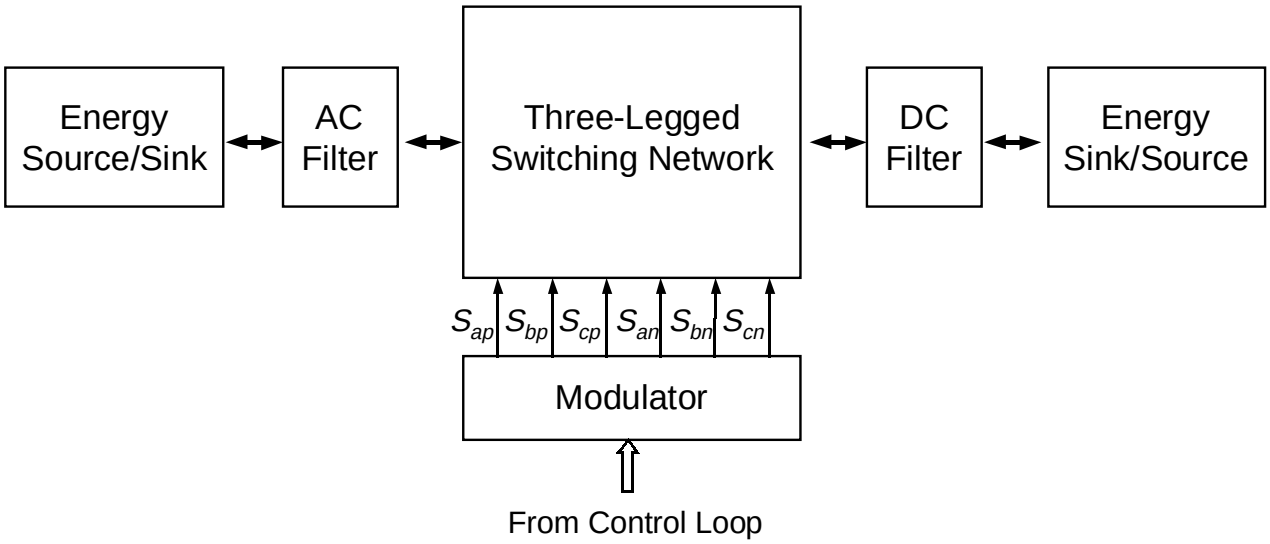


Figure 3-4 Unified block diagram of three-legged power converters

3.2.2 Review of Pulse Width Modulation

The pulse width modulation (PWM) concept is borrowed from communication systems, where a signal is modulated before its transmission, and then demodulated at the receiving terminal to recover the original signal. The same concept can be applied to a power converter. In a power converter, the switching network has an on/off nonlinear nature. The desired continuous waveform is modulated and converted to digitized signals to control the switching network. Then the modulated signals at the switching network AC terminals are demodulated by the AC filter to get the desired continuous voltage or current waveform.

Normally a sinusoidal voltage or current is the control target for a power converter. The first PWM scheme was the sinusoidal PWM (SPWM) scheme and was proposed in 1964 [B23]. Since the modulator has a great impact on voltage/current distortions, switching losses, and EMI, it is of great interest to the power electronics researcher. In the past there has been intensive research on this topic and there is much literature on it. All the proposed PWM schemes may be classified into four categories, namely, (1) SPWM and its derivations; (2) Optimal PWM (3) Space Vector Modulation (SVM); (4) Hysteresis and Bang-Bang type modulation; and (5) Random PWM.

All the PWM schemes may be evaluated under a certain switching frequency and the reference signal frequency ratio, and the input and output voltage ratio, which is also named as the modulation index M. The definition of the modulation index M is given in (3.1),

$$\mathbf{(3.1)} \qquad M = \frac{V_{ll\_pk}}{V_g}, \tag{3.1}$$

where V_{ll_pk} is the peak value of the line-to-line voltage, V_g is the DC link voltage. The performance of a modulation scheme can be evaluated based on the following five aspects: (1) distortion of the output voltage or current; (2) power losses; (3) harmonic spectrum and EMI; (4) dynamic range; and (5) complexity. It is always desirable to minimize the distortion of the output voltage or current. It may change with

the modulation index in a nonlinear curve. The power losses are related to the total number of switching actions in one switching cycle, and the current level at switching. Therefore, different modulation schemes may result in different efficiencies. A PWM scheme with minimized switching losses is desirable especially for high power applications. Harmonic spectrum of the output voltage or current is related to the EMI issue and acoustic noise. It is desirable to minimize the EMI and acoustic noise. Dynamic range refers to the maximum possible control level in steady state or during transient. It can also be interpreted as the ratio between the maximum possible output and the input. It is desirable to have a higher ratio. For a voltage source inverter, it means a better DC link voltage utilization, which is crucial for high voltage applications. It is preferable to have a PWM scheme that can be implemented easily, by either an analog means or digital means.

3.2.2.1 SPWM and Its Derivations

A basic SPWM three-phase modulator is shown in Figure 3-5(a). It consists of three independent single-phase sinusoidal pulse width modulators. The operation principle is depicted in Figure 3-5(b) using phase A as an example. To get the sinusoidal output, the reference is set to be sinusoidal. Compared with a triangle carrier, a pulse train is obtained and fed to the switching network to control the on/off of the power switches. The carrier does not necessarily have to be a triangle waveform. It could be saw-tooth waveform or any other waveform, which makes the pulse width linearly proportional to the reference signal. However, a triangle carrier leads to a smaller output harmonic distortion due to the symmetrical nature of the pulse train.

Harmonic distortion of SPWM scheme is higher than other modulation schemes especially at a high modulation index and when the switching frequency to signal frequency ratio is low, which is almost inevitable for high power applications [B1] [B17]. There are six switching actions in one switching cycle and all three phases are switched. The switching losses of SPWM will be used as a fundamental basis of comparison with other modulation schemes. The harmonic spectrum of SPWM is higher than SVM schemes since three phases are independently controlled and there is a higher

voltage/current ripple due to the circulating energy. The dynamic range of a power converter using SPWM is low. The maximum modulation index is only $\frac{\sqrt{3}}{2}$ [B15] [B1]. The most distinct advantage of SPWM is its simplicity. It only takes three analog comparators to implement.

There have been efforts to modify the basic SPWM and overcome its shortcomings. The following summarizes some of the derivations from the basic SPWM.

Synchronized SPWM: When the reference signal frequency changes, as in motor drive applications, the carrier frequency can be synchronized with the signal frequency. Synchronized SPWM can reduce a great amount of harmonic distortion especially when the carrier frequency to the signal frequency ratio is low.

Natural Sampled and Regular Sampled SPWM: Since the switching actions take place immediately after the reference signal intersects the carrier signal, the implementation shown in Figure 3-5 is called natural sampled SPWM. Natural SPWM is suited to using analog circuitry for implementation. If a digital modulator is used, the switching actions take place at regularly sampled time instants. Normally regular sampled SPWM scheme leads to higher distortion.

Harmonic Injected SPWM: By injecting the triplen harmonics into the sinusoidal reference, the so-called harmonic injected SPWM can increase the maximum modulation index, thus, the dynamic range. The injected triplen harmonics will not increase the output harmonic distortion since in a three-phase three-wire system all the triplen harmonics do not appear at the output.

3.2.2.2 Optimal PWM

Optimal PWM may be a misleading term. It actually refers to a specific PWM technique normally used for applications where the ratio between the switching frequency and the reference signal frequency is low. In such cases, it is found that certain harmonics, e.g. 5^{th} and 7^{th}, can be completely eliminated if the switching angles of the

pulse train in one reference signal period are at optimized positions. This can be implemented by using discrete Fourier analysis and optimization. It is also called Harmonic Elimination PWM scheme [B24] [B1]. Harmonic Elimination PWM is a sub-optimal PWM scheme aimed at the elimination of certain harmonics. Other optimal PWM schemes were also proposed based on different optimization target, e.g. minimum THD [B25], and minimum torque ripples [B26]. The major disadvantage of the optimized PWM schemes is that normally the optimized PWM pattern is pre-calculated and stored in a look-up table, therefore, the dynamic performance is poor. Since it is difficult to perform an on-line optimization with the Fourier analysis involved, one optimized PWM scheme is proposed in [B27], where an off-line optimization for the steady-state is combined with an on-line optimization for transient. With the ever-faster advance of high speed Digital Signal Processor, it is possible to have a real time optimized PWM scheme implemented.

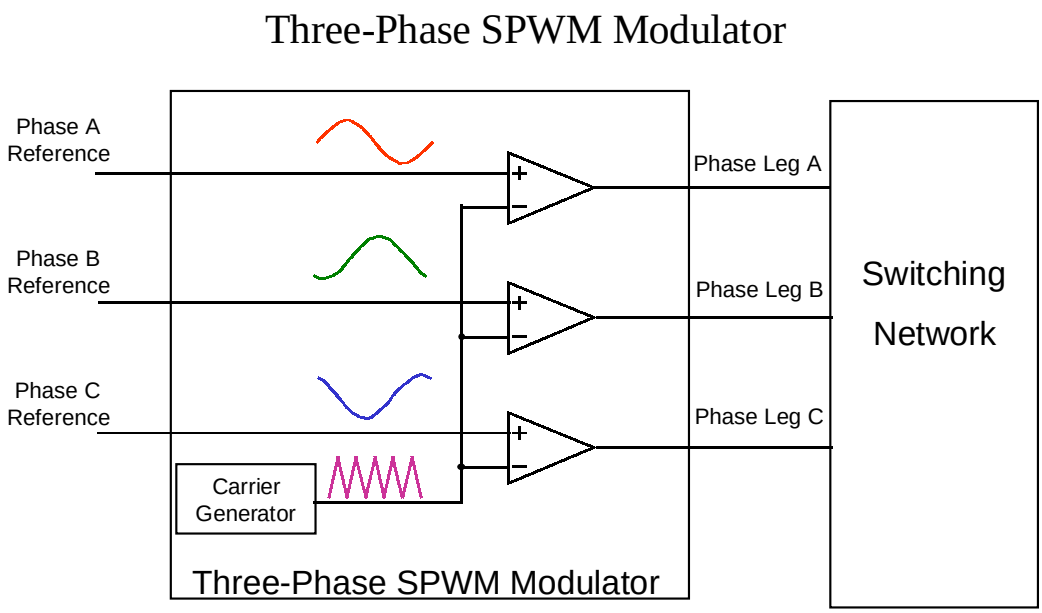
3.2.2.3 Space Vector Modulation

The block diagram of a space vector modulator is shown in Figure 3-6. Assuming a balanced three-phase three-wire system, all the eight possible switching combinations of the switching network are mapped into an orthogonal α–β coordinate. The results are six non-zero switching vectors – $V_1 \sim V_6$, and two zero vectors V_{Z1} and V_{Z2}. The six non-zero switching vectors form a hexagon. There are four steps to perform the space vector modulation. First, the reference signals for phase A, B and C are mapped into the orthogonal α–β coordinate, and are represented by a reference vector V_{ref}. Second, switching vectors are selected, including non-zero vectors and zero vectors, to synthesize the reference vector V_{ref} for one switching cycle. Third, the time durations for all selected switching vector are calculated by a simple trigonometric algorithm. The objective is to make the averaged switching vector in one switching cycle equal to the reference vector V_{ref}. Fourth, the switching vectors are sequenced and dispatched to the switching network. Since the modulation is performed on a two-dimensional α–β plane, it can be called two-dimensional space vector modulation, to differentiate it from the proposed three-dimensional space vector modulation in this dissertation.

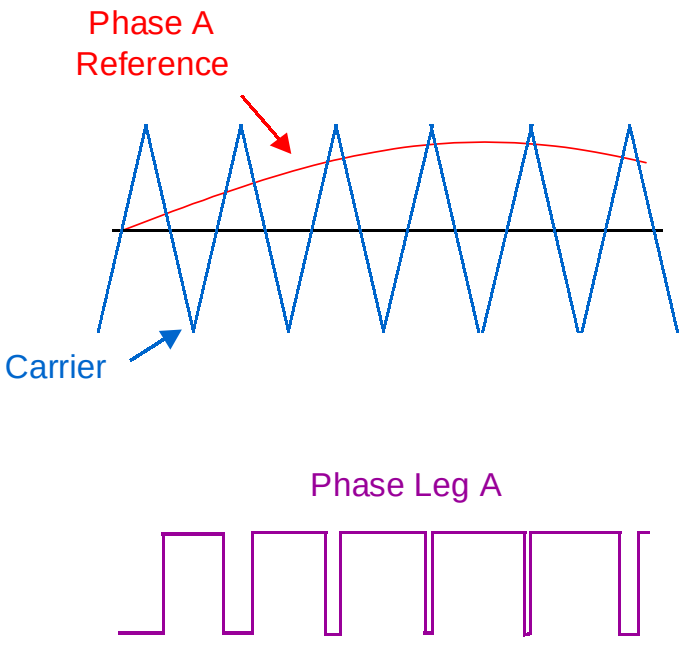
Up to now, there have been many variations in the space vector modulation schemes [B1-19] [C1-3] [D1]. Space vector modulator may be the most favorable and popular modulation scheme for most three-phase applications for the following reasons. It can render lower output voltage/current distortion than SPWM and other PWM schemes, especially at high modulation index range. Also the switching losses, harmonic spectrum and EMI can be minimized. The maximum modulation index can reach one, which is more than 15% higher than the SPWM modulator. The high modulation index means that the DC link voltage is fully utilized, and the dynamic range is extended. Although space vector modulation can be realized by using analog circuitry, it is more suited to digital implementation. Detailed analysis of the two-dimensional space vector modulation is in Section 3.2.3.

3.2.2.4 Hysteresis and Bang-Bang Type Modulation

The block diagram of a three-phase hysteresis modulator in shown in Figure 3-7(a). The pulse train is generated in a feedback fashion. The error between the reference and the feedback signal is fed into a hysteresis comparator to generate the control pulses for the switching network. The concept of a hysteresis modulator is to confine the error within a window, as shown in Figure 3-7(b). Hysteresis modulator also has the major merit of inherent stability. It is primarily used in the current controller in high-performance drive applications and power factor correction rectifiers where a fast current regulation is crucial. Another advantage of the hysteresis modulator is its simplicity. However, it suffers greatly from a wide variation of switching frequency range. Since each phase is independently controlled, there is the possibility of conflict among phases. That leads to some other major disadvantages, such as an inaccurately controlled current, large output waveform distortion, and poor utilization of the DC link voltage [B32]. Although there are some derivations of the basic hysteresis PWM scheme to address the above mentioned problems, they are still inherent problems to this family of PWM schemes. A hysteresis modulator can be implemented with very simple analog circuitry.



(a)



(b)

Figure 3-5 Three-phase SPWM modulator

(a) block diagram (b) operation principle for phase A

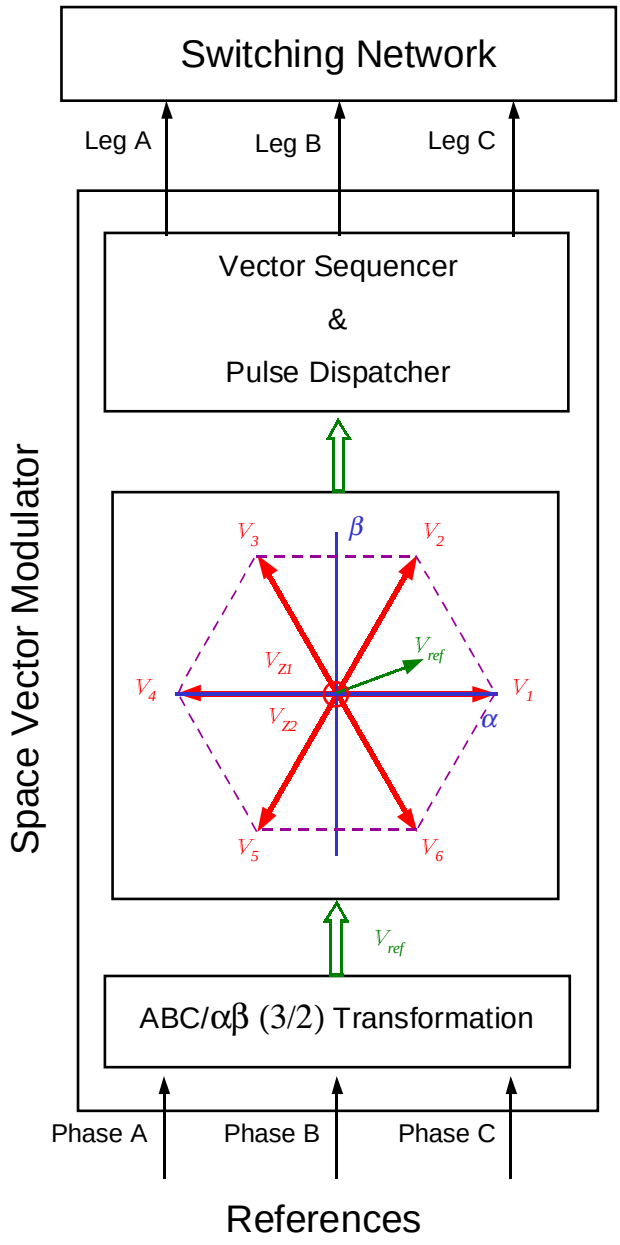
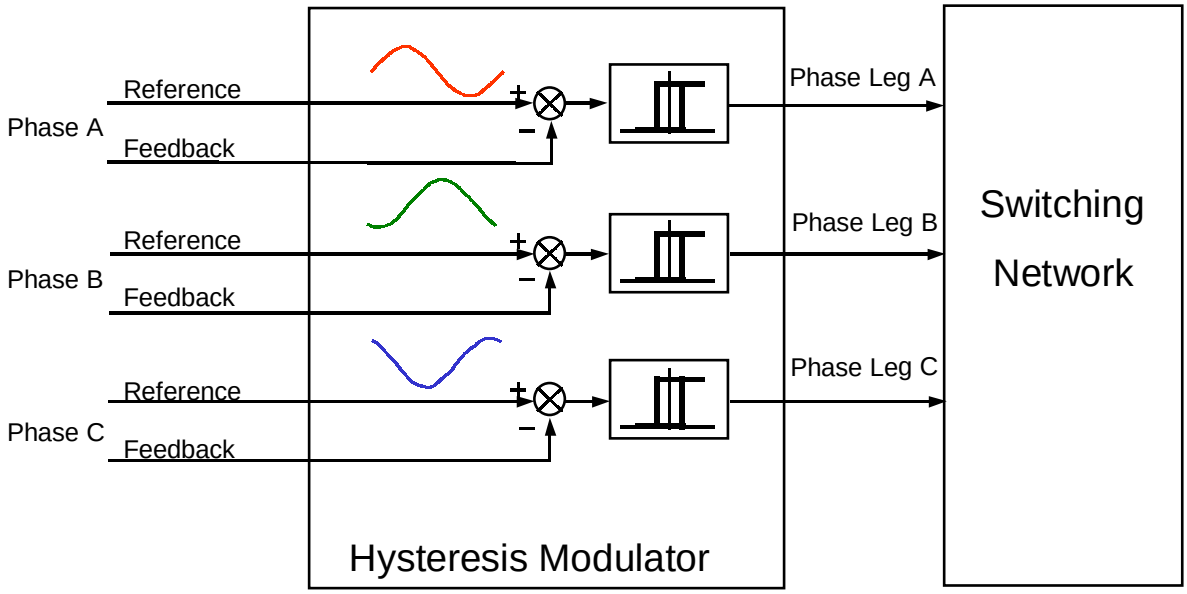


Figure 3-6 Block diagram of space vector modulator

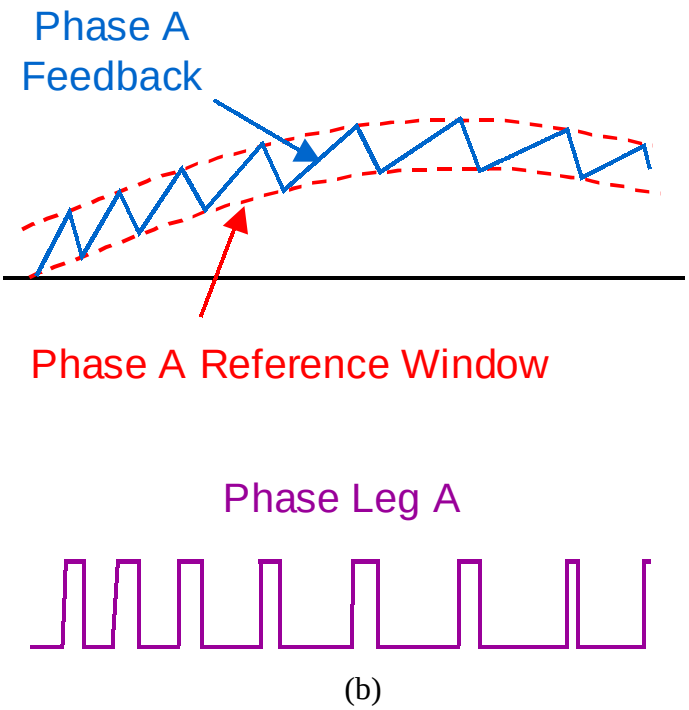
Another Bang-Bang type of modulation scheme worth mentioning is delta modulator [B28], as shown in Figure 3-8. A delta modulator is a zero hysteresis and regular sampled modulator. Delta modulators share the same advantages and disadvantages as the hysteresis modulator. The difference is that it is compatible with the digital controller due to its requirement for regular sampling. Another important fact is that the delta modulator is deemed the most natural PWM scheme for a particular family of soft-switching power converters — resonant DC link converters [B29-31]. When applied to a resonant DC link converter, the difference of the modulator is that the zero-order-hold (ZOH) is changed to the resonant-pulse-hold (RPH) [B31]. In this case, the delta modulator can hardly be called as a pulse width modulator. It is more appropriate to call it a pulse density modulator (PDM).

3.2.2.5 Random PWM Technique

Random PWM technique itself is not a PWM scheme. Rather it is a concept which can be applied to other PWM schemes. There are different versions of random PWM techniques. They all aim at alleviating the EMI problem and reducing the acoustic noise and vibrations for motor drive applications [B33-35]. All three of these problems are associated with distinct harmonic components. By randomly changing the switching frequency and/or location of the pulses, even though the total energy of harmonic components remain unchanged, the energy spreads out over a wide frequency range with a much reduced magnitude for each individual harmonic component. Random PWM may result in a higher output voltage/current distortion.



(a)



(b)

Figure 3-7 Three-phase hysteresis modulator

(a) block diagram (b) operation principle

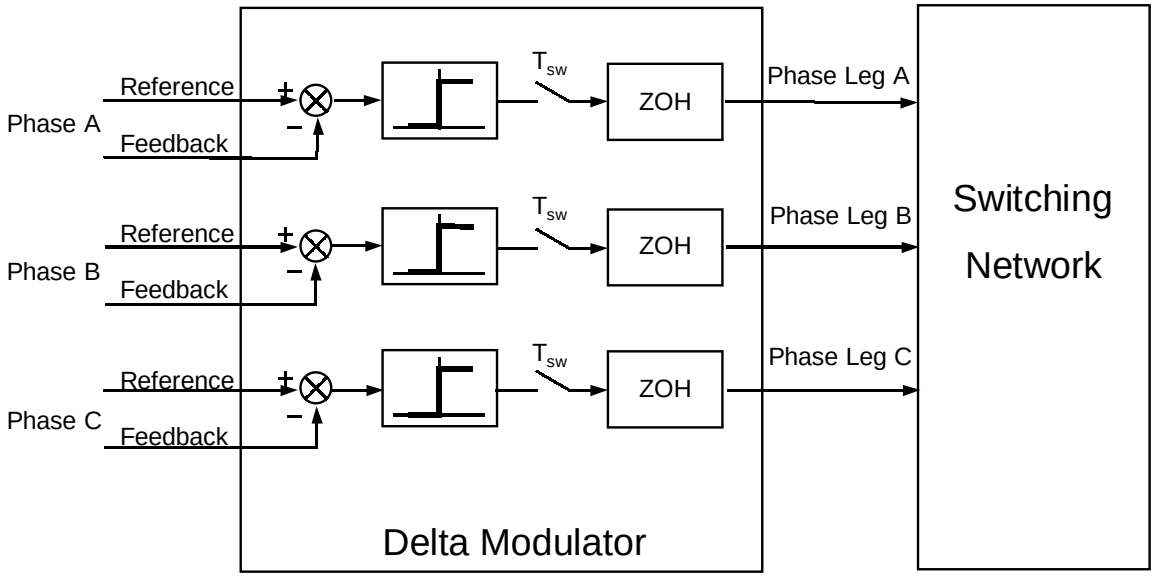


Figure 3-8 Block diagram of three-phase delta modulator

3.2.3 Two-Dimensional Space Vector Modulation

3.2.3.1 Two-Dimensional Space Vector

A. Definition

For any balanced three-phase variables, X_a, X_b, X_c, where X may be voltage or current, there is a relationship

(3.2) $$X_a + X_b + X_c = 0$$

The above equation suggests that the three variables could be mapped into a vector $\mathbb{X}$ on the orthogonal α–β plane, where

(3.3) $$\mathbb{X} = X_\alpha + jX_\beta$$

The transformation for this orthogonal coordinate mapping, sometimes called 3/2 transformation, is expressed as

(3.4) $$[X_\alpha \; X_\beta]^T = T \cdot [\, X_a \; X_b \; X_c \,]^T,$$

where T_1 is the transformation matrix and is expressed as

(3.5) $$T_1 = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$$

B. Switching Vectors

The switching network shown in Figure 3-2 has a total of eight possible switching combinations. Each switching combination is shown in Figure 3-9, and is given a name according to the phase leg connection, where ‘p’ denotes that phase leg is connected to the positive rail of the DC link, and ‘n’ denotes that phase leg is connected to the negative rail of the DC link. For example, switching combination ‘pnn’ represents the condition

where the phase A output terminal V_a is connected to the positive DC rail, and phase B and C output terminals V_b and V_c are connected to the negative DC rail.

Each switching combination results in a set of three phase voltages at the AC terminal of the switching network. A total of eight vectors are obtained by transforming the three-phase voltages into the α–β orthogonal coordinate using (3.3) ~ (3.5). Those eight vectors are called switching vectors.

There are two type of three-phase voltages that can be used for the coordinate transformation to get the switching vectors, three-phase line-to-neutral voltage and line-to-line voltage.

When using the line-to-neutral voltage, the middle point of the DC link is used as the reference neutral point V_n, as shown in Figure 3-10(a). The three-phase voltage used for the coordinate transformation would be $[V_{an} \quad V_{bn} \quad V_{cn}]^T$. Notice that (3.2) is not satisfied in this case. In fact, [B15] shows that the switching vector would be in a three-dimensional space and form a cube. It is advantageous to use the line-to-neutral voltage in cases where the neutral point potential is of interest, for example, when the neutral fluctuating problem is investigated [B18]. However, since all the input and output are balanced three-phase, the modulation is performed in the two-dimensional α–β plane and the third dimension is of no use for the modulation purpose. Therefore, all the switching vectors have to be projected on the α–β plane. This indirectness with the line-to-neutral voltage can be avoided if three-phase line-to-line voltage is used.

The line-to-line voltage $[V_{ab} \quad V_{bc} \quad V_{ca}]^T$ used for the transformation is shown in Figure 3-10(b). Since it satisfies (3.2), two-dimensional switching vectors can be obtained directly after the transformation. Figure 3-11 shows the positions of all the switching vectors using the three-phase line-to-line voltage. Each vector has a length of $\frac{2}{\sqrt{3}} V_g$. A hexagon can be seen by connecting the end point of all the non-zero vectors. The hexagon defines the controllable region. It can be further divided into six sectors denoted as I through VI. Each sector contains 60-degree region, as can be seen in

Figure 3-11. The inscribed circle of the hexagon is the maximum balanced three-phase sinusoidal output. The radius of the inscribed circle equals one, indicating that the maximum modulation index is one.

C. Reference Vector

A reference vector V_{ref} can be obtained by transforming the reference three-phase voltage into the α–β plane, as shown in Figure 3-11. Under steady state conditions, to get a balanced three-phase sinusoidal, the reference vector is rotating in the α–β plane. The trajectory of the reference vector V_{ref} draws a circle. The radius of the circle is less than or equal to one. During transient, when the reference vector V_{ref} points outside the hexagon, the actual attainable reference vector falls on and slides along the boundary of the hexagon.

3.2.3.2 Synthesis of the Reference Vector

In the space vector representation, the modulation scheme is turned into a problem of synthesizing the reference vector using the switching vectors. It can be divided into the following steps:

A. Selection of Switching Vectors

Given a reference vector, as shown in Figure 3-11, there are numerous ways to synthesize it using different vectors. For example, it can be synthesized using $\mathbb{V}_1$, $\mathbb{V}_2$, and $\mathbb{V}_{Z1}$ and/or $\mathbb{V}_{Z2}$; or using $\mathbb{V}_1$, $\mathbb{V}_2$, and $\mathbb{V}_4$. It is proven that by using the adjacent non-zero vectors, which defines each sector, and the zero vectors, the circulating energy is minimized. The current ripple and harmonic contents would also be reduced. Therefore, this is the most favorable way to select the switching vectors. It is sometimes called six-step space vector modulation. However, non-six-step space vector modulations are also useful for transient in that a faster regulation can be achieved, and for some special cases where zero vectors cannot be used [B19] [D1].

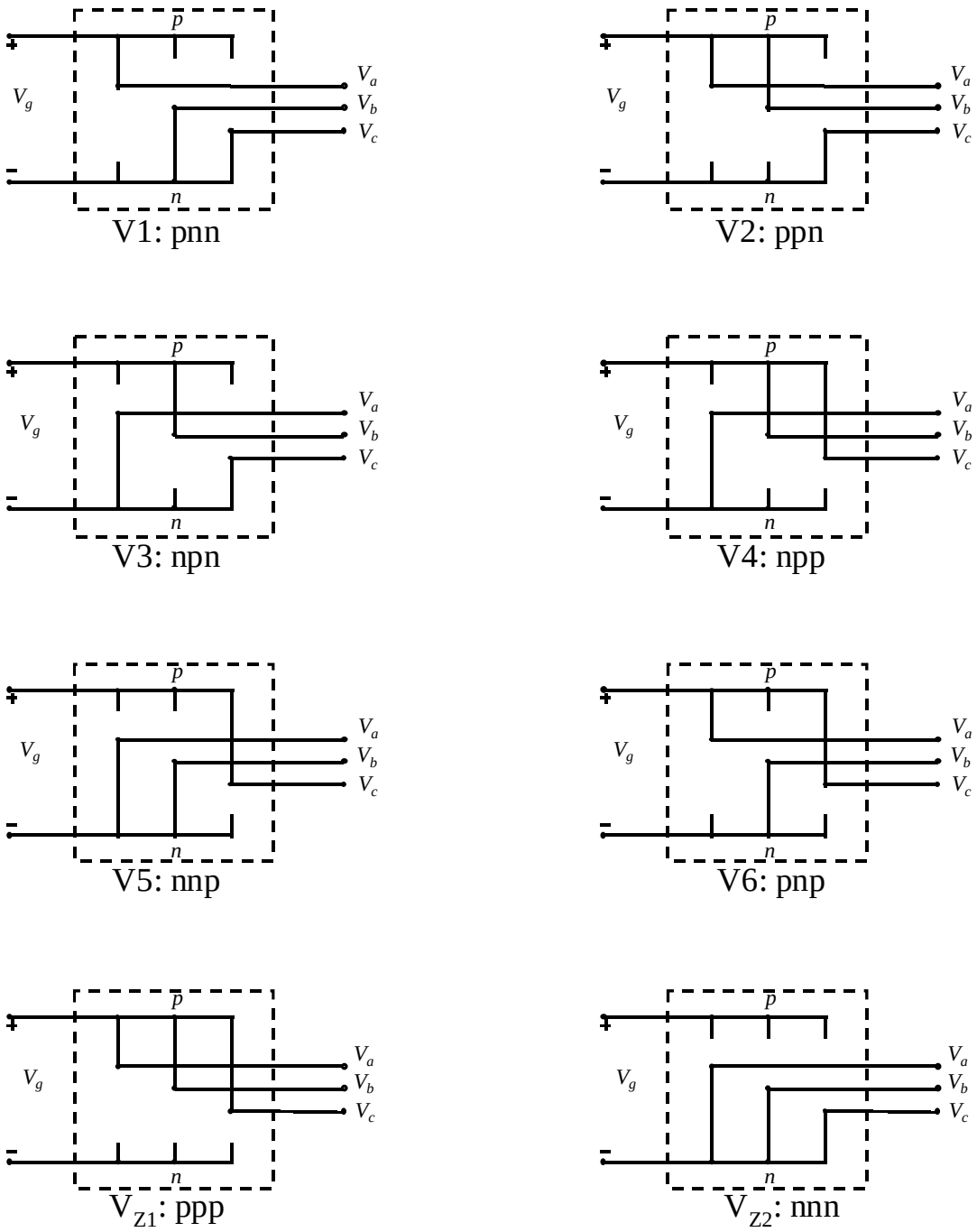
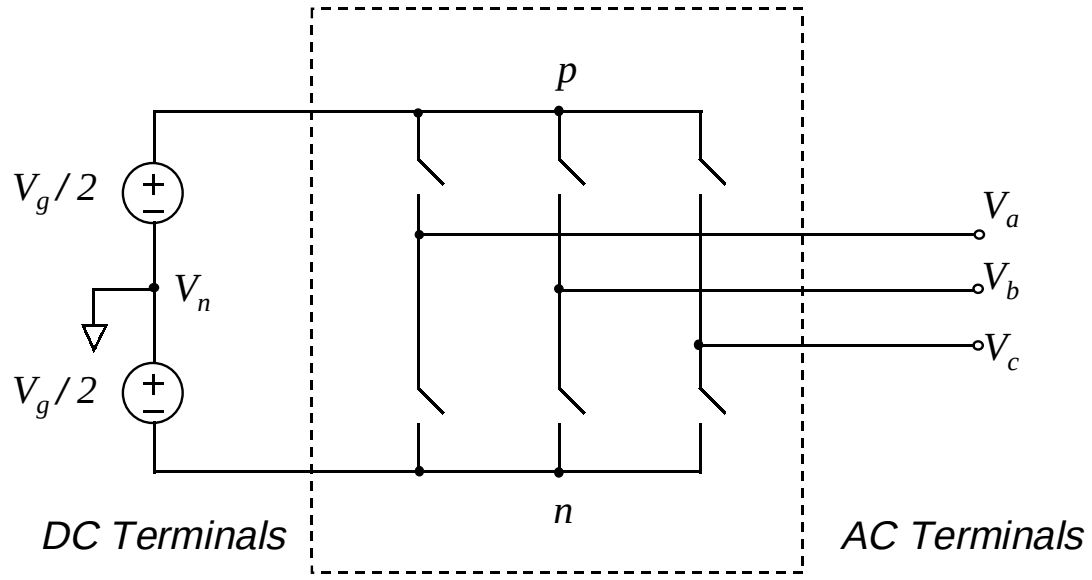
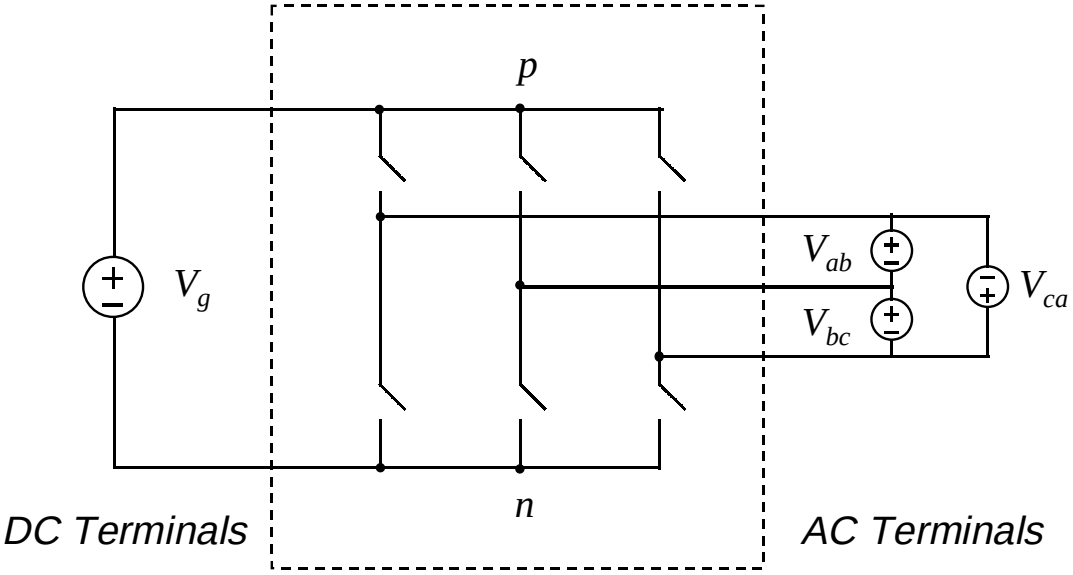


Figure 3-9 Possible switching combinations of a three-legged switching network



(a)



(b)

Figure 3-10 AC terminal voltage used for coordinate transformation

(a) three-phase phase-to-neutral voltage; (b) three-phase line-to-line voltage

B. Projection of the Reference Vector

Figure 3-12 shows one example of synthesis of the reference vector $\mathbb{V}_{ref}$ in sector I. Non-zero vectors $\mathbb{V}_1$, $\mathbb{V}_2$, and zero vectors and $\mathbb{V}_{Z1}$ and/or $\mathbb{V}_{Z2}$ are selected. Since the zero vector does not have a contribution to the position of the reference vector. Therefore, the reference vector $\mathbb{V}_{ref}$ can be projected onto the two non-zero vectors. The projection can be expressed as

(3.6) $$\mathbb{V}_{ref} = d_1 \cdot \mathbb{V}_1 + d_2 \cdot \mathbb{V}_2,$$

d_1 and d_2 are duty ratios for the non-zero vectors correspondingly. They can be calculated by simple geometric algorithm, as shown below,

(3.7) $$\begin{bmatrix} d_1 \\ d_2 \end{bmatrix} = \frac{V_m}{V_g} \begin{bmatrix} \sin(\frac{\pi}{3} - \theta) \\ \sin(\theta) \end{bmatrix},$$

where V_m is the length of the reference vector $\mathbb{V}_{ref}$, and θ is the angle between $\mathbb{V}_1$ and $\mathbb{V}_{ref}$, as shown in Figure 3-12. The rest of the time within this switching period will be occupied by the zero vectors. The duty ratio for the zero vector d_Z can then be given as,

(3.8) $$d_Z = 1 - d_1 - d_2 = 1 - \frac{V_m}{V_g} \cos(\frac{\pi}{6} - \theta)$$

There are two zero switching vectors, namely ppp and nnn, available. Either one of them or both of them can be used. The selection of the zero switching vectors is related to the sequencing of the non-zero vectors discussed next.

C. Sequencing of Switching Vectors

After selecting the switching vectors and knowing their duty ratios, the next step is to sequence them. Obviously there are infinite options to sequence the selected switching vectors. Although the sequence of the switching vectors does not change the

average vector within a switching period, it has a great impact on the power losses and harmonic contents [B10-13][B15][B17][B20]. The sequencing schemes may be summarized by two classes. Class I sequencing schemes use both of the zero switching vectors ppp and nnn. Class II sequencing schemes use only one of the zero switching vectors, either ppp or nnn. Class I schemes include four sequencing schemes, namely rising-edge aligned SVM, falling-edge aligned SVM, symmetrical SVM, and alternative sequence SVM. For each of the class I schemes, there is a counterpart in class II. Examples of the class I sequencing schemes for a reference vector located in sector I are shown in Figure 3-13. Control signals for each phase leg in the switching network are given for two consecutive switching periods. Unless specially denoted, the sequence pattern will repeat for the second switching period.

There are a total of six switching actions within one switching period for the rising-edge aligned [C3], falling-edge aligned [B8], and the symmetric aligned [B5] sequencing schemes. The switching losses associated are about the same for these three sequencing schemes. The rising-edge and falling-edge aligned sequencing schemes align all the n to p transitions or p to n transitions, respectively. They are suitable for soft-switching converters [C1-3], where the alignment of all the turn-on or turn-off transitions reduces the number of interventions of the soft-switching network, and thus, simplifies the circuit. The symmetric aligned sequencing scheme gives the lowest output distortion and harmonic spectrum in all four sequencing schemes. The alternative sequence scheme [B4][B11] applies the non-zero switching vectors in an alternative way, e.g. $|\mathbb{V}_1\ \mathbb{V}_2|\mathbb{V}_2\ \mathbb{V}_1|$. It yields the lowest switching losses among all class I sequencing schemes in that the total switching actions are reduced to three—half of the other schemes. However, since the alternative sequence repeats its pattern every two switching periods, it yields a large harmonic content at the half of the switching frequency. It can be seen that there is always a trade-off between the losses and the harmonic contents.

For high power applications, power losses are of great interest. Studies [B10-12] [B17] have shown that the switching losses can be minimized by not switching the phase carrying the highest current. All the proposed minimum loss sequencing schemes fall into the class II sequencing scheme. For example, the falling-edge aligned class II sequencing

scheme is proposed in [B11]; the symmetric aligned class II sequencing scheme is proposed in [B15]; the alternative sequence is proposed in [B12]. Compared with its class I counterpart, the class II sequencing schemes reduce the switching actions by 1/3, and save switching losses by 50% for a load with a unity power factor. The saving of the switching losses may vary with the load power factor [B10-11]. The harmonic contents using class II sequencing schemes are higher than its class I counterparts.

Different sequencing schemes result in different power losses and harmonic contents at a different modulation index and different load power factor. Overall, the symmetric aligned (class II) sequencing scheme is a good compromise between the reduction of power losses and reduction of distortion and harmonic contents.

It is possible to select the best sequencing schemes in a real time operation according to the modulation index and load condition [B15][B17]. The optimization may target a minimum power losses, or combination of power losses, harmonic distortion and modulation index by defining an objective function [B12]. On-line optimized sequencing scheme will give the best performance of the modulator in the global operation range.

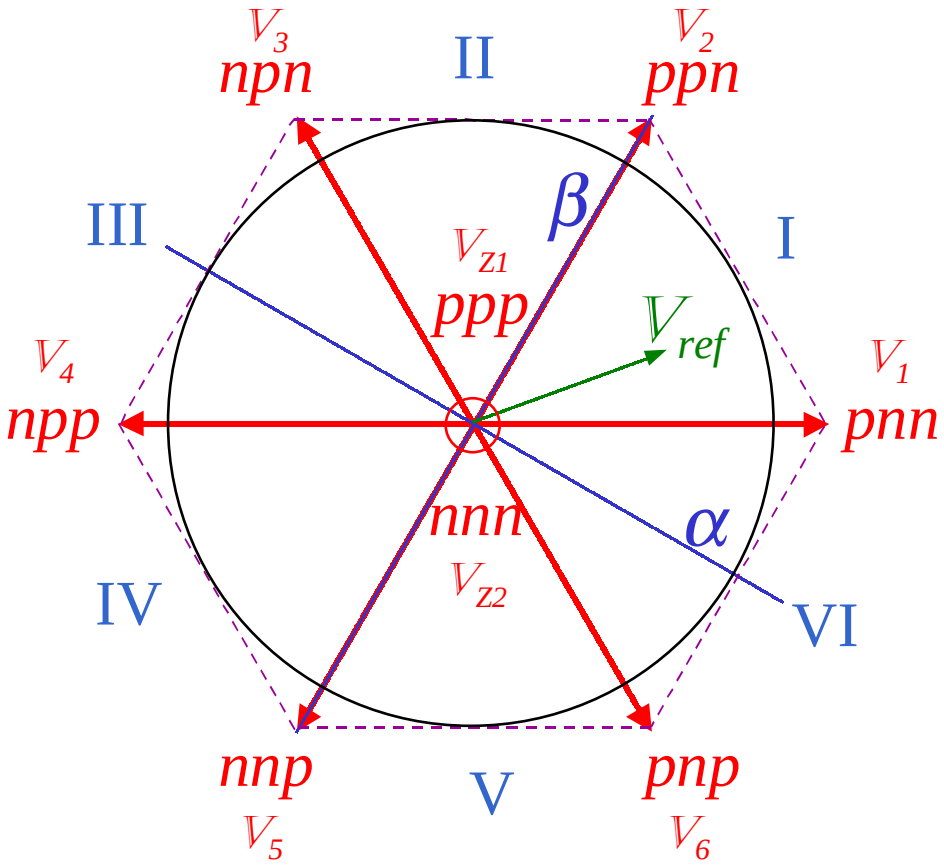


Figure 3-11 Switching vectors using line-to-line voltage

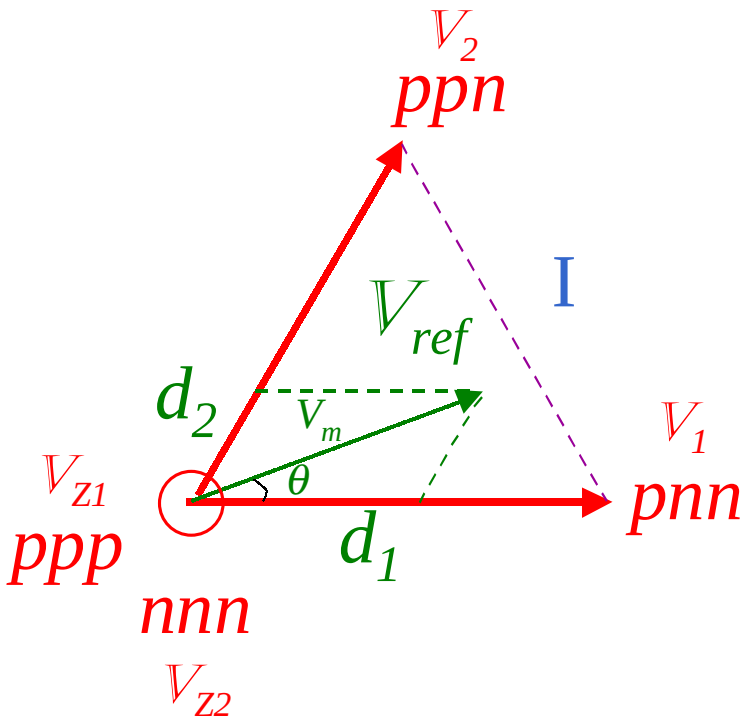
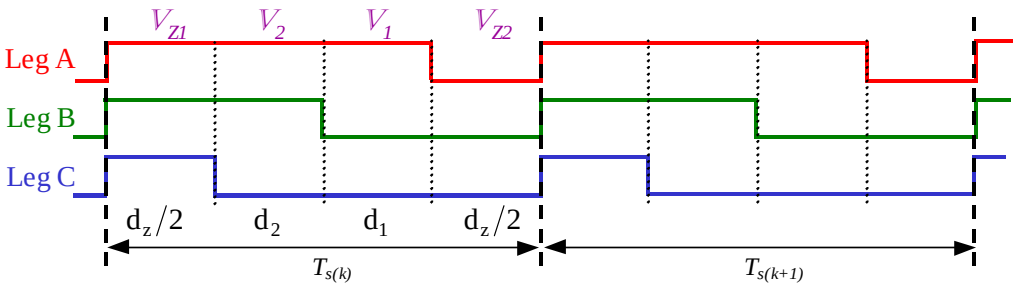
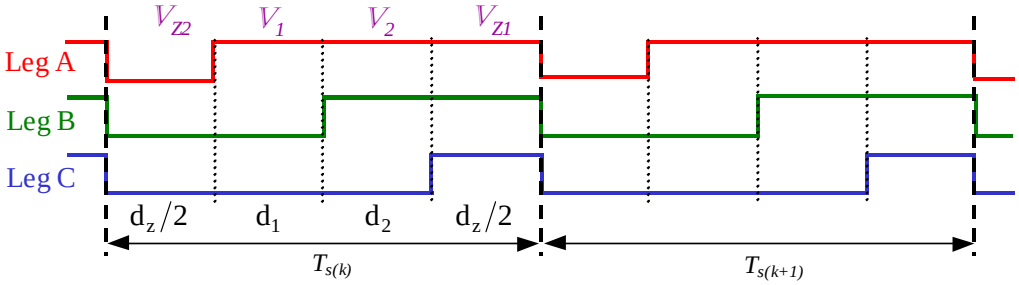


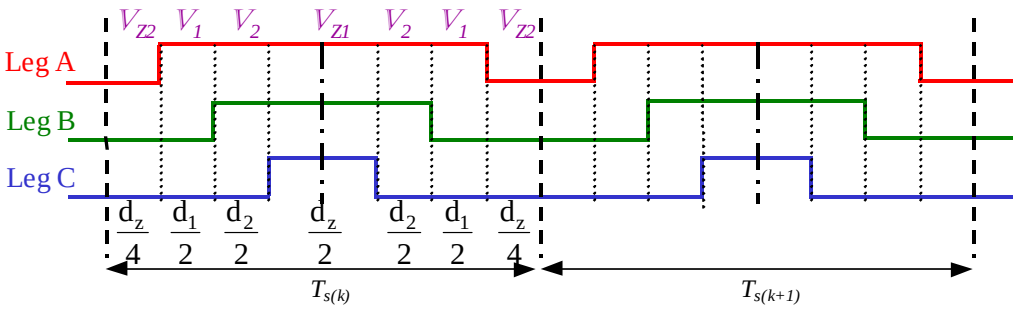
Figure 3-12 Example: synthesis of the reference vector in sector one



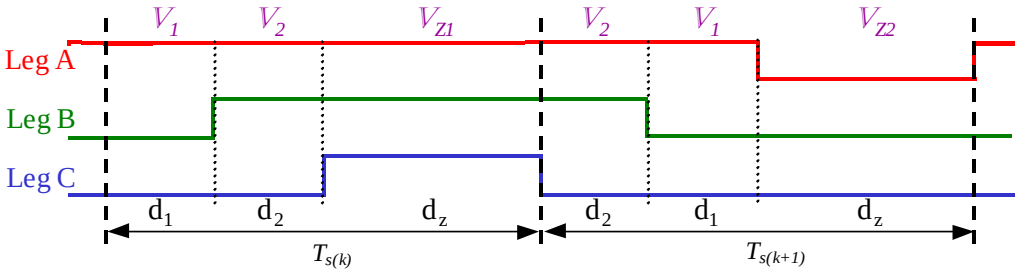
(a) Rising-Edge Aligned – Class I



(b) Falling-Edge Aligned – Class I

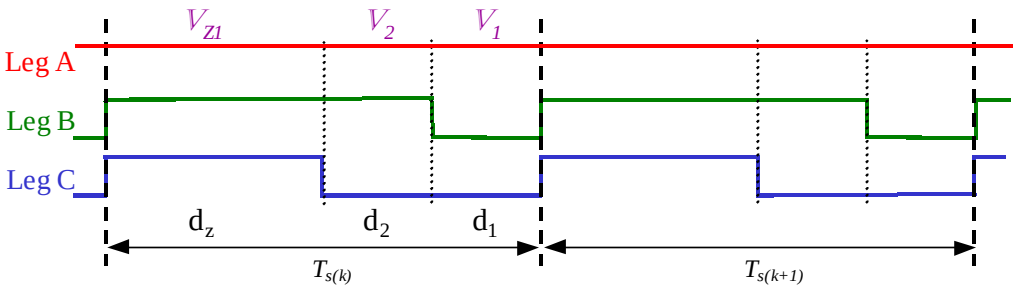


(c) Symmetric Aligned – Class I

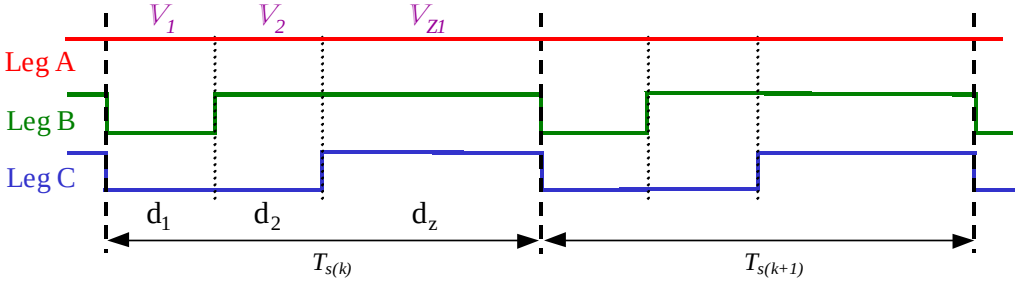


(d) Alternative Sequence – Class I

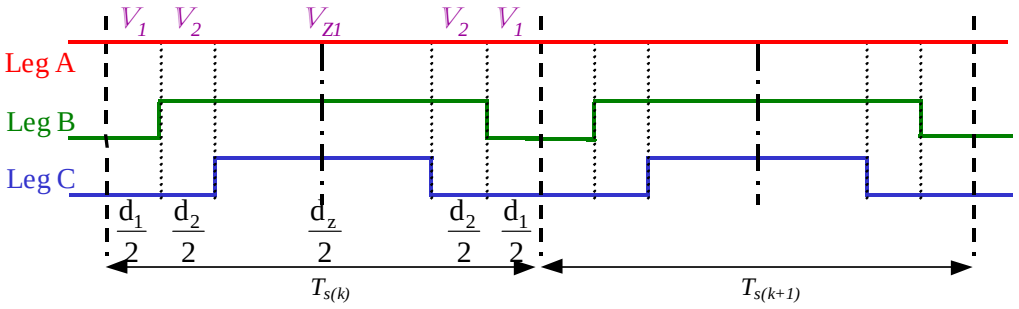
Figure 3-13 Class I sequencing schemes
(a) rising-edge aligned; (b) falling-edge aligned;
(c) symmetric aligned; (d) reverse-sequence



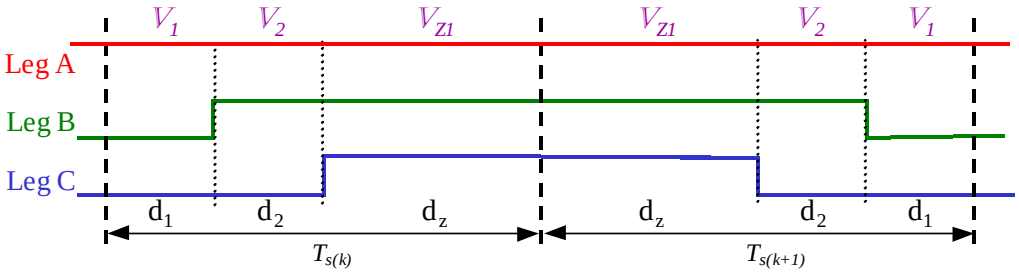
(a) Rising-Edge Aligned – Class II



(b) Falling-Edge Aligned – Class II



(c) Symmetric Aligned – Class II



(d) Alternative Sequence – Class II

Figure 3-14 Class II sequencing schemes

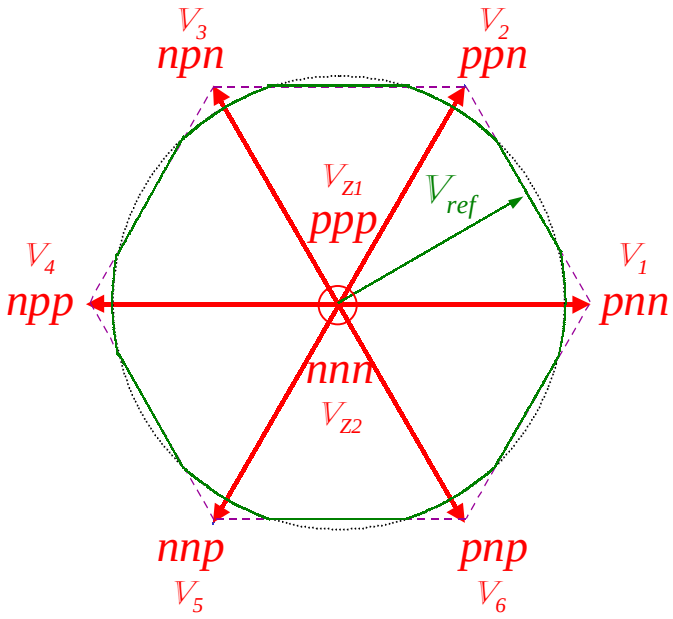
(a) rising-edge aligned; (b) falling-edge aligned;
(c) symmetric aligned; (d) reverse-sequence

3.2.3.3 Over-modulation

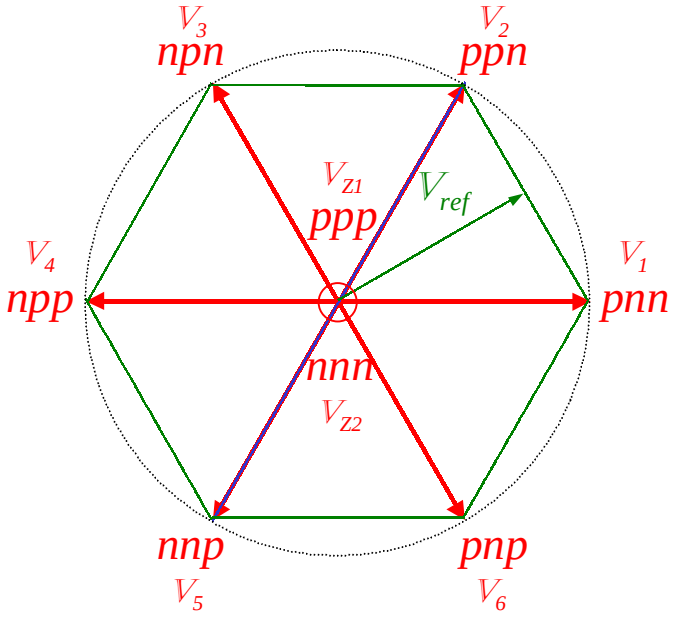
Over-modulation [B9] is a special mode for modulation index larger than one. With over-modulation, the magnitude of the fundamental output voltage can be higher at the price of a much larger distortion. It is useful for two cases: (1) to boost the output voltage, and (2) for transient when the reference vector is located outside the hexagon. When the reference vector points outside the hexagon, using (3.6) through (3.8) would result in meaningless negative duty ratios. Since the actual attainable reference vector is within the hexagon, whenever the reference vector points outside the hexagon, it is necessary to modify the reference vector to sit on the boundary.

There are two operational modes for over-modulation: (1) for modulation index M within the [1, $\frac{2}{\sqrt{3}}$] range, part of the intended reference vector, as shown in a dotted circle in Figure 3-15(a), is within the hexagon, and the rest of it is outside the hexagon. The outcome of over-modulation strategy for this modulation range is shown in a solid line in Figure 3-15(a); (2) for modulation index M greater than $\frac{2}{\sqrt{3}}$, all the intended reference vectors, as shown in a dotted circle in Figure 3-15(b), are outside the hexagon. The outcome of over-modulation strategy for this modulation index range is that the actual reference vector slides along the boundary of the hexagon, as shown in a solid line in Figure 3-15(b).

The over-modulation strategy has the behavior of a limiter. Unlike a commonly used single input limiter, the boundary of the limiter has two inputs, and is defined as a hexagon in a two-dimensional plane.



(a)



(b)

Figure 3-15 Over-modulation

(a) modulation index M = [1, $\frac{2}{\sqrt{3}}$] (b) modulation index ≥ $\frac{2}{\sqrt{3}}$

3.2.4 Three-Legged Power Converter with Unbalanced Load/Source

3.2.4.1 Three-Legged VSI with Unbalanced Load

For a three-phase three-wire system, due to the topology constraint, the sum of the three phase currents is zero, thus, there is no zero-sequence current. Only the positive-sequence and negative sequence exist in the system.

For a three-phase four-wire system, a neutral point needs to be provided. If the load is balanced, the neutral point could be floating since there is no current going through it. However, if the load is unbalanced, a floating neutral makes an inherent unbalanced three-phase output voltage because the control target of a balanced three-phase voltage contradicts with the fact that the zero-sequence current cannot exist due to the topology constraint. In order to make the control target achievable, a neutral must be provided so that the zero-sequence can flow through.

There are several passive methods to provide the neutral connection for unbalanced loads. A zero-sequence trap [A1] is a Δ/Y transformer. Connecting the Δ windings to the inverter and the Y windings to the load, the zero-sequence current caused by the load is trapped into the Δ windings. Circulating within the transformer winding, it is prevented from traveling back to the inverter and the DC link. Another passive way to provide the neutral connection is to use a zig-zag transformer. The zero-sequence currents from each phase are shifted at different phase angle, and thus can be canceled with each other. All the passive approaches suffer from bulky reactive components.

Another simple approach to provide the neutral point is to use two capacitors to split the DC link and tie the neutral point to the mid-point of the two capacitors, as shown in Figure 3-16. The split capacitor approach suffers greatly in two aspects: (1) insufficient DC link voltage utilization; and (2) huge capacitance needed to maintain the DC link voltage ripple at 2ω frequency.

A. Insufficient DC Link Voltage Utilization

With the split DC link capacitors, the three-phase inverter becomes three single-phase half-bridge inverters in that the three phases are fully decoupled and independently controlled. Using phase leg A as an example, whenever the upper switch turns on, the AC terminal voltage $V_{an} = \frac{V_g}{2}$; and whenever the bottom switch turns on, the AC terminal voltage $V_{an} = -\frac{V_g}{2}$. In one switching period, the average voltage of V_{an} would be:

(3.9) $$\overline{V}_{an} = d_a \frac{V_g}{2} - (1 - d_a)\frac{V_g}{2} = V_g(d_a - 1)$$

where d_a is the duty ratio of the phase leg A ranging from [0, 1].

The control target is

(3.10) $$V_{an\_ref} = \frac{V_{ll\_pk}}{\sqrt{3}}\sin(\omega t)$$

where V_{ll_pk} is the line-to-line peak voltage. Equating (3.9) and (3.10) yields the steady state solution for phase leg A duty ratio d_a expressed as,

(3.11) $$d_a = \frac{V_{ll\_pk}}{\sqrt{3}V_g}\sin(\omega t) + \frac{1}{2} = \frac{M}{\sqrt{3}}\sin(\omega t) + \frac{1}{2}$$

Considering that d_a is within [0, 1], from (3.11) the maximum modulation index M_{max} can be found as,

(3.12) $$M_{max} = \frac{\sqrt{3}}{2}$$

This indicates that the DC link voltage utilization is more than 15% less than would be achieved otherwise with a three-legged power converter with a two-dimensional space vector modulation.

B. Huge DC Link Capacitance Needed

When the three-phase load is balanced, there will be no ripple power drawn from the DC link, nor will the neutral current flow into the split capacitors. Ideally, there is no voltage ripple across the DC link capacitors. The DC link capacitance could be minimized and, is determined mainly by the hold-up time requirement. However, when the load is unbalanced, the voltage across the DC link capacitors will have not only the 2ω ripple due to the negative-sequence load current, but also a ripple at the fundamental line frequency ω due to the zero-sequence load current. Given a requirement of maximum allowed magnitude of the DC link capacitor voltage ripple, ΔV_g, the minimum DC link capacitance needed to handle the negative-sequence load current $C_{dc\_min\_n}$ is given by (3.13); the minimum DC link capacitance needed to handle the zero-sequence load current (neutral current) $C_{dc\_min\_o}$ is given by (3.14).

(3.13)
$$C_{dc\_min\_n} = \frac{\sqrt{3}}{4} \frac{MI_n}{\omega \cdot \Delta V_g}$$

where M is the modulation index, and I_n is the peak of the negative-sequence load current.

(3.14)
$$C_{dc\_min\_o} = \frac{I_0}{2 \cdot \omega \cdot \Delta V_g}$$

where I_0 is the peak of the zero-sequence load current. The derivations of (3.13) and (3.14) are given in Appendix A.

Since balanced single-phase nonlinear loads also contribute a lot to the neutral current, it is normally requires much more capacitance to handle the zero-sequence load current going through the neutral, simply because the zero-sequence load current has a lower frequency and/or higher amplitude than the negative-sequence load current. In the practical design described next, it can be seen that $C_{dc\_min\_0}$ is four times larger than $C_{dc\_min\_n}$. The cost increase for the DC link capacitors is tremendous due to the neutral current, especially for high voltage applications.

3.2.4.2 Three-Legged PWM Rectifier with Unbalanced Source

An unbalanced three-phase voltage source may be found in the following situations: (1) a weak utility line with an unbalanced three-phase load; (2) large single-phase load in the AC system; and (3) unsymmetrical transmission impedance. An unbalanced source can cause two problems: (1) large DC link voltage ripple; and (2) deteriorated PWM rectifier performance. The negative-sequence source voltage will cause a negative-sequence input AC current, which will in turn cause the large DC link voltage ripple. A large DC link voltage may greatly degrade the performance of the downstream power converter or even cause a stability problem. The unbalanced source and the large DC link voltage ripple also cause a heavily distorted input AC current, as shown in Figure 3-17 [F4].

Several feedforward control methods have been proposed [F1-3]. They aim at a DC link voltage free of ripple using the ‘constant power’ control strategy, which is beneficial from the downstream load point of view. However, in order to achieve this, a counter-balance negative-sequence current has to be injected by modifying the control signals. The consequence is that more current would be drawn from a weaker phase. That makes the source unbalance condition even worse. From the source point of view, it makes sense to make the source see a balanced pure resistive load. That means less current drawn from a weaker phase. A neutral current would incur with this control strategy. The split DC link capacitor method can also be used for the rectifier to handle this neutral current. It suffers from the same problems that have been pointed out for the inverter. With the ‘equal resistance’ control strategy, the DC link voltage will suffer from large ripple because of this control strategy. There is no easy trade-off between these two balancing schemes. It depends on the real application to figure out which one is more important.

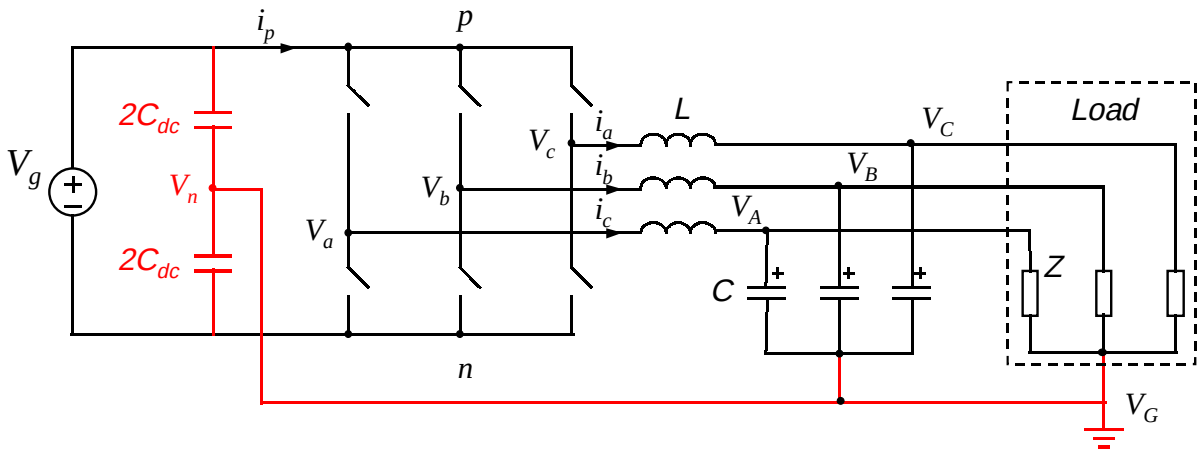


Figure 3-16 Split DC link capacitor method to provide the neutral point

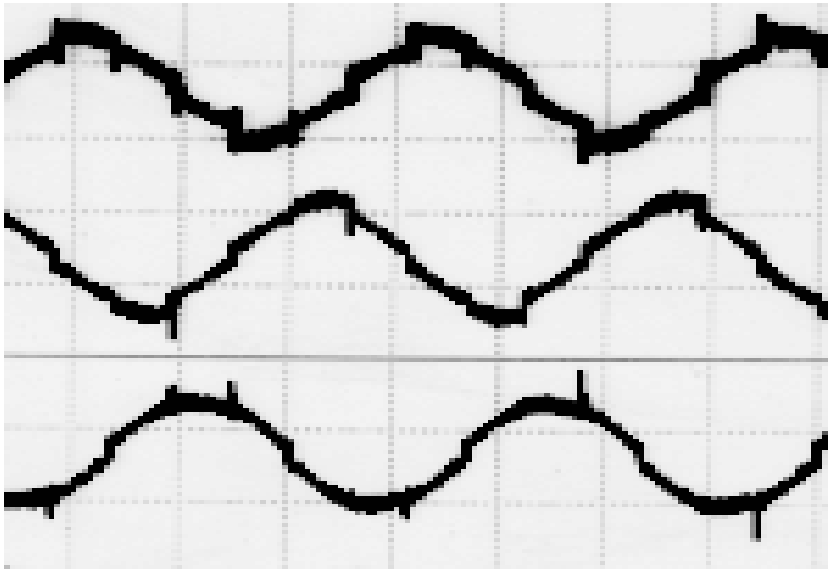


Figure 3-17 Input currents of a three-legged PWM rectifier with an unbalanced source

3.3 Four-Legged PWM Power Converters

In the past, four-legged power converters have been used for different purposes. [E2] proposed to using an additional fourth leg to assist commutation for a current-fed thyristor inverter. [E3] described an approach to eliminate the common-mode voltage for a three-phase voltage-fed converter using the fourth leg and special SVM scheme. [E1] presented a four-legged resonant DC link (RDCL) inverter to handle the neutral current for unbalanced loads. The power density modulation (PDM) or delta modulation scheme is used to control this four-legged inverter with reasons discussed in Section 3.2.2.4. The four-legged RDCL inverter proposed in [E1] has the following disadvantages: (1) high DC link voltage stress, thus, not suitable for high voltage (480 V line-to-line) applications; (2) high output voltage distortion due to PDM, thus, not suitable for high performance applications; and (3) load sensitive. The DC link voltage changes with the load current. Therefore, the dynamic performance suffers when load transient happens frequently. To overcome the drawbacks mentioned above, this dissertation proposes four-legged PWM power converters, including four-legged PWM inverter and four-legged PWM rectifier, with space vector modulation control.

By replacing the three-legged switching network with a four-legged switching network, as shown in Figure 3-18, four-legged power converters are obtained. By tying the load neutral point to the mid-point of the fourth leg, the four-legged PWM inverter, as shown in Figure 3-20, can handle the neutral current caused by an unbalanced load or balanced single-phase nonlinear loads. A balanced output voltage can be achieved due to the tightly regulated neutral point. The additional neutral inductor L_n is optional. It can reduce switching frequency ripple.

By adding the fourth leg to a three-legged PWM rectifier, as shown in Figure 3-20, under unbalanced source voltage, it is possible to control the input AC current proportional to the unbalanced voltage level so that the source sees equal resistors for all three phases. This is a more favorable operation condition to the unbalanced source. A four-legged PWM rectifier also provides the possibility of fault tolerant operation.

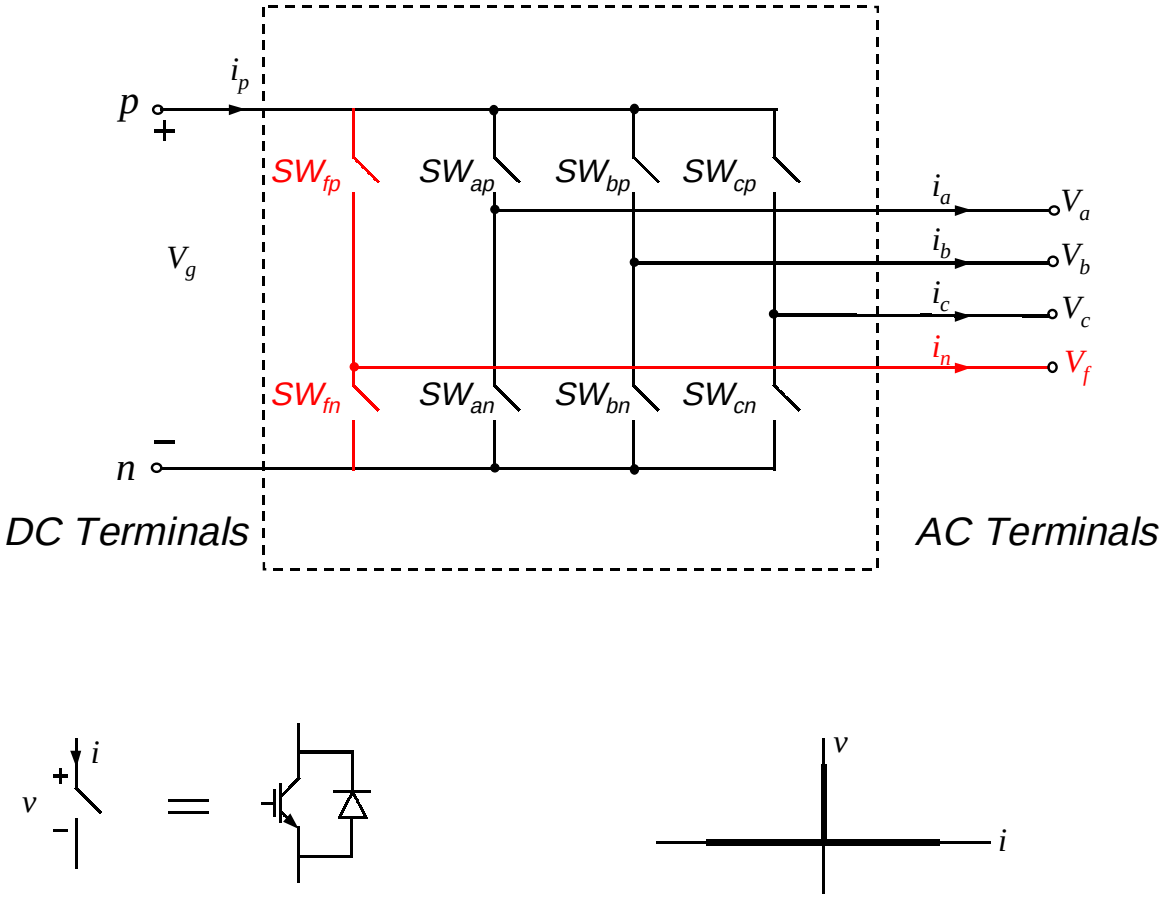


Figure 3-18 Four-legged switching network

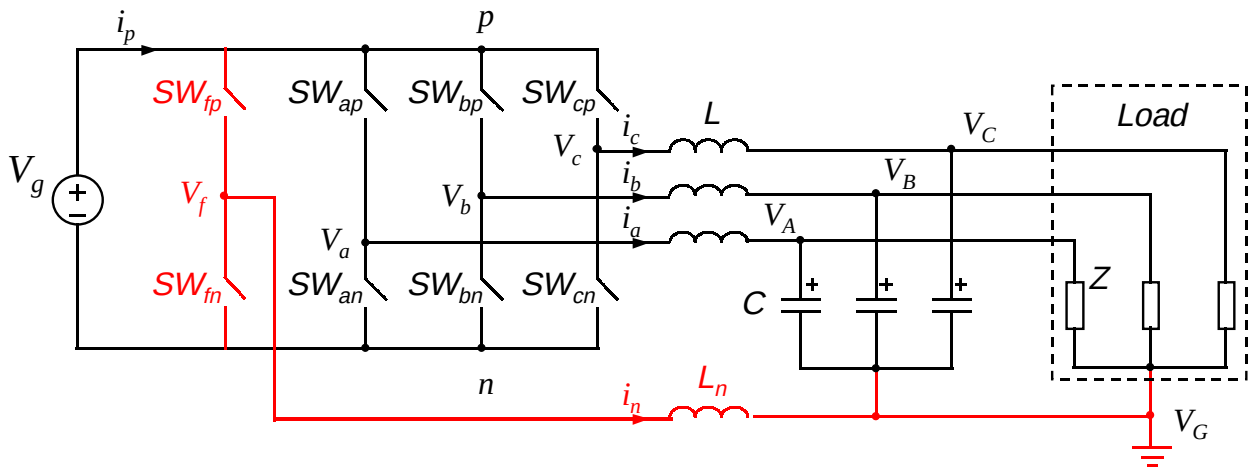


Figure 3-19 Four-legged voltage source inverter

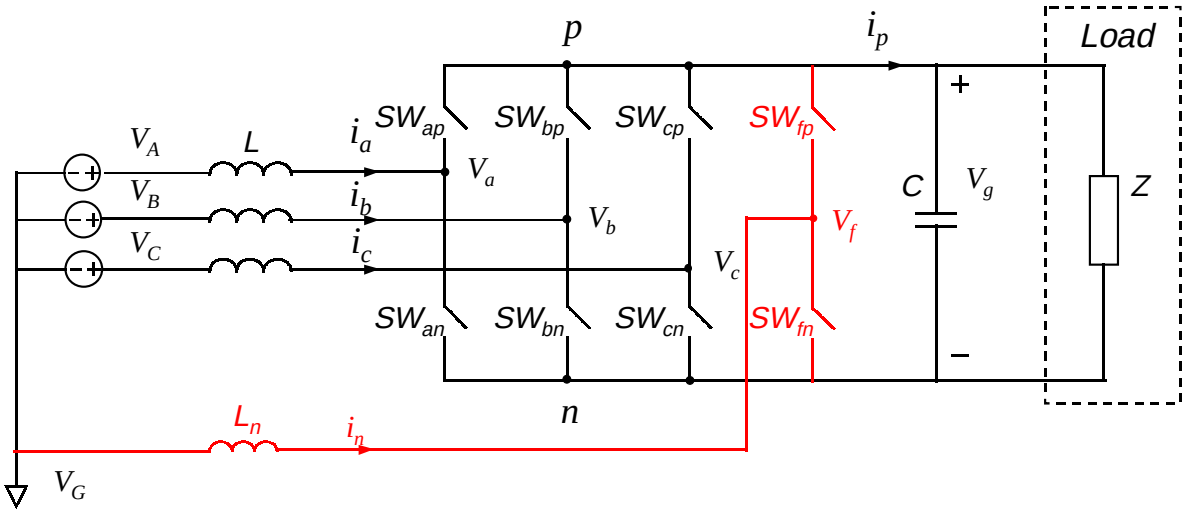


Figure 3-20 Four-legged PWM rectifier

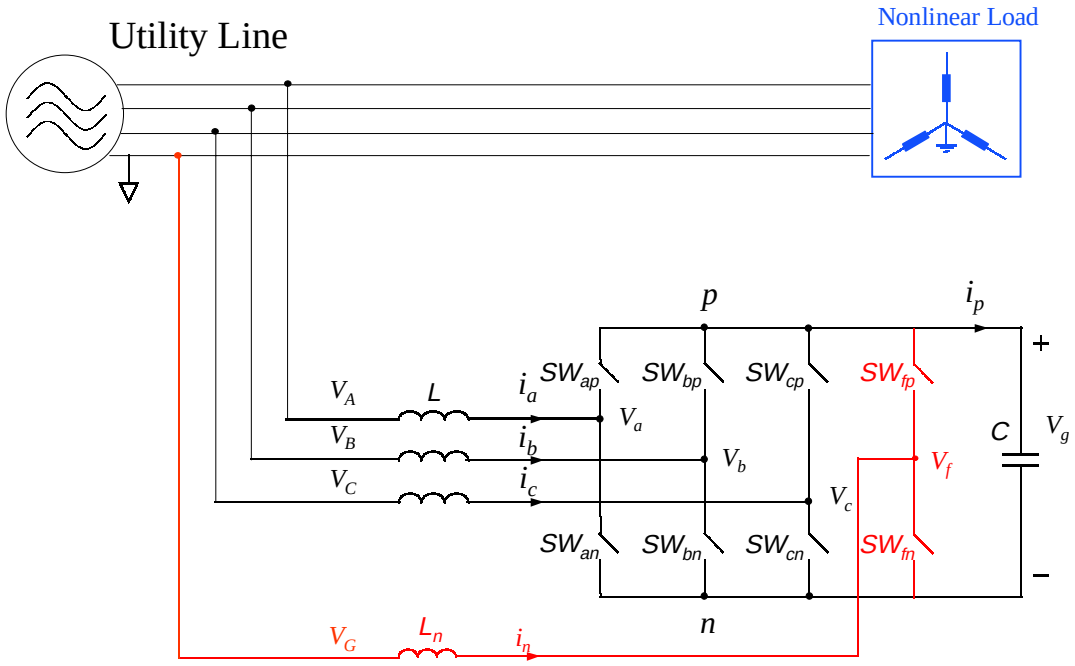


Figure 3-21 Four-legged active filter

Similarly the four-legged active filter, shown in Figure 3-21 can deal with the zero-sequence current in the transmission line. it is advantageous compared with the split DC link capacitor active filter due to higher DC link voltage utilization.

To describe the operation of the four-legged power converters, a switching function can be defined as

$$\mathbf{(3.15)} \qquad S_{jf} = \begin{cases} 1, & \text{If } S_{jp} \text{ and } S_{fn} \text{ are closed} \\ 0, & \text{If } S_{jp} \text{ and } S_{fp}, \text{or } S_{jp} \text{ and } S_{fp} \text{ are closed} \\ -1, & \text{If } S_{jn} \text{ and } S_{fp} \text{ are closed} \end{cases} \qquad j = \{a,b,c\}$$

Therefore, the AC terminal voltages will have

$$\mathbf{(3.16)} \qquad [V_{af} \quad V_{bf} \quad V_{cf}]^T = [S_{af} \quad S_{bf} \quad S_{cf}]^T \cdot V_{pn}$$

The DC terminal current i_p can be express as

$$\mathbf{(3.17)} \qquad i_p = [S_{af} \quad S_{bf} \quad S_{cf}] \cdot [i_a \quad i_b \quad i_c]^T$$

The AC terminal voltages V_{af}, V_{bf} and V_{cf} are pulsating voltages with a fixed switching period T_s. To get the averaged voltages over each switching period, the moving average operand can be applied to (3.16) and (3.17). The moving average operand applied to an arbitrary variable $X_{(t)}$ is expressed as

$$\mathbf{(3.18)} \qquad \overline{X}_{(t)} = \frac{1}{T_s} \int_{t-T_s}^{t} X_{(\tau)} d\tau$$

After the cycle-by-cycle averaging process, the averaged AC terminal voltages and the DC terminal current are expressed as

$$\left[\overline{V}_{af} \quad \overline{V}_{bf} \quad \overline{V}_{cf}\right]^T = \left[d_{af} \quad d_{bf} \quad d_{cf}\right]^T \cdot V_{pn} \qquad \textbf{(3.19)}$$

$$I_p = \left[d_{af} \quad d_{bf} \quad d_{cf}\right] \cdot \left[I_a \quad I_b \quad I_c\right]^T \qquad \textbf{(3.20)}$$

where d_{af}, d_{bf} and d_{cf} are line-to-neutral duty ratios. For the sake of simplicity, from this point on, the average value of a variable $\overline{X}$ will be simplified as X. A detailed discussion about the averaging process can be found in [I1].

The averaged large-signal model of the four-legged switching network is shown in Figure 3-22. Replacing the four-legged switching network with the averaged switching network, the large-signal average circuit model of the four-legged inverter and the four-legged PWM rectifier in the a-b-c coordinate can be found in Figure 3-23 and Figure 3-24, respectively. Unless specifically stated, the following analysis is concentrated on the four-legged inverter.

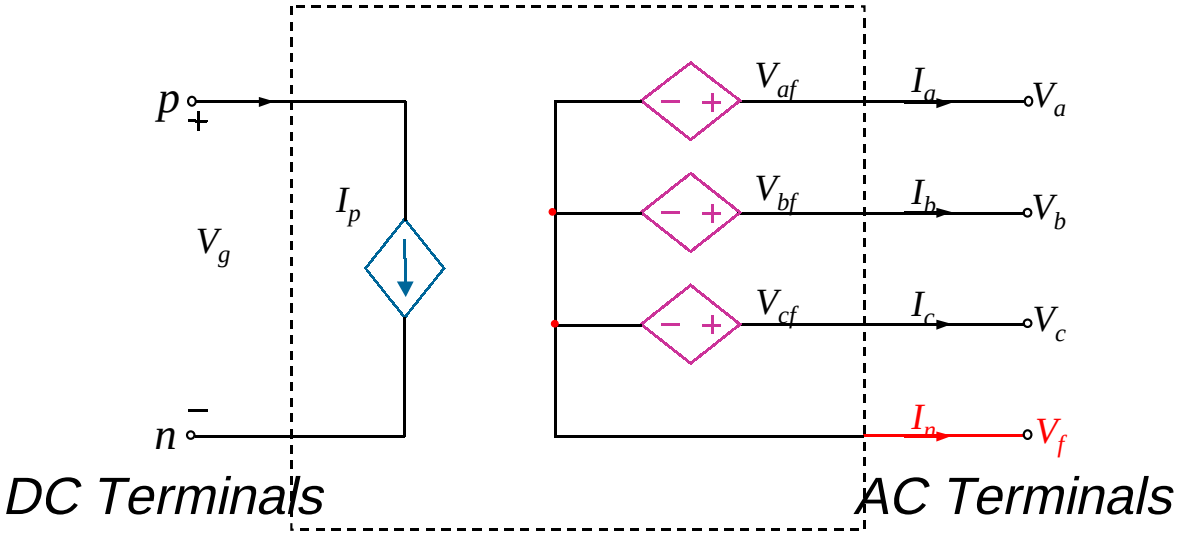


Figure 3-22 Average model of four-legged switching network

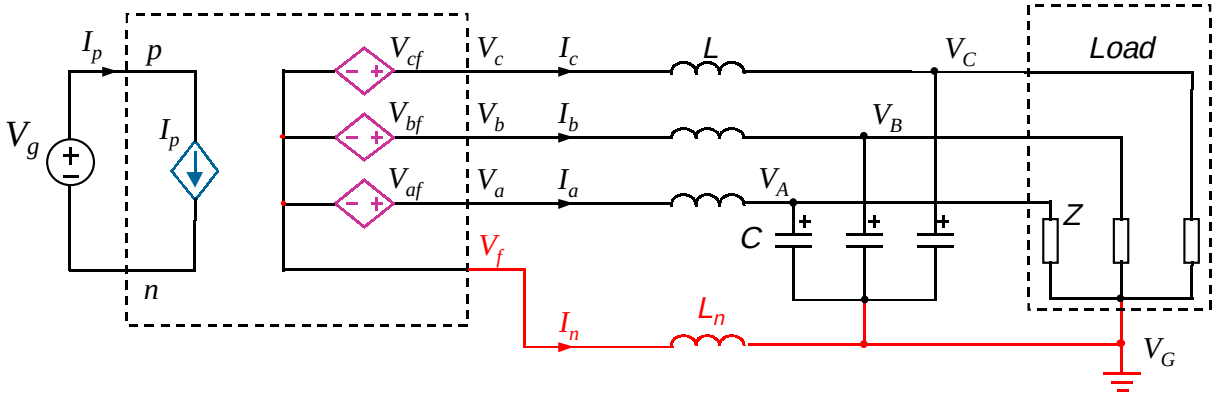


Figure 3-23 Average large-signal model of a four-legged inverter

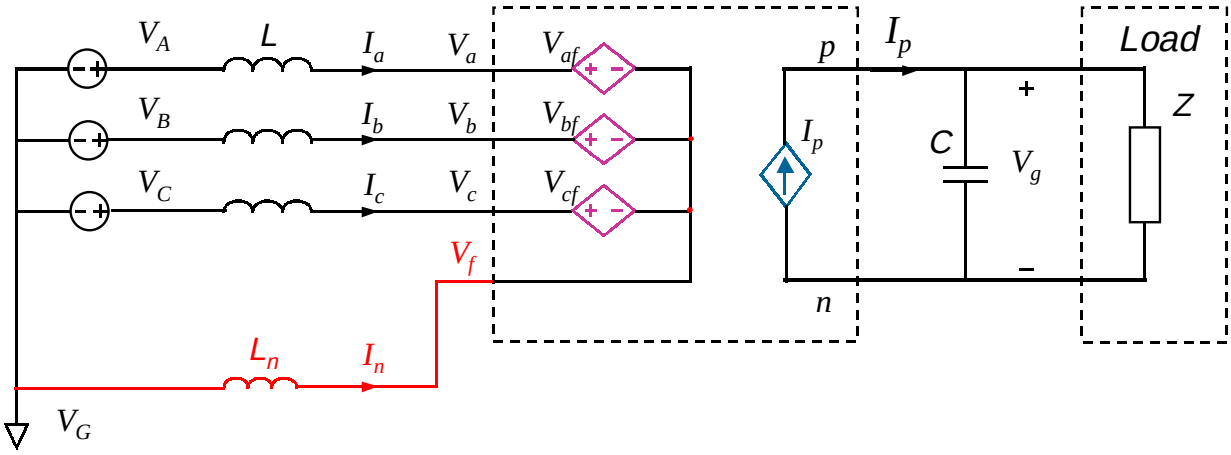


Figure 3-24 Average large-signal model of a four-legged PWM rectifier

3.4 Three-Dimensional Space Vector Modulation

3.4.1 Three-Dimensional Space Vector

3.4.1.1 Definition of Three-Dimensional Space Vector

In a conventional balanced three-phase inverter, where an assumption of $X_a+X_b+X_c=0$ is always made, only two variables are independent. Variables in a-b-c coordinate X_{abc} can be mapped in an α-β plane, as seen in Section 3.2.3.1. When the fourth neutral leg is added to a conventional three-phase inverter to deal with the zero-sequence load current, as shown in Figure 3-19, the assumption of $X_a+X_b+X_c=0$ is no longer valid. The fact that

(3.21) $$X_a + X_b + X_c \neq 0$$

suggests that the three variables become truly three independent variables, and could be only mapped into a vector $\mathbb{X}$ on the orthogonal α–β–γ coordinate in a three-dimensional space, where

(3.22) $$\mathbb{X} = X_\alpha + jX_\beta + kX_\gamma$$

The transformation for the orthogonal coordinate mapping is a true 3/3 transformation, and can be expressed as

(3.23) $$\begin{bmatrix} X_\alpha & X_\beta & X_\gamma \end{bmatrix}^T = T_2 \cdot \begin{bmatrix} X_a & X_b & X_c \end{bmatrix}^T$$

where T_2 is the transformation matrix and expressed as

(3.24)
$$T_2 = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

The inverse transformation can be found as

(3.25)
$$\begin{bmatrix} X_a & X_b & X_c \end{bmatrix}^T = T_2^{-1} \cdot \begin{bmatrix} X_\alpha & X_\beta & X_\gamma \end{bmatrix}^T$$

where the inverse transformation matrix is expressed as

(3.26)
$$T_2^{-1} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}$$

The relationship between the a-b-c coordinate and the orthogonal α–β–γ coordinate is shown in Figure 3-25 in a three-dimensional space.

3.4.1.2 Switching Vectors in α–β–γ coordinate

In a three-legged inverter, there are eight possible switch combinations. With the fourth neutral leg, the total number of switch combinations increases to sixteen. The switch combinations are represented by ordered sets [S_a, S_b, S_c, S_f], where S_a = ‘p’ denotes that the upper switch in phase A, S_{ap}, is closed, and S_a = ‘n’ denotes that the bottom switch in phase A, S_{an}, is closed. The same notation applies to phase legs B and C and the fourth neutral leg.

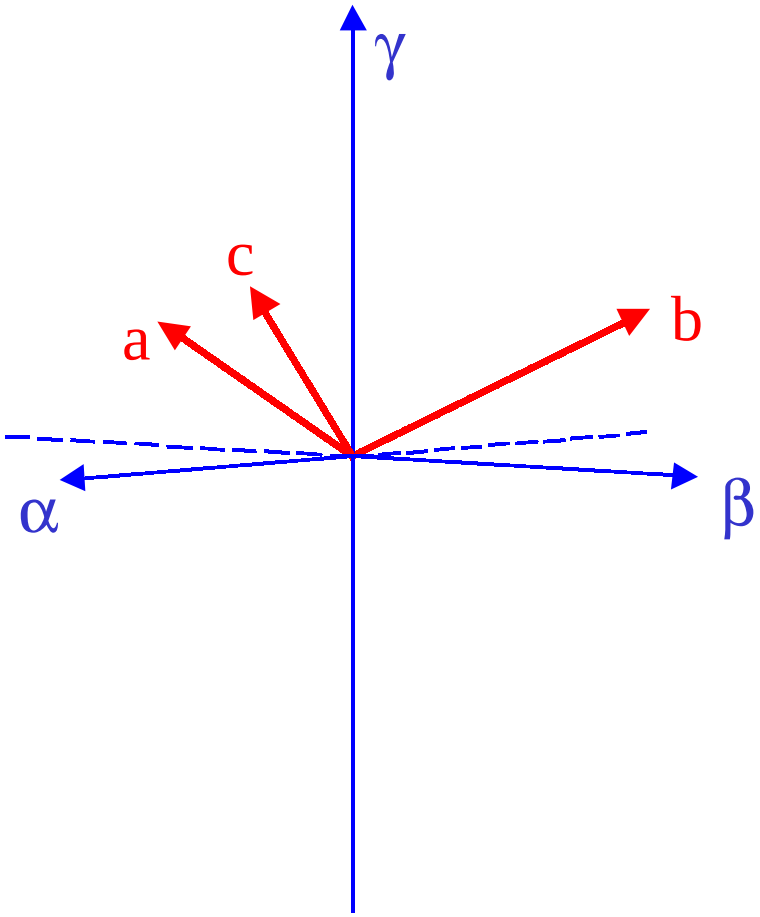


Figure 3-25 Relationship between the a-b-c coordinate and the α–β–γ coordinate

Figure 3-26 shows all the sixteen switching combinations. Table 3–1 shows the corresponding line-to-neutral voltages. By applying (3.23) and (3.24), the terminal voltages $[V_{af}\ V_{bf}\ \ V_{cf}\ ]^T$ in a-b-c coordinate listed in Table 3–1 can be transformed into $[V_\alpha\ V_\beta\ \ V_\gamma\ ]^T$ in α–β–γ orthogonal coordinate. The results of the transformation are shown in Table 3–2. It should be noted that V_γ is the zero-sequence component and related to the neutral current.

The distribution of the sixteen switching vectors expressed in Table 3–2 are represented graphically in Figure 3-27. There are two zero switching vectors (pppp, nnnn), and fourteen non-zero switching vectors. It can be viewed as that each of the switching vector for a three-legged converter splits into two switching vectors, depending on switch position of the neutral leg. All the sixteen switching vectors can be sorted into several layers. The two zero vectors, pppp and nnnn, locate at the origin of the α–β–γ coordinate. On the layer of $V_\gamma = \frac{1}{3}V_g$, there are three vectors, pnnn, npnn and nnpn. On the layer of $V_\gamma = \frac{2}{3}V_g$, there are three vectors, ppnn, nppn and pnpn. On the layer of $V_\gamma = V_g$, there is only one vector, pppn. On the layer of $V_\gamma = -\frac{1}{3}V_g$, there are three vectors, pnpp, ppnp and nppp. On the layer of $V_\gamma = -\frac{2}{3}V_g$, there are three vectors, pnnp, npnp and nnpp. On the layer of $V_\gamma = -V_g$, there is only one vector, nnnp. Projection of all switching vectors back on the α–β plane forms a hexagon, similar to that of a conventional three-phase inverter, shown in Figure 3-27. The projected vectors have a length of $\frac{2}{3}V_g$.

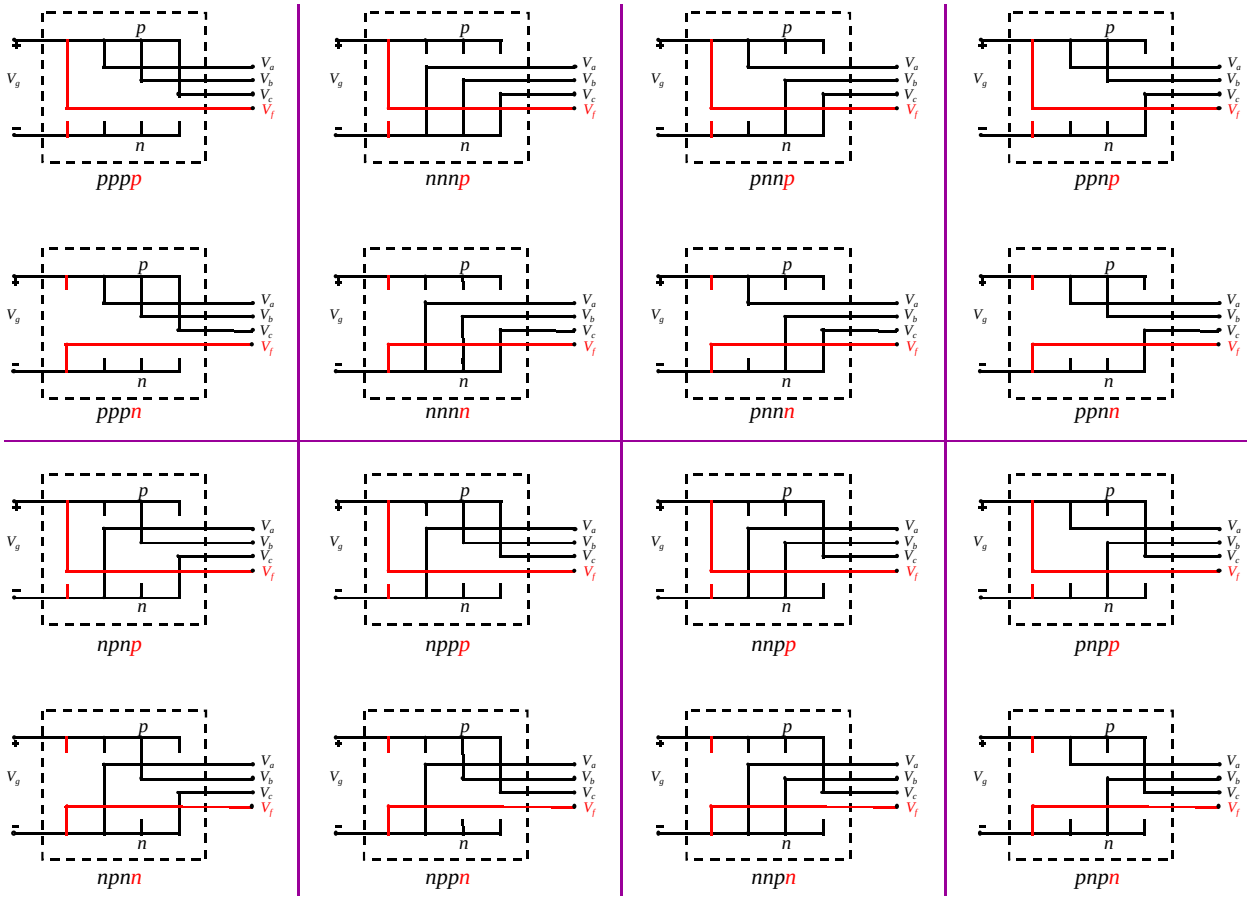


Figure 3-26 Sixteen possible switching combinations

Table 3–1 Switch Combinations and Independent Bridge Voltages

	pppp	nnnp	pnnp	ppnp	npnp	nppp	nnpp	pnpp
Vaf	0	-Vg	0	0	-Vg	-Vg	-Vg	0
Vbf	0	-Vg	-Vg	0	0	0	-Vg	-Vg
Vcf	0	-Vg	-Vg	-Vg	-Vg	0	0	0
	pppn	nnnn	pnnn	ppnn	npnn	nppn	nnpn	pnpn
Vaf	Vg	0	Vg	Vg	0	0	0	Vg
Vbf	Vg	0	0	Vg	Vg	Vg	0	0
Vcf	Vg	0	0	0	0	Vg	Vg	Vg

Table 3–2 Switch Combinations and Inverter Voltages in α–β–γ

	pppp	nnnp	pnnp	ppnp	npnp	nppp	nnpp	pnpp
V_α	0	0	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$-\frac{1}{3}V_g$	$-\frac{2}{3}V_g$	$-\frac{1}{3}V_g$	$\frac{1}{3}V_g$
V_β	0	0	0	$\frac{1}{\sqrt{3}}V_g$	$\frac{1}{\sqrt{3}}V_g$	0	$-\frac{1}{\sqrt{3}}V_g$	$-\frac{1}{\sqrt{3}}V_g$
V_γ	0	$-V_g$	$-\frac{2}{3}V_g$	$-\frac{1}{3}V_g$	$-\frac{2}{3}V_g$	$-\frac{1}{3}V_g$	$-\frac{2}{3}V_g$	$-\frac{1}{3}V_g$
	pppn	nnnn	pnnn	ppnn	npnn	nppn	nnpn	pnpn
V_α	0	0	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$-\frac{1}{3}V_g$	$-\frac{2}{3}V_g$	$-\frac{1}{3}V_g$	$\frac{1}{3}V_g$
V_β	0	0	0	$\frac{1}{\sqrt{3}}V_g$	$\frac{1}{\sqrt{3}}V_g$	0	$-\frac{1}{\sqrt{3}}V_g$	$-\frac{1}{\sqrt{3}}V_g$
V_γ	V_g	0	$\frac{1}{3}V_g$	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$\frac{2}{3}V_g$

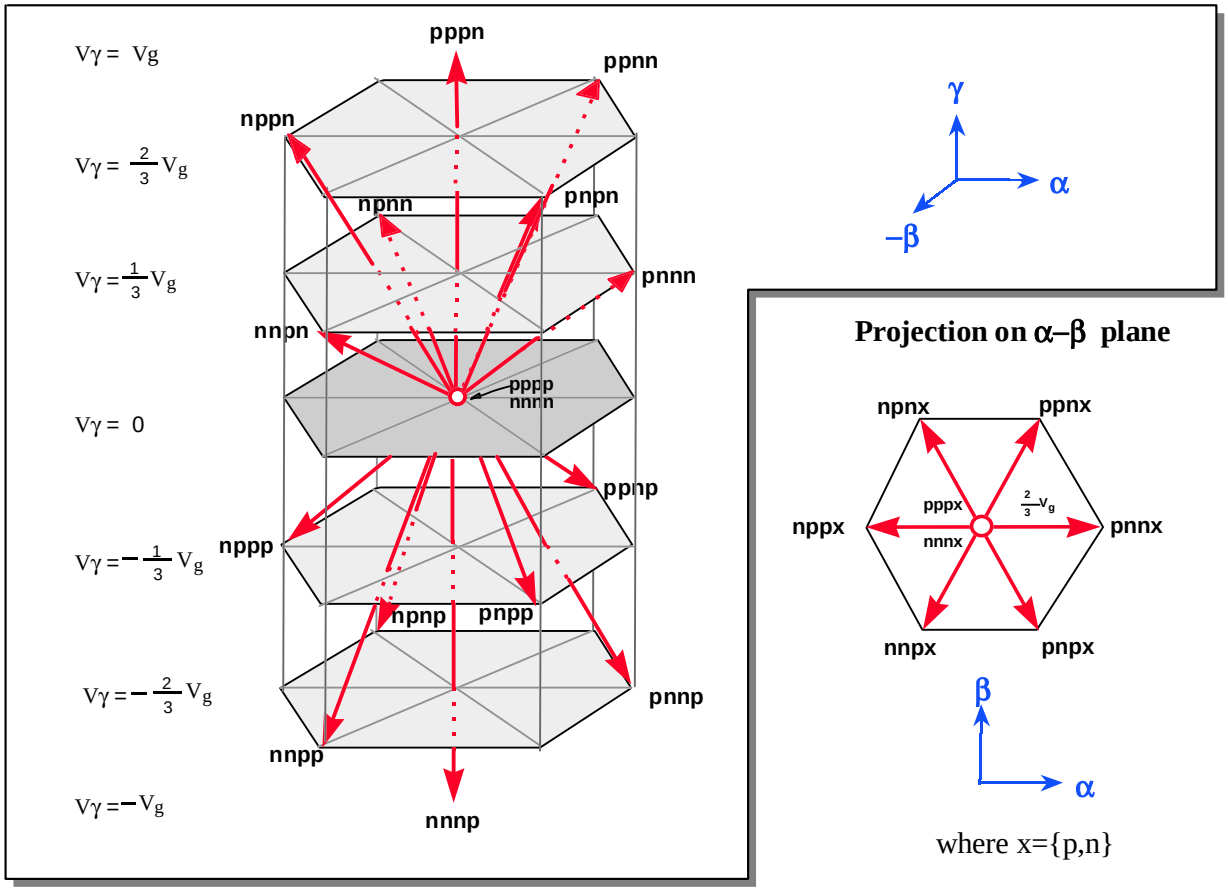


Figure 3-27 Switching vectors in α–β–γ coordinate

3.4.1.3 Reference Vector in α–β–γ coordinate

The reference vector is obtained by transforming the reference voltage $\begin{bmatrix} V_{af\_ref} & V_{bf\_ref} & V_{cf\_ref} \end{bmatrix}^T$ onto the α–β–γ coordinate. The result is the reference vector $\mathbb{V}_{ref}$ represented by $\begin{bmatrix} V_{\alpha\_ref} & V_{\beta\_ref} & V_{\gamma\_ref} \end{bmatrix}^T$.

3.4.2 Synthesis of the Reference Vector in α–β–γ coordinate

Three-dimensional space vector modulation is to synthesize the reference vector $\mathbb{V}_{ref}$ using the switching vectors in the α–β–γ coordinate. It is similar to that of two-dimensional space vector modulation, except it is more complicated than its two-dimensional version due to the doubled number of switching vectors and the additional freedom caused by the zero-sequence. Synthesis of the reference vector in the α–β–γ coordinate needs to take the following steps: (1) selection of switching vectors; (2) projection of the reference vector onto selected switching vectors; and (3) sequencing the switching vectors.

3.4.2.1 Selections of Switching Vectors

In order to minimize the circulating energy, and thus reduce the current ripple and harmonic contents, switching vectors adjacent to the reference vector should be selected. The adjacent switching vectors are easy to identify for the two-dimensional space vector modulation. For three-dimensional space vector, it takes two steps to identify the adjacent vectors. First, like the six sectors in the two-dimensional SVM, six prisms can be identified. They are numbered prism I through VI, as shown in Figure 3-28. The criteria to determine which prism the reference vector is in relies on only the projections of the reference vector on the α–β plane V_α and V_β. Therefore, it is the same as the two-dimensional SVM. Once the prism where the reference vector locates is found, there are six non-zero switching vectors and two zero switching vectors available to synthesize the

reference vector. Within each prism, four tetrahedrons can be identified, and numbered as tetrahedron 1 through 4. The example of four tetrahedrons in prism I is shown in Figure 3-29. Each tetrahedron has three non-zero switching vectors and two zero switching vectors. The signs of the line-to-neutral voltages produced by the non-zero switching vectors are also shown in Figure 3-29. It can be seen that within each tetrahedron, all the non-zero-switching vectors produce non-conflicting line-to-neutral voltages. Therefore, synthesis of the reference vector using the switching vectors defined by the tetrahedrons gives a minimum circulating energy. The adjacent switching vectors are defined by the tetrahedrons. Once we know which tetrahedron the reference vector locates at, we know which three non-zero vectors should be used. The strategy to select the zero vectors will depend on the sequencing scheme, which is similar to a two-dimensional SVM scheme.

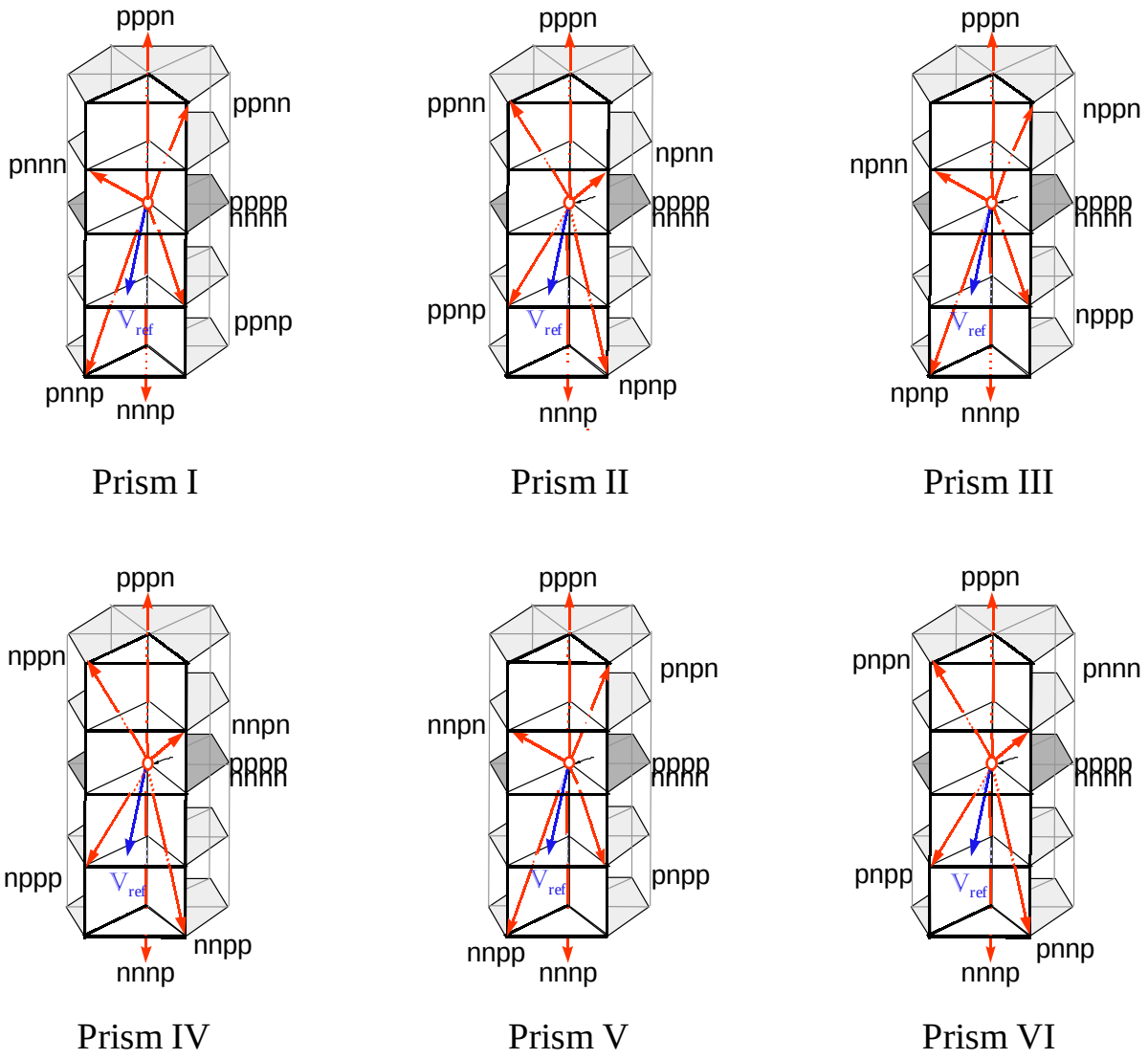


Figure 3-28 Selection of adjacent switching vectors, step one: prism identification

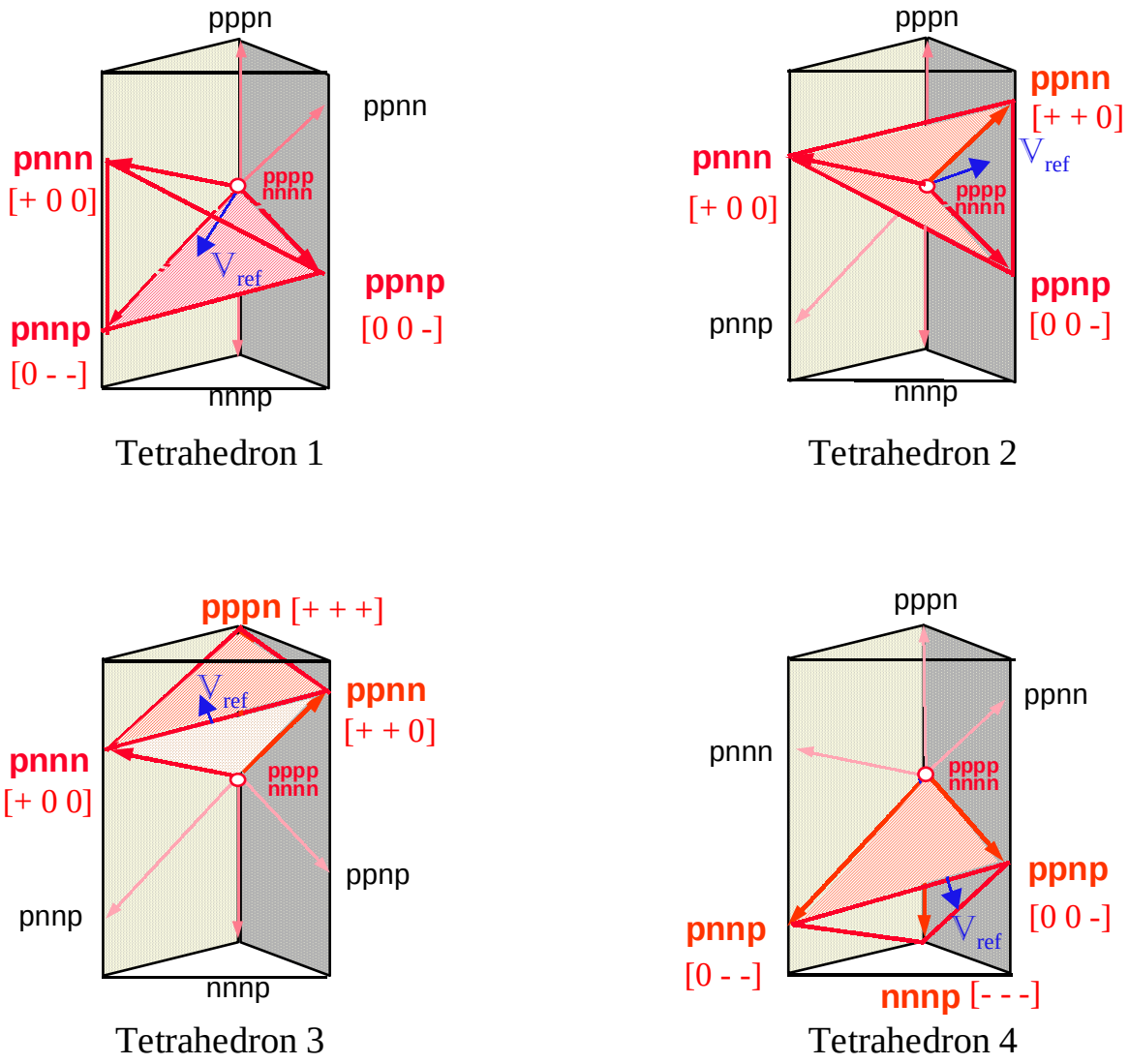


Figure 3-29 Selection of adjacent switching vectors, step two: tetrahedron identification – example for the reference vector located in prism I.

3.4.2.2 Projection of the Reference Vectors

The duration of each applied switching vectors can be easily computed by projecting the reference vector onto the switching vectors, which is similar to the two-dimensional SVM. The differences is that for three-dimensional SVM, there are three non-zero switching vectors involved in a three-dimensional space. Assuming the reference vector is in prism I and tetrahedron 1, $\mathbb{V}_{ref} = \begin{bmatrix} V_{\alpha\_ref} & V_{\beta\_ref} & V_{\gamma\_ref} \end{bmatrix}^T$, the available switching vectors are $\mathbb{V}_1$ = [pnnn], $\mathbb{V}_2$ = [pnnp], $\mathbb{V}_3$ = [ppnp], $\mathbb{V}_0$ = [pppp, nnnn]. The corresponding duty ratio of each switching vectors are given by (3.27) ~ (3.29),

(3.27) $$\mathbb{V}_{ref} = d_1 \cdot \mathbb{V}_1 + d_2 \cdot \mathbb{V}_2 + d_3 \cdot \mathbb{V}_3$$

(3.28) $$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_g} \begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix} \begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix}$$

(3.29) $$d_Z = 1 - d_1 - d_2 - d_3$$

When the reference vector is in other tetrahedrons, the only thing that needs to be changed is the matrix in (3.28). Table 3–3 shows the corresponding non-zero switching vectors, named as $\mathbb{V}_1$, $\mathbb{V}_2$ and $\mathbb{V}_3$, for all 24 tetrahedrons. Table 3–4 shows the matrix needed to compute the duty ratios.

Table 3–3 Corresponding Non-Zero Switching Vectors Named as V_1, V_2 and V_3

Tetrahedron / Prism	1	2	3	4
I	V_1 : pnnn V_2 : pnnp V_3 : ppnp	V_1 : pnnn V_2 : ppnn V_3 : ppnp	V_1 : pnnn V_2 : ppnn V_3 : pppn	V_1 : pnnp V_2 : ppnp V_3 : nnnp
II	V_1 : ppnn V_2 : ppnp V_3 : npnn	V_1 : ppnp V_2 : npnn V_3 : npnp	V_1 : ppnn V_2 : npnn V_3 : pppn	V_1 : ppnp V_2 : npnp V_3 : nnnp
III	V_1 : npnn V_2 : npnp V_3 : nppp	V_1 : npnn V_2 : nppn V_3 : nppp	V_1 : npnn V_2 : nppn V_3 : pppn	V_1 : npnp V_2 : nppp V_3 : nnnp
IV	V_1 : nppn V_2 : nppp V_3 : nnpn	V_1 : nppp V_2 : nnpn V_3 : nnpp	V_1 : nppn V_2 : nnpn V_3 : pppn	V_1 : nppp V_2 : nnpp V_3 : nnnp
V	V_1 : nnpn V_2 : nnpp V_3 : pnpp	V_1 : nnpn V_2 : pnpn V_3 : pnpp	V_1 : nnpn V_2 : pnpn V_3 : pppn	V_1 : nnpp V_2 : pnpp V_3 : nnnp
VI	V_1 : pnpn V_2 : pnpp V_3 : pnnn	V_1 : pnpp V_2 : pnnn V_3 : pnnp	V_1 : pnpn V_2 : pnnn V_3 : pppn	V_1 : pnpp V_2 : pnnp V_3 : nnnp

Table 3–4 Matrix for Switching Vector Duty Ratio Computation

Tetrahedron / Prism	1	2	3	4
I	$\begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \end{bmatrix}$	$\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 0 & \sqrt{3} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 0 & \sqrt{3} & 0 \\ -1 & 0 & -1 \end{bmatrix}$
II	$\begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -1 & 0 & -1 \end{bmatrix}$	$\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \end{bmatrix}$
III	$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \\ -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & \sqrt{3} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \\ -1 & 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 0 & \sqrt{3} & 0 \\ -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & \sqrt{3} & 0 \\ -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \end{bmatrix}$
IV	$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -1 & 0 & -1 \\ 0 & -\sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \end{bmatrix}$	$\begin{bmatrix} -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ 0 & -\sqrt{3} & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ 0 & -\sqrt{3} & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \end{bmatrix}$
V	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \\ -1 & 0 & -1 \\ \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 1 & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \end{bmatrix}$	$\begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \end{bmatrix}$	$\begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \end{bmatrix}$
VI	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\sqrt{3} & 0 \\ 1 & 0 & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \end{bmatrix}$	$\begin{bmatrix} 0 & -\sqrt{3} & 0 \\ \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & -\sqrt{3} & 0 \\ \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -1 & 0 & -1 \end{bmatrix}$

3.4.2.3 Sequencing of the Switching Vectors

Like its two-dimensional SVM counterpart, the sequencing schemes for three-dimensional SVM can also be grouped into two classes. Class I sequencing schemes use both the two zero switching vectors, pppp and nnnn. Class II sequencing schemes use only one of the two zero switching vectors. Each class has four sequencing schemes: rising-edge aligned, falling-edge aligned, symmetrical aligned, and alternative sequence. The definitions for each sequencing scheme have been given in the review of the two-dimensional SVM. The examples of class I sequencing schemes are shown in Figure 3-30 for two consecutive switching periods. The examples of class II sequencing schemes are shown in Figure 3-31 for two consecutive switching periods. All the examples assume that the reference vector locates in prism I tetrahedron 1, and assume phase A carries the largest current.

For class I schemes, there are eight switching actions in each switching period for the rising-edge aligned scheme, the falling edged scheme, and the symmetrical aligned scheme. Although the alternative sequence has six switching actions in each switching period, and thus reduces switching losses, it suffers from a large harmonic content at half of the switching frequency since the switching pattern repeats every two switching periods. The rising-edge aligned and the falling-edge aligned schemes may be adopted for soft-switching techniques, and thus may reduce switching losses. However, they have larger harmonic contents and yield larger distortion than the symmetrical aligned scheme. Due to its symmetry, the symmetrical aligned class I scheme gives the least harmonic distortion.

By selectively using the zero switching vector, class II schemes inactivate the phase carrying the highest current. Compared with class I schemes, they save two switching actions for the highest current phase for rising-edge aligned, falling-edge aligned and symmetrical aligned schemes, and save one switching action for the alternative sequence. It results in approximately 50% saving on the switching losses for a unity power factor load. The savings may vary depending on the load power factor [B20].

Overall, symmetrical aligned class II scheme is a good compromise between the switching losses and the harmonic contents, and therefore it is adopted in the real implementation.

3.4.2.4 Duty Ratios of Phase Legs in a Line Cycle

The duty ratios of phase legs d_a, d_b, d_c, and d_f can be derived from the duty ratios of the switching vectors d_1, d_2, d_3, and d_z, and the sequencing scheme used. The duty ratio of phase legs are within the range of [0,1], where '0' represents that the bottom switch of the phase leg is on all the time within the switching period, and '1' represents that the upper switch of the phase leg is on throughout the switching period.

A balanced linear load is used to show the duty ratios of phase legs. In order to produce three-phase sinusoidal output voltage under a balanced linear load, it is known from Figure 3-23 that the phase-leg-to-neutral-leg duty ratios d_{af}, d_{bf}, and d_{cf}, defined in (3.19) are three-phase sinusoidal , as shown in Figure 3-32. The duty ratios d_{af}, d_{bf}, and d_{cf} can be represented by a reference vector rotating in the α–β plane. Therefore we have

(3.30)
$$\begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix} = \frac{M}{\sqrt{3}} V_g \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \\ 0 \end{bmatrix}$$

Applying (3.27) ~ (3.29), duty ratios of switching vectors d_1, d_2, d_3, and d_z can be obtained. Considering the zero vector selection based on the sequencing scheme, the phase leg duty ratios d_a, d_b, d_c, and d_f are plotted in Figure 3-33. It can be seen that the phase leg duty ratios d_a, d_b and d_c are similar to that of a three-legged inverter, while the neutral leg duty ratio d_f is around 0.5, and has triplen harmonics.

3.4.3 Over-Modulation in α–β–γ coordinate

Over-modulation happens in the following situations: (1) large transient; (2) highly unbalance; (3) highly nonlinear; (4) fault mode operation.

When the reference vector is outside the region confined by the surfaces given by the 24 tetrahedrons, the three-dimensional space vector modulation goes into over-modulation mode. The duty ratios of switching vectors may become negative values if the reference vector is not modified.

The over-modulation mode for the three-dimensional SVM is similar to the two-dimensional version. Instead of the hexagon in the two-dimensional case, there are three over-modulation surfaces in each prism. The over-modulation surfaces confine the attainable region. The example of the three over-modulation surfaces in prism I is shown in Figure 3-34. When the reference vector intersects with any of the three over-modulation surfaces, the reference vector is modified to the intersection point on that over-modulation surface.

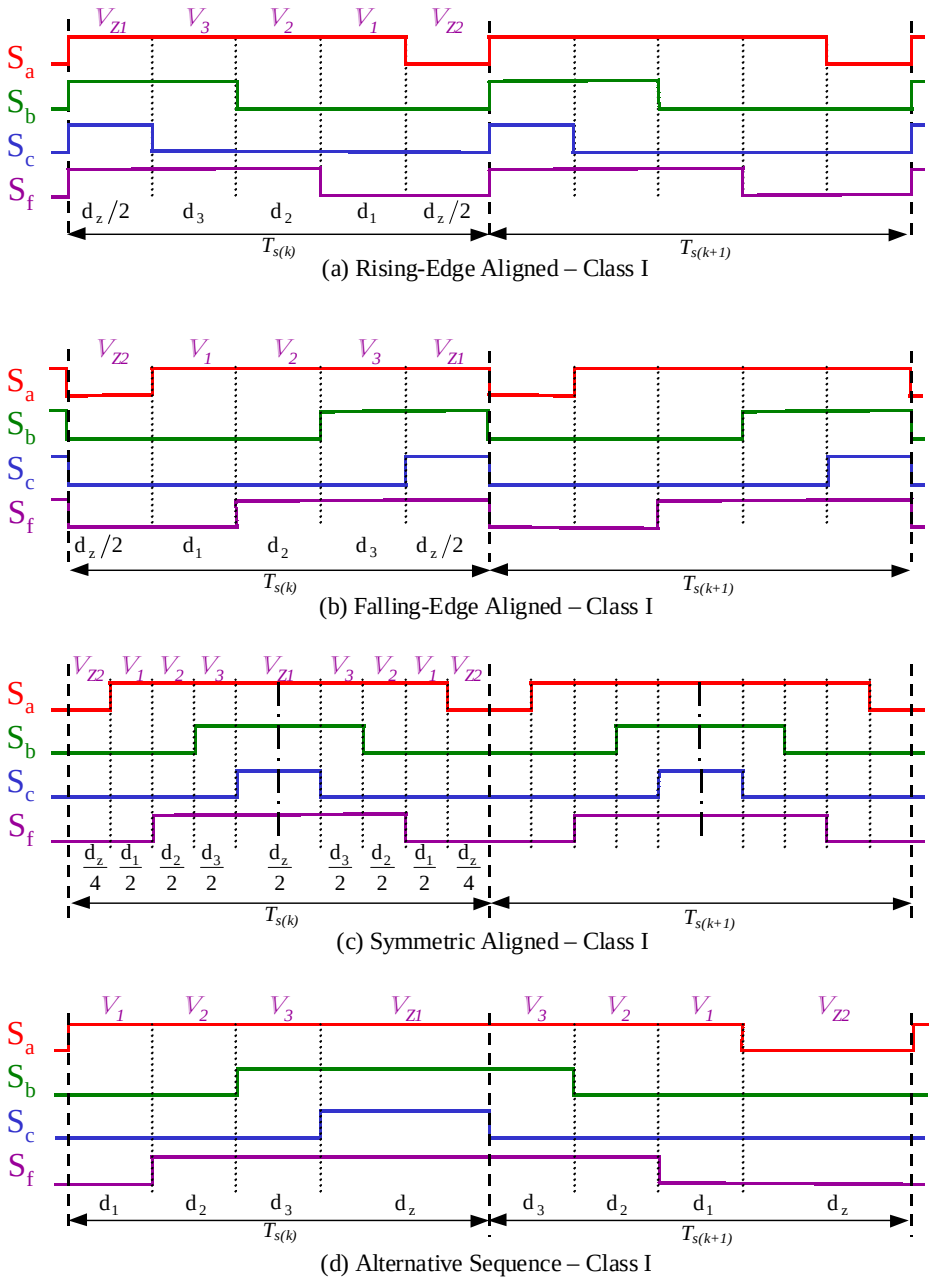


Figure 3-30 Class I sequencing schemes

(a) rising-edge aligned; (b) falling-edge aligned;
(c) symmetric aligned; (d) alternative sequence

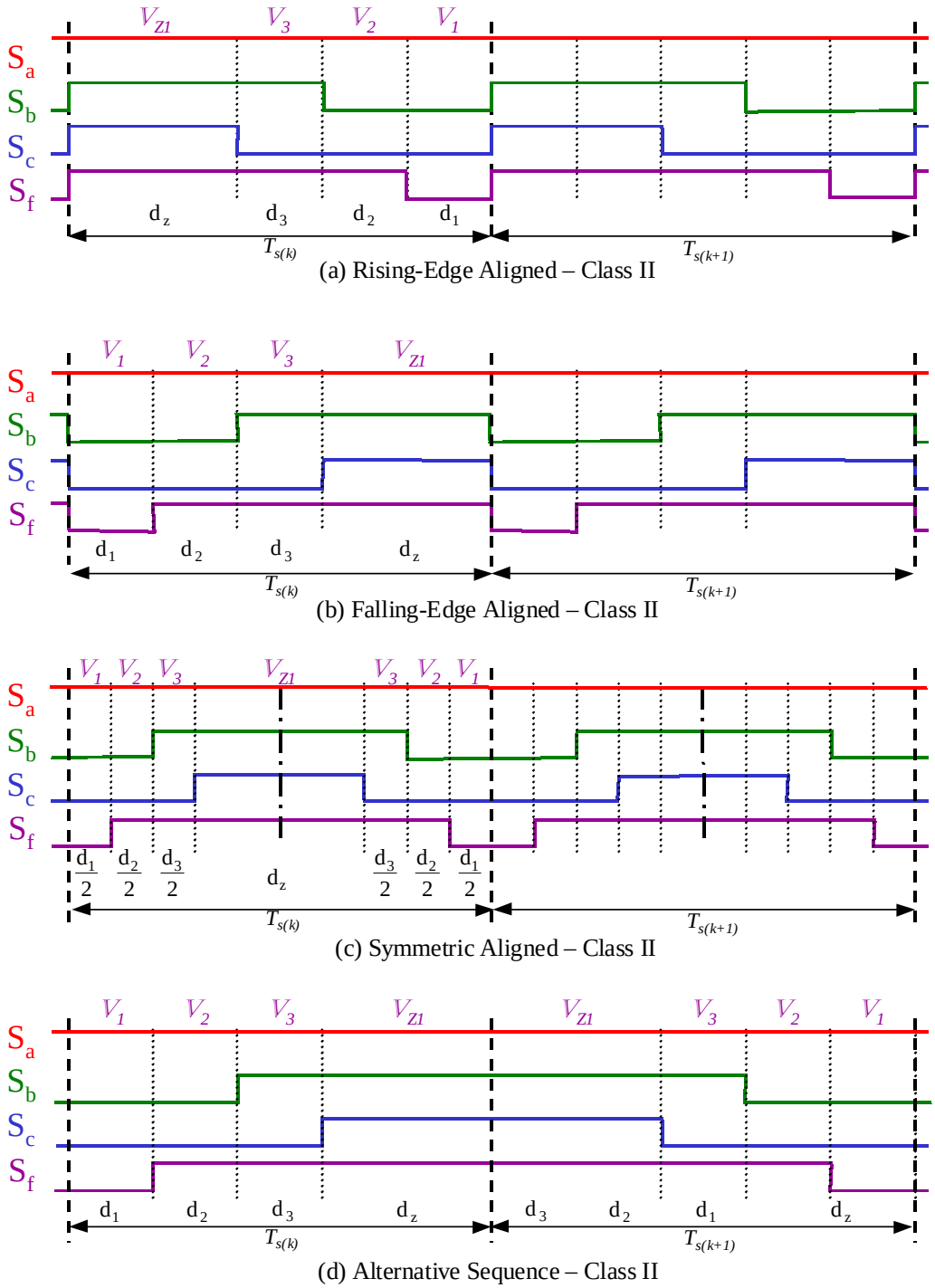


Figure 3-31 Class II sequencing schemes

(a) rising-edge aligned; (b) falling-edge aligned;
(c) symmetric aligned; (d) alternative sequence

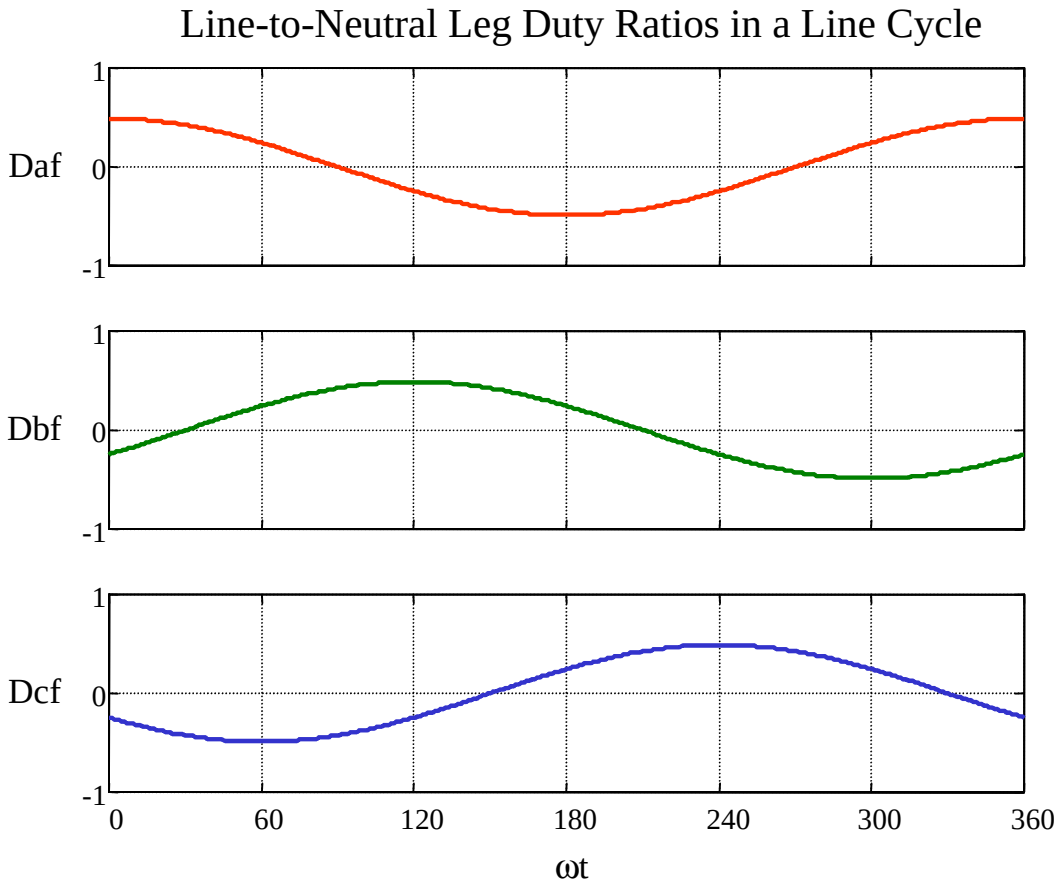


Figure 3-32 Phase-leg-to-neutral-leg duty ratios in a line cycle with a balanced linear load

(modulation index M = 0.848)

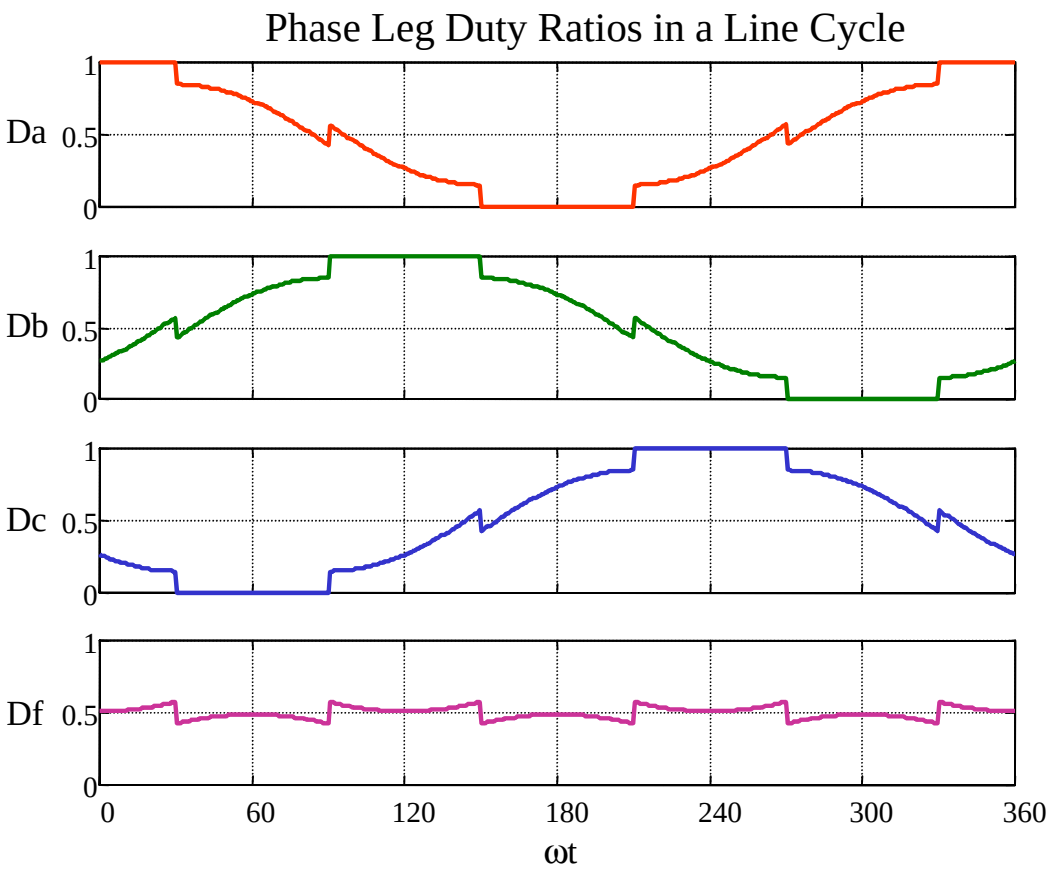


Figure 3-33 Phase leg duty ratios in a line cycle for a balanced linear load

(modulation index M = 0.848)

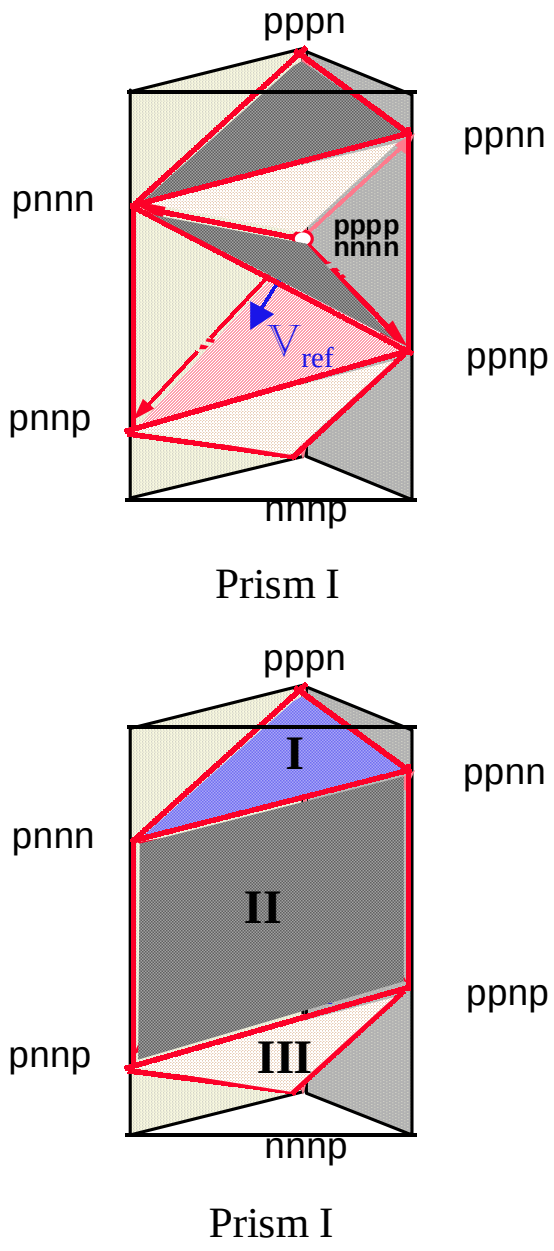


Figure 3-34 Over-modulation surfaces in prism I

3.5 Operation Principle and Design of Four-Legged Inverter

3.5.1 Load Current in α–β–γ Coordinate

Since the modulation is performed in α–β–γ coordinate, it is necessary to characterize the three-phase load current in α–β–γ coordinate. As described in Chapter 2, an arbitrarily unbalanced three-phase load current can be decomposed into three sets of balanced currents, namely positive-sequence currents I_{LA_p}, I_{LB_p} and I_{LC_p}; negative-sequence currents I_{LA_n} , I_{LB_n}, I_{LC_n}; and zero-sequence currents I_{LA_0}, I_{LB_0} and I_{LC_0}. Since all the zero-sequence currents are identical, it can be simplified as I_0. Therefore, we have load currents expressed as

$$\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \begin{bmatrix} I_{LA\_p} + I_{LA\_n} + I_0 \\ I_{LB\_p} + I_{LB\_n} + I_0 \\ I_{LC\_p} + I_{LC\_n} + I_0 \end{bmatrix} \quad \textbf{(3.31)}$$

Applying (3.23) and (3.24), the positive-sequence currents, negative-sequence currents, and the zero-sequence currents can be transformed into α–β–γ coordinate, as shown in Figure 3-35. The positive-sequence load current becomes a vector in α–β–γ coordinate rotating counter-clockwise at an angular speed of ω; the negative-sequence load current becomes a vector rotating clockwise at an angular speed of ω; and the zero-sequence load current becomes a vector moving along the γ axis back and forth once in one line period. The length of the vectors equals the peak value of the sinusoidal currents.

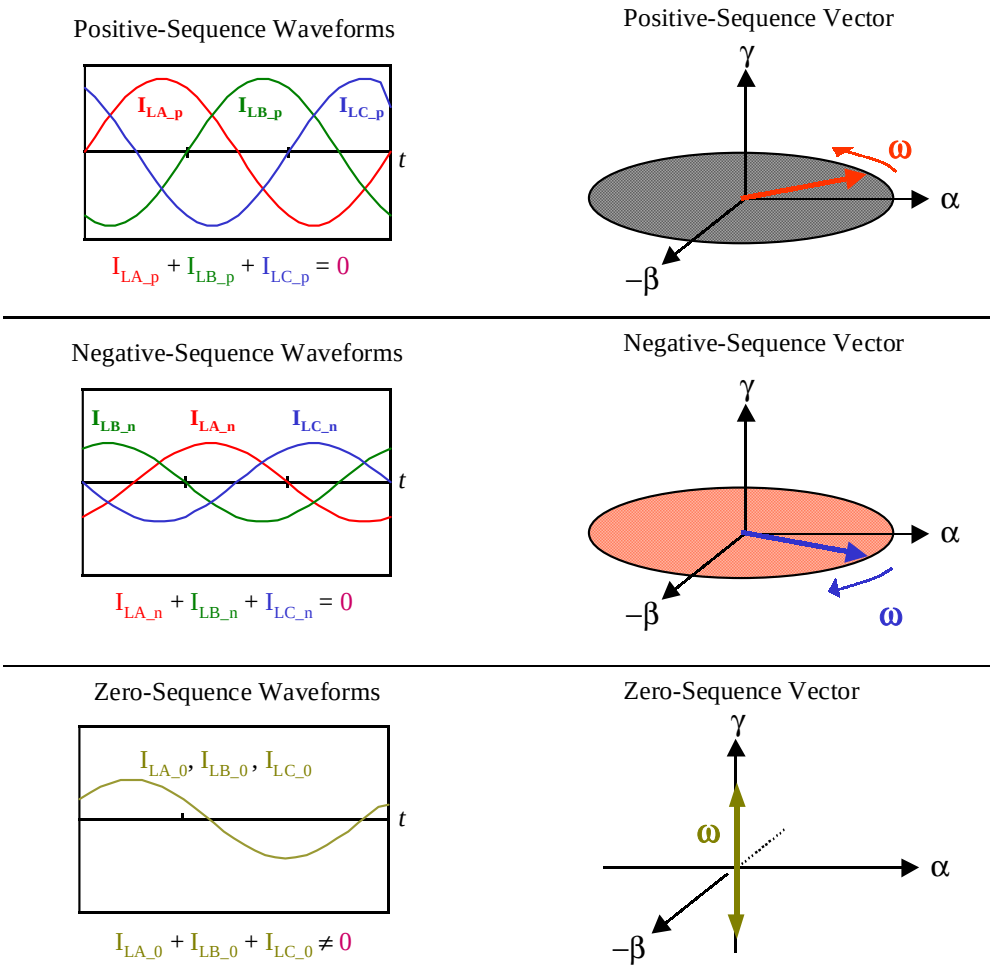


Figure 3-35 Load currents in α–β–γ coordinate

3.5.2 Steady State Analysis

From the average large signal circuit model shown in Figure 3-23, we have

$$\begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} = \begin{bmatrix} L(d\frac{I_{LA}}{dt} + Cd^2\frac{V_{AG}}{dt^2}) + V_{AG} - L_n d\frac{I_n}{dt} \\ L(d\frac{I_{LB}}{dt} + Cd^2\frac{V_{BG}}{dt^2}) + V_{BG} - L_n d\frac{I_n}{dt} \\ L(d\frac{I_{LC}}{dt} + Cd^2\frac{V_{CG}}{dt^2}) + V_{CG} - L_n d\frac{I_n}{dt} \end{bmatrix} \quad \textbf{(3.32)}$$

$$I_n = -(I_{LA} + I_{LB} + I_{LC}) - Cd\frac{(V_{AG} + V_{BG} + V_{CG})}{dt} \quad \textbf{(3.33)}$$

where I_{LA}, I_{LB} and I_{LC} are arbitrarily unbalanced three phase load currents, and I_n is the neutral current.

An arbitrary three-phase output voltage can also be decomposed into symmetrical components. It is expressed as

$$\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} = \begin{bmatrix} V_{AG\_p} + V_{AG\_n} + V_0 \\ V_{BG\_p} + V_{BG\_n} + V_0 \\ V_{CG\_p} + V_{CG\_n} + V_0 \end{bmatrix} \quad \textbf{(3.34)}$$

where V_0 is the zero-sequence output voltage.

Applying (3.31) and (3.34) to (3.33) yields

$$I_n = -3(I_0 + Cd\frac{V_0}{dt}) \quad \textbf{(3.35)}$$

(3.35) gives the relationship between the neutral current and the zero-sequence load current and zero-sequence output voltage. By applying (3.31), (3.34) and (3.35) to (3.32), the control voltage sources can also be decomposed into symmetrical components, as shown below.

(3.36)
$$\begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} = \begin{bmatrix} V_{af\_p} \\ V_{bf\_p} \\ V_{cf\_p} \end{bmatrix} + \begin{bmatrix} V_{af\_n} \\ V_{bf\_n} \\ V_{cf\_n} \end{bmatrix} + \begin{bmatrix} V_{af\_0} \\ V_{af\_0} \\ V_{af\_0} \end{bmatrix}$$

where the positive-sequence control voltage is expressed as

(3.37)
$$\begin{bmatrix} V_{af\_p} \\ V_{bf\_p} \\ V_{cf\_p} \end{bmatrix} = \begin{bmatrix} L(d\frac{I_{LA\_p}}{dt} + Cd^2\frac{V_{AG\_P}}{dt^2}) + V_{AG\_p} \\ L(d\frac{I_{LB\_p}}{dt} + Cd^2\frac{V_{BG\_p}}{dt^2}) + V_{BG\_p} \\ L(d\frac{I_{LC\_p}}{dt} + Cd^2\frac{V_{CG\_p}}{dt^2}) + V_{CG\_p} \end{bmatrix}$$

the negative-sequence control voltage is expressed as

(3.38)
$$\begin{bmatrix} V_{af\_n} \\ V_{bf\_n} \\ V_{cf\_n} \end{bmatrix} = \begin{bmatrix} L(d\frac{I_{LA\_n}}{dt} + Cd^2\frac{V_{AG\_n}}{dt^2}) + V_{AG\_n} \\ L(d\frac{I_{LB\_n}}{dt} + Cd^2\frac{V_{BG\_n}}{dt^2}) + V_{BG\_n} \\ L(d\frac{I_{LC\_n}}{dt} + Cd^2\frac{V_{CG\_n}}{dt^2}) + V_{CG\_n} \end{bmatrix}$$

the zero-sequence control voltages is expressed as

(3.39)
$$\begin{bmatrix} V_{af\_0} \\ V_{bf\_0} \\ V_{cf\_0} \end{bmatrix} = \begin{bmatrix} (L + 3L_n)(d\frac{I_0}{dt} + Cd^2\frac{V_0}{dt^2}) + V_0 \\ (L + 3L_n)(d\frac{I_0}{dt} + Cd^2\frac{V_0}{dt^2}) + V_0 \\ (L + 3L_n)(d\frac{I_0}{dt} + Cd^2\frac{V_0}{dt^2}) + V_0 \end{bmatrix}$$

In the steady state, the output voltage will be the desired balanced three-phase output voltage with the correct sequence. Therefore, only positive-sequence output voltage V_{AG_p}, V_{BG_p}, and V_{CG_p} exist, as shown below.

(3.40)
$$\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} = V_{ln\_pk} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2}{3}\pi) \\ \sin(\omega t + \frac{2}{3}\pi) \end{bmatrix}$$

where V_{ln_pk} is the peak of line-to-neutral voltage.

Setting all the negative-sequence output voltages and the zero-sequence output voltages to zero, (3.37) through (3.39) become

(3.41)
$$\begin{bmatrix} V_{af\_p} \\ V_{bf\_p} \\ V_{cf\_p} \end{bmatrix} = \begin{bmatrix} L(d\frac{I_{LA\_p}}{dt} + Cd^2\frac{V_{AG}}{dt^2}) + V_{AG} \\ L(d\frac{I_{LB\_p}}{dt} + Cd^2\frac{V_{BG}}{dt^2}) + V_{BG} \\ L(d\frac{I_{LC\_p}}{dt} + Cd^2\frac{V_{CG}}{dt^2}) + V_{CG} \end{bmatrix}$$

(3.42)
$$\begin{bmatrix} V_{af\_n} \\ V_{bf\_n} \\ V_{cf\_n} \end{bmatrix} = L \begin{bmatrix} d\frac{I_{LA\_n}}{dt} \\ d\frac{I_{LB\_n}}{dt} \\ d\frac{I_{LC\_n}}{dt} \end{bmatrix}$$

(3.43)
$$\begin{bmatrix} V_{af\_0} \\ V_{bf\_0} \\ V_{cf\_0} \end{bmatrix} = (L + 3L_n) \begin{bmatrix} d\frac{I_0}{dt} \\ d\frac{I_0}{dt} \\ d\frac{I_0}{dt} \end{bmatrix}$$

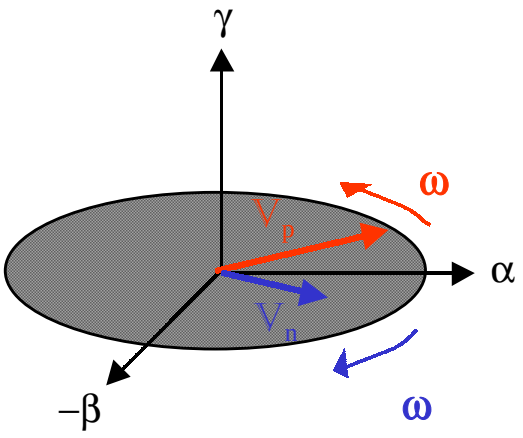
(3.36) and (3.41) through (3.43) describe the steady state operation of the inverter. Just like the load current, the positive-sequence control voltage becomes a vector $\mathbb{V}_p$, given by (3.41), rotating counter-clockwise in the α–β–γ coordinate, the trajectory of $\mathbb{V}_p$ is a circle; the negative-sequence control voltage becomes a vector $\mathbb{V}_n$, given by (3.42), also rotating counter-clockwise in the α–β–γ coordinate. The trajectory of $\mathbb{V}_n$ is a circle.

Combining the positive-sequence and the negative-sequence voltages, the control voltage on the α–β plane is a rotating vector $\mathbb{V}_{\alpha-\beta}$, as shown in Figure 3-36. When the load is balanced, since the $\mathbb{V}_n$ is zero, the trajectory of $\mathbb{V}_{ref\_\alpha\beta}$ is a circle. When the load is unbalanced, the trajectory of $\mathbb{V}_{\alpha-\beta}$ is an ellipse. The major radius of the ellipse will be $|\mathbb{V}_p| + |\mathbb{V}_n|$; the minor radius of the ellipse will be $|\mathbb{V}_p| - |\mathbb{V}_n|$.

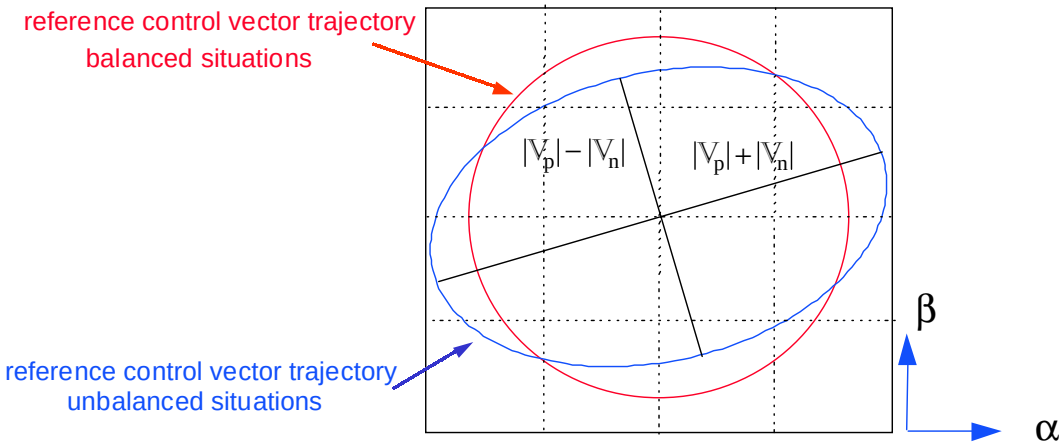
The γ axis component given by the zero-sequence control voltage vector $\mathbb{V}_0$ resulted from (3.43), makes the trajectory of the final steady state control voltage vector a skewed ellipse in the α–β–γ space.

For a balanced load current, the steady state trajectory of the control voltage vector is still a circle in the α–β plane as shown in Figure 3-37. With an unbalanced load, an example of steady state trajectories of the load current and the control voltage vectors is also shown in Figure 3-37.

The steady state trajectories for nonlinear loads, such as three-phase diode rectifiers and three single-phase diode rectifiers shown in Chapter 2, are shown in Figure 3-38 through Figure 3-42. For three-phase diode rectifiers, there is no γ axis component. In the no filter and large inductance filter cases, the discontinuous load currents, as seen in Chapter 2, would require very high control voltage. For three single-phase diode rectifiers, the projections of the load current vector on the γ axis are very large, which require large control voltage vectors on the γ axis, as can be seen in Figure 3-41 and Figure 3-42.



(a)



(b)

Figure 3-36 Steady state control voltage vector trajectory on α–β plane

(a) positive-sequence and negative sequence control voltage vectors;
(b) control voltage vector trajectory for balanced and unbalanced loads

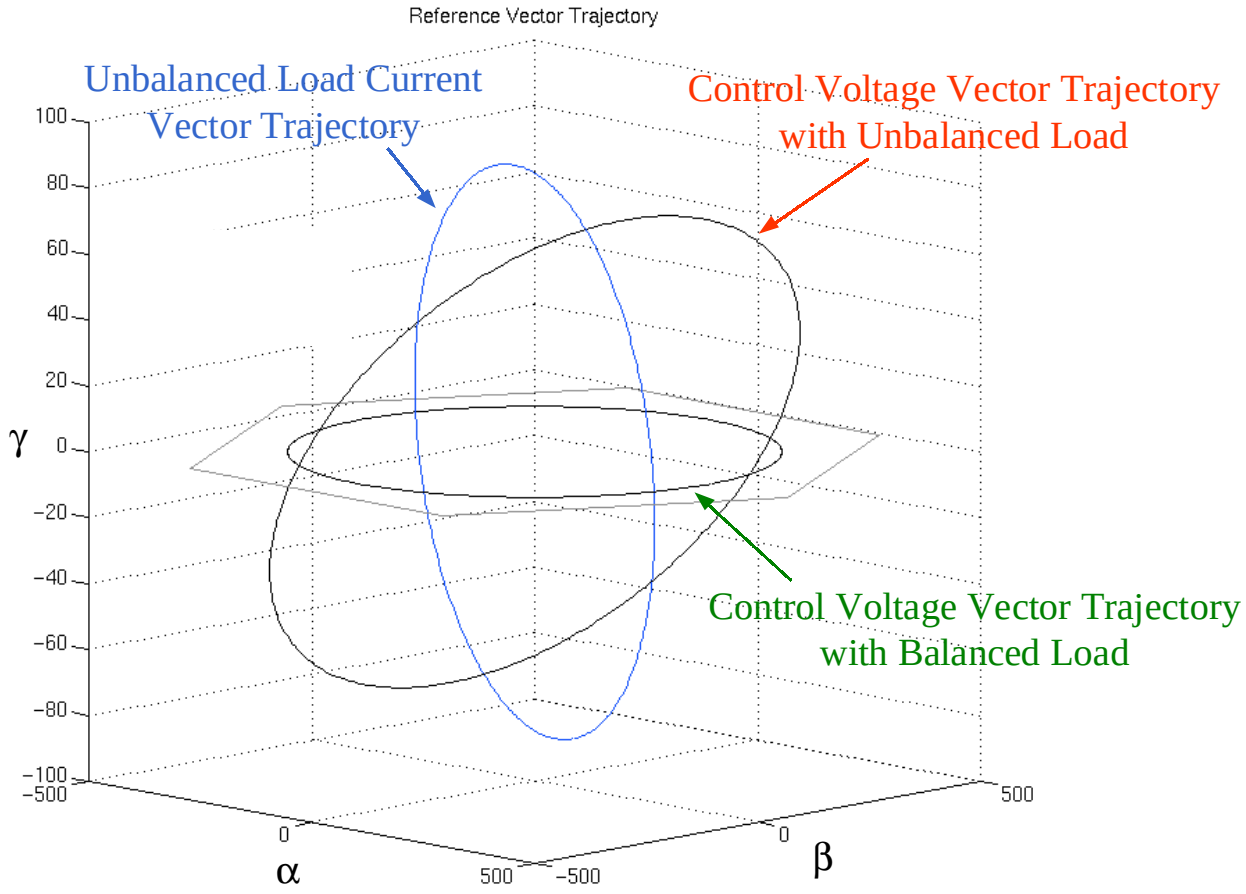


Figure 3-37 Trajectories of unbalanced load current vector and control voltage vector for balanced and unbalanced loads

$(I_A = 0\angle 0^\circ,\ I_B = 180\angle 120^\circ,\ I_C = 180\angle 240^\circ)$

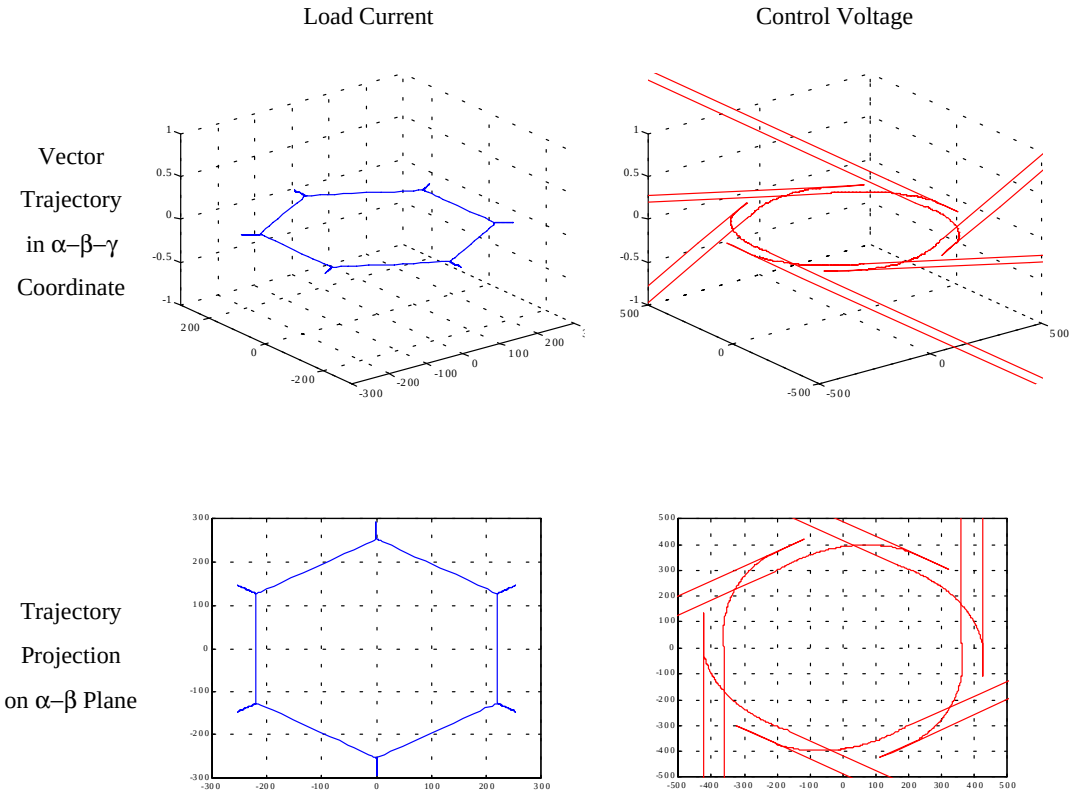


Figure 3-38 Steady state load current and control voltage vector trajectories in α–β–γ coordinate with a three-phase diode bridge rectifier without filter

(R = 2.67 Ohm)

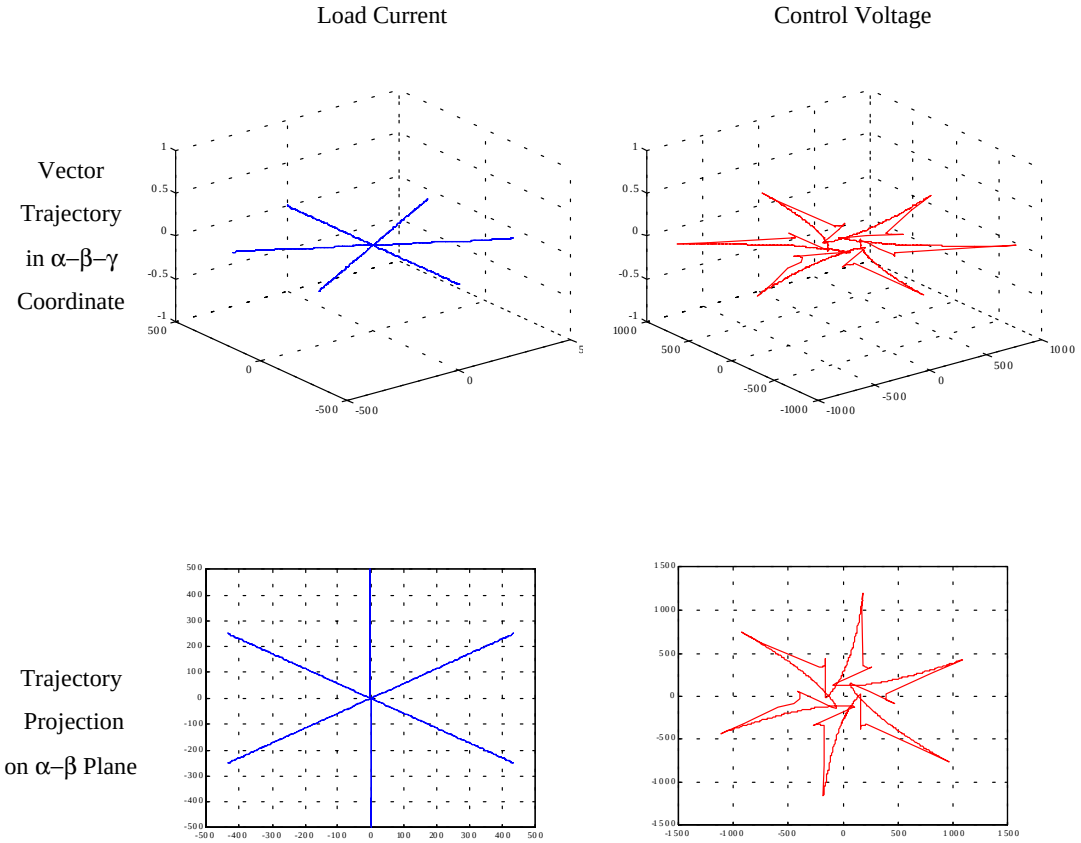


Figure 3-39 Steady state load current and control voltage vector trajectories in α–β–γ coordinate with a three-phase diode bridge rectifier with C filter

(C = 6900 uF, ESR_C = 150 mOhm, R = 2.67 Ohm)

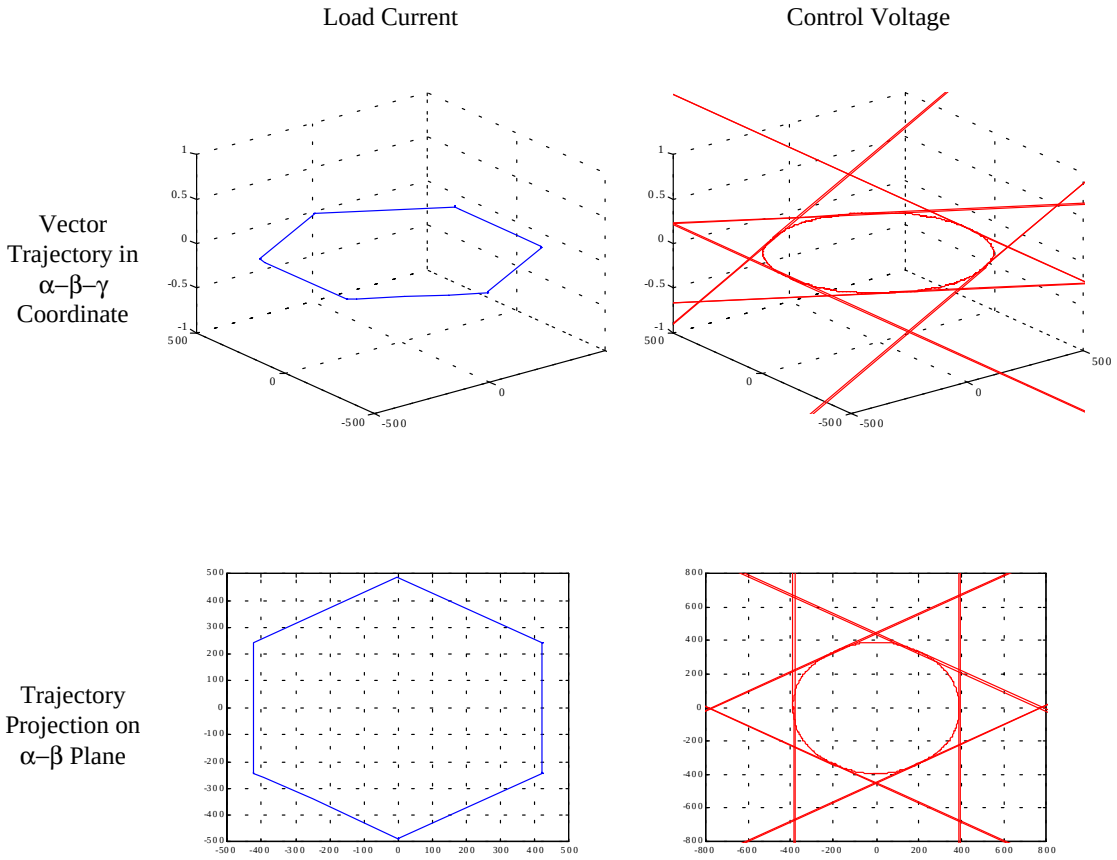


Figure 3-40 Steady state load current and control voltage vector trajectories in α–β–γ coordinate with a three-phase diode bridge rectifier with L/C filter

(L = 10 mH, C = 6900 uF, R = 2.67 Ohm)

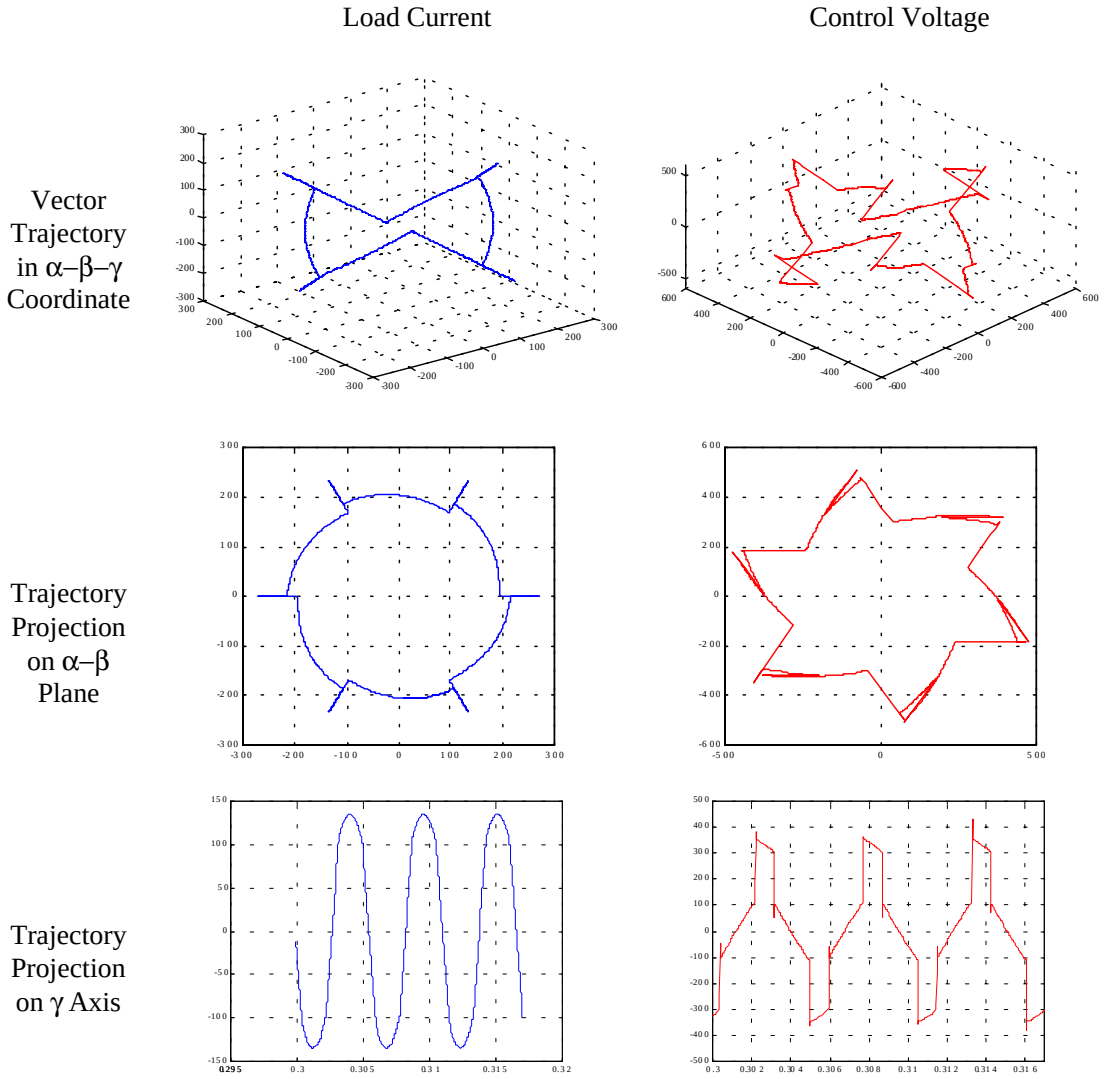


Figure 3-41 Steady state load current and control voltage vector trajectories in α–β–γ coordinate with three single-phase diode bridge rectifiers with C filter

(C = 21 mF, ESR_C = 250 mOhm, R = 2.7 Ohm per phase)

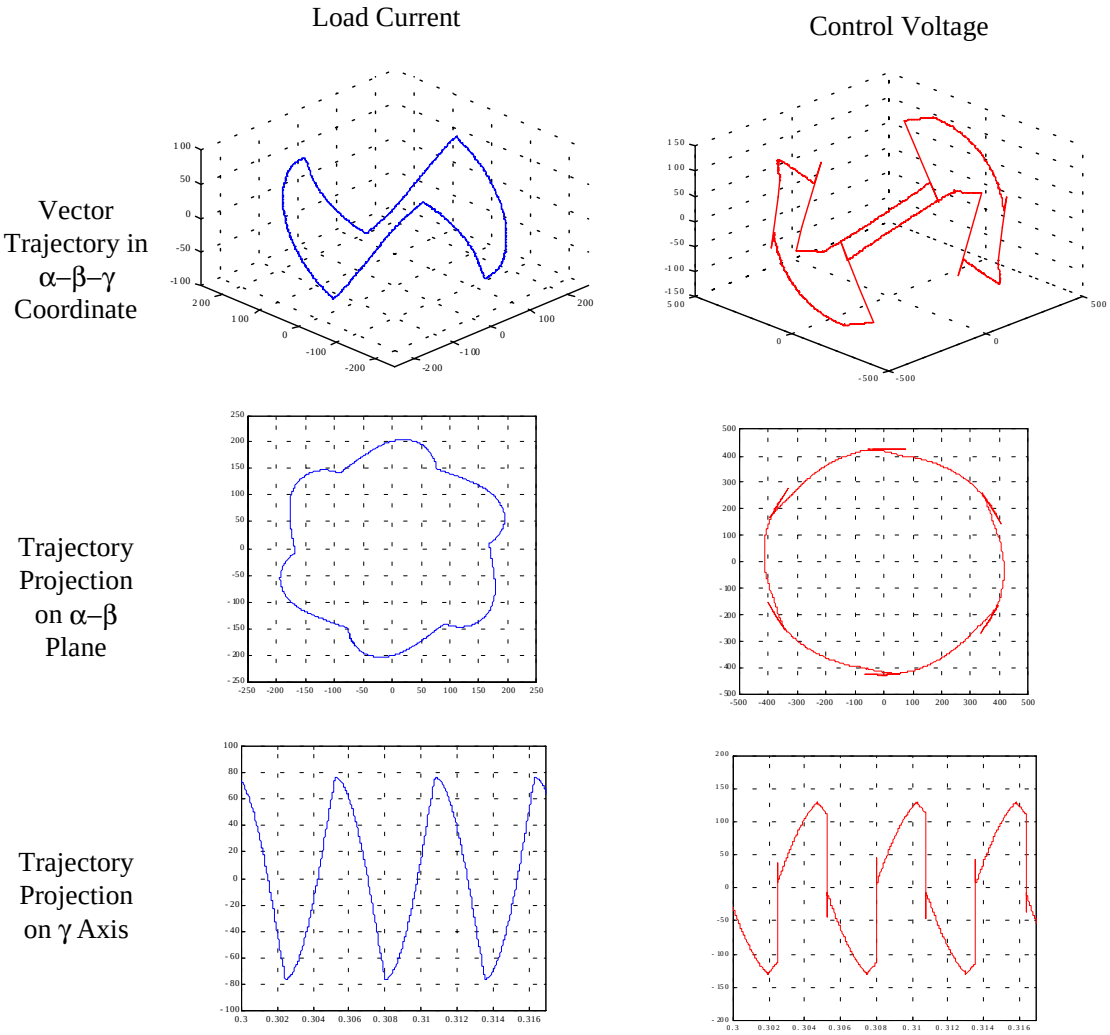


Figure 3-42 Steady state load current and control voltage vector trajectories in α–β–γ coordinate with three single-phase diode bridge rectifiers with L/C filter

(L = 1 mH, C = 21 mF, ESR_C = 250 mOhm, R = 2.7 Ohm per phase)

3.5.3 Power Flow Analysis under Unbalanced Load

The complex power consumed by an arbitrary three-phase load is expressed as:

$$S = [V_{AG} \quad V_{BG} \quad V_{CG}] \cdot [I_{LA} \quad I_{LB} \quad I_{LC}]^T \qquad (3.44)$$

where V_{AG}, V_{BG} and V_{CG} are balanced three-phase voltages. Substituting (3.31) into (3.44) yields:

$$S = P_p + P_n + P_0 \qquad (3.45)$$

where P_p is the positive-sequence power determined by the positive-sequence load current, and expressed as

$$P_p = [V_{AG} \quad V_{BG} \quad V_{CG}] \cdot [I_{LA\_p} \quad I_{LB\_p} \quad I_{LC\_p}]^T \qquad (3.46)$$

P_p is a constant at the steady state consisting of two items: first, the active power consumed by the load; second, the reactive power, a circulating power between the load and the source. The reactive power is caused by a non-unity power factor. This reactive power does not affect the design of the DC link capacitance, however, it affects the current rating of the power switches.

P_n is the negative-sequence power determined by the negative-sequence load current, and expressed as

$$P_n = [V_{AG} \quad V_{BG} \quad V_{CG}] \cdot [I_{LA\_n} \quad I_{LB\_n} \quad I_{LC\_n}]^T \qquad (3.47)$$

P_n is an AC ripple power with 2ω frequency circulating between the load and the source. Since this ripple power makes the energy drawn from the DC capacitor fluctuate at a 2ω frequency, it is the major concern when designing the DC link capacitance.

P_0 is the zero-sequence power, and expressed as

(3.48) $$P_0 = \begin{bmatrix} V_{AG} & V_{BG} & V_{CG} \end{bmatrix} \cdot \begin{bmatrix} I_0 & I_0 & I_0 \end{bmatrix}^T$$

It can be seen from (3.48) that the zero-sequence power P_0 is always zero. The physical meaning of the zero P_0 is that the zero-sequence load current exchanges energy among three phase loads such that the three-phase load can be viewed as a node with no energy exchange with the outside world. Therefore, equivalently, it can be viewed as a zero-sequence current freewheeling through three inductors; the power loss associated with this freewheeling is zero. Zero-sequence power does not affect the DC link capacitor design. It only affects the design of the neutral leg.

3.5.4 Design Example of a Four-Legged Inverter

3.5.4.1 Specifications

The design targets of the three-phase four-legged inverter are as follows:

- Output voltage: 277 V (line-to-neutral)
- Output frequency: 60 Hz
- Output voltage THD: < 3% (balanced linear load)

  < 5% (unbalanced linear load, nonlinear load)
- Output power: 150 kW (three-phase)
- Maximum per-phase power: 50 kW
- Load power factor range: [-0.8, +0.8]
- Load unbalance: negative-sequence unbalance ≤ 100 %

  zero-sequence unbalance ≤ 33 %
- Load current crest factor ≤ 2

3.5.4.2 DC Link Voltage

In a practical design, the selection of the DC link voltage V_g is a trade-off between power switch voltage stress and control headroom for transients. The negative-sequence reference voltage, hence, the negative-sequence load current, imposes a significant impact on the selection of the dc link voltage. This can be seen by projecting the reference control voltage vector trajectory on the $\alpha-\beta$ plane, as shown in Figure 3-43 (a). Since each projected switching vector has a length of $\frac{2}{3}V_g$, the size of the hexagon is determined by the DC link voltage. Under a balanced load, the maximum steady state control voltage vector trajectory is the inscribed circle of the hexagon with a radius of $\frac{1}{\sqrt{3}}V_g$. Considering a 10% control overhead for transient, for a 277 line-to-neutral output AC voltage, the resulted DC link voltage would be $277 \cdot \sqrt{2} \cdot \sqrt{3} \cdot 110\% = 746\text{V}$. It seems that a 750 V DC bus would be enough. However, it can be seen from Figure 3-43 (a) that if V_g is designed for balanced loads, under an unbalanced load the desired reference vector may exceed the controllable region confined by the hexagon, and thus will not be able to be synthesized by switching vectors. The result is an unbalanced and/or distorted three-phase output voltage. To accommodate the negative-sequence control voltage, the major radius of the ellipse should be confined within the inscribed circle of the hexagon. That can be expressed as

$$|\mathbb{V}_p| + |\mathbb{V}_n| \le \frac{1}{\sqrt{3}}V_g \qquad \textbf{(3.49)}$$

From (3.41), (3.42) and (3.49), the maximum allowed positive-sequence load current versus the negative-sequence load current curve can be plotted for a given DC link voltage, as shown in Figure 3-43 (b). All the load conditions below the curve is permitted for the certain voltage. The shaded area in Figure 3-43 (b) shows all the possible load conditions in terms of positive and negative-sequence currents given by the specifications. It can be seen that 750 V DC link voltage, which was enough for balanced load condition, may not be enough for an unbalanced load, since part of the load region can not be covered by the curve. A 780 V DC link voltage is barely enough for all

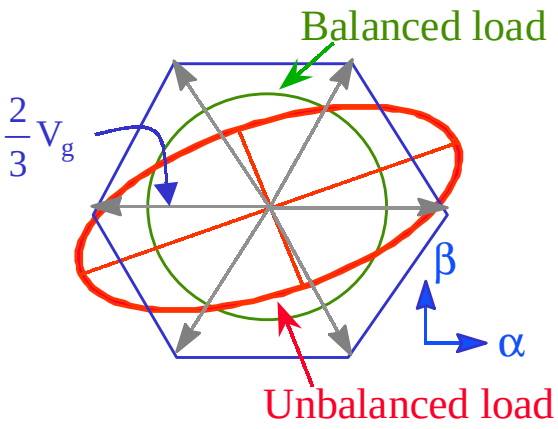
possible loads. Considering the voltage drop on the ESR of the output filter inductor under heavy load and a control overhead, finally 800 V DC link voltage is used.

3.5.4.3 DC Link Capacitance

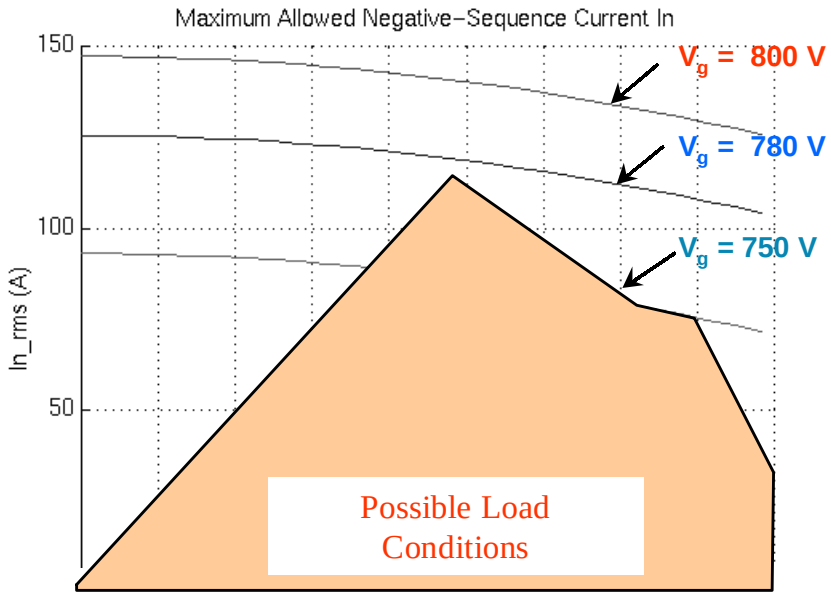
Since the zero-sequence load current will be handled by the fourth neutral leg, only the negative-sequence load current is reflected to the DC link capacitor. Design of the DC link capacitance can use (3.13). Considering 100% negative-sequence unbalance, and 16 V of the maximum allowed voltage ripple – 2% of the rated DC link voltage, the resulting DC link capacitance is 15.5 mF.

3.5.4.4 Switching Frequency

Switching frequency needs to be selected as high as possible from a control point of view, as long as there is no thermal issue. In order to find the optimum switching frequency, switching losses of power devices need to be evaluated. The gate driver and power stage layout impose great impacts on the switching behavior of power devices. With 1.5 Ohm gate resistance, laminated bus structure, and voltage clamp snubber, Figure 3-44 shows turn-on and turn-off characteristics of Powerex 1200V/600A IGBT CM600HA-24H under a 400 V DC link voltage and a 350 A switched current. The anti-parallel diode reverse recovery current during turn-on can be seen in Figure 3-44 (a). There are two voltage spikes during turn-off, as shown in Figure 3-44 (b). The first voltage spike is caused by the forward recovery voltage drop of the opposite diode and the $\frac{di}{dt}$ voltage drop on the module parasitic inductance. The second spike is the $\frac{di}{dt}$ voltage drop on the layout parasitic inductance being clamped by the snubber circuit. The test results under an 800 V DC link voltage and a 350 A switched current are shown in Figure 3-45 and Figure 3-46. Comparing Figure 3-44 with Figure 3-45 and Figure 3-46, it can be seen that the percentage ratio of the first spike during turn-off becomes smaller in high voltage test condition. This is governed by the device characteristic.



(a)



(b)

Figure 3-43 Criteria for DC link voltage selection

(a) the size of the hexagon determined by the DC link voltage also confines the controllable region; (b) permitted positive-sequence and negative-sequence load current under difference DC link voltages, and the possible load condition

The instantaneous power losses are shown as the second trace from the bottom. The turn-on or turn-off switching energies are shown as the last trace for each graph. To help design engineers to parallel IGBTs, manufacturers, such as Powerex, label each device based on its conduction voltage drop. For example, the conduction voltage drop at 25 °C for type H device ranges from 2.75 V ~ 3.05 V; and it ranges from 2.5 V ~ 2.8 V for type G device. Figure 3-45 shows switching characteristics for type G device, while Figure 3-46 shows switching characteristics for type H device. The turn-on, turn-off and total switching energies are shown in Figure 3-47. The total switching energy curve is approximated by a linear curve, which is then plugged into a spreadsheet program to calculate the switching loss over a line cycle. It can be seen that type H device has lower switching time, thus, less switching losses. However, it is preferred to use type G device due to its less conduction loss. Moreover, it can be seen from the device test results shown in Figure 3-45 and Figure 3-46 that the voltage spike of type G device during turn-off is also smaller than that of type H device. The voltage spike is critical for high voltage applications. The fact of a slower turn-off, lower turn-off voltage spike and less conduction loss for type G device, and a faster turn-off, higher turn-off voltage spike and more conduction loss for type H device, reflects the design tradeoff of the power semiconductor devices.

Based on the estimated conduction loss and the switching losses, a 5 kHz switching frequency is selected, which results in a 180 W per-module switching loss. Under a 55 °C ambient temperature and the cooling condition, the estimated junction temperature is 135 °C with the switching losses and 260 W conduction loss, .

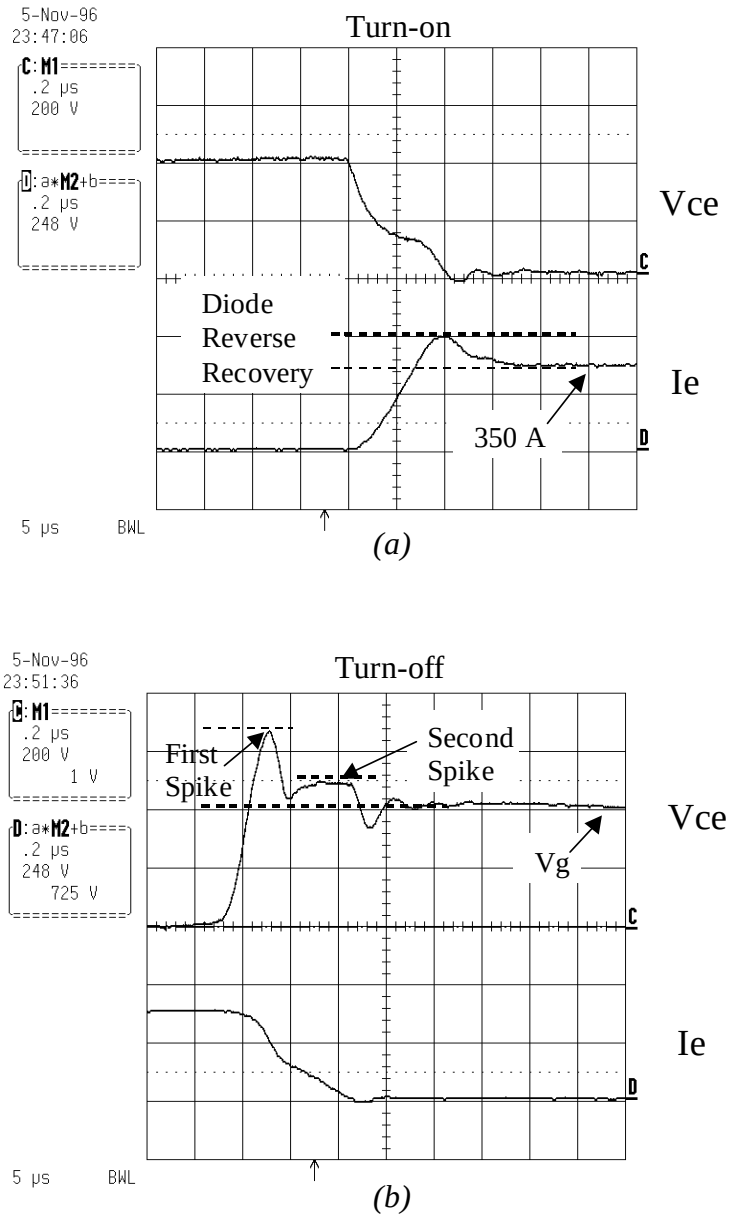
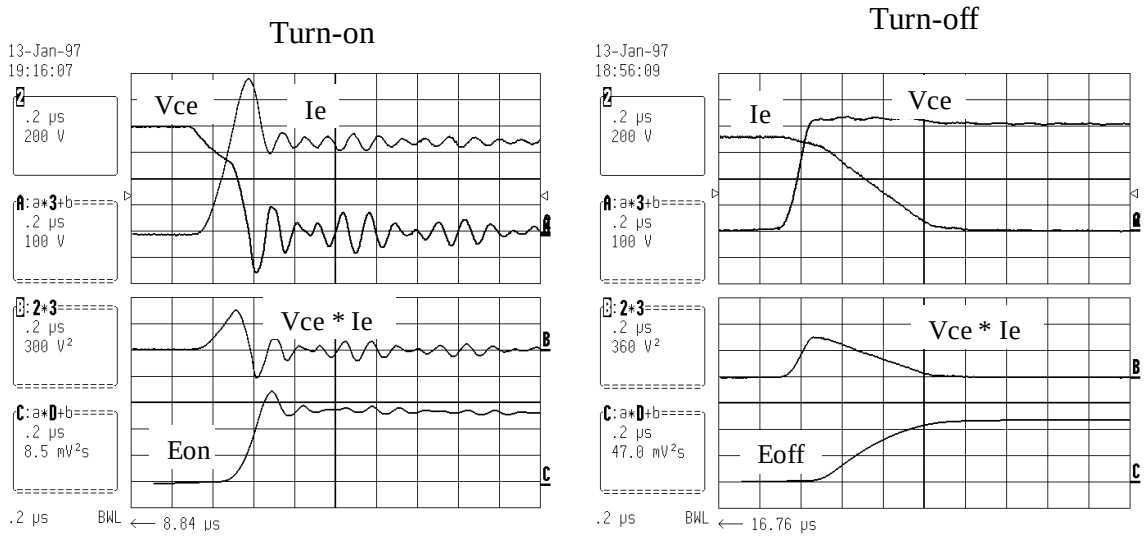


Figure 3-44 IGBT device CM600HA-24H test waveforms at 400 V DC

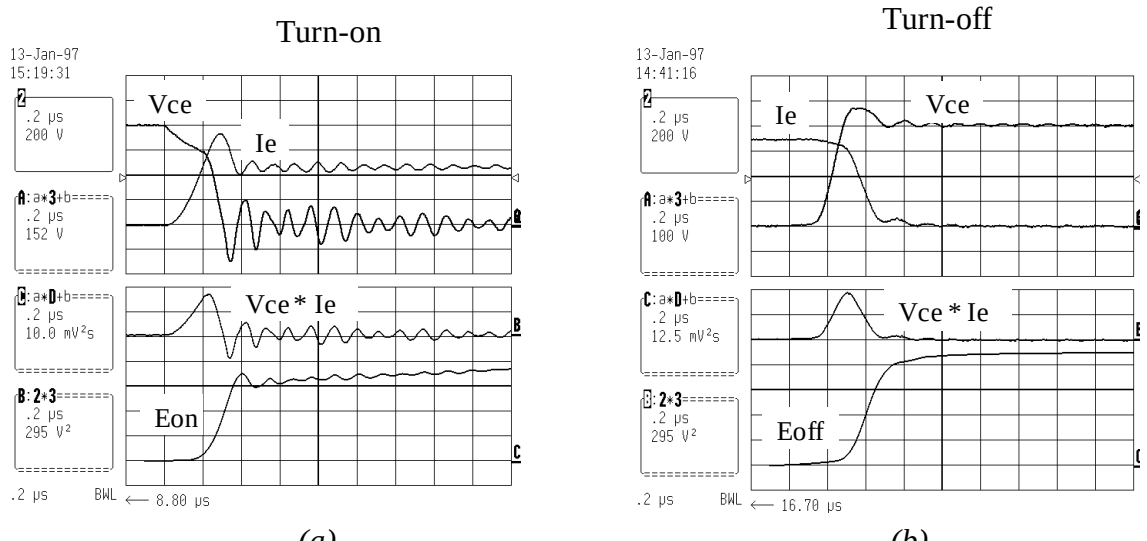
(a) turn-on at 350 A; (b) turn-off at 350 A



(a) *(b)*

Figure 3-45 IGBT device CM600HA-24H (type G) test waveforms at 800 V DC

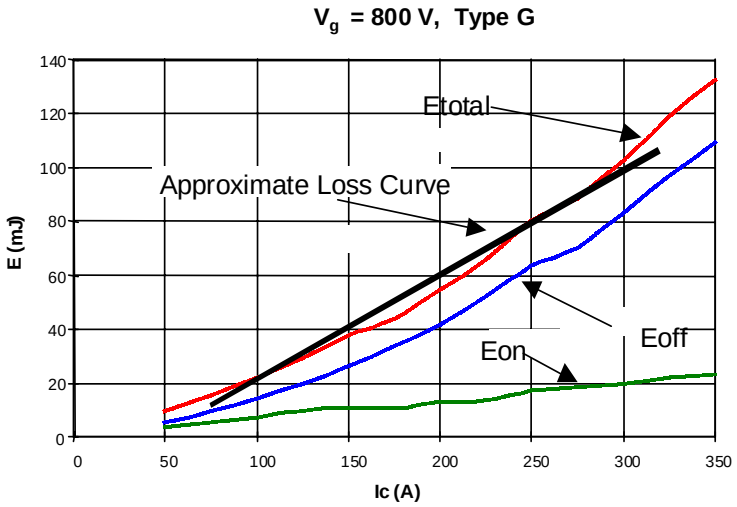
(a) turn-on at 350 A; (b) turn-off at 350 A



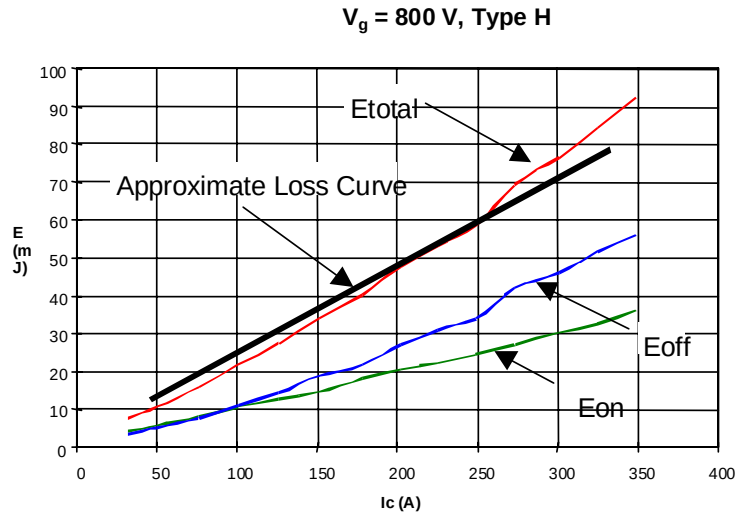
(a) *(b)*

Figure 3-46 IGBT device CM600HA-24H (type H) test waveforms at 800 V DC

(a) turn-on at 350 A; (b) turn-off at 350 A



(a)



(b)

Figure 3-47 Switching loss curves for IGBT CM600HA-24H

(a) type G; (b) type H

3.5.4.5 AC Output Filter

L and C form a 2nd-order filter with -40 dB/dec attenuation to the switching ripples. With the 5 kHz switching frequency, the resonant frequency f_{res} is selected as 500 Hz to have less than 1% of voltage ripple at the switching frequency. Neglecting the neutral inductor L_n, the worst case peak-to-peak inductor current ripple is determined by

$$I_{pp} = \frac{V_g}{L \cdot f_{sw}} |D| \cdot (1 - |D|) \qquad \textbf{(3.50)}$$

where D is the line-to-neutral duty ratio in a line cycle. In steady state, D is found as

$$D = \frac{V_{ln\_pk}}{V_g} \sin(\omega t) \qquad \textbf{(3.51)}$$

where V_{ln_pk} is the peak of the line-to-neutral voltage.

L is designed at 660 μH to have a 24% current ripple The current ripple is defined as the peak-to-peak ripple current (61A) over the peak of the rated output current (255 A). The resulted peak-to-peak current ripple in a line cycle is shown in Figure 3-48.

The filter capacitance C is easily calculated to be 153 uF from (3.52).

$$C = \left(\frac{1}{2\pi f_{res}} \right)^2 \frac{1}{L} \qquad \textbf{(3.52)}$$

Due to capacitor ESR, current through the filter capacitor will produce loss. It is normally desirable to have less than 10% of the rated load current going through the capacitor. In the rated operation point, capacitor current is 15.7 Arms, which is 8.7% of the rated load current. Neutral inductor L_n can further reduce the inductor current ripple. With L_n designed at 330 μH, the inductor current ripple can be further reduced by approximately 30% with the symmetrical aligned class II sequencing strategy.

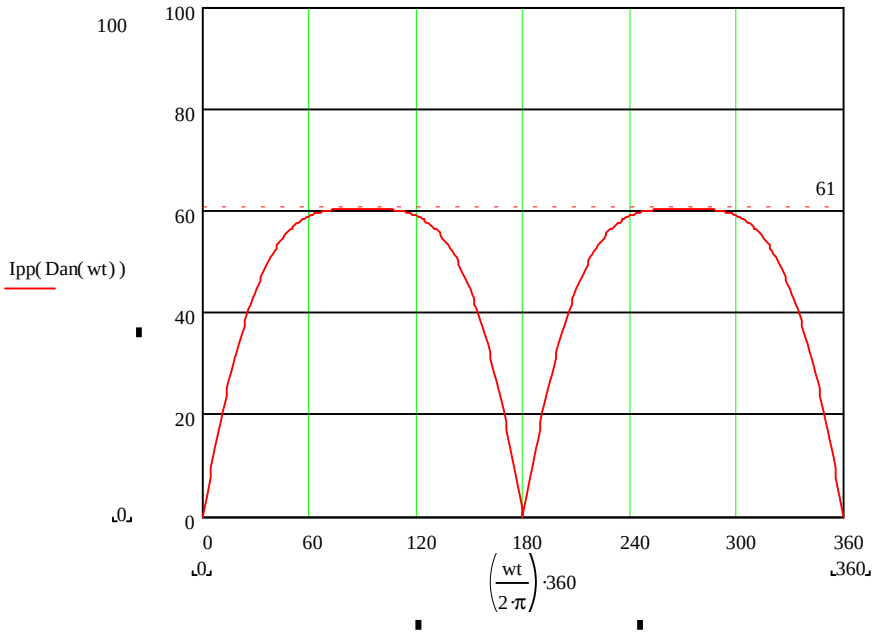


Figure 3-48 Worst case peak-to-peak inductor current ripple in a line cycle

3.5.4.6 Power Switches in the Neutral Leg

The neutral current, which flows through the neutral leg, equals three times the zero-sequence load current. With 33% specified zero-sequence unbalance, the zero-sequence current is the same as the rated per-phase current. Thus, the power switches in the neutral leg are the same as in three phase legs.

3.7 Simulation and Experimental Results for Four-Legged Power Converters

3.7.1 Simulation and Experimental Results for Four-Legged Inverter

3.7.1.1 Balanced Load

A balanced linear load is used for open loop simulation. The total power level is 150 kW with 180.5 A per-phase load current. With the symmetrical aligned class II sequencing scheme, the four-legged switching network AC terminal voltages are shown in Figure 3-49. The three-phase output line-to-neutral voltages and the neutral current are shown in Figure 3-50. The output voltage THD turns out to be 2.3%, which satisfies the specification. Despite the current ripple, the average neutral current for the balanced load is zero.

The prototype has been tested open loop up to 100 kW. The output voltage waveforms are shown in Figure 3-51 (a). From the output voltage frequency spectrum, shown in Figure 3-51 (b), it can be seen that there are two distinct harmonic contents at the 5^{th} and 7^{th} harmonics, and two harmonics around the switching frequency, $f_{sw} - f_{line}$ and $f_{sw} + f_{line}$. The 5^{th} harmonic is 34 dB less than the 60 Hz fundamental component; the 7^{th} harmonic is 43 dB less than the fundamental component; the two harmonics around the switching frequency are more than 52 dB less than the fundamental component. The tested neutral current is shown in Figure 3-52. It can be seen that although the peak-to-peak current ripple is less than 40 A, the average current is almost zero.

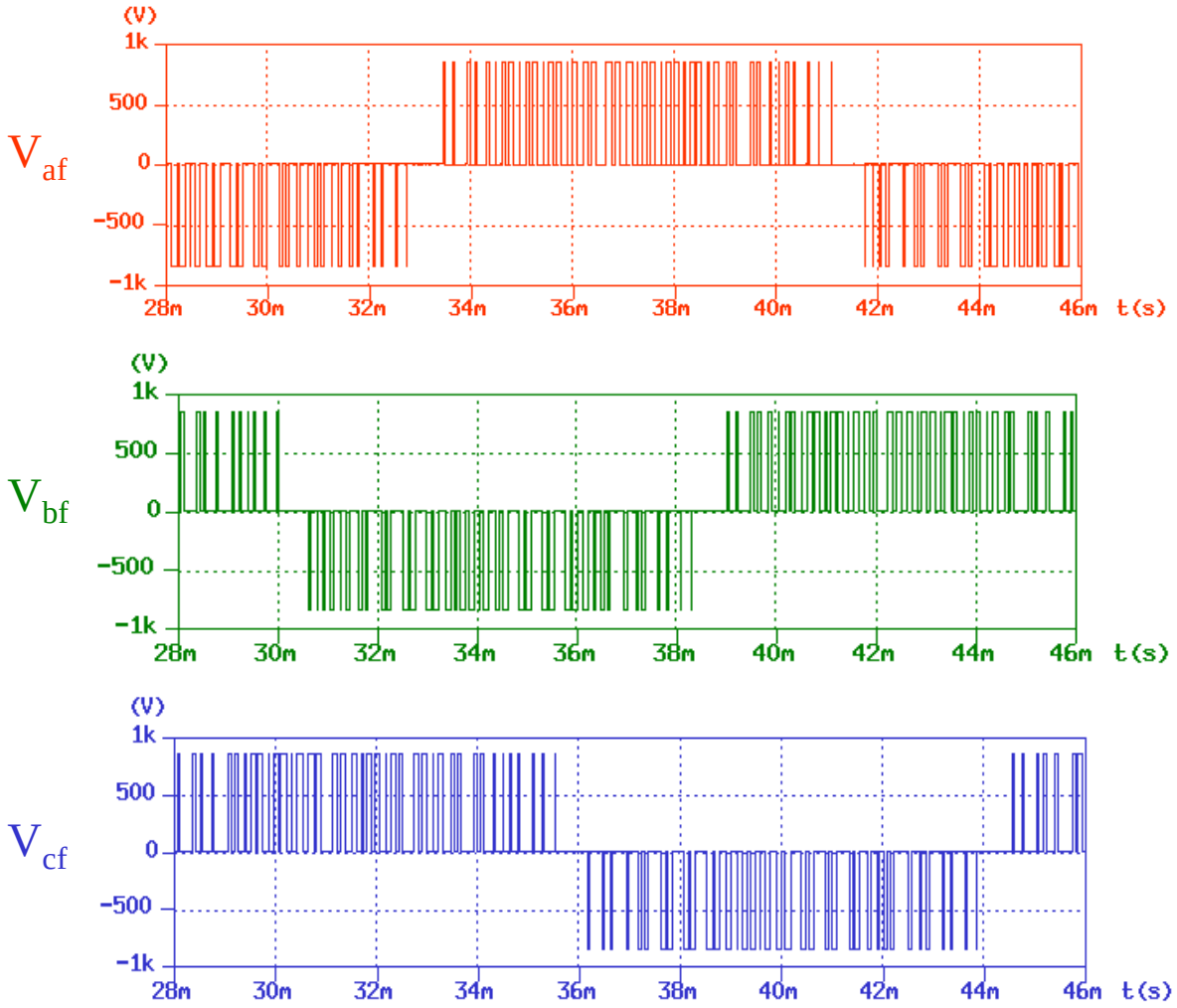


Figure 3-49 Simulated four-legged switching network AC terminal voltages with a balanced linear load

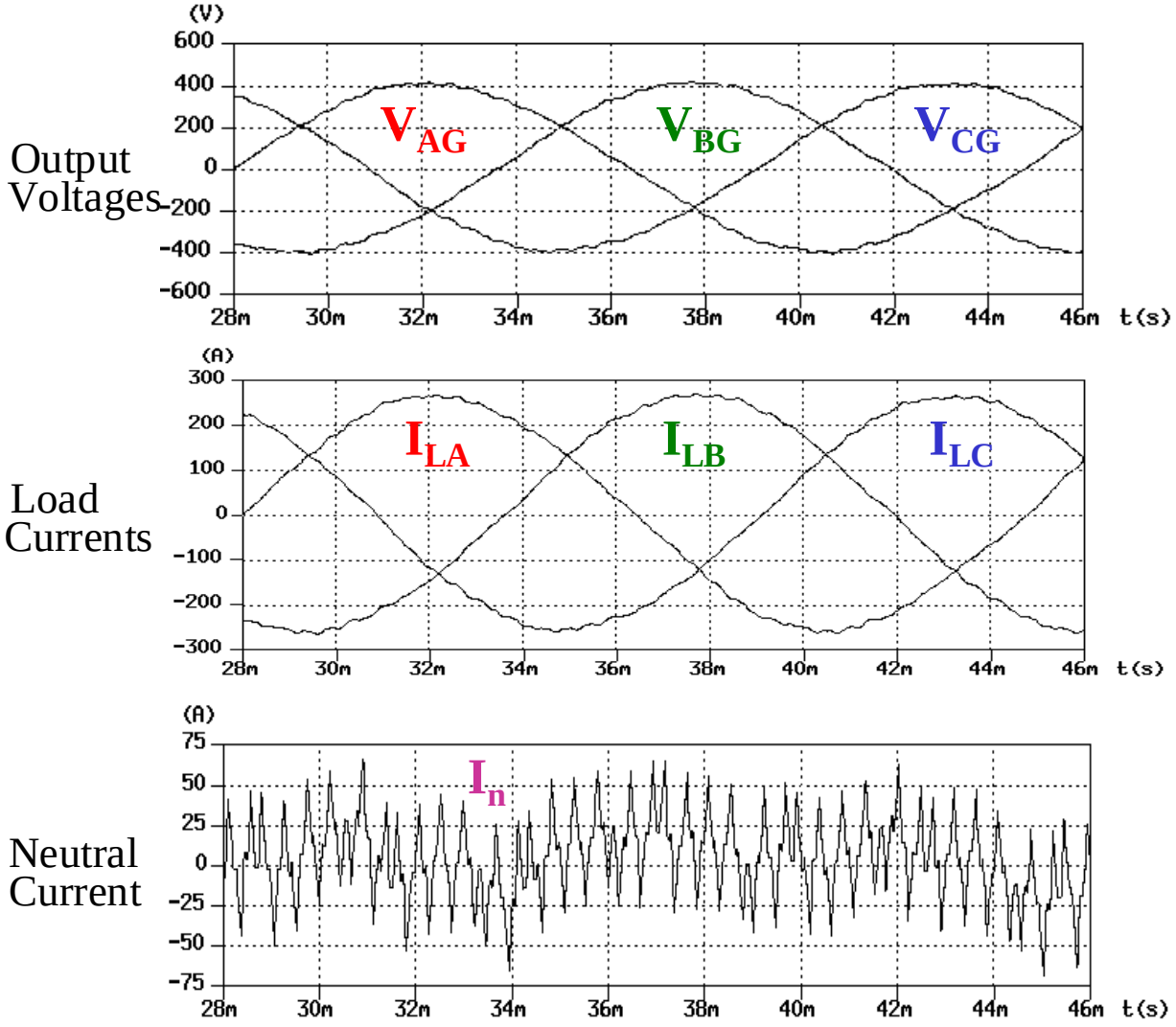
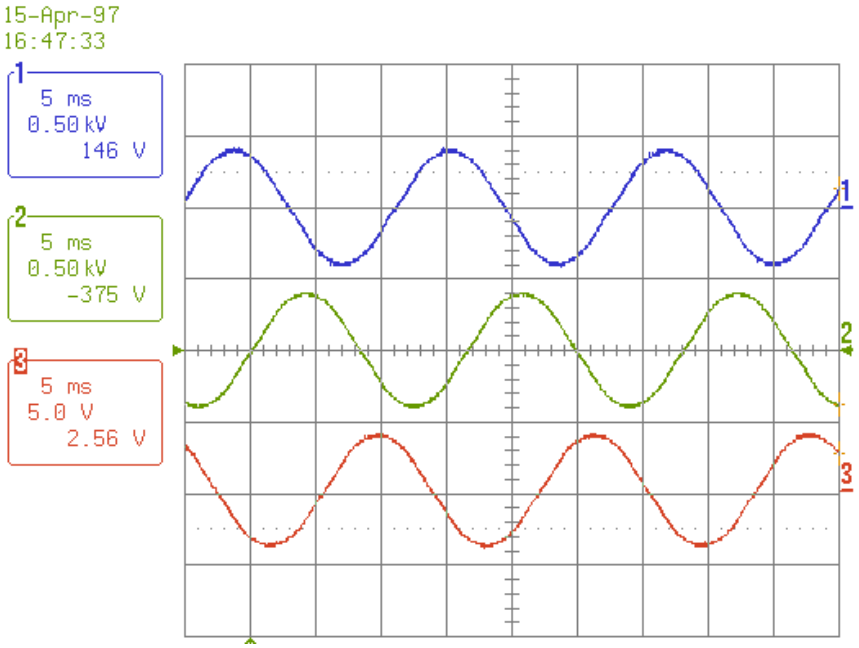
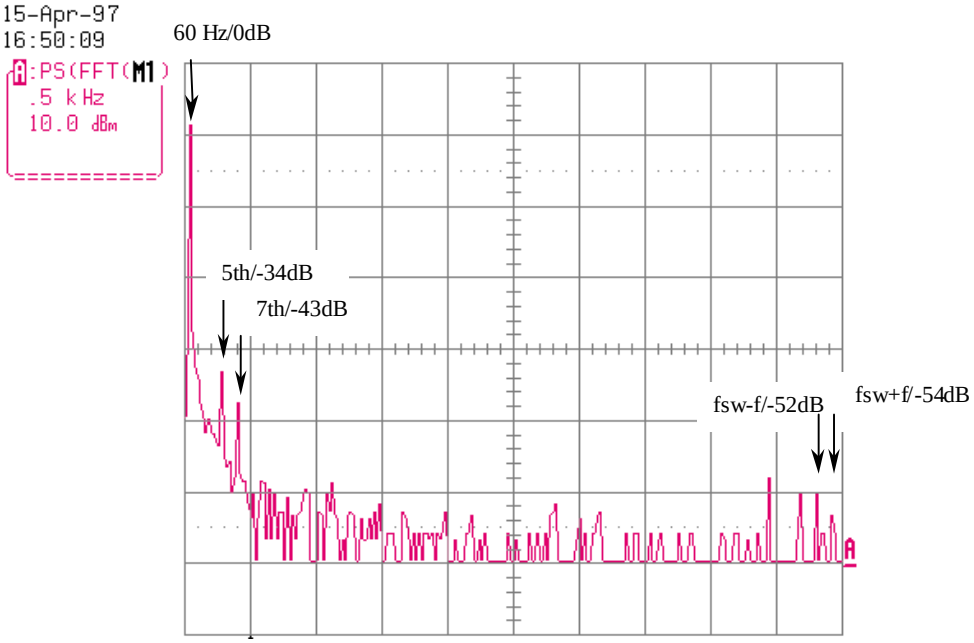


Figure 3-50 Simulated output voltages and the neutral current with a balanced linear load



(a)



(b)

Figure 3-51 Experimental output voltages with 100 kW balanced linear load

(a) output voltage waveforms; (b) output voltage frequency spectrum

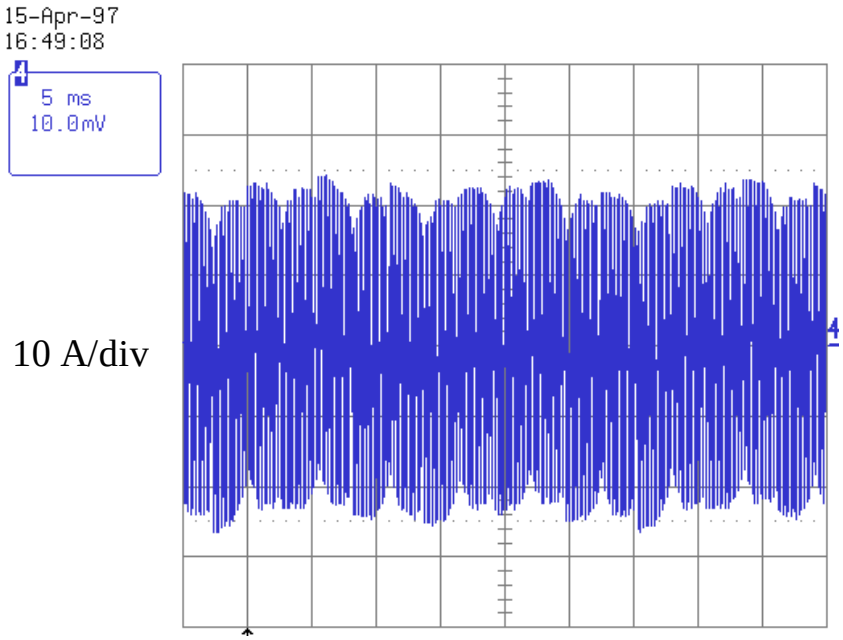


Figure 3-52 Experimental neutral current with a 100 kW balanced linear load

3.7.1.2 Unbalanced Load

Open loop simulations for an unbalanced load with $I_A = 180\angle 0^o$ A, $I_B = 90\angle -90^o$ A, and $I_C = 90\angle -240^o$ A are conducted. The unbalanced load results in a neutral current of 135 A. The reference control vector trajectory at steady state, a skewed ellipse in the α–β–γ coordinate, is pre-calculated based on the known unbalanced load. Figure 3-53 shows the simulated four-legged switching network AC terminal voltages with the symmetrical aligned class II sequencing scheme. The three-phase output line-to-neutral voltages and the neutral current are shown in Figure 3-54. The output voltage THD turns out to be 4.8%, which satisfies the specification.

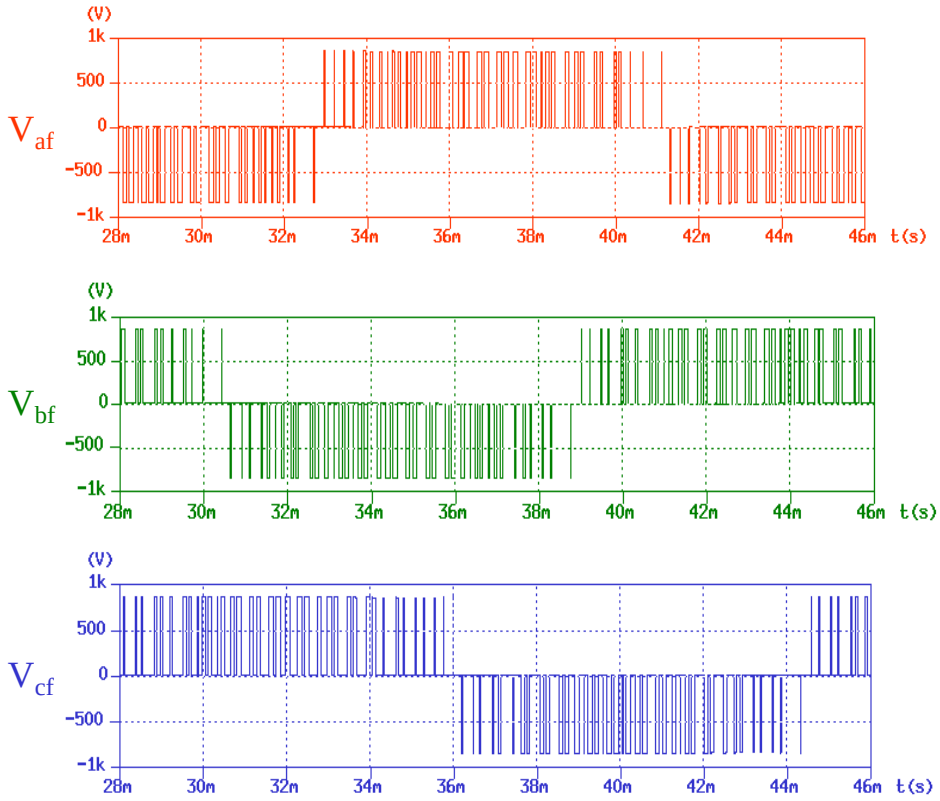


Figure 3-53 Simulated four-legged switching network AC terminal voltages with an unbalanced linear load

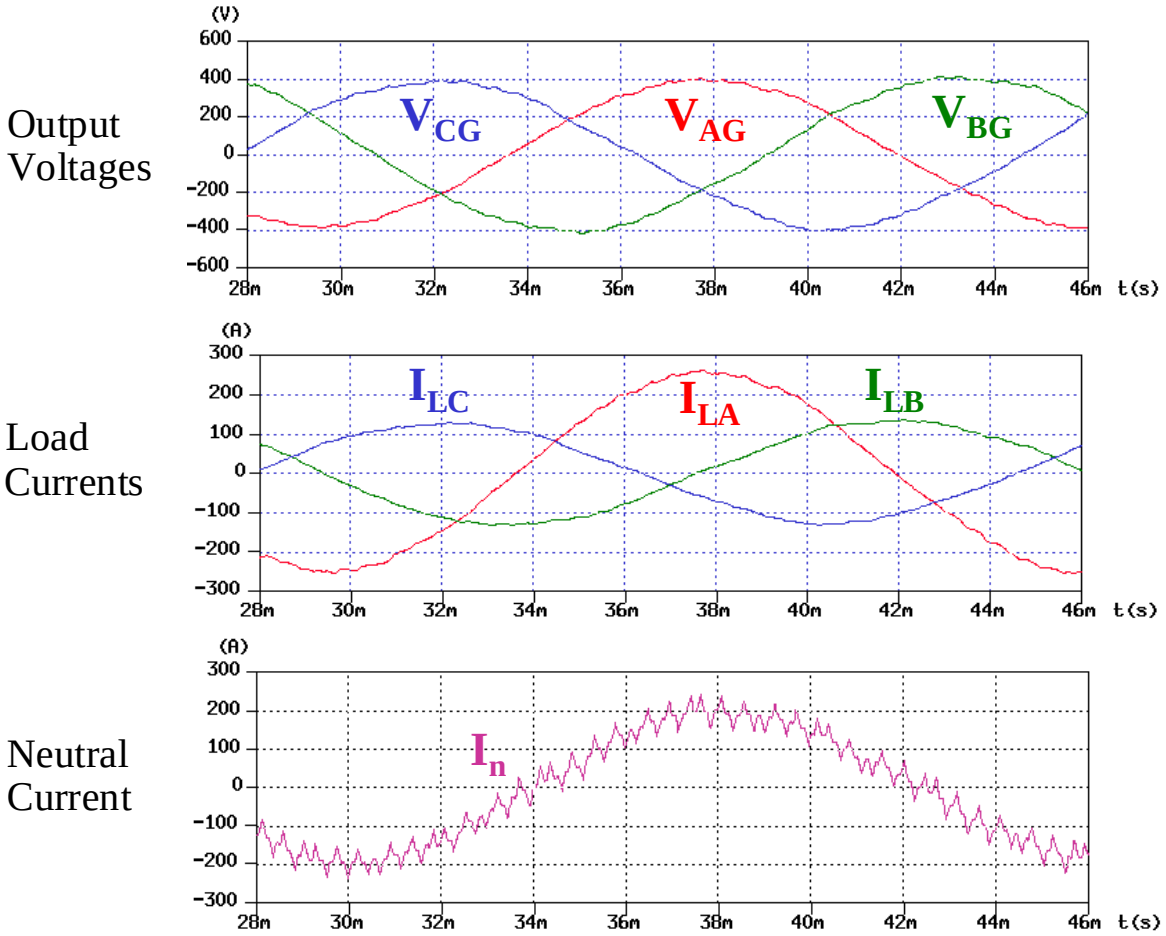


Figure 3-54 Simulated output voltages and the neutral current with an unbalanced linear load

3.7.1 Experimental Results for Four-Legged PWM PFC Rectifier

A four-legged PWM rectifier, as shown in Figure 3-20, is tested. Figure 3-55 shows the phase A input voltage and three phase input currents. It can be seen that the three phase input currents are close to three phase sinusoidal; the phase A input current is in phase with the input voltage.

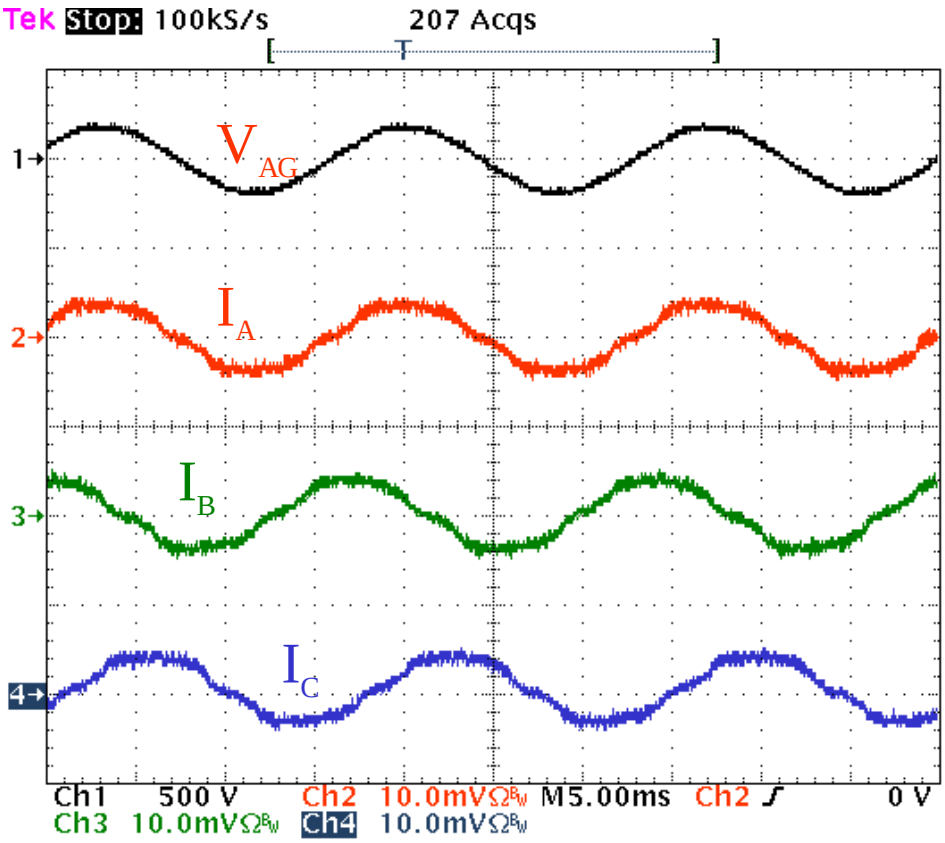


Figure 3-55 Experimental waveforms of a four-legged PWM PFC rectifier

– Phase A input voltage and three-phase input currents (20 A/div)

3.8 Conclusions

In this chapter, four-legged PWM power converters are proposed to handle the neutral current due to unbalanced and/or nonlinear load in a three-phase four-wire system. They can be used as inverter, rectifier or active filter. Detailed analysis and design guidelines are given for a four-legged inverter.

After a comprehensive review of the existing PWM schemes, it is concluded that two-dimensional space vector modulation schemes are the best choice for a high performance three-legged power converter. The space vector modulation scheme has the advantages of high DC link voltage utilization, low output distortion and harmonic contents, possibility to optimize for lower switching losses and/or distortion, and compatibility with digital controller.

Three-dimensional space vector modulation schemes, which are supersets of conventional two-dimensional space vector modulation schemes, are proposed for the four-legged power converters. Simulation and experimental results are given for both the balanced and unbalanced load for the four-legged inverter. Experimental results are also given for a four-legged PWM rectifier. All the simulation and experimental results prove the validity of the proposed three-dimensional space vector modulation schemes.

Chapter 4 Modeling and Control of Four-Legged Converters in d-q-o Rotating Coordinate

4.1 Introduction

In this chapter, average large signal models of four-legged voltage source inverter and PFC rectifier in the d-q-o rotating coordinate are given. Small signal models are derived by perturbing the large signal models at the operating point. Control loop designs based on the small signal models are performed. The unbalanced and nonlinear loads are also modeled in the d-q-o coordinate, which makes clear the challenges the control design faces when the load is unbalanced and/or nonlinear. Simulation and experimental results show performance of the four-legged voltage source inverter under different load conditions with the voltage loop closed. The fault tolerant operation of the four-legged PWM rectifier is demonstrated by simulation results.

4.2 Modeling of Four-Legged Power Converters in a-b-c Coordinate

4.2.1 Modeling of Four-Legged Inverter in a-b-c Coordinate

Neglecting all the circuit parasitic components, and assuming the switching frequency is much higher than the fundamental frequency so that all the voltage and current ripples are negligible, the "in-place" circuit averaging technique can be used to get the average large-signal circuit model from the switching model [H1~2]. For a four-legged inverter, the average large-signal circuit model is shown in Figure 2-23. Assuming the DC link voltage is an ideal voltage source V_g, the control voltage sources V_{af}, V_{bf}, V_{cf} can be expressed as

$$\begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} = V_g \begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} \quad \textbf{(4.1)}$$

where d_{af}, d_{bf}, and d_{cf} are line-to-neutral duty ratios. The differential equations describing inductor currents and the output capacitor voltages in the circuit model are expressed as

$$\frac{d}{dt}\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \frac{L_n}{L}\frac{d}{dt}\begin{bmatrix} I_n \\ I_n \\ I_n \end{bmatrix} + \frac{V_g}{L}\begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} \quad \textbf{(4.2)}$$

$$I_a + I_b + I_c + I_n = 0 \quad \textbf{(4.3)}$$

$$\frac{d}{dt}\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} = \frac{1}{C}\left\{\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} - \begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix}\right\} \quad \textbf{(4.4)}$$

where I_{LA}, I_{LB}, and I_{LC} are three phase load currents. The DC rail current is expressed as

$$I_p = \begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix}\begin{bmatrix} I_a & I_b & I_c \end{bmatrix}^T \quad \textbf{(4.5)}$$

There are several difficulties to control such a system. First, it can be seen from (4.2) and (4.4) that the system is a complicated six-order multiple-input-multiple-output system. It has a total of six state variables, including three inductor currents – I_a, I_b, and I_c, and three output capacitor voltages – V_{AG}, V_{BG}, and V_{CG}. It has three line-to-neutral duty ratios – d_{af}, d_{bf}, and d_{cf} as inputs, and three voltages – V_{AG}, V_{BG}, and V_{CG} as outputs. Second, it is known from the steady state analysis in Section 3.5.2 that the steady state solution for all the variables are sinusoidal. Due to the time varying nature of the model in a-b-c coordinate, there is no DC operating point. Therefore, there is no small-

signal model available for control loop design. The effort to design three independent compensators for three phases in a-b-c coordinate is often a trial-error process and leads to an ambiguity of stability and dynamic performance. Although there are some control methods that are not based on the small-signal model, such as hysteresis control, they suffer from poor performance due to conflict among three phase compensators.

4.2.2 Modeling of Four-Legged PWM Rectifier in a-b-c Coordinate

Assuming input to the rectifier is an ideal three-phase voltage source, the differential equations describing the average large-signal circuit model of the four-legged PWM rectifier shown in Figure 3-24, are expressed as

$$\frac{d}{dt}\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \frac{L_n}{L}\frac{d}{dt}\begin{bmatrix} I_n \\ I_n \\ I_n \end{bmatrix} - \frac{V_g}{L}\begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} \quad \textbf{(4.6)}$$

$$\frac{dV_g}{dt} = \frac{1}{C}\left(\begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix}\begin{bmatrix} I_a & I_b & I_c \end{bmatrix}^T - I_L\right) \quad \textbf{(4.7)}$$

where I_L is the load current of the DC link. (4.1), (4.3) and (4.5) are still valid for the four-legged rectifier model. It can be seen that it is a fourth order multiple-input-single-output system. The total four state variables include three inductor currents – I_a, I_b, and I_c, and the voltage across the DC link capacitor – V_g. Three inputs are line-to-neutral duty ratios – d_{af}, d_{bf}, and d_{cf}. The output is the DC link voltage – V_g. Since all the state variables in steady state are time varying, it shares the same difficulties as the four-legged inverter in control design in a-b-c coordinate.

4.3 Coordinate Transformation

It is pointed out in Section 3.5 that the steady state solution of a four-legged inverter can be represented by a rotating vector in the three-dimensional orthogonal coordinate α–β–γ. With an ideal balanced linear load, the vector rotates on the α–β plane at the line frequency ω. Its trajectory draws a circle. The rotating motion represents the

time varying nature of the system. When we view the system in the d-q coordinate rotating at the synchronized line frequency ω, as shown in Figure 4-1, the steady state solution of the system becomes a fixed vector in the rotating coordinate. Therefore, the system viewed in the rotating coordinate becomes a time-invariant system in the d-q coordinate. The transformation from three-phase variable in α–β–γ to d-q-o is expressed as

$$\begin{bmatrix} X_d & X_q & X_o \end{bmatrix}^T = T_3 \cdot \begin{bmatrix} X_\alpha & X_\beta & X_\gamma \end{bmatrix}^T \quad \textbf{(4.8)}$$

where the coordinate transformation matrix T_3 is expressed as

$$T_3 = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \textbf{(4.9)}$$

After the transformation, axes d and q rotate on the α–β plane, while o is essentially the preserved γ axis.

Combining T_2 and T_3, coordinate transformation from the a-b-c coordinate to the rotating d-q-o coordinate is expressed as

$$\begin{bmatrix} X_d & X_q & X_o \end{bmatrix}^T = T_4 \cdot \begin{bmatrix} X_a & X_b & X_c \end{bmatrix}^T \quad \textbf{(4.10)}$$

where the transformation matrix is

$$T_4 = \frac{2}{3}\begin{bmatrix} \cos\omega t & \cos(\omega t - \frac{2}{3}\pi) & \cos(\omega t + \frac{2}{3}\pi) \\ -\sin\omega t & -\sin(\omega t - \frac{2}{3}\pi) & -\sin(\omega t + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \textbf{(4.11)}$$

The inverse transformation from the d-q-o coordinate to the a-b-c coordinate is found to be

$$\begin{bmatrix} X_a & X_b & X_c \end{bmatrix}^T = T_4 \cdot \begin{bmatrix} X_d & X_q & X_o \end{bmatrix}^T \quad \textbf{(4.12)}$$

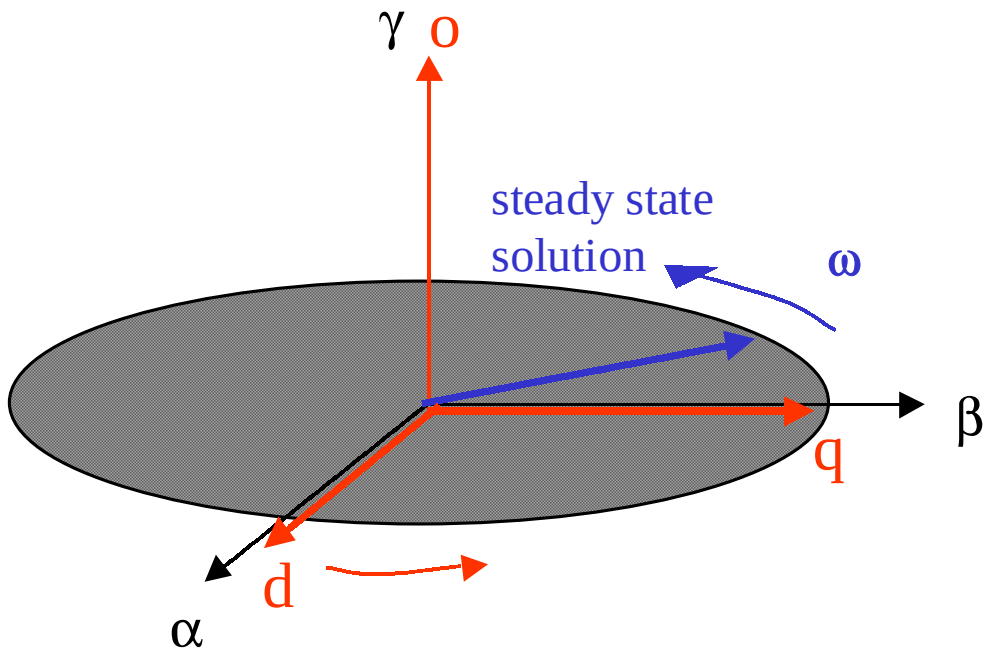


Figure 4-1 Relationship between the α–β–γ and d-q-o coordinate

where the inverse transformation matrix is

$$\textbf{(4.13)} \qquad T_4^{-1} = \begin{bmatrix} \cos\omega t & -\sin\omega t & 1 \\ \cos(\omega t - \frac{2}{3}\pi) & -\sin(\omega t - \frac{2}{3}\pi) & 1 \\ \cos(\omega t + \frac{2}{3}\pi) & -\sin(\omega t + \frac{2}{3}\pi & 1 \end{bmatrix}$$

In fact, the rotating coordinate transformation was first proposed by R. H. Park in 1929 to analyze a synchronous machine. Therefore, it is also called Park transformation.

For a four-legged inverter, applying the Park transformation to the three phase variables, we have output capacitor voltage in the d-q-o coordinate expressed as

$$\textbf{(4.14)} \qquad \begin{bmatrix} V_d & V_q & V_o \end{bmatrix}^T = T_4 \begin{bmatrix} V_{AG} & V_{BG} & V_{CG} \end{bmatrix}^T;$$

inductor current in the d-q-o coordinate expressed as

$$\textbf{(4.15)} \qquad \begin{bmatrix} I_d & I_q & I_o \end{bmatrix}^T = T_4 \begin{bmatrix} I_a & I_b & I_c \end{bmatrix}^T;$$

load current in the d-q-o coordinate expressed as

$$\textbf{(4.16)} \qquad \begin{bmatrix} I_{Ld} & I_{Lq} & I_{Lo} \end{bmatrix}^T = T_4 \begin{bmatrix} I_{LA} & I_{LB} & I_{LC} \end{bmatrix}^T;$$

and line-to-neutral duty ratios expressed as

$$\textbf{(4.17)} \qquad \begin{bmatrix} d_d & d_q & d_o \end{bmatrix}^T = T_4 \begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix}^T$$

4.4 Modeling of Four-Legged Power Converters in d-q-o Coordinate

4.4.1 Modeling of Four-Legged Inverter in d-q-o Coordinate

The average large-signal model of a four-legged inverter in the d-q-o coordinate can be obtained by applying the coordinate transformation matrix T_4 to both sides of (4.2), (4.4), and (4.5). Considering (4.14) ~ (4.17) and noting that

(4.18) $$T_4\begin{bmatrix} I_n & I_n & I_n \end{bmatrix}^T = \begin{bmatrix} 0 & 0 & -3I_o \end{bmatrix}^T$$

(4.19) $$T_4 \frac{dX_{abc}}{dt} = T_4 \frac{dT_4^{-1}}{dt} X_{dqo} + \frac{dX_{dqo}}{dt}$$

and

(4.20) $$T_4 \frac{dT_4^{-1}}{dt} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

the resulting four-legged inverter model in d-q-o coordinate is expressed as

(4.21) $$\frac{d}{dt}\begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix} = V_g G \begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} - G \begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} + \omega \begin{bmatrix} I_q \\ -I_d \\ 0 \end{bmatrix}$$

(4.22) $$\frac{d}{dt}\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \omega \begin{bmatrix} V_q \\ -V_d \\ 0 \end{bmatrix} + \frac{1}{C}\left\{ \begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix} - \begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{Lo} \end{bmatrix} \right\}$$

$$\text{where } G = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L + 3L_n} \end{bmatrix}$$

The dc rail current is expressed as

(4.23) $$I_P = \begin{bmatrix} \frac{3}{2}d_d & \frac{3}{2}d_q & 3d_o \end{bmatrix} \begin{bmatrix} I_d & I_q & I_o \end{bmatrix}^T$$

The state space model can be also obtained by rewriting equations (4.21) ~ (4.22), and expressed as

(4.24) $$\dot{X} = AX + BU + DW$$

where $X = \begin{bmatrix} V_d & I_d & V_q & I_q & V_o & I_o \end{bmatrix}^T$ are state variables; $U = \begin{bmatrix} d_d & d_q & d_o \end{bmatrix}^T$ are control input variables; $W = \begin{bmatrix} I_{Ld} & I_{Lq} & I_{Lo} \end{bmatrix}^T$ are purturbations; system matrix are expressed as

(4.25) $$A = \left[\begin{array}{cc:c} A_{dd} & A_{dq} & 0 \\ A_{qd} & A_{qq} & 0 \\ \hdashline 0 & 0 & A_{oo} \end{array}\right]_{6x6}$$

(4.26) $$B = \left[\begin{array}{cc:c} B_{dd} & 0 & 0 \\ 0 & B_{qq} & 0 \\ \hdashline 0 & 0 & B_{oo} \end{array}\right]_{6x3}$$

(4.27) $$D = \left[\begin{array}{cc:c} D_{dd} & 0 & 0 \\ 0 & D_{qq} & 0 \\ \hdashline 0 & 0 & D_{oo} \end{array}\right]_{6x3}$$

where $$A_{dd} = A_{qq} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix}_{2x2}, \qquad A_{oo} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L + 3L_n} & 0 \end{bmatrix}_{2x2},$$

$$A_{dq} = -A_{qd} = \omega I_2$$

$$B_{dd} = B_{qq} = \begin{bmatrix} 0 \\ \frac{V_g}{L} \end{bmatrix}_{2x1}, \; B_{oo} = \begin{bmatrix} 0 \\ \frac{V_g}{L + 3L_n} \end{bmatrix}_{2x1}, \; D_{dd} = D_{qq} = D_{oo} = \begin{bmatrix} -\frac{1}{C} \\ 0 \end{bmatrix}_{2x1}$$

It can be seen from (4.25) and (4.26) that the system can be partitioned into two sub-systems. While d and q channels are coupled through A_{dq} and A_{qd}, the o channel is completed decoupled from d and q channels. Due to the decoupling of d-q channels and o channel, the studied system order is reduced in d-q-o coordinate. The physical explanation to the decoupled d-q and o sub-systems is that the zero-sequence component is only in the o channel, and is independent of positve and negative-sequence components.

To facilitate analysis using circuit simulation tools and to have a better physical understanding of the model, a circuit model is developed based on (4.21) ~ (4.23), as shown in Figure 4-2. It is very clear that the inverter is partitioned into two subsystems. The o channel is a second-order system, similar to a dc/dc buck converter, while d and q channels are coupled together, and become a fourth-order system. The d and q channel inductor currents are coupled into q and d channels in a form of controlled voltage sources, ωLI_d and ωLI_q, in series with the inductors. The d and q channel capacitor voltages are coupled into q and d channels in a form of controlled current sources, ωCV_d and ωCV_q, in parallel with the capacitors. In the d-q subsystem, if the coupling sources could be decoupled, the whole system will be similar to three independent dc/dc buck converters. All the control strategies studied for dc/dc converters will be applicable. The coupling voltage sources, ωLI_d and ωLI_q, can be decoupled easily since they are in a direct series with the controlled voltage sources d_dV_g and d_qV_g. However, since the

control variables do not have a direct control on the coupling current sources ωCV_d and ωCV_q, the coupling current sources cannot be easily decoupled.

4.4.2 Steady State Analysis of Four-Legged Inverter in d-q-o Coordinate

In steady state, the output voltage should follow the desired reference, which is expressed as

$$\begin{bmatrix} V_d & V_q & V_o \end{bmatrix}^T = \begin{bmatrix} V_{ln\_pk} & 0 & 0 \end{bmatrix}^T \quad \textbf{(4.28)}$$

By setting $\dot{X} = 0$, the steady state solution can be obtained in the d-q-o coordinate. The steady state inductor currents are found as

$$\begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix} = \begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{Lo} \end{bmatrix} + V_{ln\_pk} \begin{bmatrix} 0 \\ \omega C \\ 0 \end{bmatrix} \quad \textbf{(4.29)}$$

The steady-state duty ratios are found as

$$\begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} = \frac{G^{-1}}{V_g} \cdot \frac{d}{dt} \begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{Lo} \end{bmatrix} + \frac{L\omega}{V_g} \begin{bmatrix} -I_{Lq} \\ I_{Ld} \\ 0 \end{bmatrix} + \frac{V_{ln\_pk}}{V_g} \begin{bmatrix} 1 - LC\omega^2 \\ 0 \\ 0 \end{bmatrix} \quad \textbf{(4.30)}$$

It should be noted that the steady state duty ratios are functions of differentiation of load currents. Assuming the load is a balanced linear load, the load currents in d-q-o will be constants, therefore, (4.30) can be simplified as

$$\begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} = \frac{L\omega}{V_g} \begin{bmatrix} -I_{Lq} \\ I_{Ld} \\ 0 \end{bmatrix} + \frac{V_{ln\_pk}}{V_g} \begin{bmatrix} 1 - LC\omega^2 \\ 0 \\ 0 \end{bmatrix} \quad \textbf{(4.31)}$$

With a balanced linear load, it is clear from (4.28), (4.29) and (4.31) that all the steady state variables are constants, which specify the DC operating point. The small-

signal model can be obtained by perturbing the system around the DC operating point, as shown in Figure 4-5, where the label '^' denotes perturbation. Since circuit simulation softwares, such as PSPICE and SABER, could perform the perturbation automatically around the given DC operating point, in practice, the large-signal average model shown in Figure 4-2 can be directly used to plot transfer functions. With a digital controller, additional sampling delay should be included in the model, which is discussed in Section 4.5

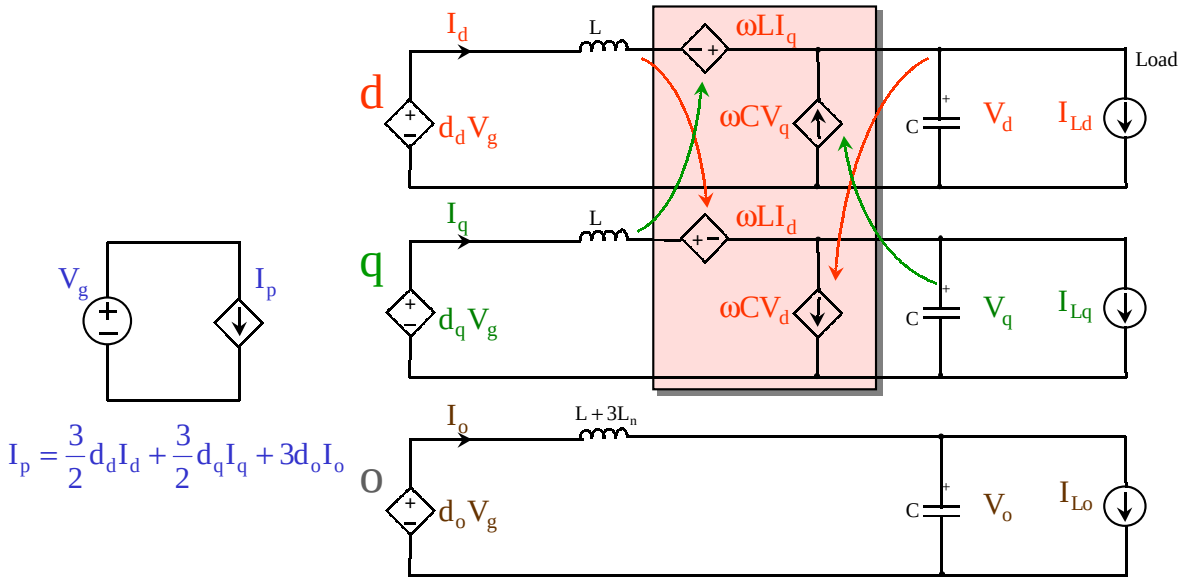


Figure 4-2 Average large-signal circuit model of a four-legged inverter in d-q-o coordinate

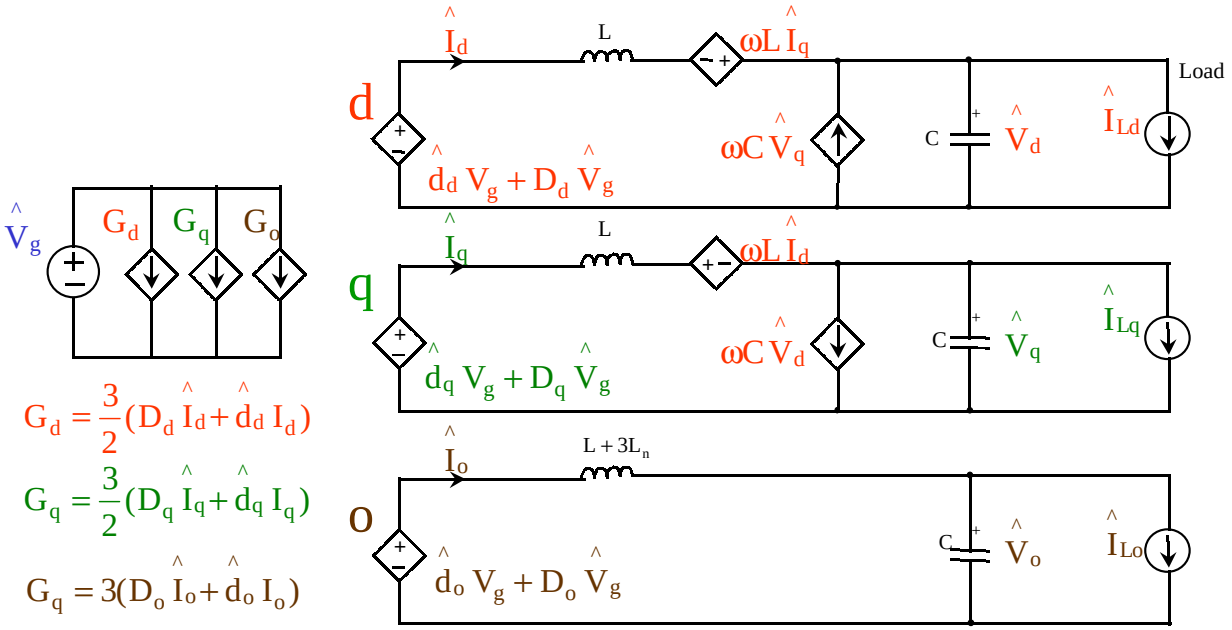


Figure 4-3 Small-signal circuit model of a four-legged inverter in d-q-o coordinate

4.4.3 Modeling of Four-Legged Rectifier in d-q-o Coordinate

Applying the coordinate transformation matrix T_4 to both sides of (4.6) and (4.7), meanwhile considering (4.18) ~ (4.20), the average large-signal model of a four-legged rectifier in d-q-o coordinate is expressed as

(4.32)
$$\frac{d}{dt}\begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix} = -V_g G \begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} + G \begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} + \omega \begin{bmatrix} I_q \\ -I_d \\ 0 \end{bmatrix}$$

(4.33)
$$\frac{dV_g}{dt} = \frac{1}{C}\left(\begin{bmatrix} \frac{3}{2}d_d & \frac{3}{2}d_q & 3d_o \end{bmatrix} \begin{bmatrix} I_d & I_q & I_o \end{bmatrix}^T - I_L \right)$$

The circuit model is developed according to (4.32) and (4.33), and is shown in Figure 4-4. It can be seen that it is a fourth order system. D and q channels are coupled through two current controlled voltage sources.

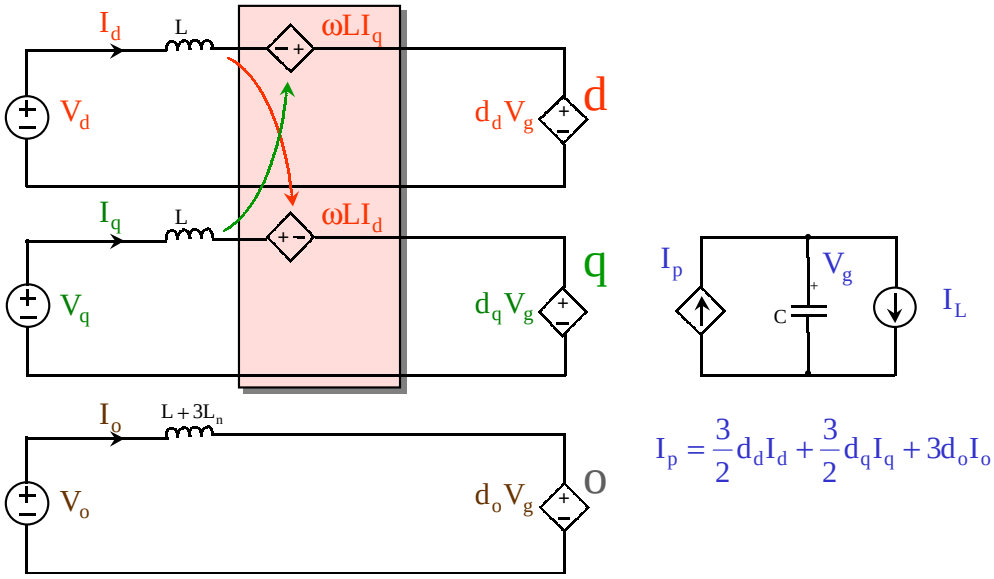


Figure 4-4 Average large-signal model of a four-legged PWM rectifier in d-q-o coordinate

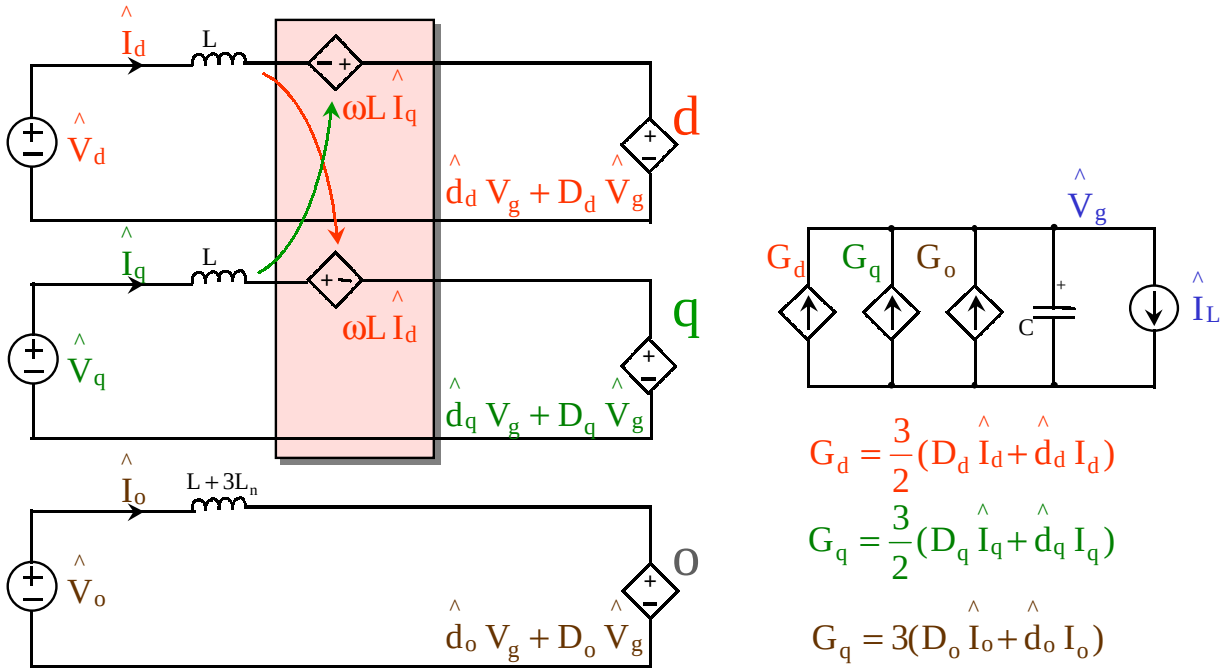


Figure 4-5 Small-signal model of a four-legged PWM rectifier in d-q-o coordinate

4.4.4 Steady State Analysis of Four-Legged Rectifier in d-q-o Coordinate

For the sake of convenience, the d axis is aligned with the $V_{AG.}$ Therefore, we have $V_d = V_{ln\_pk}$, $V_q = V_o = 0$. To achieve PFC operation, in the steady state, input currents I_a, I_b and I_c are in phase with V_{AG}, V_{BG} and V_{CG}, respectively. Thus, we have $I_d = I_m$, $I_q = I_o = 0$, where I_m is the peak of the phase current. By setting the left-hand side of (4.32) and (4.33) to zero, the steady state solution is found to be

(4.34)
$$\begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} = \begin{bmatrix} \frac{M}{\sqrt{3}} \\ -\frac{2}{\sqrt{3}}\frac{I_L}{M} \\ 0 \end{bmatrix}$$

where M is the modulation index, I_L is the load current. The steady state solution are constants, which specify the DC operating point. Perturbing the system around the DC operating point, the small signal model of a four-legged PWM rectifier is obtained and shown in Figure 4-5.

4.5 Verification of Model for Four-Legged Inverter

In order to verify the validity of the developed small-signal model of the four-legged inverter, the setup shown in Figure 4-6 has been used to measure the open loop control-to-output-voltage transfer functions. The impedance analyzer HP 4194A outputs a perturbation signal sweeping from 20 Hz to 2 kHz. The analog perturbation signal is fed to the reference channel of the impedance analyzer, and is also converted to a digital signal at a sampling frequency of 5 kHz. The system is perturbed by adding this digitized perturbation to the steady-state duty ratio in a digital signal processor (DSP). The output voltages are measured and then transformed into the d-q-o coordinate. The output voltages in d-q-o coordinate are then converted back to analog signal at a sampling rate

of 20 kHz. Going through a high pass filter formed by a RC network, the signal is fed into the test channel of the impedance analyzer to get the transfer function plot.

The measurement has been taken under a 400 V DC link voltage and a balanced three-phase resistive load with a 6.4 Ohm for each phase. The steady state duty ratios are set to be $d_d = 0.48$, $d_q = d_o = 0$.

It should be noted that due to the digital control, sampling delays are introduced into the model. In this setup, there are three sampling delay sources, (1) A/D conversion, (2) D/A conversion, and (3) space vector modulator. The sampling delays caused by A/D conversion, D/A conversion and its ZOH are obvious. It is shown in [H1] that digital space vector modulator can also cause a sampling delay. The amount of delay caused by the space vector modulator is a complicated function of the modulation index and the position of the reference vector. In the simulation, a total of 400 μs delay time is added to the simulated small-signal model. The total time delay includes a sampling delay of 200 μs caused by A/D conversion, a sampling delay of 50 μs caused by D/A conversion and its ZOH, and an additional average delay of 150 μS caused by the three-dimensional space vector modulation with the symmetrical aligned (class II) sequencing scheme. Since the D/A conversion is only for the purpose of measurement, the time delay caused by the D/A conversion and its ZOH should be excluded from the model when designing the control loops.

The comparison between the simulated and the measured transfer functions are shown in Figure 4-7, Figure 4-8 and Figure 4-9. It can be seen that the simulated direct transfer functions (perturbation and output are in the same channel) V_d/d_d, V_q/d_q and V_o/d_o match the measurements very well. There is a discrepancy between the measured and simulated coupling transfer functions (perturbation and output are not in the same channel) V_q/d_d and V_d/d_q at both the low and high frequency ranges. The discrepancy at the low frequency range may be caused by measurement inaccuracy at very small magnitude. At the higher frequency range, it may be caused by alias due to the limited sampling frequency and measurement inaccuracy at very small magnitude. The decoupling transfer functions have very little effect on the control loop design since the

direct channel transfer functions are more than 20 dB higher than the coupling channel transfer functions at the low and high frequency ranges.

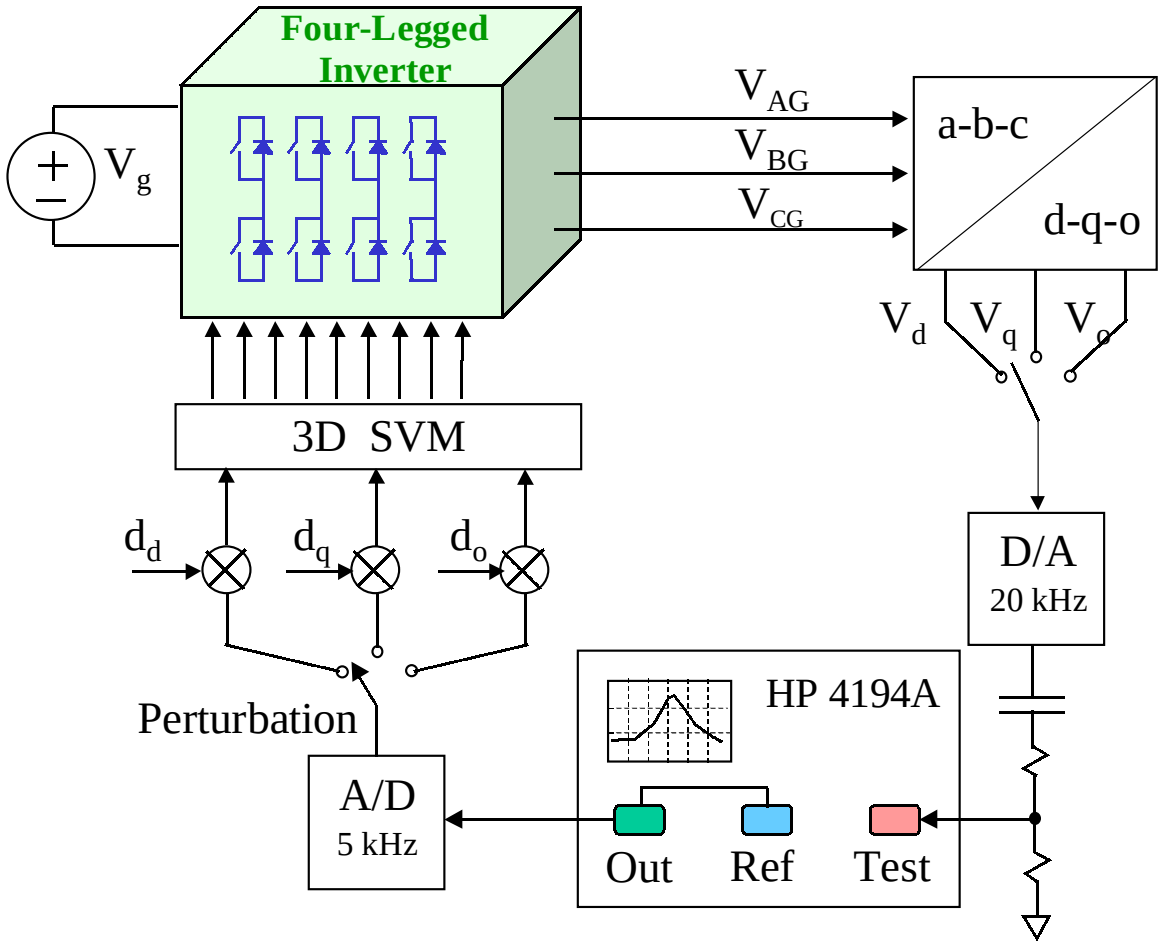


Figure 4-6 Setup for measurement of open loop transfer functions of a four-legged Inverter

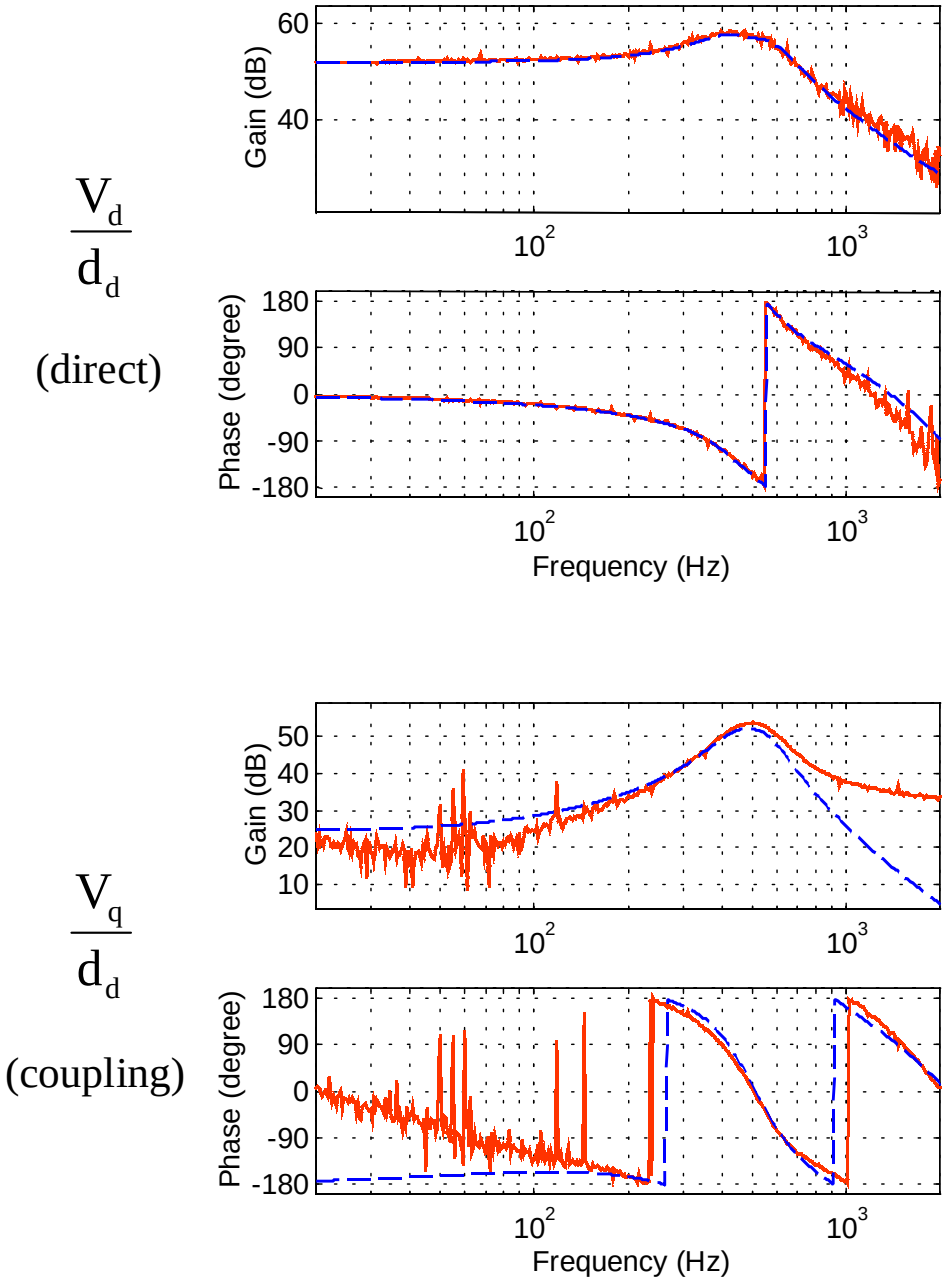


Figure 4-7 Simulated and measured control-to-output voltage transfer functions with d channel perturbation

(simulation: broken line; measurement: solid line)

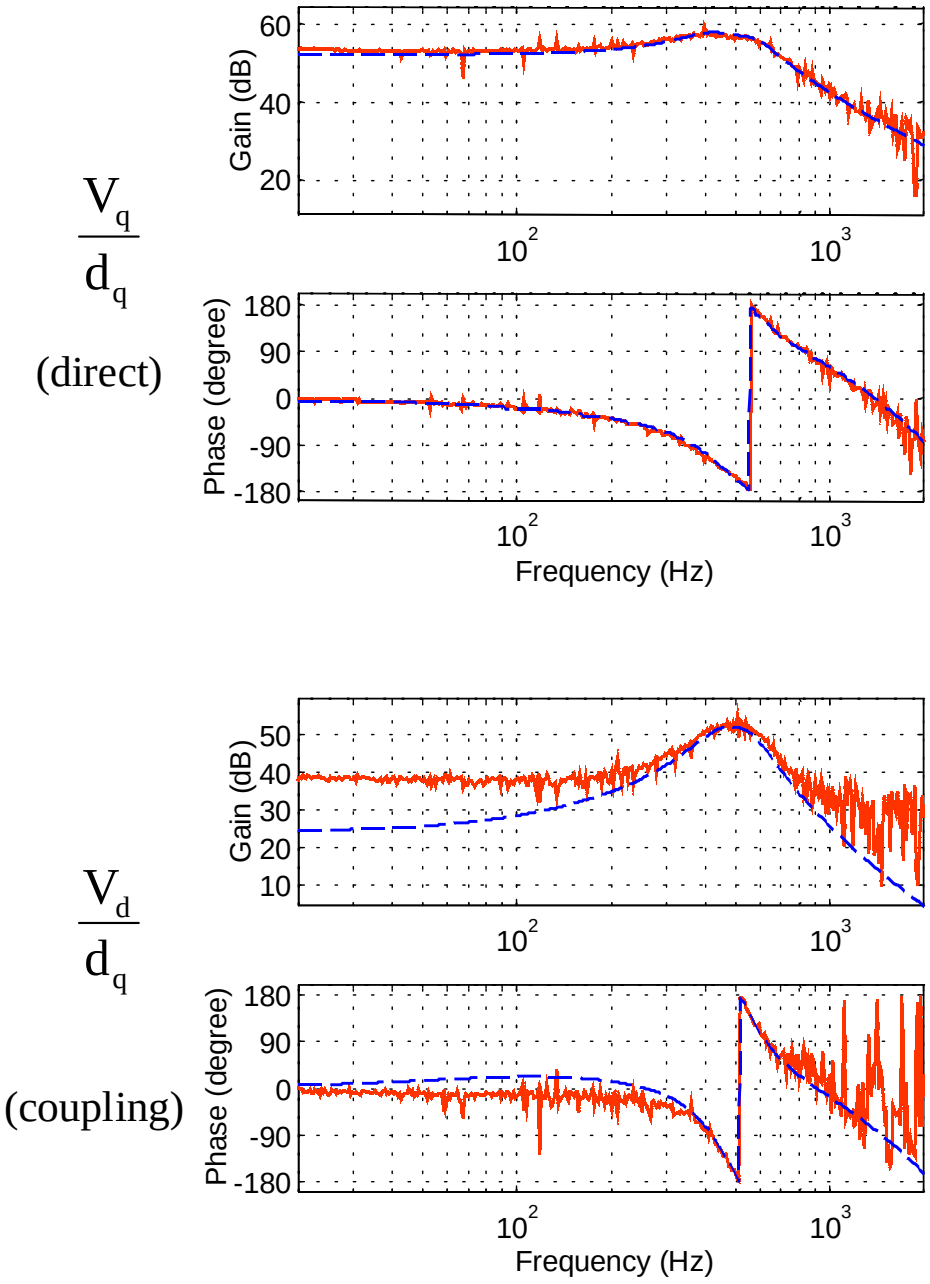


Figure 4-8 Simulated and measured control-to-output voltage transfer functions with q channel perturbation

(simulation: broken line; measurement: solid line)

$$\frac{V_o}{d_o}$$

(direct)

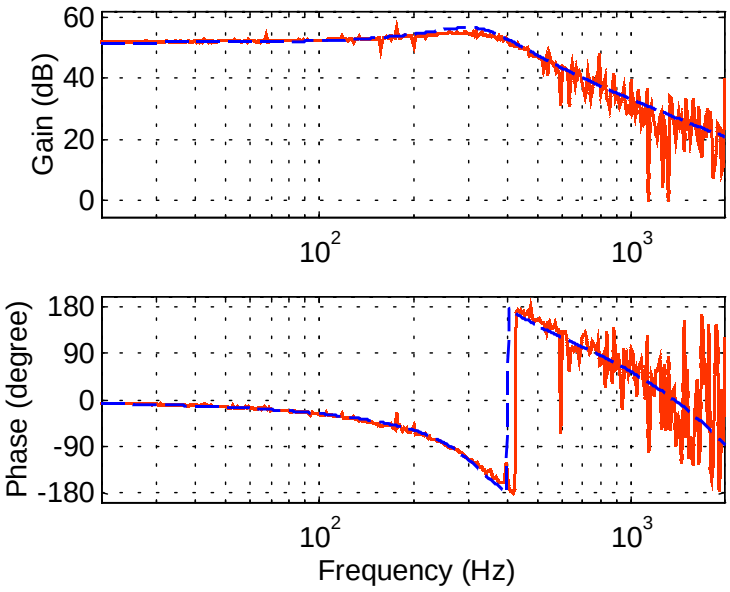


Figure 4-9 Simulated and measured control-to-output voltage transfer functions with o channel perturbation

(simulation: broken line; measurement: solid line)

4.6 Modeling of Unbalanced and Nonlinear Loads in d-q-o Coordinate

The load characteristics have profound impacts on the design of a four-legged inverter. In the a-b-c stationary coordinate, both unbalanced load and nonlinear load have a clear physical meaning, which has been discussed in Chapters 2 and 3. Since the modeling of the four-legged inverter is performed in the rotating d-q-o coordinate, it is necessary to reexamine the load current in the rotating d-q-o coordinate.

4.6.1 Balanced Load in d-q-o coordinate

A balanced load will draw a balanced and positive-sequence three-phase current at the same frequency as the output voltage. It can be expressed as

$$\begin{bmatrix} I_{LA\_p} \\ I_{LB\_p} \\ I_{LC\_p} \end{bmatrix} = I_{m\_p} \begin{bmatrix} \cos(\omega t + \varphi_p) \\ \cos(\omega t - \frac{2}{3}\pi + \varphi_p) \\ \cos(\omega t + \frac{2}{3} + \varphi_p) \end{bmatrix} \quad \textbf{(4.35)}$$

where I_{m_p} is the magnitude of positive-sequence current, φ_p is the phase shift of the positive-sequence current with respect to the output voltage. Applying the coordinate transformation matrix T_4 expressed in (4.11) to both sides of (4.35), the balanced load current in d-q-o coordinate is expressed as:

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{Lo} \end{bmatrix} = \begin{bmatrix} I_{Ld\_p} \\ I_{Lq\_p} \\ I_{Lo\_p} \end{bmatrix} = I_{m\_p} \begin{bmatrix} \cos(\varphi_p) \\ -\sin(\varphi_p) \\ 0 \end{bmatrix} \quad \textbf{(4.36)}$$

The load currents in d and q channels are two dc values, and the load current in o channel is zero.

4.6.2 Unbalanced Load in d-q-o coordinate

Unbalanced load currents can be first decomposed into three sets of balanced currents, namely, positive-sequence, negative-sequence and zero-sequence load current. The positive-sequence current is the same as a balanced load current expressed in (4.35); the negative-sequence current and the zero-sequence current are expressed in (4.37) and (4.38), respectively

$$\begin{bmatrix} I_{LA\_n} \\ I_{LB\_n} \\ I_{LC\_n} \end{bmatrix} = I_{m\_n} \begin{bmatrix} \cos(\omega t + \varphi_n) \\ \cos(\omega t + \frac{2}{3}\pi + \varphi_n) \\ \cos(\omega t - \frac{2}{3} + \varphi_n) \end{bmatrix} \quad \textbf{(4.37)}$$

$$\begin{bmatrix} I_{LA\_0} \\ I_{LB\_0} \\ I_{LC\_0} \end{bmatrix} = I_{m\_0} \begin{bmatrix} \cos(\omega t + \varphi_0) \\ \cos(\omega t + \varphi_0) \\ \cos(\omega t + \varphi_0) \end{bmatrix} \quad \textbf{(4.38)}$$

where I_{m_n} and I_{m_0} are magnitudes of the negative-sequence and zero-sequence load currents; φ_n and φ_0 are phase shifts of the negative-sequence and zero-sequence load currents. Applying the coordinate transformation matrix T_4 to (4.37) and (4.38), the load current in d-q-o can be obtained as

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{Lo} \end{bmatrix} = \begin{bmatrix} I_{Ld\_p} \\ I_{Lq\_p} \\ I_{Lo\_p} \end{bmatrix} + \begin{bmatrix} I_{Ld\_n} \\ I_{Lq\_n} \\ I_{Lo\_n} \end{bmatrix} + \begin{bmatrix} I_{Ld\_o} \\ I_{Lq\_o} \\ I_{Lo\_o} \end{bmatrix} \quad \textbf{(4.39)}$$

while the positive-sequence load current in the d-q-o coordinate $\begin{bmatrix} I_{Ld\_p} & I_{Lq\_p} & I_{Lo\_p} \end{bmatrix}^T$ is expressed in (4.36), the negative-sequence load current in the d-q-o coordinate $\begin{bmatrix} I_{Ld\_n} & I_{Lq\_n} & I_{Lo\_n} \end{bmatrix}^T$ is expressed in (4.40), and the zero-sequence load current in the d-q-o coordinate $\begin{bmatrix} I_{Ld\_0} & I_{Lq\_0} & I_{Lo\_0} \end{bmatrix}^T$ is expressed in (4.41).

$$\begin{bmatrix} I_{Ld\_n} \\ I_{Lq\_n} \\ I_{Lo\_n} \end{bmatrix} = I_{m\_n} \begin{bmatrix} \cos(2\omega t + \varphi_n) \\ -\sin(2\omega t - \varphi_n) \\ 0 \end{bmatrix} \quad \textbf{(4.40)}$$

$$\begin{bmatrix} I_{Ld\_0} \\ I_{Lq\_0} \\ I_{Lo\_0} \end{bmatrix} = I_{m\_0} \begin{bmatrix} 0 \\ 0 \\ \cos(\omega t + \varphi_0) \end{bmatrix} \quad \textbf{(4.41)}$$

It can be seen that the negative-sequence current will be 2ω ripple currents at d and q channels and zero at the o channel. The zero-sequence current is a ripple current at the fundamental frequency, and does not have any impact on d and q channels.

It is apparent that an unbalanced load imposes a greater challenge for the control loop design due to the 2ω ripple load currents in both d and q channels, and ω ripple load current in the o channel. If ripple load currents are considered a disturbance to the system, a high control gain at 2ω frequency for both d and q channels, and a high control gain at ω frequency for the o channel are desirable.

4.6.3 Nonlinear Load in d-q-o coordinate

A balanced nonlinear load draws harmonic currents expressed as

$$\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \begin{bmatrix} I_{LA\_f} \\ I_{LB\_f} \\ I_{LC\_f} \end{bmatrix} + \begin{bmatrix} I_{LA\_h} \\ I_{LB\_h} \\ I_{LC\_h} \end{bmatrix} \quad \textbf{(4.42)}$$

The fundamental current is

$$\begin{bmatrix} I_{LA\_f} \\ I_{LB\_f} \\ I_{LC\_f} \end{bmatrix} = I_{m\_1} \begin{bmatrix} \cos(\omega t + \varphi_p) \\ \cos(\omega t - \frac{2}{3}\pi + \varphi_p) \\ \cos(\omega t + \frac{2}{3} + \varphi_p) \end{bmatrix} \quad \textbf{(4.43)}$$

The harmonic current is

$$\textbf{(4.44)} \qquad \begin{bmatrix} I_{LA\_h} \\ I_{LB\_h} \\ I_{LC\_h} \end{bmatrix} = \sum_{k=3,5,7...} (I_{m\_k} \begin{bmatrix} \cos(k\omega t + \varphi_k) \\ \cos(k\omega t + \varphi_k - sgn(k)\frac{2}{3}\pi) \\ \cos(k\omega t + \varphi_k + sgn(k)\frac{2}{3}\pi) \end{bmatrix})$$

where

$$sgn(k) = \begin{cases} 0, & (\text{zero} - \text{sequence}) & k = 3,9,15... \\ +1, & (\text{positive} - \text{sequence}) & k = 7,13,19... \\ -1, & (\text{negative} - \text{sequence}) & k = 5,11,17... \end{cases}$$

The fundamental load current will be the same as a balanced linear load current in the d-q-o coordinate. All the harmonics are odd harmonic. They can be further classified into zero-sequence harmonic currents for harmonics of 3^{rd}, 9^{th}, 15^{th}, …, positive-sequence harmonic currents for harmonics of 7^{th}, 13^{th}, 19^{th}, …, and negative-sequence harmonic currents for harmonics of 5^{th}, 11^{th}, 17^{th}, …. Applying the coordinate transformation matrix T_4 to each individual harmonic current, the harmonic load currents in d-q-o coordinate can be obtained.

The zero-sequence harmonic currents in d-q-o coordinate are expressed as

$$\textbf{(4.45)} \qquad \begin{bmatrix} I_{Ld\_hz} \\ I_{Lq\_hz} \\ I_{Lo\_hz} \end{bmatrix}_{k=3,9,15...} = \sum_{k=3,9,15...} (I_{m\_k} \begin{bmatrix} 0 \\ 0 \\ \cos(k\omega t + \varphi_k) \end{bmatrix})$$

They remain unchanged and appear only at o channel.

The positive-sequence harmonic currents in d-q-o coordinate are expressed as

$$\textbf{(4.46)} \qquad \begin{bmatrix} I_{Ld\_hp} \\ I_{Lq\_hp} \\ I_{Lo\_hp} \end{bmatrix}_{k=7,13,19...} = \sum_{k=7,13,19...} (I_{m\_k} \begin{bmatrix} \cos((k-1)\omega t + \varphi_k) \\ -\sin((k-1)\omega t + \varphi_k) \\ 0 \end{bmatrix})$$

The positive-sequence harmonic currents will be even order ripple currents at (k-1)ω frequencies in both d and q channels, and zero in the o channel.

The negative-sequence harmonic currents in d-q-o coordinate are expressed as

$$\begin{bmatrix} I_{Ld\_hn} \\ I_{Lq\_hn} \\ I_{Lo\_hn} \end{bmatrix}_{k=5,11,13...} = \sum_{k=5,11,13...} \left(I_{m\_k} \begin{bmatrix} \cos((k+1)\omega t + \varphi_k) \\ -\sin((k+1)\omega t - \varphi_k) \\ 0 \end{bmatrix} \right) \quad \textbf{(4.47)}$$

The negative-sequence harmonic currents will be even order ripple currents at (k+1)ω frequencies in both d and q channels, and zero in the o channel.

To summarize, all the non-triplen harmonic currents become even harmonic currents in the d and q channels, and zero in the o channel. All the triplen harmonic currents will be preserved in the o channel.

It should be noted that the same even order harmonic current in the d-q-o coordinate may be contributed by two different harmonic currents in the a-b-c coordinate. For example, both the positive-sequence 7^{th} harmonic and the negative-sequence 5^{th} harmonic currents in the a-b-c coordinate become the 6^{th} harmonic current in both d and q channels.

4.6.4 Unbalanced and Nonlinear Load in d-q-o coordinate

When imbalance and nonlinear coexist, harmonic analysis should be performed first. Unbalanced harmonic currents can be further decomposed into positive, negative and zero sequences. Then, corresponding currents in the d-q-o coordinate can be found. Table 4-1 summarizes the mapping between the load currents in a-b-c coordinate and that in d-q-o coordinate for different load conditions.

Table 4-1 Unbalanced and Nonlinear Load in d-q-o Coordinate

		a-b-c	**d-q-o**
Balanced w/o Harmonics		$I_{m\_p}\begin{bmatrix}\cos(\omega t+\varphi_p)\\ \cos(\omega t-\frac{2}{3}\pi+\varphi_p)\\ \cos(\omega t+\frac{2}{3}+\varphi_p)\end{bmatrix}$	$I_{m\_p}\begin{bmatrix}\cos(\varphi_p)\\ -\sin(\varphi_p)\\ 0\end{bmatrix}$
Imbalance W/o Harmonics	Positive Sequence	Same as above	
	Negative Sequence	$I_{m\_n}\begin{bmatrix}\cos(\omega t+\varphi_n)\\ \cos(\omega t+\frac{2}{3}\pi+\varphi_n)\\ \cos(\omega t-\frac{2}{3}+\varphi_n)\end{bmatrix}$	$I_{m\_n}\begin{bmatrix}\cos(2\omega t+\varphi_n)\\ -\sin(2\omega t-\varphi_n)\\ 0\end{bmatrix}$
	Zero Sequence	$I_{m\_0}\begin{bmatrix}\cos(\omega t+\varphi_0)\\ \cos(\omega t+\varphi_0)\\ \cos(\omega t+\varphi_0)\end{bmatrix}$	$I_{m\_0}\begin{bmatrix}0\\ 0\\ \cos(\omega t+\varphi_0)\end{bmatrix}$
Harmonics	Positive Sequence	$I_{m\_k}\begin{bmatrix}\cos(k\omega t+\varphi_k)\\ \cos(k\omega t+\varphi_k-\frac{2}{3}\pi)\\ \cos(k\omega t+\varphi_k+\frac{2}{3}\pi)\end{bmatrix}$	$I_{m\_k}\begin{bmatrix}\cos((k-1)\omega t+\varphi_k)\\ -\sin((k-1)\omega t+\varphi_k)\\ 0\end{bmatrix}$
	Negative-Sequence	$I_{m\_k}\begin{bmatrix}\cos(k\omega t+\varphi_k)\\ \cos(k\omega t+\varphi_k+\frac{2}{3}\pi)\\ \cos(k\omega t+\varphi_k-\frac{2}{3}\pi)\end{bmatrix}$	$I_{m\_k}\begin{bmatrix}\cos((k+1)\omega t+\varphi_k)\\ -\sin((k+1)\omega t-\varphi_k)\\ 0\end{bmatrix}$
	Zero-Sequence	$I_{m\_k}\begin{bmatrix}\cos(k\omega t+\varphi_k)\\ \cos(k\omega t+\varphi_k)\\ \cos(k\omega t+\varphi_k)\end{bmatrix}$	$I_{m\_k}\begin{bmatrix}0\\ 0\\ \cos(k\omega t+\varphi_k)\end{bmatrix}$

4.7 Control of Four-Legged Inverter

In this section, control issues of a four-legged inverter for utility power supply applications are discussed. The ultimate control target is to have a stable three-phase output voltage with a low distortion under all the possible load conditions specified in Section 3.5.4.1.

4.7.1 Control Loop Design

4.7.1.1 Voltage Loop Control

Since the ultimate goal is to control the output voltage, a voltage loop feedback control is the most straightforward. In terms of control loop design, assuming the DC link voltage is an ideal voltage source, the system control block diagram with voltage loop compensators is shown in Figure 4-10. For the sake of simplicity, the small signal labels '^' are dropped. The small signal model of the power stage is represented by the transfer function blocks in the shaded boxes. The voltage loop includes three independent PI compensators H_{vd}, H_{vq} and H_{vo} for d, q and o channels to eliminate steady state error. Unterminated load, i.e. three-phase load represented by three DC current sources to give the rated output power level, is used to guarantee the stability under no load condition. To emulate the power losses, 153 Ohm resistors, which are equivalent to 1% of the total power level, are used for each channel. Including a 350 us time delay caused by the digital sampling effect and the time delay due to the three-dimensional space vector modulation with the symmetric sequencing scheme, the power stage control-to-output voltage transfer functions are plotted in Figure 4-11 at 150 kW power level. It can be seen that there are four poles and two zeros around the resonant frequency (505 Hz) for the d and q direct transfer functions $\frac{V_d}{d_d}$ and $\frac{V_q}{d_q}$. Since the poles and zeros are very close to each other, they almost cancel each other. Therefore, the transfer functions are similar to a second-order system, except for the complicated shape around the resonant

frequency. The o channel is a typical second-order system. $\frac{V_o}{d_o}$ has a double pole at the o channel resonant frequency (320 Hz). It should be noted that the resonant frequency of the o channel is different from that of d and q channels, due to the presence of the neutral inductor. The larger the neutral inductor is, the lower the resonant frequency of the o channel is. Although the neutral inductor helps to reduce the current ripple, it is not desirable to have a low resonant frequency for the o channel from a control point of view. Therefore, there is a trade-off in the design of the neutral inductor.

The open loop input impedance and output impedance for d, q and o channels are plotted in Figure 4-12 and Figure 4-13, respectively. The input impedance may be used to analyze the system interaction with the DC source. The output impedance will be used to explain the voltage distortion under nonlinear loads.

The design of the PI compensators can be easily done by following the traditional design approach, putting a zero at the resonant frequency and adjusting the gain to have the desired cross-over frequency and gain and phase margins. However, special attention should be paid to the following three points. First, it can be seen that the peaking of the control-to-output-voltage transfer function around the resonant frequency is more than 20 dB and the phase rolls down sharply to -180 degree around the resonant frequency. Therefore, the cross-over frequency should be placed below one-tenth of the resonant frequency to avoid instability at a light load. Second, there is a control ambiguity around the resonant frequency of the d and q channels due to the coupling transfer functions. It can be seen from the simulated transfer functions at the rated power level and the measured transfer functions at no load, as shown in Figure 4-14, that the coupling transfer functions $\frac{V_d}{d_q}$ and $\frac{V_q}{d_d}$ has an even higher gain than the direct transfer functions $\frac{V_d}{d_d}$ and $\frac{V_q}{d_q}$. Third, the impact of the load power factor on the control loop should be considered. Given the prototype load power factor range [-0.8,0.8], the control-to-output voltage transfer functions are plotted in Figure 4-15 with the resistive load, capacitive load and inductive load. It can be seen that both the capacitive and inductive loads shift the

resonant frequency. The capacitive load yields a lower resonant frequency. The zero of the originally designed PI comensator based on a resistive or unterminated load may not give enough phase margin with the capacitive load. Although the inductive load shifts the resonant frequency to a higher frequency, it leads to a higher peaking and phase drop due to an increased system order. Therefore, both the capacitive and inductive loads may give a worse case than a resistive or unterminated load. When designing the PI voltage loop compensators, a 10 dB gain margin is set to ensure the stability under light load, capacitive and inductive load conditions. Therefore, the cross-over frequencies have to be designed to be less than 15 Hz for the d and q channels, and less than 6 Hz for the o channel, as shown in the voltage loop gain transfer function plots in Figure 4-16. The parameters of the voltage loop compensators that are finally designed are given in Table 4-2. The closed voltage loop input impedance is shown in Figure 4-17. It should be noted that although the gain of the input impedance is the same as that of open loop input impedance, the phase starts from -180 degree at DC. If the output impedance of the source intersects with the input impedance of the closed loop inverter at the low frequency range, the cascade system may be unstable due to the interaction.

Table 4-2 Parameters of the Designed Voltage Loop Compensators

	K_P	K_I	Cross-Over	Phase Margin	Gain Margin
H_{vd}	3.54e-5	0.1107	15 Hz	90 degree	10 dB
H_{vq}	3.54e-5	0.1107	15 Hz	90 degree	10 dB
H_{vo}	1.992e-5	4.117e-2	6 Hz	90 degree	10 dB

By adopting average current control loops, the resonant peak could be damped, and that makes the design of the voltage loop easier. A current loop also provides a faster regulation and inherent over-current protection. However, since the switching frequency is only 5 kHz, the current loop cross-over frequency is in the range of 1/6~1/10 of the switching frequency (500 Hz ~ 830 Hz), to ensure that the impact of current ripple to the controller is small enough. The cross-over frequency of the superimposed voltage loops

should be well separated from the current loops, which ends up with a several tens Hz of the voltage loop cross-over frequencies. The voltage loop cross-over frequencies are not extended much compared with using voltage loop control only. Moreover, the current control loop requires expansive high current sensors. Therefore, adopting a current controller is not an effective solution in terms of performance and cost. The solution for a high performance system under unbalance and/or nonlinear loads will be proposed in Chapter 5.

The low cross-over frequency would cause an unbalanced and distorted output voltage under unbalanced and/or nonlinear loads because there is almost no output impedance reduction with the closed voltage loop beyond the cross-over frequency.

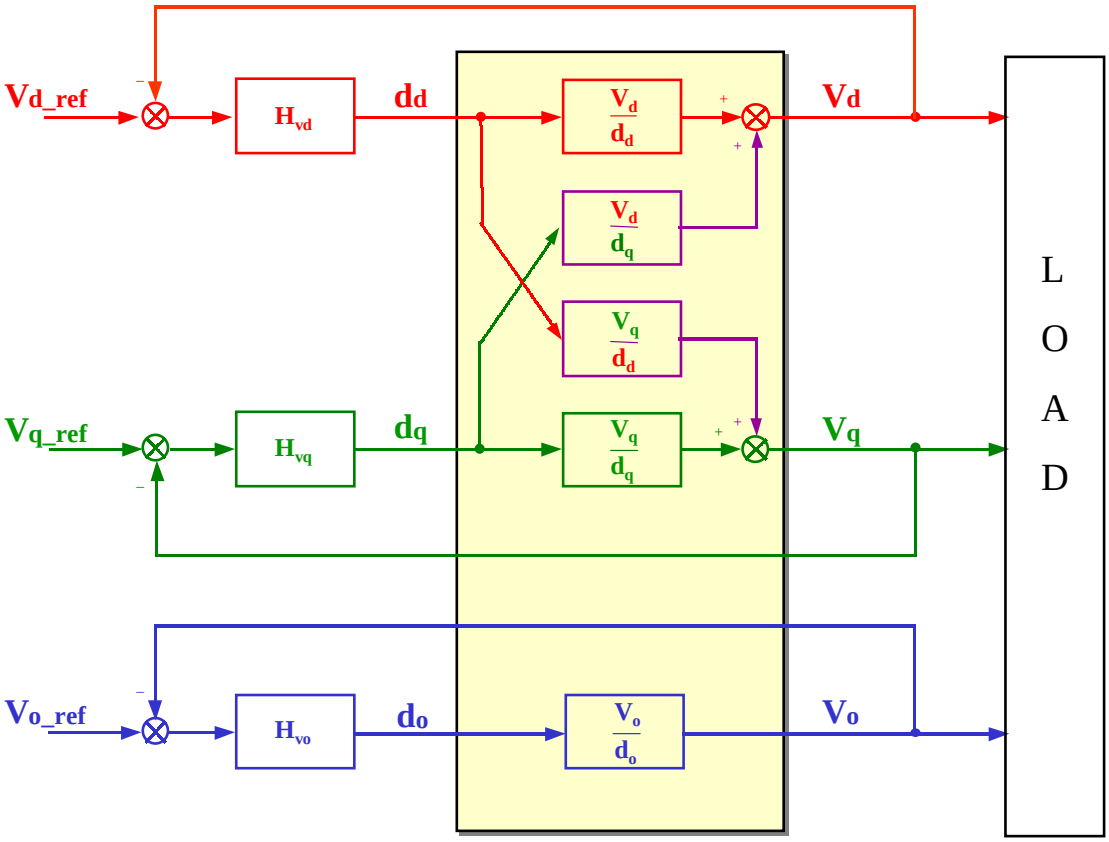


Figure 4-10 System control block diagram with voltage loop compensators

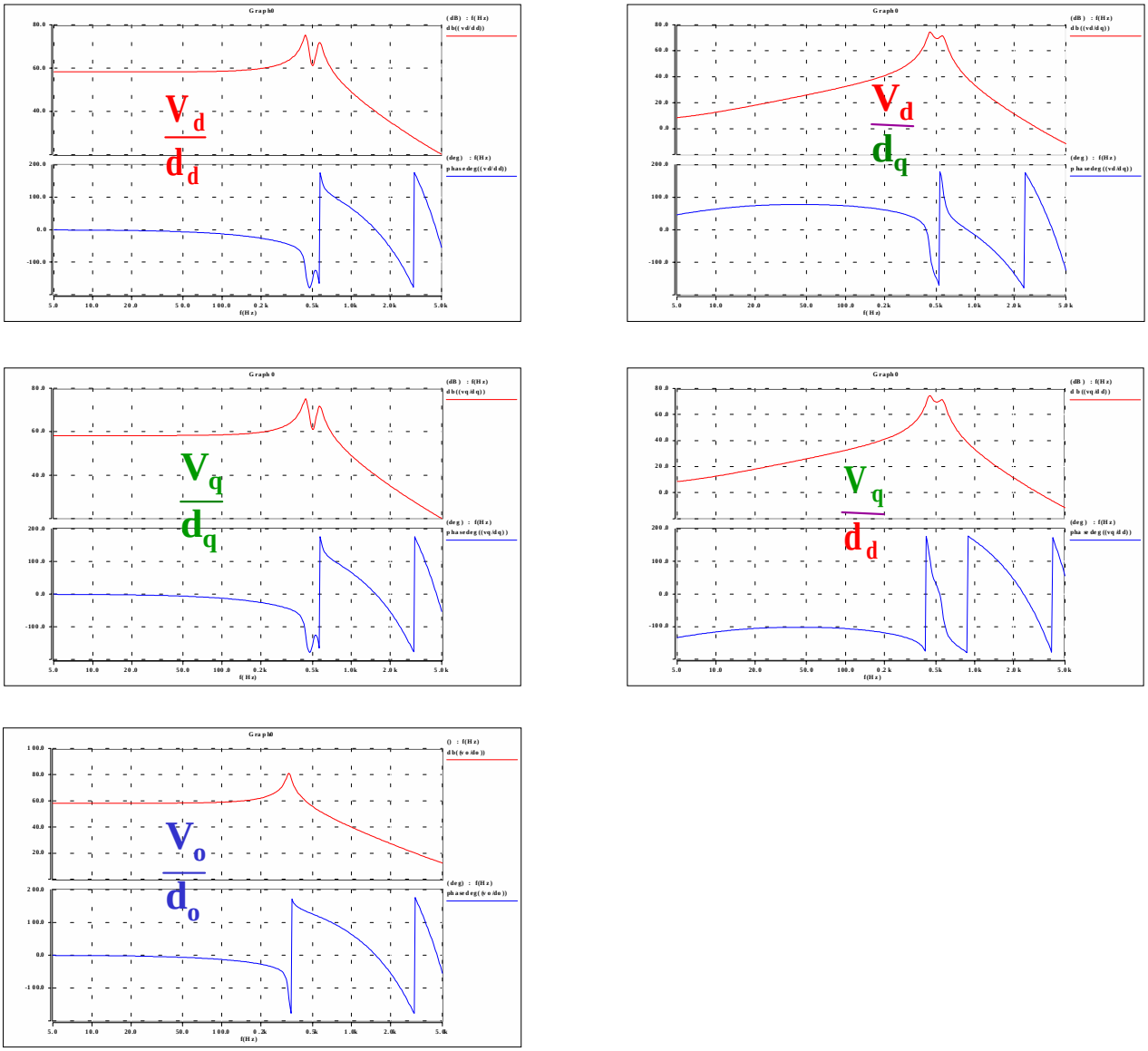


Figure 4-11 Control-to-output voltage transfer functions of a four-legged inverter with unterminated load at 150 kW

(153 Ohm resistors are terminated at each channel to emulate the power losses, a time delay of 375 us is used to account for digital sampling delay and PWM delay)

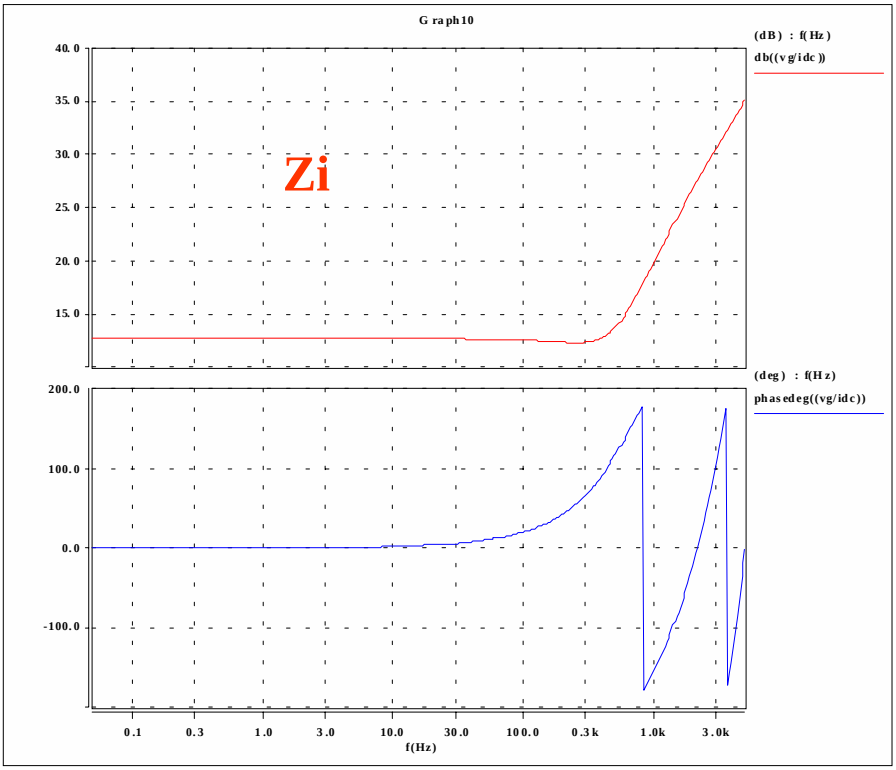
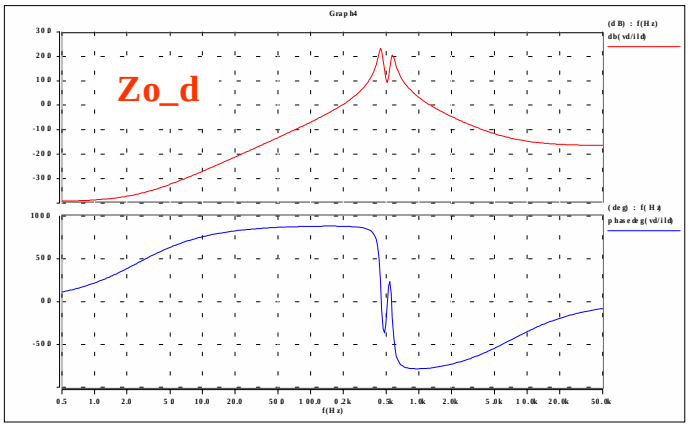


Figure 4-12 Open loop input impedance of a four-legged inverter at 150 kW with a resistive load

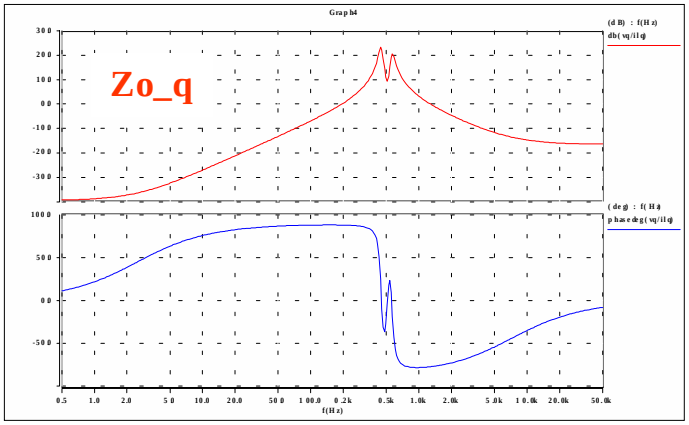
D channel

(a)



Q channel

(b)



O channel

(c)

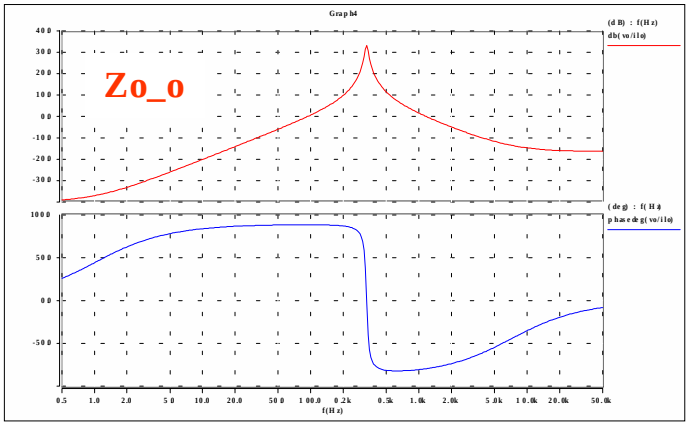


Figure 4-13 Open loop output impedance of a four-legged inverter in d-q-o coordinate with unterminated model

(a) d channel output impedance; (b) q channel output impedance; (c) o channel output impedance

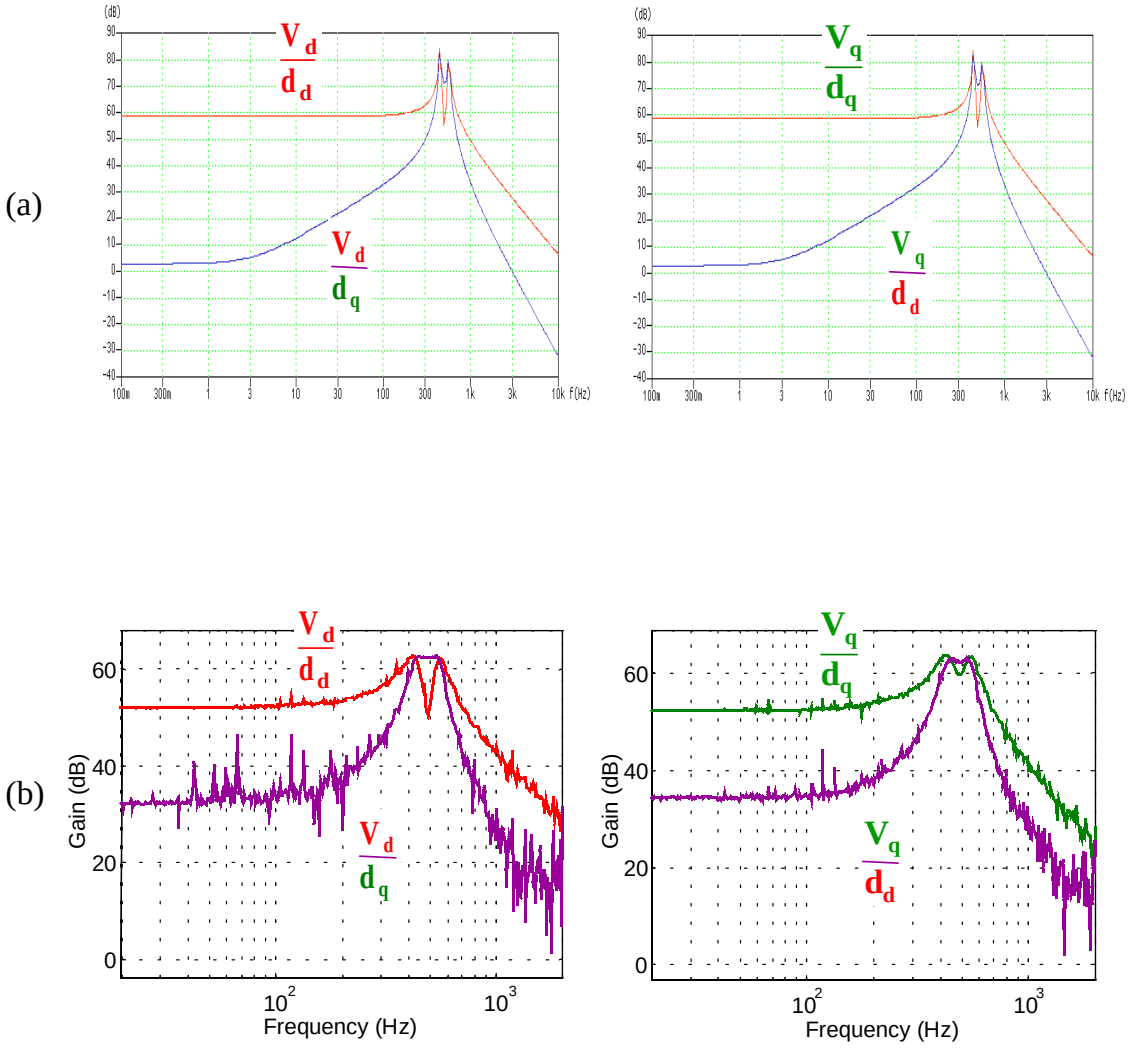


Figure 4-14 Control ambiguity around the resonant frequency at light load

(a) simulated direct and coupling transfer functions at 150 kW with unterminated load;
(b) measured direct and coupling transfer functions at no load

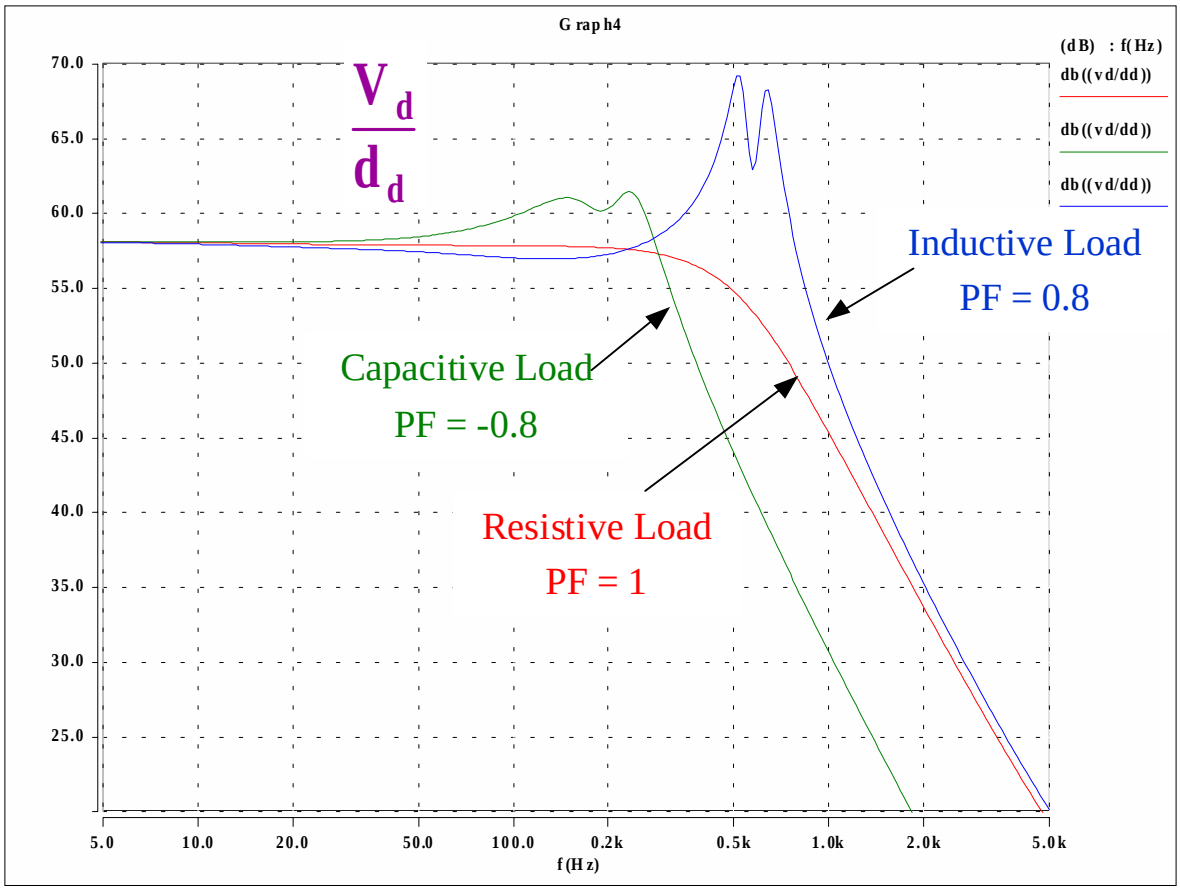
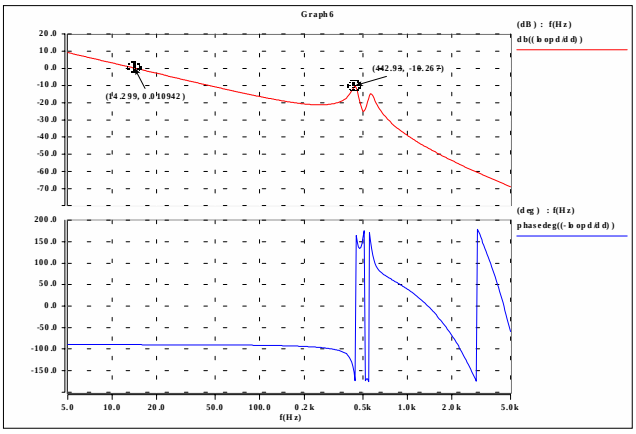


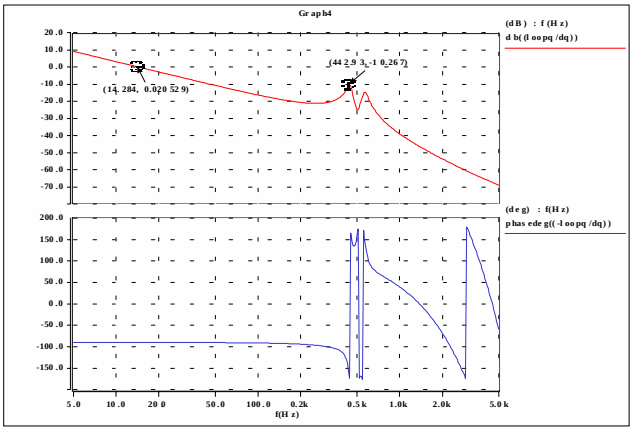
Figure 4-15 Impact of load power factor on control-to-output voltage transfer function – d channel Vd/Dd plot

(output power level: 150 kW(kVA); Resistive load: 1.53 Ohm each phase; capacitive load: 780 uF capacitor and 1.73 Ohm resistor and in parallel per phase; inductive load: 2.1 mH inductor and 1.316 Ohm resistor in series per phase)

(a) d channel



(b) q channel



(c) o channel

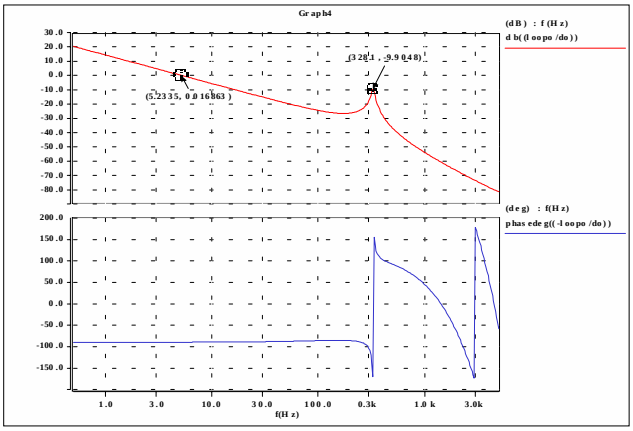


Figure 4-16 Voltage loop gain transfer functions of the four-legged inverter with PI compensators

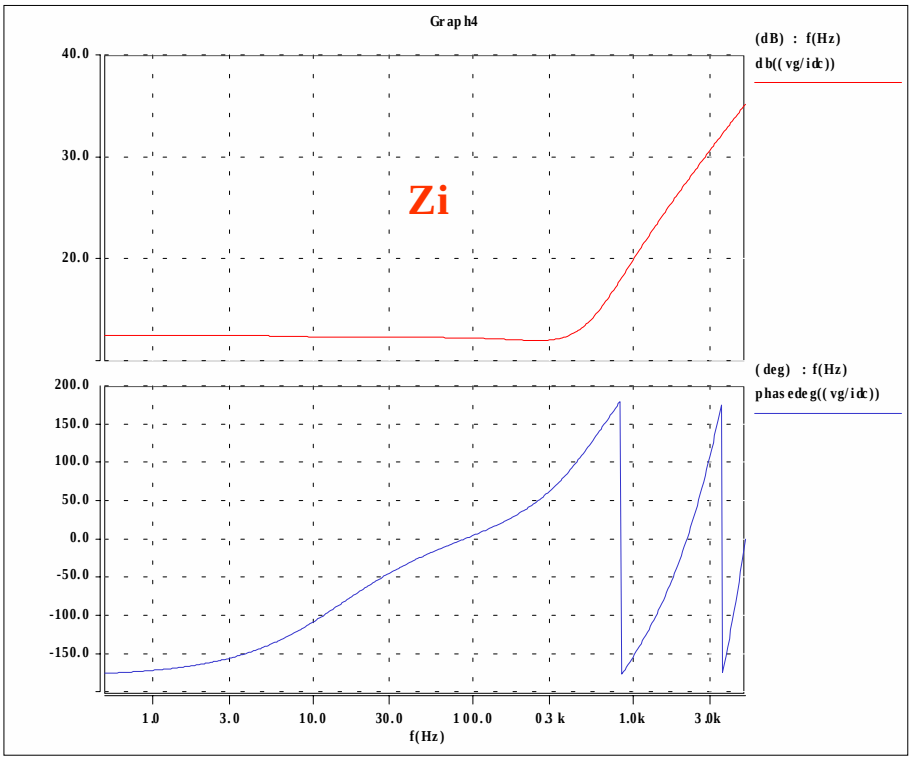


Figure 4-17 Input impedance of the four-legged inverter with voltage loop closed

4.7.1.2 Load Current Feedforward Control

When the load is heavily unbalanced, the unbalanced load current presents a large-signal disturbance in both d and q channels at 2ω frequency, and in o channel at ω frequency, as expressed in (4.40) and (4.41). This large-signal disturbance may not be able to be compensated by a slow voltage feedback loop. This leads to an unbalanced output voltage due to the limited control gain from a low cross-over frequency.

It can be seen from (4.30) that instead of constant steady state duty ratios with a balanced load, with an unbalanced load, the steady-state duty ratios in both d and q channels are a sinusoidal signal at 2ω frequency with a DC offset, in o channel is a sinusoidal at ω frequency, . If the voltage feedback loop is fast enough with a high control gain at 2ω frequency for d and q channels, and at ω frequency for o channel, this sinusoidal duty ratio is achievable; and no unbalance or distortion shows up in the system. If the voltage feedback loop is not fast enough due to a limited switching frequency for high power applications, the sinusoidal steady-state duty ratios may be given by a load current feedforward control loop, as shown in Figure 4-18. The load current feedforward controller is expressed as

$$\textbf{(4.48)} \qquad \begin{cases} G_{iLd} = \dfrac{L}{V_g}\left(\dfrac{d}{dt} I_{Ld} - \omega I_{Lq}\right) \\ G_{iLq} = \dfrac{L}{V_g}\left(\dfrac{d}{dt} I_{Lq} + \omega I_{Ld}\right) \\ G_{iLo} = \dfrac{L + 3L_n}{V_g}\dfrac{d}{dt} I_{Lo} \end{cases}$$

The applied duty ratio will be the sum of the output of the load current feedforward controller, which gives the sinusoidal steady-state value, and the output of the voltage feedback controller.

Since the load current feedforward controller needs the derivative of the load current, in the real implementation it introduces noises to the controller. Some low pass

filter may be needed to limit the noise level. Another way to get the derivatives of the load current is to sense the inductor voltage, which contains the information of the derivatives of the load currents.

It should be noted that a high feedforward gain may lead to instability, especially when the time delay in the control loop is large. It is shown in Figure 4-19 that the output voltage may be unstable with a large feedforward gain.

With the load current feedforward control, unbalanced output voltage due to a heavily unbalanced load can be corrected even with a low voltage feedback control bandwidth. It is demonstrated in Figure 4-20 when both phase A and B are loaded with 50 kW resistive load, and phase C is unloaded. Without the load current feedforward control, the maximum voltage difference among phases is 50 V, which is 12.5% of the rated output voltage. With the load current feedforward control, it is reduced down to 15 V, which is 4% of the rated output voltage.

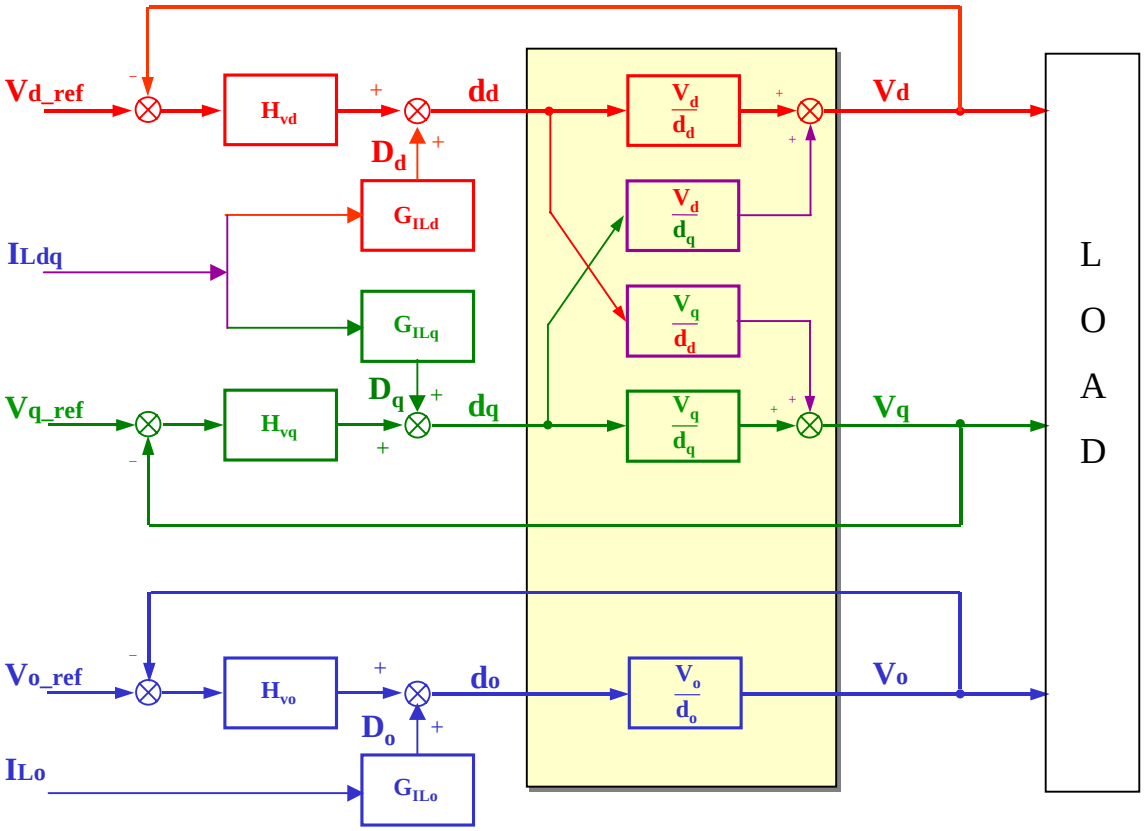
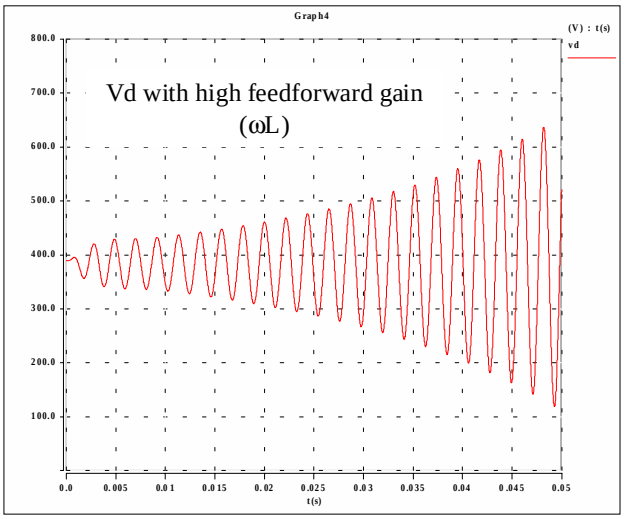


Figure 4-18 System control block diagram with load current feedforward and output voltage feedback control

(a)



(b)

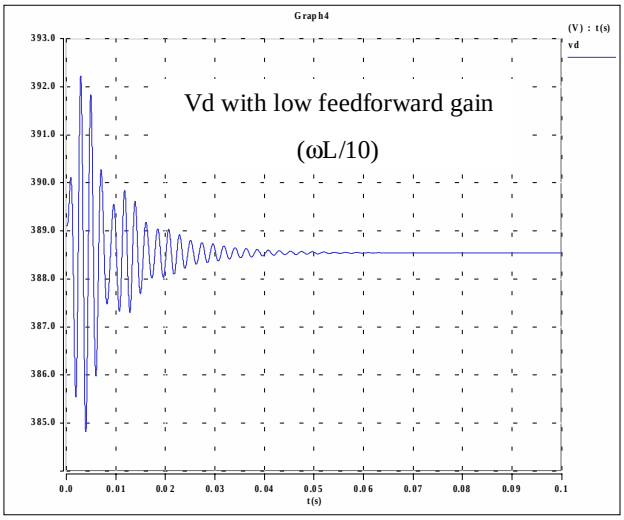
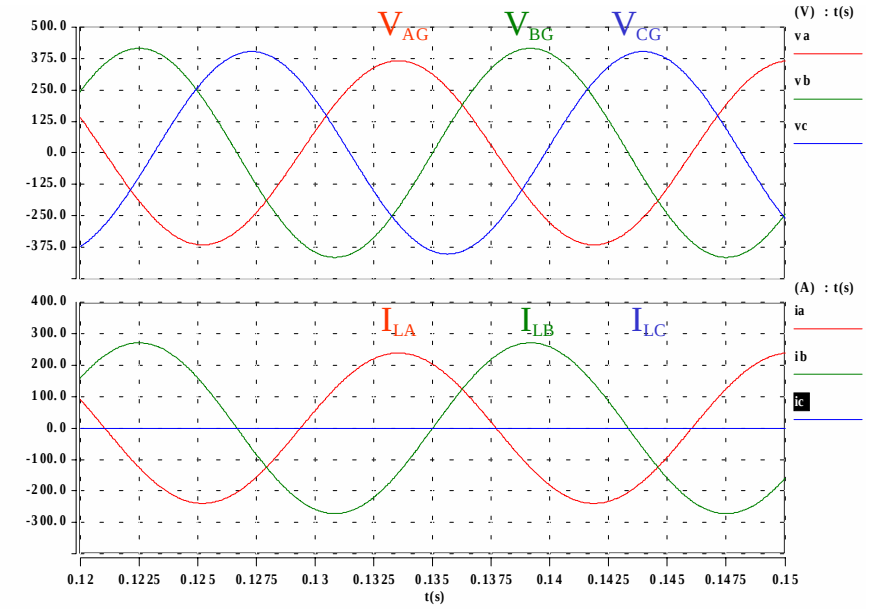


Figure 4-19 Impact of feedforward gain on stability

(a) unstable Vd with high feedforward gain (ωL); (b) stable Vd with low feedforward gain (ωL/10)

(a)



(b)

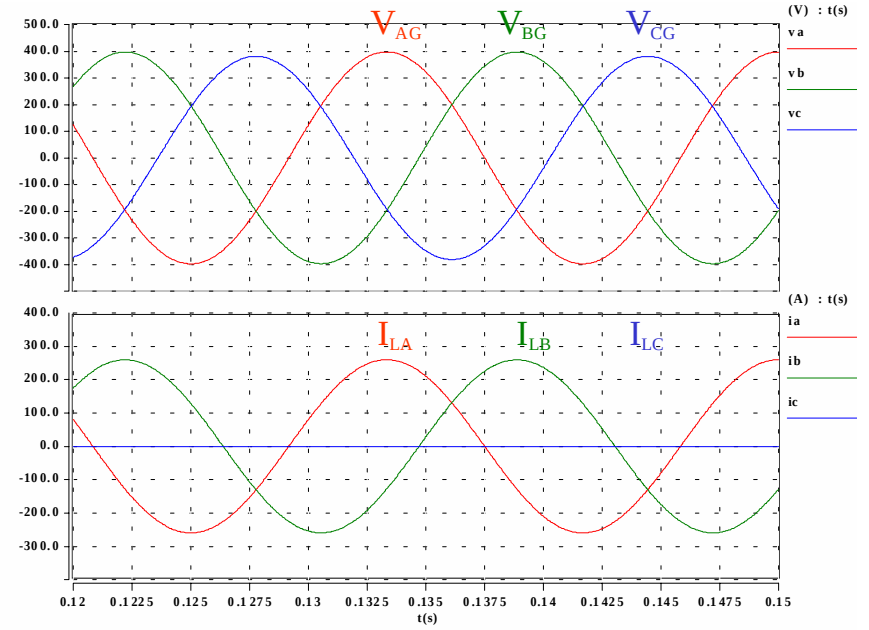


Figure 4-20 Effectiveness of the load current feedforward control with unbalanced load (phase C is unloaded)

(a) output voltage and unbalanced load current without load current feedforward control. maximum voltage difference among phases: 50 V (12.5%); (b) output voltage and unbalanced load current with load current feedforward control. maximum voltage difference among phases: 16 V (4%)

4.7.2 Implementation of Digital Controller

The digital controller performs the following functions: (1) signal conversion from the sensed analog voltage signals to digital signals; (2) coordinate transformation; (3) control loop calculation; (4) three-dimensional space vector modulation. In terms of the hardware structure, the digital controller includes a DSP board, an EPLD board and an A/D board, as shown in Figure 4-21.

The DSP board has a 32-bit floating-point digital signal processor ADSP 21062 and its peripheral circuits. It runs at a 40 MHz clock frequency and executes 40 MIPS (million-instructions-per-second), and achieves 80 MFLOPS sustained performance. With the high speed of the DSP, even more complicated control and modulation schemes can be used. The sinusoidal look-up table used for coordinate transformation is stored in the DSP memory. The DSP performs the following tasks: (1) transforming the sensed three-phase output voltage to d-q-o coordinate; (2) computing the output of the compensator; (3) selecting the switching vectors and calculating the corresponding duty ratios using three-dimensional space vector modulation scheme; and (4) sending out the encoded switching pattern and time duration information to the EPLD.

The EPLD board has two Altera FLEX 8820 programmable logic devices. Functionally it can be divided into three blocks, the address decoder, A/D controller and data cache, and digital modulator. In order to have a high speed execution, the A/D conversion functions autonomously. Once the A/D controller and data cache is trigged by the DSP board, it sends out data conversion signals to the A/D board to collect all the signal data in a preprogrammed timing sequence, and then store the sensed signals in the data cache. After that, the DSP will fetch all sensed signals at one time from the data cache in the EPLD. This way insures that all the sensed signals are synchronized for the same moment. Time delays between phases are minimized. The digital modulator has double-buffered counters and comparators. It converts the switching pattern and time duration information from the DSP into pulses, and sends them to the gate driver. The EPLD board also has several clock generators so that the switching frequency and the

line frequency are synchronized, which helps to reduce the harmonic distortions caused by the pulse width modulation.

The A/D board has four independent high-speed 10-bit A/D converters. Four analog signals can be converted to digital signals simultaneously at a speed of 20 MSPS. The data conversion runs continuously in a streamlined fashion. The converted data are sent to the EPLD data bus only when the DSP sends a data conversion command to the EPLD. Since the DSP is released from the task of controlling the data conversion, more complicated computation can be implemented in the DSP.

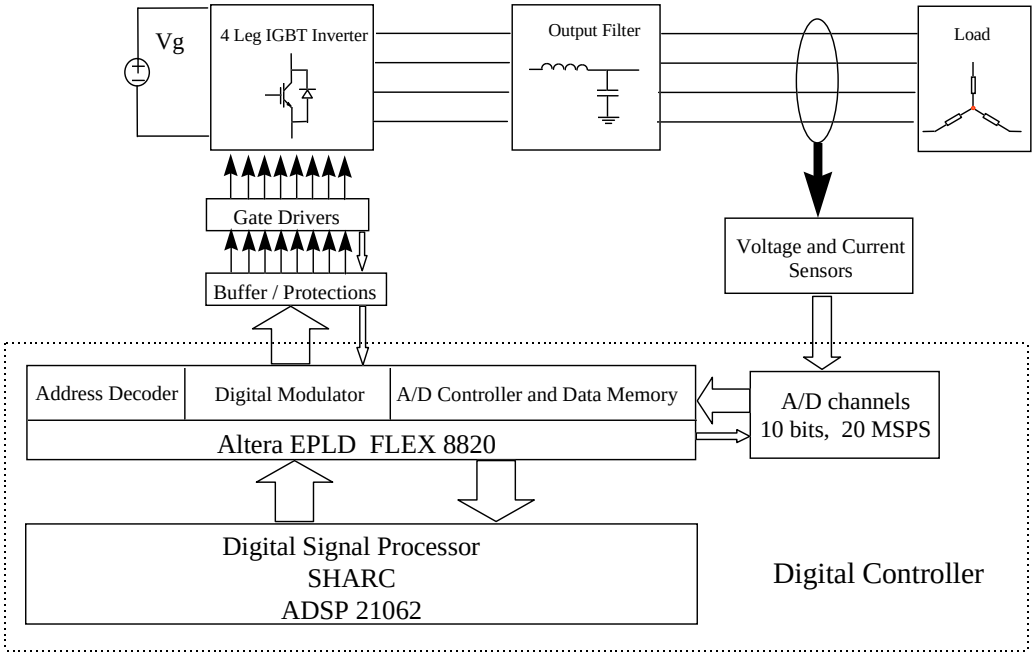


Figure 4-21 DSP controlled system block diagram

4.8 Simulation and Experimental Results of a Four-Legged Inverter

4.8.1 Balanced Load

With the designed voltage control loops, Figure 4-22 shows the measured phase A output voltage and phase A load current with a balanced resistive load at 120 V and 12 kW output. The output voltage THD is 2.6%, which satisfies the design target. Figure 4-23 shows the simulated phase A output voltages and phase A load currents with balanced resistive, capacitive and inductive loads at the rated output voltage and power level.

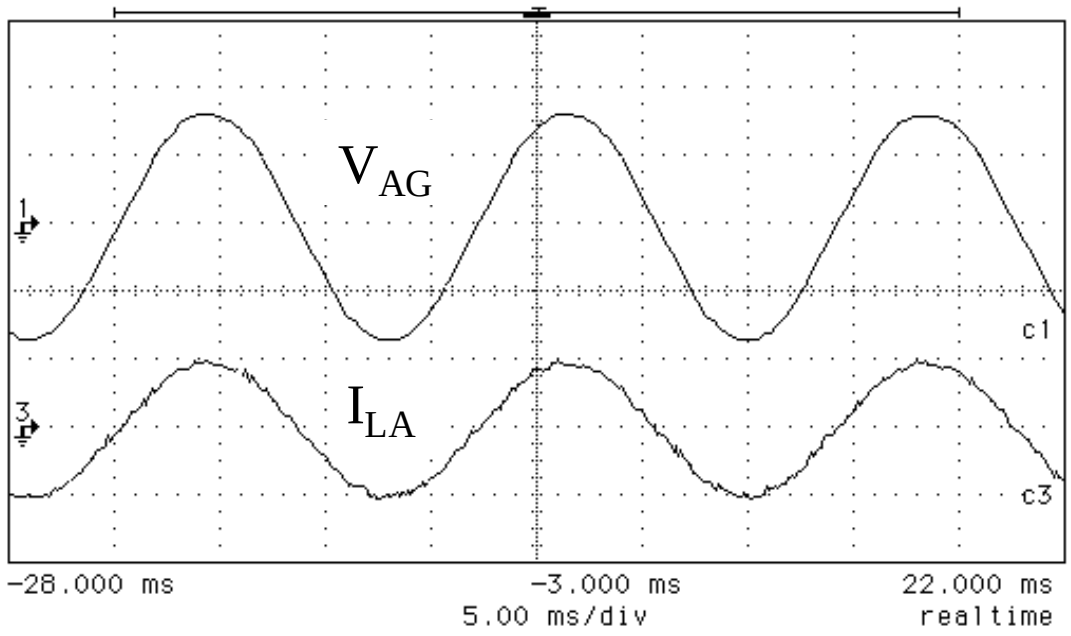
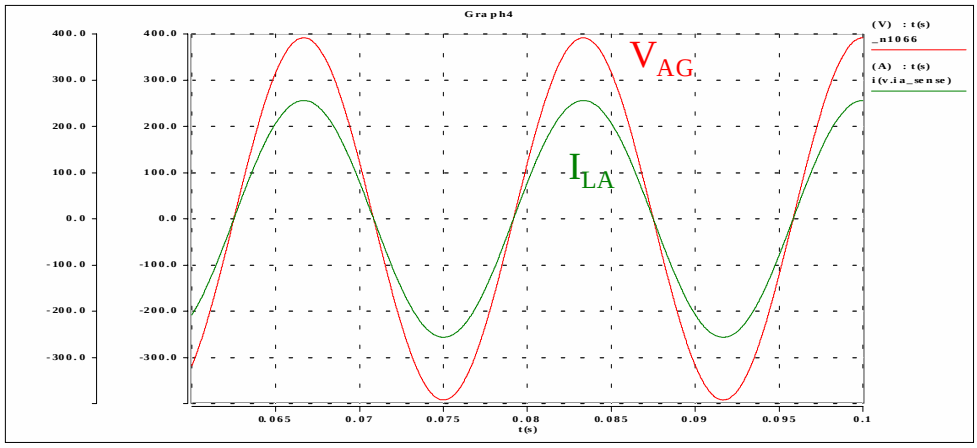


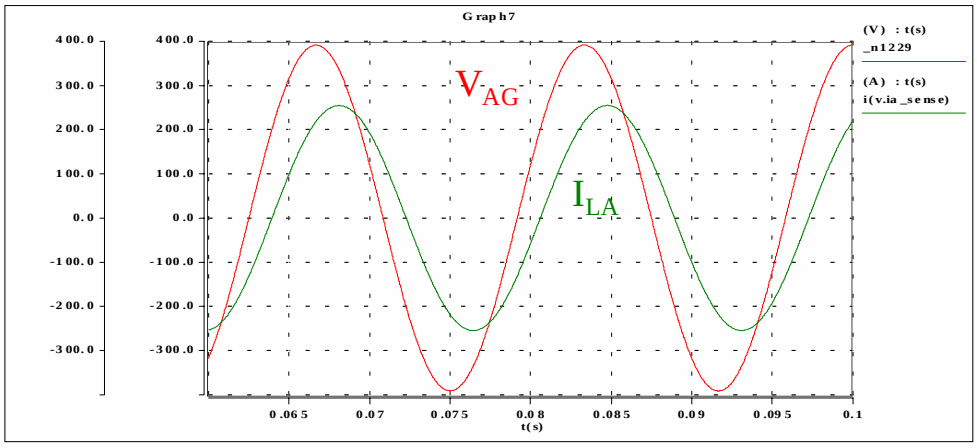
Figure 4-22 Experimental results with balanced linear load with voltage loops closed

(100 V/div, 50 A/div)

(a)



(b)



(c)

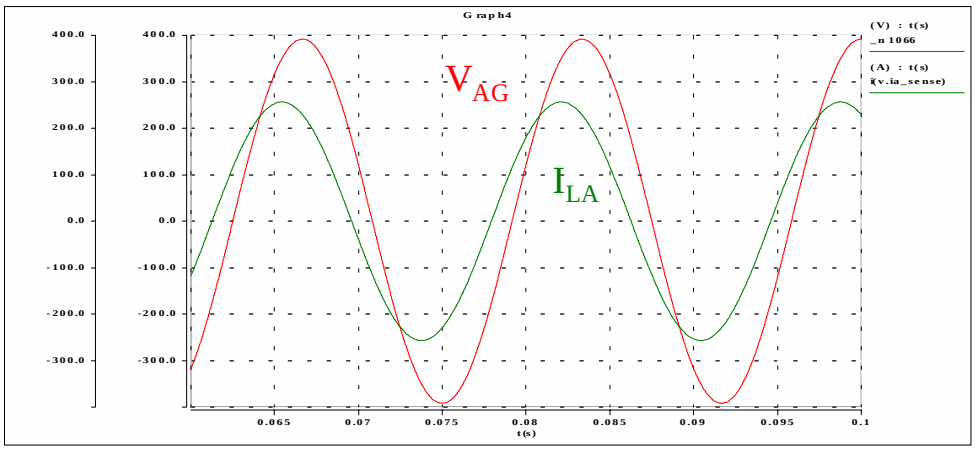


Figure 4-23 Simulation results with balanced linear load with different power factor at 150 kW (kVA) output power level

(a) resistive load; (b) capacitive load; (c) inductive load

4.8.2 Unbalanced Load

An unbalanced linear load is tested. Phase A and B are connected to 4.4 Ohm resistors. Phase C has no load. The DC link voltage is 400 V. The 140 V AC output voltages gives 30 A load currents for phase A and B. Phase C current is zero since it is unloaded. It can be seen in Figure 4-24 that the magnitude of the neutral current is almost 30 A, which is equal to the phase A and B load current. With the proposed three-dimensional space vector, a balanced three-phase sinusoidal voltage is obtained, as shown in Figure 4-25.

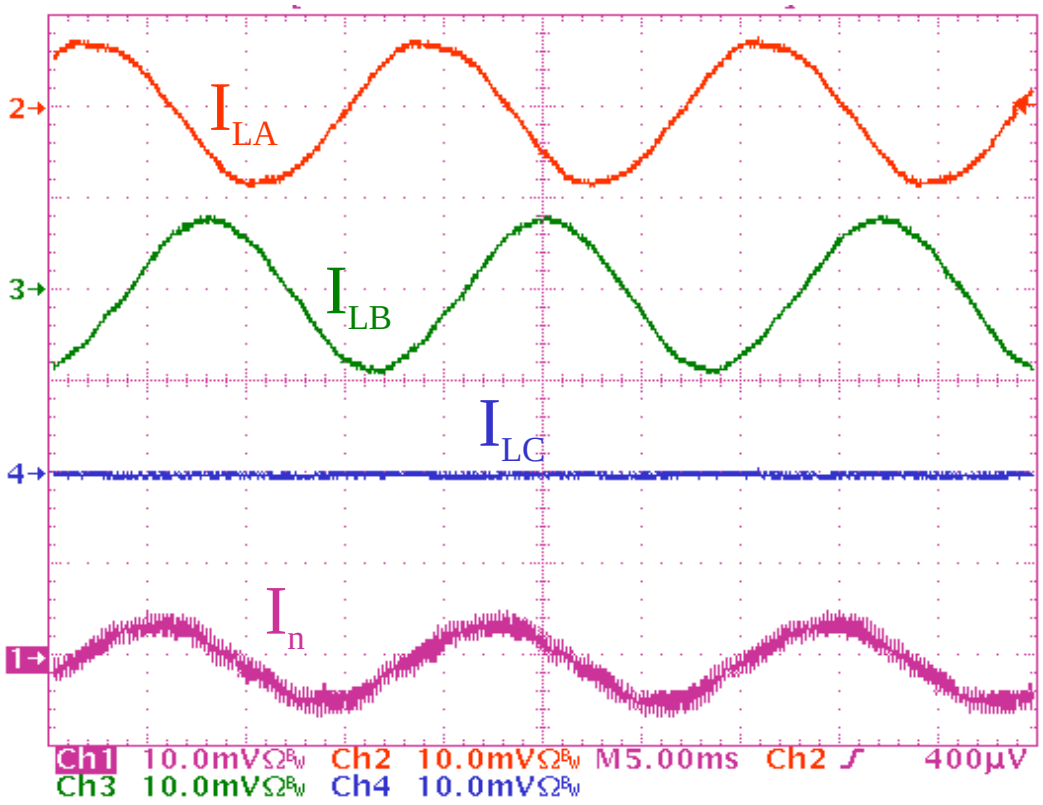


Figure 4-24 Experimental load current and neutral current with an unbalanced linear load

– Phase A and B are connected to 4.4 Ohm resistors, Phase C has no load (50 A for phase currents, 100 A/div for the neutral current)

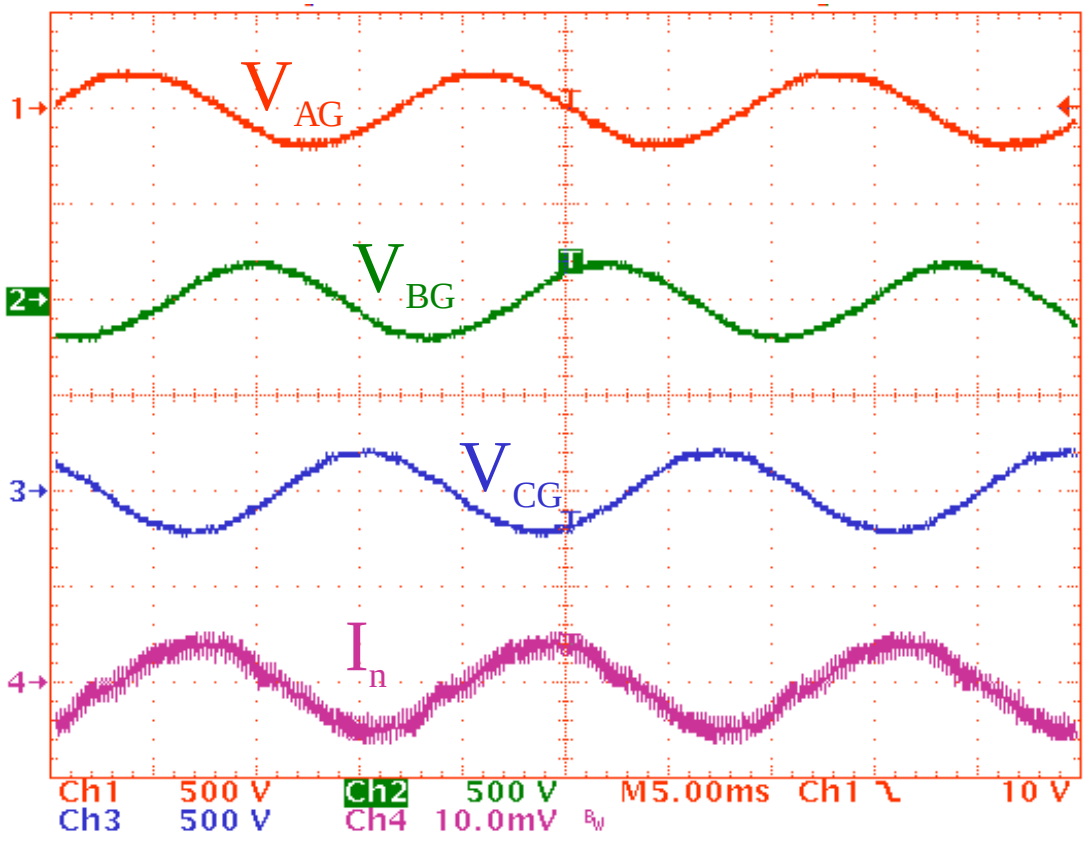


Figure 4-25 Experimental output voltage and neutral current with an unbalanced Linear Load

– Phase A and B are connected to 4.4 Ohm resistors, Phase C has no load (100 A/div for the neutral current)

4.8.3 Nonlinear Load

A combination of balanced linear load and a three-phase diode bridge rectifier is used as the nonlinear load, as shown in Figure 4-26. The experimental waveforms of the phase A output voltage V_{AG} and the phase A load current I_{LA} are shown in Figure 4-27**.** The nonlinear load current THD is 12%. The resulting output voltage THD is 10.3%, which is much higher than the specification. Therefore, the designed control loops cannot give a satisfactory performance for nonlinear loads.

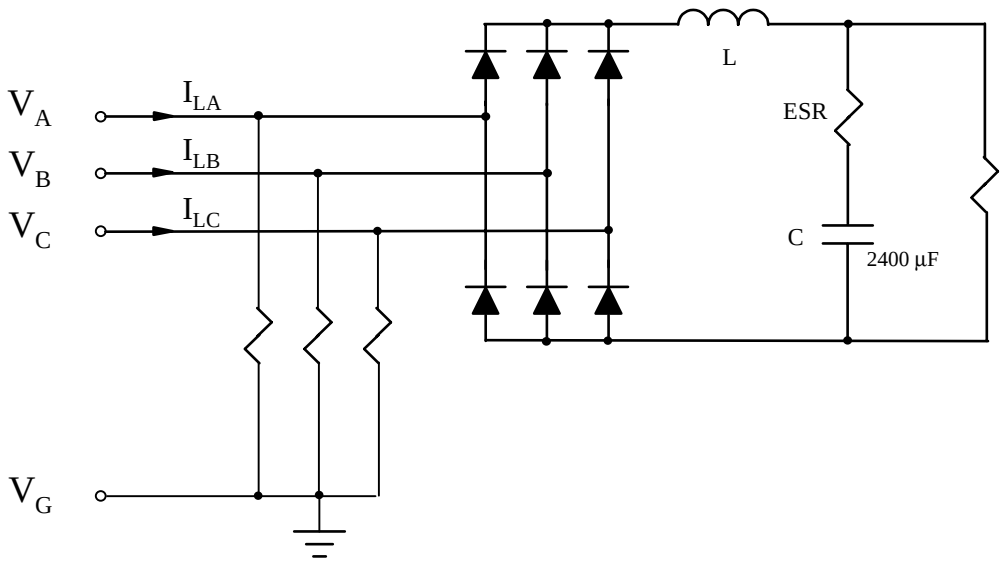


Figure 4-26 Tested nonlinear load

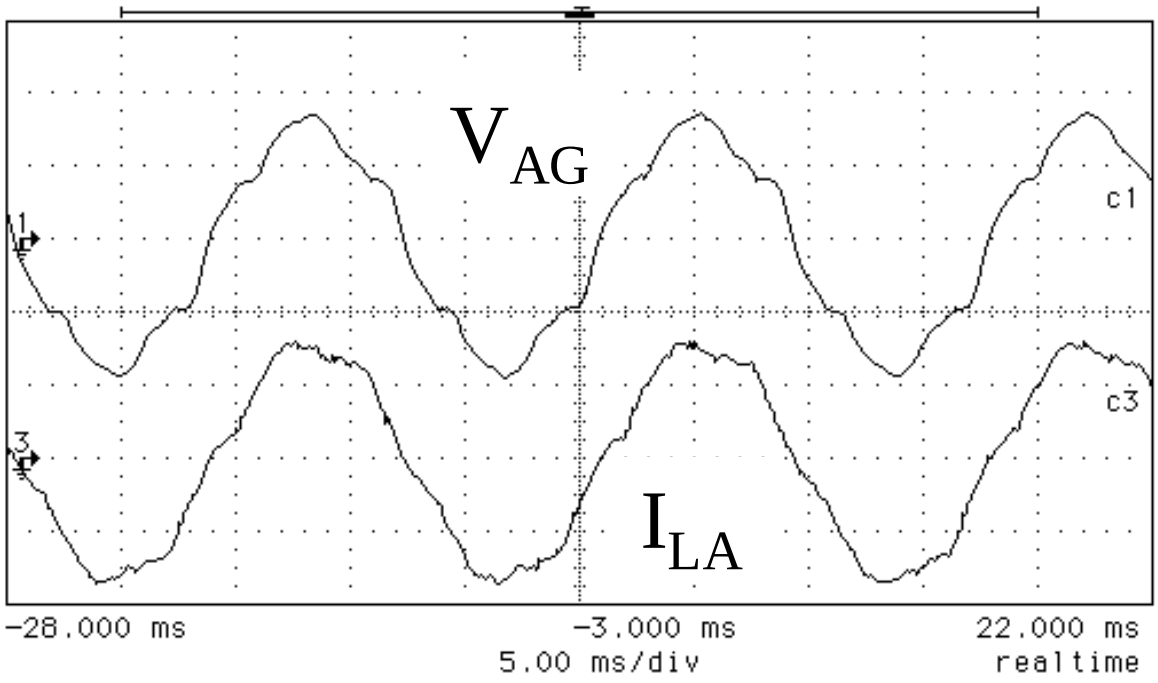


Figure 4-27 Experimental waveforms with an nonlinear load

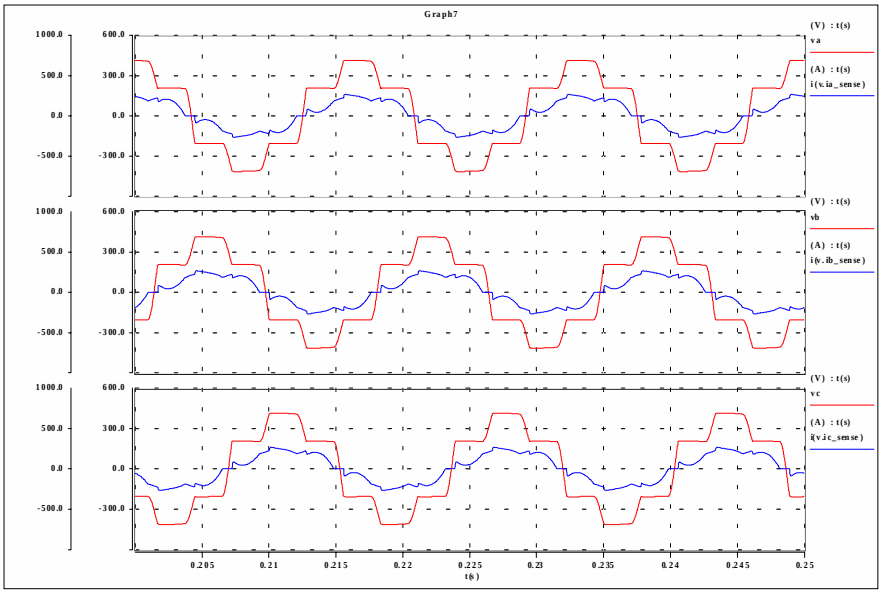
(100 V/div, 100 A/div)

The nonlinear loads described in Chapter 2 are simulated. The simulation results with three-phase diode rectifiers with capacitor filter are shown in Figure 4-28 (a). It can be seen that the output voltages have several stairs, and are highly distorted. With L/C filter, the output voltages are closer to sinusoidal. However, the voltage distortion is still very large.

Three single-phase diode rectifiers with C filter and with L/C filter are simulated. The output voltage, load current and the neutral current are shown in Figure 4-29 (a) and (b). Due to the neutral triplen harmonics, the output voltages are close to square waves and heavily distorted.

The overwhelming voltage distortion with nonlinear loads is caused by high output impedance at the frequencies of the harmonic currents. Detailed discussion about how to improve the voltage distortion under nonlinear loads will be presented in Chapter 5.

(a)



(b)

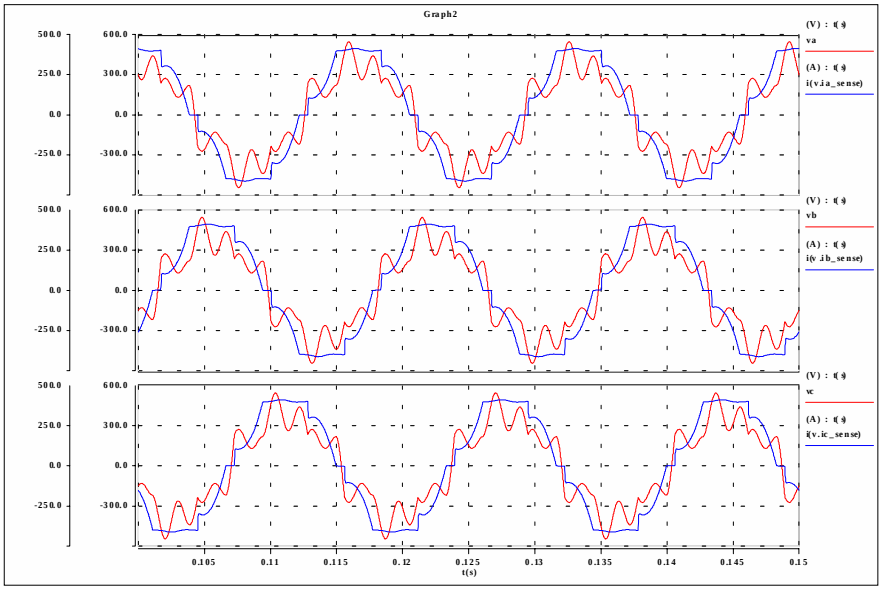
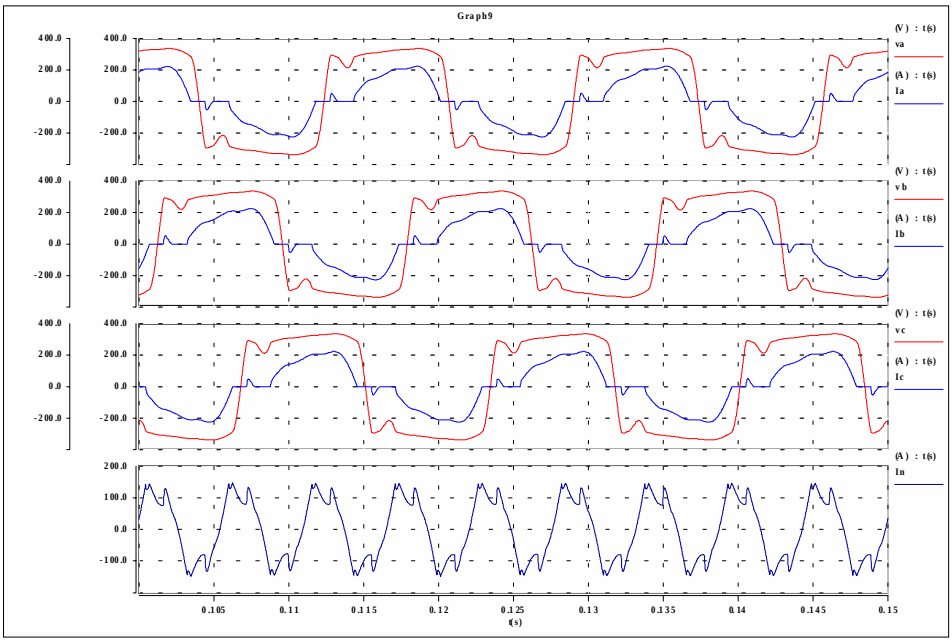


Figure 4-28 Simulated output voltages and load currents with voltage loop closed with three-phase diode bridge rectifier at 150 kW

(a) with C filter. C = 6900 μF, ESR_C = 150 mOhm, R= 2.67 Ohm;
(b) with L/C filter. L = 10 mH, C = 6900 μF, R = 2.67 Ohm

(a)



(b)

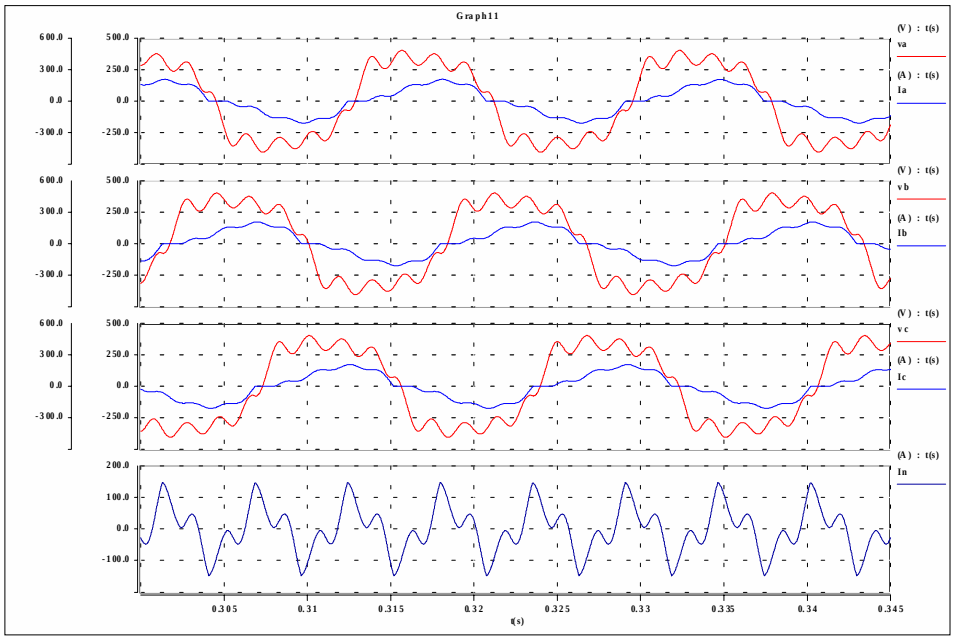


Figure 4-29 Simulated output voltages, load currents and neutral current with voltage loop closed with three single-phase diode bridge rectifiers at 150 kW

(a) with C filter. C = 6900 μF, ESR_C = 250 mOhm, R= 2.7 Ohm per phase;
(b) with L/C filter. L = 1 mH, C = 6900 μF, R = 2.7 Ohm per phase

4.9 Simulation Results of Four-Legged Rectifier with Fault-Mode Operation

One of the advantages of three single-phase PFC rectifiers over three-phase PFC rectifier is that three single-phase PFC rectifiers have fault tolerant capability. When one of the phases fails, the other two phases will still be functioning, whereas for the three-phase rectifier, the same failure will cause two phases to stop working. With the additional fourth leg, the same fault tolerant capability as three single-phase rectifiers can be achieved.

Another advantage of a four-legged rectifier is its control flexibility under an unbalanced source. The three-phase input current can be controlled to achieve constant power, equal current, or equal resistance for three phases. The constant power is the favorable option from the load point of view. The constant output power results in a minimized low frequency output voltage ripple, thus less DC filter capacitance is needed. The equal resistance is the favorable option from the source point of view. It results in currents proportional to the unbalanced voltages, and therefore, eases the burden of the weaker phase of the unbalanced source. Although it is not necessary to have the fourth leg for the constant power and equal current options, the fourth leg is required for the equal resistance option to provide a path for the resulting zero-sequence input current under an unbalanced source.

A four-legged rectifier is designed for running at a 20 kHz switching frequency with 1 μs dead time. Average current mode control is adopted. To achieve the fault tolerant operation, three independent current compensators are designed in the a-b-c coordinate. The fault tolerant operation is demonstrated by the simulation results shown in Figure 4-30. Before 30 ms, it is in the normal operation mode. There is no neutral current. After 30 ms, two failure modes of leg C are simulated.

In the first failure mode, the phase leg C blows out, and is thus disconnected from the circuit. With the leg C failure, phases A and B still work properly, and the neutral current flows through the fourth leg. Figure 4-31 shows that after the failure, the phase C

compensator goes into saturation due to the absence of the feedback current. This saturation does not affect the normal operation of the other two phases. The absence of one phase will affect the power delivered to the load, which can be seen from the DC link current shown in Figure 4-32.

In the second failure mode of leg C, only IGBTs are failed, and the anti-parallel diodes still operate normally. In this case, Figure 4-33 shows that not only phase A and B work properly, phase C inductor also has a current flowing through. Although phase C current is distorted, the total input power is higher than the case when only one or two phases operate in the fault mode. The control voltages and the DC link current in this failure mode are shown in Figure 4-34 and Figure 4-35, respectively.

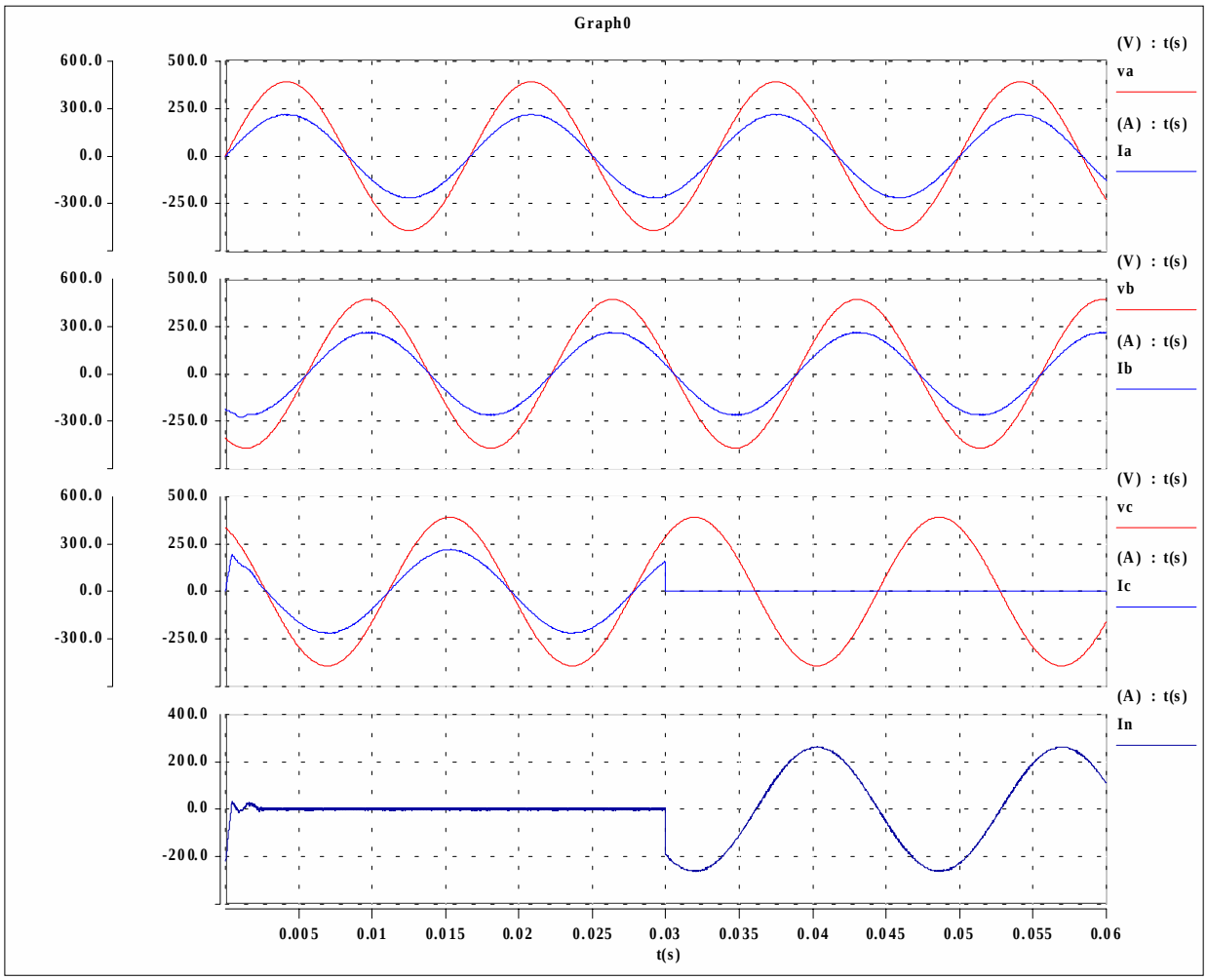


Figure 4-30 Fault mode I operation of a four-legged PWM rectifier – three-phase input voltage, input current and neutral current

(180 A per phase input current; leg C fails at 30 ms)

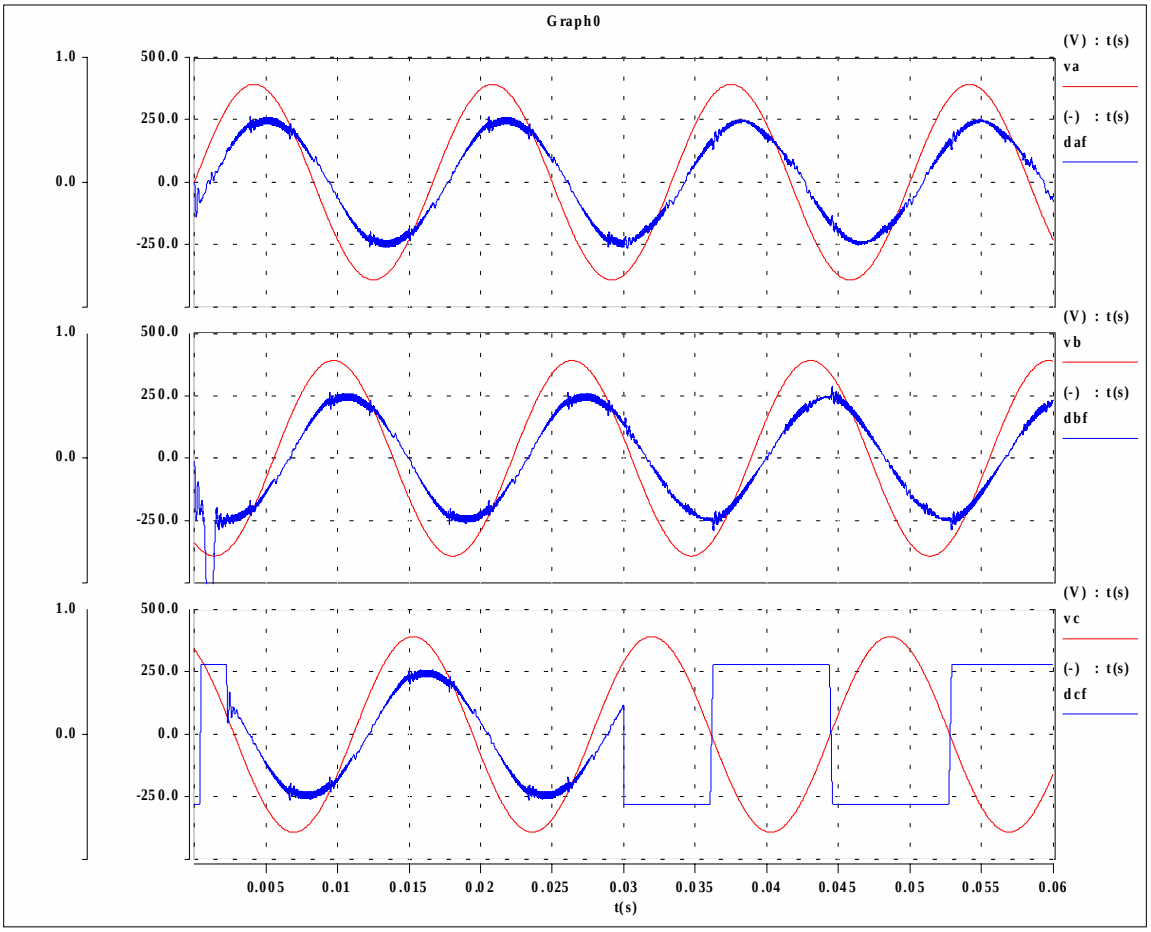


Figure 4-31 Fault mode I operation of a four-legged PWM rectifier ─ three-phase input voltage and control duty ratios

(180 A per phase input current; leg C fails at 30 ms)

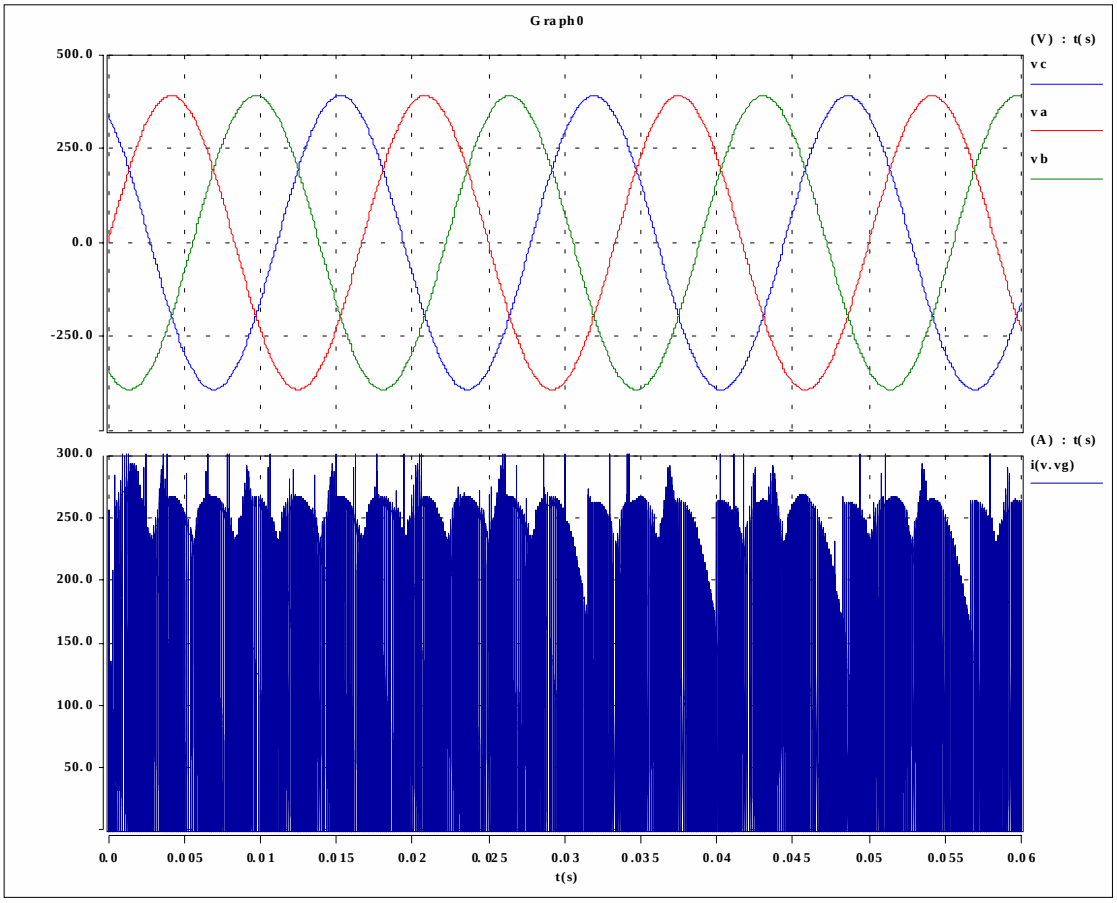


Figure 4-32 Fault mode I operation of a four-legged PWM rectifier ─ three-phase input voltage and DC link current

(180 A per phase input current; leg C fails at 30 ms)

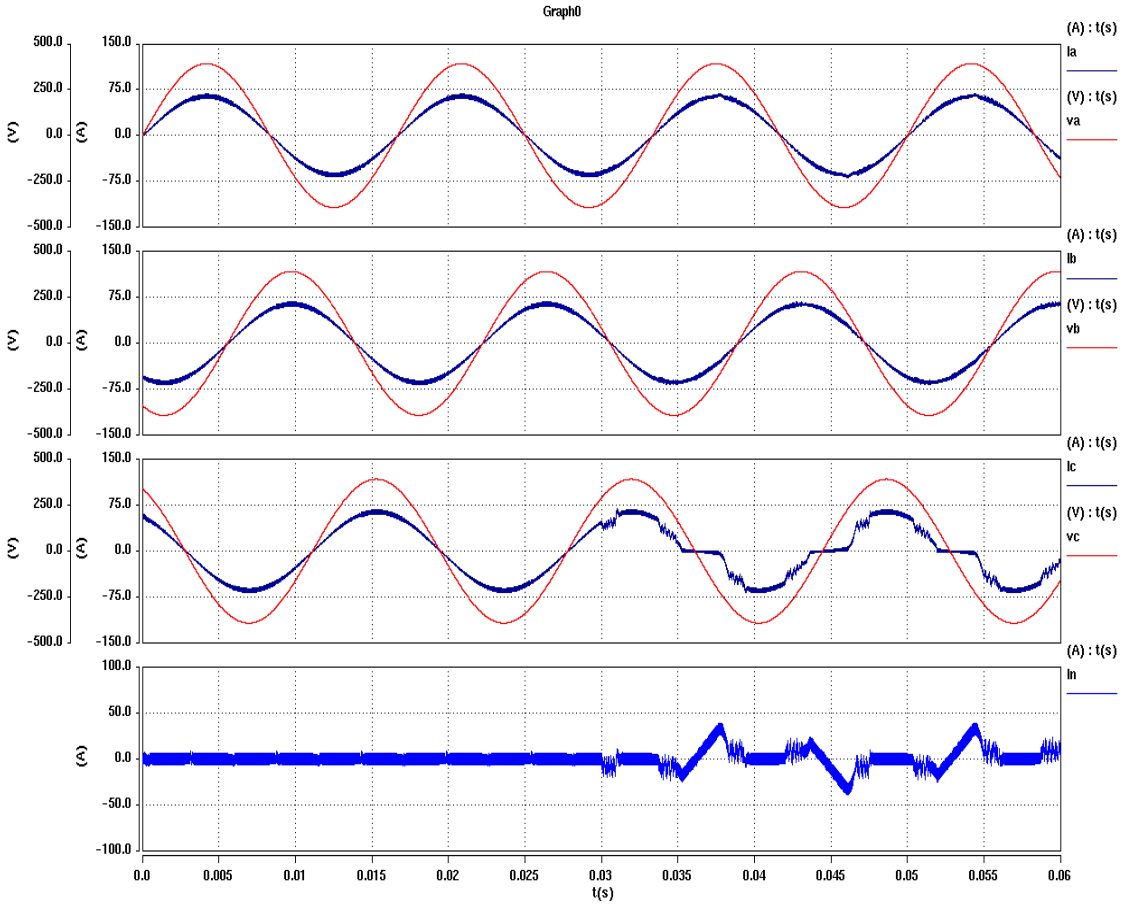


Figure 4-33 Fault mode II operation of a four-legged PWM rectifier ─ three-phase input voltage, input current and neutral current

(36 A per phase input current; leg C IGBT fails at 30 ms)

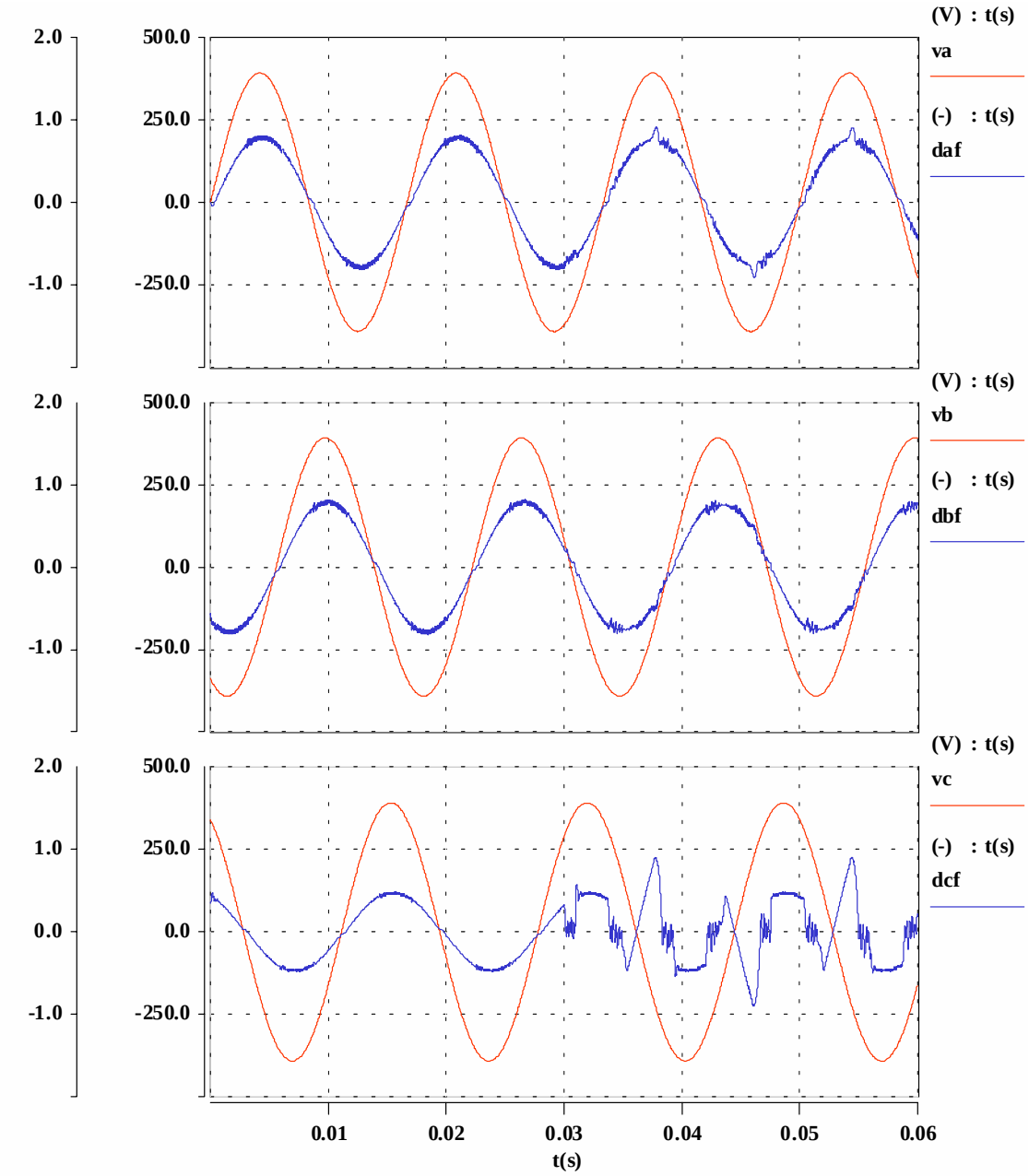


Figure 4-34 Fault mode II operation of a four-legged PWM rectifier — three-phase input voltage and control duty ratios

(36 A per phase input current; leg C IGBT fails at 30 ms)

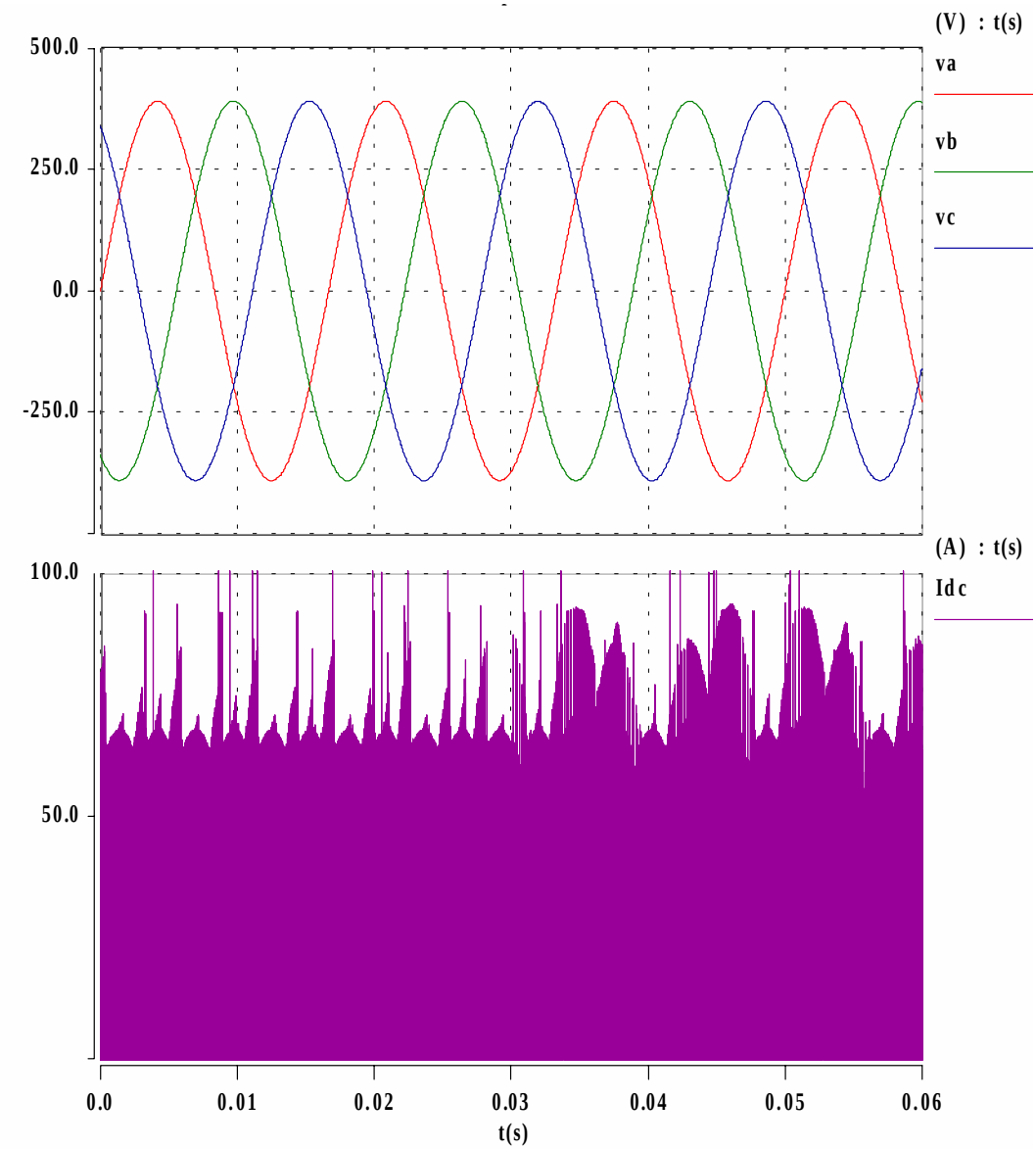


Figure 4-35 Fault mode II operation of a four-legged PWM rectifier ─ three-phase input voltage and DC link current

(36 A per phase input current; leg C IGBT fails at 30 ms)

4.10 Conclusions

Small-signal models for four-legged power converters can be obtained in the d-q-o rotating coordinate. While the d and q channels are coupled together, o channel is independent of d and q channels. Control loop design can be performed based on the small-signal model in the d-q-o rotating coordinate.

Unbalanced load current will bring 2ω ripple current to d and q channels, and ω ripple current to the o channel. Each individual harmonic current caused by nonlinear loads can be decomposed into symmetrical components. All the odd harmonic currents in the a-b-c coordinate become even harmonic currents in the d and q channels, and remain the same in the o channel. Unbalanced and nonlinear load harmonic currents require a high control bandwidth in order to achieve low output voltage distortion.

A powerful digital controller including a floating point DSP is used to implement the closed control loops and three-dimensional space vector modulation. The simulation and experimental results show that with the designed voltage control loop, system performance can meet the specifications for balanced loads and unbalanced loads. However, for nonlinear loads, the output voltage suffers from large distortion.

A four-legged rectifier is capable of fault tolerant operation.

Chapter 5 Power Converter System for Unbalanced and Nonlinear Load

5.1 Introduction

For high power applications, it is difficult to achieve a low voltage distortion with nonlinear loads due to the limited switching frequency and relatively high output impedance at frequencies of harmonic currents. It is also difficult to use soft-switching techniques to increase the switching frequency for high power applications due to the limitations of power semiconductor devices. For high power applications, the soft-switching techniques would also suffer from an inaccurate control due to the dwell time incurred by soft switching interventions.

In this chapter, a power converter system consisting of two four-legged power converters is proposed to achieve high performance with nonlinear loads. The two four-legged power converters are a main inverter and a multi-functional load conditioner. The load conditioner is in parallel with the nonlinear load. It is controlled in such a way that the equivalent load to the main converter, including the load conditioner and the real nonlinear load, is a linear load. The main inverter deals with most of the power flow running at a low-switching frequency. The load conditioner is designed at a much lower power level running at a high-switching frequency. The load conditioner can (1) act like a current source and inject harmonic currents required by the load; (2) act like an active resistor at high frequency range to provide damping to the main converter; and (3) for three-phase inverters, decouple the coupling current sources in the main inverter to make the control loop design for the main inverter much easier. This concept has been proved through simulation and experimental results on the 150 kW high performance three-phase utility power supply. The proposed system configuration can be used in high power DC/DC converters, inverters, PFC and UPS applications.

5.2 Difficulties to Reduce Voltage Distortion for High Power Applications

5.2.1 Voltage Distortion and Output Impedance

It is shown in Chapter 4 that the voltage distortion under high power nonlinear loads is extremely large. The voltage distortion is caused by the harmonic voltage drop across the output impedance produced by harmonic currents. Therefore, the key point to reduce the voltage distortion is to reduce the output impedance at frequencies of harmonic currents. Perceivably, there are two ways to reduce the output impedance, as shown in Figure 5-1, by closing the voltage loop and by increasing the switching frequency. In order to show the advantages of high switching frequency, a hypothetical high power four-legged inverter is designed at 20 kHz switching frequency. The resonant frequency of the output filter is designed to be 2 kHz. Due to the higher resonant frequency, the cross-over frequency can be increased to 30 Hz based on the design criteria given in Chapter 4.

It can be seen from Figure 5-1 that by closing the voltage loop, the output impedance is reduced in the frequency range below the cross-over frequency; and there is no reduction beyond the cross-over frequency. Therefore, it is desirable to extend the cross-over frequency in order to have an output impedance reduction at frequencies of harmonic currents. However, it is very difficult to achieve a higher control bandwidth due to the highly under-damped nature of high power converters.

It is also shown in Figure 5-1 that by increasing the switching frequency from 5 kHz to 20 kHz, and changing the output filter design, the output impedance is reduced dramatically. Beyond 6 Hz, the open loop output impedance of the 20 kHz inverter is even lower than that of the 5 kHz inverter with the voltage loop closed. In addition, the higher switching frequency allows the voltage loop to be closed at a higher frequency. The same nonlinear loads in Chapter 4 are simulated with the 20 kHz four-legged inverter with the voltage loop closed. The comparison of the output voltage, load current, and the neutral current is shown in Figure 5-2 and Figure 5-3. It can be seen that the voltage

distortion is reduced dramatically with the 20 kHz inverter. However, it is not practical to implement a 20 kHz hard switching inverter due to the overwhelming switching losses.

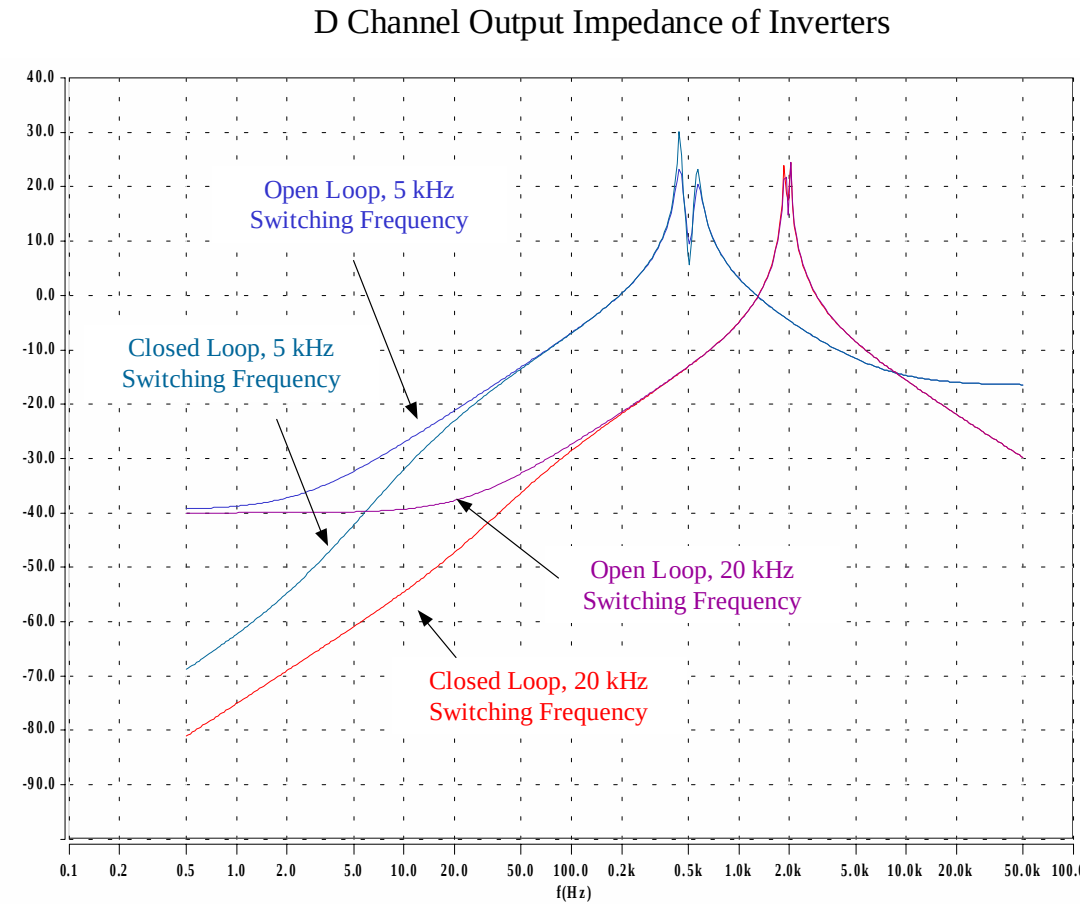
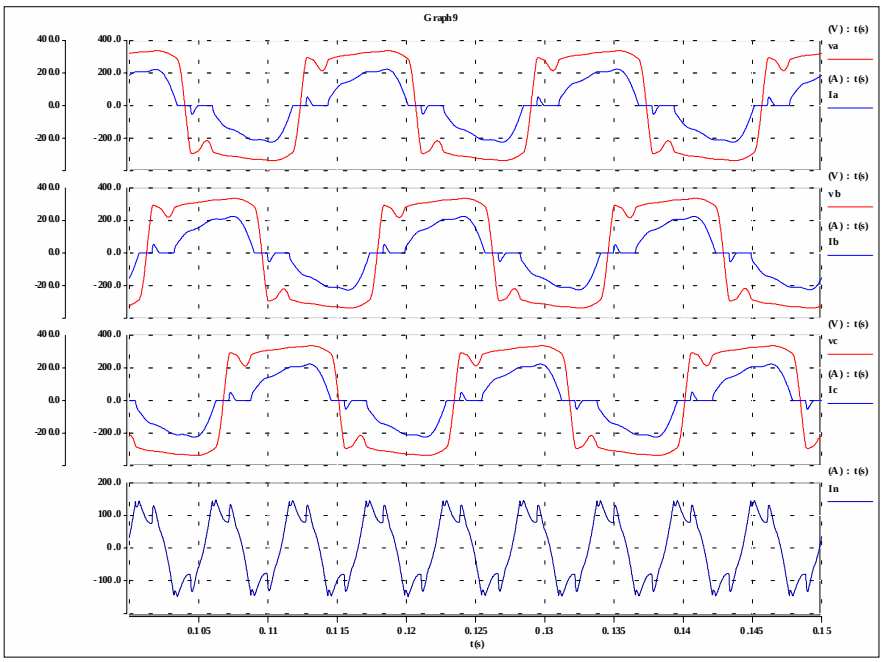


Figure 5-1 D channel output impedances of low switching frequency (5 kHz) and high switching frequency (20 kHz) four-legged inverters with and without closed coltage loops

(a)



(b)

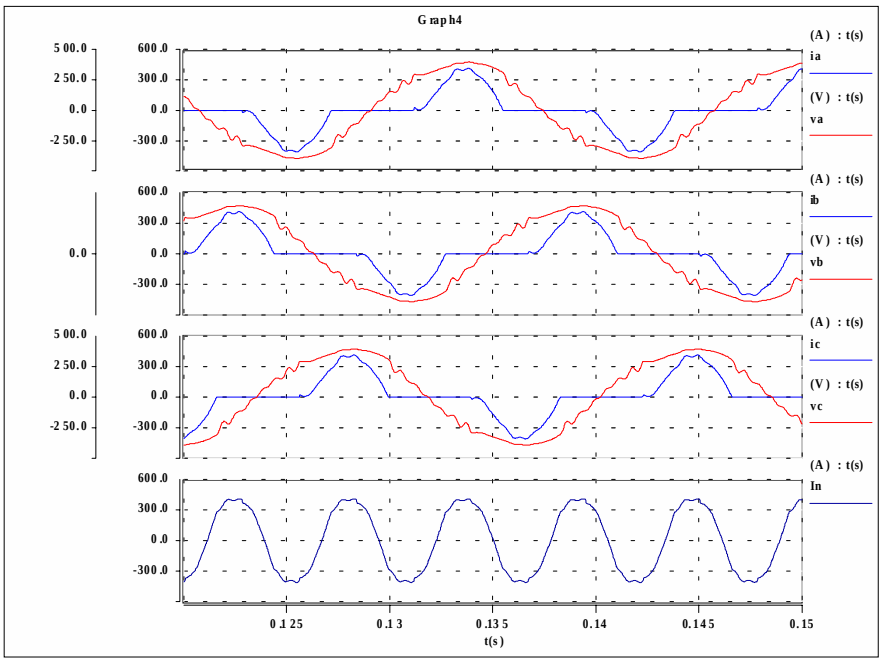
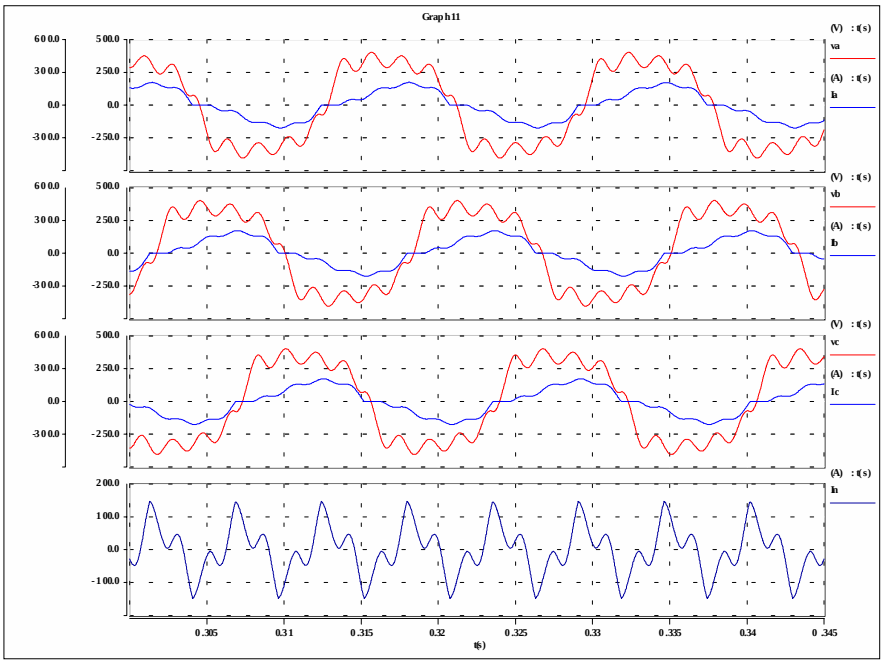


Figure 5-2 Comparison of output voltage, load current and neutral current of four-legged inverters with different switching frequencies with three single-phase diode rectifier with C filter

(a) 5 kHz switching frequency; (b) 20 kHz switching frequency

(a)



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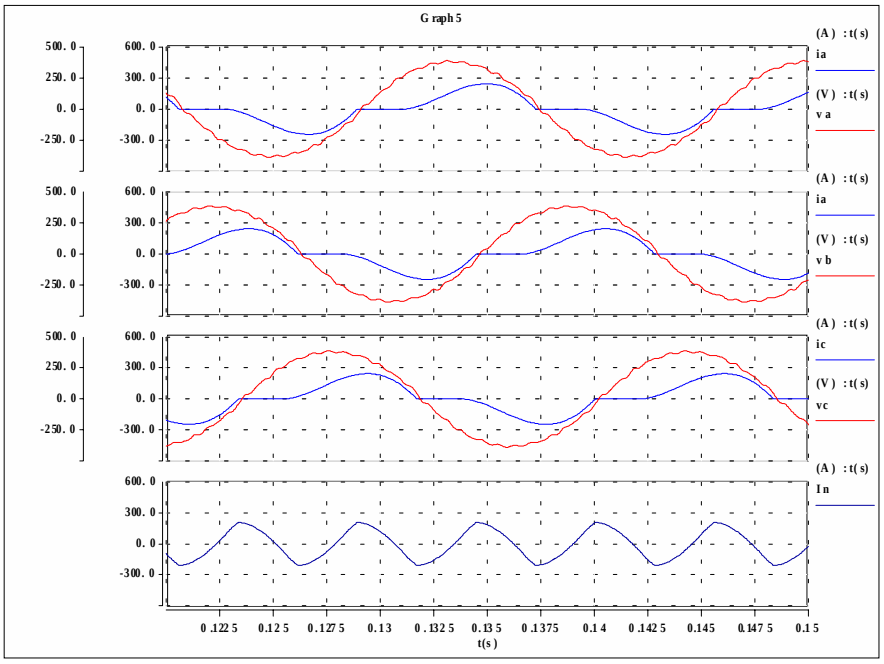


Figure 5-3 Comparison of output voltage, load current and neutral current of four-legged inverters with different switching frequencies with three single-phase diode rectifier with L/C filter

(a) 5 kHz switching frequency; (b) 20 kHz switching frequency

5.2.2 Difficulties with Soft-Switching Inverters

For low and medium power applications, soft-switching techniques are very effective to increasing the switching frequency by reducing the turn-on and/or turn-off losses. Most of the soft-switching techniques use power devices with much lower rating in the auxiliary soft-switching network. They take advantage of the much faster switching characteristics of the lower rating power devices.

For high voltage and high power applications, the power devices used in the auxiliary soft-switching network have to have relatively high voltage and high current ratings, although much lower than the current rating of the main switches. For example, in a 250 kW SMES system, 1200 V/150 A IGBTs have to be used as the auxiliary power switches [C16]. Generally, the switching speed of the auxiliary switches in high power applications is one of the barriers to designing a high power soft-switching inverters. Although there are soft-switching techniques for high power applications, which allow the auxiliary switches switching at a zero-current condition [C15-16], they suffer from a longer dwell time and a larger duty cycle loss.

The commutation of the auxiliary soft-switching network takes a certain amount of time in each switching period. This dwell time causes duty cycle loss, thus larger output distortion due to an inaccurate control. Thus, it is desirable to reduce the commutation time for soft switching by reducing the time constant of the resonant tank in the soft-switching network. However, there are several factors which limit the reduction of the dwell time in practical high power applications, for example, the larger gate drive delay, turn-on and turn-off delay of the auxiliary switches, and larger parasitic inductance and capacitance components due to wiring and layout. Typically the dwell time may be in the range of 6 μs and 10 μs for an application with output power higher than 100 kW. If the switching frequency is designed at 20 kHz, the duty cycle loss would be in the range of 12% to 20%. The effect of the dwell time is shown in Figure 5-4. Increasing the duty cycle loss from 1% to 10% and 20%, a distinct output voltage distortion can be observed. The THD of the output voltage is increased from 1% to 4.3% and 9%, respectively. It is

found that increasing the duty cycle loss leads to higher 3rd, 5th, and 7th harmonics in the output voltage. In particular, the 5th harmonic increases a great amount with a longer dwell time. A feedback control loop may help to reduce the output voltage distortion caused by the long dwell time. However, it is not effective unless the feedback loop has a high control gain at those harmonic frequencies.

The duty cycle loss caused by the dwell time may be solved by disabling the soft-switching commutations when the main switch duty cycle is small. However, depending on the load power factor, current through power switches may be very large when the duty cycle is small. Since the power converter runs into hard switching with a disabled soft-switching network, this solution may greatly reduce the saving of efficiency.

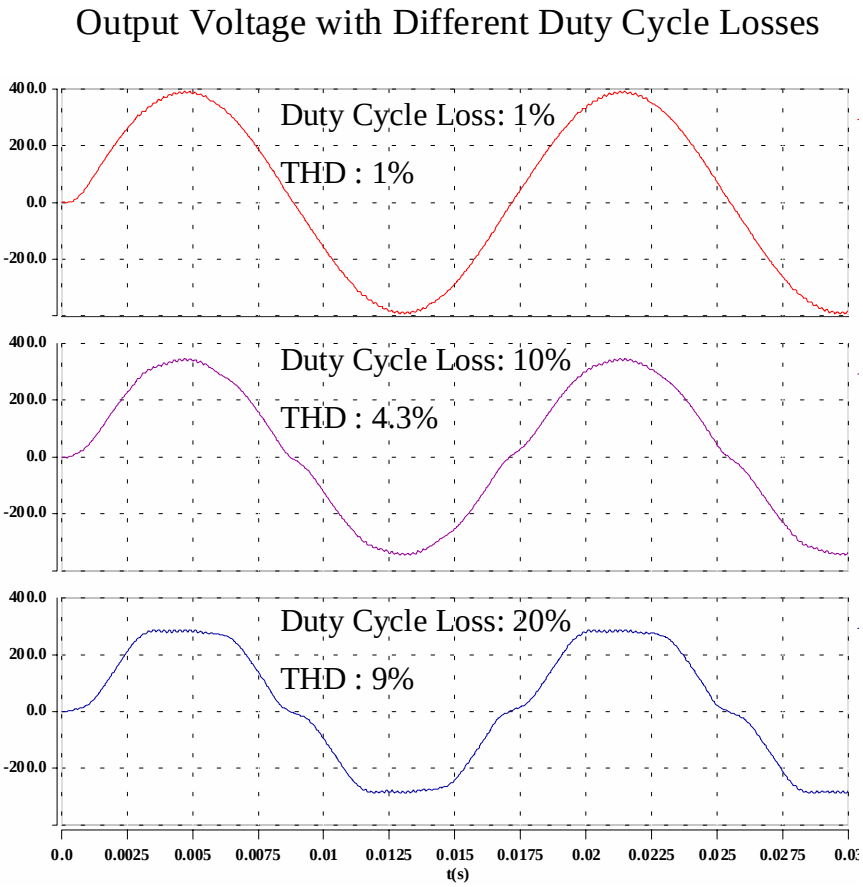


Figure 5-4 Output voltages of a four-legged inverter with different duty cycle losses

5.3 Load Conditioner Concept

5.3.1 Power Converter System with Load Conditioner

The cost to construct a power converter for a certain application is generally proportional to its power level and control bandwidth. The power level of a power converter is determined by its application and ability to withstand overload conditions. It is always desirable for the control bandwidth to be high to achieve high performance, especially for nonlinear loads described in Chapter 2. A high control bandwidth can reduce the output impedance of a power converter; therefore, the harmonic voltage drop across the output impedance due to the harmonic load currents can also be reduced. The outcome is a reduced output voltage distortion. Since a high control bandwidth demands a high switching frequency, a trade-off has to be made due to the associated high switching losses.

Traditionally, one power converter is designed to handle the worst case nonlinear load, as shown in Figure 5-6. This approach results in an excessively high control bandwidth for linear loads. The resulting power converter is very expensive and extremely difficult, if not impossible, to implement in the high power range. To make it even worse, with a given switching frequency, it is more difficult to push the control bandwidth high for a high power converter due to its highly under-damped nature. To ensure stability under light load, the control bandwidth for a high power converter normally has to be designed very low, as discussed in Section 4.7, unless a lossy dummy load is present. Therefore, the system suffers from either degraded performance due to low control bandwidth or poor efficiency and high cost.

This difficult design trade-off can be solved by the proposed power converter system architecture, as shown in Figure 5-6. The system consists of a main converter and a load conditioner. The main converter deals with most of the power flow at a low frequency range. The load conditioner is designed at a much lower power level, since harmonic currents drawn by the nonlinear load are only a small fraction of the total load

current. The load conditioner is running at a high switching frequency and has higher control bandwidth, which gives the overall system high performance.

The main converter sees the combination of the load conditioner and the real load as its equivalent load. The load conditioner can play multiple roles. First, the load conditioner can inject harmonic currents demanded by the nonlinear load so that the main converter sees a linear load; second, the load conditioner can perform the function of a resistor in the high frequency range to damp the main converter. With the help of the load conditioner, it is possible for the main converter to operate under no load; third, for three-phase inverters, the load conditioner can inject counterbalanced coupling currents to decouple the main converter coupling sources, and that makes the main inverter control design much easier.

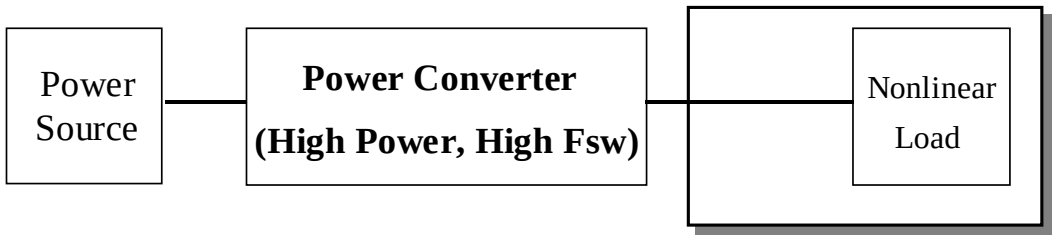


Figure 5-5 Traditional power converter to handle nonlinear load

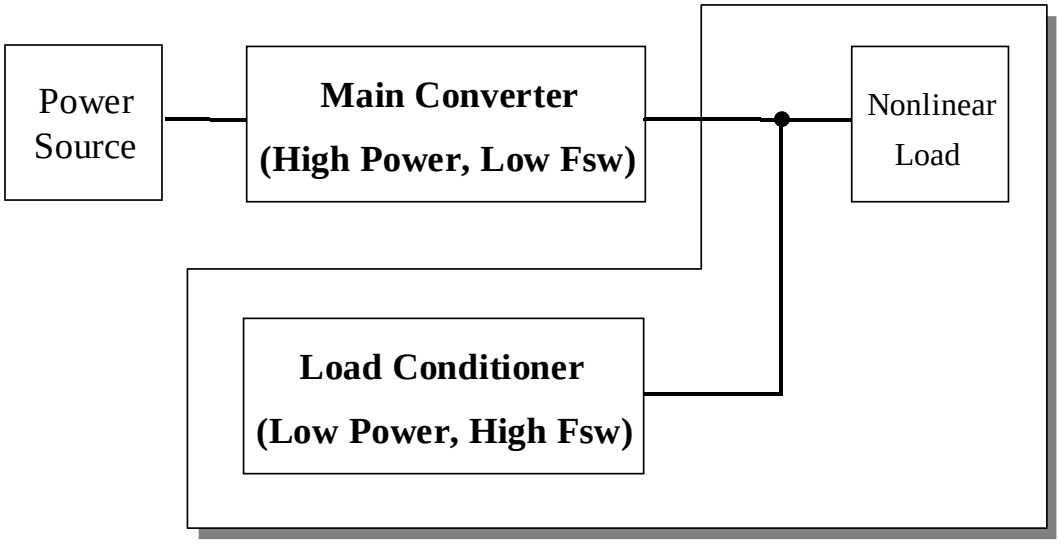


Figure 5-6 Proposed power converter system to handle nonlinear load

5.3.2 Conceptual Example of a Load Conditioner

To explain multiple functions of the load conditioner, a DC/DC converter is used as an example. The DC/DC converter with a closed control loop can be represented by an ideal voltage source with output impedance, as shown in Figure 5-7. When the converter has a nonlinear load, harmonic currents drawn by the nonlinear load flow through the output impedance and produce harmonic voltages at the output. One way to reduce the harmonic voltages is to decrease the output impedance, which calls for higher control bandwidth and thus higher switching frequency. Unfortunately, for high power applications, this means either a system that is much more expensive or technical difficulties that make it unfeasible.

An alternative is to have a load conditioner - a controlled current source - in parallel with the load, as shown in Figure 5-8. The controlled current source can be implemented by another converter with high-bandwidth current control loop. Setting different current references, the load conditioner shapes the equivalent load seen by the main converter by performing multiple functions, such as (1) active filter function, (2) active damping function, and (3) decoupling function for a three-phase inverter.

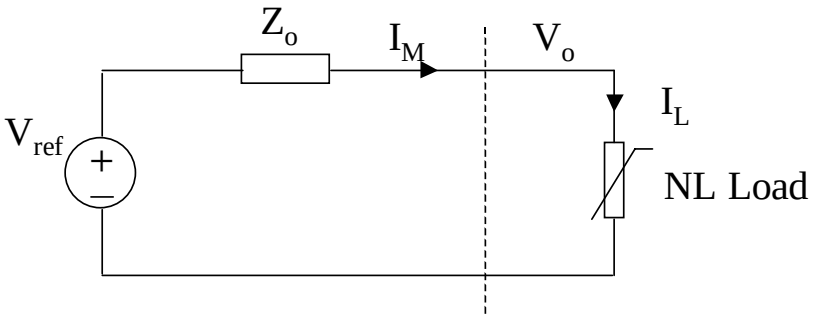


Figure 5-7 Representation of a DC/DC converter with closed control loop

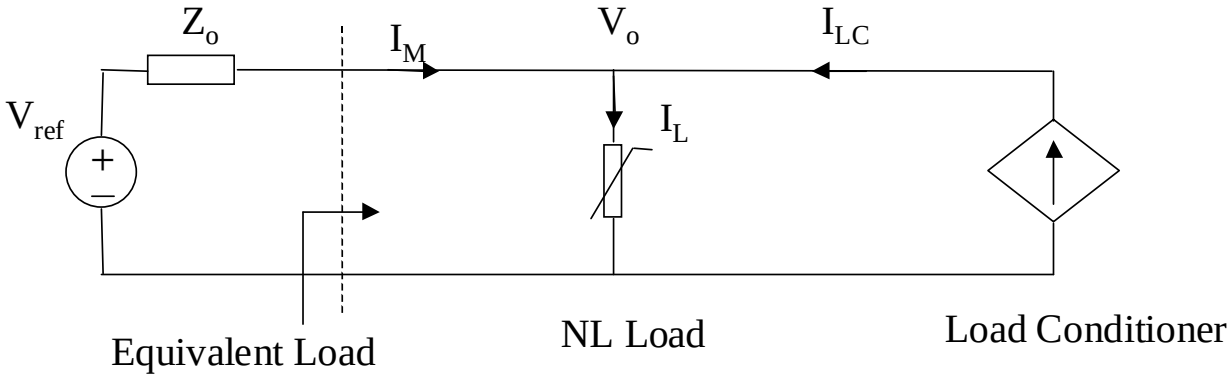


Figure 5-8 Conceptual system configuration with a load conditioner

Function 1: Active Filter

Similar to shunt active filters used in power conditioning systems for utility lines, to perform the function of an active filter harmonic currents drawn by the nonlinear load are sensed and injected by the current source. The current drawn from the main converter will be only DC current. Thus, the converter sees an overall linear load. As shown in Figure 5-9, load current I_L can be expressed as

(5.1) $$I_L = \bar{I}_L + \tilde{I}_L$$

where $\bar{I}_L$ is the dc component, and $\tilde{I}_L$ is the harmonic load current. The current reference for the load conditioner to perform an active filter function is expressed as

(5.2) $$I_{LC\_ref1} = \tilde{I}_L$$

Function 2 : Active Damping

To push the control bandwidth beyond the resonant frequency, it is desirable to damp the resonant peak in the control-to-output transfer function. Instead of using a dummy load, the load conditioner can be used. By setting the controlled current source to be proportional to the output voltage, the load conditioner mimics a resistor load. The damping is needed only around the resonant frequency, the DC current is not required to serve the damping purpose. The current reference to perform the active damping function is shown as

(5.3) $$I_{a\_ref2} = -\frac{\tilde{V}_o}{R_{ac}}$$

where $\tilde{V}_o$ is the harmonic output voltage, and R_{ac} is the ac damping resistance.

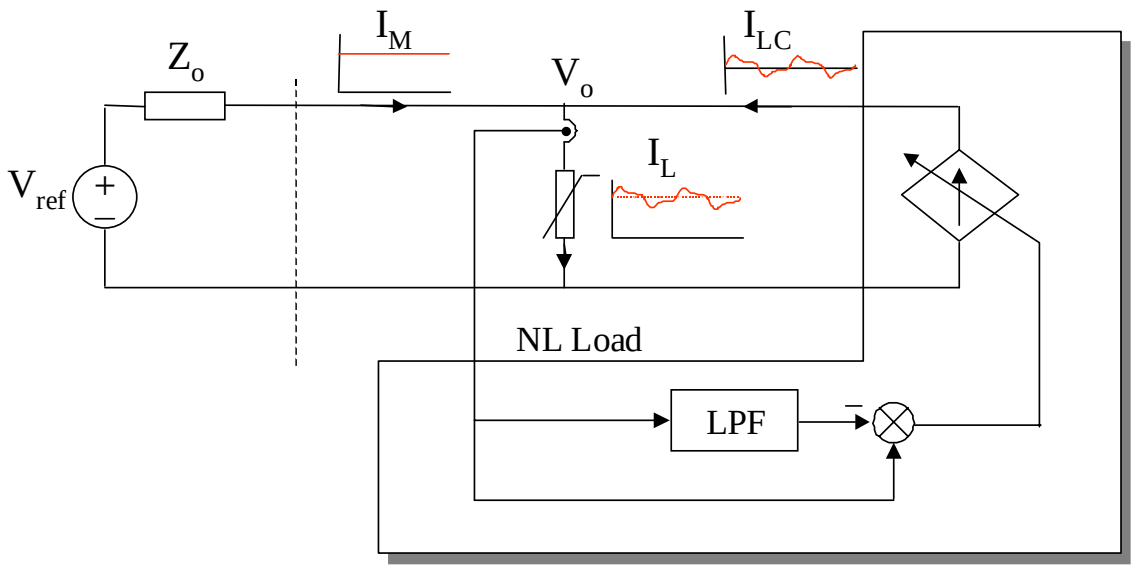


Figure 5-9 Load conditioner performing active filtering function

Figure 5-10 shows the control block diagram needed for the load conditioner to perform the active damping function. Since there is no active power being processed to perform the active damping function, there is no need to increase the power level of the load conditioner. The value of R_{ac} can be designed to be very small for a good damping effect.

Since the two controlled current sources performing the active filter and active damping functions are in parallel, they can be combined and implemented by a power converter with a high current control bandwidth. In the analysis of nonlinear loads in Chapter 2, it is known that the harmonic currents, especially harmonics higher than 7^{th} harmonic, are only a small fraction of the total load current. Therefore, to perform the active filter function, the load conditioner needs to handle only a small fraction of the total power level. The harmonic contents in the output voltage are very small. Therefore, to perform the active damping function, it is not necessary to increase the power level of the load conditioner. To design a high switching frequency load conditioner at a much lower power rating is practical. A high control bandwidth can be achieved for the load conditioner. Overall, the combination of a low switching frequency and high power main converter with a high switching frequency and low power load conditioner would give an overall high system performance under nonlinear loads.

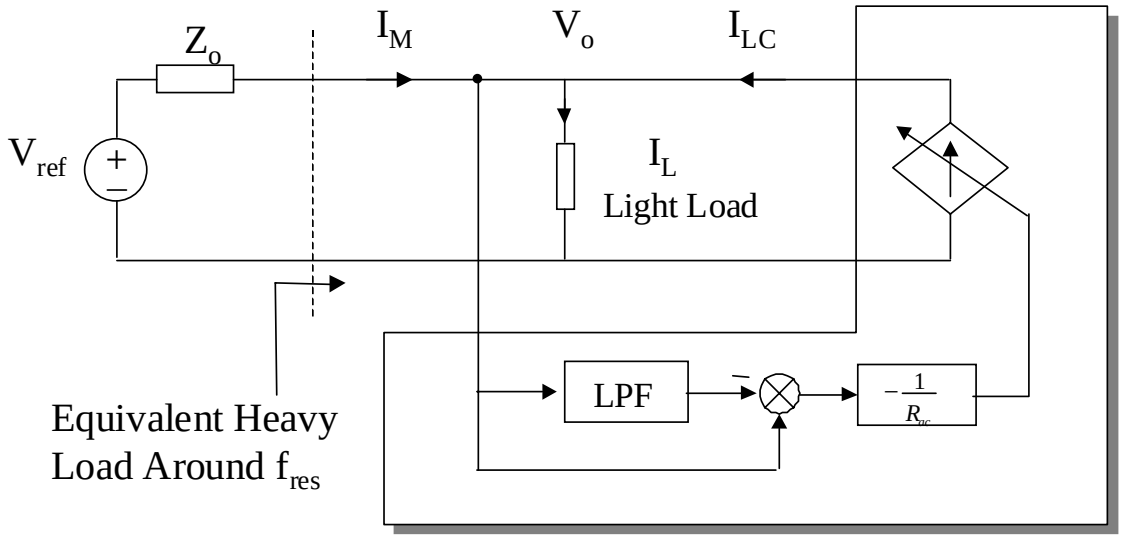


Figure 5-10 Load conditioner performing active damping function

5.4 Design of the Power Converter System

5.4.1 Configuration of the Power Converter System

In order to handle the zero-sequence harmonic load currents, a four-legged power converter can be used as the load conditioner in a power converter system for utility power supply applications. The schematic of the four-legged load conditioner is shown in Figure 5-11.

The DC link of the load conditioner may be provided in two ways: (1) a shared common DC bus with the main inverter; or (2) separate DC buses, as shown in Figure 5-12. The common DC bus configuration seems to be favorable due to its simplicity. However, a switching interaction is found between the main inverter and the load conditioner.

The main inverter and the load conditioner are switching at different switching frequencies, and are controlled separately for different tasks. It is desirable that they be completely decoupled, and the switching actions of the main inverter do not interfere with the operation of the load conditioner, and vise versa. Although in an average sense the load conditioner output current can be controlled, in each switching cycle there is a current circulating path between the main and the load conditioner. The main inverter inductor current ripple is coupled into the load conditioner through the coupling paths. Since the load conditioner is designed at a much lower power level, the circulating current ripple from the main inverter may drive the load conditioner inductor into saturation and cause failure. Even if the load conditioner still operates, due to the uncontrollable switching level circulating ripple current, the main inverter inductor current, and thus the output voltage, is significantly degraded.

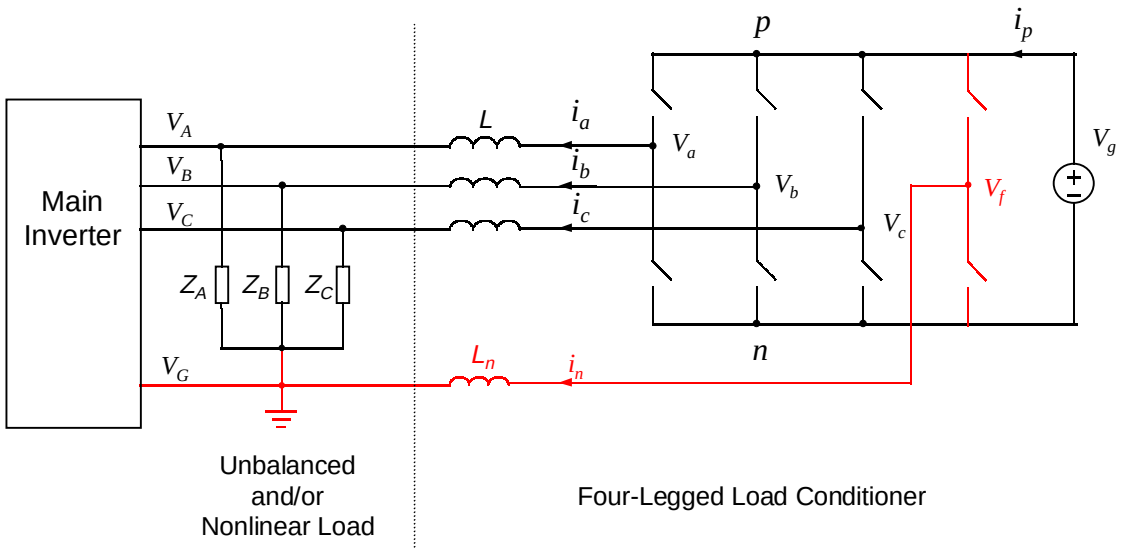
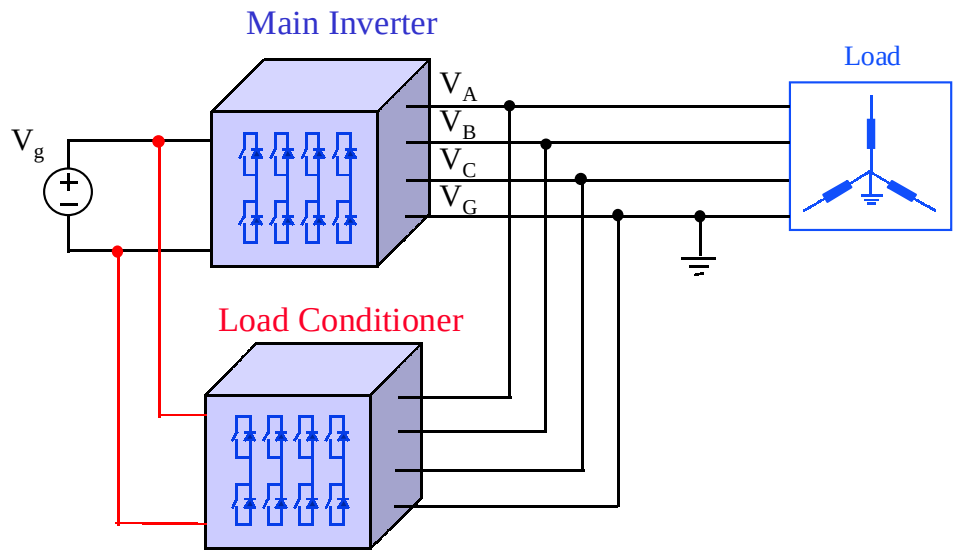
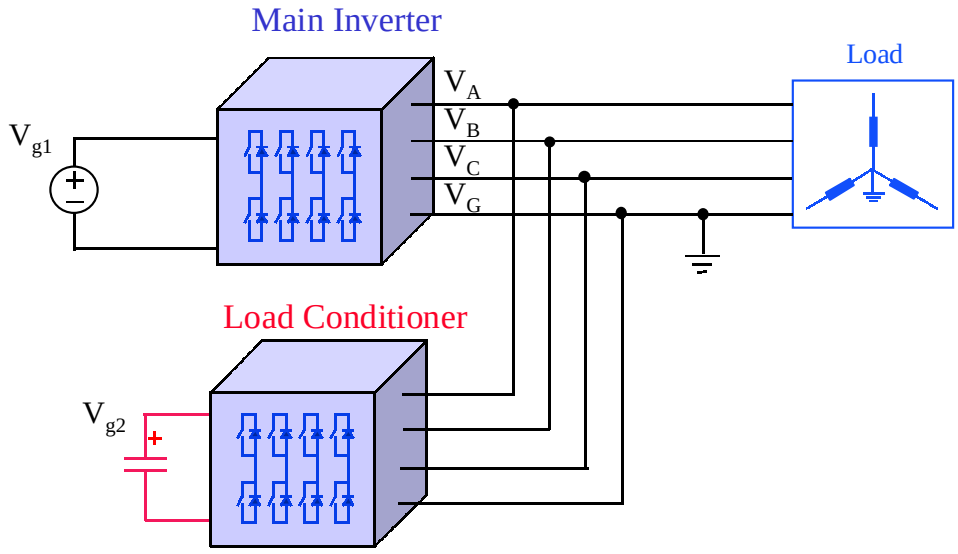


Figure 5-11 Four-legged load conditioner for utility power supply



(a)



(b)

Figure 5-12 Configuration of the power converter system

(a) a common DC bus; (b) separate DC buses

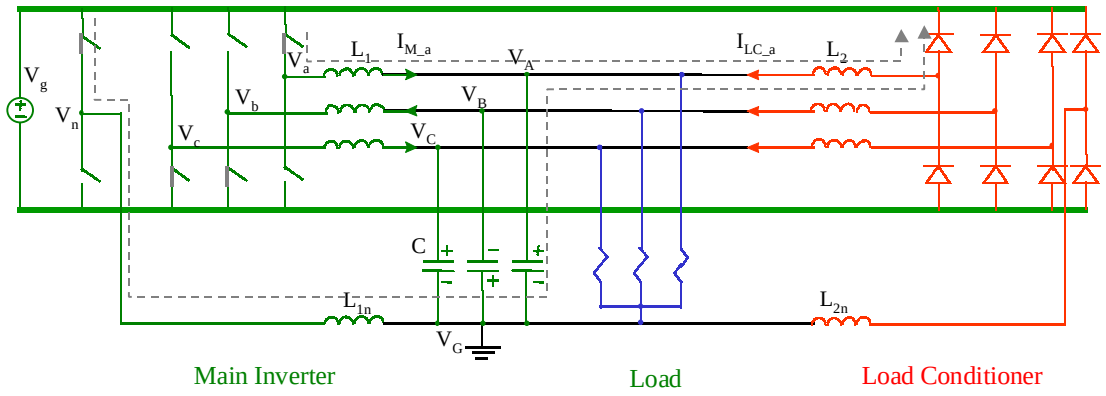


Figure 5-13 Switching interaction between the main inverter and load conditioner

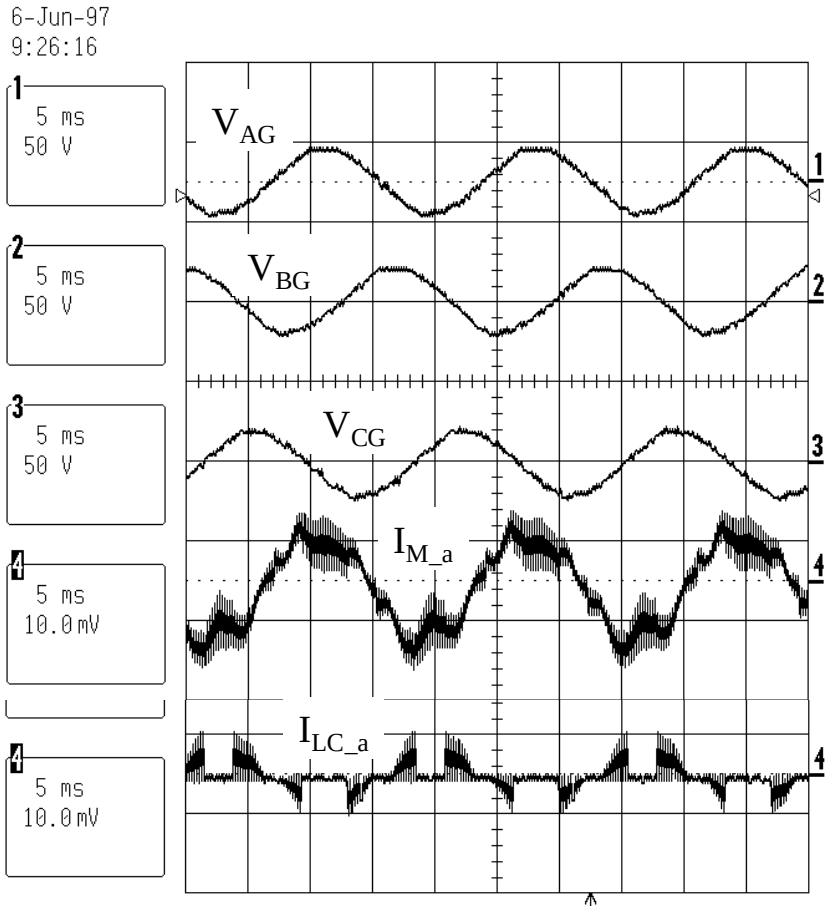


Figure 5-14 Key waveforms with a common DC bus

An example is given in Figure 5-13 to show the path of the circulating ripple current. When V_{AG} >0, V_{BG} <0, and V_{CG} >0, the reference vector may be in prism II tetrahedron 2. The switching vector pnnp may be applied, as shown in Figure 5-13. Since the V_n is connected to the positive DC rail, the voltage potential of V_A is higher than the positive DC rail. Therefore, there is a path for the ripple current, as indicated as the broken line, to circulate between the main inverter and the load conditioner. The result is switching ripple currents in the load conditioner, distorted main inverter current, and distorted output voltage, as seen in Figure 5-14. The circulating current ripple issue is not unique for a four-legged inverter. In fact, three-legged converters in parallel without synchronized switching actions may have the same switching interaction problem [D1][D5~7].

With the separate DC bus scheme, as shown in Figure 5-15, the circulating path does not exist. When the load conditioner runs as a diode bridge rectifier by disabling its gate drive signals, there is no switching ripple current going through the load conditioner. The main inverter current distortion and the output voltage distortion disappear, as shown in Figure 5-16. Therefore, the separate DC bus configuration is the only choice for the power converter system. Due to the separated DC buses, an additional voltage loop has to be added to control the DC link voltage of the load conditioner.

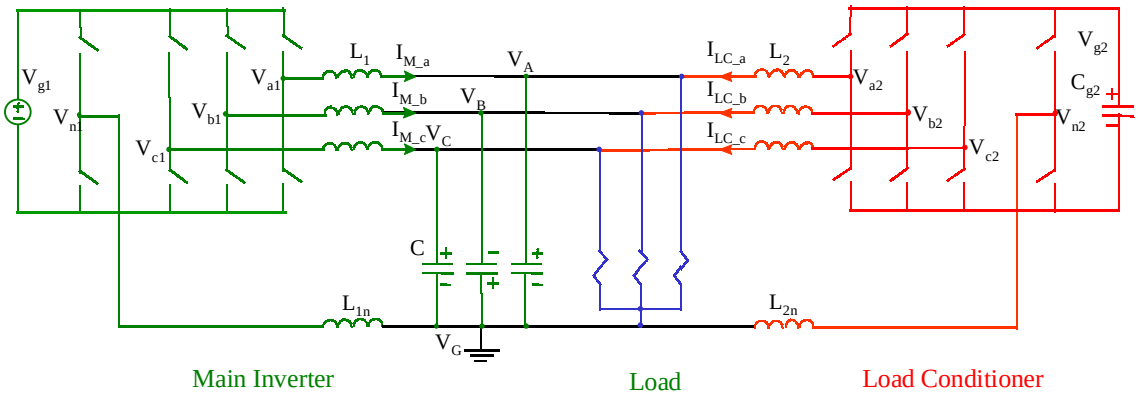


Figure 5-15 Power converter system with separate DC buses

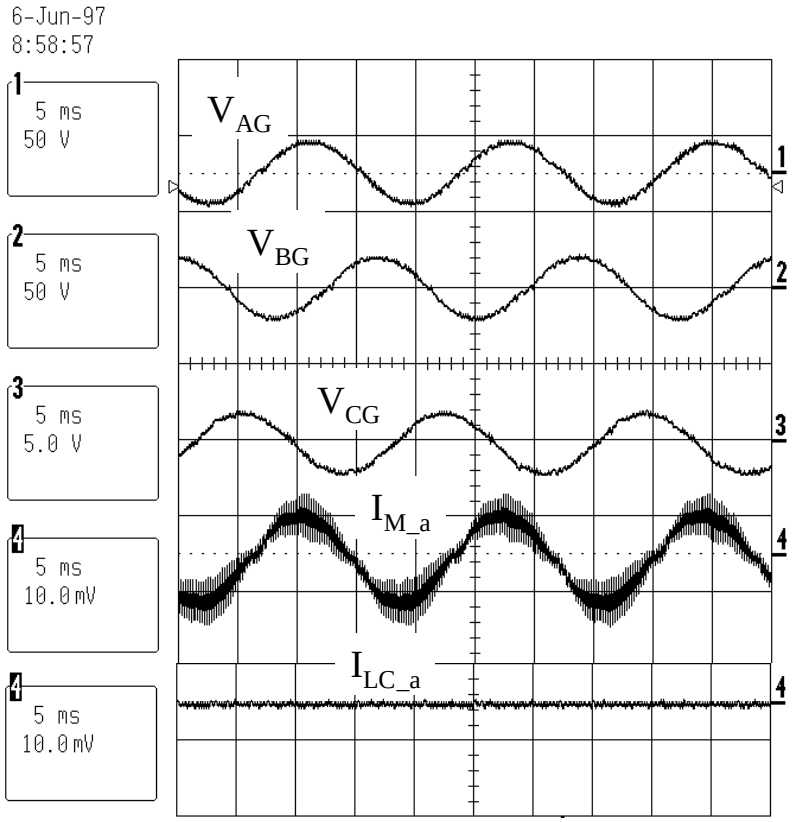


Figure 5-16 Key waveforms with separate DC buses

5.4.2 Design Consideration for the Load Conditioner

Power Level: power level of the load conditioner depends on how much harmonic load currents need to be handled by the load conditioner. It can be seen from the nonlinear load examples in Chapter 2 that the rms value of harmonic currents higher than or equal to 7^{th} harmonic is about 20% ~ 35% of the fundamental current. With the help of the load conditioner, we could increase the control bandwidth of the main inverter so that up to 5^{th} harmonic currents may be handled by the main inverter. Therefore, the power level of the load conditioner for the power converter system is selected to be 20% of that of the main inverter.

DC Link Voltage: the DC link voltage of the load conditioner is designed to be the same as that of the main inverter for the same reason as discussed in Chapter 3.

DC Link Capacitance: while a negative-sequence current at the fundamental frequency ω would draw a 2ω ripple power from the DC link, both the 5^{th} and 7^{th} harmonic load currents draw a ripple power at 6ω frequency. The equation to calculate the DC link capacitance for the load conditioner is similar to (3.13). Compared with the calculation of the main inverter DC capacitance, the DC link capacitance for the load conditioner for the same amount of ripple voltage should be scaled down three times due to the higher frequency (6ω) ripple power, and scaled down 60% due to the less ripple power level. In this practical design example, referring to the main inverter DC link capacitance design in Chapter 3, the DC link capacitance for the load conditioner turned out to be 1000 μF.

Switching Frequency: since a wide current control bandwidth is needed, a higher switching frequency is desirable. Based on the loss calculation and cooling condition, switching frequency of the load conditioner is designed to be 20 kHz.

Inductors: the load conditioner is a controlled current source; a small ripple current is desirable for an accurately controlled current. For the design example, the

inductors for each phase are designed to be 400 μH, and the neutral leg inductor is designed to be 130 μH.

5.5 Modeling of the Power Converter System

5.5.1 Modeling of the Load Conditioner in d-q-o Coordinate

As can been seen from Figure 5-11, the four-legged load conditioner is very similar to the four-legged PWM rectifier, except it is controlled for a bi-directional power conversion and there is no load at its DC link. All the modeling done for the four-legged PWM rectifier is applicable to the load conditioner, except that for the sake of convenience, all the current directions are reversed. Assuming an ideal three-phase four-wire voltage as the input to the load conditioner, the model of the load conditioner in d-q-o coordinate are expressed as

$$\frac{d}{dt}\begin{bmatrix} I_{d2} \\ I_{q2} \\ I_{o2} \end{bmatrix} = V_{g2}G_2\begin{bmatrix} d_{d2} \\ d_{q2} \\ d_{o2} \end{bmatrix} - G_2\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} + \omega\begin{bmatrix} I_{q2} \\ -I_{d2} \\ 0 \end{bmatrix} \qquad \textbf{(5.4)}$$

$$\text{where } G_2 = \begin{bmatrix} \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{L_2 + 3L_{n2}} \end{bmatrix}$$

$$\frac{dV_{g2}}{dt} = -\frac{1}{C_{g2}}\begin{bmatrix} \frac{3}{2}d_{d2} & \frac{3}{2}d_{q2} & 3d_{o2} \end{bmatrix}\begin{bmatrix} I_{d2} & I_{q2} & I_{o2} \end{bmatrix}^T \qquad \textbf{(5.5)}$$

The model described in (5.4) and (5.5) can be represented by the average large-signal circuit model shown in Figure 5-17. The small signal model of the load conditioner is shown in Figure 5-18**.**

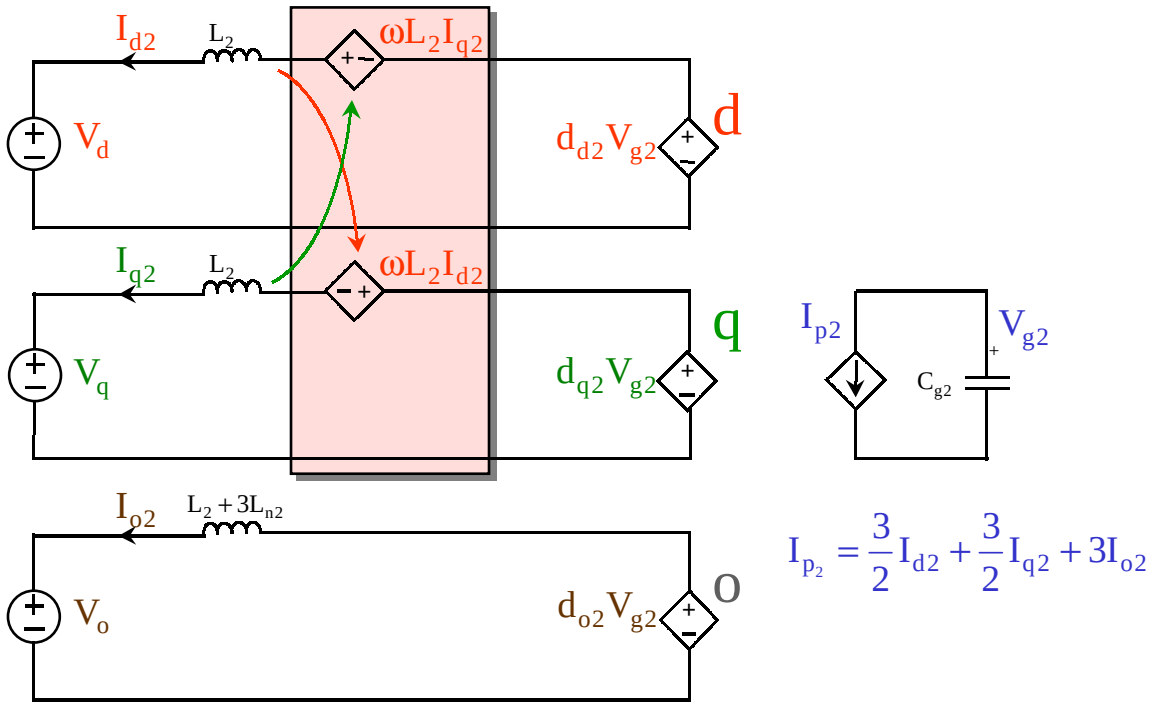


Figure 5-17 Average large-signal model of load Conditioner in d-q-o coordinate

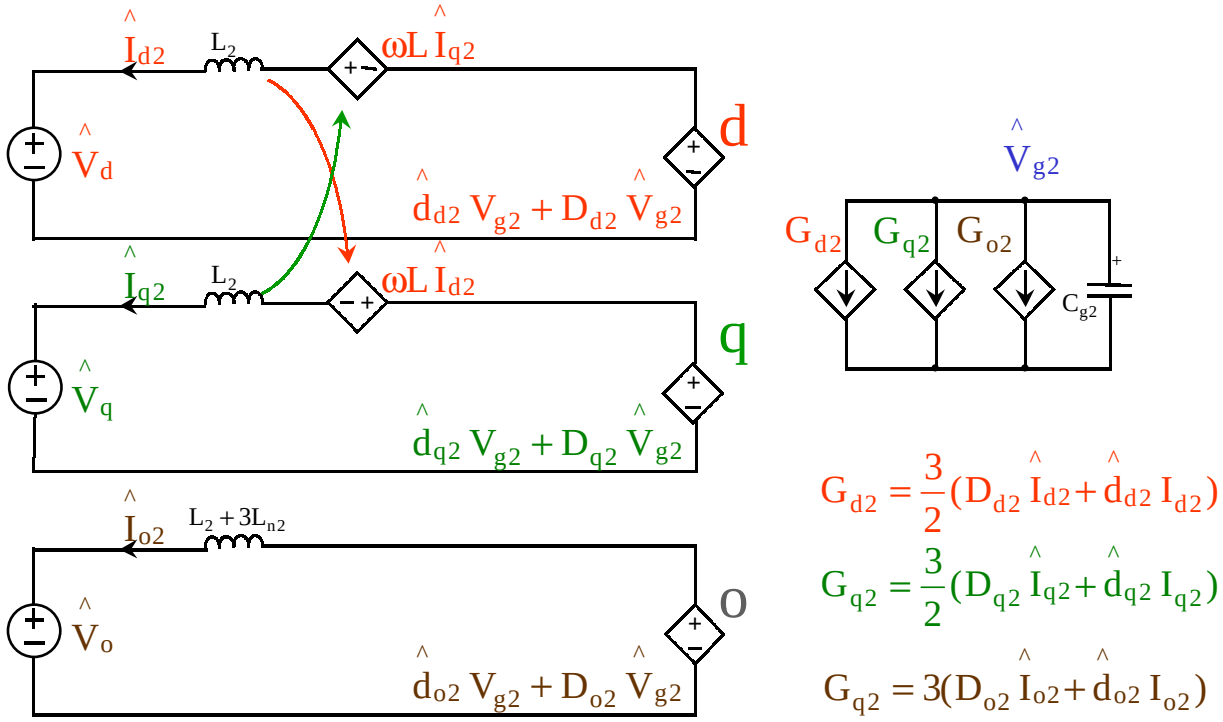


Figure 5-18 Small-signal model of load conditioner in d-q-o coordinate

5.5.2 Modeling of the Power Converter System in d-q-o Coordinate

The inputs of the load conditioner in d-q-o coordinate V_d, V_q and V_o are outputs of the main inverter. By cascading the main inverter model shown in Figure 4-2 with the load conditioner model shown in Figure 5-17, the power converter system average large-signal circuit model is obtained and shown in Figure 5-19. From the circuit model, we have the main inverter inductor current expressed as

$$\frac{d}{dt}\begin{bmatrix} I_{d1} \\ I_{q1} \\ I_{o1} \end{bmatrix} = V_{g1}G_1\begin{bmatrix} d_{d1} \\ d_{q1} \\ d_{o1} \end{bmatrix} - G_1\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} + \omega\begin{bmatrix} I_{q1} \\ -I_{d1} \\ 0 \end{bmatrix} \quad \textbf{(5.6)}$$

the load conditioner inductor current expressed as

$$\frac{d}{dt}\begin{bmatrix} I_{d2} \\ I_{q2} \\ I_{o2} \end{bmatrix} = V_{g2}G_2\begin{bmatrix} d_{d2} \\ d_{q2} \\ d_{o2} \end{bmatrix} - G_2\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} + \omega\begin{bmatrix} I_{q2} \\ -I_{d2} \\ 0 \end{bmatrix} \quad \textbf{(5.7)}$$

where $G_1 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_1 + 3L_{n1}} \end{bmatrix}$ and $G_2 = \begin{bmatrix} \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{L_2 + 3L_{n2}} \end{bmatrix}$,

the output voltage expressed as

$$\frac{d}{dt}\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \omega\begin{bmatrix} V_q \\ -V_d \\ 0 \end{bmatrix} + \frac{1}{C}\left\{\begin{bmatrix} I_{d1} \\ I_{q1} \\ I_{o1} \end{bmatrix} + \begin{bmatrix} I_{d2} \\ I_{q2} \\ I_{o2} \end{bmatrix} - \begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{Lo} \end{bmatrix}\right\} \quad \textbf{(5.8)}$$

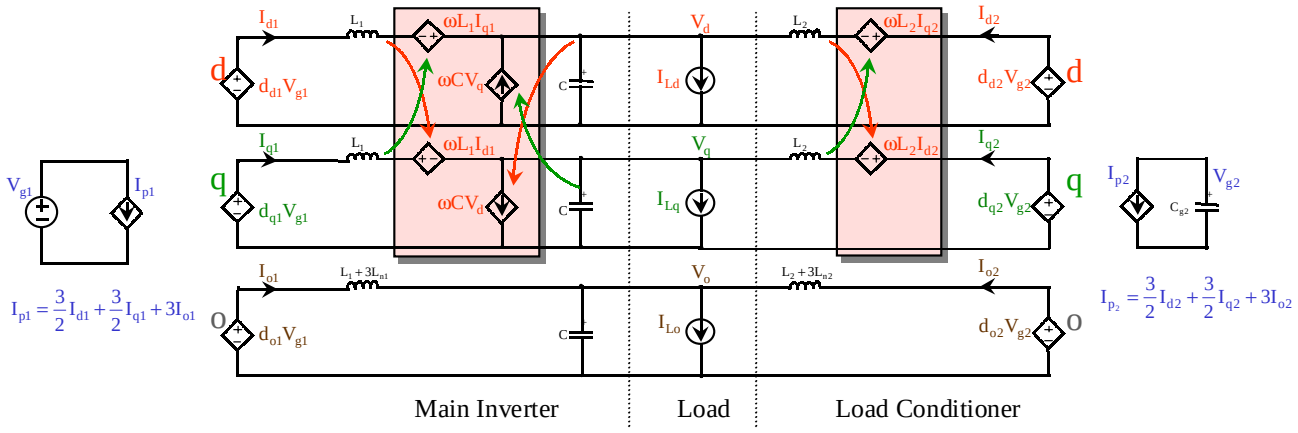


Figure 5-19 Average large-signal model of the power converter system in d-q-o coordinate

the main inverter DC link current expressed as

(5.9) $$I_{P1} = \begin{bmatrix} \frac{3}{2}d_{d1} & \frac{3}{2}d_{q1} & 3d_{o1} \end{bmatrix} \begin{bmatrix} I_{d1} & I_{q1} & I_{o1} \end{bmatrix}^T$$

the load conditioner DC link voltage expressed as

(5.10) $$\frac{dV_{g2}}{dt} = -\frac{1}{C_{g2}} \begin{bmatrix} \frac{3}{2}d_{d2} & \frac{3}{2}d_{q2} & 3d_{o2} \end{bmatrix} \begin{bmatrix} I_{d2} & I_{q2} & I_{o2} \end{bmatrix}^T$$

In the steady state for a linear load, we should have

(5.11) $$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \begin{bmatrix} V_{ln\_pk} \\ 0 \\ 0 \end{bmatrix}$$

Since all the load conditioner inductor current is equal to zero, V_{g2} remains unchanged.

(5.12) $$\begin{bmatrix} d_{d2} \\ d_{q2} \\ d_{o2} \end{bmatrix} = \begin{bmatrix} \frac{V_{ln\_pk}}{V_{g2}} \\ 0 \\ 0 \end{bmatrix}$$

The steady state solution for the main inverter should be the same as given in (4.29) and (4.31)

Small-signal model of the power converter system can also be obtained by perturbing the system around the operating point.

5.6 Control of the Power Converter System

5.6.1 Control Block Diagram for the Power Converter System

The power converter system control block diagram is shown in Figure 5-20. The load conditioner is controlled with a current loop compensator superimposed by a voltage compensator to control its DC link voltage. The current reference generator is the key for the load conditioner to perform the active filtering, active damping, and decoupling functions. The main inverter has only a voltage loop closed. The cross-over frequencies of the current loops of the load conditioner and the main inverter voltage loop are well separated.

The procedure to design the control loops for the power converter system is: first, the load conditioner current loops are designed to perform the multiple functions; second, with the current loop of the load conditioner closed, the main inverter voltage loop is closed.

5.6.2 Control Design of the Load Conditioner

5.6.2.1 Current Loops of the Load Conditioner

Since the cross-over frequencies of the main inverter and the load conditioner are well separated, to simplify the design of the load conditioner current loops, an ideal three-phase four-wire voltage source is assumed. The load conditioner control block diagram is shown in Figure 5-21. A time delay T_{d2} of 87.5 μs is considered due to the digital sampling delay and PWM delay. It can be seen that the coupling voltage sources can be easily decoupled by the two coupling gain blocks $\frac{\omega L_2}{V_{g2\_ref}}$. Proportional gain compensators are used as current compensators. With a design of $K_{id} = K_{iq} = 9.28e\text{-}3$ and $K_{io} = 30e\text{-}3$, the current loop gain transfer functions are shown in Figure 5-22. It can be

seen that the current loops are closed at 3 kHz with 35 degree phase margin. There is almost 40 dB separation between direct and coupling transfer functions. Therefore, d and q channels are decoupled.

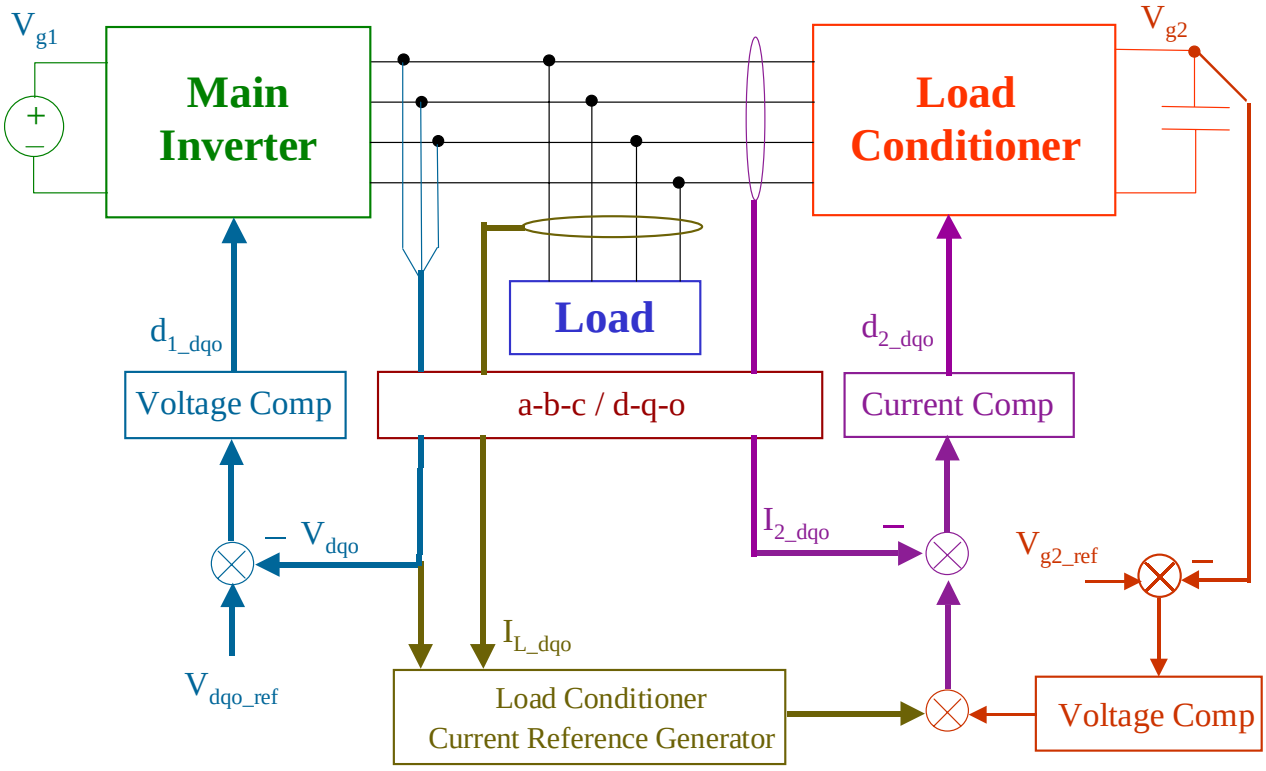


Figure 5-20 Power converter system control block diagram

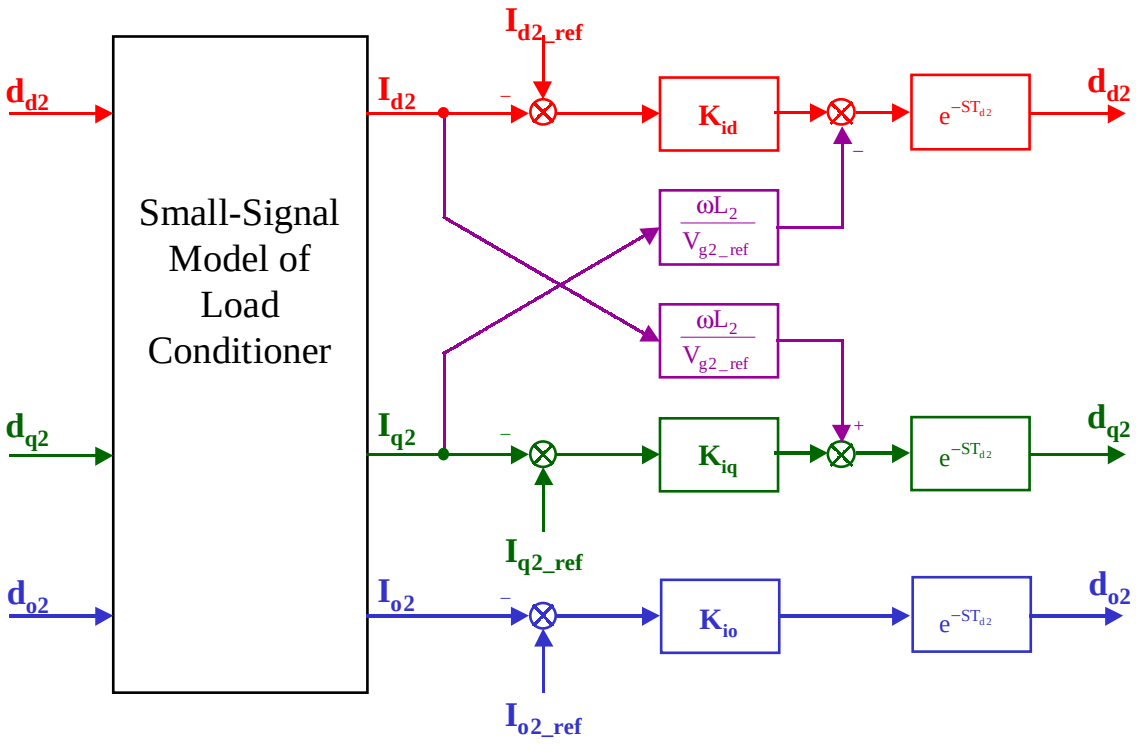


Figure 5-21 Current control block diagram for the load conditioner

The most important control aspect of the load conditioner is the generation of the current references. The d, q and o channel current references are expressed as

$$\begin{aligned} I_{d2\_ref} &= I_{d2\_ref1} + I_{d2\_ref2} + I_{d2\_ref3} + I_{d2\_ref4} \\ I_{q2\_ref} &= I_{q2\_ref1} + I_{q2\_ref2} + I_{q2\_ref3} \\ I_{o2\_ref} &= I_{o2\_ref1} + I_{o2\_ref2} \end{aligned} \qquad \textbf{(5.13)}$$

where I_{d2_ref1}, I_{q2_ref1} and I_{o2_ref1} give current commands to perform the active filtering function; I_{d2_ref2}, I_{q2_ref2} and I_{o2_ref2} give current commands to perform the active damping function; I_{d2_ref3}, I_{q2_ref3} give current commands to perform the decoupling function; and I_{d2_ref4} is the negative output of the superimposed load conditioner voltage compensator.

5.6.2.2 Control of the Load Conditioner DC Link Voltage

The design procedure for the load conditioner DC link voltage loop is very similar to that of a PWM rectifier, which has been comprehensively discussed in [H1]. The difference is that the output of the load conditioner DC link voltage compensator is much smaller compared to that of a PWM rectifier under a heavy load. Since there is no load across the DC link capacitor, there is no active power delivered. The output of the voltage compensator keeps a small value to compensate the power losses. A PI compensator is used as the voltage compensator. The voltage loop bandwidth should be designed very low to prevent it from interfering with the current loops.

During start-up, the load conditioner operates like a four-legged PWM rectifier to build up the DC link voltage. The voltage loop outputs a DC value to draw a maximum three-phase sinusoidal current from the output of the main inverter. In the steady state operation with a linear load, the output of the voltage loop is almost zero.

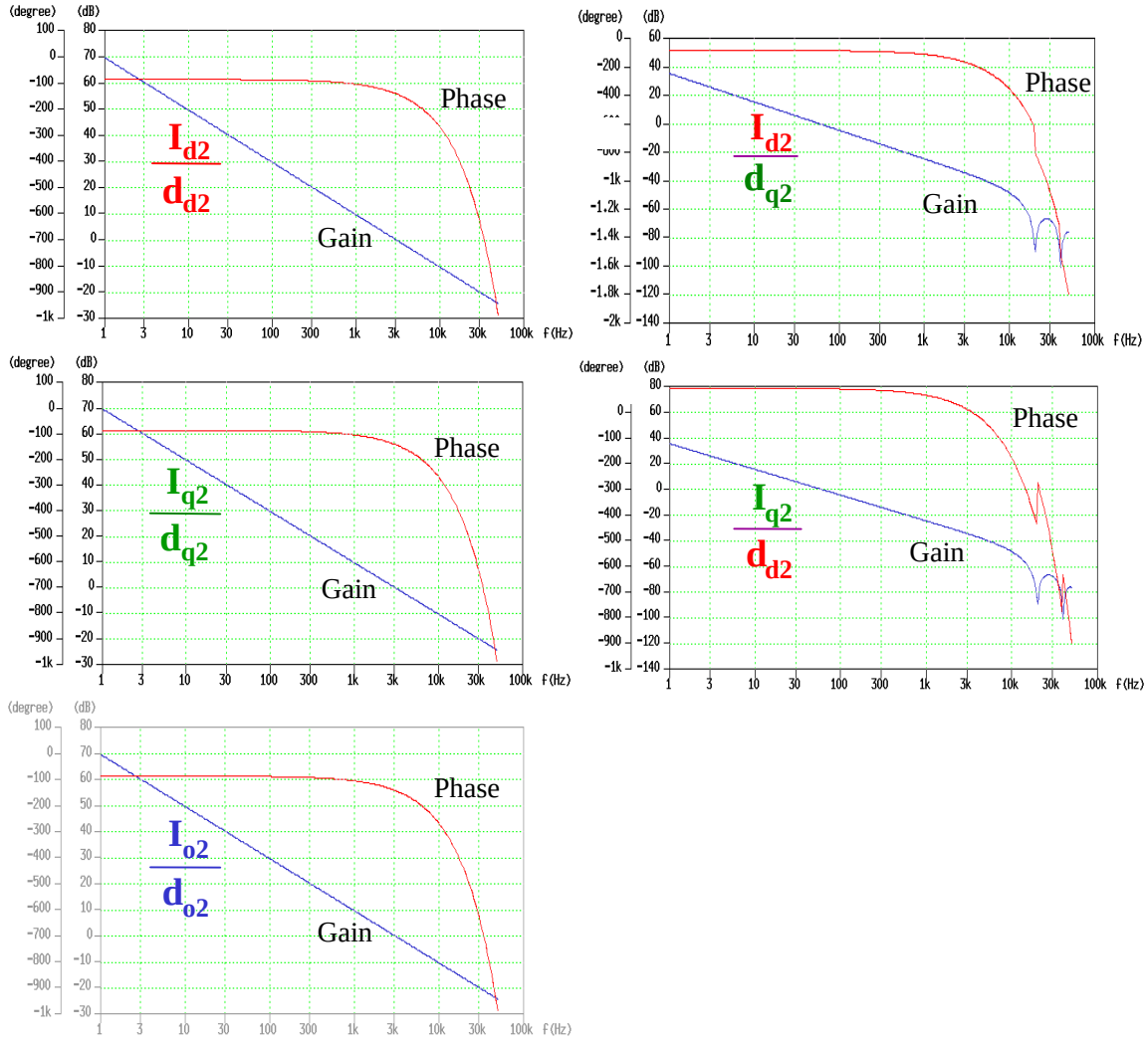


Figure 5-22 Control-to-inductor current loop gain transfer functions of the load conditioner at no load condition

5.6.2.3 Active Filtering Function

To perform the active filtering function, the load conditioner injects load harmonic currents. The power level of the load conditioner and the amplitudes of each individual harmonic current determine the lowest harmonic current that the load conditioner can handle. As discussed before, for a load conditioner with 20% of the rated power level, harmonics higher than 7^{th} can be handled by the load conditioner. The current reference for the active filter function is expressed as

$$\begin{aligned} I_{d2\_ref1} &= \tilde{I}_{Ld} \\ I_{q2\_ref1} &= \tilde{I}_{Lq} \\ I_{o2\_ref1} &= \tilde{I}_{Lo} \end{aligned} \qquad \textbf{(5.14)}$$

With the load condition performing the active filtering function, the main inverter control-to-output voltage transfer functions are shown in Figure 5-24. Compared with those shown in Chapter 4, it can be seen that the resonant peak is damped slightly due to the current loop control of the load conditioner. However, the resonant peak is still high; the direct and the coupling channel transfer functions are still close to each other.

5.6.2.4 Active Damping Function

It has been pointed out in the load conditioner concept that to perform the active damping function only harmonic voltage is needed. Therefore, the current references to perform the active damping function are expressed as

$$\begin{aligned} I_{d2\_ref2} &= -\frac{\tilde{V}_d}{R_{ac}} \\ I_{q2\_ref2} &= -\frac{\tilde{V}_q}{R_{ac}} \\ I_{o2\_ref2} &= -\frac{\tilde{V}_o}{R_{ac}} \end{aligned} \qquad \textbf{(5.15)}$$

where R_{ac} is the damping resistance at the resonant frequency. It is desirable for R_{ac} to be as small as possible to have a good damping effect. However, R_{ac} should be large enough that the inductors are not saturated during transients. A R_{ac} representing 40% of the rated output power is used for the example system.

When the load conditioner performs both the active filter and active damping function, the main inverter control-to-output voltage transfer functions are well damped, as shown in Figure 5-25. The well damped transfer functions allow the cross-over frequencies of the closed voltage loops to be extended easily, close to the resonant frequencies. The direct and coupling transfer functions are also separated by 10 ~14 dB.

5.6.2.5 Decoupling Function

In designing control loops for a multi-input-multi-output system, it is normally desirable to decouple the system to be single-input-single-output systems. It was mentioned in Chapter 4 that the coupling voltage sources $\omega L_1 I_{d1}$ and $\omega L_1 I_{q1}$ of the main inverter, as shown in Figure 4-3, can be decoupled easily, since they are in series with the controlled voltage sources $d_{d1}V_{g1}$ and $d_{q1}V_{g1}$, respectively. However, since the control variables do not have direct control to the coupling current sources ωCV_d and ωCV_q, the coupling current sources cannot be easily decoupled. Fortunately, the load conditioner is a current source in parallel with the coupling current sources. By setting the current reference to be exactly same as the coupling current source and reversing the current direction, the coupling current sources can be canceled out. Therefore, d and q channels can be completely decoupled. However, this would require the load conditioner to deliver active power.

It can be seen from Figure 4-14 that the coupling happens around the resonant frequency. D and q channels can be effectively decoupled by using only harmonic voltages as the current references. The final current references to perform the decoupling function are expressed as

(5.16)

$$I_{d2\_ref3} = -\omega C \tilde{\tilde{V}}_q$$
$$I_{q2\_ref3} = \omega C \tilde{\tilde{V}}_d$$

where $\tilde{\tilde{V}}_d$ and $\tilde{\tilde{V}}_q$ are high-order (greater than 7^{th}) voltage harmonics.

With the load conditioner performing the active filtering, active damping, and the active decoupling functions, the main inverter control-to-output voltage transfer functions are shown in Figure 5-26. It can be seen that there is an additional 10 dB separation between the direct and coupling transfer functions. The incomplete decoupling is caused by the 87.5 μs time delays in the control loops.

5.6.2.6 Summary of Current Reference Generation

Figure 5-23 summarizes all the load conditioner current references. The high-order harmonic currents and voltages are obtained by using high-pass filters (HPF). The effectiveness of the load conditioner is verified by the measured main inverter control-to-output voltage transfer functions under no load condition, as shown in Figure 5-27. By setting R_{ac} to 5 ohm, which represents 40% of the rated load at high frequency, the resonant peak of both the direct transfer function $\frac{V_d}{d_{d1}}$ and the coupling transfer function $\frac{V_d}{d_{q1}}$ are well damped due to the active damping function; the direct transfer function and the coupling transfer function are separated by more than 10 dB due to the decoupling function.

5.6.2.7 Harmonic Current/Voltage Extraction

Harmonic currents or voltages are obtained by subtracting the dc component from the total currents or voltages, as shown in Figure 5-28. The advantage of using this kind of HPF structure is that there is no phase shift in the extracted harmonic components.

For this utility power supply application, the output frequency is fixed. With a digital controller, a moving average operand is a good choice to implement the low pass filter due to its simplicity and accuracy. A moving average operand is a special FIR filter with all the coefficients equal to one. All gains at the multiple times of the window frequency are equal to zero, as shown in Figure 5-29. In this case, gains at 60 Hz and multiple times of 60 Hz components are zero. Assuming there are no sub-harmonic components in the system, the DC component can be accurately extracted. It can be easily implemented using a circular buffer in the digital controller described in Chapter 4.

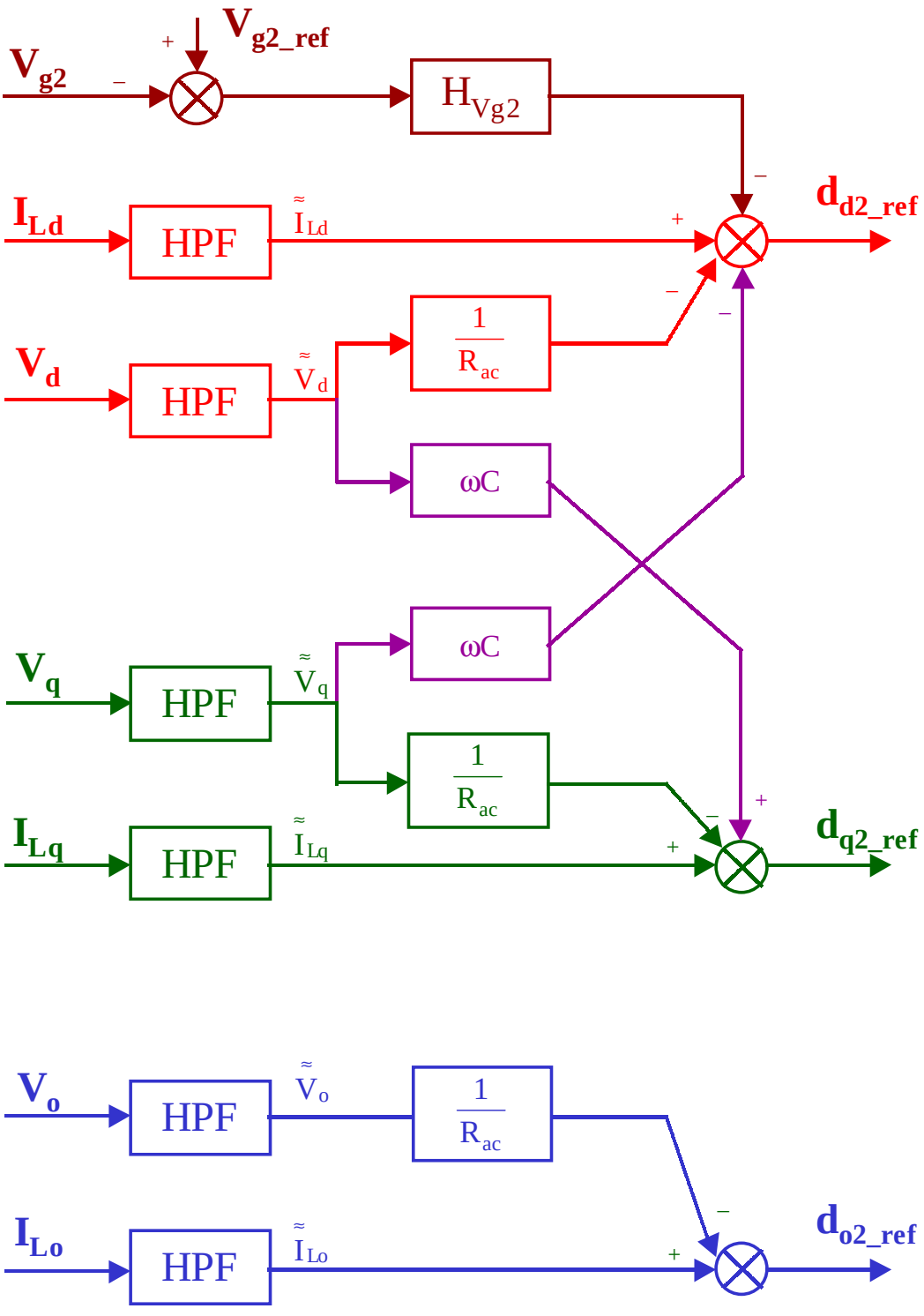


Figure 5-23 Load conditioner current reference

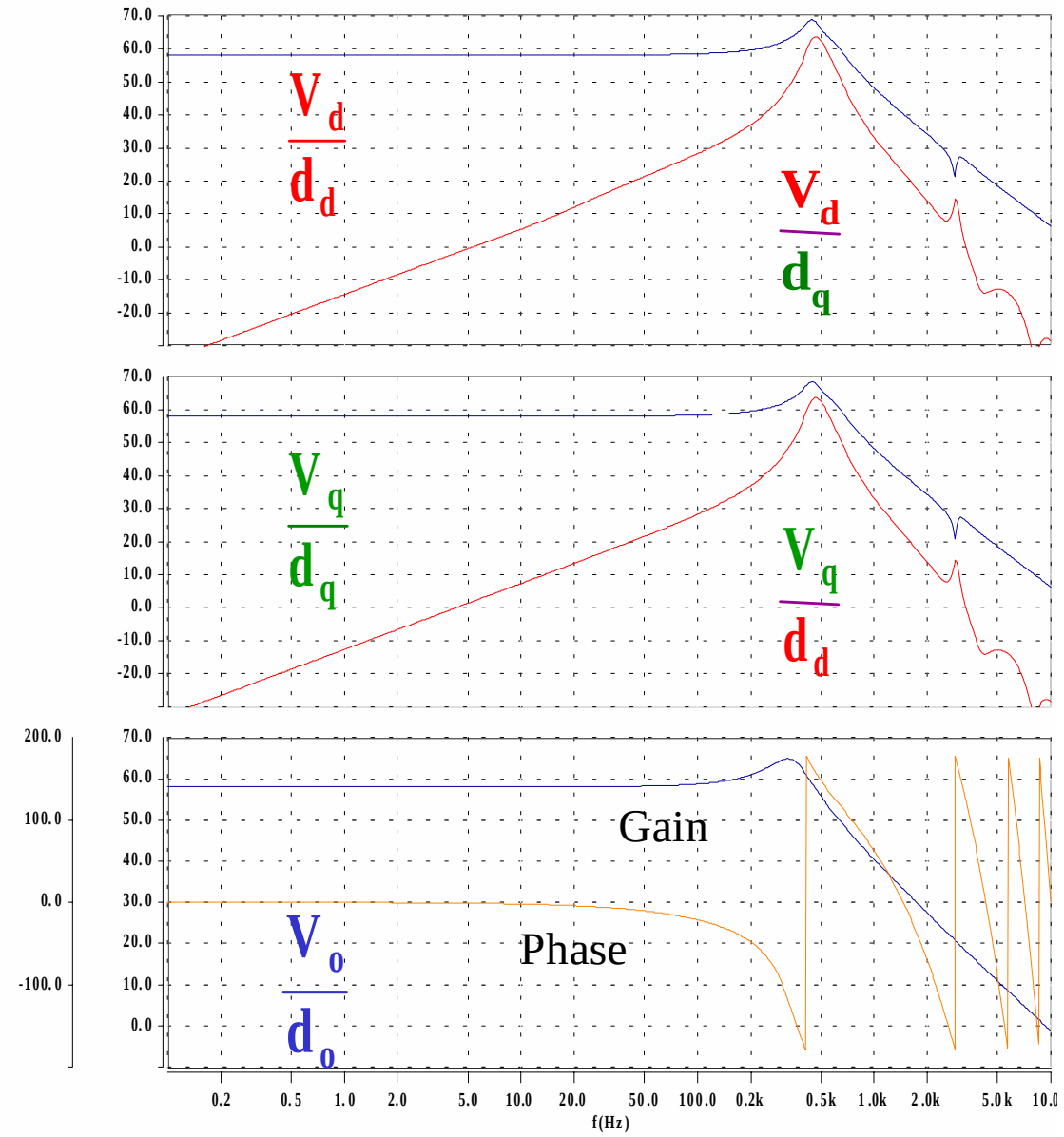


Figure 5-24 Main inverter control-to-output voltage transfer functions with the load conditioner performing active filtering function

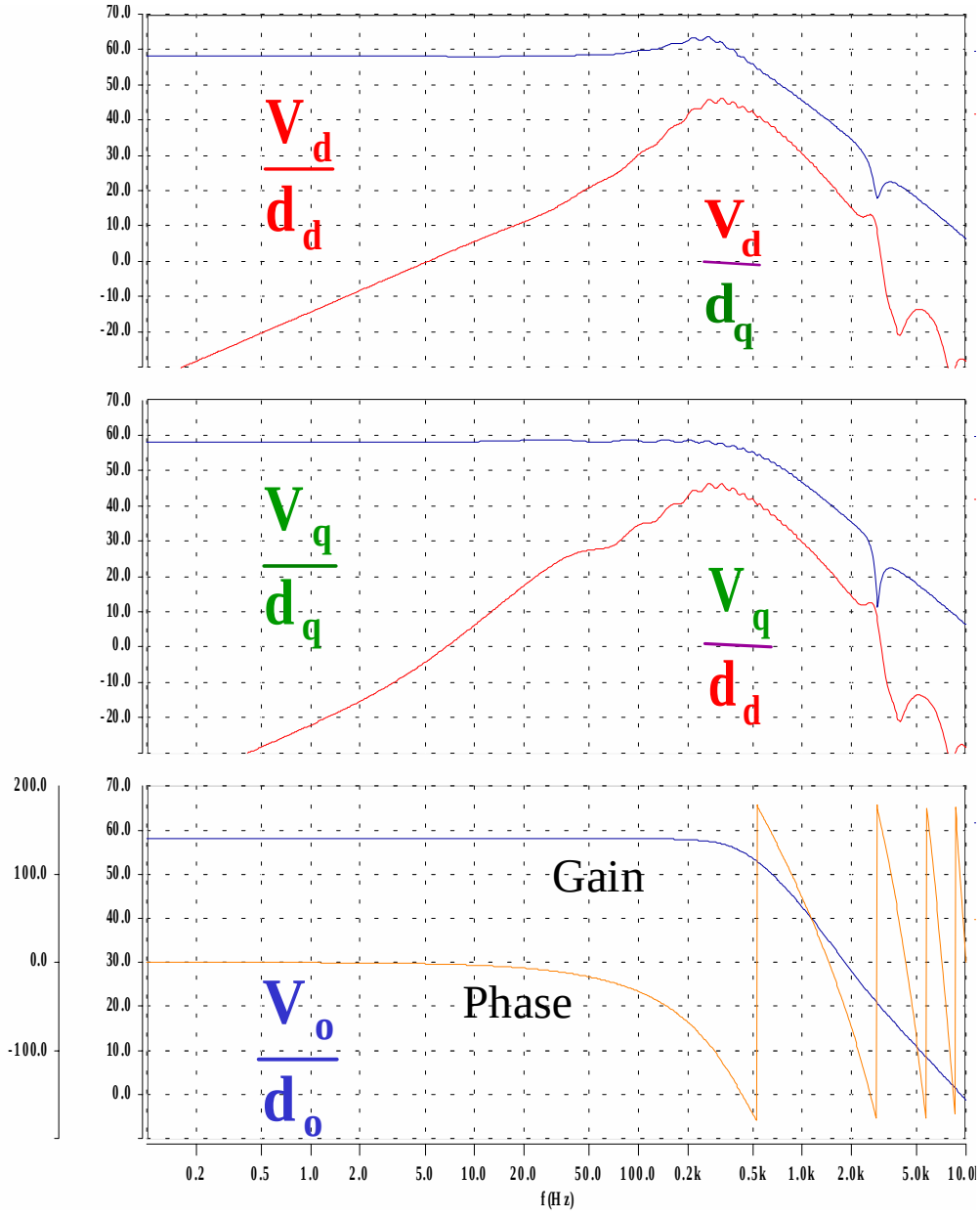


Figure 5-25 Main inverter control-to-output voltage transfer functions with the load conditioner performing active filtering and active damping functions

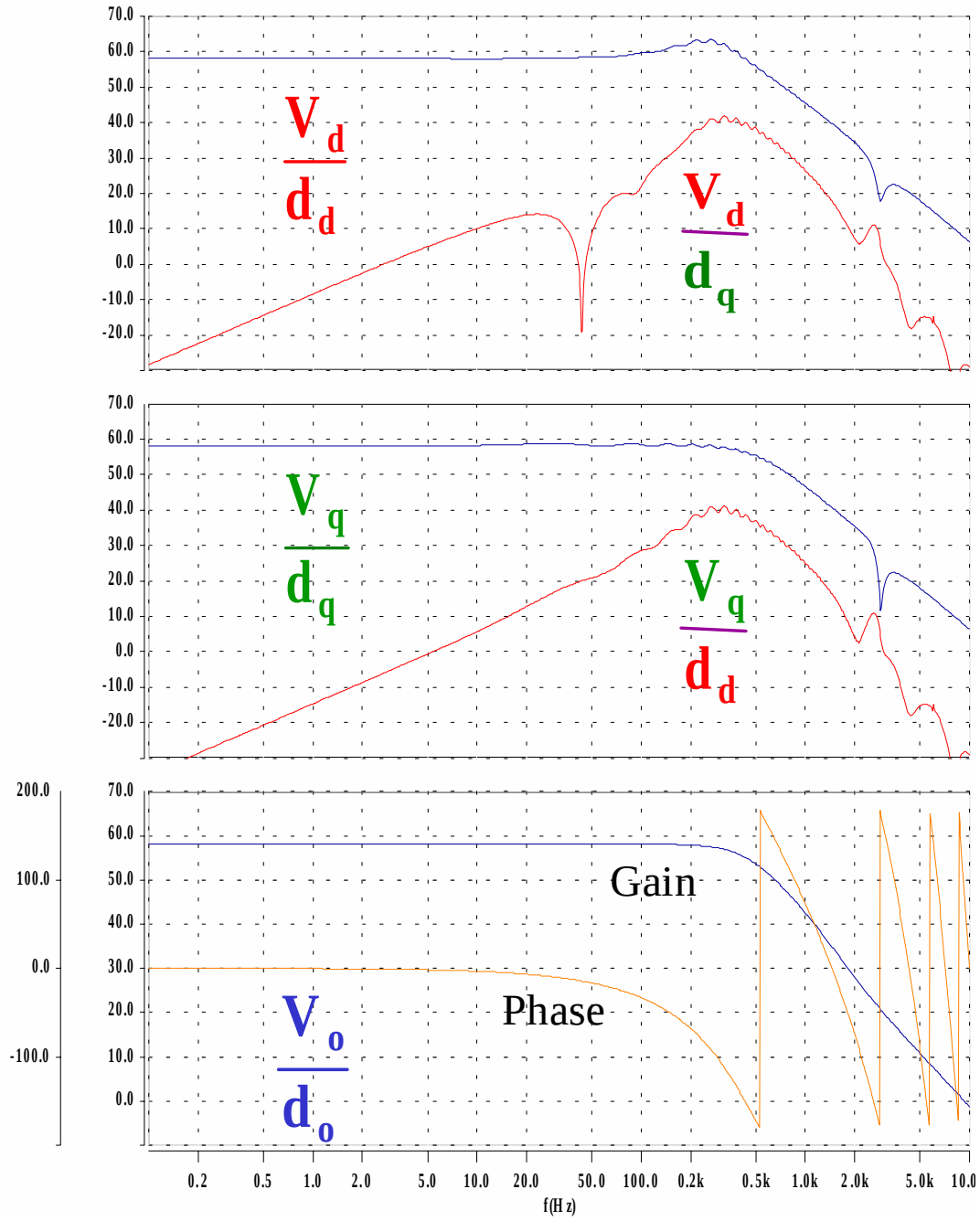
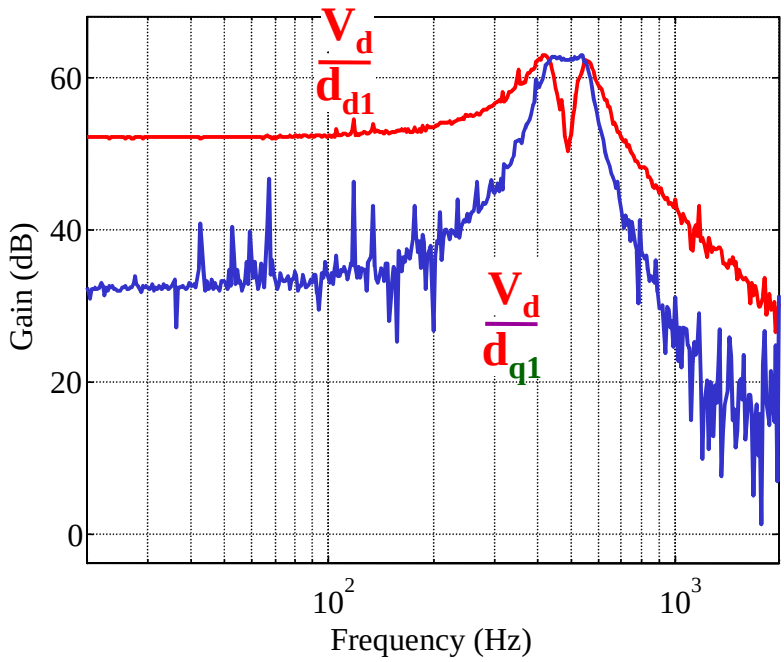


Figure 5-26 Main inverter control-to-output voltage transfer functions with the load conditioner performing active filtering, active damping and active decoupling functions

(a)



(b)

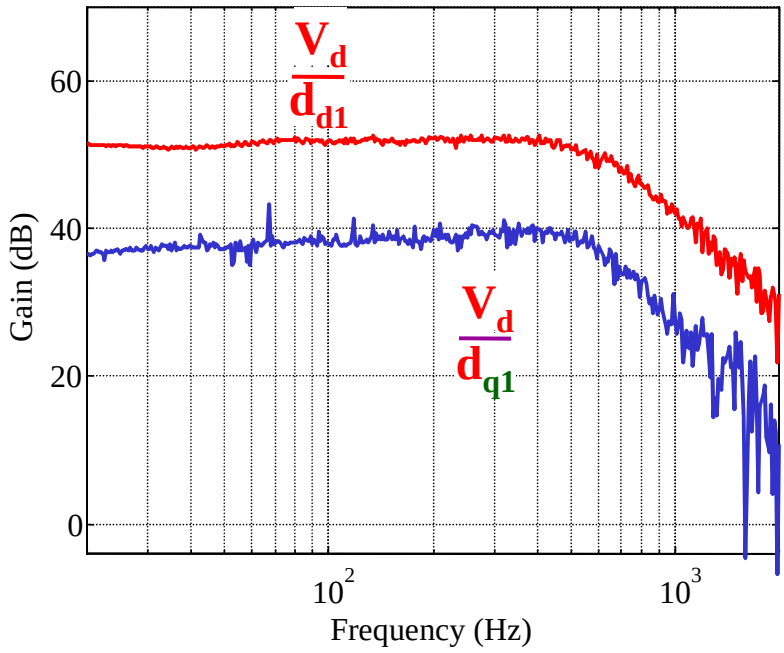


Figure 5-27 Measured main inverter control-to-output voltage transfer functions under no load

(a) without load conditioner; (b) with load conditioner

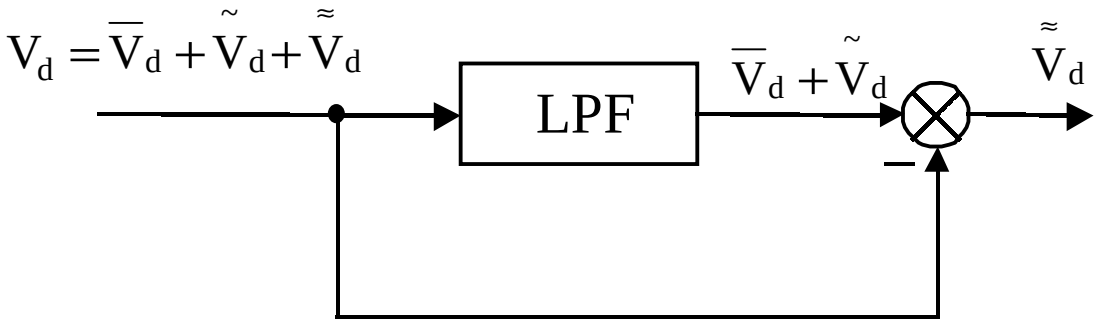


Figure 5-28 A high-pass filter implemented by using low-pass filter

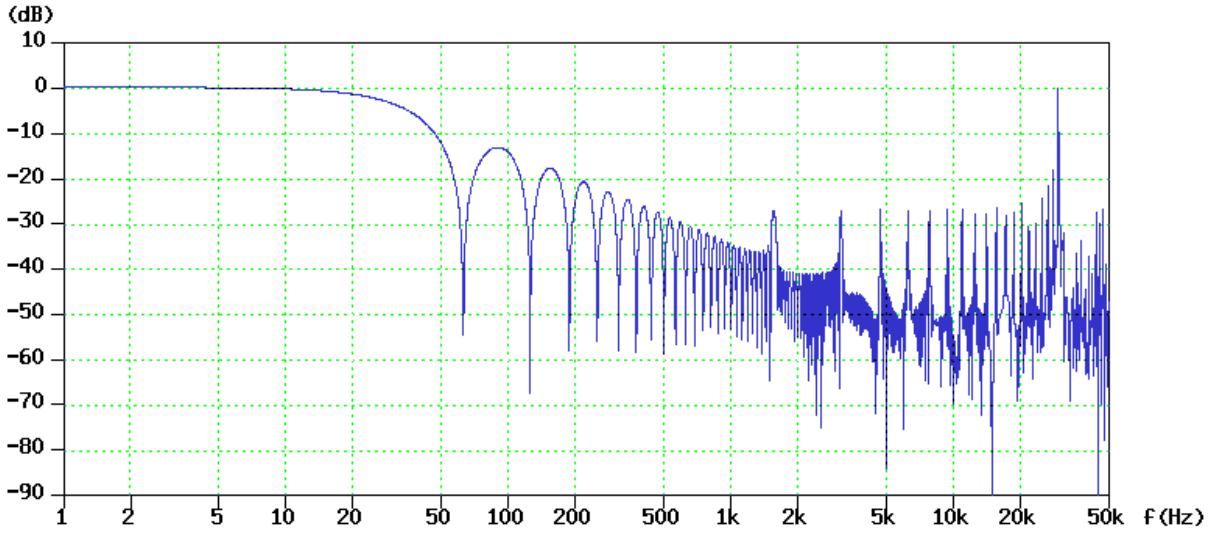


Figure 5-29 Transfer function of a moving average operand with a window frequency of 60 Hz

The algorithm of moving average operand to extract the DC component for Vd is shown in Figure 5-30 and expressed in (5.17).

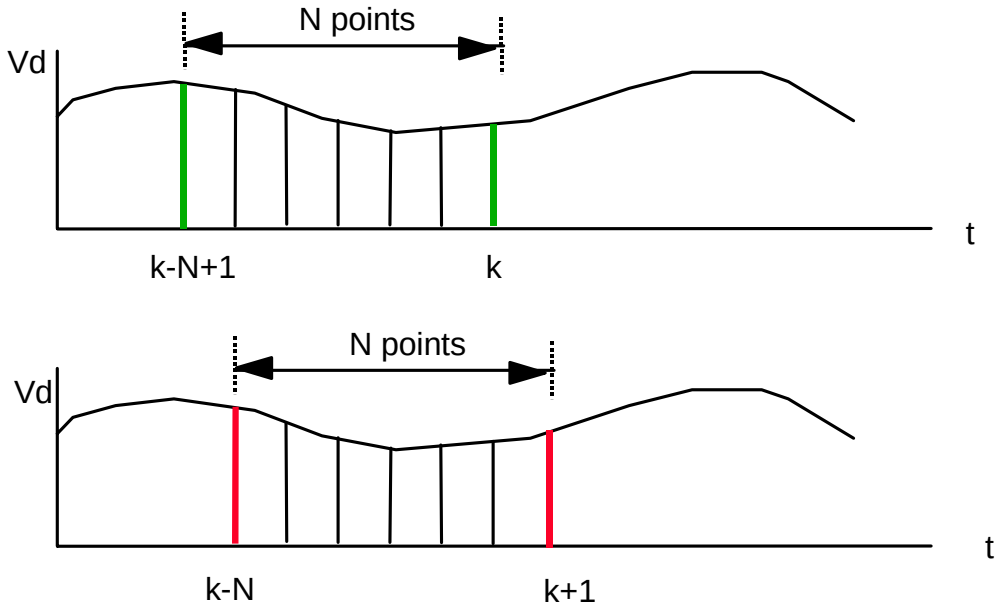


Figure 5-30 Moving average operand for dc component extraction

$$\overline{V}_{d(k)} = \frac{1}{N}\sum_{r=0}^{N-1} V_{d(k-r)}$$

$$\overline{V}_{d(k+1)} = \overline{V}_{d(k)} + \frac{1}{N}(V_{d(k)} - V_{d(k-N+1)}) \qquad \textbf{(5.17)}$$

where N is the number of sampling points within one line cycle.

Since the moving average operator can only extract the DC component, the low order harmonic components, e.g. 5^{th} harmonic, needs to be converted into a DC component in order to be extracted. This can be done by using a rotating coordinate transformation shown in (4.11), except that the rotating speed ω should be replaced by 5ω. The DC component in the rotating coordinate at 5ω frequency is the magnitude of the

5^{th} harmonic component. Using the reverse coordinate transformation shown in (4.13) and replacing the ω with 5ω, the 5^{th} harmonic components can be precisely detected. All the other low-order harmonic components due to unbalanced and/or nonlinear load can be extracted using the same approach.

5.6.3 Control Design of the Main Inverter with the Load Conditioner

After the load conditioner current loops are closed, the main inverter control-to-output voltage transfer functions are simulated at full power level with unterminated load. The simulation results, as shown in Figure 5-26, demonstrate the effectiveness of the active damping and active decoupling functions performed by the load conditioner. The main inverter loop gain transfer functions with PI compensators, shown in Figure 5-31, indicates that the main inverter voltage loop can be closed higher than 300 Hz with more than 40 degree phase margins.

The control loops parameters for the power converter system are summarized in the following tables.

Table 5-1 Load Conditioner Control Parameters

	d	q	o	DC Link
K_p	9.28e-3	9.28e-3	30e-3	0.562
K_i	—	—	—	35.2
Cross-over Frequency	3 kHz	3 kHz	3 kHz	30 Hz
Phase Margin (degree)	35	35	35	50

Table 5-2 Main Inverter Control Parameters

	d	q	o
K_p	1.0e-3	1.26e-3	1.4e-3
K_i	0.6283	2.374	0.887
Cross-over Frequency	372 Hz	430 Hz	372 Hz
Phase Margin (degree)	55	43	55

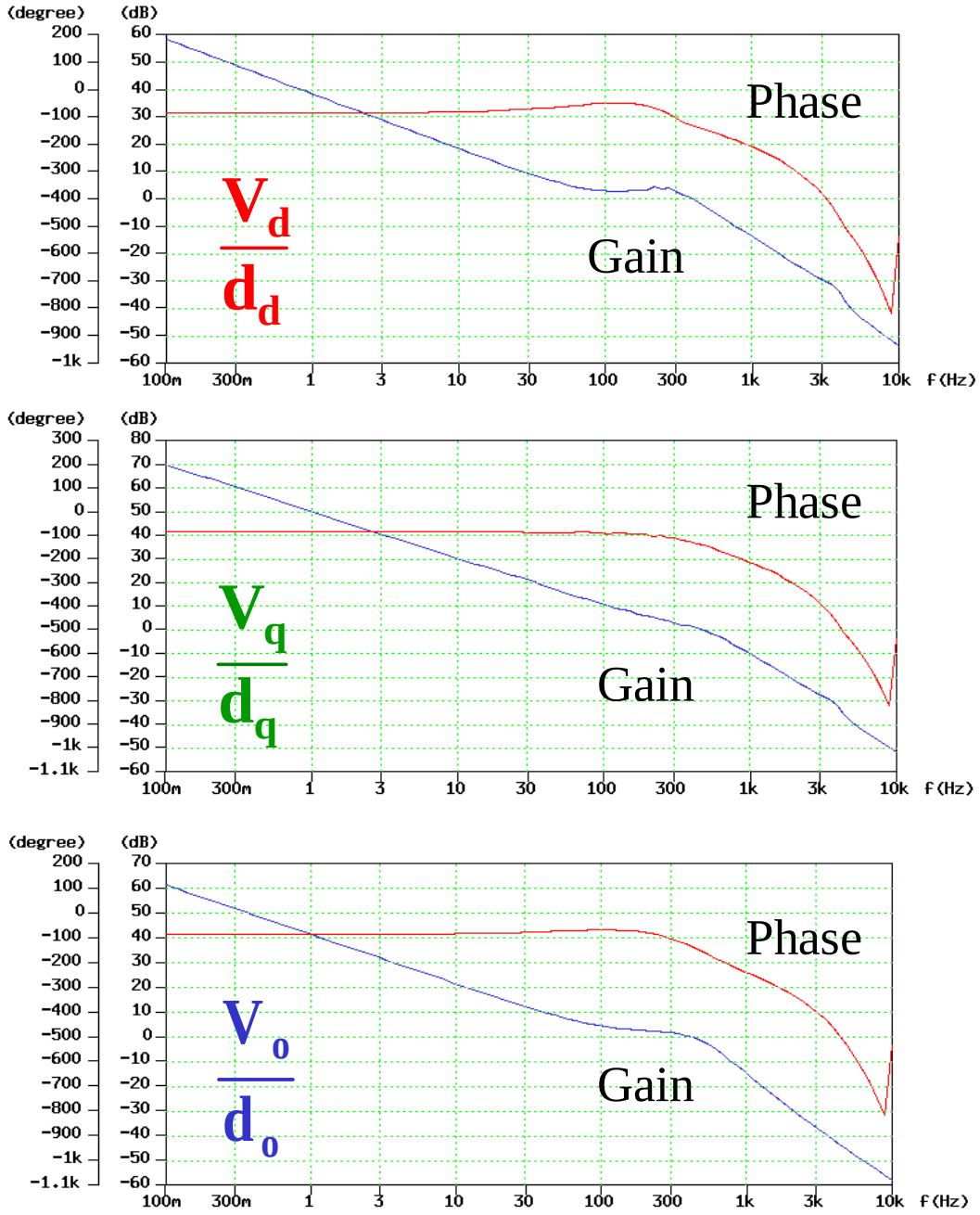


Figure 5-31 Main inverter voltage loop gain transfer functions with PI compensators with load conditioner control loops closed

5.7 Simulation and Experimental Results

5.7.1 Picture of the Prototype System

The prototype system is shown in Figure 5-32. The inverters include the 150 kVA main inverter and the 30 kVA load conditioner. They are mounted back-to-back, and connected through a laminated DC bus bar. An engine generator set, running at a variable speed, provides the power source. The control box includes the OEM SHARC board, the EPLD board which has two ALTERA FLEX 8000 family chips, and the A/D board which has 16 high speed A/D channels and 4 high speed D/A channels, as described in Chapter 4.

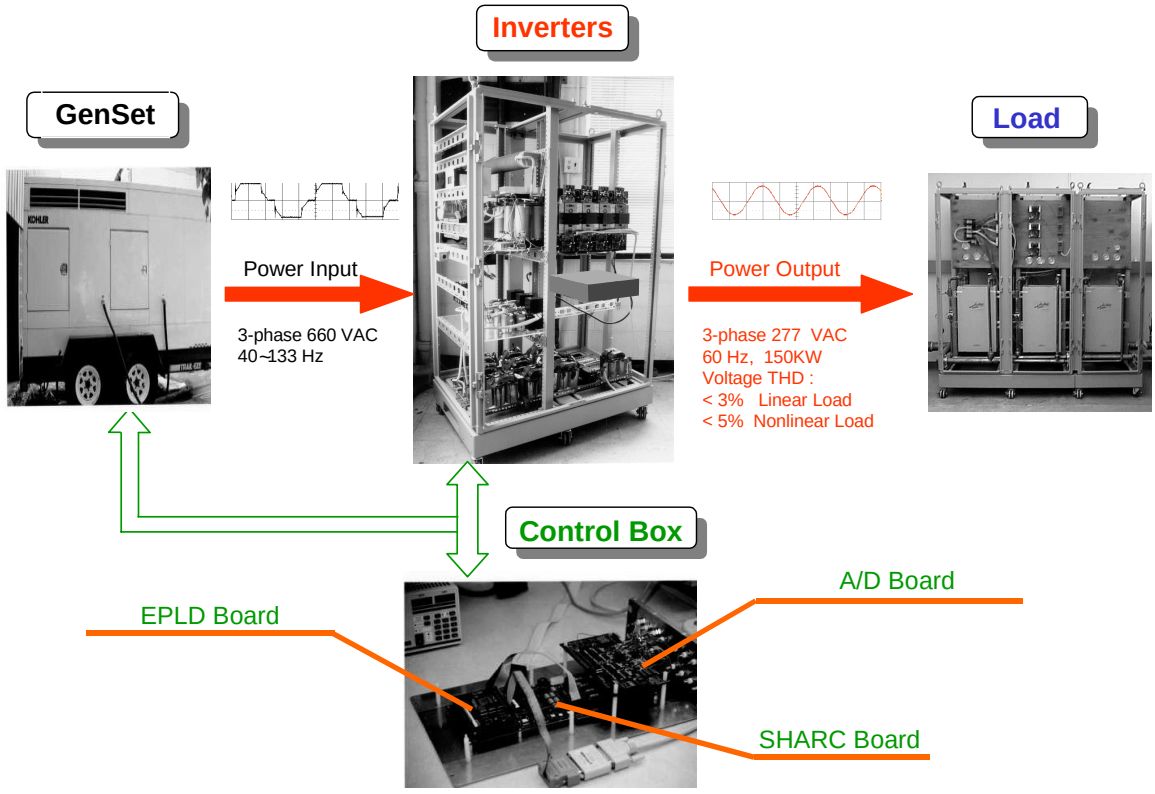


Figure 5-32 Picture of the prototype system

5.7.2 Verification of Active Damping Function

The active damping function of the load conditioner is verified by the time domain experimental results at a 57 Ohm light load condition. The main inverter voltage loop control parameters are scaled to have the cross-over frequencies given in Table 5-2 at 200 V DC link voltage. Figure 5-33 shows the output voltage waveforms without the load conditioner at different DC link voltages. By increasing the DC link voltage, the control-to-output voltage transfer function gain increases, and the actual cross-over frequency increases. It can be seen that the output voltage at a 80 V DC link voltage is stable. It has a superimposed oscillation at the resonant frequency when the DC link voltage increases up to 130 V. The output voltage is unstable when the DC link voltage increases up to 170 V. It indicates that without the load conditioner, the main inverter voltage loop bandwidth can not be pushed to 300 Hz.

Figure 5-34 shows that a stable output voltage can be achieved with a voltage loop bandwidth higher than 300 Hz. Therefore, the power converter system has much higher voltage loop bandwidth due to the damping function of the load conditioner. A much better dynamic performance can be expected with the power converter system.

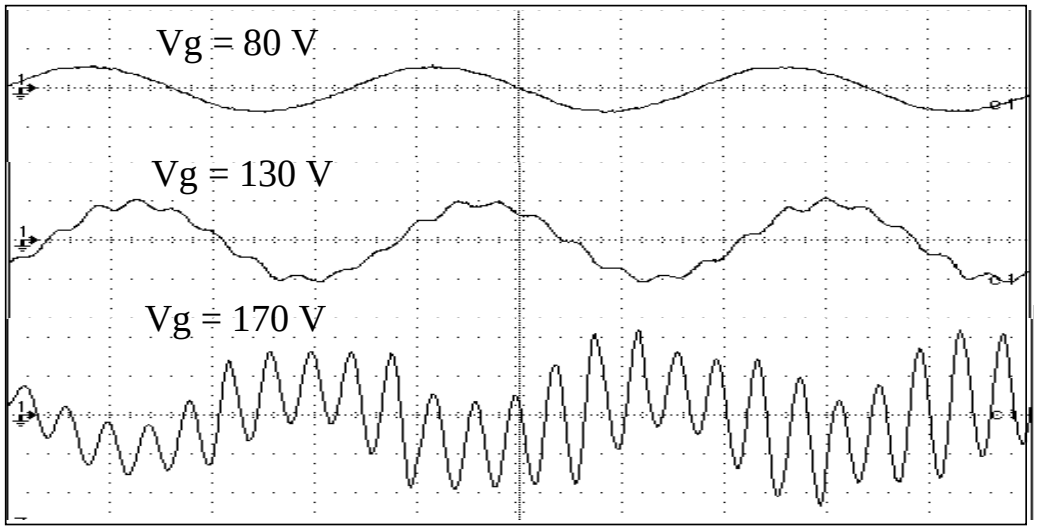


Figure 5-33 Unstable output voltage without the load conditioner (100 V/div)

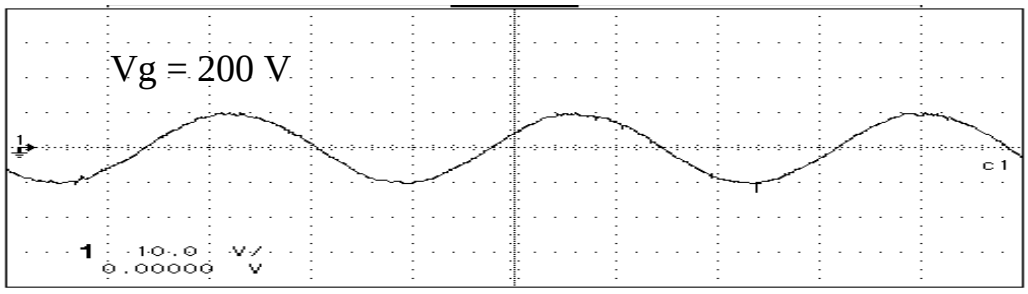


Figure 5-34 Stable output voltage with the load conditioner (100 V/div)

5.7.3 Simulation and Experimental Results with Nonlinear Load

The same nonlinear load configuration, as shown in Figure 4-17, is simulated and tested. The simulation waveforms for phase A are shown in Figure 5-35. The achieved output voltage distortion is 4.2% with a 16% load current THD. It can be seen that the main inverter inductor current is very close to sinusoidal, and the load conditioner outputs all the high-order harmonic currents.

Two nonlinear loads are tested at different power levels. In the first case, the output voltage, main inverter inductor current and the load conditioner current are shown in Figure 5-36 at a power level of 12 kW. Since the diode rectifier current occupies a large portion of the total load current, distinct current bumps can be seen in the total load current. A 2.6% output voltage THD can be achieved with 10.3% load current THD and a crest factor of 1.9. Compared with the test results shown in Chapter 4, there is a significant improvement. In the second case, the linear portion of the load is increased, thus the total output power level reaches 25 kW. Since the diode rectifier current occupies less of a portion of the total load current, there is no distinct waveform distortion in the total load current. However, the contribution of the harmonic load current can be clearly seen from the diode rectifier current. A 5% voltage THD is achieved in this case.

The simulation and experimental results show that the power converter system can provide much better performance for nonlinear loads, compared with one inverter solution.

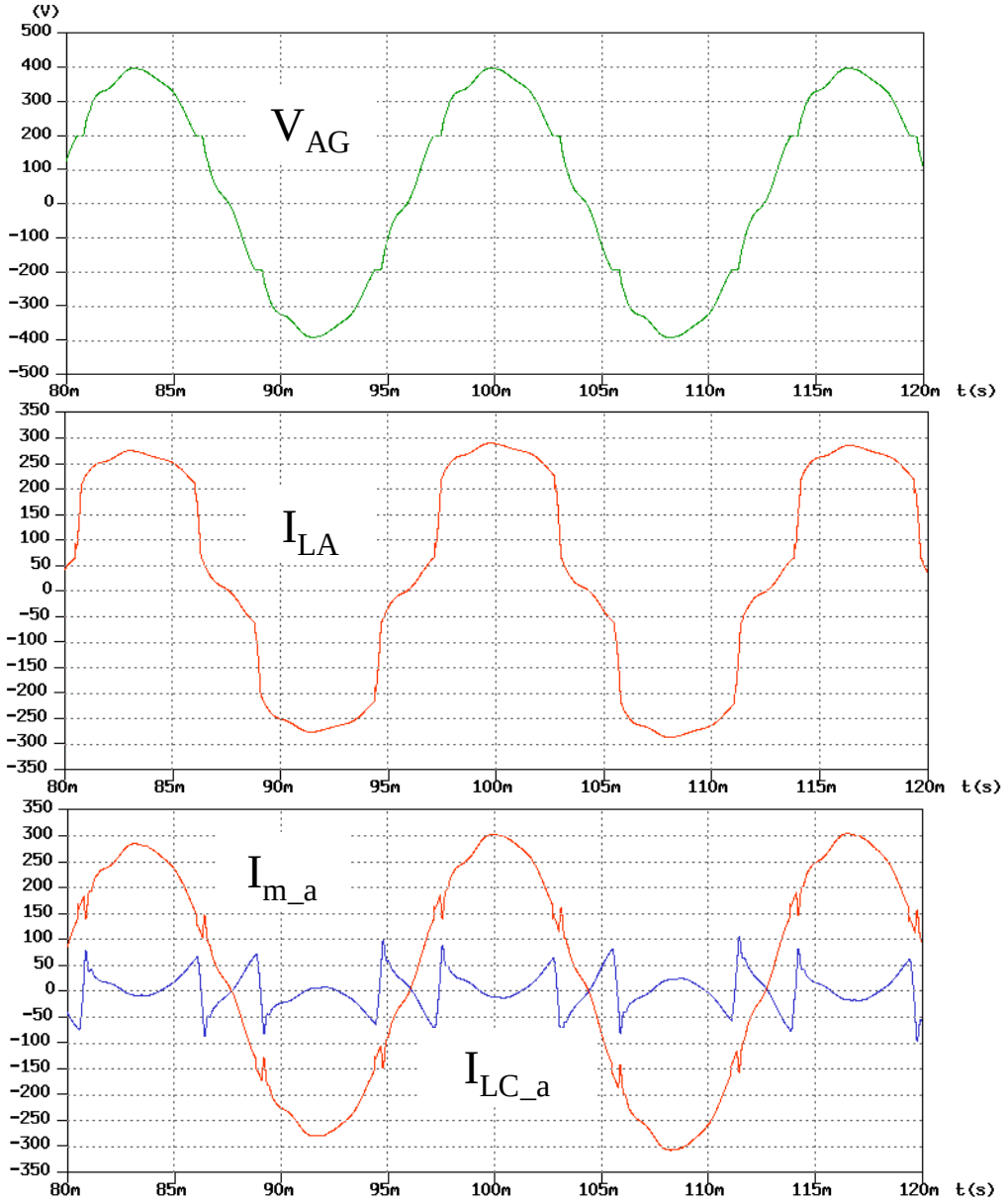


Figure 5-35 Simulation results for a nonlinear load at 150 kW

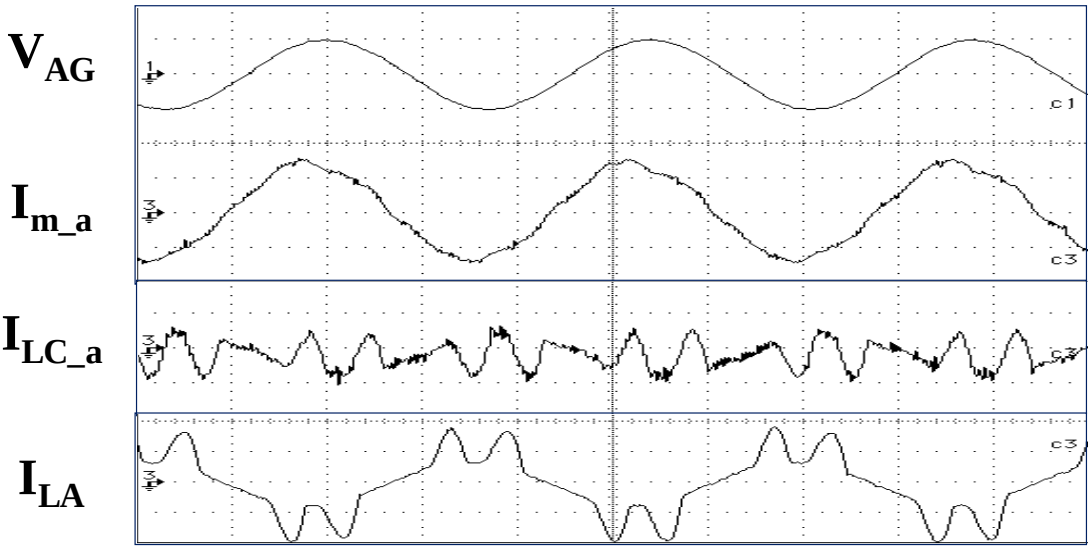


Figure 5-36 Experimental results for a nonlinear load at 12 kW

(a) output voltage (100 V/div) ; (b) main inverter inductor current (10 A/div) ; (c) load conditioner inductor current (10 A/div); (d) load current (10 A/div)

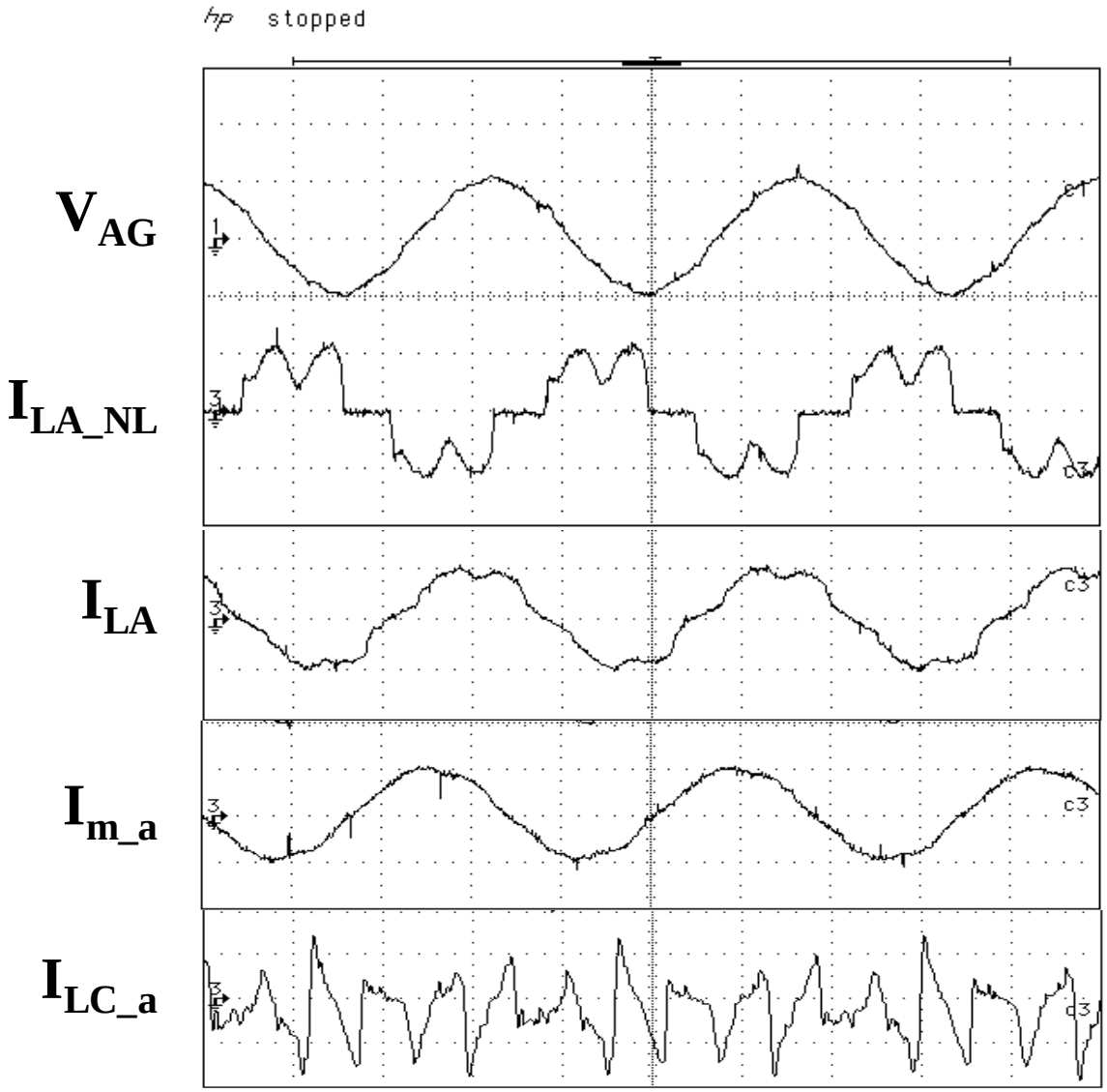


Figure 5-37 Experimental results for a nonlinear load at 25 kW

(a) output voltage (100 V/div) ; (b) diode bridge rectifier current (20 A/div); (c) load current (50 A/div); (d) main inverter inductor current (50 A/div) ; (e) load conditioner inductor current (5 A/div)

5.7.4 Simulation Results with Unbalanced Load

An unbalanced three-phase load is simulated and shown in Figure 5-38, with phases A and B loaded with 50 kW resistive load, while connecting only a 150 Watt resistive load on phase C. Since the load conditioner should not provide any low frequency currents, including negative-sequence and zero-sequence currents, almost all the currents are provided by the main inverter.

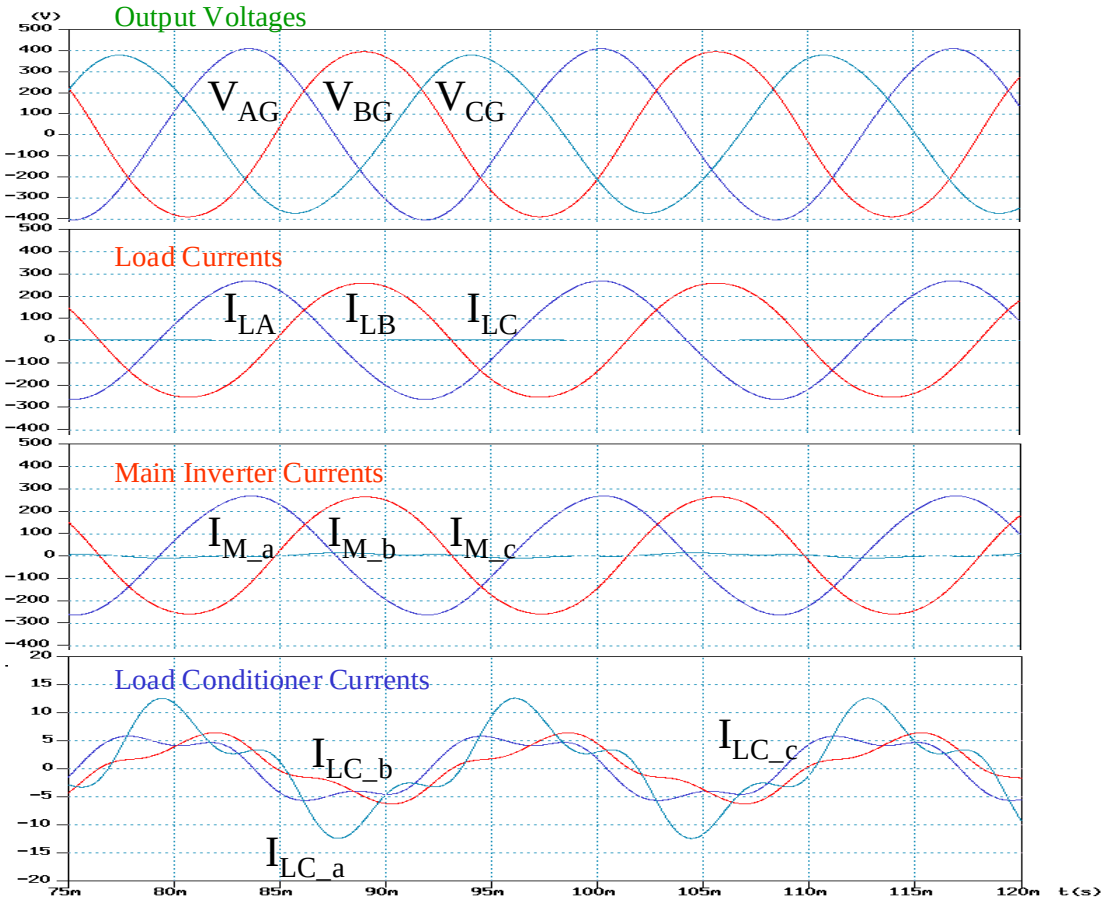


Figure 5-38 Simulation results of the power converter system with an unbalanced load

(a) output voltages; (b) load currents; (c) main inverter inductor currents; (d) load conditioner inductor currents

5.8 Conclusions

The proposed new converter system is very suitable for high power applications to achieve high performance. The load conditioner plays multiple functions to help the main converter deal with nonlinear loads and extend the main converter control loop bandwidth. A 150 kW three-phase utility power supply using the proposed converter system demonstrated the benefits of using the load conditioner. The resulting system has the advantages of low cost and high control bandwidth, and thus high performance. The simulation and experimental results verify that the system is stable under light load, and that the system has very good performance with a highly nonlinear load and unbalanced load. The proposed system architecture can be extended to other high power DC/DC converters, inverters, PFC and UPS applications.

Chapter 6 Nonlinear Loading Effects in a DC Distribution Power System

6.1 Introduction

Power electronics has evolved to a point where a large-scale power electronics system is a reality. A large-scale DC distribution power system on a ship is shown in Figure 6-1. In this system, all the sources and the loads are power converters connected to a common DC distribution bus. In the front end, the engine/generator sets provide the energy sources. Two three-phase PFC PWM rectifiers convert AC voltages into the 800 V DC voltage. Different load converters are connected to the DC distribution bus to fulfill requirements of different loads, such as AC drives, multi-phase DC motor drives and secondary utility bus generation.

Such a large-scale DC distribution power system calls for a stable and a tightly regulated DC distribution bus. In order to achieve this, the stability needs to be checked not only in a small-signal sense, but also in a large-signal sense. The small-signal stability analysis can be performed based on the interface interaction criteria, as discussed in [H4]. The discussion of a large-signal stability is the focus of this chapter.

In this chapter, a simplified DC distribution power system, including the utility subsystem and the three-phase PFC PWM rectifier, is used to elaborate the nonlinear loading effect caused by the utility subsystem with unbalanced and/or nonlinear loads. The nonlinear loading effect has a great impact on the large-signal stability of the DC distribution bus.

Two solutions are proposed to eliminate the nonlinear loading effect, thus improving the large-signal stability of the DC distribution bus. One solution is to confine

the nonlinear loading effect within the subsystem. The second solution is to use a bus conditioner to stabilize the primary DC bus.

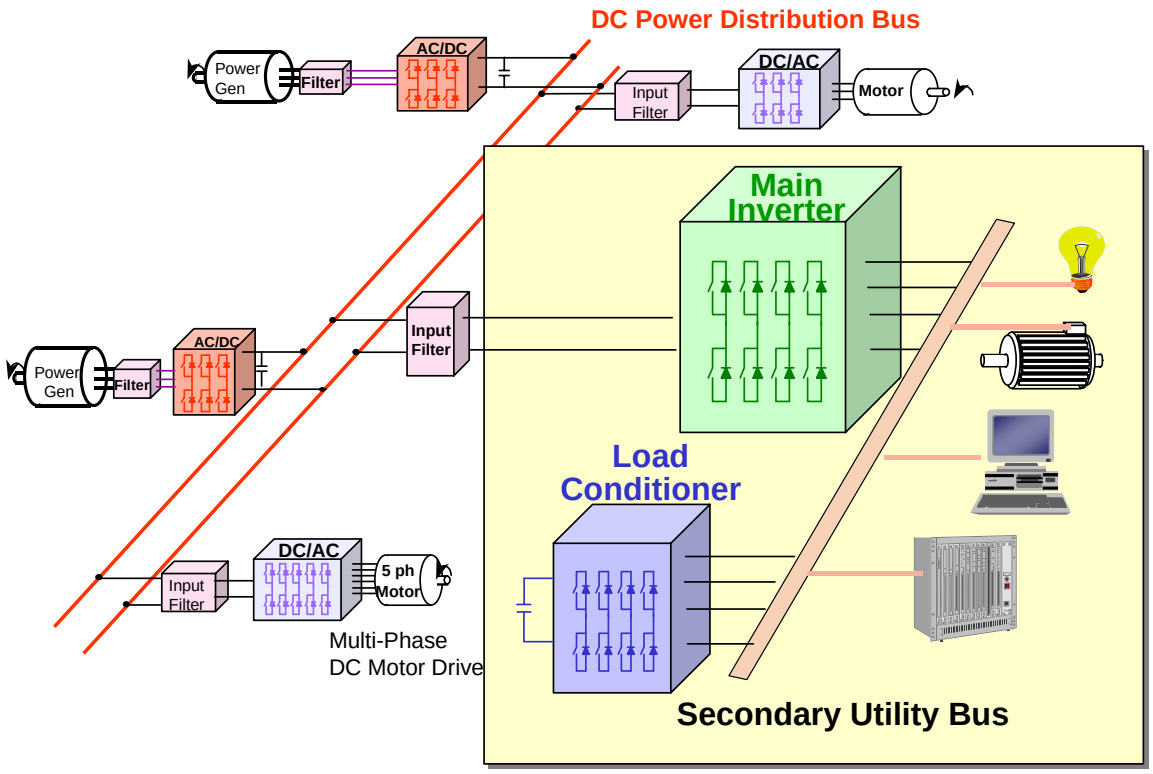


Figure 6-1 Utility sub-system in a DC distribution power system

6.2 Nonlinear Loading Effects

6.2.1 Utility Subsystem

Utility subsystem is a load converter connected to the DC primary distribution bus. It consists of a main inverter and a multi-functional load conditioner, as described in Chapter 5. The aim of the utility subsystem is to provide the three-phase four-wire secondary AC bus to unbalanced and/or nonlinear loads with a low voltage distortion.

In Chapter 5, under the assumption of an ideal DC voltage source V_g, it is shown that the utility subsystem has a high performance at the secondary AC bus for its loads. The input impedance of the power converter system and the current it draws from the ideal DC voltage source is not of a major interest. However, when the utility subsystem is connected to the DC primary bus regulated by a front-end PWM rectifier, the utility subsystem may adversely affect the regulation of the DC primary bus in twofold. First, the input impedance of the utility subsystem and the output impedance of the front-end PFC rectifier may affect the small-signal stability of the primary DC bus, causing system interaction and DC bus voltage oscillation or unstable DC bus. Second, the current drawn by the utility subsystem may present a large-signal disturbance to the primary DC bus, causing stability issue in a large-signal sense. Those are two system level stability issues. The small-signal sense DC bus stability has been discussed in [H4]. In this chapter, the large-signal stability issue is discussed.

Only the power delivered from the main inverter is reflected to the primary DC bus. The circulating energy from the load conditioner is reflected to the load conditioner DC link capacitor, thus, it is invisible to the primary DC bus. According to power balance principle, the power that the utility subsystem draws from the primary DC bus is expressed as

$$\begin{aligned} P_{bus} &= V_{bus} I_{bus} \\ P_{bus} &= V_{AG}(I_{LA} - I_{LC\_a}) + V_{BG}(I_{LB} - I_{LC\_b}) + V_{CG}(I_{LC} - I_{LC\_c}) \end{aligned} \qquad \textbf{(6.1)}$$

where I_{LA}, I_{LB} and I_{LC} are load currents; I_{LC_a}, I_{LC_b} and I_{LC_c} are load conditioner currents; V_{bus} is the primary DC bus voltage, which is the same as V_g in Chapter 5; and I_{bus} is the current drawn from the primary DC bus, which is the same as I_p in Chapter 5.

With the proposed power converter system configuration, an ideal three-phase output voltage is always achieved. With a balanced nonlinear load to the utility subsystem, such as a three-phase diode bridge rectifier or identically loaded three single-phase diode bridge rectifier, the load current has abundant 3^{rd}, 5^{th}, 7^{th}, odd harmonic currents. Since the load conditioner is designed to handle high-order ($>7^{th}$) harmonic load currents, high order harmonic load currents are provided by the load conditioner DC link, and thus, are invisible to the primary DC bus. However, the low-order harmonic currents are reflected to the primary DC bus. For a negative-sequence 5^{th} order harmonic load current caused by a three-phase diode bridge rectifier, it can be derived from (6.1) that a 6^{th} order harmonic ripple powers will be drawn from the primary DC bus. For the 3^{rd} order harmonic load current (zero-sequence) caused by identical three-single phase diode bridge rectifier, it can be derived from (6.1) that the power drawn from the primary DC bus is zero. Therefore, it does not affect the primary DC bus regulation. As a summary, for nonlinear loads to the utility subsystem, the utility subsystem will draw low-order ($\leq 6^{th}$) even harmonic ripple power from the primary DC bus.

With an unbalanced load to the utility subsystem, it is known from the discussion in Chapter 2 that there are positive-sequence, negative-sequence and zero-sequence load currents. Substituting them in (6.1), it can be seen that the positive-sequence load current draws a constant power from the primary DC bus; the negative-sequence load current draws a 2^{nd} harmonic ripple power from the primary DC bus; and the zero-sequence load current does not draw any power from the primary DC bus. Since we may have 100% negative-sequence unbalance, the utility subsystem draws very high 2^{nd} harmonic ripple power from the primary DC bus, which affects the primary DC bus regulation greatly.

6.2.2 Front-end PFC Bus Regulator

The primary DC bus is regulated by a front-end PFC PWM rectifier, as shown in Figure 6-2. Assuming the output of the engine/generator set is an ideal three-phase AC source, [H1] gives the average large-signal model, as shown in

Figure 6-3. The design of current compensators to control the input current follow the shape of the three-phase sinusoidal voltage at the output of the Generator, and the design of the superimposed voltage compensator to control the DC bus voltage have been given in [H1]. The power stage and control parameters of the three-phase PFC bus regulator are shown in Appendix B. The resulting current loop bandwidth is 1.5 kHz, and the DC bus voltage loop bandwidth is 500 Hz.

Normally a constant current source or a fixed resistor is used as the load when designing the bus regulator control loops. However, in a real DC distribution power system, the load to the front-end PWM rectifier is either a constant power load due to a closed loop controlled power converter, or a load which draws a large ripple power. The constant power loads present a challenge to the small signal stability of the primary DC bus due to its dynamic negative resistor characteristics. The loads drawing a large ripple power present a challenge to the large signal stability of the primary DC bus. The large-signal stability due to the loads drawing a large ripple power is a unique issue in the design of the PWM rectifier in a large-scale power electronics system. It is not evaluated in the design procedure of the PWM rectifier.

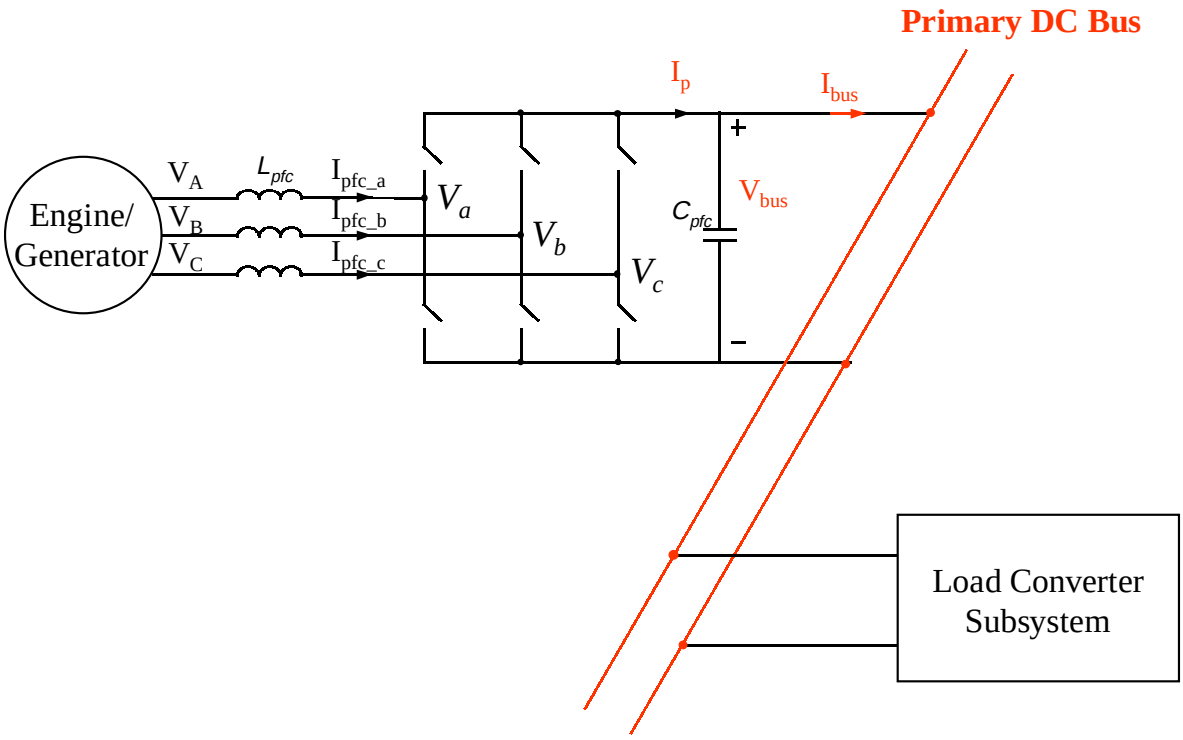


Figure 6-2 Front-end PWM rectifier in a DC distribution power system

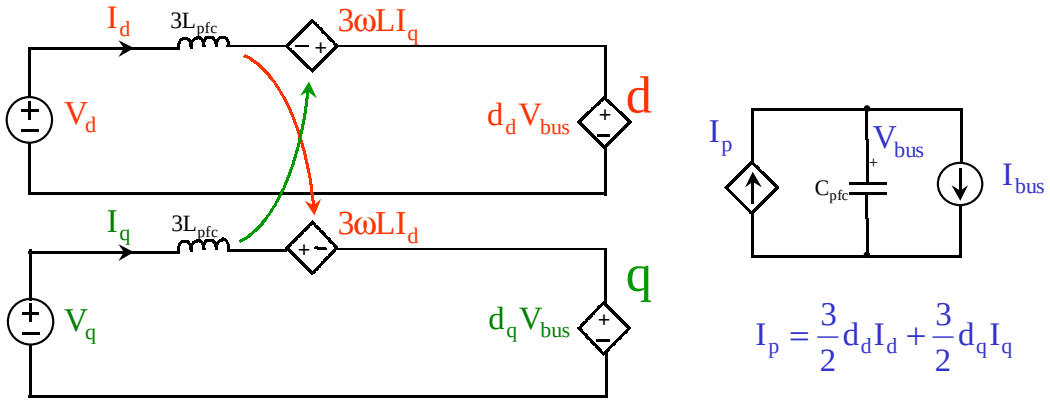


Figure 6-3 Average large-signal model of the front-end PWM rectifier

6.2.3 Definition of Nonlinear Loading Effects

Figure 6-4 shows the block diagram of a simplified DC distribution power system consisting of one source converter and one load converter system. The nonlinear loading effect to the primary DC distribution bus is described as: when the load to the load converter subsystem, e.g. utility subsystem, is unbalanced or nonlinear load, the load converter subsystem behaves like a nonlinear load to the primary DC bus by drawing a large ripple power. The nonlinear loading effect is a large-signal disturbance to the primary DC bus. Particularly for the utility subsystem, the ripple power drawn from the primary DC bus has 2^{nd}, 6^{th} harmonic or other even-order harmonic contents.

The nonlinear loading effect to the distribution bus is a result of an unbalanced and/or nonlinear load condition to the load converter subsystem. Depending on the percentage of unbalance, the peak-to-peak ripple current drawn from the DC distribution bus could be as large as 100% of the rated current. The original design of the controller for the three-phase PFC PWM rectifier based on a small signal model may become unstable under this large signal disturbance.

When there are several load converter subsystems drawing ripple currents at different frequencies and phase shifts, all those ripple currents modulate over the DC distribution bus. This may lead to an unstable DC bus or even cause damage to the load converters.

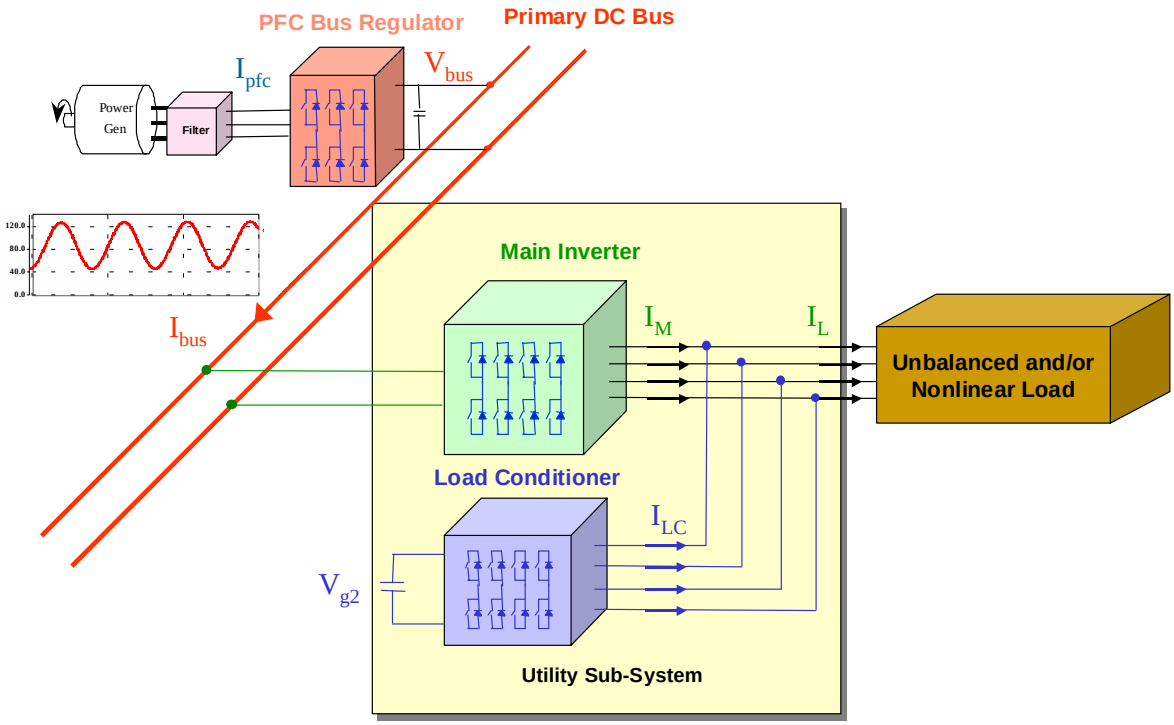


Figure 6-4 A simplified DC distribution power system

6.2.4 System Performance with Nonlinear Loading Effect

The nonlinear loading effect is evaluated with an unbalanced load to the utility sub-system. The unbalanced resistive load is given such that phase A and B output 33 kW each phase, and phase C has no load. The output voltages of the secondary AC bus and its load currents are shown in Figure 6-5.

Due to the nonlinear loading effect, there is a 80 A peak-to-peak ripple current drawn from the DC bus at the 2ω frequency, which causes the primary DC distribution bus voltage to oscillate at a magnitude of 40 V, as shown in Figure 6-6. This oscillating DC bus voltage also degrades the performance of the PFC bus regulator, causing a heavily distorted three-phase input current, as shown in Figure 6-7. Consequently, those harmonic currents could travel back to the generator causing additional problems, such as increased copper and iron losses and a ripple torque.

Since the load conditioner does not handle the 2ω and 6ω ripple currents, its output currents are very small, as shown in Figure 6-9. On the contrary, the main inverter output currents are unbalanced, as shown in Figure 6-8, indicating that the main inverter is handling the 2ω ripple current.

In summary, the nonlinear loading effect causes an oscillating or even unstable primary DC bus voltage, stability problem of other load converters on the same DC distribution bus, degraded performance of the PFC PWM bus regulator, and increased copper and iron losses and ripple torque in the engine/generator set.

To solve the nonlinear loading effect, the low frequency ripple currents have to be kept from entering the DC distribution bus and interfering with the PFC bus regulator. Two solutions are proposed to eliminate the problems caused by the nonlinear loading effect of the load converters, which are discussed in the following two sections.

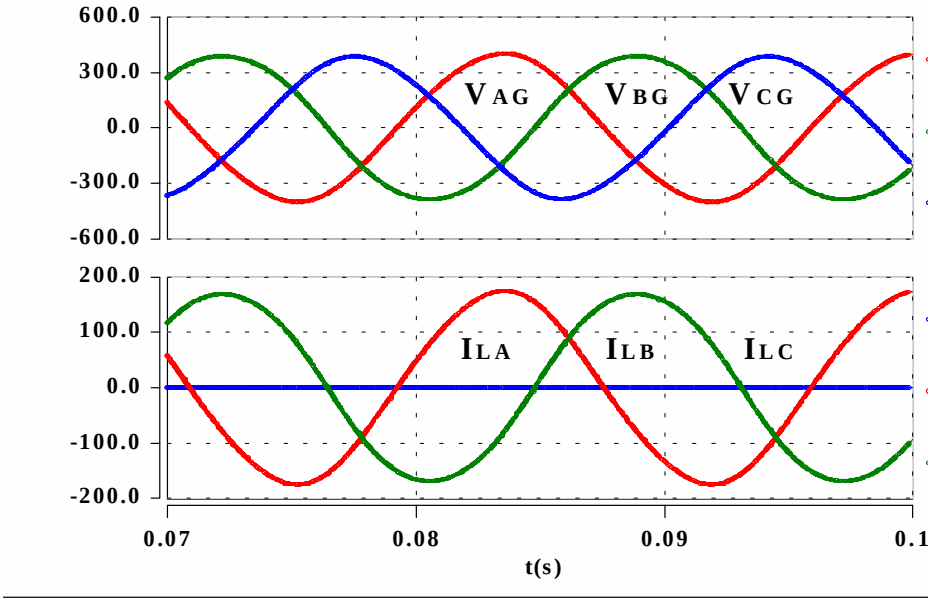


Figure 6-5 Utility sub-system output voltages and unbalanced load currents

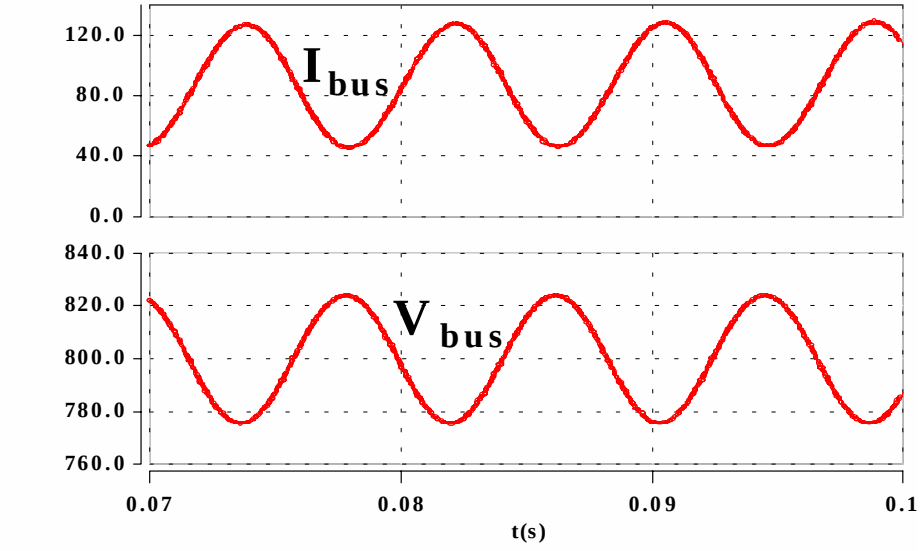


Figure 6-6 Nonlinear loading effect to the primary DC distribution bus

(a) ripple bus current; (b) oscillating primary DC bus volage

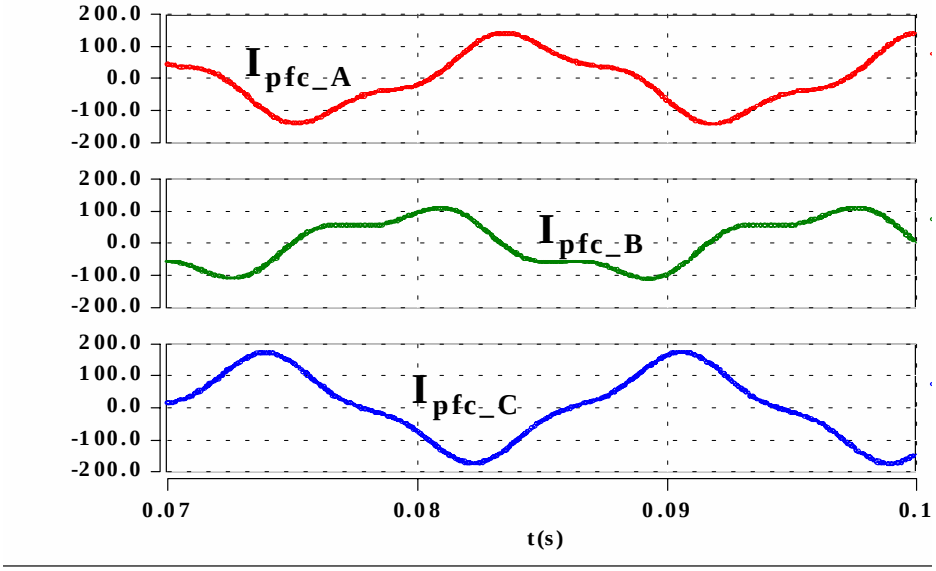


Figure 6-7 Three-phase PFC bus regulator input currents with nonlinear loading effect

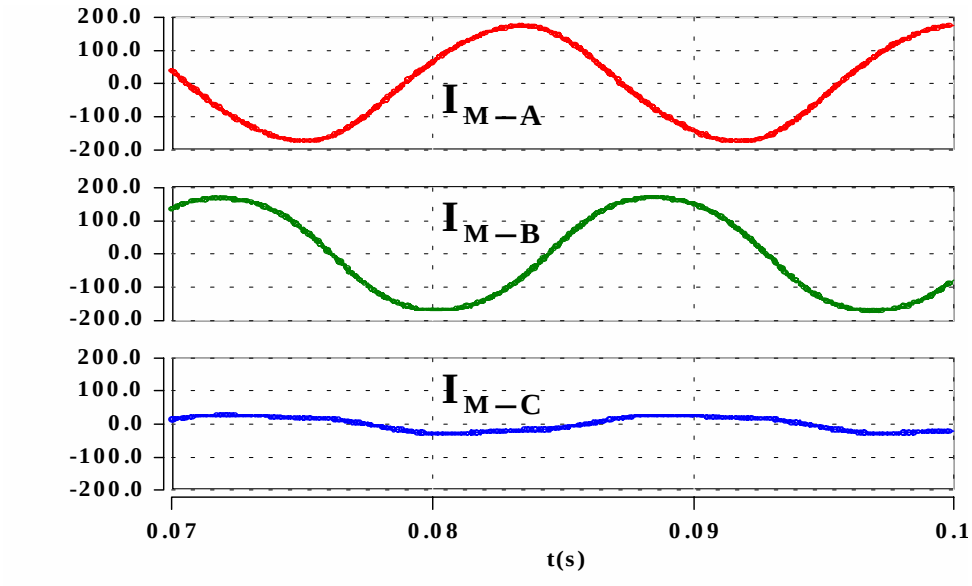


Figure 6-8 Main inverter output currents with nonlinear loading effect

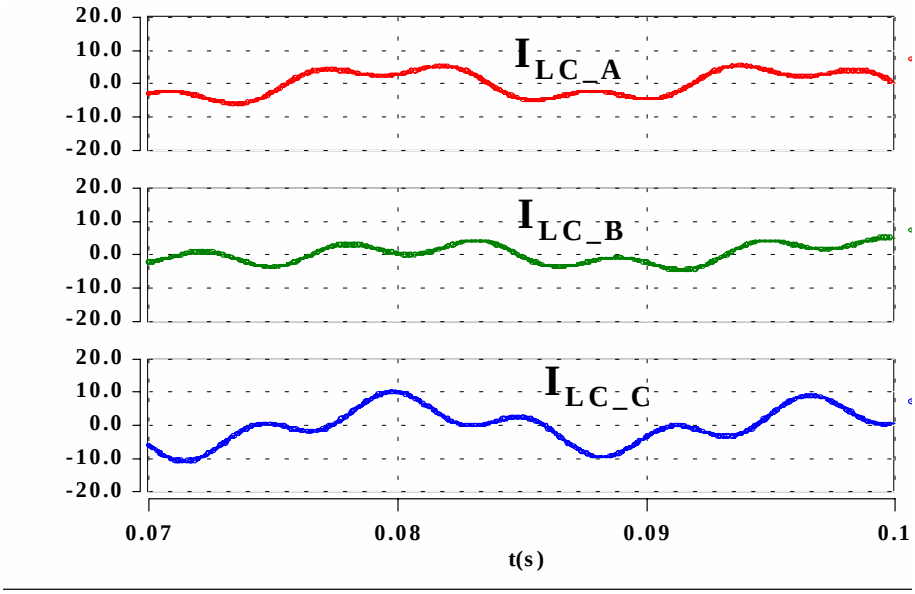


Figure 6-9 Load conditioner output currents with nonlinear loading effect

6.3 Elimination of Nonlinear Loading Effect Using Load Conditioner

Without changing the system configuration shown in Figure 6-4, the load conditioner can be designed to handle not only high frequency harmonic currents, but also low frequency ripple currents. This can be easily accomplished by modifying the load conditioner current references shown in (5.13) ~ (5.16) to the following,

$$
\begin{aligned}
I_{d2\_ref} &= I_{d2\_ref1} + I_{d2\_ref2} + I_{d2\_ref3} + I_{d2\_ref4} \\
I_{q2\_ref} &= I_{q2\_ref1} + I_{q2\_ref2} + I_{q2\_ref3} \\
I_{o2\_ref} &= I_{o2\_ref1} + I_{o2\_ref2}
\end{aligned}
\qquad \textbf{(6.2)}
$$

$$
\begin{aligned}
I_{d2\_ref1} &= \tilde{I}_{Ld} \\
I_{q2\_ref1} &= \tilde{I}_{Lq} \\
I_{o2\_ref1} &= \tilde{I}_{Lo}
\end{aligned}
\qquad \textbf{(6.3)}
$$

$$I_{d2\_ref2} = -\frac{\tilde{V}_d}{R_{ac}}$$

$$I_{q2\_ref2} = -\frac{\tilde{V}_q}{R_{ac}} \qquad \textbf{(6.4)}$$

$$I_{o2\_ref2} = -\frac{\tilde{V}_o}{R_{ac}}$$

$$I_{d2\_ref3} = -\omega C \tilde{V}_q$$

$$I_{q2\_ref3} = \omega C \tilde{V}_d \qquad \textbf{(6.5)}$$

where $\tilde{I}_{Ld}$, $\tilde{I}_{Lq}$ and $\tilde{I}_{Lo}$ are harmonic load currents, including low-order harmonics, e.g. 2nd, 6th; $\tilde{V}_d$, $\tilde{V}_q$ and $\tilde{V}_o$ are harmonic secondary AC bus output voltages, including low-order harmonics, e.g. 2nd, 6th. (6.3) gives the load conditioner current reference for the active filter function; (6.4) gives the load conditioner current reference for the active damping function; (6.5) gives the load conditioner current reference for the decoupling function. From the implementation point of view, the only difference is the cut-off frequency of the high-pass-filter (HPF) shown in Figure 5-19. (6.3) ~ (6.5) requires a low cut-off frequency so that all the harmonic contents, except for the DC component, can pass through the HPF.

By extracting the DC component from the sensed load current in d-q-o coordinate and using it as the current reference for the active filter function--expressed as I_{d_ref1} in (6.3), this 2nd and 6th order ripple power will be handled by the DC link of the load conditioner, instead of the primary DC distribution bus. The ripple power is confined within the sub-system itself and thus, is invisible to the DC distribution bus and other load converters.

When using this approach to eliminate the nonlinear loading effect, there are several impacts on the subsystem design. The power level of the load conditioner has to be increased to handle the large amount of low frequency ripple power. The inductors

have to be designed to withstand the large ripple current without saturation. The DC link capacitor of the load conditioner has to be designed to have small enough voltage ripple when the rated low frequency ripple current flows through it. Since there is no need to detect the low-order harmonic contents, the algorithm is simpler.

Figure 6-10 shows the block diagram using the load conditioner to eliminate the nonlinear loading effect. With an increased DC link capacitance to 10 mF and a modified current reference, the load conditioner handles the 2ω and other low order harmonic ripple power. The utility sub-system draws a DC current with this unbalanced load, and thus the DC distribution bus voltage is stabilized to 800 V again, as shown in Figure 6-11. Due to the elimination of the nonlinear loading effect, the three-phase PFC bus regulator has a normal three-phase sinusoidal input current again, as shown in Figure 6-12.

Since the load conditioner handles the 2ω ripple current, the main inverter output currents are balanced, as shown in Figure 6-13. However, the load conditioner output currents are unbalanced, as shown in Figure 6-14. It can be seen in Figure 6-15 that there is a large (80 A peak-to-peak) 2ω ripple current flowing through the DC link capacitor of the load conditioner. The nonlinear loading problem has been removed from the DC distribution bus and shifted to the load conditioner DC link.

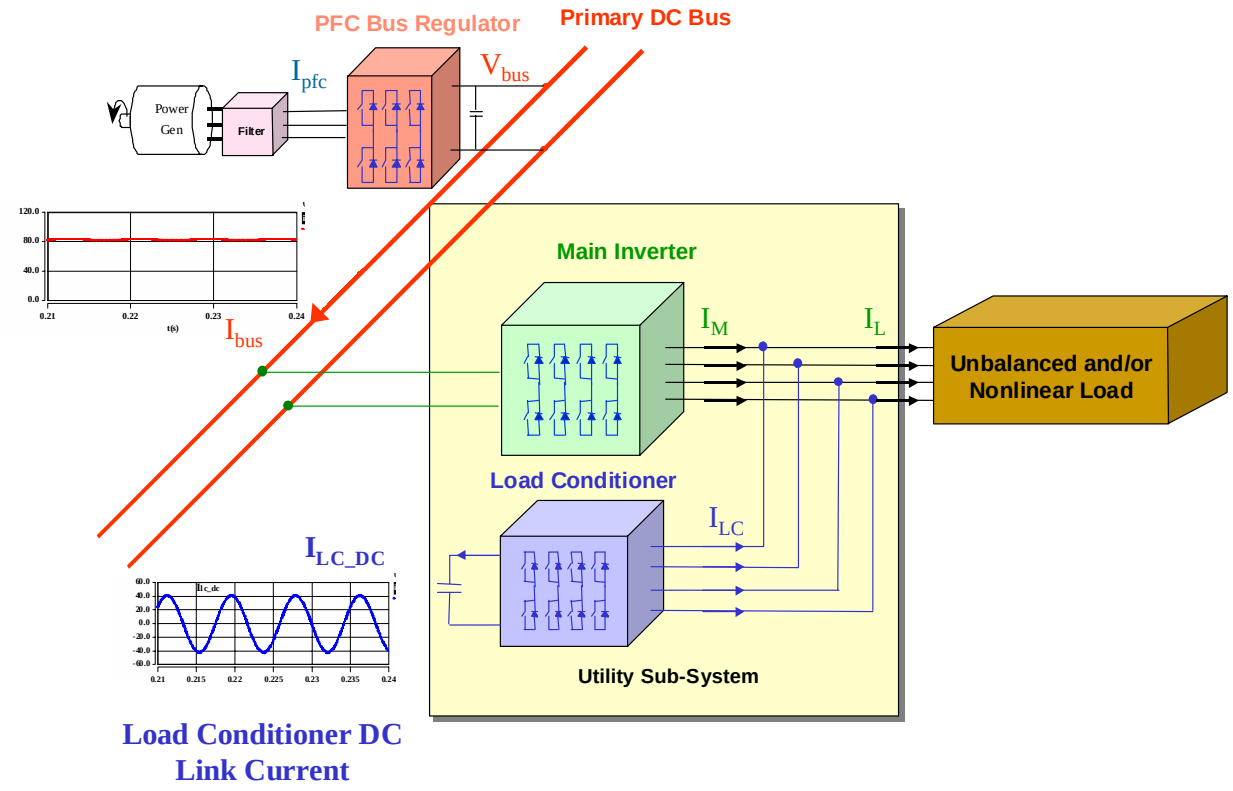


Figure 6-10 Load conditioner to eliminate nonlinear loading effect

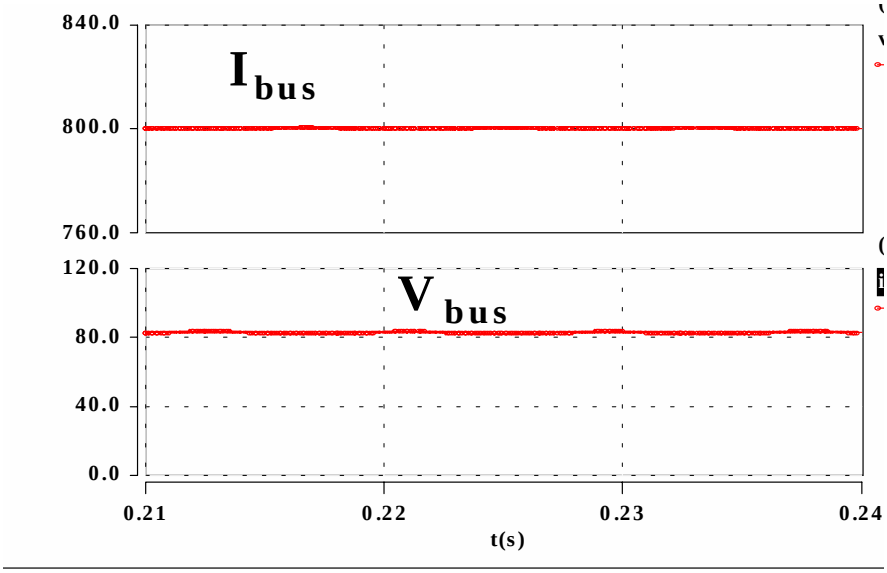


Figure 6-11 Using load conditioner to eliminate nonlinear loading effect

(a) bus output current; (b) primary bus voltage

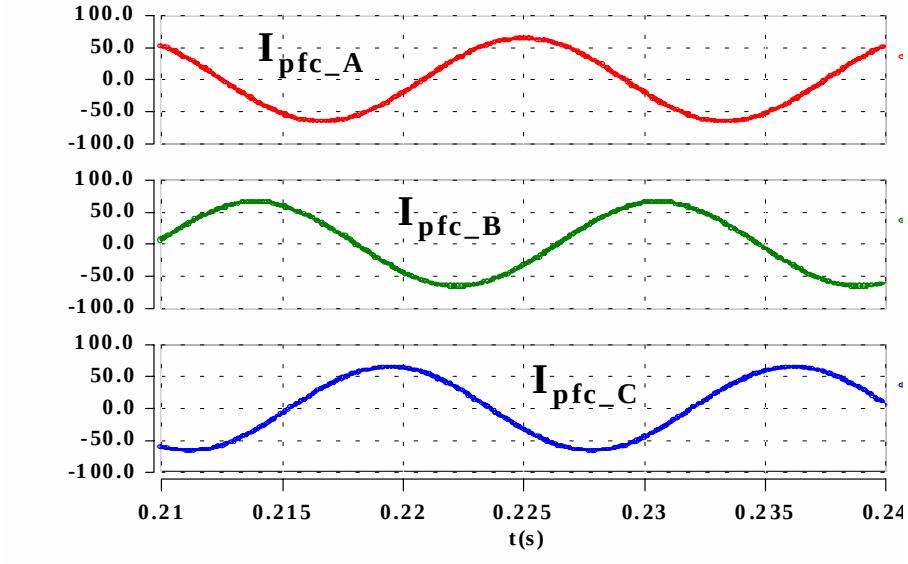


Figure 6-12 Using load conditioner to eliminate nonlinear loading effect

– PFC bus regulator input currents

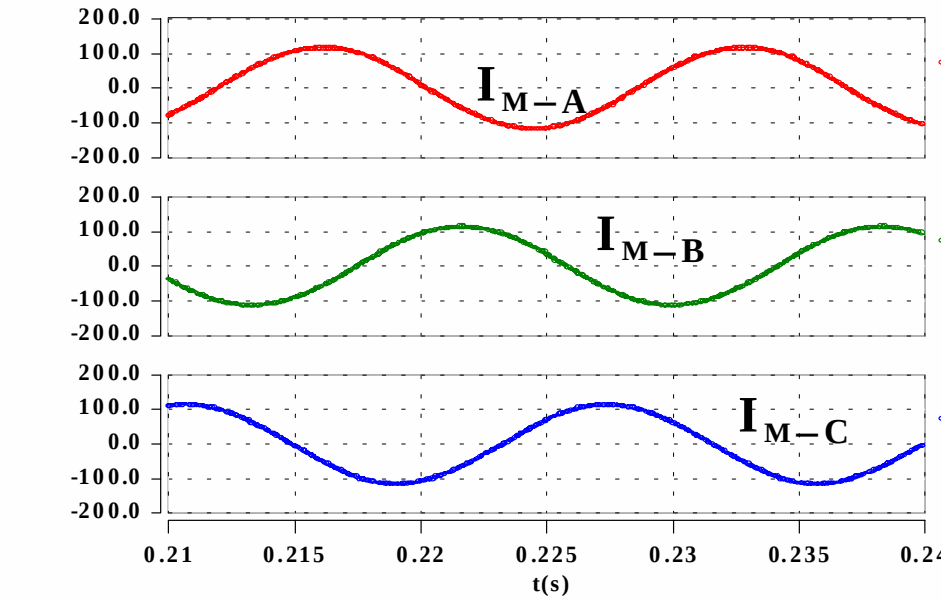


Figure 6-13 Using load conditioner to eliminate nonlinear loading effect

– main inverter output currents

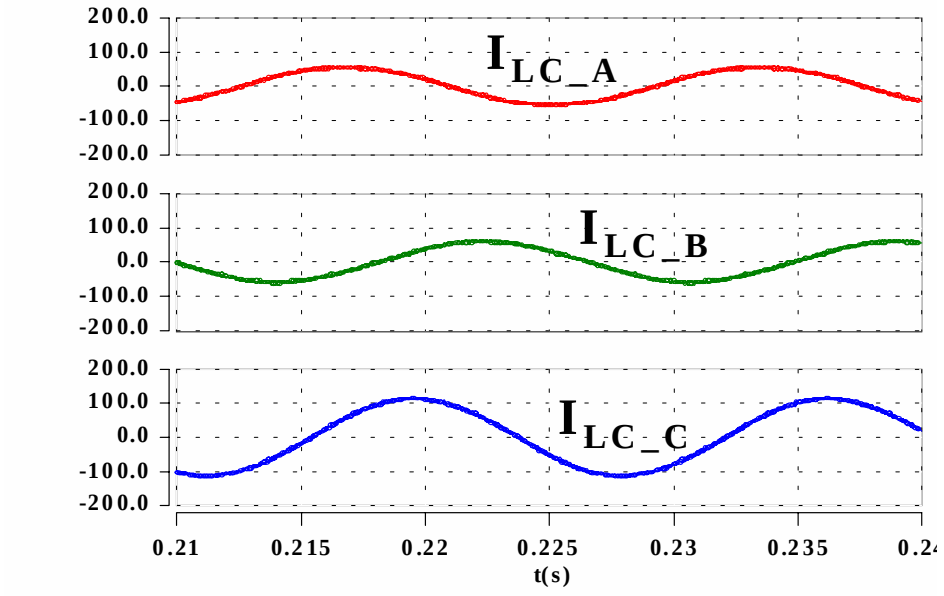


Figure 6-14 Using load conditioner to eliminate nonlinear loading effect

– load conditioner output currents

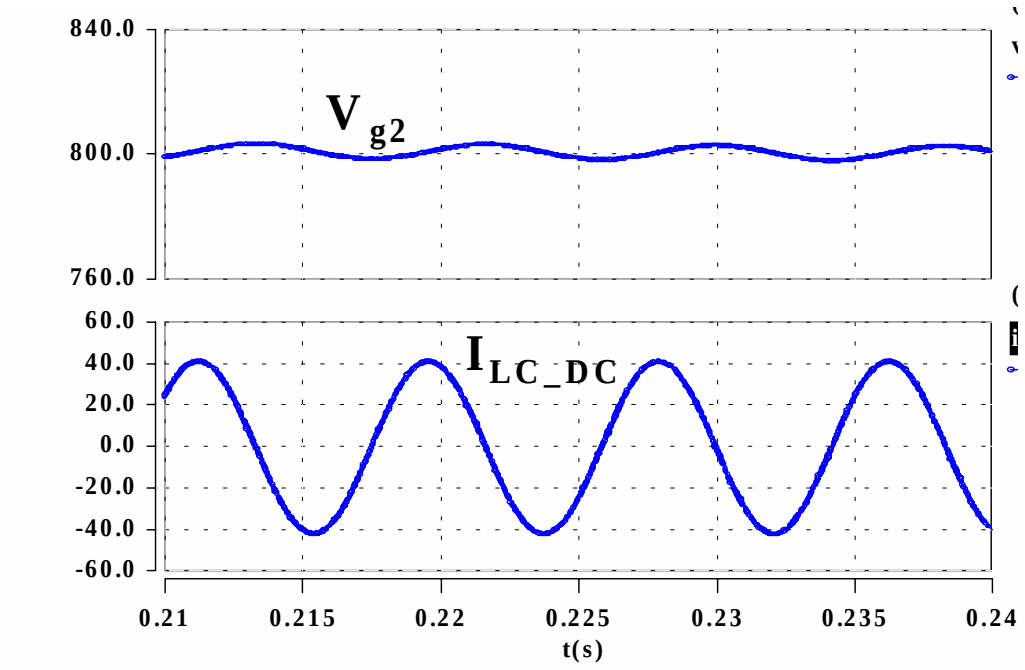


Figure 6-15 Using load conditioner to eliminate nonlinear loading effect

– (a) load conditioner DC link voltage; (b) load conditioner DC link current

6.4 DC Bus Conditioner to Eliminate Nonlinear Loading Effect

The load conditioner concept, proposed in Chapter 5, may be considered a three-phase AC bus conditioner. It prevents the harmonic currents from traveling back to the AC bus. It also provides active damping to the AC bus. We can extend this concept and apply it to the DC distribution bus. Since the utility subsystem is a load to the primary DC distribution bus, a bus conditioner can be used to eliminate the nonlinear loading effect, as shown in Figure 6-16. The power stage topology of the DC bus conditioner could be a full bridge configuration, as shown in Figure 6-17. Using "in-place" averaging technique, the average large signal model of the DC bus conditioner is obtained and shown in Figure 6-18. The duty ratio d_{BC} is within [-1,1].

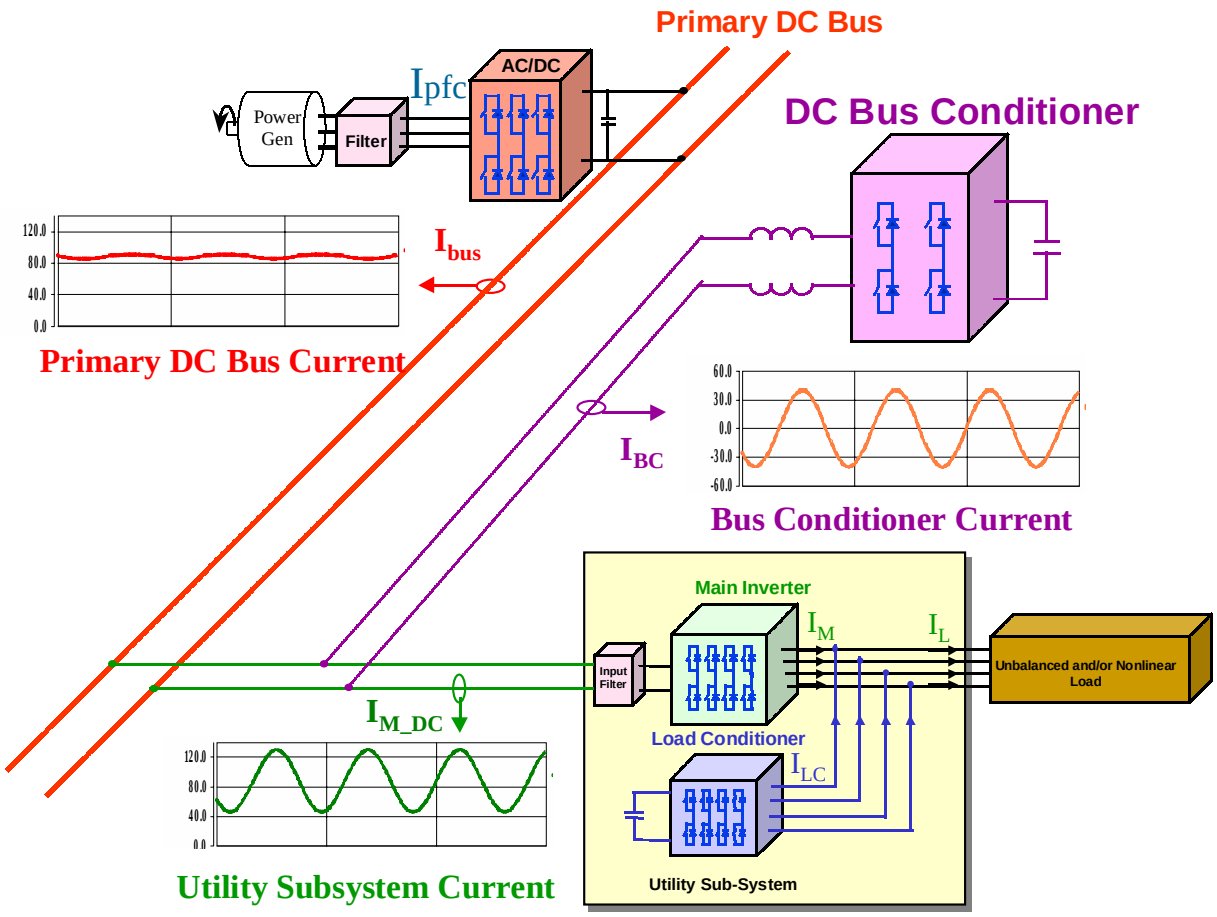


Figure 6-16 DC bus conditioner to eliminate nonlinear loading effect

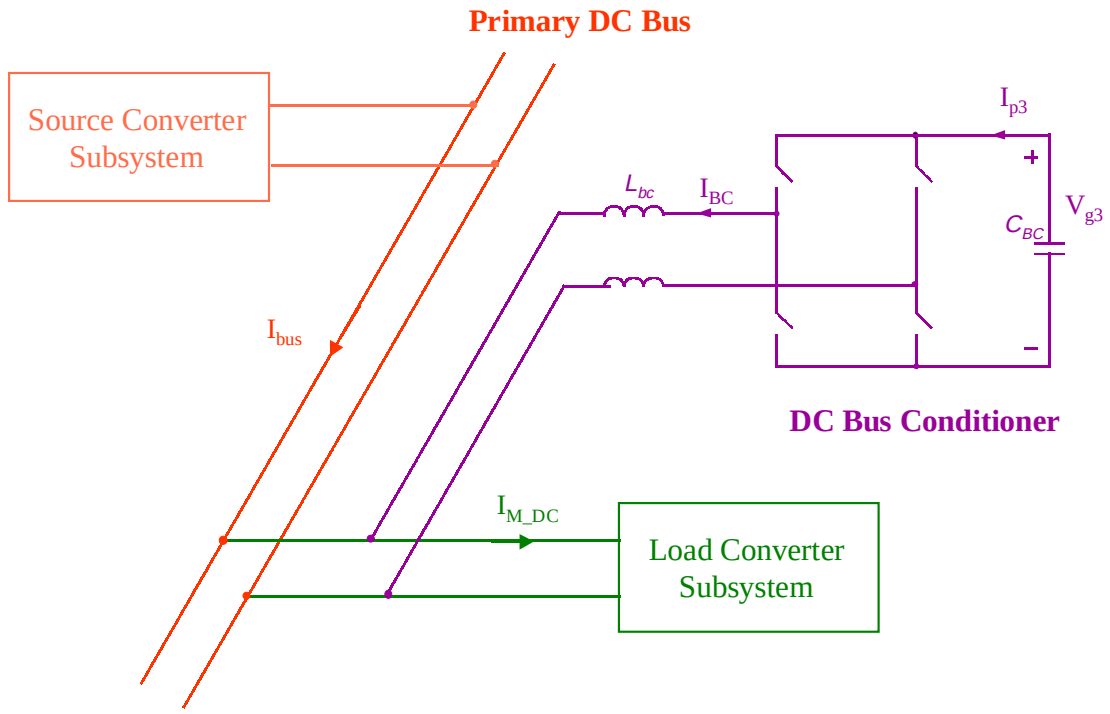


Figure 6-17 Power topology of the DC bus conditioner

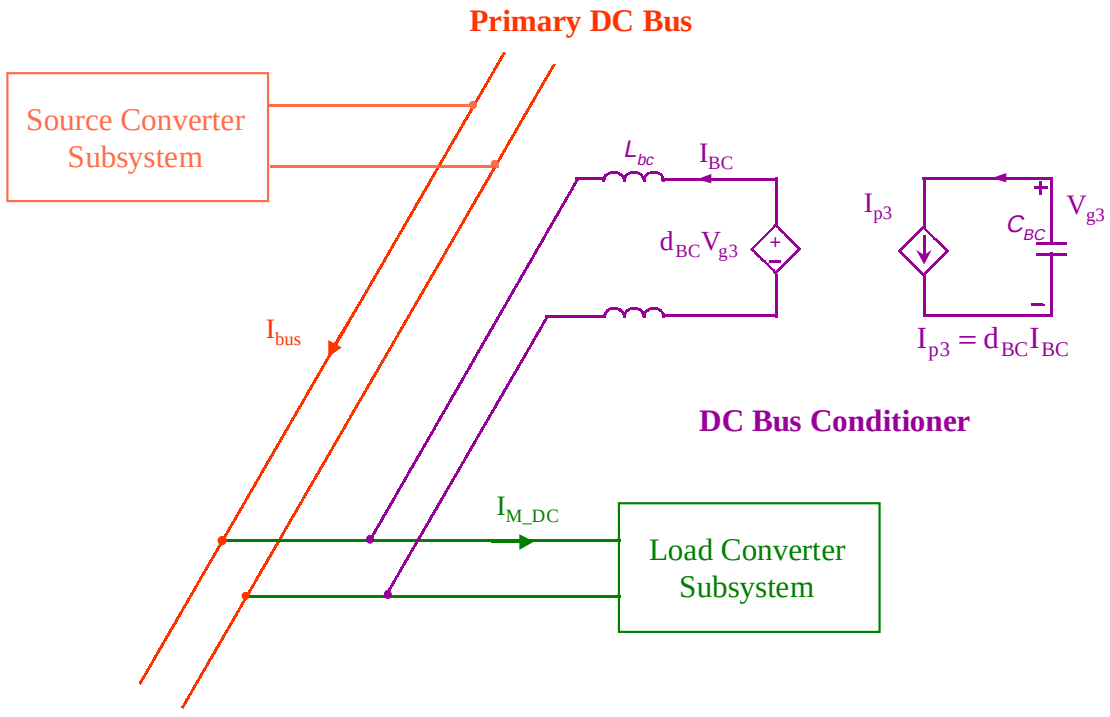


Figure 6-18 Average large-signal model of the DC bus conditioner

Just like the load conditioner in the utility subsystem, the DC bus conditioner has a current loop and a superimposed voltage loop to control its DC link voltage. The DC bus conditioner is controlled to be a current source to perform two functions ─ the active filter function and the active damping function. The current reference of the bus conditioner is given as

$$\mathbf{(6.6)} \qquad I_{BC\_ref} = I_{BC\_ref1} + I_{BC\_ref2}$$

$$\mathbf{(6.7)} \qquad I_{BC\_ref1} = \tilde{I}_{M\_DC}$$

$$\mathbf{(6.8)} \qquad I_{BC\_ref2} = -\frac{\tilde{V}_{bus}}{R_{AC}}$$

where $\tilde{I}_{M\_DC}$ is the harmonic current drawn by the main inverter, $\tilde{V}_{bus}$ is the harmonic contents of the primary bus voltage, and R_{AC} is the desired AC damping resistance. (6.7) is used to perform the active filter function. The bus conditioner senses and traps the low frequency harmonic currents from the load converter system.

The DC distribution bus is highly under-damped when the load on the bus is light. It is desirable to provide damping to such a system. (6.8) is used to perform the active damping function. The bus conditioner senses the harmonic contents of the DC bus voltage, and draws a current proportional to the harmonic voltage to mimic a resistor at high frequency range. The designed power stage and control parameters can be found in Appendix C. The current loop bandwidth has been designed at 12 kHz; the voltage loop bandwidth has been designed at 8 Hz.

The effectiveness of the bus conditioner is demonstrated in the simulation results. With the same unbalanced load condition, Figure 6-19 shows an almost constant primary DC bus current and stabilized primary DC bus voltage. Under the favorable primary DC bus condition, the input current of the PFC bus regulator is three-phase sinusoidal, as shown in Figure 6-20. It is seen that the nonlinear loading effect is eliminated. Figure 6-21 indicates that the utility subsystem still requires I_{M_DC}, a DC current

superimposed by a large 2nd harmonic ripple current. The ripple portion of the utility subsystem DC link current I_{M_DC} is trapped by the DC bus conditioner. The net current drawn from the primary DC distribution bus I_{bus} is almost constant. Since the operation of the utility subsystem is almost the same as the original one when we had nonlinear loading problem, the main inverter output currents and the load conditioner output currents, as shown in Figure 6-22 and Figure 6-23, are similar to those in Figure 6-8 and Figure 6-9.

Compared with the solution of using the load conditioner to eliminate the nonlinear loading effect, the DC bus conditioner is a more general solution to the nonlinear loading problem of the DC distribution bus. Several load converters may share one DC bus conditioner. In the construction of a real system, where the DC bus conditioners are installed will affect their effectiveness. The DC bus conditioner should be carefully arranged when there are multiple load converters.

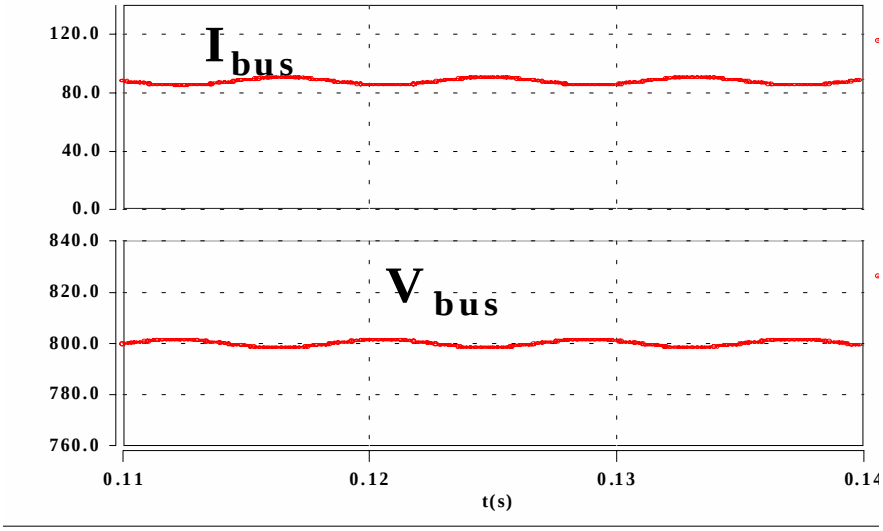


Figure 6-19 Using DC bus conditioner to eliminate nonlinear loading effect

– (a) primary DC bus current; (b) primary DC bus voltage

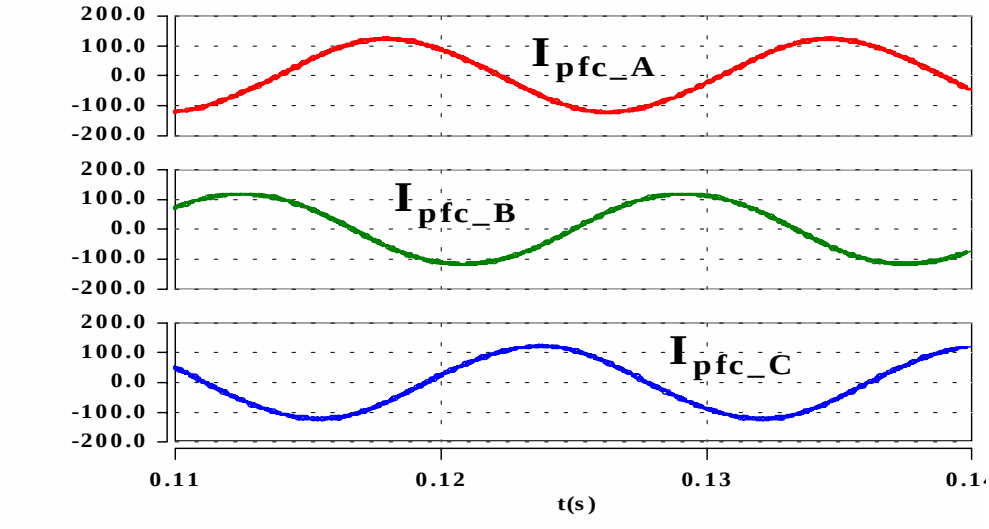


Figure 6-20 Using DC bus conditioner to eliminate nonlinear loading effect

– PFC bus regulator input currents

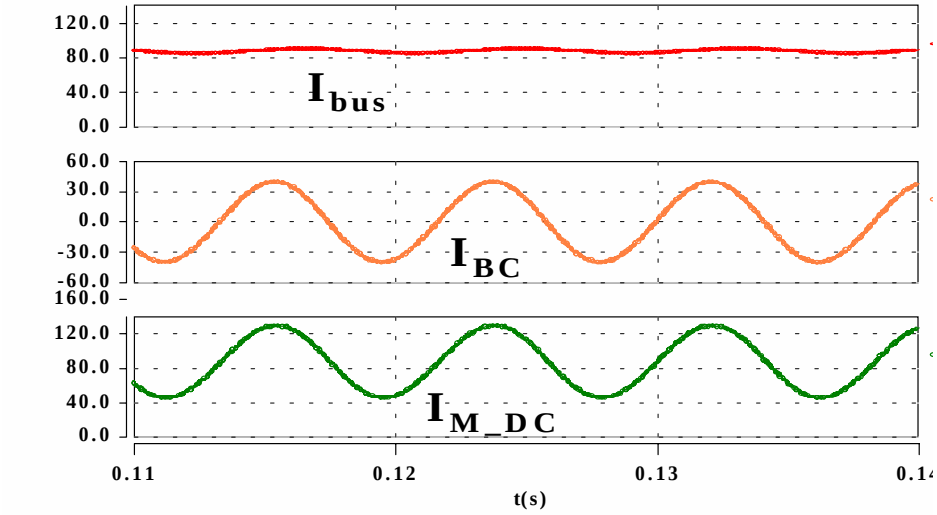


Figure 6-21 Using bus conditioner to eliminate nonlinear loading effect

– (a) primary DC bus current; (b) Bus conditioner current; (c) Utility subsystem current

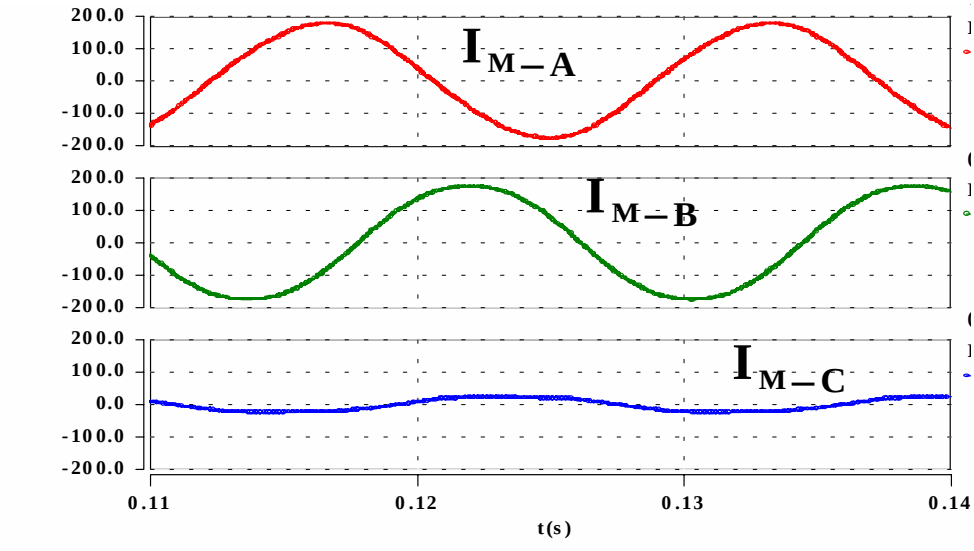


Figure 6-22 Using bus conditioner to eliminate nonlinear loading effect

– main inverter output current

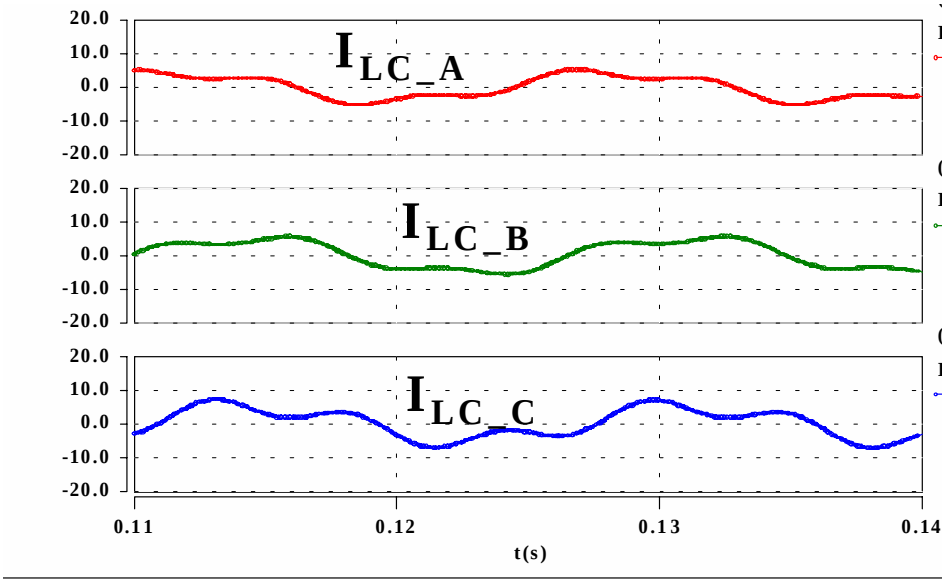


Figure 6-23 Using bus conditioner to eliminate nonlinear loading effect

– load conditioner output current

6.5 Conclusions

When the utility sub-system is connected to the DC distribution bus, a couple of system-level issues are observed. In addition to a system interaction problem in a small signal sense, the nonlinear loading effect of the load converter is highlighted. This nonlinear loading effect may cause a severe system stability problem in a large-signal sense.

Two approaches to solve this large-signal nonlinear loading effect, using a load conditioner and using a bus conditioner, are proposed in this chapter to keep the large-signal low-frequency ripple current from the DC distribution bus. Confining the low frequency ripple within the utility subsystem could solve the problem generated locally by the unbalanced load. A more general approach is to use a DC bus conditioner. The DC bus conditioner follows the same concept as the load conditioner, providing a counterbalance ripple current and damping to the DC distribution bus. The arrangement of the DC bus should be carefully designed in order to have an economical and effective system. It is proved that the nonlinear loading effect could be solved by both approaches.

Chapter 7 Conclusions

This dissertation deals with nonlinear and unbalanced load/source at different levels:

1. Power Converter Level

- Four-legged voltage source power converters, including inverter and PFC rectifier, are analyzed under nonlinear and unbalanced load, and unbalanced source,
- Comprehensive design guidelines for four-legged voltage source power converters are given taking the load and source conditions into consideration,
- Three-dimensional space vector modulation schemes are proposed for four-legged voltage source power converters,
- Characteristics of unbalanced and nonlinear loads in both stationary and rotating coordinate are analyzed,
- Modeling and control design of four-legged power converters are presented, and
- Fault tolerant operation of four-legged PFC rectifier is proposed and demonstrated

2. Power Converter System Level

- Load conditioner concept is proposed to construct high-performance power converter system under nonlinear load, and
- Modeling and control design of a power converter system for nonlinear loads are presented.

3. Large-Scale Power Electronics System Level

- Nonlinear loading effect of a load converter subsystem to the primary DC bus in a DC distribution power system is analyzed,
- Using the load conditioner with a modified control scheme to eliminate the nonlinear loading effect is proposed, and
- Using a bus conditioner, which is an extension of the load conditioner concept, to eliminate the nonlinear loading effect is also analyzed.

Unbalanced and/or nonlinear load and unbalanced source are the most common and realistic situations for most power conversions. The large neutral current and high control bandwidth requirement for a high performance present challenges to both power topology and control design.

Four-legged PWM converters are effective in a three-phase four-wire system to handle the neutral current caused by nonlinear and/or unbalanced load or unbalanced source. Compared with traditional ways to provide the neutral connection by using split DC link capacitors or other passive means, four-legged converters can reduce size, weight and cost due to significantly reduced low frequency reactive components, and can give better performance.

Three-dimensional space vector modulation schemes, proposed in Chapter 3, are superset of traditional two-dimensional space vector modulation schemes, and therefore, much more complicated than their two-dimensional counterparts. However, they are the best choice for four-legged voltage source power converters for high voltage and high power applications. They inherit all the merits of two-dimensional space vector modulation schemes, such as high DC link voltage utilization, low output distortion and harmonic contents, possibility to optimize for lower switching losses, and compatibility with digital controller.

The unbalanced and/or nonlinear load imposes special requirements for the power stage design, for example the DC link voltage selection and the power rating of the neutral leg, that are different from a three-legged power inverter design.

The average large-signal models of four-legged power converters are given in both the a-b-c stationary coordinate and the d-q-o rotating coordinate. The modeling procedure is the same as that for three-legged power converters. However, the additional o channel is added in the d-q-o rotating coordinate. The o channel manifests the effect of the neutral current caused by an unbalanced and/or nonlinear load. Small-signal models are developed in the d-q-o coordinate for control loop design. The models are verified by measurement results. It is verified by simulation and experimental results that the four-legged power inverter is effective for balanced and unbalanced linear load.

A four-legged inverter is effective for nonlinear load if its control loop bandwidth can be designed high. However, for high power applications, the control bandwidth is limited by a relatively low switching frequency. In order to have a high performance under nonlinear load for high power applications, the load conditioner concept is proposed to handle only high frequency harmonics, which is only a small fraction of the total load power level. The load conditioner is augmented to a low switching frequency high power inverter to construct a power converter system. Running at a high switching frequency and with a high control bandwidth, the load conditioner performs active filtering, active damping and decoupling functions. With the load conditioner, not only the main inverter voltage control bandwidth can be extended to higher frequency range, but also a high current control bandwidth is achieved for the whole system. The power converter system structure can achieve better system performance under unbalanced and/or nonlinear load at a low cost.

When the power converter system is embedded in a large-scale power electronics system such as a DC distribution power system, the power converter system becomes a subsystem. Some system-level issues emerge. Instead of an ideal DC voltage source to the subsystem, the DC source is provided by other power converters, for example, PFC bus regulators. System-level issues exist at both the small-signal level and large-signal

level. The nonlinear loading effect of the subsystem to the primary DC bus is analyzed. It is a major system-level large-signal stability issue. Two solutions are proposed to eliminate the nonlinear loading effect. One is to modify the control scheme of the load conditioner so that the low-frequency ripple power is also handled by the load conditioner. This approach confines the problem within itself. By extending the concept of the load conditioner used for secondary AC bus to the primary DC bus, the other approach uses a bus conditioner to handle the low-frequency ripple power, and to provide damping to the primary DC bus. The bus conditioner is a more general approach to the nonlinear loading effect on the primary DC bus.

Future research may concentrate on the following:

- Simplify three-dimensional SVM algorithm,
- Investigate the impact of three-dimensional SVM schemes on grounding and the common-mode noise issues,
- Develop a model, and implement control design in Z domain and incorporate predictive control so that the controller is more compatible with the digital controller and also the limitation caused by digital delay can be alleviated,
- Apply the load conditioner concept to all the load converters on the primary bus to have a “bus friendly” load converter. The “bus friendly” load converter can provide damping and thus improve the stability of the primary DC bus,
- Explore the possibility of adding perturbation to the load converters and source converters to implement on-line impedance identification for real time stability diagnosis,
- Comprehensive trade-off study of the large-scale power electronic system design, for example, the bus conditioner design and installment in the system, and

- Develop a simplified load converter subsystem behavior model both in large-signal and small-signal for evaluation of system level stability.

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Appendix A Calculation of DC Link Capacitance for Four-Legged Inverter and Three-Phase Half-Bridge Inverter

A.1 DC Link Capacitance for Four-Legged Inverter

DC link capacitance for four-legged inverter is calculated assuming a balanced three-phase AC output voltage $[V_{AG} \quad V_{BG} \quad V_{CG}]$ is obtained, and the permitted DC link voltage ripple ΔV_g is very small compared with the DC link voltage V_g, i.e. $\Delta V_g << V_g$, where ΔV_g is the peak value of the ripple voltage.

The ripple power delivered to the load is the negative-sequence power due to the unbalanced load can be expressed as

(A.1) $$P_n = [V_{AG} \quad V_{BG} \quad V_{CG}] \cdot [I_{LA\_n} \quad I_{LB\_n} \quad I_{LC\_n}]^T$$

where $[I_{LA\_n} \quad I_{LB\_n} \quad I_{LC\_n}]$ is the negative-sequence load current. From (A.1) it can be seen that the negative-sequence power is a 2ω ripple power, which can be in turn expressed as

(A.2) $$P_n = \frac{3}{2} V_m I_n \cos(2\omega t + \varphi_{p_n})$$

where V_m is the peak of AC output voltage, and I_n is the peak of negative-sequence load current. Therefore, the peak-to-peak energy ripple required by the load is

(A.3) $$\Delta E_{pp} = \frac{3 V_m I_n}{2\omega}$$

On the other hand, the peak-to-peak energy ripple across the DC link capacitor can be found as

(A.4) $$\Delta E_{pp} = \frac{1}{2} C_{dc} (V_g + \Delta V_g)^2 - \frac{1}{2} C_{dc} (V_g - \Delta V_g)^2 = 2 C_{dc} V_g \Delta V_g$$

By equating (A.3) and (A.4), the minimum DC link capacitance for a ripple voltage ΔV_g is given by

(A.5) $$C_{dc\_min\_n} = \frac{3 V_m I_n}{4 \cdot \omega \cdot V_g \cdot \Delta V_g}$$

Further, the above equation can be written as

(A.6) $$C_{dc\_min\_n} = \frac{\sqrt{3}}{4} \frac{M I_n}{\omega \cdot \Delta V_g}$$

where M is the modulation index. It can be seen that the required DC link capacitance is smaller with lower modulation index.

A.2 DC Link Capacitance for Three-Phase Half-Bridge Inverter

A three-phase half-bridge uses split DC link capacitors. Since two capacitors are in series, each capacitor is expressed as $2C_{dc}$. Since the neutral current, expressed in (A.7), flows through the middle point of the two DC link capacitors, equivalently these two DC link capacitors are in parallel ($4C_{dc}$) to handle the neutral current.

(A.7) $$I_n = I_{nm} \cos(\omega t + \varphi_0) = 3 I_0 \cos(\omega t + \varphi_0)$$

where I_{nm} is the peak of the neutral current; and I_0 is the peak of the zero-sequence current. Therefore the peak voltage ripple across each of the DC link capacitor due to the neutral current is expressed as

(A.8) $$\Delta V_{C_{dc}} = \frac{3 I_0}{4 \omega C_{dc}} = \frac{1}{2} \Delta V_g$$

From (A.8), we can have the minimum DC link capacitance due to the zero-sequence load current expressed as

(A.9) $$C_{dc\_min\_0} = \frac{3I_0}{2\omega\Delta V_g}$$

A.3 Comparison

Physically a 100% negative-sequence imbalance means the 2ω ripple power is the same as the rated three-phase total power, while a 100% zero-sequence imbalance means the neutral conductor carries three times per phase rated load current. A 33% negative-sequence imbalance means the 2ω ripple power is the same as the rated per phase power, while 33% zero-sequence imbalance means the neutral conductor carries the rated per phase load current.

The two DC link capacitances given by (A.6) and (A.9) are compared for a design example described in Chapter 3, Section 3.5.4.1. The resulting modulation index M based on the design is 0.848. The comparison is based on a 2% of DC link voltage ripple, which is 16 V. Under 100% negative-sequence and zero-sequence imbalance, the resulting minimum DC link capacitance are 15.5 mF and 63.5 mF, respectively. Under 33% negative-sequence and zero-sequence imbalance, the resulting minimum DC link capacitances are 5.2 mF and 21.2 mF, respectively. Therefore, for this specific design example, to achieve the same voltage ripple, the capacitance needed for a four-legged inverter is four times smaller than a three-phase half-bridge inverter using split DC link capacitors.

Appendix B Parameters of Front-End PFC Bus Regulator

B.1 Power Stage Parameters

- Input Inductor: 330 μH
- DC Link Capacitor: 720 μF

B.2 Control Loop Parameters

Current Compensators

	D	Q
K_P	0.01	0.01173
K_I	12.566	

DC Link Voltage Compensator

K_P	1.2
K_I	376.6

Appendix C Bus Conditioner Parameters

C.1 Power Stage Parameters

- Input Inductor: 400 μH
- DC Link Capacitor: 5 mF / 1600 V

C.2 Control Loop Parameters

Current Compensators

K_P	0.0282
K_I	3.5437

DC Link Voltage Compensator

K_P	1.1

Vita

The author was born in Kunming, Yunnan, P. R. China, in March 1968. He received the B.S. degree and M.S. degree from the Tsinghua University, in 1989 and 1993, respectively, both in electrical engineering.

From 1989 to 1991 he was employed as a Design Engineer at Tsinghua Ziguang Company, where he worked on power converter designs for ultrasonic cleaner, electronic ballast, and induction heating, as well as digital controllers for power converters.

In fall, 1994, the author enrolled at VPI&SU as a doctoral student. He conducted research on soft-switching three-phase PFC rectifiers, single-stage AC/DC power conversion, and bi-directional power conversion, digital controller and power converter modeling and control. Since 1996 his major research has focused on high power high performance standalone utility power conversion and DC distributed power systems.

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