SOFT-SWITCHING TECHNIQUES FOR PULSE-WIDTH-MODULATED CONVERTERS

by

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(ABSTRACT)

The concept of soft-switching pulse-width-modulated (PWM) technique was proposed aimed at combining the advantages of both the conventional PWM technique and the resonant technique. This work presents four new families of soft-switching PWM converters: the zero-voltage-switched (ZVS) PWM converters, the zero-current-switched (ZCS) PWM converters, the zero-voltage-transition (ZVT) PWM converters, and the zero-current-transition (ZCT) PWM converters.

The family of ZVS- and ZCS-PWM converters are developed to improve the performance of the ZVS and ZCS quasi-resonant converters, respectively. The principles of operations of these two families of converters are presented, and the merits and limitations are assessed. A number of experimental converters are breadboarded to verify the theoretical analysis.

Both the ZVT-PWM and ZCT-PWM techniques use the concept of shunt resonant network to achieve soft-switching. In this way, the new converters achieve soft-switching without increasing the voltage and current stresses of the power switches and diodes. By using the boost topology as an example, a complete dc analysis of the ZVT-PWM and ZCT-PWM converters is presented, and the dc voltage-conversion ratio

characteristics are derived. Design trade-offs are examined, and design procedures are established. The theoretical analysis and novel features of the proposed converters are verified on a number of breadboarded converters.

Finally, the typical small-signal characteristics of the ZVT-PWM converters are analyzed and verified experimentally by using the boost converter as an example.

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CHAPTER 1

INTRODUCTION

1.1 General Background

To accommodate the ever-increasing requirements for smaller size, lighter weight, and higher efficiency power supplies, switched-mode power conversion technologies have evolved from basic pulse-width-modulated (PWM) converters to resonant converters [A1-29], quasi-resonant converters (QRCs) [B1-36], multi-resonant converters (MRCs) [C1-15], and most recently to soft-switching PWM converters. Due to circuit parasitics and hard-switching condition, operation of a PWM converter involves high switching losses, switching stresses, and switching noises. These are the major factors that restrict PWM converters from operating at a higher frequency for size/weight reduction and performance improvement.

With the available devices and circuit technologies, PWM converters generally have been designed to operate with a 50-200 kHz switching frequency. In this frequency range, the power supply is deemed optimal in weight, size, efficiency, reliability, and cost. In more recent applications such as adaptor, notebook, and labtop computers where high power density is of primary concern, it is desirable to push the conversion frequency as high as the upper-hundreds kilohertz to lower-megahertz range. However, higher switching frequency invariably results in increased switching losses. The switching loss at turn-off is primarily caused by the leakage inductance of the power transformer. As the semiconductor device turns off, the sharp di/dt induces high voltage spike across the leakage inductance. To reduce switching stress, dissipative snubbers are typically used. At turn-on, switching losses are mainly caused by abrupt discharging of the energy stored in the parasitic capacitance of the semiconductor devices. When the transistor is turned on, the energy stored in its output capacitance is dissipated in the device. In addition, the rectifier's junction capacitance is dissipatively charged through the active switch, increasing switching loss and stress. Also, turn-on at high voltage levels induces a severe switching noise coupled through the Miller capacitance into the drive and control circuits. The aforementioned detrimental effects of the circuit parasitics become much more pronounced as the switching frequency is increased.

To improve switching conditions for semiconductor devices in switched-mode converters, several resonant techniques were proposed. The traditional series and parallel resonant converters, class-E converters [D1-7, D12-15], quasi-resonant converters, multi-resonant converters, and resonant dc link

converters [D9, D10] are included in this category. By incorporating certain types of resonant network into a PWM topology, numerous resonant converters can be formed, offering a zero-voltage switching (ZVS) or zero-current switching (ZCS) condition for the switches. This improvement significantly reduces switching losses and enables the converter to operate at a higher switching frequency. However, due to the resonant nature of the current and voltage waveforms, the operation of resonant converters usually involves high circulating energy which results in a substantial increase in conduction losses. For instance, the ZVS-QRC technique employs an LC resonant network to shape the switch voltage waveform so that the power switch is operated with ZVS. Although the switching loss is reduced, the transistor suffers from an excessive voltage stress that is proportional to the load range [C2]. The ZVS-MRC technique utilizes a multi-element resonant network to implement ZVS for both the active and passive switches. The unique arrangement of the multi-resonant network is aimed at absorption of all major parasitic components, including transistor output capacitance, diode junction capacitance, and transformer leakage inductance. This allows the ZVS-MRCs to operate at high frequencies while each semiconductor device in the circuit can operate at its switching condition. Nevertheless, both the active and passive switches in a ZVS-MRC are subjected to peak voltage and current stresses significantly higher than those in their PWM counterparts. Another major limitation of the resonant converters is variable frequency operation. For converters operating with a wide input voltage range or load range, the switching frequency range is also wide. As a result, the optimum design of the magnetic components (inductors and transformers) and EMI and output filters is difficult to achieve. In addition, the

bandwidth of the closed-loop control is compromised, since it is determined by minimum switching frequency. Therefore, to attain a greater benefit from high-frequency operation, it is desirable to operate the converter at a fixed frequency. Although a number of constant-frequency resonant converters operating under either ZVS or ZCS have been proposed [E1-18], operation of these converters still involves high circulating energy.

As a compromise between the PWM and resonant techniques, the soft-switching PWM techniques were proposed aimed at achieving soft-switching without a significantly increase in circulating energy [F1-39]. Generally, a soft-switching converter utilizes some form of resonant technique to soften the switching transition. When the switching transition is completed, the converter reverts back to the familiar PWM mode of operation so that the circulatory energy can be minimized. Meanwhile, the switching frequency of the converter is kept fixed so that the circuit optimization can be easily attainable.

1.2 Present Work

This work presents four families of soft-switching PWM converters: the ZVS-PWM converters, the ZCS-PWM converters, the zero-voltage-transition (ZVT) PWM converters, and the zero-current-transition (ZCT) PWM converters.

The ZVS-PWM technique can be considered an extension of the ZVS-QRC technique [F14, F37-F39]. It uses an auxiliary switch across the resonant

inductor in a ZVS-QRC to create a freewheeling stage within the quasi-resonant operation, enabling the converter to operate with a constant frequency and much reduced circulating energy. The problems of the ZVS-PWM technique are associated with the resonant inductor which is in the main power path. First, for single-ended topologies, this resonant inductor induces a high voltage spike on the power switch which is proportional to the load current. Second, the rectifier diode sees severe parasitic ringing due to the resonance between the diode junction capacitance and the resonant inductor. In addition, the ZVS condition of the converter is quite sensitive to line voltage or load change. A particular topology in this family, the bridge-type ZVS-PWM topology [F9-F12], is deemed most desirable, since its switches are subjected to minimum voltage stresses.

For high-power applications where minority-carrier devices such as BJTs, IGBTs, GTOs, and MCTs are used as the power switches, the ZCS technique is deemed more desirable than ZVS in reducing the device switching losses. As a dual circuit technique to the ZVS-PWM technique, a family of ZCS-PWM converters is proposed to implement ZCS for the power switch(es) and ZVS for the rectifier diode(s) without having too much circulating energy [F37-F39]. The ZCS-PWM technique presents a significant improvement over the ZCS-QRC technique. The limitations of the ZCS-PWM technique, which include severe parasitic ringing on power switch, high voltage stress of the rectifier diode, and the line and load dependence of the ZCS condition, are associated with the use of the resonant inductor in series with the power switch. In particular, the severe parasitic ringing between the output capacitance of the power switch and the resonant inductor increases the voltage stress of the power switch and

necessitates the use of a power device with higher voltage rating and slower switching characteristics.

Both the ZVT-PWM technique and the ZCT-PWM technique use a shunt resonant branch to achieve soft-switching. During the switching transition, the shunt resonant network is activated to create a partial resonance to achieve ZVS or ZCS. When the switching transition is over, the shunt resonant network is disabled so that the operation of the converter resembles that of the PWM converter during most portions of the switching cycle. In this way, the new converters can achieve soft-switching without increasing the voltage and current stresses of the switches. Since the shunt resonant network only handles little switching transition energy, the V/I ratings and sizes of the auxiliary components are quite small compared to those of the major power stage components.

Since the ZVT-PWM technique implements ZVS for both the power switch and the rectifier diode, it is deemed particularly attractive for high voltage applications (such as power factor correction circuits) where the reverse-recovery problem of the high-voltage diode is of primary concern [F26-F33]. The ZCT-PWM converters, however, are deemed attractive for high-power applications where minority-carrier devices such as BJTs, IGBTs, GTOs, and MCTs are used as power switches [F34-F39]. In this study, the boost topology is used as an example to illustrate the operation and evaluate the performance of the ZVT- and ZCT-PWM converters.

Since the operation of the ZVT- and ZCT-PWM converters is the same as that of the conventional PWM converters, except during the short switching transition time, the design of the main power stage components of the new

converters is basically the same as that of their PWM counterparts. Therefore, the focus of the analytical work is on the design of the shunt resonant branch components. From the equations obtained from steady-state analysis, design trade-offs are analyzed and design guidelines are proposed for both the ZVT- and ZCT-PWM converters. In addition, a small-signal analysis of the ZVT-PWM boost converter is performed to see how soft-switching operation impacts the small-signal behavior of the ZVT-PWM converters.

1.3 Dissertation Outline

This dissertation consists of six chapters.

In Chapter 2, the principle of operation of the ZVS-PWM technique is introduced, and a family of ZVS-PWM converters is derived. The experimental results of several breadboarded converters are also presented.

Chapter 3 presents the principle of operation and dc characteristics of the family of ZCS-PWM converters.

In Chapter 4, the principle of operation of the ZVT-PWM technique is presented, and a family of ZVT -PWM converters is derived. Using the boost topology as an example, a complete dc analysis of the ZVT-PWM converters is presented, and the dc voltage-conversion ratio characteristics are derived. Design trade-offs are examined, and design guidelines are defined. In addition,

the typical small-signal characteristics of the ZVT-PWM converters are analyzed and verified experimentally.

In Chapter 5, a family of ZCT-PWM converters is presented. Using the boost topology as an example, a complete dc analysis of the ZCT-PWM converters is performed, and the dc voltage-conversion ratio characteristics are derived. Design trade-offs are examined, and design procedures are established. The theoretical analysis and novel features of the proposed converters are verified on several experimental converters.

Conclusions of this work are given in Chapter 6.

CHAPTER 2

ZERO-VOLTAGE-SWITCHED PWM CONVERTERS

2.1 Introduction

As one of the typical resonant-type ZVS techniques, the ZVS-QRC technique eliminates the capacitive turn-on loss which plagues ZCS-QRCs and PWM converters [B19]. The drain-to-source voltage of the power MOSFET in a ZVS-QRC is shaped to zero prior to turn on, thus eliminating turn-on switching loss and the Miller effect. In addition, the active switch in a ZVS-QRC is subjected to a relatively low current stress and hence is preferable over that of the ZCS-QRC technique for high-frequency conversion where MOSFETs are employed.

However, the ZVS-QRC technique has several limitations. First, the power switch in a single-ended ZVS-QRC suffers from a high voltage stress which is proportional to the load range. Using the buck ZVS-QRC as an example, for a 10% to 100% load range, the peak voltage stress of the power switch can be 11 times the input voltage. Therefore, a high voltage MOSFET accompanied by high on-resistance and large input capacitance has to be used, resulting in a substantial increase in conduction loss and the gate driver loss. Second, a wide switching frequency range is required for a ZVS-QRC to operate with a wide input voltage and load range. The wide frequency range makes optimization of the power transformer, input/output filters, control circuit, and gate-drive circuit difficult. For example, to decrease conduction loss, power MOSFETs with low on-resistance are preferred. However, MOSFETs with low on-resistance are accompanied by large input capacitances, which can cause significant driver loss at high-frequency operation, especially at high line and light load [F14].

Another limitation of the ZVS-QRC technique is severe parasitic ringing between the resonant inductor and the diode junction capacitance. Due to the presence of the large resonant inductor, this parasitic ringing is enhanced as compared to its PWM counterpart. In a practical circuit, the severe parasitic ringing not only increases switching loss and switching noise, but may result in possible instability in the closed-loop system as well [B17].

In principle, the voltage stress of the power switch in a ZVS-QRC can be reduced at the expense of a partial loss of ZVS at light load. This may not cause a thermal problem, since the switch conduction loss is low at light load. In a real

circuit, however, to operate a ZVS-QRC in an adequate frequency range, an external capacitor as part of the resonant capacitor usually needs to be placed in parallel with the power switch. In this case, the partial loss of the ZVS at light load may not be allowed, considering both high switching loss and high switching noise. In particular, the switching frequency increases as load current decreases; thus the capacitive turn-on loss can easily become intolerable at light load. With a wide load range, optimization of ZVS-QRCs is very difficult to achieve.

This chapter presents a new class of ZVS-PWM converters. Employing an auxiliary switch across the resonant inductor in a ZVS-QRC allows the new converter to operate with much reduced circulating energy and with a constant frequency. It is also shown that the use of a saturable inductor can further improve the performance of the proposed ZVS-PWM converters.

2.2 A Family of ZVS-PWM Converters

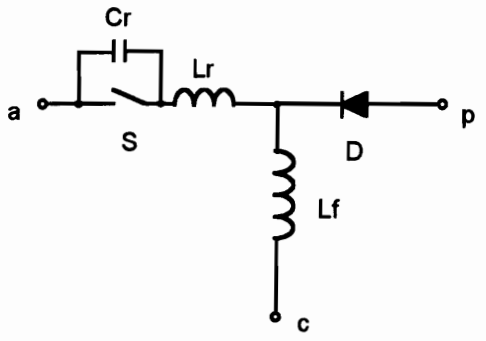
2.2.1. ZVS-PWM Switching Cell

The concept of ZVS quasi-resonant switch was introduced to perform a systematic analysis of topologies and features of the ZVS-QRCs [B5, B6]. By incorporating the PWM switching cell concept, a ZVS quasi-resonant switching cell can be derived, as shown in Figure 2.1(a) [F39]. In this figure, S is the

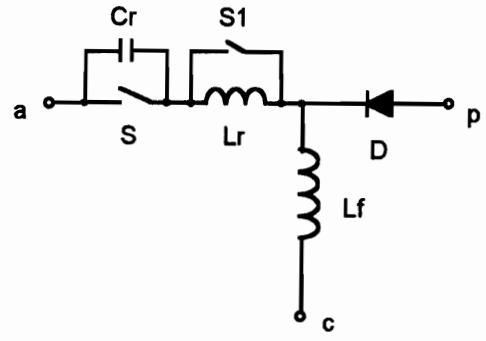
active switch, D is the rectifying diode, L_f is the energy storage inductor, C_r is the resonant capacitor, and L_r is the resonant inductor. To achieve ZVS, the off-time of the power switch is fixed. The output voltage is regulated by varying the on-time of the switch. By adding an auxiliary switch (S1) across the resonant inductor, the ZVS-PWM switching cell shown in Fig 2.1(b) is obtained. This auxiliary switch makes the off-time of the power switch (S) controllable. It enables the converter to regulate the output while operating at a fixed switching frequency.

In the ZVS quasi-resonant switching cell, the resonant inductor begins to oscillate with the resonant capacitor after the power switch is turned off. The power switch is turned on with ZVS after the resonance brings C_r voltage zero. The off-time of the power switch is determined by the resonant period of the resonant components. Thus a ZVS-QRC operates with constant off-time control. Consequently, a ZVS-QRC operating with a wide input voltage or load range has a wide frequency range.

In Fig. 2.1(b), S1 is turned on before the power switch is turned off. When the power switch is turned off, the resonant inductor current freewheels through S1 for a period of time. During this freewheeling time, the energy stored in the resonant inductor remains unchanged until S1 is turned off, when the resonant inductor begins to oscillate with resonant capacitor. The power switch is turned on after the resonance brings the capacitor voltage to zero. By controlling the time interval of the freewheeling stage, the off-time of the power switch can be varied, enabling the converter to operate with a fixed frequency.



(a)



(b)

Fig. 2.1. (a) ZVS quasi-resonant switching cell, and (b) ZVS-PWM switching cell.

To introduce the principle of operation of the ZVS-PWM converters, the buck ZVS-PWM converter is used as an example. The circuit schematic and key waveforms of the buck ZVS-PWM converter are shown in Fig. 2.2. It can be seen that the new circuit differs from a buck ZVS-QRC by an additional auxiliary switch placed in parallel with the resonant inductor. The output filter inductor is considered as a current source (I_o) in the analysis. As shown in Fig. 2.3, five topological stages exist within one switching cycle:

(1) T0-T1: Before time T0, the power switch S is conducting, and the rectifier diode D is off. At time T0, S is turned off . The freewheeling diode D is off, and the resonant inductor current remains at I_o value during this interval. The resonant capacitor (C_r) is charged linearly by I_o until its voltage reaches the input voltage. The equivalent circuit of this topological stage is shown in Fig. 2.3(a). This time interval is given by:

$$\Delta T_{01} = \frac{C_r V_i}{I_o}. \tag{2.1}$$

(2) T1-T2: At time T1, D starts to conduct. The L_r current still remains constant by circulating through the auxiliary switch S1. Therefore, the energy stored in the resonant inductor (which is used to achieve ZVS for S) stays unchanged.

(3) T2-T3: At time T2, S1 is turned off, and the resonance between L_r and C_r begins. This interval lasts until T3, when resonance brings V_{Cr} to zero and the anti-parallel diode of S starts to conduct. This time period is approximately three quarters of the resonant period, i.e.,

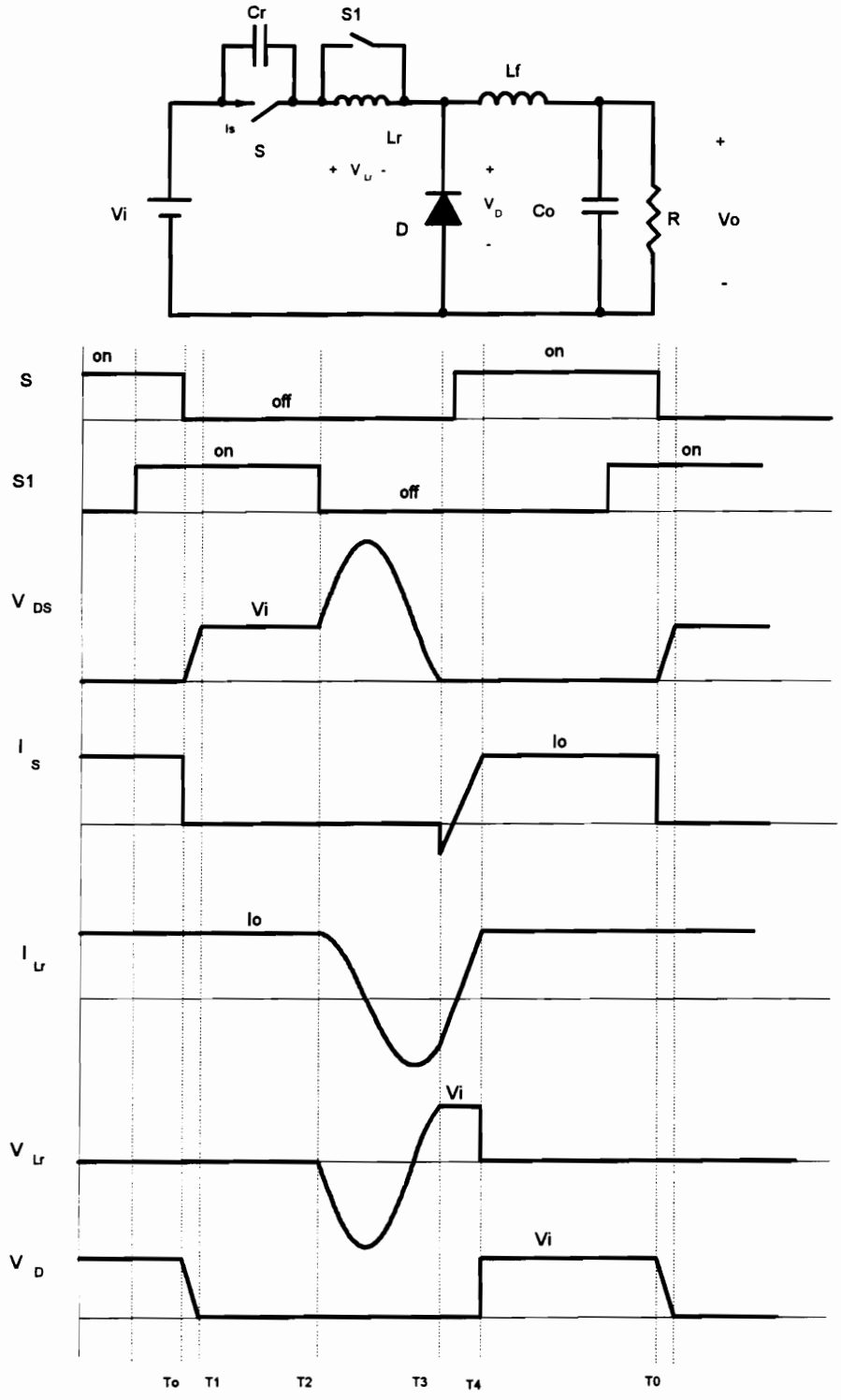
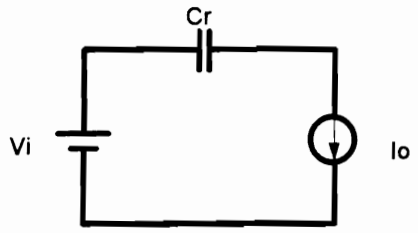
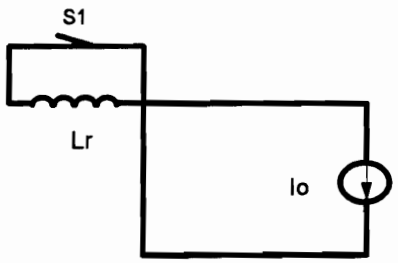


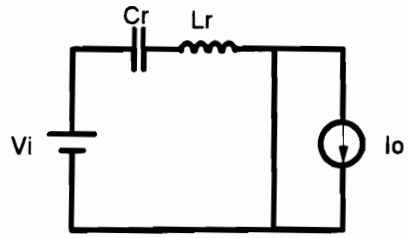
Fig. 2.2. Buck ZVS-PWM converter and its key waveforms.



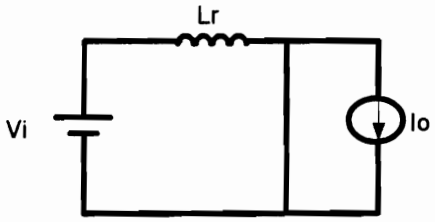
(a) T0 - T1



(b) T1 - T2



(c) T2 - T3



(d) T3 - T4

(e) T4 - T0

Fig. 2.3. Equivalent circuits for five operation stages.

$$\Delta T_{23} = \frac{3}{4}\sqrt{L_r C_r}. \tag{2.2}$$

(4) T3-T4: S is turned on with ZVS during this time interval. The L_r current increases linearly while the diode D current decreases. At T4, diode D is turned off with ZCS.

(5) T4-T0: S1 is turned on with ZVS before S is turned off. This interval lasts until T0, when S is turned off, and the cycle is repeated.

From the above description, it can be seen that the operation of the ZVS-PWM buck converter differs from that of the buck ZVS-QRC by possessing an extra freewheeling stage, (T1-T2), during which the resonant inductor current flows through S1 and remains constant. Constant-frequency operation is achieved by controlling this freewheeling time interval (T1-T2). Furthermore, the resonant interval (T2-T3) can be relatively short with respect to the switching period. In this way, the operation of the proposed circuit is similar to that of the conventional PWM converter during most portions of a switching cycle. Compared to a ZVS-QRC, the size of the resonant components becomes much smaller, and circulating energy of the circuit is much reduced.

The design strategy for the proposed buck ZVS-PWM converter is quite different from that of the buck ZVS-QRC. To limit the switch voltage stress, the circuit can be designed to operate with ZVS only at relatively heavy load (e.g., above 50 % load). Thus the maximum voltage stress of the active switch is approximately three times the input voltage at full load. At light load, ZVS is partially lost. This does not cause a thermal problem since the conduction loss is

low at light load. Furthermore, with only a partial voltage applied at turn on and constant frequency operation, the switching loss is not significant. At very light load, the operation of the proposed circuit is similar to that of a conventional PWM buck converter.

When the resonant frequency of the buck ZVS-PWM converter is designed to be much higher than the switching frequency, the parasitic ringing across the rectifier becomes less pronounced. The high frequency ringing can be easily suppressed. In addition, due to the constant frequency operation, snubber loss is constant with changes in load current. The buck ZVS-PWM converter presents a significant improvement over its ZVS-QRC counterpart.

2.2.2. Basic ZVS-PWM Topologies

A ZVS-PWM converter can either be derived from a conventional PWM converter or from a ZVS-QRC. By simply adding an auxiliary switch across the resonant inductor in ZVS-QRCs, the new class of ZVS-PWM converters is generated.

The procedure for converting a PWM topology into a ZVS-PWM topology is also straightforward. To derive a ZVS-PWM converter from a PWM converter, the following steps are followed:

1. A resonant capacitor is added in parallel with the power switch.

2. A resonant inductor is inserted in the loop containing the power switch and the diode.
3. An auxiliary switch is placed in parallel with the resonant inductor.

The above steps should only be viewed as a simple way of describing the relative positions of the resonant components. In fact, there exist several topological variations for each basic ZVS-PWM converter, which can be identified by using the capacitor- and inductor-shift rules. This issue is essentially identical to that found in ZVS-QRCs. The shifting of a resonant component results in a different dc bias applied to that component, but does not affect the basic operation of the circuit.

The six basic ZVS-PWM converter topologies, buck, boost, buck-boost, Cuk, Sepic, and Zeta, are shown in Fig. 2.4. Since the auxiliary switch is in parallel with the resonant inductor, it has to be a voltage-bidirectional switch, which can be implemented by a MOSFET in series with a reverse-voltage blocking diode.

2.2.3. ZVS-PWM Topologies with Isolation Transformer

By simply adding an auxiliary switch across the resonant inductor in each isolated ZVS-QRC topology, the isolated ZVS-PWM converters are generated. Figure 2.5 shows several basic ZVS-PWM converter topologies with isolation transformers.

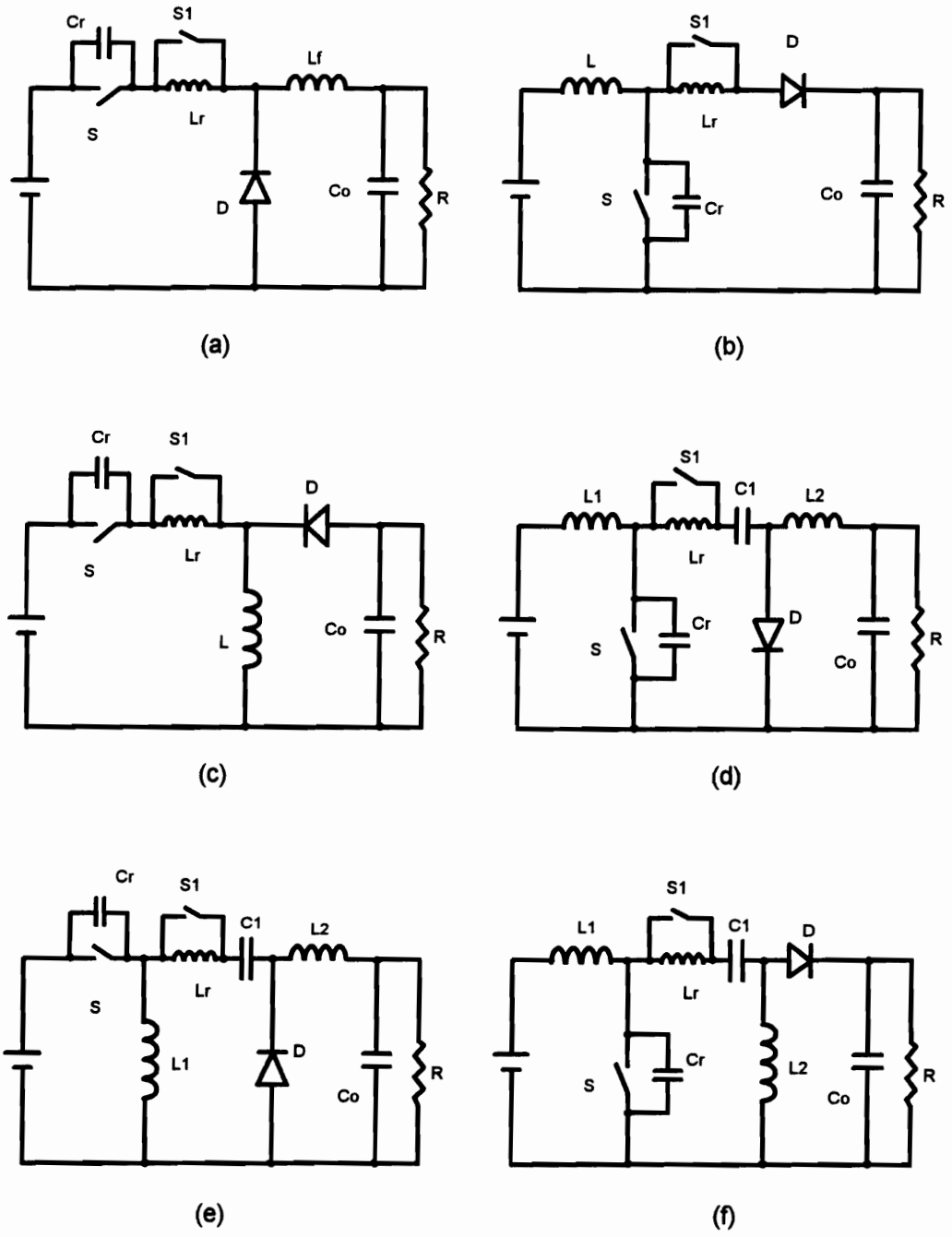


Fig. 2.4. Six basic ZVS-PWM converter topologies: (a) buck, (b) boost, (c) buck-boost, (e) Cuk, (e) Sepic, and (f) Zeta

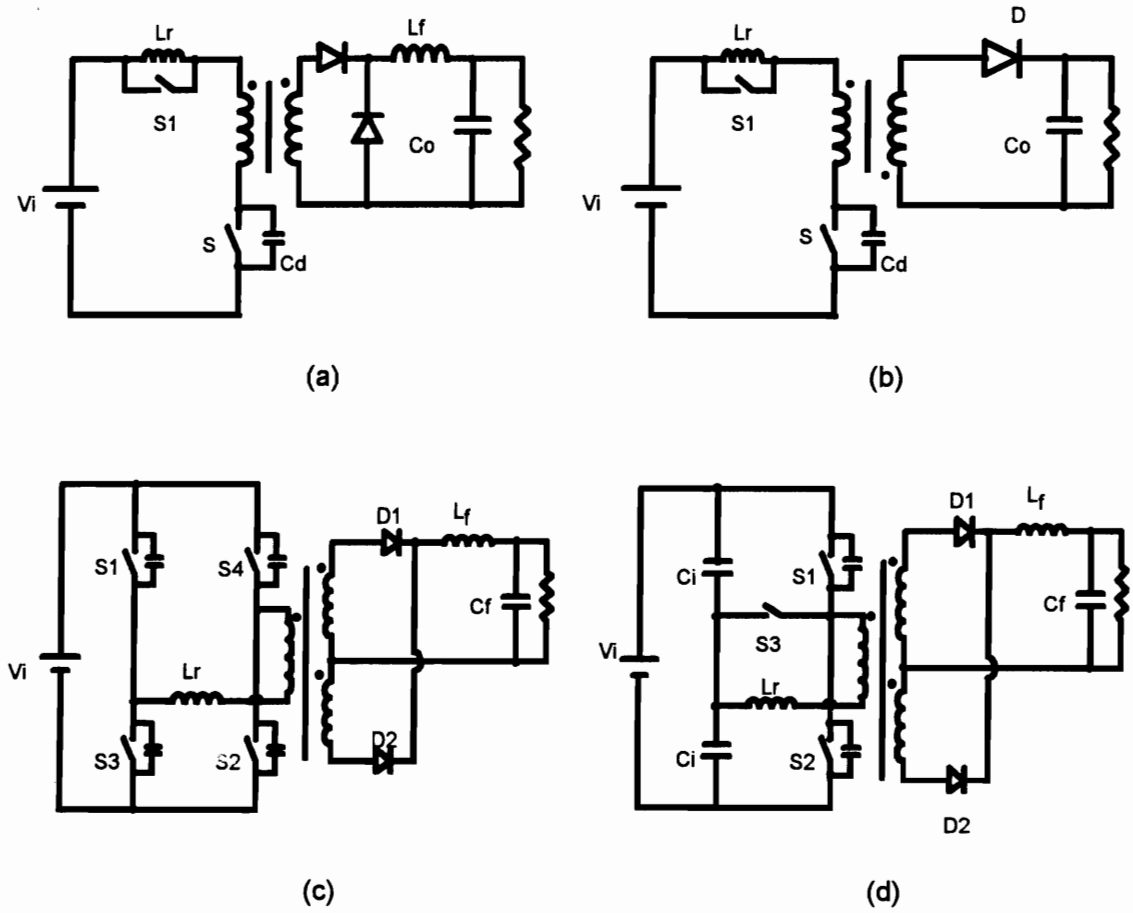


Fig. 2.5. Several topologies of the isolated ZVS-PWM converters: (a) forward, (b) flyback, (c) full-bridge, and (d) half-bridge.

Two interesting isolated topologies generated by using the ZVS-PWM switch are the full-bridge (FB) and half-bridge (HB) ZVS-PWM converters, as shown in Fig. 2.5 (c) and (d). Since the maximum voltage stress of the primary switches in these two converters is clamped to the input voltage, they are particularly useful for off-line applications.

The operation of the FB-ZVS-PWM converter is fully described in [F7]. The configuration of this converter is identical to that of the FB-ZVS-QRC. However, its operation differs from the latter by applying phase-shift control, which essentially creates an extra freewheeling operation stage during which the resonant inductor current circulates through the two upper or lower switches. During the freewheeling time, the voltage across the transformer primary or secondary is zero, and the resonant inductor current is circulating through the upper or lower half of the bridge. Thus the equivalent circuit during this operation stage is identical to that with an auxiliary switch employed cross the resonant inductor. Consequently, no auxiliary switch is needed in this particular topology.

The HB-ZVS-PWM converter combines the merits of the conventional HB-PWM converter and the HB-ZVS-QRC. The use of the auxiliary switch introduces an additional freewheeling stage within the operation of the HB-ZVS-QRC. Constant-frequency operation is achieved by controlling this freewheeling time interval. Since the transformer leakage and the output capacitances of the MOSFETs are utilized to achieve ZVS, switching losses are significantly reduced at a limited increase of conduction loss. The auxiliary switch (S3) also operates with ZVS and is subjected to a voltage stress of only half of the input voltage.

The auxiliary switch must be a bidirectional switch. It can be implemented by either two anti-paralleled MOSFETs or a bridge-type switch consisting of one MOSFET and four diodes. The HB-ZVS-PWM converter can be used for low-to-mid power conversion applications.

The operation and the key waveforms of the HB-ZVS-PWM converter are similar to those of the FB-ZVS-PWM converter. The major difference is that during the freewheeling time, the resonant inductor current in the HB converter circulates through the auxiliary switch instead of flowing through the upper or lower two switches as is the case of the phase-shift controlled FB-ZVS-PWM converter.

2.2.4 Experimental Verifications

A 1 MHz, 100 W buck ZVS-PWM converter has been breadboarded to verify the operation of the buck ZVS-PWM converter. The circuit is regulated at 24 V output with a 48 V input. Figure 2.6 shows the circuit diagram of the breadboarded converter. The FET output capacitance (Coss=650 pf at Vds=25 V) is used as the resonant capacitor (Cr). The control circuit is implemented by a PWM controller, UC 3823. It is simple compared to the control circuit of the buck ZVS-QRC. Power MOSFET S is driven by a fast driver, TSC 429.

The converter in Fig. 2.6 is designed to ensure ZVS operation above 50% load; thus the maximum voltage stress of the power switch is approximately

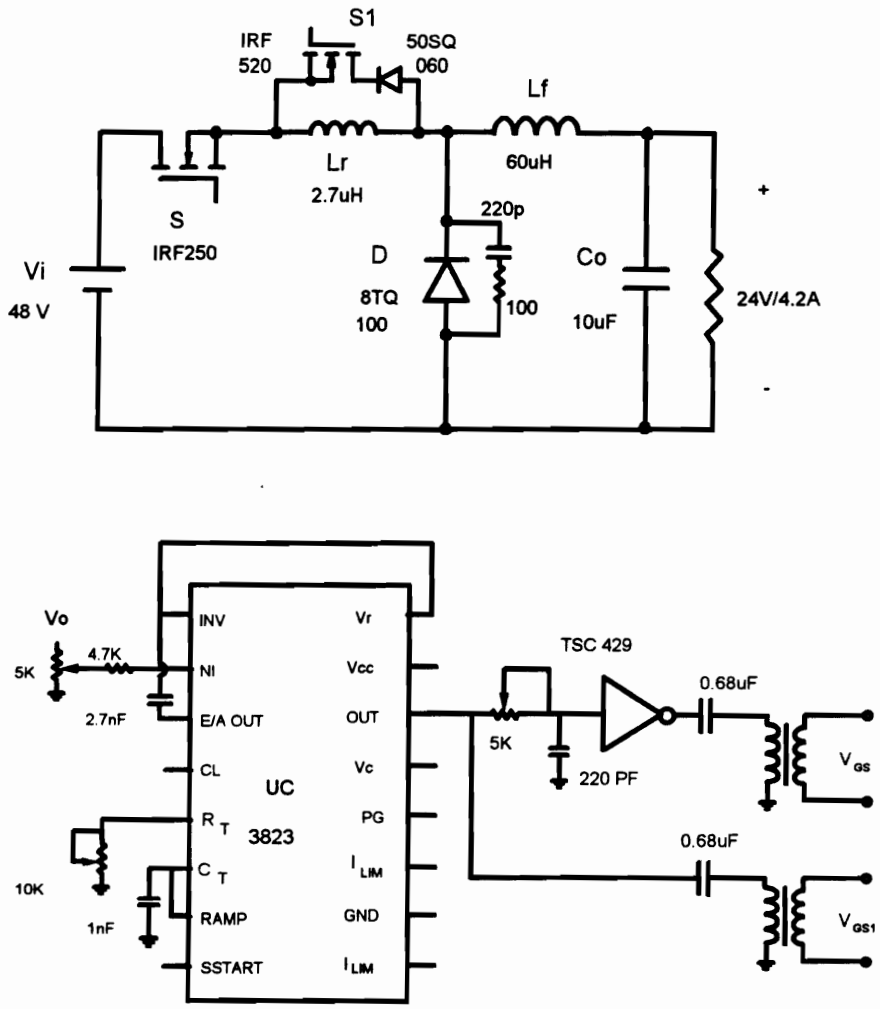


Fig. 2.6. Circuit diagram of the experimental 1 MHz, 100 W buck ZVS-PWM converter.

three times the input voltage. Figure 2.7 shows the oscillograms of the circuit operating at full load, half load, and 25% load. It can be seen that the ZVS operation is maintained at half load. At 25% load, the power switch is turned on with half of the input voltage, and ZVS is partially lost; the capacitive turn-on loss is approximately a quarter of that in a buck PWM converter. At very light load, the operation of the converter is similar to that of the buck PWM converter.

2.3 Improvement of ZVS-PWM Converters

2.3.1. ZVS-PWM Converters Using a Saturable Inductor

The power switch in single-ended ZVS-QRCs suffers from a high voltage stress which is proportional to the load range. This is one of the major limitations of the ZVS-QRC technique. In a single-ended ZVS-QRC, the voltage applied to the power switch and the resonant capacitor reaches its maximum value as the resonant inductor reaches zero current, that is, when the inductor energy is completely transferred to the resonant capacitor. Thus this maximum voltage stress is essentially determined by the energy stored in the resonant inductor.

For a linear inductor, the amount of energy stored in the inductor is $\frac{1}{2}L_r I^2$. Therefore, for a ZVS-QRC using a linear resonant inductor, the amount

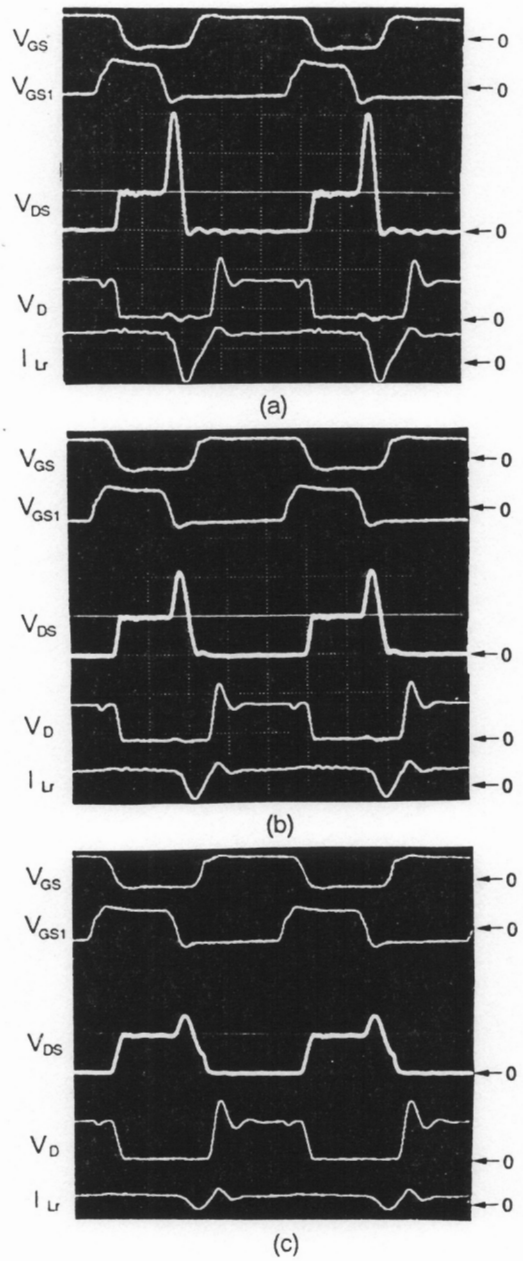


Fig. 2.7. Experimental waveforms of the buck ZVS-PWM converter at (a) full load, (b) half load, and (c) 25% load.
1st waveform: V_{GS}, 20 V/div;
2nd waveform: V_{GS1}, 20 V/div;
3rd waveform: V_{DS}, 50 V/div;
4th waveform: V_D, 50 V/div;
5th waveform: I_{Lr}, 5 A/div;
Time scale: 200 ns/div.

of energy stored in the resonant inductor depends on the load current. To achieve ZVS under a given load range, the amount of energy stored in the resonant inductor at minimum load has to be sufficient to discharge the energy stored in the resonant capacitor. As the load current increases, the inductor energy or the circulating energy increases, and the voltage stress of the power switch also increases proportionally. Therefore, the wider the load range, the higher the circulating energy, and the higher the voltage stress of the power switch.

Consider the case when a saturable inductor is used as the resonant inductor. The B-H characteristics of a saturable inductor as compared to those of a linear inductor are shown in Fig. 2.8. For an ideal saturable inductor, its inductance becomes zero when the inductor current exceeds the critical saturation current, Ic. The energy stored in an inductor is determined by the integral of the H field over the flux density, i.e.:

$$E = \int HdB \tag{2.3}$$

The maximum energy stored in a saturable inductor is $\frac{1}{2}L_{ro}I_c^2$, which is not dependent on the inductor current after it saturates. Therefore, if a saturable inductor is used in a ZVS-QRC, the maximum circulating energy will be limited by the saturation inductor energy. If the saturable inductor is designed to saturate at minimum load, the energy stored in the inductor remains constant as the load current increases (as shown in Fig. 2.8). Consequently, with a saturable inductor employed, a ZVS-QRC can achieve a much wider ZVS load range without further increasing the voltage stress of the power switch [B36].

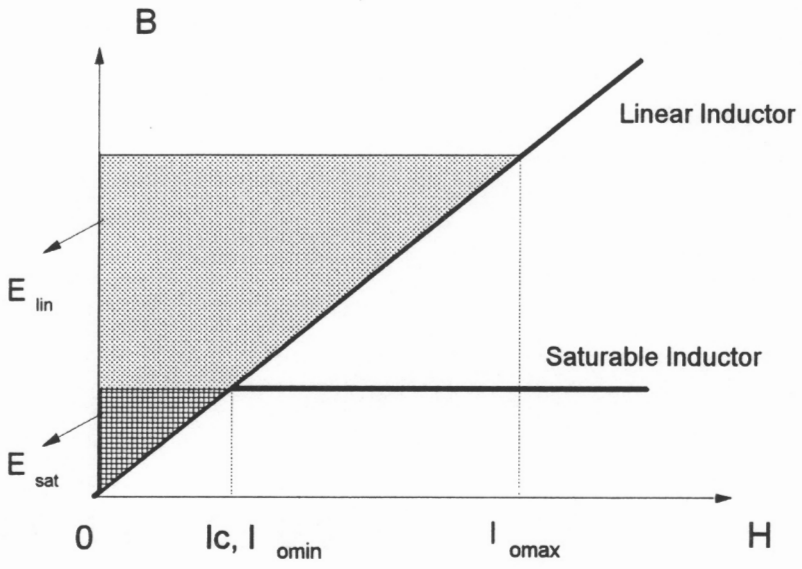


Fig. 2.8. B-H characteristics of a saturable inductor and a linear inductor.

If the linear inductor is replaced by a saturable inductor in a ZVS-PWM converter, the situation will be similar. The operation of the improved converters is illustrated by using the buck converter shown in Fig. 2.9. The operation of this circuit is slightly different from that shown in Fig. 2.2. When S is turned off at T0, the inductor current decreases very quickly, until the inductor gets out of saturation. The inductor energy ($\frac{1}{2}L_{ro}I_c^2$) remains unchanged until T2, when S1 is turned off, and the inductor L_r starts to resonate with the capacitor C_r. When the resonant inductor reaches zero current and its energy is completely transferred to C_r, the power switch reaches its maximum voltage, V_{DSMax}:

$$V_{DS}^{\max} = Vi + \sqrt{\frac{L_{ro}}{C_r}} I_c. \tag{2.4}$$

To ensure zero-voltage turn-on for the power switch at T3, the inductor energy has to be large enough to discharge C_r to zero voltage, i.e.:

$$\frac{1}{2}L_{ro}I_c^2 \geq \frac{1}{2}C_r V_i^2. \tag{2.5}$$

Equations (2.4) and (2.5) imply that to achieve ZVS, the maximum voltage stress of the power switch cannot be less than twice the input voltage. However, since the energy stored in the saturable inductor is constant, the maximum voltage stress of the power switch is load independent. Therefore, a wider ZVS load range can be achieved without increasing the voltage stress of the power switch. Theoretically, if the inductor in a buck ZVS-PWM converter is designed to have a critical current (I_c) equal to one-tenth of the maximum load current, the converter will operate with 10% load to full load ZVS range, while keeping the

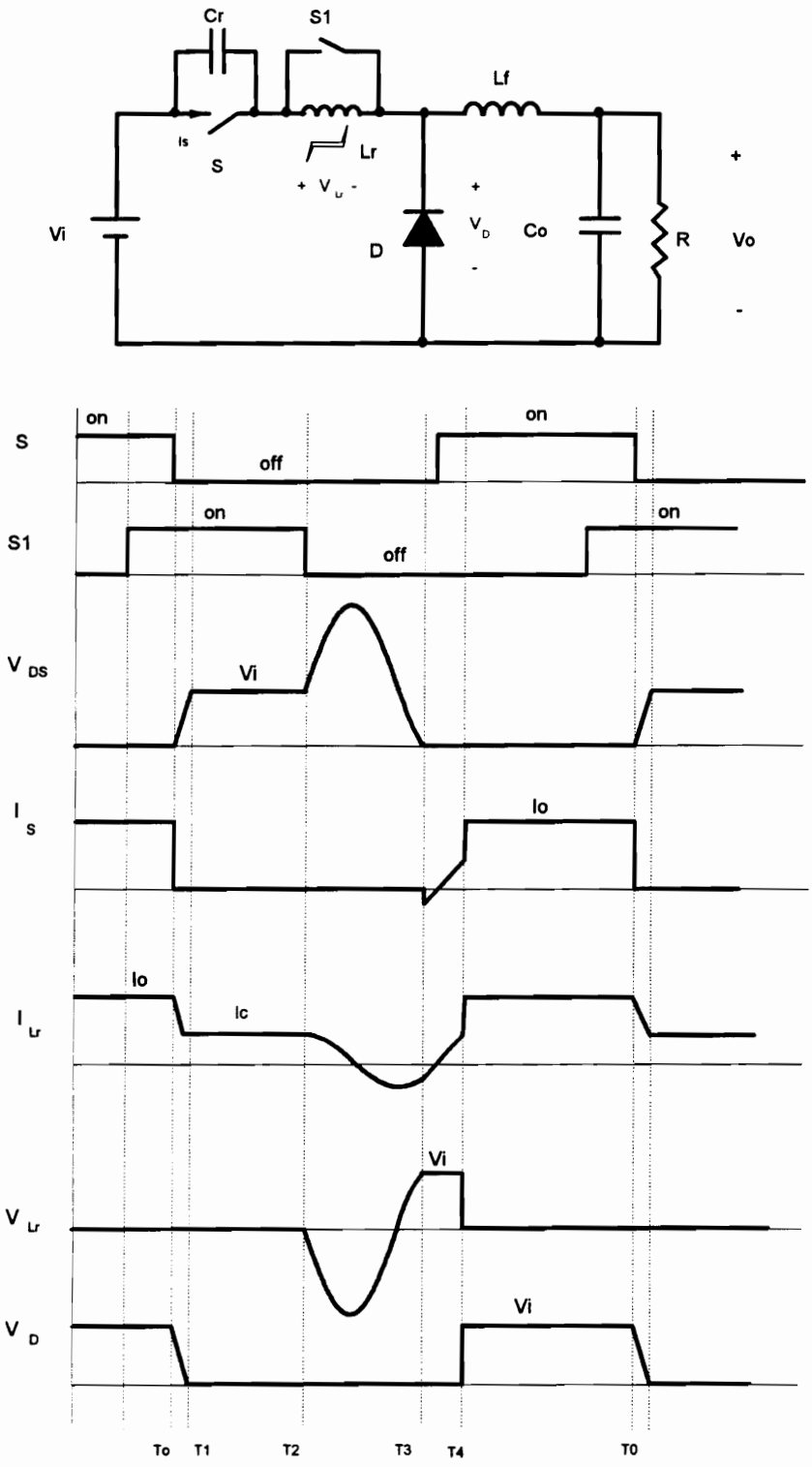


Fig. 2.9. Buck ZVS-PWM converter using a saturable resonant inductor and its key waveforms.

peak voltage stress as low as twice the input voltage.

During the time interval T3-T4, the inductor current increases linearly until it reaches Ic at T4, when the inductor saturates, and its current rises abruptly to I_O. Meanwhile, the voltage across the diode also rises abruptly to V_i, causing parasitic ringing between the diode junction capacitance and the resonant inductor. With a saturable inductor, this parasitic ringing is less severe, since the inductance is drastically reduced after the core is saturated. Another benefit of using a saturable inductor is the reduced conduction loss in S1. Due to the low conduction current (I_C) during the freewheeling time (T1-T2) when S1 is on, a small auxiliary switch can be used.

By simply replacing the resonant inductor in a ZVS-PWM converter with a saturable inductor, the improved ZVS-PWM converters are derived. Several topologies of the ZVS-PWM converters using a saturable inductor are illustrated in Fig. 2.10. The advantages of the improved converters can be summarized as follows:

- wider load range can be achieved with ZVS without increasing the circulating energy;
- the parasitic ringing between the resonant inductor and the rectifier junction capacitance is significantly reduced;
- conduction loss of the auxiliary switch is reduced.

For the single-ended topologies shown in Fig. 2.10(a)-(c), the first merit implies that the converter can achieve a wider load range with ZVS without significantly increasing the voltage stress of the active switch. For the HB or FB

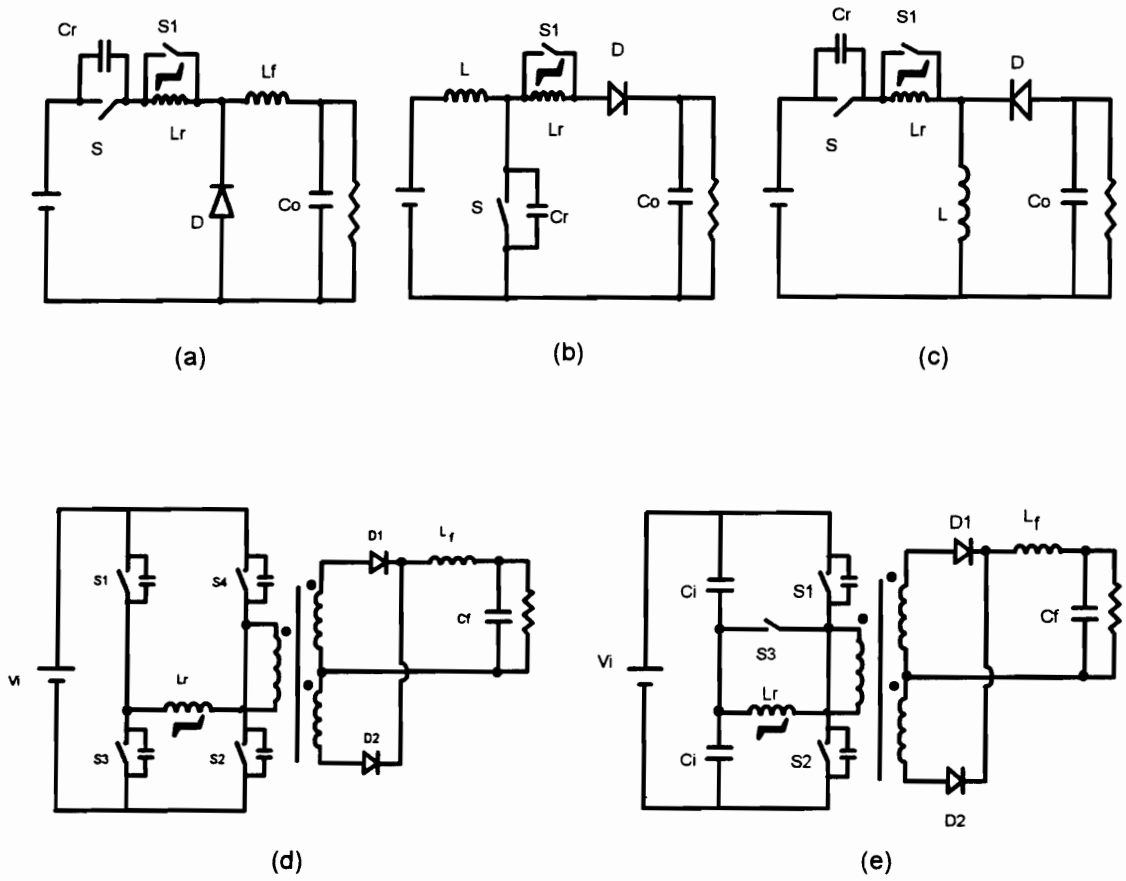


Fig. 2.10. Several topologies of the ZVS-PWM converters with a saturable inductor: (a) buck, (b) boost, (c) buckboost, (d) full-bridge, and (e) half-bridge.

topologies, however, the maximum voltage stress of the active switches is always clamped to the input voltage. In this case, the use of a saturable inductor reduces the circulating energy by increasing the effective duty cycle, which leads to a reduction in the current stress of the primary switches and in the voltage stress of the secondary rectifiers. A detailed analysis of the FB-ZVS-PWM converter using a saturable inductor will be given in the following section.

One design consideration of the ZVS-PWM converters using saturable inductors is the high core loss due to the large flux change and high-frequency operation. However, the size of the saturable core in this case is rather small, since the magnetic material with very high permeability can be employed; thus the total core loss is still limited. In practice, the thermal issue of the saturable core has to be taken into consideration.

2.3.2. FB-ZVS-PWM Converter Using a Saturable Inductor

As a particular member of the family of ZVS-PWM converters, the FB converter topology is widely used for mid- and high-power conversion since the switch voltage is clamped to input voltage. It features the benefits of both the ZVS-QRC and PWM techniques while avoiding their major drawbacks. The leakage inductance of the power transformer is utilized to achieve ZVS for the power switches. Furthermore, the converter operates with a fixed frequency, making the design optimization of the circuit easy to attain.

However, due to the requirement of a relatively large resonant inductor, the FB-ZVS-PWM converter operates with high circulating energy, which substantially increases the current stress of the primary switches, voltage stress of the rectifier diodes, and the parasitic oscillations between the resonant inductor and the diode junction capacitances. These are the major limitations of the FB-ZVS-PWM converter.

Figure 2.11 shows the circuit diagram and key waveforms of the FB-ZVS-PWM converter. Compared to its PWM counterpart, the FB-ZVS-PWM converter uses a resonant inductor (L_r) to achieve ZVS of the primary switches. The value of L_r is determined by the load and input voltage range under which ZVS is maintained. To reduce the switching losses for a wide load and input voltage range, a large resonant inductance is required. However, a large resonant inductance causes higher circulating energy that substantially increases the conduction loss. Therefore, the load current under which ZVS is maintained is relatively limited in practical circuits.

The amount of the circulating energy determines a loss of duty cycle at the secondary side, ΔD:

$$\Delta D = D - D_e, \tag{2.6}$$

where D and D_e are the duty cycles of the primary-voltage and secondary-voltage, respectively. This ΔD is caused by the finite time (T1-T2) necessary to change the direction of the primary current due to the presence of the large resonant inductor, as shown in Fig. 11. Referring to Fig. 11, ΔD can be obtained as:

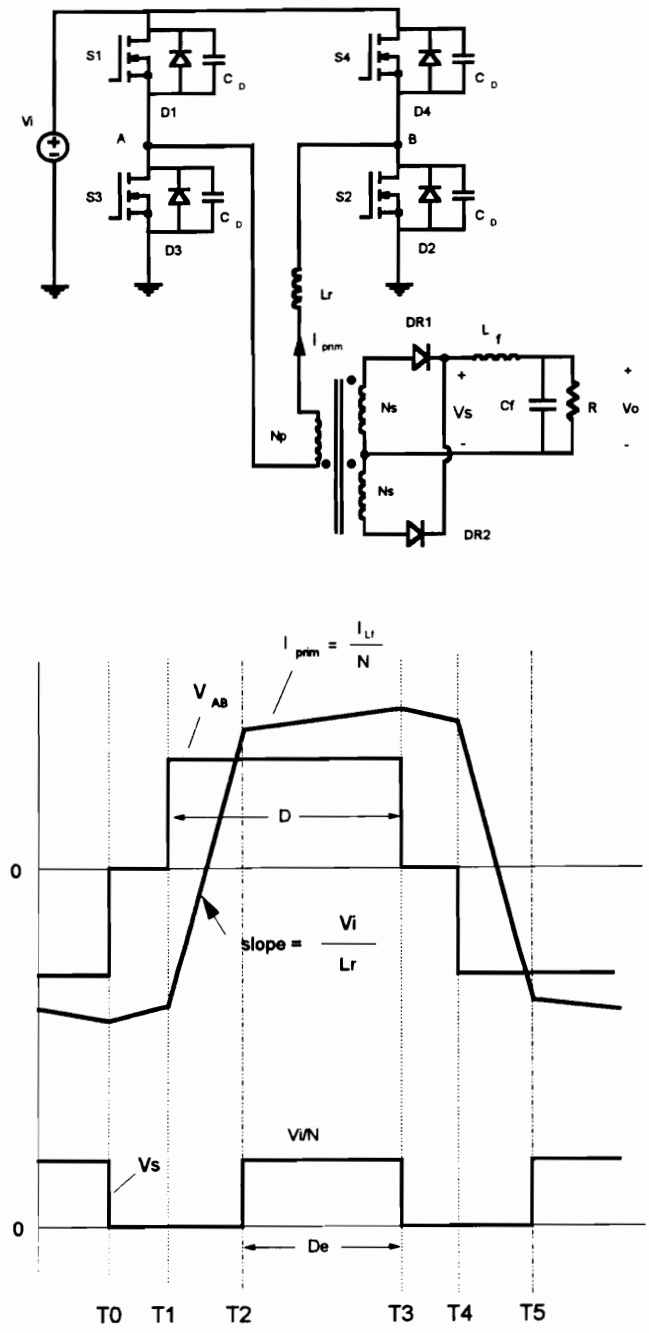


Fig. 2.11. FB-ZVS-PWM converter and its key waveforms.

$$\Delta D = \frac{2L_r f_s I_o}{NV_i}, \tag{2.7}$$

where fs=1/Ts is the PWM switching frequency of the converter, and N is the turns ratio of the transformer. Thus the output voltage of the converter can be given by:

$$V_o = \frac{DV_i}{N} - \frac{2L_r f_s I_o}{N^2}. \tag{2.8}$$

It can be seen that the output voltage of the converter is load current dependent, which is not the case for an ideal PWM converter (L_r=0). For a given duty cycle, a larger L_r value makes the output voltage more sensitive to load current variation. In a real circuit, a larger L_r value leads to a lower output voltage, which in turn requires a smaller transformer turns ratio (N) to meet line regulation. Consequently, the primary current, I_0/N, is increased, which leads to higher conduction losses. At the same time, the voltage stress of the secondary diodes, $2V_i/N$, is also increased, necessitating the use of rectifier diodes with higher voltage rating and higher forward voltage drop.

Another drawback of the FB-ZVS-PWM converter is the severe parasitic ringing between the diode junction capacitances and the resonant inductor [F12]. It is more severe than that in the FB-PWM converter since the resonant inductance in the ZVS-PWM converter is considerably larger than the transformer leakage inductance of the conventional PWM converter. The ringing frequency is:

$$f_r = \frac{N}{2\pi\sqrt{L_r C}}, \qquad (2.9)$$

where C is the equivalent capacitance of the rectifier diode and the transformer windings. For a large value of L_r, the ringing frequency is low, causing higher diode voltage stress, higher snubber loss, and higher switching noise [F10].

The above-mentioned drawbacks of the FB-ZVS-PWM converter can be alleviated by using a saturable inductor.

The circuit diagram and the key waveforms of the improved FB-ZVS-PWM converter with a saturable inductor are shown in Fig. 2.12. It should be noted that a power transformer with a minimum leakage inductance is preferred in this case. The operation of the modified circuit is slightly different from that of the previously discussed FB-ZVS-PWM converter. At time T2 or T5, the inductor current reaches its critical saturation current, I_C, and the inductor is saturated. Then the inductor current rises abruptly until it reaches the reflected filter inductor current, I_0/N; at the same time the secondary voltage also jumps to V_i/N. Consequently, the effective duty cycle of the converter is increased by ΔD_e, as shown in Fig. 2.12. Assuming an ideal saturable inductor, when switch S1 is turned off at T3, the inductor current will decrease quickly, until it reaches I_C, and the inductor gets out of saturation. Thus the switch current stress during the freewheeling stage is decreased, and the conduction loss of the primary switches is reduced.

Due to reduced loss of duty cycle, the output voltage of the converter using a saturable inductor is less sensitive to load change. Referring to Fig. 2.12, the output voltage of the converter is given by:

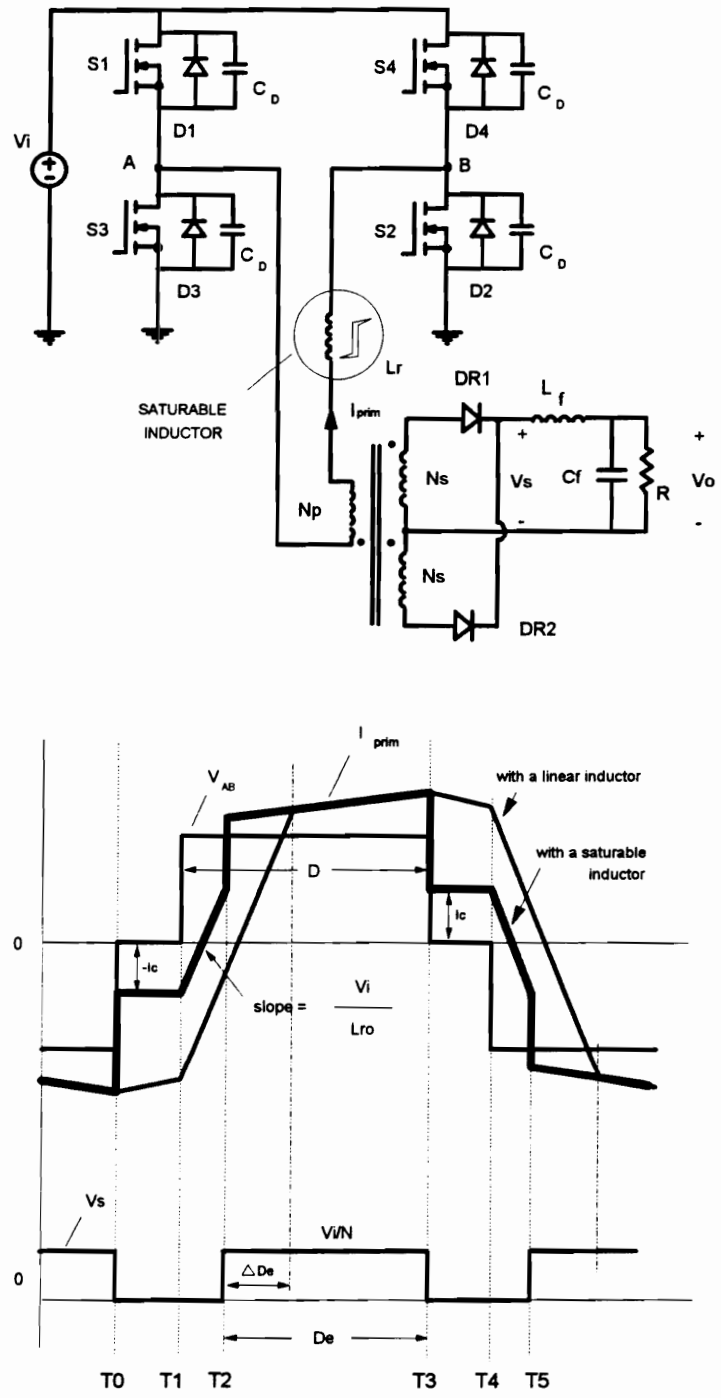


Fig. 2.12. FB-ZVS-PWM converter incorporating a saturable inductor and its key waveforms.

$$V_o = \frac{DV_i}{N} - \frac{2L_r f_r I_o}{N^2}; \quad \text{when } \frac{I_o}{N} < I_c, \tag{2.10}$$

$$V_o = \frac{DV_i}{N} - \frac{2L_r f_r I_c}{N^2}; \quad \text{when } \frac{I_o}{N} > I_c. \tag{2.11}$$

It can be seen that when the reflected output current exceeds I_C, V_O becomes load current independent. Assuming that $I_C=I_{Omax}/5N$, the typical ideal output characteristics of the FB-ZVS-PWM converters using a linear resonant inductor and a saturable resonant inductor with the same inductance are shown in Fig. 2.13. It can be seen that the output characteristics of the FB-ZVS-PWM converter using a saturable inductor are closer to those exhibited by the conventional FB-PWM converter.

Another benefit of using a saturable inductor is the reduction of parasitic oscillations between the diode junction capacitances and the resonant inductor. When a linear resonant inductor is used, the diode junction capacitances start to resonate with the inductor at the T2 and T5, when the diodes suffer from a prompt reverse voltage. The large resonant inductance produces low frequency ringing that increases rectifier voltage stress and switching noise. With a saturable inductor, this parasitic ringing is dramatically reduced, since the resonant inductor gets saturated at time T2 and T5, and its inductance is much reduced before the abrupt voltage is applied to the rectifier diodes. The much reduced inductance results in less ringing with the junction capacitances of the diodes. Since the ringing frequency is significantly higher than the switching frequency, it is easier to snubber.

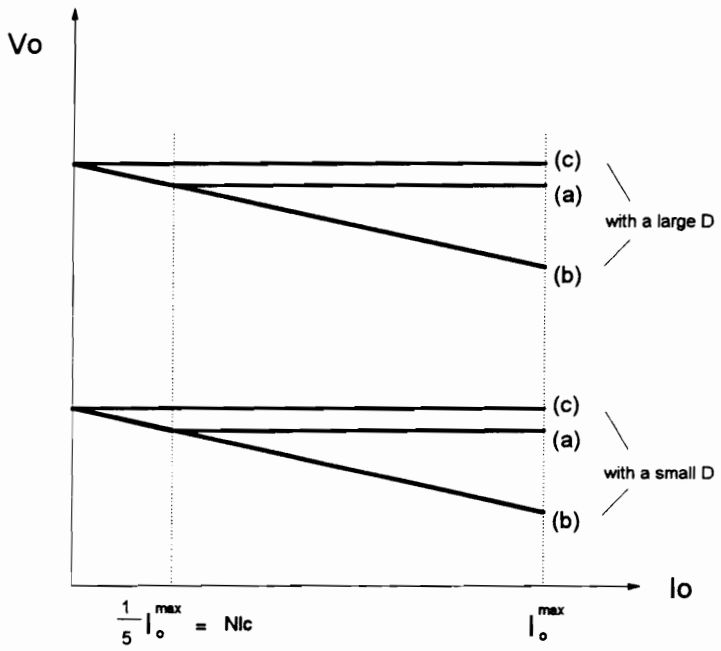


Fig. 2.13. Comparison of the typical ideal output characteristics for three cases: (a) FB-ZVS-PWM using a linear inductor; (b) FB-ZVS-PWM using a saturable inductor; and (c) Conventional FB-PWM converter.

The advantages of the FB-ZVS-PWM converter incorporating a saturable resonant inductor are summarized as following:

- reduced conduction loss of the switches due to reduced circulating energy;
- increased effective duty cycle resulting in the use of a larger transformer turns ratio to minimize the current in the primary circuit and the voltage in the secondary circuit;
- improved output characteristics;
- reduced secondary parasitic ringing and rectifier voltage stresses, so that rectifier diodes with lower voltage rating and lower forward voltage can be used; and
- wider load range which can be achieved with ZVS without increasing the circulating energy.

The size of the saturable inductor is quite small, since magnetic material with very high permeability can be employed. Nevertheless, due to a large flux change in the core (from negative saturation area to positive saturation area), the switching frequency range of the converter might be limited to several hundred kHz, which is mainly determined by the thermal tolerance of the core material.

Another way to implement the proposed scheme is to move the resonant inductor from the primary to the secondary, as shown in Fig. 2.14(a). The operation of this converter is similar to that of the FB-ZVS-PWM converter with the saturable inductor in the primary, since the secondary inductor can be reflected to primary during each operation stage. It also works for the circuit with an FB rectifier, as shown in Fig. 2.14(b). However, the flux in L_{r1} or L_{r2} only

operates in the first quadrant instead of traveling from negative saturation to positive saturation as was the case in the circuit shown in Fig. 2.12; thus the core loss is significantly reduced compared to the circuit operating at the same switching frequency in Fig. 2.12.

2.3.3. Experimental Verifications

A 500 kHz, 100 W buck ZVS-PWM converter using a saturable inductor is implemented to verify the theoretical analysis. The circuit diagram of the breadboarded converter is the same as that in Fig. 2.6, except that the resonant inductor is replaced by a saturable reactor, which is implemented with six turns on a small H7F-ER-9.5/5-Z core.

Figure 2.15 shows the oscillograms of the buck ZVS-PWM converter using a saturable inductor. It can be seen that ZVS is maintained at 15% load. Compared to the buck ZVS-PWM converter operating at the same input and output conditions, this converter achieved a much wider ZVS load range. The incorporation of the saturable inductor extends the ZVS load range from 50% load to 15% load without increasing the voltage stress of the power switch.

Another 500 kHz, 200 W FB-ZVS-PWM converter using a saturable inductor is also implemented to demonstrate the feasibility of the improved ZVS-PWM converter technique. It is regulated at 5 V output with a 250-350 V input and a 0-40 A load range. The power stage in Fig. 2.12 consists of the following components:

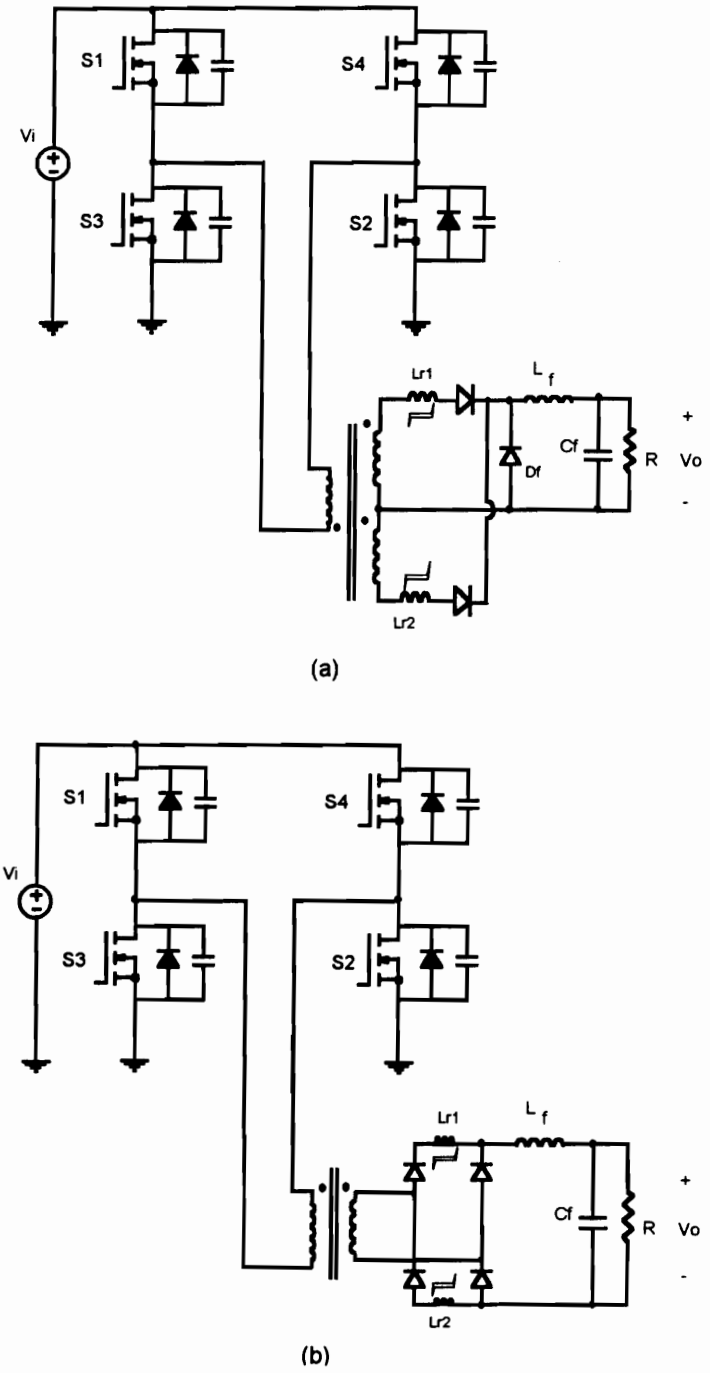


Fig. 2.14. FB-ZVS-PWM converter using the saturable inductors at the secondary with: (a) a half-bridge rectifier, and (b) a full-bridge rectifier.

S1-S4 - IRF740 (International Rectifier);

DR1,2 - 60CNQ030 (International Rectifier);

L_f - core: H7C4-RM7Z52B, 5.5 turns;

L_r - core: H7F-ER9.5/5Z, 6 turns;

TR - core: half 3F3-782E272 (Philips);

primary: 58 turns of 100/44 Litz wire;

secondary: 2 turns, center tapped, 3 mil Cu foil;

C_{in} - 0.33 uF / 400 V metal polypropleme;

C_f - 4 X 15 uF tantalum & 3 X 0.33 uF ceramic.

The transformer turns ratio was designed at N_p/N_s=29 to get 5 V/40 A output with a 0.9 duty cycle at 250 V input. The saturable inductor is implemented with six turns on a small ungapped H7F-ER-9.5/5-Z core. Figure 2.16(a) shows the experimental waveforms of the FB-ZVS-PWM converter using the saturable resonant inductor on the primary side. If a linear resonant inductor were used, the transformer turns ratio would have to be reduced to N_p/N_s=24 to get the same output under the same input and duty cycle conditions. This reduction would result in a significant increase in the primary conduction loss (about 40%) and rectifier voltage stresses (shown in Fig. 2.16(b)). The increased rectifier voltage stress necessitates the use of a Schottky diode with a higher voltage rating (45 V instead of 35 V) and a higher forward voltage drop. Here both circuits are designed to maintain zero-voltage switching above 65% load at nominal line (V_i=300 V). In addition, the secondary parasitic ringing in the circuit with a saturable inductor is much less than that occurring in a circuit with a linear inductor, as can be seen from Fig. 2.16.

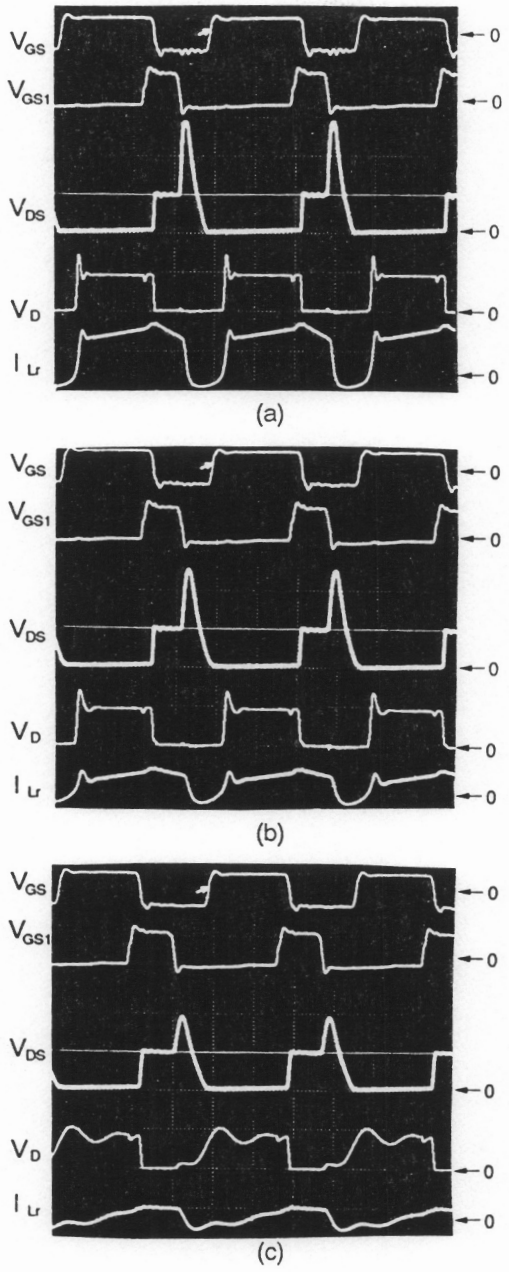


Fig. 2.15. Experimental waveforms of the buck ZVS-PWM converter using a saturable inductor at (a) full load, (b) half load, and (c) 15% load.
1st waveform: V_{GS}, 20 V/div;
2nd waveform: V_{GS1}, 20 V/div;
3rd waveform: V_{DS}, 50 V/div;
4th waveform: V_D, 50 V/div;
5th waveform: I_{Lr}, 5 A/div;
Time scale: 500 ns/div.

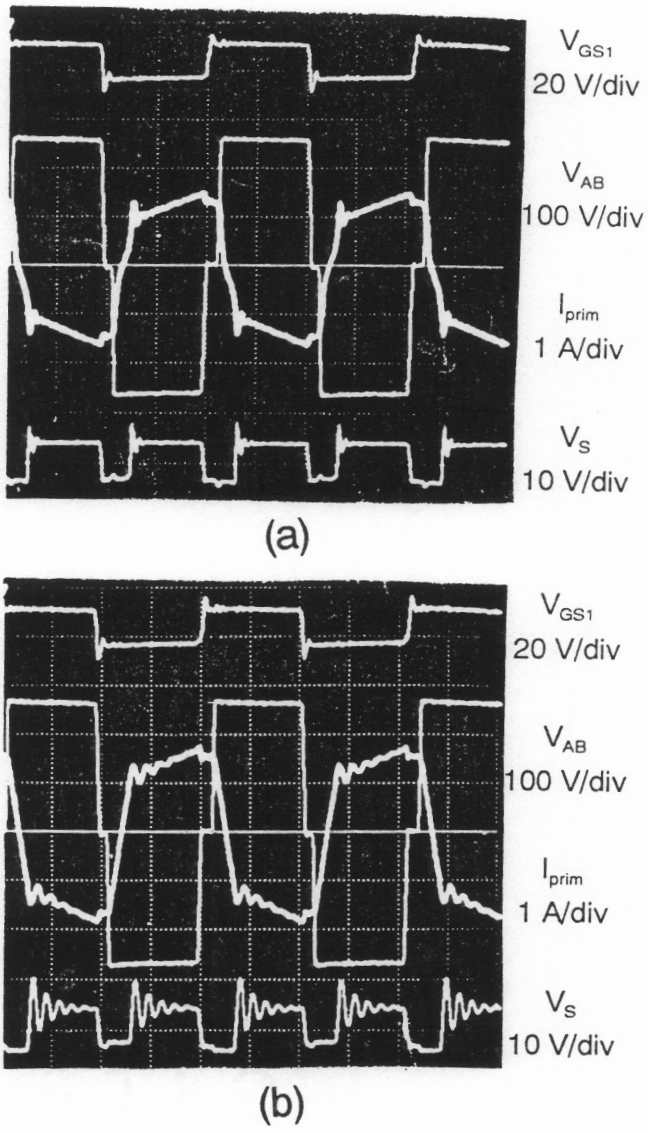


Fig. 2.16. Experimental waveforms of the 500 kHz, 200 W FB-ZVS-PWM converter with:
(a) a saturable resonant inductor, and
(b) a linear resonant inductor
at V_i=250 V and D=0.9.

To reduce core loss of the saturable reactor and to further extend the load range for zero-voltage switching, another design was attempted with the saturable inductors in the secondary. The converter was designed to maintain ZVS above 45% load at 300 V input. Each saturable inductor was implemented with 1.5 turns on half H7F-ER-9.5/5-Z core. Figure 2.17 gives the overall efficiency of the breadboarded converter. Due to reduced saturable core loss, this circuit has higher efficiency (about 0.7%) than that with the saturable inductor in the primary. Including the control circuit and driver losses, a maximum overall efficiency of 87.8% is achieved. Table 2.1 gives the estimated loss breakdown of the three converters at full load and 300 V input.

2.4 Summary

Switching losses, stresses, and noise due to parasitic oscillations are inherent in the PWM technique, and these limitations have restricted the PWM converters from operating at higher frequencies for size/weight reduction and for performance improvement. Although the ZVS-QRC technique has eliminated most of the switching losses and parasitic oscillations associated with the power switch(es), it imposes additional constraints on the power converter circuits, such as high voltage stresses, limited load range, and variable frequency operation. This chapter presents a novel circuit configuration which combines the merits of the PWM and ZVS-QRC techniques. Employing an auxiliary switch

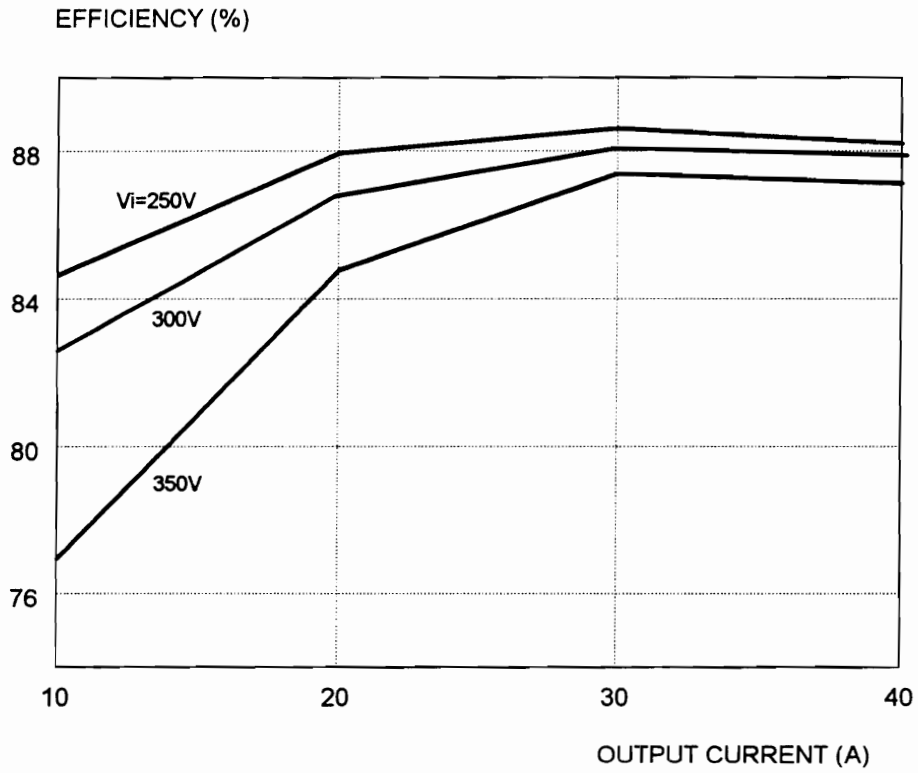


Fig. 2.17. Overall efficiency of the 500 kHz, 200 W FB-ZVS-PWM converter with the saturable inductors in the secondary.

Table 2.1. Loss breakdown at full load and 300 V input.

	Case 1	Case 2	Case 3
Component Losses	Linear inductor	Saturable inductor at the primary	Saturable inductor at the secondary
S1-S4 cond.	3.9 W	2.7 W	2.7 W
D1, D2 cond.	17.6 W	15.2 W	15.2 W
Transformer	3.4 W	3.4 W	3.4 W
Resonant inductor	0.6 W	3.3 W	1.6 W
Diode snubber	1.8 w	0.9 W	0.7 W
Control	1.8 W	1.8 W	1.8 W
Filters	1.8 w	1.8 w	1.8 W
Others	0.5 W	0.5 W	0.5 W
Total	31.4 W	29.6 W	27.7 W
Efficiency	86.4%	87.1%	87.8%

across the resonant inductor of a ZVS-QRC, it creates a freewheeling stage within the quasi-resonant operation. The advantages of this additional freewheeling stage are two-fold. First, it enables constant-frequency operation by controlling the time interval of this freewheeling stage. Second, the freewheeling stage can occupy a substantial portion of a cycle so that the proposed circuit resembles that of a conventional PWM converter. Resonant operation takes place only during a small portion of a cycle and is used only to create a ZVS condition for the power switch. In this way, the circulating energy required for ZVS-QRC operation can be significantly reduced. To further enhance the circuit capability of handling a wide load range, a saturable inductor is employed to replace the linear resonant inductor.

The detailed operation of the new converters is discussed by using the buck ZVS-PWM converter and the FB-ZVS-PWM converter as examples. A prototype 1 MHz, 100 W buck ZVS-PWM converter, and a 500 kHz, 100 W buck ZVS-PWM converter employing a saturable inductor are breadboarded to demonstrate the operation of the proposed converters. It is shown that the use of a saturable inductor extends the ZVS range from 50% to 15% load, while limiting the switch voltage stress close to three times the input voltage. In addition, another 500 kHz, 200 W FB-ZVS-PWM converter using a saturable inductor was also implemented to demonstrate the feasibility of the new technique.

The proposed technology can be considered an extension of the ZVS-QRC technique. Among the large family of the ZVS-PWM converters, the FB-ZVS-PWM converter and the HB-ZVS-PWM converter are deemed most attractive for practical applications, since the power switches are subjected to minimum voltage stress the same as those in their PWM counterparts.

CHAPTER 3

ZERO-CURRENT SWITCHING PWM CONVERTERS

3.1 Introduction

Due to continuous improvement of switching characteristics, lower conduction losses, and lower cost, IGBTs are gaining wide acceptance in switched-mode power converters/inverters. Since IGBT is a minority-carrier device, it exhibits a current tail at turn-off, which causes considerably high turn-off switching losses. To operate IGBTs at relatively high switching frequencies, either the ZVS or the ZCS technique can be employed to reduce switching losses. Basically, the ZVS eliminates the capacitive turn-on loss and reduces the turn-off switching loss by slowing down the voltage rise and thereby reducing the overlap between the switch voltage and the switch current. This technique can be effective when applied to a fast IGBT with a relatively small current tail.

For slow IGBTs, however, a large external resonant capacitor is required to reduce the turn-off switching loss effectively. But this may not be tolerable from the circuit point of view because of topology and design constraints. The ZCS technique eliminates the voltage and current overlap by forcing the switch current to zero before the switch voltage rises. Thus ZCS is deemed more effective than ZVS in reducing IGBT switching losses, particularly for slow devices.

Compared to the ZVS converter topologies, the ZCS converter topologies are less mature. For high-frequency power conversion, the ZCS-QRC technique is most frequently used. This technique offers ZCS for the power transistor and ZVS for the rectifier diode. The diode junction capacitance and the transformer leakage inductance are utilized to achieve soft-switching.

One of the major limitations of the ZCS-QRC technique is high circulating energy caused by the resonant inductor which is in series with the power transistor. As a result, the power switch suffers from a high current stress, and the rectifier from a high voltage stress. The second limitation is severe parasitic ringing on the power switch. Since the output capacitance of the power switch is not utilized, it oscillates with the resonant inductor when the switch is turned off. This low frequency parasitic ringing not only causes significant switching loss and noise, but also increases the voltage stress of the power switch. The third limitation of the ZCS-QRC technique is capacitive turn-on loss and noise of the power switch. The capacitive turn-on loss problem may not be severe for power converters using IGBTs or BJTs, since these devices have relatively low output capacitance, and the operating frequency is also relatively low. For high-

frequency power conversion in which power MOSFETs are used as the power switch, however, this capacitive turn-on loss can be significant. Another limitation is variable frequency operation, since the ZCS-QRCs operate with constant on-time control.

This chapter presents a family of ZCS-PWM converters. Employing an auxiliary switch in series with the resonant capacitor in a ZCS-QRC allows the new converter to operate with constant frequency and much reduced circulating energy. The ZCS-PWM converters can also be derived by simply applying circuit duality to the ZVS-PWM converters. The ZCS-PWM technique is an extension of the ZCS-QRC technique.

3.2. A Family of ZCS-PWM Converters

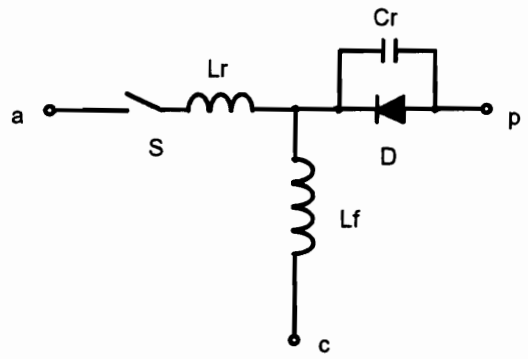
3.2.1. ZCS-PWM Switch

Figure 3.1(a) shows the basic configuration of the ZCS quasi-resonant switching cell, where L_r and C_r are the resonant inductor and resonant capacitor, respectively [F39]. In the ZCS quasi-resonant switching cell, the resonant inductor begins to oscillate with the resonant capacitor when the power switch is turned on. The power switch is turned off with ZCS after the resonance brings switch current to zero. To achieve ZCS for the power switch, the on-time

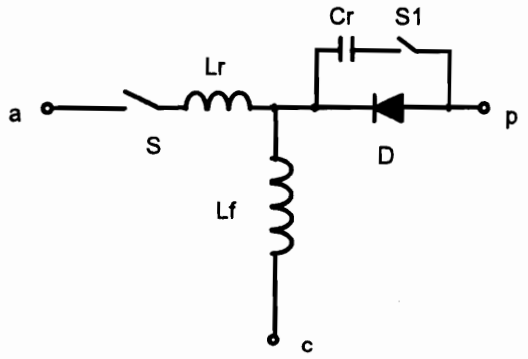
of the power switch, which is determined by the resonant period of the resonant tank, is fixed. The output voltage is regulated by varying the off-time of the switch. Thus a ZCS-QRC operates with constant on-time control. Consequently, a ZCS-QRC operating with a wide input voltage or load range has a wide frequency range.

By inserting an auxiliary switch (S1) in series with the resonant capacitor, the ZCS-PWM switching cell shown in Fig 3.1(b) is obtained. In the ZCS-PWM switching cell, S1 is off when the power switch is turned on. The resonance between L_r and C_r does not occur until S1 is turned on. When S1 is turned on, L_r starts to resonate with C_r. After the resonance brings the L_r current to zero, S is turned off with ZCS. Therefore, the function of S1 is to hold off the resonance for a period of time. By controlling this hold-off time period, the on-time of the power switch can be varied, enabling the ZCS-PWM converters to regulate the output while operating at a fixed switching frequency.

In principle, the power switch in Fig. 3.1 can be implemented with either a half-wave or a full-wave switch [B5, B6]. Since all the ZCS-PWM converters can be operated with fixed-frequency, different implementation of the power switch does not significantly affect the basic characteristics of the converter. In practice, since the implementation of the half-wave switch requires the use of a diode in series with the power transistor, it will increase the conduction loss of the converter. To simplify the analysis, only the full-wave version is discussed in the following.



(a)



(b)

Fig. 3.1. (a) ZCS quasi-resonant switching cell, and (b) ZCS-PWM switching cell.

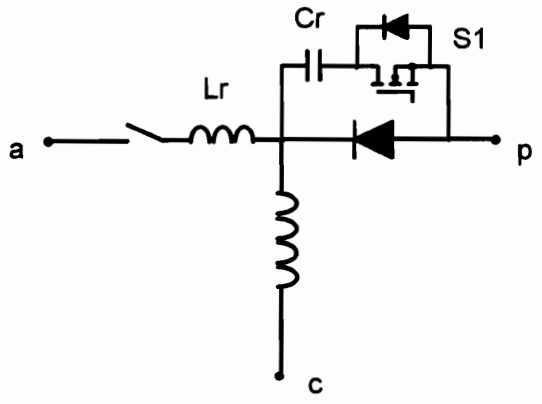
For each ZCS-PWM converter, the auxiliary switch can be implemented in two ways, as shown in 3.2. With different implementation, both the operation and the performance of a ZCS-PWM converter are slightly different. In the following section, the buck ZCS-PWM converter is used as an example to introduce the principle of operation of the ZCS-PWM converters.

3.2.2 Buck ZCS-PWM Converter

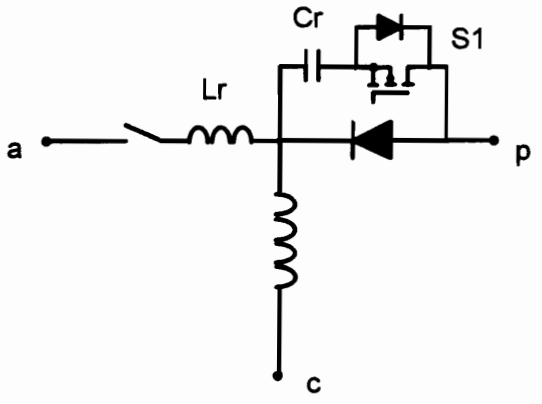
3.2.2.1. Buck ZCS-PWM Converter (I)

Figure 3.3 shows the circuit schematic and the waveforms of the ZCS-PWM buck converter (I). This converter can be derived by replacing the PWM switching cell of the buck converter with the ZCS-PWM switching cell shown in Fig. 3.2(a). This converter differs from the buck ZCS-QRC by the introduction of an auxiliary switch which is in series with the resonant capacitor. To simplify the analysis, the input filter inductor and the output filter capacitor are assumed to be sufficiently large to be considered a dc current source (I_i) and a voltage source (V_o), respectively. As shown in Fig. 3.4, this converter has five topological stages in steady-state operation:

(a) T0-T1: Before time T0, the power switch (S) is off, and the rectifier diode is conducting. At time T0, S is turned on. The resonant inductor current increases linearly until it reaches I_o at T1. Meanwhile, the current through



(a)



(b)

Fig. 3.2. Two ZCS-PWM switching cells with different implementation of the auxiliary switch.

the freewheeling diode D decreases at a rate of V_i/L_r. This time interval is given by:

$$\Delta T_{01} = \frac{I_o L_r}{V_i}. \tag{3.1}$$

(b) T1-T2: At time T1, the current through the rectifier diode reduces to zero and the diode is turned off with ZCS. Since the auxiliary switch (S1) is off, no resonance occurs between L_r and C_r. This operating stage is equivalent to the transistor on stage of the PWM buck converter.

(c) T2-T3: S1 is turned on at T2, initiating the resonance between L_r and C_r. This resonance first introduces a positive current peaking on the power switch. During this time, the L_r current or the S current is:

$$I_{Lr} = I_o + \frac{V_i}{Z_n} \sin\left(\frac{1}{2\pi\sqrt{L_r C_r}} t\right), \tag{3.2}$$

where $Z_n = \sqrt{L_r/C_r}$ is the characteristic impedance of the resonant tank. After a quarter of the resonant period, the power switch current reaches its peak value, I_S^{peak}:

$$I_S^{peak} = I_o + \frac{V_i}{Z_n}. \tag{3.3}$$

At the end of this time interval, the current through S1 starts to reverse. This time period is a constant:

$$\Delta T_{23} = \pi\sqrt{L_r C_r}. \tag{3.4}$$

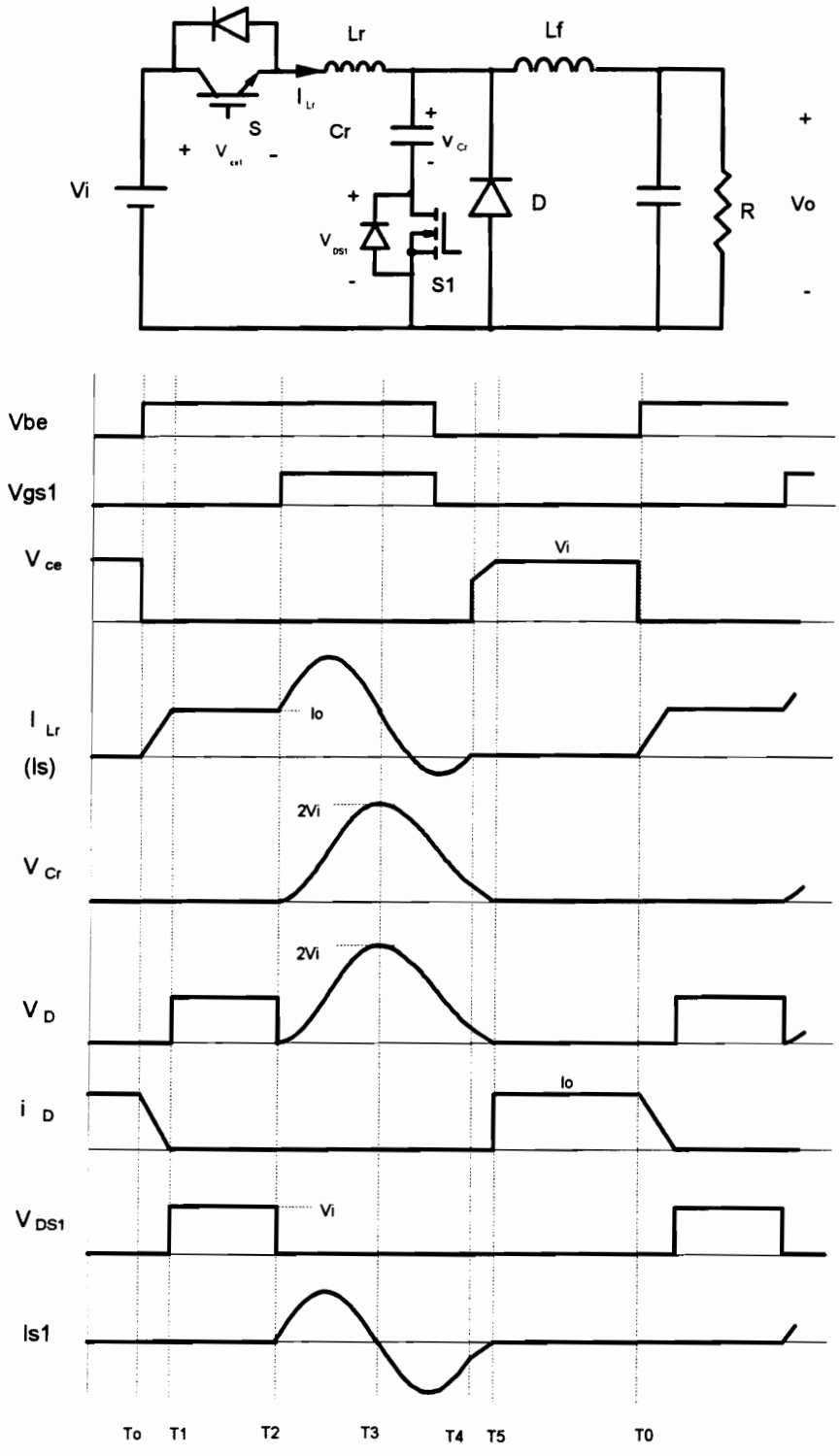


Fig. 3.3. Buck ZCS-PWM converter and its waveforms.

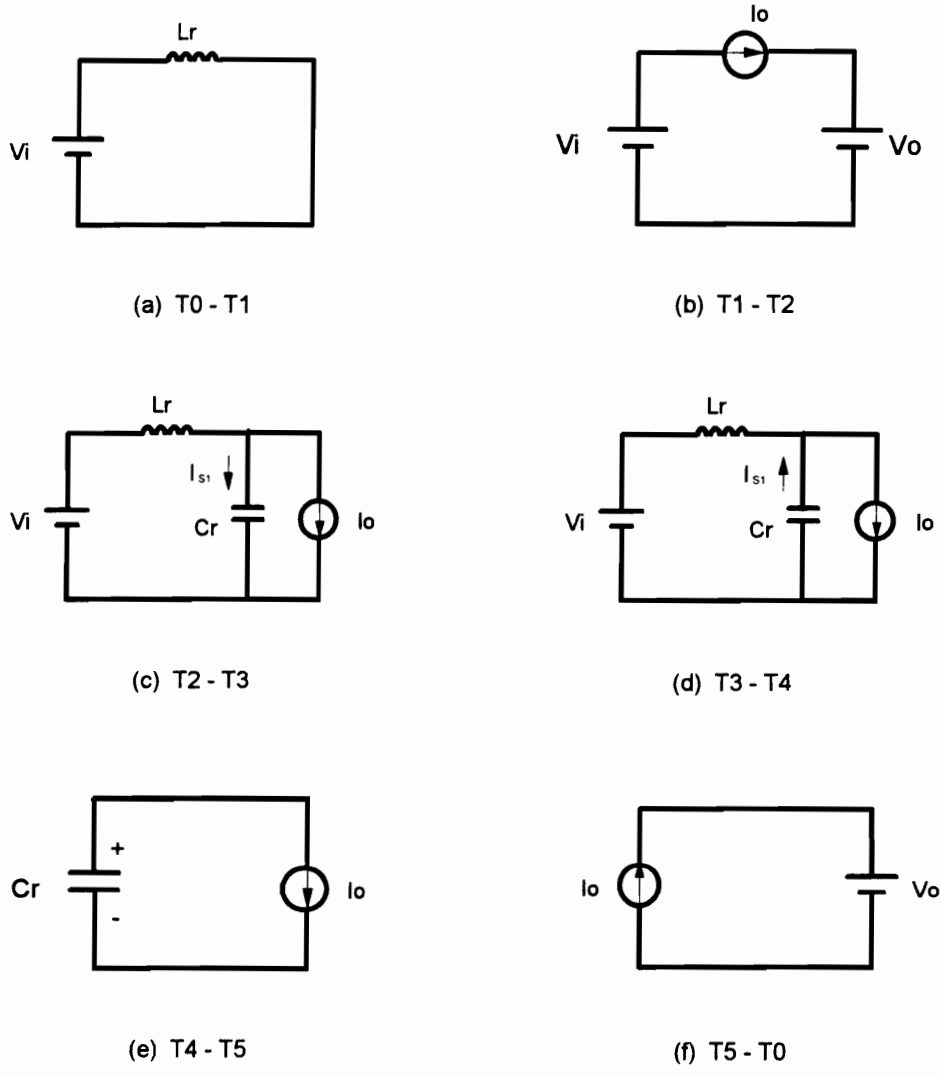


Fig.3.4. Equivalent circuits for different operating modes of the buck ZCS-PWM converter.

(d) T3-T4: L_r and C_r continue to resonate, and the anti-parallel diode of S1 is in conduction during this time interval. During this time, the L_r current is given by:

$$I_{Lr} = I_o - \frac{V_i}{Z_n}\sin\left(\frac{1}{2\pi\sqrt{L_r C_r}}t\right). \tag{3.5}$$

After one quarter of the resonant period, this resonance will bring the L_r current to a negative peak value if:

$$\frac{V_i}{Z_n} > I_0, \tag{3.6}$$

At this moment, the gate-drive signals for S and S1 can be disabled at the same time, so both S and S1 are turned off with ZCS. It can be seen that the worst operating condition occurs at full load and low line. The resonant inductor current flows through the anti-parallel diode of S when it goes negative. This interval lasts until T3, when the current through the anti-parallel diode of S decays to zero and is turned off. This operating stage is topologically identical to the previous one.

(e) T4-T5: At T4, C_r is still biased with certain voltage. During this time interval, C_r is quickly discharged by current I_O.

(f) T5-T0: C_r is discharged to zero voltage at T4. The L_f current freewheels through D during this time interval. This operating stage is identical to the freewheeling stage of the PWM buck converter. This interval lasts until T0, when S is turned off, and the switching cycle is repeated.

From the above description, it can be seen that the operation of the ZCS-PWM buck converter differs from that of the buck ZCS-QRC by possessing an extra operating stage, (T1-T2). This operating stage is identical to the transistor on stage of the PWM buck converter. Due to the presence of this operating stage, the on-time of the power switch does not need to be fixed. Therefore, constant-frequency operation can be achieved by controlling this time interval (T1-T2). Furthermore, the resonant interval (T2-T4) can occupy a small portion of the switching period. In this way, the operation of the proposed circuit is similar to that of the conventional PWM converter during most portions of a switching cycle.

Compared to a ZCS-QRC, the size of the resonant components becomes much smaller, and the circulating energy of the circuit is significantly reduced. In addition, due to much reduced resonant inductance, the parasitic ringing between the output capacitance of the power transistor and the resonant inductor becomes less significant.

3.2.2.2. Buck ZCS-PWM Converter (II)

It is interesting to note that a constant-frequency buck ZCS-QRC was proposed by Barbi in [F6]. The circuit diagram and waveforms of the constant-frequency buck ZCS-QRC are given in Fig. 3.5. In fact, this constant-frequency buck ZCS-QRC, which is referred to as the buck ZCS-PWM converter (II), can be derived by replacing the PWM switch of the buck converter with the ZCS-PWM switching shown in Fig. 3.2(b). Both the operation and the characteristics

of this converter are similar to those of the buck ZCS-PWM converter (I) described above. By comparing the two converter topologies, it can be seen that the auxiliary switches are implemented differently. As a result, the circuit operations are also slightly different. Specifically, the sequences of second and third operating stages in the two converters are reversed. Due to slightly different implementations and operations, the performances of these two converters are also slightly different from each other:

- In terms of control, converter (I) is preferred since it requires a simpler control circuit. First, the auxiliary switch in converter (I) does not require a floating driver. Second, the gate-drive signal of the auxiliary switch is easier to generate, since both the power switch and the auxiliary switch in converter (I) can be turned-off at the same time.
- In terms of switching condition of the auxiliary switch, converter (I) is preferred. From the circuit waveforms, it can be seen that the anti-parallel diode of the auxiliary switch in converter (I) is turned off with both ZCS and ZVS. In converter (II), however, it is turned-off only with ZCS. If the anti-parallel diode of the auxiliary switch is slow (e.g., when using a MOSFET), it will suffer from a reverse-recovery problem. In this case, a series blocking diode and a fast anti-parallel diode will be required to prevent conduction of the slow body diode.

- In terms of the switching condition of the rectifier diode, converter (II) is preferred. Since the rectifier diode in converter (I) is turned off with ZCS only, and the diode in converter (II) is turned off with both ZCS and ZVS, a relatively slow diode can be used in converter (II).

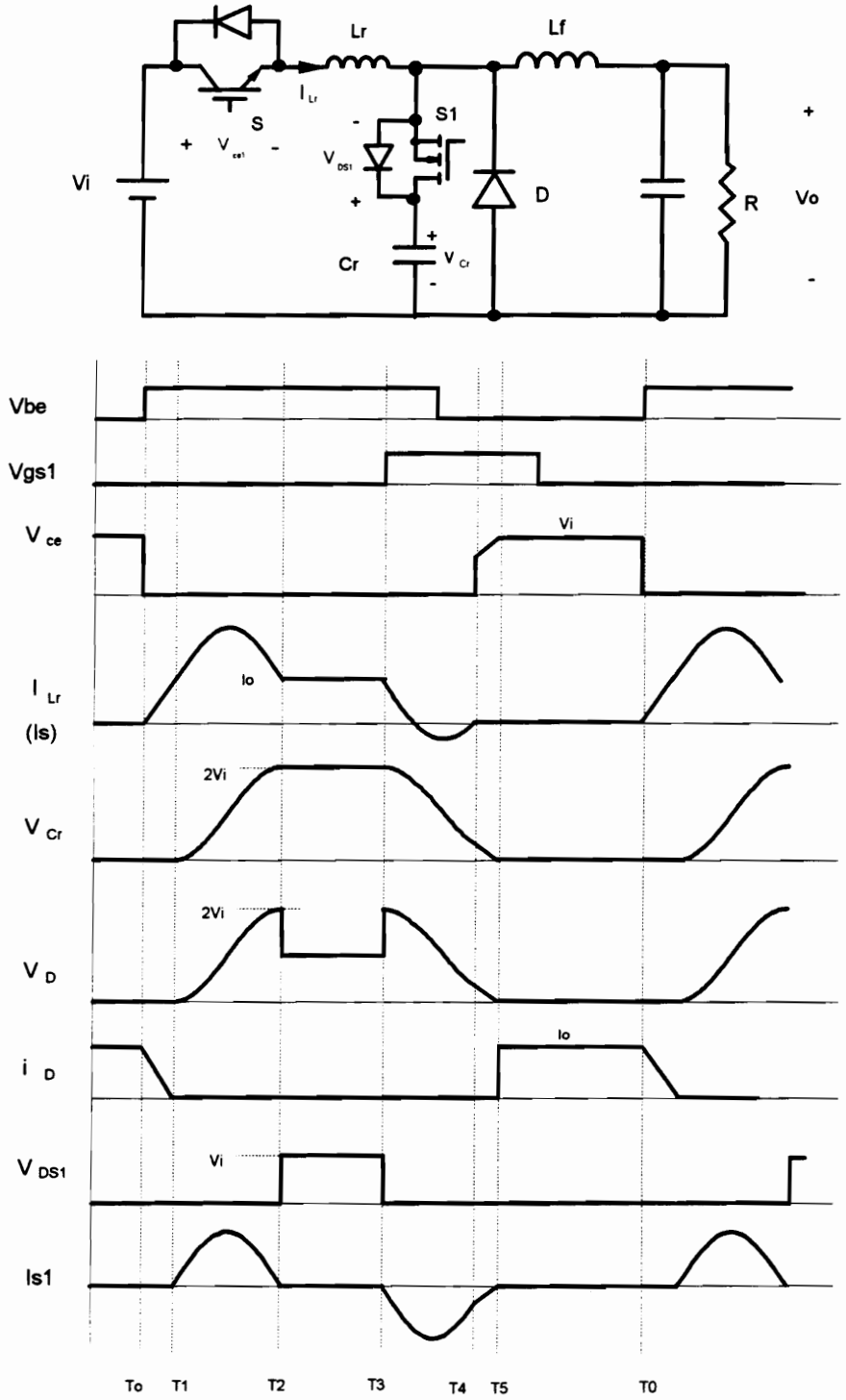


Fig. 3.5. Circuit diagram and key waveforms of the constant-frequency buck ZCS-QRC proposed by Barbi.

Besides, from the circuit waveforms it can be seen that the buck ZCS-PWM converter (I) is dual to the ZVS-PWM boost converter introduced in Chapter 2.

3.2.3. A Family of ZCS-PWM Converters

Simply by inserting an auxiliary switch in series with the resonant capacitor in the ZCS-QRC topologies, or by applying circuit duality to the ZVS-PWM converters, a family of ZCS-PWM converters are derived. Figure 3.6 shows six basic ZCS-PWM topologies. Figure 3.7 shows several isolated ZCS-PWM topologies.

The features of the ZCS-PWM converters are summarized below.

Merits:

- ZCS for both the power transistor and the auxiliary switch,
- ZCS for the rectifier diode;
- much reduced circulating as compared to the ZCS-QRCs;
- constant-frequency operation.

Limitations:

- high voltage stress of the rectifier diode;

  The rectifier diode experiences a voltage stress twice as high as that in its PWM counterpart;

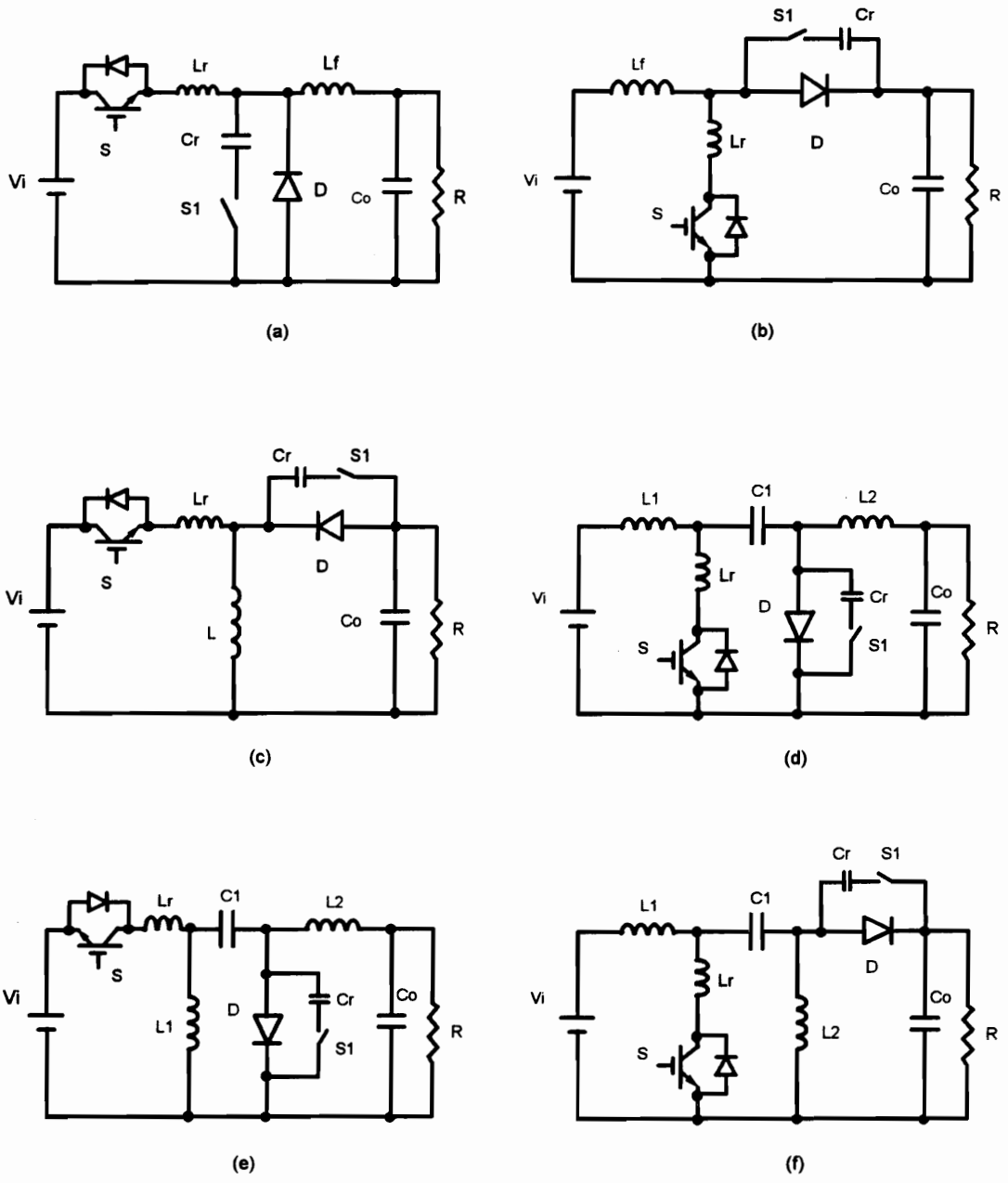


Fig. 3.6. Six basic ZCS-PWM converter topologies: (a) buck, (b) boost, (c) buck-boost, (e) Cuk, (e) Sepic, and (f) Zeta

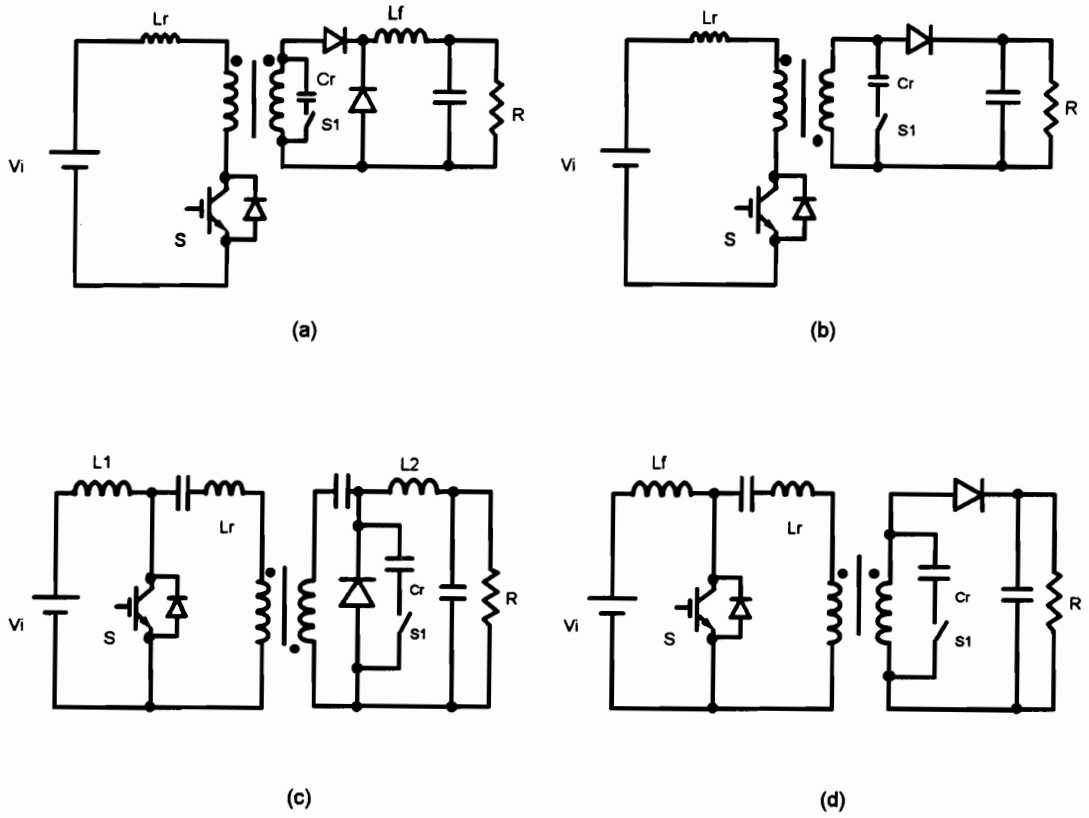


Fig. 3.7. Several topologies of the isolated ZCS-PWM converters: (a) forward, (b) flyback, (c) Sepic, and (d) Cuk.

- still significant circulating energy at light load;

  The circulating energy of the converter is determined by the energy stored in the resonant capacitor. When load current decreases, the peak voltage on the resonant capacitor does not change (it is twice as high as the input voltage for the buck topology). Thus the circulating energy remains the same.

- parasitic ringing across the power switch;

  Since the resonant inductor still in series with the power switch, the power switch still sees parasitic voltage ringing at turn-off. However, this parasitic ringing is less significant since the resonant inductance used in a ZCS-PWM converter is typically much lower as compared to the ZCS-QRCs.

Among the family of ZCS-PWM topologies, one particularly interesting topology is the FB-ZCS-PWM converter shown in Fig. 3.8 [F20], which is a dual circuit of the FB-ZVS-PWM converter. All the semiconductor devices operate with soft-switching and are subjected to low voltage and current stresses associated with those in their PWM counterparts. Applying phase-shift control, constant-frequency control is achieved without using any auxiliary switch. In practice, this converter can be used for high-power applications. Detailed operation and features of the FB-ZCS-PWM converter are explained in the following section.

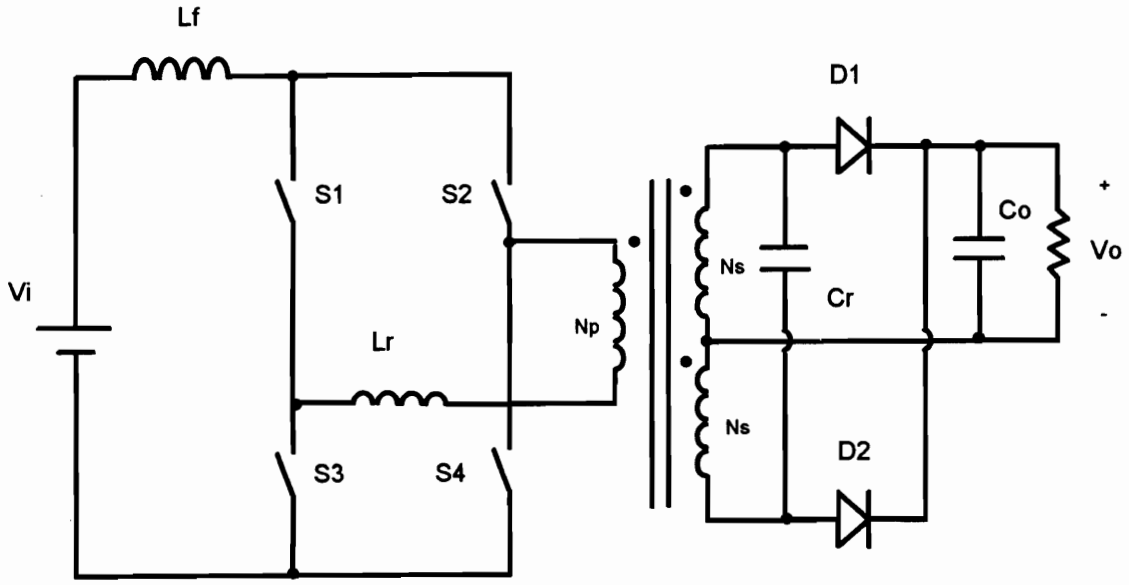


Fig. 3.8. Basic circuit diagram of the FB-ZCS-PWM converter.

3.3 Full-Bridge Zero-Current-Switched PWM Converter

As a particular member of the family of ZVS-PWM converters, the FB-ZVS-PWM converter is deemed desirable for high-power applications, since it combines the advantages of the conventional PWM and ZVS-QRC techniques, while overcoming their respective major limitations. Applying phase-shift control, the FB-ZVS-PWM converter achieves constant-frequency operation without using any auxiliary switch. In addition, the leakage inductance of the power transformer can be utilized to achieve zero-voltage-switching for the power switches. This topology is considered one of the most successful soft-switching topologies, and is widely used in industry today.

Similarly, in the family of ZCS-PWM converter, there is also a special member that is deemed attractive for practical applications, that is, the FB-ZCS-PWM converter. This converter also uses the phase-shift control to achieve fixed-frequency operation. All the primary switches operate with ZCS, while the rectifier diodes operate with ZVS, and they are subjected to low voltage/current stresses similar to those in their PWM counterparts. Therefore, switching losses are greatly reduced without significantly increasing the voltage and current stresses of the switches. These soft switching features, together with its constant-frequency operation, make the FB-ZCS-PWM converter attractive for high-power applications where high-power devices such as IGBTs, BJTs, GTOs, and MCTs are used.

As will be shown below, the FB-ZCS-PWM converter is dual to the FB-ZVS-PWM converter. Detailed operation of this circuit is described in the following section.

3.3.1. Principle of Operation

The simplified circuit diagram and key waveforms of the FB-ZCS-PWM converter are shown in Fig. 3.9. L_r is the resonant inductor which incorporates the leakage inductance of the transformer, and C_r is the resonant capacitor which incorporates the junction capacitance of the rectifier diodes and the winding capacitance of the power transformer. Similarly to the FB-ZVS-PWM converter, the FB-ZCS-PWM converter also uses phase-shift control to achieve constant-frequency operation.

To simplify the analysis, the input filter inductance is assumed to be sufficiently large to be considered as a dc current source, and the transformer magnetizing current is assumed negligible. In steady state, this converter presents ten topological stages within one switching cycle:

(1) T0-T1: Initially, S1, S4, and D2 are conducting. At t=T0, S3 is turned on. During this time interval, the resonant inductor sees a reflected output voltage, $-(N_p/N_s)V_o$. Therefore, the L_r current decreases at a rate of $(N_p/N_s)V_o/L_r$, and the current which initially flows through S4 is transferred to S3. The equivalent circuit is shown in Fig. 3.10(a). The switch S1

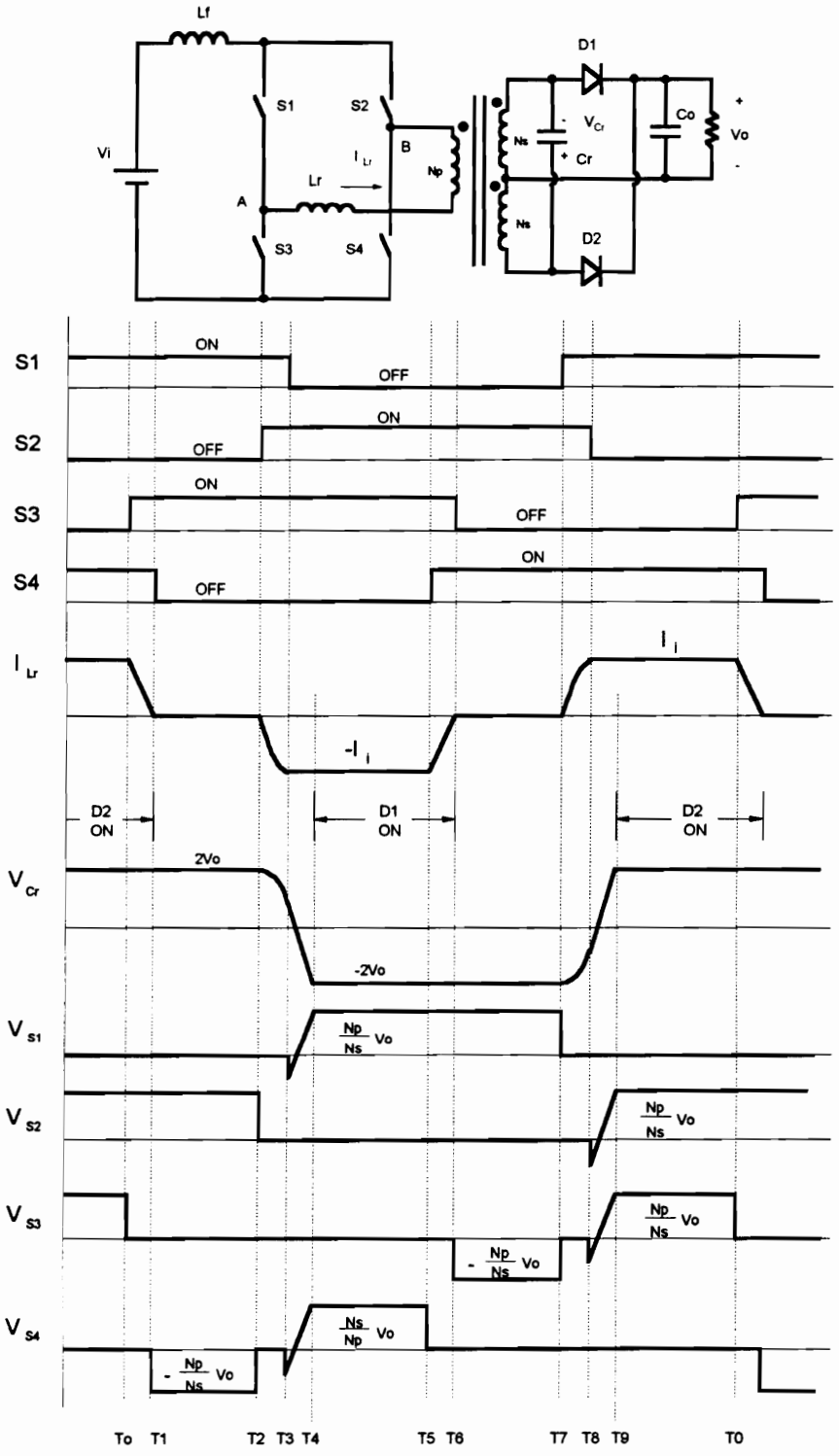
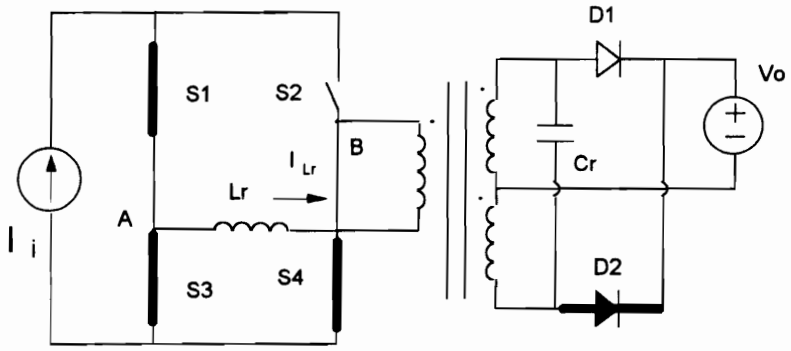
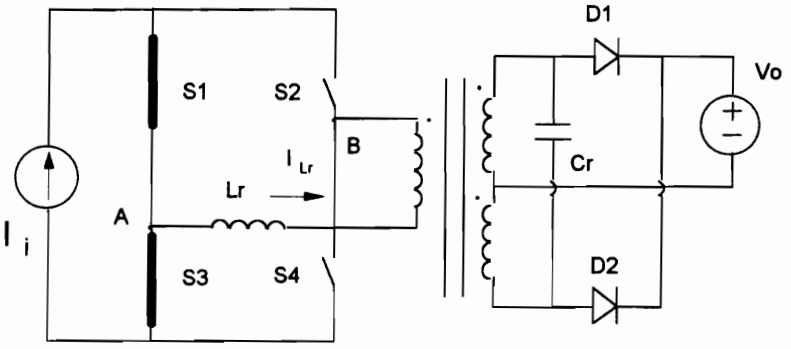


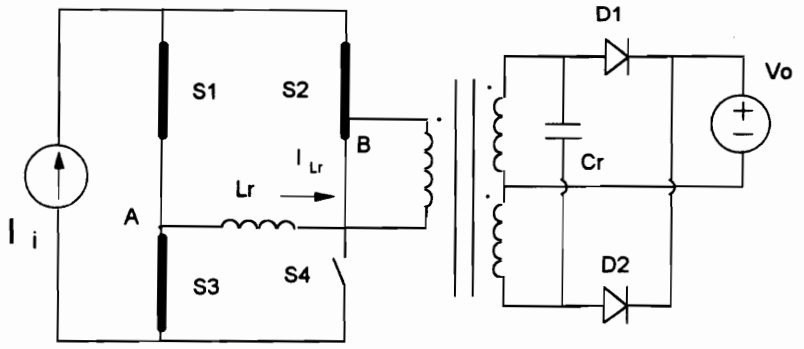
Fig. 3.9. Simplified circuit diagram and typical waveforms of the FB-ZCS-PWM converter.



(a) T0 - T1

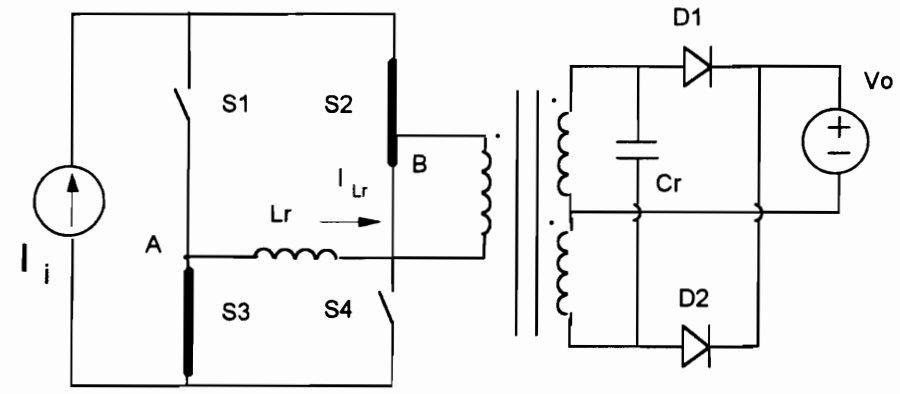


(b) T1 - T2

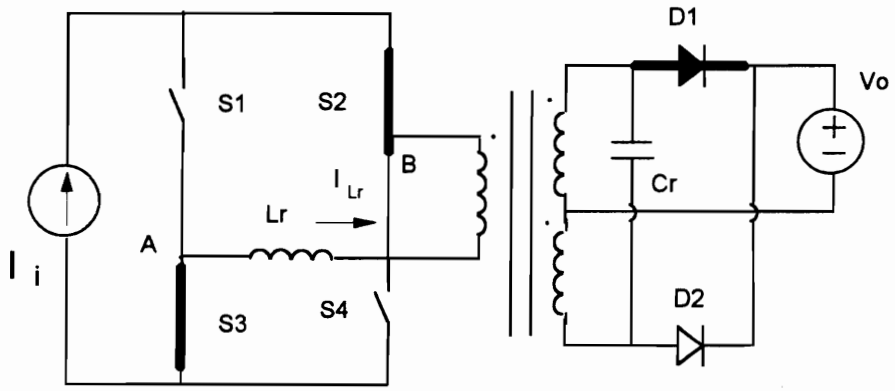


(c) T2 - T3

Fig. 3.10. Equivalent circuits of the FB-ZCS-PWM converter for different topological stages.



(d) T3 - T4



(e) T4 - T5

Fig. 3.10. Equivalent circuits of the FB-ZCS-PWM converter for different topological stages.

current and resonant capacitor voltage remain constant during this interval. At time T1, the current through L_r is reduced to zero. Diode D2 is turned off with both ZCS and ZVS.

(2) T1-T2: The current through S4 is reduced to zero, and S4 is turned off with ZCS at time T1. A negative voltage, $-(N_p/N_s)V_o$, is applied to S4. During this time interval, both diodes are off, and the voltage across D2 remains at zero.

(3) T2-T3: At T3, switch S2 is turned on, and the resonance between L_r and C_r begins. The current through S1 is transferred to S2 in a resonant fashion during this time. At time T3, S1 is turned off. To achieve zero-current turn off for S1, the energy stored in C_r has to be large enough so that the peak L_r current can reach I_i value (i.e., S1 current can be forced to zero) at T3. Therefore, ZCS operation can be achieved for all load and line conditions if the following condition is satisfied:

$$\frac{1}{2}C_r(2V_o)^2 > \frac{1}{2}L_r I_{i\max}^2, \tag{3.4}$$

where I_{imax} is the maximum input current which occurs at low line and full load condition.

(4) T3-T4: When the inductor current reaches I_i at T3, S1 is turned off with ZCS. The resonant capacitor is discharged linearly until its voltage achieves -2Vo, and the diode D1 is turned on at T4.

(5) T4-T5: Switches S2, S3, and the diode D1 are on during this interval. At T5, S4 is turned on, starting the other half cycle of the operation.

(6) T5-T6 to (10) T9-T0: Operation of the circuit during this half switching cycle is symmetrical to the first half cycle.

It can be seen from the above description that the active switches and rectifier diodes are operated with zero-current switching and zero-voltage switching, respectively. In a practical circuit, the switching transition time can be very short with respect to the switching cycle. As compared to the PWM converter, the switching losses are greatly reduced at the expense of a moderate increase in conduction loss. Similarly to the FB-ZVS-PWM converter, regulation of the proposed converter is accomplished by regulating the phase shift between the upper and the lower two switches. Thus the FB-ZCS-PWM converter also operates with a constant frequency.

Since the proposed converter is operated with zero-current switching, the parasitic capacitances of the active switches are not utilized. Therefore, the capacitive turn-on loss and parasitic ringing problems usually associated with the ZCS operation are also observed in this circuit. When high-power minority-carrier devices like IGBTs are employed, these problems are less severe, since high-power minority devices have relatively small output capacitance. Furthermore, the operation frequency of the IGBT circuit is usually considerably lower than that of the MOSFET circuit. Hence, the capacitive turn-on loss and parasitic ringing problems are less pronounced.

In Fig. 3.9, all the primary switches should have reverse-voltage blocking capability. In fact, only S3 and S4 need to have bidirectional-voltage blocking capability. S1 and S2 can be implemented by either a voltage-bidirectional or current-bidirectional switch. If S1 and S2 are implemented by current

bidirectional switch, the operating waveforms in Fig. 3.9 will be slightly modified That is, the negative voltage peaking on S1 and S2 will disappear. In practice, it is desirable to use current-bidirectional switch for S1 and S2 because of easier implementation. S3 and S4 can be implemented by either an IGBT in series with a reverse-voltage blocking diode, or an IGBT with reverse-voltage blocking capability, or a GTO.

The rectifier diodes of the ZCS-PWM converter are commutated with ZVS. This feature makes the new converter attractive for applications with high output voltage (e.g., power factor correction circuits), where the rectifiers suffer from severe reverse-recovery problem when conventional PWM, ZVS-QRC, or ZVS-PWM converter techniques are used.

3.3.2. Duality — FB-ZVS-PWM Converter vs. FB-ZCS-PWM Converter

The FB-ZCS-PWM converter can be derived from the well-known FB-ZVS-PWM converter by simply applying the duality principle [F20]. A brief description of the duality relationship between these two circuits is given below.

The topology of FB-ZVS-PWM converter differs from that of the conventional FB-PWM converter by using a resonant inductor in series with the transformer primary. The resonant inductor can be the leakage inductance of the transformer. In this case, the topologies of the two circuits are identical. The

FB-ZVS-PWM converter uses phase-shift control to achieve output regulation. The duty cycle for each switch is close to 50%. Instead of turning on or off the diagonal-opposite switches simultaneously, a phase lag is introduced between them to regulate the output. The detailed operation is described in [F7].

Assuming the filter inductor is sufficiently large for its current to remain essentially constant, the FB-ZVS-PWM converter can be regarded as a voltage source supplying power to a current sink. During the zero-voltage switching transition time, the primary current always simultaneously charges the output capacitance (C_{DS}) of one switch and discharges C_{DS} of the other switch in the same leg. Thus, the operation of FB-ZVS-PWM converter with one C_{DS} across each switch is equivalent to the operation of one with a resonant capacitor ($C_r=2C_{DS}$) across the tank. Figure 3.11(a) shows the converter equivalent to the FB-ZVS-PWM converter described in Chapter 2.

By applying circuit duality, the dual of the topology shown in Fig. 3.11(a) is derived, as shown in Fig. 3.11(b). The duality relationship is briefly described as follows

(1) The voltage source (V_i) becomes a current source (I_i'), and the current source (I_o) becomes a voltage source (V_o');

(2) the inductor (L_r) in series with the transformer primary becomes a capacitor (C_r') in parallel with the transformer primary, and the capacitor (C_r) becomes an inductor (L_r');

(3) two switches in series in each leg become two in parallel (e.g., S1, S2 $\Rightarrow$ S1', S2'); and

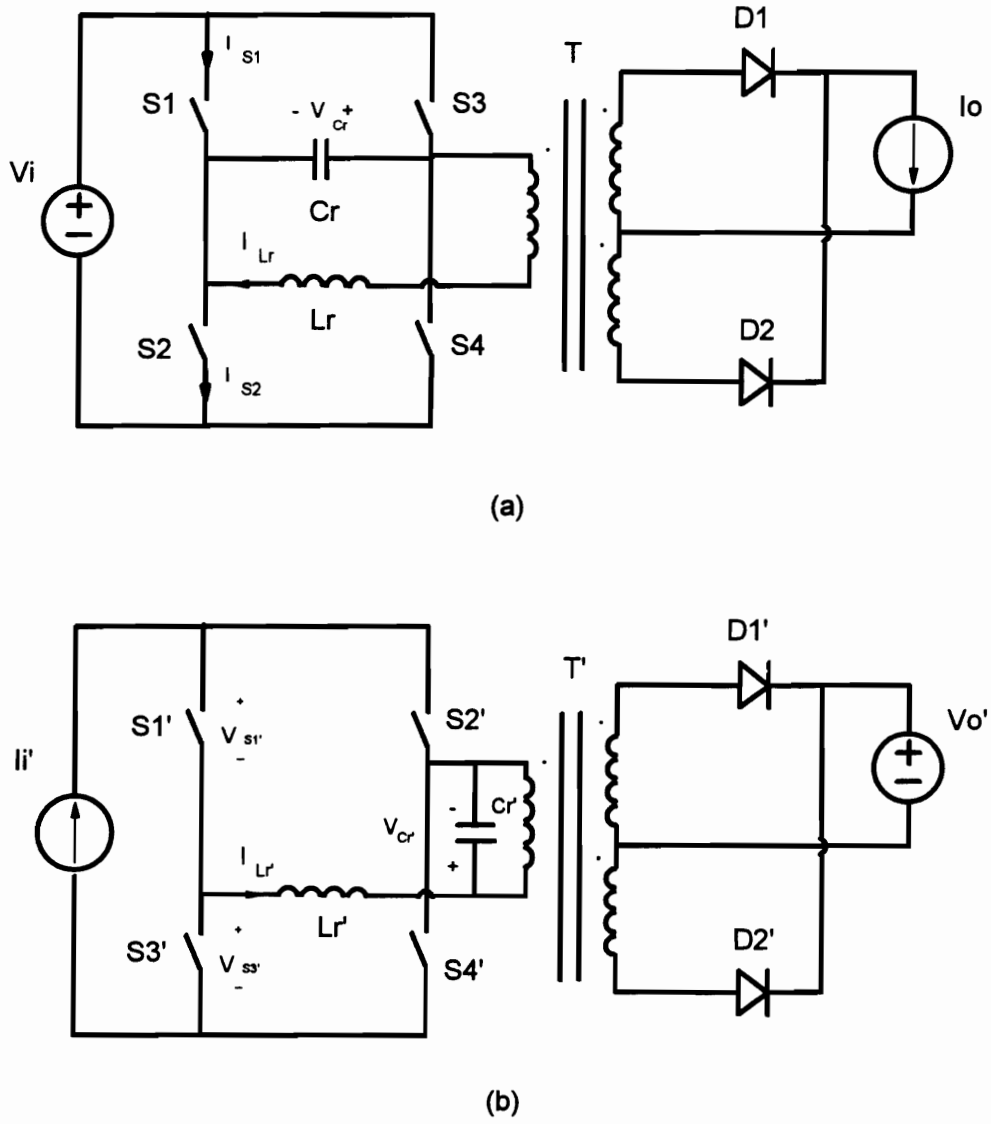


Fig. 3.11. Simplified topologies of two dual converters:
(a) FB-ZVS-PWM converter, and
(b) FB-ZCS-PWM converter.

(4) the dual of the transformer (T) is still a transformer (T'), with the turns ratio reversed, however.

A comparison of the key waveforms of the two converters discussed above is shown in Fig. 3.12. The waveforms clearly display the duality relationship between the two converters. Since the dual of an open-circuit is a short-circuit and vice versa, the gate control signals for dual switches are complementary. A detailed comparison of the equivalent circuits for each topological stage can also show the duality between the two topologies. In fact, the dual properties between them are true both qualitatively and quantitatively. For instance, the conversion ratio of the ZCS converter can be derived from that of the ZVS converter simply by applying the duality.

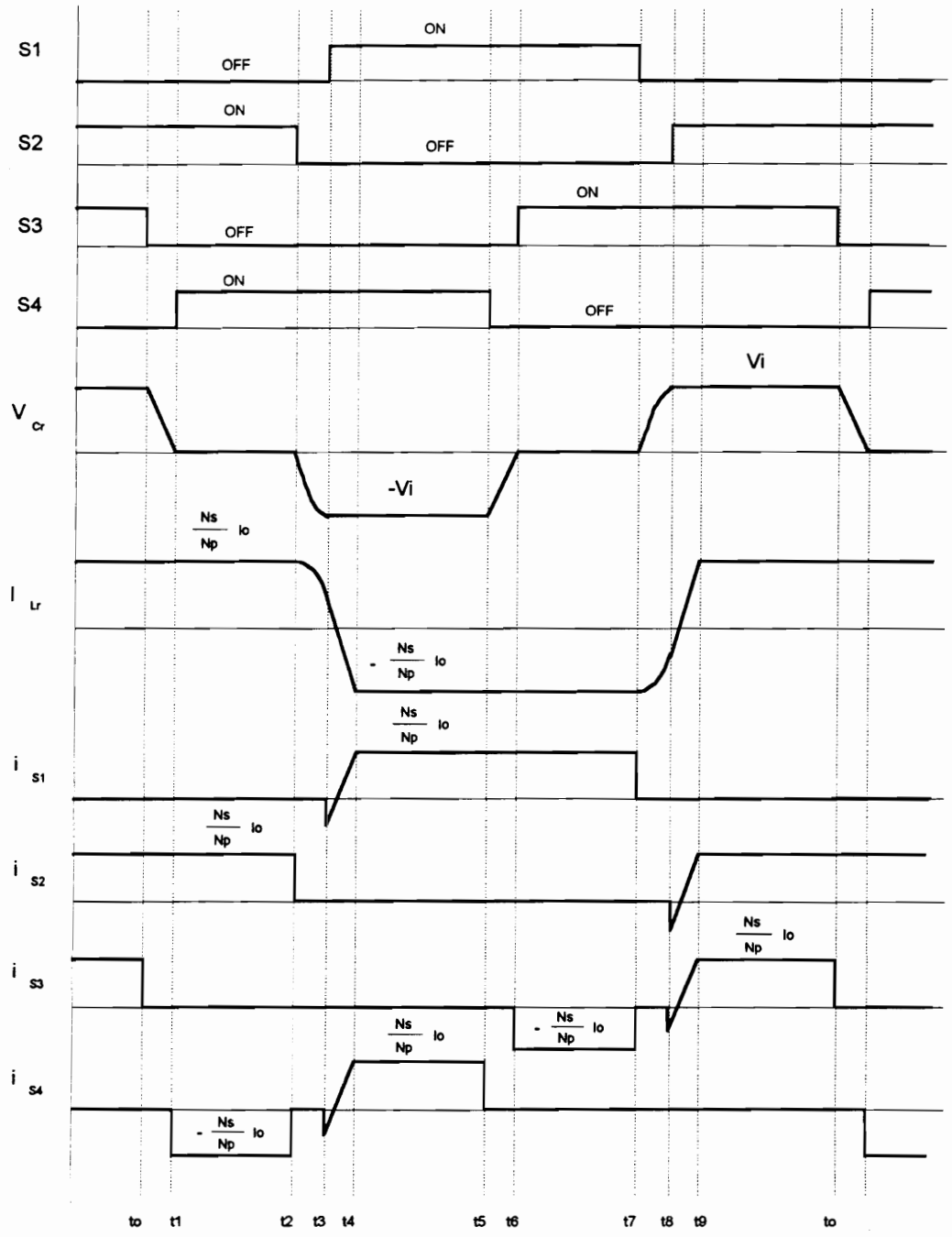
Table I summarizes some dual characteristics of the FB-ZVS-PWM converter and the FB-ZCS-PWM converter.

3.3.3. Experimental Results

An 80 kHz (switching frequency), 200 W ZCS-PWM converter with 100-200 V input and 48 V output was implemented to demonstrate the operation of the proposed converter. The power stage consists of the following components:

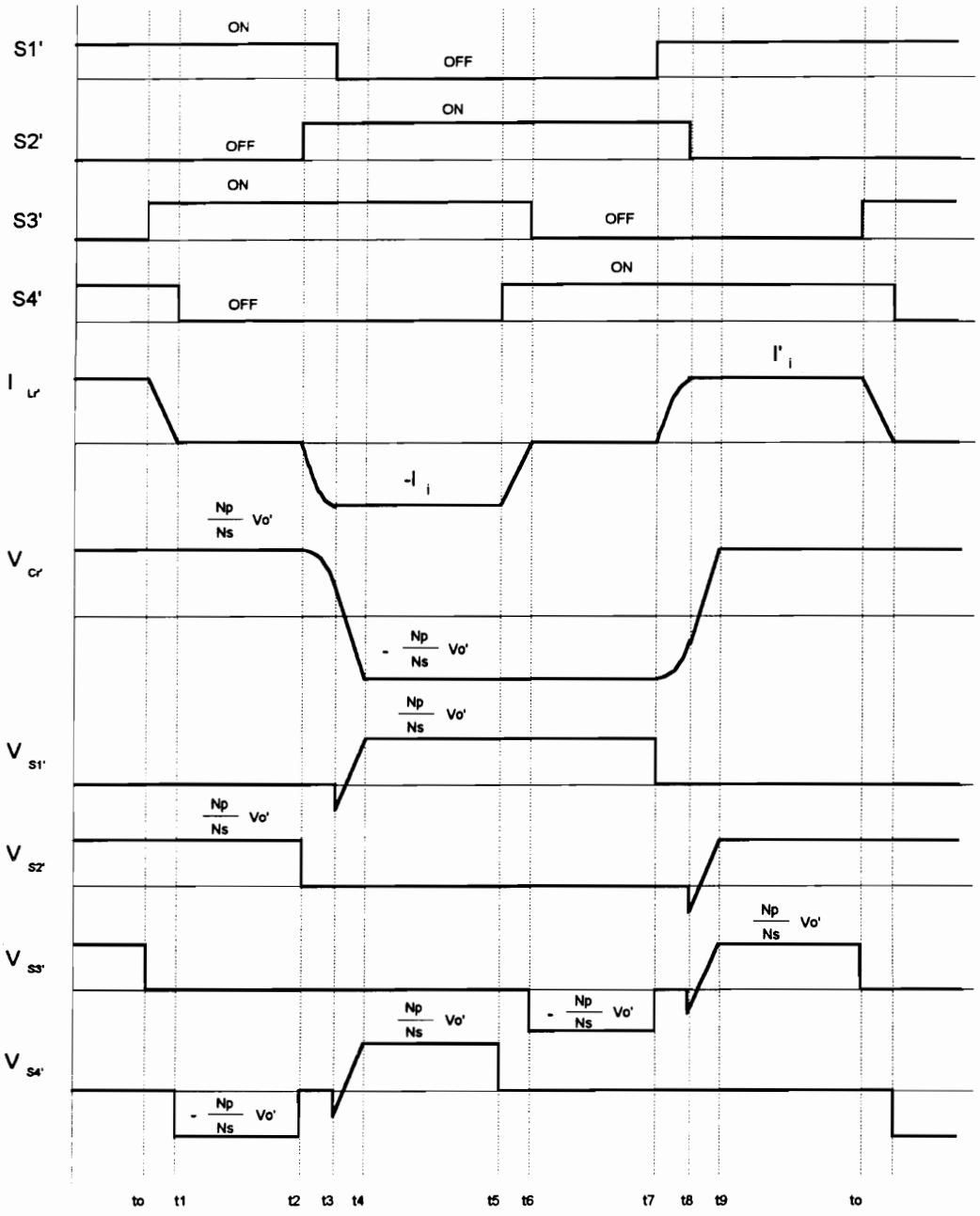
S1-S4 - IXGP10N50 (IXYs' IGBT, V_{ces}=500 V, I_C=10 A, t_f=2.0 us) in series with UES1106 (diode);

D1,D2 - UES1403;



(a)

Fig. 3.12. Comparison of the waveforms between (a) the FB-ZVS-PWM converter, and (b) the FB-ZCS-PWM converter.



(b)

Fig. 3.12. Comparison of the waveforms between (a) the FB-ZVS-PWM converter, and (b) the FB-ZCS-PWM converter.

Table 3.1. Dual characteristics of the FB-ZVS-PWM converter and the FB-ZCS-PWM converter

	FB-ZVS-PWM	FB-ZCS-PWM
Topology type	buck type	boost type
Switching condition for active switches	ZVS	ZCS
Switching condition for diode	ZCS	ZVS
Soft-switching easy to achieve at	heavy load	light load
Implementation of active switches	current-bidirectional	voltage-bidirectional

L_f - 0.8 mH, magnetic core PQ 2016 (material H7C4);

TR - core: PQ 2625 (material H7C4);

primary: 48 turns of magnet wire AWG # 24;

secondary: 15 turns, center tapped, AWG # 23 X 2;

L_r - 12 uH, magnetic core RM 5Z52B (material H7C4);

C_r - 22 nF, ceramic capacitor;

C_f - 2 X 22 uF, aluminum capacitors.

Since the primary switches in the FB-ZCS-PWM converter also require phase-shift control, the control circuit designed for the FB-ZVS-PWM converter can be used also in this converter. Figure 3.13 shows the oscillograms of the experimental ZCS-PWM converter. The measured overall efficiency of the converter is given in Fig. 3.14. The efficiency of the converter drops significantly at low line and heavy load, since the IGBTs begin to lose the ZCS property.

3.4. Summary

In high-power applications, minority-carrier devices such as BJTs, IGBTs, and GTOs are predominantly used. Operating these high-power devices at higher frequencies requires switching mechanism and commutation techniques with much reduced switching losses than the hard-switching PWM technique. Due to poor turn-off switching characteristics, these high-power, minority devices prefer zero-current switching. Although the ZCS resonant or quasi-resonant

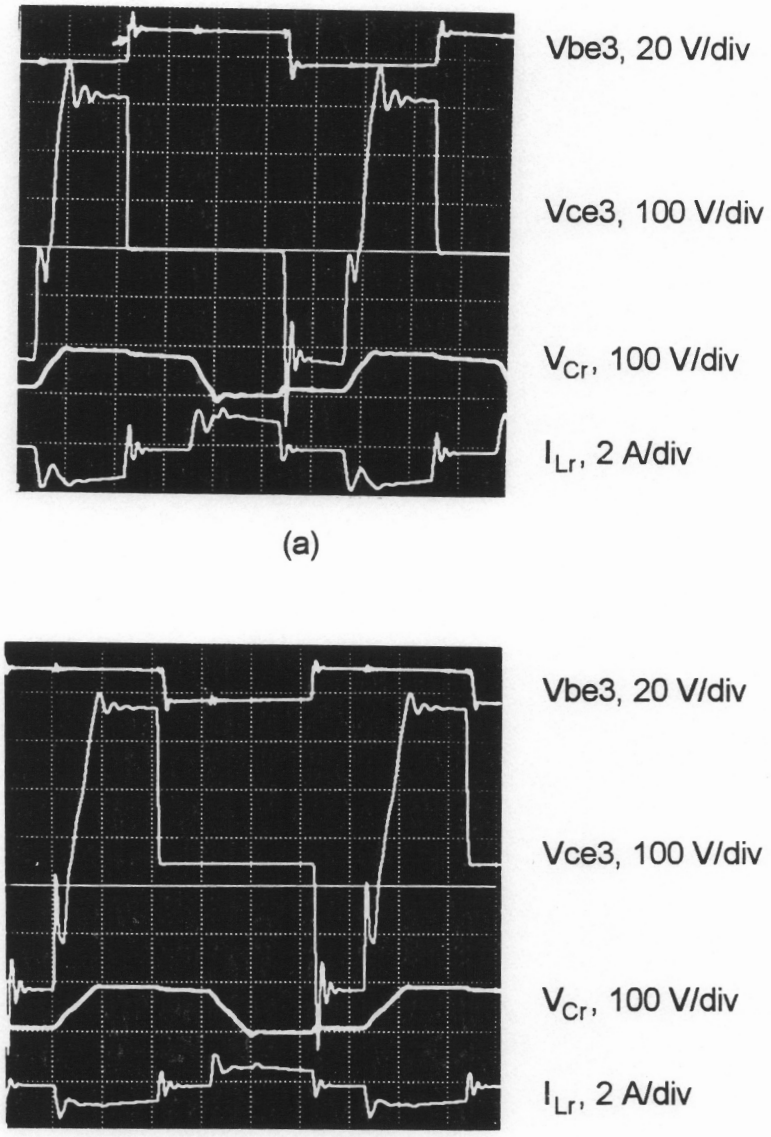


Fig. 3.13. Gate-drive (V_{be3}), switch voltage (V_{ce3}), resonant capacitor voltage (V_{Cr}), and primary current (I_{Lr}) of the 80 kHz, 200 W FB-ZCS-PWM converter at Vi=150 V, (a) full load, and (b) half load.

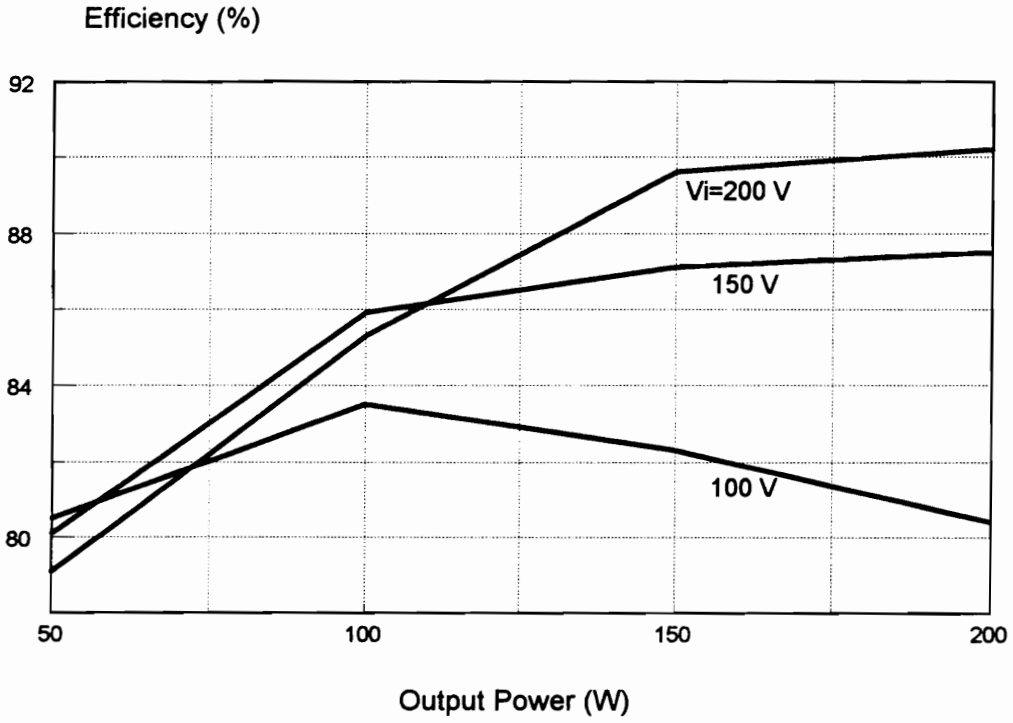


Fig. 3.14. Overall efficiency of the experimental FB-ZCS-PWM converter.

technique is capable of eliminating most of the switching losses, it imposes high circulating energy which significantly increases conduction losses. Furthermore, these resonant circuits usually operate with variable frequencies, making the converter difficult to optimize.

This chapter presents a family of ZCS-PWM converters which combine the merits of the conventional PWM and ZCS-QRC techniques while avoiding their major shortcomings. The use of an auxiliary switch in series with the resonant capacitor partially kills the resonance by disconnecting the resonant capacitor from the resonant inductor during power switch on-time. As a result, a ZCS-PWM converter does not require fixed on-time control and can be controlled by duty cycle control. In addition, the circulating energy is significantly reduced as compared to its ZCS-QRC counterpart, since the ZCS resonant period can occupy only a small portion of the switching cycle. This results in a significant reduction in both conduction losses and the size of the resonant components. The ZCS-PWM technique presents a significant improvement in circuit performance over the ZCS-QRC technique.

One of the limitations of the ZCS-PWM technique is that the rectifier diode suffers from a high voltage stress which is twice as high as that in a PWM converter. Another limitation is the parasitic ringing which appears on the power switch because of the resonance between the resonant inductor and the output capacitance of the switch. However, it should be noted that this limitation is less pronounced compared to a ZCS-QRC, since a much smaller resonant inductance can be used in a ZCS-PWM converter.

As a particular member of the family of ZCS-PWM converters, the FB-ZCS-PWM converter is particularly deemed desirable for high-power applications. All the primary switches operate with ZCS, while the rectifier diodes operate with ZVS, and they are subjected to low voltage/current stresses similar to those in their PWM counterpart. In addition, by applying phase-shift control, the FB-ZCS-PWM converter achieves constant-frequency operation without using any auxiliary switch. Another desirable feature is that both the leakage inductance of the power transformer and the junction capacitance of the rectifier diodes are utilized to achieve soft-switching. This unique feature, which is not exhibited by most other soft-switching PWM converters, makes the FB-ZCS-PWM converter particularly attractive for very-high-voltage applications, in which the transformer leakage inductance and the diode junction capacitance often cause series problems.

As an example, the duality relationship between the FB-ZVS-PWM converter and the FB-ZCS-PWM is characterized. This relationship establishes a framework to transfer knowledge systematically from the ZVS-PWM converter family to the ZCS-PWM converter family.

CHAPTER 4

ZERO-VOLTAGE-TRANSITION PWM CONVERTERS

4.1 Introduction

For minimization of size and weight, high-frequency operation of the traditional PWM converters requires a substantial reduction of switching losses. In recent years, a number of soft-switching technologies have been proposed. Unfortunately, switching losses in these new circuits can be reduced only at the expense of much increased voltage/current stresses of the switches, which leads to a substantial increase in conduction loss.

The active switch in a ZVS-QRC is subjected to relatively low current stress. However, in a single-ended ZVS-QRC topology, the active switch suffers from an excessive voltage stress which is proportional to the load range [C2].

Although the active switch operates with ZVS, the rectifier diode operates with ZCS. The parasitic junction capacitance of the rectifier diode interacts with the large resonant inductor, which results in severe switching oscillation noise. As an extension of the ZVS-QRC technique, the ZVS-PWM technique significantly improves the ZVS-QRC technique by using an auxiliary switch to enable constant-frequency operation and to reduce circulating energy. However, due to the presence of the resonant inductor in the main power path, the operation of a ZVS-PWM converter still imposes a high voltage stress on the power switch, and severe parasitic ringing on the rectifier diode.

The ZVS-MRC technique utilizes all major parasitics of the power stage. All semiconductor devices in a ZVS-MRC operate with ZVS , which substantially reduces the switching losses and switching noise. Nevertheless, both active and passive switches in a ZVS-MRC are subjected to voltage and current stresses significantly higher than those in their PWM counterparts. Although the switching losses are eliminated, the conduction loss increases significantly. In addition, the advantage of the smaller size of the reactors (the power transformer and filters) due to high-frequency operation is also partially mitigated by the need for a relatively large resonant inductor, whose size is usually comparable to that of the power transformer. This resonant inductor also introduces additional core loss and copper loss.

The constant-frequency ZVS-QSC technique offers ZVS for both the active and passive switches without increasing their voltage stresses [F2]. This is a very desirable feature for high-frequency conversion where MOSFETs are used, since power MOSFETs favor the zero-voltage switching operating mode, and their conduction characteristics are strongly dependent on voltage rating.

However, the switches in a ZVS-QSC suffer from a high current stress which can be more than twice of that in its PWM counterpart; thus, the conduction losses are greatly increased. In addition, the high turn-off current of the main switch tends to increase the turn-off loss. In particular, when minority-carrier power devices such as IGBTs and BJTs are used as the power switches, using ZVS-QSC technique may increase the switching loss as compared to a hard-switching PWM converter.

This chapter presents a new class of zero-voltage-transition (ZVT) PWM converters. By using a resonant network in parallel with the switches, the proposed converters achieve ZVS for both the active and passive switches without increasing their voltage and current stresses [F22-F33]. The concept of ZVT-PWM technique will generalized by using the ZVT-PWM switching cell in Section 4.3. In the following section, the boost ZVT-PWM converter is used as an example to illustrate the operation of the new converters.

4.2 ZVT-PWM Boost Converter

4.2.1. Principle of Operation and DC Analysis

Figure 4.1 shows the circuit diagram and the key waveforms of the boost ZVT-PWM converter. It differs from a conventional boost PWM converter by the

introduction of a shunt resonant network consisting of a resonant inductor (L_r), an auxiliary switch (S1), and a diode (D1). C_r is the resonant capacitor which incorporates the output capacitance of the power switch. and the junction capacitance of the rectifier diode. To simplify the analysis, it is assumed that:

a) the input filter inductance is sufficiently large to be approximated by a current source with a value equal to input current, I_i.

b) the output filter capacitance is sufficiently large for the output voltage to be represented by an ideal dc voltage source, V_o.

c) all power stage components are ideal, i.e., all parasitic resistances are zero, and the semiconductor devices have zero conduction voltage drops and zero switching times.

As shown in Fig. 4.2, the converter presents seven operation stages within one switching cycle:

(a) T0-T1: Prior to T0, the main switch (S) and the auxiliary switch (S1) are off, and the rectifier diode (D) is conducting. At T0, S1 is turned on. The L_r current linearly ramps up until it reaches I_i at T1, at which time D is turned off with soft-switching. Because of controlled dv/dt and di/dt at turn off, the reverse-recovery current of D is negligible if a fast-recovery diode is used. This time interval, ΔT_{01}, is given by:

$$\Delta T_{01} = \frac{I_i}{V_o / L_r}. \qquad (4.1)$$

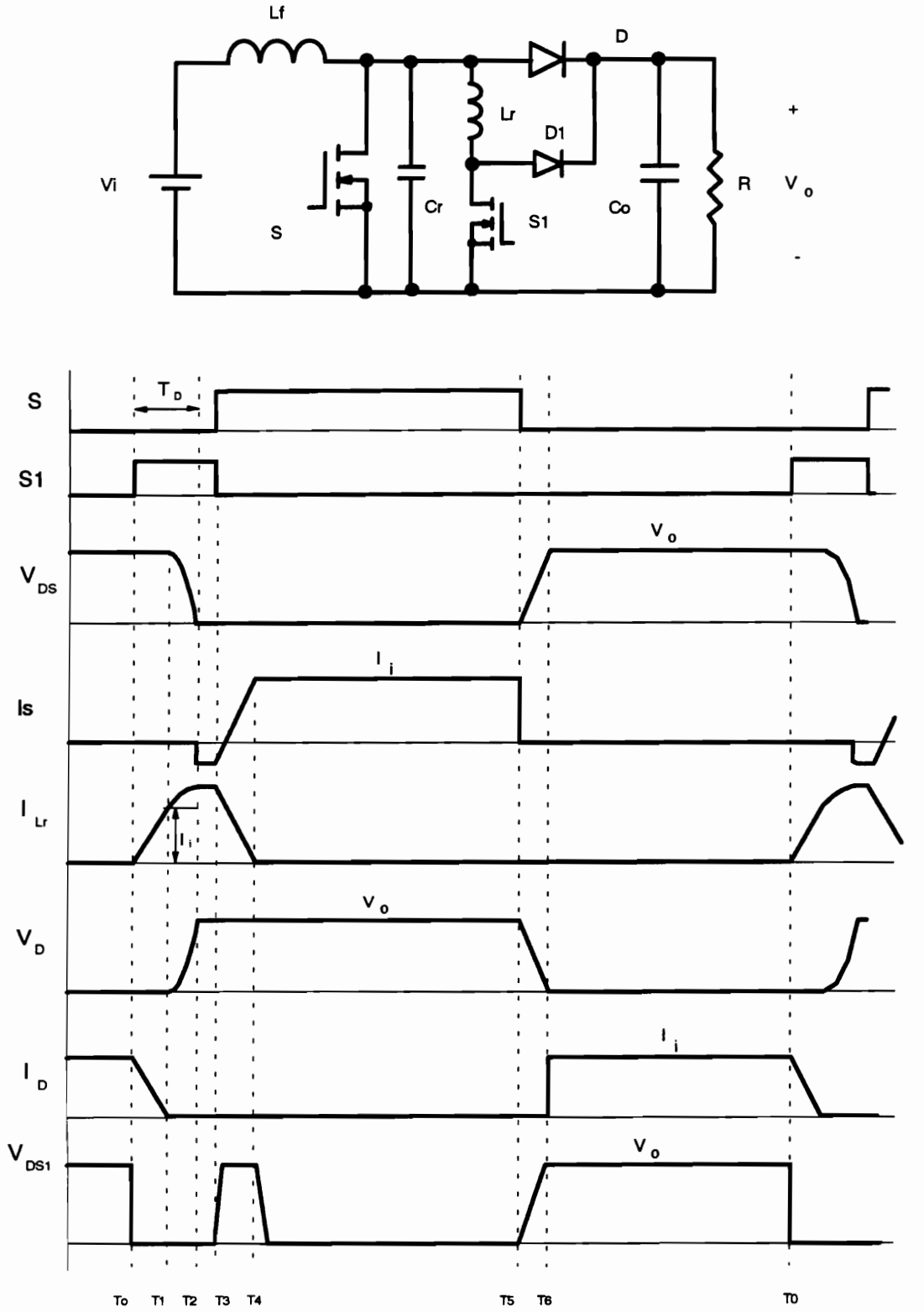


Fig. 4.1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

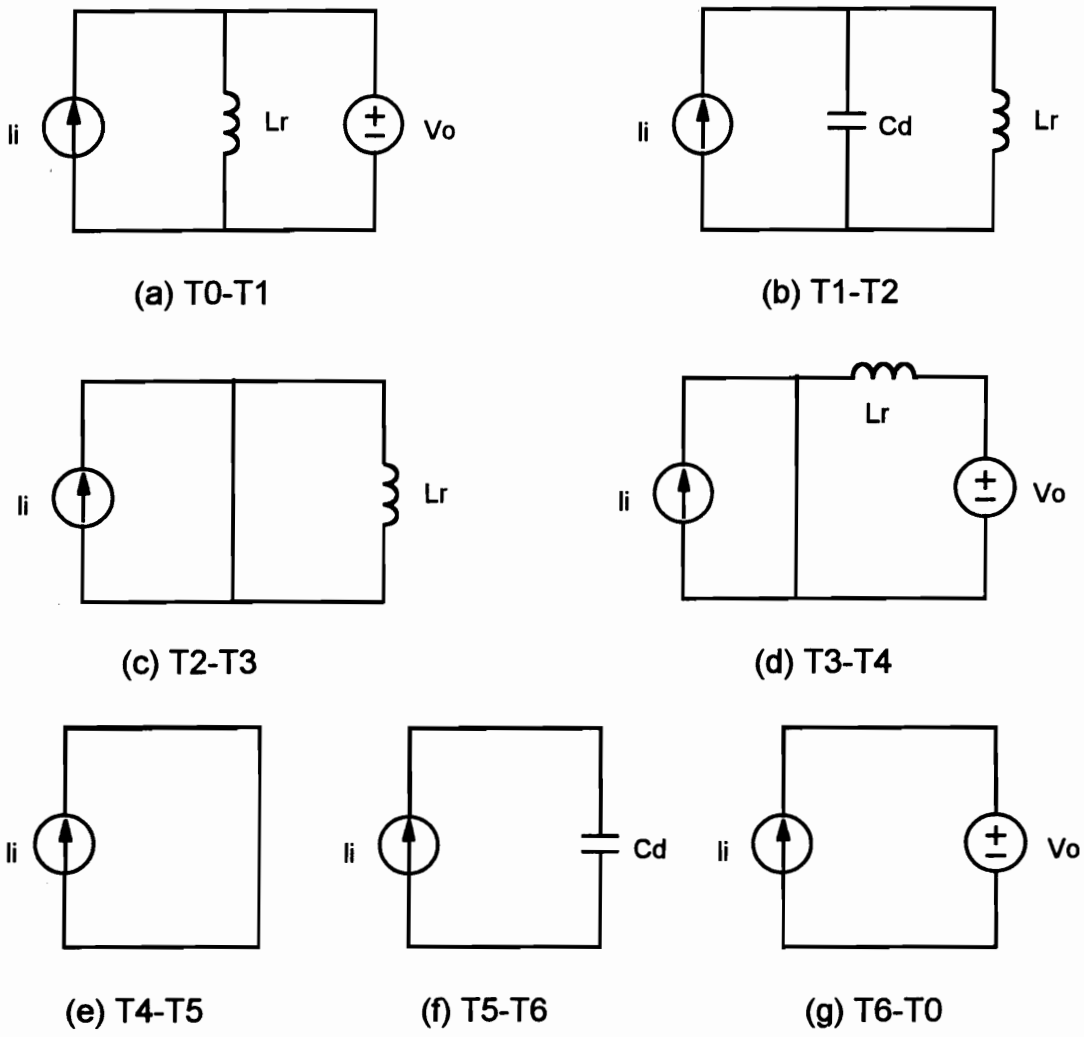


Fig. 4.2. Equivalent circuits for different operation stages of the ZVT-PWM boost converter.

(b) T1-T2: The L_r current continues to increase due to the resonance between L_r and C_r. During this time, the current through L_r increases and the voltage across S or C_r decreases in a resonant fashion:

$$I_{Lr} = I_i + \frac{V_o}{\sqrt{L_r/C_r}} \sin\left(\frac{1}{\sqrt{L_r C_r}} t\right), \tag{4.2}$$

$$V_{DS} = V_o \cos\left(\frac{1}{\sqrt{L_r C_r}} t\right). \tag{4.3}$$

C_r is discharged until the resonance brings its voltage to zero at T2, at which time the anti-parallel diode of S starts to conduct. This resonant time period, ΔT_{12}, is equal to a quarter of the resonant period:

$$\Delta T_{12} = \frac{\pi}{2}\sqrt{L_r C_r}. \tag{4.4}$$

(c) T2-T3: The anti-parallel diode of S is on. To achieve ZVS, the turn-on signal of S should be applied while its body diode is conducting. Besides, the duty cycle of S1, D_1, which determines the time delay between S1 and S gate signals, has to satisfy the following condition:

$$D_1 T_s \geq \Delta T_{01} + \Delta T_{12}, \tag{4.5}$$

$$D_1 T_s \geq \frac{L_r I_i}{V_o} + \frac{\pi}{2}\sqrt{L_r C_r}. \tag{4.6}$$

(d) T3-T4: At T3, S1 is turned off, and its voltage is clamped at V_O due to the conduction of D1. The energy stored in the resonant inductor is transferred to the load during this time interval. L_r current decreases linearly until it decays to zero at T4.

(e) T4-T5: D1 is turned off at T4. The operation of the circuit at this stage is identical to the transistor-on stage of the PWM boost converter.

(f) T5-T6: At T5, S is turned off. C_r is linearly charged by I_i to V_i voltage. This time interval is given by:

$$\Delta T_{56} = \frac{C_r V_o}{I_i}. \tag{4.7}$$

(g) T6-T0: This interval is identical to the freewheeling stage of the boost PWM converter. At T0, S1 is turned on again, starting another switching cycle.

It should be noted that the boost circuit described in [16] has the same features as the above-analyzed converter. However, the implementation of the auxiliary resonant branch for that circuit requires more components. In addition, it is only one member of a large converter family of ZVT-PWM converters [F26].

Based on the above description, the features of the ZVT-PWM boost converter can be summarized as follows:

A. Soft-switching for both the transistor and rectifier diode.

It can be seen that in addition to the power switch, the rectifier diode in the ZVT-PWM boost converter is also commutated under soft-switching. This

feature makes the ZVT-PWM technique particularly attractive for high-voltage conversion applications, in which the rectifier diodes suffer from severe reverse recovery problems. For instance, in a power-factor correction (PFC) boost circuit, both the power switch and the rectifier diode are subjected to high voltage. With the conventional PWM, or the ZVS-QRC, or the ZVS-PWM technique employed, due to the reverse recovery of high-voltage p-n junction diode, the high switching loss, high EMI noise, and device failure problems become more pronounced. Therefore, implementing soft-switching for both the transistor and the rectifier diode in such a circuit is particularly rewarding.

B. Minimum switch voltage and current stresses.

From Fig. 4.1, it can be seen that the voltage and current waveforms of the switches in the ZVT-PWM boost converter are essentially square-wave, except during the turn-on and turn-off switching intervals, when the zero-voltage-switching transition takes place. Both the power switch and the rectifier diode are subjected to minimum voltage and current stresses. In addition, the ZVT time intervals T0-T3 and T5-T6 can be very short with respect to the switching cycle, so the operation of the new converter resembles that of the boost PWM converter during most portions of the cycle. Circulating energy employed to realize ZVS is therefore minimum. The auxiliary switch can be a low current rating device compared to the main switch, as it only handles small amounts of resonant-transition energy. Since soft-switching is achieved without increasing switch voltage and current stresses, the penalty of increase in conduction loss is minimal.

C. Soft-switching maintained for wide line and load range.

One drawback of the ZVS-QRC and ZVS-PWM techniques is that the soft-switching condition is strongly dependent on load current and input voltage. At light load, ZVS is usually difficult to maintain, since the energy stored in the resonant inductor at light load is not sufficient to completely discharge the resonant capacitor prior to turn-on of the active switch [F22]. At high line, ZVS is easier to lose, since it needs more energy to discharge the resonant capacitor.

The situation is opposite in a ZVT-PWM converter. In the ZVT-PWM boost converter, I_i decreases when the load current is reduced, or when the line voltage increases. From inequality (4.5), when I_i decreases, ΔT_{01} also decreases, and ΔT_{12} remains constant. Therefore, as long as condition (4.5) is satisfied at full load and low line, soft-switching operation will be ensured for the whole load and line range.

This unique feature is deemed attractive for many applications. Owing to the advances in device and soft-switching converter technologies, high power capability, low conduction loss, and low cost IGBT devices are frequently used in today's switched-mode power processing circuits. In order to reduce the turn-off loss of the IGBT device, a considerably large external capacitor across IGBT is often used to soften the switching process. Quite often, this external capacitor can cause excessive device current stress and intolerable capacitive turn-on loss if ZVS is lost, or partially lost, at light load and high line. In addition, even though losing ZVS at light load

does not cause a thermal problem, EMI due to switching noises may be intolerable in a practical circuit.

D. Constant-frequency operation.

Due to constant-frequency, the design optimization of the new circuit is easily attainable. In addition, since the operation of the proposed converter resembles that of its PWM counterpart except during short ZVT time, the conventional PWM control ICs and current-mode control can be directly applied to the new converter.

One limitation of the ZVT-PWM technique is that the auxiliary switch does not operate with soft-switching. However, the switching losses involved in the operation of the auxiliary resonant branch are typically much lower than those of a PWM converter. First, the major switching loss that occurs in the ZVT-PWM converter is the capacitive turn-on loss of the auxiliary switch (S1). It is much lower than the capacitive turn-on loss of the main switch in a PWM converter due to the fact that S1 only handles a much lower rms current, and thus a smaller MOSFET with lower output capacitance can be used as S1. The turn-off loss of S1 is negligible if S1 is implemented by a MOSFET, and its gate-drive impedance is sufficiently low. Second, the auxiliary diode of a ZVT-PWM converter always operates with ZCS. Thus it does not suffer from a reverse-recovery problem. For a PWM converter, however, the reverse-recovery loss of the rectifier diode normally dominates the total switching loss in high voltage applications, where p-n junction diodes are used. For this reason, the ZVT-PWM converters are particularly deemed attractive for high-voltage applications

where the reverse-recovery problem of the rectifier diode is of important concern.

4.2.2. DC Voltage-Conversion Ratio

Due to the fixed-frequency operation and quasi-square-like circuit waveforms, the dc characteristics of the ZVT-PWM converters are relatively easy to derive. Based on the steady-state operation waveforms given in the previous section, applying volt-seconds balance on the filter inductor yields:

$$V_i T_s = \int_0^{T_s} V_{DS} dt, \tag{4.8}$$

or

$$V_i T_s = V_o \left[(1 - D - D_1) T_s + \Delta T_{01} - \frac{1}{2} \Delta T_{56} \right] + \int_{T_1}^{T_2} V_{DS} dt, \tag{4.9}$$

where T_S is the switching period of the converter, and D and D_1 are the duty cycles of S and S1, respectively. Defining

$$M = \frac{V_o}{V_i} \tag{4.10}$$

as the dc voltage-conversion ratio, Eq. (4.9) can be rewritten as:

$$M = \frac{1}{(1 - D - D_1) + \dfrac{\Delta T_{01} + \dfrac{2}{\pi}\Delta T_{12} - \dfrac{1}{2}\Delta T_{56}}{T_s}}. \qquad (4.11)$$

By recalling the ZVS gate-drive timing requirement given by Eq. (4.5), it can be seen that the voltage-conversion ratio of the ZVT-PWM boost converter is always higher than that of the PWM boost converter under a given duty cycle. This is because the conduction of the auxiliary switch increases the equivalent duty cycle of the converter.

In general, the auxiliary switch (S1) in a ZVT-PWM converter can be controlled in two ways. The first approach is to use fixed on-time control. The on-time of S1 is fixed at a certain value so that the converter will operate with soft-switching for the entire load and line range. The second approach is to use variable on-time control. In this way, the on-time of S1 is regulated according to line voltage and load current variations so that the converter can just achieve soft-switching. Under different control strategy, the dc voltage-conversion ratio of the ZVT-PWM boost converter is different.

4.2.2.1. DC Voltage-Conversion Ratio Under Fixed S1 On-Time Control

This control scheme is relatively simple and easy to implement. The converter is designed to achieve soft-switching for the worst condition, which occurs at full load and low line. In other words, the on-time of the auxiliary switch is set at:

$$D_1 T_s = \Delta T_{01} + \Delta T_{12} = \frac{I_i^{\max} L_r}{V_o} + \frac{1}{4} T_r, \tag{4.12}$$

where $T_r = 2\pi\sqrt{L_r C_r}$ is the resonant period of the resonant tank, and $I_i^{\max}$ is the maximum input current which occurs at full load and low line condition. At full load and low line, ΔT_{23} is zero. As the line voltage increases or load current decreases, ΔT_{23} increases. Substituting Eqs. (4.1) - (4.7) into Eq. (4.9) yields:

$$M = \frac{1}{(1 - D - D_1) + \dfrac{I_i L_r / V_o + \sqrt{L_r C_r} - V_o C_s / 2 I_i}{T_s}}, \tag{4.13}$$

or

$$M = \frac{1}{1 - D - D_1 + \dfrac{T_r}{2\pi T_s}\left(\dfrac{M}{r} - \dfrac{1}{2}\dfrac{r}{M} + 1\right)}, \tag{4.14}$$

where

$r = \dfrac{R_L}{Z_n}$ is the normalized load impedance; and

$Z_n = \sqrt{\dfrac{L_r}{C_r}}$ is the characteristic impedance of the resonant tank.

The analytical solution of Eq. (4.10) can be directly given by:

$$M = \frac{D + D_1 - 1 - \dfrac{T_r}{2\pi T_s} + \sqrt{\left(1 - D - D_1 + \dfrac{T_r}{2\pi T_s}\right)^2 + \dfrac{T_r}{2\pi r T_s} + \dfrac{1}{2}\left(\dfrac{T_r}{\pi T_s}\right)^2}}{\dfrac{T_r}{\pi r T_s}}. \tag{4.15}$$

In addition, it should be noted that Eqs. (4-13) - (4.15) are only valid when the ZVS condition given by Eq. (4.6) is satisfied. Equation (4.6) can be rewritten as:

$$D_1 \geq \left(\frac{1}{2\pi}\frac{M}{r}+\frac{1}{4}\right)\frac{T_r}{T_s}. \tag{4.16}$$

Figure 4.3 (a) shows the voltage-conversion ratio as a function of duty cycle (D) with the normalized load impedance (r) as a running parameter for $T_r=10\%T_S$ and D_1=10%. Compared with the voltage-conversion ratio of the PWM boost converter which is also given in Fig. 4.3 (a), it can be seen that the ZVT-PWM boost converter has a higher voltage-conversion ratio. When the normalized load impedance (r) is low or the load current is high, the voltage-conversion ratio of the ZVT boost converter is quite close to that of the PWM boost converter. To show the influence of D_1 value on the voltage-conversion ratio, Fig. 4.3 (b) shows the voltage-conversion ratio of the ZVT-PWM boost converter with D_1 increased to 15%. It can be see that for a given D value, the voltage-conversion ratio increases as D_1 increases.

The bold lines shown in Fig. 4.3 (a) and (b) represent the boundary conditions given by Eq. (4.16). It means that the duty cycle range of the ZVT boost converter is limited in order to achieve ZVS for a given D_1 value. One intuitive explanation follows: for a fixed output voltage, the input current of the converter increases as D increases or the input voltage decreases; thus according to Eq. (4.12), ΔT_{01} also increases. On the other hand, in order for the ZVT-PWM converter to achieve soft-switching, the maximum ΔT_{01} is limited for a given D_1 value. Therefore, for a given D_1 value, the ZVS line/load range of the ZVT boost converter is also limited. Besides, it is obvious that the ZVS

line/load range of the ZVT-PWM boost converter can be extended if D_1 value is increased. This can be clearly seen by comparing Fig. 4.3 (a) and Fig. 4.3 (b).

4.2.2.2. DC Voltage-Conversion Ratio Under Variable S1 On-Time Control

To minimize the conduction loss of S1, it is desirable to use variable on-time control for S1. In this approach, the on-time of S1 is kept minimum to maintain ZVS for the main switch. The on-time of S1 is given by:

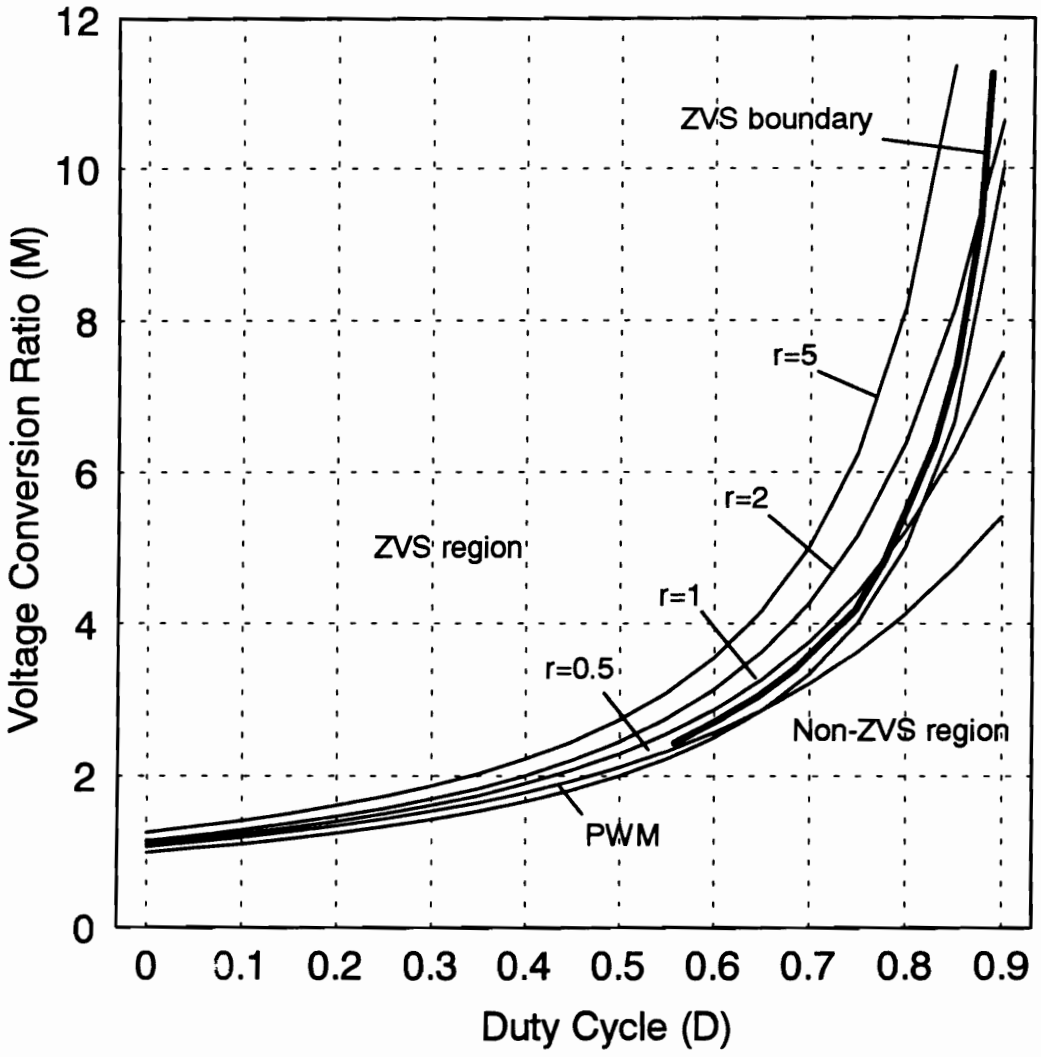
$$D_1 T_s = \Delta T_{01} + \Delta T_{12} = \frac{L_r I_i}{V_o} + \frac{1}{4} T_r. \tag{4.17}$$

Therefore, it should be regulated according to line voltage and load current variations. In a practical circuit, this can be easily done by sensing the main switch voltage or using feed-forward control. To sense the main switch voltage, the auxiliary switch should be turned off right after the main switch voltage drops to zero.

Substituting Eq. (4.17) into Eq. (4.14) yields:

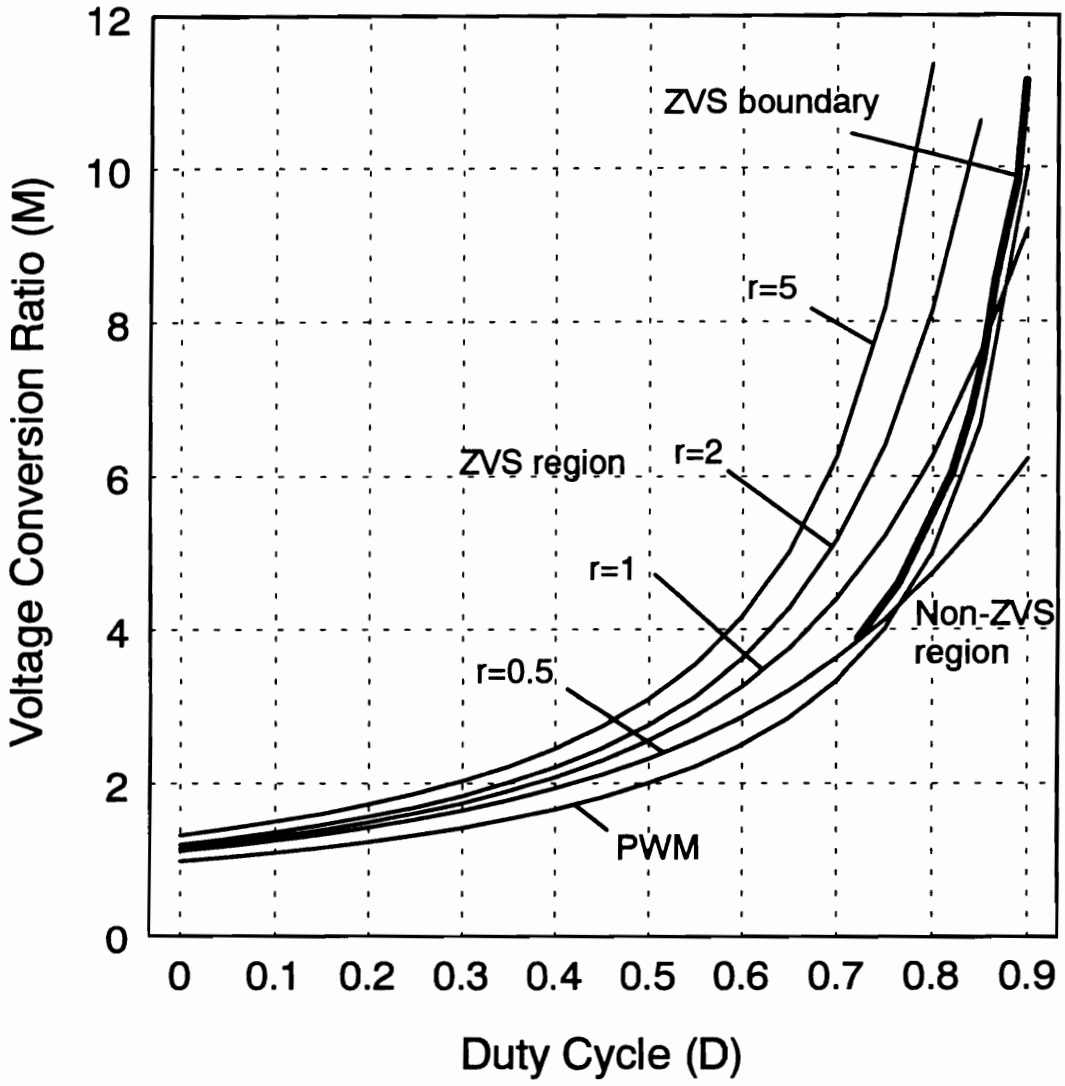
$$M = \frac{1}{1 - D - \frac{T_r}{2\pi T_s}\left(\frac{1}{2}\frac{r}{M} + 0.363\right)}. \tag{4.18}$$

Thus, the voltage-conversion ratio of the ZVT-PWM boost converter is given by:



(a)

Fig. 4.3. DC voltage-conversion ratio characteristics of the ZVT-PWM boost converter under fixed S1 on-time control and (a) T_r/T_s=10%, D1=10% , (b) T_r/T_s=10%, D1=15%



(b)

Fig. 4.3. DC voltage-conversion ratio characteristics of the ZVT-PWM boost converter under fixed S1 on-time control and (a) T_r/T_s=10%, D1=10% , (b) T_r/T_s=10%, D1=15%

$$M = \frac{1 + \frac{r}{4\pi}\frac{T_r}{T_s}}{1 - D - 0.058\frac{T_r}{T_s}}. \qquad (4.19)$$

Figure 4.4 shows the voltage-conversion ratio as a function of duty cycle (D) for T_r=20%T_S with the normalized load impedance (r) as a running parameter. It can be seen that the resultant voltage-conversion ratio characteristics are very close to the those exhibited by the PWM boost converter.

4.2.3. Design Guidelines for ZVT-PWM Boost Converter

4.2.3.1. Design Trade-Offs

From the circuit point of view, the ZVT-PWM boost converter can be considered to consist of two parts of circuitry: the main power stage and the auxiliary resonant branch. The main power stage transfers most of the output power, while the auxiliary branch transfers only a small portion of the output power. Due to the fact that the auxiliary branch is operated in deep discontinuous conduction mode, the power transfer of the auxiliary branch is not as efficient as that of the main power stage. Therefore, it is desirable to reduce the amount of energy that is processed by the auxiliary branch.

Since the operation of the ZVT-PWM boost converter resembles that of the PWM boost converter during most portions of the switching cycle, the design

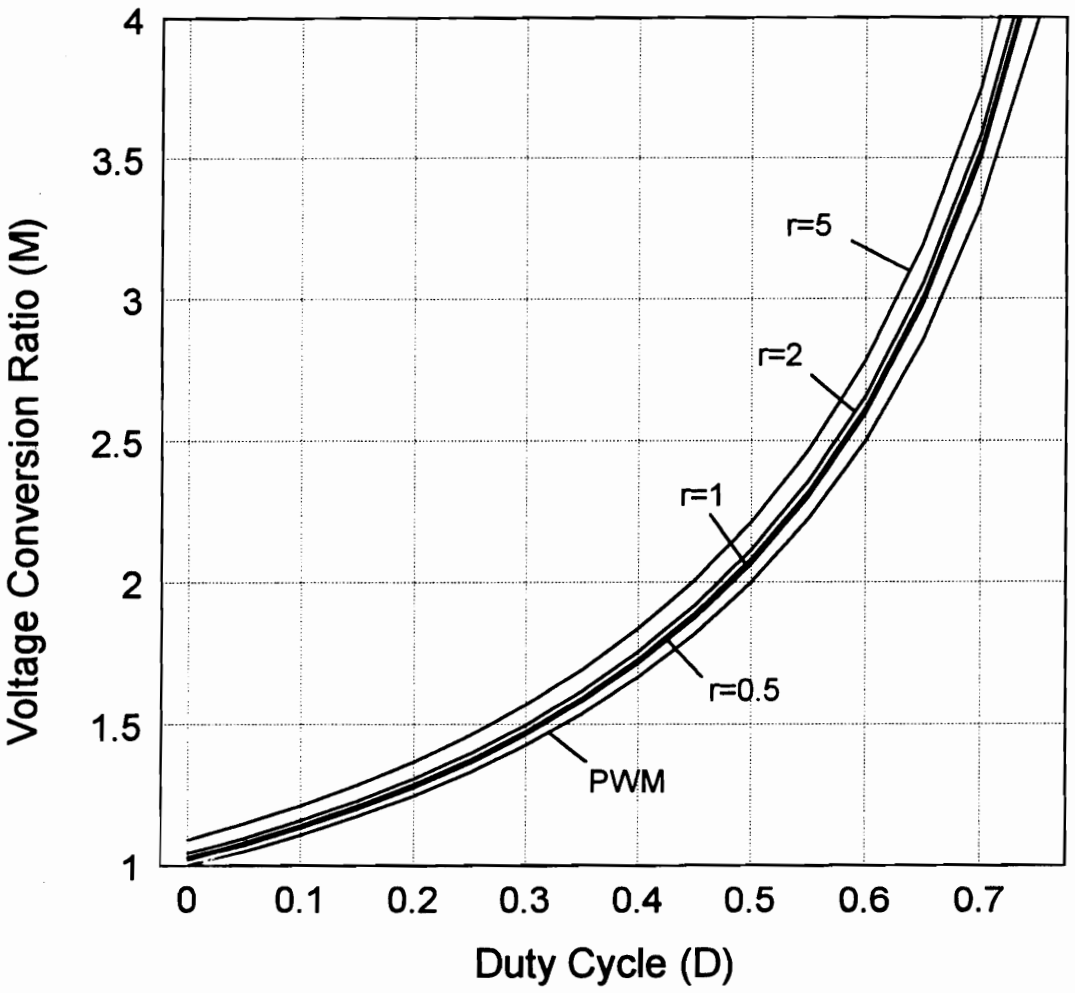


Fig. 4.4. DC voltage-conversion ratio of the ZVT-PWM boost converter with T_r/T_S=20% under variable S1 on-time control.

of major power stage components of the ZVT-PWM boost converter is similar to the PWM converter. Due to the fact that the auxiliary branch is only activated for a short period of resonant transition time, and that it only processes a small portion of the output power, the selection of these auxiliary components is generally not so critical. This section discusses some design trade-offs of the components in the auxiliary resonant network.

1. Selection of resonant capacitance

The resonant capacitance, C_r, consists of the output capacitance of the main switch, the junction capacitance of the rectifier diode, and the external resonant capacitor. The value of C_r affects the dv/dt during the switching transition, which in turn affects the switching losses and the conducted and radiated EMI noise. A larger C_r reduces the switching losses and switching noise, but it also increases losses in the auxiliary resonant network. Referring to Fig. 4.1, the peak current of the auxiliary switch, which is equal to the peak resonant inductor current, is given by:

$$I_{s1}^{peak} = I_i + \frac{V_o}{Z_n}. \tag{4.20}$$

From Eqs. (4.6) and (4.20) it can be seen that for a given L_r value, both the peak current stress and the conduction time of the auxiliary switch will increase if C_r increases.

When the main switch is implemented by a power MOSFET, the switching loss of the switch is negligible if the gate-drive impedance is sufficiently low. The output capacitance of the MOSFET can be used as the resonant capacitance, and no external resonant capacitance is needed. In this way, the amount of energy handled by the auxiliary network is minimized, and the circuit efficiency is optimized.

When the main switch is implemented by an IGBT, however, the selection of C_r becomes more critical, since the IGBT switching loss is sensitive to dv/dt at turn-off. With ZVS, the turn-on loss of the IGBT is completely eliminated regardless of the C_r value. Although ZVS does not completely eliminate IGBT turn-off loss, it can reduce the turn-off loss by several times if enough external resonant capacitance is added. Obviously, the use of a larger C_r results in less IGBT turn-off loss. On the other hand, a larger C_r also increases the power loss in the auxiliary network, as explained above. Therefore, the selection of the optimum C_r value depends on the switching characteristics of the IGBT device used.

2. Selection of resonant inductor

The value of the resonant inductance, L_r, affects the conduction time of the auxiliary switch, the peak current stress of the auxiliary switch, and switching *di/dt* and *dv/dt* at diode D turn-off. From Eq. (4.5) it can be seen that a larger L_r value leads to longer conduction time of the auxiliary switch and thus more conduction loss in the auxiliary branch. However, it also reduces the peak current stress of the auxiliary switch and results in lower *di/dt* and *dv/dt* at diode D turn-off.

3. Selection of auxiliary switch

Since the auxiliary switch only handles a small amount of resonant-transition energy, it can be implemented by a MOSFET with a relatively low current rating. Although using a big MOSFET would help to reduce the conduction loss of the auxiliary switch, it is not desirable, since it would cause more capacitive turn-on loss and increase circuit cost. In addition, the use of a bigger MOSFET would enhance the parasitic ringing between the output capacitance of the auxiliary switch and the resonant inductor. This would result in more loss in the auxiliary network, as will be explained in section 4.2.3.3.

4.2.3.2. Design Procedure for ZVT-PWM Boost Converter

In general, the design of the ZVT-PWM converters is much easier and more flexible than that of most resonant converters. Based on the trade-offs described in the previous section, the following design procedure can be established for the ZVT-PWM boost converter. This design procedure is also applicable to other ZVT-PWM topologies.

1. Design the main power stage components.

   The basic design of the main power stage components is similar to that of the PWM boost converter. One of the design considerations is the selection of the power switch. For some applications where the circuit efficiency is an important concern, the power switch can be oversized to reduce the

conduction loss without a penalty of increased capacitive turn-on loss due to ZVS operation. Regarding the selection of the rectifier diode, a relative slow diode that is typically less expensive diode and has a lower forward drop can be used because of soft-switching operation.

2. Select the resonant capacitance.

   When the power switch is implemented by a MOSFET, the selection of the resonant capacitance mainly depends on the speed of the gate driver. If the output impedance of the gate-driver is sufficiently low, which is the case when a separate fast driver is used as the gate-driver, the output capacitance of the power MOSFET can be used as the resonant capacitance. If the power MOSFET is directly driven by the PWM control IC (which is typically slow), an external resonant capacitor should be used to reduce the turn-off switching loss. The value of the external capacitor can be selected at about two to three times as high as the output capacitance of the MOSFET.

3. Select the resonant inductance.

   The value of the resonant inductance can be selected based on the recovery softness of the rectifier diode used. This value is difficult to calculate accurately because of the recovery characteristics variation among different rectifiers. A good starting point is to set the diode turn-off *di/dt* rate, V_0/L_r, at a value that is two or three times lower than the *di/dt* value under which the reverse-recovery time is specified in the manufacturer's data book.

4. Select the auxiliary switch.

   The auxiliary switch can be sized to have a current rating that is equal to about one third of the main switch.

5. Select the auxiliary diode.

   The auxiliary switch is selected based on the peak current stress that is given by Eq. (4.19). Since the auxiliary diode only carries low average current, the current rating of the auxiliary switch can be much lower than that of the main rectifier diode.

4.2.3.3. Practical Considerations

In practice, the ZVT-PWM boost converter shown in Fig. 4.1 has a problem. That is, due to the interaction between the output capacitance of the auxiliary and the resonant inductance, part of the input current flows though the auxiliary diode (D1) instead of the main diode (D) during the freewheeling time (T6-T0). As a result, the auxiliary diode suffers from a reverse-recovery problem, which causes considerable switching losses and noise in the auxiliary resonant branch.

Figure 4.5 shows the real circuit waveforms of the ZVT-PWM boost converter with the output capacitance of S1 taken into consideration. During time interval T3-T4, the energy stored in the resonant inductor is transferred to

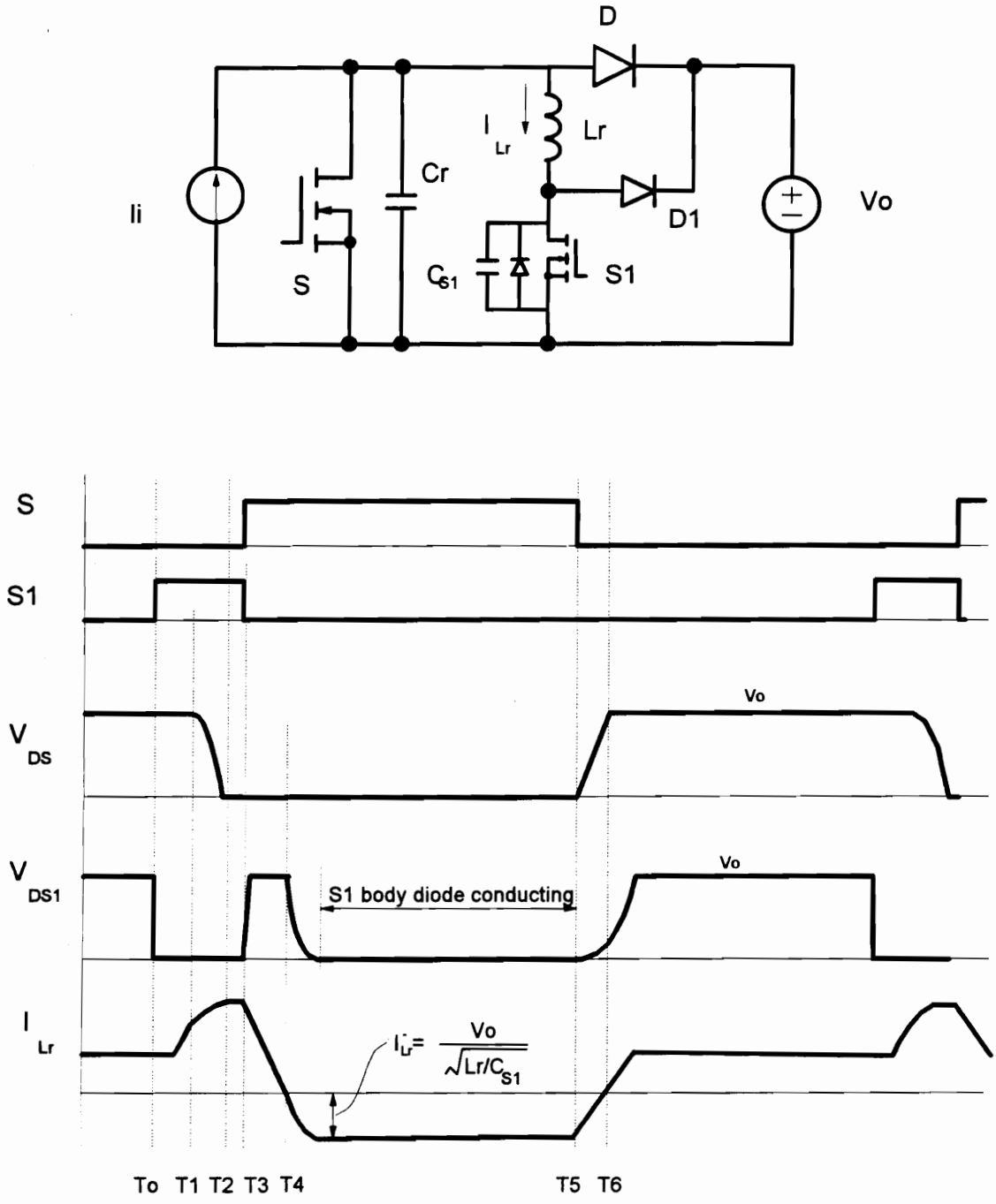


Fig. 4.5. Circuit waveforms of the ZVT-PWM boost converter with the output capacitance of the auxiliary switch taken into consideration.

the load. The auxiliary diode (D1) is on, and the output capacitance of S1, C_{S1}, sees the output voltage. When L_r current decays to zero at T4, C_{S1} starts to resonate with L_r. This resonance lasts until the C_{S1} voltage drops to zero, where the L_r current starts to freewheel through the anti-parallel diode of S1. The amplitude of this negative L_r current is given by:

$$I_{L_r}^{-} = \frac{V_0}{\sqrt{L_r / C_{S1}}}. \tag{4.21}$$

It can seen that it is desirable to use an auxiliary switch with smaller C_{S1} in order to minimize $I_{L_r}^{-}$. This negative L_r current continues to freewheel through the slow body diode of S1 until T5, where S is turned off and the drain voltage of S increases up to V_O. As a result, the body diode of S1 suffers from a reverse-recovery problem. To solve this problem, a small, fast-recovery blocking diode (D2 in Fig. 4.6) can be used in series with L_r or S1 to prevent the slow body diode of S1 from conduction.

With the use of D2, the C_{S1} voltage does not go down to zero during the time the main switch conducts. However, it is still lower than the output voltage. After the main switch is turned off and its drain voltage rises to V_O at T6, C_{S1} and L_r form another partial resonance. Due to this resonance, L_r builds up certain current at the time C_{S1} is charged up to V_O. This current freewheels thought the auxiliary diode D1 until S1 is turned on at T0. As a result, D1 suffers from a reverse-recovery problem. To resolve this problem. a saturable reactor can be used in series with the resonant inductor. Since the saturable reactor is

a high-impedance component, the current flows through D1 during the freewheeling time (T6-T0) becomes negligible.

Another effective way to solve the above-mentioned problem is to insert a couple inductor in the resonant branch, as described in [F30].

4.2.4. Experimental Results

A 300 kHz, 600 W ZVT-PWM boost dc-dc converter has been implemented to demonstrate the operation. It is regulated at 300 V output with a 150-200 V input range. The power stage circuit diagram is given in Fig. 4.6, where L_S is a saturable reactor used to eliminate the ringing between L_r and S1 output capacitance. It is implemented with five turns on a Toshiba "Spike Killer" core, SA10x6x4.5. The fast-recovery diode D2 is used to prevent the conduction of S1 body diode. It should be noted that the current rating of the auxiliary switch (IRF730, 400 V, 5.5 A) is much lower than that of the main switch (IRFP 350, 400 V, 16 A).

Figure 4.7 shows the oscillograms of the breadboarded circuit operating at full load and 165 V input. It can be seen that all the waveforms are quite clean and agree well with the theoretical analysis. Both the power MOSFET and the rectifier diode operate with ZVS for the full line range and load range. The breadboarded converter achieved a remarkable maximum overall efficiency of 97.5% at full load and high line. Compared to the PWM version operating at the same input and output conditions, the circuit efficiency is improved by 2-3%. Moreover, the ZVT-PWM converter is much less noisy.

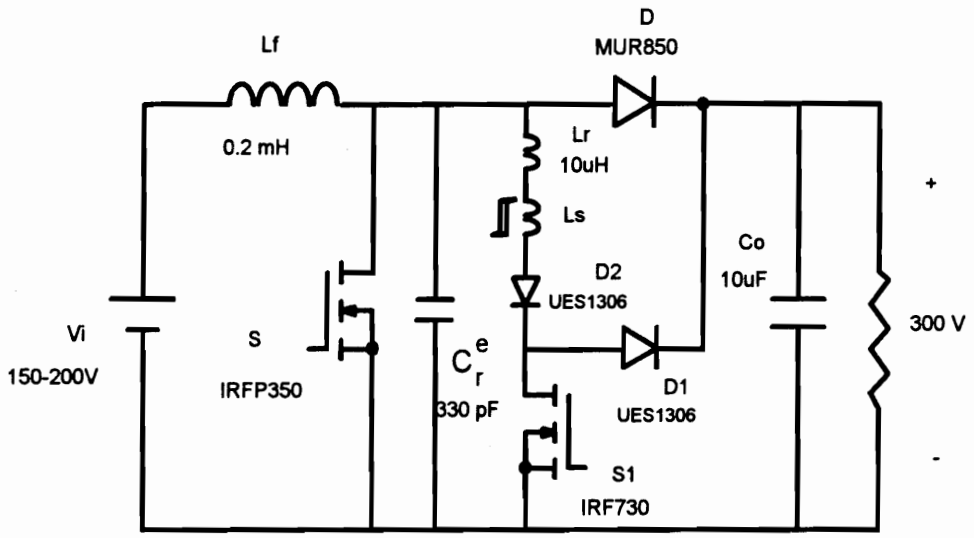


Fig. 4.6. Circuit diagram of the 300 kHz, 600 W experimental boost ZVT-PWM converter.

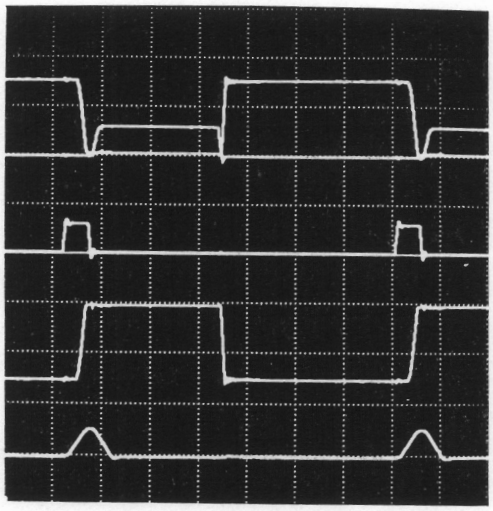


Fig. 4.7. **Oscillograms of the 300 kHz, 600 W experimental boost ZVT-PWM converter at full load and 175 V input.**
1st waveform: V_{ds}, 200 V/div;
2nd waveform: V_{gs}, 20 V/div;
3rd waveform: V_{gs1}, 20 V/div;
4th waveform: V_D, 200 V/div;
5th waveform: I_{Lr}, 5 A/div.

Figure 4.8 shows the circuit diagram of a 100 kHz, 600 W PFC circuit using the ZVT-PWM boost topology. To reduce the cost of the circuit, an IR TO-220 package IGBT, IRGBC30U, is used as the power switch. To reduce the IGBT turn-off loss and further reduce EMI noise, a 4.4 nF external resonant capacitor (C_{re}) is used to soften the switching actions. Although the auxiliary switch has a low rms current, it should still be implemented by a MOSFET, since it is subjected to high turn-off current. The breadboarded circuit is regulated at 380 V output with a 90-260 VAC universal input range.

To compare the performance of the ZVT PFC circuit with that of the PWM circuit, the auxiliary resonant branch is removed. To achieve good thermal stability, the 20 W heatsink used for the IGBT device in the ZVT circuit is replaced by a 40 W one. Figure 4.9 shows the efficiency measurement of two PFC circuits. It can be seen that the ZVT technique significantly improves the circuit efficiency. Moreover, owing to soft-switching operation, the ZVT circuit also significantly reduces circuit switching noise. It is interesting to compare the performance of the ZVT-PWM boost converter with that of the PWM boost converter using a passive snubber. It was concluded in [F27] that the ZVT technique is more effective in improving circuit efficiency and reducing switching noise. For the ZVT-PWM boost converter, however, the price paid is the addition of a small auxiliary switch.

It should be noted that the efficiency of the PFC circuit is strongly dependent on the line range. When the ZVT PFC circuit shown in Fig. 4.8 is operated at 100 kHz, 1kW with a 180-260 VAC input range (European line range), it can achieve a 97-98% overall efficiency [F29].

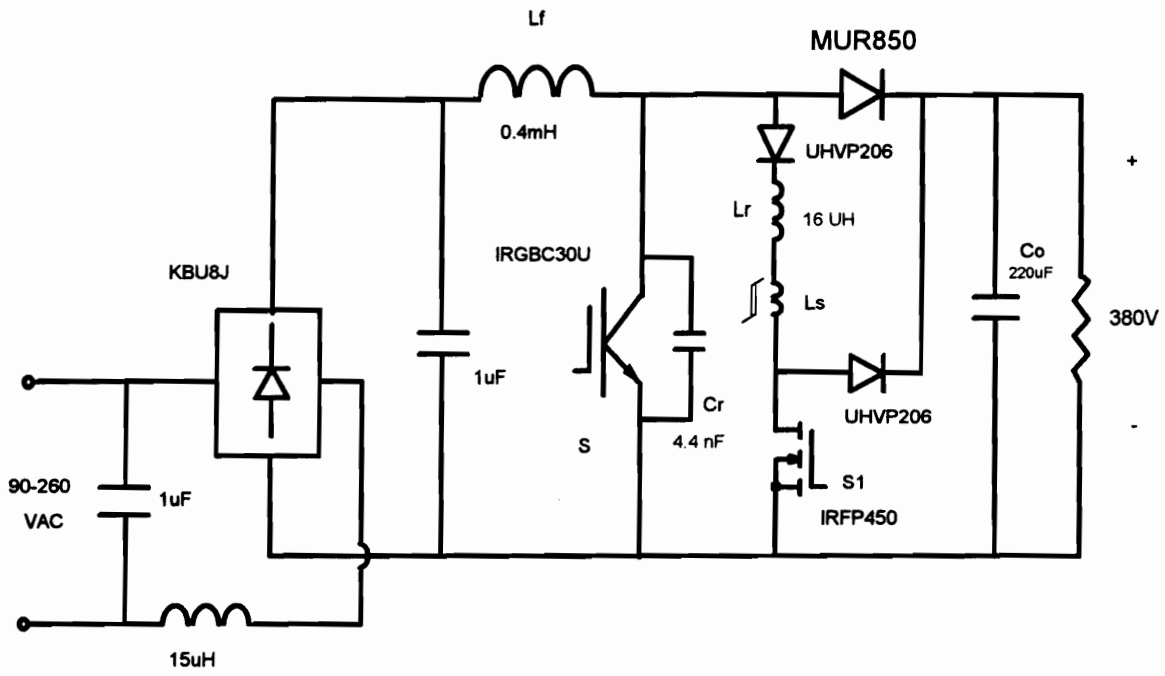


Fig. 4.8. Circuit diagram of the 100 kHz, 600 W PFC circuit using ZVT-PWM converter and IGBT.

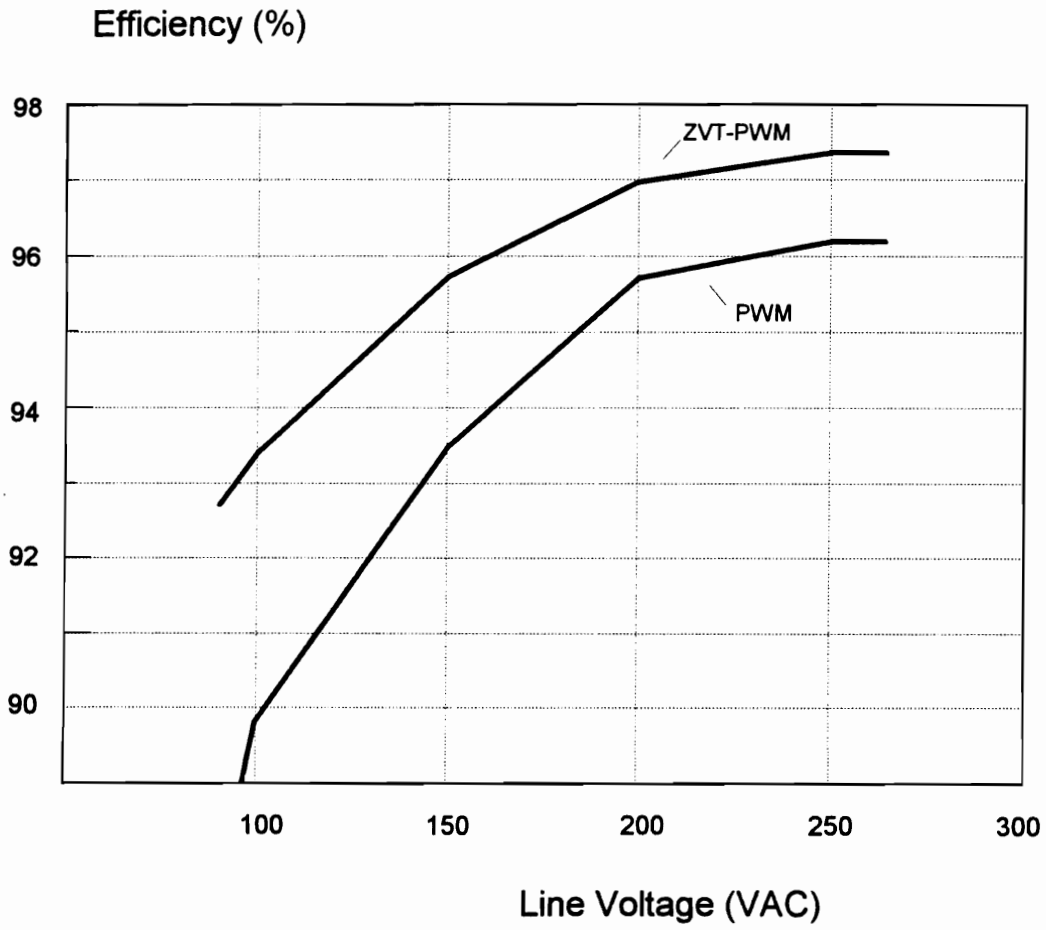


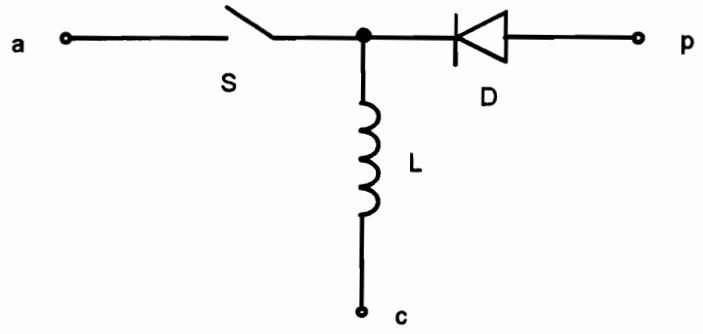
Fig. 4.9. Efficiency comparison of 100 kHz IGBT PFC circuits using ZVT-PWM boost converter and conventional PWM boost converter.

4.3. A Family of ZVT-PWM Converters

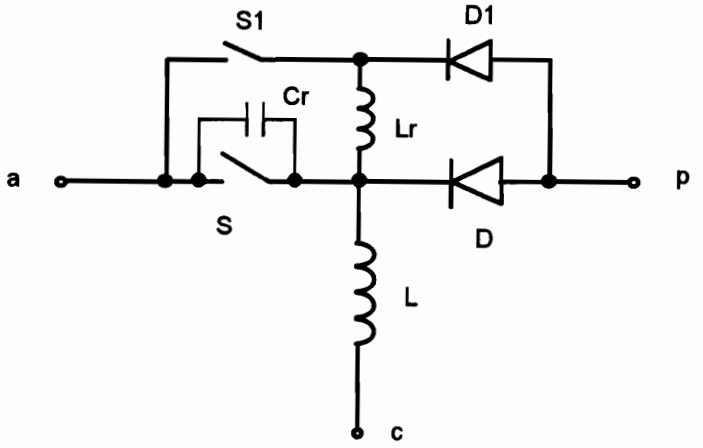
The switching cells shown in Fig. 4.10 can be used to generalized the ZVT concept described above. Shown in Fig. 10(a) is the well-known PWM switching cell from which PWM topologies can be derived. The ZVT-PWM switching cell is derived by adding a shunt branch which consists of an auxiliary switch S1, an auxiliary diode D1, a resonant capacitor C_r, and a resonant inductor L_r, as shown in Fig. 4.10(b). According to the capacitor-shift rule, the resonant capacitor can also be placed across the rectifier diode in Fig 4.10(b). The function of this shunt branch is to create a partial resonance during short switching transition time to achieve ZVS condition. The principle of operation of the ZVT-PWM switching cell has been illustrated by using the boost topology as an example in the previous section.

By replacing the PWM switching cell in a PWM converter with the ZVT-PWM switching cell shown in Fig. 4.10(b), a family of ZVT-PWM converters are derived. Figure 4.11 shows six basic ZVT-PWM topologies. The principle of operation of the new converters is similar to that of the ZVT-PWM boost converter.

It has been pointed out that the switches in a ZVT-PWM converter are subjected to minimum voltage stresses which are the same as those in their PWM counterparts. This feature can be explained by using the sub-circuit shown in Fig. 4.12(a), which can be extracted from a PWM topology simply by



(a)



(b)

Fig. 4. 10. (a) The PWM switching cell, and (b) the ZVT-PWM switching cell.

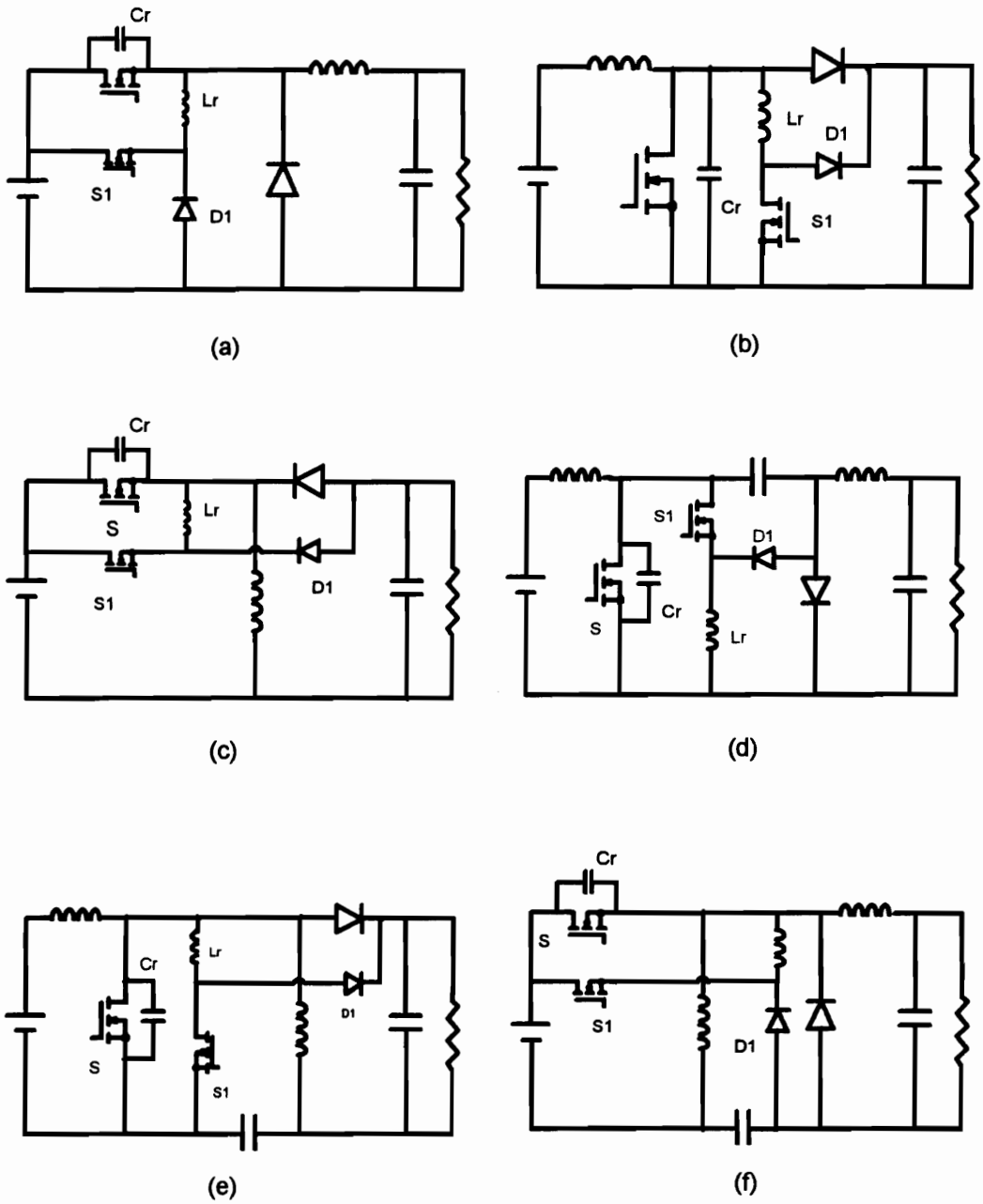


Fig. 4.11. Six basic topologies of the ZVT-PWM converters: (a) buck, (b)boost, (c)buck-boost, (d) Cuk, (e) Sepic, and (f) Zeta.

opening the filter inductor(s). In Fig. 4.12(a), S is the active switch with a body diode D_S, D is the rectifier diode, and V_{DC} is a dc voltage source that represents the input/output voltage or the filter capacitor voltage. It is obvious that the maximum voltage across the active switch or the diode cannot exceed V_{DC}. Therefore, the switches in any converter containing this sub-circuit suffer from the voltage stresses the same as those in its PWM counterpart. A ZVS-QSC or a ZVT-PWM converter contains this sub-circuit; thus, their switches are subjected to minimum voltage stresses.

Figure 4.12(b) shows another sub-circuit extracted from a ZVS-QRC by opening the filter inductor(s), where L_r is a resonant inductor and C_r is a resonant capacitor. Due to the presence of the resonant inductor, the maximum voltage stress of S is not limited to V_{DC} any more. Similarly, a ZVS-PWM converter or a ZVS-MRC also contains such a sub-circuit; thus, the power switch can be subjected to a voltage stress that is much higher than that in its PWM counterpart.

Figure 4.13 shows several isolated topologies of the ZVT-PWM converters. In these isolated ZVT-PWM converters, since the active switch and the rectifier diode do not share a common ground, a coupled-inductor serving as the resonant inductor is used to transfer the resonant-transition energy to input source or the energy-storage capacitor in primary side. Although this part of energy can also be delivered to the load by placing D1 and L_r secondary across the output filter capacitor, it is normally not desirable, since this coupled inductor has to meet high-voltage isolation requirement in this case. Similarly to the ZVS-QSC technique, the limitation of the isolated ZVT-PWM converters is that

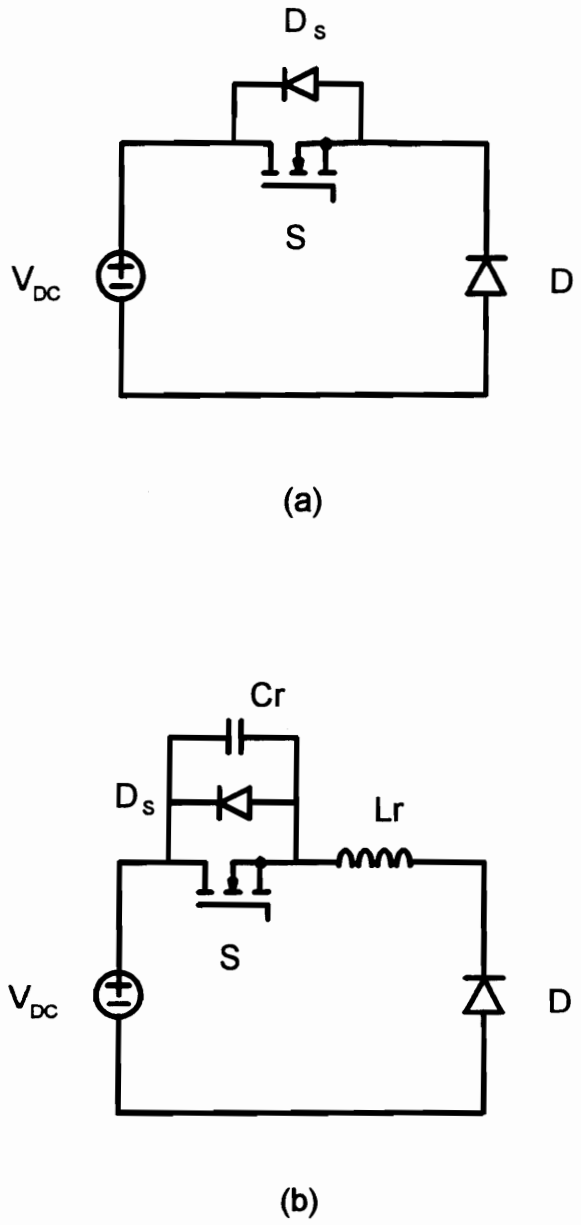


Fig. 4.12. (a) A sub-circuit extracted from a PWM converter; (b) A sub-circuit extracted from a ZVS-QRC.

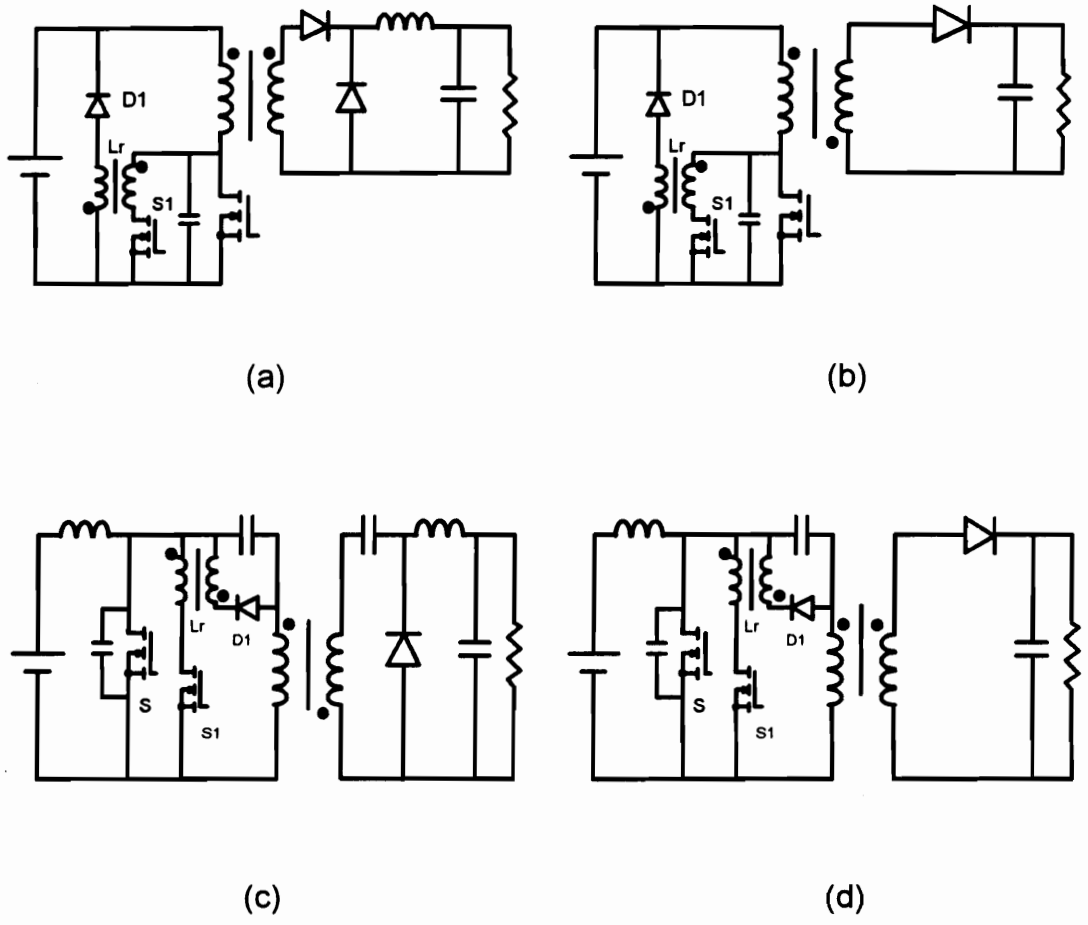


Fig. 4.13. Several isolated ZVT-PWM topologies: (a) forward, (b) flyback, (c) Cuk, and (d) SEPIC.

they do not utilize the leakage of the power transformer. Therefore, the transformer should be designed with a minimum leakage. The leakage inductance of a transformer, as well as its ac winding resistance (which determines the copper loss), can be minimized by using the interleaving technique, at the penalty of much increased winding capacitances. When the conventional PWM technique is used, the energy stored in these winding capacitances will be dissipated in the switches, thus significantly increasing the capacitive turn-on loss. Using the ZVT-PWM converter technique, these winding capacitances become part of C_r; thus, they do not cause additional switching loss.

Figure 4.14 shows the FB-ZVT-PWM converter and its switch gate-drive signals. In this diagram, S_a and S_b are two auxiliary switches, and D_a and D_b are two auxiliary diodes. The operations of two half-bridges are completely symmetrical. When two diagonal main switches are conducting, the lower switch of the bridge (S2 or S3) is always turned off first, so that ZVS of the corresponding upper switch in the same leg is accomplished by discharging the resonant capacitor by the reflected output filter inductor current. ZVS of the lower-arm switch of the totem pole, however, is achieved by transferring the energy stored in the resonant capacitor through the auxiliary resonant network to the input source prior to its turn-on. To reduce secondary parasitic ringing, it is desirable to minimize the transformer leakage inductance. If the transformer leakage is sufficiently low, the junction capacitance of the rectifier diodes can be reflected to the primary and becomes part of the resonant capacitor. Compared to the FB-ZVS-PWM converter, the FB-ZVT-PWM converter has several advantages:

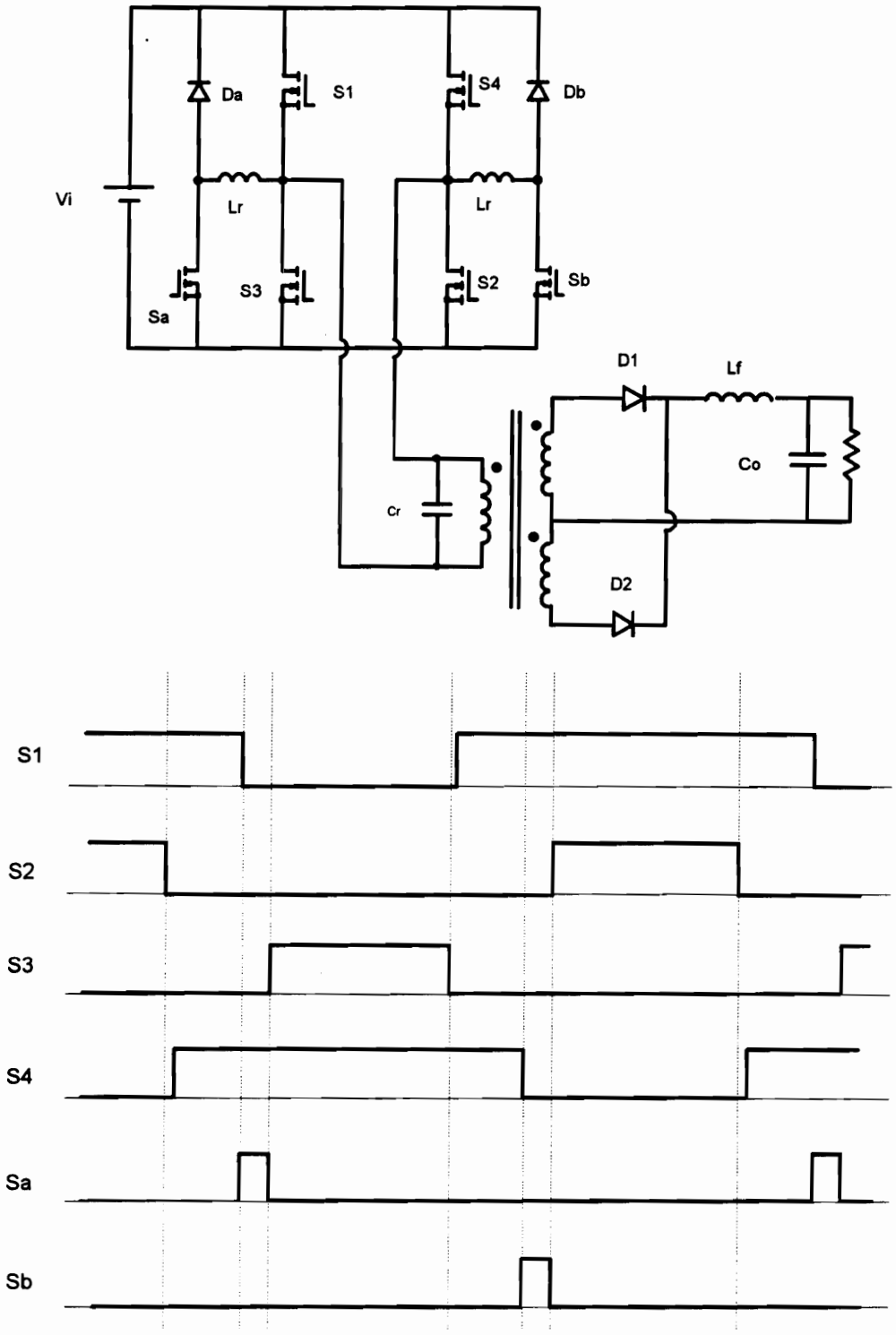


Fig. 4.14. Full-bridge ZVT-PWM converter.

a) much less circulating energy, since no resonant inductor is used in the main power path;
b) no severe secondary parasitic ringing;
c) soft-switching for the rectifier diodes, and
d) soft-switching operation maintained for the entire line range and load range.

These features make the new topology attractive for high-power applications, especially when IGBTs or BJTs are used as the main switches.

Another interesting topology is the current-fed FB-ZVT-PWM converter, which can also be referred to as "FB-ZVT-PWM boost converter". The circuit diagram and its waveforms are shown in Fig. 4.15. The principle of operation of this converter is very similar to that of the ZVT-PWM boost converter. Due to the use of the auxiliary network, all the power switches and the rectifier diodes are commutated under ZVS. Since this is a current-fed converter, it is suited for PFC applications. Similarly, this concept can also be extended to the two-switch isolated boost converter (Clarke converter).

The proposed ZVT technique can be applied to any dc-dc, dc-ac, ac-dc, or ac-ac power conversion topology [F29-F32].

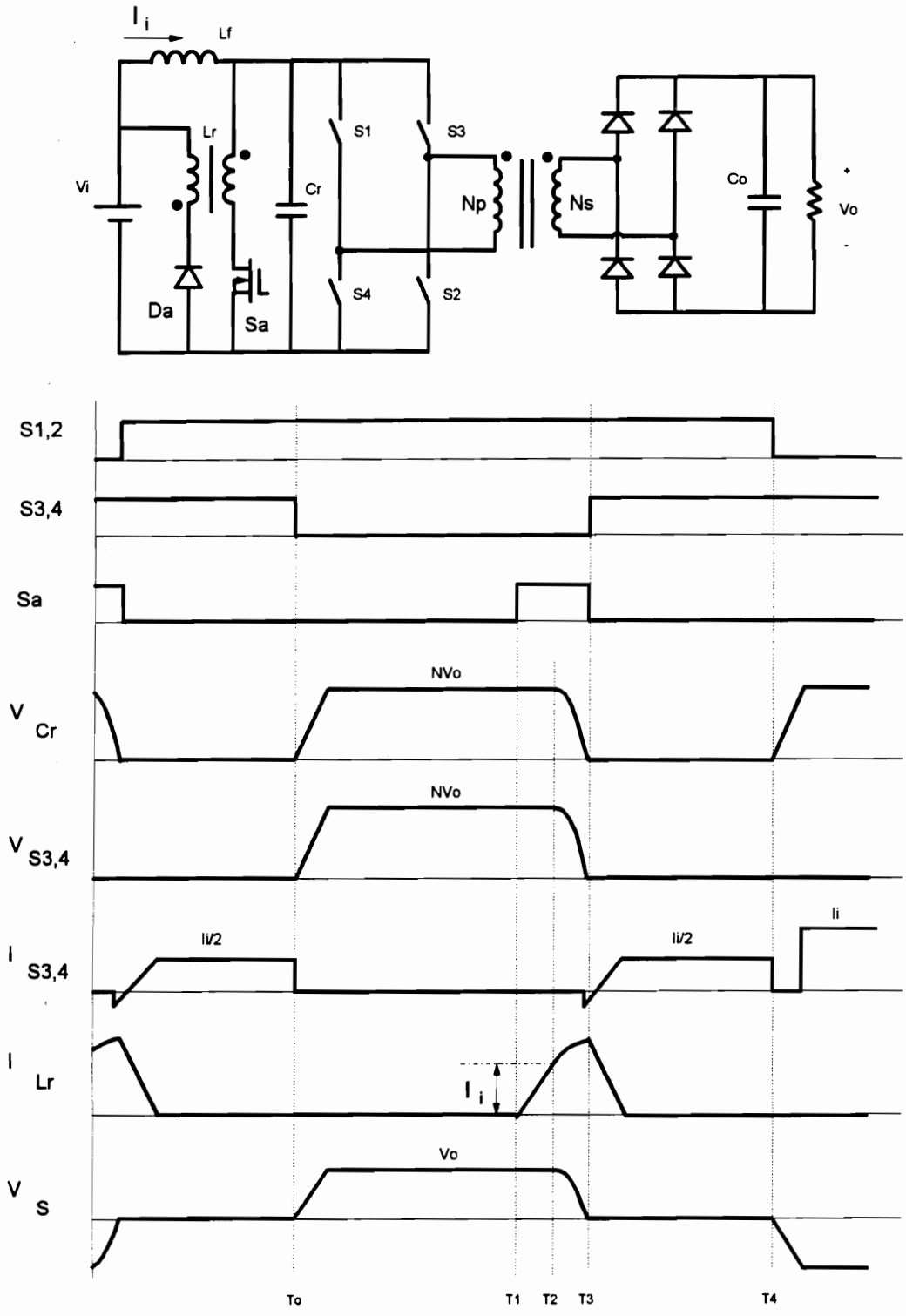


Fig. 4.15. Current-fed FB-ZVT-PWM converter and its waveforms.

4.4 Small-Signal Analysis of ZVT-PWM Converters

4.4.1. Method of Analysis

In this section, the small-signal characteristics of ZVT-PWM converters are analyzed by using the boost topology as an example. The basic approach utilized to perform this analysis is the *equivalent controlled-source averaging method*, which is an extension of the *state-space averaging method*. In this approach, each switch (active or passive) is replaced by a controlled voltage source or a controlled current source whose value is equal to the average voltage or current of the switch over a switching period. To simplify the analysis, it is assumed that:

a) all power stage components are ideal, i.e., all parasitic resistances are zero, and the semiconductor devices have zero conduction voltage drops and zero switching times;
b) the converter is operated in the continuous conduction mode;
c) the resonant transition time of the ZVT-PWM boost converter is relatively short compared to the switch period (typically 5-30% of the switching period); and
d) the converter uses fixed S1 on-time control, i.e., the duty cycle of S1, D_1, is a constant.

4.4.2. Small-Signal Model

For simplicity, the main power switch S in Fig. 4.1 is modeled by using a controlled voltage source, and S1, D, and D1 by a controlled current source.

A. Modeling of the power switch

Based on the operating waveforms of the ZVT-PWM boost converter shown in Fig. 4.1, the average voltage across the main switch over a switching period is derived as:

$$v_s = \left(1 - d - D_1 - \frac{\Delta T_{56}}{2T_S} + \frac{\Delta T_{01}}{T_S} + \frac{2}{\pi}\frac{\Delta T_{12}}{T_S}\right)v_o, \tag{4.22}$$

where d is the duty cycle of the main switch, and ΔT_{01}, ΔT_{12}, and ΔT_{56} are given by Eqs. (4.1), (4.4) and (4.7), respectively. By introducing small-signal perturbations on d and v_i, we can get small-signal perturbations on ΔT_{01}, ΔT_{12}, ΔT_{56} , v_o, and v_s:

$$d = D + \hat{d},$$

$$v_i = V_i + \hat{v}_i,$$

$$\Delta T_{01} = \overline{\Delta T_{01}} + \Delta \hat{T}_{01},$$

$$\Delta T_{12} = \overline{\Delta T_{12}} + \Delta \hat{T}_{12},$$

$$\Delta T_{56} = \overline{\Delta T}_{56} + \Delta \hat{T}_{56},$$

$$v_o = V_o + \hat{v}_o,$$

$$i_L = I_L + \hat{i}_L,$$

and

$$v_s = V_s + \hat{v}_s.$$

From Eqs. (4.1), (4.4) and (4.7), $\Delta \hat{T}_{01}$, $\Delta \hat{T}_{12}$, and $\Delta \hat{T}_{56}$ can be derived as:

$$\Delta \hat{T}_{01} = \frac{L_r}{V_o} \hat{i}_L - \frac{L_r i_L^{T_1}}{V_o^2} \hat{v}_o, \tag{4.23}$$

$$\Delta \hat{T}_{12} = 0, \tag{4.24}$$

and

$$\Delta T_{56} = \frac{C_r}{i_L^{T_5}} \hat{v}_o - \frac{C_r V_o}{\left(i_L^{T_5}\right)^2} \hat{i}_L, \tag{4.25}$$

where $i_L^{T_1}$ and $i_L^{T_5}$ are the input inductor currents at times T_1 and T_5, which are approximately:

$$i_L^{T_1} \approx I_L + \frac{(D + D_1) V_i T_s}{2 L_f}, \tag{4.26}$$

$$i_L^{T_5} \approx I_L - \frac{(D + D_1) V_i T_s}{2 L_f}. \tag{4.27}$$

Substituting Eqs. (4.23)-(4.27) into Eq. (4.22) yields:

$$\hat{v}_s = \left(\frac{Vi}{Vo} - \frac{C_r}{2T_s i_L^{T_5}} - \frac{L_r i_L^{T_1}}{T_s V_o^2} \right) \hat{v}_o - V_o \hat{d} + \left(\frac{C_r V_o^2}{2T_s \left(i_L^{T_5} \right)^2} + \frac{L_r}{T_s} \right) \hat{i}_L . \tag{4.28}$$

Normally, the values of the second and third terms in the first parentheses on the right side of Eq. (4.28) are negligible compared to that of the first term. Therefore, the equation can be simplified to:

$$\hat{v}_s \approx \frac{Vi}{Vo} \hat{v}_o - V_o \hat{d} + \left(\frac{C_r V_o^2}{2T_s \left(i_L^{T_5} \right)^2} + \frac{L_r}{T_s} \right) \hat{i}_L . \tag{4.29}$$

B. Modeling of the rectifying diode

From Fig. 4.1, the average current flowing through the rectifying diode D is:

$$i_D = \left(1 - d - D_1 - \frac{\Delta T_{56}}{T_s} + \frac{\Delta T_{01}}{2T_s} \right) i_L . \tag{4.30}$$

By introducing a small-signal perturbation on d and v_i, we get a corresponding small-signal perturbations on i_D:

$$\hat{i}_D = -I_L \hat{d} + \frac{V_i}{V_o} \hat{i}_L + \frac{I_L}{T_s} \left(\frac{C_r}{i_L^{T_5}} - \frac{L_r i_L^{T_1}}{2V_o^2} \right) \hat{v}_o . \tag{4.31}$$

The coefficient of the third term on the right side of Eq. (4.31) is usually very small; thus the equation can be approximated by:

$$\hat{i}_D \approx -I_L\hat{d} + \frac{V_i}{V_o}\hat{i}_L. \tag{4.32}$$

C. Modeling of the auxiliary switch and the auxiliary diode

The average currents flow through S1 and D1 are respectively given by:

$$i_{S1} = \frac{\Delta T_{01}}{2T_s} i_L^{T_1} + \frac{\Delta T_{12}}{T_s}\left(i_L^{T_1} + \frac{2}{\pi}\frac{V_o}{Z_n}\right) + \left(D1 - \frac{\Delta T_{01}}{T_s} - \frac{\Delta T_{12}}{T_s}\right)\left(i_L^{T_1} + \frac{V_o}{Z_n}\right), \tag{4.33}$$

and

$$i_{D1} = \frac{\left(i_L^{T_1} + \frac{V_o}{Z_n}\right)^2 L_r}{2V_o T_s}. \tag{4.34}$$

If small-signal perturbations are applied on d and v_i, the resultant small-signal perturbations on i_{S1} and i_{D1} are:

$$\hat{i}_{S1} = \left(D_1 - \frac{L_r i_L^{T_1}}{V_o T_s} - \frac{L_r}{Z_n T_s}\right)\hat{i}_L + \left(\frac{L_r (i_L^{T_1})^2}{2T_s V_o^2} + \frac{D_1}{Z_n} - \frac{0.09T_r}{T_s Z_n}\right)\hat{v}_o, \tag{4.35}$$

$$\hat{i}_{D1} = \left(\frac{L_r i_L^{T_1}}{T_s V_o} + \frac{L_r}{Z_n T_s}\right)\hat{i}_L + \frac{L_r}{2T_s}\left(\frac{1}{Z_n^2} - \left(\frac{i_L^{T_1}}{V_o}\right)^2\right)\hat{v}_o. \tag{4.36}$$

Normally, the coefficients of the second terms on the right side of these two equations are very small; thus, Eqs. (4.35) and (4.36) can be approximated by:

$$\hat{i}_{S1} \approx \left(D_1 - \frac{L_r i_L^{T_1}}{T_s V_o} - \frac{L_r}{Z_n T_s}\right)\hat{i}_L, \tag{4.37}$$

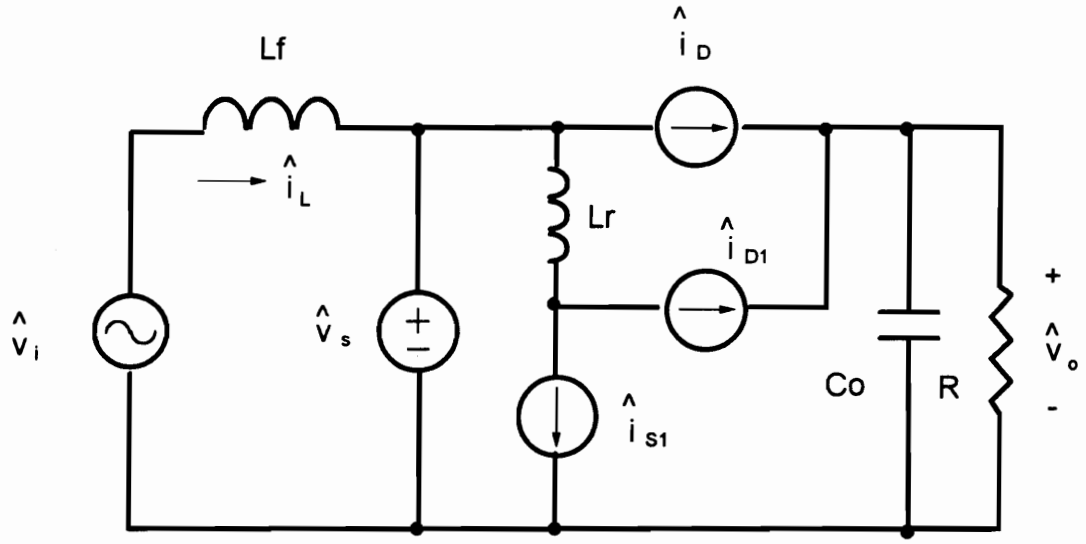
$$\hat{i}_{D1} \approx \left(\frac{L_r i_L^{T_1}}{T_s V_o} + \frac{L_r}{Z_n T_s} \right) \hat{i}_L. \tag{4.38}$$

The complete small-signal model of the ZVT-PWM boost converter is shown in Fig. 4.16, where $\hat{v}_s$, $\hat{i}_D$, $\hat{i}_{S1}$, and $\hat{i}_{D1}$ are given by Eqs. (4.29), (4.32) (4.37), and (4.38), respectively.

4.4.3. Small-Signal Characteristics of the Power Stage

Based on the small-signal model shown in Fig. 4.16, the small-signal characteristics of the ZVT-PWM boost converter can be easily simulated by using PSPICE. To illustrate the typical small-signal behavior of ZVT-PWM converters, a ZVT-PWM boost converter with the following specifications is simulated by using PSPICE:

- input voltage V_i=100 V,
- output voltage V_O=200 V,
- output power P_O=200 W,
- switching frequency f_S=100 kHz,
- input filter inductance L_f=840 uH, R_{Lf}=0.5 ohm,
- output filter capacitance C_f=44.7 uF,
- resonant inductance L_r=48 uH,
- resonant capacitance C_r=3.6 nF,
- auxiliary switch duty cycle D_1=15%.



$$\hat{v}_s = \frac{Vi}{Vo}\hat{v}_o - V_o\hat{d} + \left(\frac{C_r V_o^2}{2T_s\left(i_L^{T_5}\right)^2} + \frac{L_r}{T_s}\right)\hat{i}_L$$

$$\hat{i}_D = -I_L\hat{d} + \frac{V_i}{V_o}\hat{i}_L$$

$$\hat{i}_{Sl} = \left(D_l - \frac{L_r i_L^{T_l}}{T_s V_o} - \frac{L_r}{Z_n T_s}\right)\hat{i}_L$$

$$\hat{i}_{Dl} = \left(\frac{L_r i_L^{T_l}}{T_s V_o} + \frac{L_r}{Z_n T_s}\right)\hat{i}_L$$

Fig. 4.16. Small-signal model of the ZVT-PWM boost converter.

Figure 4.17 shows the control-to-output transfer functions of the PWM boost converter (dashed line) and of the ZVT-PWM boost converter (solid line). It can be observed that the differences between the dc gains and resonant peakings are apparent. To gain insight on how the shunt resonant network influences the power stage transfer function, the values of the resonant components (L_r and C_r) are changed to see the variations in control-to-output transfer functions. Figure 4.18 shows several control-to-output transfer functions of the ZVT-PWM boost converter with the resonant period (T_r) changing from 0% (for the PWM converter) to about 30% of the switching period while keeping the resonant impedance (Z_n) fixed. It can be seen that the double-pole is first damped and then split as the resonant period increases. This behavior is similar to that of the PWM boost converter using inductor current feedback control. One intuitively physical explanation follows: from Fig. 4.1, it can be seen that the switching transition times (ΔT_{01} and ΔT_{56}) of the ZVT-PWM boost converter are functions of the input inductor current. As a result, the effective duty cycle of the converter decreases as the input inductor current increases. This effect is similar to that of applying inductor current feedback in the control loop. Furthermore, as T_r increases, the effective duty cycle of the ZVT-PWM converter becomes more sensitive to inductor current change. As a result,, the differences in the small-signal characteristics between the PWM converter and ZVT-PWM boost converter also become more significant. Besides, it can be seen from Fig. 4.18 that for typical ZVT-PWM converter designs where T_r is only about 5-10% of the switching period, these differences are not quite significant.

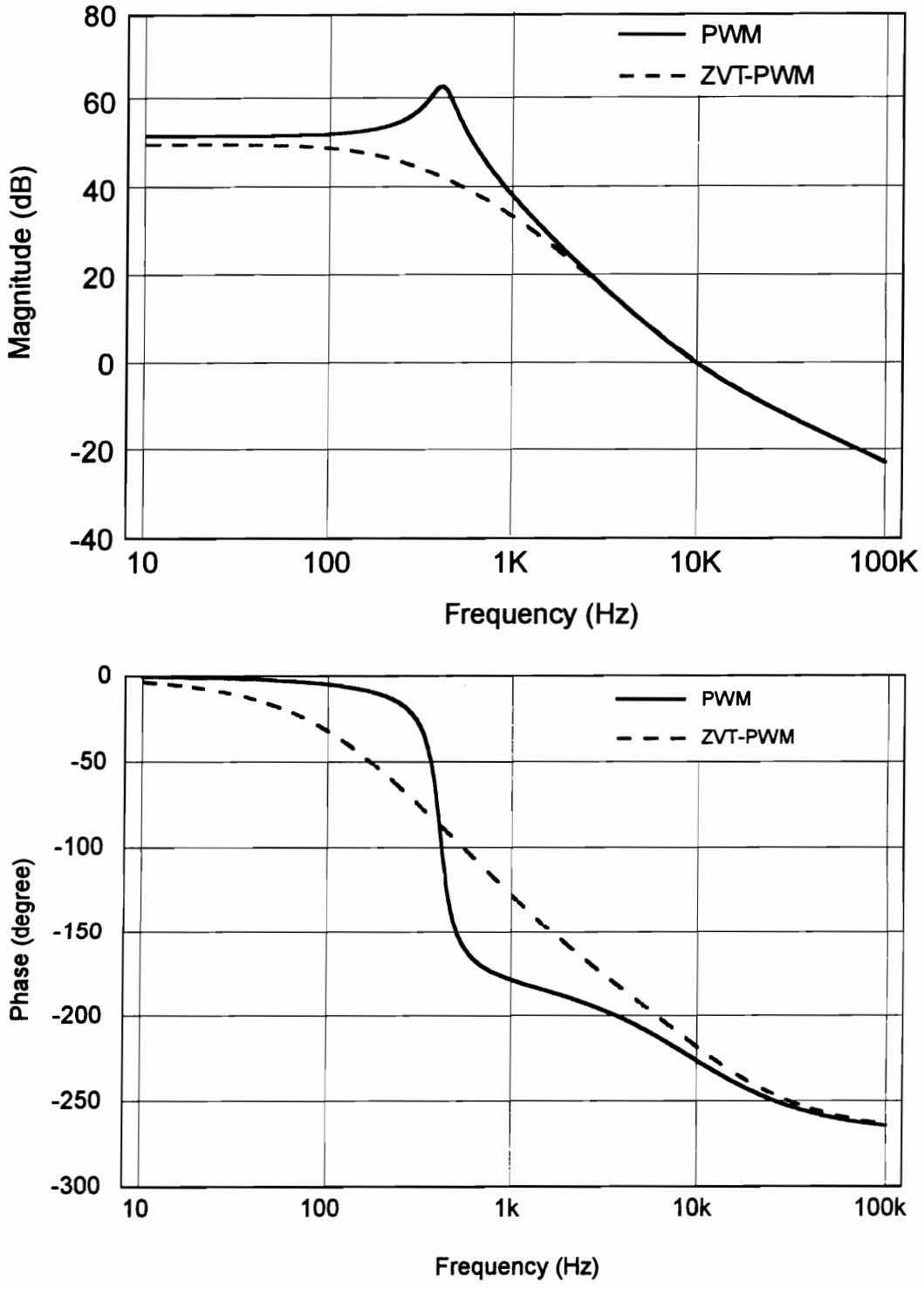


Fig. 4.17. Control-to-output transfer functions of the PWM and ZVT-PWM boost converters.

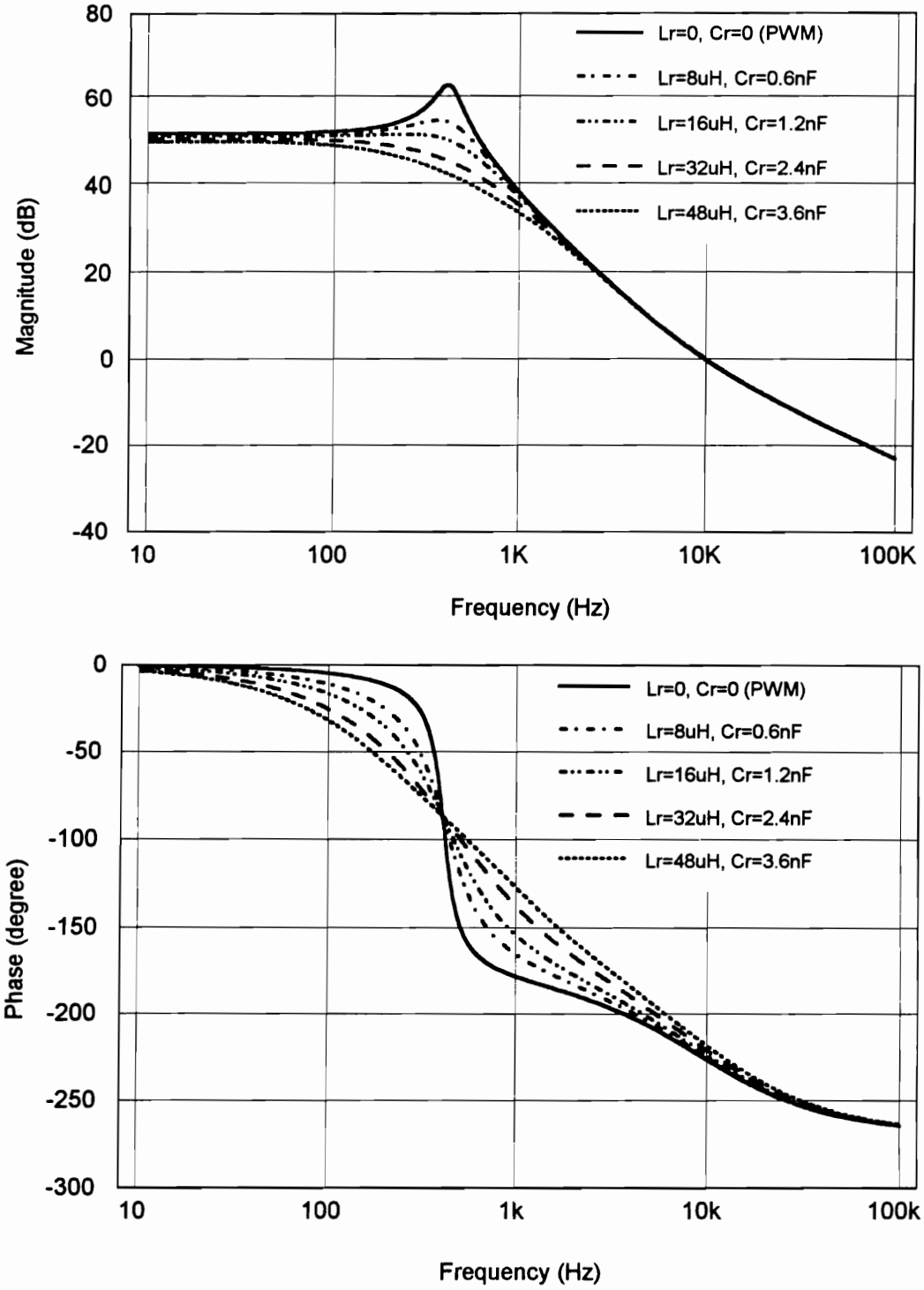


Fig. 4.18. Control-to-output transfer functions of the ZVT-PWM boost converter using different values of resonant components.

Figure 4.19 shows the output impedance of the ZVT-PWM boost converter using different values of resonant components. It can be seen that the output impedance of the ZVT-PWM boost converter becomes higher at low frequencies as T_r increases. Such behavior is expected, knowing that the effective duty cycle of the ZVT-PWM boost converter is a function of the input inductor current. Figure 4.20 compares the audio susceptibilities of the PWM and the ZVT-PWM boost converters.

4.4.4. Experimental Verification

To verify the results of the analysis, a ZVT-PWM boost converter with same component values as given in Section 4.4.3 was implemented. The measured control-to-output transfer function is shown in Fig. 4.21. Both the gain and phase characteristics agree very well with the theoretical predictions. Figure 4.22 shows the output impedance of the converter. Again, the agreement between the prediction and measurement is very good. Finally, it is observed that the model predictions and the experimental measurements show that the small-signal behavior of the ZVT-PWM converter is identical to the PWM boost converter at high frequencies (well above converter natural resonant frequency).

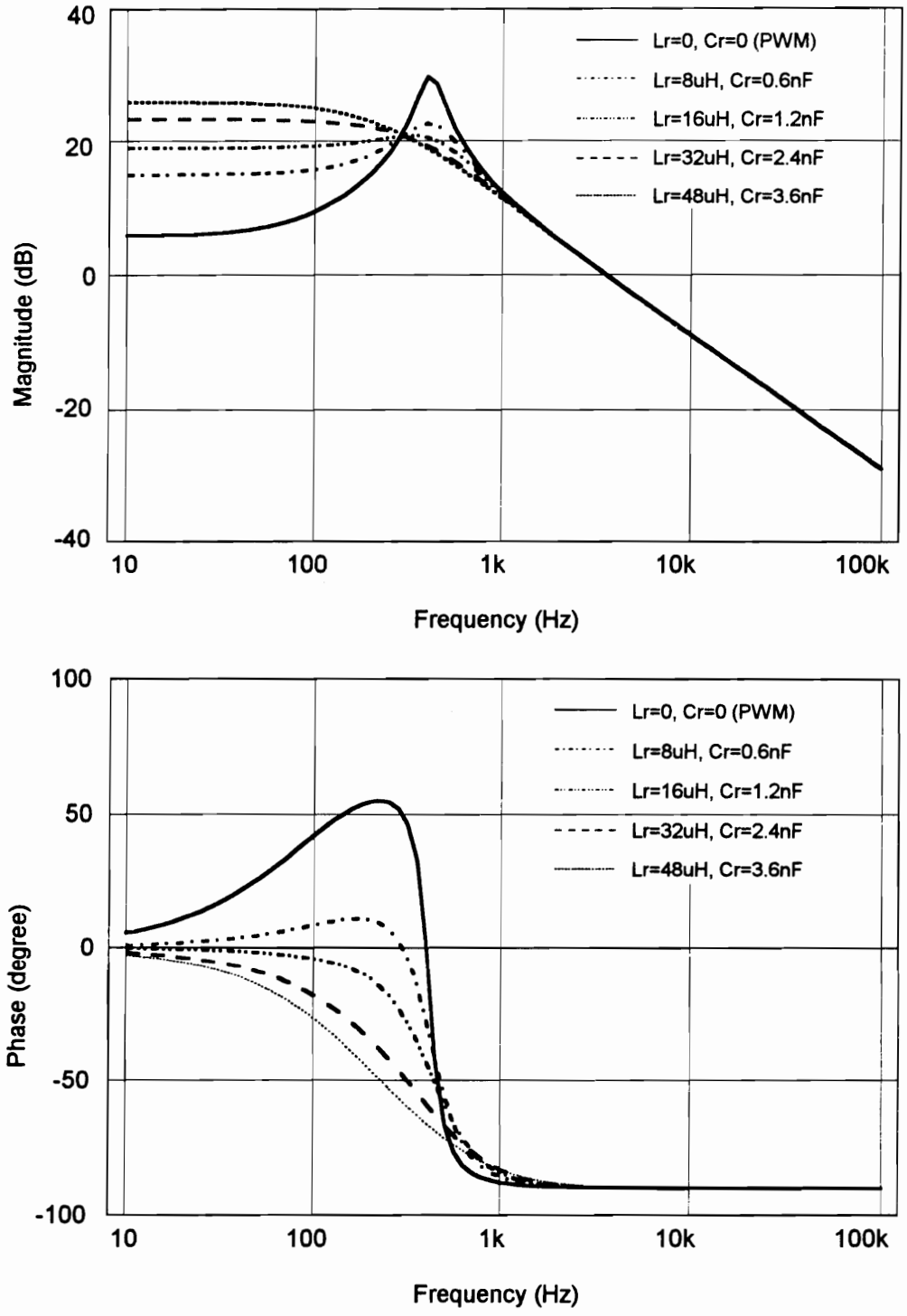


Fig. 4.19. Output impedances of the PWM converter and ZVT-PWM boost converter using different values of resonant components.

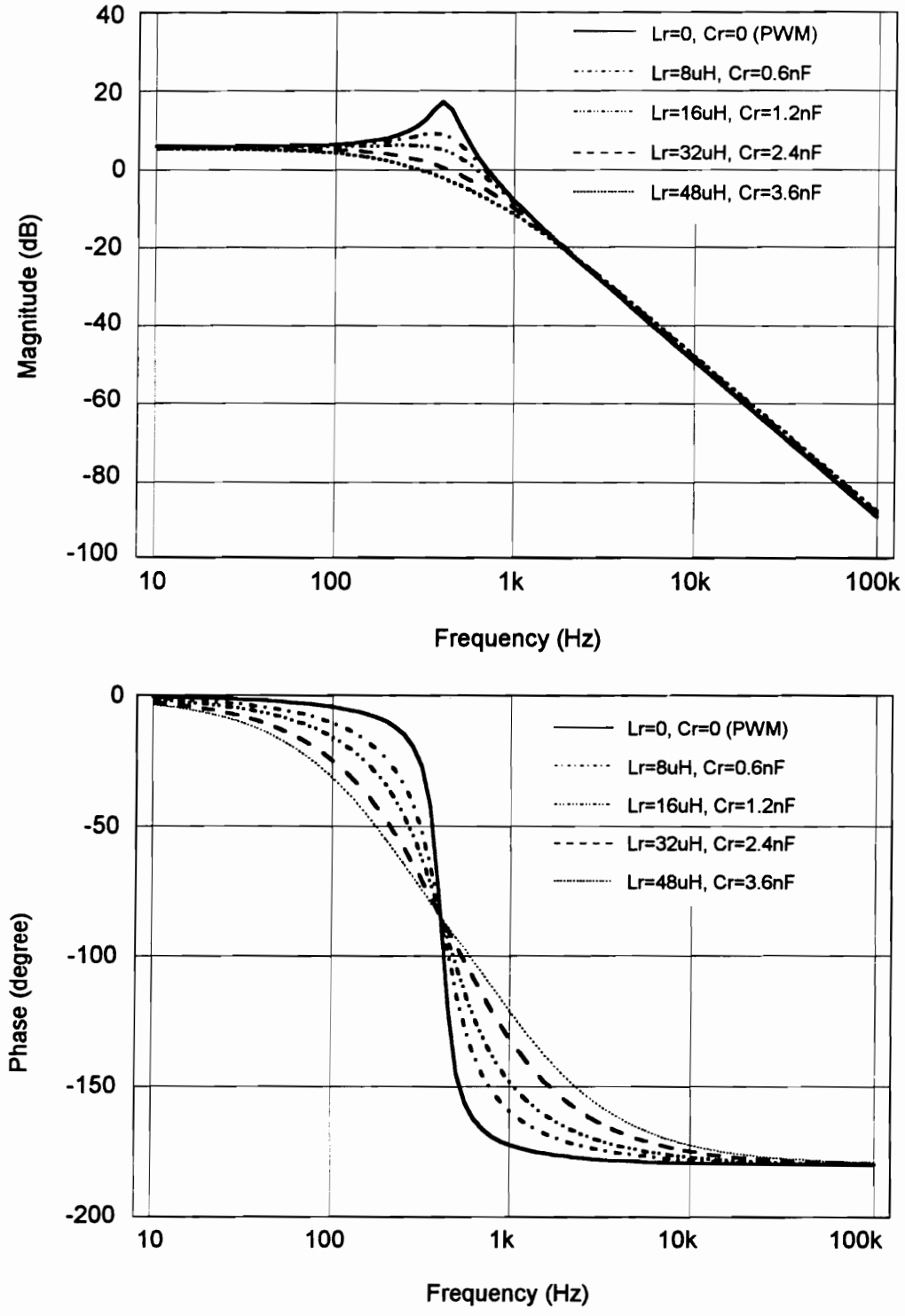


Fig. 4.20. Audio Susceptibilities of the PWM and ZVT-PWM boost converters.

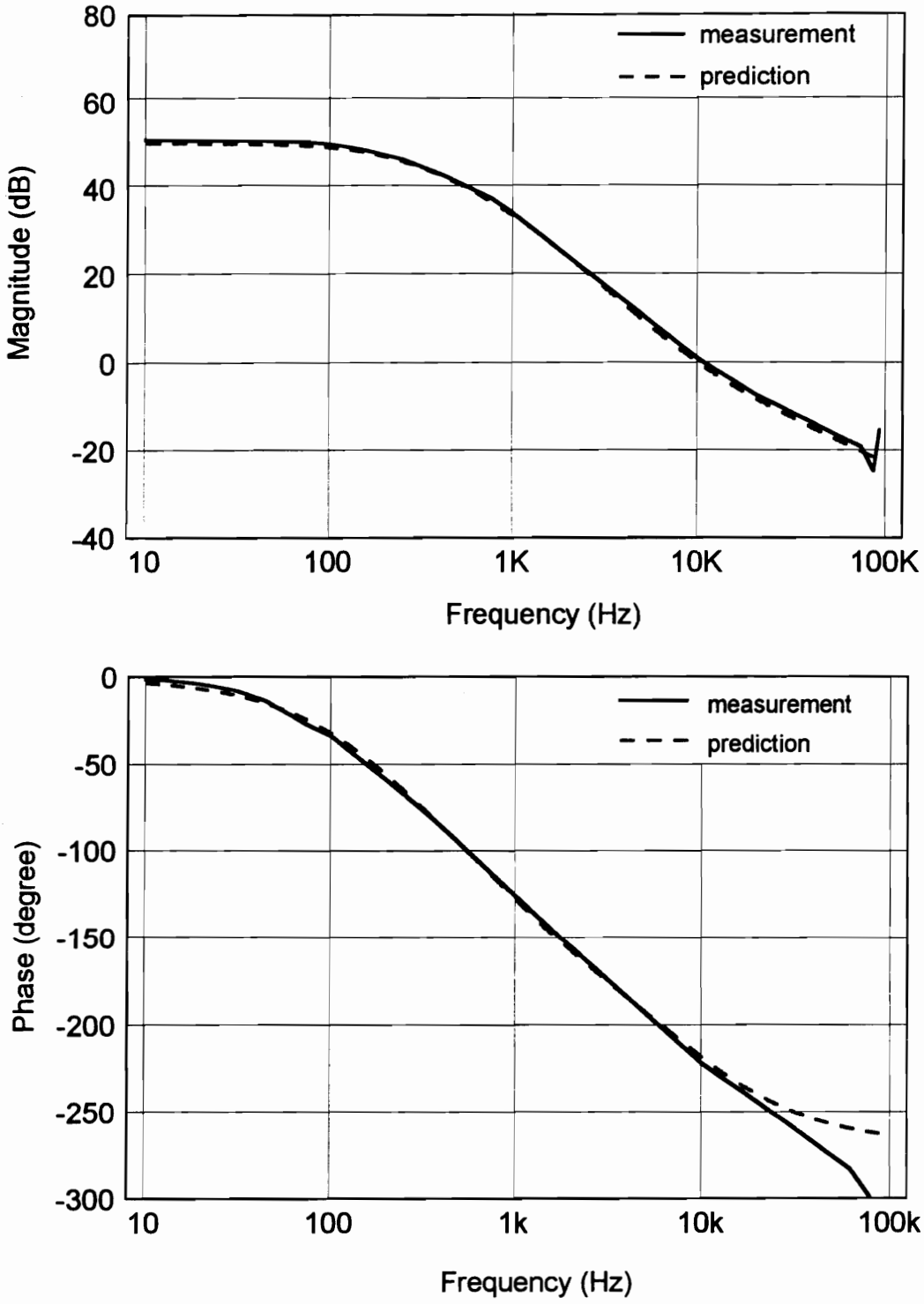


Fig. 4.21. Experimental measurement and model prediction of control-to-output transfer functions of the ZVT-PWM boost converter.

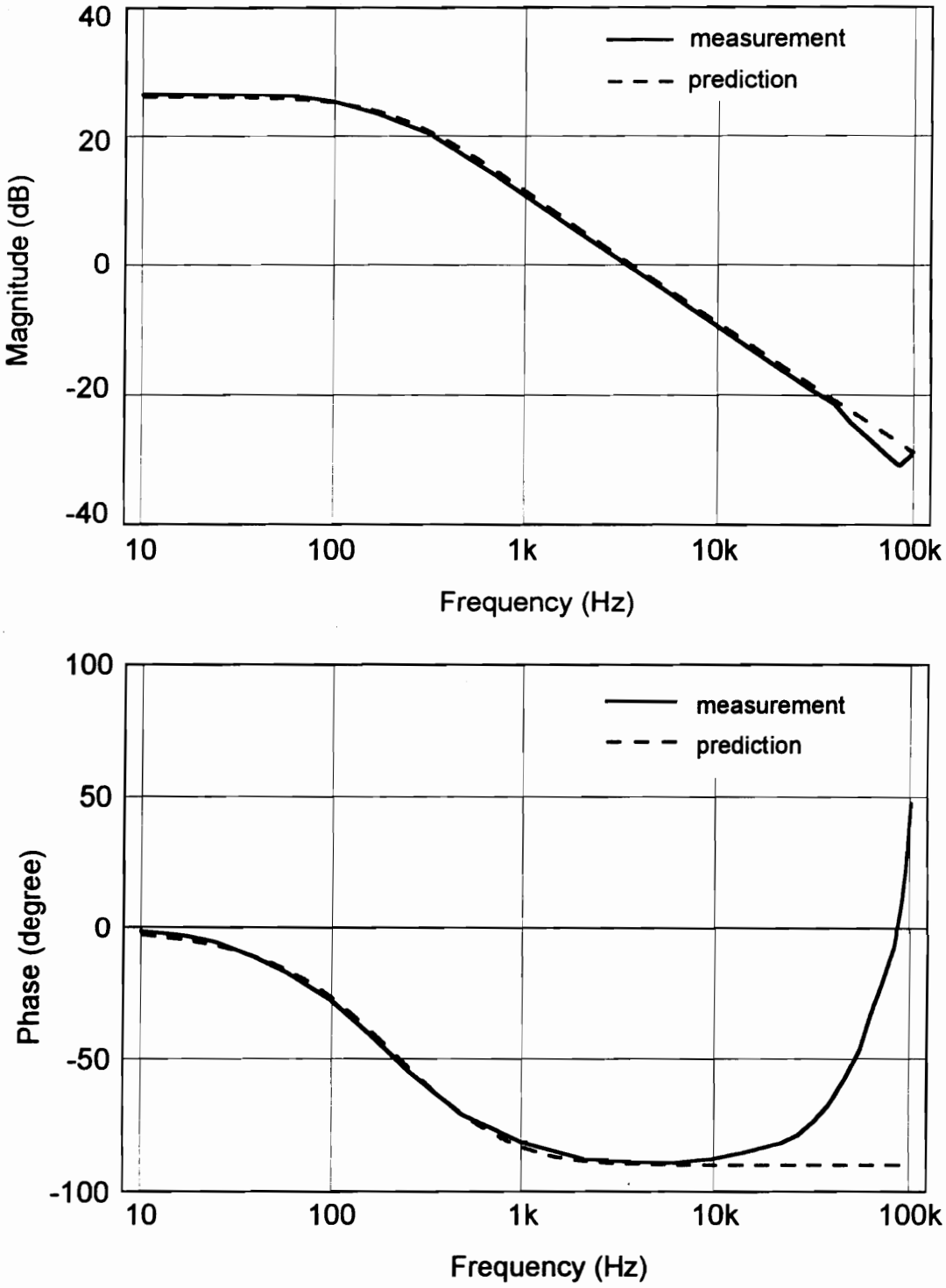


Fig. 4.22. Experimental measurement and model prediction of output impedances of the ZVT-PWM boost converter.

4.5. Summary

Up to date, soft-switching techniques applied to the PWM converters, with the exception of few isolated cases, are subjected to either high voltage stresses or high current stresses, or both. This chapter presents a novel ZVT-PWM converter technology which combines the advantages of the conventional PWM and the resonant techniques. The features of the proposed ZVT-PWM converters are summarized as follows:

- both the active and passive switches operate with ZVS;
- both switches are subjected to minimum voltage and current stresses the same as those in their PWM counterparts;
- soft-switching operation can be easily maintained for wide line range and load range; and
- the switching frequency is constant.

Compared to a conventional PWM converter, the price paid is the addition of a small auxiliary switch, a small inductor, and a small diode. Since this auxiliary resonant network only handles a small fraction (typically about 5-15%) of the total output power, all these additional components are of small-size and low-lost. Since the ZVT-PWM technique implements soft-switching for both the power switch and the rectifier diode, it is particularly suited for high-voltage

applications (such as PFC circuits) where the reverse-recovery of high-voltage p-n junction diode is of primary concern. In these applications, the benefits obtained from ZVT operation such as greater efficiency (which allows smaller and less expensive heatsinks) and lower EMI (which reduces the cost of shielding and filtering) generally far outweight the disadvantages associated with greater complexity and parts count.

The operation of the proposed converters was analyzed by using the boost ZVT-PWM converter as an example. A 300 kHz, 600 W ZVT-PWM boost dc-dc converter, and a 100 kHz, 600 W PFC circuit using the ZVT-PWM technique and IGBT device were breadboarded to show the operation of the proposed converters. It is shown that the new circuit technology significantly improves the converter performance in terms of circuit efficiency, switching stress and switching noise.

In order to characterize the typical small-signal behavior of ZVT-PWM converters, a small-signal analysis is performed on the ZVT-PWM boost converter. It is shown that small-signal characteristics of the ZVT-PWM boost converter are similar to those of the PWM boost converter using inductor current feedback control. Owing to the use of the shunt resonant network, the double-pole of the PWM converter is first damped and then split as the resonant period of the resonant components increases. The experimental results agree very well with theoretical analysis.

CHAPTER 5

ZERO-CURRENT-TRANSITION PWM CONVERTERS

5.1 Introduction

In high-power applications, minority-carrier devices such as IGBTs, BJTs, and GTOs are predominantly used. Due to poor turn-off switching characteristics, these high-power, minority devices prefer ZCS. Although the ZCS resonant and quasi-resonant techniques are capable of eliminating most of the switching losses, they impose high circulating energy which significantly increases conduction losses. Furthermore, these resonant circuits usually operate with variable frequencies, making the converter difficult to optimize.

In Chapter 3, a family of ZCS-PWM converters was presented. The ZCS-PWM technique is an extension of the ZCS-QRC technique. Using an auxiliary

switch in series with the resonant capacitor, it periodically kills the resonance between the resonant inductor and the resonant capacitor. As a result, the ZCS-PWM converters are able to achieve fixed-frequency operation and realize ZCS with much reduced circulating energy as compared to their ZCS-QRC counterparts. The ZCS-PWM technique represents a significant improvement over the ZCS-QRC technique.

The limitations of the ZCS-PWM technique are associated with the use of the resonant inductor which is in series with the power switch. One of the limitations of the ZCS-PWM technique is that the rectifier diode suffers from a high voltage stress which is twice as high as that in a PWM converter. Another limitation is the parasitic ringing that appears on the power switch owing to the iteration between the output capacitance of the switch and the resonant inductor. In practice, this parasitic ringing causes significant switching noise, switching loss, and switching stresses at high-voltage levels.

This chapter presents a new family of ZCT-PWM converters. Similarly to the ZVT-PWM technique, the ZCT-PWM technique uses a shunt resonant network to create the ZCS condition for the power switch. In this way, the ZCT-PWM converters implement ZCS turn-off for the transistors without substantially increasing voltage/current stresses of the switches. They are particularly suited for high-power/high-voltage applications, where the minority-carrier semiconductor devices (such as IGBTs, BJTs, and MCTs) are used as the power switches. As will be discussed in Section 5.3, a ZCT-PWM switching cell can be used to derived a family of ZCT-PWM converters. In the following section, the

ZCT-PWM boost converter is used as an example to illustrate the principle of operation and dc characteristics of the new converters.

5.2 ZCT-PWM Boost Converter

5.2.1. Principle of Operation

The circuit diagram and key waveforms of the ZCT-PWM boost converter are shown in Fig. 5.1. The converter differs from a conventional PWM boost converter by the introduction of a resonant branch, which consists of a resonant inductor, L_r, a resonant capacitor, C_r, an auxiliary switch, S1, and an auxiliary diode, D1. This resonant branch is active only during a short switching-transition time to create the ZCS condition for the main switch. To simplify the analysis, it is assumed that:

a) the input filter inductance is sufficiently large to be approximated by a current source with a value equal to input current, I_i.
b) the output filter capacitance is sufficiently large for the output voltage to be represented by an ideal dc voltage source, V_o.
c) all power stage components are ideal, i.e., all parasitic resistances are zero, and the semiconductor devices have zero conduction voltage drops and zero switching times.

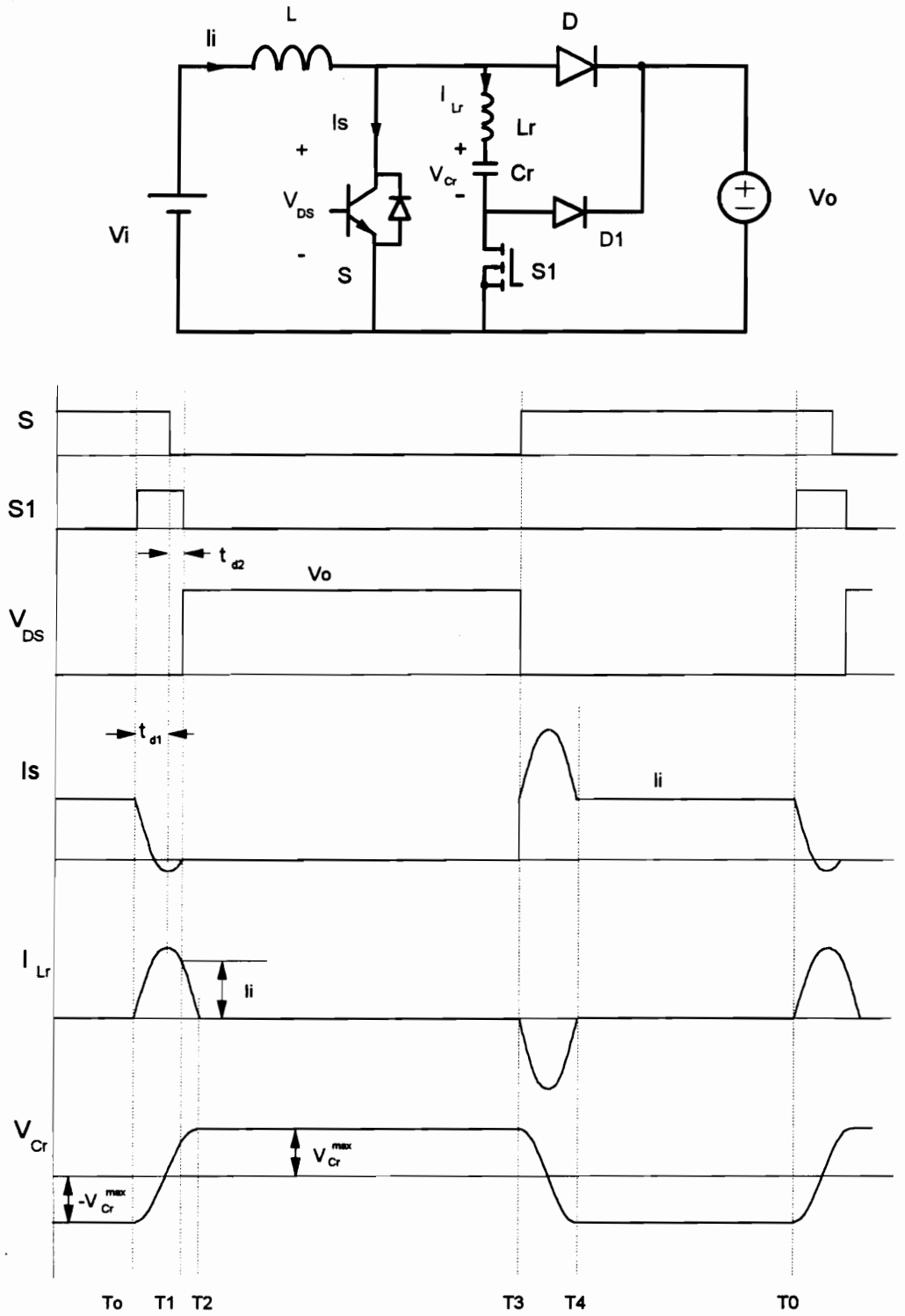


Fig. 5.1. Circuit diagram and key waveforms of the ZCT-PWM boost converter.

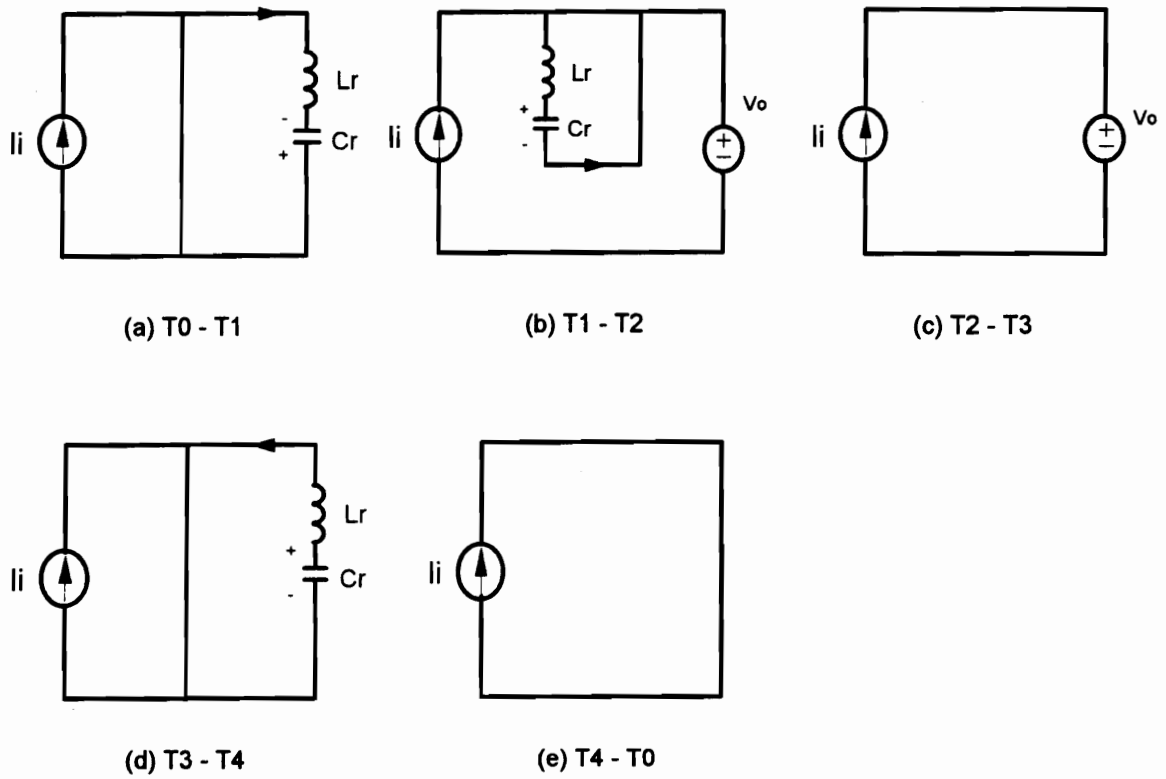


Fig. 5.2. Equivalent circuits for five topological stages.

As shown in Fig. 5.2, in steady-state, the ZCT-PWM boost converter has five operating stages:

(a) T0-T1: Prior to T0, the main switch S is conducting, and C_r is charged with certain negative voltage, $-V_{Cr}^{peak}$. At T0, the auxiliary switch S1 is turned on, starting a resonance between C_r and L_r. This resonance forces the transistor current to decrease, and the L_r current builds up in a sinusoidal fashion:

$$I_{Lr} = \frac{V_{Cr}^{\max}}{Z_n} \sin\left(\frac{1}{\sqrt{L_r C_r}} t\right), \tag{5.1}$$

where $Z_n = \sqrt{L_r / C_r}$ is the characteristic impedance of the resonant tank. After a quarter of the resonant period, T_{d1}, the C_r voltage reduces to zero, and the L_r current reaches its peak value, I_{Lr}^{peak}:

$$T_{d1} = \frac{1}{4} T_r, \tag{5.2}$$

$$I_{Lr}^{peak} = \frac{V_{Cr}^{\max}}{Z_n}, \tag{5.3}$$

where $T_r = 2\pi\sqrt{L_r C_r}$ is the resonant period of the resonant tank. It can be seen that to achieve ZCS, I_{Lr}^{peak} has to be greater than I_i. After the transistor current drops to zero and its anti-parallel diode starts to conduct, the gate-drive signal of S is disabled at $t = T_0 + T_{d1}$.

(b) T1-T2: S1 is turned off shortly after S is turned off. In steady-state operation, the resonant inductor current at T1 is always equal to I_i, as explained later. Thus the time delay between these two gate-drive turn-off signals, T_{d2}, determines the peak voltage of C_r:

$$V_{Cr}^{\max} = \frac{Z_i I_i}{\cos(2\pi T_{d2}/T_r)}, \tag{5.4}$$

if

$$V_{Cr}^{\max} \le V_{0.} \tag{5.5}$$

In steady-state operation, $V_{Cr}^{\max}$ cannot exceed V_O, since D1 would otherwise conduct during operating stage T4-T0. Defining:

$$\alpha = 2\pi \frac{T_{d2}}{T_r}, \tag{5.6}$$

Eq. (5.4) becomes:

$$V_{Cr}^{\max} = \frac{Z_n I_i}{\cos\alpha}. \tag{5.7}$$

Combining Eqs. (5.3-5.7) yields:

$$I_{Lr}^{peak} = \frac{I_i}{\cos\alpha} \ge I_i, \tag{5.8}$$

which means that as long as condition (5.5) is satisfied, the ZCS operation will be guaranteed, regardless of the input voltage and load current.

Theoretically, the converter will marginally operate with ZCS even if T_{d2} or α is zero. In a practical circuit, however, T_{d2} has to have a finite value in order to ensure the ZCS operation, as will be discussed in Section 5.2.3. When S1 is turned off at T1, both D and D1 start to conduct, and L_r and C_r continue to resonate until the I_{Lr} current decays to zero at T2.

(c) T2-T3: At T2, L_r and C_r complete the half-cycle resonance, and D1 is reverse-biased. This operating stage is identical to the transistor-off stage of the PWM boost converter.

(d) T3-T4: At T3, S is turned on, and the boost inductor is charged by the input voltage. Meanwhile, C_r and L_r form a half-cycle resonance through S and the anti-parallel diode of S1, which reverses the polarity of the C_r voltage. This time interval is a half of the resonant period:

$$\Delta T_{45} = \frac{T_r}{2}. \tag{5.9}$$

(e) T4-T0: Operation of the circuit is identical to that of the transistor-on period of the PWM boost converter. At T0, S1 is turned on again, and the switching cycle is repeated.

It is interesting to note that in steady-state operation, the energy stored in the resonant tank remains constant over the entire switching cycle. This can be seen from the circuit operation. From the equivalent circuits shown in Fig. 5.2, it can be seen that during each topological stage, either the voltage across the resonant tank (L_r plus C_r) is zero or the current through it is zero, so there is no energy transfer between the resonant tank and other parts of the circuit. Figure

5.3 shows the state-plane trajectory of the resonant tank. The energy stored in the resonant tank, which is self-adjusted in accordance with line and load conditions, is by:

$$E_{tank} = \frac{1}{2} L_r \left(\frac{I_i}{\cos\alpha} \right)^2 . \tag{5.10}$$

This circulating energy increases as input current increases (when the line voltage decreases or load current increases). In a practical circuit, since the resonant transition time is very short with respect to the switching cycle, the resonant inductance is very small compared to boost inductance. Therefore, the circulating energy of the ZCT-PWM converter is quite small compared to that of a conventional ZCS resonant converter.

It was mentioned that in the steady-state operation, the resonant inductor current at T1 is always equal to I_i, regardless of line voltage or load current variations. Assuming that for some reason I_{Lr} at T1 is larger than I_i, in this case, there will be an additional topological stage inserted between mode (b) and mode (c) in Fig. 5.2, as shown in Fig. 5.4 (a). During this operating stage, the resonant branch transports energy to the load. Therefore the energy stored in the resonant branch decreases. In contrast, if I_{Lr} at T1 is lower than I_i, there will be another topological stage inserted between mode (b) and mode (c) in Fig. 5.2, as shown in Fig. 5.4 (b). It can be seen that the boost inductor will pump some energy into the resonant branch during this operating stage. Therefore, the energy stored in the resonant branch will increase until it reaches the balance point given by Eq. (5.10).

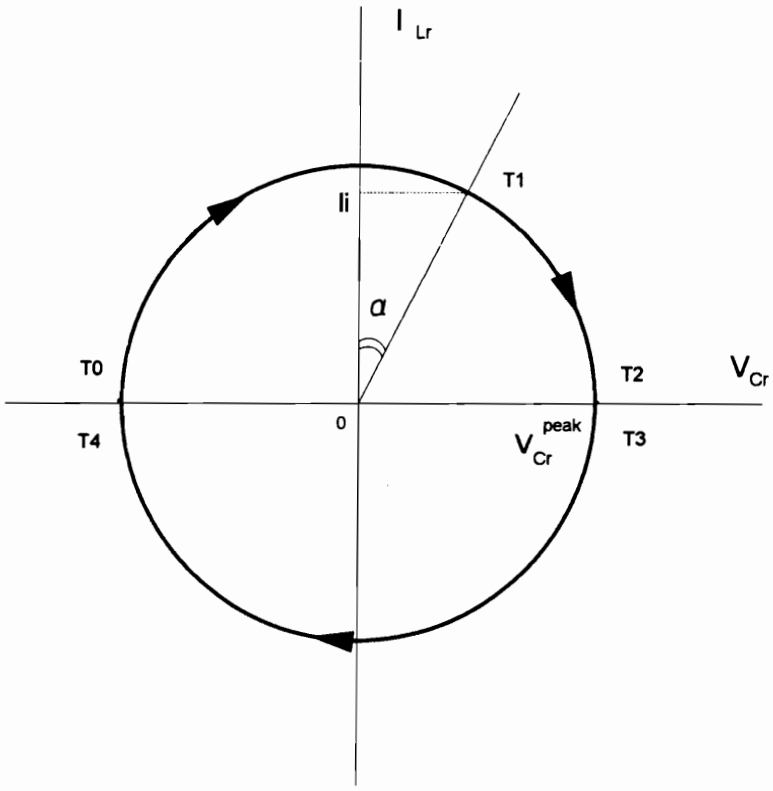
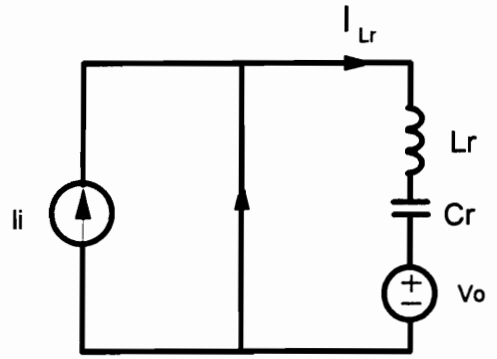
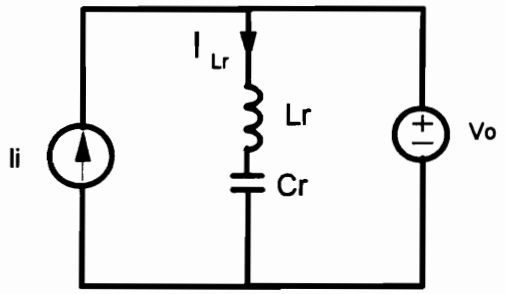


Fig. 5.3. State-plane trajectory of the resonant tank.



(a) $I_{Lr} > Ii$

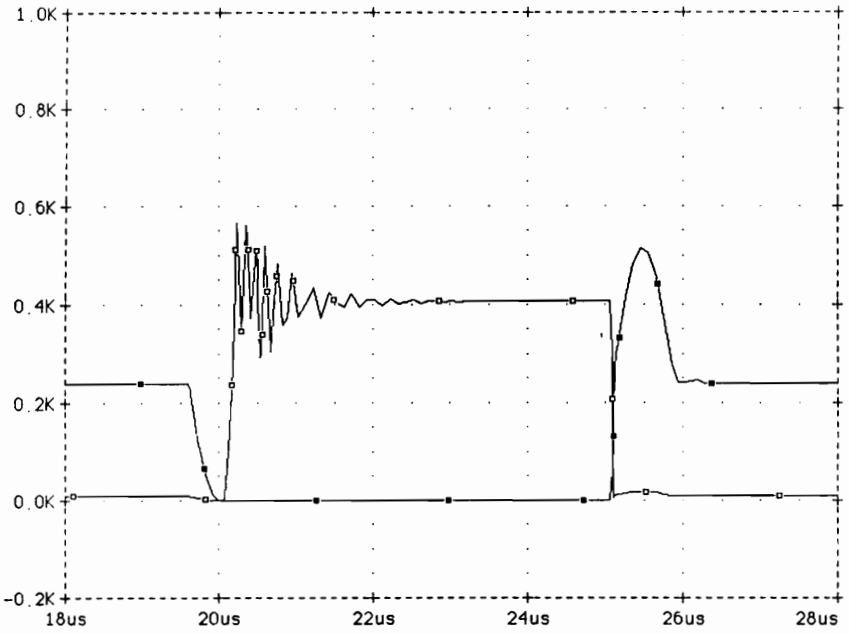


(b) $I_{Lr} < Ii$

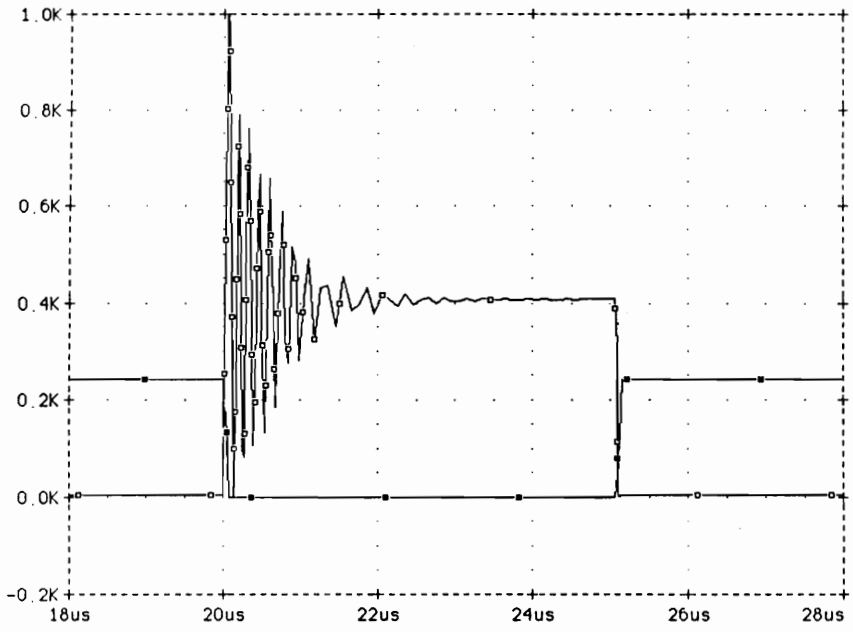
Fig. 5.4. An additional topological stage occurs when the circuit offsets the balance operating point: (a) $I_{Lr}>Ii$, and (b) $I_{Lr}<Ii$ at T1.

From the steady-state operation, it can be seen the ZCT-PWM technique implements ZCS turn-off for the power transistor without penalizing the voltage stresses of both the power transistor and the rectifier diode. Although the main switch current waveform exhibits a resonant peaking, it does not increase the conduction loss, since the average current through the power switch (IGBT) is essentially the same as compared to its PWM counterpart. Another unique advantage of the proposed technique is that it has minimum circulating energy. Equation (5.8) reveals that regardless of the line and load changes, the energy stored in the resonant tank will always be adaptively adjusted so that it is only slightly higher than what is needed for creating the ZCS condition.

For high-voltage applications (such as PFC) in which the PWM boost diode suffers from a severe reverse-recovery problem, an additional inductor (or a saturable inductor) in series with the rectifier diode or the main switch is usually used to soften the switching loss and switching noise problems associated with severe reverse-recovery of the rectifier diode. At transistor turn-off, this inductor invokes a high-voltage spike on the transistor due to high di/dt across the inductor. To suppress this voltage spike, a large dissipative snubber is frequently used. For a ZCT boost converter with the same additional inductor, however, this voltage spike is much reduced due to controlled di/dt across the inductor at transistor turn-off. As a result, a much smaller snubber can be used to absorb this ringing. Figure 5.5 shows the simulation results of typical transistor voltage waveforms in these two cases. Similarly, for isolated topologies, the ZCT technique can significantly reduce the transistor turn-off voltage spike caused by the leakage inductance of the transformer.



(a)



(b)

Fig. 5.5. Typical transistor V/I waveforms of boost converters using an additional inductor for damping reverse-recovery of the diode: (a) with the ZCT-PWM technique, and (b) with the PWM technique.

5.2.2. DC Voltage-Conversion Ratio

The voltage-conversion ratio of the ZCT-PWM boost converter can be derived based on the steady-state operation waveforms shown in Fig. 5.1. Applying volt-seconds balance on the input filter inductor yields:

$$V_i T_s = \int_0^{T_s} V_{DS} dt, \tag{5.11}$$

or

$$M = \frac{V_o}{V_i} = \frac{1}{1 - D - T_{d2}/T_s}. \tag{5.12}$$

It can be seen that the voltage-conversion ratio of the ZCT-PWM boost converter is the same as that of the PWM boost converter with an equivalent duty cycle, D_e, equal to:

$$D_e = D + \frac{T_{d2}}{T_s}. \tag{5.13}$$

Since the value of T_{d2} is usually quite small with respect to T_S, the conversion-ratio characteristics of the ZCT-PWM converter are quite close to those exhibited by the PWM boost converter.

5.2.3. Design Guidelines for ZCT-PWM Boost Converter

5.2.3.1. Design Considerations

Since the operation of the ZCT-PWM boost converter resembles that of the PWM boost converter during most portions of the switching cycle, the design of major power stage components of the ZCT-PWM boost converter is similar to that used in the PWM converter. This section discusses some design trade-offs of the auxiliary resonant network.

1. Selection of the resonant components

In principle, the resonant period (T_r) of the resonant tank in the ZCT-PWM boost converter can be as small as one wants in order for the power switch to operate with ZCS. For a minority-carrier power device such as IGBT, however, ZCS does not necessarily mean no switching loss or low switching loss. To effectively reduce the turn-off switching loss of an IGBT, the voltage across the IGBT needs to stay at zero for a certain period of delay time, T_d, after the switch current is reduced to zero. This delay time T_d allows most charge stored in the device junction to be recombined, thus eliminating the turn-off current tail of the IGBT. The value of T_d is determined by the switching characteristics of the IGBT used. Due to the above-mentioned reason, the value

of T_r in the ZCT-PWM boost converter cannot be too small. In Fig. 5.1, the power switch sees the output voltage as the switching current passes the second zero-crossing. Therefore, the following condition has to be satisfied in order for the IGBT to have a low switching loss:

$$2T_{d2} > T_{d.} \tag{5.14}$$

On the other hand, the rms current that flows through S1 is given by:

$$I_{s1}^{rms} = \sqrt{\frac{T_r}{T_s}} \frac{I_i}{2\cos\alpha}. \tag{5.15}$$

Therefore, the use of a too large T_r will lead to high circulating energy and high conduction loss in the shunt resonant network. Substituting Eq. (5.6) into (5.15) yields:

$$I_{s1}^{rms} = \sqrt{\frac{T_r}{T_s}} \frac{I_i}{2\cos\left(2\pi\frac{T_{d2}}{T_r}\right)}. \tag{5.16}$$

For a given T_{d2}, I_{s1}^{rms} can be minimized when T_r is selected at:

$$T_r = 9.6T_{d2} = 4.8T_d. \tag{5.17}$$

Under this T_r value, α is approximately 37°, and the L_r peak current and the S1 rms current are respectively given by:

$$I_{Lr}^{\max} = 1.25 I_i, \tag{5.18}$$

$$I_{s1}^{rms} = 0.62\sqrt{\frac{T_r}{T_s}} I_i = 1.37\sqrt{\frac{T_d}{T_s}} I_i. \tag{5.19}$$

2. Selection of the auxiliary switch

Although the auxiliary switch (S1) in the ZCT-PWM boost converter is turned on with ZCS, it turns off with I_i current. Therefore, S1 should be implemented by a power MOSFET. From Eq. (5.19) it can be seen that the rms current of S1 is usually quite low compared to that of the main switch. Thus S1 should be implemented by a MOSFET with a current rating that is much lower than that of the main switch. Although using a big MOSFET would help to reduce the conduction loss of the auxiliary switch, it is not desirable, since it will cause more capacitive turn-on loss.

5.2.3.2. Design Procedure for ZCT-PWM Boost Converter

Based on the trade-offs described in the previous section, the following design procedure can be established for the ZCT-PWM boost converter. This design procedure is also applicable to other ZCT-PWM topologies.

1. Design the main power stage components

The basic design of the main power stage components is similar to that of the PWM boost converter. Since the rectifier diode in the ZCT-PWM boost converter is operated with hard-switching, it should be implemented by a fast-recovery diode.

2. Select the resonant capacitance and resonant inductor

As long as the main power stage components are selected, the resonant components can be designed. Based on the power device selected, the value of T_d is determined. Usually T_d can be selected at a value that is comparable with the specified turn-off switching time of the switch used. Then the resonant period (T_r) can be calculated by using Eq. (5.17). The selection of the resonant impedance (Z_n) is quite flexible. According to Eq. (5.5), the maximum C_r voltage cannot exceed the output voltage in steady-state operation. The maximum value of V_{Cr}^{max} in Eq. (5.7), which occurs at low line and full load condition, can be selected at about one half of the output voltage. Then the value of Z_n can be calculated from Eq. (5.7). Finally, the values of L_r and C_r are given by:

$$L_r = \frac{1}{2\pi}\sqrt{Z_r T_r}, \tag{5.20}$$

$$C_r = \frac{1}{2\pi}\sqrt{T_r / Z_n}. \tag{5.21}$$

3. Select the auxiliary switch

The voltage rating of the auxiliary switch (S1) is the same as that of the power switch. The current rating of S1 can be selected based on the rms current given by Eq. (5.19). It should be noted that the anti-parallel diode of S1 needs to conduct a reverse current peaking during time interval (T3-T4) in Fig. 5.1. Thus, the implementation of S1 requires the use of a small series diode and another fast-recovery diode in addition to the MOSFET, as shown in Fig. 5.6.

5.2.3.3. Design Example of ZCT-PWM Boost Converter

To illustrate the design procedure, a ZCT-PWM boost converter with the following specifications is used:

- V_{in} = 200 - 300 V,
- V_o = 400 V,
- P_{omax} = 1 kW, and
- f_s = 100 kHz.

From the design specifications, the maximum input current at low line and full load is about 5A.

1. In this design, an IR fast-series IGBT, IRGPF40 (V_{CE}=600 V, I_C=30 A, t_r=37 nS, and T_f=420 nS) is selected as the power switch. The rectifier diode is implemented by an IR ultra-fast series diode, HEXFRED-10 (V_D=600 V, I_D=10 A, and T_{rr}=19 nS).

2. Since the turn-off switching time of the IGBT device is 420 nS, T_d is selected at 400 nS here. From Eq. (5.17), T_r=1.9 uS. Let the maximum V_{Cr}^{max}=200 V. Equation (5.7) gives Z_n=32 ohm. From Eqs. (5.20) and (5.21), L_r=9.8 uH, and C_r=9.5 nF.

3. From Eq. (5.19), the maximum rms current of S1 is $I_{s1}^{rms} = 1.37A$. The IR MOSFET, IRF830 (V_{DS}=500 V, I_D=4.5 A, R_{on}=1.5 ohm) is selected as S1.

5.2.4. Experimental Verification

Based on the design given in the previous section, a 100 kHz, 1 kW ZCT-PWM boost converter was implemented to verify the operation of the proposed converters. The circuit was regulated at 400 V output with a 200-300 V input range. The circuit diagram of the experimental converter is shown in Fig. 5.6. In the breadboarded converter, the main power switch is implemented by an IR fast-series IGBT, IRGPC40F (V_{CE}=600 V, I_C=30 A, t_r=37 nS, and T_f=420 nS, rated for up to 8 kHz switching frequency operation). Since the auxiliary switch only handles a small amount of resonant transition energy, a small MOSFET, IRF830, is employed. The small diode in series with S1 is used to block its slow body-diode from conduction. L_r and C_r are selected at 10 uH and 9.5 nF, respectively. In this design, the maximum circulating energy of the circuit, which occurs at full load and low line, is approximately 18 W, which is less than 2% of the output power.

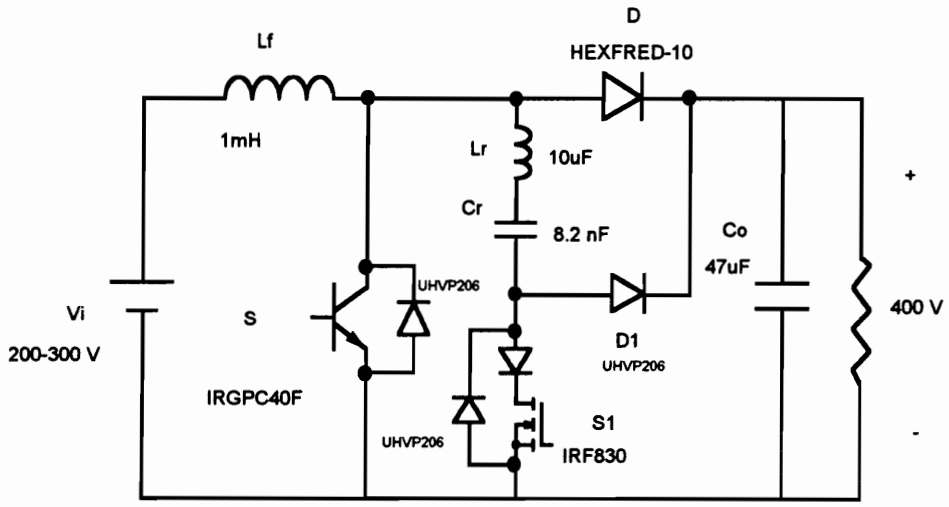
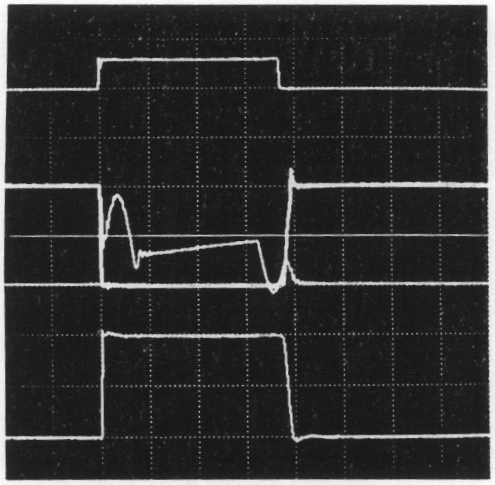


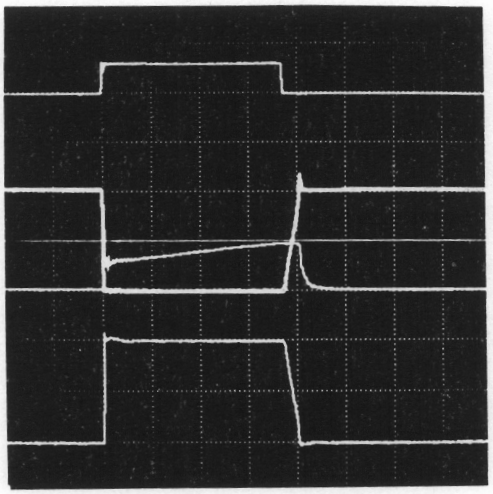
Fig. 5.6. Power stage circuit diagram of the 100 kHz, 1 kW ZCT boost converter.

It is shown that ZCS is always maintained when the line voltage or load current changes in a wide range. Figure 5.7(a) shows the oscillograms of the ZCT-PWM boost operating at 250 V input and 700 W output. Compared with the waveforms of the PWM circuit operating under the same conditions, it can be seen that the IGBT turn-off current tail is essentially alleviated. Figure 5.8 shows the efficiency measurements of ZCT and PWM boost converters. It can be seen that the ZCT technique significantly improves the efficiency. Due to the high turn-off switching loss of the IGBT device, the hard-switched PWM circuit is not able to operate at above 800 W output power. Table I shows the loss breakdown estimation for two boost converters operating at 250 V input and 700 W output. For the PWM converter, it can be seen that the major power dissipation comes from the turn-off switching loss of the IGBT, which is about 37 W. The estimation of IGBT switching losses is based on the actual switch voltage/current waveforms, roughly in agreement with the data given in the IGBT designer's manual [F34]. For the ZCT circuit, when the converter is operated at 250 V input and 700 W output, the conduction loss of the auxiliary switch is about 0.8 W, and the total power losses involved in the operation of the auxiliary resonant shunt are only about 2.1 W, which is about 0.3% of the output power.

To compare the switching losses of IGBTs under hard-switching, ZVT, and ZCT conditions, another 50 kHz, 2 kW boost converter was built and tested. The converter is regulated at 400 V output with an 200 V input voltage. An IR fast-series IGBT, IRGPC50F, and an IR ultra-fast diode, HEXFRED-10, are used as the main power switch and the main diode, respectively For the ZVT-PWM converter, the resonant inductance and resonant capacitance are selected at 24



(a) Using ZCT-PWM technique



(b) Using PWM technique

Fig. 5.7. Oscillograms of two IGBT boost converters operating at Vi=250 V, Po=700 W, and fs=100 kHz.

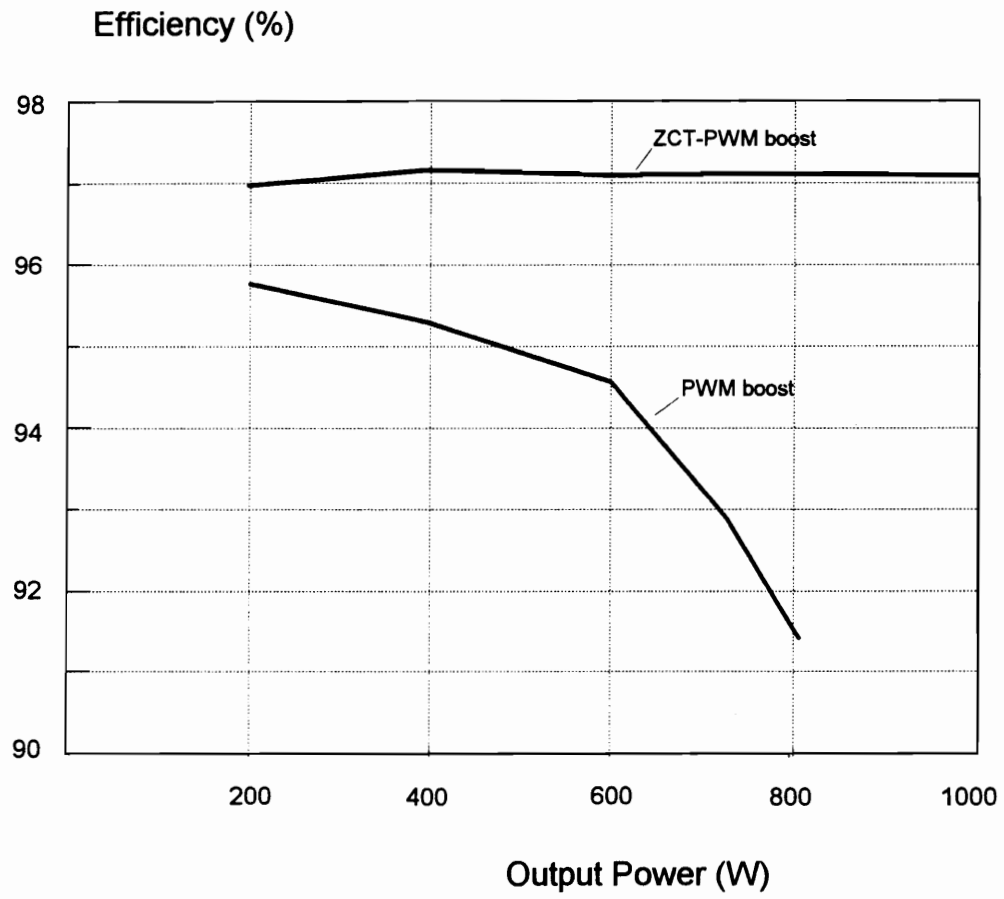


Fig. 5.8. Efficiency comparison of ZCT-PWM and PWM boost converters using IGBT.

Table I. Loss breakdown of PWM and ZCT-PWM boost converters at P_O=700 W and V_i=250 V.

Component losses	PWM boost	ZCT-PWM boost
IGBT conduction	3.3 W	3.0 W
IGBT turn-on switching	3.0 W	3.0 W
IGBT turn-off switching	37.0 W	5.1 W
auxiliary switch	N/A	1.1 W
auxiliary diodes	N/A	0.7 W
resonant tank (L_r and C_r)	N/A	0.3 W
diode conduction	1.7 W	1.6 W
diode switching	2.9 W	2.9 W
boost inductor	2.0 W	1.9 W
others	1.5 W	1.5 W
total	51.4 W	21 w
efficiency	93.1%	97.1%

uF and 4.4 nF respectively. The 4 nF external capacitance is used to reduce the IGBT turn-off loss. For the ZCT-PWM converter, L_r and C_r are selected at 16nF and 24 uF, respectively. Figure 5.9 shows the efficiency measurements of three boost converters. It can be seen that the ZCT-PWM boost converter gives the best efficiency at heavy load. Shown in Fig. 5.10 is the IGBT turn-off voltage and current waveforms of the converter at 1200 W output. It can be seen that the IGBT under ZCS has the minimum turn-off loss. At 1200 W output, the IGBT turn-off switching loss is estimated at 42 W, 10 W, and 2 W for the PWM, ZVT-PWM, and ZCT-PWM converters, respectively.

Finally, it should be mentioned that the rectifying diodes in the ZCT-PWM converters still operate with hard-switching. This is the major limitation of the ZCT-PWM technique presented here. For this reason, although the ZCT-PWM technique is deemed more effective in reducing IGBT turn-off loss, the ZVT-PWM technique can be more desirable for reducing the overall switching losses of the converter, especially for the applications where the reverse-recovery problem of the rectifying diode is significant [F21].

5.3 A Family of ZCT-PWM Converters

The ZCT-PWM switching cell shown in Fig. 5.11 can be used to generalize the ZCT concept described above. Based on the PWM switching cell shown in Fig. 4.10(a), the ZCT-PWM switching cell is derived by adding a shunt

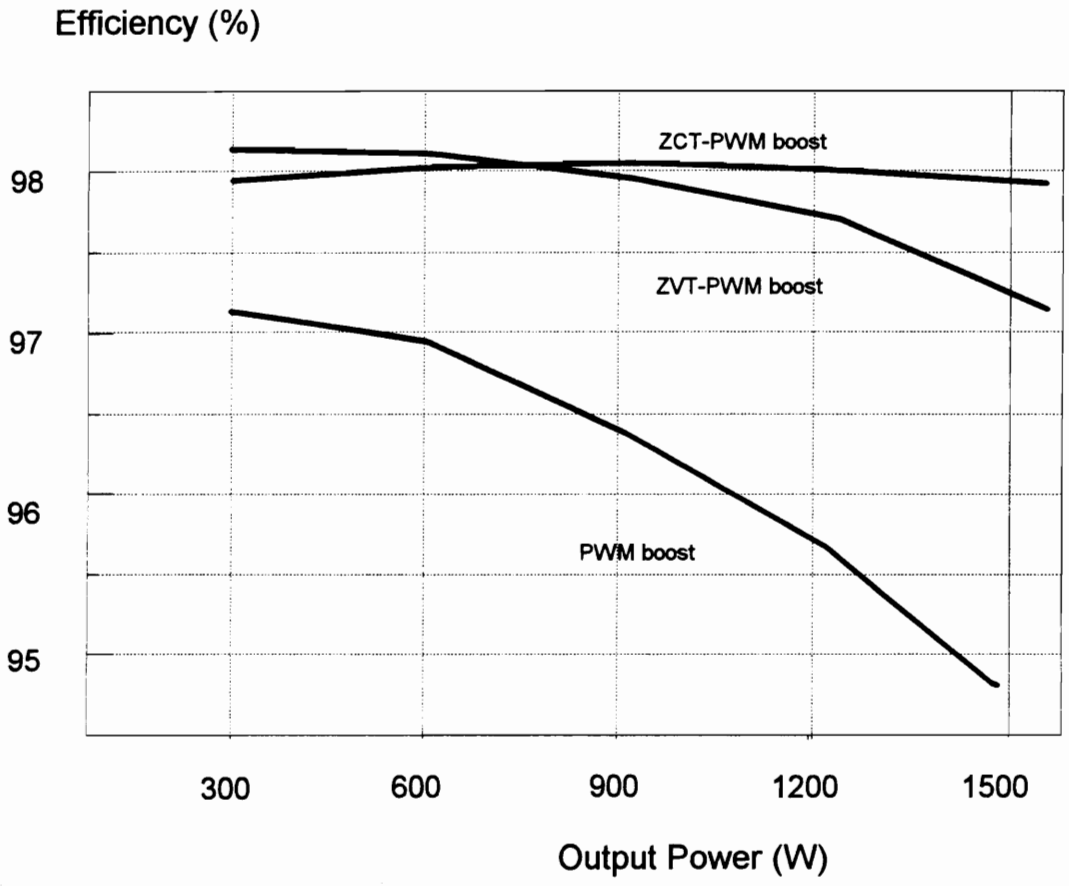
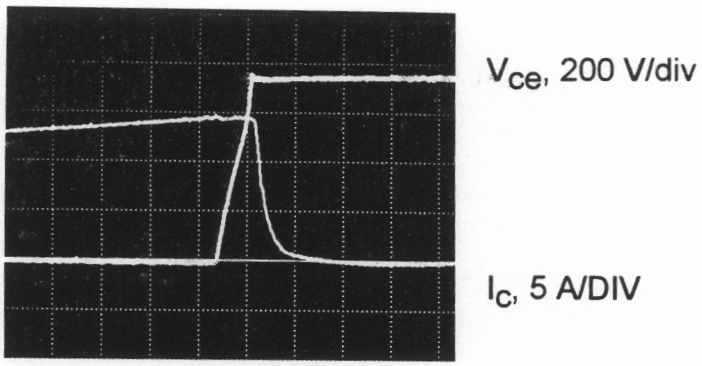
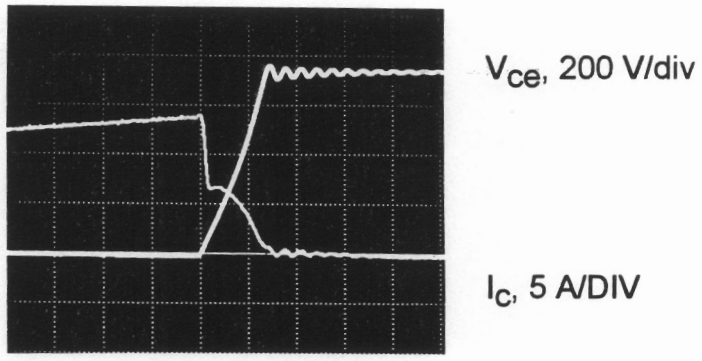


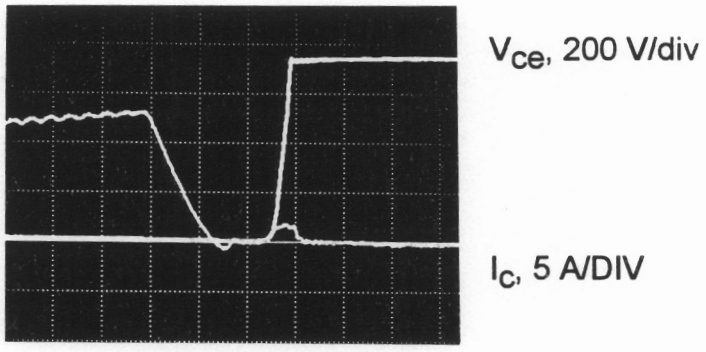
Fig. 5.9. Efficiency measurements of three boost converters using IGBT.



(a) Using PWM technique



(b) Using ZVT-PWM technique



(C) Using ZCT-PWM technique

Fig. 5.10. IGBT turn-off V/I wavefoms of the 50 kHz, 1200 W boost converter under different switching conditions: (a) hard-switching, (b) ZVT, and (c) ZCT.

branch, which consists of an auxiliary switch S1, an auxiliary diode D1, a resonant capacitor C_r, and a resonant inductor L_r. The function of this shunt branch is to create a partial resonance during short switching transition time to achieve ZCS. The principle of operation of the ZCT-PWM switching cell has been illustrated in the previous section by using the boost topology as an example.

By replacing the PWM switching cell in a PWM converter with the ZCT-PWM switching cell shown in Fig. 5.11, a family of ZCT-PWM converters is derived. Figure 5.12 shows six basic ZCT-PWM topologies. Figure 5.13 shows a single-switch three-phase ZCT-PWM boost rectifier converter. By running this circuit in the discontinuous conduction mode, it can provide a fairly good power factor with simple fixed-frequency and fixed-duty-cycle control. The use of the shunt resonant network enables the circuit to operate at much higher switching frequencies. The operation of this converter is quite similar to that of the ZCT-PWM boost converter [F36].

Due to the fact that the power switch and rectifier diode do not share a common ground in isolated converters, the ZCT-PWM switching cell shown in Fig. 5.11 is not directly applicable to isolated topologies. The implementation of the ZCT concept in an isolated converter would require the use of an additional voltage source. As an example, Fig. 5.14 shows a full-bridge ZCT-PWM boost converter. In Fig. 5.14, V_C is an auxiliary voltage source with a amplitude equal to the reflected output voltage, NV_O. The operation and circuit waveforms of this converter are the same as those of the ZCT-PWM boost converter shown in Fig. 5.1. However, since this converter requires the use of the auxiliary voltage source V_C, it does not seem to be attractive for practical applications.

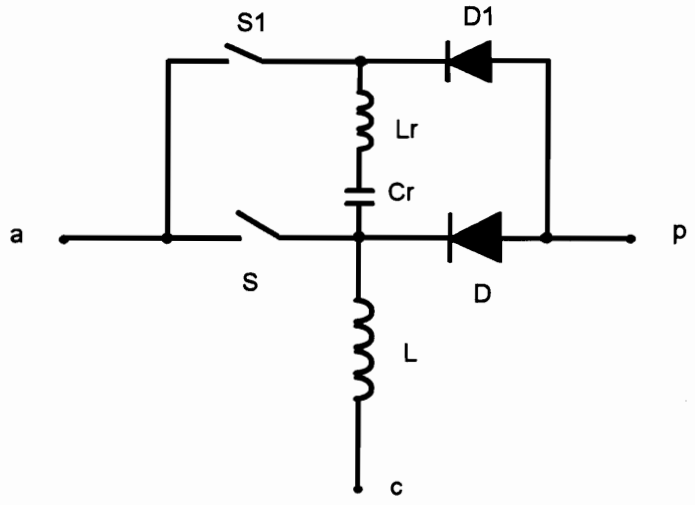


Fig. 5. 11. The ZCT-PWM switching cell.

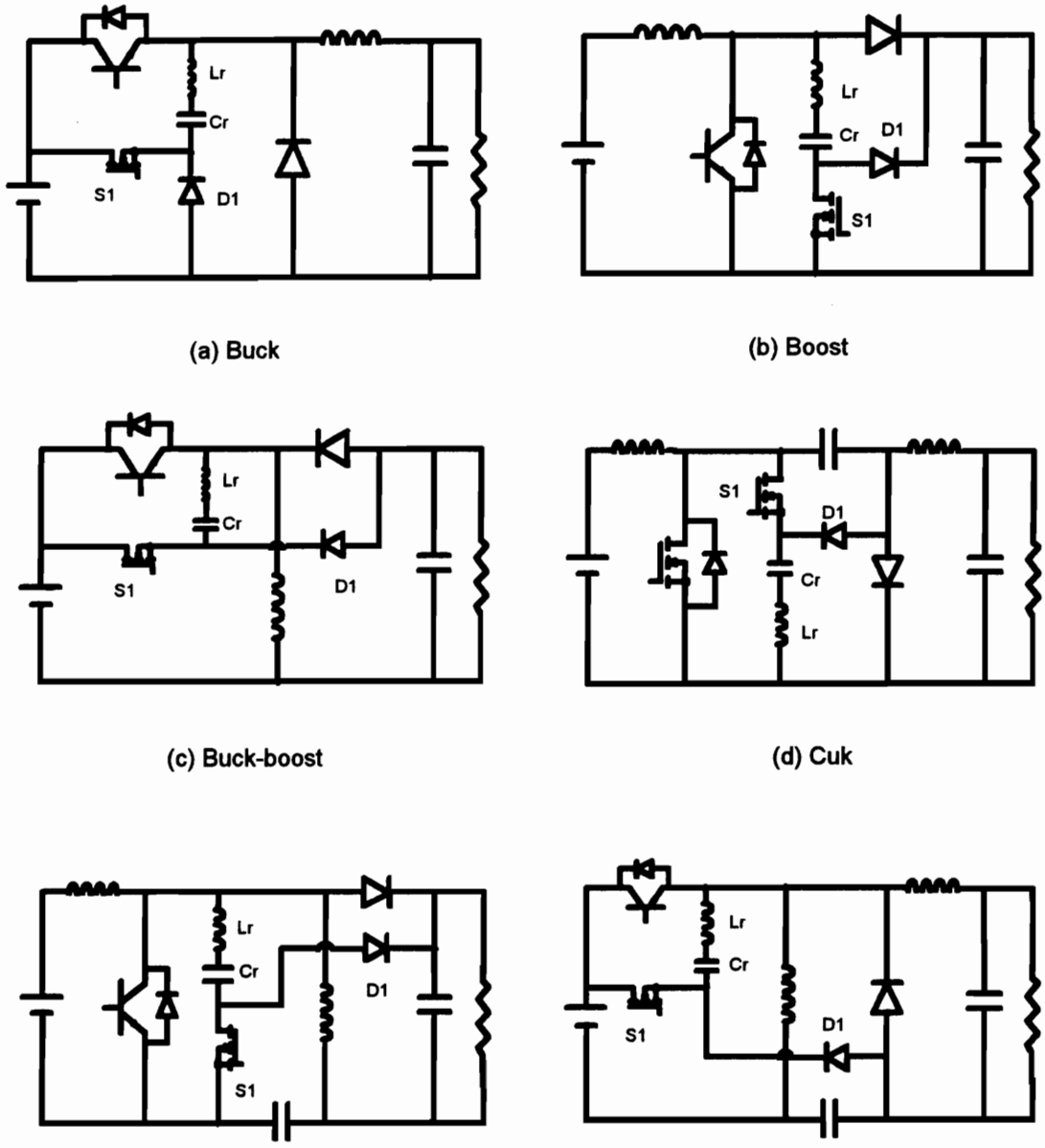


Fig. 5.12. Six basic ZCT-PWM topologies.

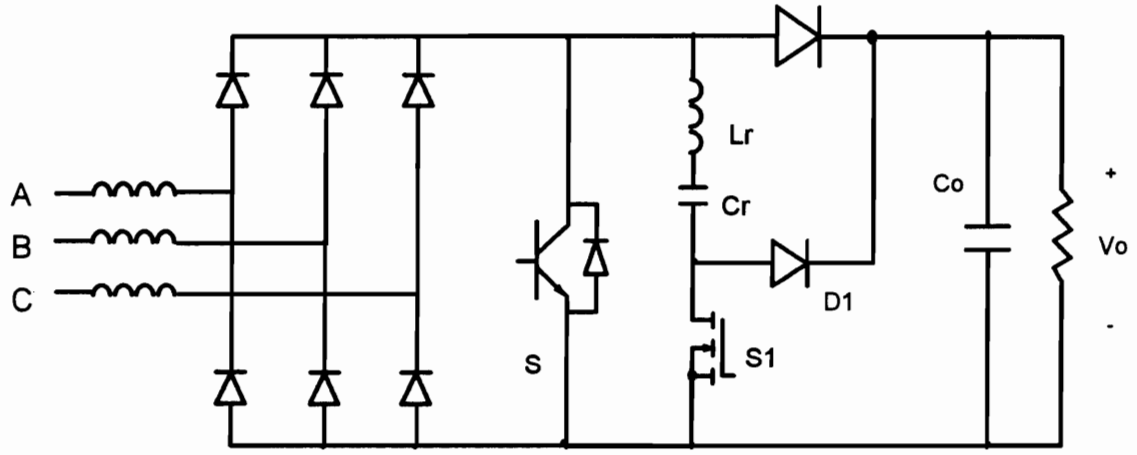


Fig. 5.13. A simple three-phase ZCT-PWM boost converter.

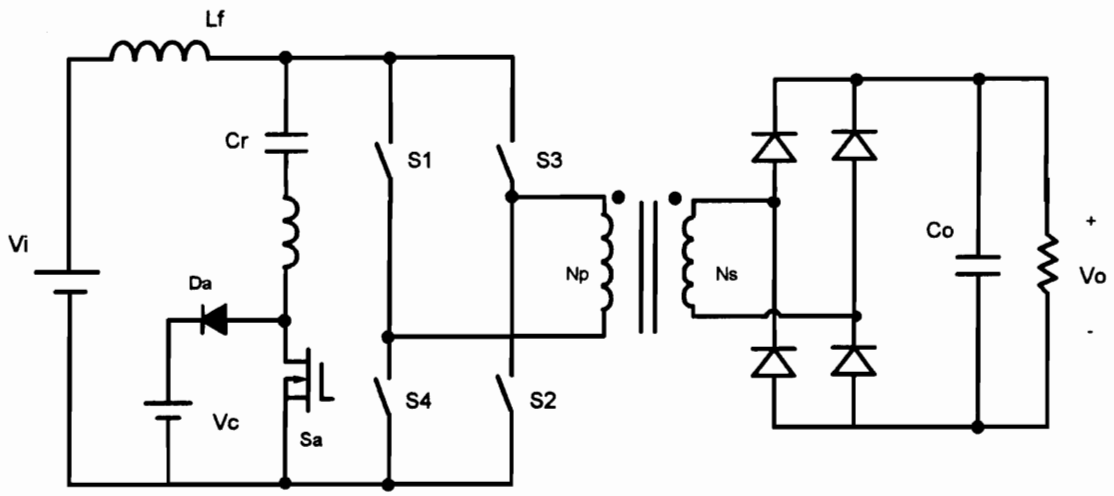


Fig. 14. FB-ZCT-PWM boost converter.

The features of the ZCT-PWM converters are summarized as follows:

- ZCS for the power switch,
- low voltage/current stresses of the power switch and rectifier diode,
- minimal circulating energy,
- wide line and load ranges for ZCS,
- constant-frequency operation.

5.4. Summary

Because of continuous improvement of switching characteristics, lower conduction losses, and lower costs, IGBTs are gaining wide acceptance in today's power processing circuits, particularly in high-power applications. In practice, due to high switching losses (mainly turn-off current tail), the switching frequency of the hard-switched IGBT circuits has been limited to low tens of kHz range. Performance (efficiency, size, weight, and EMI noise, etc.) of these converters can be significantly improved by implementing ZCS and thereby boosting the operating frequency. Although a number of ZCS resonant techniques have been presented to date, they all have severe limitations, such as high circulating energy, limited load range, variable frequency control, and complicated design.

Based on the concept of shunt resonant network, this chapter presents a novel ZCT technique and a new family of ZCT-PWM converters. The proposed

converters feature ZCS turn-off for the power transistor, while retaining the advantages of conventional PWM converters, such as low voltage/current stresses of the semiconductor devices and constant-frequency operation. The shunt resonant network operates only during switching-transition, thus during most portions of the switching cycle, the converter operates like a PWM circuit. Consequently, the design of the power stage components and control is similar to that of the conventional PWM converters. Furthermore, ZCT operation is independent of line and load conditions, and the circulating energy of the converter is always maintained at minimum. These features make the ZCT-PWM technique attractive for many applications where the minority-carrier devices such as IGBTs, BJTs, and MCTs are employed.

The principle of operation and dc characteristics of the ZCT-PWM converters are illustrated by using the boost topology as an example. In addition, a design procedure is established for the proposed converters. The theoretical analysis is verified on a 100 kHz, 1kW ZCT-PWM boost converter using an IGBT.

CHAPTER 6

CONCLUSIONS

Switching losses, stresses, and noise due to circuit parasitics are inherent in the PWM technique, and these limitations have restricted the PWM converters from operating at higher frequencies for size/weight reduction and for performance improvement. To alleviate these problems, many resonant techniques were developed. Typically, a resonant converter incorporates a certain type of resonant network into a PWM topology to shape the switch voltage/current waveforms so that the power switches are commutated with either ZVS or ZCS. The improved switching conditions enable the resonant converters to operate at much higher frequencies with significantly reduced switching losses, stresses, and noise. Unfortunately, due to resonant nature and high circulating energy, the V/I ratings of the power switches and reactive components are significantly increased when compared to their PWM counterparts. This results in a significantly increase in conduction losses.

To facilitate soft-switching operation while preserving the merits of the PWM technique, a number of soft-switching PWM techniques were proposed. As hybrid circuits between the PWM and resonant converters, these soft-switching PWM converters utilize some form of partial resonance to soften the switching process. When switching transition is completed, the converter reverts back to the familiar PWM mode of operation so that the circulatory energy can be minimized compared to resonant converters. Thus, switching losses are reduced at the cost of a minimal increase in conduction losses.

This work presented four families of soft-switching PWM converters: the ZVS-PWM converters, the ZCS-PWM converters, the ZVT-PWM converters and the ZCT-PWM converters.

The ZVS-PWM technique is an extension of the ZVS-QRC technique. It uses an auxiliary switch across the resonant inductor to create a freewheeling stage within the quasi-resonant operation, enabling the converter to operate with a constant frequency and much reduced circulating energy. The problems of the ZVS-PWM technique are associated with the use of the resonant inductor that is in the main power path. First, for single-ended topologies, this resonant inductor induces a high voltage spike on the power switch that is proportional to the load current. Second, the rectifier diode suffers from severe parasitic ringing due to the resonance between the diode junction capacitance and the resonant inductor. In addition, the ZVS condition of the converter is sensitive to line voltage or load variations. To enhance the circuit capability of handling a wide load range without further increasing the circulating energy, a saturable inductor can be used to replace the linear resonant inductor. A particular

topology in this family, the bridge-type ZVS-PWM topology, is deemed most desirable, since their switches are subjected to minimum voltage stresses.

For high-power applications where minority-carrier devices such as BJTs, IGBTs, and GTOs are used as the power switches, the ZCS technique is deemed more desirable than ZVS in reducing the switching losses. As an extension of the ZCS-QRC technique, the ZCS-PWM technique uses an auxiliary switch in series with the resonant capacitor of a ZCS-QRC to periodically kill the circuit resonance. In this way, the ZCS-PWM converters implement ZCS for the power switch(es) and ZVS for the rectifier diode(es) with much reduced circulating energy. The limitations of the ZCS-PWM technique, which include severe parasitic ringing on power switch, high voltage stress of the rectifier diode, and line and load dependence of the ZCS condition, are associated with the use of the resonant inductor that is in series with the power switch.

Recognizing that the major limitations of the most soft-switching converters are related to the use of certain resonant elements in the main power path, a concept of using a shunt resonant network to implement soft-switching was proposed. On the basis of the shunt resonant network concept, two families of soft-switching PWM converters were derived: the ZVT-PWM converters, and the ZCT-PWM converters. During switching transition, the shunt resonant network is activated to create a partial resonance to achieve ZVS or ZCS. When switching transition is over, the shunt resonant network is disabled so that the operation of the converter resembles that of the PWM converters during most portions of the switching cycle. In this way, the new converters can achieve soft-

switching without increasing the voltage and current stresses of the switches. In addition, since the shunt resonant network only handles little switching transition energy, the V/I ratings and sizes of the auxiliary components are quite small compared to the main power stage components.

The steady-state operation and dc characteristics of the ZVT- and ZCT-PWM converters are analyzed by using the boost topology as an example. Design trade-offs are analyzed and design guidelines are defined for both the ZVT- and ZCT-PWM converters. In addition, a small-signal analysis of the ZVT-PWM boost converter was performed to see the small-signal behavior of the ZVT-PWM converters.

Since the ZVT-PWM technique implements ZVS for both the power switch and the rectifier diode, it is particularly deemed attractive for high voltage applications (such as power factor correction circuits) where the reverse-recovery problem of the high-voltage diode is of primary concern. The ZCT-PWM converters, however, are deemed desirable for high-power applications where minority-carrier devices such as BJTs, IGBTs, GTOs, and MCTs are used as the power switches. The ZVT- and ZCT-PWM techniques have been extended to many dc-dc, dc-ac, and ac-dc power conversion applications.

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