CHAPTER 2

CONCEPT OF QUASI-SINGLE-STAGE (QSS) POWER CONVERSION

2.1 Introduction

The preliminaries and soft-switching issues of the three-phase buck rectifier are discussed in this chapter to facilitate the discussions on the isolated buck rectifier and the charge control issue in the later chapters. The general concept of quasi-single-stage (QSS) power conversion topology is also introduced and defined following an illustrative example of a cascaded buck rectifier. The family of QSS power converters feature single-stage power processing without a dc-link low-pass filter (LPF), a unidirectional pulsating dc-link voltage, soft-switching capability with minimal extra commutation circuitry, simple PWM control, and high efficiency and reliability. Some other non-isolated QSS power conversion examples including the cascaded VSI/CSR, and QSS ac-ac converter are also given.

Throughout this dissertation, if a three-phase ac source is involved, it is assumed to be balanced and sinusoidal to facilitate discussions. If the source is distorted or unbalanced, usually corrective measures, such as those reviewed in Chapter 1 for buck rectifiers, need to be included in the modulation scheme to prevent performance deterioration of the rectifier

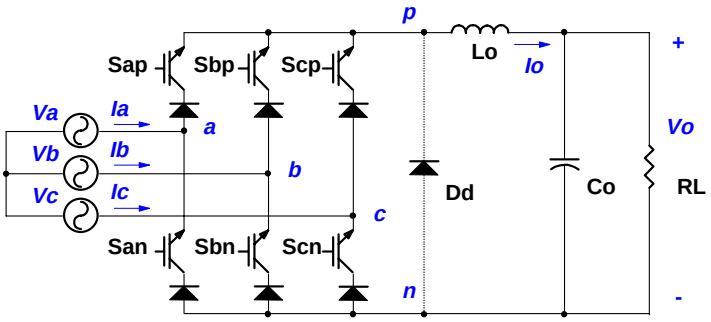
system. Also, the input or output filter will not be considered for simplicity of the discussion.

2.2 Illustrative Example: Cascaded Three-Phase Buck Rectifier

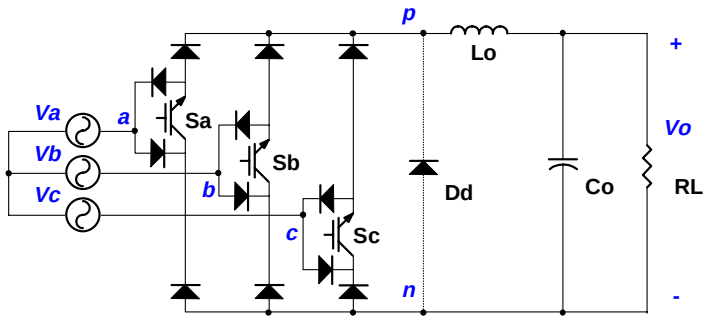
2.2.1 Three-Phase Buck PWM Rectifier

The requirements of rigid harmonic standards rule out the use of simple diode rectifiers as the front-end converter for high-power ac-dc applications, e.g. beyond 10 kW. Both the six-switch boost (current-fed) and buck (voltage-fed) three-phase PWM rectifiers provide solutions to the problem [H3]. With them, low total harmonic distortion (THD), power factor correction (PFC), constant power flow, and so minimal filtering component size and cost can be easily achieved. Buck or buck-derived topologies [A1]-[A8] [H3] can be of choice, especially when the input line voltage is high so that the boost topology suffers from high device voltage ratings, or when a variable output dc voltage is a must. Also, better dynamic response, as akin to buck dc-dc converters, and no starting and shoot-through problems are among the other advantages of the buck-type topology.

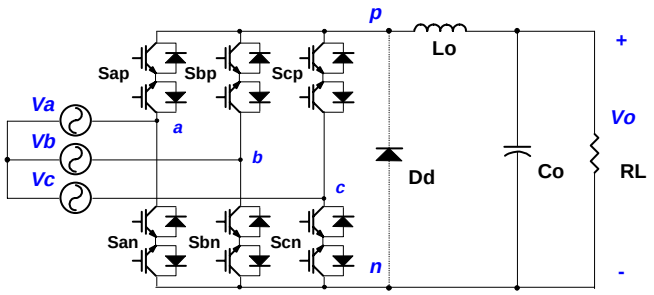
The basic six-switch buck rectifier shown in Fig. 2.1(a) is composed of a six-switch three-phase bridge, an output LPF consisting of L_o and C_o, and a capacitive input LPF which is not shown [A1]-[A4]. An extra freewheeling diode D_d across the dc-side of the bridge can be used to effectively reduce the conduction loss. Because most of the modern turn-off switches have no reverse voltage blocking capability, a block diode needs to be in series with each active switch. Without the freewheeling diode, the bridge switches have to be controlled as normal-on switches; while with it, they can be controlled as either normal-on or normal-off switches.



(a) Buck rectifier.



(b) Three-switch buck rectifier.



(c) Current bi-directional buck rectifier.

Fig. 2.1. Three-phase buck rectifier topologies.

It can be seen that for rectifier operation, the upper and lower switches of the same phase leg can be gated on and off at the same time with no influence to the circuit operation. Doing this usually simply increases the loading to the gate drivers. However, because of this feature, the two switches in the same phase leg can be combined into one. The resulting

three-switch buck rectifier is shown in Fig. 2.1(b) [A6]. Compared with the six-switch version, it incurs on-drop voltage of two more diodes in the current path.

Although the buck rectifier does have the energy regeneration capability through reversing the bridge output voltage if the freewheeling diode is not present, the output current of the rectifier bridge is unidirectional. To achieve bi-directional current flow capability, an extra anti-parallel buck rectifier bridge needs to be added. Combining the two bridge leads to the current bi-directional buck rectifier as shown in Fig. 2.1(c) [A5]. The topology is of matrix-type in nature. Certainly, there are different ways to implement these four-quadrant switches.

2.2.2 PWM Schemes

The basic task for the modulation of the buck rectifier is to regulate the output voltage V_o and shape the input phase currents sinusoidally. Formally, it can be stated as follows [B4]: Given a set of balanced input phase voltages:

$$\begin{aligned} V_a &= V_m \cos(\omega t), \\ V_b &= V_m \cos(\omega t - 120^o), \\ V_c &= V_m \cos(\omega t + 120^o), \end{aligned} \tag{2.1}$$

and a dc output current I_o = constant, find a control law for the six bridge switches in Fig. 2.1(a) such that the synthesized input phase currents have the same low-frequency component as the input voltages in (2.1), that is,

$$\begin{aligned} I_a &= I_m \cos(\omega t - \phi), \\ I_b &= I_m \cos(\omega t - 120^o - \phi), \\ I_c &= I_m \cos(\omega t + 120^o - \phi), \end{aligned} \tag{2.2}$$

and the output voltage V_o = constant. In (2.1) and (2.2), V_m and I_m are the amplitudes of the input phase voltages and currents, respectively, ω the angular frequency of the input line voltage, and ϕ the phase shift between the input voltage and the synthesized input current.

There are many carrier-based and algorithm-based PWM schemes developed for the control of the buck rectifiers. Among them, the six-step PWM or space vector modulation secures minimal switching actions in a PWM period [A2] [B4] [H3]. So it is adopted as the modulation scheme for all the discussed buck topologies in this dissertation. With the six-step PWM, a line cycle is divided into six sectors, each with 60°, as shown in Fig. 2.2. In each sector, the switch corresponding to the phase with highest or lowest voltage can be kept on, and only two switches associated with the other two phases need to be switched. For example, in sector *I* with $\theta \in (-30^o, 30^o)$, which is shaded in Fig. 2.2, S_{ap} for the basic buck topology shown in Fig. 2.1(a) is kept closed, and only S_{bn} and S_{cn} are switched once in each PWM period, T_s.

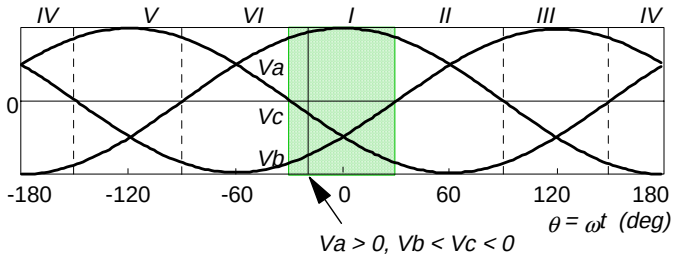


Fig. 2.2. Three-phase input phase voltages.

For the input phase voltages given in (2.1) and shown in Fig. 2.2, the duty cycles of S_{bn} and S_{cn} corresponding to sector *I* in Fig. 2.2, denoted as d_1 and d_2 respectively, are given by

$$\begin{aligned} d_1 &= T_1 / T_s = m\left|\cos(\omega t - 120^o)\right|, \\ d_2 &= T_2 / T_s = m\left|\cos(\omega t + 120^o)\right|, \\ d_0 &= T_o / T_s = 1 - (d_1 + d_2), \end{aligned} \tag{2.3}$$

where $\omega t \in$ (-30°, 30°), d_o is the "zero" or freewheeling duty cycle, T_1 and T_2 are the corresponding duty-times, respectively, and $m \in [0, 1]$ is the modulation index defined as

$$m \equiv \frac{V_o}{(3/2)V_m}. \tag{2.4}$$

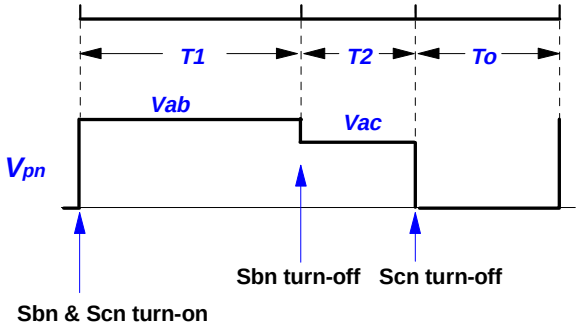
If the input currents are controlled to be in phase with the input voltages, then $\phi = 0^o$, and the output voltage is given as

$$V_o = \frac{3}{2} m \cdot V_m \cdot \cos\phi = \frac{3}{2} m \cdot V_m. \tag{2.5}$$

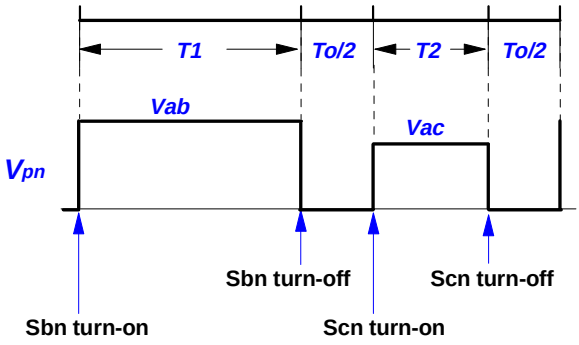
Analogous to the PWM schemes for the popular VSIs, the zero duty-cycle can usually be disposed within a PWM cycle in different ways, resulting in different PWM patterns and different converter behaviors in terms of harmonic spectra, and switching losses.

Two basic PWM patterns for the buck rectifier are shown in Fig. 2.3. The pattern shown in Fig. 2.3(a) has a concentrated zero duty-cycle T_0, while the two active duty-cycles T_1 and T_2 are stacked together. As a result, the two switches in action can be turned on at the same time, with the bigger duty-cycle T_1 ended with the turn-off of S_{bn}, the circuit automatically changes to duty-cycle T_2. Notice that when S_{bn} turns off, the voltage transition across it is only the difference between the two acting line-to-line voltages. This results in a considerable reduction in turn-off loss of the circuit. To secure the operation with this PWM pattern, the bigger duty-cycle needs to be always exercised first. This pattern is favorable for ZVT type of soft-switching schemes because the commutation circuit needs to

be activated once in a PWM cycle. Later in Chapter 5, it will also be shown that this pattern is easy to generate with the proposed charge control scheme. In carrier based modulation realization, it can be generated with two phases of saw-tooth type of carriers instead of the triangular carriers normally used. The only disadvantage of this pattern is that the amplitude of the switching frequency ripple on the output filter inductor is larger.



(a) PWM with concentrated zero duty-cycle.



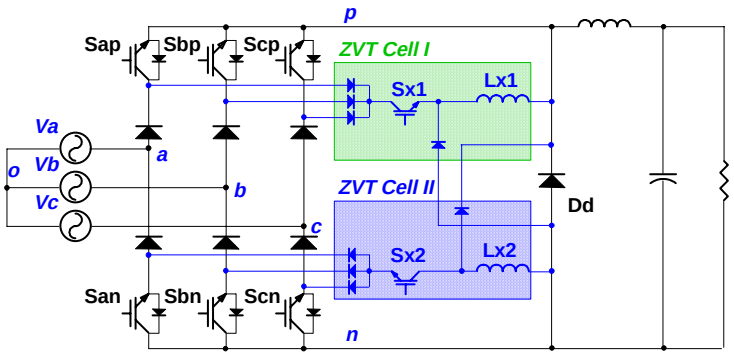
(b) PWM with distributed zero duty-cycle.

Fig. 2.3. Six-step PWM patterns for buck rectifiers.

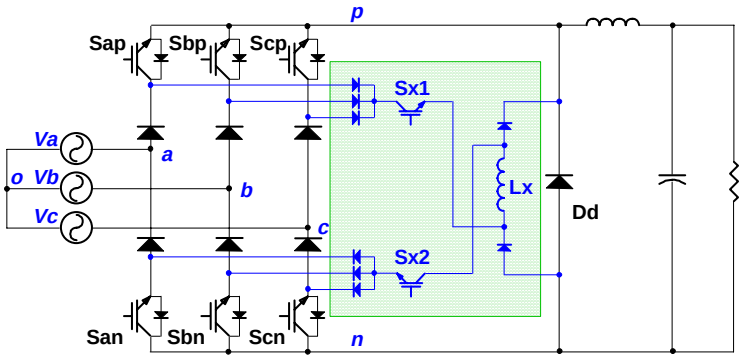
The PWM pattern shown in Fig. 2.3(b) has the equally distributed zero duty-cycle within a PWM cycle. It can be generated with two phases of triangular carriers in carrier-based modulation. All the switching instants with this pattern happen separately. So the resulting switching loss is higher. However, it is optimal for the current ripple of the output inductor.

2.2.3 Soft-Switching Schemes

As reviewed in Chapter 1, there is hardly any mature soft-switching scheme for non-isolated buck rectifiers available. A relatively promising scheme is shown in Fig. 2.4(a) [H9]. As can be seen, one ZVT commutation cell plus some guiding diodes connected to the middle point of the switch and diode connection is responsible for each of the upper and lower half of the buck rectifier bridge. By doing so, ZVS turn-on can be achieved for the bridge switches. Given the fact that the two ZVT cells never need to be activated simultaneously, the two commutation inductors can be combined into one, and the circuit can be simplified as shown in Fig. 2.4(b).



(a) A ZVT buck rectifier [H9].



(b) Simplified ZVT rectifier.

Fig. 2.4. ZVT buck rectifier.

The high-frequency operation waveforms of the ZVT buck rectifier are shown in Fig. 2.5 for the input phase voltages in (-30°, 0°) of sector *I* in Fig. 2.2. The pattern with the concentrated zero duty-cycle is adopted for the reason discussed above. It can be seen that both S_{bn} and S_{cn} are turned on at the same time under zero voltage.

From Fig. 2.5, it can be seen that the first duty-cycle is distorted by the ZVT intervention. As a result, the input current for phase *b* presents peculiar shape which is not quite easy to compensate. The charge control technique developed later in Chapter 5 can be a good candidate to tackle the problem.

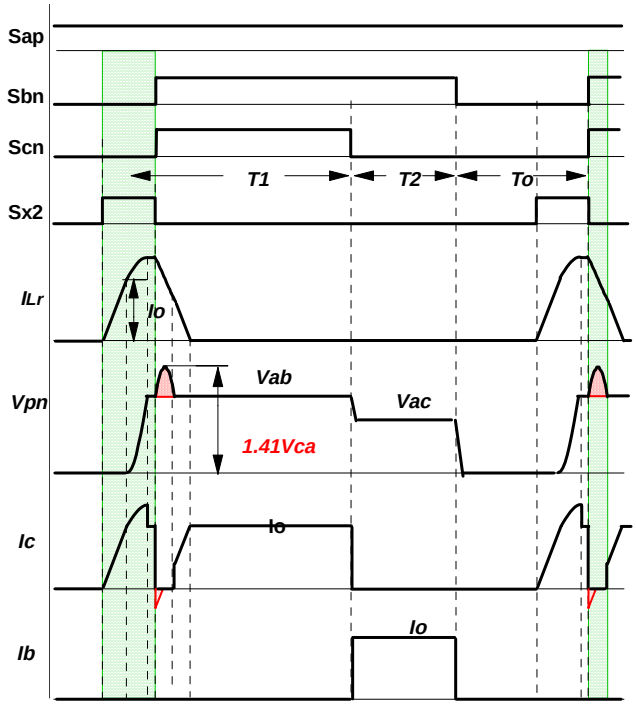


Fig. 2.5. High-frequency operation waveform of ZVT buck rectifier.

A temporary over-voltage resulting from the discharging of the energy trapped in the commutation inductor L_x builds up on the dc-side simply because the buck rectifier is current-unidirectional. Simple calculation shows that the peak voltage can be 1.4 times the input line-to-line voltage at that moment. It will be lower in the actual circuit because of the

losses in the commutation circuitry. Another factor to consider is the difficulty in circuit layout of this converter due to the massive distribution of the commutation circuitry.

2.2.4 Cascaded Three-Phase Buck Rectifier

A so-called cascaded buck-rectifier topology is shown in Fig. 2.6. It consists of a six-switch buck bridge and a buck PWM cell in direct series connection without intermediate filtering components. With this topology, low switching loss can be achieved by using only one fast switch in the buck PWM cell, while the front buck bridge switches can switch on and off stressless. It can be clearly seen in Fig. 2.6 that because the dc-rail buck switch is in series (or cascading connection) with the front buck bridge switches, so the load current can be switched on and off by one of them. By proper timing relative to each other, all or most of the switching losses originally incurred in the bridge switches, S_{ij}, $i \in \{a, b, c\}$, and $j \in \{p, n\}$, can be transferred to the dc-rail switch. This is realized by turning-on the bridge-switches S_{ij} before S_d and turning-off S_{ij} after S_d, as shown in the timing diagram in Fig. 2.7. A small dead time, T_d, is inserted between the switching of the bridge switches and the dc-rail switch to secure commutation of the bridge switches under zero-current condition.

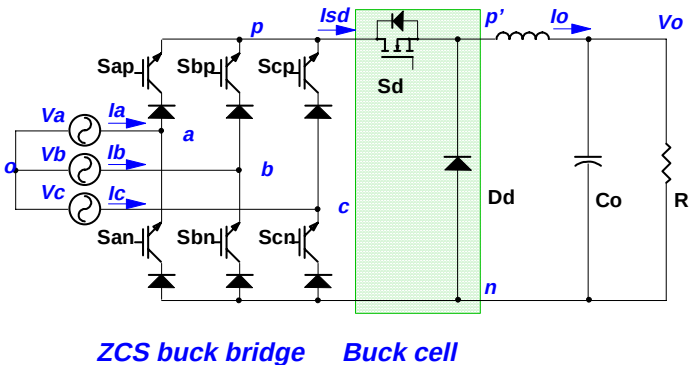
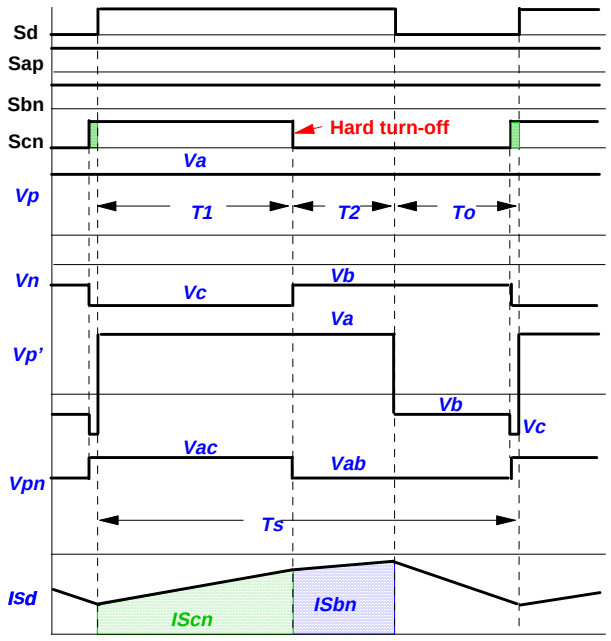


Fig. 2.6. Cascaded three-phase buck rectifier.

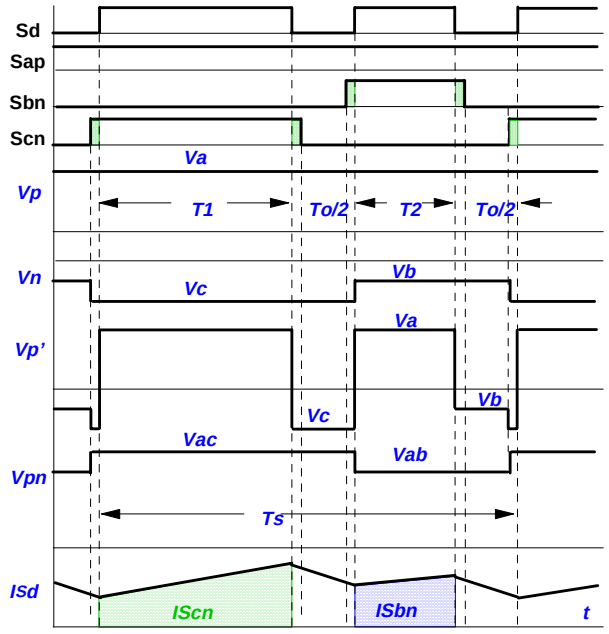
As discussed above, the PWM pattern with concentrated zero duty-cycle features the bigger duty-cycle T_1 directly followed by the smaller duty-cycle T_2 in a high-frequency PWM cycle, while the complete zero duty-cycle T_0 ensues, as shown in Fig. 2.7(a). With this pattern, only one bridge switch, S_{cn} in this case, needs to be switched in a PWM cycle, while the other switching action is done by the dc-side switch, S_d, instead. As a result, almost all the turn-on losses happen in the buck cell if S_{cn} is turned on earlier than S_d. Although the bridge switch needs to hard turn off the load current at the end of the big duty-cycle, the voltage swing is always less than half of the input line-line voltage, and the average turn-off loss is only about 21% of that happening in the whole converter.

In the PWM pattern with distributed duty-cycle as shown in Fig. 2.7(b), the bridge switches do not need to switch any current and function only as a switching network to rectify the input three-phase ac voltage into a high-frequency pulsating dc voltage on the dc side, while the duty-cycle control, and therefore, the input PFC and output voltage regulation are all furnished by the S_d. Notice that in this case the buck cell switch S_d needs to switch twice in one PWM cycle, and almost all the major switching losses in the circuit happens inside it. Thus, a fast device, e.g. MOSFETs or fast IGBTs should be used for it.

As is clear from Fig. 2.7, in the cascaded buck rectifier, the pulsating dc bus voltage V_{pn} never drops below half of the input line-line voltage, so the voltage swing is reduced compared to the original buck rectifier. Only the voltage $V_{p'n}$ swings between 0 and the lower rectified line-to-line voltage. Because the parasitic capacitance of node p' is also relatively small, the common-mode noise performance for the cascaded buck rectifier should be better, esp. with the PWM pattern with concentrated zero duty-cycle.



(a) PWM with concentrated zero duty-cycle.



(b) PWM with distributed zero duty-cycle.

Fig. 2.7. Six-step PWM patterns of cascaded buck rectifier.

The switching losses in the converter can be reduced with a fast-recovery diode used for D_d and a fast switch for S_d. Further reduction of switching losses can be achieved by implementation of suitable soft-switching for S_d and/or D_d, as is done for the three-phase voltage-source inverter/boost rectifier with a dc-rail switch/diode [C23]-[C25]. Basically, any soft-switching techniques available for simple buck dc-dc converters can be transplanted almost without modification. The circuit schematic with a ZVT cell is shown in Fig. 2.8, and the addition of auxiliary components is minimal considering the setting for a three-phase rectifier. The corresponding operation waveforms are illustrated in Fig. 2.9. The main operation waveforms are essentially the same as shown in Fig. 2.5 for the previous ZVT buck rectifier.

2.3 Concept of QSS Power Conversion

2.3.1 Definition of QSS Power Converter

From the above example of the cascaded buck rectifier, it can be seen that with the direct cascading of two buck (or boost) power conversion units, a series connection of two switches along the power transfer path is created. If the switching instants of the two units are further synchronized, one of the series switches can assume most or all the switching losses by turning-on later and turning-off earlier than the other switch. In other word, one of the cell takes most of the responsibility to synthesize the duty-cycle and the other one just run at full duty-cycle. In the previous example, the front buck bridge basically runs at the modulation index which approaches one.

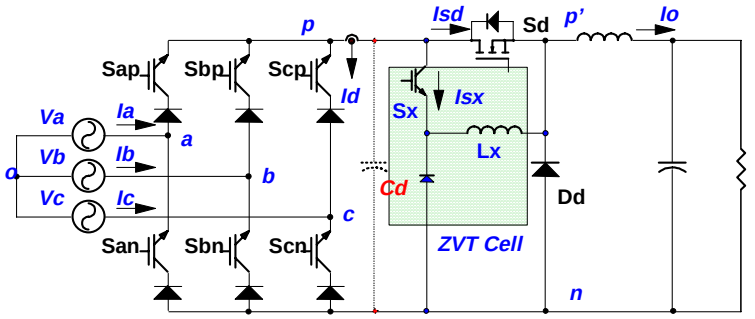


Fig. 2.8. ZVT realization for cascaded buck rectifier.

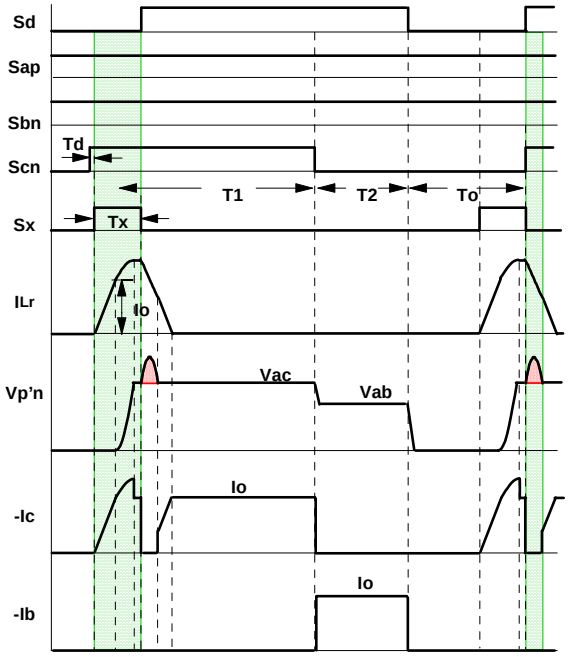


Fig. 2.9. Operation waveforms of cascaded buck rectifier with ZVT.

Generalizing this idea leads to the concept of the generic QSS power conversion topology, which is defined as follows:

Definition of QSS Power Conversion Topology: *A QSS power conversion topology is a converter for ac-dc rectification, and/or dc-ac inversion, which is composed of two buck or two boost PWM switching networks in direct cascading and with synchronized switching. Each of the PWM switching networks can be an elementary PWM cell, a full-bridge with or without isolation, or a three-phase bridge etc., which is capable of either unidirectional or bi-directional power flow.*

The concept is graphically illustrated in Fig. 2.10, where the dotted lines show the case of three-phase ac terminal connections. The intermediate bus between the two PWM units carries in most cases a pulsating dc voltage. Its unipolar pulsating nature can facilitate the implementation of circuit functions such as voltage clamping, and ZVS etc.

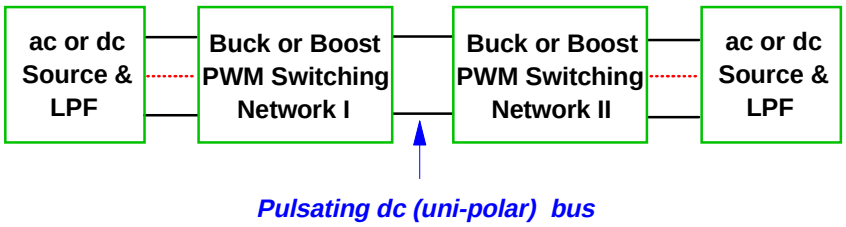


Fig. 2.10. Generic QSS power conversion topology.

Because the equivalent function of the series connection of two buck (or boost) units is still of buck (or boost) type, the low-pass filters (LPFs) at the two ends have to be of dual nature. For example, a QSS buck converter will have a capacitive input filter while a inductive filter at the output.

It is noted that although the direct cascading of a buck PWM switching network and a buck-boost PWM switching network, or a buck-boost PWM switching network and a boost switching network also leads to functional QSS power conversion circuits, they are intentionally excluded from the definition of the generic QSS topology above simply because of their limited practical values in high-power applications.

2.3.2 Generic Features of QSS Power Conversion Topology

The generic features of the proposed QSS power conversion topology are summarized as follows:

1) The circuit topology always has two buck or boost PWM switching networks of the same kind in cascading;

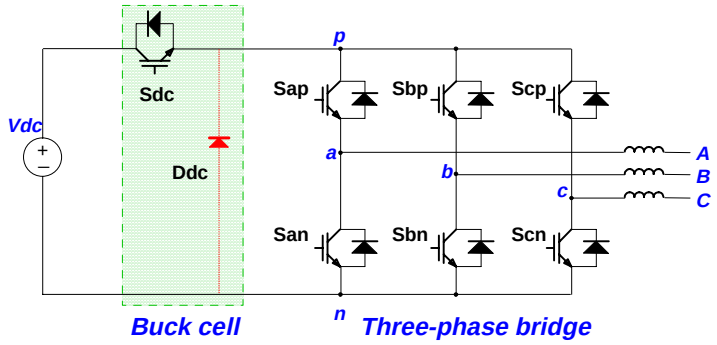
2) Single-stage power conversion is realized in the sense that the load current is switched by the power devices in either one of the two PWM switching networks;
3) Inherent soft-switching capability is built in the topology for part of the circuit, usually one of the two PWM switching networks;
4) Minimum auxiliary commutation circuitry is required to realize soft-switching, esp. in isolated cases;
5) Simpler PWM pattern and control can be used compared with matrix or cycloconverter type of circuit topology;
6) Higher efficiency and reliability can be realized thanks to the single-stage power processing and soft-switching capability.

2.4 Other Non-Isolated Three-Phase QSS Topologies

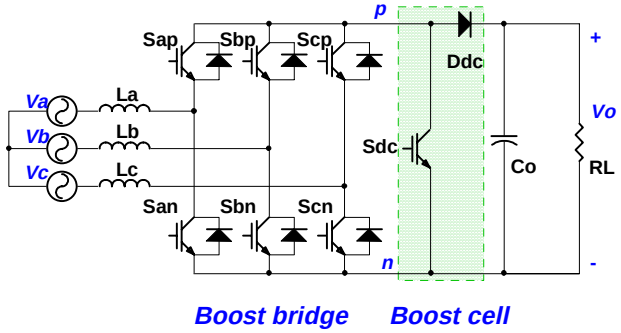
2.4.1 Cascaded VSI/CSR

As reviewed in Chapter 1, many of the dc-side soft-transition VSIs need a serial switch on the dc link to disengage the source voltage and create the voltage notch across the three-phase bridge during the bridge switch turn-on instants. Such a scheme without the auxiliary soft-commutation circuitry is shown in Fig. 2.11(a). The circuit can be considered as two buck units, an simple buck cell and a VSI bridge in cascading. The function of the diode D_{dc} is apparently redundant with the freewheeling diodes in the VSI bridge, so it can be removed. As explained in [C25], with the dc-side switch S_{dc} there, ZVT commutation circuit needs to be constructed for only S_{dc} with one or two extra switches, dependent on the power factor of the ac load. At the same time, a majority of the turn-off loss which

otherwise happens in the bridge switches can be shifted to the S_{dc}, where it is easier to reduce.



(a) Cascaded VSI.



(b) Cascaded boost rectifier (or CSR).

Fig. 2.11. Cascaded VSI/CSR.

The cascaded boost rectifier is shown in Fig. 2.11(b). It consists of a three-phase boost bridge and an elementary boost cell in direct cascading. A variation of this circuit with just the dc-side diode D_{dc} was proposed to facilitate the ZVT implementation, shoot-through protection, and six-step PWM realization [C23]. Although the extra switch in the circuit is again redundant, it is used to divert the switching loss otherwise happening in the main bridge to that switch. It can be shown that if the input power factor is unity, almost all the turn-on loss and 73% turn-off loss can be transferred to S_{dc}. As a result, various soft-

switching schemes can be implemented just for S_{dc} to reduce the total switching loss in the circuit.

It can be easily seen that both of the circuits have series elements in the main power path, and extra conduction losses are incurred. Even the shunt switch S_{dc} in Fig. 2.11(b) increases the conduction loss of the circuit, which happens when the input PFC inductors are charged with the S_{dc} closed to provide the charging path. For these reasons, the practical values of these circuits seem limited.

2.4.2 QSS AC-AC Converter

The QSS ac-ac converter as shown in Fig. 2.12 was introduced in [A61] as an alternative to the well-known nine bi-directional matrix converter. It was also used to illustrate the space vector modulation concept in [A68]. The voltage across *p* and *n* is pulsating with a constant average dc value in the line cycle in steady-state operation. If the load at the output side can run into any power factor, current feedback path is required. Therefore, a bi-directional buck front bridge is necessary. The total number of switches is the same as a matrix converter. If the load side phase-shift is constantly less than 30^{o}, only a current unidirectional buck bridge with three or six active switches is necessary, leading to some saving in cost.

The creation of a pulsating dc bus which is connected to all the six converter legs makes it possible to place a small snubber capacitor across the bus to absorb the voltage ringing caused by the layout parasitic inductance. Switching loss scheduling and distribution inside the circuit is an interesting and untouched topic.

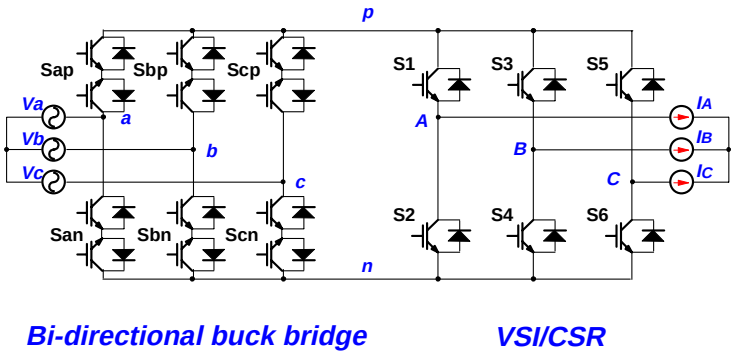


Fig. 2.12. QSS ac-ac converter.

The creation of a pulsating dc bus which is connected to all the six converter legs makes it possible to place a small snubber capacitor across the bus to absorb the voltage ringing caused by the layout parasitic inductance. Switching loss scheduling and distribution inside the circuit is an interesting and untouched topic.

2.5 Summary

The general topological concept of quasi-single-stage (QSS) isolated power conversion is introduced and defined with an illustrative example of cascaded buck rectifier. The same example also serves as an introduction to the issues pertaining to the buck rectifiers. The family of QSS power converters features single-stage power processing without a dc-link low-pass filter, a unidirectional pulsating dc-link voltage, soft-switching capability with minimal extra commutation circuitry, simple PWM control, and high efficiency and reliability. Some other non-isolated QSS power conversion examples including VSI/CSR, and matrix converter are also given.