Low-Temperature Sintering of Nanoscale Silver Paste for Semiconductor Device Interconnection

by

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ABSTRACT

This research has developed a lead-free semiconductor device interconnect technology by studying the processing-microstructure-property relationships of low-temperature sintering of nanoscale silver pastes.

The nanoscale silver pastes have been formulated by adding organic components (dispersant, binder and thinner) into nano-silver particles. The selected organic components have the nano-particle polymeric stabilization, paste processing quality adjustment, and non-densifying diffusion retarding functions and thus help the pastes sinter to ~80% bulk density at temperatures no more than 300°C. It has been found that the low-temperature sintered silver has better electrical, thermal and overall thermomechanical properties compared with the existing semiconductor device interconnecting materials such as solder alloys and conductive epoxies. After solving the organic burnout problems associated with the covered sintering, a lead-free semiconductor device interconnect technology has been designed to be compatible with the existing surface-mounting techniques with potentially low-cost. It has been found that the low-temperature sintered silver joints have high electrical, thermal, and mechanical performance. The reliability of the silver joints has also been studied by the 50-250°C thermal cycling experiment. Finally, the bonging strength drop of the silver joints has been suggested to be ductile fracture in the silver joints as micro-voids nucleated at microscale grain boundaries during the temperature cycling.

The low-temperature silver sintering technology has enabled some benchmark packaging concepts and substantial advantages in future applications.

To my wife, Qing

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NOMENCLATURE

c	Heat capacity, J/Kg-K
d	Thickness, m
E	Elastic Modulus, GPa
I	Current, A
K	Thermal Conductivity, W/m-K
L, l	Length, m
m	Mass, Kg
R	Electrical Resistance, Ω
R_{th}	Thermal Resistance, K/W
$1/R$	Curvature, m^{-1}
S	Area, m^2
T	Temperature, °C
t	Time, s
V	Voltage, Volt
α	Thermal diffusivity, m^2/s
v	Poisson's ratio
ρ	Density, Kg/m^3
ρ_e	Electrical Resistivity, $(\Omega \cdot m)^{-1}$
σ	Stresses, MPa

ACRONYMS

AC	Alternative Current
BGA	Ball Grid Array
CPES	Center for Power Electronic Systems
CSP	Chip-Scale Package
CTE	Coefficient of Thermal Expansion
DBC	Direct Bond Copper or Direct Copper Bonding
DC	Direct Current
DSC	Differential Scanning Calorimetry
EDS	Energy Dispersive Spectrometry
FAST	Field-Activated Sintering Technique
FEA	Finite Element Analysis
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IPEM	Integrated Power Electronic Module
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
POL	Power OverLay
PZT	Lead Zirconate Titanate
SAM	Scanning Acoustic Microscopy
SEM	Scanning Electron Microscopy
TGA	Thermogravimetric Analysis
UBM	Under Bump Metallization
XPS	X-ray Photoelectron Spectroscopy

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Chapter 1
Introduction

Electronic packaging provides electrical connection or isolation, thermal cooling, mechanical support, and physical protection for power electronic components that make up the circuits. Therefore, the overall performance of a single-chip power package, a multichip power module as well as a whole power system is not only determined by the electrical components and the circuit layouts, but also affected by their packaging technology. Over last twenty years, industrial and academic research efforts on electronic power conversion are making the move toward high-frequency synthesis, which results in great improvement in converter performance, miniaturization in physical size and reduction of mass weight and loss. It is pushing the limits of existing power packaging and thermal management technology. On the other hand, wide-bandgap semiconductors such as silicon carbide (SiC) based electronic devices and circuits are presently being developed for advantageous use in high-temperature, high-power, and/or high-radiation conditions. The applications of SiC pose another significant challenge for packaging of these electronic devices. The conventional technology for interconnecting power devices typically involves die-attaching one terminal of the semiconductor die to a heat-sinking substrate with solder alloys or conductive epoxies and wirebonding fine aluminum or gold wires to the other terminal(s). Such an interconnect technology is not able to meet the high-temperature operating requirement of the wide-bandgap devices. It is device interconnecting and packaging technology the dominant technical barrier that currently limits the rapid growth of power electronics. New interconnecting materials and technologies are needed before high-temperature devices and circuits can be scaled-up and reliably incorporated into power electronic systems.

The sintering of powder compacts has been widely applied in microelectronics for making hybrid circuits, cofired multilayer metal/ceramic interconnecting substrates, multilayer ceramic capacitors, magnetic components, and etc. Since the conventional

sintering normally requires a temperature that may be substantially higher than the maximum temperature a semiconductor device can tolerate, any means of lowing the sintering temperature is desirable and necessary for the successful implementation.

This research presents a new semiconductor device interconnect technology using low-temperature sinterable nanoscale silver pastes for electronic packaging applications. First, the silver pastes were formulated through a metal colloidal/paste process with the aid of cutting-edge nanotechnology. Then a new power device interconnect technology was developed and the reliability of the low-temperature sintered silver joints was evaluated and their failure mechanisms were discussed. Finally, the potential applications of the technology were demonstrated at conceptual levels.

1.1 Overview of Power Electronic Packaging

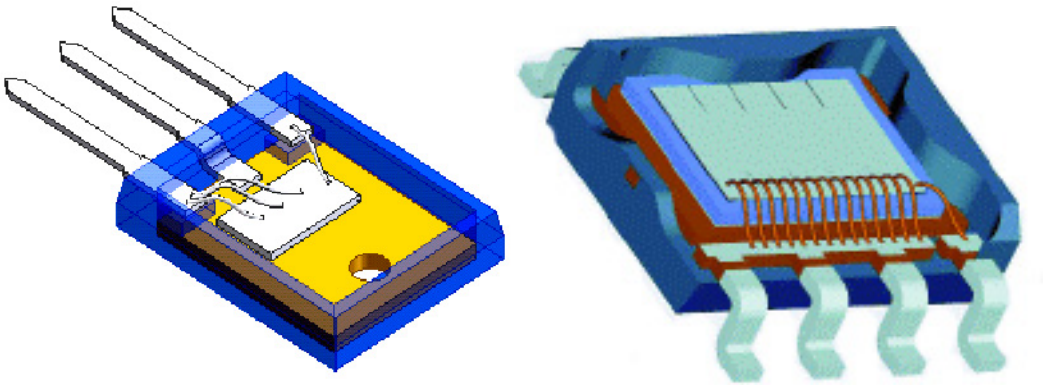
Hierarchically, electronic packaging begins from the interface of a semiconductor chip itself--which is considered as the first-level or chip-level packaging--to higher levels of packaging such as board-level and system-level packaging. Chip-level packaging deals with the attachment of one or more bare chips to a substrate, the interconnection from these chips to package leads, and encapsulation. In power electronic systems, the first-level chip interconnection plays a vital role because it directly interfaces with the power chips that contain millions of transistor circuits not only electrically but also thermally and mechanically. It has to fulfill very different requirements compared with those for microelectronic integrated circuit (IC) chips. Firstly, since power devices typically operate at high switching frequencies, parasitic noises must be reduced in order to maintain a high level of circuit performance and efficiency. Secondly, compared with IC interconnections, larger cross-sectional areas and current-handling capabilities are needed in power interconnections because the flowing current increases by several orders of magnitude. Furthermore, the increased power density drives the first-level packaging to improve its roles in heat dissipation and thermal management. At last, the reliability of the first-level power interconnections is essential to ensure the electronic systems to have an extended lifetime.

1.1.1 Current Chip-Level Interconnect Technologies

A. Wirebond

The traditional chip-level interconnect technology in power electronics is wirebond. This is primarily due to the fact that the technology can easily accommodate changes in package design with the minimum modification of facilities and lowest cost per interconnection. The flexibility and the low cost combined with a continuous effort in reliability improvement indicate that wirebond will continue to be the prominent method for chip-level interconnections [1].

In a typical single-chip package, the source and gate terminals are connected from the aluminum chip bonding pads to nickel-plated copper leads. The chip and wirebonds are encapsulated with molding compound for insulation, mechanical support and protection. Figure 1.1(a) shows a wirebond transistor-outline package (TO-247) and (b) shows the famous small outline package (SO-8) with the top molding hidden for clarity. The die-attachment of the devices is connected by solder reflow.



(a) (b)

Figure 1.1. Top views of the wirebond TO-247 (a) and SO-8 (b) MOSFET packages.

In a wirebond multichip power module, a direct bond copper (DBC) substrate (see Appendix A) is usually used for attaching the switching devices. The die-attach material is usually solder. Aluminum wires ranging from 5 to 20-mil (125-500 μm) thick are used to connect power chips and conductor leads (or traces) at the periphery of the power module. In order to achieve high current capability, several power chips may be used in parallel and connected by tens or even hundreds of aluminum bonding wires, as shown in Figure 1.2.

The ultrasonic bonding is the most common method for wirebond process. The aluminum wires are bonded to aluminum metallization on chip pads without use of a heat source. During the process, an aluminum wire is first passed through a hole in a capillary. By applying a continuous downward force and ultrasonic horizontal rubbing (60 to 120 kHz) of the wire to the bonding surfaces, the aluminum wire plastically deforms and breaks the aluminum oxide layers to allow a pure aluminum-to-aluminum contact. After the first bond, the bonding machine forms a second bond between the wire and the nickel-plated copper substrate to finish a bond cycle.

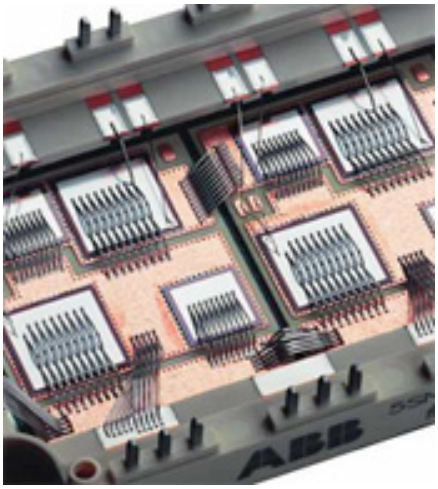


Figure 1.2. Top view of a wirebond multichip power module.

In a wirebond power package, the wirebond and the top-metal-sheet resistances contribute about 90% of the packaging resistance. They are the primary contributors to electrical and thermal losses from packaging. The wirebonds also have significant parasitic inductance at high frequencies and they are one of the causes of failure. Therefore, several alternative chip-level interconnect technologies have been developed to eliminate the bonding wires.

B. Deposited metallization

One of the wirebond-free interconnect technologies is the metal deposition method. In this method, device interconnections are constructed with metals (usually copper) that are deposited directly on the device electrodes. The deposited metals form power and signal linkages from power chips to the rest of the circuit. The metal deposition covers both physical (sputter and e-beam) and chemical (electroplating and electroless-plating) ways. Since metal deposition could be processed in parallel, the

technology has advantages in making multichip power modules. Representative packaging schemes using deposited metallization include General Electric's (GE's) power overlay (POL) [2] and the embedded power developed in the Center for Power Electronics Systems (CPES) [3].

The POL technology proposed by GE eliminated wirebonds through the use of metallized copper via holes in a polyimide film. As shown in Figure 1.3, POL has a multilayer structure, which includes power semiconductor devices soldered to a DBC substrate from the backside, the polyimide dielectric layer, and the deposited copper on the topside. Differences in device thickness are compensated by copper-tungsten or molybdenum shims.

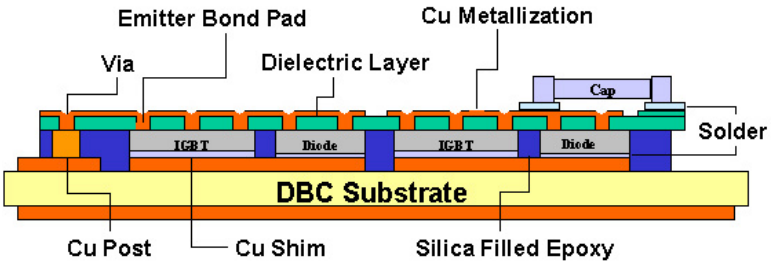


Figure 1.3. Cross-sectional schematic of power overlay module [2].

The fabrication process of GE's POL power module starts with laser-drilling or mechanical punching of via-holes in a polyimide film. Power devices are then attached to the bottom side of the polyimide film using a special adhesive with the device electrodes accurately aligned with the via-holes. Next, topside of the whole assembly is metallized with titanium, nickel and copper using sputtering and electroplating process. The sputtering of titanium, nickel and copper is similar to the under bump metallization (UBM) schemes used in the IC packaging. Proper circuit patterns are then formed through wet-etching of the deposited metal layers. After cleaning, the devices along with the left copper/polyimide layers are solder-attached to an etched DBC substrate. A final step of silicone gel-filling is needed to protect devices from moisture. Figure 1.4 is a top view of a prototype POL converter module fabricated in CPES at Virginia Tech. Because the process can be realized by fine resolution photolithography, the POL interconnect technology is capable of achieving high density interconnections with via-hole diameter down to 0.25 mm (10 mil).

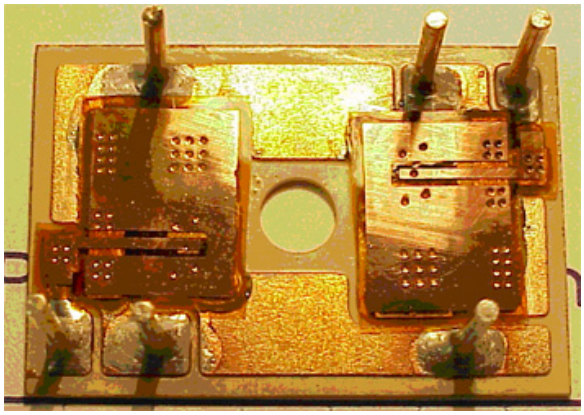


Figure 1.4. A prototype of power module packaged using power overlay interconnect technology.

Another interconnect strategy using the metal deposition method is called embedded power [3]. Different from the POL, which uses the polyimide films, the embedded power applies ceramic substrates and screen-printed dielectric materials. Figure 1.5 shows a cross-sectional schematic of an embedded power module. There are three major parts in the structure: the control circuit on the top, the embedded power stage in the middle, and the base substrates at the bottom. The core element in the structure is the embedded power stage constructed by the laser-cut ceramic frames, the inserted power chips, the dielectric fillings and the deposited metallization layers.

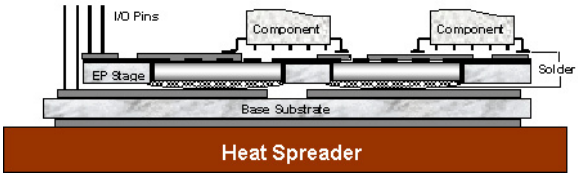


Figure 1.5. Cross-sectional schematic of embedded power module [3].

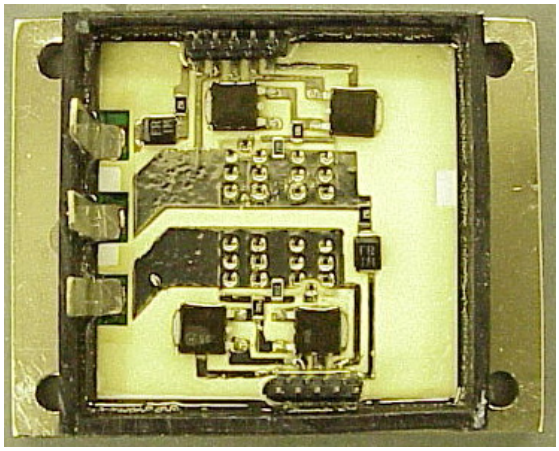


Figure 1.6. An IPEM packaged by the embedded power technology [3].

The metal deposition process in embedded power is similar to GE's POL. Figure 1.6 shows an integrated power electronics module (IPEM) packaged by the embedded power interconnect technology.

Generally speaking, the electrical performance and efficiency of a deposited metallization power module are significantly improved compared to a wirebond power module mainly due to the reduction of packaging inductance.

C. Solder interconnections

Solder interconnection is another effective strategy to get rid of wirebonds. Actually either in a wirebond or in a deposited metallization (both POL and embedded power) power package, solder reflow is already used for attaching power chips onto metallized substrates. In some other power packages, solder is not only used for the die-attachment, but also used for the interconnections of the top electrodes (gate and source) of the power chips. These technologies are usually referred to solder interconnections. The origin of solder interconnections dates back to the early 1960s, which is known as the IBM's controlled collapse chip connection (C4) technology [4]. In recent years, there was a continuous progress to apply more solder interconnections in power electronics. Follows we introduce several power packaging concepts that utilize solder interconnections.

Vishay Siliconix has developed a PowerConnect technology to replace the traditional wirebonds with direct interconnections between the die and the copper leadframe, as shown in Figure 1.7 [5]. To accomplish the solder interconnections, the top surface of the power MOSFET was made solderable by developing a nickel-based metallization on top of the aluminum pads. The leadframe can be attached to both the bottom and top surfaces of the die. It is reported that the resistance contribution by the interconnections has been cut down to less than 1 mΩ, thereby doubling the current capability of the low-voltage MOSFET in an SO-8 package. The power dissipation has also been enhanced. However, reliability is a big concern in the PowerConnect structure because of the coefficient of thermal expansion (CTE) mismatch between the large-area copper leadframe and the silicon die.

To mitigate the reliability concerns due to the large-area interconnections between CTE mismatched copper and silicon, Fairchild Semiconductor developed a SO-8 wireless

package [6] use solder bumps to reduce the interconnect resistance and improve heat transfer. The package outline is the same as the conventional SO-8 package as shown in Figure 1.8. The majority of heat is still conducted through the bottom drain leadframe while the solder bumps can also be served a heat path.

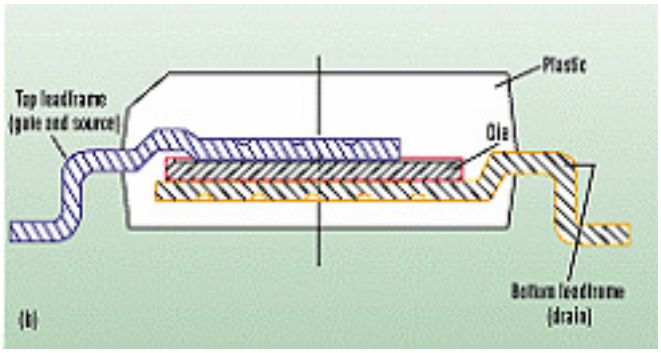


Figure 1.7. Cross-sectional schematic of a PowerConnect chip-level power package [5].

Figure 1.8. Cross-sectional view of a SO-8 Wireless chip-level power package [6].

Wireless versions of the SO packages reduce the package resistance but do not significantly improve the thermal performance. Fairchild Semiconductor's Bottomless package as shown in Figure 1.9 [7] accomplishes both goals simultaneously by eliminating the bottom drain leadframe and allowing the solderable backsides of the MOSFET die to directly contact printed circuit board (PCB) substrates by solder reflow. The top source leadframe keeps the same as in the Wireless and still uses solder bumps for interconnection. As a result, package resistance is further reduced and it can handle 60% more current than the same die in a conventional SO-8 package. It is also reported that the Bottomless reduces the junction-to-case thermal resistance below 1°C/W, which is a dramatic improvement from 25°C/W in a conventional SO-8 package.

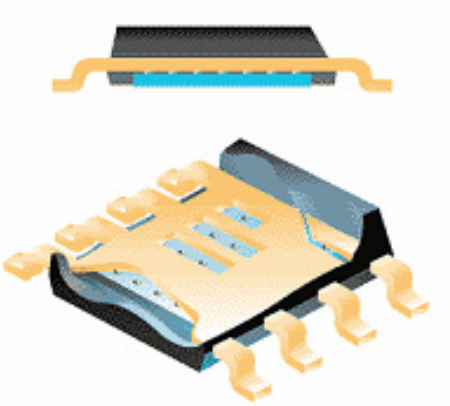


Figure 1.9. Chip-level power packages interconnected by SO-8 Bottomless technology [7].

In 1999, Fairchild Semiconductor introduced new low-$R_{DS(on)}$ power MOSFETs in the form of solder ball grid array (BGA) chip-scale package (CSP) [8]. To overcome the drawbacks in a traditional package, Fairchild Semiconductor encased the low-voltage MOSFET in a fine-pitch BGA for flip-attachment of the CSP onto a PCB substrate using the surface mount technology. Figure 1.10 shows the structure of a BGA power MOSFET package. By allowing direct connection using solder balls, BGA MOSFET eliminates the undesired parasitic contribution from wirebonds or leadframes. Furthermore, BGA MOSFET is only 0.7-mm high and it consumes less than 50% the PCB area for a conventional package. Its unique design and construction allow heat to dissipate directly from the die to the PCB board through the solder balls. As a result, BGA MOSFET offers a 35% reduction in on-resistance over the Wireless SO-8 package and improves heat dissipation over 175% compared with the Wireless SO-8 package.

Figure 1.10. Schematic of Fairchild Semiconductor's BGA MOSFET [8].

In 2000, International Rectifier Corporation (IR) introduced a true CSP called FlipFET, in which all of the terminals are on a single side of the die in the form of solder bumps [9]. Figure 1.11 shows a FlipFET power MOSFET package. FlipFET combines the latest die design and wafer level packaging technology to make 100% silicon-to-

footprint ratio possible. Thus, FlipFET is advantageous for advanced portable power application such as digital cameras, MP3 players and cell phones.

Researchers in CPES have also developed a CSP structure termed as the Die-Dimensional BGA (D^2BGA) [10]. Figure 1.12 shows a power MOSFET constructed using the D^2BGA interconnect technology. The D^2BGA power devices have been successfully applied in the Flip-Chip on Flex IPEMs as shown in Figure 1.13 and better electrical performance has been achieved than the conventional wirebond power modules[11].

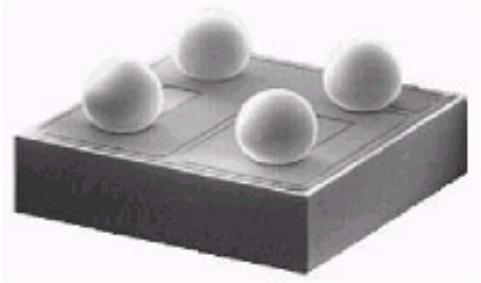
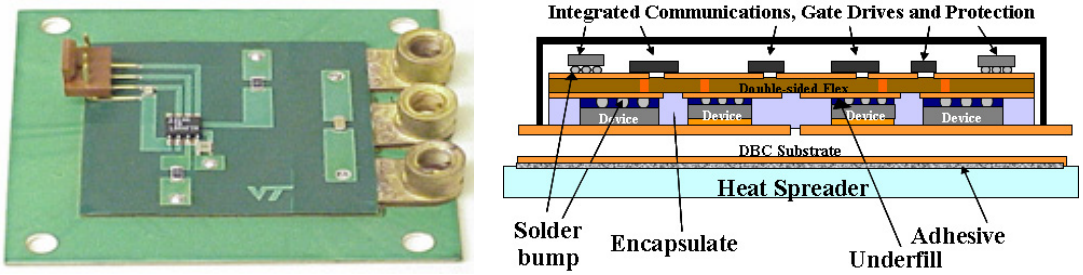


Figure 1.11. IR's FlipFET power MOSFET [9].

Figure 1.12. Die-dimensional BGA power packages developed in CPES [10].



(a) (b)

Figure 1.13. A Flip-chip on flex integrated power electronics module (a) and its schematic structure (b) [11].

Other power packaging structures making use of the solder interconnections with some modifications include Harris Semiconductor's ThinPack [12] and CPES' Metal Post Interconnect Parallel Plate Structures (MPIPPS) [13].

D. Conductive epoxy interconnections

IR's CopperStrap as shown in Figure 1.14 [14] replaces the wirebonds that connect the source to the leadframe with a solid strap that covers the surface of the die. Different from Vishay Siliconix's PowerConnect, silver-filled conductive epoxy is used to attach the copper straps to aluminum pad surfaces of the power dies. Because the conductive epoxy has a much lower elastic modulus than solder and it serves as a stress buffer layer, thermal stresses caused by the CTE mismatch of the copper strap and silicon is reduced dramatically. However, there is a payment for higher packaging resistance.

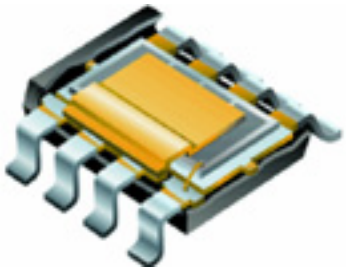
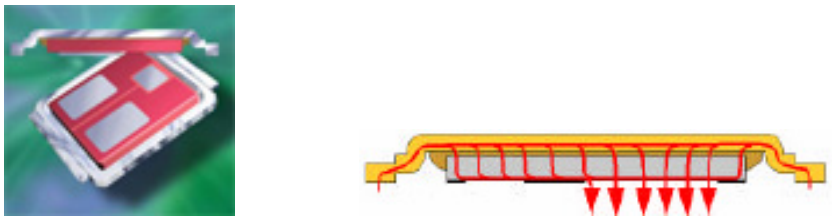


Figure 1.14. A chip-level CopperStrap power package [14].



(a) (b)

Figure 1.15. IR's DirectFET power package (a) and its cross-sectional schematic (b) [15].

Aiming at reducing footprint size and increasing performance, IR released another interconnect technology called DirectFET [15]. Same as that in the CopperStrap, DirectFET uses conductive epoxy that directly mounts a power device into a copper "can" and applies patterned solderable areas for flip-mounting as shown in Figure 1.15. Combining a proper passivation system, a surface mountable package with ultra-low profile is realized. It has only 1/20 junction-to-case thermal resistance compared with the wirebond SO-8 package. DirectFET is among the first commercial packaging technologies which has the double-sided cooling capability.

E. Press pack

Another interesting wirebond-free interconnect technology is the press pack interconnections that was originally developed by Fuji, Toshiba and ABB [16]. The structure has been applied to high power devices such as diodes and gate turnoff

thyristors as shown in Figure 1.16 with proven reliability. Molybdenum is usually applied for less CTE mismatch.

Figure 1.16. Gate turnoff high power devices packaged using the press pack technology [16].

SemiKron International's SkiiPPack [17] is another example using the press pack technology. One of the disadvantages of the interconnect technology is its expensive manufacturing cost involved with precise machining and planarization. Therefore, the press pack technology is only proposed for extremely high power packages so far.

F. Pressure-assisted silver sintering

Silver paste sintering has been widely used in microelectronic packages due to the high electrical and thermal performance of silver [18-20]. However, the paste containing microscale silver powders requires high sintering temperatures (>500^{o}C) that are beyond what semiconductor devices can withstand. Studies [21 - 24] showed that the application of external pressure can lower the sintering temperature of silver pastes. Figure 1.17 shows schematically one of the setups for low-temperature sintering of microscale silver paste with the assistance of external pressures. Compared with the solder reflow interconnection, pressure-assisted silver sintering has the advantages such as more environmental friendly due to the lead (Pb)-free materials, more uniform interconnecting layers, better electrical and thermal performance, and higher reliability. However, similar to the press pack, the application of external pressure tends to complicate the manufacturing process and thus increases the cost.

Other technologies are also being tried to lower the processing temperatures of the silver joints but they are still not fully developed [25].

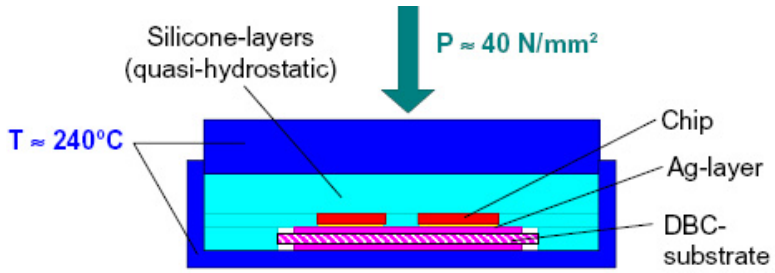


Figure 1.17. Schematic of a pressure-assisted silver paste sintering setup [26].

1.1.2 Summary of Current Chip-Level Interconnect Technologies

In power electronic packaging, it is unlikely to come out a universal chip-level interconnect technology that can cover all the applications from the low-power levels to the extremely high-power levels. Each interconnect technology has pros and cons as summarized in Table 1.1. Therefore, various types of power packages are found in nowadays power electronic market.

Table 1.1. Pros and cons of various chip-level interconnect technologies.

Interconnect technologies	Interconnect materials	Advantages	Disadvantages	Application examples
Wirebond	Pure Al wire or Al wire with 1% silicon or Au wire	High flexibility; Low cost; Improved reliability	Large packaging parasitics; Poor thermal management; Hard for integration	Still dominant power packaging technology
Metal deposition	Ti, Ni, Cr, Cu, Ag, Mo, Au, etc.	3-D integrated structure; Better electrical and thermal performance	High parasitic capacitance; High cost due to sputtering and machining; Reliability concerns	Multichip power modules such as GE's POL and CPES' embedded power
Solder interconnections	Lead-tin or lead-free or high-temperature solders	3-D integrated structure; Better electrical and thermal performance; High Si-to-board ratio	Reliability concerns on large-area soldering; Possible lead contamination	PowerConnect; Wireless; Bottomless; FlipFETs; BGA; D^2BGA
Conductive epoxy curing	Silver or gold filled conductive epoxies	3-D integrated structure; Better overall performance; High reliability	Incapability of high-temperature packaging; Low electrical and thermal conductivity of the materials	CopperStrap and DirectFET
Press pack	N/A	Better overall performance	High cost	Only for extremely high-power
Pressure-assisted silver sintering	Microscale silver pastes	Much better overall performance	Not mature technology; High cost	Only for large-area contacts such as die-attachment

Admittedly, one can see several clear development trends among the incredible abundance through the fast growth of chip-level interconnect technologies.

One of the trends is moving toward higher silicon-to-footprint ratio. For instance, Figure 1.18 shows the discrete power package development roadmap from IR, one of the major power management product vendors. From a merely 10% silicon-to-footprint ratio of SOT-89 in 1985, the number has reached to 100% in today's chip-scale package thanks to flip-chip solder bump technology.

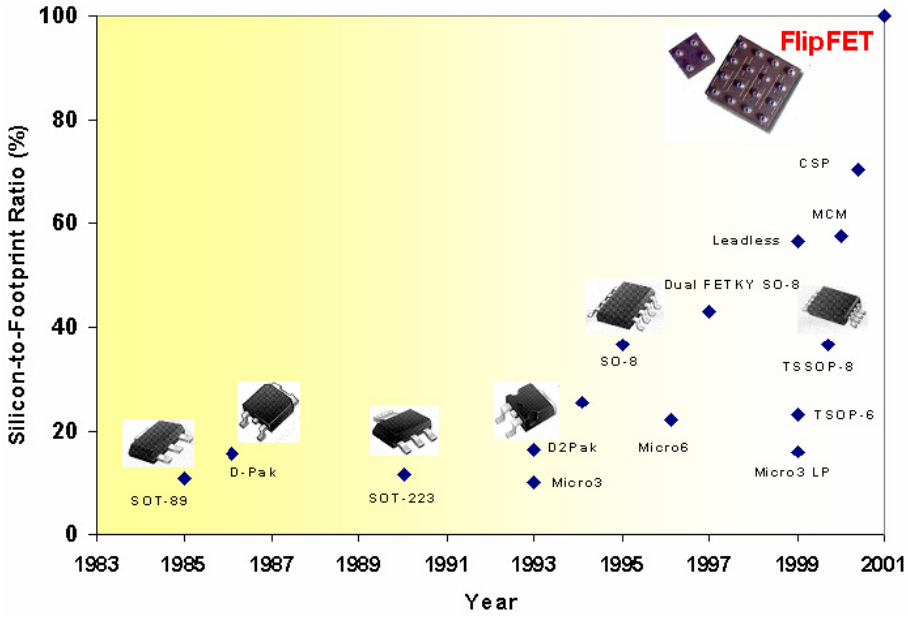


Figure 1.18. Technology roadmap of International Rectifier's chip-level discrete power packages.

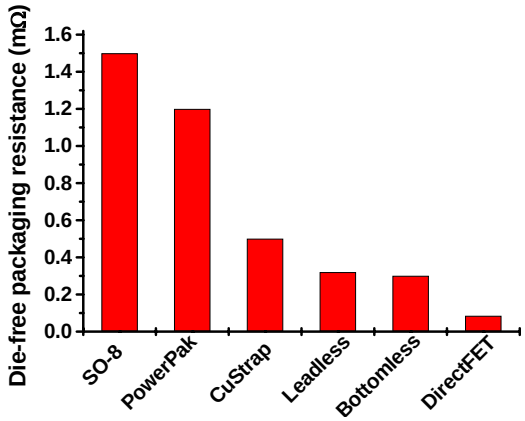


Figure 1.19. Reduction of die-free package resistance along IR's chip-level discrete power package developing roadmap.

Another clear trend in chip-level power packaging is the continuous reduction of die-free package resistance (DFPR) as shown in Figure 1.19. Compared with the

conventional wirebond SO-8 discrete power package, the DFPR of recent DirectFET has reduced from about 1.5 mΩ to less than 0.1 mΩ.

The third trend needs to pay attention to is the thermal management, since power chips are generating lots of heat during their operation. Similar as the electrical resistance, continuous reduction of the thermal resistance also happens. For example, compared with the conventional wirebond SO-8 discrete power package, the silicon to ambient thermal resistance $R_{th(j-a)}$ of the recent DirectFET reduces from about 30°C/W to less than 10°C/W thanks to the advanced packaging technologies and the double-sided cooling method.

At last, reliability of the chip-level interconnections must be considered and evaluated so as to deliver a robust power package that can meet the custom requirements. Strategies have been taken to enhance the reliability of the interconnections whenever possible.

In general, chip-level interconnections are vital components which connect semiconductor devices with the rest of the power systems. Different from microelectronic packages, power electronic packages handle and control electromagnetic energy conversion and transportation instead of signals. A good chip-level interconnect technology for power electronic packaging should meet all the package requirements on integration (silicon-to-die ratio, profile and power density), electrical performance and efficiency, thermal management (power dissipation and junction temperature), reliability (operation life and robustness), and processing complexity (cost objectives). Furthermore, power packages need to accommodate special demands in some applications such as higher operating temperatures or high radiations. The packaging technologies address issues from all of the aspects have better opportunities to stand out.

1.2 Overview of Sintering Theory

Sintering of powder compacts is a process used over thousands of years for making ceramic tools. Today, sintering is employed in a diverse range of products that include rocket nozzles, ultrasonic transducers, automobile engines, semiconductor packaging substrates, and dental implants. There have been considerable research

activities in the materials community aiming at understanding the physics of sintering through the establishment of the connection between controllable variables, such as pressure, temperature, gaseous atmosphere, and particle size [27].

1.2.1 Sintering Mechanisms

Sintering is usually classified into several types based on the mechanisms that are thought to be responsible for shrinkage or densification. Sintering proceeded by solid-state diffusion falls under *solid state sintering*. Polycrystalline materials are usually sintered by this process. On the other hand, amorphous materials are sintered by viscous flow and are considered to undergo *viscous sintering*. Another type of sintering that makes use of a transient second phase that exists as a liquid at the sintering temperature is known as *liquid phase sintering* [28,29]. The liquid phase under the right conditions can provide a path for rapid transport and, therefore, rapid sintering. Finally, processes that make use of an externally applied pressure to enhance densification are classified under *pressure assisted sintering*.

The entire sintering process is generally considered to occur in three stages [30,31]: initial stage, intermediate stage, and final stage. There is no clear-cut distinction between the stages since the processes associated with each stage tend to overlap each other. However, some generalizations can be made to distinguish one stage from the next. In the initial stage, particles can be rearranged into more stable positions by rotating and sliding in response to the sintering forces. This contributes to shrinkage and an overall increase in density. During particle rearrangement, there is an increase in interparticle contact, enabling the formation of necks between particles. Neck formation and growth can take place by diffusion, vapor transport, plastic flow, or viscous flow. The initial stage is assumed to last until a neck radius of around 0.4 to 0.5 of the particle radius is attained. The intermediate stage is considered to begin when the pores have attained their equilibrium shapes as dictated by surface and interfacial energies. Because the density remains low at this point, the pores are still continuous or interconnected. Densification is assumed to take place by the reduction in cross section of the pores. Eventually, pores become unstable and are pinched off from each other, leading to the final stage of sintering. Of the three stages, the intermediate stage covers the majority of the sintering

process. The final stage covers the elimination of the isolated pores until the theoretical density is reached. This stage is also characterized by grain growth in which the larger grains tend to increase in size at the expense of the smaller grains. The extent of grain growth is dependent on both the material and the sintering condition.

Polycrystalline materials generally are sintered by diffusional processes while amorphous materials densify by viscous flow. The driving force for all the mechanisms is the tendency of the material to reduce its chemical potential or energy. This is accomplished by material transport from regions of high energy to regions of lower energy. Surfaces, interfaces and grain boundaries have associated energies that depend on surface or boundary curvature. By eliminating or minimizing these surfaces or by reducing their curvature, the overall energy of the material is reduced. There are at least six different mechanisms of sintering in polycrystalline materials and they are summarized in Table 1.2. Only volume diffusion of matter from the grain boundaries or from dislocations in the neck region can produce densification. The other mechanisms, though, cannot be ignored because they can reduce the neck curvature and thus the driving force and the densification rate.

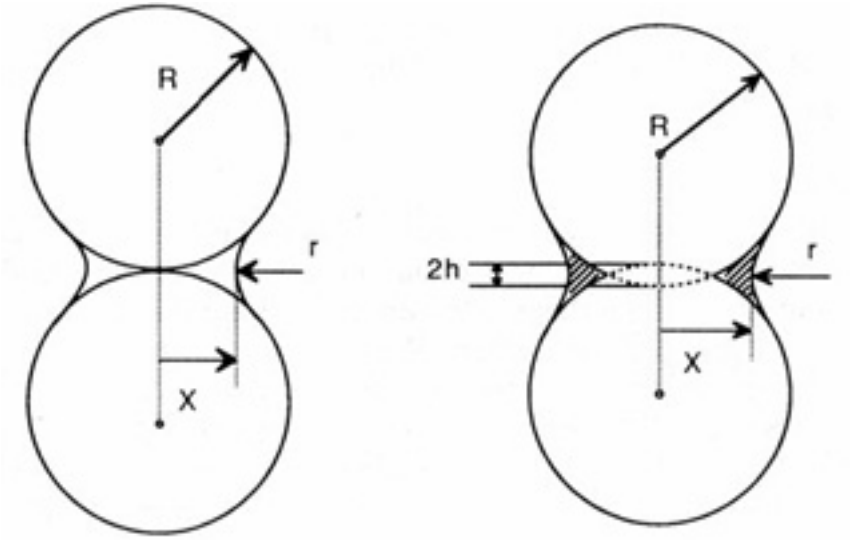
Table 1.2. Sintering mechanisms in polycrystalline and amorphous solids [30,32].

Type of solid	Mechanism	Source of matter	Sink of matter	Densifying
Polycrystalline	Surface diffusion	Surface	Neck	No
	Lattice diffusion	Surface	Neck	No
	Vapor transport	Surface	Neck	No
	Grain boundary diffusion	Grain boundary	Neck	Yes
	Lattice diffusion	Grain boundary	Neck	Yes
	Lattice diffusion	Dislocations	Neck	Yes
Amorphous	Viscous flow	Unspecified	Unspecified	Yes

1.2.2 Theoretical Analysis of Sintering

Several approaches have been used to analyze sintering. These include the scaling laws [33], analytical models, empirical or phenomenological equations, and statistical and numerical techniques. Sintering models are often simplified and idealized representations of the particles in a sintering body. It was necessary to assume an idealized structure of the powder system to facilitate the mathematical analysis of what are clearly complex phenomena. Therein lies the problem with these analytical models because real systems are far from being ideal. In these models, the particles are assumed

to have a spherical shape and the same size and are uniformly packed. A unit of the powder, referred to as the *geometric model*, is then taken to represent the entire system. For the assumed model, the sintering equations are then obtained by formulating the corresponding mass transport equations and solving them using the appropriate boundary conditions.



(a) (b)

Figure 1.20. Two-particle geometric model for the initial stage of sintering [32].

In the analysis of the initial stage of sintering, a model consisting of two equal sized spheres of radius R that are in contact is usually assumed [32,34]. The models for densifying and non-densifying mechanisms are slightly different to reflect the changes that arise from the mechanisms concerned. The geometrical models are shown in Figure 1.20. The equation for neck growth can be expressed in the general form [34 - 37] of

$$\left(\frac{X}{R}\right)^m = \frac{H}{R^n}t \qquad (1.1)$$

where X is the radius of the neck formed between the particles, m and n are constants that depend on the mechanism involved, H is a coefficient characteristic of the mechanism, and t is the time. The equation for neck growth by viscous flow was first derived by Frenkel [38]. Table 1.3 summarizes the coefficients and constants for the various mechanisms.

The geometrical model for intermediate stage sintering of polycrystalline materials is different from that of amorphous systems. The model that is most commonly used was proposed by Coble [39], where he derived equations for lattice and grain

boundary diffusion. The powder compact is assumed to consist of equal-sized particles with the shape of a tetrakaidecahedron, with cylindrical pores along the edges. A tetrakaidecahedron is constructed by trisecting the edges of an octahedron and discarding the six vertices. The resulting structure has 36 edges, 24 corners, and 14 faces with 8 being hexagonal and 6 square. Based on Coble's derivation, the densification rates for lattice and grain boundary diffusion can be approximated as follows:

$$\text{Lattice diffusion: } \frac{\dot{\rho}}{\rho} \approx \frac{AD_l\gamma_{sv}\Omega}{\rho G^3 kT} \tag{1.2}$$

$$\text{Grain boundary diffusion: } \frac{\dot{\rho}}{\rho} \approx \frac{4}{3}\frac{D_{gb}\delta_{gb}\gamma_{sv}\Omega}{G^4 kT(1-\rho)^{1/2}} \tag{1.3}$$

where ρ is the density, $\dot{\rho}$ is the changing rate of densification, A is a constant and G is the grain size. Because of the approximations made by Coble, these equations are no more than order-of-magnitude calculations. Refinements to Coble's model have been made to account for the more complex pore structure [40,41].

Table 1.3. Values for the constants m and n in Equation 1.1.

Mechanism	m	n	H
Surface diffusion	7	4	$56D_s\delta_s\gamma_{sv}\Omega/kT$
Lattice diffusion from surface	4	3	$20D_l\gamma_{sv}\Omega/kT$
Vapor transport	3	2	$3p_0\gamma_{sv}\Omega/(2\pi mkT)^{1/2}kT$
Grain boundary diffusion	6	4	$96D_{gb}\delta_{gb}\gamma_{sv}\Omega/kT$
Lattice diffusion from grain boundary	5	3	$80\pi D_l\gamma_{sv}\Omega/kT$
Viscous flow	2	1	$3\gamma_{sv}/2\eta$

For the densification of amorphous systems, a structure consisting of a cubic array of intersecting cylinders was proposed by Scherer [42]. The equation is rather complex and does not explicitly express the density or densification rate as a function of time. However, it has been shown experimentally to predict well the densification of materials such as colloidal gels, polymeric gels, and consolidated glass particles. Coble [39] used a procedure similar to that used in deriving intermediate stage equations to obtain the final stage sintering equations. From his derivation, the densification rate for lattice diffusion of the final stage can be expressed as

$$\frac{\dot{\rho}}{\rho} \approx \frac{BD_l\gamma_{sv}\Omega}{\rho G^3 kT} \tag{1.4}$$

where B is a constant. Note that this is strikingly similar to the equation for intermediate stage sintering, Equation 1.2, except in the numerical constants. Coble did not derive the equation for grain boundary diffusion but this can be obtained from the models that he developed for diffusional sintering under applied pressure [43,44].

For viscous flow, the work done by Mackenzie and Shuttleworth [45] using a concentric sphere model seems to be appropriate. The densification rate is

$$\dot{\rho} \approx \frac{3}{4}\frac{p}{\eta}(1-\rho) \tag{1.5}$$

where p is $2\gamma/r$, with r being the pore radius. This equation is considered as a reasonable representation of the last stage of sintering when the pores are closed and isolated.

Based on the preceding discussions of the analytical models, it is clear that the sintering phenomenon in polycrystalline solids is much more complex than that in amorphous materials. The sintering of polycrystalline materials is more dependent on the microstructure of the powder system. The result is that simplifications in the models make the corresponding sintering equations mere approximations and tend to be more useful in making qualitative descriptions. However, this does not detract from their usefulness. For example, with the temperature dependence of the process known beforehand, they can be used to determine from experimental data the dominant mechanism through the activation energy values. On the other hand, amorphous materials are less sensitive to microstructure such that idealization of the structure can lead to analytical solutions that can quantify the sintering behavior satisfactorily. It is this simplicity that has led others to extend viscous sintering concepts to the analysis of data from polycrystalline materials. More recently, a combined-stage sintering model was proposed wherein a single equation was derived to represent the sintering process from beginning to end [46].

1.2.3 Driving Forces for Sintering

As mentioned earlier, sintering is accompanied by a lowering of the free energy of the system. The processes and other phenomena that provide the impetus for reducing the free energy are usually referred to as the driving forces for sintering and include the force associated with the curved surfaces of particles, externally applied pressure, and chemical

reaction(s). While the effect of the latter two sources appears straightforward by "pumping" mechanical energy and heat directly into the process, the surface curvature does not add energy to the system but instead works by reducing the total interfacial and surface energies. During sintering, necks forming between particles substitute grain boundary area for surface area, always with a net reduction in total energy.

Excluding externally applied pressure and chemical reactions, the driving forces that cause materials to be transported are the chemical potential gradient and the stress generated at the contacts between particles. In the former, material flows into the neck area under the influence of a chemical potential gradient arising from the differences in curvature of the surface. The chemical potential, μ, of an atom beneath a curved surface is altered by the surface curvature. For a curved surface with principal radii of curvature r_1 and r_2, the potential difference is given by

$$\Delta\mu = \mu - \mu_o = \gamma\Omega\left(\frac{1}{r_1} + \frac{1}{r_2}\right) \tag{1.6}$$

where Ω is the atomic volume and γ is the surface energy of powder particle. The radius is positive when the surface is convex and negative if the surface is concave. The chemical potential gradient also produces a gradient in the vapor pressure above these two surfaces such that

$$\Delta\mu = kT\ln\left(\frac{P_v}{P_o}\right) \tag{1.7}$$

where P_v is the partial vapor pressure over a curved surface, P_o is the partial vapor pressure over a flat surface. Atoms move from the convex to the concave regions to decrease the potential gradient. The vacancies move countercurrent to the diffusion of the atoms and therefore, diffuse away from the contact area between the solid particles and sink at the dislocations or grain boundaries.

Referring to Figure 1.20, the outer edge of the contact is subjected to a stress, σ, given by [47]

$$\sigma = \gamma\left(\frac{1}{r} - \frac{1}{x}\right) \tag{1.8}$$

where γ is the surface tension. Under a concave surface, this stress is tensile and under a convex surface, compressive. Therefore, a stress gradient exists between the particle

interior and the neck, leading to material transport by microscopic viscous or plastic flow during the sintering of the powder compacts. The stress can be related to the densification rate for diffusion-controlled mechanism by the general form that includes an externally applied pressure p_a

$$\frac{\dot{\rho}}{\rho} = -\frac{3}{L}\frac{dL}{dt} = \frac{3}{\eta_\rho}\left(p_a\phi + \sigma\right) \tag{1.9}$$

where *(1/L)dL/dt* is the linear strain rate for sintering, ϕ is the stress intensification factor, and η_ρ has the dimensions of viscosity and is referred to as the densification viscosity. The quantity σ is the thermodynamic driving force with the units of pressure or stress and is referred to either as the sintering pressure or sintering potential. The equation for σ is actually more complex for a polycrystalline ceramic than that given in Equation 1.8 because the pores are in contact with grain boundaries and may be of the form [48]

$$\sigma = \frac{2\gamma_{gb}}{G} + \frac{2\gamma_{sv}}{r} \tag{1.10}$$

where γ_{gb} is the grain boundary energy, γ_{sv} is the surface energy, G is the grain size and r is the pore radius. Equation (1.9) can be rewritten as

$$\frac{\dot{\rho}}{\rho} = \frac{3\phi}{\eta_\rho}\left(p_a + \Sigma\right) \tag{1.11}$$

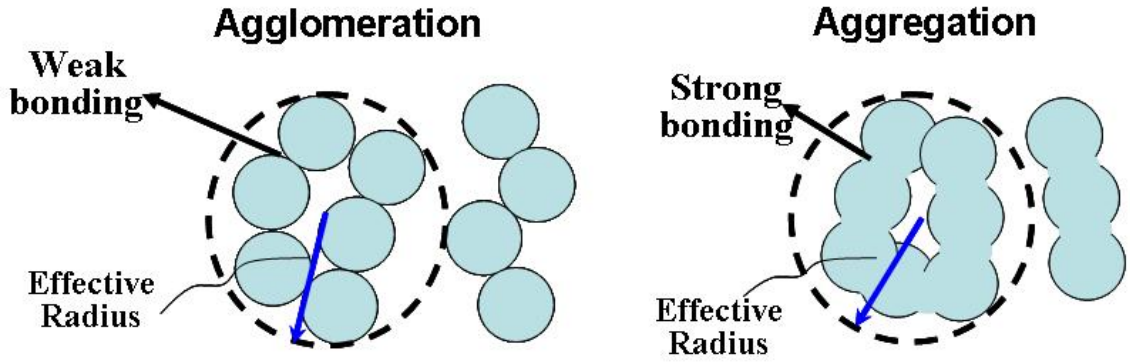
where $\Sigma = \sigma/\phi$ has the units of stress and is referred to as the sintering stress. It occurs in linear combination with the externally applied pressure, p_a, and may be considered as the *equivalent externally applied stress* with the same effect on the sintering as the curved surfaces of the pores and grain boundaries. The definition is useful in analyzing cases where mechanical stresses are present such as in pressure sintering and constrained sintering. It provides a basis for the experimental measurement of the driving force for sintering.

1.2.4 Challenges Associated with Nanomaterial Sintering

Nanomaterial refers to the material with the feature size from 1 to 100 nm. Compared with conventional microscale materials, nanoscale material has significantly larger surface energy. Thus, reducing the silver particle size from the microscale to the nanoscale range can theoretically lower the sintering temperature. However, because of

sintering is a processing which depends on atomic diffusions, the densification rate is not only determined by how easy the atoms can diffuse, but also by how they diffuse.

The first challenge associated with nanoscale material sintering is the agglomeration/aggregation of the nanomaterials. Agglomeration and aggregation are more likely occur in nanomaterials due to their fine particle sizes. Agglomeration is a procedure that the pre-sintering powder compacts are attracted together by weak forces such as Van der Waals/electrostatic forces; while aggregation is a procedure that the pre-sintering material is bonded together by solid necks of significant strength such as metallic force [49]. One of the major differences between agglomerate and aggregate is that the agglomerate can usually be re-dispersed by external energy such as mechanical or ultrasonic forces while the aggregate cannot. Figure 1.21 illustrates the difference between agglomeration and aggregation.



(a) (b)

Figure 1.21. Illustration of agglomeration (a) and aggregation (b) and their effective particle sizes.

Both agglomeration and aggregation result in inhomogeneous distribution of particles and thus the initial (green) density of powder compacts before sintering could be significantly lower due to the loose pack of the agglomerate/aggregate [50]. The lower initial (green) density is detrimental for sinterability. The effective radius instead of the real radius of particle, are usually used to characterize the degenerated sintering capability of agglomerated/aggregated particles. Figure 1.21 shows that the effective radius can be much larger than that of particles. When the effective radius reaches the micron size, the advantages of nanoscale particles are lost. As discussed before, agglomerate can be re-dispersed before sintering but the aggregate cannot. Thus, aggregate should be avoided as much as possible during the preparation of nanomaterials.

Another challenge for nanomaterial sintering is the non-densifying diffusions at low-temperatures. As discussed before, for a polycrystalline material, there are least six different diffusions happen during a sintering procedure. Among the six sintering mechanisms, only volume diffusion of matter from the grain boundaries or from dislocations in the neck region can produce densification. Other diffusion of matter from surfaces cause particle necking and coarsening rather than densify them as illustrated in Figure 1.22.

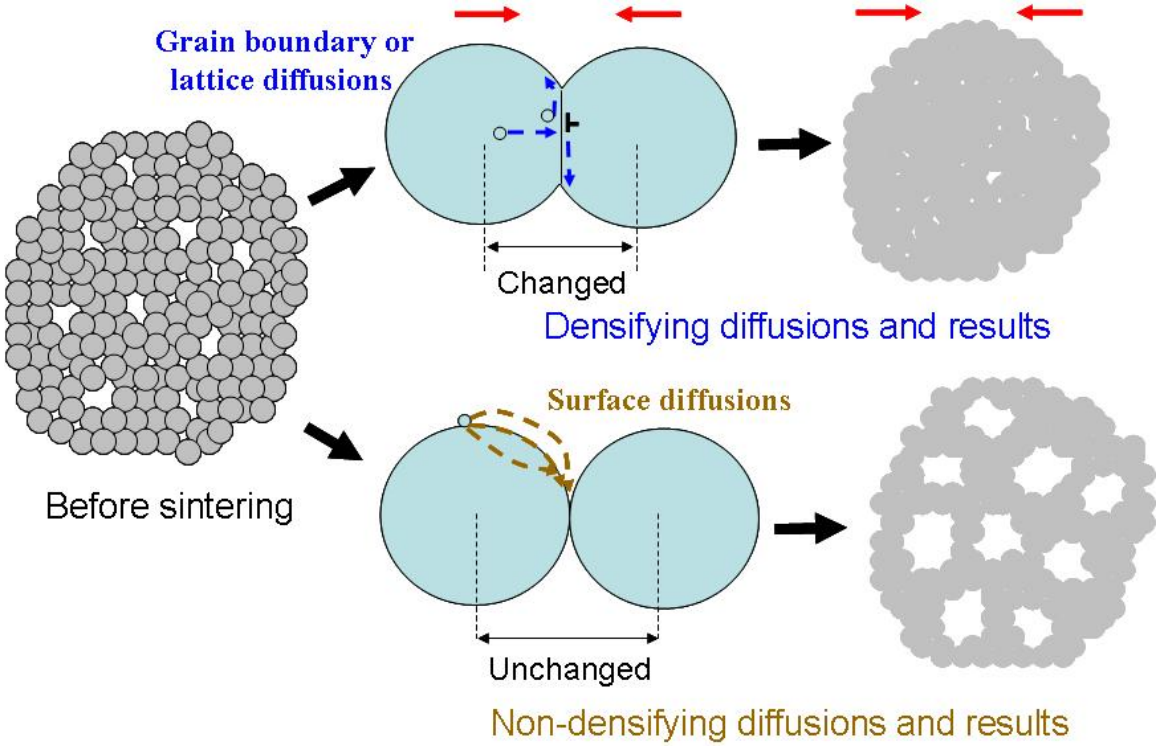


Figure 1.22. Illustration of densifying and non-densifying diffusions and their sintering results.

The non-densifying diffusions and densifying diffusions [51] are dominant at different temperature ranges as shown in Figure 1.23 mainly due to their different active energies. At relatively low temperatures, the sintering process is controlled by surface diffusions and results in neck formation between particles but little actual densification. At higher temperatures, grain boundary/lattice diffusions dominate the sintering process and lead to densification. If a non-densifying diffusion is allowed to proceed, it will consume the driving force that is needed for a densifying diffusion happen, making the sintering material difficult to achieve high density even in a later high-temperature sintering process. Nanomaterials are particularly susceptible to this problem because their

high surface to volume ratio, which results in surface diffusions happen at very low temperatures.

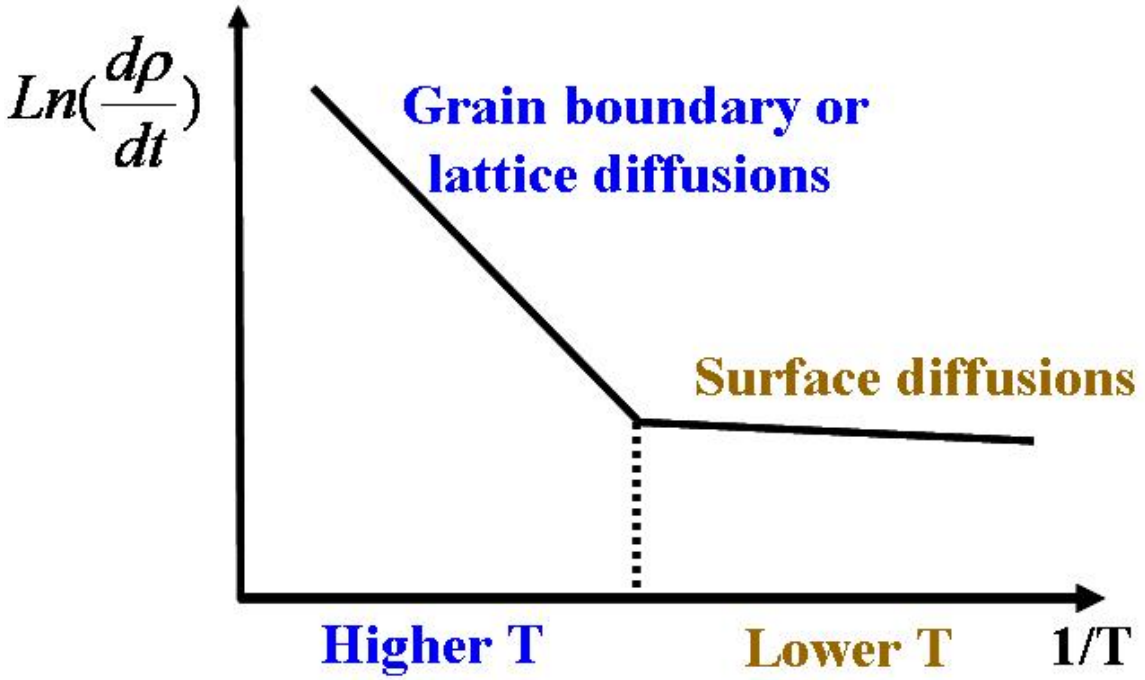
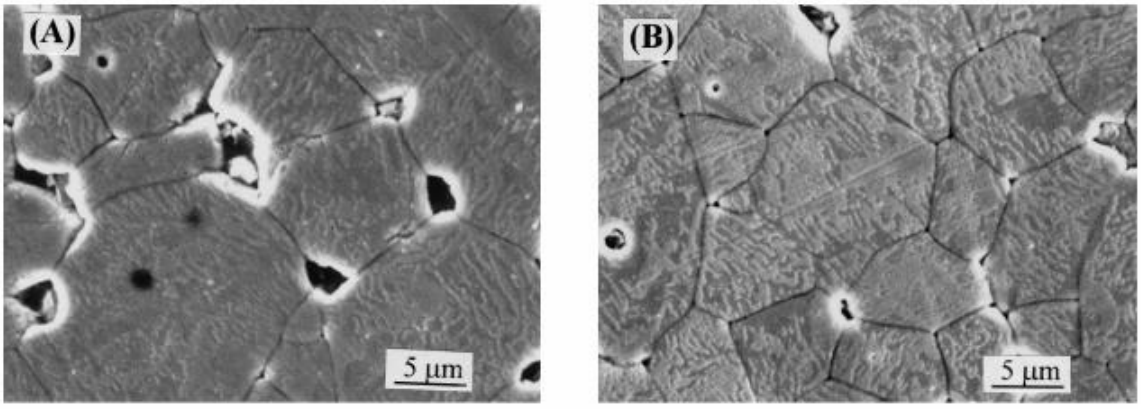


Figure 1.23. Schematic diagram of change in densification rate with temperature. According to rapid rate sintering theory, the two regimes should corresponding to poor or no densification (surface) at low temperatures and much more efficient densification (via grain boundary or lattice diffusion) at high temperature [51].

An approach to reduce non-densification diffusions is to use a fast heating rate to bypass the low-temperature regime quickly. With this approach, the surface diffusion has not sufficient time to occur and the non-densification diffusions are limited. After passing the low-temperature range, the densification diffusions such as grain boundary/lattice diffusions have already dominated and they can densify the powders. Several advanced sintering techniques have been developed to increase the heating rate, such as microwave sintering, plasma activated sintering, laser sintering, field-activated sintering technique (FAST), etc [52 -55]. It is reported that an extremely high heating rate (4900ºC/min) realizing by microwave sintering suppresses grain growth and enhances densification rates by up to 4 orders of magnitude compared to slower conventional heating [56]. Figure 1.24 shows lead zirconate titanate (PZT) sintered at 1150ºC for 2 hours in air: (a) with the heating rate 0.5°C/minute; (b) with the heating rate 100°C/minute [57]. The sintered PZT with faster heating rate has much denser microstructures than the one with a slower heating rate. Another example shows that a faster heating rate by microwave can

sinter nanoscale copper into a higher final density than the conventional furnace sintering [58]. All these evidences show that faster heating rates can enhance the densification and prevent particles coarsening.



(a) (b)

Figure 1.24. The SEM micrographs of PZT sintered at 1150ºC for 2 hours in air: (a) with the heating rates of 0.5ºC/min and (b) 100ºC/min [57].

The enhanced heating rate, however, may induce significant thermal shock, thus it has disadvantages for bonding semiconductor devices because thermal shock is one of the major failure mechanisms in an electronic package. Also, the equipments to realize faster heating rate are much more complicated and expensive than the conventional baking ovens (for conductive adhesives) and reflow furnaces (for solders). Due to these reasons, a fast heating-rate sintering is not practicable for our application and we need look for other strategies to achieve the nanosilver densification.

1.2.5 Summary

The science of sintering has been widely applied in microelectronics for making hybrid circuits, cofired multilayer metal/ceramic interconnecting substrates, multilayer ceramic capacitors, magnetic components, and etc. Recently there have been a few studies [21-24] on the use of sintering powder compacts for attaching semiconductor devices. Since sintering normally requires a temperature that may be substantially higher than the maximum temperature a device can be exposed to, any means of lowing the sintering temperature is desirable and necessary for successful implementation. Pressure-assisted sintering method has been the common approach for attaching semiconductor devices to a substrate at a temperature lower than the pressure-less sintering.

Unfortunately, the approach is difficult to implement in a mass-manufacturing environment. From the above discussion, the driving force of sintering increases with decreasing particle size. It is theoretically achievable to form interconnects by pressure-less sintering of a nanoscale metal powder paste at a low-temperature that is within the maximum post-processing temperature of a device. It is based on this premise this research is developed to formulate the interconnect solutions for power semiconductor devices.

1.3 Motivation of Research

In this section, the motivations of this research are addressed along with the driving force for developing new semiconductor device interconnecting material and technology.

1.3.1 Issues Associated with Current Interconnect Technologies

As discussed before, there are five general aspects that can evaluate a semiconductor device interconnect technology and they are:

(1) Integration capability;

(2) Electrical performance;

(3) Thermal management;

(4) Reliability;

(5) Manufacturability and the cost.

Table 1.4. Pros and cons of various chip-level interconnect technologies.

Interconnect technologies	Integration	Electrical	Thermal	Reliability	Manufacturability
Wirebond	Poor	Poor	Poor	Good	Good
Metal deposition	Good	Good	Good	Poor	Fair
Solder reflow	Good	Fair	Fair	Fair	Good
Conductive epoxy curing	Good	Bad	Bad	Good	Good
Press pack	Fair	Good	Good	Fair	Poor
Pressure-assisted silver sintering	Fair	Good	Good	Good	Poor

The current chip-level interconnect technologies can be assigned into three general evaluation levels of “Good”, “Fair” or “Poor” on each of the above aspects as listed in Table 1.4. In the follows, we will discuss the major issues associated with each

of the current available interconnect technology. Along the discussion, the necessity for developing new interconnect technologies will be addressed.

A. Wirebond

Although wirebond has been a mature and dominant interconnect technology and it is still going through a continuous improvement from all the aspects, there are a few bottlenecks that prevent it from the choice for next generation highly integrated power packages and modules. The concerns include:

- Its poor integration capability. Because wirebond is basically a 2-D packaging technology and it is not adaptable to the imminent 3-D integrated packaging for power devices and modules. The distributions of long and thin bonding wires cause the package with high profile and low silicon-to-footprint ratio.
- Its poor electrical performance. The long and thin bonding wires cause big packaging loop inductance, and thus slow down switching speeds, lower efficiency and higher voltage overshoots [59,60]. The high overshoots bring extra voltage pressures to the power devices. Also, mutual coupling effects between adjacent wirebonds can lead to the change of impedance of different bonding wires and thus result in the uneven current loading and large electromagnetic interference (EMI) noise.
- Its poor thermal management. The long thin wires themselves cannot take out much heat due to their big thermal resistance. To make the situation even worse, the bonding wires prevent attaching any heat removal components from the top of the devices. The current crowding at each wire-to-chip joints and the uneven current distribution cause hot spots.

B. Metal deposition

Metal deposition is good for building up 3-D high density structures. Also the high electrical and thermal conductivities of deposited thin metal films make it ideal for current handling and thermal removal capability. However, the major concerns associated with the metal deposition are:

- Its poor interconnect reliability. Because both semiconductor devices and the deposited metal (usually copper) are hard materials and they usually have

large CTE mismatches. When two CTE mismatched materials are bonded together and encounter temperature changes, thermomechanical stresses are induced at the bonding interfaces. As an example, Figure 1.25 shows the finite elemental analysis (FEA) results of large thermal stresses induced at the direct metal bonds in the embedded power structures [61] when the power MOSFET device working at around 94°C. The large stresses imposed on the silicon die may cause it to crack.

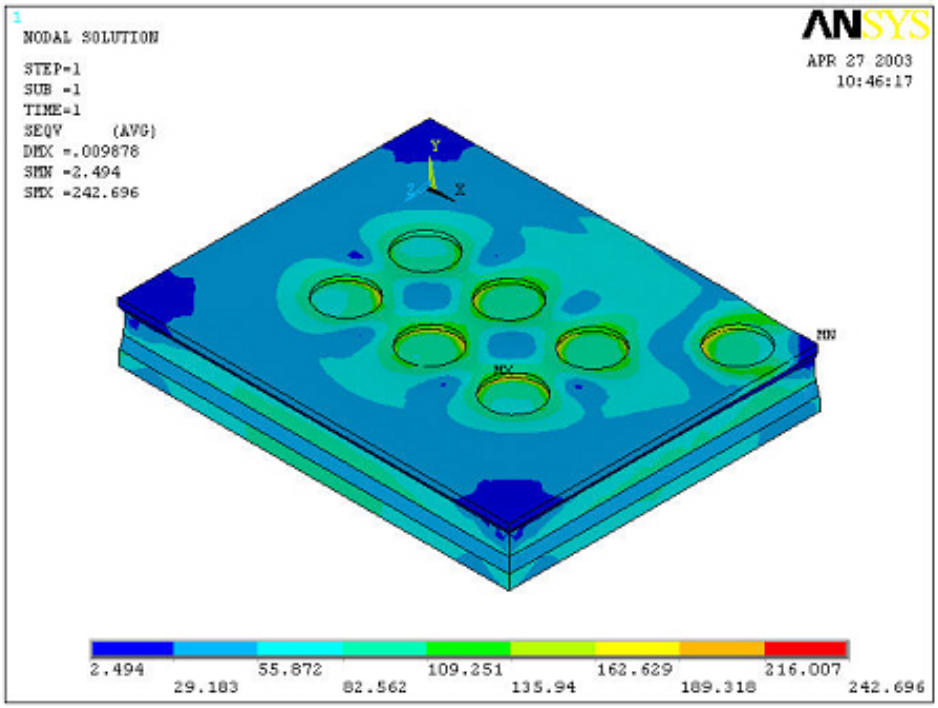


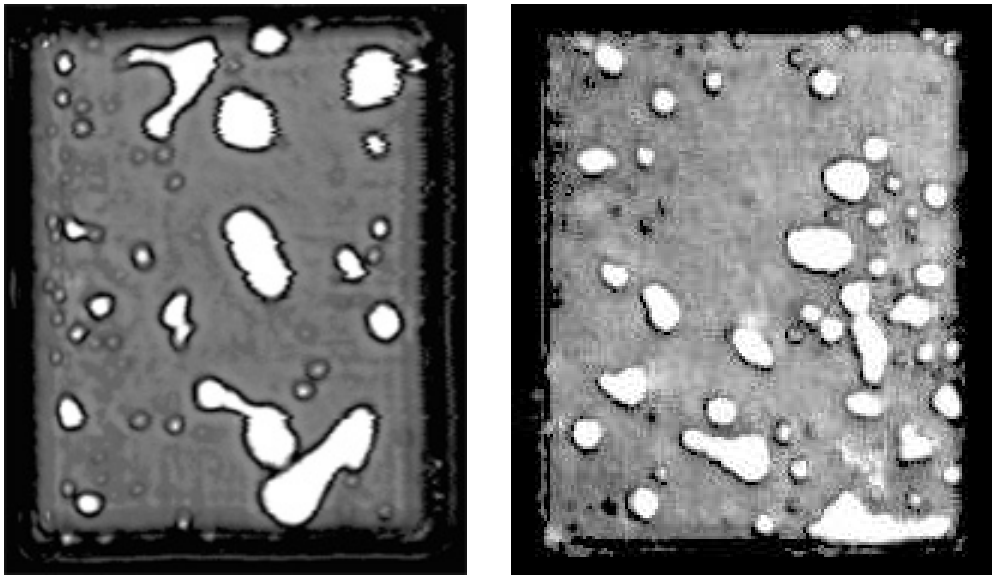
Figure 1.25. Thermal stress distribution in the local position when the MOSFET operating at 94°C in an embedded power module [61].

- Its fair processing simplicity. Because the metal deposition usually involves in vacuum sputtering or e-beaming. The high vacuum deposition is relatively time-consuming and expensive.

C. Solder reflow

Solder reflow is also good for building up 3-D high density structures. But the electrical and thermal conductivities of typical solder are not as good as pure metals. Though one can use low-profiled solder bump or even direct solder layers to reduce the electrical and thermal resistance of the solder joints, there are still several concerns associated with solder reflow:

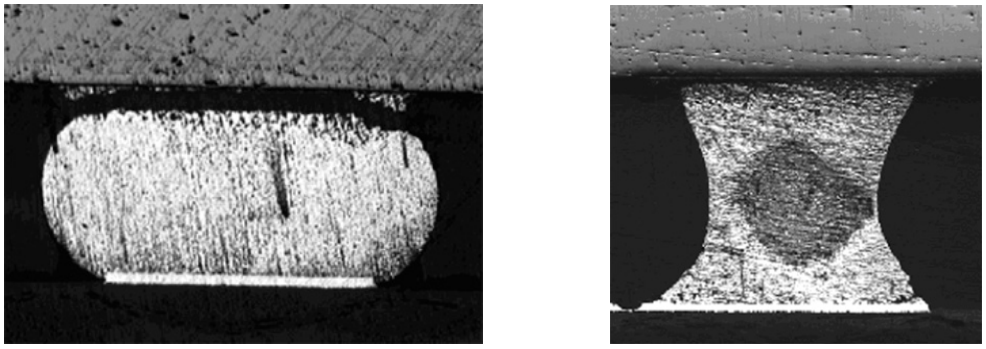
- Its fair thermal management. Partially due to the relatively low thermal conductivity of solder and partially due to the initial void problems as an example shown in Figure 1.26. The initial voids are formed due to flux evaporation during solder reflow. Use fluxless and vacuum solder reflow can mitigate the initial void problem. Moreover, the solder/copper substrate interfaces usually have a considerable large interfacial thermal resistance associated [62], which is in turn added up to the total thermal resistance.



(a) (b)

Figure 1.26. The initial void problems in the reflowed die-attaching solder layers in (a) lead-tin solder and (b) lead-free solder.

- Its fair reliability. Because solders are usually binary or trinary alloy systems. These alloy systems are not stable thermodynamically. During temperature changes, the solder alloys turn to have crack initiation and growth problems which can cause joint failure eventually. The crack initiation and growth are associated with phase separation because dislocations in the solder materials may pinch out and accumulate at the phase boundaries. Examples of the failure of solder joints are shown in Figure 1.27 after thermal cycling [63].



(a) (b)

Figure 1.27. The solder bump failure after thermal cycling. (a) Barrel-shaped solder joints and (b) hourglass-shaped solder joints [63].

Furthermore, solder reflow also causes contamination problems if lead (Pb) - contained solder is used.

D. Conductive epoxy curing

Conductive epoxy curing is a relatively new packaging technology although it has been successfully applied in some power packages like IR's CopperStrap and DirectFET. The technology has no problem for 3-D high density integration and is also excellent for enhanced reliability since it is a very soft material. However, conductive epoxy curing is usually only good for low-power packages because:

- Its poor electrical performance. Though making improvement, the electrical conductivity of curable epoxy is still much lower than pure metals and solder. The high electrical resistance limits its current handling capability. In the structure design, large-area and thin-layer joints are usually used to mitigate the disadvantages.
- Its poor thermal management. The argument is similar to the electrical performance mainly due to its much lower thermal conductivity than pure metals and solder.

Also, the curable conductive epoxy cannot work at high-temperature because of the organic polymer composition.

E. Press Pack

Press pack has excellent electrical performance and thermal management. But the interconnect technology have concerns as follows:

- Its fair integration capability. The mechanical fixture for the pressure contacts is typically not easy to be adapted for 3-D high-density packaging.
- Its fair reliability. Similar with the metal deposition, press pack brings two CTE mismatched materials—semiconductor and metal—together directly and thus the interconnections have thermomechanical stress concerns. Therefore, molybdenum is usually used for better CTE match.
- Its poor manufacturability. The use of mechanical fixture for the pressure generation makes the structure pretty expensive. The interconnect technology is only used in extremely high power (hundreds of kilowatt) when the cost per package is a less concern.

F. Pressure-assisted silver sintering

Similar to the press pack, the pressure assisted silver sintering has excellent electrical performance and thermal management because of the very high conductivities of the sintered silver. The reliability of the sintered silver is also very good. However, the interconnect technology have concerns as follows:

- Its fair integration capability. Use a similar argument with the press pack. The external pressure applied during the processing makes it is almost impossible to build up the sintered silver interconnections from the both sides of the power devices.
- Its poor manufacturability. Use the same argument with the press pack. Actually this is one of the reasons why SemiKron [26] did not use the technology for mass production although it has been demonstrated the electrical, thermal and mechanical performances of the sintered silver joints are much better than the conventional solder joints.

1.3.2 Advantages of Low-Temperature Nanoscale Silver Sintering

This dissertation presents a new interconnect material—nanoscale silver paste—and its subsequent low-temperature sintering process to provide high-quality power device joints at a relatively low cost level. Because of the reduction of silver particle size and the proper selection of the organic vehicle for the paste system, external pressure is

not necessary anymore to sinter the silver paste at low temperatures. The absence of external pressure during processing not only makes the 3-D high-density integration possible, but also greatly reduces the fabrication complexity and thus the cost. The nanoscale silver pastes can be either screen/stencil-printed or syringe-dispensed and they can be served as a direct drop-in substitution to the commercially available solders. They can be sintered to a density of over 80% after sintered at 280^{o}C, a temperature closes to the maximum processing temperature in today's lead-free soldering process. The electrical and thermal conductivities of the low-temperature sintered silver are ~3-5 times higher than those of the best solder or conductive epoxy. The silver joints formed by the low-temperature sintering technology have a bonding strength about 40 MPa on the silver-coated substrates, similar to the eutectic solder joint strength. Due to the solidus interdiffusion of bonding mechanism, initial voids are avoided from the silver joints and they are more uniform than solder joints and therefore they have better thermal management. Also, the porous microstructure gives the sintered material a low modulus of ~10 GPa, making it mechanically compliant for relieving thermomechanical stresses in the attachment. Finally, once the attachment is formed at low temperatures, the maximum use temperature of the package is limited by the device and substrate, not by the die-attach material. Thus, the low-temperature sintering technology can be used to interconnect wide-bandgap semiconductor devices, such as SiC devices for switching power supplies or GaN light-emitting devices, to enable them to function at temperatures over 300^{o}C.

In the following, the detailed advantages of the low-temperature silver sintering technology are listed and discussed, and thus lead to our research motivation.

A. Integration capability

Because of the elimination of external pressure during the low-temperature sintering of nanoscale silver paste, the interconnect technology can be easily adapted to build 3-D high-density power packages like processing conventional solder paste. Compared with solder reflow, the low-temperature sintering has extra advantages for simpler processing. Unlike solder reflow, the nanoscale silver paste is sintered at temperatures far below the melting point of bulk silver. The sintered silver film or joint can retain their shapes at the sintering temperatures. Therefore, it is very convenient to

process the low-temperature sintering as many times as desired to complete a 3-D high-density power package. Otherwise several solders with different melting points have to be carefully chosen in the construction of a solder-reflowed package.

B. Electrical performance

The electrical conductivity of the low-temperature sintered silver is about 3-5 times of those of the best solders and also much higher than that of the conductive epoxies. Therefore it has great current handling capability and excellent electrical performance.

C. Thermal management

The thermal conductivity of the low-temperature sintered silver is also about 3-5 times of those of the best solders and also much higher than that of the conductive epoxies. Furthermore, the uniformity of silver joint eliminates the possible hot spots of the power device. Therefore low-temperature silver sintering has superior thermal management capability.

D. Reliability

The low-temperature sintered silver has around 20% porosity with microscale porous trapped in. The porous microstructure gives the sintered material a low effective modulus at about 10 GPa. The value is even lower than that of the soft solder such as eutectic lead-tin at the room temperature. For a power device-metallized substrate interconnection, a softer interconnecting material can be advantageous since it transfers less of thermal stress due to the semiconductor-metal CTE mismatch. Using this argument, the low-temperature sintered silver has superior thermomechanical properties and it will help achieve a more reliable interconnection. Furthermore, since the interconnect material is pure silver, a single phase material with a much higher melting point than solders, its reliability is high because the phase separation and creep failure are avoided or greatly reduced.

E. Manufacturability and cost

Because of the elimination of external pressure during the low-temperature silver sintering, the technology can be easily adapted to the process of conventional solder paste and epoxy. We have carefully designed our low-temperature silver interconnect

technology so that it can serve as a direct-drop in substitution of solder paste reflow. Compared with pressure-assisted silver sintering, the complexity and thus the cost of processing have been greatly reduced, which permit use the interconnect material at a relative low cost level. Considering of the greatly improved performance and prolonged usage life, the interconnect technology is potentially very cost effective.

1.4 Objectives and Significance of Study

In this study, we developed a lead-free semiconductor device interconnect technology by studying the processing-microstructure-property relationships of low-temperature sintering of nanoscale silver pastes. The specific objectives of this research are listed as follows.

1. **To understand the dispersion mechanisms of the nano-silver particles and the functions of the selected organic components for the preparation of uniformly-dispersed, screen/stencil printable, and low-temperature sinterable nanoscale silver pastes.** Under this objective, we purposely designed our pastes to be compatible with the current surface mount technologies such as syringe-dispensing and screen/stencil-printing. To achieve the objectives, we carefully selected dispersant, binder and thinner organic components so as to disperse and stabilize the nanosilver particles, adjust the paste viscosity, and retard the non-densifying diffusions at low-temperatures.
2. **To analyze the physical mechanisms involving organic burnout, densification and grain-growth for the nanoscale silver pastes.** Under this objective, we studied the binder burnout and paste densification kinetics for achieving low-temperature sintering. The final properties of the sintered paste were dictated by the low-temperature firing process, which typically consists of organic burnout/removal and power compact densification. We found that it was essential to completely remove all the organic components in the paste before the on set of densification to ensure the desired final microstructure and properties, since any residual organic components will affect the mass transport in the particular porous structure.

3. **To characterize the low-temperature sintered silver as a new interconnect material.** Under this objective, we measured the important properties of the low-temperature sintered silver at the material level for the semiconductor device bonding applications. The properties such as density, electrical resistivity, thermal conductivity, modulus and CTE of the sintered silver were determined.
4. **To resolve binder burnout and the compatibility issues associated with the interaction between interconnecting metal substrates and device metallization for achieving strong and reliable joints.** Under this objective, we studied binder burnout problems associated with covered sintering and the effects of surface treatment on the silver joint preparation. We used electroless or electroplating methods to coat nickel/silver or nickel/gold to prevent oxidation and form the silver joints. Also, we carefully designed sintering profiles to achieve strong silver bondings.
5. **To evaluate low-temperature sintered silver joints.** Under this objective, we evaluated the important properties of the low-temperature sintered silver joints for the semiconductor device bonding applications. We mainly used the die-shear test, SAM, and SEM to determine the bonding strength and uniformity of the sintered silver joints. The effects of the silver loadings, joint sizes, and firing temperature and time were studied.
6. **To study the reliability of sintered silver joints.** Under this objective, we studied reliability and failure mechanism of the sintered silver joints. Thermal cycling experiment was explored to evaluate the reliability of the sintered silver joints. During the thermal cycling, the die-shear test, SAM, and SEM were used to identify the failure mechanisms of the sintered silver joints.

In summary, we developed the scientific knowledge and engineering known-how for the interconnection of power semiconductor devices by investigating the processing-microstructure-property relationships of low-temperature sintering of nanoscale silver pastes. The goal of the study is to address the fundamental issues associated with this process development. The completion of the study provided solutions that can fill the gap in the development of the advanced semiconductor devices and packaging technologies

in power electronics and it can significantly impact the future growth of the trillion-dollar electronics industry.

1.5 Organization of Dissertation

The dissertation is organized into five chapters according to the following scheme.

The current chapter (Chapter 1) provides a background review of the research topics such as current power chip interconnect technologies and sintering mechanisms and a statement of the motivation and objectives of the research.

Chapter 2 covers all the detailed experimental procedures involved in this research. It starts from formulation of the nanoscale silver paste. After preparation of the interconnect material, study of low-temperature sintering shows that the nanoscale silver paste can be sintered at low-temperatures of 280-300°C. Then at this stage, the electrical and thermal conductivities, effective elastic modulus, yield and tensile strengths, and CTE of the low-temperature sintered silver are determined. Then Ni/Ag metallized devices are attached onto either Ni/Ag or Ni/Au coated DBC substrates to form the silver joints. Then the low-temperature silver joints are evaluated by die-shear, SAM and SEM. Finally the silver joints are undergone temperature cycling experiment to study their failure mechanisms.

Chapter 3 addresses experimental results and discussions. First we present the measuring results of the sintered silver at the materials level, then the characterization results at the silver joint level, and finally is the reliability results and failure mechanism discussion of the sintered silver joints.

Chapter 4 talks about the potential applications of the low-temperature sintered silver joints in power electronics, both in single-chip packages and multi-chip modules. And then the discussion is extended to the other potential applications in high power photonic devices such as power lasers and light-emitting diodes (LEDs).

Chapter 5 is the summary, conclusion and recommendation for future work.

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Chapter 2
Experimental Procedure

The experimental work of this research starts from the formulation of the nanoscale silver paste as a new power chip interconnecting material. After preparation of the interconnect material, study of low-temperature sintering finds that the silver paste can be sintered to around 80 wt.% bulk density at temperatures as low as 280°C. At this stage, some of the important properties like the electrical and thermal conductivities, effective elastic modulus, yield and tensile strengths, and the CTE of the low-temperature sintered silver were determined. Then Ni/Ag metallized semiconductor devices were die-attached onto either Ni/Ag or Ni/Au-coated substrates to form the strong bonding of silver joints. After the silver joint preparation, the silver joints were evaluated using die-shear test, SAM and SEM. Finally, the sintered silver joints were undergone thermal cycling experiment to evaluate their reliability and to identify the failure mechanisms.

2.1 Formulation of Nanoscale Silver Pastes

Many techniques such as mechanical attrition, vapor deposition, chemical precipitation have been developed to synthesize large quantities of nanoscale metal particles like Ag, Au, Cu, Fe, Ni, Cr, Mo, Pd, Ti, and Pt and their alloys. In this study, we chose either chemically precipitated (self-prepared) or vapor deposited (commercially available) nano-particles because the two methods generally provide better control over particle size and its distribution, agglomeration/aggregation, contamination and oxidation, and particle surface modification. Among the metal particles, we chose silver because of its several potential advantages for the applications such as its superb electrical and thermal conductivities, superb resistance to oxidation and corrosion, high melting point for creep failure resistance, and relatively low cost. Besides the nanoscale metal selection, the organic dispersant/binder/thinner selection is also critical for the

preparation of a uniformly dispersed metal paste and its subsequent low-temperature sintering steps. The selection of the organic dispersant/binder/thinner usually means the considerations of the trade-off between their burnout temperatures and their functionalities for the paste formulation.

2.1.1 Preparation of Nanoscale Silver Particles

Initially, the modified Carey Lea method [1,2] was chosen to prepare nanoscale silver particles. In the technology, a reducing agent was prepared by mixing 35-ml 40% sodium citrate ($Na_3Citrate•2H_2O$, Sigma Aldrich, Milwaukee, WI) and 25-ml 30% as-prepared ferrous sulfate ($FeSO_4•7H_2O$, Alfa Aesar, Ward Hill, MA). The mixture was then added slowly to a solution of 25-ml 10% silver nitrate ($AgNO_3$, Alfa Aesar, Ward Hill, MA) under vigorous stirring to form a blue-black precipitate which was recovered by centrifuging the solution. The suspension was then isolated by centrifugation to recover precipitation. The precipitation was dispersed in 50-ml water and flocculated using 50-ml 40% sodium citrate solution for three times. Finally the precipitation was dispersed in water. After water evaporation, the dried silver particles were obtained. The procedure was scaled-up and repeated to produce sufficient nanoscale silver particles for the low-temperature sintering tests.

Alternatively, nanoscale silver powder or slurry is available commercially from various suppliers in various sizes at a cost of roughly $1-2 per gram. Below is a list of some companies and their websites known to supply the nanoscale silver:

(1) Nanostructured & Amorphous Materials, Inc.:
http://www.nanoamor.com

(2) Ferro, Inc.:
http://www.ferro.com

(3) Inframat® Advanced Materials™ LLC:
http://www.advancedmaterials.us/47MN-0001.htm

(4) Sumitomo Electric U.S.A., Inc.:
http://www.sumitomoelectricusa.com

(5) Kemco International Associates:
http://www.kemcointernational.com/index.html

Generally speaking, commercially available nano-silvers are more time and cost effective than the self-prepared samples. However, the commercial nano-silvers are mainly targeted for either biomedical applications or personal hygiene applications. Many of them are already coated with less than 1 wt.% dispersant to prevent the particle from agglomeration/aggregation. Thus, the original dispersant in the silver powder/slurry needs to be carefully examined before the nano-silver can be used for our low-temperature sintering applications. Otherwise their original dispersant may not be suitable for our specific applications as discussed below.

2.1.2 Selection of Organic Dispersant, Binder, and Thinner

To formulate a nanoscale silver paste that suitable for screen/stencil-printing or syringe-dispensing like the solder paste or microscale silver paste, organic components such as dispersant (or called surfactant), binder and thinner need to be added into the nanoscale silver particles. The functions of the dispersant, binder, and thinner components in the paste are associated with particle dispersion/polymeric stabilization, paste printability and flowability, respectively, as illustrated in Figure 2.1.

First, the dispersant component usually has a polar acid function in one end and a hydrocarbon chain in the other. During dispersion, the polar acid can anchor chemically onto the hydrated silver particle surface and the left hydrocarbon chain can surround the metal particles and thus prevent them from agglomeration by a polymeric stabilization mechanism [3]. The possible candidates for dispersant include fatty acid, fish oil (a natural combination of fatty acids), poly(diallyldimethylammonium chloride) (PDDA), poly(acrylic acid) (PAA), and polystyrene sulfonate (PSS). The menhaden fish oil (Sigma-Aldrich Co., Milwaukee, WI) with a polar acid function of -COOH and was chosen for this application and the dispersant can adhere to silver nano-particles through hydrogen bonds as illustrated in Figure 2.1.

Secondly, the binder usually composites of polymer with long hydrocarbon chains so that it can hold up the dispersed silver particles to prevent cracks during processing of the paste and subsequent heat treatment. The possible choices for the binder include RV 914 binder, polyvinyl alcohol (PVA), polyvinyl butyral (PVB), and wax. The RV 914 binder (Heraeus Inc., Chandler, AZ) was chosen to formulate the nanoscale silver pastes.

Finally, the thinner usually composites of polymer with short hydrocarbon chains so as to adjust the viscosity of the nanoscale silver paste. The possible thinner can be Heraeus HVS 100, Heraeus RV 372, Heraeus RV 507, Heraeus RV 912, Texanol, and Terpineol. The RV 912 thinner (Heraeus Inc., Chandler, AZ) was chosen for this application.

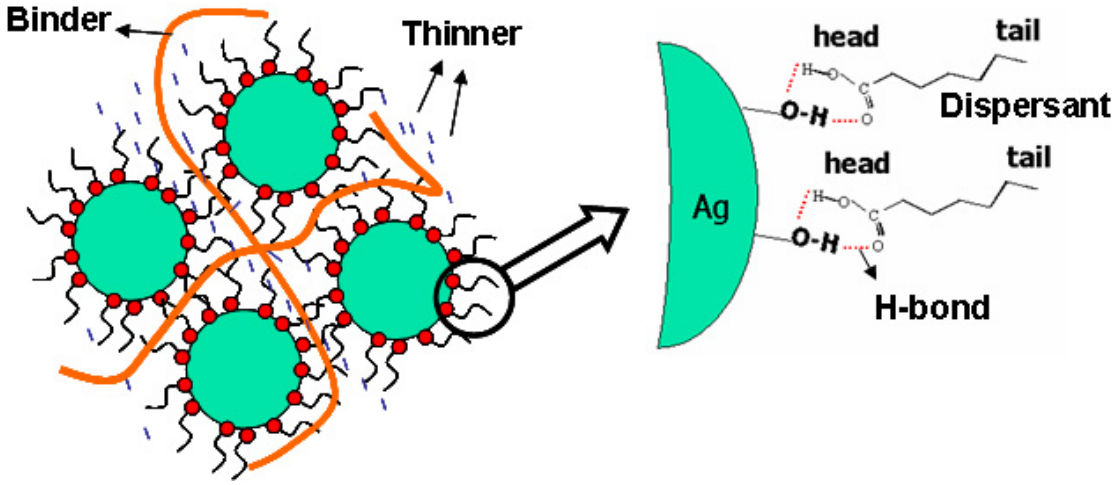
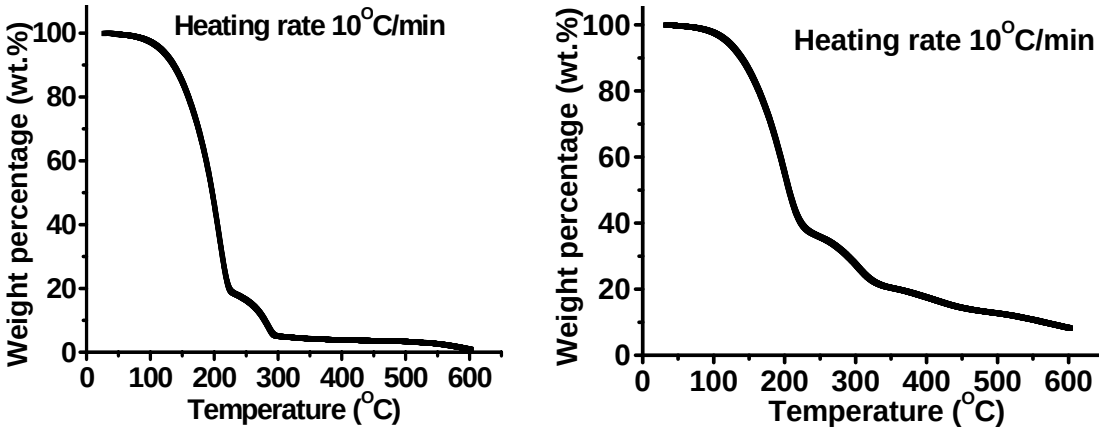


Figure 2.1. Functions of the dispersant, binder and thinner in the formulation of nanoscale silver pastes.

During the paste formulation, an important consideration was the selection of the organic components such that the organic burnout temperature ranges allow sintering to take place at low-temperatures. Generally speaking, the selected dispersant, binder, and thinner must be able to burn out below the targeted sintering temperature, since it is found that the burnout of the added organic components is a prerequisite for the low-temperature sintering. As an example, the thermogravimetric analysis (TGA) curves of the selected Heraeus RV 912 thinner and Heraeus RV 914 binder are shown in Figure 2.2. One can see that almost all the thinner and binder component can evaporate/burn out at temperatures lower than 300°C. This means that the selected materials can be used for the formulation of nanoscale silver paste that can be sintered at around 300°C. Also, since the RV 914 binder is relatively more difficult to burn out compared with the RV 912 thinner, one may want to use less binder in the paste formulation as long as the desired paste quality was reached.



(a) (b)

Figure 2.2. Thermogravimetric analysis (TGA) curves of the thinner (a) and binder (b) selected for the silver paste formulation. Heat treatment condition is 10°C/min in air. Note the quick weight percentage drops at temperatures below 300°C.

Another example is on how to select the fatty acid dispersant. From Figure 2.3, one can see that boiling points of the fatty acids increase with the number of carbon atoms in the molecular of the dispersant. Since the boiling points of the fatty acids are roughly the same with their burnout temperatures, fatty acids with a certain number of carbon atoms or lower have to be selected to formulate a nanoscale silver paste that can be sintered at a certain temperature. For example, if one wants to formulate a paste that can be sintered at around 280°C, the fatty acids with carbon atoms around 11 should be selected, otherwise the fatty acids cannot be burned out and the paste cannot be sintered at the temperature.

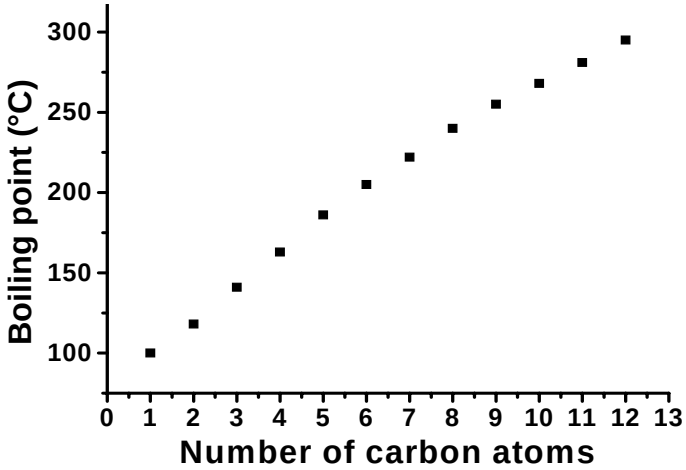


Figure 2.3. The relationship of the boiling point of fatty acid versus their number of carbon atoms (Adapted from the Sigma-Aldrich websites).

During the selection of the dispersant and thinner and binder, the second important effect needs to be considered is the functionalities of the organic components in the formation of the paste. Again take the selection of fatty acids as an example. It was found that the fatty acids with relatively longer hydrocarbon chain can disperse the nanoscale silver particles better than those with relatively shorter hydrocarbon chain. Better dispersion usually means better paste quality. From this point of view, the fatty acids with relatively longer hydrocarbon chain, i.e., more carbon atoms have advantages. Finally, after consider the trade-off between the burnout temperatures and disperse effects, one may want to select the fatty acids that could be burned out just below the targeted sintering temperatures.

2.1.3 Preparation of Nanoscale Silver Pastes

During the nanoscale silver paste formulation, an organic solvent (acetone or alcohol) was used to serve as a dispersing vehicle and later on the solvent needs to be evaporated out. The organic components (dispersant, binder and thinner) were firstly added into the organic solvent to get a uniform colloidal solution. Then the nanosilver particles in either a powder or slurry form was slowly added into the colloidal solution while mechanical stirring and ultrasonic vibration. Both mechanical stirring and ultrasonic vibration were continued for another 3 hours to make sure that the silver particles were thoroughly and uniformly dispersed. Icy cooling was needed to keep a low-temperature environment during the dispersion. Finally the nanoscale silver paste was obtained by vacuum evaporation to remove the organic solvent. A detailed preparation procedure is shown in Figure 2.4.

The total silver loading and the degree of dispersion of the silver particles were two of the important factors to obtain a uniform paste with proper viscosity that suitable for screen/stencil-printing or syringe-dispensing. We adjusted organic components to approximate the printing characteristics of commercial silver paste. Nanoscale silver pastes with 78, 81, 84, 87 and 90 wt.% silver loadings were prepared. The percentages were obtained from the initial weighting of the nanoscale silver particles and their initial impurities and added surfactant, binder and thinner components. However, as shown in Figure 2.5, the volume loading of the silver pastes is quite different from the weight

loading considering the difference in the densities of silver and organics. As a result, the green density of the nanoscale silver pastes is ranged from 35~45% of bulk silver. The higher silver-loadings are usually corresponding to the higher green density. However, the green density depended on not only the composition of silver and organics, but also the degree of dispersion. Given the same silver and organic composition, the better dispersed pastes have higher green density.

The prepared nanoscale silver pastes were stored in covered containers in a refrigerator at about 5°C as the usual solder pastes and microscale silver pastes to prevent thinner evaporation.

Figure 2.4. Preparation procedure of nanoscale silver pastes.

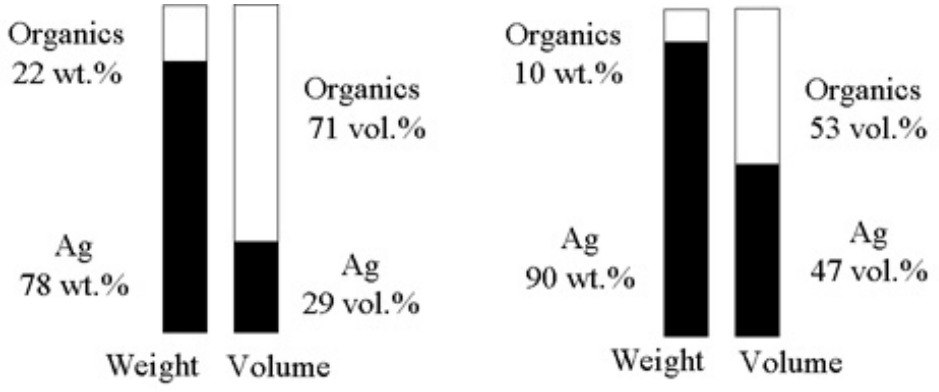


Figure 2.5. The weight and volume percentages of the 78 wt.% silver paste (a) and those of the 90 wt.% silver paste (b).

2.2 Low-Temperature Sintering of Nanoscale Silver Pastes

During the low-temperature sintering, it is found that the organic components have to be burned out before the nanoscale silver could be sintered. It is also found that the oxygen in the air is helpful for the organic burnout. In the case of open-air sintering, the paste is relatively easier to get sintered. A temperature profile shown in Figure 2.6 is usually used for the low-temperature sintering. The 20-min temperature ramp and the 10-min dwell at 280°C are designed to provide sufficient time for the volatilization and burnout of the organic components in the paste.

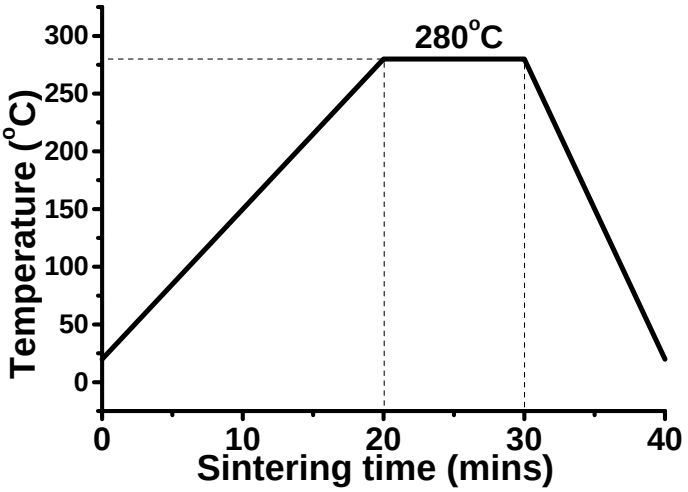


Figure 2.6. Typical temperature profile for sintering nanoscale silver pastes.

However, in the covered sintering case, the organic components are not easy to burn out and the oxygen is not easy to get in either. Therefore, the paste is much harder to get sintered. The difficulty of the covered sintering was found to associate with the organic loadings in the sintering silver paste and the covering size. Several strategies were developed to study the covered sintering such as the use of the higher silver-loading pastes, the introduction of oxygen-rich environment, and the design of increased sintering temperatures and prolonged sintering profiles.

Both X-ray photoelectron spectroscopy (XPS) and energy dispersive spectroscopy (EDS) were used to determine the element compositions after the low-temperature sintering.

2.3 Characterization of Sintered Silver

The low-temperature sintered silver was characterized electrically, thermally, and mechanically to determine the important properties for the high-power packaging applications. The properties that were determined include the electrical and thermal conductivities, elastic modulus, yield and tensile strength and coefficient of thermal expansion (CTE) [4]. Whenever possible, the properties were determined at both room temperature and elevated temperatures.

2.3.1 Determination of Electrical Resistivity

The screen as shown in Figure 2.7 was used to print resistor patterns on an alumina substrate. The resistance of the low-temperature sintered silver was measured from room temperature up to 650°C. During the measurement, the two resistor pattern tips were clamped together using the nickel/gold-plated copper electrodes as shown in Figure 2.8. The entire assembly as illustrated in Figure 2.9 was placed into a furnace for heating up. The resistor patterns are long and thin as shown in Figure 2.7 and their resistance values are around several ohms so that the contact resistance of electrodes (typically in mΩ) can be ignored during the measurement. The cross-sectional area S of the resistor patterns was determined by a DekTak3 profilometer. Cross-sectional areas at 5 randomly-selected locations were measured and averaged to improve accuracy. With the designed length l of the resistor patterns known, the electrical resistivity of the sintered silver was determined by

$$\rho_e = R\frac{S}{l} \tag{2.1}$$

A commercial microscale silver paste with silver particle size of 1-3 micron (C-1075, Heraeus Inc., Chandler, AZ) was also screen-printed onto alumina substrates and heated using the same profile in Figure 2.6 and then put into furnace for the electrical resistivity comparison.

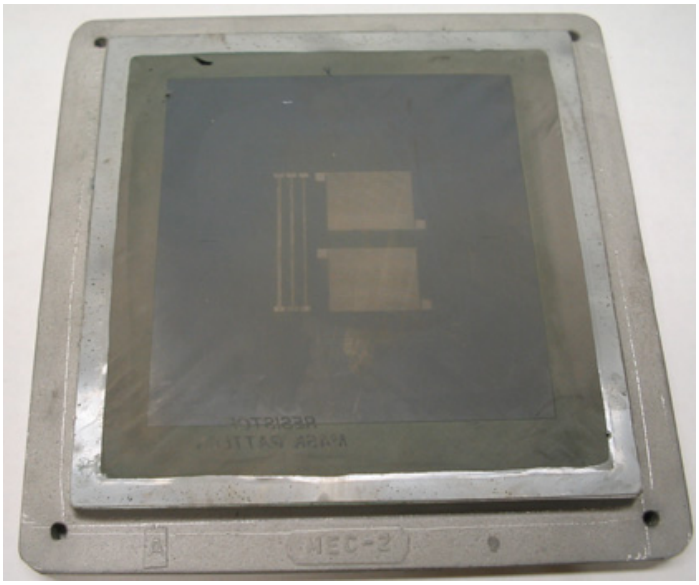


Figure 2.7. Screen was used for printing resistor patterns.

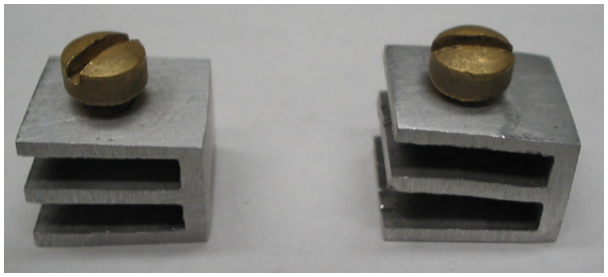


Figure 2.8. Two electrodes used for the measurement of electrical resistance.

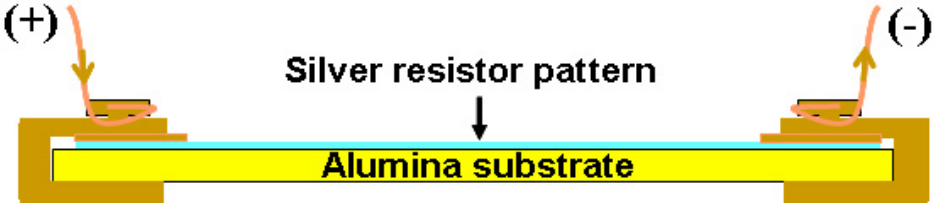


Figure 2.9. Illustration of electrical resistivity determination from printed resistor patterns.

2.3.2 Determination of Thermal Conductivity

Disc-shaped specimens with different thickness and dimensions as shown in Figure 2.10 were prepared by molding and low-temperature sintering of the nanoscale silver paste. Then the disc samples are polished into rectangular discs with two normal and parallel surfaces. The density ρ, specific heat c, and thermal diffusivity α of the sintered silver were determined by the Archimedes method, differential scanning calorimetry (DSC), and laser flash method [5], respectively.

(a) (b)

Figure 2.10. The disc-shaped silver specimens prepared by molding and low-temperature sintering.

In the Archimedes method, after the weight of a sample in both air and water are measured, the density of the sample can be determined by

$$\rho = \frac{\rho_{water} m_{air} - \rho_{air} m_{water}}{m_{air} - m_{water}} \tag{2.2}$$

where the ρ_{water} and ρ_{air} are the density of water and air at the measuring temperature, respectively. In most case, the density of the water at the room temperature is estimated to be 1 g/cm^3 and weight loss due to the air can be neglected. Then Equation 2.2 can be simplified into:

$$\rho = \frac{m_{air}}{m_{air} - m_{water}} \tag{2.3}$$

The results of the sample density are in the unit of g/cm^3.

In the DSC method, the specific heat of the sintered silver samples is measured by a differential scanning calorimeter (Model DSC-4, Perkin-Elmer, Norwalk, CT). The values are determined at several temperature points.

In the laser flash method, the experimental conditions described by Parker *et al.* [5], the ASTM method E1461-01 [6] and those of Hasselman and Donaldson [7] were followed. The flash source consisted of an Apollo Nd-glass laser with a beam diameter of 1.56 cm, a wavelength of 1.06 μm and a pulse width of approximate 250 μs. The flash was passed through a beam expander which allowed using the central portion of the beam, which generally is spatially more uniform than at edges of the beam. The uniformity of the radiation which impinged on the sample was checked by using photo-sensitive foot-print paper. Following the spatially uniform radiation of the flash on one side of the disc-shaped specimen as illustrated in Figure 2.11, the transient temperature of the opposite

face of the specimen was monitored by a liquid-N_2 cooled InSb infrared detector (Electro-Optical Systems, Inc., Malvern, PA). The time ($t_{1/2}$) to reach one half of the final temperature at which the sample reached thermal equilibrium was recorded. The thermal diffusivity of the low-temperature sintered silver was determined from disc-shaped specimens, by the flash technique using Parker's equation [5]

$$\alpha = 0.1388L^2 / t_{1/2} \tag{2.4}$$

α is the thermal diffusivity, L is the thickness of the disc-shaped specimen, and $t_{1/2}$ is the half temperature rise time at the specimen's rear surface.

After the three material properties were determined, the corresponding thermal conductivity k was obtained by

$$k = \rho c \alpha \tag{2.5}$$

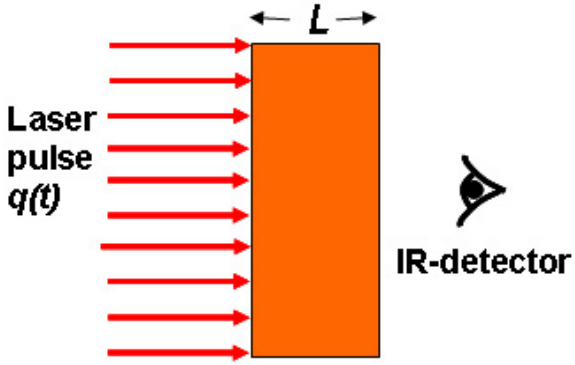


Figure 2.11. Illustration of the laser-flash experiment.

2.3.3 Determination of Elastic Modulus, Yield and Tensile Strengths

To determine the elastic modulus of the sintered silver, nanoscale silver paste was screen-printed onto the polished surface of a silicon wafer substrate. The detailed steps for the sample preparation are shown in Figure 2.12. Multiple layers were printed and sintered to obtain thicker silver films. Unlike solder-reflow, the nanoscale silver paste was sintered at temperatures far below the melting point of the bulk silver. Thus, the sintered silver films were stable enough at the sintering temperature that the thickness of the films can be increased by printing and sintering several times without drastic changes in the microstructure. After depositing and sintering 5 layers, the film was removed from the silicon substrate by soaking in very dilute HCl solution (~0.01%) with the assistance of ultrasonic vibration. After debonding from the silicon wafer, the thickness of sintered

silver film was measured and found to be about 101 μm. The silver film was sliced into 50.0 mm × 7.5 mm rectangular specimens for stress-strain measurements using in a ComTen 95 series machine (ComeTen Industries, Pinellas Park, FL) with a 2000-lb load cell. The setup of tensile test machine is shown in Figure 2.13. From the obtained stress-strain curves, one can determine the elastic modulus, 2% offset yielding strength and tensile strength.

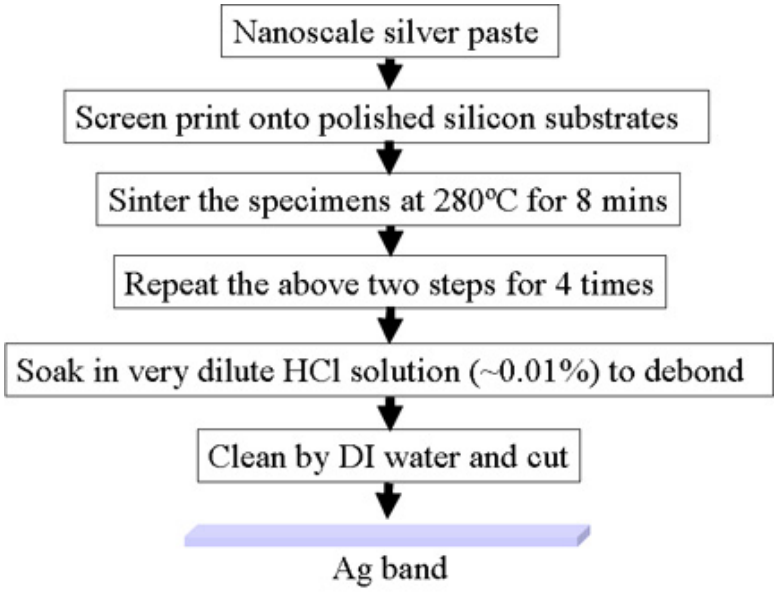


Figure 2.12. Preparation steps of the sintered sliver band-shaped samples for the tensile tests.

Figure 2.13. Setup of ComTen tensile test machine.

Several nickel/gold plated copper rods with ½-inch diameter as shown in Figure 2.14(a) were also jointed by low-temperature sintering of the nanoscale silver paste. Then

the silver joints were debonded as illustrated in Figure 2.14(b) using the ComTen tensile test machine to study the sintering properties for the large-area bondings.

(a) (b)

Figure 2.14. Nickel/gold plated copper rods for the preparation of sintered silver joints (a) and their debonding illustration.

2.3.4 Determination of Coefficient of Thermal Expansion

Disc-shaped specimens were also used to measure CTE of the sintered silver up to 275°C using a quartz dilatometer following the ASTM E228 and ASTM D696 standard test procedures. During the measurement runs, the thickness of the specimens was recorded at different temperatures. Since the quartz sample holder as shown in Figure 2.15 has a negligible thermal expansion at the temperature range of interest, CTE of the sintered silver could be determined directly from the thickness-temperature plots.

Figure 2.15. The quartz dilatometer used for the CTE measurement.

2.3.5 Determination of Thermal Stress in Silver Sintered on Silicon

Thermal stresses in the low-temperature sintered silver film on the silicon substrates were also determined. A curvature-based technique was used to measure the stresses in thin films of sintered silver on silicon substrates. For this purpose, the following equation can be derived with reference to a buckled bilayer composite as shown in Figure 2.16.

$$\frac{1}{R} = \frac{6(d_f + d_s)d_f}{M_f d_f^3 + M_s d_s^3}\sigma_f \tag{2.6}$$

where $M = E/(1-v)$ is the biaxial elastic modulus of the substrates and d_f and d_s are the thickness of the film and substrate, respectively. When $d_f << d_s$, it reduces into the famous Stoney formula [8]:

$$\frac{1}{R} = \frac{6d_f}{M_s d_s^2}\sigma_f \tag{2.7}$$

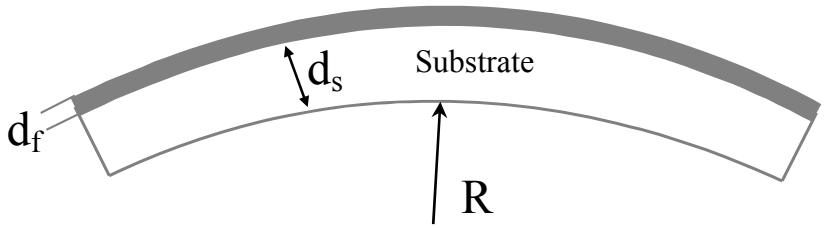


Figure 2.16. Deformation of a film–substrate bilayer composite.

So, after we measure the curvature *1/R* of the bilayer composite, we can estimate the stress in the film using the Stoney formula.

Figure 2.17 shows the optical setup for the curvature measurement and its schematic is shown as in Figure 2.18. The optical setup mainly consists of two parts: the optical scanning component and the hot stage mounted on the translation stage [9,10]. During the curvature measurement, a bilayer composite specimen is placed on the setter in the hot stage with the coated surface facing down. Then the smooth substrate surface (typically silicon) will reflect the incoming laser beam. The translation stage can carry the specimen to move so that the laser beam scans a certain distance *d* on the curved composite specimens as shown in Figure 2.19. During the scanning, the reflected laser beam will be projected onto a position-sensitive photodetector so that the distance changes *d′* due to the curvature can be recorded.

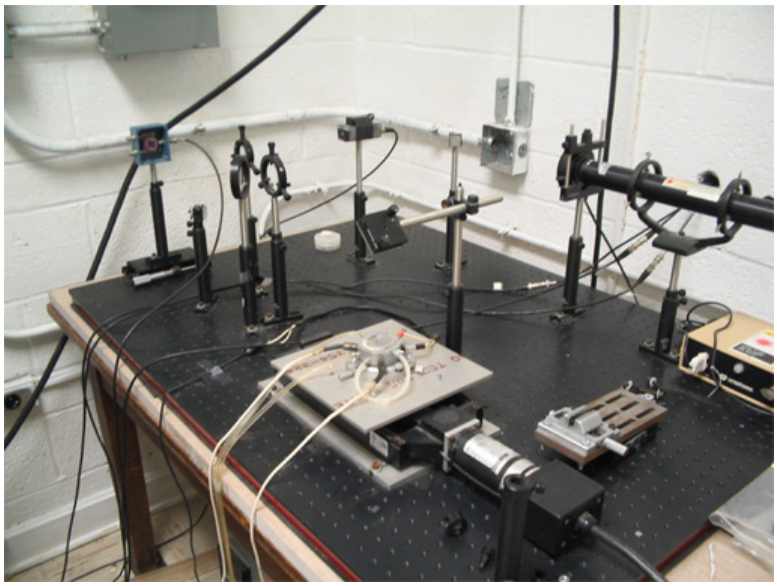


Figure 2.17. The optical setup for measuring the curvature of bi-layer composite during thermal heating.

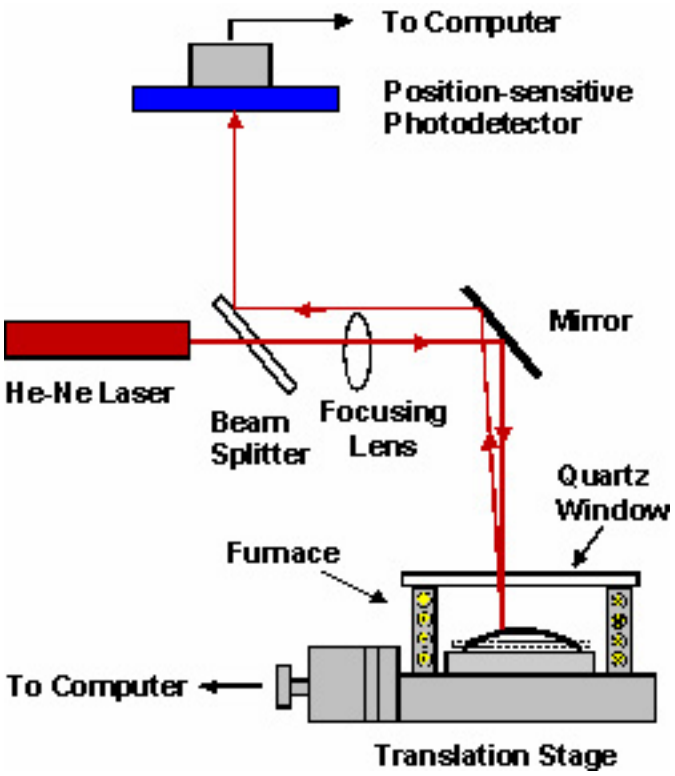


Figure 2.18. The schematic of optical setup for measuring the curvature of bi-layer composite during thermal heating.

The position-sensitive photodetector (Hamamatsu Corporation) is as shown in Figure 2.20(a) and the device can linearly change the perpendicular positions of an incoming laser beam into the output voltage values as shown in Figure 2.20(b). With the

assistance of the photodetector, the translate relationships in the optical setup during the measurement are shown in Figure 2.19. In the relationships, $m=d'/d$ is the slope during the curvature scan and it could be determined by the experiment. So once the length of the optical path length l is measured, we can get the curvature value $1/R$.

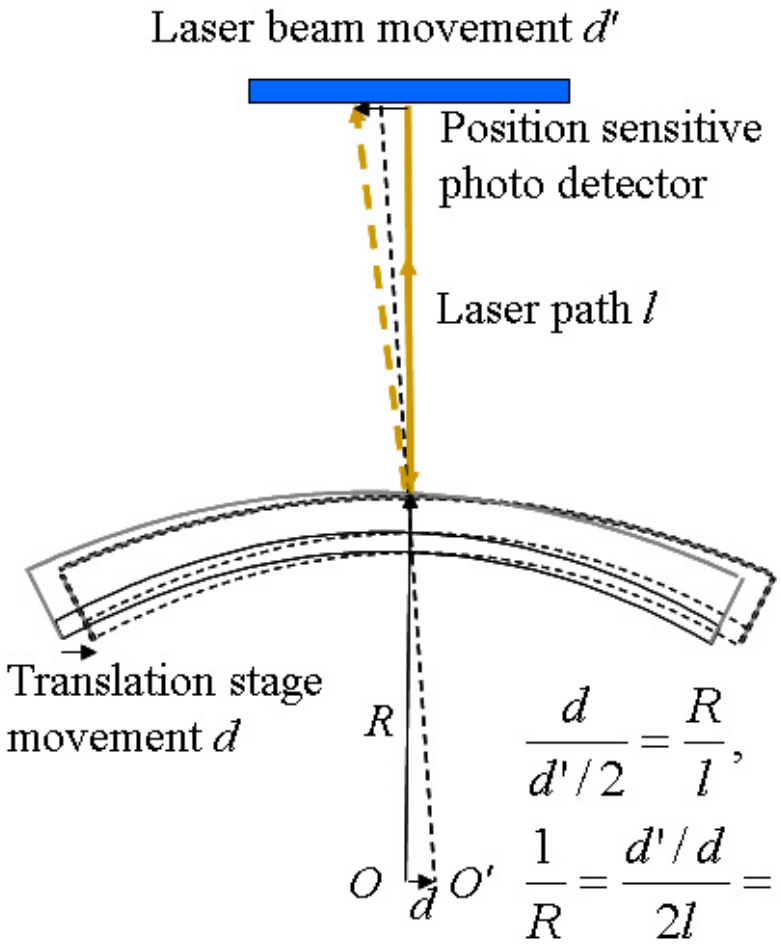
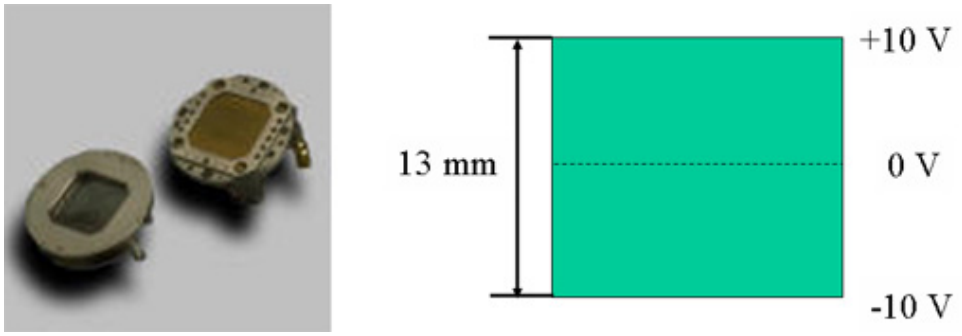


Figure 2.19. The illustration of the translate relationships in the optical setup during the curvature measurement.



(a) (b)

Figure 2.20. The position sensitive photodetectors used in the curvature determination optical setup (a) and their position-sensing mechanism (b).

For the sample preparation, we screen-printed nanoscale silver onto an ultra thin (~50 μm) double-side polished silicon substrate (Virginia Semiconductor, Inc., Fredericksburg, VA) and then sintered the coating silver on the silicon substrate at low temperatures. The thickness of the sintered silver was ~20 μm. Then the bilayer composite was cut into 5×2 mm^2 rectangular-shaped small specimens and put into the setter of the hot stage for the measurement.

In Figure 2.16, if the curvature of the bilayer composite is due to CTE mismatch related thermal stresses, we also have:

$$\frac{1}{R} = \frac{6M_f d_f (\alpha_s - \alpha_f)(T - T_0)}{M_s d_s^2} \tag{2.8}$$

Assume we know the properties of silicon substrates at the interested temperature ranges and the Poisson's ratio v and CTE α of the silver, the elastic modulus of the sintered silver can be also estimated after measuring curvatures at least two temperature points.

2.4 Device Attachment to Form Silver Joints

The preparation steps for the sintered silver joints are summarized in Figure 2.21. Direct bond copper (DBC, or called direct copper bond, IXYS Corporation, Santa Clara, CA) or pure copper substrates instead of printed circuit board (PCB) were used for bonding power devices. DBC substrates had either an aluminum oxide or an aluminum nitride ceramic base with 0.3-mm thick copper layers bonded directly on both sides and they were particularly good for the interconnection of the future high-power electronic circuits [11]. To prevent the copper oxidization during the sintering and form the sintered silver bonding, either nickel/silver or nickel/gold was coated on the DBC copper surfaces. The metallization procedure for coating nickel, gold or silver is described in Appendix A. The nickel layer was used as a diffusion barrier to prevent gold/copper interdiffusion or copper oxidization. And the gold or silver layer was used for the interdiffusion bonding to form the silver joint during sintering. The nickel/gold or nickel/silver coated DBC and copper substrates are shown in Figure 2.22.

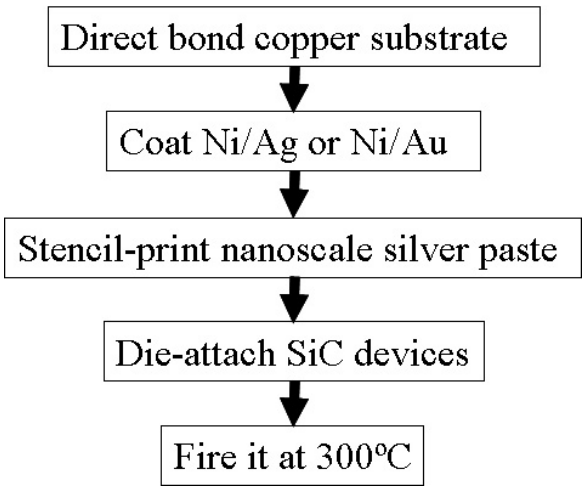
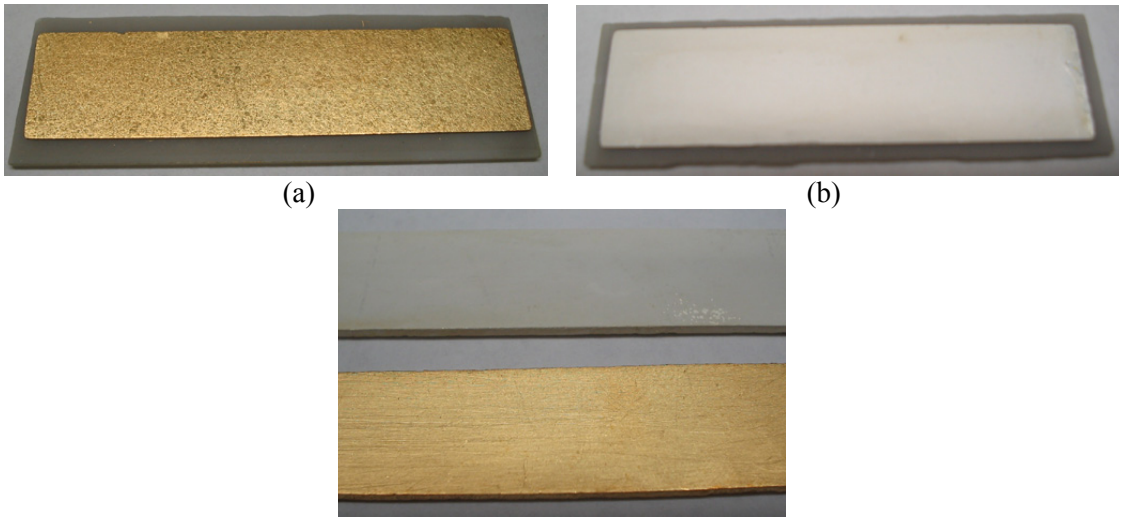


Figure 2.21. Preparation steps of the sintered sliver joint samples.

After the substrate metallization, the fabricated silver pastes were stencil-printed onto the DBC substrates and the copper substrates. The thickness of printed silver paste films was about 50 μm (2 mil). During stencil printing, it was important to use a rubber squeegee (soft) to print the silver paste back and forth for several times to make sure that the paste had good initial contact with the metallized substrate. This is illustrated in Figure 2.23. Otherwise the silver paste was more likely to induce cracks during sintering. Another parameter needed to take care is the thickness of the stencil printed paste. Too thick printed films were also prone to induce cracks during the sintering.



(a) (b)

(c)

Figure 2.22. Nickel/gold (a) and nickel/silver (b) coated AlN DBC and the nickel/silver and nickel/gold coated copper substrates (c).

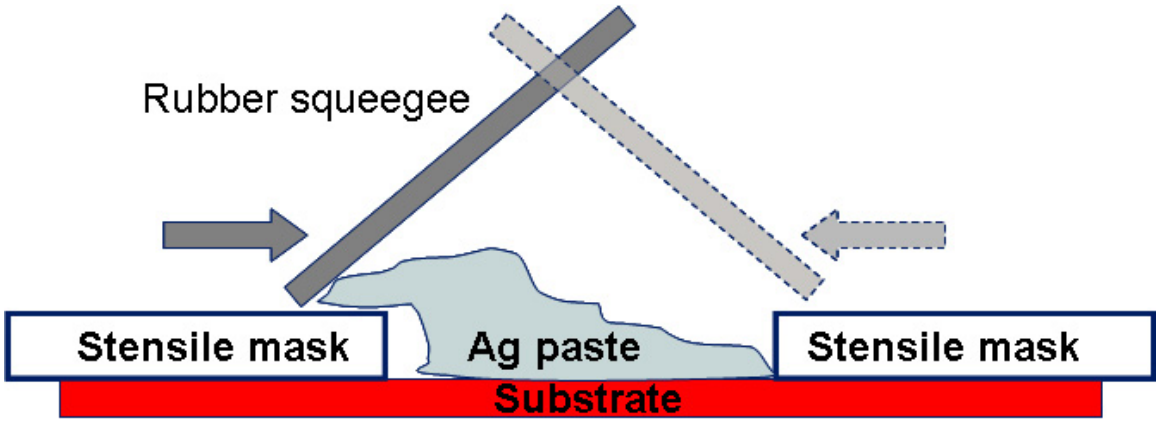
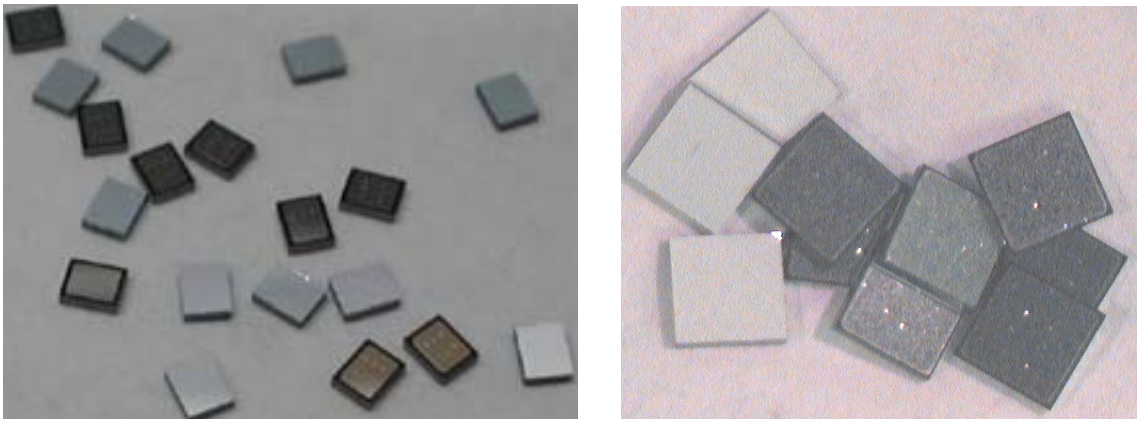


Figure 2.23. Illustration for the stencil printing process.

After stencil printing of nanoscale silver paste, two types of SiC Schottky rectifiers as shown in Figure 2.24 were used to form the sintered silver joints. They had characteristics as listed in Table 2.1 and they were free samples obtained from Infineon Technologies (Kanata, Ontario) and CREE Power, Inc. (Durham, NC), respectively. The cathode surfaces of the both devices were already metallized with Ni/Ag (e.g., the thickness of Infineon device metallization is totally 1.4 μm thick) when they were obtained, thus no further metallization was needed before the die-attachment.

During the device attachment, it is also important to smear the device around the printed silver paste to get the good initial contacts. A 100% initial contact is important for the nanoscale silver to diffuse into the gold or silver layers to form the strong bonding during the low-temperature sintering.



(a) (b)

Figure 2.24. Infineon (a) and CREE (b) SiC devices used to form sintered silver joints.

Table 2.1. The properties of two types of SiC Schottky rectifiers obtained from industry. Data from Infineon and CREE datasheets, respectively (under the condition of T_J=25°C).

Chip type	Die size (mm × mm)	Break down voltage (V_{BR})	Average forward current I_F	Forward voltage (I_F=10A)	Reverse leakage current (V_R=300V)
Infineon SIDC24D30SIC3	1.706 × 1.38	300 V	10 A	1.5 V	15 μA
CREE CPWR-0600S010C	2.26 × 2.26	600 V	10 A	1.6 V	50 μA

To study the relationship of the bonding strength versus the sintering time, the silver joints were sheared-off after sintered at 300°C for 10, 20, 30, 40, 50, 60, 75, and 90 mins, respectively, to check their bonding strengths. Finally, a sintering temperature of 300°C and a 40-min dwelling time as shown in Figure 2.25 was chosen to form strong silver bondings. Figure 2.26 shows some of the die-attached SiC devices that were ready for joint quality evaluation.

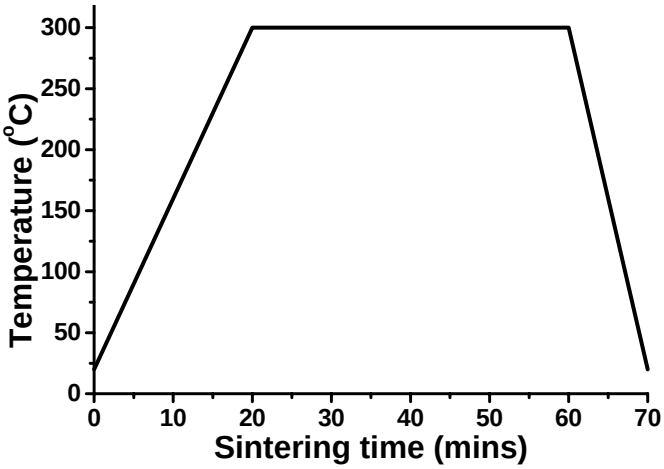
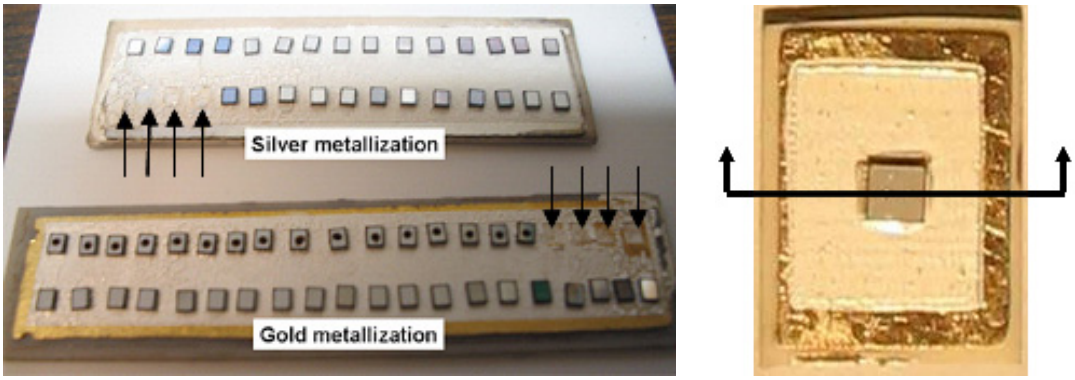


Figure 2.25. The sintering profile for achieve high bonding strength in the silver joints.



(a) (b)

Figure 2.26. (a) Die-attached Infineon SiC devices on silver or gold-coated DBC substrates for the die-shear tests. Arrows indicate the die-attaching cavities where the devices have been sheared-off. (b) A die-attached CREE device for the cross-sectional inspections.

2.5 Evaluation of Sintered Silver Joints

After the silver joint preparation, both nondestructive and destructive tests were explored to evaluate the joint quality. The nondestructive tests include the I-V curve measurements of the SiC Schottky rectifiers using a high-power curve tracer and the initial void inspection using scanning acoustic microscopy (SAM).

In the curve tracer tests, Sony Tektronix 371 programmable high-power curve tracer was used to obtain the typical forward and reverse I-V curves of the die-attached SiC devices. During the experiment, a two-probe test fixture as shown in Figure 2.27 was used to connect the two electrodes of the devices. To take out the voltage-drop due to the fixture, the two-probes of the test fixture were also connected directly onto a DBC surface to get an I-V curve for subtraction. The test condition was pulse width 250 μs and duty cycle <0.5% so that the junction temperature did not rise up drastically.

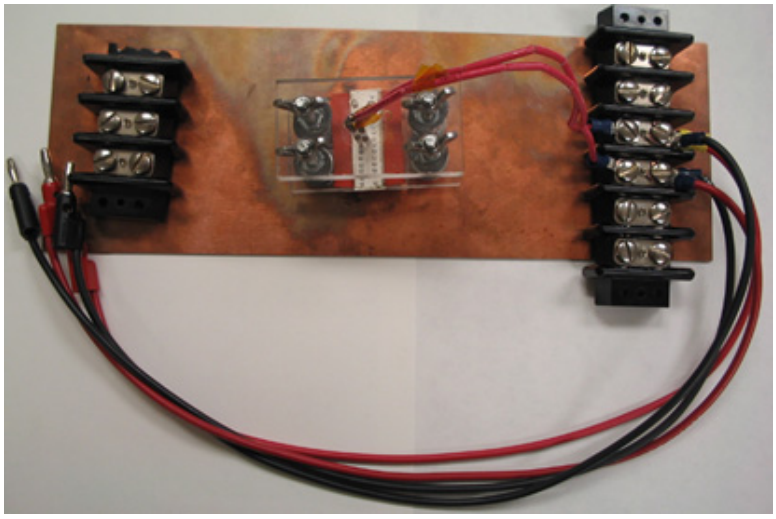


Figure 2.27. Fixture for the high-power curve tracer tests.

In the SAM inspection, a pulse-echo mode with a 75-MHz transducer (Sonix, Springfield, VA) was used to check voids in the silver joint layers [12]. In the SAM mode as illustrated in Figure 2.28, transducer produces a high-frequency sound wave which interacts with the sample and the reflected sound is used to produce images. Whenever a sudden change in acoustic impedance is encountered, like at a material boundary, a portion of sound is reflected and the remainder propagates through the boundary. The uniformity of an interested interface can be reflected by the image brightness.

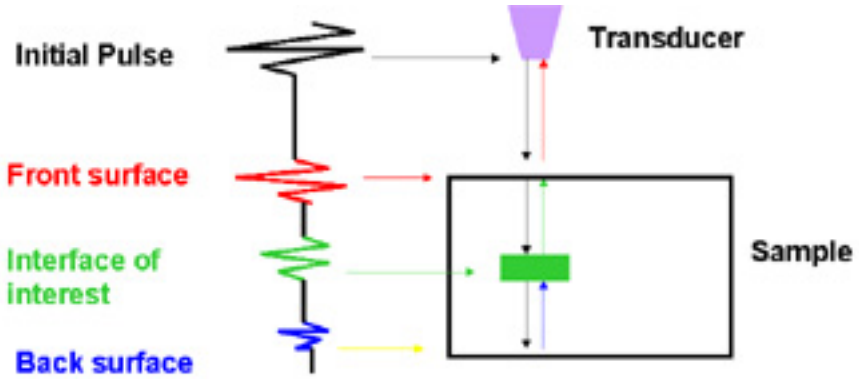


Figure 2.28. The pulse-echo mode illustration in scanning acoustic microscopy.

Figure 2.29 shows how to determine the position of interested silver joint layer from an SAM signal curve. Typically, a front surface follower (FSF) is enabled during the scanning. Since the signals from the front surface of the specimen (top surface of the SiC device) are typically very strong and they form the first intersection with the line of the front surface follower. The depth of the signal is then counted from the first intersection. Then the signal peak from the bottom metallization layer of the SiC device at a depth is given by:

$$t = \frac{2d}{v_l} \tag{2.9}$$

where d is the SiC thickness, which is 0.355 mm from the Infineon SiC device datasheet, v_l is the longitudinal sound velocity in SiC material, which is about 11,800 m/s from Ref. [13]. From the calculation, there should be a signal peak for the device metallization layer at about 0.06 μs. The peak is as shown in Figure 2.23 at a depth of 0.063 μs. Once the position of the back metallization layer is known, the next signal peak must associate with the silver joint layer. To obtain good quality images, the width of the gate signal should be wide enough to cover all of the signals from the silver joint layer as shown in Figure 2.29.

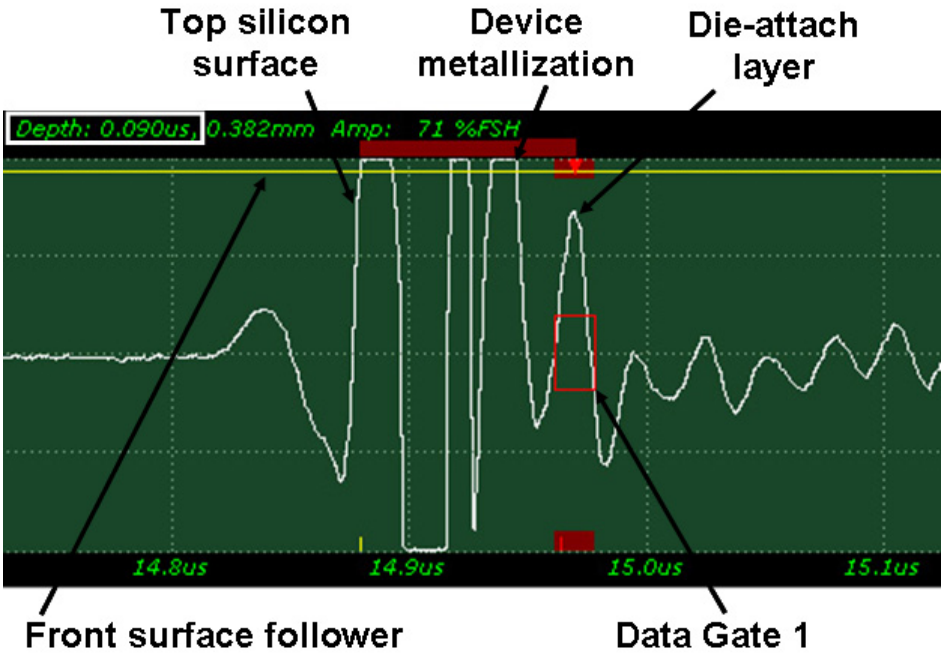
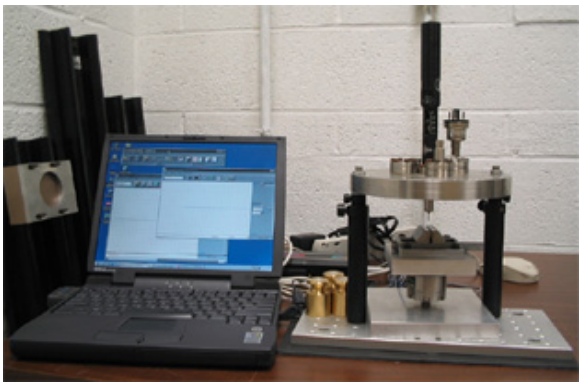
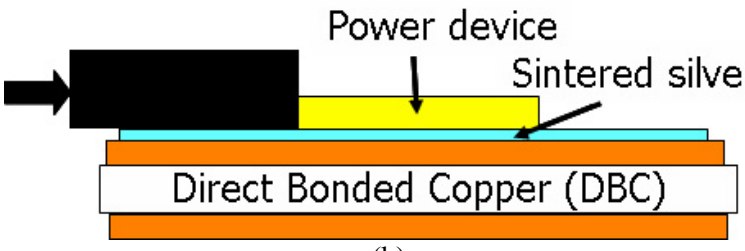


Figure 2.29. A typical scan SAM image of an Infineon SiC device die-attached silver joint.

The destructive tests include the die-shear, joint cross-sectional polishing, and joint broken tests in liquid nitrogen. In the die-shear tests, the die-attached SiC devices were sheared off using the setup in Figure 2.30 to determine the bonding strengths. Some eutectic lead-tin solder reflow-attached devices were also prepared for the bonding strength comparison.



(a)



(b)

Figure 2.30. The die-shear tester for die-shear-off test (a) and illustration for die shear-off (b).

In the cross-sectional polishing tests, the die-attached devices were molded in cured epoxies and then cut and polished for cross-sectional inspections using optical microscopy. The detailed experimental procedure can be found in Ref. [14]. One of the polished specimens is shown in Figure 2.31.

Figure 2.31. A silver joint specimen molded in cured epoxy for polishing and inspection.

Finally, in the joint broken tests, the silver joints were broken at low temperatures to prevent plastic deformation so as to obtain clearer microstructures using SEM. Liquid nitrogen was used to lower the temperature.

2.6 Silver Joint Reliability Assessment

Thermal cycling experiment was conducted to evaluate the reliability of the sintered silver joints and to identify their failure mechanisms. In the experiment, a number of the Infineon SiC devices were die-attached onto either silver or gold-coated Al_2O_3 DBC, AlN DBC, or nickel/silver-coated copper substrates. As a result, totally five types of sintered silver joints were prepared on:

(1) Silver-coated aluminum-oxide DBC;

(2) Silver-coated aluminum-nitride DBC;

(3) Gold-coated aluminum-oxide DBC;

(4) Gold-coated aluminum-nitride DBC;

(5) Silver-coated copper substrates.

Some of the samples prepared for a 50-250°C thermal cycling are shown in Figure 2.32. The two types of DBC substrates and copper substrates have different effective CTEs. So they can impose different thermal stresses to the silver joints during the temperature cycling.

Figure 2.32. The die-attached Infineon SiC devices used for the 50-250°C thermal cycling experiment. From top to bottom: Ag-coated Al_2O_3 DBC, Ag-coated AlN DBC, Au-coated Al_2O_3 DBC, Ag-coated AlN DBC, and Ag-coated copper substrates.

During the experiment, a Sikama belt reflow oven (Sikama International Inc., Santa Barbara, CA) was adapted as shown in Figure 2.33 to achieve a thermal cycling of 50-250°C. The temperature profile is shown in Figure 2.34. Sample holders with loaded samples are shown in Figure 2.35. The sample holders were made of aluminum bands with a smooth bottom surface. During the experiment, the sample holders were attached into the belt oven using the chains of the reflow oven and the rotating chains would carry the sample holders to fulfill the thermal cycles as illustrated in Figure 2.36. Several strategies were taken to approximate the temperature profile:

(1) The sample holders were adjusted so that they had good contact with the heating and cooling slots of the belt oven. This is shown in Figure 2.37. The good contacts help the sample holders heat up and cool down quickly.

(2) As shown in Figure 2.33, only four of the total five slots of the belt oven were set for heating up and the last one were left at room temperature for

the cooling down. The four slots for heating are set to 280°C during the experiment, a temperature much higher than 250°C, so that the samples could reach 250°C during the cycling.

(3) The belt oven was left up and two fans were used to blow from the underneath of the reflow oven for more effective cooling down when the samples were cycled under the belt oven.

(4) The belt oven was covered with a lid from the topside to reserve heat and the high temperatures.

(5) The speed of the rotating chains of the belt oven was set to be 12 inch/min. The rotation time for one thermal cycle was 7 minutes and 6 seconds. About 2 minutes of the total cycling time was for heating and the left 5.1 minutes was for cooling.

(6) Before the experiment, a surface-mountable thermocouple was attached to the sample holder to monitor temperature profile to make sure it approximates the temperature profile as shown in Figure 2.34.

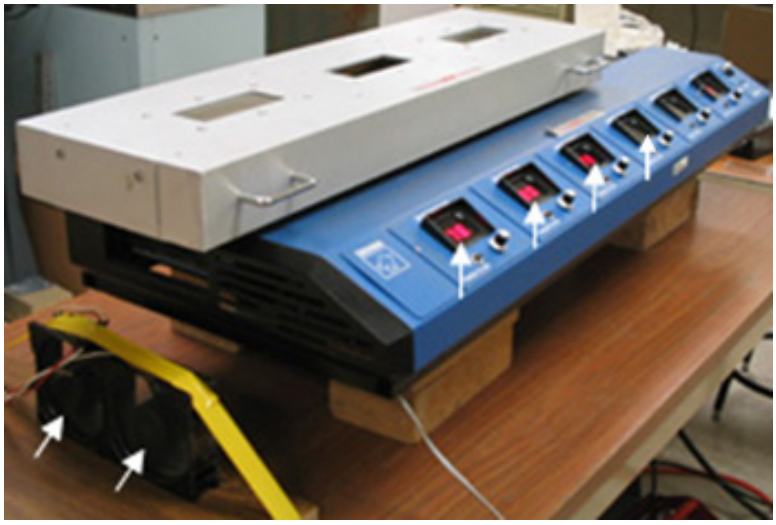


Figure 2.33. The Sikama belt reflow oven adapted for the 50-250°C thermal cycling experiment. The four perpendicular arrows in the middle show the four of the total five slots were set to be 280°C. The fifth is left for cooling and the last window is for setting the cycling speed. The two arrows in the lower left corner indicate the two blowing fans for cooling down.

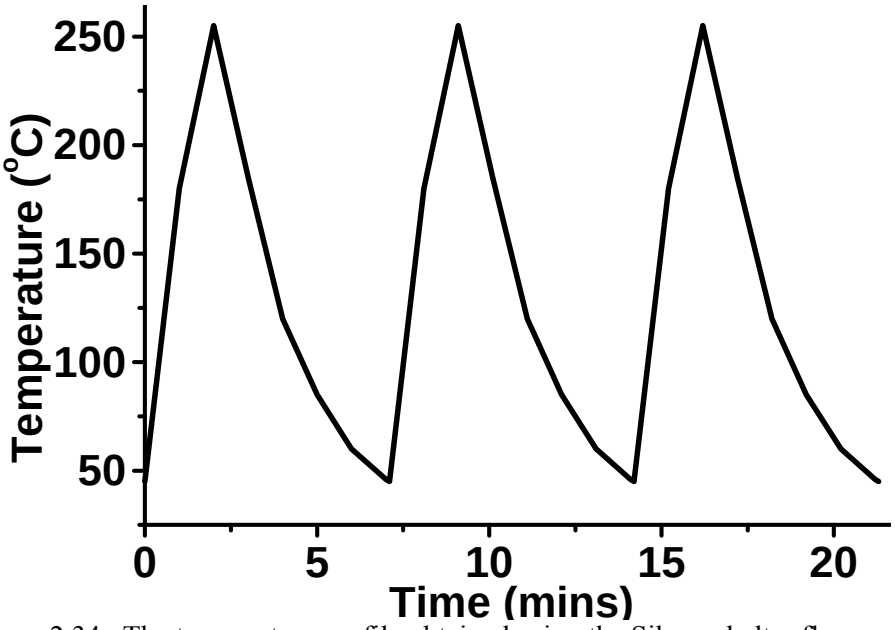


Figure 2.34. The temperature profile obtained using the Sikama belt reflow oven.

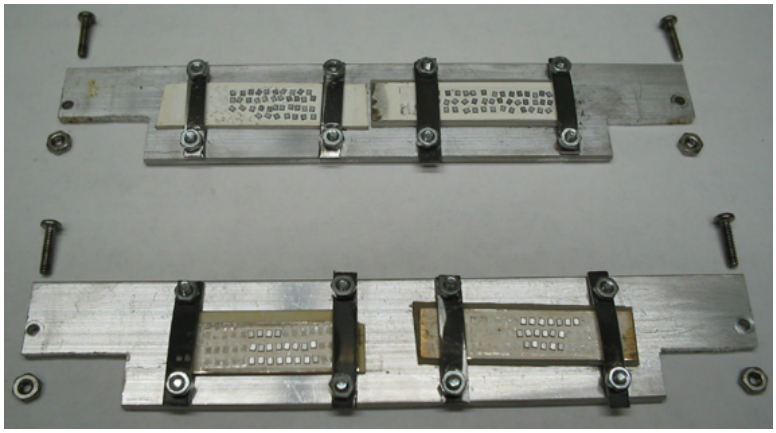


Figure 2.35. The fixture and samples used for the 50-250°C thermal cycling.

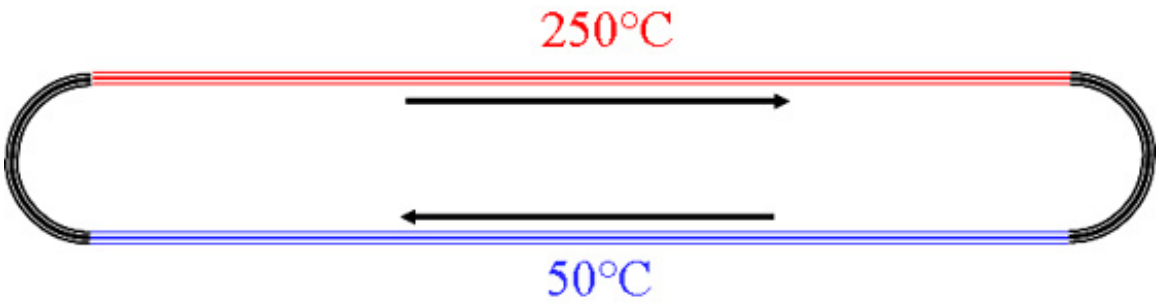


Figure 2.36. Realization of 50-250°C temperature profile using the Sikama belt reflow oven.

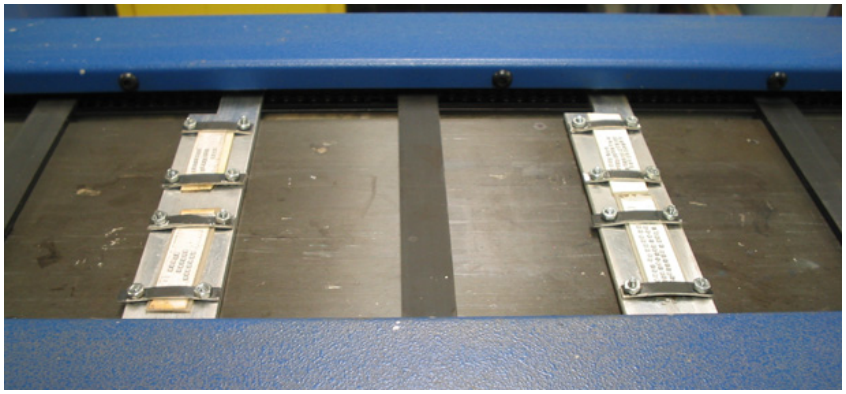


Figure 2.37. The loaded sample holders installed in the belt oven during the 50-250°C thermal cycling. The covering lid was removed for clarity.

During the thermal cycling experiment, the samples were taken out occasionally from the thermal cycling oven for both the non-destructive and destructive inspection. Again, the non-destructive inspection included SAM and I-V curve tests and the destructive inspection included the die shear-off test and the SEM inspection of the debonded joints.

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[13] NIST websites: http://www.ceramics.nist.gov/srd/summary/scdscs.htm.

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Chapter 3
Results and Discussion

In this chapter, we present the experiment results and discussions. First, the properties of the prepared silver paste and the electrical, thermal and mechanical measurement results of the low-temperature sintered silver are presented. Then it is followed by the electrical, thermal and mechanical performances of the sintered silver joints. Based on the temperature cycling results, the reliability and failure mechanism of the silver joints are also discussed. Along the discussion, the advantages of the low-temperature silver sintering technology in the power electronic packaging applications are presented.

3.1 Properties of Silver Paste and Low-Temperature Sintered Silver

Figure 3.1 shows the 78, 84, and 90 wt.% silver-loading nano-pastes stored in containers. The 78 wt.% silver paste was also put into a plastic syringe for dispensing. Generally, among the prepared nanoscale silver pastes with 78, 81, 84, 87 and 90 wt.% silver loadings, the pastes with lower silver loadings such as 78 wt.%, 81 wt.%, 84 wt.% were found to have better flowability similar to commercial microscale silver paste and they were suitable for syringe-dispensing or screen-printing; while the pastes with higher silver loadings such as 87 wt.% and 90 wt.% were relatively dry and only can be stencil-printed. They all had a black color which was quite different from microscale silver paste shown in Figure 3.2(a).

The scanning electron microscopy (SEM) image in Figure 3.3 shows the microstructure of an as-prepared nanoscale silver paste with 78 wt.% silver loading. The green density of the 78 wt.% silver paste was about 38% of bulk silver.

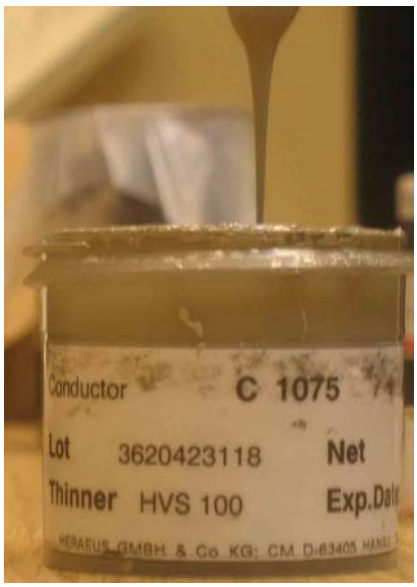
(a)

(b)

(c)

(d)

Figure 3.1. The 78 wt.% (a), 84 wt.% (c), and 90 wt.%(d) silver-loading nano- pastes stored in containers. (b) The 78 wt.% silver paste stored in a plastic syringe.



(a)

(b)

Figure 3.2. Good flowability of the commercial microscale silver paste (a) and that of the 78 wt.% nanoscale silver paste.

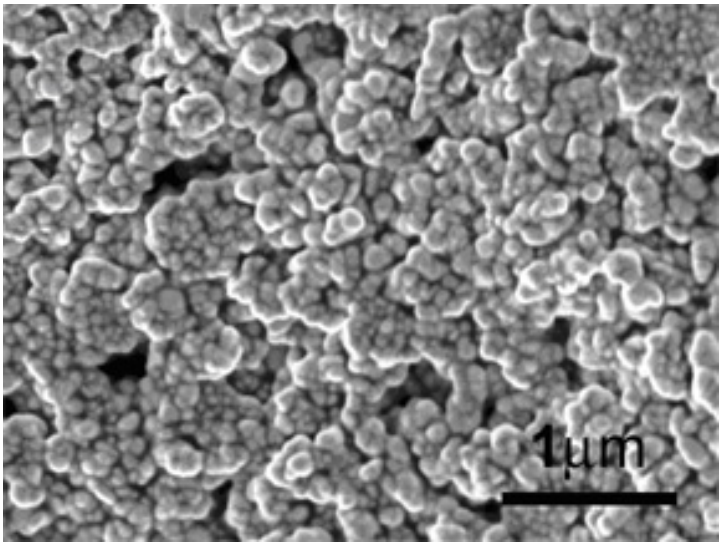
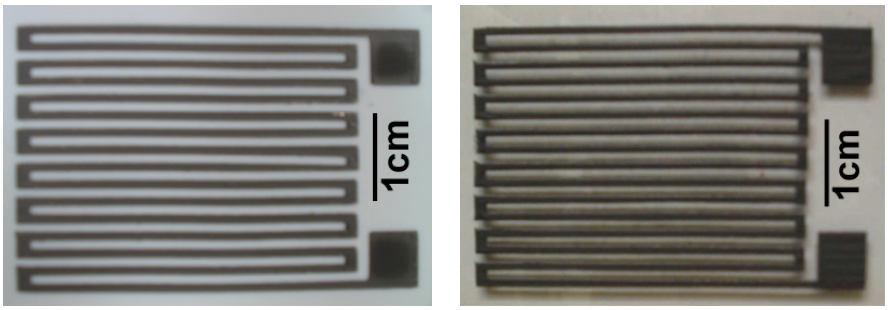


Figure 3.3. Scanning electron microscopy of the as-prepared 78 wt.% nanoscale silver paste.

The pastes can be processed onto most substrates including metals, silicon, alumina, glass, and kapton films for the low-temperature sintering. Figure 3.4 shows the printed silver paste patterns before sintering.

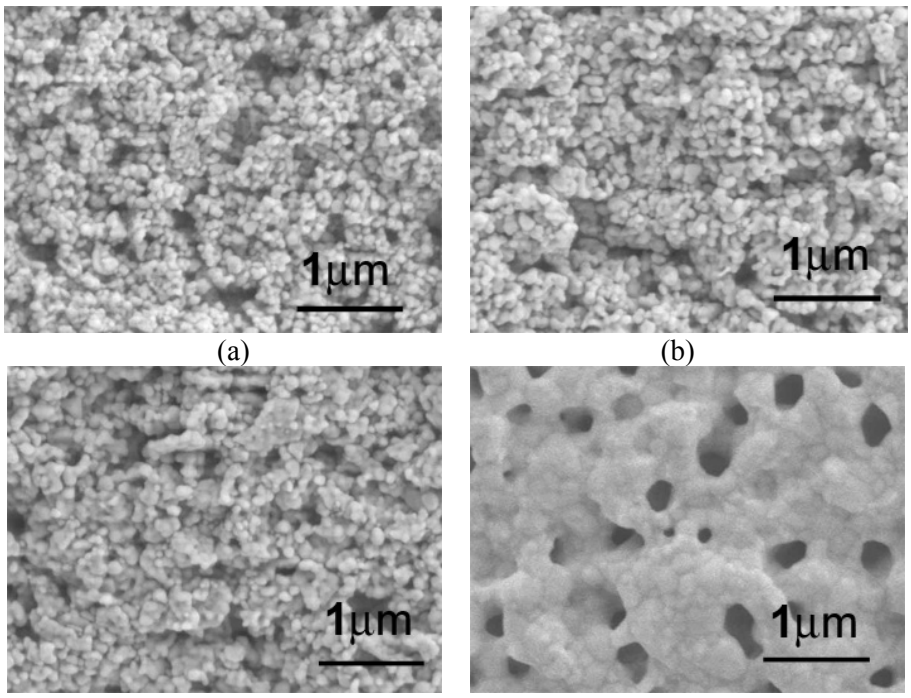


(a) (b)

Figure 3.4. The stencil-printed nanoscale silver pattern on alumina (a) and that on glass (b) before sintering.

The following phenomena were observed during the low-temperature sintering:

(1) The sinterable temperature of the formulated nanoscale silver paste was controlled by the highest burnout temperatures of the three organic components (usually it is the binder or surfactant). With the organic components still in the pastes, the nanoscale silver could not be sintered. As shown in Figure 3.5, the microstructures of the nanoscale silver paste retained until about 275°C, at what temperature the organic burned out and then the silver paste was sintered rapidly. At 275-280°C, the rapid densification was observed right after most of the binder components were gone.



(a) (b)

(c) (d)

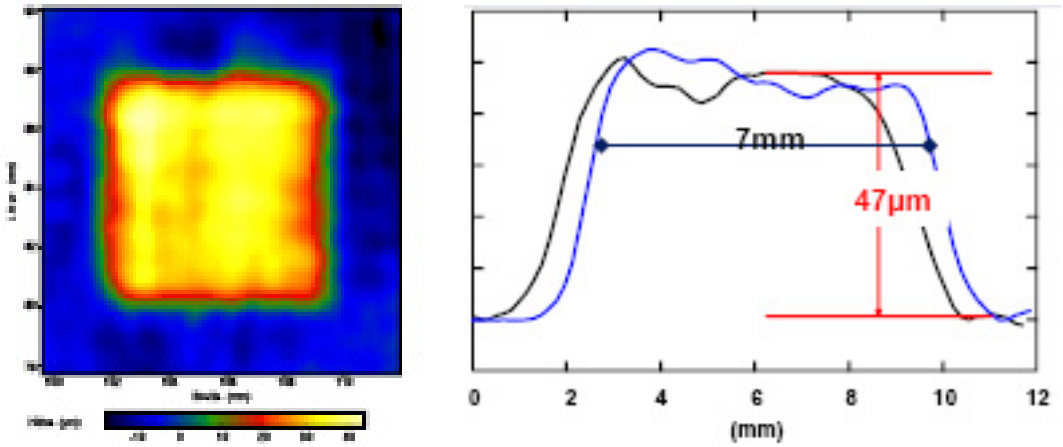
Figure 3.5. The microstructure changes of nanoscale silver heated up to 200°C (a), 225°C (b), 250°C (c) and 275°C, respectively, during the low-temperature sintering.

(2) The oxygen in air played an important role during the organics burnout and thus the silver paste sintering. The increase of the partial pressure of oxygen during sintering helped the organics burnout and thus sped up the sintering of the nanoscale silver pastes. Experiments did in vacuum and pure nitrogen found that the nanoscale silver paste could not be sintered at temperatures even as high as 350°C at the extreme conditions without oxygen. It is believed that the oxygen help to break the hydrocarbon chain during the organic component burnout and thus help on the sintering.

(3) Given the same sintering temperature, the silver pastes with higher silver loadings tended to be sintered earlier. The effects were more evident in the case of covered sintering, in which case the organic components were more difficult to burn out and oxygen was harder to get in due to the coverage. The difficulty of organic burnout and thus the paste sintering would be discussed in detail later since the formation of the silver joints was of the case of covered sintering.

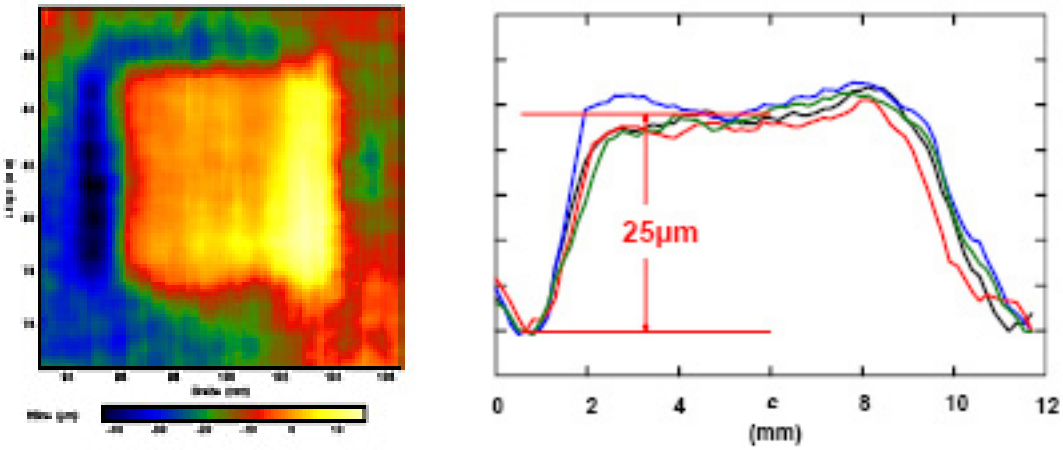
(4) In the general case, thickness of the as-printed silver paste was reduced by about 50% after the low-temperature sintering. This is shown in Figures

3.6 and 3.7. Correspondingly, the density of the sintered silver increased from 35-45 wt.% bulk silver density to about 80 wt.%.



(a) (b)

Figure 3.6. Topological image (a) and its two topological profiles (b) of the printed nanoscale silver paste before sintering.



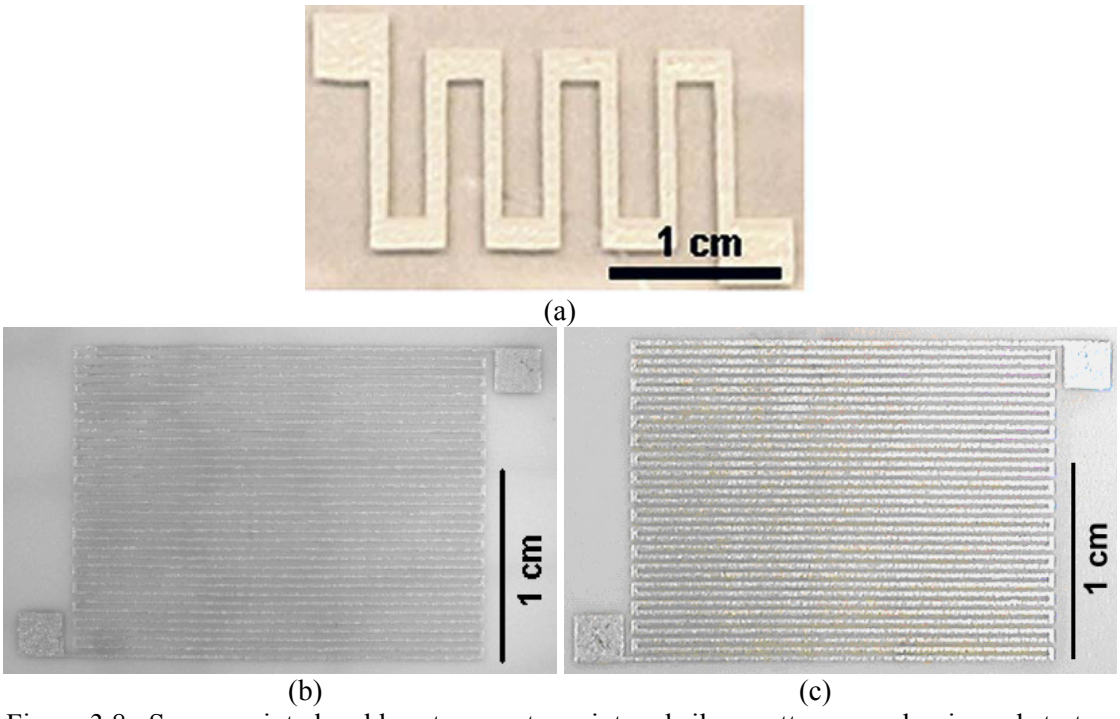
(a) (b)

Figure 3.7. Topological image (a) and its two topological profiles (b) of the printed nanoscale silver paste after sintering.

From the above experimental results, we can conclude that the existing organic components in the silver paste have three major functions. They not only stabilize the nanosilver particles and make the paste easy process, but also help the nanoparticles passing the low-temperature zone and thus densify them upon the organic burnout.

Several stencil or screen-printed and low-temperature sintered silver patterns on alumina substrates are shown in Figure 3.8. The thickness of printed silver was reduced about 50%, from 50 µm (2 mil) to 25 µm (1 mil), during the sintering. The density of the partially sintered silver at this point, measured by a density case (the Archimedes method), was about 8.6 g/cm^3, which was ~80 wt.% of bulk silver. Since the initial

density of silver paste was about 35-45 wt.% of the bulk silver, the density changes were consistent with the thickness changes during the low-temperature sintering.



(a)

(b) (c)

Figure 3.8. Screen-printed and low-temperature sintered silver patterns on alumina substrates.

The XPS analysis [1] results of the as-prepared silver paste and that after the paste sintering are shown in Figure 3.9. Because the XPS signals were from a thickness only about 10 nm, there were still significant amounts of carbon and oxygen after the low-temperature sintering. However, from a typical SEM/EDS analysis which had a much larger detectable thickness of ~1μm, it was found that the silver paste had a purity of 99.8% after the low-temperature sintering as shown in Figure 3.10. Furthermore, no oxygen element was detectable. This meant that almost all the organic components in the original silver paste were burn out during the low-temperature sintering and therefore the sintered material was almost pure silver.

SEM revealed that the microstructure of the low-temperature sintered silver consisted of a dense network with microscale pores shown in Figure 3.11. The porous microstructure of the sintered silver indicated that the sintering was still in its intermediate stage as discussed in Chapter 1. The microscale pores could gradually pinch off if the dwelling temperature during the sintering was prolonged, leading to the final sintering stage. Due to the sintering temperature was far below the melting point of bulk silver, the transfer time from the intermediate stage to the final stage took a very long

period (in magnitude of months as discussed in Section 3.3). This meant that the porous silver, though was in its intermediate sintering stage, was already a pretty stable structure that could be used for bonding the power devices. As our discussion later, the porous microstructure of the low-temperature sintered silver has advantages for the power device bonding applications.

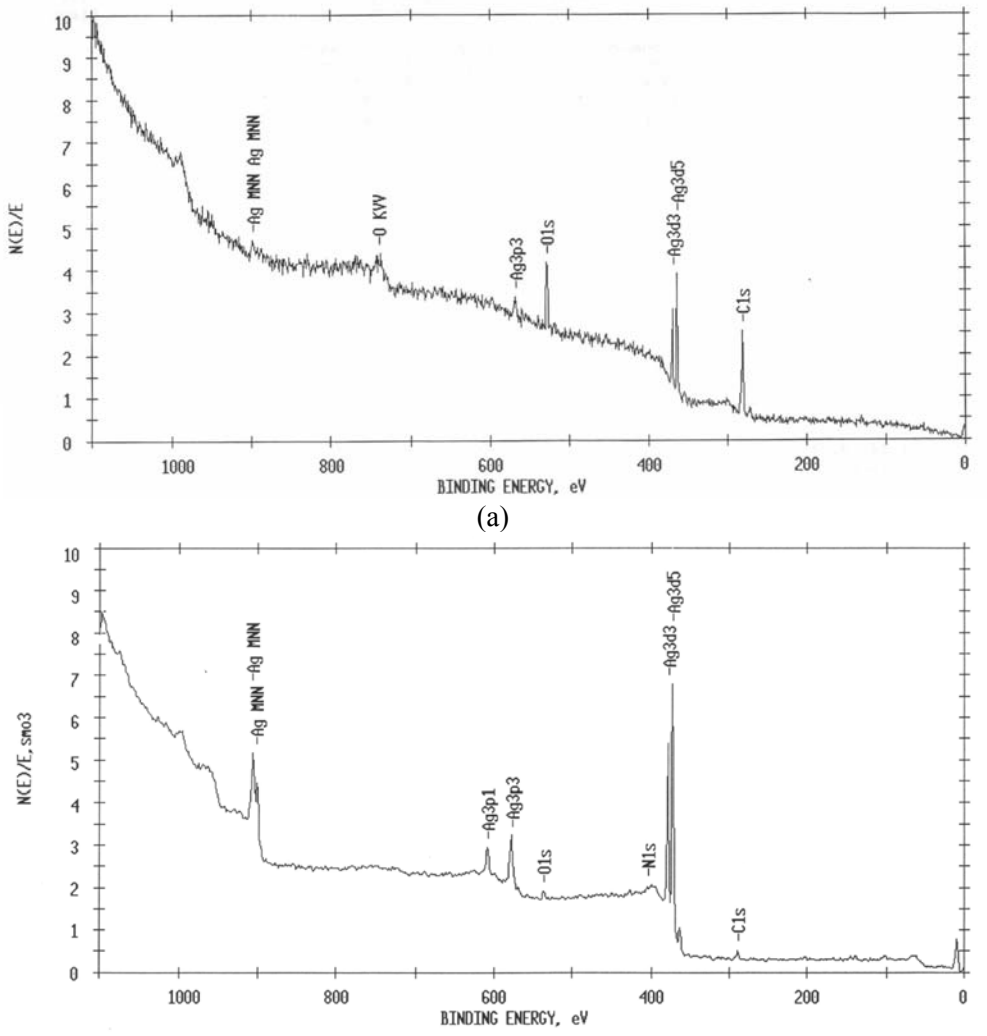


Figure 3.9. XPS analysis of the as-prepared 78 wt.% silver paste (a) and that of after the low-temperature sintering (b). Compared (b) to (a), it was found that the carbon and oxygen were reduced more than 90% during the low-temperature sintering.

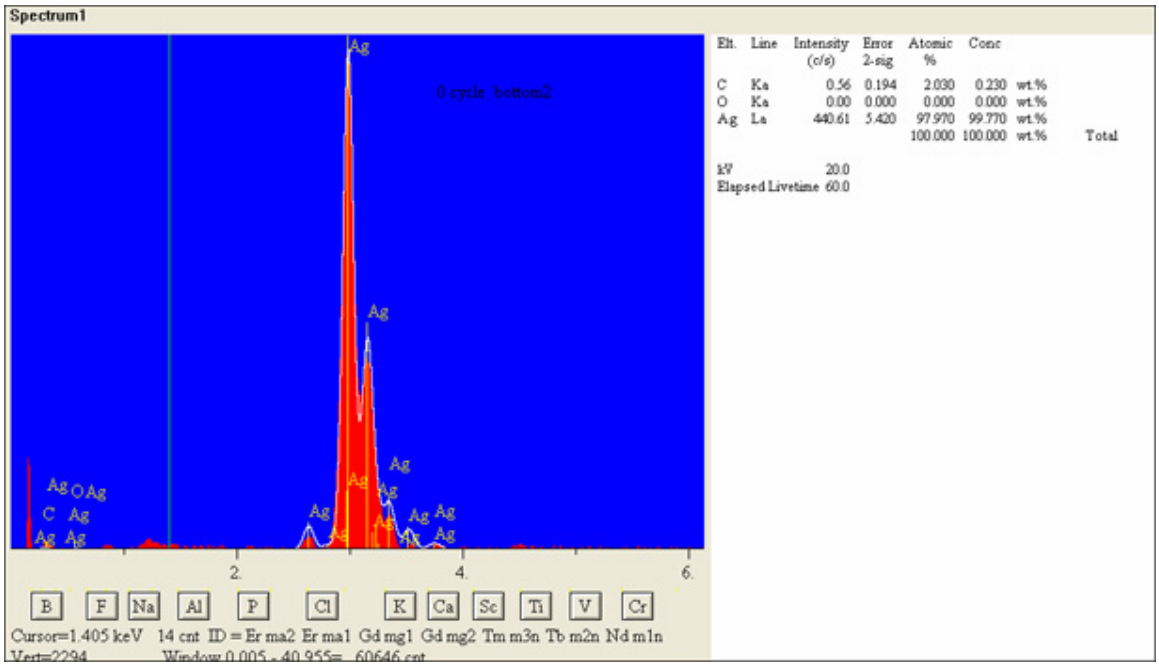
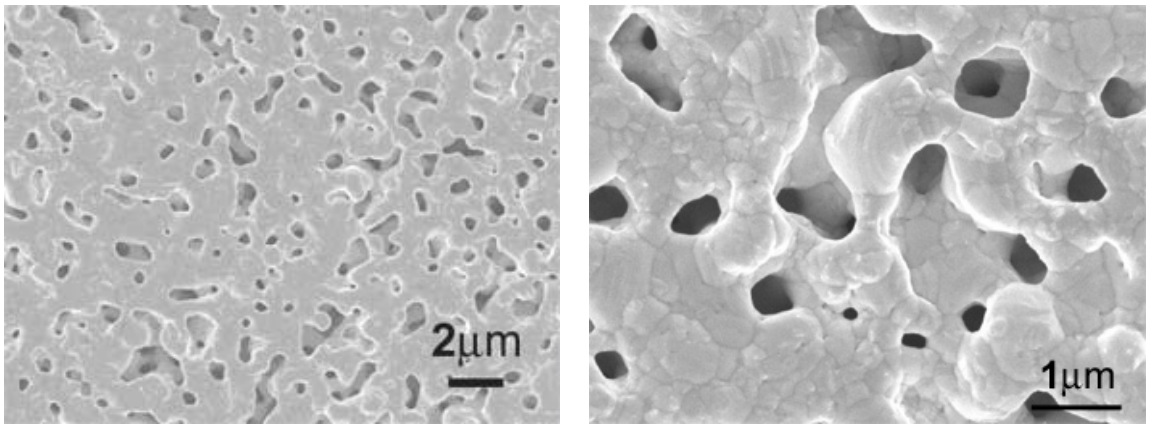


Figure 3.10. EDS analysis of the 78 wt.% silver paste after the low-temperature sintering. Silver is about 99.77 wt.% after the low-temperature sintering and the rest of the sintered silver is carbon (~0.23 wt.%). There is no detectable oxygen left.

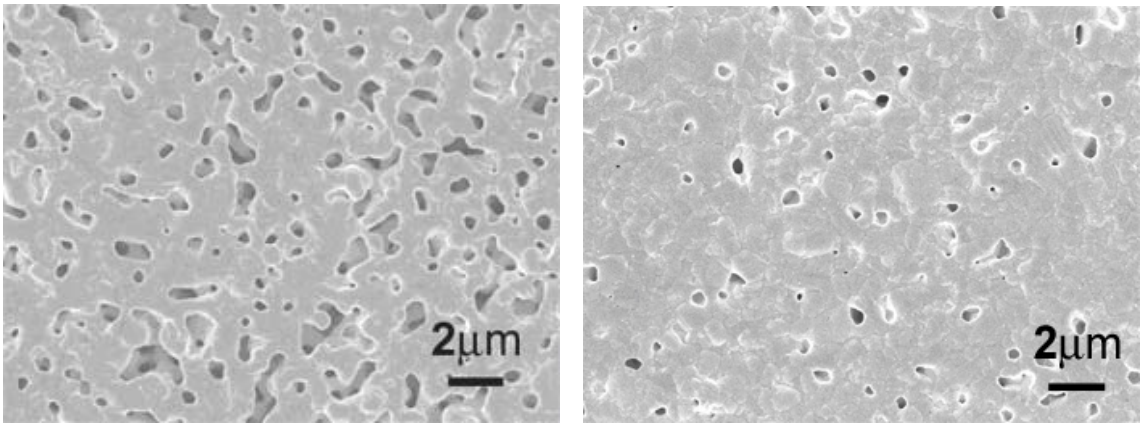


(a) (b)

Figure 3.11. Microstructure of the low-temperature sintered nanoscale silver on an alumina substrate (top surface of a sintered film with thickness about 1 mil). (a) at 10 Kx and (b) 50 Kx.

The microstructures of the low-temperature sintered silver films were also affected substantially by the sintering profile as well as the sintering substrates. Generally speaking, abrupt sintering (i.e., directly put onto a hot plate of 280°C) resulted in a more sintered dense structure with less porosity as shown in Figure 3.12. This was because as discussed in Chapter 1, both densifying and none-densifying diffusions could happen during the sintering procedure. However, the none-densifying diffusions (surface diffusions) were more favorable at relatively low-temperatures and the densifying

diffusions (lattice and grain-boundary diffusion) were dominant at relatively high-temperatures. At relatively low temperatures, the none-densifying diffusions only resulted in significant grain growth but little density increase. They typically resulted in a net work formation and prevented further densification even at higher temperatures. A common approach to avoid the problem was to use faster sintering rate to bypass the low-temperature regime quickly so that densification could happen at higher sintering temperatures [2-4].

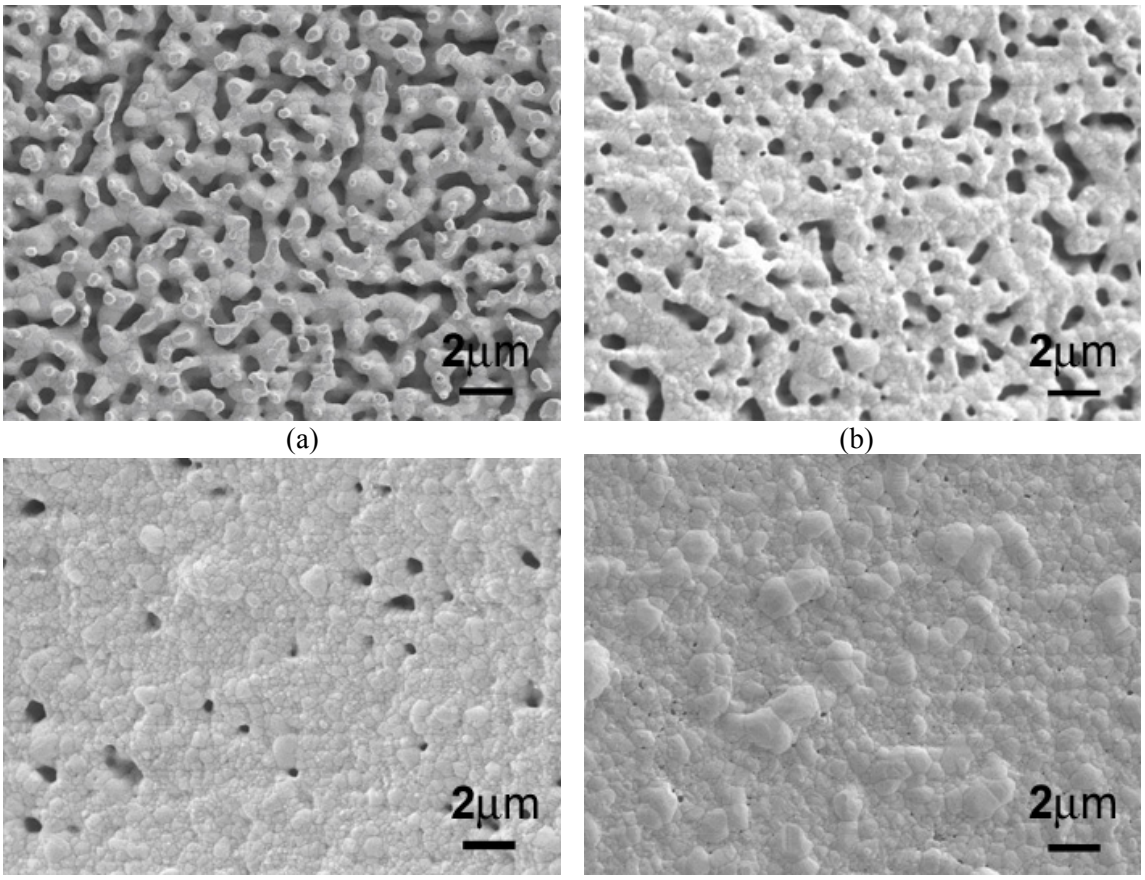


(a) (b)

Figure 3.12. Microstructures of the low-temperature sintered nanoscale silver (a) by follows the profile in Figure 2.6 and (b) abrupt sintering, respectively.

The effect of sintering substrates could be explained by the constrained sintering effect [5,6]. The constraining effect during sintering resulted in larger porosities in the partially sintered materials as shown in Figure 3.13, the closer to the constraining interface, the more evident the constraining effect was. The effective thickness could be up to several mils from the constraining interface. The effect was also related to the properties of the particular constraining substrates and sintering materials.

In the following part, the characterization results of the electrical, thermal, and mechanical properties of the low-temperature sintered silver were presented. The characterization based on an assumption that the low-temperature sintered silver reached about 80% density of bulk silver. This was confirmed by the density measurement after the low-temperature sintering.



(a) (b)

(c) (d)

Figure 3.13. Microstructures of the low-temperature sintered nanoscale silver on a silicon substrate (a) at the silicon-silver interface, and at 1 mil (b) and 4 mil (c) away from the interface and (d) free sintering case (pill off the baked silver paste film and then sinter). All sintering profiles follow that shown in Figure 2.6.

3.1.1 Electrical Properties

Electrical resistivity is one of the very important parameters for the interconnect materials, since the power device typically needs to handle large current flow. The resistance of the interconnections is directly related to the current handling capability and the extra power loss. Resistor patterns as shown in Figure 3.8(b) and (c) were used to measure the resistance of low-temperature sintered silver. Figure 3.14 shows the electrical resistivity values of the nanoscale silver paste and the microscale silver paste (C-1075, Heraeus Inc., Chandler AZ) after the identical heat treatment at 280°C. Resistivity values of three types of solders and that of the bulk silver are also included for comparison. From Figure 3.13, one can see that the nanoscale silver paste has about 2.4 times of the electrical resistivity of that of the bulk silver at room temperature. But the

value is substantially lower than those of the solder alloys. The value is also lower than that of the sintered commercial silver paste. Moreover, at temperatures above 500ºC, the resistivity values of the sintered nanoscale silver paste are still stable but not those of microscale silver paste. These results provide evidence that the nanoscale silver paste is sintered at 280ºC into a relatively stable intermediate stage and it is relatively stable up to 650ºC as shown in Figure 3.15. But the microscale silver paste is not. At 280°C, the microscale silver is not sintered at all; at temperatures above 500ºC, the microscale silver paste starts to sinter and thus its electrical resistance begins to change. Figure 3.16 shows the SEM pictures of the microscale silver paste before and after the resistivity measurement, where (a) shows that the microscale silver paste is not sintered at 280°C and (b) shows that the microscale silver paste are partially sintered during the resistivity measurement. The results also demonstrates that the reduction of the particle size from the microscale to nanoscale has reduced the sintering temperature of silver pastes from above 500°C to lower than 300°C.

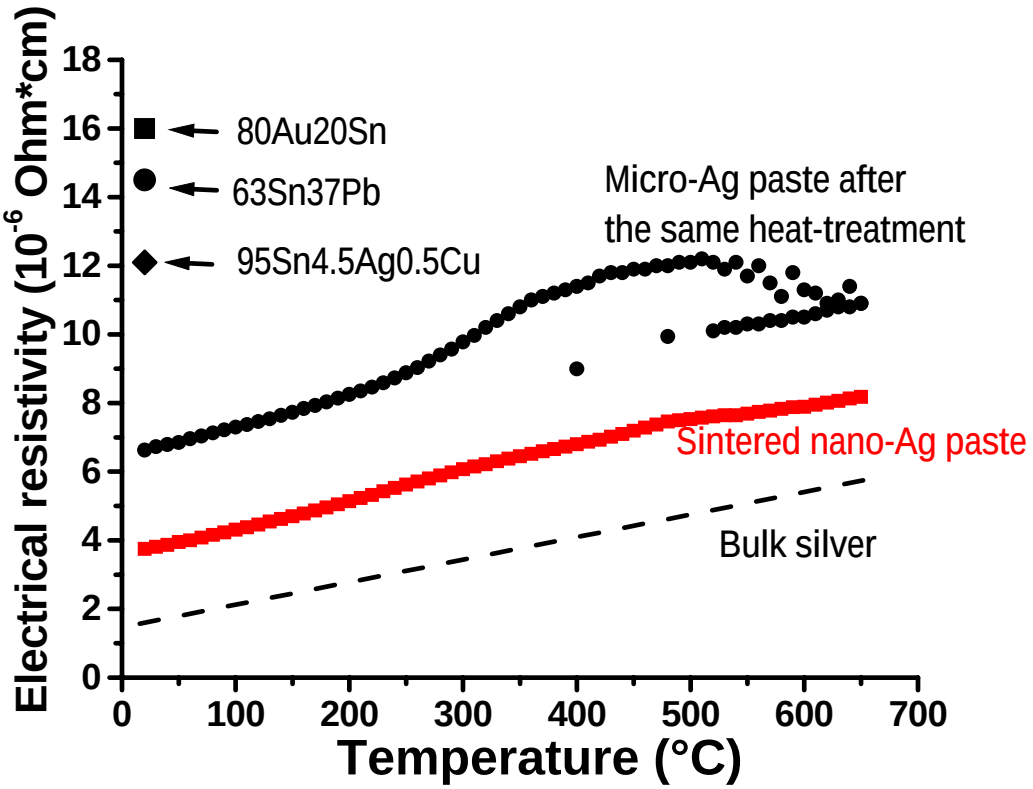
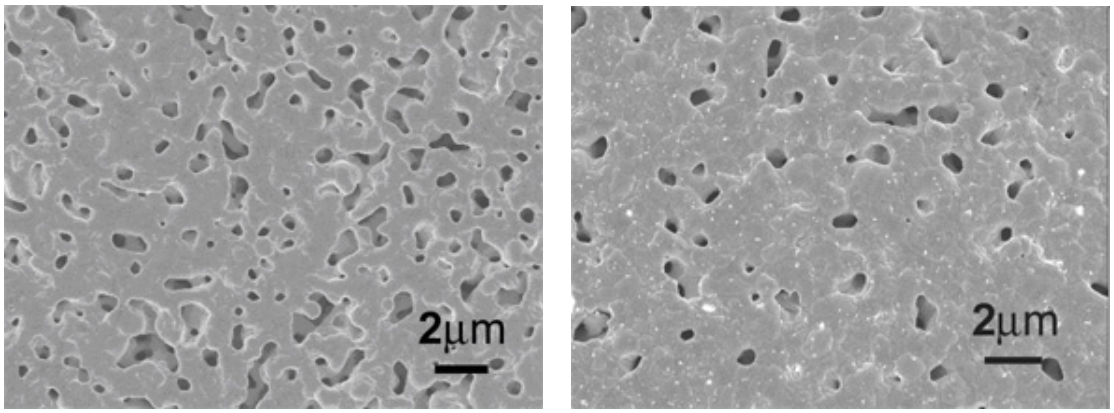
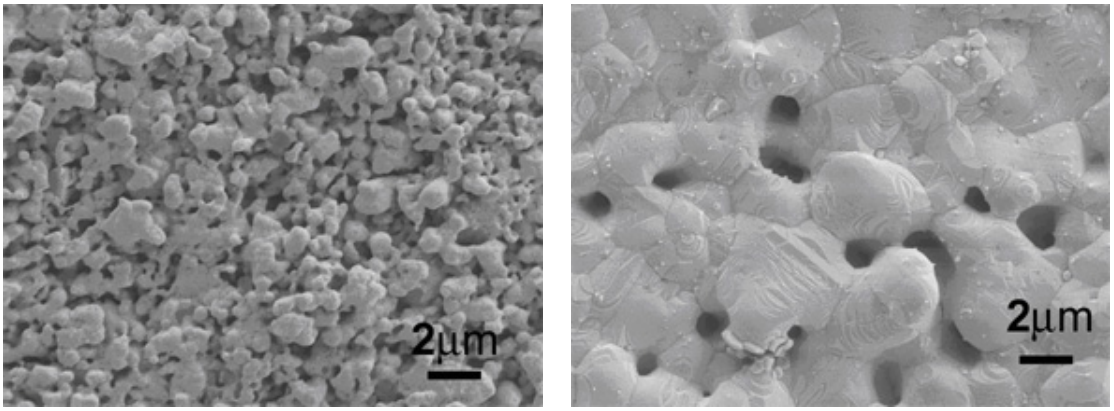


Figure 3.14. Comparison of electrical resistivity of several possible materials for semiconductor device interconnection.



(a) (b)

Figure 3.15. The microstructure evolution of the nano-silver paste before (a) and after (b) the heat treatment during the electrical resistivity measurement.



(a) (b)

Figure 3.16. The microstructure evolution of the microscale silver paste before (a) and after (b) the heat treatment during the electrical resistivity measurement.

After we plot values of electrical conductivity of the common used interconnect materials at the room temperature (25°C) with those of our low-temperature sintered nanoscale silver in Figure 3.17, one can see that the low-temperature sintered silver have obvious advantages since it has 3~4 times electrical conductivity of the solders and the value is substantially higher than the conductive epoxies.

The high electrical conductivity of the low-temperature sintered nanoscale silver makes it a potentially excellent interconnecting material with high current handling capability and enhanced electrical performance. Furthermore, since the low-temperature sintered silver has a relatively stable resistance up to 650°C, it is a potentially good candidate for high-temperature electronic packaging applications.

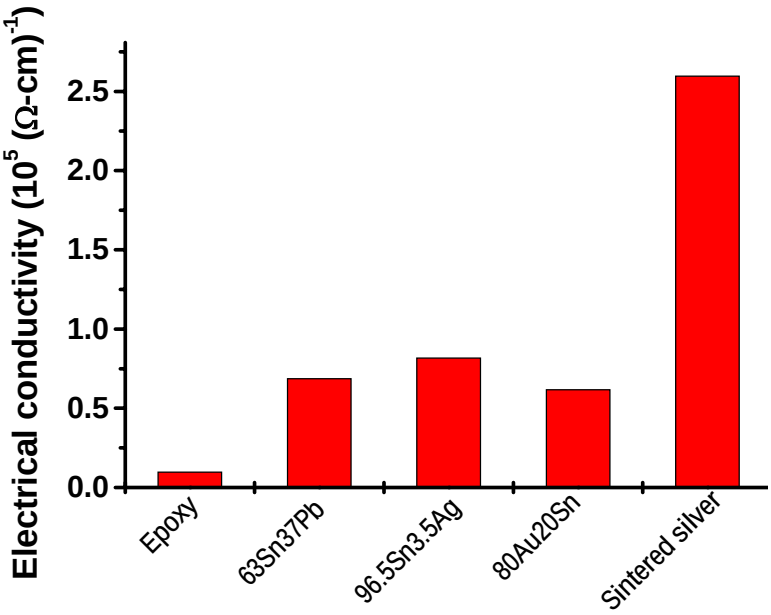


Figure 3.17. Comparison of electrical conductivity values of the common-used interconnecting materials with that of the sintered silver.

3.1.2 Thermal Properties

Thermal conductivity is another very important parameter for power packaging since the thermal resistance of the interconnections is directly related to the heat removal capability and thermal management of the power package. To determine the thermal conductivity of the low-temperature sintered silver, the density, specific heat, and thermal diffusivity of the material have to be known.

The density of the low-temperature sintered nanoscale silver is about 80% of the density of the bulk silver. It is because the low-temperature sintered silver is still in its intermediate sintering stage and it has microscale pores trapped in. Actually the value could vary between 75-85% dependent on the sintering materials and parameters. We used the samples with about the average values for the thermal property determination.

The data of specific heat of the low-temperature sintered silver are listed in Table 3.1. It can be seen that the specific heat of the sintered silver has about the same specific heat with bulk silver (bulk silver has a specific heat of 0.235 J/g-K at room temperature from Ref. [7]). The results of specific heat provided other evidence that the most organic components had been removed and the low-temperature sintered silver was almost pure

silver. Or else the specific heat of the organic components should be quite different from that of silver.

Table 3.1. The values of specific heat of the sintered nanoscale silver paste at different temperatures. Tabulated data has been compared to reference data for sapphire.

	25°C	30°C	40°C	50°C
Sample I	0.233 J/g-K	0.235 J/g-K	0.236 J/g-K	0.237 J/g-K
Sample II	0.233 J/g-K	0.235 J/g-K	0.236 J/g-K	0.238 J/g-K

The data of determined thermal diffusivity are plotted in Figure 3.18. After the 280°C low-temperature sintering, the thermal diffusivity of the sintered silver is ~1.19 cm^2/s at room temperature. The thermal diffusivity of silver could increase a little bit to ~1.32 cm^2/s after 400°C annealing for about 30 mins. The former values are around 70% of that of bulk silver at the room temperature.

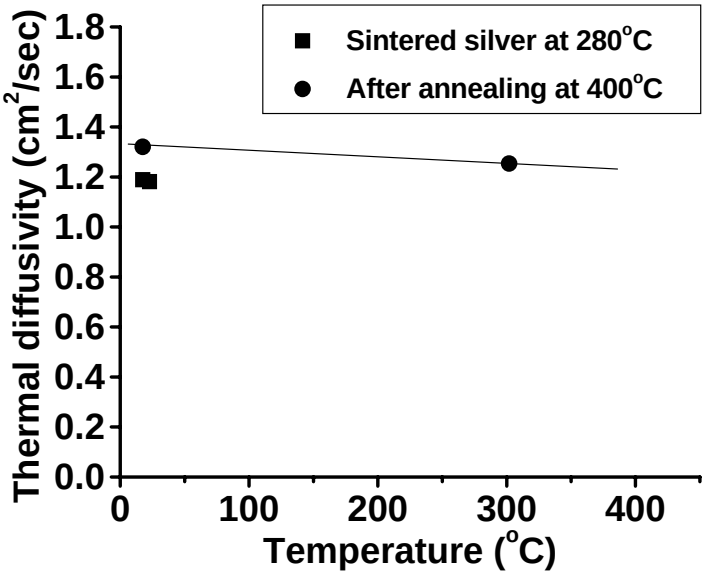


Figure 3.18. Data plot of thermal diffusivity of the low-temperature sintered silver versus temperature.

Room temperature (25°C) values of the density, specific heat, thermal diffusivity, and thermal conductivity of a 280°C-sintered silver are listed in Table 3.2. For reference, the values for bulk silver are also listed. The sintered silver has a relative 82% density, 99% specific heat, 68% thermal diffusivity, and 55% thermal conductivity of bulk silver. However, as shown in Figure 3.19, the thermal conductivity of the sintered silver is still much higher than those of the solder alloys that are most commonly used for interconnecting power semiconductor devices. For example, the thermal conductivities of the 63Sn37Pb, 96.5Sn3.5Ag and Au80Sn20 are 0.51, 0.60 and 0.58 W/K-cm,

respectively. The thermal conductivity of the sintered silver is also much higher than that of conductive epoxy. This means our low-temperature sintered silver has much better heat removal capability than those of currently used interconnect solders and conductive epoxies.

Table 3.2. Thermal properties of the sintered nanoscale silver paste and those of bulk silver.

	Density ρ (g/cm^3)	Specific heat c (J/g-K)	Diffusivity α (cm^2/s)	Conductivity κ (W/K-cm)
Sintered silver	8.58	0.233	1.19	2.38
Bulk silver*	10.5	0.235	1.74	4.29

*Data from www.matweb.com.

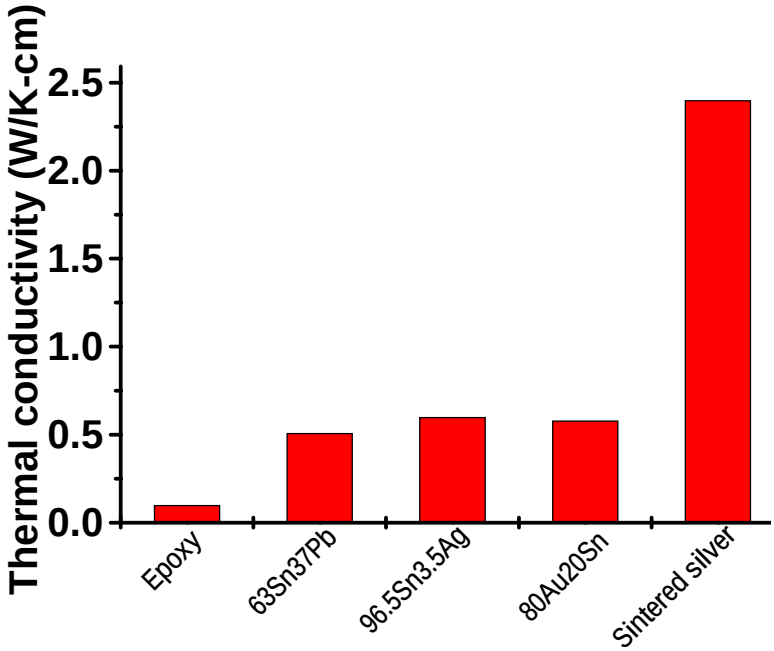


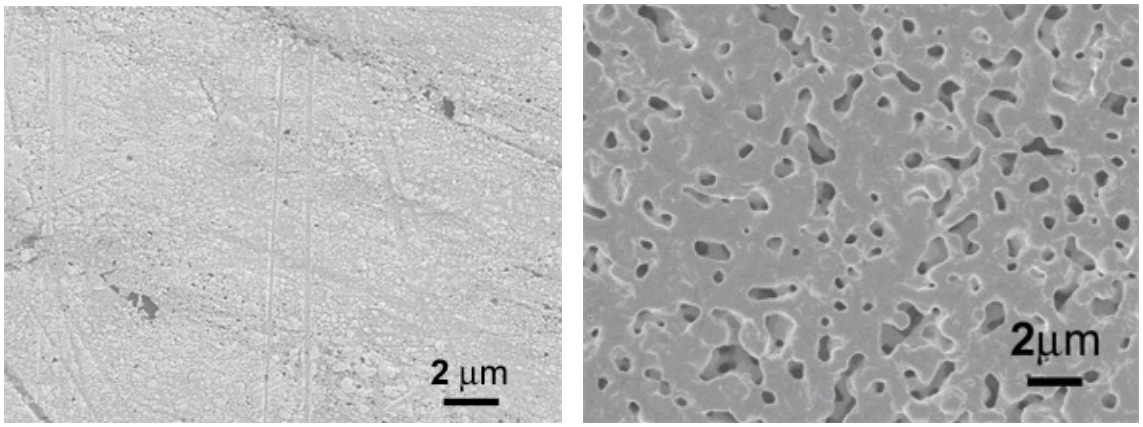
Figure 3.19. Comparison of thermal conductivity values of the common-used interconnecting materials with that of the sintered silver.

Finally, Wiedemann-Franz law [8] says that for a pure metal, the ratio of thermal to electrical conductivity is given by:

$$\frac{\kappa}{\sigma} = \frac{\pi^2}{3}\left(\frac{k_B}{e}\right)^2 T = LT \tag{3.1}$$

Where Lorenz number L is a constant of $2.45\times10^{-8}\ W\Omega/K^2$ theoretically. For the bulk silver at the room temperature, the experimental data is $2.31\times10^{-8}\ W\Omega/K^2$. While for our low-temperature sintered silver, the number is about $3.0\times10^{-8}\ W\Omega/K^2$. The difference is believed due to the microstructure difference in the sample for the thermal and electrical conductivity measurements as shown in Figure 3.20. Although the two samples have a

similar density (both about 80% of bulk silver), their microstructures are quite different because of the different sample preparation methods. Specifically, the disc samples for determining thermal conductivity were molding-sintered, a case similar to covered and free sintering. It resulted in less porosity but relatively more organic components left in the microstructure. While the samples for electrical conductivity determination were constraining-sintered on alumina substrates in an open-air environment. It resulted in relatively more porosity but less organic components left.



(a) (b)

Figure 3.20. Comparison of surface microstructures of the polished samples for the thermal conductivity measurement (a) and those for the electrical conductivity measurement (b) (non-polished).

3.1.3 Mechanical Properties

Elastic modulus and coefficient of thermal expansion (CTE) are two important mechanical properties of for the interconnect materials. Because both of them are directly related to the thermal stress level that could induced in the joint. The stress level in a joint are associated with the reliability of the joint structure directly.

From the stress-strain curve of the silver bands as shown in Figure 3.21, the apparent elastic modulus, the tensile strength, and the 0.2% offset yield strength were determined. First, the apparent elastic modulus of the sintered silver was determined to be about 9 GPa by taking the steepest slope of the curve (Step (1) in the figure). Secondly, the tensile strength was determined to be about 43 MPa by reading the maximum stresses before failure (Step (2) in the figure). Finally the 0.2% offset yield strength was estimated to be about 43 MPa by off-setting the steepest portion of the stress-strain curve to the 0.2% strain value (Step (3) in the figure).

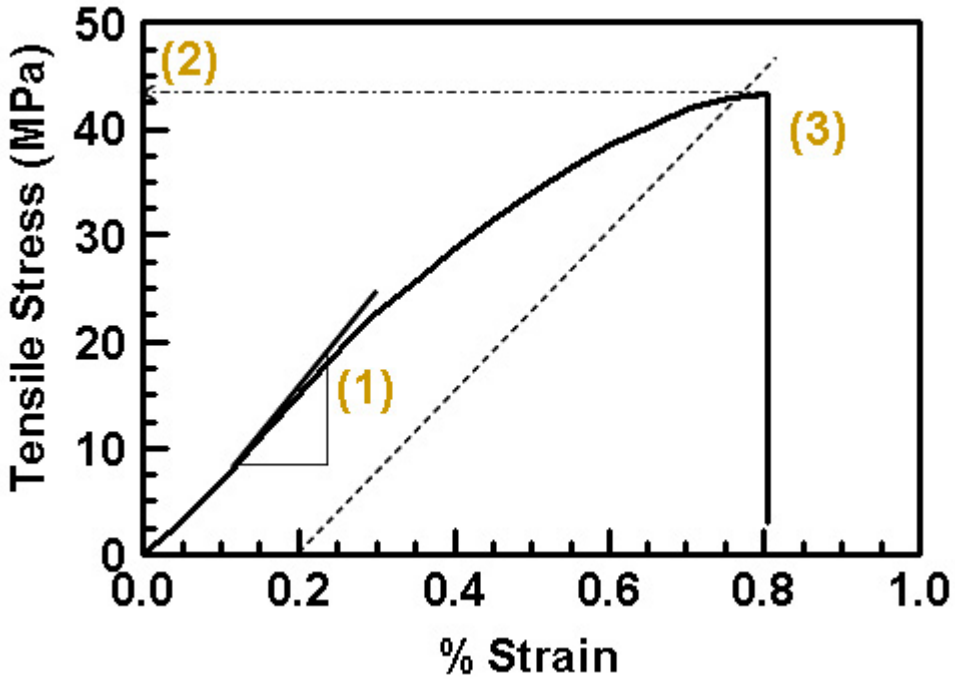


Figure 3.21. A typical stress-strain curve of the sintered silver in the tensile test.

The low apparent elastic modulus could be explained by the porosity of the sintered silver. The phenomena were also observed in other paste systems such as gold [5]. Porous material had a lower mechanical modulus than the corresponding bulk material [9]. As a result, the sintered porous silver had only about 12% of the elastic modulus of bulk silver and the number was also smaller than those of most solder alloys such as eutectic lead-tin at room temperature as shown in Figure 3.22.

Continuous thermal expansion data versus temperature are plotted in Figure 3.23. The CTE of sintered silver was about 19 ppm/°C, almost the same as that of bulk silver. The CTE of the silver was obtained by the slope of linear portion of the sample thickness changes–temperature curve in Figure 3.23. The CTE of the sintered silver provided other evidence that almost all the organic components were gone due low-temperature sintering, otherwise the organic components in the sintered silver are expected to have a different CTE with bulk silver.

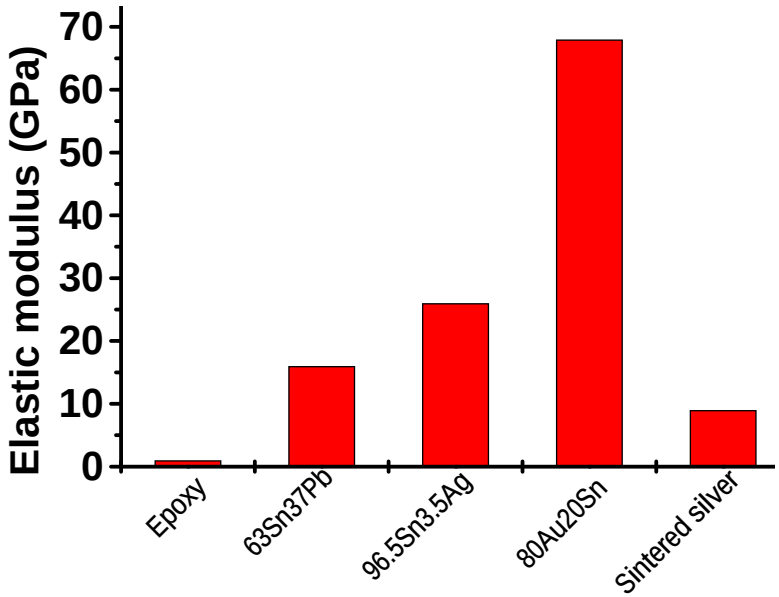


Figure 3.22. Comparison of elastic modulus values of common-used interconnecting materials with that of the sintered silver.

The low-temperature sintered silver had the yield strength similar to the failure strength because of the large amount of pores in the sintered structure. As a result, the porous silver quickly failed after reaching its yield point.

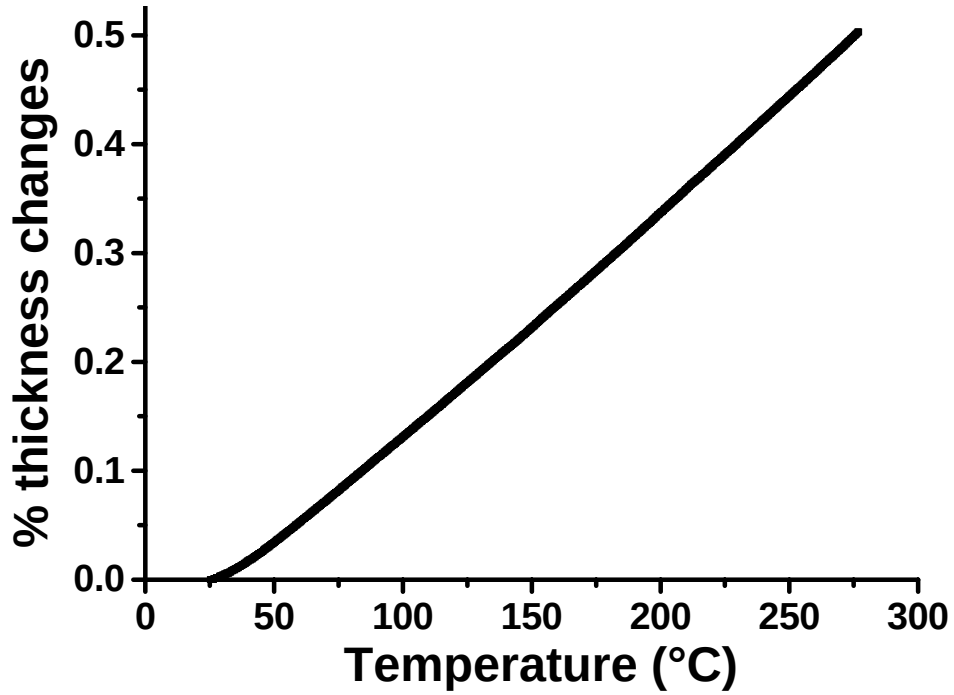


Figure 3.23. A typical thickness change-temperature curve of the quartz dilatometry test.

Finally, for a semiconductor device-metallized substrate interconnection, a softer interconnecting material can be advantageous since it transfers less of thermal stresses

due to the semiconductor-metal CTE mismatch. Using this argument, sintered silver has superb thermomechanical properties and will help achieve a more reliable semiconductor-metal interconnection. The argument is also supported by a comparison of finite element analysis (FEA) as shown in Figure 3.24. In the FEA, a SiC device measured 2×2 mm^2 was assumed to die-attach to an AlN DBC substrate either using the high-temperature gold-tin solder or using our low-temperature sintered silver. After plugging in the necessary mechanical properties of the gold-tin solder and the sintered silver, it is found that the sintered silver induces much lower thermal stress level than that of the gold-tin solder at the same temperature changes. Since the lower thermal stresses in a packaging structure usually mean higher performance and higher reliability, the simple comparison demonstrates that the low-temperature sintered silver has advantages due to its lower apparent elastic modulus.

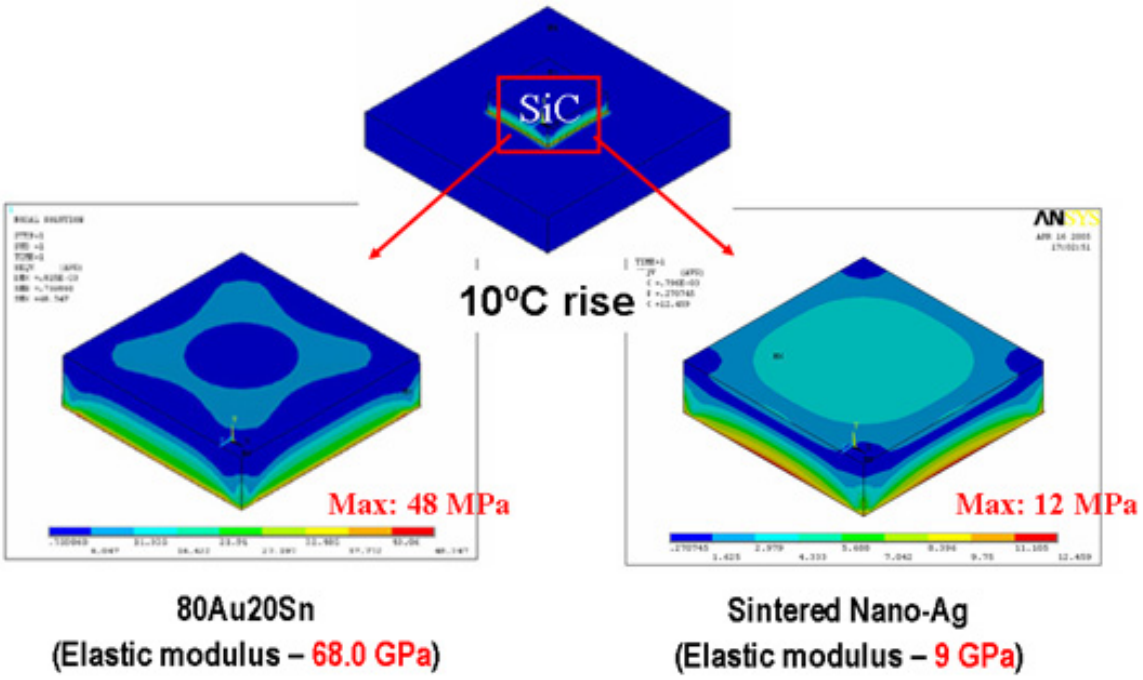


Figure 3.24. A finite element analysis shows that the sintered silver induces less thermal stresses than those of gold-tin solder.

Direct evidence is also shown from the curvature experiment. Figure 3.25 shows the data plots of the position changes in the photodetector versus the scanning distance. From the slopes *m* of the data plots, the curvatures *1/R* of the silver and silicon composite are determined by

$$\frac{1}{R} = \frac{m}{2l} \tag{3.2}$$

The optical path l in the experiment is measured to be 927 mm. The determined curvatures and stresses in the sintered silver film at both 250°C and 25°C are list in Table 3.3.

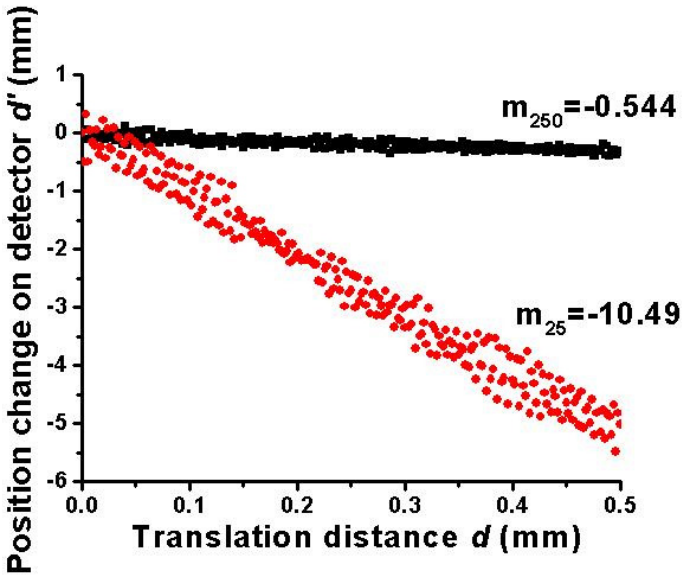


Figure 3.25. The date plot of the position changes in the photodetector versus the scanning distance from the curvature experiment.

In Table 3.3, the positive values of the stress means the sintered silver film is under tension at both 25°C and 250°C temperatures. This is easy to understand because the sintering temperature is 280°C, at which point the silver film-silicon substrate composite is about stress-free. At lower temperatures, the sintered silver films tend to shrink more than the silicon substrates, while the silicon substrate will hold on the shrinkage. Thus the sintered silver films are under tension stresses. Furthermore, the induced stress values are relatively small considering the big range of the temperature changes.

Table 3.3. The determined curvature and stress values from the curvature experiment.

	25°C	250°C
Curvature $1/R$ (m^{-1})	5.66	0.293
Stress σ_f (MPa)	+21.3	+1.11

If we use the mechanical property values of the silver film and the silicon substrates as listed in Table 3.4 and only leave the elastic modulus of the silver film for determination and assume all the values are constants at the interested temperature range

(25-250°C), we can get an estimation of the elastic modulus of the sintered silver using Equation 2.8. The value of the elastic modulus of the sintered silver films is estimated to be around 7 GPa by this way. This value is not very far from the direct determination. Later on we use 9 GPa for the effective elastic modulus of the low-temperature sintered silver.

Table 3.4. The mechanical property values of the sintered silver films and silicon substrates.

	Elastic modulus	Poisson's ratio	Coefficient of thermal expansion
Sintered silver films	Left for determination	0.37 (use bulk value)	19 ppm (exeperimentally measured)
Ultrathin silicon substrates	150 GPa	0.17	3 ppm

3.1.4 Summary

Properties of the sintered nanosilver paste along with those of other interconnect materials are summarized in Table 3.5. It is useful to compare all the interconnect materials from a combination of all the electrical, thermal and mechanical properties. In most of the relevant material properties, the low-temperature sintered silver behaves much better compared to the other interconnect materials. For example, the density of the sintered silver is not very high and its processing temperature is also low enough to bond most power semiconductor devices. Both the electrical and thermal conductivities of the sintered silver are 3-5 times those of the solders and much higher than that of the conductive epoxy. The effective elastic modulus of sintered silver is smaller than even the soft solders although the value is larger than that of the epoxy. The yield and tensile/shear strengths are high to form strong enough bondings. Finally, the CTE of the sintered silver is comparable with those of solders and epoxies.

Furthermore, the low-temperature sintered silver has some other fundamental advantages compared with the other common-used interconnect materials. First, the bonding mechanism of the silver joint is solidus sintering and interdiffusion, this unique property makes it free of the die-swimming problems. Secondly, the processing temperature of the silver sintering is far below the melting point of the bulk silver, which makes the serial process possible. Thirdly, the pure silver composition of the low-temperature sintered silver makes it has no phase segregation problems and thus

possesses potentially high reliability. Finally, the very high maximum use temperature of the sintered silver makes it more favorable for high-temperature applications.

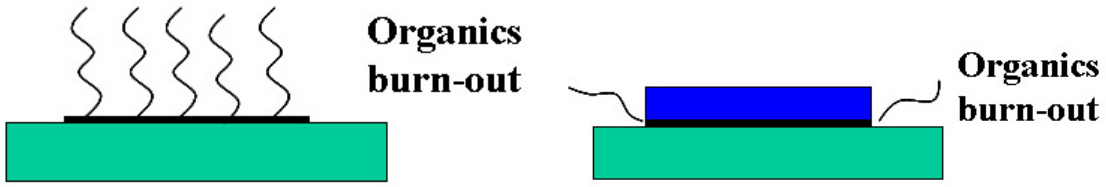
Table 3.5. Property comparison of some commonly used solder alloys with our low-temperature sintered silver pastes.

	Eutectic lead-tin solder	Lead-free solder	Eutectic gold-tin solder	Conductive Epoxy	Nanosilver paste
Bonding mechanism	Liquidus reflow	Liquidus reflow	Liquidus reflow	Epoxy curing	Sintering/solidus interdiffusion
Peak process temperature	214°C	260°C	320°C	~150°C	280-300°C
Composition	Pb37Sn63	Sn96.5Ag3.5	Au80Sn20	Silver filler and organic resin and hardener	Pure silver (>99.8 wt.%)
Maximum use temperature	<180°C	<220°C	<280°C	<150°C	<960°C
Electrical conductivity	0.69×10^5 $(\Omega\text{-cm})^{-1}$	0.82×10^5 $(\Omega\text{-cm})^{-1}$	0.62×10^5 $(\Omega\text{-cm})^{-1}$	$\sim0.1\times10^5$ $(\Omega\text{-cm})^{-1}$	2.6×10^5 $(\Omega\text{-cm})^{-1}$
Thermal conductivity	51 (W/K-m)	60 (W/K-m)	58 (W/K-m)	~0.1 (W/K-m)	240 (W/K-m)
Coefficient of thermal expansion	25 (PPM/°C)	22 (PPM/°C)	16 (PPM/°C)	~25 (PPM/°C)	19 (PPM/°C)
Elastic modulus	16 GPa	26 GPa	68 GPa	<1 GPa	10 GPa
Yield Strength	27 MPa	22.5	N/A	N/A	43 MPa
Tensile strength	27 MPa	52 MPa	275 MPa	~10 MPa	43 MPa

3.2 Performance of Sintered Silver Joints

The preparation of low-temperature sintered silver joints has to involve the covered sintering as illustrated in Figure 3.26. In the case of covered sintering, the sintering of silver is more difficult than the open-air case due to the problems of organic component burnout and the oxygen diffusion. As discussed in Chapter 2, if the organic cannot burn out, the nanoscale silver paste cannot be sintered. This phenomena is clearly shown from a half-inch thick copper rod surface as shown in Figure 3.27, the middle part (dark colored) of the debonded silver layer, a lot of organic is still left and the paste is not sintered. However, at the edge of the debonded surface, the organics have burn out and paste is sintered. Figure 3.28 reveals the clear difference in the microstructures of the unsintered nanoscale silver with those of the sintered paste. In the unsintered paste, the nanoscale silver particles in the paste are still maintained as shown in Figure 3.28(a). But

in the sintered paste, obvious grain growth and densification are observed as shown in Figure 3.28(b). Another side-effect is that the unsintered silver cannot reach a full bonding strength as shown in Figure 3.20. Actually the silver joint in this case was debonded at only about 4 MPa, ten times lower than the full strength.



(a) (b)

Figure 3.26. The organic components are more difficult to burn out in covering case (b) than in the open-air case (a).

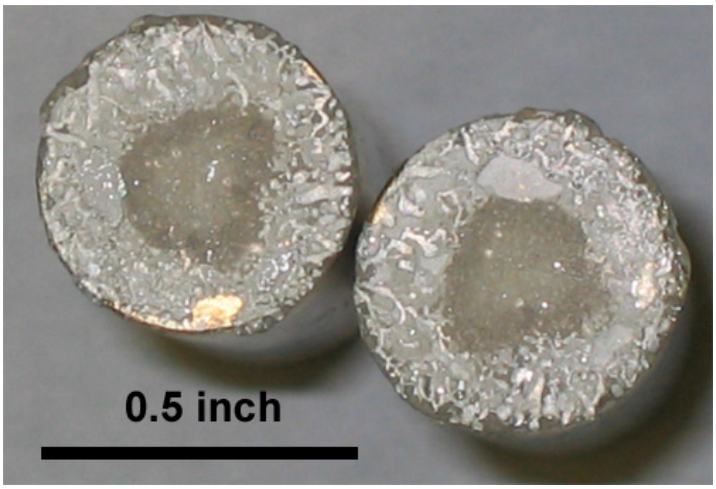
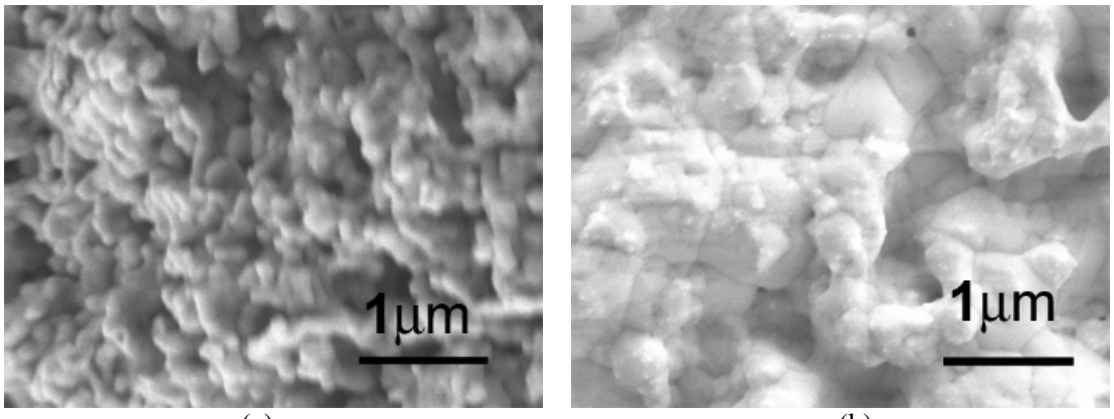


Figure 3.27. Low-temperature sintered silver at half-inch thick rod surfaces after debonding.

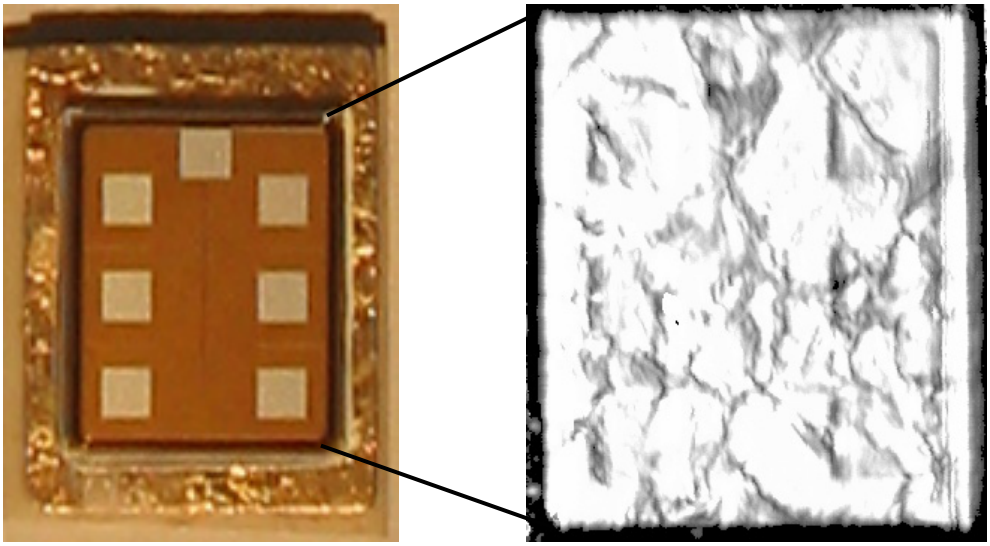


(a) (b)

Figure 3.28. The comparison of the microstructures of unsintered silver (a) with those of sintered silver (b).

Scanning acoustic microscopy (SAM) can also reveal the covered-sintering problems from the large-area solder joints. Figure 3.29(a) shows a silicon power IGBT

device (IXSD35N120A, IXYS Corporation, Santa Clara, CA) with a size of 8.91×7.22 mm^2 that are bonded to a gold-coated DBC using the low-temperature silver sintering. It is found that the silver is unsintered like that in Figure 3.27 and the SAM picture in Figure 3.29(b) shows that the unsintered silver cannot form a uniform bonding. These results are quite different from the sintered silver joints that will be discussed later.



(a) (b)

Figure 3.29. The silver sintering die-attached power IGBT with a size of 8.91×7.22 mm^2 (a) and its SAM image (b).

To avoid the unsintering problem in the covered-sintering situation, one of the effective strategies is to reduce the organic loadings (thus increase the silver loadings) to enhance the silver paste sintering. This is because less organic loading allows less organic burnout time. These phenomena are clearly shown in Figure 3.30. To uncover the effects of the silver loading in the covered-sintering, transparent glass slides with size of 4×4 mm^2 were used to cover the sintering paste. After the same sintering profile (10-min dwell at 300°C), the organic components in the 84 wt.% silver paste were burned out and the paste was sintered as shown in Figure 3.30(b), however, the 78 wt.% silver paste left lots of organics and was not sintered as shown in Figure 3.30(a). The higher silver-loading pastes contained less organic components that needed to be burn out, so they could be sintered more easily in the covered sintering case. However, in open-air sintering, the effects of different silver loadings were not so evident because in that case the organic components were much easier to remove.

(a) (b)

Figure 3.30. The 78 wt.% (a) and 84 wt.% (b) silver paste sintering under the 4×4 mm^2 glass slide coverage after 10-min dwell sintering at 300°C.

Another experiment was also done to evaluate the effects of covering size on the low temperature sintering. The 84 wt.% silver-loading paste was used in the study. The glass slide in Figure 3.31(a) was measured by 6×6 mm^2 while that in (b) was only 3×3 mm^2. It was found that nanoscale silver paste under the 3×3 mm^2 glass slide in (b) could be completely sintered after only about 5-min dwell at 300°C. However, the silver paste under the 6×6 mm^2 slide needed much longer time. Both pictures in Figure 3.31(a) and (b) were taken after a 5-min dwell at 300°C. One can see that the middle part of the covered silver paste under the larger glass slide still had organics left and had not been sintered yet. The incomplete sintering phenomena in a larger bonding were similar with those in the copper rod debonding tests. Therefore, the second strategy to enhance the burnout of organics and thus the silver paste sintering was to use the small patterns as illustrated in Figure 3.31 for large area silver bondings. The air gaps between the small silver paste patterns would allow oxygen diffusion and organic burnout. This strategy could be even better if it was combined with an oxygen-enriched sintering method.

(a) (b)

Figure 3.31. The 84 wt.% silver paste sintering under a 6×6 mm^2 glass slide (a) and that under a a 3×3 mm^2 glass slide coverage after 5-min dwell at 300°C.

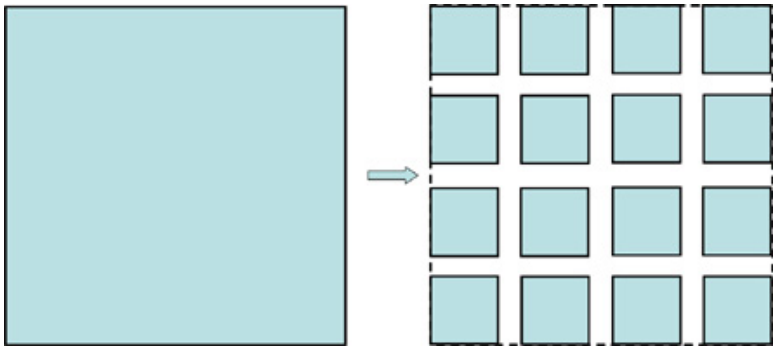


Figure 3.32. Illustration of using small patterns for the enhancement of organic burnout and paste sintering for large area silver bonding.

The third strategy could use is to bake the covered partially burnout of organics before placing the power devices. However, there is disadvantageous in this strategy. With the baked silver paste, the attaching device will be more difficult to achieve a 100% initial contact since the original organic components in the silver paste help to achieve a good "wetting" situation during the die-attachment. The 100% initial contact is a prerequisite for the interdiffusion during sintering and thus it is very important for the formation of a uniform and strong silver bonding.

The fourth strategy is to sinter the silver paste in an oxygen environment since oxygen can enhance the organic burnout and thus the sintering of the silver. The oxygen source can be from outside or inside. However, in the case of covered-sintering, the oxygen source from the outside cannot help much because the coverage. It would be advantageous if we could introduce an extra oxygen source from the inside of the silver paste during the sintering. The oxygen agent in the silver paste must have the following properties:

(1) The oxygen agent should not be harmful to the environment (for example it should not be toxic). Otherwise it is not a favorable candidate.

(2) The oxygen agent must decomposite and provide oxygen at around the temperatures for the organic component burnout and the sintering. If the decomposition temperature is too high, the agent cannot serve as the extra oxygen source during the low-temperature sintering.

(3) After the decomposition of the oxygen agent, the residue of the agent should not have negative side-effects on the sintered silver joints for their applications. Otherwise the addition of the agent is not favorable.

After the considerations of the above prerequisites for the selection of an oxygen agent, there is not much freedom left anymore. The possible candidates for the oxygen agents that could be added into nanoscale silver will be discussed in Chapter 5.

The last strategy could take is to use higher temperature and prolonged sintering profile. For these purpose, a sintering profile with 40-min dwell at 300°C was designed for sintering of the silver joints with an area of 4×4 mm^2 or under. The sintering profile is plotted in Figure 3.33. The sintering profile was designed not only for the sintering enhancement, but also for the full bonding strength development as discussed later.

In the following sections, the characterization results of the electrical, thermal, and mechanical performance of the low-temperature sintered silver joints are presented. The characterization is based on the assumption that the organic components in the silver joints have been burned out and the silver paste is sintered. This is assured by following the sintering profile as shown in Figure 3.33 for the silver joints smaller than 4×4 mm^2. Also, the electrical, thermal, and mechanical performance of the silver joints is often evaluated indirectly as discussed below, when the direct measurements are impossible.

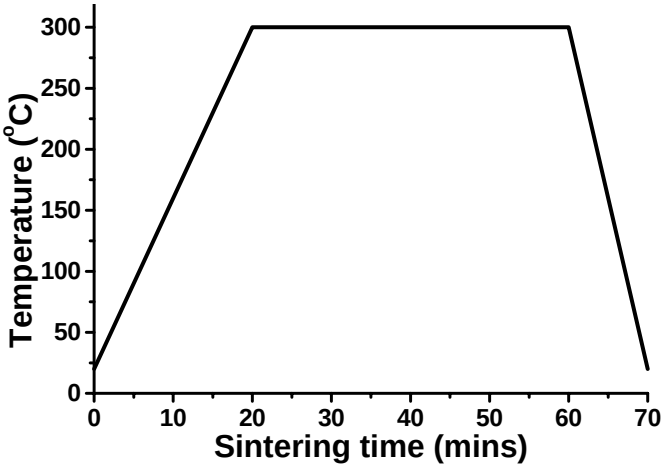
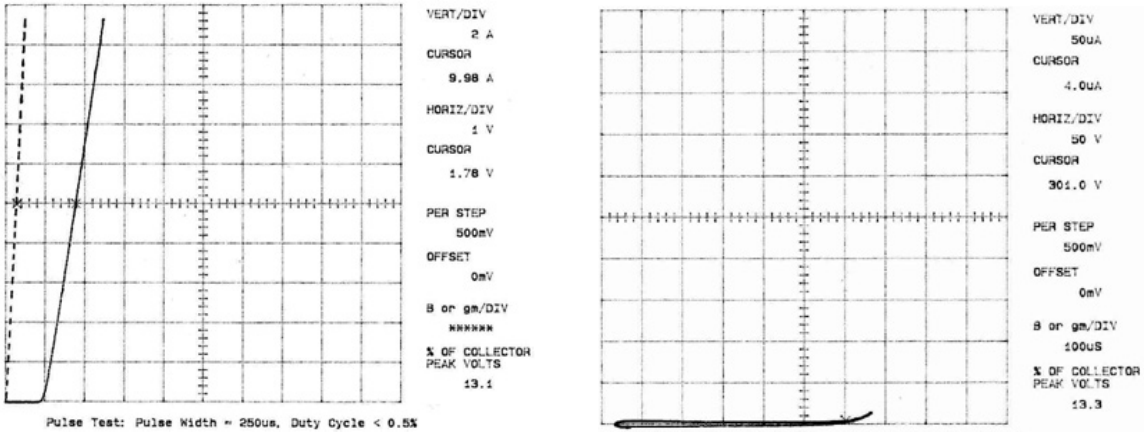


Figure 3.33. The sintering profile for achieving enhanced sintering and high bonding strength for the silver joints with size 4×4 mm^2 or below.

3.2.1 Electrical Performance

Figure 3.34 shows the typical forward and backward I-V curves obtained from the sintered silver die-attached Infineon SiC devices. In Figure 3.34(a), the forward curves were tested up to 20A, which was two times of the datasheet rating of the devices. The forward voltage (the solid line) was 1.78 V at the datasheet current rating 10 A, which

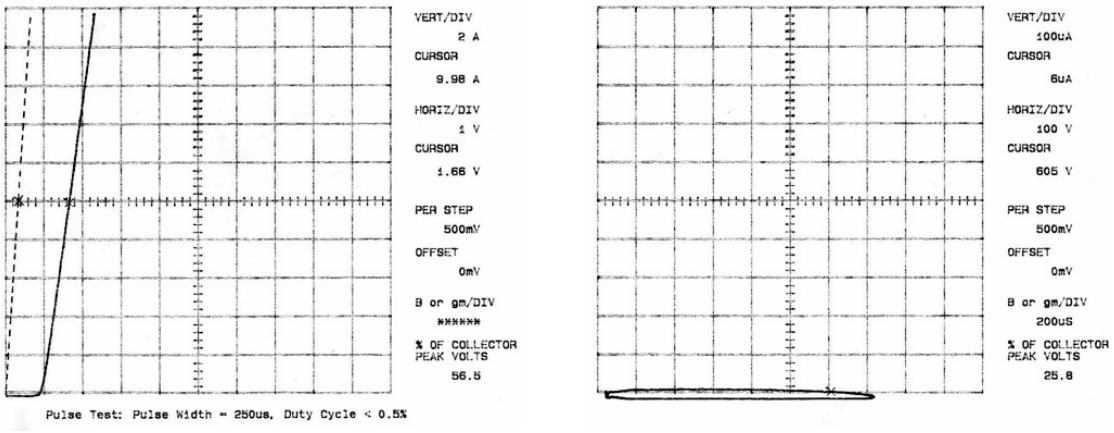
was higher than the datasheet value of 1.50 V. But after subtraction of the corresponding voltage drop due to the fixture (the dashed line), the net forward voltage drop of the Infineon devices was 1.49 V at 10 A, which was compatible with the datasheet value. The leakage current at the breakdown voltage of the devices was 4.0 μA as in Figure 3.34(b), which was also consistent with the datasheet value.



(a) (b)

Figure 3.34. Forward (a) and reverse (b) I-V curves obtained from the Infineon devices. Dashed curve in (a) is due to the test fixture.

The forward and backward I-V characteristics are also obtained from the silver die-attached CREE SiC devices and they are as shown in Figure 3.35. After taking into account of the voltage drops from the test fixture, the net forward voltage drops of the CREE device are also small.



(a) (b)

Figure 3.35. Forward (a) and reverse (b) I-V curves obtained from the CREE devices. Dashed curve in (a) is due to the test fixture.

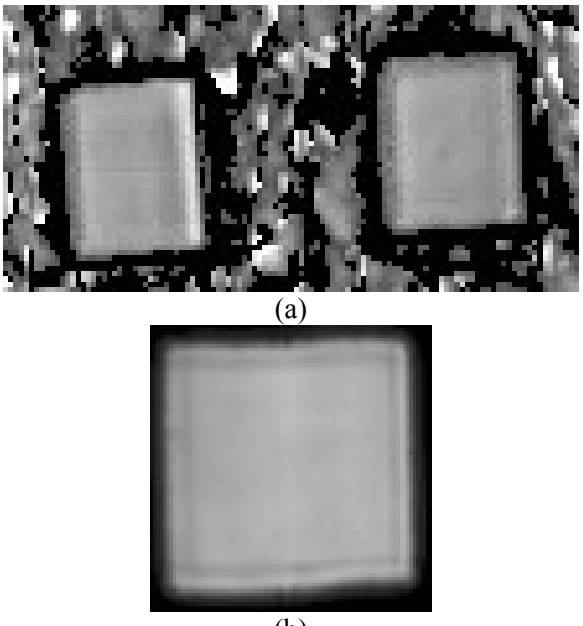
All of the measurement results are summarized in Table 3.6. The small forward voltage drops in the both silver bonded power devices are beneficial for the device applications.

Table 3.6. The static curve tracer test results of the two types of SiC devices.

Chip type	Forward voltage drop at standard forward current	Reverse leakage current at breakdown
Infineon SIDC24D30SIC3	1.49 V (10 A)	4 μA (at 300 V)
CREE CPWR-0600S010C	1.37 V (10 A)	6 μA (at 600 V)

3.2.2 Thermal Performance

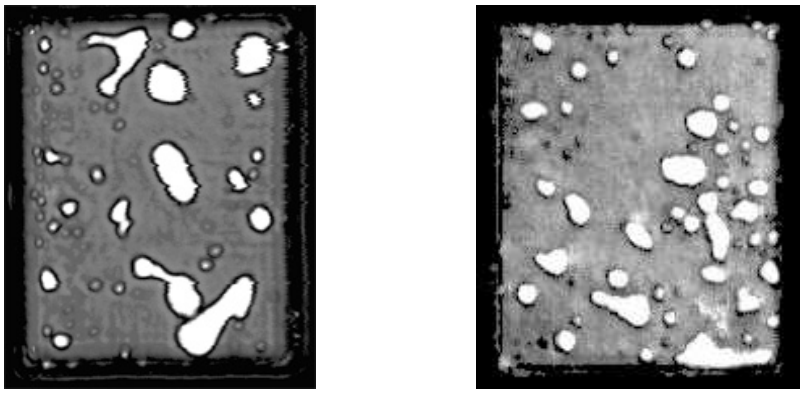
Figure 3.36 shows the SAM images got from two of the silver bonded Infineon devices at the silver joint interfaces and that from a CREE device. All the silver joints do not have large voids/low-density areas that could occur in the reflowed solder joints [10], which are clearly shown in Figure 3.37. These results are also very different from that in Figure 3.29. Because the silver joints are constructed by solidus diffusion, extensive redistribution of material like that in liquidus solder reflow does not occur. The pore size of the sintered silver layers is usually limited to microscale.



(a)

(b)

Figure 3.36. SAM images of the sintered silver joints between the SiC devices and the gold-coated DBC substrate. (a) from the Infineon devices measured of 1.706 × 1.38 mm^2 and (b) from the CREE devices measured of 2.26 × 2.26 mm^2.



(a) (b)

Figure 3.37. The initial void problems in the reflowed die-attaching solder layers (a) lead-tin solder and (b) lead-free solder.

Since large voids are avoided from the sintered silver joints, thermal management of the attached high-temperature devices is expected to be much better because of the elimination of non-uniform heating during the device operation. The SAM is unable to resolve the microscale pores in the sintered silver.

3.2.3 Mechanical Performance

Figure 3.38 shows the bonding strength development of the silver joints with the change of dwell time during the sintering. The results were obtained by die shearing-off tests and they indicated that an enough sintering time was important for the full bonding strength development. As shown in Figure 3.39, when the sintering time was not long enough, the debonding was more likely to happen at the silver-silver interface, which was associated a weaker bonding strength. However, when the sintering dwell time was longer than 40 mins, the bonding strength of the silver-silver joint reached the failure strength of the sintered silver itself, which was about 40 MPa (this was a value similar to the tensile strength as shown in Figure 3.21), the bonding strength would not increase anymore. The failure mechanism was changed from the coherent failure (i.e., the failure at the bonding interface) to the inherent failure (i.e., the failure in the bonding silver layer itself). As shown in Figure 3.38, it usually took about 40-min dwell at 300°C for the silver-silver bonding to build its full strength, while the gold-silver bonding needed much longer time. The big difference in the shear strengths and their development obtained on gold- or silver-coated substrates could be explained by the faster self-diffusion of silver

than the interdiffusion between silver and gold. This was also why we chose a sintering profile with 40-min dwelling time.

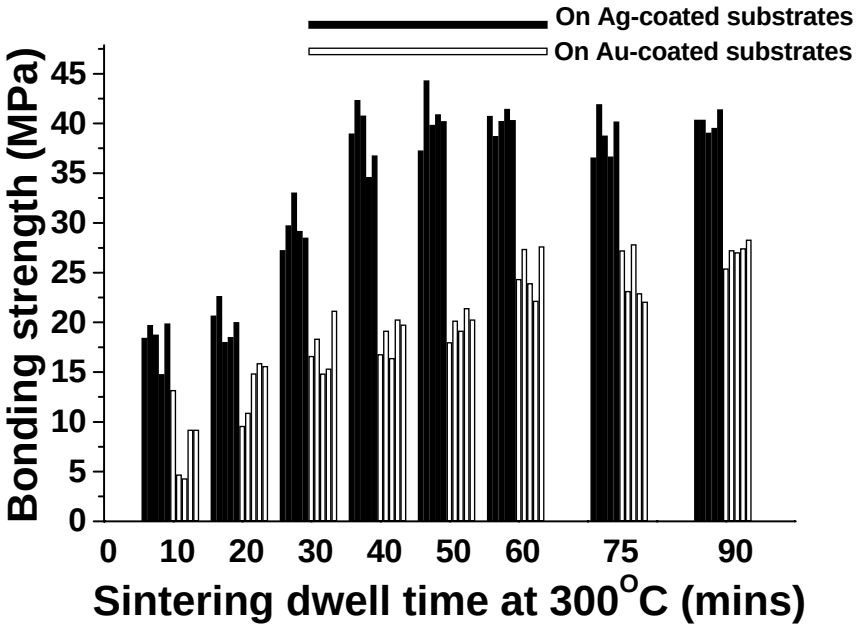
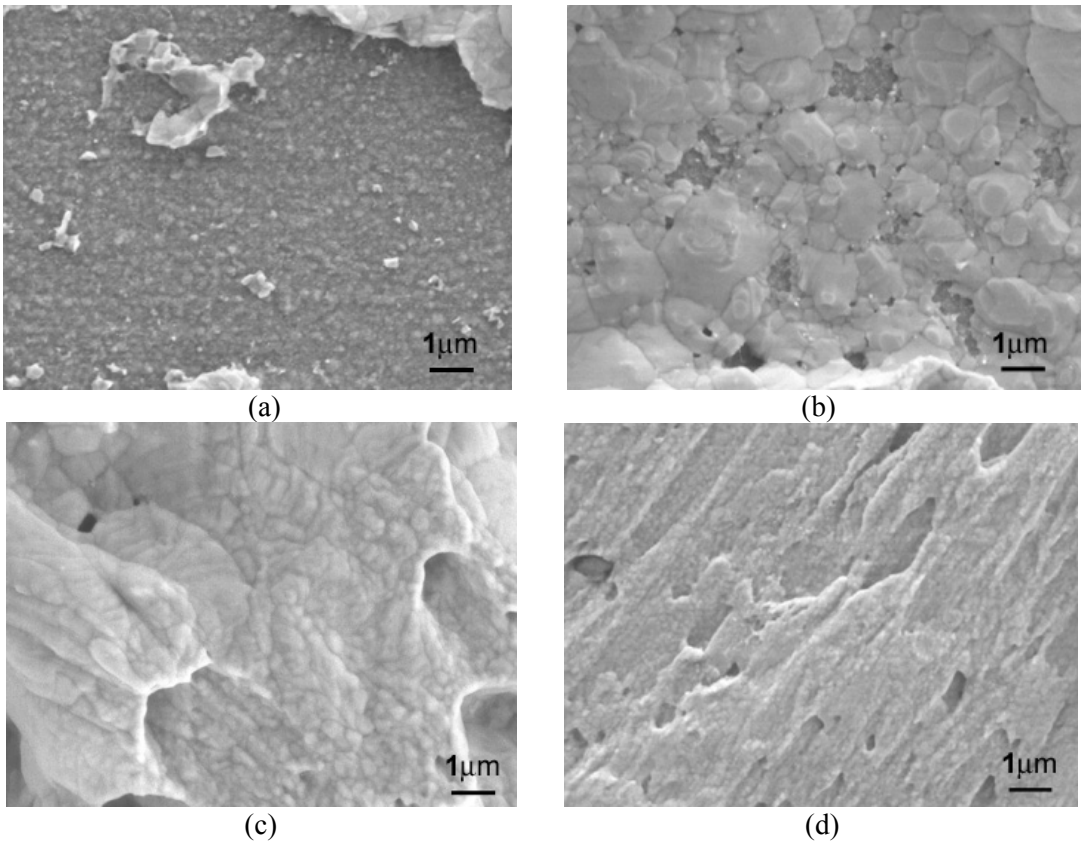


Figure 3.38. The bonding strength development versus the sintering dwell time.



(a) (b)

(c) (d)

Figure 3.39. Microstructures of the debonded sintered silver joints on the silver-coated SiC devices after dwelling sintering at 300°C for (a) 10 mins, (b) 20mins, (c) 40mins, and (d) 60 mins.

After sintering the silver joints with a 40-min dwell time at 300°C, another set of the die-shear test results from the Infineon SiC devices attached using different bonding materials and DBC substrate metallizations are shown in Figure 3.40. The shear strengths on the gold-coated DBC substrates are around 21 MPa; while those on the silver-coated substrate are significantly higher at around 38 MPa. Again one can see that the shear strength of the sintered silver joints on the silver-coated substrates is already comparable to the failure strength of the low-temperature sintering material (43 MPa). This means the full bonding strength has been developed. The fully developed silver-silver bonding strength is also comparable to that of reflowed solder joints.

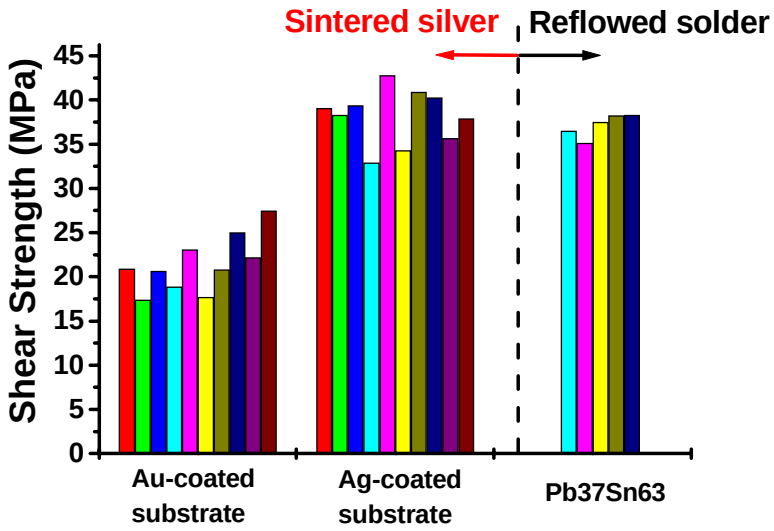
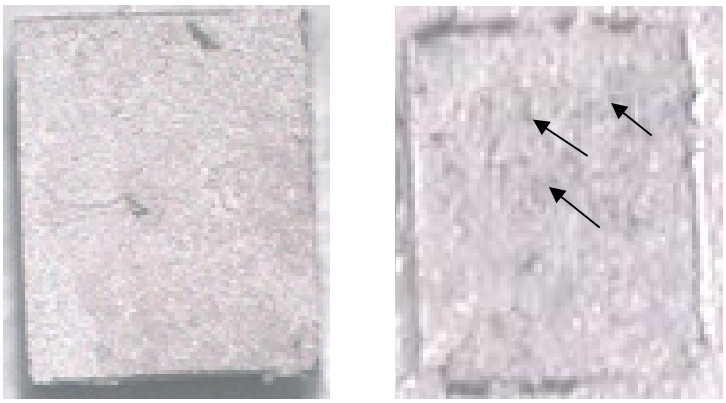


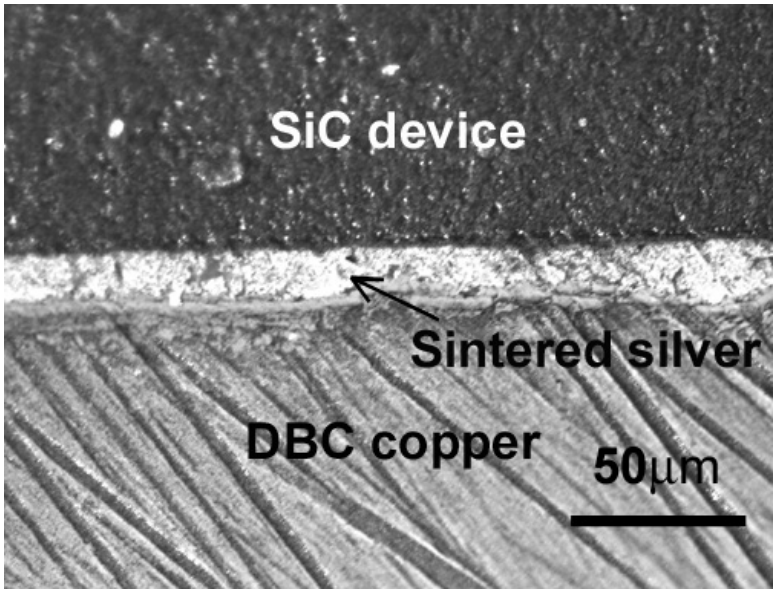
Figure 3.40. The comparison of the shear strength of the low-temperature sintered silver with that of the reflowed solder.



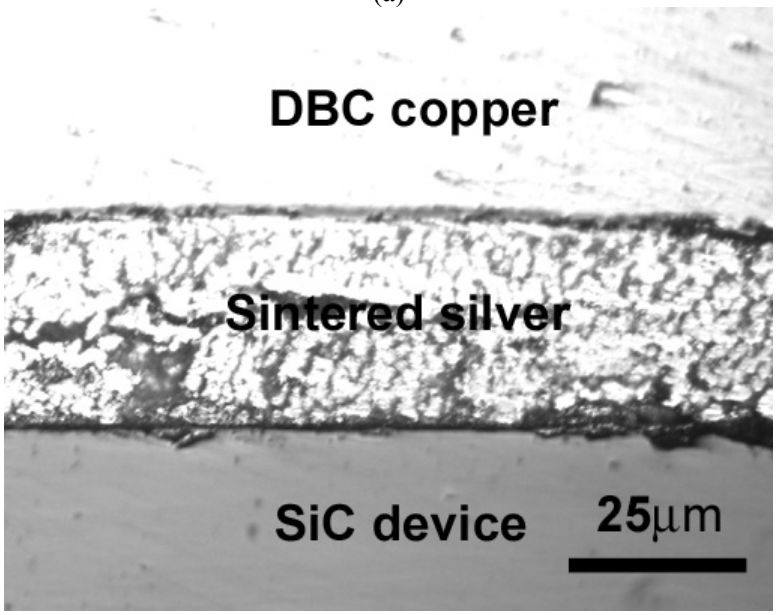
(a) (b)

Figure 3.41. Optical microscopy pictures of one of the sheared-off Infineon SiC device (a) and the corresponding die-attach cavity on the gold-coated DBC substrate (b). The arrows in (b) indicate the debonding areas from the gold-silver interface.

One of the sheared-off Infineon devices and its corresponding die-attach cavity on a gold-coated DBC substrate are shown in Figure 3.41. In the optical image, one can see that in the debonded cavity on the gold-coated DBC substrates, the debonding is partially from metallized gold-sintered sliver interface. On the other hand, no debonding is found from the metallized silver-sintered silver interface. These phenomena provide other edvidence that silver-silver bondings are stronger than the gold-silver bondings.



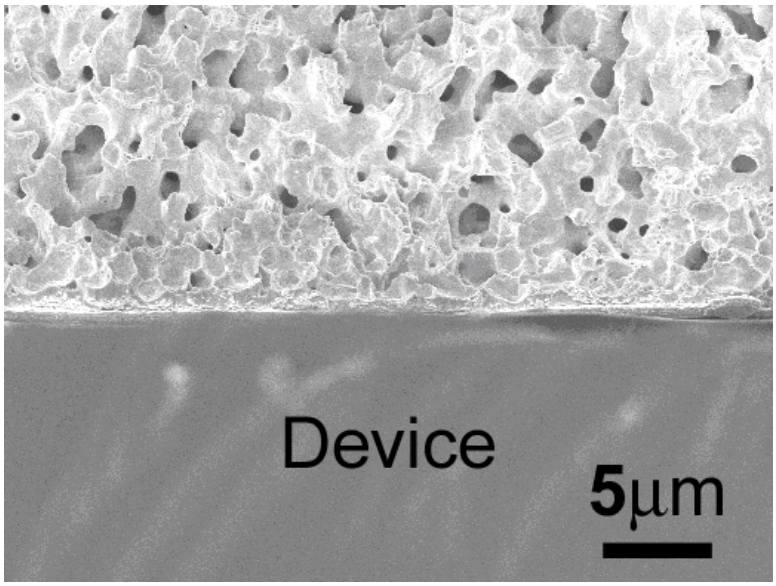
(a)



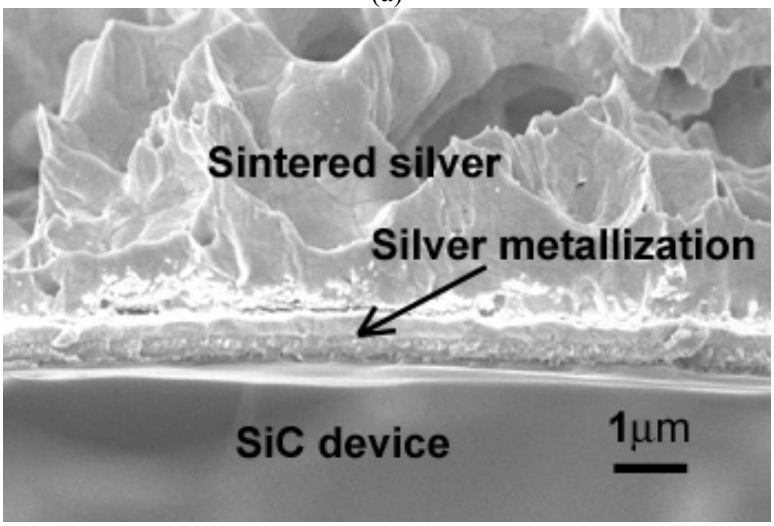
(b)

Figure 3.42. Optical microscope pictures of the cross-section of the sintered silver joints.

The SEM images in Figure 3.42 from the cross-sectional view of the sintered silver joints provide a closer looking at the debonded silver joints. The images were obtained from the molded and polished silver joints.



(a)



(b)

Figure 3.43. Scanning electron microscope pictures of the cross-section of the sintered silver joints.

Figure 3.43 shows the SEM images of another silver joint which is debonded in liquid nitrogen. Compared with the images in Figure 3.42, the microstructures of the sintered silver in Figure 3.43 are reserved better due to the plastic deformation is prevented at the low-temperatures. Also from Figure 3.43, one can clearly see that the sintered silver have form strong bondings with the metallized silver layer on the SiC

devices. Also, the sintered silver has been consolidated into a pretty dense structure with pores that are limited in microscale. The low resistance and the high bonding strengths of the sintered silver joints can be explained by the dense microstructures of the sintered silver. Since the melting point of silver is 961°C, the low-temperature silver joints have potential to function well at extremely high temperatures for most high-power semiconductor devices with high performance and high reliability. Once the silver joints is formed, the maximum use temperature of the power package is then limited by the semiconductor device and the DBC substrates, not by the interconnect material anymore.

3.2.4 Summary

Several strategies have been taken to enhance the silver sintering so as to build the full bonging strengths of the silver joints. The low-temperature silver sintering technologies have been successfully applied to the silver joints with an area up to 4×4 mm^2. Research found that 40-min dwell sintering at 300°C is long enough for the silver joints to build its full bonding strength on a silver-coated device (substrate).

The forward and reverse I-V curves of silver bonded SiC devices shows that the devices have excellent switching characteristics after the silver die-attachment. The results provide evidence that the devices can "survive" well after the low-temperature sintering. Also, the low forward voltage drops of the die-attached devices are partially due to the low electrical resistance of the sintered silver joints.

SAM images revealed that the well-prepared low-temperature sintered silver joints have not shown any detectable voids and the joints are more uniform than that of the reflowed lead-tin or lead-free solder joints. This means the sintered silver joints have excellent thermal performance, especially when the low thermal resistance of the sintered silver is also considered.

After building up the full strength, the debonding of the silver joints is most likely from the sintered silver layer itself instead of the bonding interface. The debonding strength in this case is similar to the tensile strength of the low-temperature sintered silver, which is about 40 MPa. This value is comparable with the bonding strength of the eutectic solder joints and the value is high enough for most semiconductor device bonding applications. Consider the low-processing temperature but the high-melting

point of the interconnect material, the silver sintering technology has advantages in the high-temperature packaging applications.

3.3 Reliability of Sintered Silver Joints

In the following part, we first present the results form the thermal cycling experiment, and then discuss their reliability issues and failure mechanisms based on the experimental results.

In the reliability tests of the sintered silver joints, we observed that the possible failures from the alumina DBC substrates. Two failed alumina DBC substrates are shown in Figures 3.44 and 3.45, respectively. The alumina DBC shown in Figure 3.44 was failed during 100-200 cycles with a temperature range from 50°C to 300°C. The failure was severe and the crack was prorogated parallel to the alumina layer until it broke the whole DBC structure horizontally. We concluded that the alumina DBC substrates were not suitable to be cycled at this high temperature. This was one of the reasons we chose a temperature profile from 50°C to 250°C in our reliability test.

Figure 3.44. An alumina DBC substrate broken from the alumina layer between 100-200 cycles switching from 50°C to 300°C.

Figure 3.45 shows another alumina DBC substrate that was broken between 500 to 1000 cycles during the temperature cycling from 50°C to 250°C. Since the broken was only at the corner and the crack was perpendicular to the DBC structure, we still could cycle the silver joints on the substrate. Later on we did see more perpendicular cracks from both alumina and aluminum-nitride DBC substrates after 8000 thermal cycles. Also, we found that the aluminum-nitride DBC substrates could usually withstand the larger

switching temperature ranges or more temperature cycles than the aluminum-oxide DBC substrates.

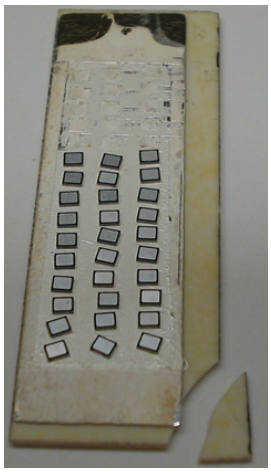


Figure 3.45. Another alumina DBC substrate broken from the alumina layer between 500 to 1000 cycles switching from 50°C to 250°C.

As discussed in Chapter 2, the temperature profile we chose for the reliability test is shown in Figure 3.46, which was realized using an adapted belt reflow oven. In the following sections, the experiment results were all obtained after thermal cycles using this temperature profile unless mentioned specially.

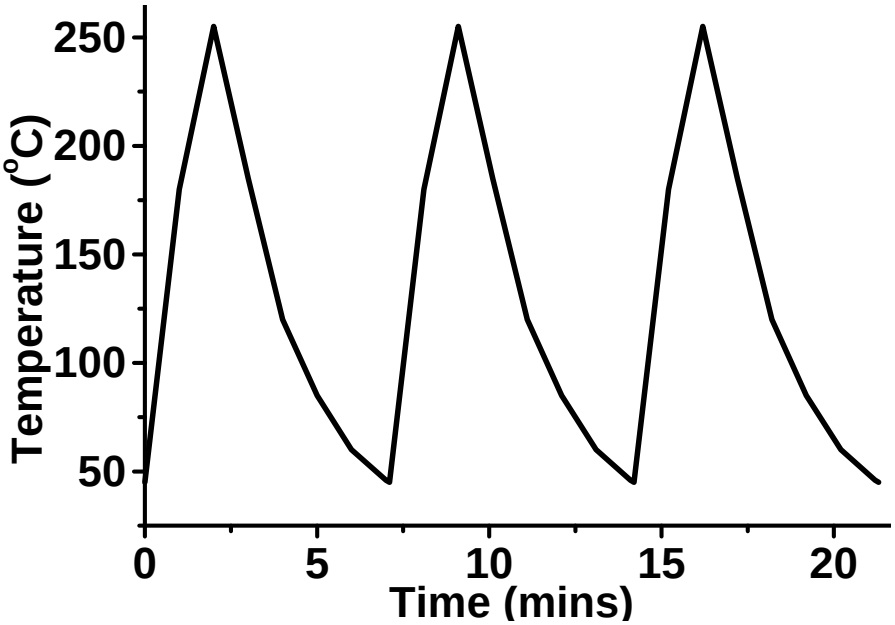


Figure 3.46. The temperature profile obtained using the Sikama belt reflow oven.

3.3.1 Temperature Cycling Experimental Results

From the SAM images of the thermal cycled silver joints shown in Figures 3.47 and 3.48, it was found that the silver joints could maintain almost intact up to about 2000 thermal cycles on both aluminum-oxide or aluminum-nitride DBC substrates, no matter the substrates were silver or gold coated. However, at thermal cycles beyond 4000, some non-uniformity in the silver joints was shown with low-density areas or partially debonds. Furthermore, the evolution of the debonding in the silver joints was quite different with that in the solder joints. In the case of solder joints, the debonding areas had no interconnections anymore and debonding boundaries were clearly observed as shown in Figure 3.49 [11]. While in the case of the silver joints, the boundaries of the debonding areas could not be clearly defined. Even in the debonding areas of the silver joints, there were still partial interconnections as discussed later on in the die-shear off test results. This was in consistence with I-V curve tracer test results, in which experiment we did not see the obviously increase in the electrical resistance of the silver joints after the thermal cycle.

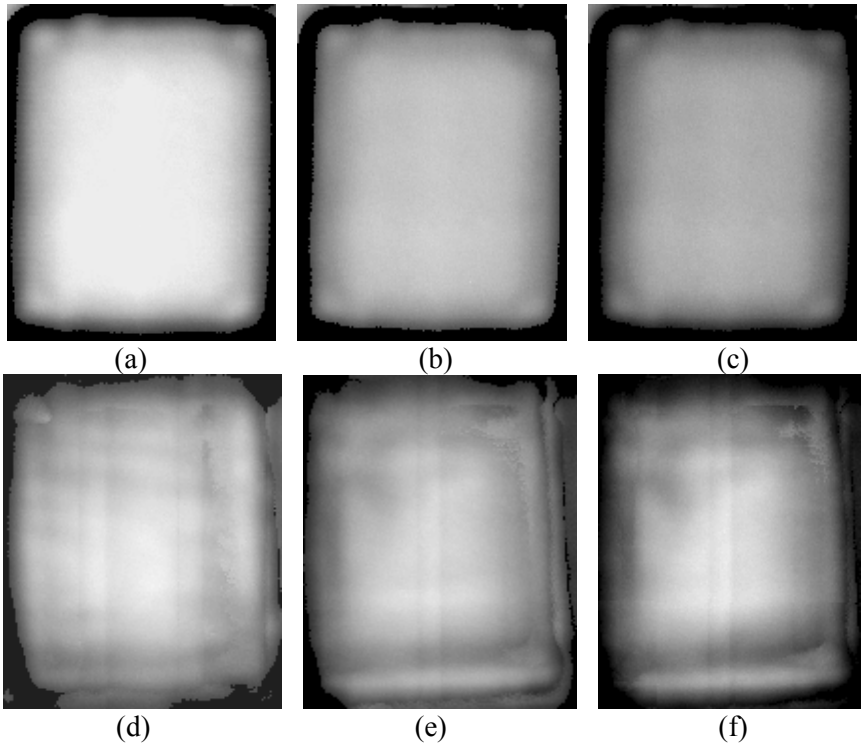


Figure 3.47. The SAM images of the sintered silver joints on nickel/silver-coated AlN DBC after 0 (a), 1000 (b), 2000 (c), 4000 (d), 6000 (e), and 8000 (f) thermal cycles, respectively.

It was also found that the debonding of the silver joints on the copper substrates was formed much earlier than those on the DBC substrates as shown in Figure 3.50. Usually the silver joints could only maintain intact up to 500 thermal cycles on the copper substrates. This was because the copper substrates had a much larger CTE mismatch with the SiC devices than that of either aluminum-oxide or aluminum-nitride DBC substrates. Therefore, during the thermal cycles, there were higher thermal stresses in the silver joints on the copper substrates than those on the DBC substrates. The higher thermal stresses in turn caused quicker silver joints debonding.

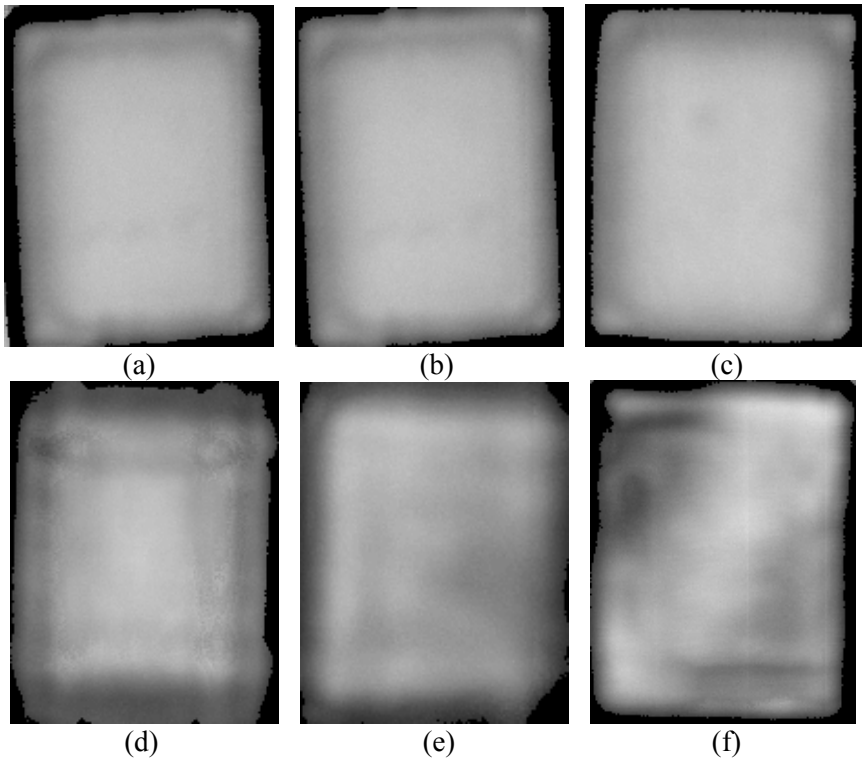


Figure 3.48. SAM images of the sintered silver joints on nickel/gold-coated Al_2O_3 DBC after 0 (a), 1000 (b), 2000 (c), 4000 (d), 6000 (e), and 8000 (f) thermal cycles, respectively.

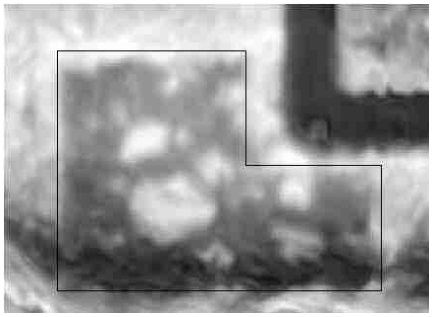
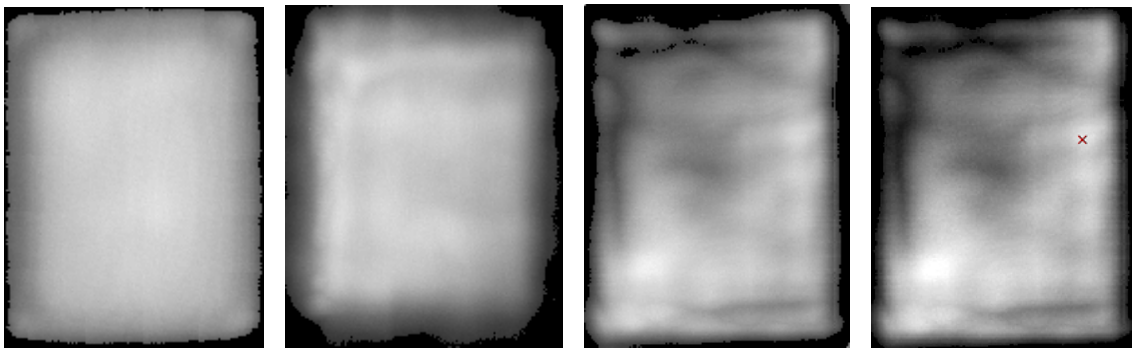


Figure 3.49. The debonding of the eutectic lead-tin solder joints after 875 temperature cycles between -55—150°C. The enclosed area indicates the initial extent of the solder joints.



(a) (b) (c) (d)

Figure 3.50. The SAM images of the sintered silver joints on nickel/silver-coated copper substrates after 0 (a), 500 (b), 1000 (c), and 2000 (d) thermal cycles, respectively.

The changes of the bonding strength during the thermal cycling experiment were summarized in Figures 3.51, 3.52, and 3.53. If we set the 50% strength drop (the average value) as the failure criterion, the silver joints were failed at around 4000 cycles on the nickel/silver-coated DBC substrates, 6000 cycles on the nickel/gold coated DBC substrates, and 500 cycles on nickel/silver coated copper substrates. However, the silver-coated substrates usually have much higher absolute values of bonding strength than those of the gold-coated substrates.

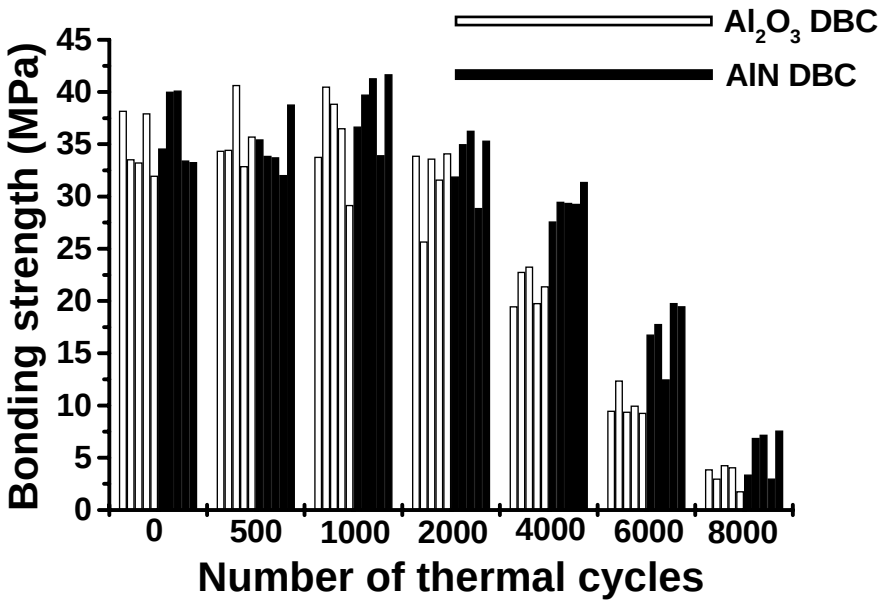


Figure 3.51. Changes of shear strength of the low-temperature sintered silver joints on nickel/silver-coated DBC substrates during the temperature cycling experiment.

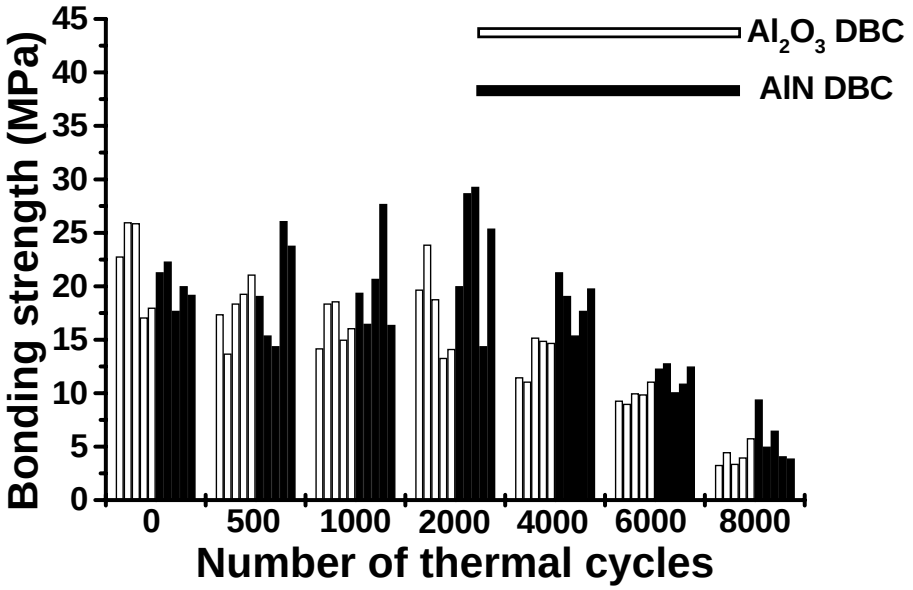


Figure 3.52. Changes of shear strength of the low-temperature sintered silver joints on nickel/gold-coated DBC substrates during the temperature cycling experiment.

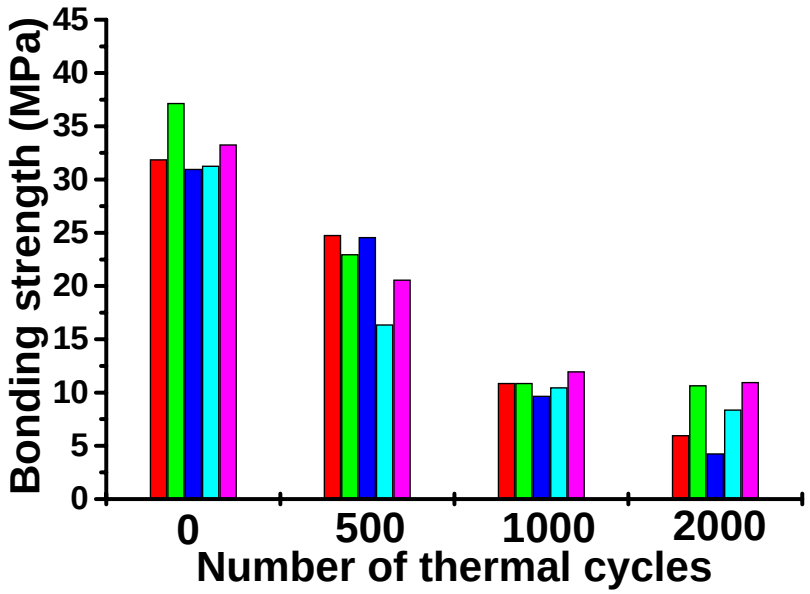
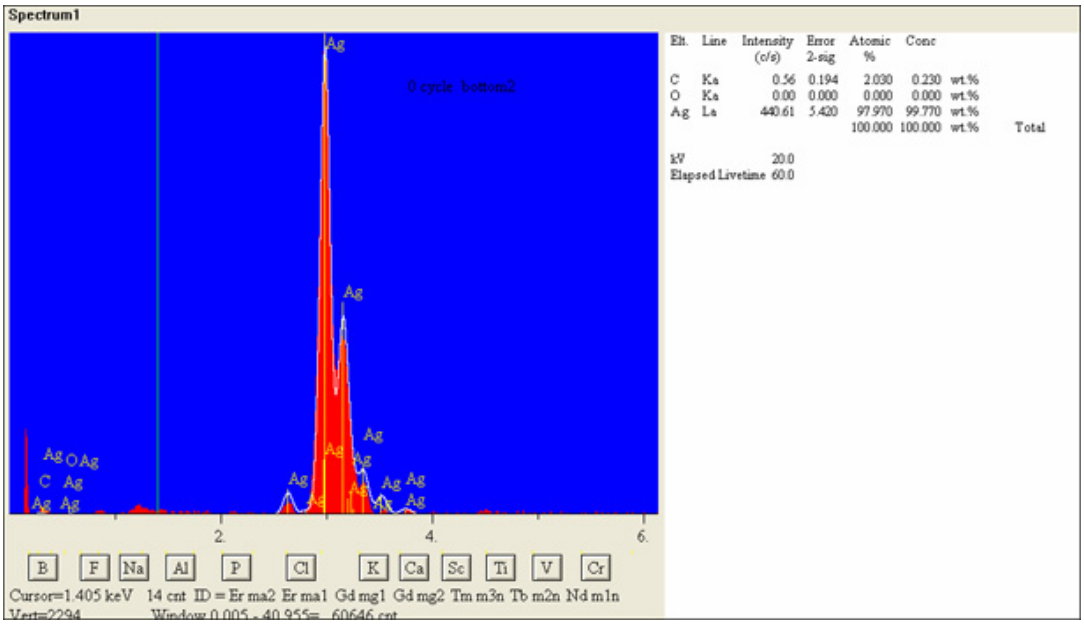
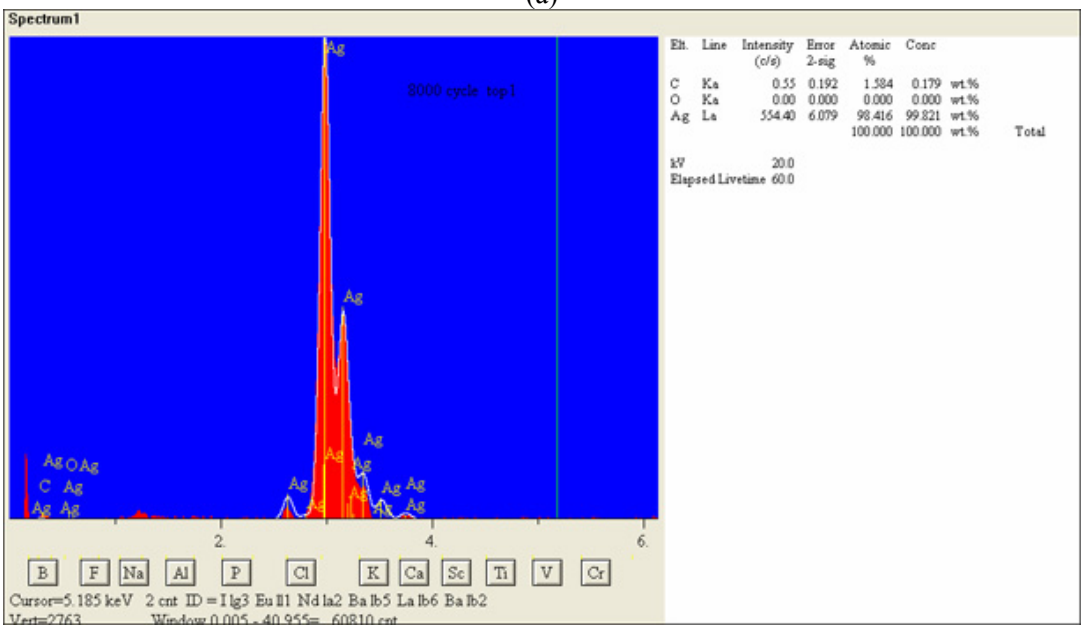


Figure 3.53. Changes of shear strength of the low-temperature sintered silver joints on nickel/silver-coated copper substrates during the temperature cycling experiment.

From the SEM/EDS analysis of the debonded silver joints after the thermal cycles, carbon compositions in the sintered silver joints keep almost unchanged and there is no detectable oxygen components increase. This means the silver joints are not oxidized during the thermal cycling experiment.



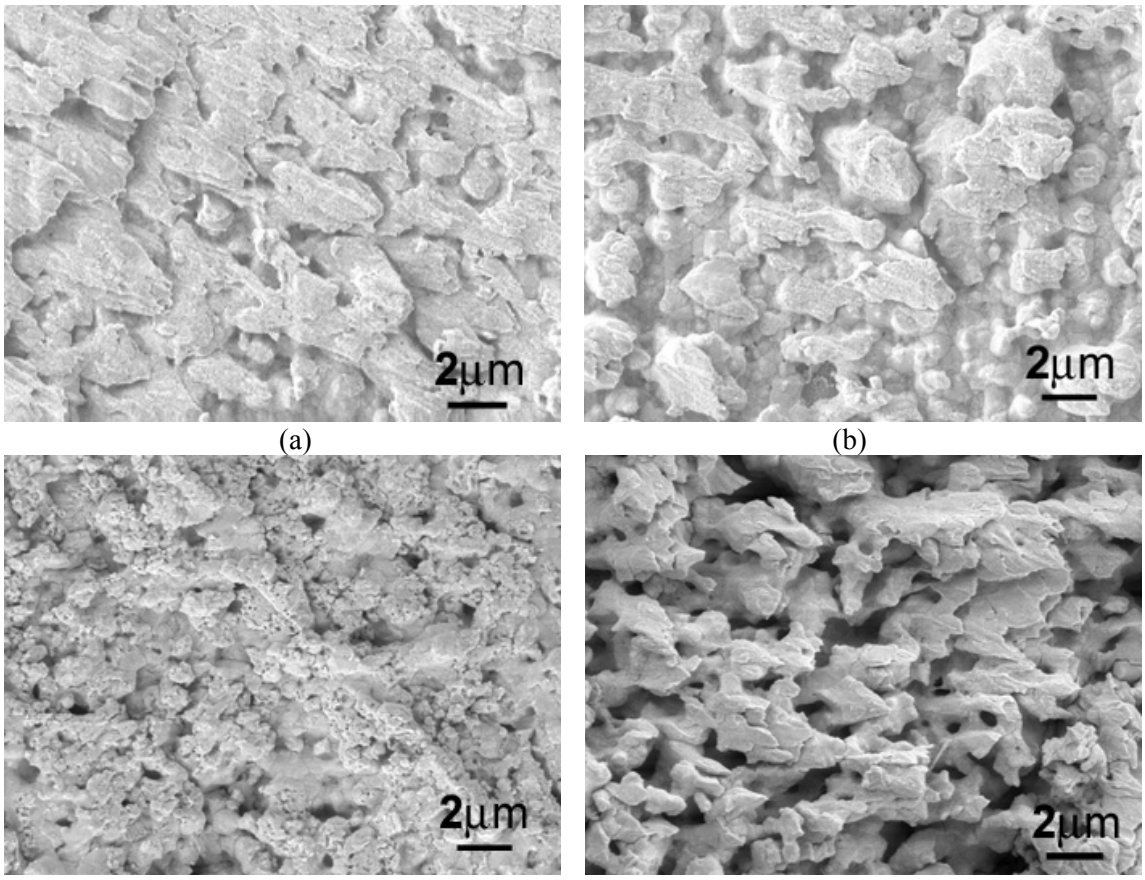
(a)



(b)

Figure 3.54. EDS analysis of the silver joints before (a) after (b) the 8000 50—250°C thermal cycles. Silver is about 99.8 wt.% and the rest component is carbon. There is no detectable oxygen element before and after thermal cycles.

However, it was found that the microstructures of the sintered silver joints changed significantly during the thermal cycles as shown in Figure 3.55. One of the most evident changes was that new micro-cavities were created again after about 2000-4000 thermal cycles in the silver joints on the DBC substrates. For the silver joints on the copper substrates, the creation of new pores was much earlier at about 500-1000 cycles.



(a) (b)

(c) (d)

Figure 3.55. Microstructures of the debonded sintered silver joints on the silver-coated SiC devices after (a) 0, (b) 2000, (c) 4000, and (d) 6000 cycles. The silver joints were debonded from the nickel/silver aluminum-nitride DBC substrates.

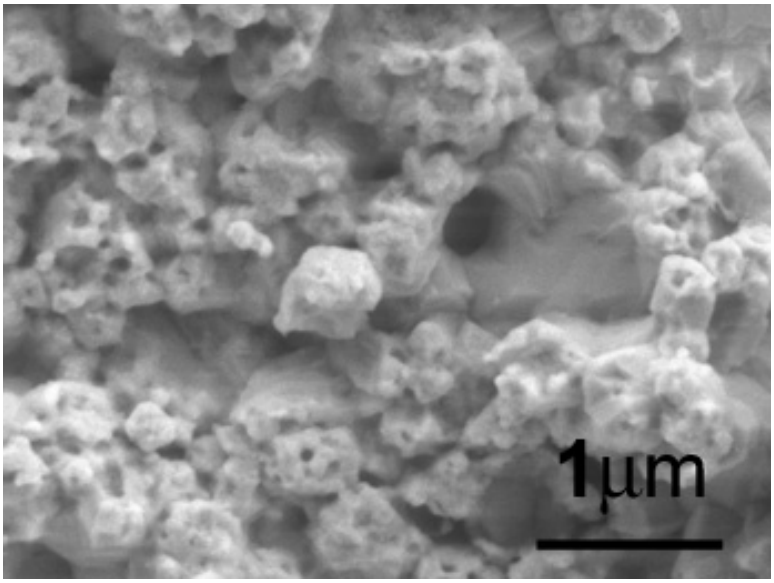


Figure 3.56. Microstructure changes of the debonded sintered silver joint surfaces after 4000 thermal cycles. The silver joints were debonded from the nickel/silver aluminum-oxide DBC substrates.

Figure 3.56 shows the closer looks of the debonded surfaces after 4000 thermal cycles in which the newly created microcavities during the thermal cycling are clearly shown. As a result, the fracture surface consists of small dimples which represent the microcavities after coalescence.

3.3.2 Discussion on Reliability and Failure Mechanisms

A deformation-mechanism (Weertman-Ashby) map [12] of bulk silver is shown in Figure 3.57. It is a graphical description of creep, representing the ranges in which the various deformation modes are rate-controlling in the stress versus temperature space. The Weertman-Ashby plots assume, for simplicity, that there are six independent and distinguished ways by which a polycrystal can be deformed, retaining its crystallinity:

(1) Above the theoretical shear strength, plastic flow of the material can take place without dislocations, by simple glide of one atomic plane over another.
(2) Movement of dislocation by glide.
(3) Dislocation creep; this includes glide and climb, both being controlled by diffusion.
(4) Nabarro-Herring creep [13].
(5) Coble creep.
(6) Twinning; stress-assisted and strain-induced martinsitic transformations.

From the deformation-mechanism map one can see that the theoretical shear stress of pure silver is approximately equal to $G/20$ and it is practically independent of temperature. For values of σ/G between 10^{-1} and 10^{-2}, slip by dislocation movement is the controlling mode at all temperatures. It can be seen that the grain size affects the extant of the fields. The fields also depend on strain rate and the map was made for a strain rate of 10^{-8} s^{-1}. The Coble and Nabarro-Herring mechanisms, especially, are affected by the grain size, because of their nature. Generally speaking, the smaller the grain size, the more shift the Coble and Nabarro-Herring fields towards to lower temperature.

The average grain size of the low-temperature sintered silver is only about 1 μm. Thus, the Coble creep field is expected to shift significantly towards the lower temperature. The temperature cycling range in our experiment is about 50-250°C, that is 0.26-0.42 T/T_m in the deformation-mechanism map. Since the significant shift of the

Coble field, the higher temperature range in the thermal cycling is already enough to create the plastic deformation such as by Coble creeps. Especially in the low-temperature sintered silver, there are many microscale grains, pores, and internal interfaces with irregular shape, thermal strains at some regions could be tremendous high enough to create the plastic deformation due to the high-stress concentration.

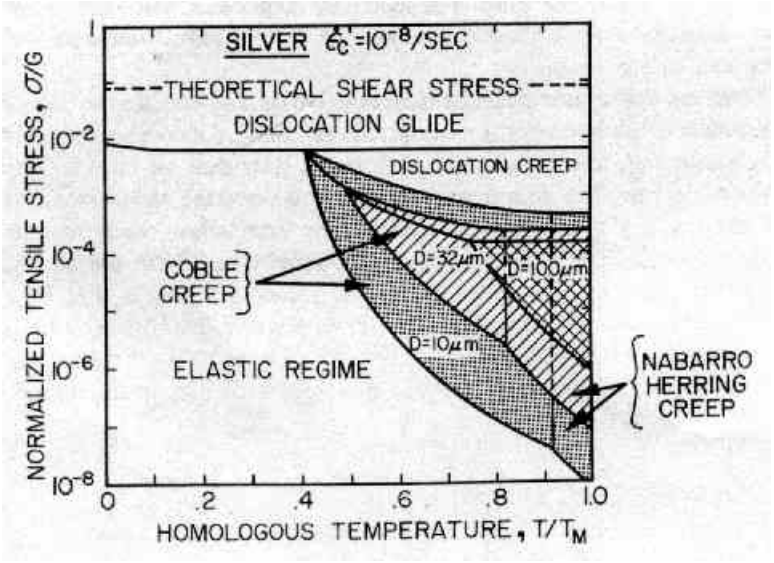
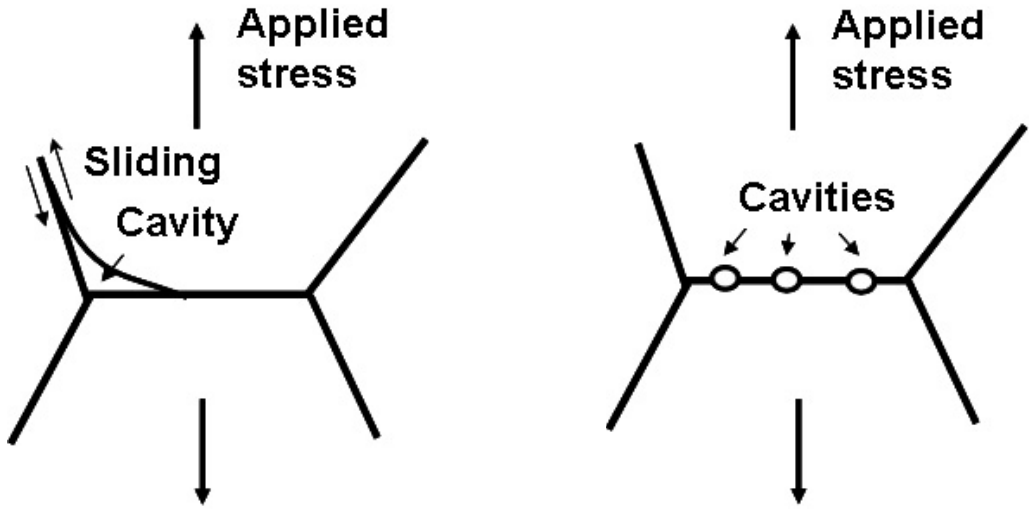


Figure 3.57. The deformation-mechanism map for pure silver, established for a critical strain rate of 10^{-8} s^{-1}; it can be seen how the deformation-mechanism fields are affected by the grain size (reprinted from Ref. [12], p.677).

In a ductile fracture, the role of plastic deformation is very important. The important point in the fracture of a ductile material is the flexibility of slip. Dislocations can move on a large number of slip systems and even cross from one plane to another (cross-slip). In the case of single crystal, a ductile metal undergoes slip throughout its section. There is no nucleation of cracks and the crystal deforms plastically until the start of plastic instability called necking. However, in the case of a ductile material with many microstructural elements, microcavities may be nucleated in regions of high stress concentrations in a manner similar to that of semibrittle materials. Microscopically, Zener [14] was the first one to propose that in crystalline solids micro-cracks can be nucleated by grouping up of dislocations piled up against a barrier. During the crack nucleation, high stresses at the head of a pile up are relaxed. But this would occur only in case there is no relaxation of stresses by dislocation movement on the other side of the barrier. At relatively high temperatures, two other types of cracking are observed:

(1) The first one occurs at a triple point (where three grain boundaries meet) as illustrated in Figure 3.58(a). Due to grain boundary sliding that occurs at high temperatures, stress concentrations are developed at triple points. This type of crack is called *w*-type.

(2) Another type of cracking occurs under conditions of low stresses and high-temperature. Small cavities form on the grain boundaries that are, predominantly, at approximately 90° to the stress axis as illustrated in Figure 3.58(b). These are called *r*-type cavities.



(a) (b)

Figure 3.58. *w*-type cavitation at a grain-boundary triple point (a) and *r*-type cavitation at a grain boundary normal to the stress axis (adapted from Ref. [12], pp. 146-147).

In Figure 3.56, both *w* and *r*-types of the microcavities are likely shown up. The cavitation was nucleated during the thermal cycling experiment. The nucleation together with the usual necking mechanism during the thermal cycles lowered the bonding strength at the fracture interface, which could explain the drop of the bonding strengths of the sintered silver joints after the thermal cycles. Furthermore, the work-hardening mechanism at the fracture surface during the thermal cycles made the debonding of the sintered silver behavior like a semibrittle material.

At the higher thermal cycles, the microcavities at the grain boundary may grow and form connections with each other so as to pinch-off a large grain into several smaller grains by a de-sintering mechanism. The de-sintering mechanism competes with the temperature dwell effect (which turns to coarsen the grains) during a temperature cycling

and they both introduce microstructure changes and loosen the sintered silver from grain boundaries.

Finally, from both Figures 3.57 and 3.58, one can see that the silver deformation and growth of the microcavities are tensile stress dependent. The higher the tensile strength means the faster the deformation. Thus the bonding strengths of the silver joints on the copper substrate drop much faster than those of on the DBC substrates because copper and SiC has a much larger CTE mismatch than that of DBC and SiC, and thus much higher thermal stresses could be induced in the silver joints on copper substrates than those on the DBC substrates during the thermal cycling.

3.3.3 Summary

The failure mechanism of the low-temperature sintered silver joints is quite different with that of the solder joint during a temperature cycling experiment. The failure mechanism in a solder joint is typically explained by the phase coarsen/separation induced crack initiation and growth because the dislocations piled up at the phase boundaries. On the other hand, the low-temperature sintered silver has no phase-separation problem since the composition of the sintered silver is pure silver. However, the tremendous microstructural elements and small grain sizes in the low-temperature sintered silver result in microcavities nucleated at the gain boundaries due to the stress-concentration and the crept/piled-up dislocations. The nucleation and growth of the microcavities at the grain boundaries could explain the bonding strength drops after the temperature cycling.

Generally speaking, the low-temperature sintered silver joints should have much higher temperature capability than solder joints considering the high-temperature profile used in the thermal cycling experiment of the silver joints.

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Chapter 4
Applications of Sintered Silver Joints

Since the nanoscale silver pastes can be sintered at a temperature low enough so that it does not affect functionality of most power devices, the technology can be used widely in power electronics packaging with many potential advantages. It can be also used in other high-power packages such as photonics. In the following sections, we present the potential applications of the low-temperature sintered silver joints in the single-chip power packaging, multi-chip power module packaging and high-power white light-emitting diode (LED) packaging.

4.1 Applications in Single-Chip Power Packages

The selection of an interconnecting material and packaging technologies usually depends on applications that being dictated by the packaging size, substrate material, devices and operating environmental requirements. As discussed in Chapter 1, currently the dominant packaging technologies are as illustrated in Figure 4.1(a), which involves attaching one terminal of the silicon device to a heat-sinking substrate with a lead-containing solder alloy and wire-bonding fine aluminum wires to the other terminal(s). The main features of the power package are as follows:

(1) It is usually used for packaging silicon semiconductor devices.

(2) Its operating temperature can be only up to 125~200ºC due to the low-melting points of solder alloys and the tolerance of silicon devices.

(3) It usually needs to attach a heat sink for thermal management.

(4) It has relatively low integration, low power density, and low electrical and thermal performance.

With these disadvantages, the interconnect technology is very hard to be adapted to the next generation of power packages which contain wide-bandgap semiconductor

devices with high integration, high power density, and high electrical and thermal performance requirements. However, making use of our low-temperature nanoscale silver paste sintering technology, we can hopefully meet all the requirements. In a proposed packaging structure as shown in Figure 4.1(b), if we interconnect all the terminals of a wide-bandgap semiconductor device using the low-temperature sintered silver to metal substrates, we can come out a highly integrated power package with high power density. Due to the high electrical and thermal conductivities of the sintered silver joints, the performance of the power package should be better. Furthermore, because of the high melting-point of the sintered silver (961°C), once accomplished, operating temperature of the power package is only limited by the power device instead of the interconnect material. Therefore, for the future high-temperature devices, it is possible to let them to operate at elevated temperatures so that the conventional heat sink/fan systems are not necessary anymore. The difference from the high operating temperature and the ambient is sufficient for the heat removal. By removing bulky heat sink cooling systems, the packaging cost is cut down and the power density is enhanced dramatically. In summary, the main features of the future single-chip power package may be as follows:

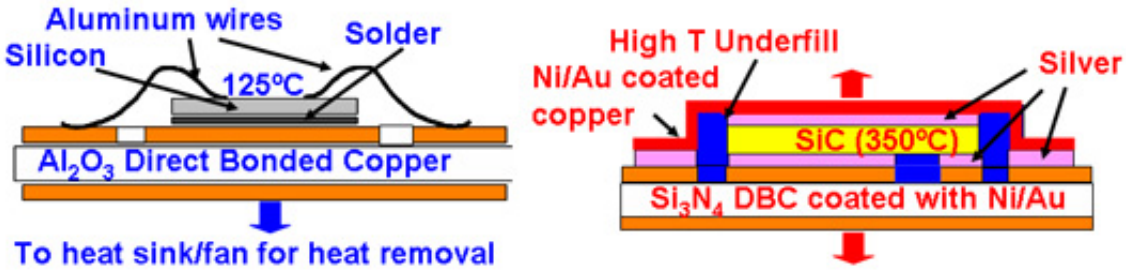
(1) It is good for silicon semiconductor device packaging but especially good for wide-bandgap semiconductor devices such as silicon carbide.

(2) Its operating temperature can be up to the up-limits of the power devices, e.g., for SiC this temperature could be 350~500°C.

(3) It may not need to attach a heat sink for thermal management because it can work at the elevated temperatures.

(4) It has high integration, low power density, and low electrical and thermal performance.

To demonstrate the packaging technology using the low-temperature sintered silver joint technology, we packaged some power IGBT bare dies into the single-chip power packages. Here we still used silicon power devices for the packaging concept demonstration.

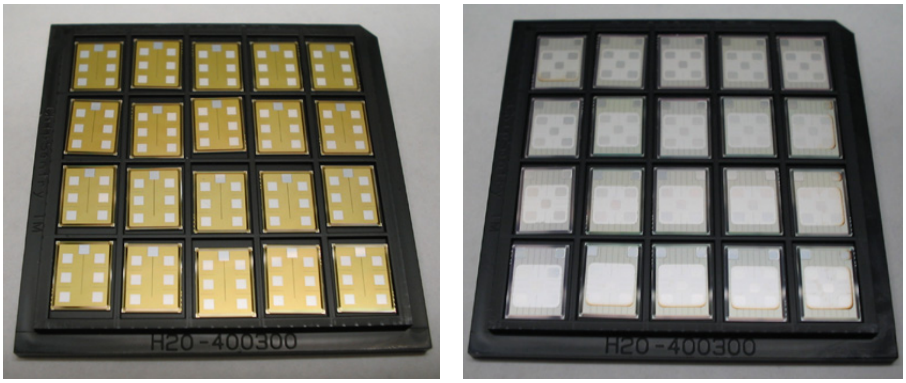


(a) (b)

Figure 4.1. The solder die-attaching and wire-bonding technology (a) versus the low-temperature silver sintering technology (b).

The bare dies with type # of IXSD35N120A and IXSD1765 from IXYS Corporation (Santa Clara, CA) are used for the fabrications of single-chip power packages. They are shown in Figure 4.2(a) and (b), respectively. Although they have equivalent datasheet with type # of IXSH35N120A as described in Appendix B [1], their die maps are quite different. Furthermore, the IXSD35N120A is unsolderable with aluminum pad and passivation on the gate and source terminals. But the IXSD1765 is solderable with Ni/Ag metallization already on both drain and the gate/source terminals.

The fabrication steps for silver joint single-chip power packages are shown in Figure 4.3. In the case of unsolderable dies such as the IXSD35N120A, fabrication starts from a metallization procedure quite similar to the under bump metallization method in a flip-chip power packaging [2]. This is shown in the Step (I) in Figure 4.3. In this step, the gate and source are sputtered Ti/Ni/Ag for the formation of silver joints. However, in the case of solderable devices such as IXSD1765, this step can be skipped.



(a) (b)

Figure 4.2. The IXYS bare dies used for single-chip power packaging demonstration. (a) Bare power IGBTs with type # of IXSD35N120A; (b) Bare power IGBTs with type # of IXSD1765.

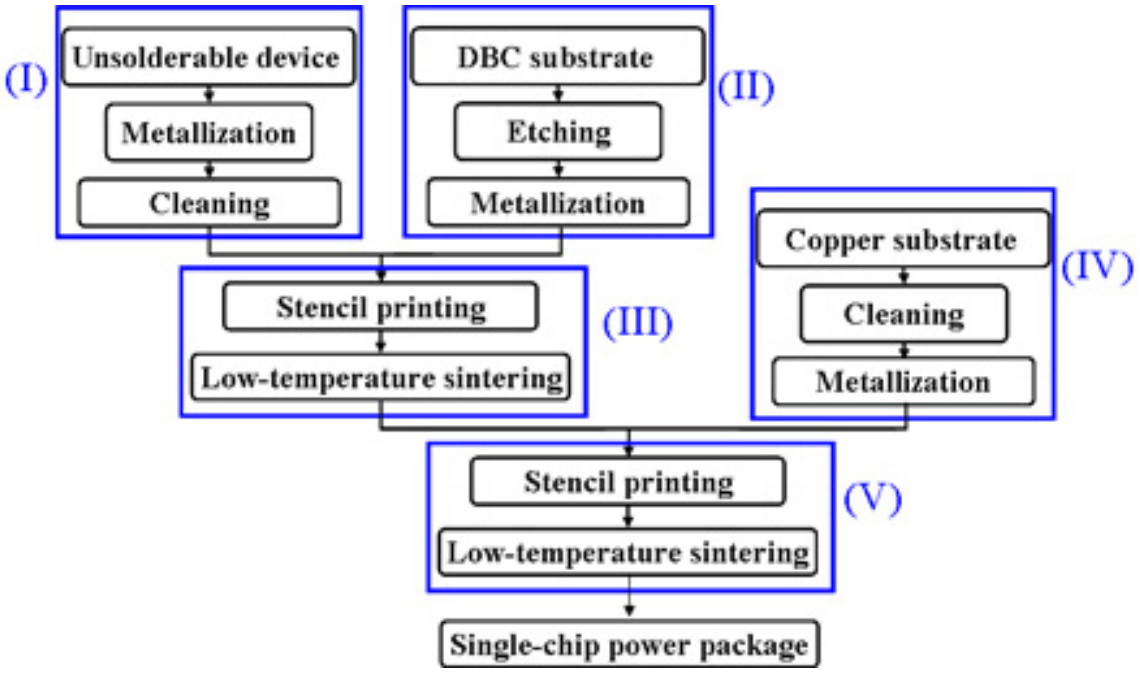
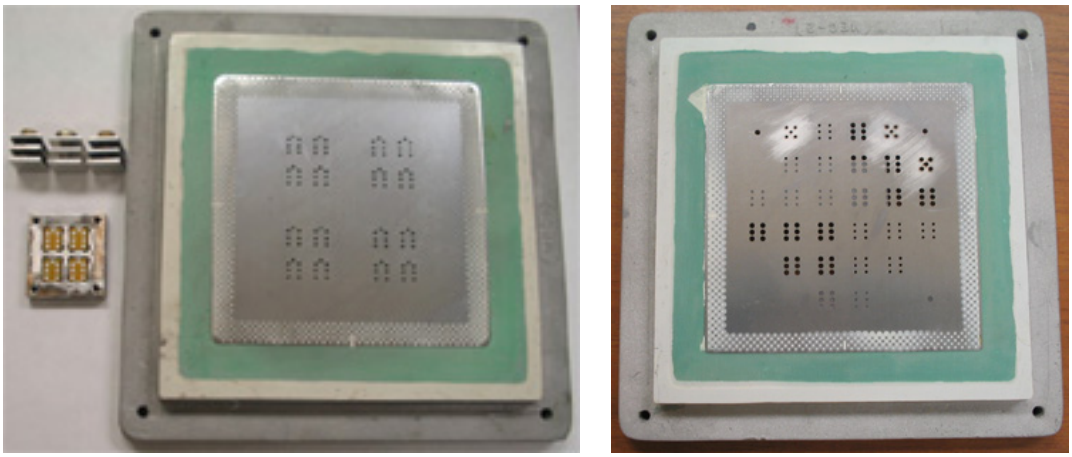


Figure 4.3. The fabrication steps for the silver jointed single-chip power packages.

After the device metallization, we stencil-printed nanoscale silver paste onto the sputtered gate and source patterns and then sintered in open-air to thicken the silver joints. The stencil fixtures and patterns in Figure 4.4(a) were used to print the patterns on the gate/source sides of the IXSD35N120A dies while the stencil in (b) was used to print the drain terminals. The stencil-printed silver patterns on the IXSD35N120A dies are shown in Figure 4.5 after the low-temperature sintering. As an option, solder mask could be patterned on the bare dies as shown in Figure 4.6. The solder mask can protect the gate fingers on the gate and source sides of the bare dies and prevent the possible drops in the breakdown voltage. This step is not shown in Figure 4.3.

Step (II) is etching and metallization of DBC substrates for the gate/source terminals. The etching was done by screen printing etching resist and patterning by an ultraviolet photolithography method as described in Ref. [3]. The metallization procedure involves coating either nickel/gold or nickel/silver onto etched DBC substrates as described in Appendix A. After the etching and metallization, the DBC substrates are as shown in Figure 4.7. The etched patterns in Figure 4.7(a) were designed for the IXSD35N120A dies while those in (b) were designed for the IXSD1765 dies.



(a) (b)

Figure 4.4. The stencil masks and fixtures used for stencil-printing silver paste. (a) The stencil pattern designed for the IXSD35N120A bare dies, and (b) the pattern for the drain terminals of the silver joints.

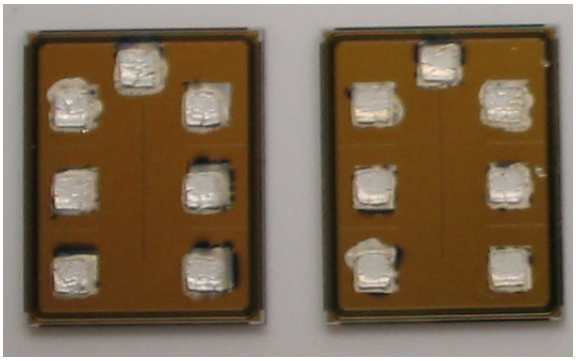


Figure 4.5. The IXSD35N120A bare dies after the sputtering metallization and low-temperature sintering of stencil-printed silver paste on the gate and source terminals. The top middle square is for gate and other six are for the source.

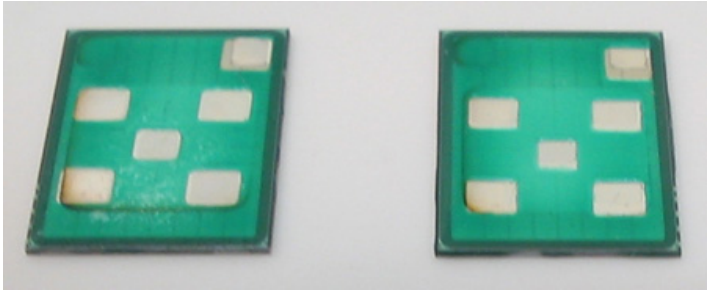
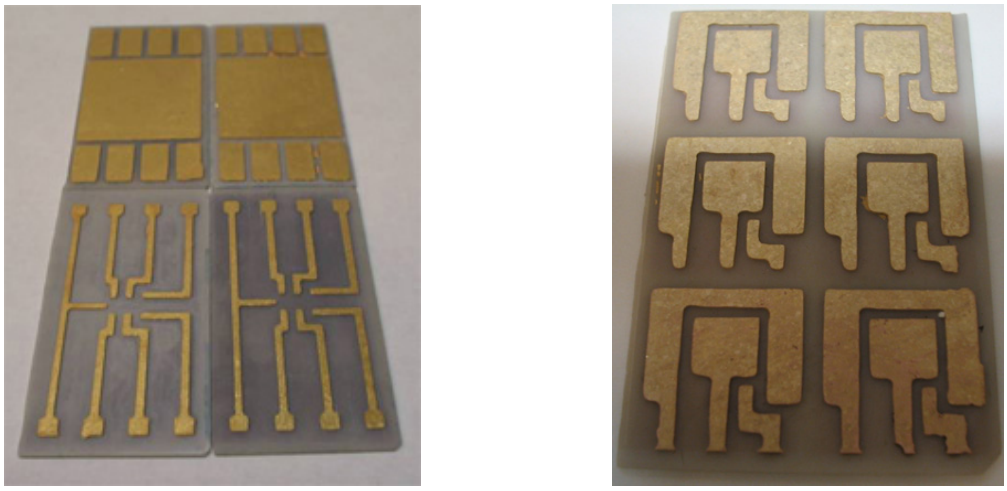


Figure 4.6. The IXSD1765 bare dies after the solder mask deposition to protect the exposed gate fingers. Note that the IXSD1765 dies are already metallized nickel/silver at the open windows for the gate and source terminals.



(a) (b)

Figure 4.7. The etched and nickel/gold coated DBC substrates for the IXSD35N120A dies (a) and those for the IXSD1765 dies (b).

After the bare die and DBC substrate preparation, nanoscale silver paste was stencil-printed on the DBC substrates again for the device attachment. In one case, the device could be flip-attached on the etched DBC substrate as shown in Figure 4.8. This is Step (III).

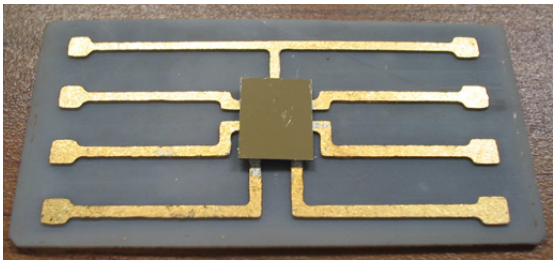
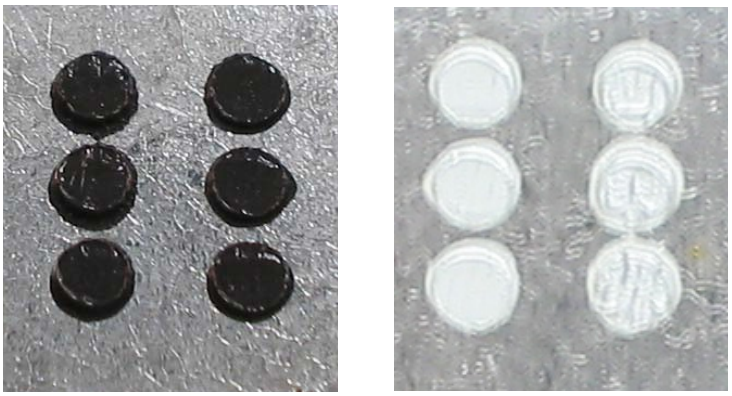


Figure 4.8. Flip die-attached IXSD1765 on the nickel/gold coated DBC substrate.

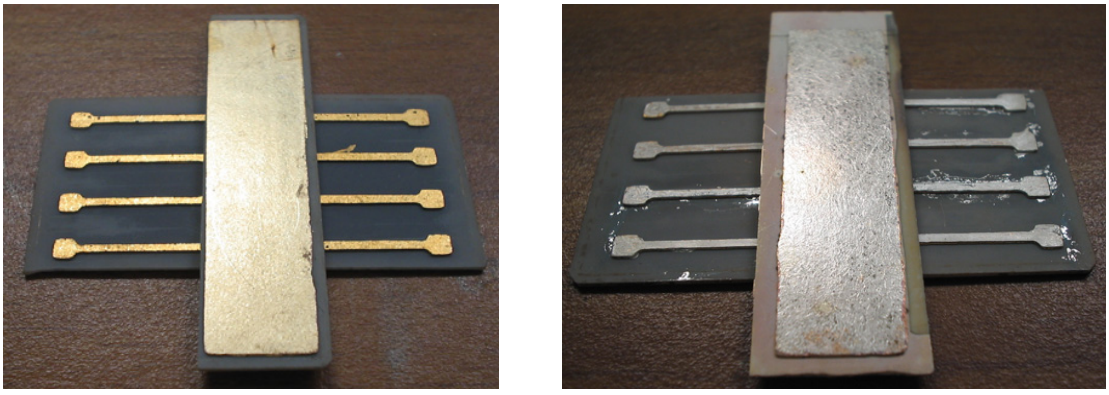
In Step (IV), we metallized DBC or copper substrates with either nickel/gold or nickel silver for the drain terminal interconnection. Since the die size is about 9 mm × 7 mm for both IXSD35N120A and IXSD1765, the drain terminals are need to patterned to small sizes to achieve better silver joint bondings as discussed in Chapter 3. Otherwise the drain terminals are too big for entire silver joint to burnout all its organic components in the nanoscale silver paste during the low-temperature sintering. One of the patterns for the drain terminal silver joints is as shown in Figure 4.9. The pattern leaves enough gaps for the organic burnout during the silver paste sintering.



(a) (b)

Figure 4.9. The stencil-printed silver paste patterns on nickel/silver coated DBC substrates (a) and those after the low-temperature sintering (b).

Finally in Step (V), we interconnect the drain terminals of the device to the DBC substrates with the patterned solder joints. Figure 4.10 shows the finished single-chip power packages for the IXSD35N120A devices, using nickel-gold plated DBC substrates (a) and the nickel-silver plated DBC substrates (b), respectively. The single-ship power package is convenient for electrical test.



(a) (b)

Figure 4.10. The finished single-chip power packages for the IXSD35N120A devices (a) using the nickel-gold plated DBC substrates and (b) the nickel-silver plated DBC substrates.

Another option for the drain terminal interconnection is to use copper substrates instead of DBC substrates as shown in Figure 4.11. The copper substrates have an advantage of flexibility so that they can be curved into a cavity easily. In this case, it is more convenient to interconnect the drain terminals first. Figure 4.11 shows two of the IXSD1765 devices that were interconnected to a nickel/gold coated copper cavity using the low-temperature sintered silver joints. After the drain terminal interconnection, the IXSD1765 device with the copper cavity was flipped attaching to the nickel/gold coated substrates as shown in Figure 4.7(b). Again we used the low-temperature sintered silver

joints. Finally metal leads were attached to the single-chip package as shown in Figure 4.12. In the prototype structure, we still used solder for the lead attachment. But later on we can use sintered silver conveniently. Unlike solder-reflow, the nanoscale silver paste was sintered at temperatures far below the melting point of the bulk silver. Thus, the sintered silver films were stable enough at the sintering temperature and sintering several times in series was possible during a power package fabrication.

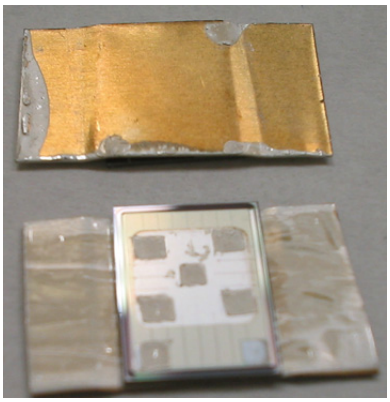


Figure 4.11. The IXSD1765 dies with the drain terminals interconnected to nickel-gold coated copper cavities.

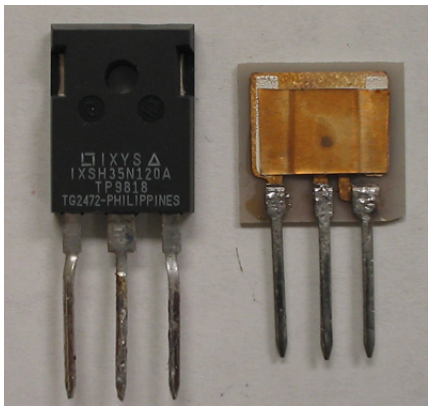


Figure 4.12. Comparison of the commercial wire-bonded single-chip power package (left, TO-247 power package) with the low-temperature sintered silver joint power package (right).

In the sintered silver jointed power package, both the long and thin bonding wires bonded to the gate/source terminals and the low-melting solder for the drain terminals are substituted with the low-temperature sintered silver. Packaging parasitics are not only reduced by switching to a better interconnect material, but also from the packaging structure points of view, since the silver joints could be designed with lower profile and larger areas for the bonding.

4.2 Applications in Multi-Chip Power Modules

With a little bit modification, the low-temperature silver sintering technology can be used in multi-chip power modules. Making use of the high-melting point of the sintered silver, the technology is especially good for the fabrication of the future high-temperature integrated power electronics modules. Figure 4.13 shows an illustration of a low-temperature silver jointed multi-chip power module.

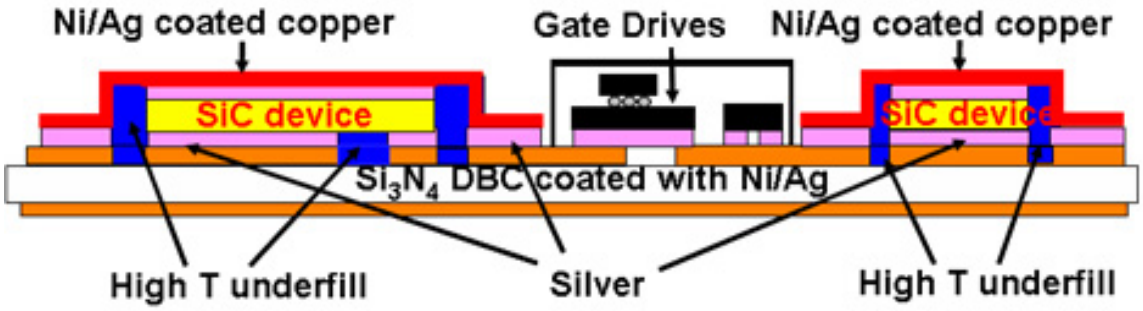


Figure 4.13. Illustration of a high-temperature integrated power electronics module bonded using low-temperature sintered silver.

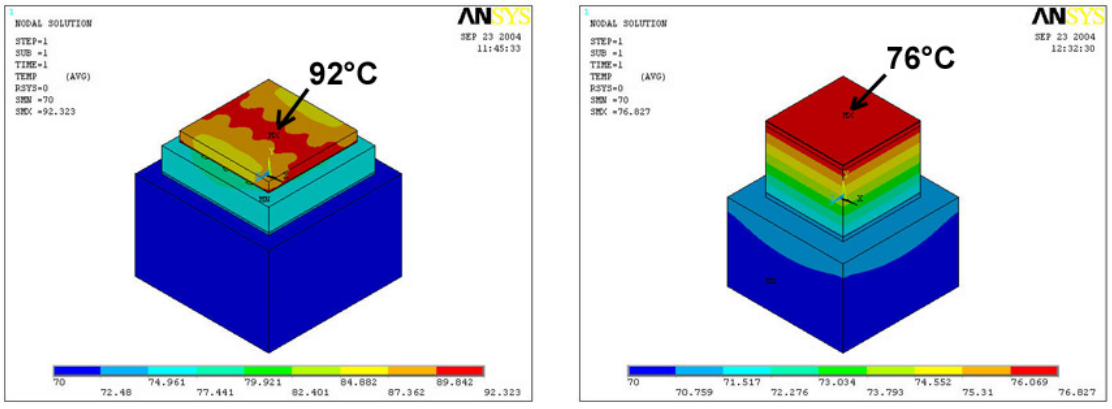
In the sintered silver bonded power electronics modules, high-temperature power devices like SiC could be used. The whole power module could be built on a Si_3N_4 substrate for a better CTE match. The power devices are packaged using the structure like that in a single-chip power package. If necessary, heat removal path could be built from the top of the power devices for double-sided cooling. The gate drive components are put in between the power devices for the nearest control. Since the date drives are separated with the power stages, the conventional packaging methods can still be applied in the control stage.

4.3 Other Applications

Besides the applications in power electronics, the low-temperature silver sintering technology can also be applied in other high-power packages such as white LED packaging and power laser packaging. The LEDs and power lasers are usually made of wide-bandgap semiconductor materials. They have features of small size but high heat flux density. Therefore, they put lots of pressure on the packaging technologies. Actually,

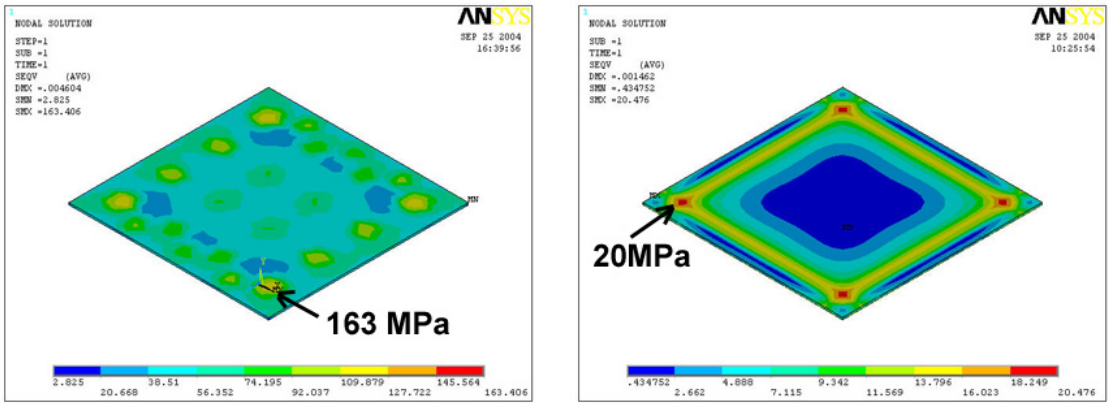
many situations the laminating power of these devices is limited by the packaging methods and thermal management.

On thermal management, to show how much improvement we may expect from our proposed package compared with the flip-chip LED package, we performed a preliminary finite-element analysis on the thermal and thermomechanical performance of the two types of packaging approaches. For both, we assumed that the chip was 1×1 mm^2 and it generated 1 W of heat. Using thermal properties of all the known packaging materials [4] and those of the sintered silver, we found that the junction-to-case thermal resistance in our proposed package was reduced by a factor of three compared with that in the flip-chip package (see Figure 4.14 for the temperature distributions in the two packages). By assuming that the packages were in the stress-free state at the respective die-attach temperatures, we analyzed the stresses generated due to mismatched CTE in the two structures during their operation. We found that the maximum thermomechanical stress in our package was more than a factor of five smaller than that in the solder bumps of the flip-chip package (see Figure 4.15). This large reduction in thermomechanical stresses came from two contributions: one was due to better thermal performance in our package which resulted in a smaller temperature rise; the other was attributed to the porous sintered silver whose elastic modulus was a only fraction of that of the solder material used in the flip-chip package. Furthermore, since solder was known to cause fatigue failure, we expected that our package would be significantly improved in long-term reliability.



(a) (b)

Figure 4.14. FEM thermal modeling of the temperature distributions in our proposed LED package versus the flip-chip LED package.



(a) (b)

Figure 4.15. FEM modeling of thermomechanical stress distributions in the packaged LED devices versus that in the flip-chip LED device during operation (the stress-free state was assumed to be at the respective die-attach temperatures).

Some tiny (0.07-mm^2 die area) white GaN LEDs with sapphire substrates obtained from Lumileds Lighting LLC (San Jose, CA) were used to demonstrate the advantages of the low-temperature sintered silver as a better die-attach materials. The device was used for manufacturing the conventional "5-mm lamp".

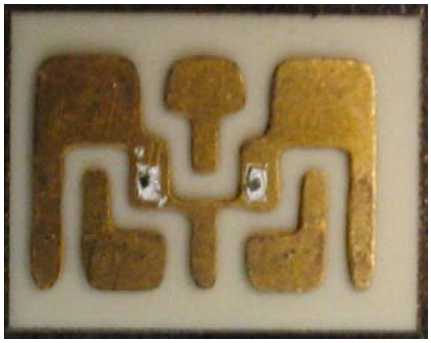


Figure 4.16. Low-temperature sintered silver die-attached LEDs. The two white parts are dispensed-silver after low-temperature sintering and the two blacks squares are two die-attached LEDs.

During the LED silver die-attachment, nickel and gold were electroless-plated on to an etched aluminum oxide DBC substrates. Chromium, nickel and silver were also e-beamed onto the sapphire substrates of the LED devices for the silver bonding. Then nanoscale silver paste was dispensed onto the nickel/gold coated DBC patterns. After the LED die-attachment, the silver paste was sintered to form the silver joints. Two finished samples at this stage are shown in Figure 4.16. At last, gold wires were bonded from the anode and cathode electrodes (gold) of the LEDs. For comparison, the conductive epoxy die-attached samples were also prepared.

After the experiment, it was found that the low-temperature sintered silver die-attached LEDs could power up at least 2 times as much as power without failure compared to the conventional way of die-attaching using conductive epoxy curing.

4.4 Summary

As a summary, the applications of the low-temperature silver sintering technologies in single-chip power package, multi-chip power module, and power white LEDs have been demonstrated at the conceptual levels. Some finite-elemental analysis and preliminary experiment results based on the prototypes demonstrated the potential advantages of the interconnect technology in the high-power packaging.

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Chapter 5
Summary and Conclusions

Power device interconnections are extremely important in power electronics packaging since they are limits for electrical performance, thermal management, integration, reliability and cost of power systems. The state-of-the-art solder and wirebond interconnect technologies cannot meet the future power electronics requirement due to their inherited limitations. Especially, the adoption of wide-bandgap semiconductor devices in power electronics demands a new generation of advanced interconnecting materials and packaging technologies with larger operating temperature scales. In this study, we formulated a nanoscale silver paste as a novel interconnect material and developed the subsequent low-temperature sintering technology as a lead-free joint method. The electrical, thermal and mechanical features of sintered silver material and sintered silver joints indicate that the low-temperature silver sintering technology can be applied into single-chip power packaging, multi-chip power module packaging, and other high-power device interconnections with many potential advantages. In the following paragraphs, the conclusions and significance of this research are further elaborated.

5.1 Low-Temperature Silver Sintering Technology

Nanoscale silver pastes were formulated by adding dispersant/binder/thinner into nano-silver particles. It has been found that by reducing the silver particle size down to nanoscale, the sintering temperature of the silver pastes dropped from above 600°C to below 300°C. This is a temperature low enough for bonding most types of semiconductor devices. It is found that the sintering temperature of the nanoscale silver pastes is controlled by the burnout of the organic components inside the pastes. After sintering, the nano-silver particles are densified into a material with about 20% microscale porosity.

The low-temperature sintered silver has 3-5 times of electrical and thermal conductivities of the common solders. Furthermore, the low elastic modulus of the sintered silver material makes it a good thermal stress buffer for the semiconductor-metallized substrate bondings. To fabricate the sintered silver joints, Ni/Ag metallized SiC power devices are die-attached onto either Ni/Ag or Ni/Au coated DBC or copper substrates to form the silver bondings. After a 40-min dwell sintering at 300°C, it is found that the low-temperature sintered silver joint has excellent electrical, thermal, and mechanical performance such as low joint resistance, highly-uniform bondings, and high bonding strengths. The 50-250°C thermal cycling experiments on the sintered silver joints demonstrate their improved high-temperature capability. The drops of the bonding strength after the thermal cycling can be explained by the nucleation and growth of the micro-cavities at the microscale grain boundaries of the low-temperature sintered silver.

As a summary, this research demonstrates the feasibility and potential advantages of using a method of solidus sintering/interdiffusion to bond power chips. The method is quite different from the traditional liquidus solder reflow. Nanoscale silver pastes and their subsequent low-temperature sintering technology are developed for power electronic packaging application.

5.2 Applications of Sintered Silver Joints

The applications of the low-temperature sintered silver joints are demonstrated in single-chip power packaging, multi-chip power module packaging, and other high power device packaging such as light emitting diodes. Preliminary results have shown that the silver joints have electrical, thermal, and mechanical advantages compared to the conventional interconnect materials and packaging technologies such as solder reflows and conductive epoxy curing.

5.3 Recommendations for Future Work

Solidus sintering/interdiffusion for bonding semiconductor devices is relatively new topic in electronic packaging and the exploration in this dissertation research is far from completion. However, it enables industry to appreciate the technology for further progress. The following research topics are recommended by the author to further improve the low-temperature sintering technology.

5.3.1 Formulation of Nano-Pastes for Larger Joints

Because of the organic components burnout problems during the covered silver sintering, the prepared nanoscale silver pastes so far were found only good for 4×4 mm^2 or less bonding areas. Any area larger may have a component-burnout problem. Although several strategies such as increase of silver loading, small patterning, organic evaporating before covering, and prolonged sintering have been taken to improve the bonding quality for the silver joints, the problems have yet been completely solved. As discussed in Chapter 3, the last strategy has yet been tried is to add proper oxygen agents in the silver pastes to help the organic burnout.

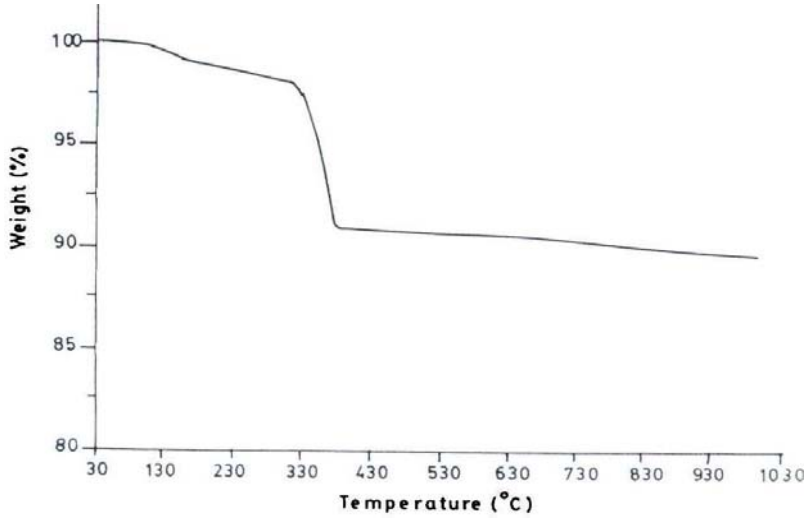
Ag_2O or AgO are possible candidates for the oxygen agents to be added into nanoscale silver because in both cases only silver is left after the decomposition. However, TGA curves of the microscale Ag_2O or AgO powders as shown in Figure 5.1 reveal both powders cannot decomposite into pure silver at temperatures below 300°C [1]. The possibility for success is to reduce the size of Ag_2O or AgO particles into nanoscale so that the decompositions could happen at lower temperatures.

5.3.2 Formulation of Nano-Pastes Sinterable at Lower Temperatures

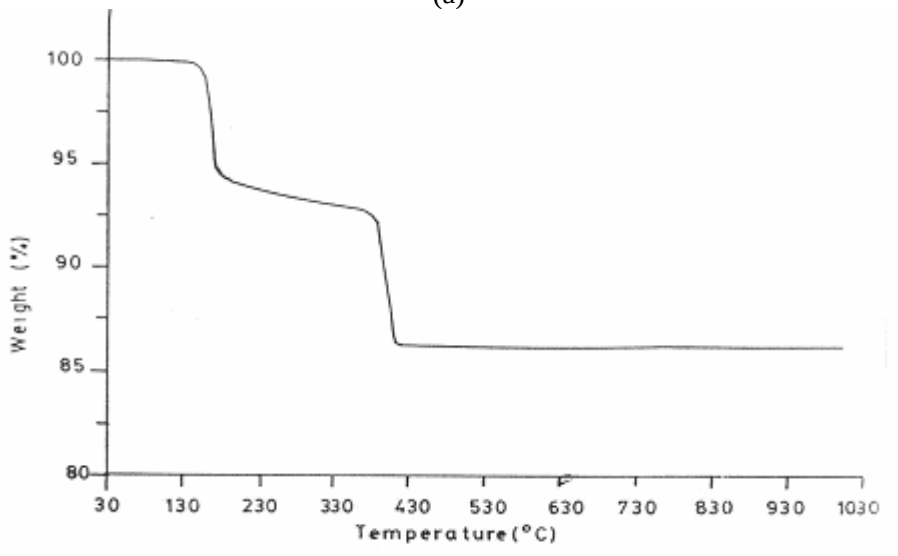
It is always desirable to further reduce the processing temperatures of the nanoscale silver pastes. As discussed before, for small enough nano-silver particles, the sintering temperatures of the silver paste are controlled by the burnout temperature of organic components in the paste. Therefore, it is possible to further reduce the sintering temperature by replacing current organic components with those having lower burnout temperatures. However, as discussed in Chapter 2, the selection of organic components

for a paste must be a balance between the burnout temperatures of the components and their functionalities for the paste formulation.

Also, one may switch to even smaller nanosilver particles to enhance the sintering and densification at further reduced sintering temperatures. As discussed in Chapter 1, the prevention of the agglomeration/aggregation is the most important to use the nanoparticles properly.



(a)



(b)

Figure 5.1. TGA curves of microscale Ag_2O (a) and AgO (b).

5.3.3 Solutions for Silver Migration

Migration of conductive materials such as silver, solder, and even copper in a power package under electrical bias and moisture is a well known phenomenon. However,

special attention must be paid to silver migration because it is usually much more severe due to the high mobility of silver. In the dry air case, oxygen is typically involved in the silver migration by following two reactions [2,3]:

$Ag_2O \rightarrow 2Ag^+ + ½O2 + 2e^-$,

Ag (metal) $\rightarrow Ag^+ + e^-$.

Therefore, the initial oxygen layers in the silver electrodes play an important role in the silver migration. At higher temperatures, the first reaction is enhanced since silver oxide is unstable at temperature above 300°C.

In the case of humid environment, the silver migration could become more severe due to very complex migration mechanisms usually involved in the H^+ and OH^- ions of water [4].

In conclusion, both electrical bias and high-temperature can enhance the silver migration such that silver migration could quickly become a dominant failure mode in a power package [5]. Furthermore, both oxygen and water can cause the situation severer. Therefore, proper underfill and encapsulation to protect the low-temperature sintered silver from oxygen and humidity are important. After proper encapsulation, the selected hermetic material and structure should serve as a direct barrier in the silver migration path as well as a prevention of air and moistures.

5.3.4 Implementation of Sintered Silver Joints in Applications

We demonstrated the feasibility of applying low-temperature sintered silver joints in power electronics and high power light emitting diodes. But the demonstration is mostly on a conceptual level, it is worthwhile and technically important to build-up more prototypes by using this newly developed interconnect material and packaging technology.

References

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Appendix A
Processing of DBC or Cu Substrates for Silver Joints

A.1 Introduction to Direct Bond Copper (DBC) Substrates*

DBC means Direct Bond Copper (or Direct Copper Bonding) and denotes a process in which copper and a ceramic material are directly bonded. Normally, DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) or aluminum-nitride (AlN) ceramic base. The DBC process yields a super-thin base and eliminates the need for the thick, heavy copper bases that were used prior to this process. Because power modules with DBC bases have fewer layers, they have much lower thermal resistance values and because the expansion coefficient matches silicon, they have much better power cycling capabilities (up to 50,000 cycles). Properties of DBC ceramic substrates include:

- Good mechanical strength; mechanically stable shape, good adhesion and corrosion resistant;
- Excellent electrical insulation;
- Very good thermal conductivity;
- Superb thermal cycling stability;
- The thermal expansion coefficient is close to that of silicon, so no interface layers are required;
- Good heat spreading;
- May be structured just like printed circuit boards or insulated metal substrates;
- Environmentally clean.

* Content from IXYS Corporation Semiconductor Data Book, 1998.

Their advantages to users include:

- The 0.3 mm thick copper layer permits higher current loading for the same conductor width. Assuming the same copper cross-section the conductor needs to be only 12% of that of a normal printed circuit board;
- The excellent thermal conductivity provides the possibility of very close packaging of the chips. This translates into more power per unit of volume and improved reliability of systems and equipment;
- The high insulation voltage results in improved personnel safety;
- DBC ceramic is the basis for the "chip-on-board" technology which represents the packaging trend for the future.

DBC ceramic substrates are the base materials of the future for both the construction and the interconnection techniques of electronic circuits. They will be employed as base material for electronic components with high values of power dissipation and demanding requirements concerning their thermal shock behavior as well as their failure rate, whenever normal printed circuit boards are no longer adequate. Application examples for DBC include:

- Power hybrids and power control circuits;
- Power semiconductor modules;
- Smart power building blocks;
- Solid state relays;
- High frequency switch mode power supplies (SMPS);
- Electronic heating devices;
- Building blocks for automobile electronics, the military as well as aerospace technology.

Following tables include the properties and design parameter data for the DBC substrates.

Table A.1(a). Properties and parameters of commonly available DBC substrates.

Uncladed ceramic	**Aluminum oxide DBC**	**Aluminum nitride DBC**
Purity	≥ 96%	≥ 97%
Dielectric strength	10 kV/mm	~14 kV/mm
Electrical resistivity	$>10^{14}$ Ωcm	$>10^{14}$ Ωcm
Thermal conductivity	24-28 W/mK	≥ 150 W/mK
Dimensions maximum	138×178 mm (5.4"×7.0")	75×57 mm (2.95"×2.24")
Thickness	Standard: 0.63, 0.38, 0.25 mm (25, 15, 10 mil)	Standard: 0.63 mm (25 mil)

Table A.1(b). Properties and parameters of commonly available DBC substrates.

Claded ceramic	Aluminum oxide DBC	Aluminum nitride DBC
Surface finish	Cu or (electroless) nickel plated Cu	Cu or (electroless) nickel plated Cu
Cu thickness	Standard: 0.3 mm (12 mil)	Standard: 0.3 mm (12 mil)
Ni thickness	Max. 7 µm (0.28 mil)	Max. 7 µm (0.28 mil)
Usable metallized area	Max. 127×169 mm (5.00"×6.65")	Max. 73×55 mm (2.87"×2.17")
Total thickness (resp. Cu-AlN-Cu)	Standard: 1230 µm (48 mil)	Standard: 1230 µm (48 mil)
Cu bonding strength	≥ 6 N/mm; 34.3 lb/inch (in accordance with DIN 53 289)	≥ 3 N/mm; 17.2 lb/inch (in accordance with DIN 53 289)
Thermal expansion coefficient	7.4×10^{-6} K^{-1} @ (50 - 200)°C	5×10^{-6} K^{-1} @ (50 - 200)°C
Application temperature (inert atmosphere)	-55 ... +850°C	55 ... +850°C
Hydrogen embrittlement	Up to 400°C	Up to 380°C

Table A.2. Design rules for DBC substrates.

Dimensions	Application dependent for aluminum oxide DBC	Application dependent for aluminum nitride DBC
Minimum width of Cu pattern*	0.5 mm (19.7 mil)	0.5 mm (19.7 mil)
Minimum spacing between Cu patterns*	0.5 mm (19.7 mil)	0.5 mm (19.7 mil)
Minimum spacing between Cu pattern and ceramic edge	0.35 mm (13.8 mil)	0.35 mm (13.8 mil)

*Dependent on copper thickness.

A.2 Etching of DBC Substrates

As described in last section, in the aluminum oxide or aluminum nitride DBC substrates, the ceramic layers have significantly higher thermal conductivities than the glass fiber-reinforced polymer boards such as printed circuit boards of FR-4 [1;2], which is good for heat spreading in high-power applications. The thick copper layer is also good for high current carriage in the applications [3]. Since the DBC substrates could meet the demands of both heat spreading and high current carriage for high-power electronics packaging, they were chosen for making the low-temperature sintered silver joints in this research.

The aluminum oxide and aluminum nitride DBC substrates with the ceramic layers 25-mil thick and the copper layers 12-mil thick were used in this study. They were

bought commercially from IXYS Corporation (Santa Clara, CA). During the etching of DBC substrates, the substrates were first use a brush and a mild detergent to scrub the surface and then rinse thoroughly and then ultrasonically cleaned using a degreasing detergent and alcohol. Then the cleaned DBC substrates were baked at about 70°C to remove moisture. Then photo-imaginable etch-resist (PHOTRAK ETP240, Electra Polymers & Chemicals Inc., Santa Charles, IL) was either screen-printed (for large areas >2×2 inch^2) or spinning-coated (for small areas ≤2×2 inch^2) onto the DBC substrates. The thickness of the coating layer can be controlled either by the screen placement or spinning speeds so as to get an etch-resist layer with a thickness of 8-10 μm after baking. The baking of etch-resist layers was processed in open-air environment at 80 to 85°C for at least 40 mins. All the above process of etch-resist was done in a darkroom.

The etch patterns are usually designed using an AutoCAD program. After the design of etch patterns, the patterns were printed on a white paper with the black areas for etching-off. Then the patterns on the paper are transferred to a clear receiver film using a negative paper. During the etch pattern design, one of the important issues need to consider is the over-etch problem. Since etching of the substrates are normally done in ferric chloride solution and the etching procedure is isotropic, the degree of over-etching is also increased with the thicker copper patterns. The phenomena of over-etch are shown in Figure A.1. Other issues like the thickness of AutoCAD drawing lines and the printer tolerant must be considered. It is good to use the drawing lines of 0.00 mm in thickness in the AutoCAD program for the finest line printing.

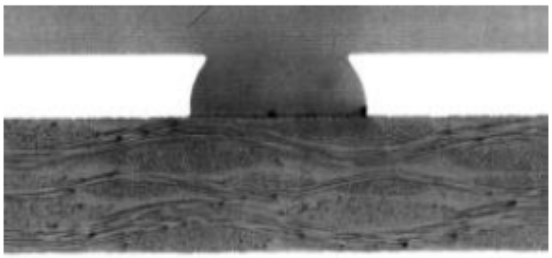

Figure A.1. The over-etch phenomena during the isotropic etching of DBC substrates. For the etching of 0.3 mm DBC Cu layer, the over-etching is about 0.1 mm (100 μm).

After the etch patterns transferred onto the clear receiver films, the films were used to cover the baked etch-resist films and exposed in a flatbed ultraviolet (UV) exposure unit for 20 to 30 mins. After exposure, the substrates were immersed in a diluted (1:10 or so) developer solution to produce the etch patterns on the DBC

substrates. The etch-resist of covered areas will be wash away in the developer solution. Compared with most photoresists and solder masks, etch-resist can be developed much faster in about 2 mins. Therefore, diluted developer solution must be used and the developing procedure must be monitored carefully to avoid the over-develop problem.

A $FeCl_3$ spray etcher is used for the etching of the exposed DBC copper layers. It is usually takes about 30-60 mins to finish etching a 0.3-mm thick copper layer on DBC. During the time, the DBC substrates need to relocate in the spray etcher every 10 mins to achieve more uniform etch.

Figure A.2 shows examples of etched patterns on an aluminum oxide DBC substrate for packaging white LEDs.

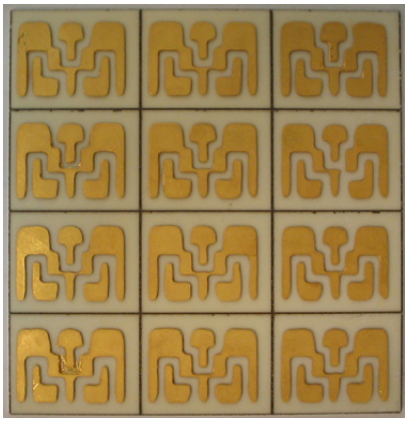

Figure A.2. The etched aluminum oxide DBC substrate for packaging white LEDs.

A.3 Metallization of DBC and Cu Substrates for Silver Joints

To form strong bondings by the low-temperature silver sintering, gold or silver are needed to coat onto the etched DBC substrates or copper substrates. Before the gold or silver coating, a thin layer of nickel is usually coated onto the copper substrates to prevent the copper/silver or copper/gold interdiffusion and the copper oxidation. Therefore, metallization of the DBC and Cu substrates for the sintered silver joints involves the coating of nickel, gold or silver. Theoretically, both physical (like sputtering or e-beam) and chemical (like electroplating or electroless-plating) metal deposition methods are possible for these metal depositions. However, a proper metallization method was selected after considering the quality and ease of the processing. Electroless-plating can provide good quality of coating films and it is an effective way to deposit

nickel, gold, or silver onto discontinued copper patterns and therefore the methods were chosen in this research.

A.3.1 Nickel Deposition

The nickel electroless-plating involves the preparation of chemical solutions and subsequent plating process. Four bottles of solutions—acid cleaner, microetcher, initiator, and nickel plating solutions are usually needed to prepare. The pH value of the prepared nickel plating solution also needed to be adjusted when it is necessary. The preparation of the four solutions is described in Table A.3.

Table A.3. Preparation Instructions of Chemical Compositions for Nickel Electroless-Plating

(1). ACID CLEANER (700mL) 1) 500mL DI H_2O 2) 20-30% (140-210mL) PC-455 *(180mL)* 3) Top off to 700mL if under
(2). MICROETCHER (700mL) 1) 500mL DI H_2O 2) 1-2% (7-14mL) Sulfuric Acid, H_2SO_4 *(10mL)* 3) Cool to 21-30°C *(25°C)* 4) Stir slowly and carefully while adding 42-84g of AD-485 *(65g)* 5) Top off to 700mL if under
(3). INITIATOR (700mL) 1) 400mL DI H_2O 2) Stir slowly and carefully while adding 3% (21mL) Hydrochloric Acid HCl 3) Stir slowly and carefully while adding 2% (14mL) Initiator 852 4) Top off to 700mL if under
(4). NICKEL PLATING (750mL) 1) 500mL DI H_2O 2) 6% (45mL) Ni-8600A 3) 20% (150mL) Ni-8600B 4) Top off to 750mL if under 5) Pre-heat solution to 85°C 6) PH should be 4.7-4.9, adjust as needed (see below)
PH ADJUSTMENTER 1) Mix 1:3 ratio of Ammonium Hydroxide, NH_4OH, with DI H_2O in order to increase the PH 2) Mix 1:4 ration of Sulfuric Acid, H_2SO_4, with DI H_2O in order to decrease the PH 3) Add either 1) or 2) in small amounts checking PH frequently until 4.7-4.9

NOTES: (i). Clean all beakers thoroughly before all usage; (ii). Italic characters are median values; (iii). Percentages are for total batch size.

After the preparation of the nickel electroless-plating solutions, four clean beakers and two thermal baths are needed for the electroless-plating. The following plating process described in Table A.4 was followed.

Table A.4. Nickel Electroless-plating process

1) Beaker 1, Acid Clean 5 minutes @ 45°C DI H_2O wash for 2-5 min
2) Beaker 2, Microetch* No more than 2 minutes *(1 min 45 sec)* @ 21-27°C *(25°C)* DI H_2O wash for 2-5 min
3) Beaker 3, Initiator 2 minutes @ Room Temp DI H_2O wash for 2 min 4) Beaker 4, Nickel Plating** 30 minutes @ 85°C (in heated bath) for 0.24-0.4 mils DI H_2O wash for 1-3 min

*Microetch (step 2) is not good for sputtered layers. **After 30 minutes air (or at least I'm assuming they are air) bubbles will appear and the Ni surface is not at smooth and nice anymore.

After the nickel electroless-plating, thickness of the nickel layer measured about 6-8 microns. It is thick enough for the interdiffusion and oxidation prevention.

A.3.2 Gold Deposition

The gold electroless-plating solutions (gold(I) potassium cyanide, tonic) were bought from Alfa Aesar (Ward Hill, MA) with stock # 42307. The gold plating solution can deposit thin films of 24 Kt gold on nickel, nickel coated or copper surfaces without the use of anodes or current. The deposit is extremely dense with no variance in thickness on any area or recess reached by the solution. The solution is able to deposit gold in a thickness 0.5-2 micron. The thickness is enough for our applications.

Table A.5. Gold Electroless-plating process

pH*	5.0-5.5
Agitation	Preferred but not heavily
Time	30-60 mins
Temperature	65-75°C (using glass beaker in a thermal bath)
Tank	Glass lined or plastic lined steel
Deposition rate	0.05-0.075 micron/minute for a maximum of 0.2 micron in 30 mins at 71°C. The thickness of the gold can be increased up to 0.4~0.5 micron at a higher temperature of 75°C
Coverage	Assuming 50% of the gold is used, the coverage will be approximately 635 in^2/l for an average thickness of 0.125 micron

*The pH has a tendency to drop with use. It can be adjusted by adding small amounts of concentrated ammonium hydroxide.

Before the gold deposition, the surface of the object to be plated should be thoroughly cleaned. First, use a brush and a mild detergent to scrub the surface and then rinse thoroughly. Next use a dilute hydrochloric acid solution to remove any surface

oxides and rinse thoroughly. However, if we could plate gold onto the nickel-plated substrates right away, the nickel as-coated layers are clean enough and these steps can be skipped.

The operating conditions of the gold electroless-plating are described in Table A.5.

A nickel and gold electroless-plated aluminum nitride DBC substrate sample is as shown in Figure A.3.

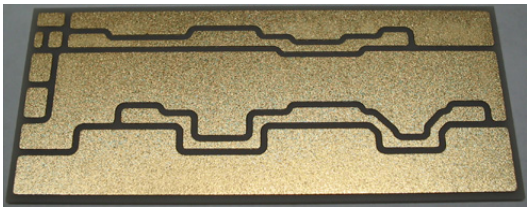

Figure A.3. An nickel and gold electroless-plated aluminum nitride DBC substrate sample.

A.3.3 Silver Deposition

The silver electroless-plating solutions were also bought from Alfa Aesar (Ward Hill, MA) with stock # 44068. The silver plating solution can deposit thin and uniform layers of bright silver by an electroless immersion process. The process operates by an electroless displacement of base metals by silver brought about by a difference in the electromotive force (EMF) potentials. The product is designed to produce bright silver plating on copper, brass and copper alloys with excellent adhesion. Plating occurs on other metals with varying degrees of adhesion.

Table A.6. Silver Electroless-plating process

pH*	11
Time	5-10 minutes
Temperature	90°C (using Pyrex glass beaker in a thermal bath)
Tank	Pyrex glass
Bath life	To exhaustion of silver
Storage	Room temperature
Plating capacity	8 grams silver metal per gallon. Equivalent to 55 square feet coating at 1 mg per square inch. The coating thickness can up to about 0.2 μm

Other electroless-plating methods can be found in Ref. [4]

Another option to plate silver more quickly and thick is to electroplating. As an example, silver electroplating solution can be made from silver cyanide (36 g/L), potassium cyanide (60 g/L), and potassium carbonate (45 g/L) [5].The silver plating can

be carried out at room temperature with a current density at 5-15 A/ft^2. Agitation in terms of cathode rod movement is desirable during the plating.

An important requirement in silver plating is that a preliminary silver "strike" operation, which is essential prior to silver plating. The silver strike paths and operating conditions can be found in pp.111-112 in Ref. [5].

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Appendix B

Datasheets of Power Devices Used in This Research

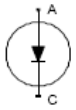
B.1 Infineon SIDC24D30SIC3 Silicon Carbide Schottky Diodes†

FEATURES:

- Revolutionary semiconductor material - Silicon Carbide
- Switching behavior benchmark
- No reverse recovery
- No temperature influence on the switching behavior
- No forward recovery

Applications:

- SMPS, snubber, secondary side rectification



Chip Type	V_{BR}	I_F	Die Size	Package	Ordering Code
SIDC24D30SIC3	300V	10A	1.706 x 1.38 mm^2	sawn on foil	Q67050-A4163-A103

MECHANICAL PARAMETER:

Raster size	1.706x 1.38	mm
Anode pad size	1.405 x 1.08	
Area total / active	2.354 / 1.548	mm^2
Thickness	355	µm
Wafer size	75	mm
Flat position	0	deg
Max. possible chips per wafer	1649 pcs	
Passivation frontside	Photoimide	
Anode metalization	3200 nm Al	
Cathode metalization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	Electrically conductive glue or solder	
Wire bond	Al, ≤ 350µm	
Reject Ink Dot Size	∅ ≥ 0.3 mm	
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

† Infineon Technologies Technical Datasheet.

Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Repetitive peak reverse voltage	V_{RRM}		300	V
Surge peak reverse voltage	V_{RSM}		300	
Continuous forward current limited by T_{jmax}	I_F		10	A
Single pulse forward current (depending on wire bond configuration)	I_{FSM}	T_C =25°C, t_P =10 ms sinusoidal	36	
Maximum repetitive forward current limited by T_{jmax}	I_{FRM}	T_C = 100°C, T_j=150°C, D=0.1	45	
Non repetitive peak forward current	I_{FMAX}	T_C =25°C, tp=10µs	100	
Operating junction and storage temperature	T_j , T_{stg}		-55...+175	°C

Static Electrical Characteristics (tested on chip), T_j=25 °C, unless otherwise specified

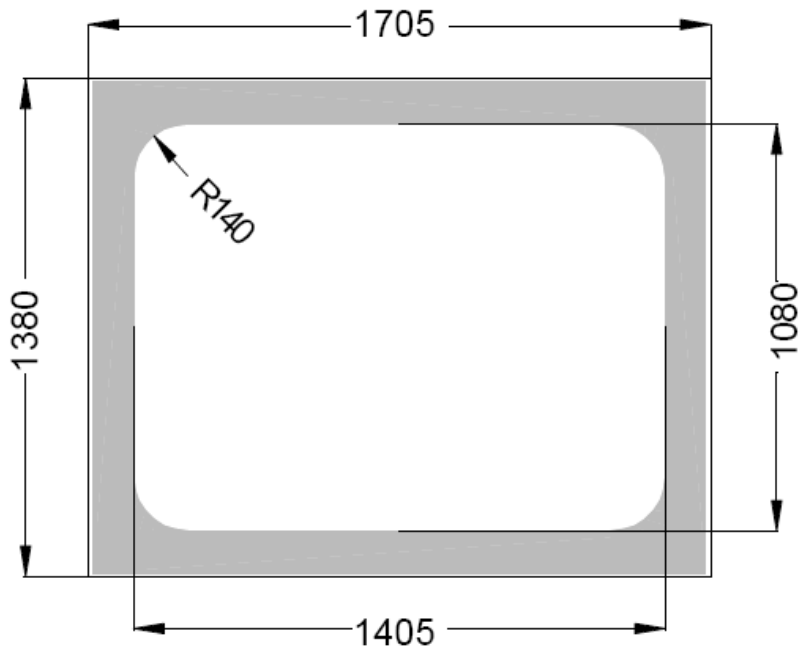
Parameter	Symbol	Conditions		Value			Unit
				min.	Typ.	max.	
Reverse leakage current	I_R	V_R=300V	T_j=25°C		15	200	µA
Forward voltage drop	V_F	I_F=10A	T_j=25°C		1.5	1.7	V

Dynamic Electrical Characteristics, at T_j = 25 °C, unless otherwise specified, tested at component

Parameter	Symbol	Conditions		Value			Unit
				min.	Typ.	max.	
Total capacitive charge	Q_C	I_F=10A di/dt=200A/µs V_R=200V	T_j = 150 °C		23		nC
Switching time	t_{rr}	I_F=10A di/dt=200A/µs V_R= 200V	T_j = 150 °C		n.a.		ns
Total capacitance	C	I_F=10A di/dt=200A/µs T_j=25°C f=1MHz	V_R=1V		600		pF
			V_R=150V		55		
			V_R=300V		40		

Edited by INFINEON Technologies, AI PS DD HV3, Edition 1, 22.04.2004

CHIP DRAWING:



FURTHER ELECTRICAL CHARACTERISTICS:

This chip data sheet refers to the device data sheet	INFINEON TECHNOLOGIES	SDP10S30

Description:

AQL 0,65 for visual inspection according to failure catalog

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Test-Normen Villach/Prüffeld

Published by
Infineon Technologies AG
Bereich Kommunikation
St.-Martin-Strasse 53
D-81541 München

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B.2 CREE CPWR-0600S010 Silicon Carbide Schottky Diodes‡

CREE POWER

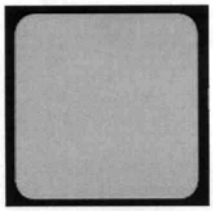
CPWR-0600S010

ZERO RECOVERY™ RECTIFIER
600V, 10A, CHIP

Features

- 600 Volt Schottky Rectifier
- Zero Reverse Recovery
- Zero Forward Recovery
- High Frequency Operation
- Temperature Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F

Chip Outline



Maximum Ratings

Parameter	Symbol	Value	Unit
Repetitive Peak Reverse Voltage	V_{RRM}	600	V
Surge Peak Reverse Voltage	V_{RSM}	600	V
DC Blocking Voltage	V_{DC}	600	V
Average Forward Current T_J=175°C	$I_{F(AV)}$	10	A
Repetitive Peak Forward Surge Current T_C=25°C, t_p=8.3ms, Half Sine Wave	I_{FRM}	50	A
Non Repetitive Peak Forward Surge Current T_C=25°C, t_p=10µs, Pulse	I_{FSM}	250	A
Operating Junction and Storage Temperature	T_J , T_{stg}	-55 to +175	°C

‡ CREE Power Technical Datasheet.

ELECTRICAL CHARACTERISTICS

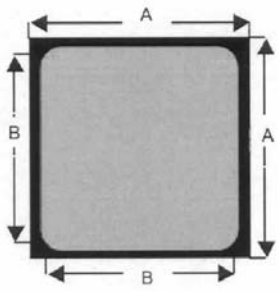
Parameter	Symbol	Min	Typ	Max	Units
Forward Voltage I_F = 10A T_J=25°C I_F = 10A T_J=150°C	V_F		1.6 2.0	1.8 2.4	V
Reverse Current V_R = 600V T_J=25°C V_R = 600V T_J=150°C	I_R		50 100	200 1000	µA
Total Capacitive Charge V_R = 600V,I_F = 10A, di/dt = 500 A/µs, T_J = 25°C	Q_C		40		nC
Total Capacitance V_R = 0V, T_J = 25°C, f =1MHz V_R = 200V, T_J = 25°C, f =1MHz V_R = 400V, T_J = 25°C, f =1MHz	C		550 65 50		pF

NOTE:
1. This is a majority carrier diode, so there is no reverse recovery charge.

MECHANICAL PARAMETERS

Die Size	2.26 x 2.26	mm
Anode Pad Size	2.12 x 2.12	mm
Anode Pad Opening	2.01 x 2.01	mm
Thickness	350	µm
Wafer Size	75	mm
Anode Metalization (Al)	4	µm
Anode Metalization (Ni/Ag)	3.5	µm
Cathode Metalization (Ni/Ag)	0.8	µm
Frontside Passivation	Polyimide	

Chip Dimensions



symbol	dimension	
	mm	inch
A	2.26	0.0889
B	2.14	0.0843

Part Number	Anode	Cathode	Package	Marking
CPWR-0600S010B	Al	Ni/Ag	Sawn on Foil	Wafer # on Foil
CPWR-0600S010C	Ni/Ag	Ni/Ag	Sawn on Foil	Wafer # on Foil

This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems, or weapons systems.

Cree, Inc.
Power Products
4600 Silicon Drive • Durham, NC 27703 • USA
Tel: 919-313-5300 • Fax: 919-313-5451
www.cree.com

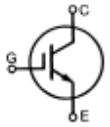
B.3 IXYS Corporation IXSH35N120A Single-Chip Packaged IGBT[§]

IXYS

High Voltage, High speed IGBT — **IXSH 35N120A**

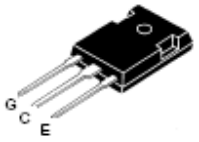
V_{CES} = 1200 V
I_{C25} = 70 A
$V_{CE(sat)}$ = 4 V

Short Circuit SOA Capability



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1200	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	70	A
I_{C90}	T_C = 90°C	35	A
I_{CM}	T_C = 25°C, 1 ms	140	A
SSOA (RBSOA)	V_{GE} = 15 V, T_J = 125°C, R_G = 22 Ω Clamped inductive load, L = 30 µH	I_{CM} = 70 @ 0.8 V_{CES}	A
t_{SC} (SCSOA)	V_{GE} = 15 V, V_{CE} = 0.6 • V_{CES}, T_J = 125°C R_G = 22 Ω, non repetitive	10	µs
P_C	T_C = 25°C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		6	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-247 AD



G = Gate, C = Collector,
E = Emitter, TAB = Collector

Features

- International standard package JEDEC TO-247
- High frequency IGBT with guaranteed Short Circuit SOA capability
- Fast Fall Time for switching speeds up to 20 kHz
- 2nd generation HDMOS™ process
- Low $V_{CE(sat)}$
  - for minimum on-state conduction losses
- MOS Gate turn-on
  - drive simplicity

Applications

- AC motor speed control
- DC servo and robot drive
- Uninterruptible power supplies (UPS)
- Switch-mode and resonant-mode power supplies
- Welding

Advantages

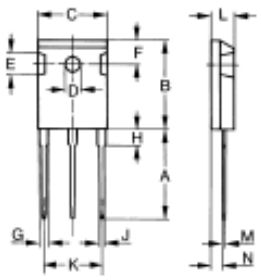
- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- High power density

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{CES}	I_C = 3 mA, V_{GE} = 0 V		1200			V
$V_{GE(th)}$	I_C = 4 mA, V_{CE} = V_{GE}		4	6	8	V
I_{CES}	V_{CE} = 0.8 • V_{CES} V_{GE} = 0 V	T_J = 25°C T_J = 125°C			400 1.2	µA mA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
$V_{CE(sat)}$	I_C = I_{C90}, V_{GE} = 15 V				4	V

§ IXYS Corporation Technical Datasheet.

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	$I_C = I_{C90}$; V_{CE} = 10 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %	20	26		S
$I_{C(on)}$	V_{GE} = 15 V, V_{CE} = 10 V		170		A
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		3750		pF
C_{oes}			235		pF
C_{res}			60		pF
Q_g	$I_C = I_{C90}$, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}		150	190	nC
Q_{ge}			40	60	nC
Q_{gc}			70	100	nC
$t_{d(on)}$	Inductive load, T_J = 25°C		80		ns
t_{ri}	$I_C = I_{C90}$, V_{GE} = 15 V, L = 100 µH		150		ns
$t_{d(off)}$	V_{CE} = 0.8 V_{CES}, R_G = 2.7 Ω		400	900	ns
t_{fi}	Remarks: Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G		500	700	ns
E_{off}			10		mJ
$t_{d(on)}$	Inductive load, T_J = 125°C		80		ns
t_{ri}	$I_C = I_{C90}$, V_{GE} = 15 V, L = 100 µH		150		ns
E_{on}	V_{CE} = 0.8 V_{CES}, R_G = 2.7 Ω		2.5		mJ
$t_{d(off)}$	Remarks: Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G		400		ns
t_{fi}			700		ns
E_{off}			15		mJ
R_{thJC}				0.42	K/W
R_{thCK}			0.25		K/W

TO-247 AD (IXSH) Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	19.81	20.32	0.780	0.800
B	20.80	21.46	0.819	0.845
C	15.75	16.26	0.610	0.640
D	3.55	3.65	0.140	0.144
E	4.32	5.49	0.170	0.216
F	5.4	6.2	0.212	0.244
G	1.65	2.13	0.065	0.084
H	-	4.5	-	0.177
J	1.0	1.4	0.040	0.055
K	10.8	11.0	0.426	0.433
L	4.7	5.3	0.185	0.209
M	0.4	0.8	0.016	0.031
N	1.5	2.49	0.057	0.102

Fig.1 Saturation Characteristics

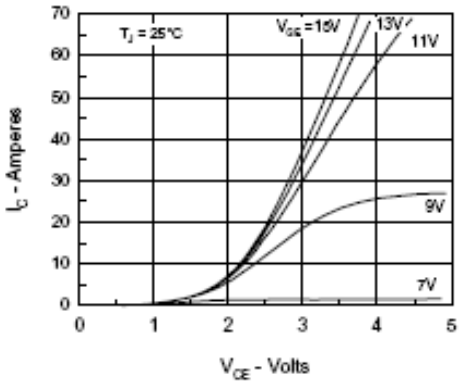


Fig.2 Output Characterstics

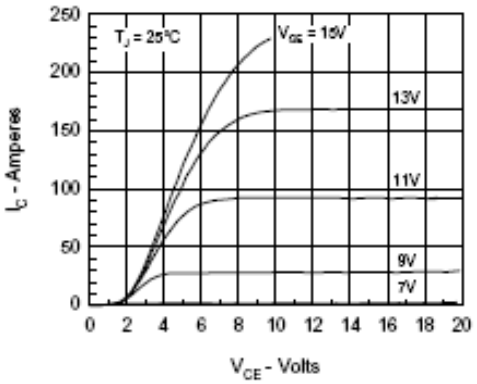


Fig.3 Collector-Emitter Voltage vs. Gate-Emitter Voltage

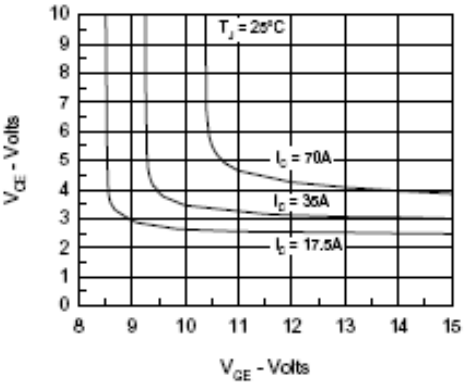


Fig.4 Temperature Dependence of Output Saturation Voltage

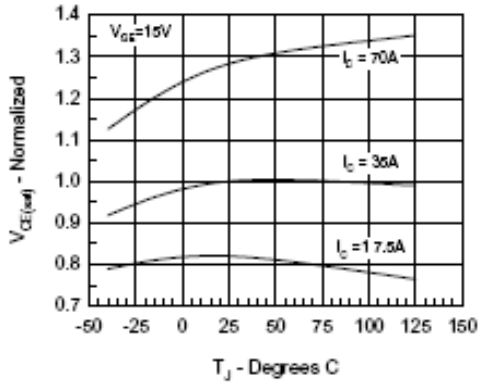


Fig.5 Input Admittance

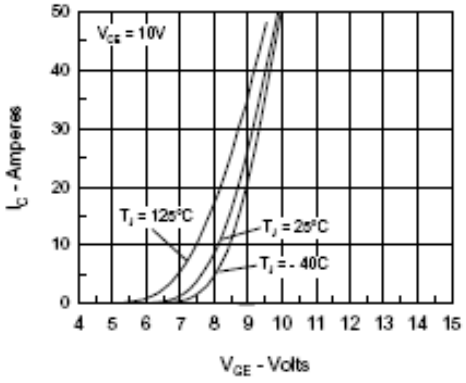


Fig.6 Temperature Dependence of Breakdown and Threshold Voltage

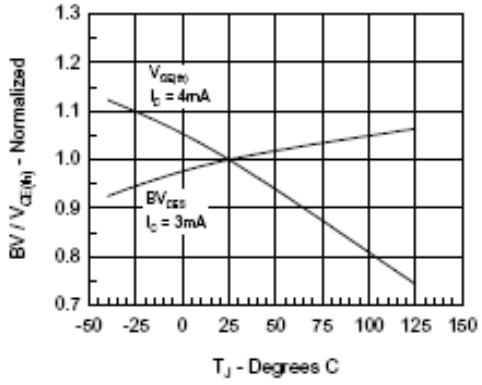


Fig.7 Turn-Off Energy per Pulse and Fall Time on Collector Current

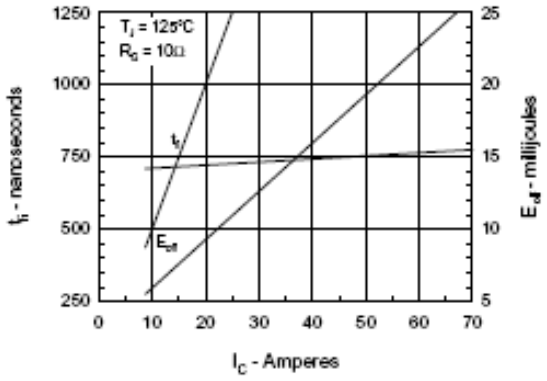


Fig.8 Dependence of Turn-Off Energy Per Pulse and Fall Time on R_G

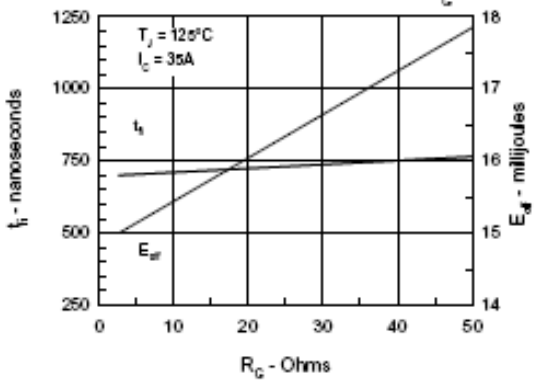


Fig.9 Gate Charge Characteristic Curve

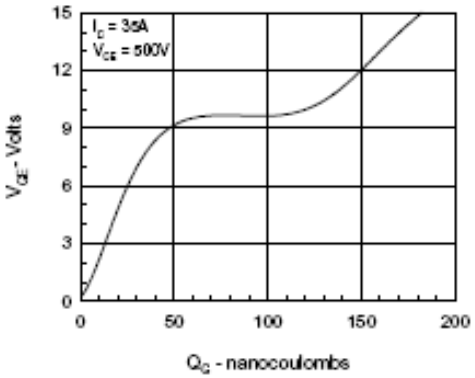


Fig.10 Turn-Off Safe Operating Area

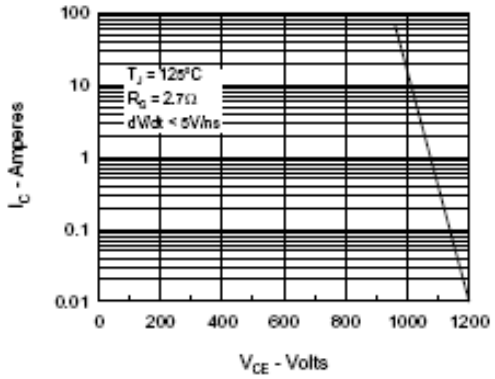
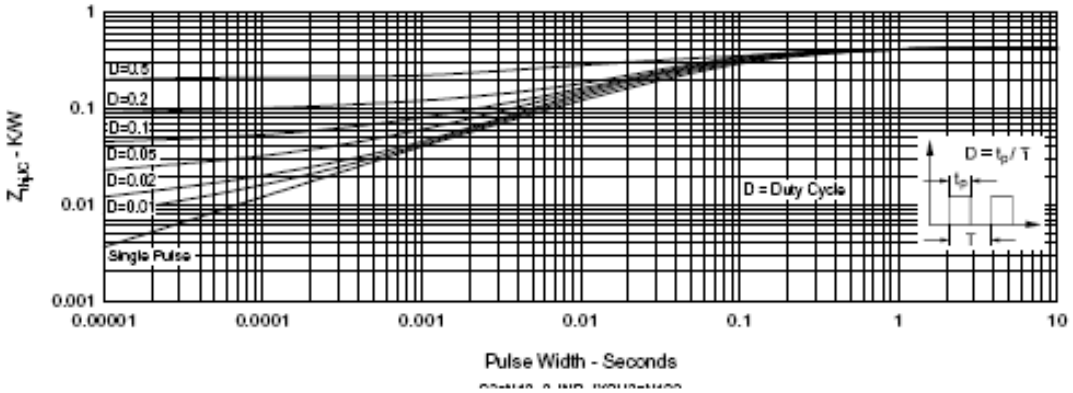


Fig.11 Transient Thermal Impedance



Appendix C

Material Properties Involved in Power Packaging

Table C.1. Some material properties for power electronics packaging applications.

	Materials	Elastic Modulus (GPa)	Poisson's Ratio	Yield Strength (MPa)	UTS/UCS /USS (MPa)	CTE (ppm/K)	Thermal Cond. (W/m-K)	Density (g/cm^3)	Specific Heat (J/Kg*K)	Ref. T (ºC)
Sintered silver		~10	0.37	43	43	19.0	~240	8.4	234	25
Conductive epoxy		<1			~10	~25	0.1			25
Solder	63Sn37Pb	26.4	0.36	36.4		25.2				0
		15.7	0.362	27.2		25.5	51	8.47	150	25
		12.5	0.365	15.2		26.1				50
	96.5Sn3.5Ag	26.2	0.36	22.5	52//	22	60	7.36	215?	25
	SnAgCu (typical)	54.65		41.645		9.25				-25
		50.86		31.835		15.5	60	7.41		25
		42.6		13.635		16.8				125
	90Pb10Sn	19	0.4	13		28.9		10.94		25
	80Au20Sn	68			275	16	58	14.5		25
Device	Si	160	0.28	FS:300-7000	/120/	2.5-3.2	144	2.3	714	25
	SiC	411?				2.8-4.0	270			25
	GaN	180	0.35			3.5	130			25
Metal	Aluminum (wirebond)	69	0.33	55	47.4//	23	216	2.7	910	25
	Copper	120	0.34	138-340	351//	16.5	400	8.9	390	25
	Bulk silver	75	0.37	140		19.0	419	10.5	234	25
	Nickel	207	0.31	103-206	482/?/?	14	60			25
	Titanium	116	0.34			10	17			25
	Cu-W (15/85-180)	275				7.1	180	16.1		25
	Molybdenum	327			690/?/?	5.2	138	10.2	250	25
Substrate	Alumina (Al_2O_3)	303	0.21	196	323/?/?	7	25-30	3.7	850	***Below ε: 9-10***
	DBC (total, Al_2O_3)	220?	0.27?			7.4	24-28	6.4		
	AlN	330	0.23	FS:2000	350//	4.2	180	3.26	734	***8.9***
	DBC (total, AlN)	230?	0.28?			5	≥150			
	Si_3N_4	310	0.27	FS:830		3.3	30	3.29		
	Passivation	72				0.3-0.5	6-10			***3.5-4.0***
	Phralux (2/3 Cu)	6.1	0.36			20	393	1.4/ 6.4	1090/	25
	MMC (70SiC30Al)	227				6.8	180	2.9		
	FR-4	22	0.25			16-20 (x,y) 60-90 (z)	0.35	1.9		

Table C.2. Visco-plastic properties of solders in Anand's model for ANSYS input.

	C1 (s_0) (MPa)	C2 (Q/R) (K)	C3 (A) (1/Sec)	C4 (ξ)	C5 (m)	C6 (h_0) (MPa)	C7 (s) (MPa)	C8 (n)	C9 (a)
63Sn37Pb	12.41	9400	4.0E+6	1.5	0.303	1378.95	13.79	0.07	1.30
90Pb10Sn	1.00	7416	2000	6.0E-4	0.303	1.0E-9	1.00	1.0E-9	1.00
60Sn40Pb	1	6359	7208	8.703E-2	0.3014	0	1	0	1
96.5Sn3.5Ag	39.09	8900	2.23E+4	6	0.182	3321.15	73.81	0.018	1.82

Table C.3. Kinematic inputs of aluminum and copper materials.

	Elastic modulus (MPa)	Poisson's ratio	Yield strength (MPa)	Yield strain (%)	Hardening modulus after yield (MPa)
Aluminum (wire)	69000	0.33	55	0.0797	502
Copper	120000	0.34	138	0.115	1350

Appendix D
Related Research Work by the Author

D.1 Flip-Chip on Flex Integrated Power Electronics Modules

Three-dimensional flip-chip on flex (FCOF) integrated power electronics modules (IPEMs) have been fabricated for high-density power applications. In this FCOF-IPEM structure, solder-bumped devices were flip-soldered to a flexible substrate with electrical circuits etched on both sides. One side of the flex provides interconnection to power devices while the other is used to construct a simple gate-drive circuit; via holes through the flex integrate the power stage and gate-drive together. Solder-bumped MOSFET devices were obtained by a metallization processing and were used in the FCOF power module construction to improve thermal performance, power density, and integration. With this packaging approach, the multiple solder bumps, instead of the thin, long bonding wires were utilized to connect the power devices to the flex substrate and to improve heat dissipation, lower parasitic oscillations, and reduce package size. Reliability of solder joints has been dealt with through selection of materials, such as the use of flexible substrates and underfill encapsulation, and design of joint shape for lower thermomechanical stresses. A comparative study of continuous switching test results has shown that the FCOF-IPEMs have better electrical performance than commercial wire bonded power modules.

Introduction

The engineering and market environment for power electronics is particularly demanding on their performance, reliability, and cost. Since packaging enables a product to meet its functional (electrical, thermal, mechanical, electromagnetic) specifications, physical (size and weight) requirements, life-time, and cost, research and development

activities for innovative packaging technologies are critical for advancing power electronics. The state-of-the-art packaged power devices such as MOSFETs and insulated gate bipolar transistors (IGBTs) are in the forms of single-in-line package (SIP), dual-in-line package (DIP), small outline package (SOP), and quad flat pack (QFP). Inside these power devices as well as the state-of-the-art power modules, interconnection of power devices is accomplished with wire bonding. Recently, issues concerning the limited thermal performance, parasitic oscillations [1], and difficulties with high-density integration associated with the wire-bond interconnection technology sparked a series of research activities for developing alternative interconnection techniques aimed largely at the development of high-density power modules.

In power electronics, it is generally believed that advancement can be achieved through a system-level approach by developing intelligent, integrated power electronics modules (IPEMs) that enable greater integration [2, 3]. As a result, it has been envisioned that the packaging of 3-D high-density multichip modules (HDMCMs) can meet the requirement for future power electronics systems [4]. There are several HDMCMs-based packaging technologies under development [5- 9]. These technologies have yet to prove their manufacturability, reliability, and cost-effectiveness.

The flip-chip technology emerged firstly in IC as low-cost, high density, and reliable interconnections [10,11]. This technology eliminates wire-bonds and utilizes solder joints that are capable of carrying large currents for interconnecting devices. The low-profiled solder joints introduce smaller parasitic inductance and capacitance than conventional wire-bond connections. Compared to conventional wire bonded packaging, flip-chip technology enables an engineer to pack larger die into the same packaging area since the latter does not need lead-frame and epoxy bleed-out around the chip [12]. Also, the use of an underfill dielectric material between the devices and substrate helps to achieve protection and stress reduction in the devices as well as improve heat transfer. In spite of all these potential benefits, flip-chip technology is yet to be fully implemented for power electronics packaging [13].

In this paper, we present a flip-chip packaging approach in which we use flexible substrates for integrating a gate-drive circuit along with a half bridge switching power stage. We called the packaging technology flip-chip on flex (FCOF) because in the

fabrication process, solder-bumped semiconductor devices were flip-soldered to a flexible substrate. The integrated power electronics modules (IPEMs) were designed specifically for an electric water pump driver with rating of 42 V for a future vehicle. In the following sections, design issues related to materials selection and reliability of the 3-D structure and interconnections are discussed, along with the fabrication process of the IPEMs. Continuous switching test results from the IPEMs are presented and discussed.

Packaging Design and Processing

From an electrical circuit design point of view, power modules are normally quite simple; however, design issues related to materials selection, thermal management, and the reliability of the 3-D structure and the interconnections are difficult because of the high voltages and large currents, as well as the high-power dissipated in the modules. Flip-chip on flex integrated power electronics modules (FCOF-IPEMs) are envisioned to have higher levels of integration of power semiconductor devices, gate drive, and control circuitry for a wide range of power electronics applications. Fig. 1 shows the cross section of the designed FCOF-IPEM structure. In the multilayer structure, the top layer is a double-sided flexible copper-clad laminate, which has circuits etched on both sides to provide interconnections to the solder-bumped power devices and to the gate-drive circuit. The power stage and control parts are interconnected by punched holes through the flex. The bottom layer is an insulated metal substrate (IMS) for die attaching of the power devices.

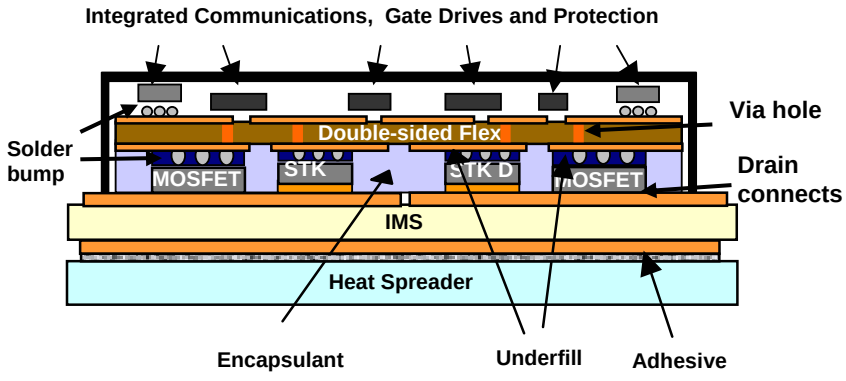


Fig. 1. Schematic structure of an FCOF-IPEM built using solder-bumped power devices.

For the construction of the FCOF-IPEMs, the fabrication flow chart is shown in Fig. 2. First, as the commercial power devices (MOSFETs and Schottky diodes (STK Ds)) for our specific ratings were not solderable, an in-house metallization processing was developed to make the chips solderable. Solder joints were then formed on the solderable pads of the chips. After the flex preparation, the solder-bumped devices were flipped and aligned and solder-bonded to the power stage circuitry on one side of the flex. Then the assembly of power devices on flex was attached to a bottom IMS. Finally the gate driver components and the snubber capacitors were attached by either surface mount or flip chip technology.

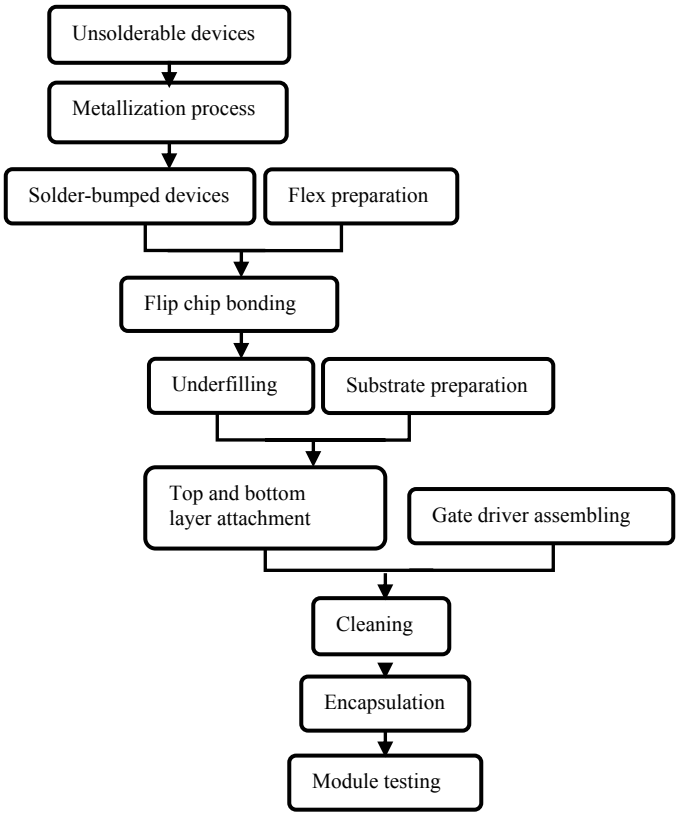


Fig. 2 The FCOF-IPEM fabrication flowchart.

In the following sections, we discuss the fabrication procedure step-by-step. The design issues on the materials selection, reliability, and applicability of implementing the FCOF-IPEMs will be particularly addressed.

A. Ball-grid-array fabrication

Currently, the devices in commercial power modules are interconnected using bonding wires. Almost all commercial bare power devices are designed for wire bonding

instead of solder joint interconnections. The power MOSFETs and Schottky diodes used in this research were acquired from IXYS, with part number IXFD80N08-70 and C-DWS 32-100 [14], respectively. The power MOSFET has source and gate pads with approximately 4 μm thick Al-Si (1%) alloy as shown in Fig. 3 (a). The metal lines of device field ring connecting to gate (by gate fingers) run parallel to each other along the periphery of the die. Except for the pads and the peripheral lines, the rest of the die is covered with P-doped glass passivation commonly known as silox to form the insulation between the pads and the die edges. The backside (drain) of the die has a Cr/Ni/Ag solderable metallization. For the power Schottky diode, the anode is an Al-Si alloy layer and the cathode is a Cr/Ni/Ag solderable metallization layer. The absence of solderable metallization on the source and gate pads in the MOSFETs and anodes in the Schottky diodes has to be addressed in order to achieve solder interconnection for BGA solder bumps.

In the metallization process, a Ti/Ni/Ag under bump metallization (UBM) scheme was selected and deposited by sputtering. The Ti layer adheres well to the Al surface on the device pads and thus acts as an adhesion promoter to the UBM. The Ag layer on top aids in solder wetting and serves as an oxidization layer. The Ni layer has three functions: 1) It acts as a diffusion barrier between Al and Ag, otherwise intermetallic formation between them could lead to the depletion of the Ag layer, thereby preventing solder wetting. 2) It is an excellent solder diffusion barrier especially for 63Sn/37Pb eutectic solder. 3) It may also provide a solder wetting surface in case Ag in the top of the UBM is consumed. In the metallization process, solder mask was firstly spin-coated to the surfaces and patterned by photolithography to define the positions for solder joints as an example shown by a MOSFET in Fig. 3 (b). The solder-mask covered the gate fingers (if have) of the devices to prevent from circuit short or any leaking current at high voltage levels. For metal deposition, a Kapton film mask was patterned and mechanically cut and covered to the device surfaces to serve as the sputtering mask. The power devices were cleaned to remove oxides or organic residue prior to metal deposition. Then the UBM layers were obtained by sputtering Ti/Ni/Ag onto the top surfaces of the MOSFETs and diodes. After sputtering, the Kapton film mask was peeled off and the UBM pads for

solder interconnection would be left as shown in Fig. 3 (c). The total thickness of the UBM layers, measured by a Dektak profilometer, is about 3 μm.

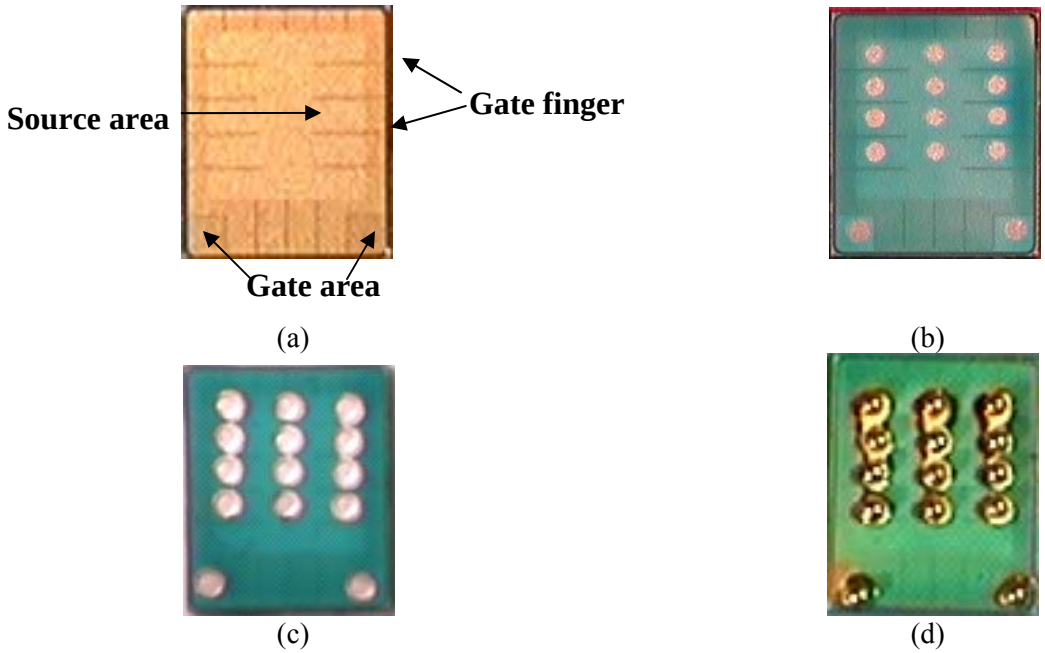


Fig. 3 (a) A commercial unsolderable power MOSFET from IXYS. (b) The MOSFET after solder-mask process. Except the gate and source pads, the entire surface is covered by solder mask. (c) The MOSFET after UBM sputtering process. (d) The solder-bumped MOSFET.

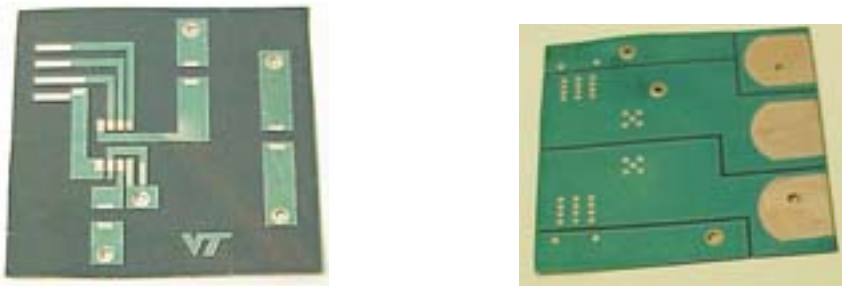
After metallization, the eutectic solder paste with a melting temperature of 183 ºC was dispensed onto each of these pads. By adjusting dispensing time and the air pressure of the dispenser, the amount of solder paste can be reasonably controlled. After dispensing, one high-leaded solder ball with a diameter of 30 mil and a melting temperature of 268 ºC was attached on each pad, and then reflowed to obtain a solder bump according to the manufacturer's recommended reflow profile. During the reflow, the high-lead solder balls were not melted because the highest temperature point of the reflow is lower than the 268 ºC. After reflow, the solder-bumped devices were obtained and cleaned. Fig. 3 (d) shows a prepared solder-bumped MOSFET. At this stage, high power test was conducted on the solder-bumped devices to screen the bad devices by soldering them to a tester using In97Ag3 solder with a melting temperature of 143 ºC.

B. Flex preparation

The flex substrate in the FCOF-IPEM, which was acquired from DuPont Co., is a double-sided, copper-clad laminate consisting of a 2-mil thick polyimide film bonded to 2-mil copper foils on both sides. (If it is needed, the Cu foil could be thickened to 5 mil

or more by electroplating to increase current-carrying capacity.) The utilization of flex substrate is particularly advantageous for stress relief between solder joints, devices and substrates [15]. The laminate has excellent handling characteristics for fabrication, outstanding dimensional stability, excellent assembly performance over a wide range of processing temperatures, low thermal expansion coefficient, excellent thermal resistance for high-temperature assembly processes and is compatible with conventional oxide treatments and wet chemical plated-through-hole desmear processes.

The patterns of Cu traces were formed by photolithography of etch resist and chemically etched in a spray etcher. Solder mask was spin-coated and patterned to define soldering pad and circuit outlet locations. Via holes were punched through the flex to integrate the power stage and the gate driver together. Fig. 4 shows a flex substrate that was etched and solder-masked on both sides and was ready for flip chip bonding and attaching power buses. The soldering pad locations defined by patterned solder mask were used for attaching gate drive components, power buses or power devices, and connecting the gate driver and power stage circuits through the punched holes.



(a) (b)

Fig. 4 A flex substrate which has a simple gate driver circuit on one side (a) and the power stage circuit on the other side (b).

C. Flip-chip bonding

After the solder-bumping fabrication and flex substrate preparation, a flip-chip bonding process was undergone to solder assemble the selected solder-bumped devices and prepared flex. Fig. 5 shows the three steps of the process and Fig. 6 shows the assembly of two MOSFETs and two Schottky diodes attached to the etched and solder-masked flex substrate. In the flip-chip bonding process, eutectic solder paste was first dispensed on the exposed Cu bonding pads. Then the tested solder-bumped devices were flip-chip attached to the bond pads. For a comparative study, we packaged two C-DWS 32-100 Schottky diodes in some modules while in other modules we just used body-

diodes of the MOSFETS to carry the fly back currents. Finally the assembled structure was heated to melt the solder paste and form a metallurgical bond with the bond pad.

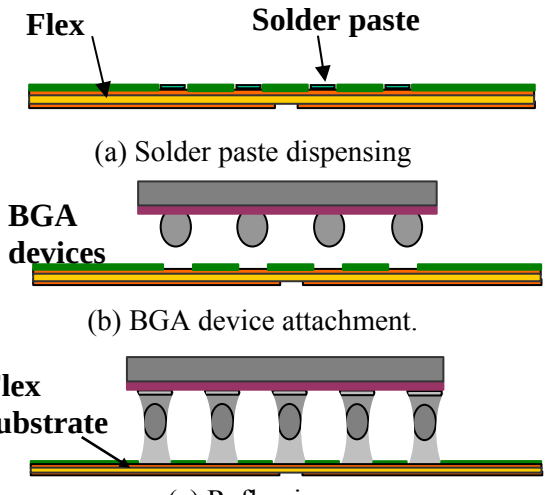


Fig. 5 The three steps of flip-chip bonding.

Fig. 6 The power devices and flex substrate assembly after flip-chip bonding.

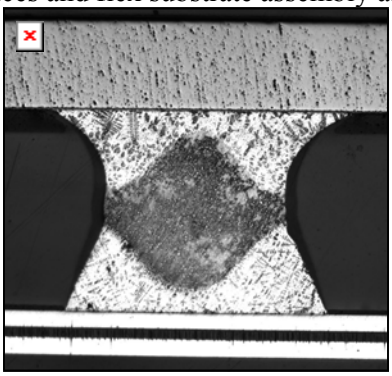


Fig. 7 SEM image of a triple stacked hourglass shaped solder bump.

Based on our temperature cycling experiment [16] and some published work on finite element analysis [17] on solder joint geometry, optimized hourglass-shaped solder bumps are more reliable than barrel-shaped solder bumps [18]. In our experiment, we carefully controlled the open areas of solder mask on flex and the UBM pads on power devices and the amount of the dispensed solder paste to optimize the geometry of the solder bumps. As an example, a triple stacked hourglass shaped solder bump is shown in Fig. 7.

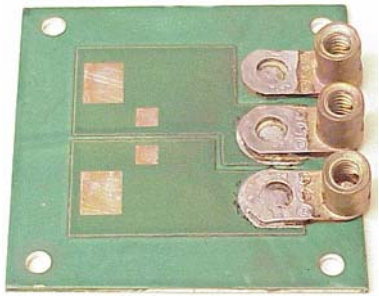


Fig. 8 An IMS after etching, solder mask patterning process and attaching power outlets.

After hourglass-shaped solder bumps were obtained, the whole assembly structure was cleaned to remove solder flux and other contaminations. At this stage, the devices were tested again by using a curve tracer. The assembly with KGDs was encapsulated in underfill polymer material to reduce the thermo-mechanical stresses imposed on the solder joints.

D. Substrate preparation

An IMS acquired from the Bergquist Company was etched and patterned by solder mask to serve as the bottom substrate as shown in Fig. 8. Three electrical outlets were attached using Pb95Sn5 solder with a melting temperature of 268 ºC. The IMS serves three functions: 1) heat spreader for power devices; 2) electrical connection; and 3) mechanical support.

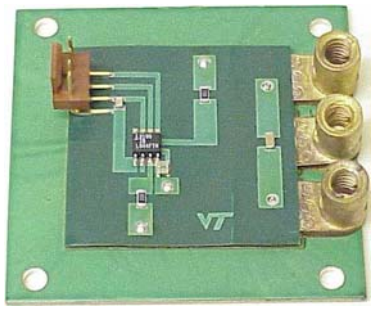


Fig. 9 A completed half-bridge FCOF-IPEM module.

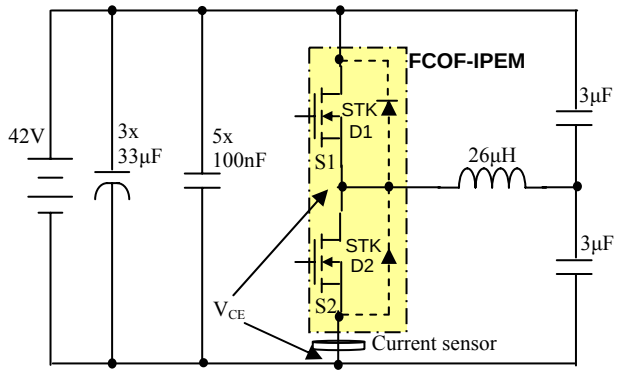
E. Gate driver assembly

After IMS preparation and flip-chip bonding, the flex with power devices was flipped again, and the backsides of the power device were attached onto the IMS using In97Ag3 solder with a melting temperature of 143 ºC. The low temperature solder was selected for the die-attachment to avoid melting the eutectic and Pb95Sn5 solders during the reflow. Thermal conductive encapsulant was filled in the gap between the flex substrate and the IMS to make the package robust, help distributing and dissipating heat, and improve package reliability. Finally the gate driver components were attached on the

top flex surface. Fig. 9 shows a completed half-bridge FCOF-IPEM with gate driver components built on top of the flex. After the IPEMs were completed and cleaned, they were tested for functionality under continuous and transient switching.

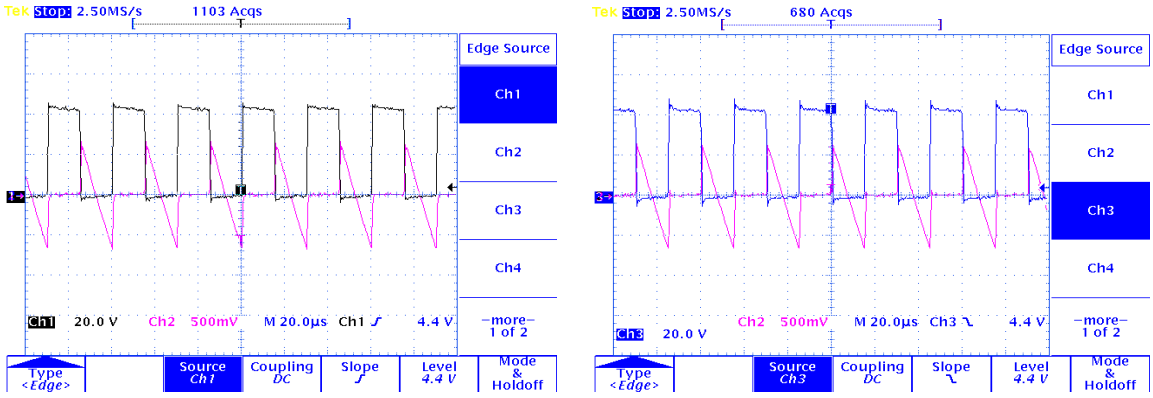
Test Results and Discussion

The FCOF-IPEMs were tested at 33 kHz switching frequency with 40% duty ratio and 42 volts DC power bus input. Fig. 10 shows the test circuit setup for the continuous switching test. To simplify the illustration, the gate driver part of the FCOF-IPEMs is not shown. The testing results from the low-side switch of the FCOF-IPEMs without the Schottky diodes (STK D1&D2) packaged in are illustrated in Fig. 11(a). With 42 DC volts load, the peak current is approximately ± 6.5 A. The signals are read from V_{CE} (Ch1 in Fig. 11(a) and Ch3 in Fig. 11(b)) and the current sensor (Ch2 in both Fig. 11 (a) and (b)), respectively. For comparison, the continuous switching test results on a commercial module from Semikron with a part number of SK 100 MB 10, in which the power interconnections are bonding wires [6], are also shown in Fig. 11(b). From Fig. 11 (a) and (b), one can see that the FCOF-IPEM exhibits smaller voltage overshoots when turned on/off during continuous switching. This result is expected because the solder-bumped chips in FCOF-IPEMs have shorter pad-to-circuit connections and larger contact areas than wire-bonded chips as demonstrated in Fig. 12; thus the parasitic inductance associated with the FCOF-IPEM is smaller than that in the wire bond module.



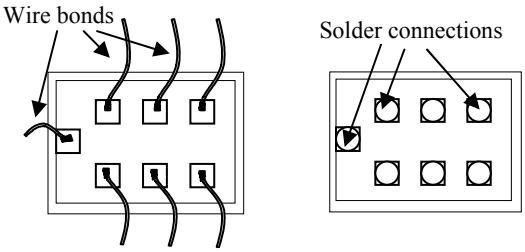
S1&S2: BGA Power MOSFET (IXFD80N08-70)
STK D1&D2: BGA Schottky Diode (C-DWS 32-100)

Fig. 10 Continuous switching test circuit.



(a) (b)

Fig. 11 Voltage and current waveforms from a continuous switching test. (a) The results from FCOF-IPEM; and (b) a commercial wire bonding power module.



(a) (b)

Fig. 12 Contact geometries of wire-bonds vs. flip-chip solder bump interconnections: (a) The long wire bonds with small contact areas; (b) the short flip-chip solder bumps with large contact areas (Victor).

Conclusion

This paper reports the development of a 3-D flip-chip on flex (FCOF) power packaging technology for integrated power electronics modules (IPEMs). By demonstrating a working 42-V half bridge power module, the FCOF technology is shown to be a viable alternative to existing power-packaging technology, especially for high-density power integration applications. By using area bonding ball-grid-array (BGA) devices and optimizing the shape of the triple-stacked solder bump, the package offers enhanced electric performance during switching because of much lower parasitic inductance of the interconnections. Improvements in thermal management of the package are also expected.

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D.2 Reliability Discussion on Solder-Bump and Direct-Solder Packages

Power device packages with solder-bump (SB) and direct-solder (DS) interconnections were fabricated and some of their thermomechanical reliability issues were discussed based on both thermal cycling experiment and finite element analysis (FEA). The SB interconnection shows superior over the DS interconnection in the thermal cycling experiment because the mismatched coefficient of thermal expansion (CTE) leads to smaller stresses at the SB interconnection under the same temperature changes. On the other hand, FEA results show that the DS package has significantly lower operating temperatures under the same double-sided cooling condition. After considering the operating temperature difference, the DS package is superior over the SB package in the power cycling analysis.

Introduction

Packaging of power semiconductor devices provides electrical interconnections as well as mechanical support, environmental protection, and heat removal [1]. However, because of the higher heat dissipation of a power device than an IC device, thermal management is more critical in power packaging. Special consideration must be paid to the thermally induced stresses due to coefficient of thermal expansion (CTE) mismatches among the packaging materials to ensure the package reliability. With the trend towards higher power density [2], issues concerning the difficulties of integration, limited thermal performance, and parasitic oscillations [3] associated with the wire-bond interconnection technology sparked a series of research activities for developing alternative interconnection techniques. Specifically, new interconnection technology must be designed to dissipate heat effectively to prevent the maximum power device operating temperature, usually 125ºC for a silicon device, from being exceeded. On the other hand, device temperature excursions during normal operating conditions must be limited for

reliability goals to be achieved and this implies that the operating temperatures may have to be kept even lower than the maximum rating of the device.

For a given situation, there are many issues such as cost, operating environment, and available space that limit the choice of cooling approaches and the design of cooling systems, which in turn limit the further reduction of the die-to-environment thermal resistance. Further increasing the heat transfer coefficient at a heatsink surface may require bulky and expensive solutions. Benefits could be derived if the topside of the device is utilized as an additional heat removal path. The traditional wire-bond technology, while having the advantages of maturity, flexibility and low cost, is a two-dimensional interconnecting solution and the topside of a wire-bond package is usually not designed as a heat dissipation path.

Soft solder alloys are desirable interconnection materials because their low melting points allow the production of metallic joints with specific geometry at moderate processing temperatures. Among the power packages utilizing solders as interconnection materials, solder-bump (SB) packages are characterized by the multiple discrete solder joints for interconnecting the source/gate surfaces of power device. A SB interconnection is often closely associated with flip-chip, so called because of the way of device mounting on the substrate (upside down). The roots of flip-chip can be traced back to the IBM's C4 technology that was developed in the early 1960s. Unlike ICs, only a few interconnections are needed for power packages. The cross-sectional area of each joint can be made larger to increase the current handling capability of the package and at the same time the taller interconnection length usually means higher reliability [4]. Recently developed power packages that implement this form of interconnection include Fairchild Semiconductor's BGA MOSFET [5-7], International Rectifier (IR)'s FlipFET [8,9] and Motorola's multichip Mechatronics power package [10]. All three packages include an innovative method to bring the back contacts to the front side. A similar structure for application in power modules developed at Virginia Tech is flip-chip on flex (FCOF) [11,12].

Direct solder (DS) packages eliminate the discrete solder joint contacts found in a SB package and are characterized by larger area solder layer contacts at both the source/gate and drain surfaces of power devices. From an electrical standpoint, a DS

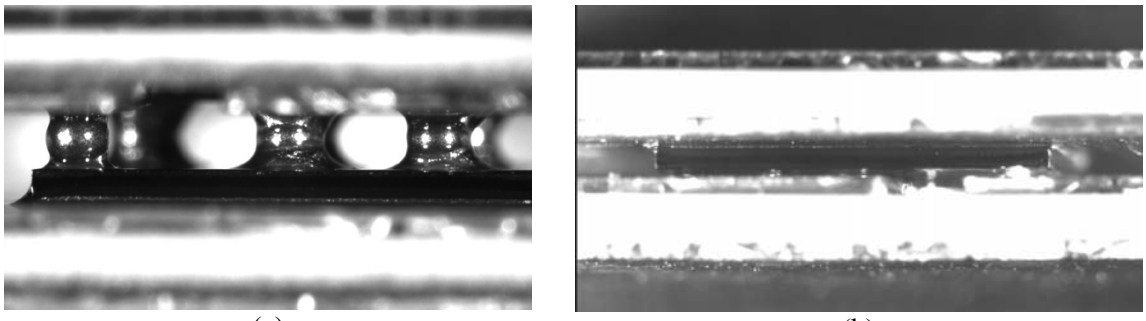
interconnection is superior because it further increases the current handling capability. Heat flow is also improved because of the wider area through which heat conduction can occur. Overall, the interconnection results in very compact, low-profile packages with high power density and very low electrical and thermal resistances. However, compared to a SB interconnection, stresses at a DS interconnection are expected to be higher and they may cause die crack and/or premature delamination after processing. While thicker solder layers can alleviate these effects, processing consistency may be a challenge. With improvements in electrical and thermal performance, conductive epoxy could become an alternative interconnection material for power packages, offering potential advantages concerning process control and reliability. Packages that make use of this kind of interconnection include Vishay Siliconix's PowerConnect [13], IR's CopperStrap [14] and DirectFET [15,16]. With these packages, it is claimed that the packaging resistances are reduced substantially compared to the standard SO-8 packages using the conventional wire-bond interconnections.

Since bonding wires are eliminated from the SB and DS packages, double-sided cooling becomes possible if thermally conductive substrates and heatsinks are attached to both sides of the packages. In this study, some thermomechanical reliability issues of the SB and DS packages are discussed based on the results of both experiment and computer simulation. The experimental portion involves fabrication of the two types of packages and subjecting them to the same thermal cycling experiment to predict potential sites and time to fail. The finite element analysis (FEA) portion involves both thermal and thermomechanical analyses to simulate their operating conditions for their power cycling reliability comparison.

Experimental

Two 13.2 mm (0.52 in)×10.2 mm (0.40 in) alumina direct bond copper (DBC) substrates (IXYS Corporation, Santa Clara, CA) and two solder reflows were required to assemble either the SB or the DS package. Each DBC substrate had 0.3-mm (12-mil) thick copper layers bonded on both sides of the alumina with total thickness 1.23 mm (48 mil). For both packages, 100 μm (4 mil) thick lead-free solder (Sn3.5Ag, melting point 221ºC) layer was used to die-attach the drain side of MOSFET power device

(International Rectifier Corporation, El Segundo, CA) first onto the bottom DBC substrate. The power device has silver metallization on the both drain and source/gate sides. In the SB package, eutectic lead-tin solder paste (Sn36Pb2Ag, melting point 183°C) and high-lead solder balls (Pb-5Sn) with diameter of 0.700±0.050 mm were used to form the solder bumped device and interconnect the source/gate of the MOSFET onto the top DBC substrate. About 10% source/gate side of the MOSFET was used to form the six 1 mm-high solder bumps. Hourglass shaped solder bumps were formed for higher reliability [17] by controlling the amount of the Sn36Pb2Ag solder paste. In the DS package, over 90% of the source/gate side was used to form two 100 μm-thick interconnection layers using the same Sn36Pb2Ag solder paste to interconnect the source and gate of the MOSFET. Close-up views of both the SB and DS packages are shown in Fig. 1(a) and (b).



(a) (b)

Fig. 1. (a) A SB package with the source/gate of the power MOSFET device attached to the top DBC substrate via six 1-mm-high solder-bumps, (b) a DS package with the source/gate of the device attached to the top DBC substrates via 100 μm solder layers. Both 10X magnification.

About 40 SB and DS packages were subjected to the thermal cycling test to evaluate their thermomechanical reliability under the same temperature changes. Thermal cycling was carried out following one of the specified profiles (-55ºC--150ºC) in the JEDEC recommended conditions (standard No. 22-A104-B) as illustrated in Fig. 2 in a Tenney Jr. environmental test chamber. Each package was initially tested for the drain-source resistance of $R_{DS}(ON)$ and randomly selected samples were examined with the scanning acoustic microscope (SAM) prior to loading in the thermal cycling chamber. The samples were periodically taken out for inspection and electrical resistance measurements. A failure criterion based on the 20% increase of the $R_{DS}(ON)$ resistance used during the thermal cycling experiment. Failed samples were removed from the

cycling regime and mounted, sectioned and polished for failure analysis via optical microscopy and SAM.

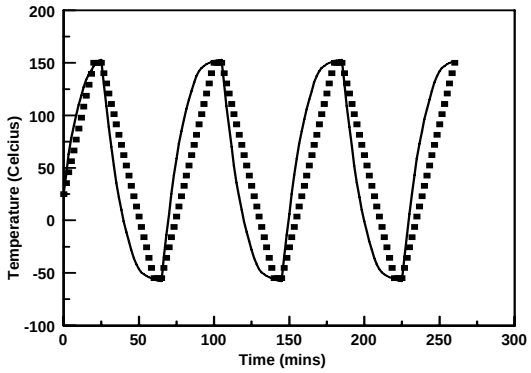


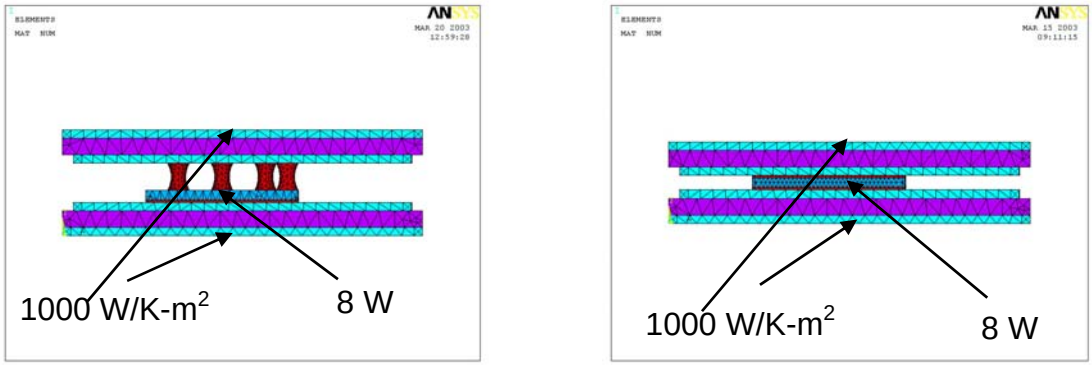
Fig. 2. Temperature profiles for the thermal cycling experiment. Solid line: experimental temperature profile; Squares: temperature datum inputs for the thermal cycling FEA simulation.

Finite Elemental Analysis

Both thermal and thermomechanical analyses were done on the SB and DS packages by FEA using ANSYS 7.1. The detail properties of the materials used in the both analyses are listed in Table I and the dimensional inputs followed the experimental samples. In the thermal analysis, the device operating temperatures were derived by assuming the same heat dissipation of 8 W for the power MOSFET and the same equivalent heat-transfer coefficient of 1000 W/K-m^2 from the top and bottom DBC substrates as shown in the Fig. 3. The numbers were based on the assumption of the conventional heatsink plus forced-air cooling with the size effects taken into account and they are consistent with the experiment done by Pang *et al*. [18].

Table II. Linear property inputs of the materials for static analyses.

Materials	**Elastic Modulus (GPa)**	**Poisson Ratio**	**CTE (ppm/K)**	**Thermal Conductivity (W/K-m)**	**Reference Temperature (ºC)**
Copper	120	0.34	16.5	400	25
Alumina	303	0.21	7	30	25
Sn3.5Ag (Die attach solder)	26.2	0.36	22	60	25
Silicon (Device)	160	0.28	2.5	144	25
Sn36Pb2Ag	26.4	0.360	25.2		0
	15.7	0.362	25.5	51	25
	12.5	0.365	26.1		50



(a) (b)

Fig. 3. The thermal FEA models for (a) the SB package and (b) the DS package.

In the thermomechanical analyses, transient FEA were conducted to simulate both thermal cycling and power cycling for the failure prediction of the SB and DS packages. Large deformation effect option was enabled (NLGEOM, ON) in the analyses. DBC copper, Sn36Pb2Ag and Sn3.5Ag solders, and the rest materials were modeled by kinematic hardening, Anand's models and linear elastic solids, respectively. In the kinematic hardening model, copper was characterized by its yield strength of 138 MPa at ε = 0.115% and with a hardening modulus 1350 MPa after yielding. The Anand constants for the Sn36Pb2Ag and Sn3.5Ag solder alloys used in FEA are taken from Ref. [19] and they are listed in Table II.

Table II. Anand's model constants for the Sn36Pb2Ag and Sn3.5Ag solder alloys.

Constants defined in ANSYS	Parameters	Definition	Sn36Pb2Ag	Sn3.5Ag
C1	s_0 (MPa)	Initial value of deformation resistance	42.32	39.09
C2	Q/R ($1/^0$K)	Activation energy/Boltzmann's Constant	11262	8900
C3	A (1/sec)	Pre-exponential factor	2.3E7	2.23E4
C4	ξ	Multiplier of stress	11	6
C5	M	Strain rate sensitivity of stress	0.303	0.182
C6	h_0 (MPa)	Hardening constant	4121.31	3321.15
C7	$\hat{s}$ (MPa)	Coefficient for deformation resistance saturation value	80.79	73.81
C8	N	Strain rate sensitivity of saturation value	0.0212	0.018
C9	A	Strain rate sensitivity of hardening	1.38	1.82

The thermal cycling life of the eutectic Sn36Pb2Ag solder was derived using the crack initiation and growth model proposed by Darveaux [20,21]. In the Darveaux's model, FEA results were utilized to calculate the inelastic work per unit volume (i.e., inelastic strain energy density) accumulated per cycle. The fatigue life of a solder joint was determined by the cycles for the crack initiation, N_0, and cycles for the crack growth, N_1, which is defined by a crack propagation rate, da/dN_1:

$$N_0 = K_1 \Delta W_{avg}^{K_2} \tag{1}$$

$$\frac{da}{dN_1} = K_3 \Delta W_{avg}^{K_4} \tag{2}$$

where K_1, K_2, K_3 and K_4 are the crack growth constants, a is the characteristic crack length (interconnection diameter). The inelastic strain energy density, ΔW_{avg} (in psi) is averaged across the element along the solder interface where the crack propagates and it can be defined by

$$\Delta W_{avg} = \frac{\sum (\Delta W \times V)}{\sum V} \tag{3}$$

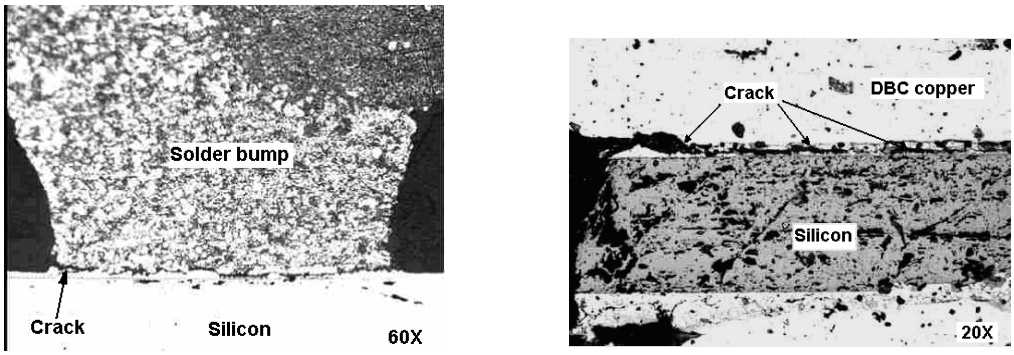
where the Σ operation includes all the elements in a thin layer that contains the crack propagation path in the solder interconnection, ΔW is the visco-plastic strain energy density accumulated in one cycle for each element in the thin layer, which is given by inelastic strain energy in ANSYS modeling, and V is its volume. If the crack propagation rate is assumed as a constant, the fatigue life of the solder, N, in terms of cycles, can be obtained by

$$N = N_0 + \frac{a}{da / dN_1} \tag{4}$$

Results and Discussion

Based on the failure criterion of 20% increase of $R_{DS}(ON)$, both SB and SD packages have about 50% cumulative failure after around 400 thermal cycles. The maximum temperature used for the test (150ºC) was very close to the melting point of the Sn36Pb2Ag solder (183ºC) and thus both interconnections failed at relatively low numbers of thermal cycles. Failed SB and SD interconnections were investigated by

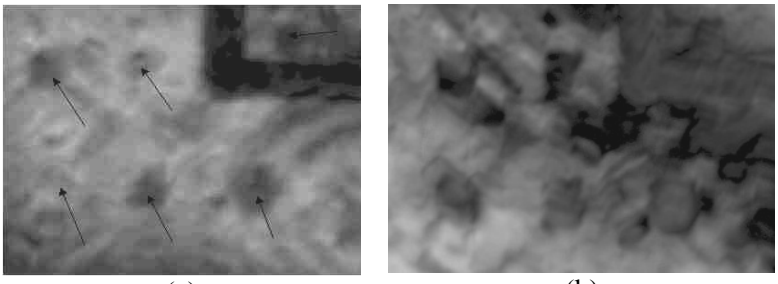
optical microscopy as shown in Fig. 4(a) and (b), respectively. Compare Fig. 4(a) with (b), one can see that the cracks in the DS interconnection are longer and much more evident than those in the SB interconnection. This is consistent with the fact that larger/thinner interconnections are more susceptible to fail via crack initiation and growth under the same temperature changes. It is also interesting to point that in the both SB and DS interconnections as shown in Fig. 4, cracks were initiated from left to right towards the neutral plane near the interface with the silicon device. These are because both interconnections experienced larger stresses at the position farther away from the neutral point. The SB interconnection also lost its original hourglass shape as seen in Fig. 1(a) with the solder ball being pushed out of position as a result of the extreme high temperatures in the thermal cycling.



(a) (b)

Fig. 4. Cracks at the solder-silicon interfaces in a failed SB package (a) and those in a failed DS package (b) after 875 thermal cycles.

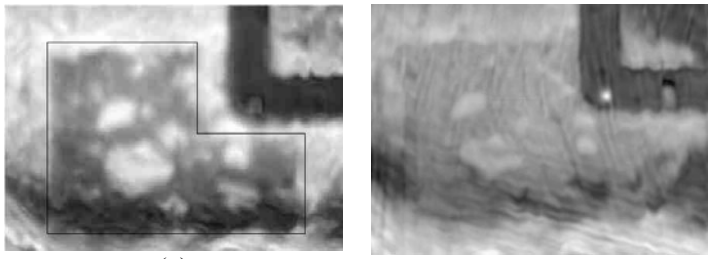
Failed samples were also examined using SAM to investigate the failure locations. The SAM images in Fig. 5 are for the SB interconnections. Arrows pointing to the power device side of the six SB interconnections in Fig. 5(a) indicate debonding or cracking of at least one of the interconnections. However, Fig. 5(b) indicates that the six interconnections are still intact on the copper side. The smaller CTE mismatches between the solder and more pliant copper layer in DBC may have slowed the failure at the solder-copper interface. However, at the solder-silicon device interface, the CTE mismatch is larger such that stress should be higher.



(a) (b)

Fig. 5. SAM images of the SB interconnections in a failed SB package taken after 875 thermal cycles. (a) At the solder/power device interface and (b) at the solder/DBC copper interface.

A similar situation is presented by the SAM images in Fig. 6 for the DS interconnections. Fig. 6(a) was taken at the solder/silicon interface while (b) was taken at the solder/copper interface. A comparison of the two images indicates that the solder interconnection was largely intact on the copper side while significant debonding had taken place on the silicon side. Again, the less CTE mismatch of solder-copper than that of solder-silicon interprets the results.



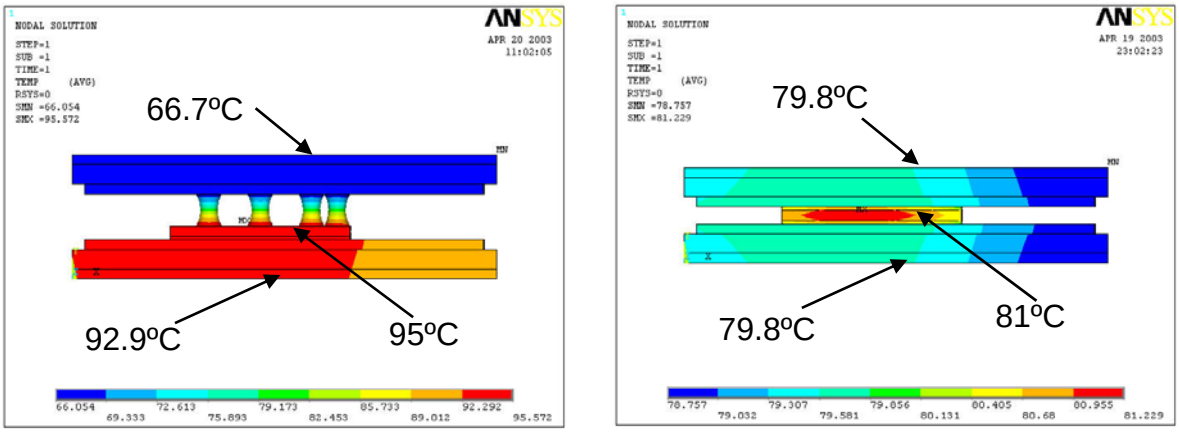
(a) (b)

Fig. 6. SAM images of the DS interconnection in a failed DS package taken after 875 thermal cycles. (a) At the solder/power device interface and (b) at the solder/DBC copper interface.

FEA Results and Discussion

Thermal Analysis

A comparison of the temperature distribution results in the DS and SB packages is shown in Fig. 7. For the SB package, the device operating temperature is about 95ºC and it dissipates 2.24 W (28%) heat through the top DBC; while in the DS package, the two numbers are 81ºC and 4 W (50%), respectively. The results show that the DS package has a superior thermal management capability over that of the SB package mainly because of the lower thermal resistance of the DS interconnections than the SB interconnections.



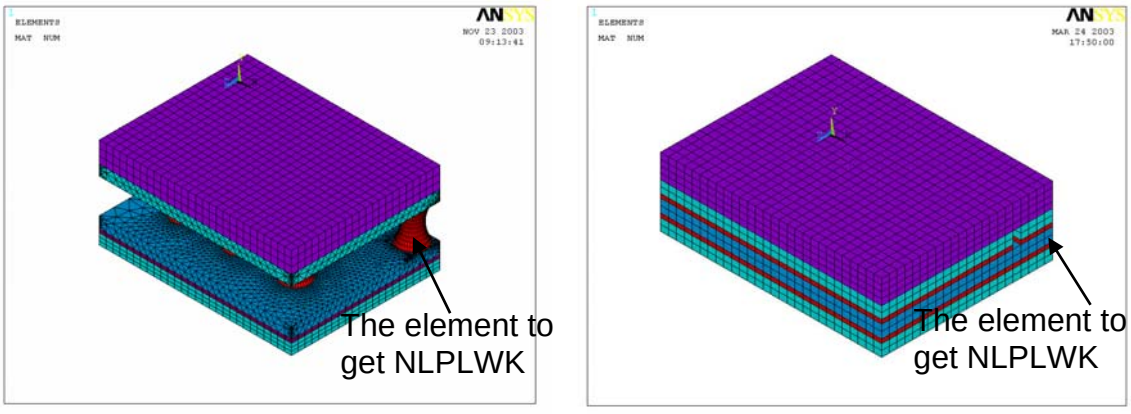
(a) (b)

Fig. 7. Thermal FEA temperature distribution results of (a) the SB and (b) the DS packages under the same operation and double-sided cooling conditions.

Thermal Cycling Analysis

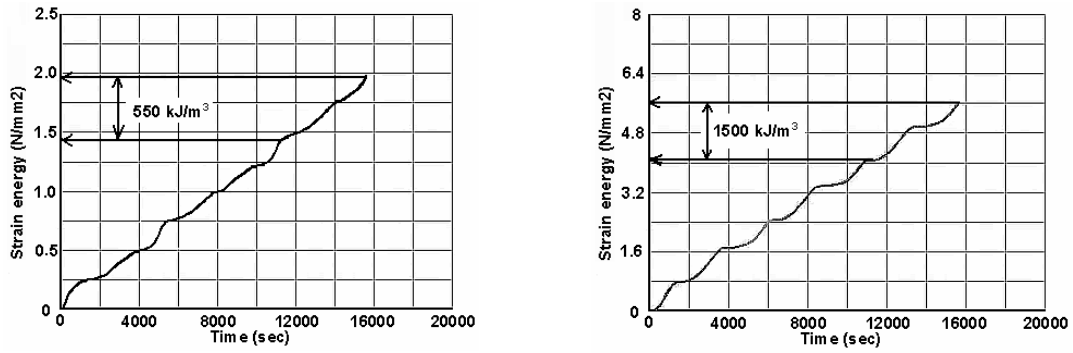
Finite element models as shown in Fig. 8(a) and (b) were used to represent the SB and DS packages in thermal cycling simulation, respectively. Room temperature was set to be stress-free in both cases. The accumulations of average density of inelastic strain energy at the corner elements of the SB and DS interconnections during the first three thermal cycles are plotted in Fig. 9(a) and (b), respectively. The energy accumulation per cycle reaches a saturated value quickly within the first three cycles. Therefore, the values of the accumulation per cycle were determined using the third temperature cycle, which are about 550 and 1500 kJ/m^3 for the SB and DS interconnections, respectively. For the SB package, $\Delta W \cong 0.55$ MPa = 79.805 psi, the crack will initiate at about 37 cycles with a crack growth rate about 4.67E-5 in/cycle, therefore the SB interconnection will fail in about 880 cycles. As for the DS package, the crack will initiate at about 9 cycles with a crack growth rate about 10.26E-5 in/cycle and the DS interconnection will fail in about 680 cycles. These results are compatible with the thermal cycling experiment considering the experimental imperfections. Again these FEA results show that the SB interconnection is superior to the DS interconnection under the same temperature changes. It is necessary to point out that the change of the stress-free temperature only affects the energy density accumulation in the first thermal cycle. The results will be almost the same after the first three cycles because the residual stresses in the solder are

released during the first thermal cycle and inelastic energy accumulation saturates quickly.



(a) (b)

Fig. 8. The finite element models of the SB (a) and DS (b) packages used in the transient thermomechanical analysis to simulate both thermal and power cycling experiment.



(a) (b)

Fig. 9. The average inelastic strain energy density accumulation at the corner elements of the SB (a) and DS (b) interconnections, respectively, during the first three thermal cycles.

Power Cycling Analysis

The two models in Fig. 8 were used again for a power cycling simulation. Unlike those in the thermal cycling simulation, different temperature profiles were assigned to the SB and DS packages in the power cycling to simulate their operating conditions. Making use of the thermal analysis results, the SB model was cycled between 25ºC and 81ºC while the DS model was cycled between 25ºC and 95ºC as shown in Fig. 10. Fig. 11(a) shows the accumulation of average density of inelastic strain energy at the corner elements of the SB interconnection while (b) shows the corresponding value in the DS interconnection. When the same fatigue life estimation model was used as shown in Ref. [21], the results show that the SB interconnection will fail at about 7900 power cycles

while the DS interconnection will fail at about 12200 power cycles. Therefore, under the particular double-sided cooling operation conditions, the DS package is more reliable than the SB package.

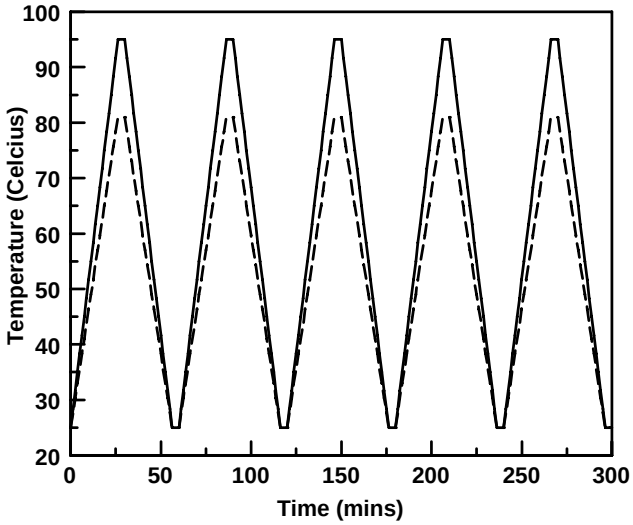
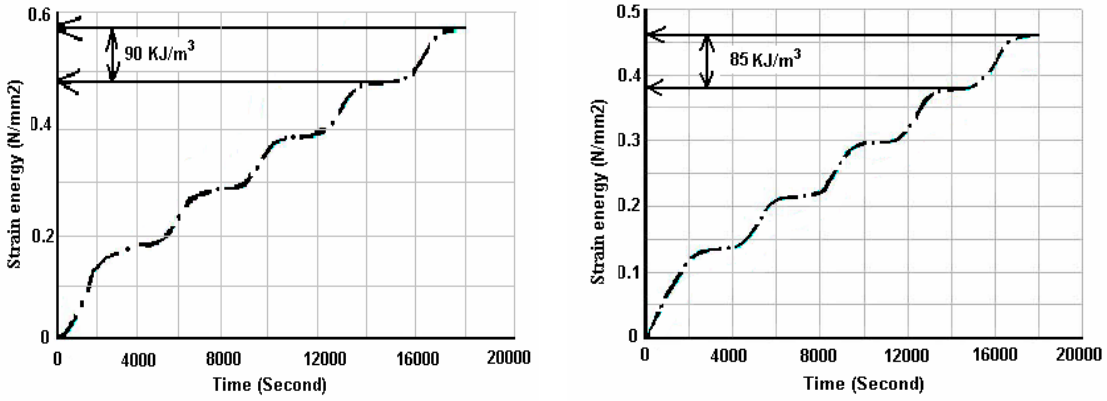


Fig. 10. Temperature profiles for power cycling simulation. Solid line for the SB package and dashed line for the DS package.



(a) (b)

Fig. 11. The average inelastic strain energy density accumulation at the corner elements of the SB (a) and DS (b) interconnections, respectively, during the first five power cycles.

Conclusion

Solder bump (SB) and direct solder (DS) bonded power device packages with double-sided cooling capabilities were fabricated and some of their thermomechanical reliability issues were compared using thermal cycling experiment and finite element analyses (FEA). The SB package induces lower thermal stresses than the DS package

under the same temperature changes and thus the former is more reliable under thermal cycling experiment. On the other hand, the DS package has better thermal management over the SB package because the DS interconnection has less thermal resistance. Take into account of the difference in operating temperatures, the DS package is more reliable than the SB package in the power cycling simulation.

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D.3 Characterization of Solder/Copper Interfacial Thermal Resistance

A feasibility study was conducted to determine the interfacial thermal resistance (ITR) in both bi- and tri-layered eutectic lead-tin solder/copper specimens by the flash technique. The solder/copper ITR results of the two sets of specimen showed excellent agreement. The values were found to range from 0.011 to 0.033 Kcm^2/W and with an average of about 0.020 Kcm^2/W. The variation was attributed primarily to the imperfection of the solder/copper bonding established by scanning acoustic microscopy.

Introduction

Interfacial thermal resistances (ITR) for thermally demanding applications are critical design variables because they can contribute significantly to the total thermal resistance of a heat path [1]. In an electronic package, semiconductor devices–the major heat sources–are usually die-attached to a copper substrate with a several-mil-thick solder layer frequently composed of eutectic lead-tin. The die-attach layer serves as a mechanical support, an electrical interconnection and a primary heat dissipation path. For a perfectly bonded solder/copper interface, the intrinsic reasons of an ITR are usually due to the mismatched crystal structure and the difference of elastic moduli across the interface, which result in electron and phonon scattering at the interface [2]. In practice, further contributions to ITR may come from poor wetting of the substrate by the solder because of surface oxidation and contamination and interfacial voids. The purpose of this study was to explore the feasibility of using the flash technique, initially developed by Parker *et al*. [3] for measuring thermal diffusivity of single phase materials and subsequently extended to multilayer samples [4 - 6], to determine the ITR of solder/copper interfaces.

Experimental

The materials in this study consisted of pure copper [Alloy 101 Oxygen-Free (Electronic Grade), McMaster] and a eutectic composition of lead-tin solder (Sn-37Pb, Easy ProfileTM 256, Kester). Two sets of specimens were prepared. The bi-layered specimens consisted of one copper layer and one solder layer with only one solder/copper interface in each specimen. The tri-layered specimens consisted of a sandwich of the Cu/solder/Cu with two solder/copper interfaces. The copper layers were in form of rectangular cylinders with a diameter of 1.27 cm and their thicknesses were measured by a micrometer. The solder layers were formed by reflowing the eutectic lead-tin solder paste, their thicknesses controlled by varying the amount of solder paste. The specimens were then cleaned and polished to obtain rectangular cylinders and the thicknesses of the solder-layers were measured directly in an optical microscope with micrometer resolution.

The experimental conditions described by Parker *et al.* [3], the ASTM method E1461-01 [7] and those of Hasselman and Donaldson [8] were followed. The flash source consisted of an Apollo Nd-glass laser with a beam diameter of 1.56 cm, a wavelength of 1.06 μm and a pulse width of approximate 250 μs. The flash was passed through a beam expander which allowed using the central portion of the beam, which generally is spatially more uniform than at edges of the beam. The uniformity of the radiation which impinged on the sample was checked by using photo-sensitive foot-print paper. Following the spatially uniform radiation of the flash on one side of the specimen, the transient temperature of the opposite face of the specimen was monitored by a liquid-N2 cooled InSb infrared detector (Electro-Optical Systems, Inc., Malvern, PA). The time (*t1/2*) to reach one half of the final temperature at which the sample reached thermal equilibrium was recorded. Each specimen was measured five times. The estimated accuracy of *t1/2* is about 2%.

To obtain the solder/copper ITR, bulk thermophysical properties of both solder and copper - density ρ, specific heat c and thermal diffusivity α - have to be known accurately. The density values were obtained by the Archimedes' method. The specific heat values were measured using the differential scanning calorimetry method. The thermal diffusivities of the solder and copper were determined from disc-shaped pure solder and pure copper specimens, respectively, by the flash technique using Parker's equation [3]

$$\alpha = 0.1388 l^2 / t_{1/2} \qquad (1)$$

where α is the thermal diffusivity, l is the thickness of the disc-shaped specimen, and *t1/2* is the half temperature rise time at the specimen's rear surface. In the case of single phase specimens, Eq. (1) can be used directly to obtain the thermal diffusivity of the material once the half temperature rise time is known.

The solder/copper ITR in the bi-layered specimens was then determined with the appropriate computational technique developed by Lee [4]. In the method, the density, specific heat and thermal diffusivity of solder and copper and the half temperature rise time at the rear solder surface were used as inputs to derive the solder/copper ITR using commercially available software. The half temperature rise times of bi-layered specimens were measured again by the flash technique.

Two methods were used to derive the ITR in the tri-layered specimens. The first method was used by Hasselman *et al.* [5] to study the ITRs of thermal adhesives for an electronic packaging application. In the method, the bulk thermal resistance of the solder layer *Rsolder* plus the two solder/copper ITRs, *Ri*, which constitute the total middle layer thermal resistance *Rtotal*, are given by:

$$R_{total} = R_{solder} + 2R_i = \frac{d}{k} + 2R_i \qquad (2)$$

where *d* and *k* are the thickness and thermal conductivity of the solder layer, respectively. Since *Rtotal* includes all the thermal resistance in the tri-layered specimens other than the two copper layers, it can be determined using the same method for the bi-layered specimens [4]. Then *Ri* was obtained by the least-square-linear fit and extrapolating the thickness *d* to zero in the *Rtotal* vs. *d* plot.

The second method obtained R_i directly in the tri-layered specimens using finite-element analysis (FEA). In the method, finite-element models were created in I-DEAS™ following the geometries of the tri-layered specimens. In I-DEAS™, it is convenient to characterize an ITR by defining a "thermal coupling coefficient" (which is the reciprocal of the ITR) at the interfaces of the composite specimens. By simulating the laser flash and boundary conditions of the experiment, a typical temperature variation curve at the rear surface of a specimen is plotted in Fig. 1. The half temperature rise time $t_{1/2}$ was obtained from the intersection of the rear surface temperature transient curve and the T =

$T_f/2$ line as shown, where T_f is the final temperature rise in the specimen after thermal equilibrium. The rear surface temperature transient curve was re-plotted more accurately in Fig. 2. By comparing the FEA simulated $t_{1/2}$ with the measured $t_{1/2}$ from the flash experiment, a new value of ITR R_i was chosen for the second try, and so on until the two $t_{1/2}$ match. By this reversed method, R_i could be determined.

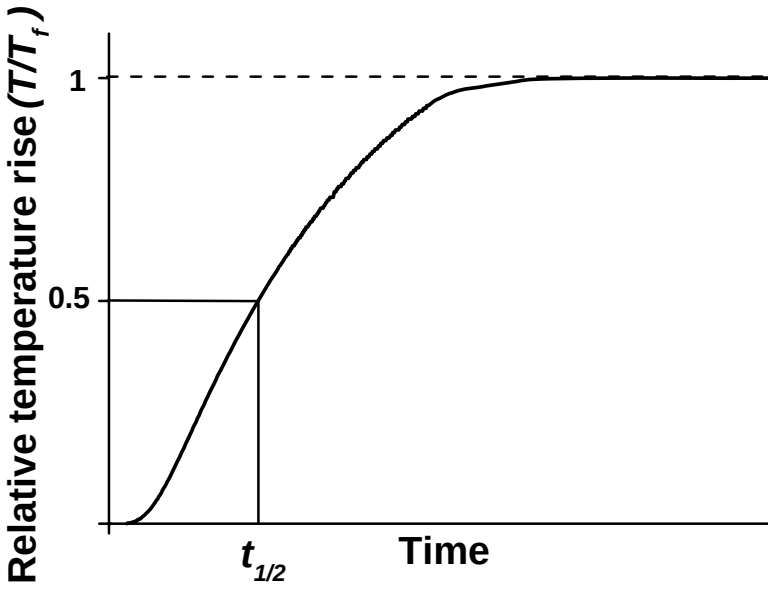


Fig. 1. A typical temperature transient curve at the rear surface of a specimen after the laser flash.

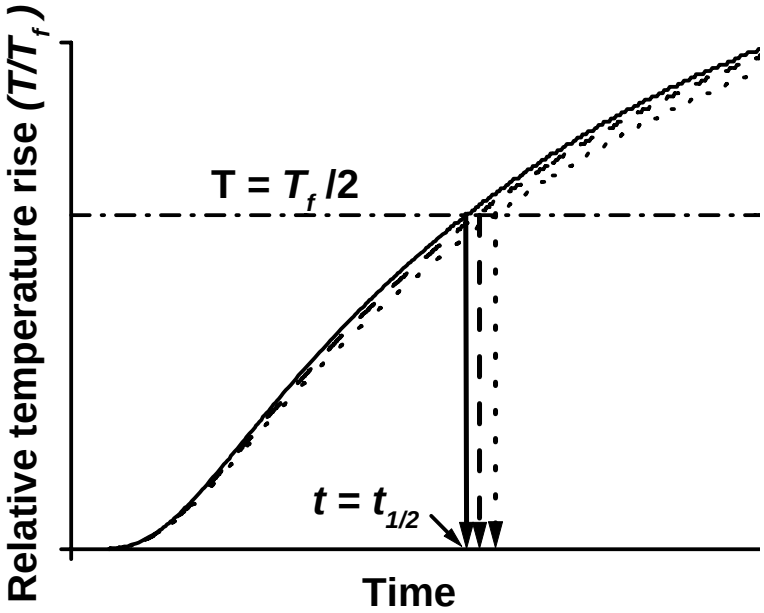


Fig. 2. The changes of the temperature transient curve at the rear surface of a specimen when changing the values of the solder/copper interfacial thermal resistance.

Experimental Results and Discussion

The thickness values of the solder and copper layers in the bi- and tri-layered specimens are presented in Tables I and II, respectively. The experimental data of half temperature rise time are listed in the last columns.

Table I: Experimental data of the bi-layered specimens.

2-layered	Thicknesses of bi-layered specimens		Half temp. rise time $t_{1/2}$ (ms)
	Flashed copper (cm)	Rear solder (cm)	
#1	0.2373	0.1768	48.6
#2	0.3145	0.1247	40.8
#3	0.4549	0.1281	60.0
#4	0.4172	0.0991	43.6
#5	0.3650	0.1108	43.0
#6	0.4014	0.1264	52.2

Table II: Experimental data of the tri-layered specimens.

3-layered	Thicknesses of tri-layered specimens			Half temp. rise time $t_{1/2}$ (ms)
	Flashed copper (cm)	Middle solder (cm)	Rear copper (cm)	
#1	0.3780	0.0041	0.2751	66.8
#2	0.2791	0.0050	0.3141	55.2
#3	0.1261	0.0214	0.3207	47.6
#4	0.2658	0.0248	0.2750	66.0
#5	0.2120	0.0279	0.2169	52.4
#6	0.2287	0.0340	0.2801	67.8
#7	0.2608	0.0450	0.3202	99.2
#8	0.1910	0.0534	0.1896	55.8

The values of the density, specific heat, and diffusivity for the solder and copper are listed in Table III. The corresponding thermal conductivity values were obtained by multiplying the thermal diffusivity, density and specific heat. Data from a website [9] are also listed for reference.

The values of R_{total} obtained from the tri-layered specimens using the first method are plotted versus the thickness of solder layer in Fig. 3. A linear curve-fit (see Eq. (2)) of the data results in values of 0.0109 Kcm^2/W for the solder/copper ITR R_i and 0.355 W/K-cm for the thermal conductivity of the solder, respectively. The 95% confidence limit gives the uncertainty range of the R_i about 0.005~0.020 Kcm^2/W as shown in Fig. 3. In view of the uncertainties, the thermal conductivity value for the solder agrees fairly well with the corresponding value of 0.47 W/cm-K obtained with the bulk sample. Exact agreement is not expected as in the tri-layered samples grain growth is constrained by the

pressure of the neighboring copper which could result in a textured structure with electrical and thermal properties different from those of the bulk sample.

Table III: Bulk properties of solder and copper for the calculation of the solder/copper interfacial thermal resistance.

		Density ρ (g/cm^3)	Specific heat c (J/g-K)	Diffusivity α (cm^2/s)	Conductivity k (W/K-cm)
Sn-37Pb	Reference	8.47	0.195	0.309	0.51
	Measured	8.22 (5×2)	0.185 (2×4)	0.310 (6×5)	0.47
Cu	Reference	8.94	0.385	1.150	3.96
	Measured	8.91 (5×2)	0.372 (2×4)	1.026 (8×5)	3.41

(#×#): number of specimen prepared × times of each specimen measured.

Table IV: Summary of the solder/copper ITR data obtained from the bi-layered specimens using Lee's method and those from the tri-layered specimens using the FEA method.

Specimen #	Solder/copper ITR R_i (Kcm^2/W)	
	2-layered	3-layered
#1	0.022	0.017
#2	0.029	0.014
#3	0.020	0.018
#4	0.011	0.012
#5	0.033	0.022
#6	0.025	0.018
#7	---	0.028
#8	---	0.019
Average	0.023	0.018

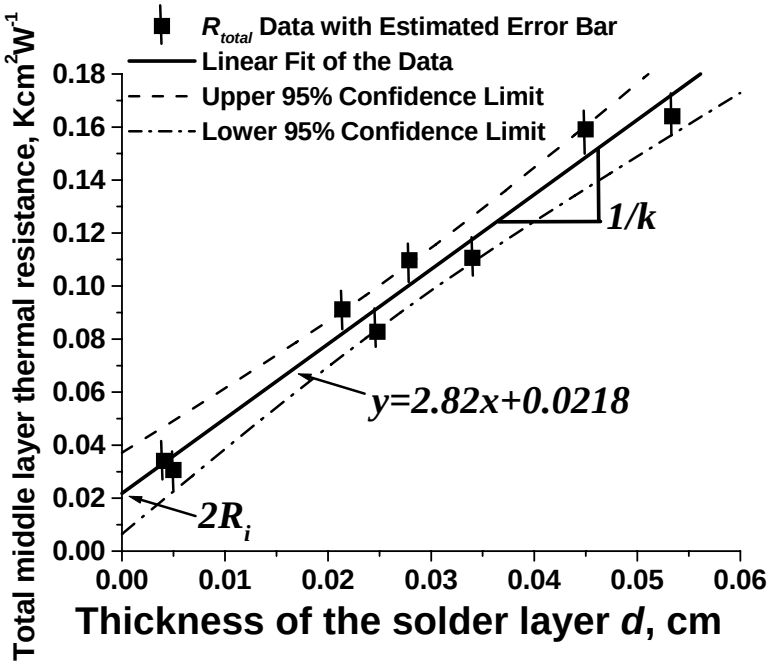
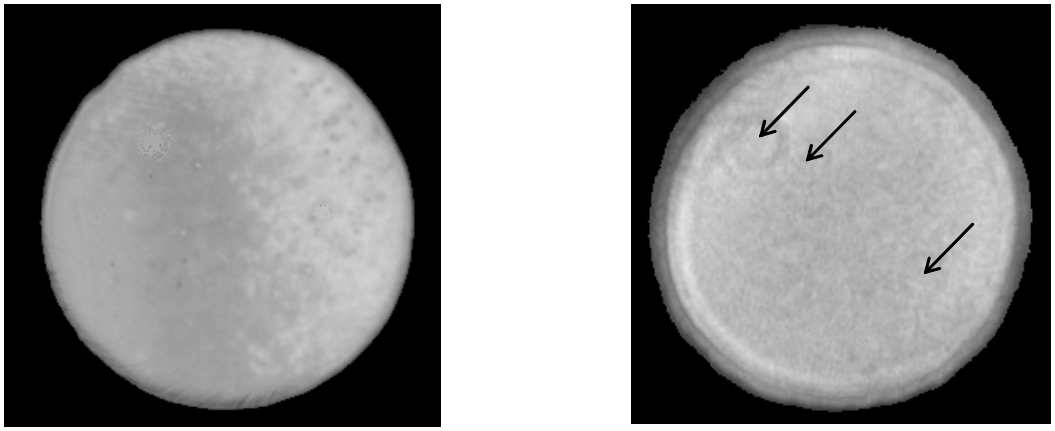


Fig. 3. Total thermal resistance R_{total} of solder in the tri-layered specimens as a function of the solder layer thickness.

All the solder/copper ITR R_i results obtained from the bi-layered specimens using Lee's method [4] and those from the tri-layered specimens using the FEA method are summarized in Table IV. The solder/copper ITR values were found to be in a range of 0.011~0.033 Kcm^2/W and with an average of 0.020±0.005 Kcm^2/W. Again, the agreement between both sets of results from the bi- and tri-layered specimens is considered excellent.



(a) (b)

Fig. 4. SAM images of the solder/copper interface in the bi-layered specimens #4 (a) and #5 (b), respectively. Both specimens have a diameter of 1.27 cm. Arrows in (b) indicate the low density areas at the solder/copper interface.

To investigate the reasons for the range in the solder/copper ITR results, a pulse-echo mode of scanning acoustic microscopy (SAM) was used to check the solder/copper interfaces. In the SAM mode, the transducer produces a high frequency sound wave which interacts with the sample. The reflected sound was used to produce images. Whenever a sudden change in acoustic impedance is encountered, like at a material boundary, a portion of sound is reflected and the remainder propagates through the boundary. The uniformity of an interface of interest can be related to the image brightness. Fig. 4 shows two of the SAM images obtained from the bi-layered specimens #4 and #5, respectively, by a 15 MHz sonic transducer. From Fig. 4, one can see that the solder/copper interface in specimen #4 is more uniform than that in #5; this is believed to be the reason why the ITR in specimen #4 is much smaller than that in #5. The latter shows at least three round-shaped low density areas at the solder/copper interface with diameters of 1~2 mm, which could be poor wetting areas/voids induced at the interface during the solder reflow. As discussed before, the imperfection could add a large extrinsic ITR onto the intrinsic ITR. In an electronic package, the non-uniform structures

are very harmful to the thermal performance and reliability of the interconnection layers and they should be avoided as much as possible.

Finally, it is pointed out that the ~0.02 Kcm^2/W solder-related ITR is equivalent to the thermal resistance of a ~100 μm thick eutectic lead-tin solder layer, which means that for a solder layer less than 100 μm thick, the interfacial contact resistance will contribute more than half of the total thermal resistance. Therefore, it is clear that a designer of electronic packages must address both the bulk and interfacial resistance.

Conclusion

We demonstrated the feasibility of using the flash technique for measuring eutectic lead-tin solder/copper interfacial thermal resistance (ITR) from both the bi- and tri-layered specimens. The solder/copper ITR was found to be about 0.020 Kcm^2/W and within a range of 0.011~0.033 Kcm^2/W. After consideration of the measurement uncertainties and the extrinsic reasons for the existence of ITR, the results from both the bi- and tri-layered specimens show excellent agreement.

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Vita

Guofeng Bai was born in Zhengding County, Hebei Province, China on March 26th, 1974. He received his B.S. degree and M.S. degree both in physics from Tianjin University in 1995 and Beijing University in 1998, respectively. Then he went to Dartmouth College, Hanover, New Hampshire and got his second M.S. degree in materials science. Since 2000, he has been with the Center for Power Electronics Systems (CPES) and Department of Materials Science and Engineering at Virginia Polytechnic Institute and State University, Blacksburg, Virginia.