7. HIGH-FREQUENCY NOISE REDUCTION IN PARALLEL THREE-PHASE CONVERTERS

Parallel converters can reduce differential-mode current ripple by using an interleaving technique. Due to its symmetrical architecture, the common-mode dv/dt noise can also be significantly reduced using an interleaved center-aligned symmetrical PWM scheme. The converters discussed in this chapter are current-bidirectional converters only. The concept, however, can also be generalized to current-unidirectional converters.

Based on the concept that a symmetrical circuit can reduce common-mode dv/dt noise, this work presents an inverter power supply without common-mode noise. The inverter can be used for unbalanced and nonlinear load. With a proposed modulation scheme and control, the inverter can deal with both high- and low-frequency common-mode components.

7.1 DIFFERENTIAL-MODE AND COMMON-MODE NOISE REDUCTION IN A PARALLEL CURRENT-BIDIRECTIONAL CONVERTER SYSTEM

If the two parallel voltage source inverters (for example, and as shown in Figure 7.1) are synchronized, it is common practice to use an interleaving operation, which shifts the two PWMs by 180 degrees (half a switching cycle).

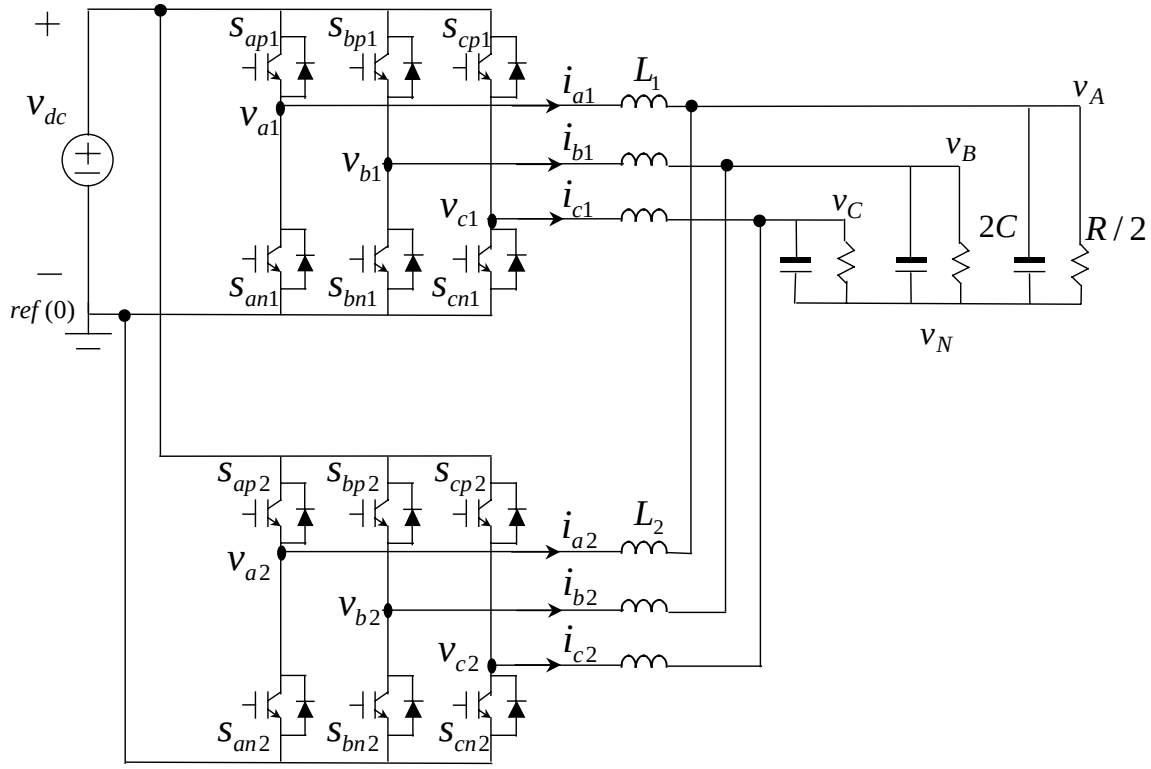


Figure 7.1 Parallel voltage-source inverters.

Figures 7.2 and 7.3 show two typical PWM schemes, asymmetrical and symmetrical, with alternating zero vectors. Figures 7.4 and 7.5 show the individual converter current ripple and the combined current ripple of the two schemes.

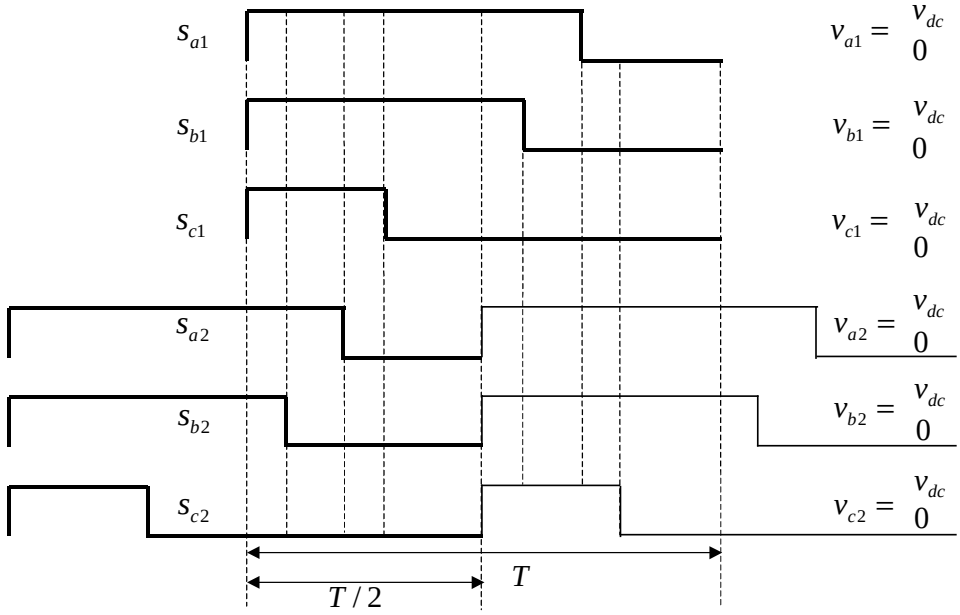


Figure 7.2 Interleaved asymmetrical PWM scheme.

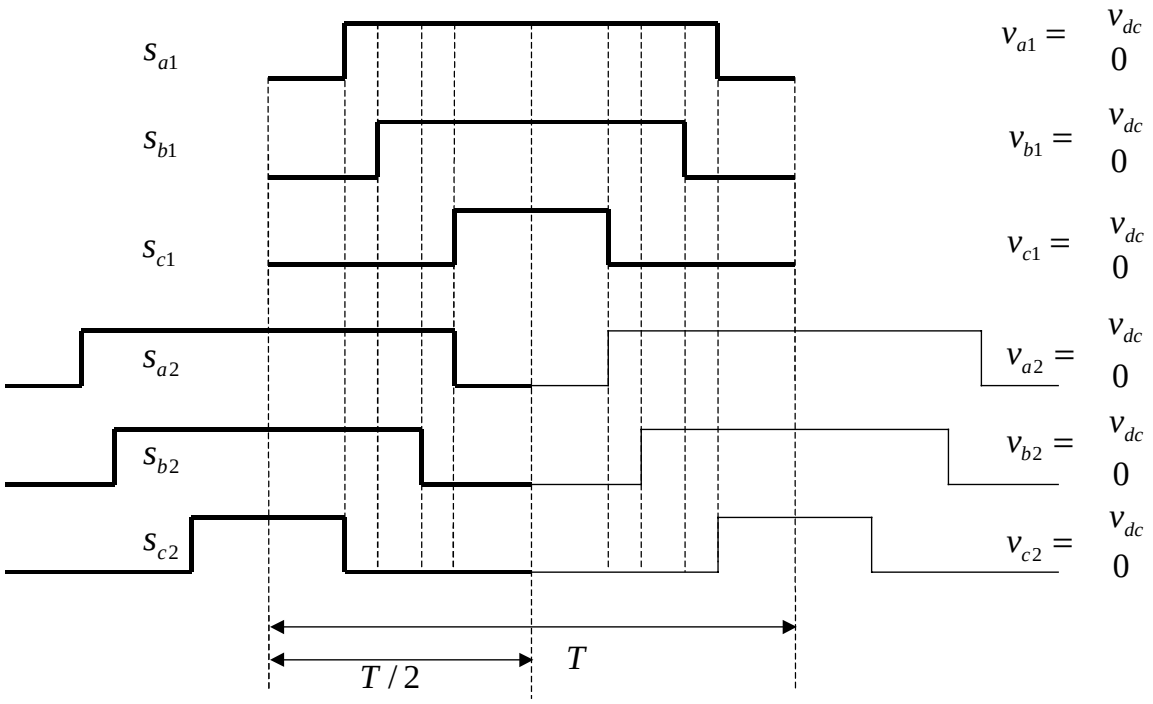


Figure 7.3 Interleaved symmetrical PWM scheme.

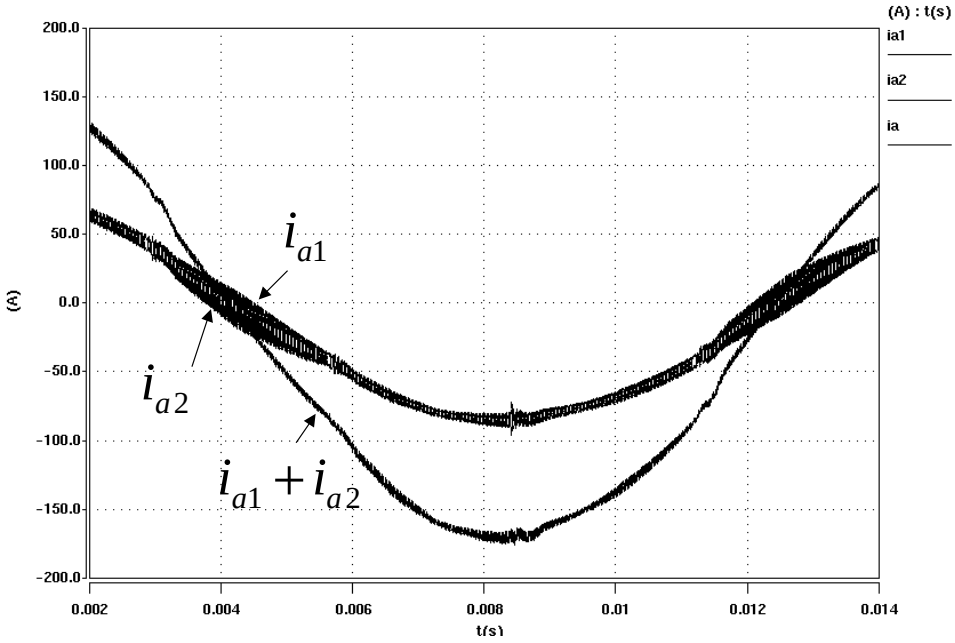


Figure 7.4 Simulated differential-mode current ripples with interleaved asymmetrical PWM scheme.

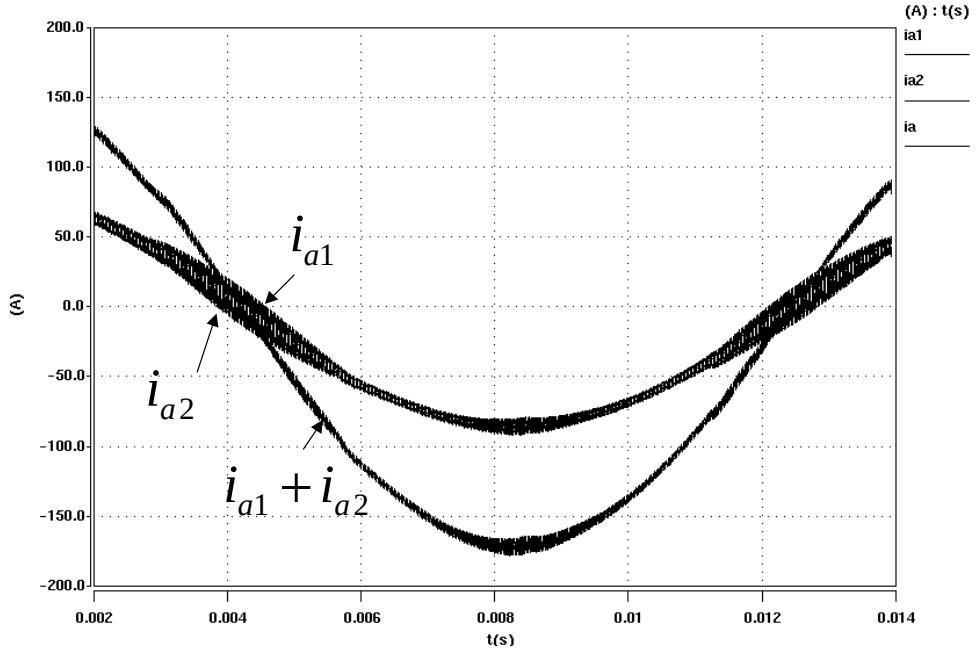


Figure 7.5 Simulated differential-mode current ripples with interleaved symmetrical PWM scheme.

It can be seen that the two schemes have little difference in the interleaving effect. However, there is significant difference in their levels of common-mode dv/dt noise, as shown in Figures 7.6 and 7.7. This can be explained as follows.

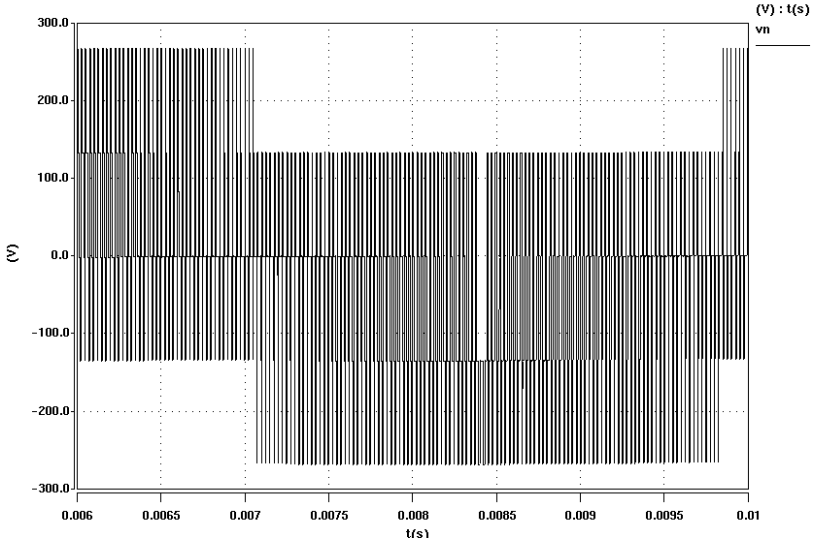


Figure 7.6 Simulated common-mode voltage with interleaved asymmetrical PWM scheme.

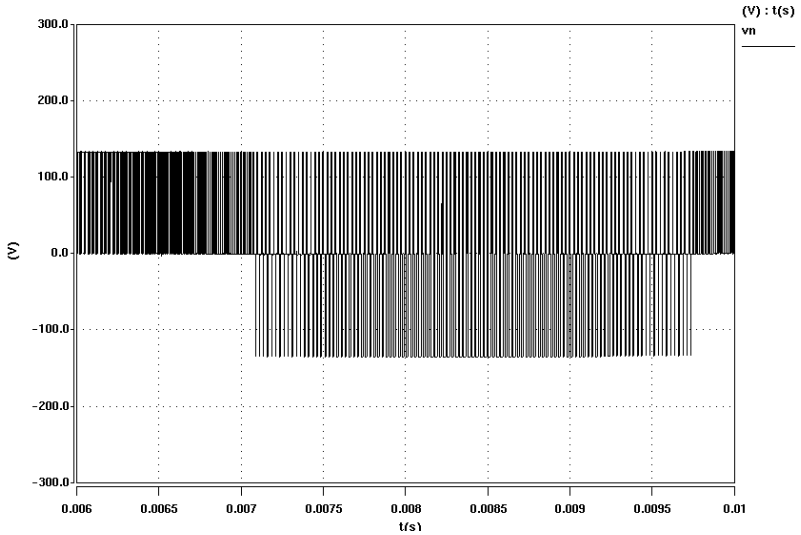


Figure 7.7 Simulated common-mode voltage with interleaved symmetrical PWM scheme.

The circuit in Figure 7.1 has equations:

$$v_{a1} = L\frac{di_{a1}}{dt} + Zi_a + v_n,\ v_{b1} = L\frac{di_{b1}}{dt} + Zi_b + v_n,\ v_{c1} = L\frac{di_{c1}}{dt} + Zi_c + v_n, \quad (7.1)$$

$$v_{a2} = L\frac{di_{a2}}{dt} + Zi_a + v_n,\ v_{b2} = L\frac{di_{b2}}{dt} + Zi_b + v_n,\ v_{c2} = L\frac{di_{c2}}{dt} + Zi_c + v_n, \quad (7.2)$$

where Z is the impedance of the resistor and the capacitor in parallel.

Summing up all equations in (7.1) and (7.2), the following equation can be obtained

$$v_{a1} + v_{b1} + v_{c1} + v_{a2} + v_{b2} + v_{c2} = L\frac{d(i_{a1} + i_{b1} + i_{c1} + i_{a2} + i_{b2} + i_{c2})}{dt} + 2Z(i_a + i_b + i_c) + 6v_n. \quad (7.3)$$

Since

$$i_{a1} + i_{b1} + i_{c1} + i_{a2} + i_{b2} + i_{c2} = i_a + i_b + i_c = 0, \quad (7.4)$$

the common-mode voltage v_n is then derived as follows:

$$v_n = \frac{v_{a1} + v_{b1} + v_{c1} + v_{a2} + v_{b2} + v_{c2}}{6}. \quad (7.5)$$

Based on (7.5), Figures 7.8 and 7.9 explain why the common-mode dv/dt noise of the symmetrical PWM is significantly smaller than that of the asymmetrical scheme.

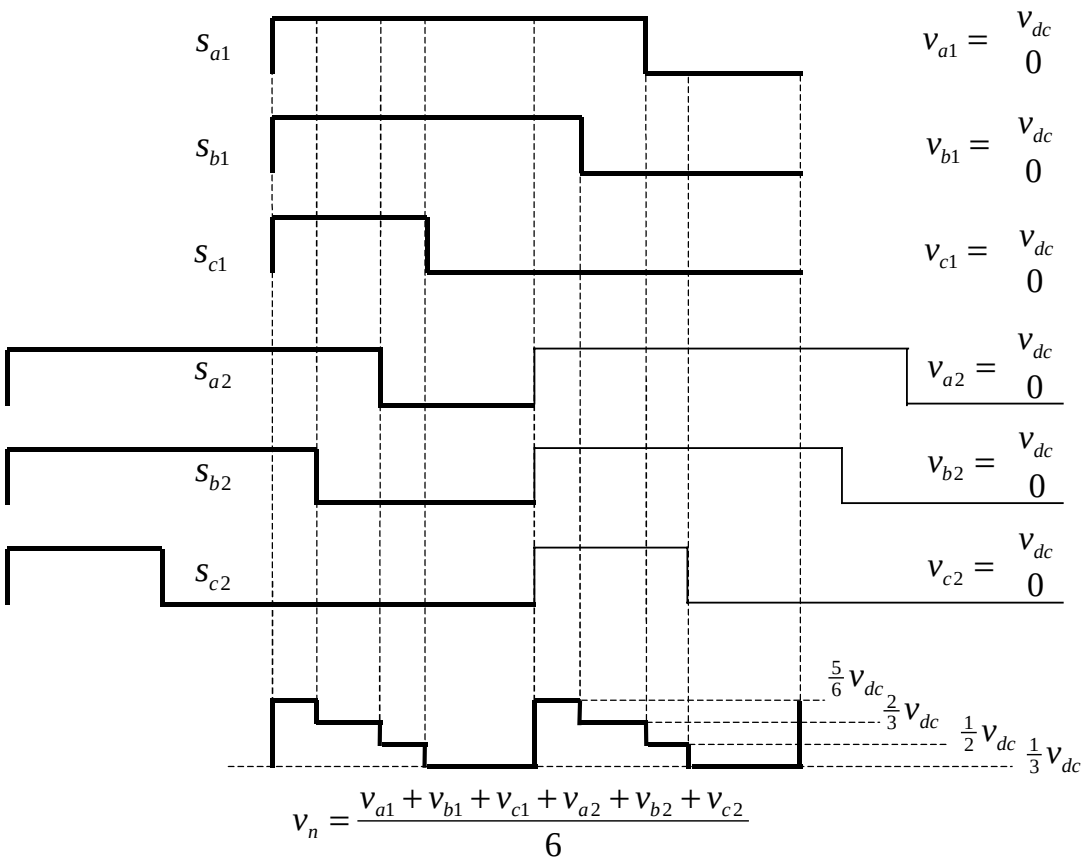


Figure 7.8 Derived common-mode voltage with interleaved asymmetrical PWM scheme.

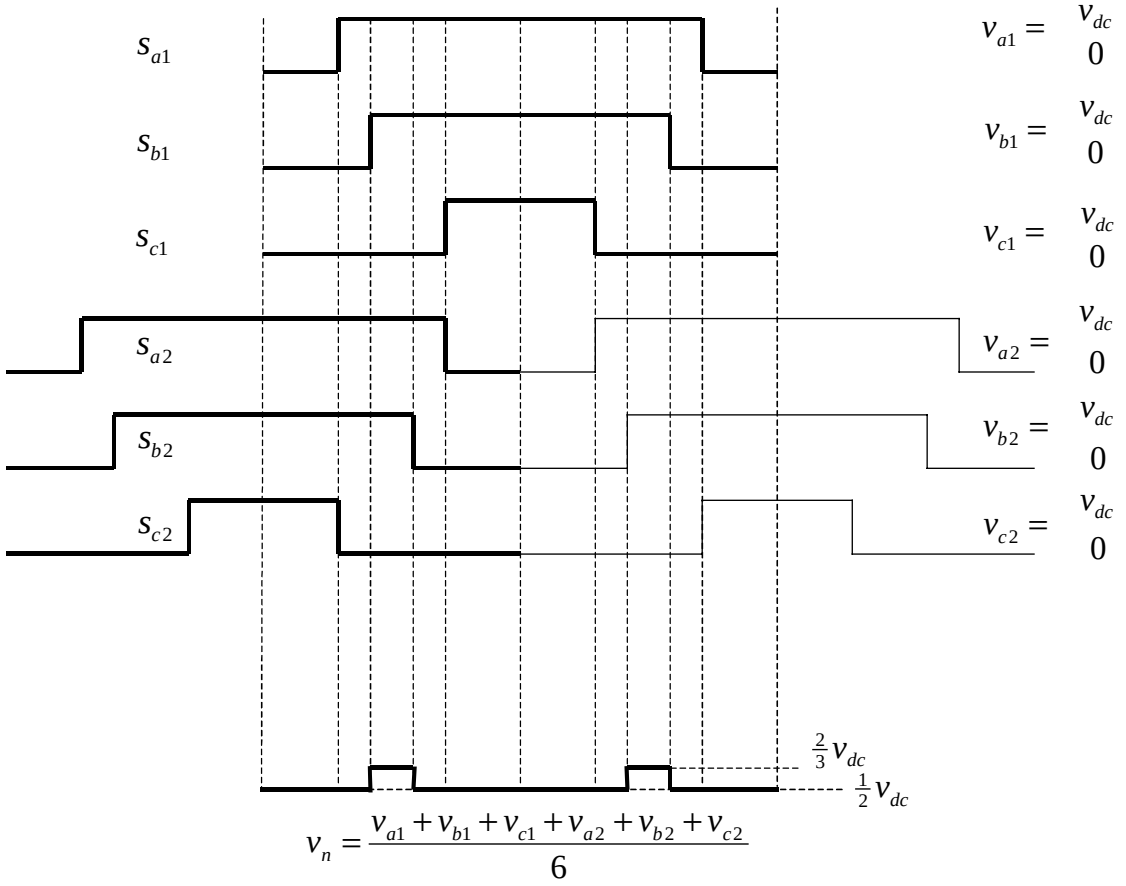


Figure 7.9 Derived common-mode voltage with interleaved symmetrical PWM scheme.

The common-mode noise of the parallel converter system with interleaved symmetrical PWM has much smaller magnitude and fewer jumps than that of the single converter and the asymmetrical scheme.

Therefore, it is desirable to use an interleaved symmetrical PWM scheme in the parallel current-bidirectional converter system in order to reduce both differential-mode and common-mode noise.

Similar to the idea that a symmetrical circuit can reduce common-mode noise, the next section introduces a new three-phase, four-leg inverter that can deal with both low and high frequencies' common-mode components.

7.2 AN INVERTER POWER SUPPLY FOR UNBALANCED AND NONLINEAR LOAD WITHOUT COMMON-MODE NOISE

Some uninterruptible power supplies (UPSs) and active filters are required to provide three-phase, four-wire in order to deal with unbalanced and nonlinear load. There are two popular topologies used today. One is a three-phase, three-leg inverter with split DC-link capacitors [66]-[70]. The other is a three-phase, four-leg inverter [71]-[81], as shown in Figure 7.10. The neutral inductor of the four-leg inverter is optional. Although the four-leg converter requires two additional switches, it is advantageous over the spilt capacitors' solution because of its much smaller DC capacitors, better DC bus voltage utilization and output voltage regulation.

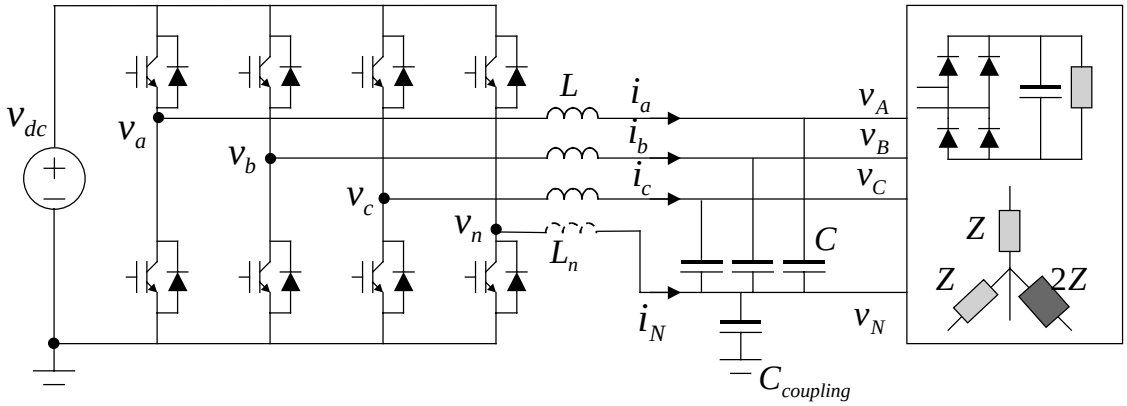


Figure 7.10 Three-phase, four-leg inverter.

With the advancement of fast switching devices, power converters are built with increasing switching frequency. This leads to more compact size and better dynamic performance for the converters. However, these converters in turn cause high-frequency electromagnetic interference (EMI) noise, such as differential-mode and common-mode noise. The differential-mode noise is usually well taken care of by input and output filters during the power stage design. The common-mode noise, however, is difficult to predict. There is no solid design guideline in most applications. To mitigate the common-mode noise, passive solutions are traditionally used. Active solutions, however, are becoming popular due to the reduced size of the overall system. Similar to the idea that a symmetrical circuit can reduce common-mode dv/dt noise, a new concept of common-mode noise reduction was proposed in [46] by adding a fourth leg to a three-phase three-

leg converter. The concept has been experimentally validated in motor drive applications [46].

Based on that concept, this section presents a modified three-phase, four-leg inverter that has an additional capacitor C_n in series with the inductor L_n in the fourth leg, as shown in Figure 7.11, in order to reduce the common-mode dv/dt noise. The objective of this chapter is to investigate the effectiveness of the modified fourth leg in handling unbalanced and nonlinear load, in addition to its ability to reduce common-mode noise.

With the modified fourth leg, the average model of the four-leg inverter is derived. Based on the model, the control design is also modified with respect to the modified fourth leg. A new SVM scheme is proposed to both reduce the common-mode noise and to synthesize a reference vector in a three-dimensional space. With the designed control and the modulation, not only can the inverter nearly eliminate the high-frequency common-mode noise, but it can also handle low-frequency common-mode components that occur due to unbalanced and nonlinear load.

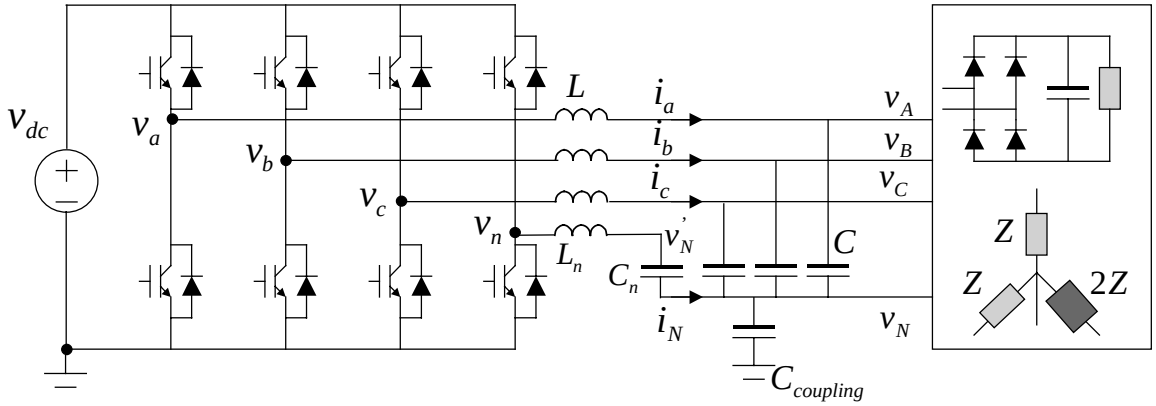


Figure 7.11 New three-phase, four-leg inverter with active common-mode filter function.

7.2.1 Modeling of the Four-Leg Inverter

Applying the phase-leg averaging technique, the average model of the four-leg inverter in Figure 7.11 can be obtained, as shown in Figure 7.12. The load is represented by the load current.

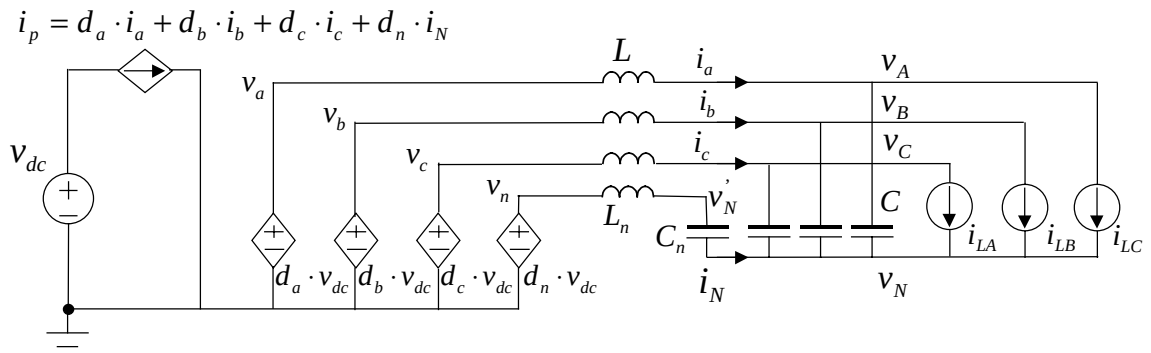


Figure 7.12 Average model of new four-leg inverter based on phase-leg averaging.

The averaged switching network is:

$$i_p = \begin{bmatrix} d_a & d_b & d_c & d_n \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_N \end{bmatrix}, \tag{7.6}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \\ v_n \end{bmatrix} = \begin{bmatrix} d_a \\ d_b \\ d_c \\ d_n \end{bmatrix} \cdot v_{dc} . \tag{7.7}$$

Since the control objective of the inverter is to make the output phase-to-neutral voltages sinusoidal, as defined in (2.14), it is desirable to describe the model based on phase-to-neutral variables. In the circuit, it is obvious that

$$i_a + i_b + i_c + i_N = 0 . \tag{7.8}$$

The following equations can be easily obtained from (7.6)-(7.8).

$$i_p = \begin{bmatrix} d_{an} & d_{bn} & d_{cn} \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \tag{7.9}$$

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} \cdot v_{dc} . \tag{7.10}$$

where:

$$\begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} = \begin{bmatrix} d_a - d_n \\ d_b - d_n \\ d_c - d_n \end{bmatrix}. \tag{7.11}$$

As a result, the average model is shown in Figure 7.13.

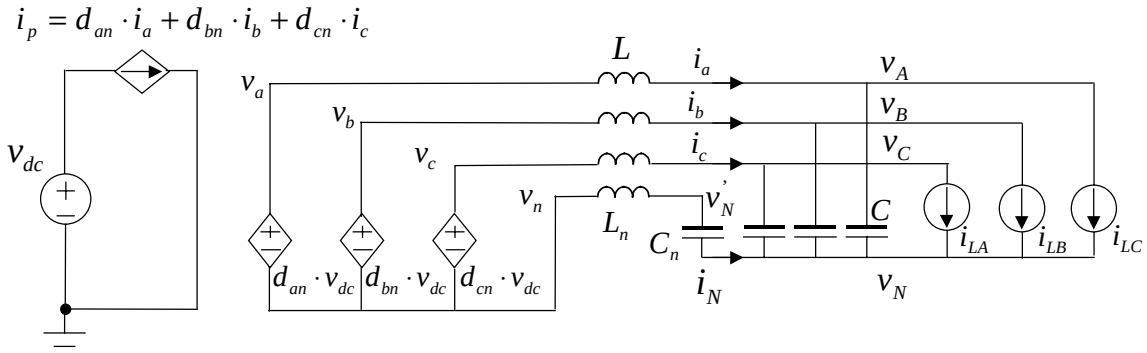


Figure 7.13 Simplified average model of new four-leg inverter.

It should be noted that, in Figure 7.13, the controlled voltage sources are the voltage potentials between the three phases to the neutral phase. Therefore, the ground connection no longer appears in the AC side.

The differential equations of the average model are:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{1}{L}\begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} \cdot v_{dc} - \frac{1}{L}\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{N'N} \\ v_{N'N} \\ v_{N'N} \end{bmatrix} + \frac{L_n}{L}\frac{d}{dt}\begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix}, \tag{7.12}$$

$$\frac{d}{dt}\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \frac{1}{C}\begin{bmatrix} i_{LA} \\ i_{LB} \\ i_{LC} \end{bmatrix}, \tag{7.13}$$

$$\frac{dv_{N'N}}{dt} = \frac{1}{C_n} i_N, \tag{7.14}$$

where

$$v_{N'N} = v_{N'} - v_N. \tag{7.15}$$

Transforming the model in the stationary into one in the rotating coordinates, one can obtain:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \frac{1}{L}\begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} \cdot v_{dc} - \frac{1}{L}\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} + \frac{1}{L}\begin{bmatrix} 0 \\ 0 \\ \sqrt{3}v_{N'N} \end{bmatrix} + \frac{L_n}{L}\frac{d}{dt}\begin{bmatrix} 0 \\ 0 \\ \sqrt{3}i_n \end{bmatrix} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} \quad (7.16)$$

$$\frac{d}{dt}\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \frac{1}{C}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} - \frac{1}{C}\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{Lo} \end{bmatrix} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix}. \quad (7.17)$$

Since

$$i_N = -(i_a + i_b + i_c) = -\sqrt{3}i_o, \quad (7.18)$$

then

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \frac{1}{L}\begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} \cdot v_{dc} - \frac{1}{L}\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} + \frac{1}{L}\begin{bmatrix} 0 \\ 0 \\ \sqrt{3}v_{N'N} \end{bmatrix} + \frac{L_n}{L}\frac{d}{dt}\begin{bmatrix} 0 \\ 0 \\ 3i_o \end{bmatrix} - \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}, \quad (7.19)$$

$$\frac{d(\sqrt{3}v_{N'N})}{dt} = \frac{1}{C_n}3i_o. \quad (7.20)$$

The equivalent circuit is shown in Figure 7.14. The voltage across the capacitor $C_n/3$ is $\sqrt{3}v_{N'N}$.

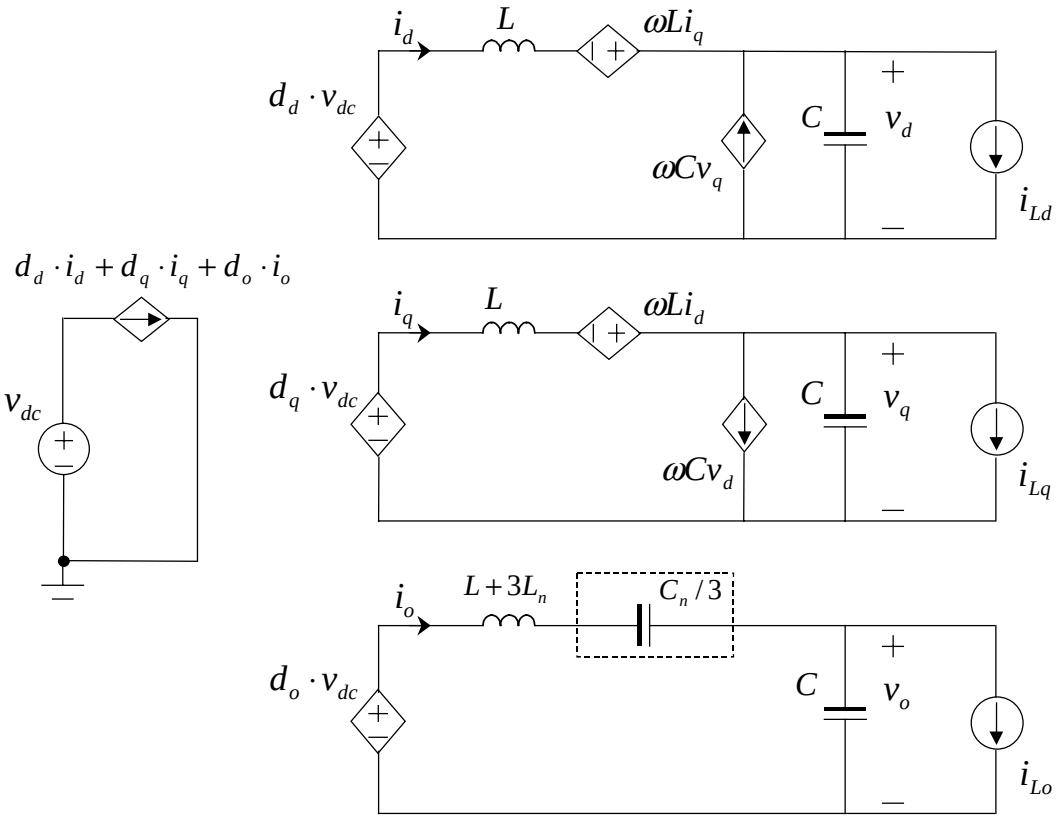


Figure 7.14 Average model of new four-leg inverter in rotating coordinates.

This model is different from the model of the conventional three-phase four-leg inverter in Figure 7.10 only by the additional capacitor, framed with a dotted rectangle, in the o channel [73], [77], [78]. Therefore, the control design for the d and q channel is the same as the design for a conventional inverter. Only the o channel needs to be reexamined.

Because of the series capacitance, the new o-channel open-loop control-to-output transfer function has the form:

$$\frac{\tilde{v}_o}{\tilde{d}_o} = \frac{K \cdot s}{(s/p_1 + 1)(s/p + 1)(s/p^* + 1)}, \tag{7.21}$$

where K, p_1 and p depend on the converter parameters.

The converters' parameters in this chapter are given below.

V_{dc}=800V, $V_{xn,rms}$=120V, (x=a,b,c), P_{Load}=100kW (three-phase), f_{sw}=10 kHz, L=660µH, C=210µF, L_n=660µH, C_n=210µF for the inverter in Figure 7.11 , C_n=∞µF for the inverter in Figure 7.10, common-mode capacitive coupling $C_{coupling}$=1nF, unbalanced

resistive load: P_a=33 kW, P_b=33 kW, P_c=28 kW, nonlinear load: combined resistive load (80kW) and three single-phase diode rectifiers(20kW).

The Bode plot of the transfer function is simulated as shown in Figure 7.15, both with and without C_n.

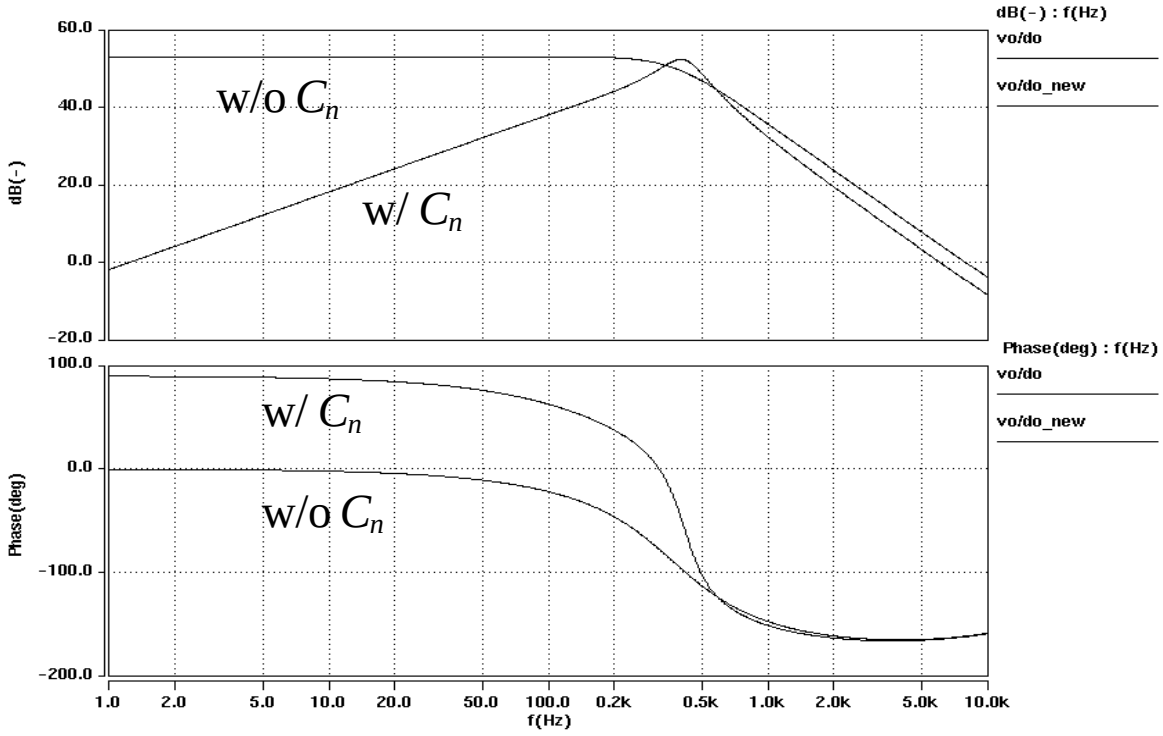


Figure 7.15 Transfer function $\tilde{v}_o / \tilde{d}_o$ with and without neutral capacitor.

Because of the capacitor $C_n/3$, the o-channel transfer function has a zero at the origin. In order to regulate the neutral line voltage without steady-state error, a compensator with a double integrator is necessary:

$$H_o = \frac{1}{s} \cdot (K_p + \frac{K_i}{s}). \tag{7.22}$$

The o-channel loop gain with the designed regulator is plotted in Figure 7.16.

Although a compensator with more poles and zeros can be used to optimize the loop gain, it is usually sufficient to use the integrator and proportional-integral regulator to characterize the dominant loop gain.

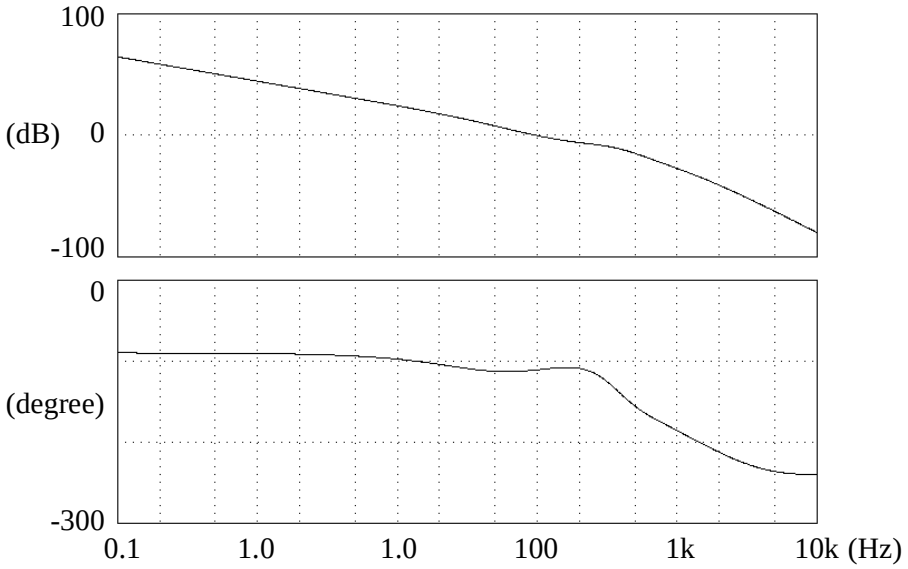


Figure 7.16 O-channel loop gain.

7.2.2 A New Modulation Scheme

With the additional capacitor, the new inverter is able to eliminate the common-mode noise.

In Figure 7.11, there are:

$$\begin{aligned} v_a &= L\frac{di_a}{dt} + v_{AN} + v_N \\ v_b &= L\frac{di_b}{dt} + v_{BN} + v_N \\ v_c &= L\frac{di_c}{dt} + v_{CN} + v_N \\ v_n &= L\frac{di_N}{dt} + v_{N'N} + v_N \end{aligned} \tag{7.23}$$

Summing them up:

$$v_a + v_b + v_c + v_n = L\frac{d(i_a + i_b + i_c + i_N)}{dt} + (v_{AN} + v_{BN} + v_{CN} + v_{N'N}) + 4v_N \,. \tag{7.24}$$

Based on (7.8),

$$v_N = \frac{v_a + v_b + v_c + v_n}{4} + \frac{v_{AN} + v_{BN} + v_{CN} + v_{N'N}}{4} \,. \tag{7.25}$$

Because v_{AN} , v_{BN} , v_{CN} and $v_{N'N}$ are the voltages across the capacitors, they normally do not have high dv/dt components. Therefore, the condition to have minimal common-mode dv/dt is to have

$$v_a + v_b + v_c + v_n = \text{constant.} \tag{7.26}$$

With the reference at the negative DC point, the constant is $v_{dc} / 2$.

The common-mode voltage v_N will remain very small provided that the modulation constraint in (7.26) is satisfied.

Some modulation schemes have been proposed to satisfy the condition in (7.27) [47]. However, they only synthesize the reference vector in a plane (not in a three-dimensional space) because they are used in motor drives in which the load is balanced. In the four-leg inverter, the trajectory of a reference vector is in a three-dimensional space when the load is unbalanced or nonlinear.

To modulate the four-leg inverter, a three-dimensional SVM was proposed [78]. In total, there are sixteen switching vectors, as shown in Figure 7.17.

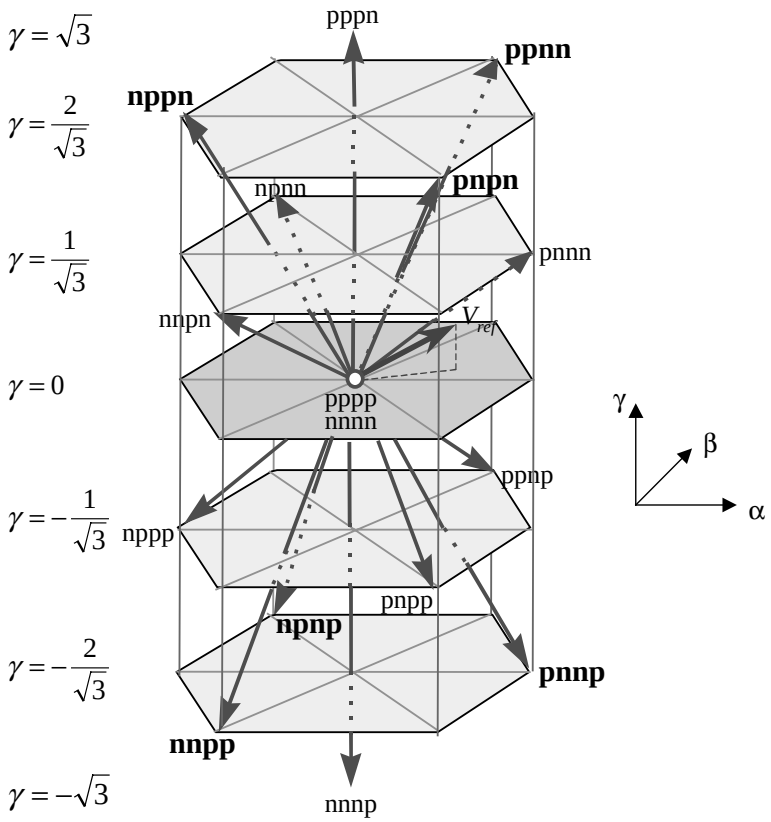


Figure 7.17 Switching vectors in α-β-γ coordinates.

Conventionally, adjacent vectors are used in the synthesis of a reference vector in order to have minimum switching actions and ripples. However, in this case, (7.26) is not satisfied and the common-mode voltage v_N with high-frequency common-mode dv/dt will exist in the system, as shown in Figure 7.18.

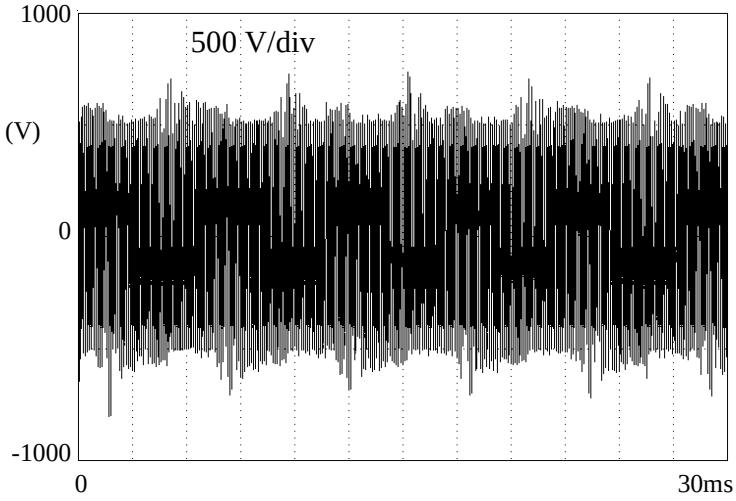


Figure 7.18 Common-mode *dv*/*dt* of conventional inverter modulated with adjacent vectors.

In order to satisfy the condition in (7.26), the previously proposed three-dimensional SVM needs to be modified. Equation (7.26) indicates that only the vectors with two switches connected to the positive rail (p) and two switches connected to the negative rail (n) can be used. In all, there are six available vectors, shown with bold font in Figure 7.17. Three vectors have $\gamma = 2/\sqrt{3}$, while the other three vectors have $\gamma = -2/\sqrt{3}$. Figure 7.19 shows the projections of the six vectors in the α-β plane. It is observed from Figure 7.17 that, although there are only six available vectors because of the restriction in (7.26), the six vectors are still distributed in the three-dimensional space. That means a reference vector in three-dimensional space can still be synthesized by the six vectors. In other words, the modified 3D-SVM can handle unbalanced and nonlinear loads that result in a three-dimensional reference vector trajectory.

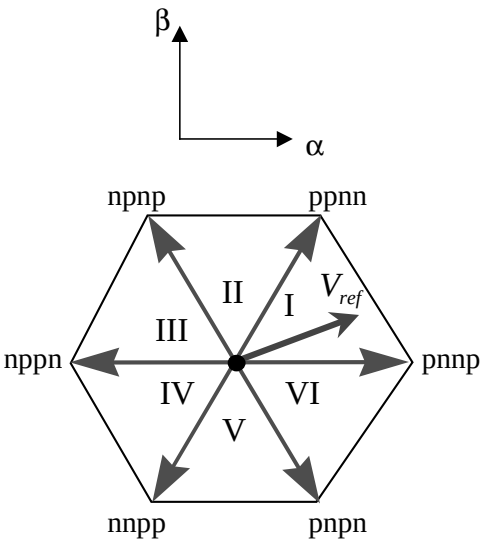


Figure 7.19 Six available switching vectors in α-β plane.

To synthesize the reference vector V_{ref} in Figure 7.17, for example, the vectors pnpn, pnnp, ppnn and npnp are used. Referring to Figure 7.19, the reference vector is synthesized by the most adjacent four vectors in the α-β plane. The following method is used to obtain the duty cycles of the four vectors.

The six vectors in abc coordinates are as follows:

$$
\begin{aligned}
V_{pnnp}^{abc} &= [0 \quad -V_{dc} \quad -V_{dc}]^T, \\
V_{ppnn}^{abc} &= [V_{dc} \quad V_{dc} \quad 0]^T, \\
V_{npnp}^{abc} &= [-V_{dc} \quad 0 \quad -V_{dc}]^T, \\
V_{nppn}^{abc} &= [0 \quad V_{dc} \quad V_{dc}]^T, \\
V_{nnpp}^{abc} &= [-V_{dc} \quad -V_{dc} \quad 0]^T, \\
V_{pnpn}^{abc} &= [V_{dc} \quad 0 \quad V_{dc}]^T.
\end{aligned} \tag{7.27}
$$

The six vectors in the $\alpha\beta\gamma$ coordinates can be obtained by

$$
V^{\alpha\beta\gamma} = T_{abc/\alpha\beta\gamma} \cdot V^{abc}, \tag{7.28}
$$

where

$$T_{abc/\alpha\beta\gamma} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \tag{7.29}$$

$T_{abc/\alpha\beta\gamma}$ is an orthogonal matrix.

Therefore, the six vectors in the $\alpha\beta\gamma$ coordinates are:

$$\begin{aligned}
V_{pnnp}^{\alpha\beta\gamma} &= \left[\frac{\sqrt{2}}{\sqrt{3}}V_{dc} \quad 0 \quad -\frac{2}{\sqrt{3}}V_{dc}\right]^T, \\
V_{ppnn}^{\alpha\beta\gamma} &= \left[\frac{1}{\sqrt{6}}V_{dc} \quad \frac{\sqrt{2}}{2}V_{dc} \quad \frac{2}{\sqrt{3}}V_{dc}\right]^T, \\
V_{npnp}^{\alpha\beta\gamma} &= \left[-\frac{1}{\sqrt{6}}V_{dc} \quad \frac{\sqrt{2}}{2}V_{dc} \quad -\frac{2}{\sqrt{3}}V_{dc}\right]^T, \\
V_{nppn}^{\alpha\beta\gamma} &= \left[-\frac{\sqrt{2}}{\sqrt{3}}V_{dc} \quad 0 \quad \frac{2}{\sqrt{3}}V_{dc}\right]^T, \\
V_{nnpp}^{\alpha\beta\gamma} &= \left[-\frac{1}{\sqrt{6}}V_{dc} \quad -\frac{\sqrt{2}}{2}V_{dc} \quad -\frac{2}{\sqrt{3}}V_{dc}\right]^T, \\
V_{pnpn}^{\alpha\beta\gamma} &= \left[\frac{1}{\sqrt{6}}V_{dc} \quad -\frac{\sqrt{2}}{2}V_{dc} \quad \frac{2}{\sqrt{3}}V_{dc}\right]^T.
\end{aligned} \tag{7.30}$$

A reference vector can be obtained using feedback control:

$$V_{ref} = \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix}. \tag{7.31}$$

When the reference is in sector I, the four vectors $V_{pnpn}^{\alpha\beta\gamma}$, $V_{pnnp}^{\alpha\beta\gamma}$, $V_{ppnn}^{\alpha\beta\gamma}$ and $V_{npnp}^{\alpha\beta\gamma}$ are used. Their duty cycles, d_{pnpn}, d_{pnnp}, d_{ppnn} and d_{npnp} can be calculated from

$$\begin{aligned}
&d_{pnpn} \cdot V_{pnpn}^{\alpha\beta\gamma} + d_{pnnp} \cdot V_{pnnp}^{\alpha\beta\gamma} + d_{ppnn} \cdot V_{ppnn}^{\alpha\beta\gamma} + d_{npnp} \cdot V_{npnp}^{\alpha\beta\gamma} = V_{ref} \\
&d_{pnpn} + d_{pnnp} + d_{ppnn} + d_{npnp} = 1
\end{aligned}. \tag{7.32}$$

Equation (7.32) is rewritten in matrix form:

$$\begin{bmatrix} \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{\sqrt{3}} & \frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ -\frac{\sqrt{2}}{2} & 0 & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{2}{\sqrt{3}} & -\frac{2}{\sqrt{3}} & \frac{2}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \\ 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} d_{pnpn} \\ d_{pnnp} \\ d_{ppnn} \\ d_{npnp} \end{bmatrix} = \begin{bmatrix} V_\alpha / V_{dc} \\ V_\beta / V_{dc} \\ V_\gamma / V_{dc} \\ 1 \end{bmatrix}, \tag{7.33}$$

then

$$\begin{bmatrix} d_{pnpn} \\ d_{pnnp} \\ d_{ppnn} \\ d_{npnp} \end{bmatrix} = \begin{bmatrix} -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{4\sqrt{3}} & \frac{1}{2} \\ \frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{2\sqrt{3}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{2\sqrt{3}} & 0 \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{4\sqrt{3}} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} V_\alpha / V_{dc} \\ V_\beta / V_{dc} \\ V_\gamma / V_{dc} \\ 1 \end{bmatrix}. \tag{7.34}$$

Similarly, the duty cycles in sector II-VI can be obtained.

As shown in Figure 7.20, the modulation scheme greatly reduces the common-mode dv/dt, compared with that in Figure 7.18. Furthermore, it will be demonstrated in the next section that even under unbalanced and nonlinear load, the dv/dt remains very small.

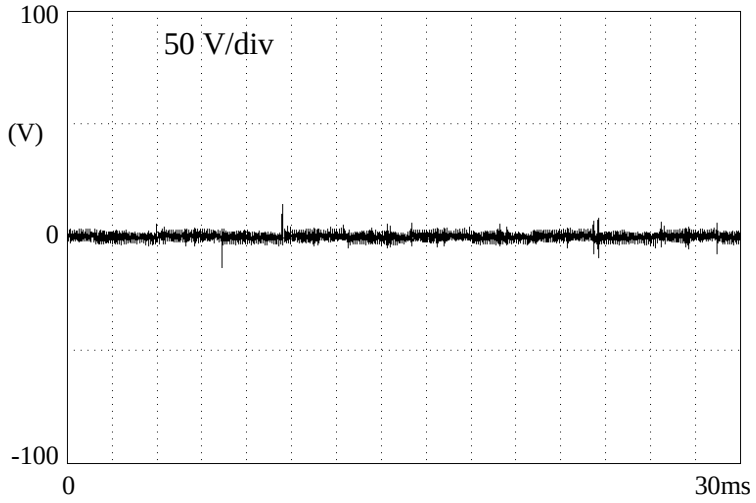
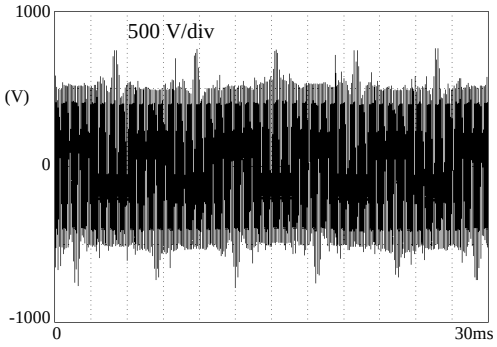


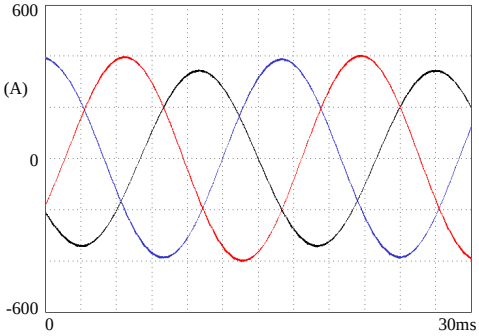
Figure 7.20 Common-mode voltage v_n of new inverter with proposed modulation.

7.2.3 Simulation Results

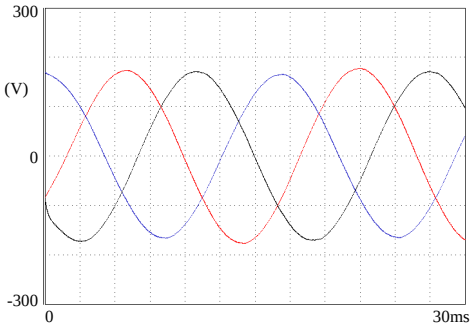
Based on the modified o-channel control design, the new inverter can not only reduce high-frequency common-mode dv/dt, but can also handle low-frequency common-mode components under unbalanced and nonlinear load conditions. Figures 7.21 and 7.23 show the simulated waveforms using the switching model of the conventional four-leg inverter shown in Figure 7.10 for the unbalanced and nonlinear load. Figures 7.22 and 7.24 show the simulated waveforms using the switching model of the new inverter shown in Figure 7.11 for the unbalanced and nonlinear load. The model parameters are in section 7.2.1.



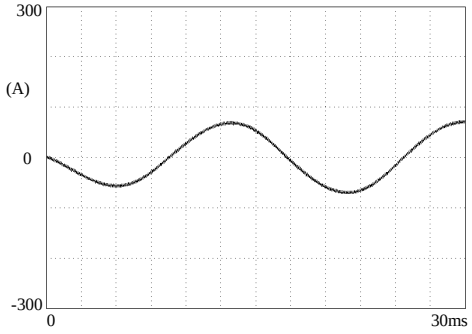
(a) v_n.



(b) i_a, i_b, i_c.

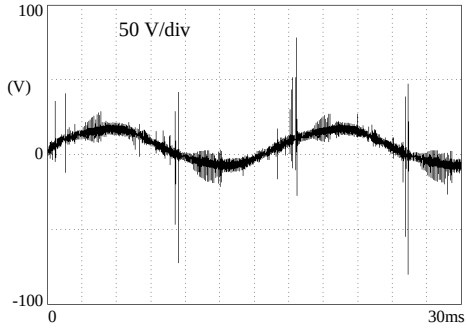


(c) v_{an}, v_{bn}, v_{cn}.

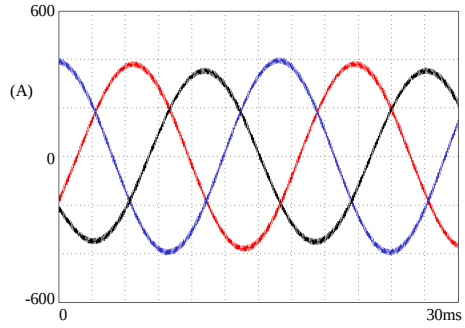


(d) i_N.

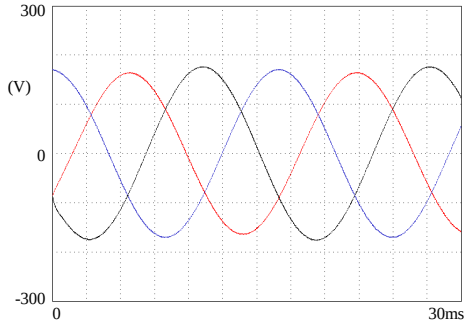
Figure 7.21 Simulated waveforms of inverter in Figure 7.10 under unbalanced load.



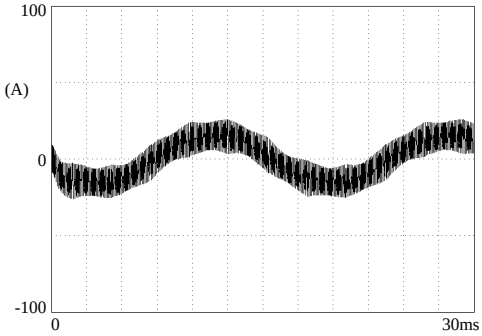
(a) v_n.



(b) i_a, i_b, i_c.

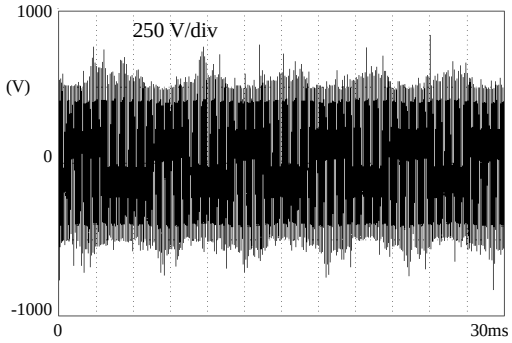


(c) v_{an}, v_{bn}, v_{cn}.

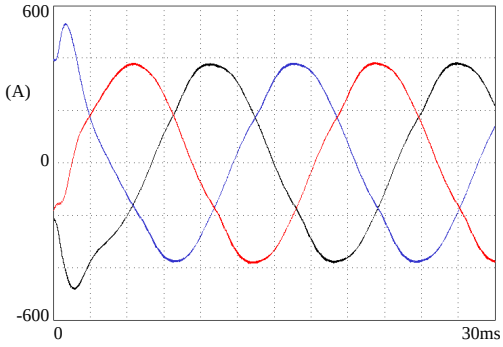


(d) i_N.

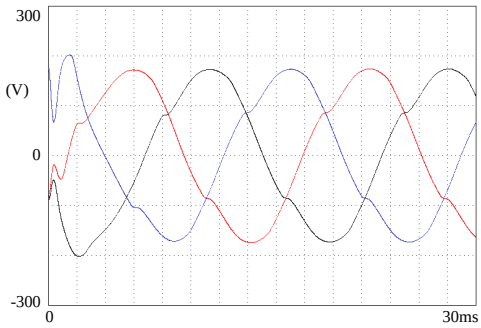
Figure 7.22 Simulated waveforms of new inverter in Figure 7.11 under unbalanced load.



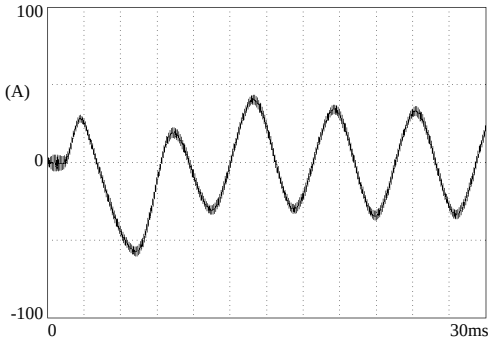
(a) v_n.



(b) i_a, i_b, i_c.

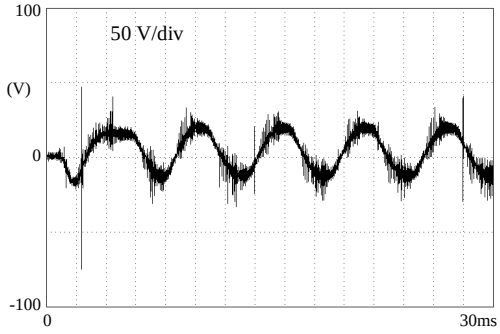


(c) v_{an}, v_{bn}, v_{cn}.

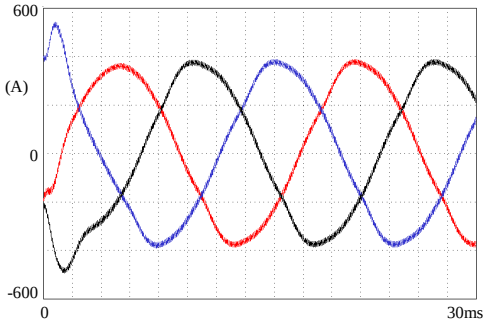


(d) i_N.

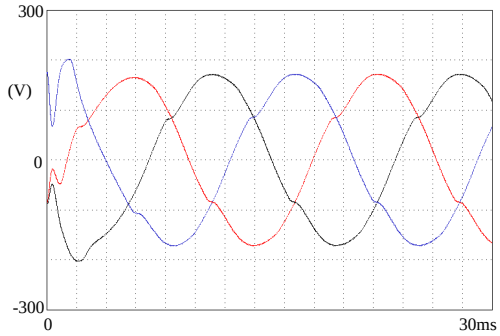
Figure 7.23 Simulated waveforms of inverter in Figure 7.10 under nonlinear load.



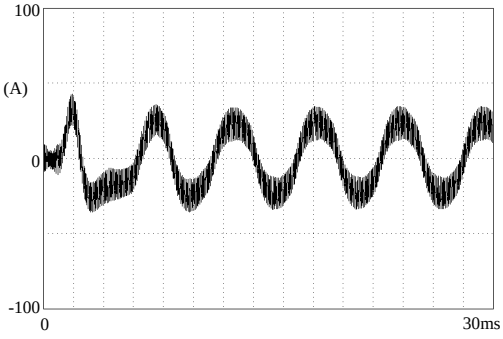
(a) v_n.



(b) i_a, i_b, i_c.



(c) v_{an}, v_{bn}, v_{cn}.



(d) i_N.

Figure 7.24 Simulated waveforms of new inverter in Figure 7.11 under nonlinear load.

It can be seen from Figures 7.22 and 7.24 that the new inverter has nearly eliminated common-mode dv/dt under any load condition. Meanwhile, the low-frequency common-mode current is still able to flow through the fourth leg so that a balanced three-phase output voltage can be achieved even under unbalanced and nonlinear load conditions. Figure 22(d) shows a fundamental line-frequency neutral current due to the unbalanced load, and Figure 24(d) shows a sixth-order harmonic neutral current due to the nonlinear load.

7.2.4 Performance Trade-Off Analysis

Because there are fewer available switching vectors in the new inverter, the differential-mode current ripple is two times higher than that of the inverter in Figure 7.10 modulated with adjacent vectors. This situation is illustrated in Figures 7.21(b), 7.22(b), 7.23(b) and 7.24(b), which show the inductor currents under different cases. In order to compensate for the higher differential-mode current ripple, the output filter inductor L and capacitor C have to be larger.

Another trade-off occurs with the maximum modulation index, defined as $M = V_{l-l,peak} / V_{dc}$, where $V_{l\text{-}l,peak}$ is the peak value of line-to-line output voltage. The modulation with adjacent vectors has M=1 [78], but the proposed modulation scheme has M=0.866, because there are only six available switching vectors. The derivation of the maximum modulation index is as follows.

Figure 7.25 shows one reference vector position.

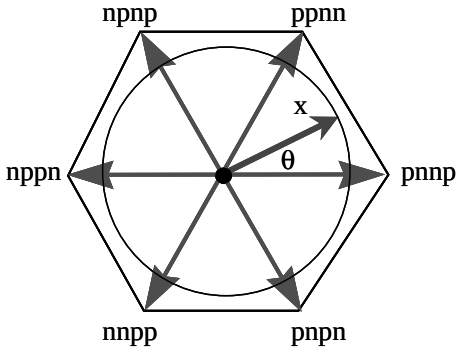


Figure 7.25 Projection of reference vector and six switching vectors on α-β plane.

Assuming the maximum attainable circle radius is x, and its projections on the α-β-γ axes are $x\cos\theta$, $x\sin\theta$, and 0 respectively, where $0 \le \theta \le 60°$, the duty cycles of the vectors pnpn, pnnp, ppnn and pnpn can be calculated by:

$$\begin{bmatrix} d_{pnpn} \\ d_{pnnp} \\ d_{ppnn} \\ d_{npnp} \end{bmatrix} = \begin{bmatrix} -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{4\sqrt{3}} & \frac{1}{2} \\ \frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{2\sqrt{3}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{2\sqrt{3}} & 0 \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{4\sqrt{3}} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} x\cos\theta \\ x\sin\theta \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} -\frac{1}{\sqrt{6}} x\cos\theta - \frac{\sqrt{2}}{2} x\sin\theta + \frac{1}{2} \\ \frac{\sqrt{2}}{\sqrt{3}} x\cos\theta \\ \frac{1}{\sqrt{6}} x\cos\theta + \frac{\sqrt{2}}{2} x\sin\theta \\ -\frac{\sqrt{2}}{\sqrt{3}} x\cos\theta + \frac{1}{2} \end{bmatrix}. \quad (7.35)$$

All duty cycles should be larger than zero at any angle. Therefore:

$$\begin{aligned} &-\frac{1}{\sqrt{6}} x\cos\theta - \frac{\sqrt{2}}{2} x\sin\theta + \frac{1}{2} \ge 0, \\ &\frac{\sqrt{2}}{\sqrt{3}} x\cos\theta \ge 0, \\ &\frac{1}{\sqrt{6}} x\cos\theta + \frac{\sqrt{2}}{2} x\sin\theta \ge 0, \\ &-\frac{\sqrt{2}}{\sqrt{3}} x\cos\theta + \frac{1}{2} \ge 0, \end{aligned} \quad (7.36)$$

where $0 \le \theta \le 60°$. The solution to (7.36) is:

$$x \le \frac{\sqrt{6}}{4}. \quad (7.37)$$

Since the length of the six vectors in the α-β plane is $2/\sqrt{6}$, the modulation index is

$$M_x = \frac{\sqrt{6}}{4} \cdot \frac{2}{\sqrt{6}} = 0.5. \quad (7.38)$$

Here, 0.5 refers to the line-to-neutral value. After being converted to line-to-line value, the maximum modulation index can be obtained as:

$$M = 0.5 \cdot \sqrt{3} = 0.866. \quad (7.39)$$

In conclusion, the three-phase, four-leg inverter can produce a balanced three-phase voltage with drastically reduced common-mode dv/dt under any load conditions (balanced, unbalanced or nonlinear) with the proposed three-dimensional SVM strategy

and the modified o-channel control design. The penalty is a somewhat increased differential-mode ripple and a 15% smaller maximum modulation index.