Characterization and Modeling of Silicon and Silicon Carbide Power Devices

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Abstract

Power devices play key roles in the power electronics applications. In order for the power electronics designers to fully utilize the performance advantages of power devices, compact power device models are needed in the circuit simulator (Saber, P-spice, etc.). Therefore, it is very important to get accurate device models. However, there are many challenges due to the development of new power devices with new internal structure and new semiconductor materials (SiC, GaN, etc.).

In this dissertation, enhanced power diode model is presented with an improvement in the reverse blocking region. In the current power diode model in the Saber circuit simulator, an empirical approach was used to describe the low-bias reverse blocking region by introducing an effect called “conduction loss,” a parameter that causes a linear relationship between the device voltage and current at low bias voltages with no physics meaning. Furthermore, this term is not sufficient to accurately describe the changes to the device characteristics as the junction temperature is varied. In the enhanced model, an analytical temperature dependent model for the reverse blocking characteristics has been developed for Schottky/JBS diodes by including the thermionic-emission mechanism in the low-bias range. The newly derived model equations have been implemented in Saber

circuit simulator using MAST language. An automated parameter extraction software package developed for constructing silicon (Si) and silicon carbide (SiC) power diode models, which is called DIode Model Parameter extrACtion Tools (DIMPACT). This software tool extracts the data necessary to establish a library of power diode component models and provides a method for quantitatively comparing between different types of devices and establishing performance metrics for device development.

This dissertation also presents a new Saber-compatible approach for modeling the inter-electrode capacitances of the Si CoolMOS^{TM} transistor. This new approach accurately describes all three inter-electrode capacitances (i.e., gate-drain, gate-source, and drain-source capacitances) for the full operating range of the device. The model is derived using the actual charge distribution within the device rather than assuming a lumped charge or one-dimensional charge distribution. The comparison between the simulated data with the measured results validates the accuracy of the new physical model.

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I would like to thank my husband, Nan, and son, Noah, for their understanding and support during the pursuit of my degree. I would also like to express my sincere appreciation for years of love and support to my parents, Liang Yang and Zhenhua Fang; my parents-in-law, Lixin Wu and Guoling Feng; to my grandparents, Jingtian Fang and Shilan Yu.

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Chapter 1 Introduction

Various types of power semiconductor devices are available today that provide advantages in different applications. They are the key enabling technology for power switching conversion applications. In order for power conversion system designers to accurately predict and fully utilize the performance advantages of power devices, compact models are needed in circuit and system simulators, and model parameter extraction tools are required to characterize power semiconductor devices. Hence, the development of compact models and model parameter extraction tools is especially important.

1.1 Compact Models for Power Devices

Take the Insulated Gate Bipolar Transistor (IGBT) as an example to evaluate the importance of the compact power device models for circuit and system simulation. The IGBT was invented in the 80s, which is fairly recent. However, with annual sale close to $ 1 billion, it starts to dominate the power device market used for medium power conversion applications from hundreds watts to megawatts. The medium power conversion applications market is approximately $40 billion annually and includes applications such as automotive ignitions systems, industrial motor drives, electronic lighting ballasts, and traction motor drives from electric vehicles to diesel-electric locomotives. The standard Physical model for IGBTs was developed at the National

Institute of Standards and Technology (NIST) [1], which brought an $18 million benefit to the market by reducing the cost of product designing and testing and a $40 million annual benefit in product improvements, due largely to energy reduction [2].

Based on the obvious advantages of the time, energy and monetary savings that simulation offers, it is apparent why the popularity of circuit simulators, compact device models, and parameter extraction tools has increased dramatically over the past two decades. The quick simulation time allows engineers to verify their concepts and leave the days of breadboarding multiple designs behind.

1.2 Power Semiconductor Devices

Power semiconductor devices are the semiconductor devices employed as switching parts in the power electronics circuit. From a historical perspective, power semiconductor devices have played an increasingly important rile in the development of power electronic systems over the last 50 years. The applications for power semiconductor devices are quite diverse as shown in Figure 1-1, where the power ratings of the system are shown as a function of system operating frequency. It can be seen that the power ratings range from a few hundred watts to a few hundred megawatts for various power applications [3]. An ideal switch should be capable of handling high power rating with low conduction losses, and also switching at a high speed with low power dissipation. However, so far, there is no power semiconductor device that is able to offer all the

advantages mentioned above. Depend on the application, trade off needs to be considered among switching speed, conduction loss and switching power dissipation.

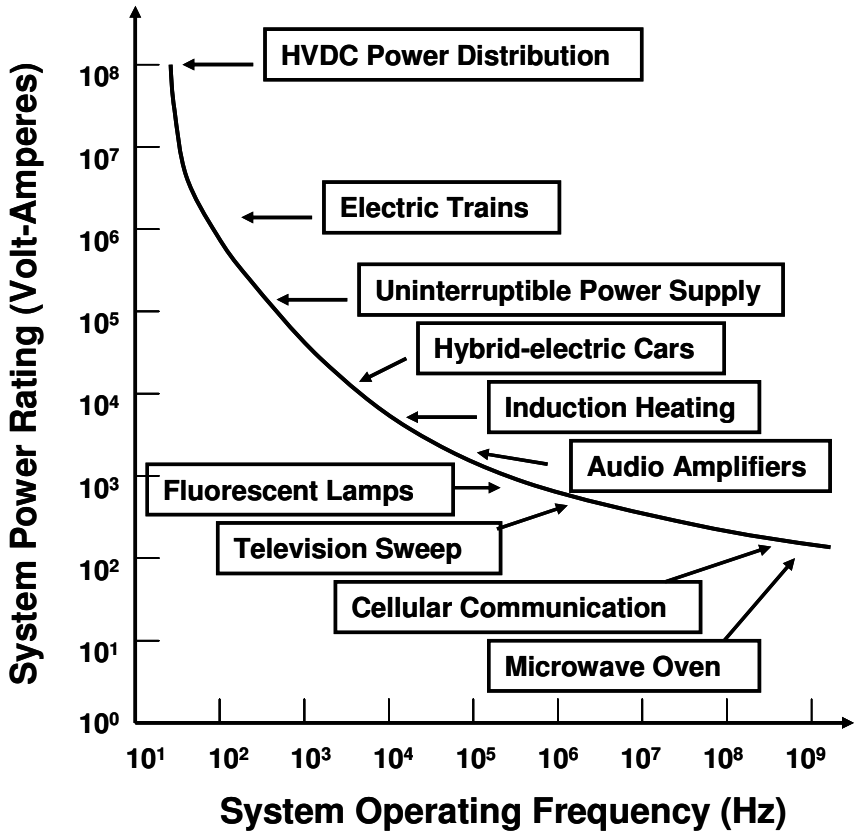


Figure 1-1 Applications for power semiconductor devices as a function of operating frequency and power rating

The power semiconductor devices can be categorized based on the device terminals as shown in Figure 1-2. The operation of two terminal devices or diodes depends on the external power circuit. They are used as freewheeling diodes in parallel with main active power switches (i.e power MOSFET or IGBT), power switches together with main active power switches and power rectifiers. It can be seen from Figure 1-2 that, there are three kinds of power diodes including PiN diodes, Schottky diodes, and MPS (or JBS) diodes.

The details of power diodes will be presented in Chapter 3. As shown in Figure 1-2, three-terminal devices consist of power MOSFETs, JFETs, IGBTs, BJTs, thyristors etc. Unlike two-terminal devices, the operation of three-terminal devices depends not only on their external power circuit, but also on their gate driving signals.

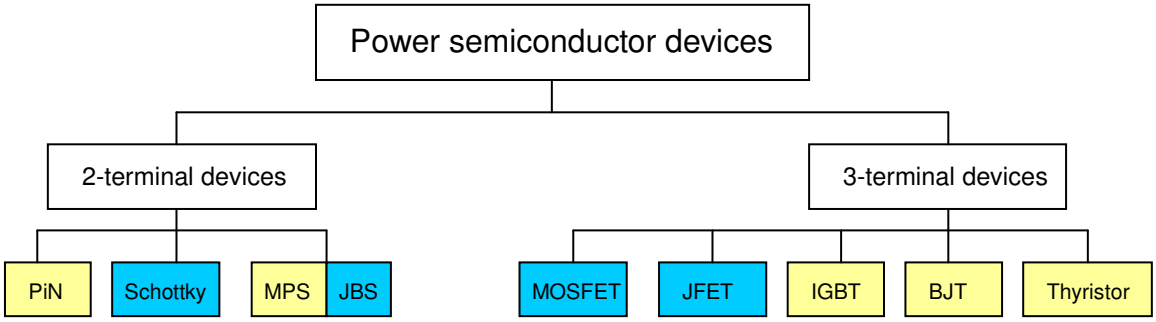


Figure 1-2 Family diagram of power semiconductor devices

A less obvious classification is also shown in Figure 1-2, which has a strong influence on device performance. The devices in yellow represent that they are minority carrier devices and the devices in blue represent that they are majority carrier devices. The former use both types of carriers (i.e electrons and holes) and the latter use only one type of carriers. The majority carrier devices offer high switching speed but suffer from high conduction losses. On the other hand, the minority carrier devices offer better on-state performance due to conduction modulation but suffer from low switching speed. Both minority carrier devices and majority carrier devices are selected based on their application in the circuit design.

1.3 Beyond Power Devices with Silicon (Si)

There is no doubt that silicon (Si) is the most commonly used semiconductor material in manufacturing power devices because of its high availability and low production cost. However, the deficiency starts to show as for the application under high frequency, high temperature and high voltage rating condition comparing to wide bandgap compound materials (i.e SiC and GaN). Some of the important physical properties are shown in Table 1-1. It can be seen from Table 1-1 that SiC offers a higher thermal conductivity, higher breakdown electric field, larger bandgap, and higher saturation velocity than Si. In addition, SiC is an extremely rugged and stable material, which is considered as a more ideal material for power electronics. Silicon carbide power devices are expected to open up new markets for power conversion in high-voltage (>10 kV), high-temperature (>150 ^{o}C), and high-frequency (20 kHz) applications where Si technology is fundamentally inadequate. To day, there are GaN power devices (less than 200 V) available in the market. Higher voltage level power devices (400 V ~ 800 V) are under research development.

Recently, SiC power devices have begun to emerge with performance that is superior to that of Si power devices. For a given blocking voltage, SiC minority carrier conduction modulated devices, such as a PiN diode, are expected to show an improvement in switching speed by a factor of 100 as compared to Si, while majority carrier SiC devices are expected to show a factor of 100 advantage in resistance compared to Si. Prototype

devices have already demonstrated improvements over Si technology for devices of various current and voltage ratings [4], and SiC Schottky diodes, JBS diodes, PiN diodes, power MOSFETs, and power JFETs are all currently under development by research and manufacturing organizations (such as Cree, Northrop Grumman, Semisouth, Infineon, and Rockwell Scientific). Currently, only Shottky diodes and JFETs have been the only power devices released into the commercial marketplace [5]-[7].

Table 1-1 Semiconductor Electrical Properties

Material	Bandgap (Eg) (eV)	Thermal Conductivity (W/cmoC)	Breakdown Electric Field (V/cm)	Saturated Electron Drift Velocity (cm/s)	Additional Information
Si	1.1	1.3	3.1e5	1.0e7	
3C-SiC	2.7	3.6	>1.5e6	2.5e7	Superior transport properties,but used less due to smaller bandgap and lack of substrate technology
4H-SiC	3.26	3.7	3.5e6	2.0e7	Ideal for power devices. Material well up the learning curve. Can use to develop simple commercial devices. Broad future markets and application. More isotropic than 6H-SiC.
6H-SiC	3.0	3.7	2.5e6	2.0e7	The 6H means a hexagonal type lattice with an arrangement of 6 different Si+C layers before the pattern repeats itself. This is the polytype of SiC initially used as substrates for growth of GaN blue LEDs.
GaN	3.2	1.3	3.0e6	2.5e7	Primarily used in optical devices (blue LEDs); power devices type focused on High Electron Mobility Transistors (HEMT), Ideal for RF switching devices (S-Band and up). Recently has be used for MOSFETs below 200 V, High material cost, high defect density.

These emerging power device technologies which utilize SiC material promise to extend high frequency power conversion into the 10 kV to 25 kV range with applications in power distribution, energy storage devices, and ship propulsion systems. Presently, there are significant efforts underway to develop high voltage semiconductor devices needed for commercial and military high-voltage, high-frequency power conversion applications. The Electric Power Research Institute (EPRI) has reported (1001698,1002159) that a solid-state distribution transformer referred to as the Intelligent Universal Transformer (IUT) is a viable replacement for conventional distribution transformers, and would add significant new functional capabilities to those available from conventional copper and ion transformers [8]. Yet another EPRI report (1009516) identified SiC devices as a potential solution for high voltage semiconductor devices needed for the IUT. Furthermore, the goal of an ongoing Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor Technology High Power Electronics (WBST-HPE) program is to support the research and development necessary to realize the SiC switches and diodes necessary to demonstrate the viability of the Solid State Power Substations (SSPS) for future Navy warships [9].

Other U.S. military interests in SiC power electronics are for their hybrid-electronic combat vehicles. Hybrid-electric vehicles must utilize high-power converters and motor drivers that are capable of operating within harsh environments. A second major area of interest to the military is in pulsed power applications (such as electromagnetic rail guns).

Pulsed power applications require very high power coupled with extremely fast device responses [10], [11].

Energy companies are interested in SiC power electronics as well. Deep earth drilling encounters hostile environments and extreme temperatures in which it is nearly impossible to use silicon electronics. With SiC, it will be possible to send electronics "down-hole", thereby improving motor drive control and efficiency; increasing exploration and sensing capabilities; and possibly aiding in the discovery of previously hidden energy sources.

Further energy applications include power factor correction circuits, where the reduced switching energy of the SiC diodes yields less stress on the MOSFETs used in the circuit. Decreasing the stress inflicted on the MOSFETs allows for utilizing de-rated switches, and thus the ability to increase switching frequency and ultimately decrease EMI filter and passive component size [12]-[18]. In addition, uninterruptible power supplies, switched mode power supplies, motor control inverters, and welding equipment can benefit from significant savings in switching energy by replacing freewheeling Si diodes with SiC Schottky diodes to pair with Si IGBTs. The turn-on switching losses of the IGBTs are strongly influenced by the reverse recovery characteristics of the freewheeling diode, hence SiC Schottky diodes can cut the IGBT switching losses by up to 50%, while the diode switching losses are cut by 80% [13].

Gallium Nitride (GaN), as another candidate which is possible to use under high frequency and high temperature environments, is primarily used in optical devices (i. e

blue LEDs). As for the usage in power electronics area, GaN is the ideal semiconductor material for low power RF switching devices such as High Electron Mobility Transistors (HEMT). Due to the high material cost and high defect density (around $10^{13}/cm^3$) [14], GaN can not be used to manufacture high power rating devices (i.e IGBTs and MOSFETs).

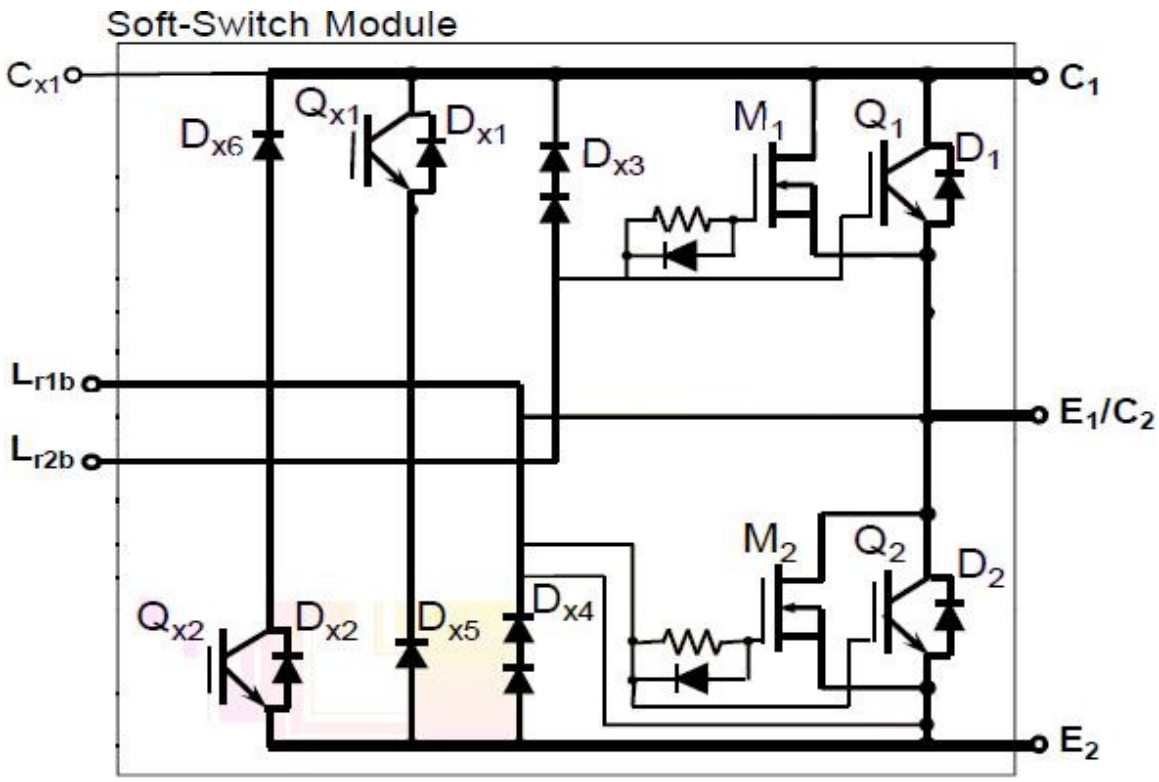
As the production cost becomes less expensive and the yielding becomes higher, SiC will have more and more markets in power electronics field especially motors and motor drives.

1.4 Power Devices in the Electrical Vehicle Project

From the global environmental point of view, green energy and low CO_2 exhaustion machines have become more and more important tasks for engineers. Today, most of the air pollution is the vehicle exhaustion from the usage of the gasoline. Fortunately, this problem has been recognized and researches are being conducted to develop high efficiency and environmental friendly vehicles among which the electrical vehicle is very promising.

For the merging hybrid electrical vehicles and electric vehicles industry, there are many key technologies [19]-[21] involved in the field of power electronics; especially the selection of power semiconductor devices. The behavior of power semiconductor devices will affect the performance of the circuit or even the whole system. In order to optimize the circuit or system performance and achieve high efficiency, the selection of power

devices is very critical. Based on the above discussion, candidate's power devices have to be characterized carefully and modeled accurately. Figure 1-3 shows the circuit schematic of the soft-switch module.



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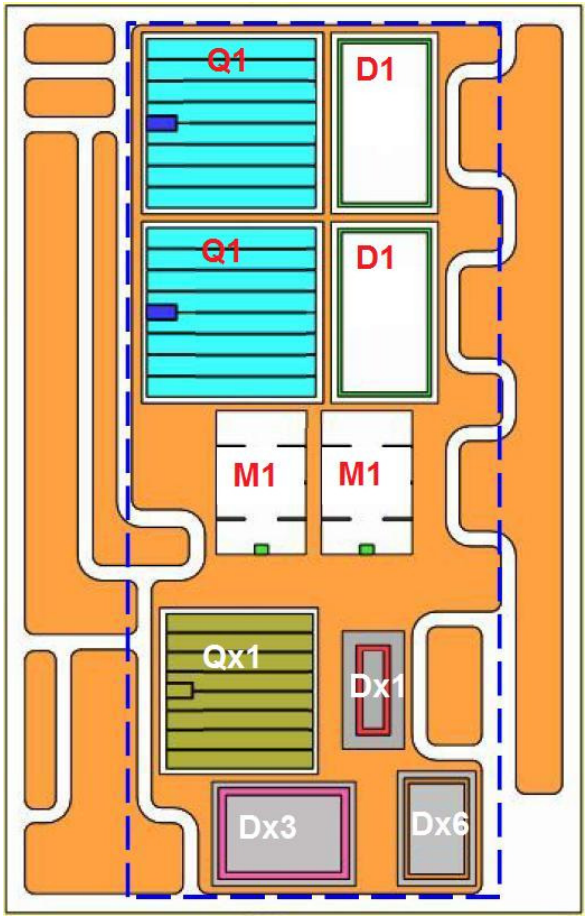


(b)

Figure 1-3 Circuit schematic of soft-switch module (a); Device layout with labels (b)

As illustrated in Figure 1-3, in the above module, power devices include 600 V Si IGBTs, 650 V Si CoolMOS^{TM}, 600 V Si PiN diodes, 600 V SiC Schottky diode, etc.. In this dissertation, the device models for power diodes (in chapter 3), and Si CoolMOS^{TM} (in chapter 6) will be presented.

Chapter 2 Power Semiconductor Materials

In order to model the characteristics of the power semiconductor devices, it is especially important to understand the physics background of the semiconductor materials. For power electronics application, it has been known that silicon (Si) is the most commonly used semiconductor material. As a relatively new material, silicon carbide (SiC) has been recognized to have superior properties when compared to Si as seen from Table 1-1. In this chapter, it will be presented the material properties of Si and SiC are related to the binding energy of the covalent bonds in the semiconductor.

2.1 Crystal Structure

The crystal structure of semiconductor materials consists of a repeatable atomic structure with the smallest cell as unit cell. A unit cell is a small portion of any given crystal that could be used to reproduce the crystal. The crystal structure of Si is called diamond, which means each Si atom has four nearest neighbors as shown in Figure 2-1 (a). In the case of compound semiconductor material such as SiC, the same cubic structure is referred to as zincblende as shown in Figure 2-1 (b) in which the black atoms designate Si ad the white atoms designate C. The two structures have identical physical arrangements in space, but differ in that the diamond structure consists of only a single atomic species, while the zincblende structure consists of two atomic (or molecular) species. For SiC, depend on the "stacking" sequence of the atoms, there has been found

in over 200 polytypes. The most well known polytypes of SiC are 3C-SiC, 4H-SiC and 6H-SiC, where H stands for a hexagonal crystal structure and C means cubic [15], [16].

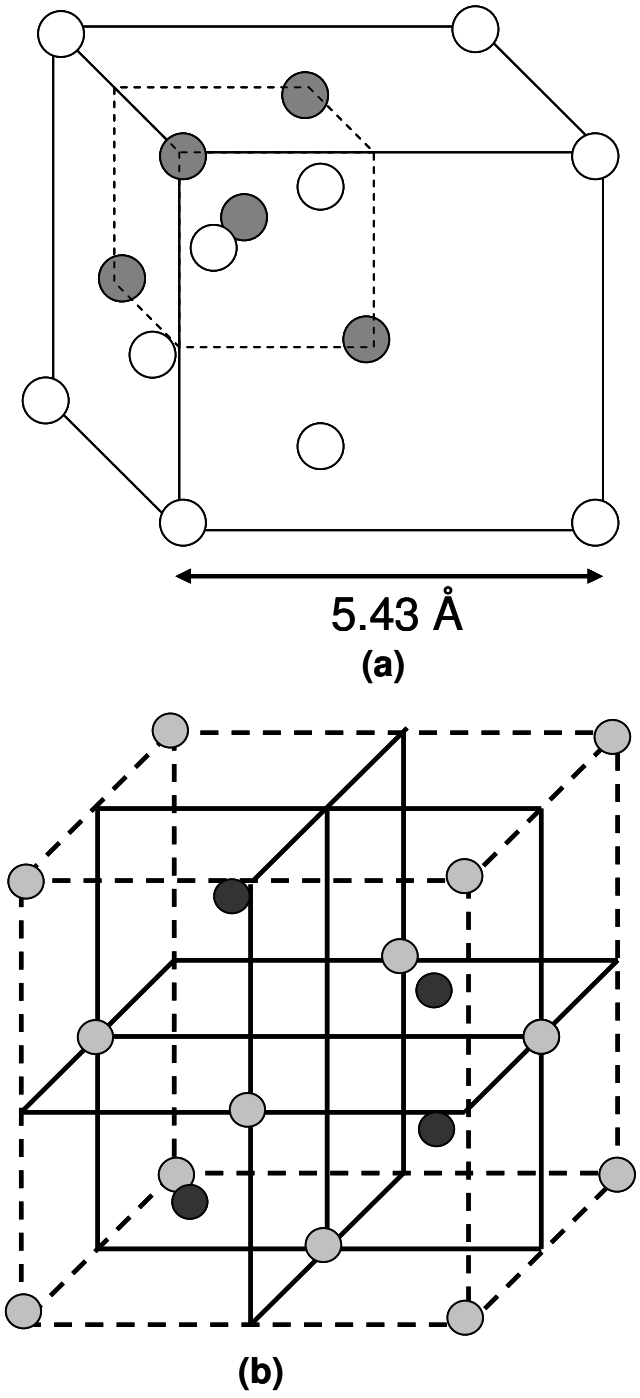


Figure 2-1 Diamond structure for Si (a); Zincblende structure for SiC, Si atoms are black and carbon atoms are white (b)

The semiconductor mechanical properties are listed in Table 2-1, from which it can be seen that SiC has a slightly larger density as compare to Si. Because both Si and C are relatively small atoms, the density of Si and SiC is small. The number of Si atoms per cm^3 is the same in SiC as in Si, but SiC also has C atoms intertwined in the lattice [15]. The shorter bond of the atomic packing in SiC results in a larger bond strength, bankgap, and hardness.

Table 2-1 Semiconductor mechanical properties

Property	Si	3C-SiC	4H-SiC	6H-SiC	GaN
Eg (eV)	1.12	2.4	3.2	3	3.4
Lattice a (Å)	5.43	4.36	3.08	3.08	3.189
Lattice c (Å)	NA	NA	10.08	15.12	5.185
Bond Length (Å)	2.35	1.89	1.89	1.89	1.95
TCE (10^{-6}/K)	2.6	3	4.5	4.5	5.6
Density (g/cm^3)	2.3	3.2	3.2	3.2	6.1
Thermal Conductivity (W/cmK)	1.5	5	5	5	1.3
Melting point (^oC)	1420	2830	2830	2830	2500

2.2 Electrical Properties

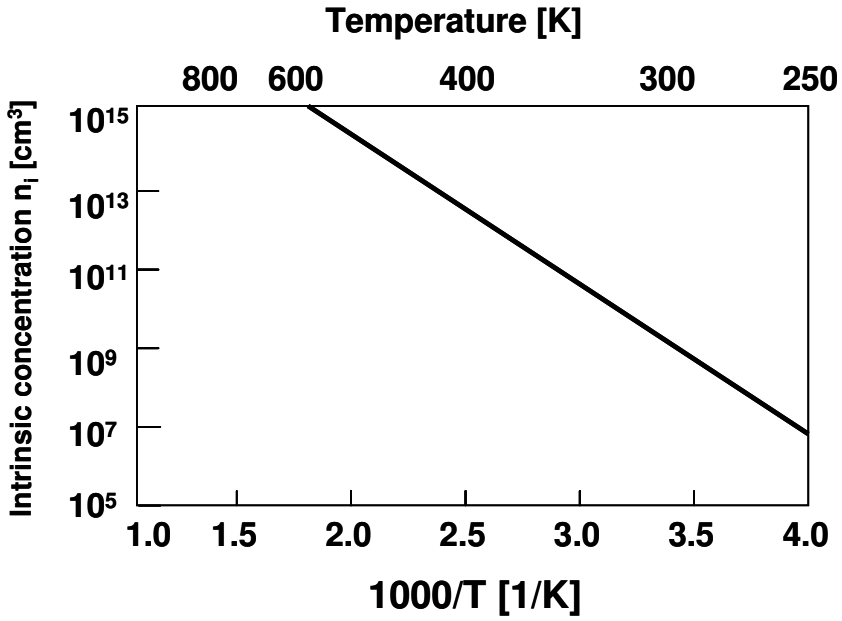
Some of the important electrical properties are listed in [17].

Table 2-2 Semiconductor electrical properties

Property	Si	3C-SiC	4H-SiC	6H-SiC	GaN
Eg (eV)	1.12	2.4	3.2	3	3.4
Ec (MV/cm)	0.25	2	2.2	2.5	3
Vsat (10^7cm^2/s)	1	2.5	2.0	2.0	2.5
μ_n, -c (cm2/Vs)	1350	1000	950	500	400
μ_n, ‖c (cm2/Vs)	-	-	1150	100	-
μ_n (cm2/Vs)	480	40	120	80	30
ε_r	11.9	9.7	10	10	9.5
n_i (/cm^3) @ 300K	10^{10}	0.093	2.7e-8	3e-6	2.8e-10
Direct/Indirect Bandgap	I	I	I	I	D

As seen from Table 2-2, the bandgaps of 4H-SiC and GaN are approximately three times higher than the one of Si resulting in a low intrinsic carrier concentration (n_i) as shown in equation (2-1). The wide bandgap also results in an increase in the amount of energy needed by an electron in the valence band in order to make the transition to the conduction band. If the energy is large enough, an electron can jump to the conduction band, creating an electron-hole pair. However, as the temperature increases, the increase of the intrinsic carrier concentration of SiC is much lower than Si due to the wide bandgap as shown in Figure 2-2. It is for this reason that SiC devices are a better match for high-temperature applications.

$$n_i = (N_c * N_v)\exp(-E_g / 2k_B T) \tag{2-1}$$



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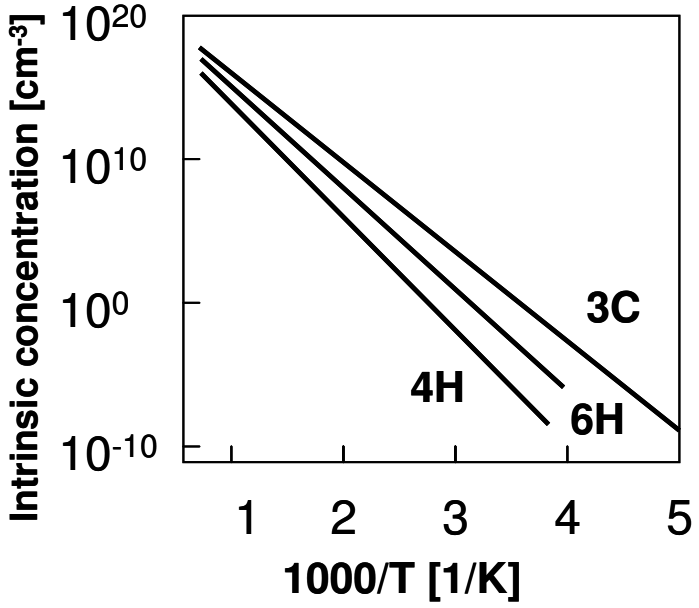


(b)

Figure 2-2 Intrisic carrier concentration (ni) versus temperature for Si (a); Intrisic carrier concentration (ni) versus temperature for SiC (b)

Another consequence of the wide bandgap is an increase in the critical electric field, which is very important in the high power system applications. The breakdown electric field of 4H-SiC is an order of magnitude higher than the one of Si as seen from Table 2-2, which means SiC power devices has a higher capability for voltage blocking application. Figure 2-3 shows the breakdown voltage for an ideal infinite parallel plane junction at different doping levels for the ideal case of Si [18] given by

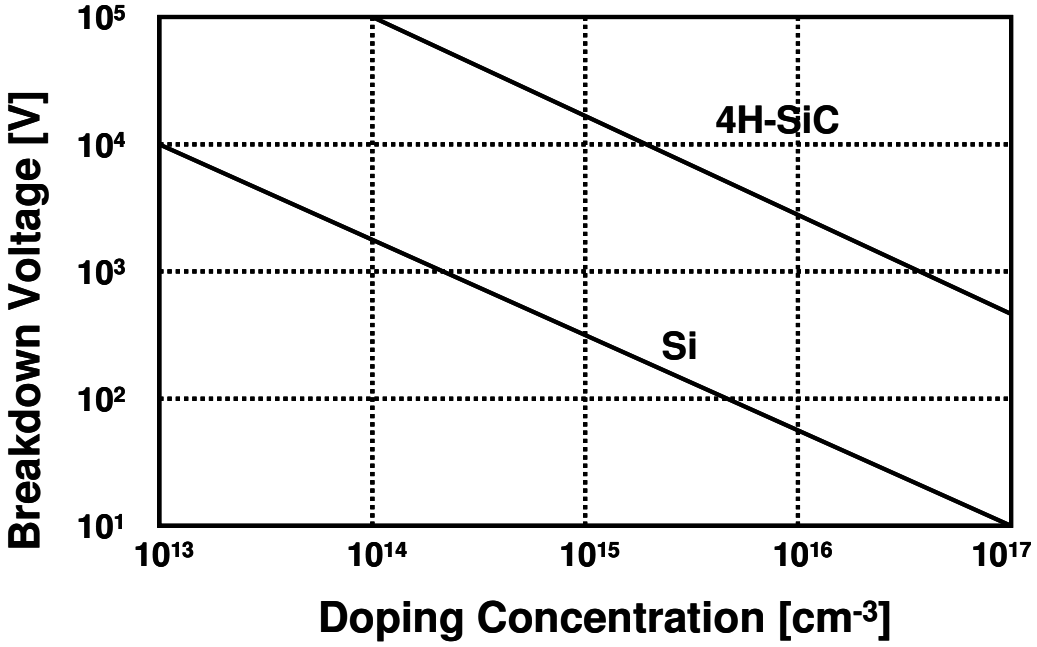


Figure 2-3 Ideal parallel plane breakdown voltage comparison for Si and SiC devices at different doping levels

$$V_B = 5.34 \times 10^{13} N_B^{-3/4} \qquad V \tag{2-2}$$

and for SiC [22] given by

$$V_B = 3.0 \times 10^{15} N_B^{-3/4} \qquad V \tag{2-3}$$

where N_B is the doping concentration in the voltage blocking Epi layer. From Figure 2-3, it can be seen that for the same doping density, SiC device has over an order of

magnitude voltage blocking capability than Si device. It is also obvious from this figure that for a given breakdown voltage, it is possible to use a much higher doping concentration in the drift region for 4H-SiC devices when compared with Si devices.

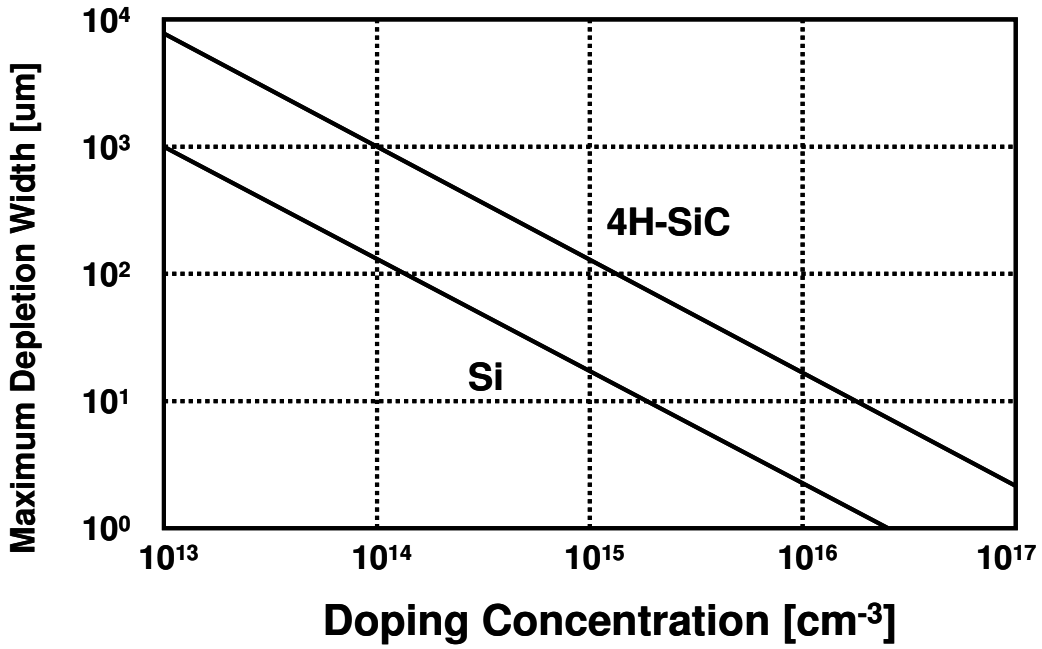


Figure 2-4 Maximum depletion width at breakdown in Si and 4H-SiC

Still using the power law equation, analytical solution for the maximum depletion layer width can be derived as for Si [18] given by

$$W_{c,pp} = 2.67 \times 10^{10} N_B^{-7/8} \tag{2-4}$$

and for SiC [22] given by

$$W_{c,pp} = 1.82 \times 10^{11} N_B^{-7/8} \tag{2-5}$$

Figure 2-4 shows the maximum depletion width reached at the breakdown voltage for Si and SiC. From this figure, it can be seen that for the same doping concentration, the maximum depletion width in 4H-SiC is 6.8 times larger than that in Si because it can stand for a much larger electric field. However, for a given breakdown voltage, the

depletion width in 4H-SiC is smaller than for a Si device because of the much larger doping concentration in the drift region. This smaller depletion width, in conjunction with the far larger doping concentration, results in an enormous reduction in the drift region on-resistance in 4H-SiC when compared with Si.

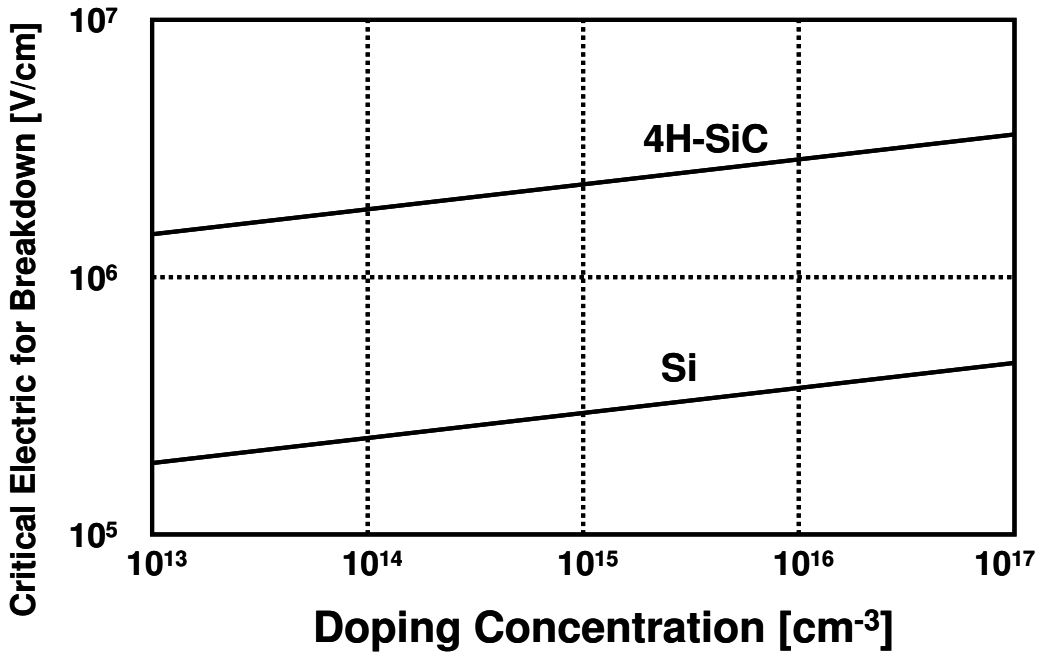


Figure 2-5 Critical electric field for breakdown in Si and 4H-SiC

The critical electric field for 4H-SiC can be compared with that for Si using Figure 2-5. From this figure, it can be seen that for the same doping concentration, the critical electric field in 4H-SiC is 8.2 times larger than in Si. The analytical solution for the critical electric field can be derived as for Si [18] given by

$$E_{c,pp} = 4010 N_B^{1/8} \tag{2-6}$$

and for SiC [22] given by

$$E_{c,pp} = 3.3\times 10^4 N_B^{1/8} \tag{2-7}$$

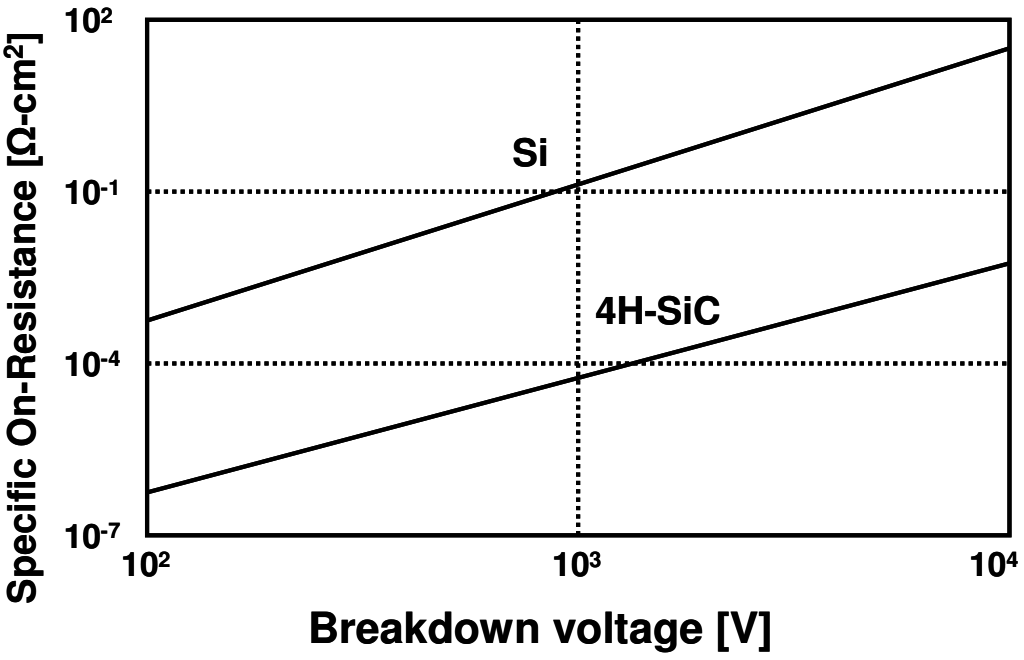


Figure 2-6 Specific drift region on-resistance in Si and 4H-SiC

The specific drift region on-resistance is compared between 4H-SiC and Si devices in Figure 2-6. For the same breakdown voltage, the resistance value of 4H-SiC is about 2000 times smaller than the one for Si devices. The specific on-resistance of the drift region is related to the breakdown voltage by equation (2-8).

$$R_{on,sp} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3} \tag{2-8}$$

From the above comparison between Si and 4H-SiC, it is obvious to see that 4H-SiC has better material properties than Si for the applications in high frequency and high voltage rating. However, Si exceeds the performance at low voltage and it is the material used for the majority of semiconductor devices for many reasons. One of the most important reasons is the ease of manufacture from raw material as compared with SiC.

2.3 Material Growth

In this section, it will be presented that Si is much easier to be manufactured than SiC resulting in low cost and high yielding. The most commonly employed method yielding large single crystals of Si is know as the Czochralski method. The Czochralski process is shown in Figure 2-7. In this process, the ultrapure polycrystalline silicon is placed in a quartz crucible and heated in an inert atmosphere to form a melt. Next, a small single crystal, or Si "seed" crystal, with the normal to its bottom face carefully aligned along a predetermined direction (i.e <111> or <100>), is then clamped to a metal rod and dipped into the melt. Once thermal equilibrium is established, the temperature of the melt in the vicinity of the seed crystal is reduced, and silicon from the melt begins to freeze out onto the seed crystal in the same crystal direction. The seed crystal is rotated and pulled out slowly from the melt and finally forms into a silicon ingot with 200 mm in diameter and 1 to 2 meters in length. The big ingot is cut into thin wafers by using a diamond-edged saw. From the above description, it can be seen that the manufacture process is simple, costless and productive which meets all the requirements for industrial manufacture.

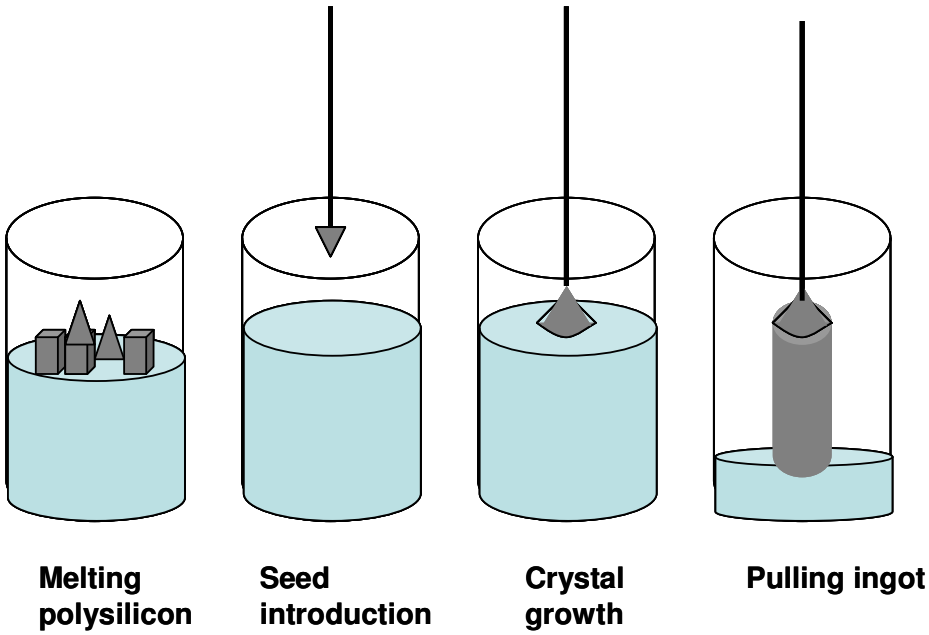


Figure 2-7 Czochralski process of growing Si ingot

On the other hand, the growth of SiC is more complicated. The epilayer growth is achieved by using Chemical Vapor Deposition (CVD) technology as shown in Figure 2-8. With the growing temperature at 1700 ^{o}C, the growth rate can reach 25 um/h [23].With this rate, in order to grow a 1 mm thick 4H-SiC, it will take 40 hours. Plus in order to reduce the micropipe defects, expensive source gases such as SiH_4 and C_3H_8 have to be employed, which add up the production cost of 4H-SiC.

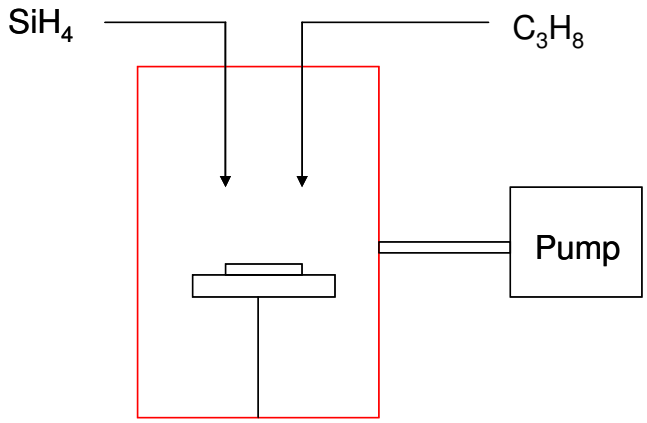


Figure 2-8 Growth of 4H-SiC with hotwall CVD

The market price for regular 8" Si wafers is about $30 for 400 pieces. For 4H-SiC wafer, it costs over $300 on a 10mm x 10mm wafer. The expensive cost limits the application pace of SiC especially in industrial commercialization. However, as SiC becomes less expensive and more readily available, the entire commercial industry of motors and motor drives will open up.

Chapter 3 Power Diodes

As a two-terminal switching device, power diode is considered to have a simple device structure compared with MOSFET and IGBT. Generally speaking, there are three classes of power diodes: (i) Schottky diodes, which offer extremely high switching speed but suffer from high leakage current and high drift region resistance; (ii) PiN diodes, which offer low leakage current but suffer from low switching speed; and (iii) Junction Barrier Schottky (JBS) / Merged PiN Schottky (MPS) diodes, which offer Schottky-like on-state while working in the JBS mode and PiN-like on-state while working in the MPS mode and fast switching characteristics, and PiN-like off-state characteristics [3].

3.1 Power Schottky Diode

Power Schottky diode is also interpreted as Metal-Semiconductor (MS) diode as seen from Figure 3-1. An ideal MS contact has the following properties: (1) The metal and semiconductor are assumed to be in intimate contact on an atomic scale. (2) No inter-diffusion or intermixing between metal and semiconductor. (3) No impurities or extra surface charges at the MS interface [24]. In this sub-section, detailed description will be presented for both static and transient characteristics including the forward conduction characteristic, the reverse blocking characteristic, the capacitance voltage characteristic, and the reverse recovery characteristic.

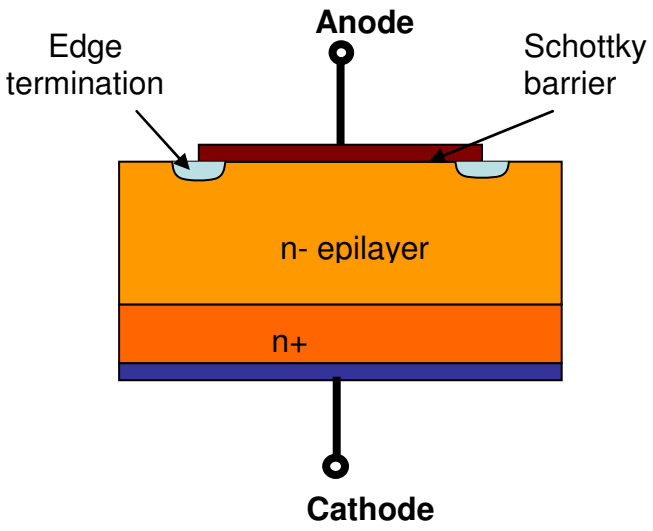


Figure 3-1 Structure of power Schottky diode

3.1.1 Forward Conduction

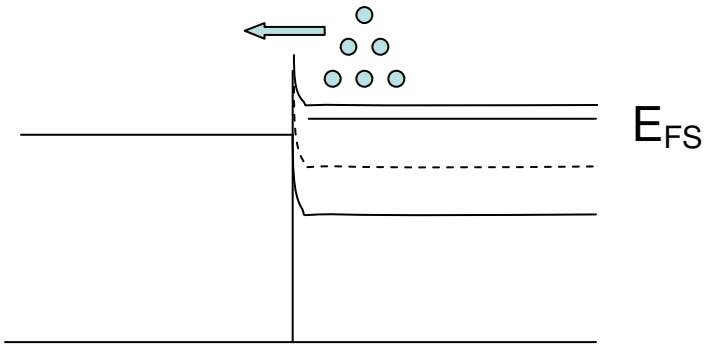


Figure 3-2 Band diagram for MS contact under forward bias condition

Under forward conduction, a positive bias is applied to the metal with respect to the N-type semiconductor as shown in Figure 3-2. Electrons transport from the semiconductor over the potential barrier into the metal which makes the current flow from metal to semiconductor, which is called as thermionic emission current described in equation (3-1).

$$I = AA^{*}T^{2}e^{-(q\phi_b/kT)}e^{(qV/kT)} \tag{3-1}$$

Where A is the area of the device active region, A* is the Richardson constant and ϕ_B is the barrier height. The published value of Richardson constant is 120 A/cm^2/K^2 for Si [24] and 146 A/cm^2/K^2 for SiC [25]. As a majority carrier device, Schottky diode does not have conductivity modulation in its drift region due to the lack of minority carrier injection. Consequently, the on-state resistance is relatively high although the thickness of the drift region is thin.

3.1.2 Reverse Blocking

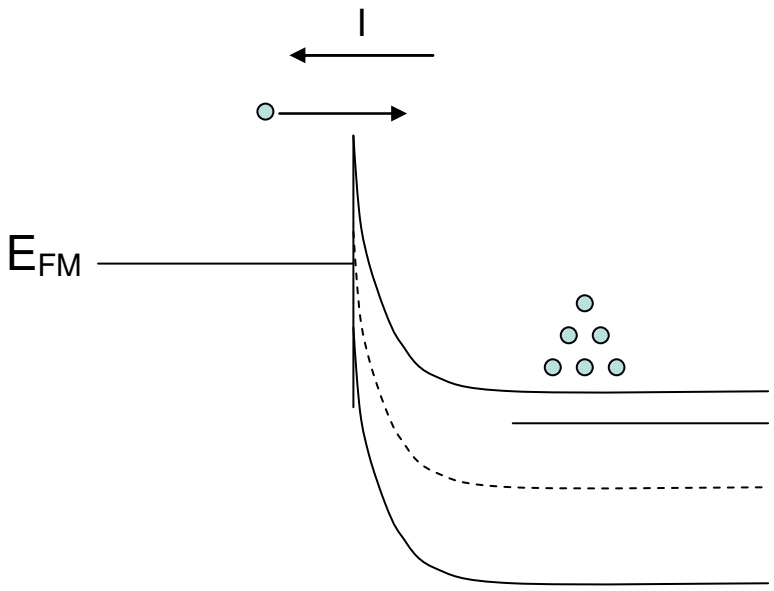


Figure 3-3 Band diagram for MS contact under reverse bias condition

Under reverse bias, the voltage is supported across the depletion epi-layer which extends into the semiconductor as illustrated in Figure 3-3. Leakage current is the main concern under reverse bias in real application. For Schottky/JBS diodes, there are several types of leakage current including injection of carrier across the barrier height (thermionic emission current), depletion region R-G current, surface leakage and defect induced leakage current, among which the first type of leakage current dominates.

For an ideal Schottky diode, the barrier height does not change as the bias increases, which means reverse leakage current will saturate as the dotted line in Figure 3-4. However, in reality as the bias increases, the barrier height will become lower which is called Schottky Barrier Lowering or Image Force Lowering. The direct effect caused by this barrier lowering is the increase of the reverse leakage current. The process can be explained by equation (3-2) where ϕ_B is the effective barrier height, ϕ_{B0} is the barrier height under zero-bias and $\Delta\phi_B$ is the change of barrier height. $\Delta\phi_B$ is a function with the bias voltage as illustrated in equation (3-3).

$$I_R = -AA^*T^2 e^{-(q\phi_B/kT)} = -AA^*T^2 e^{-(q(\phi_{B0}-\Delta\phi_B)/kT)} \tag{3-2}$$

$$\Delta\phi_B = \left(\frac{q \cdot E_m}{4\pi \cdot \varepsilon_r \varepsilon_0}\right)^{1/2} \tag{3-3}$$

where $E_m = \left[\frac{2qN_B}{\varepsilon_r \varepsilon_0}\left(V_R + V_{bi} - \frac{kT}{q}\right)\right]^{1/2}$

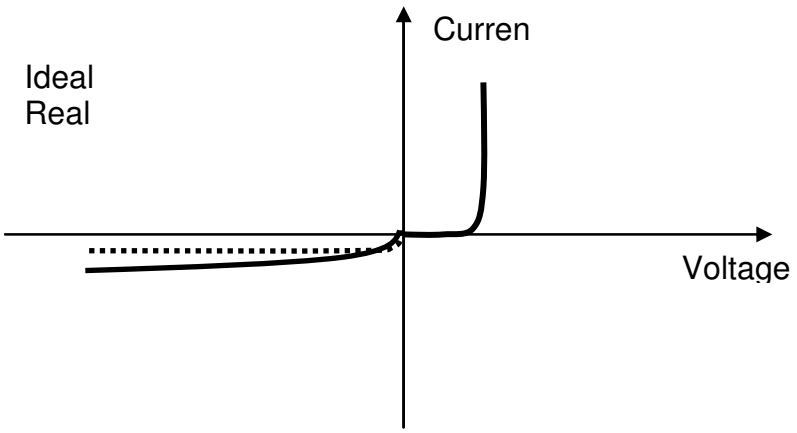


Figure 3-4 IV characteristics of Schottky diode

3.1.3 Transient Behavior

Because Schottky diodes are majority carrier devices, these devices exhibit extremely fast reverse recovery speed. However, the fast turn-off with high di/dt and dv/dt will cause severe ringings in the current and voltage waveforms due to the parasitic inductance and capacitance.

3.2 Power PiN Diode

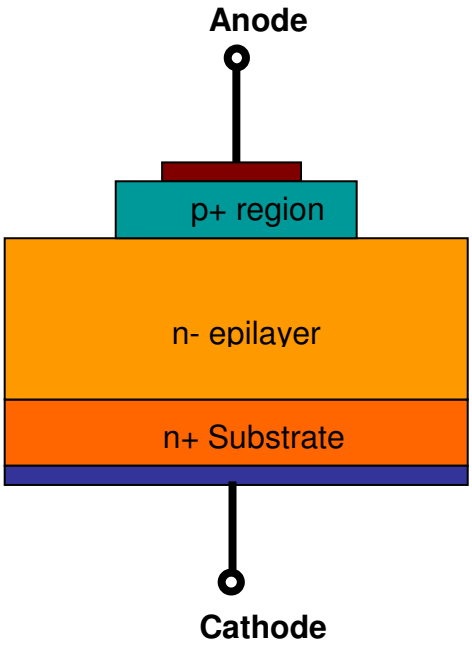


Figure 3-5 Structure of power PiN diode

The power PiN diode was one of the earliest power devices developed for power circuit application. Differ from a p-n junction diode; there is an intrinsic layer (usually lightly doped N-type semiconductor) in between, which offers the capability of high voltage blocking. As a minority carrier device, under forward conduction, holes will be injected into the n- epilayer as illustrated in Figure 3-5 which is called conduction

modulation. Due to this, the resistance of the i-region becomes very small allowing these devices to carry a high current density during the forward conduction. However, there are two major drawbacks of PiN diodes that need to be stated out. First, when device is turned on with a high di/dt, there is a voltage overshoot which is called forward recovery. This overshoot comes from the initial high resistance in i-region before the conduction modulation. The second drawback is its poor reverse recovery characteristics during turn-off caused by the minority carriers that injected into the i-region. Two major mechanisms employed to get rid of the minority carriers in the i-region are electric field sweep-out and recombination.

3.2.1 Forward Conduction

The physics of the forward conduction of PiN diode is more complicated than the one used for Schottky diode. The nature of the current-voltage (IV) characteristic depends strongly upon the current level as shown in Figure 3-6, which are Recombination current, Low-Level Injection current, High level Injection current, Emitter recombination current and Series resistance region [24]. At very low current levels, the current flow in the PiN diode is mostly generation and recombination in the depletion region about the P-I junction due to the presence of recombination centers. Assuming an applied bias of V_a, the minority carrier concentration n_p on the P-side of the junction is

$$n_p = \frac{n_i^2}{N_A} e^{\frac{qV_a}{kT}} \tag{3-4}$$

where N_A is the acceptor dopant density, where q is the electronic charge, n_i is the intrinsic carreier concentration, k is Boltzmann's constant, and T is temperature. Consequently, the pn product on the P-side is given by

$$pn = n_i^2 e^{\frac{qV_a}{kT}} \tag{3-5}$$

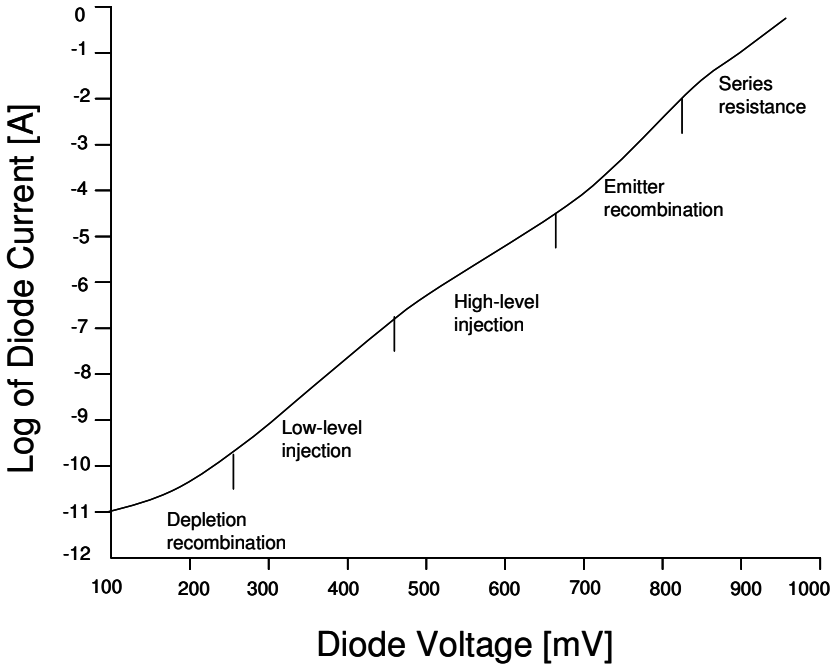


Figure 3-6 Forward conduction characteristics of PiN diode

Using Schockley-Read-Hall recombination theory, the recombination rate U is given by [24]

$$U = \frac{np - n_i^2}{\tau_{SC}(n + p + 2n_i)} \tag{3-6}$$

where τ_{SC} is the lifetime in the space charge or depletion region. Using equations (3-5) and (3-6), and assuming that $p = n$, the forward current density due to recombination in the depletion region is

$$J_{DR} = \frac{qn_i W_D}{2\tau_{SC}}\left(e^{\frac{qV_a}{2kT}} - 1\right) \tag{3-7}$$

where W_D is the depletion layer width. In equation (3-7) the quantity $qn_i W_D \big/ 2\tau_{SC}$ is defined as the saturation current density, and when multiplied by the device area becomes the saturation current. Also, an ideality factor is usually defined, which in this case is the 2 in the denominator of the exponential. It will be shown that all five modes of forward operation will have a similar form to equation (3-7).

As the current density increases, the diode enters low-level injection. The low-level injection condition in the base is given by $p << n$. Assuming that the width of the N region is much larger than the minority carrier diffusion length, the expression of the low-level injection current can be found by first considering the law of the junction to determine the hole concentration at the edge of the depletion region on the N-side $p_N(0)$ [24]

$$p_N(0) = p_{0N} e^{\frac{qV_j}{kT}} \tag{3-8}$$

where p_{0N} is the equilibrium hole concentration on the N-side. The minority carrier holes diffuse away from the junction (x=0) by a diffusion length L_p before recombining and

$$p_N = p_N(0) e^{\frac{-x}{L_p}} \tag{3-9}$$

Assuming a step, the current flow due to low-level injection is due to diffusion and given by

$$J_{LL} = aD_p\left(\frac{dp_N}{dx}\right)_{x=0} = \frac{qD_p p_{ON}}{L_p}\left(e^{\frac{qV_j}{kT}} - 1\right) \tag{3-10}$$

If the minority carrier diffusion length is on the order of the base width, then the carrier distribution becomes slightly altered and current density becomes

$$J_{LL} = \frac{qD_p p_{ON}}{L_p \tanh(W/L_p)}\left(e^{\frac{qV_j}{kT}} - 1\right) \tag{3-11}$$

Power PiN diodes are usually operated at very high current densities and therefore operate under high-level injection conditions. During high-level injection there is a significant change in the majority carrier concentration in the base, which gives rise to an electric field [26]. Therefore, carrier motion in the base is influenced by both drift and diffusion, and ambipolar transport must be considered.

Assuming negligible recombination in the emitter and end regions, an expression for the high level injection current density can be derived. In order to derive the expression for high-level injection in the base, it is assumed that recombination in the emitter and end region is negligible. In that case, the high-level injection current is determined by recombination in the base and is given by [27]

$$J_{HL} = \int_0^{W_B} qRdx \tag{3-12}$$

where R is the recombination rate given by $R = n(x)/\tau_{HL}$ and τ_{HL} is the high-level lifetime. The current density is now given by

$$J_{HL} = \frac{2qn_a d}{\tau_{HL}} \tag{3-13}$$

where n_a is the average carrier density.

For PiN diodes with highly doped anode and cathode regions, very high current densities are required to obtain emitter and end region recombination currents. The description of these current components is similar to low-level injection theory since the density of minority carriers injected into the end regions is much smaller than the background doping of the highly doped end regions [18].

3.2.2 Reverse Blocking

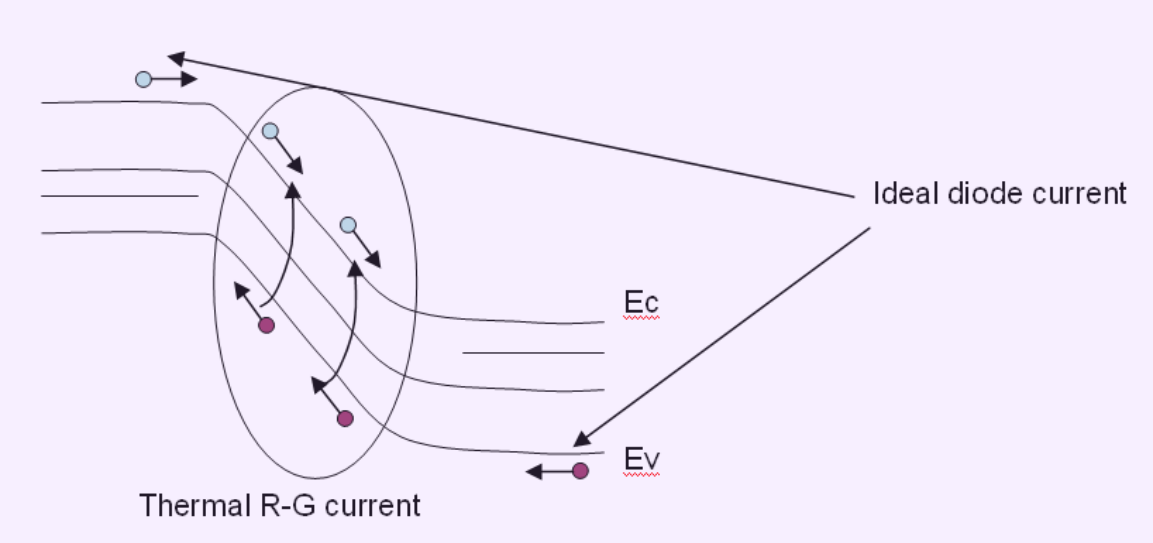


Figure 3-7 Band diagram of p-n junction under reverse bias condition

The power PiN diode is designed to be used in high voltage rating application. The capability of voltage blocking depends on the doping profile and the thickness of the drift region. Differ from the Schottky diodes, power PiN diodes offer much lower reverse leakage current. As illustrated from Figure 3-7, there are mainly two types of leakage current: depletion region thermal R-G current given by [24]

$$I_{R-G} = \frac{qAn_i}{2\tau_{SC}}(W - W_0) \tag{3-14}$$

where $W = \sqrt{\frac{2\varepsilon}{qN_D}(V_{bi} - V_a)}$

and ideal diffusion current given by [24]

$$I_0 = qA\frac{D}{L}\frac{n_i^2}{N_D} \tag{3-15}$$

where D is the diffusivity, L is the diffusion length.

The leakage current caused by the above two mechanism is much smaller than the one caused by the thermionic emission current across the barrier height in Schottky diode.

3.2.3 Transient Characteristics

When the diode is forward biased the excess carrier concentration builds up. Hence, when the device is turned off, the excess carrier must be removed before the junction goes to the blocking mode. The process of removing excess charge from the base and the resulting ability of the diode to block voltage is known as the reverse recovery phenomenon. The process consists of the sweeping out of stored charge due to the electric field, the diffusion of stored charge out of the base, and the recombination of stored charge. Once the junction can block voltage, the voltage begins to rise across the diode as the remaining stored charge decays.

3.3 Power Junction Barrier Schottky (JBS)/Merged PiN Schottky (MPS)

The structure of JBS/MPS diodes combines Schottky and PiN diodes as illustrated in Figure 3-8 with p-well embedded in the n- epilayer. Under forward bias, there are two operation modes JBS and MPS which is determined by the forward bias voltage level.

When the bias voltage is not high enough to turn on the inherent PiN diode, only the Schottky-part is conducting as shown in Figure 3-8 (a). As the bias increases, minority carriers start to be injected into n- layer from p-well to modulate the conductance in the epilayer. This type of operation is referred to as the MPS mode.

Under reverse bias, the depletion region starts to expand in order to support the blocking voltage as shown in Figure 3-8 (b). As seen from Figure 3-8 (b), the depletion layers will intersect under the Schottky barrier when the reverse bias exceeds a certain level, which is called *pinch-off*. After depletion layer pinch-off, further increase in applied voltage is supported by it with the depletion layer extending toward the n+ substrate, and the potential barrier shields the Schottky barrier from the applied voltage. This shielding prevents the Schottky barrier lowering phenomenon and eliminates the large increase in leakage current observed for conventional Schottky diodes. Ideally, once the pinch-off condition is established, the leakage current remains constant. Due to the suppressed leakage current, the Schottky barrier height used in the JBS diode can be significantly less than for the conventional Schottky diodes.

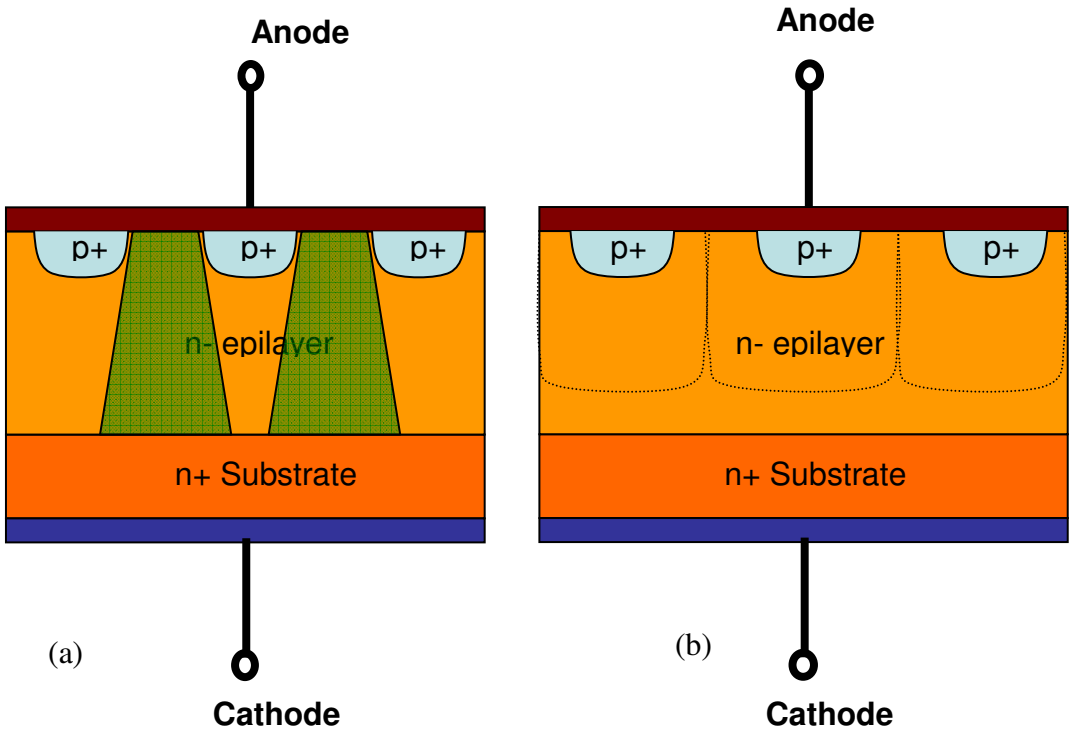


Figure 3-8 Structure of power JBS/MPS diode under forward bias (a); under reverse bias (b)

Chapter 4 Modeling and Automated Model Parameter Extraction for Power Diode

A wide range of diodes are currently available to fulfill the needs of various applications. Furthermore, new diodes are being developed and introduced that take advantage of advanced semiconductor materials (e.g., SiC and GaN) and advanced internal device structures. Circuit simulation using physics based models provides a means to select appropriate diode types for a given application and to optimize circuit performance, provided that accurate models can be readily produced from measured device characteristics. The purpose of this chapter is to introduce a new software package called DIode Model Parameter extrACtion Tools (DIMPACT) that enables rapid development and validation of device models for both Si and SiC power diodes.

The device model constructed using the extracted parameters are validated against the measured forward-biased conduction characteristics versus temperature, and junction capacitance characteristics at room temperature as well as a wide range of switching conditions that can occur in various applications.

4.1 Introduction to DIMPACT

As shown in Figure 4-1, this new software package provides a method to extract the necessary modeling parameters for three classes of power diodes: (a) Si and SiC Schottky/JBS diodes, which offer high switching speed but suffer from high leakage current; (b) Si and SiC PiN diodes, which offer low leakage current but suffer from slow reverse recovery switching characteristics; and (c) SiC Merge PiN Schottky (MPS)

diodes, which combine the advantages of Schottky and PiN diodes to offer Schottky-like on-state and switching characteristics and PiN-like off-state characteristics [4].

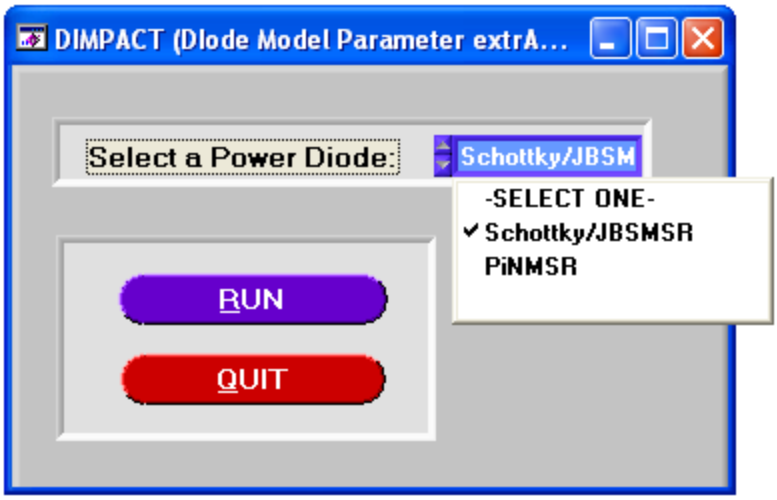


Figure 4-1 Power diode selection panel

By clicking the "RUN" button in purple, it will display another panel as shown in Figure 4-2. There are four types of model parameters extraction available including forward IV characteristics, reverse leakage characteristics, capacitance-voltage characteristics and the transient characteristics – reverse recovery.

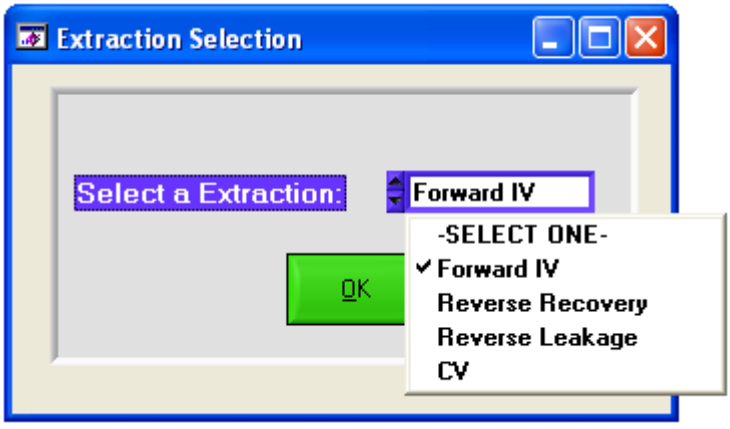


Figure 4-2 Extraction type selection panel

Some of the important physical parameters need to be set before extraction in the panel. As shown in Figure 4-3, the physical parameters are P-N grading coefficient (M),

forward-bias depletion capacitance coefficient (FC), Bandgap (EG), electron mobility (MUN), hole mobility (MNP), thermal voltage (VT), junction voltage (VJ), intrinsic carrier concentration (NI) and Richardson constant (A*). The values of the physical parameters will change corresponding to the selected material and characterization temperature. As seen from the material drag-down in this figure, the program is ready to extract both Si and SiC power diodes.

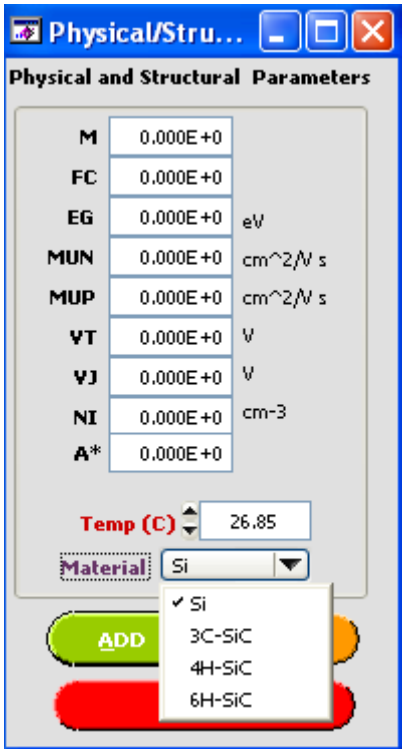


Figure 4-3 Panel of physical and structural parameters

The temperature dependence of the bandgap and carrier mobility for Si [28] are given by

$$EG_{Si}(T) = \left(EG(300K) + 0.05\right) - \frac{7.02\times10^{-4}\cdot T^{2}}{T + 1108} \tag{4-1}$$

$$\mu_n(T) = \mu_n(300K)\left(\frac{T}{300}\right)^{-2.5} \tag{4-2}$$

$$\mu_p(T) = \mu_p(300K)\left(\frac{T}{300}\right)^{-2.5} \tag{4-3}$$

and for SiC [25] are given by

$$EG_{SiC}(T) = EG(300K) - 3.3\times10^{-3}\left(T - 300K\right) \tag{4-4}$$

$$\mu_n(T) = \frac{\mu_n(300K)}{1+\left(\frac{N_B}{1.94\times10^{17}}\right)^{0.61}}\left(\frac{T}{300}\right)^{-2.15} \tag{4-5}$$

$$\mu_p(T) = 15.9\frac{\mu_p(300K)}{1+\left(\frac{N_B}{1.76\times10^{19}}\right)^{0.34}}\left(\frac{T}{300}\right)^{-2.15} \tag{4-6}$$

In the following sections, the detailed descriptions of the extraction procedure of Schottky/JBS program and PIN program will be presented.

4.2 Schottky/JBS Program

By selecting “Schottky/JBS” from Diode Selection Panel shown in Figure 4-1, the extraction selection panel will be displayed. The extraction sequence for static characteristics is Forward IV -> CV -> Reverse Leakage. In fact, the transient Reverse Recovery Characteristics (bottom-half part) share the same front panel with the static Forward IV Characteristics (top-half part) as shown in Figure 4-4 because they were developed first. In the following subsections, the model parameters will be extracted in sequence starting from Forward IV.

4.2.1 Static Forward-bias Characteristic

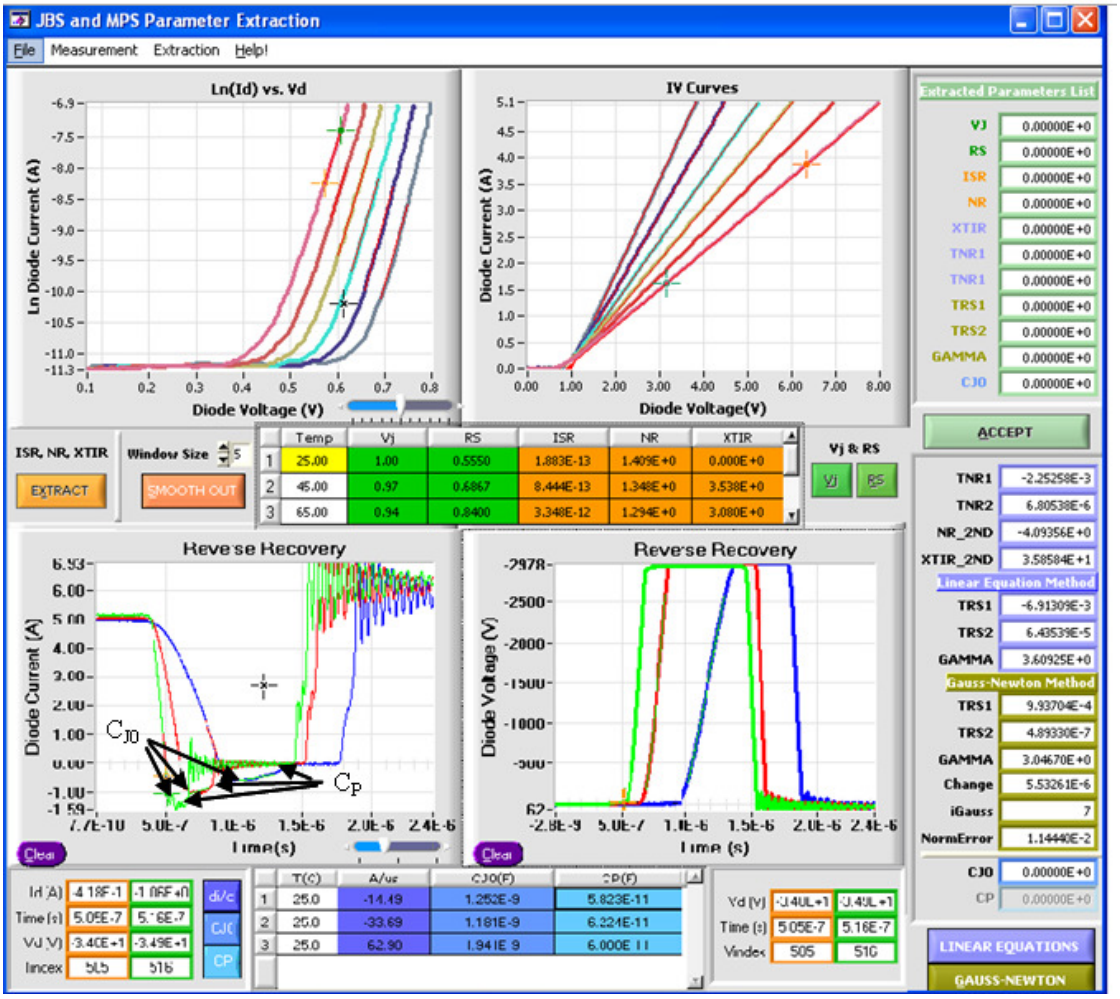


Figure 4-4 Front panel for Schottky/JBS/MPS program extraction on forward IV & reverse recovery

This part of program enables rapid extraction of the Schottky/JBS/MPS diode model parameters for the model described in [29] including the low-level recombination saturation current (ISR), low-level recombination emission coefficient (NR), ISR temperature exponent (XTIR), built-in junction potential (V_J), forward series contact resistance (R_S), linear NR temperature coefficient (TNR1), quadratic NR temperature coefficient (TNR2), linear R_S temperature coefficient (TRS1), quadratic R_S temperature coefficient (TRS2) and R_S temperature exponent (GAMMA). These parameters are

shown in the parameter list on the right half of Figure 4-4 as they are extracted. The extraction steps are performed in sequence as described in the following:

The extraction sequence begins with the selection of the semiconductor material type as well as the test fixture temperature. By selecting the "ADD" button, the extraction temperature will be loaded into the table located in the middle of the Figure 4-4. To perform the extraction, the anode diode current is measured as a function of the anode-cathode diode voltage at temperatures from 25 ^{o}C to 175 ^{o}C. Two commercial semiconductor curve tracers are used to aid in the parameter extraction process. The upper-left graph of Figure 4-4 shows diode current versus diode voltage on a logarithmic scale for the low-current range, which is used to extract parameters ISR, NR, and XTIR. The measurement is performed using the low-power curve tracer which can measure down to 1 μA. The measured data is loaded into the graph using the "File" pull-down menu by selecting the "Load Low LN Curve" option from the "Load" submenu. The upper-right graph shows the diode current versus diode voltage for the high-current range, which is used to extract parameters V_J and R_S. The measurement is performed using the high-power curve tracer with power up to 3 kW. The measured data are loaded into the graph using the "File" pull-down menu by selecting the "Load single IV curve" option from the "Load" submenu. Here, the user should make sure that the data loaded for each extraction correspond to the test fixture temperature highlighted in the table.

An iterative extraction loop is formed while extracting these parameters in order to acquire more accurate results. The first step is to extract the low-level parameters including ISR, NR and XTIR. Note that the voltage drop across R_S (V_{Rs}) is assumed to be negligible at the beginning of the extraction. Line the two cursors in the linear region of

the low-level logarithm plot. By clicking on the "EXTRACT" button in orange, it will get a straight line where the *y-intercept* and *slope* are used to extract ISR and NR, respectively. This process can be deduced and verified from equation (4-7). The extraction results of ISR, NR and XTIR will be displayed in the orange columns of the same table where extraction temperature is added from the Physical and Structure Parameter Panel as shown in Figure 4-3. These results will be used as the initial values to calculate the voltage drop across R_S (V_{Rs}) using equation (4-8). The second step is to extract the high-level parameters including V_J and R_S. By clicking on the "V_J" button in green, V_J is extracted from the x-intercept of the extrapolation line which is obtained by lining the two cursors in the linear region of the high-level diode current versus voltage plot. By clicking on the "R_S" button in green, a window with the new graph of V_{Rs} calculated from equation (4-8) versus the diode current is popped up for R_S extraction. By lining the two cursors in the linear region of this graph, R_S is extracted from the slope of the extrapolation line. By clicking on the "Accept" button, the extraction result of R_S will be displayed in the same table; and a message window will be popped up asking if the low-level logarithm graph located on the upper-left of the front panel needs to be re-plotted by subtracting out the voltage drop of R_S from the diode voltage. If "Yes" is selected, the low-level logarithm graph will be re-plotted and the parameter extraction will start over again from the first step using the re-plotted logarithm graph. The more this extraction procedure is repeated, the more accurate the extraction results are. If "No" is selected, the extraction loop will be ended and all the extraction results displayed in the table will be the final extraction results for that extraction temperature.

For the extraction of the temperature dependent coefficients or exponents, measurements of both low-level and high-level diode current versus voltage need to be done under different temperatures. By taking the natural logarithmic both sides of equation (4-9) [30], it can be written as equation (4-10) in order to extract XTIR.

$$I = ISR \cdot \left(e^{\frac{V}{N_R \cdot V_T}} - 1 \right) \tag{4-7}$$

$$V_{Rs} = V - \left(\ln(I) - \ln(ISR)\right) \cdot N_R \cdot V_T \tag{4-8}$$

$$ISR(T) = ISR(TNOM) \cdot \left(\frac{T}{TNOM} \right)^{XTIR} \cdot e^{\left[\left(\frac{T}{TNOM}\right)-1\right] \cdot \left(\frac{EG}{NR \cdot VT}\right)} \tag{4-9}$$

$$XTIR = \frac{\ln\left(\frac{ISR(T)}{ISR(TNOM)}\right) - \left[\left(\frac{T}{TNOM}\right)-1\right] \cdot \left(\frac{EG}{NR \cdot VT}\right)}{\ln\left(\frac{T}{TNOM}\right)} \tag{4-10}$$

$$N(T) = N(TNOM) \cdot \left[1 + TNR1 \cdot (T - TNOM) + TNR2 \cdot (T - TNOM)^2\right] \tag{4-11}$$

$$R_S(T) = R_S(TNOM) \cdot \left[\left(\frac{T}{TNOM} \right)^{GAMMA} + TRS1 \cdot (T - TNOM) + TRS2 \cdot (T - TNOM)^2 \right] \tag{4-12}$$

Equation (4-11) is used to extract TNR1 and TNR2 by using the Linear Equation Method as shown in the following matrix equation:

$$\begin{pmatrix} \frac{N(T_1)}{N(T_{nom})} - 1 \\ \bullet \\ \bullet \end{pmatrix} = TNR1 \begin{pmatrix} T_1 - T_{nom} \\ \bullet \\ \bullet \end{pmatrix} + TNR2 \begin{pmatrix} (T_1 - T_{nom})^2 \\ \bullet \\ \bullet \end{pmatrix}. \tag{4-13}$$

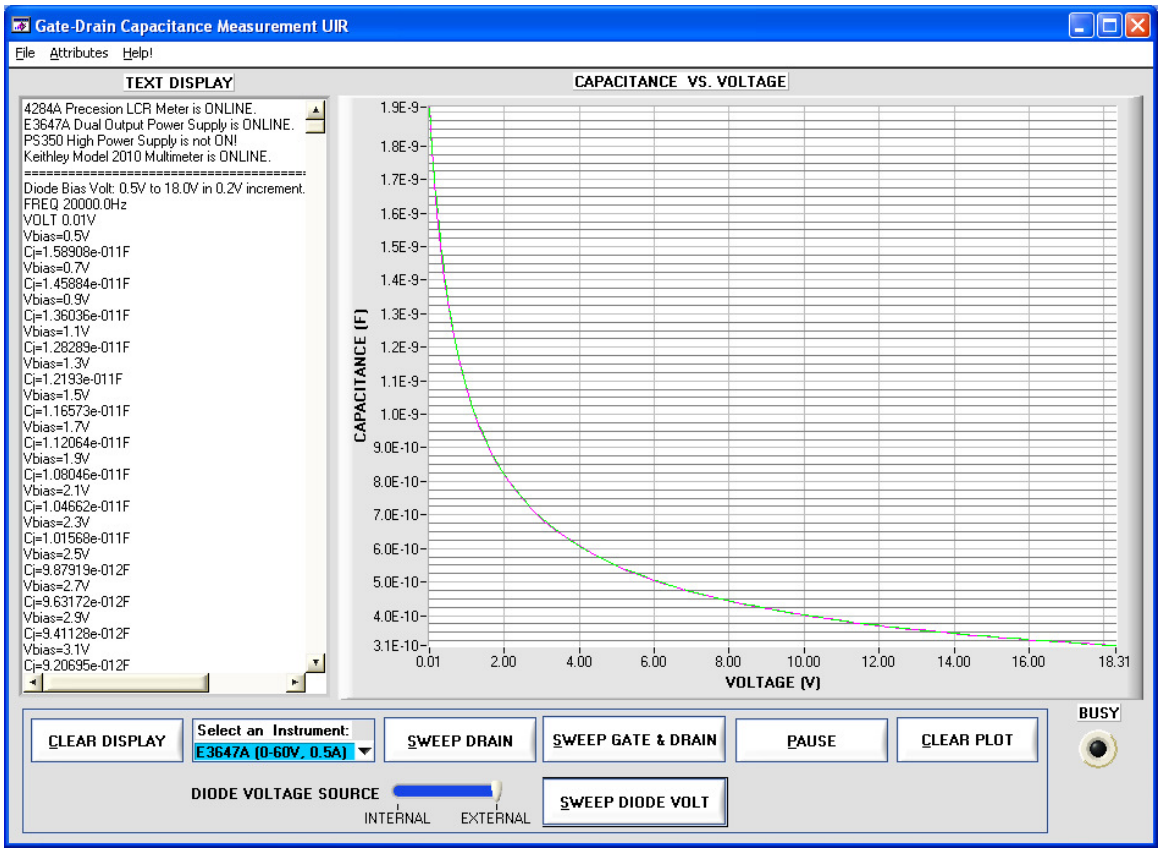
The resulting TNR1 and TNR2 parameters are displayed in the parameter list located on the right side of the front panel by selecting on the “LINEAR EQUATIONS” button. The TRS1, TRS2, and GAMMA parameters are extracted from equation (4-12) by using two different methods: (i) the Linear Equation Method as shown in the following equation:

$$\begin{pmatrix} \frac{R(T_1)}{R(T_{nom})} \\ \bullet \\ \bullet \end{pmatrix} = \begin{pmatrix} \frac{T_1}{T_{nom}} \\ \bullet \\ \bullet \end{pmatrix}^{GAMMA} + TRS1 \begin{pmatrix} T_1 - T_{nom} \\ \bullet \\ \bullet \end{pmatrix} + TRS2 \begin{pmatrix} (T_1 - T_{nom})^2 \\ \bullet \\ \bullet \end{pmatrix} \tag{4-14}$$

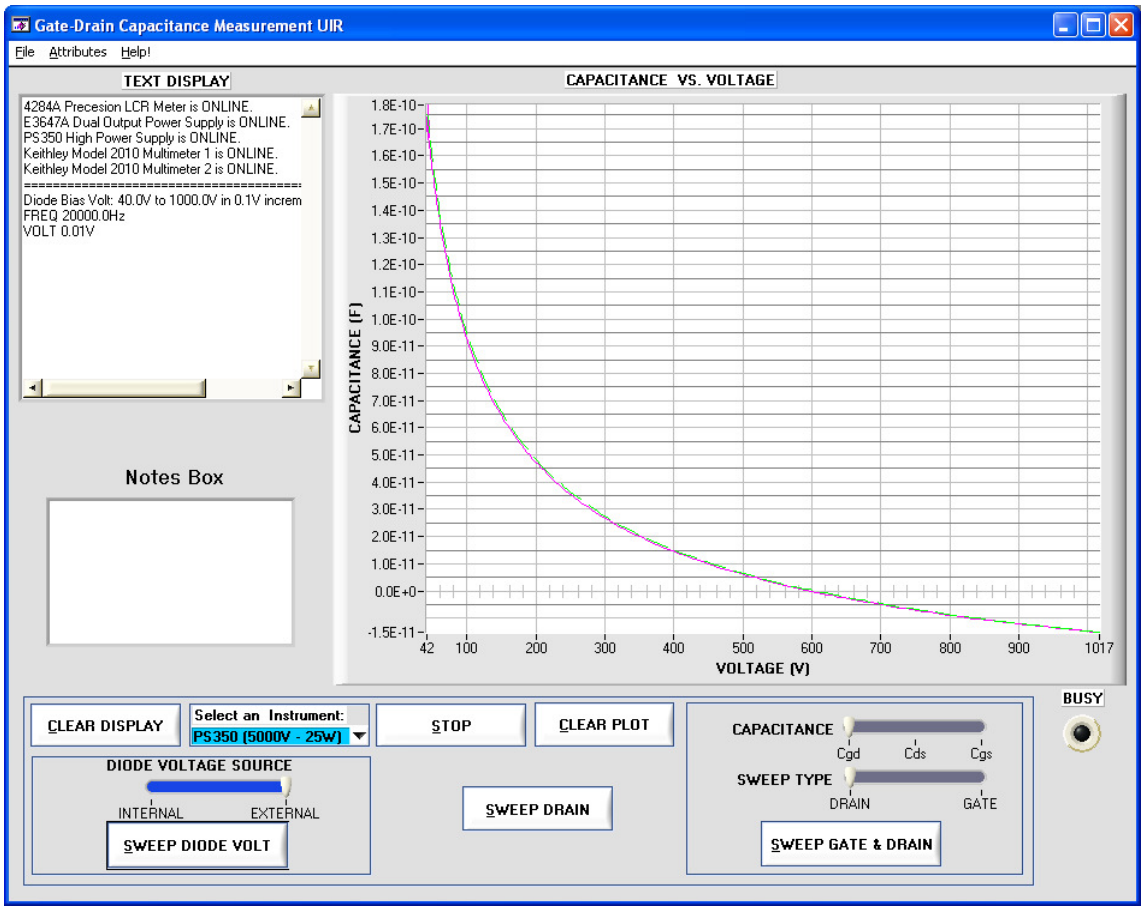
and (ii) the Gauss-Newton Algorithm [31]. The resulting TRS1, TRS2, and GAMMA parameters are displayed in the parameter list located on the right part of the front panel by selecting the "LINEAR EQUATIONS" button using (i) and the "GAUSS-NEWTON" button using (ii). Statistically speaking, in order to extract the temperature dependent coefficients or exponents using the above two methods, there have to be at least three sets of model parameters extracted at different temperatures. All the resulting model parameters are displayed in the parameter list on the upper right corner of the front panel by selecting on the "ACCEPT" button.

4.2.2 Junction Capacitance Characteristic

The junction capacitance versus diode voltage (C-V) measurement is used to perform the extraction on C_{J0}, V_{bi} and N_B for both low and high voltage power diodes. The measurement panel is shown in Figure 4-5 and the parameter extraction panels are shown in Figure 4-6 for a 45 V, 15A Si Schottky diode (a) and a 10 kV, 5A SiC JBS diode (b). The details of the C-V measurement setup can be found in Parrish Ralston's Master Thesis, in which she explains the selection of the circuit components and the theoretical prediction on the measurement accuracy.

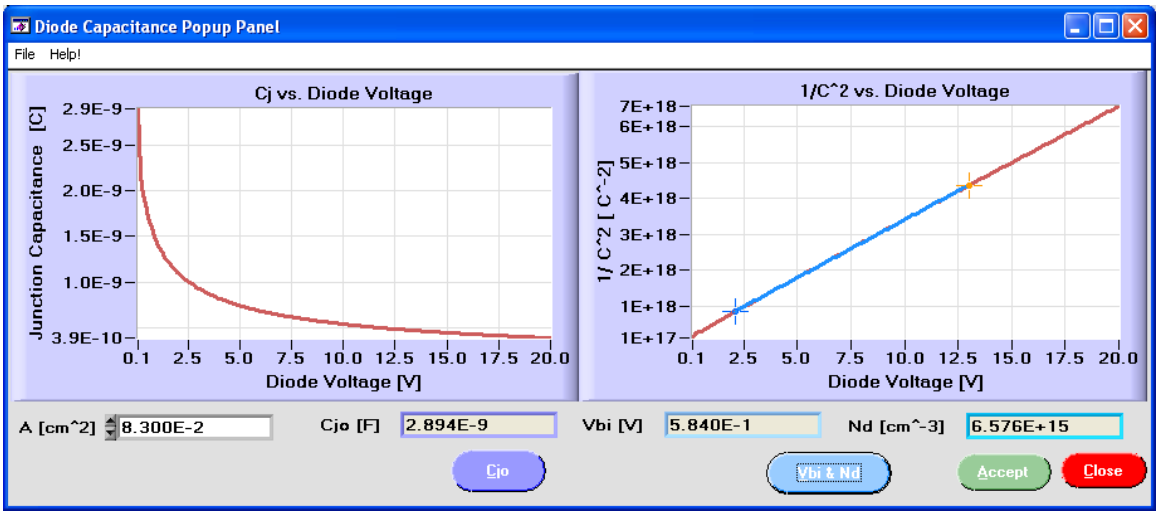

Gate-Drain Capacitance Measurement UIR
File Attributes Help!
TEXT DISPLAY
4284A Precesion LCR Meter is ONLINE.
E3647A Dual Output Power Supply is ONLINE.
PS350 High Power Supply is not ON!
Keithley Model 2010 Multimeter is ONLINE.
Diode Bias Volt: 0.5V to 18.0V in 0.2V increment.
FREQ 20000.0Hz
VOLT 0.01V
Vbias=0.5V
Cj=1.58908e-011F
Vbias=0.7V
Cj=1.45884e-011F
Vbias=0.9V
Cj=1.36036e-011F
Vbias=1.1V
Cj=1.28289e-011F
Vbias=1.3V
Cj=1.2193e-011F
Vbias=1.5V
Cj=1.16573e-011F
Vbias=1.7V
Cj=1.12064e-011F
Vbias=1.9V
Cj=1.08046e-011F
Vbias=2.1V
Cj=1.04662e-011F
Vbias=2.3V
Cj=1.01568e-011F
Vbias=2.5V
Cj=9.87919e-012F
Vbias=2.7V
Cj=9.63172e-012F
Vbias=2.9V
Cj=9.41128e-012F
Vbias=3.1V
Cj=9.20695e-012F
CAPACITANCE VS. VOLTAGE
CAPACITANCE (F)
1.9E-9
1.8E-9
1.7E-9
1.6E-9
1.5E-9
1.4E-9
1.3E-9
1.2E-9
1.1E-9
1.0E-9
9.0E-10
8.0E-10
7.0E-10
6.0E-10
5.0E-10
4.0E-10
3.1E-10
0.01
2.00
4.00
6.00
8.00
10.00
12.00
14.00
16.00
18.31
VOLTAGE (V)
CLEAR DISPLAY
Select an Instrument:
E3647A (0-60V, 0.5A)
SWEEP DRAIN
SWEEP GATE & DRAIN
PAUSE
CLEAR PLOT
BUSY
DIODE VOLTAGE SOURCE
INTERNAL
EXTERNAL
SWEEP DIODE VOLT

(a)

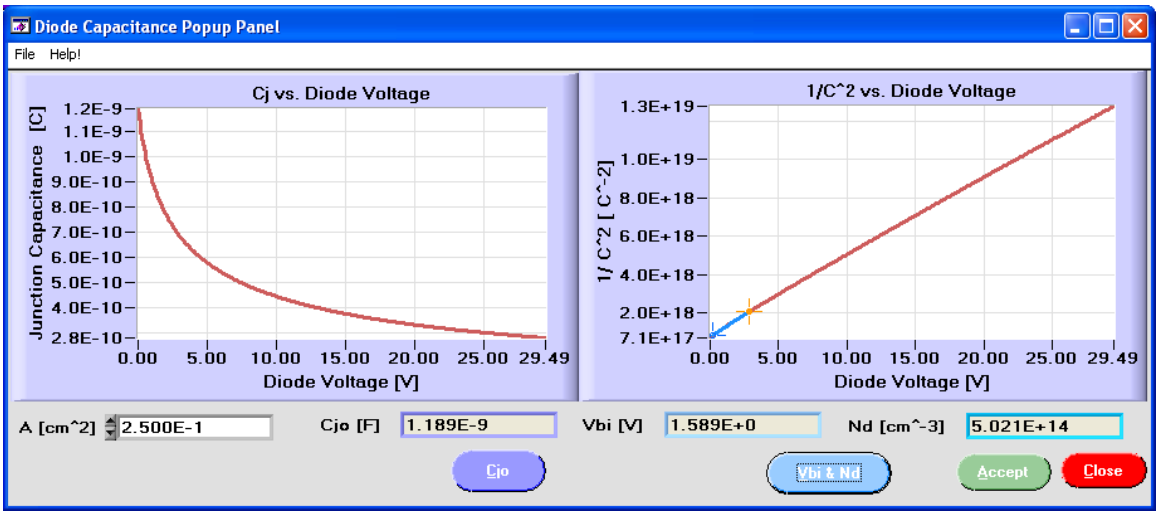


(b)

Figure 4-5 C-V measurement interface for a 45 V, 15 A Si Schottky diode (a); and a 10 kV, 5 A SiC JBS diode (b)



(a)



(b)

Figure 4-6 The extraction panel for a 45 V, 15 A Si Schottky diode (a); and a 10 kV, 5 A SiC JBS diode (b) on parameters C_{J0}, V_{bi}, and N_B

From Figure 4-5, it can be seen that junction capacitance decreases as the bias voltage increases due to the increase of the depletion width. The situation is physically identical to what takes place inside a parallel plate capacitor. It can be written by analogy in the form of equation (4-15).

$$C = \frac{\varepsilon_r \varepsilon_0 A}{W} \tag{4-15}$$

The depletion width is given by

$$W = \left[\frac{2\varepsilon_r \varepsilon_0}{qN_B} (V_{bi} - V_A) \right]^{1/2} \tag{4-16}$$

By substituting (4-16) into (4-15), and reorganize the equation into a linear form with the voltage as shown in equation (4-17).

$$\frac{1}{C^2} = \frac{2}{qN_B \varepsilon_r \varepsilon_0 A^2} (V_{bi} - V_A) \tag{4-17}$$

The $1/C^2$ versus V plot of the experimental data of Figure 4-6 exhibits a nearly straight line dependence in agreement with equation (4-17). Per equation (4-17) the semiconductor doping could be deduced from the slope of the straight line fitted to the plot points, V_{bi} from the extrapolated $1/C^2 = 0$ intercept and $1/C_{J0}^2$ from the extrapolated y-intercept where V=0. The extracted parameters will be saved for the use in the following extraction.

4.2.3 Reverse Recovery Characteristic

The reverse recovery current for Schottky diodes is caused by the junction and packaging capacitances. So, the reverse recovery measurement is the second method to perform the extraction on C_{J0} for high voltage power diodes. The test system independently controls the turn-off forward current, reverse voltage, di/dt, dv/dt and temperature. Figure 4-7 (a) shows the test circuit used for characterizing the high voltage diodes for reverse recovery, and Figure 4-7 (b) shows the behavioral representation including parasitic elements used for diode model validation. It is important to note that the test circuit in Figure 4-7 (a) is well-characterized, meaning that the values of all

circuit components and parasitic elements are known. To operate the test circuit in Figure 4-7 (a), first the vacuum tube is turned on to establish the test current i_L in the inductor L. Once the test current is reached, the tube is ramped off and the inductor current is commutated to the Device Under Test (DUT). To initiate the reverse recovery test, the tube is ramped on with a well-controlled di_Q / dt at the tube anode. This results in a negative di_Q / dt being applied to the DUT. As the diode begins to recover the diode voltage v rises toward the power supply voltage Vs completing the recovery test.

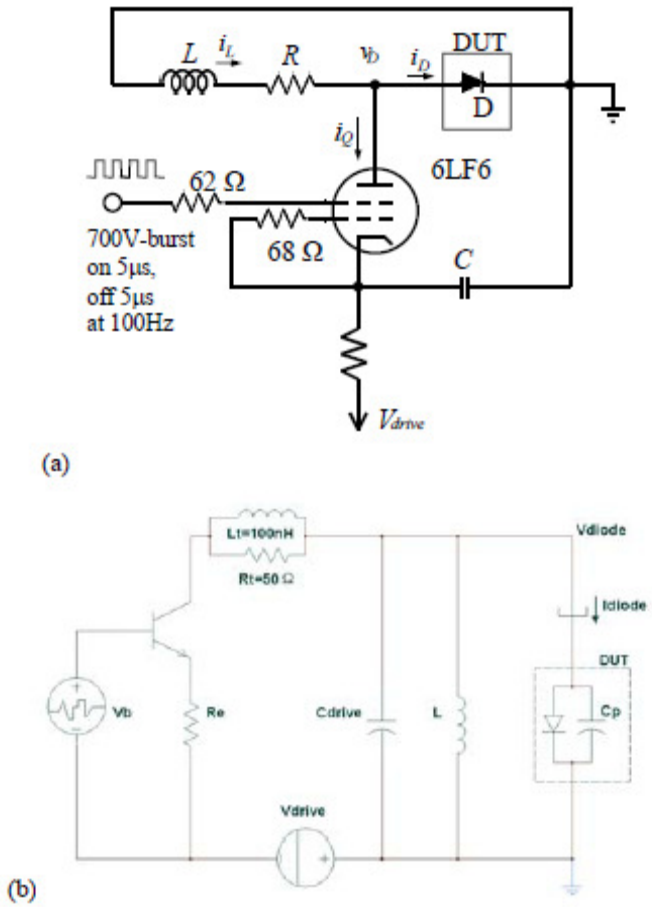
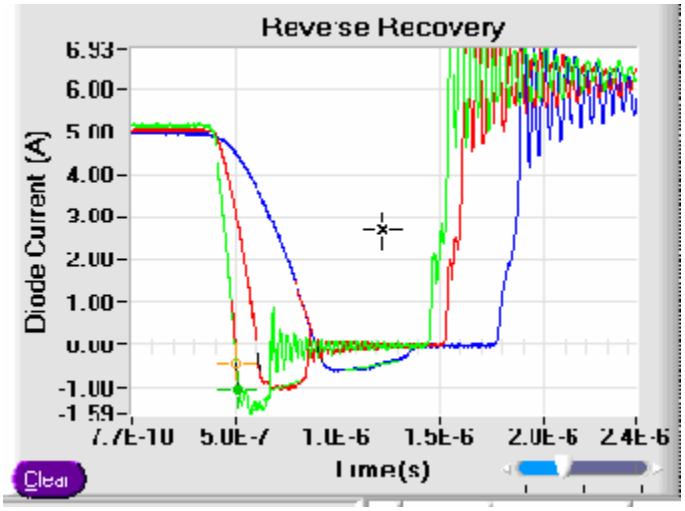


Figure 4-7 High-speed reverse recovery test circuit (a); and behavior model of reverse recovery test circuit in (b)

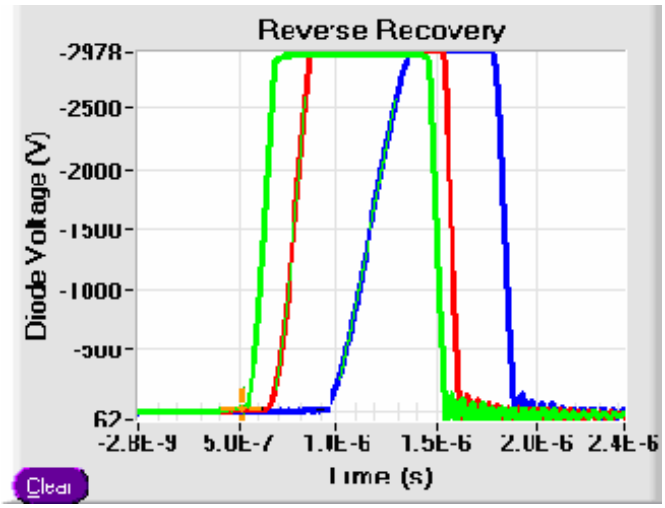
The circuit of Figure 4-7 (a) uses a 6LF6 vacuum tube as a driver device in place of the usual MOSFET to achieve low parasitic capacitance at the DUT anode and an extremely fast switching speed. The 51 Ω resistor R isolates the DUT from the parasitic capacitance of the 30 mH inductor L and is also used to quickly reset the inductor current to zero after each test. The dv/dt of the square wave applied to the tube screen is varied to achieve different di/dt values for the DUT. With a 700 V peak drive to the screen grid of the tube, the circuit can test over 12 A of combined forward and reverse DUT current, and the applied voltage to the DUT can be up to 2000 V. For higher current drive capability, a similar 50 A, 5000 V reverse recovery test system is used.

The reverse recovery tests are performed for various values of forward diode current i, diode reverse bias power supply voltage V_s, di/dt, and dv/dt, where dv/dt is controlled by placing various driver capacitors across the DUT. By independently controlling V_s, di/dt, dv/dt, and the forward diode current at turn-off the test circuit enables testing of SiC diodes for the full range of conditions that occur for various application conditions. Varying the value of v emulates the application conditions for circuits with different DC buss voltages, varying the value of di/dt emulates the application conditions of different speed anti-parallel switching devices, and varying the value of dv/dt emulates the application conditions of using anti-parallel switching devices of different output capacitance. Also, it aids in the determination of the portion of the diode reverse recovery due to charge storage and the portion due to device capacitance by varying the value of dv/dt. It aids in the determination of the portion of current that is due to emitter recombination and the portion that contributes to charge storage by varying the value of the forward diode current at turnoff.

The behavioral representation of the test circuit, Figure 4-7 (b), uses an ideal bipolar transistor model with an emitter follower resistor, Re, to emulate the di/dt applied by the tube. The bipolar transistor model capacitance parameters are set to zero and replaced by the 40 pF output capacitance of the tube (combined with Cdrive in Figure 4-7 (b)). The next most important parasitic elements of the test circuit are the 100 nH tube inductance Lt and the 50 Ω tube resistance Rt that result in a small voltage overshoot near the end of the diode current recovery waveforms. The inductor L remains at 30 mH as in Figure 4-7 (a). The pulse width of the signal generator Vb is varied to determine the forward current for the reverse recovery test, and the rise time of Vb determines the di/dt applied to the DUT at turn off.



(a)



(b)

Figure 4-8 Transient reverse recovery measurement: reverse recovery diode current (a); and reverse recovery diode voltage versus time (b)

Measurement data is loaded onto the lower-two graphs of Figure 4-4 to perform parameter extraction as shown in Figure 4-8. The measurement was done with three different di/dt : 15 A/us, 32 A/us and 67 A/us to emulate different switching conditions. Two cursors (green and orange) are used to measure the di/dt slope and the result is loaded into the second column of the bottom table of Figure 4-4. C_{J0} and Cp are extracted from the first and second corner of reverse recovery current diagram as shown in Figure 4-8 (a) using equation (4-18).

$$i = C\frac{dv}{dt} \tag{4-18}$$

dv/dt is calculated by taking the derivative of second order polynomial fit of v(t) in the form of $v(t) = at^2 + bt + c$. Hence, $dv/dt = 2at + b$ with the know vectors a and b from the polynomial fit. The extracted C_{J0} and Cp will be loaded into the third and fourth column of the same table into where the di/dt is loaded. The parameters extracted from

the reverse recovery measurement in Schottky/JBS program are less than the ones in PIN program.

4.2.4 Reverse-bias Characteristic

In the current power diode model in the Saber circuit simulator, an empirical approach was used to describe the low-bias reverse blocking region by introducing an effect called "conduction loss," a parameter that causes a linear relationship between the device voltage and current at low bias voltages with no physics meaning [32]. Furthermore, this term is not sufficient to accurately describe the changes to the device characteristics as the junction temperature is varied. A more accurate model is required in order to adjust different systems, to fine tune the parameters of the energy management system, and to design power electronics system [33]. In this paper, a new physics-based model of the reverse blocking characteristics for power Schottky/JBS diodes was developed by including the thermionic-emission mechanism in the low-bias range and was implemented in the Saber circuit simulator as an enhancement to the current power diode model.

The reverse-bias leakage mechanisms consist of thermionic emission current (injection of carriers across the barrier), depletion region recombination and generation (R-G) current, diffusion current, surface leakage current and defect induced leakage current. As majority carrier devices, thermionic emission current is the one dominate over the other leakage mechanisms, given by

$$I_{th} = A \cdot A^{*} \cdot T^{2} e^{\frac{\phi_{B0} - \Delta\phi_{B}}{kT}} \tag{4-19}$$

where A^* is the effective Richardson constant, ϕ_{B0} is the zero-biased Schottky barrier height, and $\Delta\phi_B$ is the lowering of the barrier height given by [34]

$$\Delta\Phi_B = q\left[\frac{q|E|}{4\pi\varepsilon}\right]^{1/2}. \tag{4-20}$$

In (4-20), E represents the internal electric field at the Schottky contact written in the form of

$$E = \sqrt{\frac{qN_d}{2\varepsilon}\left(V_R + \psi_{bi} - \frac{kT}{q}\right)} \tag{4-21}$$

where N_d is the background doping concentration, and Ψ_{bi} is the junction build-in voltage. The equation for pre-avalanche breakdown impact ionization effect is an exponential relationship adopted from the current power diode model in the form of

$$i_i = X_{BV} \cdot \left(e^{-(V_j+BV)/N_{BV}\cdot V_T} - e^{-BV/N_{BV}\cdot V_T}\right) \tag{4-22}$$

where

$$X_{BV} = \frac{I_{BV} - I_{th}}{e^{\frac{V_j+BV}{N_{BV}\cdot V_T}} - e^{\frac{BV}{N_{BV}\cdot V_T}}}, \tag{4-23}$$

BV: Breakdown Voltage

I_{BV}: Leakage Current at Breakdown Voltage

The impact ionization is the initial stage of Avalanche breakdown, which is defined as the process that an electron (or hole) with enough kinetic energy can create one or multiple electron-hole pair. The Avalanche process starts when the multiplication factor (M) goes to infinite. The multiplication factor is inversely proportional to the integral of

the impact ionization coefficient as $M \propto \left(1-\int_0^W \alpha dx\right)^{-1}$, from which it can be concluded that when $\int_0^W \alpha dx \to 1, M \to \infty$. However, the impact ionization coefficient decreases as temperature increases as illustrated in Figure 4-9 (a) and (b) [36, 37]. This decrease of impact ionization coefficient will make the device breakdown at higher voltage, which means the device is suppose have higher breakdown voltage at higher temperature.

As described in Chapter 3, the JBS diode is a Schottky diode structure with a p-n junction grid integrated into its drift region. When the reverse bias exceeds certain voltage, the depletion layer become pinched-off and a potential barrier is formed in the channel. The reverse leakage current of a JBS diode can be expressed by

$$I_{th} = R \cdot A \cdot A^* T^2 e^{-\frac{(\Phi_{B0} - \Delta\Phi_B)}{kT}} \tag{4-24}$$

where R is a ratio parameter related to the window area and mask region of the p-n grids as well as structural dimensions [34]. Ideally, once the neck region becomes pinched-off, the electric field at the Schottky contact remains constant (independent of the reverse-bias voltage). Hence, the leakage current from the thermionic-emission should not change with the increase of the reverse-bias voltage (V_R). However, it is reported that instead of being constant after pinch-off, the electric field at the Schottky contact is still changing with V_R but raised to a different power [35]. Thus, for JBS diodes the internal electric field can be described as

$$E = \left[\frac{qN_d}{2\varepsilon}\left(V_R + \psi_{bi} - \frac{kT}{q}\right)\right]^{\alpha} \tag{4-25}$$

where α is introduced as the fitting parameter for the electric field at the Schottky contact. The equation for the pre-avalanche breakdown impact ionization effect is the same as the one used for conventional Schottky diodes as shown in (4-22).

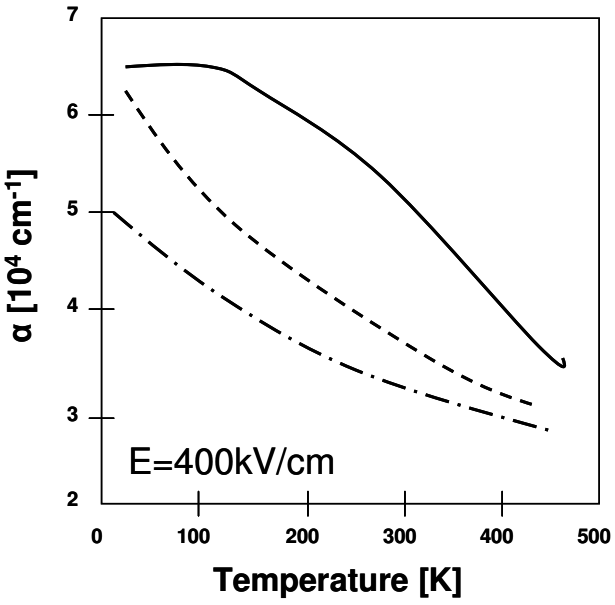
Parameters BV, I_{BV}, and N_{BV} have already been defined in the present Saber model [32]. Among the parameters that evolved in the new enhanced model, ϕ_{B0} (or BH0) is varied according to temperature in the form of

$$\phi_{B0}(T) = \phi_{B0}(TNOM) \cdot [1 + T\phi_{B0}1 \cdot (T - TNOM) + T\phi_{B0}2 \cdot (T - TNOM)^2] \quad (4\text{-}26)$$

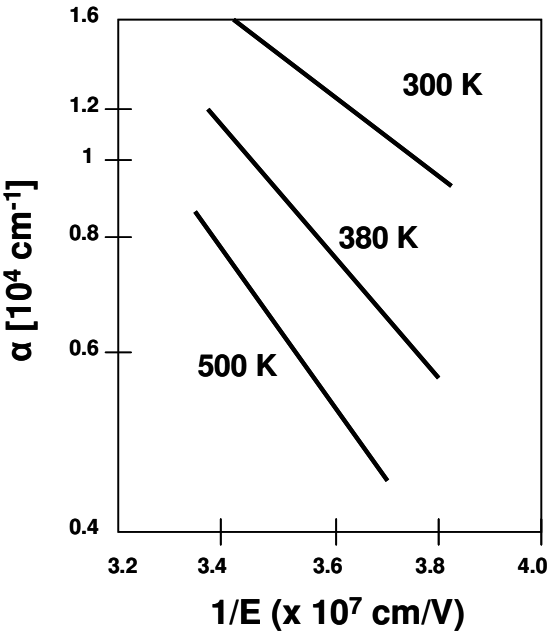
where $T\Phi_{B0}1$ (or TBH01) and $T\Phi_{B0}2$ (or TBH02) are the linear and quadratic temperature coefficients for ϕ_{B0} (or BH0). Here α varies with temperature according to

$$\alpha(T) = \alpha(TNOM) \cdot [1 + T\alpha1 \cdot (T - TNOM) + T\alpha2 \cdot (T - TNOM)^2] \quad (4\text{-}27)$$

where Tα1 and Tα2 are the linear and quadratic temperature coefficients for α. All the model parameters employed in the new model can be extracted automatically using DIMPACT.



(a)



(b)

Figure 4-9 Impact ionization coefficient versus temperature for Si (a); and for SiC (b)

In Figure 4-10, a comparison between the measured data, the simulated curves of the new enhanced model, and the simulated curves of the current model are shown for the 10 kV SiC JBS diodes at 125 ^{o}C. At 1 kV, excellent agreement between the measured data and the simulated curve using the new model is obtained. On the other hand, the error between the measured data and the simulated curve using the old model has been found to be 27 %. It is obvious that this new model will allow the validation of system behavior with a high degree of accuracy under the reverse blocking condition, especially for most of the low-bias range.

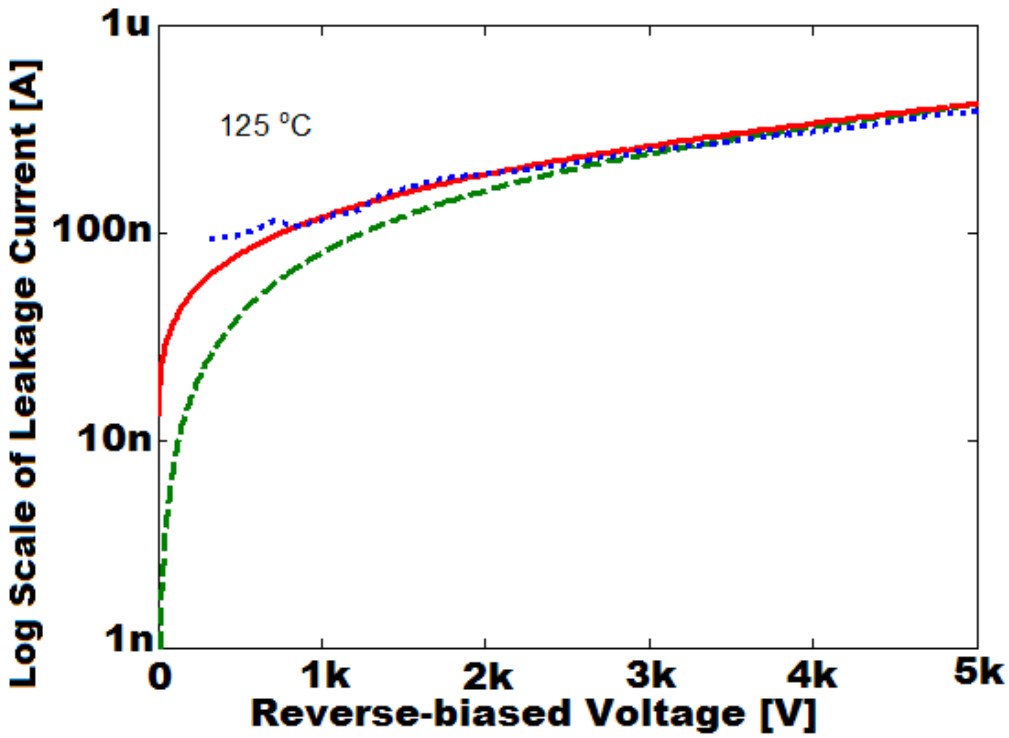


Figure 4-10 Comparison between measured data (dotted line), simulated curve of current model (dashed line), and simulated curve of new enhanced model (solid line) for the 10 kV SiC JBS diode at 125 °C in the low bias range

This new physics-based model for the reverse leakage characteristics has been developed as an enhancement to the present power diode model in the Saber circuit simulator. Correspondingly, the newly derived model equations are implemented in DIMPACT for automatic parameter extraction. Figure 4-11 shows the sub-panel of the parameter extraction program for the reverse leakage measurement which is selected from the drop-down list as shown in Figure 4-2 (b).

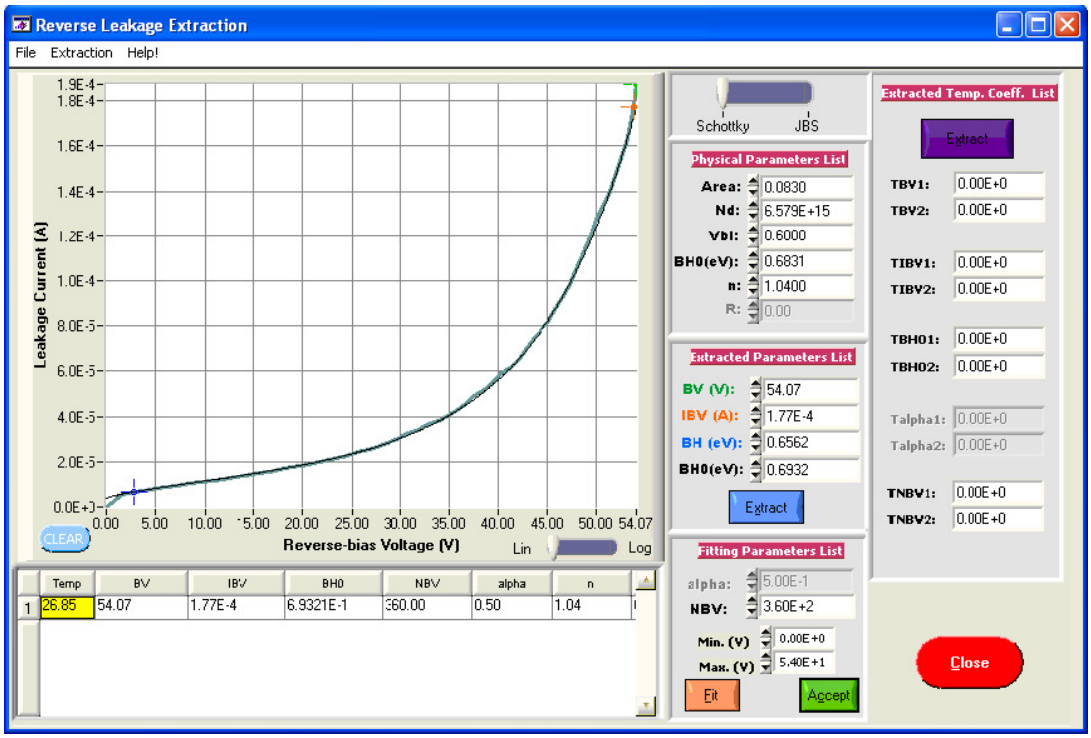


Figure 4-11 Sub-panel for extracting parameters from Reverse Leakage for Si and SiC JBS diodes

This program enables the extraction of the parameters in the new model described in Section II including BV, I_{BV}, N_{BV}, ϕ_{B0}, and α, as well as the temperature coefficients for these parameters. Note that α and R are model parameters used only for JBS diodes. A sliding bar is added next to the plotting area, which is used as an option to select the extraction between Schottky and JBS diodes. When the sliding bar is at "Schottky" position, the numerical controls for α, R, $T\alpha 1$, and $T\alpha 2$ are dimmed. The extraction sequence also begins with the selection of the test fixture temperature and the material type of the power device. The input value for the test fixture temperature will be loaded into the table located at the bottom of the front-panel. The measured reverse leakage data are loaded and then plotted in the graph of Figure 4-11 using the "File" pull-down menu by selecting the "Load" option. Physical and structural device parameters such as area

(device active area), N_d, V_{bi}, and BH0 (zero-biased barrier height, or ϕ_{B0}) are displayed in the numerical controls under the "Physical Parameter List" label because of their role in the calculation of model parameters as shown in equations (4-19) and (4-21). Note that the values for N_d and V_{bi} are extracted from the **CV** program as described in subsection 4.2.2; and the parameter BH0 displayed here is calculated from the saturation current extracted from the low-current range of the forward conduction measurement in the **Forward IV** program. Two cursors were activated to aid in the extraction process as shown in the graph of Figure 4-11 where the blue cursor is enabled to extract the leakage current (y-axis value of the cursor) and the bias voltage (x-axis value of the cursor) in the very low-bias range; whereas the orange cursor is enabled to extract IBV and BV in the breakdown region. The leakage current extracted using the blue cursor is substituted into (4-19) to calculate the Schottky barrier height (BH or ϕ_B) by assuming the impact ionization current is negligible when the bias is very low. The corresponding bias voltage extracted using the blue cursor is substitute into (4-20) to calculate the lowering effect of the Schottky barrier (ΔBH, or $\Delta\phi_B$) which is then used to calculate BH0 by adding together with BH. The "Extraction" button is used to read current and voltage values from the cursors, perform calculations as described above using an internal function, and display the extracted values for BV, IBV, BH, and BH0 into the numerical controls located under the "Extracted Parameters List" label. Notice that this program provides two methods of extracting the value for BH0: (i) from the forward-bias region and (ii) from the reverse-bias region. It offers an approach to verifying the accuracy of the extracted parameters by comparing the values for BH0 extracted separately using (i) and (ii).

The temperature-dependent coefficients are ready to be extracted after repeating the extraction procedure for each test fixture temperature. The “Extraction” button in purple is used to extract the values for TBV1, TBV2, TIBV1, TIBV2, TBH01, TBH02, TNBV1, TNBV2, Talpha1, and Talpha2 using the form of (4-26) and loading the extracted values into the numerical controls located under the “Extracted Temp. Coeff. List” label on the right side of the sub-panel.

4.2.5 Model Parameters for Schottky/JBS diodes

Table 4-1 shows the complete model parameters employed for Schottky/JBS diodes in the Saber template. The model parameters highlighted in yellow are used for the forward conduction range; the parameters highlighted in blue are used for C-V measurement; and the parameters highlighted in light green are used for the reverse blocking range.

Table 4-1 Complete model parameters employed for Schottky/JBS diodes

Schottky/JBS				
Parameter	Parameter Name	Extraction Characteristic	Schottky	JBS
RS	Forward series contact resistance	High to medium current on-state slope	x	x
ISR	Low-level recombination saturation current	Low current on-state region	x	x
NR	Low-level ideality factor	Low current on-state region	x	x
XTIR	ISR temperature exponent	Low current on-state vs. temperature	x	x
TNR1	Linear NR temperature coefficient	Low current on-state vs. temperature	x	x
TNR2	Quadratic NR temperature coefficient	Low current on-state vs. temperature	x	x
TRS1	Linear RS temperature coefficient	High to medium current on-state slope vs.temperature	x	x
TRS2	Quadratic RS temperature coefficient	High to medium current on-state slope vs.temperature	x	x
GAMMA	RS temperature exponent	High to medium current on-state slope vs.temperature	x	x
CJ0	Zero-bias junction capacitance	Capacitance-Voltage Or Reverse Recovery	x	x
NB	Drift region background doping concentration	Capacitance-Voltage	x	x
VBI	Junction built-in voltage	Capacitance-Voltage	x	x
BV	Breakdown Voltage	Reverse-bias breakdown region	x	x
IBV	Current at breakdown voltage	Reverse-bias breakdown region	x	x
BH0	Zero-bias junction barrier height	Reverse-bias low-level region	x	x
ALPHA	Electric field power rate			x
R	JBS diode structure coefficient			x
TBV1	Linear BV temperature coefficient	Reverse-bias breakdown vs. temperature	x	x
TBV2	Quadratic BV temperature coefficient	Reverse-bias breakdown vs. temperature	x	x
TIBV1	Linear IBV temperature coefficient	Reverse-bias breakdown vs. temperature	x	x
TIBV2	Quadratic IBV temperature coefficient	Reverse-bias breakdown vs. temperature	x	x
TBH1	Linear BH temperature coefficient	Reverse-bias low-level vs. temperature	x	x
TBH2	Quadratic BH temperature coefficient	Reverse-bias low-level vs. temperature	x	x
TALPHA1	Linear ALPHA temperature coefficient			x
TALPHA2	Quadratic ALPHA temperature coefficient			x
TNBV1	Linear NBV temperature coefficient		x	x
TNBV2	Quadratic NBV temperature coefficient		x	x

4.3 PiN Program

By selecting “PiN” from Diode Selection Panel shown in Figure 4-1, the extraction selection panel will be displayed. So far, there are two extraction selections for PiN program, which are **Forward IV** and **Reverse Recovery**. Likewise, the transient Reverse Recovery Characteristics (bottom-half part) share the same front panel with the static forward conduction characteristics (top-half part) as shown in Figure 4-12 because they were developed first. In the following subsections, the model parameters will be extracted starting from forward conduction measurement. As described in chapter 3, in the forward conduction range, more processes are involved depend on the injection of the current level for PiN diodes. Consequently, more model parameters need to be extracted in order to construct power diode model for PiN diodes.

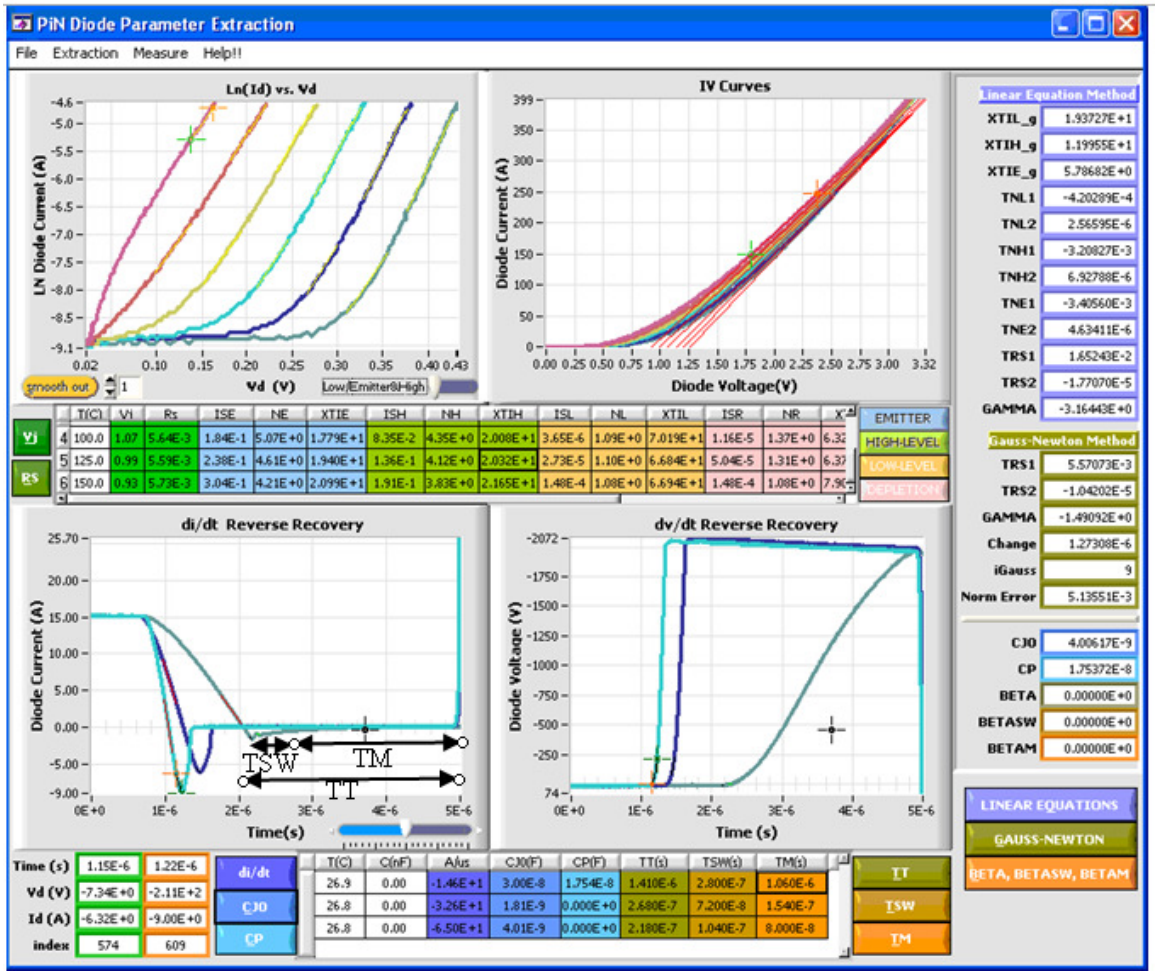


Figure 4-12 Sub-panel for extracting parameters from Forward IV/Reverse Recovery for Si and SiC PiN diodes

4.3.1 Static Forward-bias Characteristic

Figure 4-12 shows the sub-panel of the parameter extraction program (**Forward IV/Reverse Recovery**) for PiN diodes, which is similar to the **Forward IV/Reverse Recovery** extraction sub-panel in the JBSMSR program but contains more model parameters. The top half of the sub-panel was designed for the parameter extraction program of **Forward IV**, which is capable of extracting all the model parameters used in the forward-bias region for PiN diodes including the low-level recombination saturation current (ISR), low-level recombination emission coefficient (NR), ISR temperature

exponent (XTIR), low-current injection saturation current (ISL), low-current injection emission coefficient (NL), ISL temperature exponent (XTIL), high-current injection saturation current (ISH), high-current injection emission coefficient (NH), ISH temperature exponent (XTIH), emitter level saturation current (ISE), emitter level emission coefficient (NE), ISE temperature exponent (XTIE), built-in junction potential (V_J), forward series contact resistance (R_S), linear NR temperature coefficient (TNR1), quadratic NR temperature coefficient (TNR2), linear NL temperature coefficient (TNL1), quadratic NL temperature coefficient (TNL2), linear NH temperature coefficient (TNH1), quadratic NH temperature coefficient (TNH2), linear NE temperature coefficient (TNE1), quadratic NE temperature coefficient (TNE2), linear R_S temperature coefficient (TRS1), quadratic R_S temperature coefficient (TRS2) and R_S temperature exponent (GAMMA) [29, 38]. These parameters are shown in the table located in the middle of the sub-panel as well as in the parameter list on the right half of the sub-panel in Figure 4-12 as they are extracted.

Equations similar to (4-7) are also used for the high- and low-level base injection currents, unless both conditions apply; then the equations are coupled to provide better continuity and flexibility in characterization

$$i_0 = \frac{2i_L}{1+\left[1+\left(2\frac{ISL}{ISH}\right)^{N_{eff}} e^{V_j/V_T}\right]^{1/N_{eff}}} \tag{4-28}$$

where

$$Neff = \frac{1}{\frac{1}{NL}-\frac{1}{NH}}. \tag{4-29}$$

In (4-28), i_L is the low level injection current that takes the form of (4-7), and ISL, ISH, NL, and NH are the saturation currents for the low- and high-level injection regions and the corresponding emission coefficients, respectively. Each current component's saturation current I_S is also a function of temperature. Their relationships have the following form:

$$I_S(T) = I_S(TNOM) \cdot \left(\frac{T}{TNOM}\right)^{XTI} \cdot e^{\left[\left(\frac{T}{TNOM}\right)-1\right]\cdot\left(\frac{EG}{N\cdot VT}\right)} \tag{4-30}$$

where XTI is the saturation current temperature exponent for each current component, and N is the temperature dependent emission coefficient for each current.

The extraction sequence for PiN diodes is similar to the one used for Schottky/JBS diodes, which begins with the selection of the semiconductor material type as well as the test fixture temperature. Again, two commercial semiconductor curve tracers are used to aid in the parameter extraction process. The upper-left graph of Figure 4-12 shows the diode current versus diode voltage on a logarithmic scale for the low-current range, which is used to extract parameters ISR, NR, and XTIR from the depletion region recombination range; and ISL, NL, and XTIL from the low-level injection range. The measured data are loaded and plotted in the graph using the "File" pull-down menu by selecting the "Load Low LN Curve" option from the "Load" submenu. The upper-right graph shows the diode current versus diode voltage for the high-current range, which is used to extract parameters ISH, NH, and XTIH from the high-level injection range; ISE, NE, and XTIE from the emitter recombination range; and V_J and R_S from the series resistance range. Similarly, the measured data are loaded and plotted in the graph using the "File" pull-down menu by selecting the "Load single IV curve" option from the

"Load" submenu. The top two graphs are for the test fixture temperature shown highlighted in the table. As described for the extraction techniques used in the JBSMSR program, the extraction is performed for each temperature first, and the extracted parameters are displayed in the table as shown in Figure 4-12. The temperature coefficients and exponents are then extracted using two different methods: the Linear Equation and the Gauss-Newton Algorithm, which have been described in detail in the JBSMSR program. Finally, all the extracted parameters are displayed in the parameter list located on the right-side of the sub-panel as shown in Figure 4-12.

4.3.2 Reverse Recovery Characteristic

The bottom half of the sub-panel as shown in Figure 4-12 is used for the parameter extraction program of **Reverse Recovery** for PiN diodes, which enables accurate model parameter extraction of C_{J0}, C_P, and three time-related parameters: TT, TSW, and TM due to the role of minority carriers in the intrinsic region as discussed in [29]. The reverse recovery measurements are performed using the same test system as the one used for Schottky/JBS diodes. The measured data are loaded and plotted in the bottom two graphs using the "File" pull-down menu by selecting the "Load Single RR Curve" option from the "Load" submenu. The buttons of "di/dt, CJ0, and CP" are used to extract the values for the di/dt rate, C_{J0} and C_P, respectively, in the same way as described in the JBSMSR program. The buttons of "TT, TSW, and TM" are used to extract the values for TT, TSW, and TM from the corresponding range as shown in Figure 4-12. All the extracted values are displayed in the table located at the bottom of the sub-panel.

4.3.3 Model Parameters for PiN diodes

Table 4-2 shows the complete model parameters employed for PiN diodes in the Saber template. The model parameters highlighted in yellow are used for the forward conduction range; the parameters highlighted in blue are used for C-V measurement; and the parameters highlighted in light green are used for the reverse blocking range.

Table 4-2 Complete model parameters for PiN diodes

PiN			
Parameter	Parameter Name	Extraction Characteristic	PiN
RS	Forward series contact resistance	High to medium current on-state slope	x
ISR	Low-level recombination saturation current	Low current on-state region	x
NR	Low-level ideality factor	Low current on-state region	x
ISL	Low-level injection saturation current	Low current on-state region	x
NL	Low-level injection emission coeffcient	Low current on-state region	x
ISH	High-level injection saturation current	Low to medium current on-state region	x
NH	High-level injection emission coeffcient	Low to medium current on-state region	x
ISE	Emitter recombination saturation current	Low dv/dt reverse recovery current dependence	x
NE		Low dv/dt reverse recovery current dependence	x
XTIR	ISR temperature exponent	Low current on-state vs. temperature	x
XTIL	ISL temperature exponent	Low current on-state vs. temperature	x
XTIH	ISH temperature exponent	Low to medium current on-state vs. temperature	x
XTIE	ISE temperature exponent	Medium to high current on-state vs. temperature	x
TNR1	Linear NR temperature coefficient	Low current on-state vs. temperature	x
TNR2	Quadratic NR temperature coefficient	Low current on-state vs. temperature	x
TNL1	Linear NL temperature coefficient	Low current on-state vs. temperature	
TNL2	Quadratic NL temperature coefficient	Low current on-state vs. temperature	
TNH1	Linear NH temperature coefficient	Low to medium current on-state vs. temperature	
TNH2	Quadratic NH temperature coefficient	Low to medium current on-state vs. temperature	
TNE1	Linear NE temperature coefficient	Medium to high current on-state vs. temperature	
TNE2	Quadratic NE temperature coefficient	Medium to high current on-state vs. temperature	

TRS1	Linear RS temperature coefficient	High to medium current on-state slope vs.temperature	x
TRS2	Quadratic RS temperature coefficient	High to medium current on-state slope vs.temperature	x
GAMMA	RS temperature exponent	High to medium current on-state slope vs.temperature	x
CJ0	Zero-bias junction capacitance	Capacitance-Voltage Or Reverse Recovery	x
TT	Charge decay parameter	Low current, low dv/dt reverse recovery tail current	x
TSW	Charge sweep out time	Low current, low dv/dt reverse recovery tail current	x
TM	Mid-region recombination time	Low current, low dv/dt reverse recovery tail current	x
BETA	TT temperature exponent	Low current, low dv/dt reverse recovery tail current vs. T	x
BETASW	TSW temperature exponent	Low current, low dv/dt reverse recovery tail current vs. T	x
BETAM	TM temperature exponent	Low current, low dv/dt reverse recovery tail current vs. T	x
BV	Breakdown Voltage	Reverse-bias breakdown region	x
IBV	Current at breakdown voltage	Reverse-bias breakdown region	x
k	Thermal R-G current coefficient	Reverse-bias region	x
TBV1	Linear BV temperature coefficient	Reverse-bias breakdown vs. temperature	x
TBV2	Quadratic BV temperature coefficient	Reverse-bias breakdown vs. temperature	x
TIBV1	Linear IBV temperature coefficient	Reverse-bias breakdown vs. temperature	x
TIBV2	Quadratic IBV temperature coefficient	Reverse-bias breakdown vs. temperature	x
TK1	Linear K temperature coefficient	Reverse-bias low-level vs. temperature	x
TK2	Quadratic K temperature coefficient	Reverse-bias low-level vs. temperature	x
TNBV1	Linear NBV temperature coefficient		x
TNBV2	Quadratic NBV temperature coefficient		x

4.4 Model Validation Results

The extracted model parameters are input into the power diode Saber template to construct power diode models for Schottky/JBS and PiN diodes. Figure 4-13 to Figure 4-17 show the comparison of measured (dashed) and simulated (solid) output characteristics over a temperature range from 25 ^{o}C to 150 ^{o}C for the 10 kV SiC JBS

diode, the 600 V SiC Schottky diode, the 10 kV SiC PiN diode, the 45 V Si Schottky diode, and the 600 V Si PiN diode, respectively. Figure 4-18 to Figure 4-20 show the comparison of measured (red dashed) and simulated (black solid) junction capacitance for the 600 V SiC Schottky diode, the 10 kV SiC JBS diode, and the 45 V Si Schottky diode, respectively. Figure 4-21 and Figure 4-22 show the comparison of measured (dashed) and simulated (solid) reverse blocking characteristics over a temperature range from 25 ^{o}C to 175 ^{o}C for the 600 V SiC Schottky diode, and the 10 kV SiC JBS diode. Figure 4-23 to Figure 4-25 show the comparison of measured (dashed) and simulated (solid) reverse recovery at 25 ^{o}C for the 600 V SiC Schottky diode,10 kV SiC JBS diode, and the 10 kV SiC PiN diode, respectively.

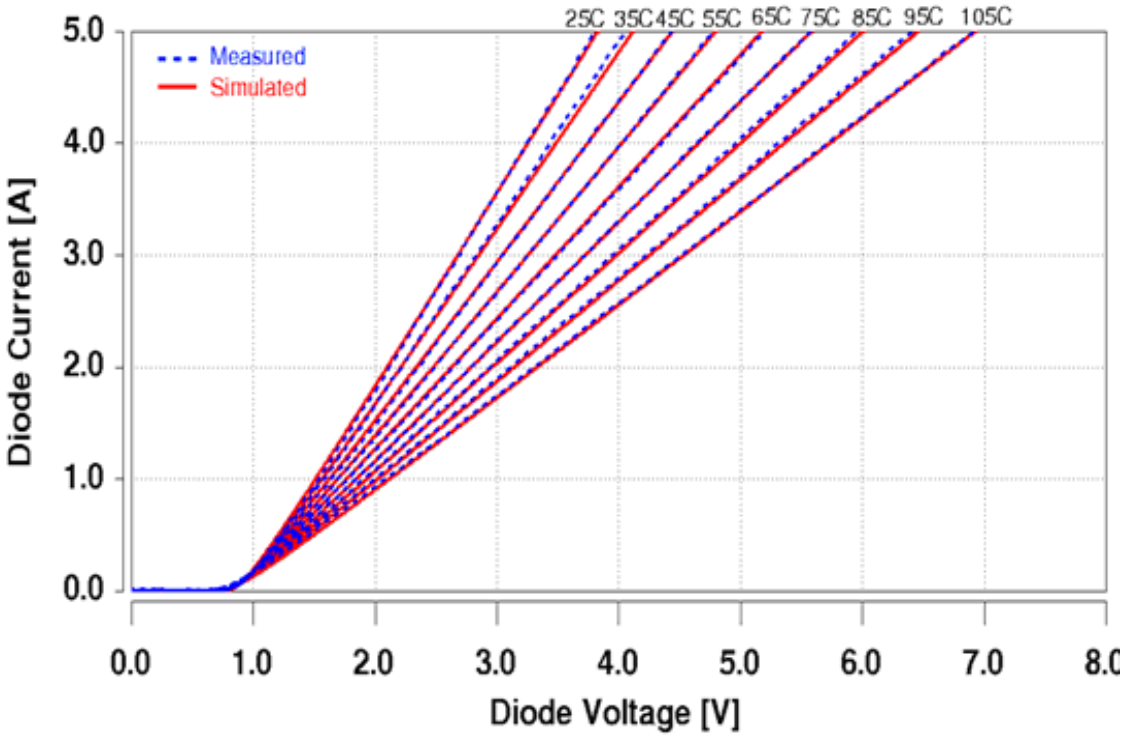


Figure 4-13 Comparison of measured (dashed) and simulated (solid) output characteristics at 25^{o}C, 35^{o}C, 45^{o}C, 55^{o}C, 65^{o}C, 75^{o}C, 85^{o}C, 95^{o}C, and 105^{o}C for a 10 kV, 5 A SiC JBS diode

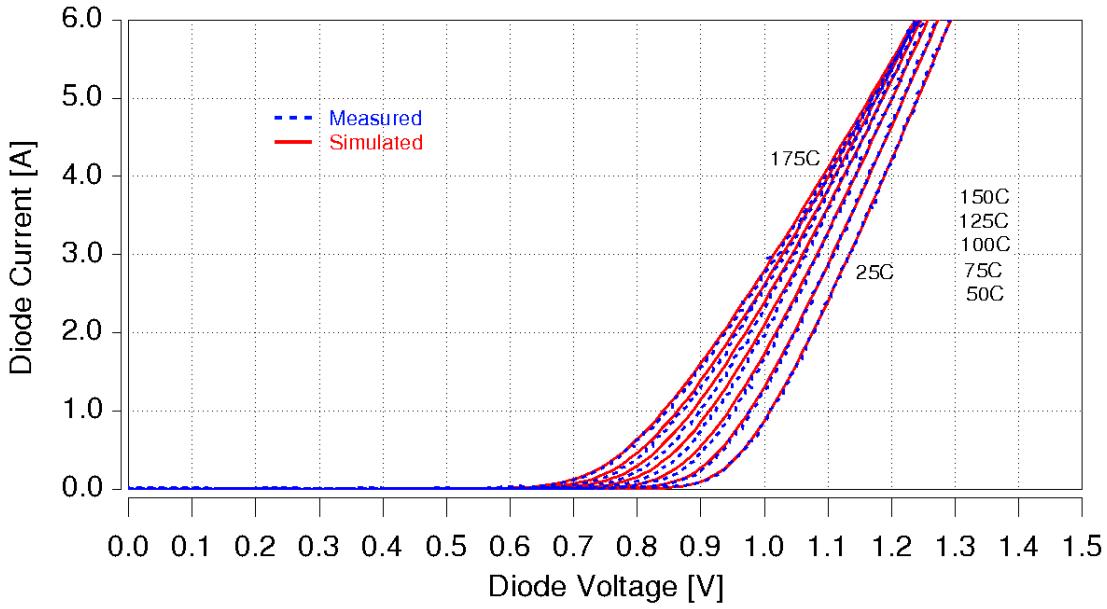


Figure 4-14 Comparison of measured (dashed) and simulated (solid) output characteristics at 25°C, 50°C, 75°C, 100°C, 125°C, and 150°C for a 600 V, 6 A SiC JBS diode

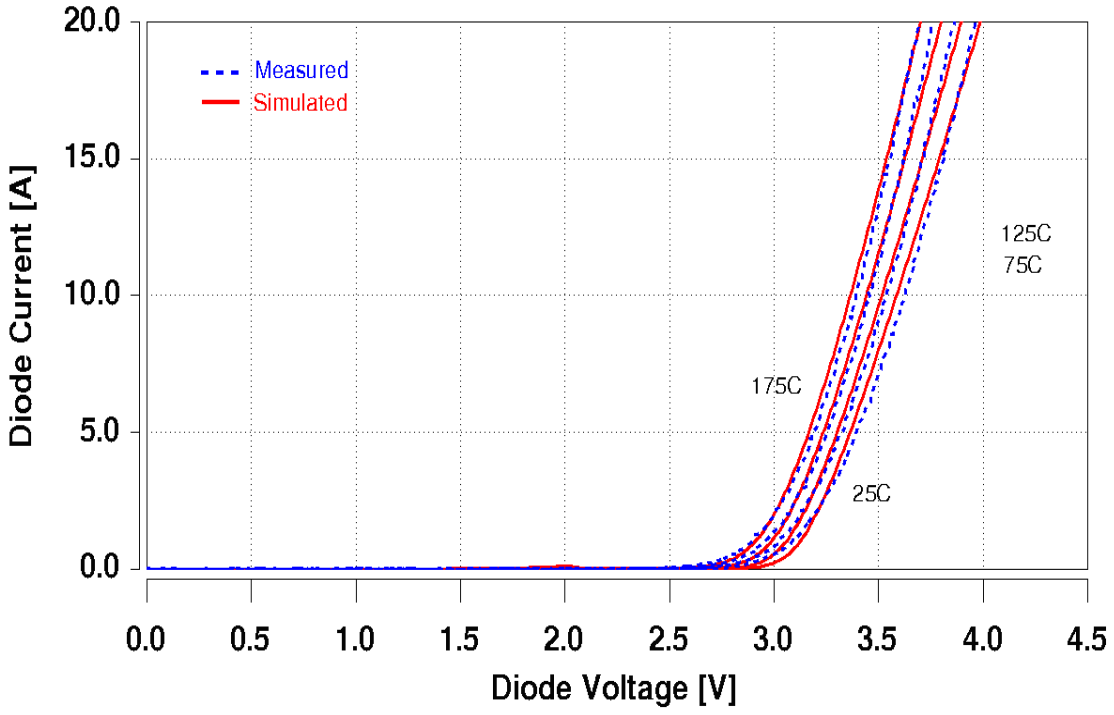


Figure 4-15 Comparison of measured (dashed) and simulated (solid) output characteristics at 25°C, 75°C, 125°C, and 175°C for a 10 kV, 20 A SiC PiN diode

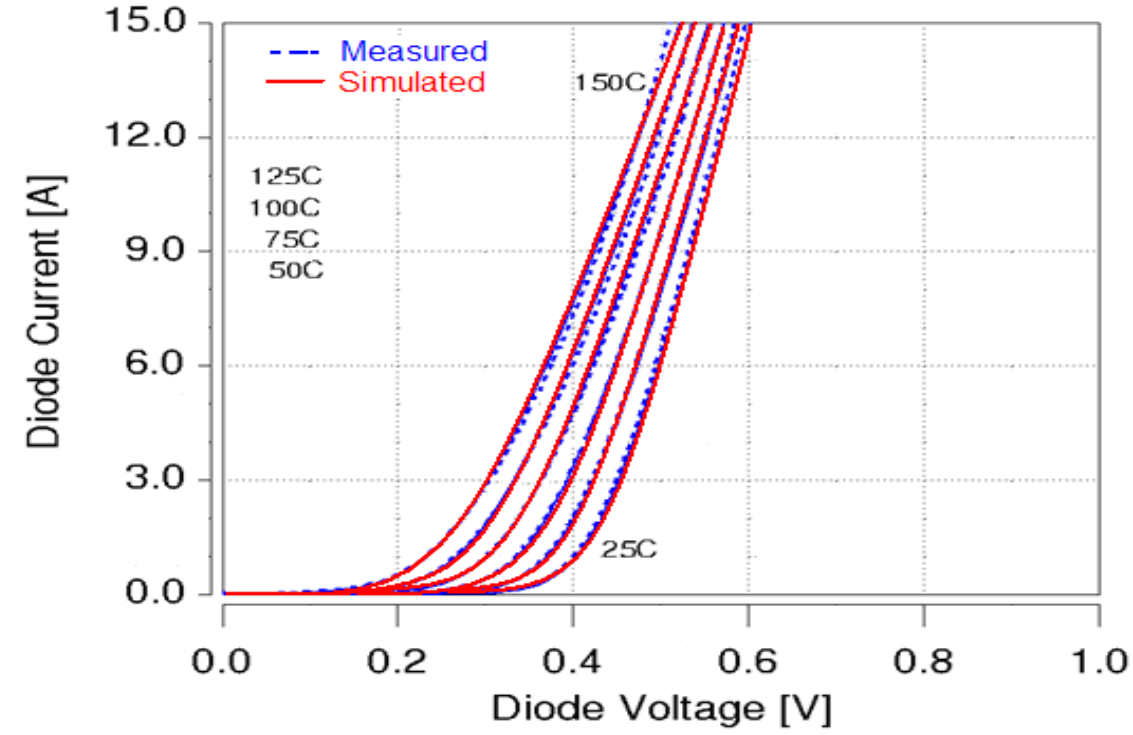


Figure 4-16 Comparison of measured (dashed) and simulated (solid) output characteristics at 25°C, 50°C, 75°C, 100°C, 125°C, and 150°C for a 45 V, 15 A Si Schottky diode

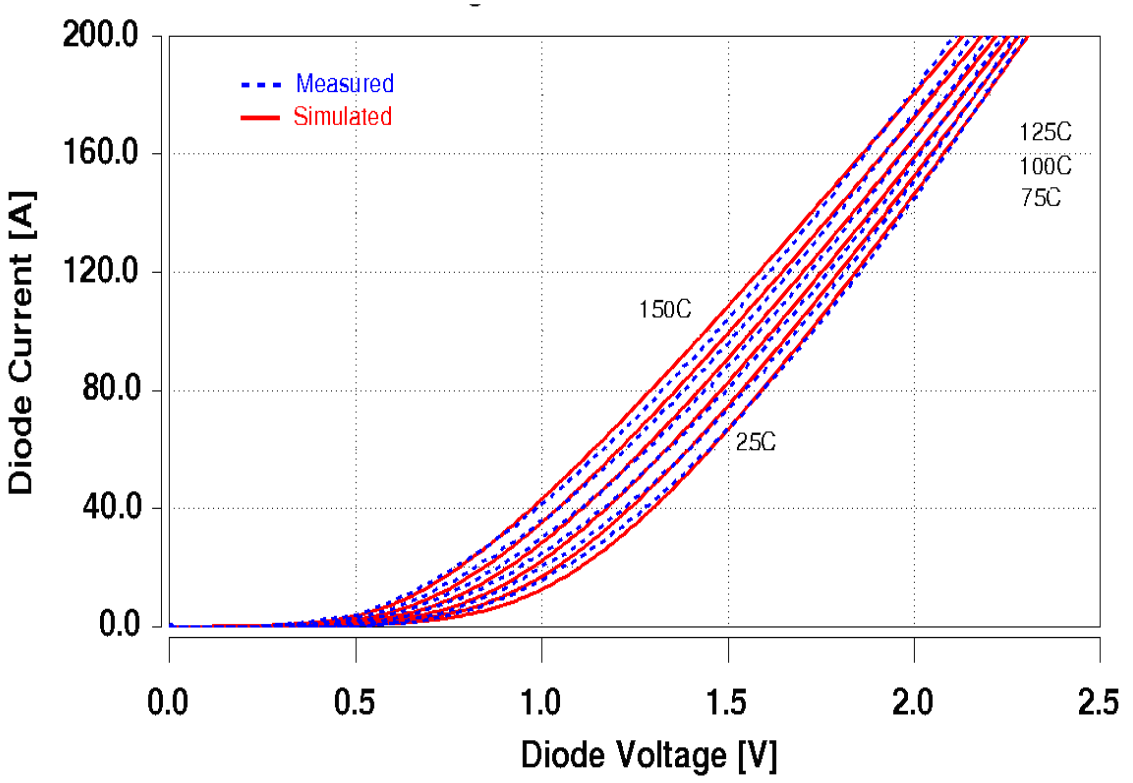


Figure 4-17 Comparison of measured (dashed) and simulated (solid) output characteristics at 25°C, 50°C, 75°C, 100°C, 125°C, and 150°C for a 600 V, 200 A Si PiN diode

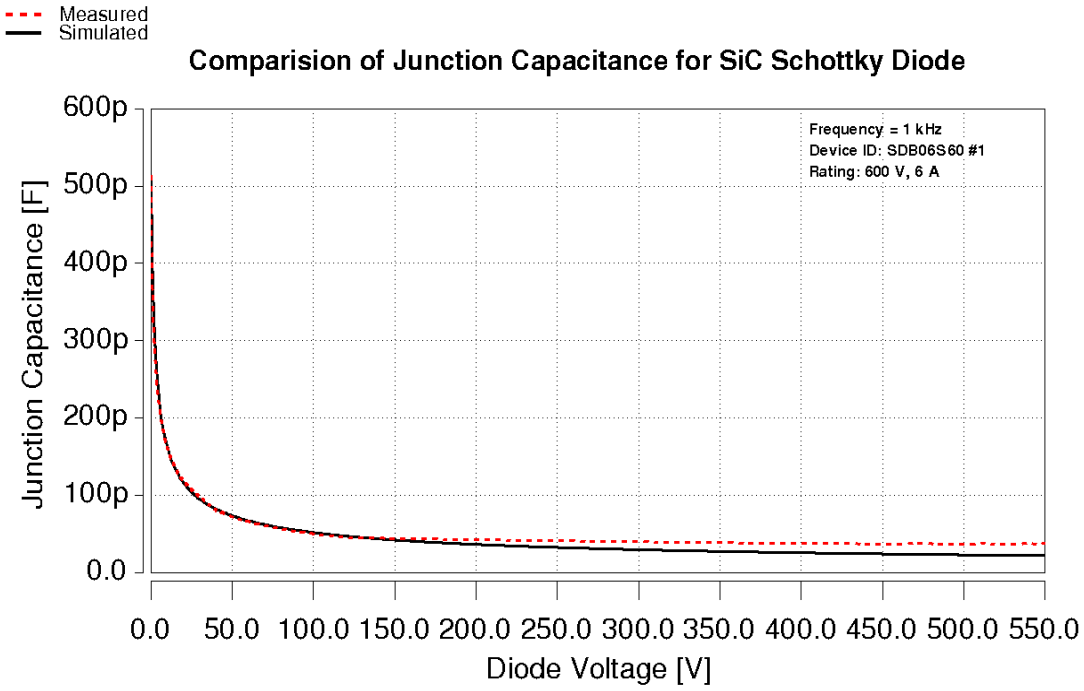


Figure 4-18 Comparison of measured (red dashed) and simulated (black solid) junction capacitance for a 600 V, 6 A SiC Schottky diode

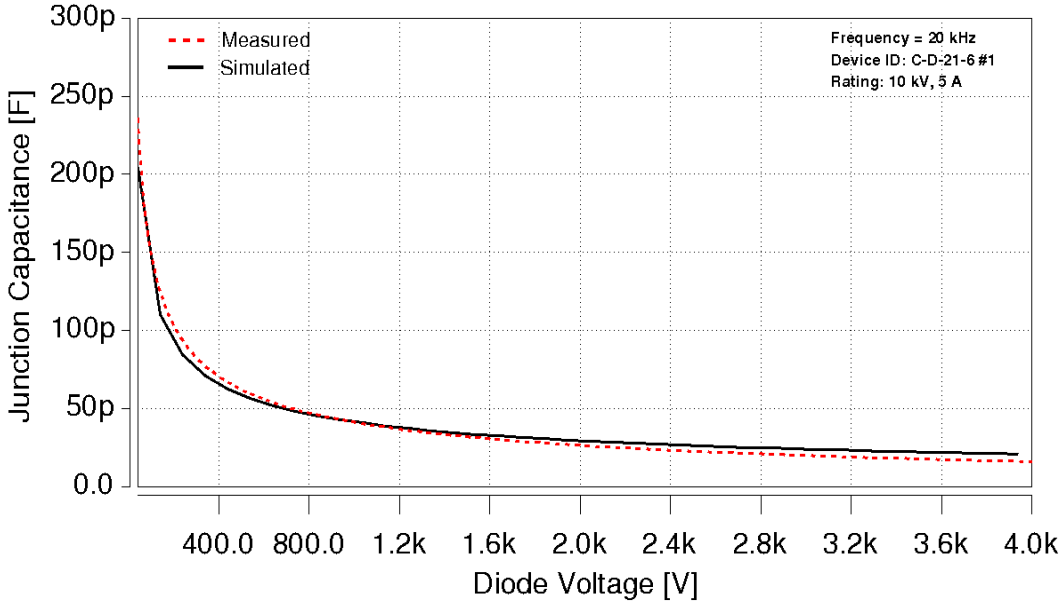


Figure 4-19 Comparison of measured (red dashed) and simulated (black solid) junction capacitance for a 10 kV, 5 A SiC JBS diode

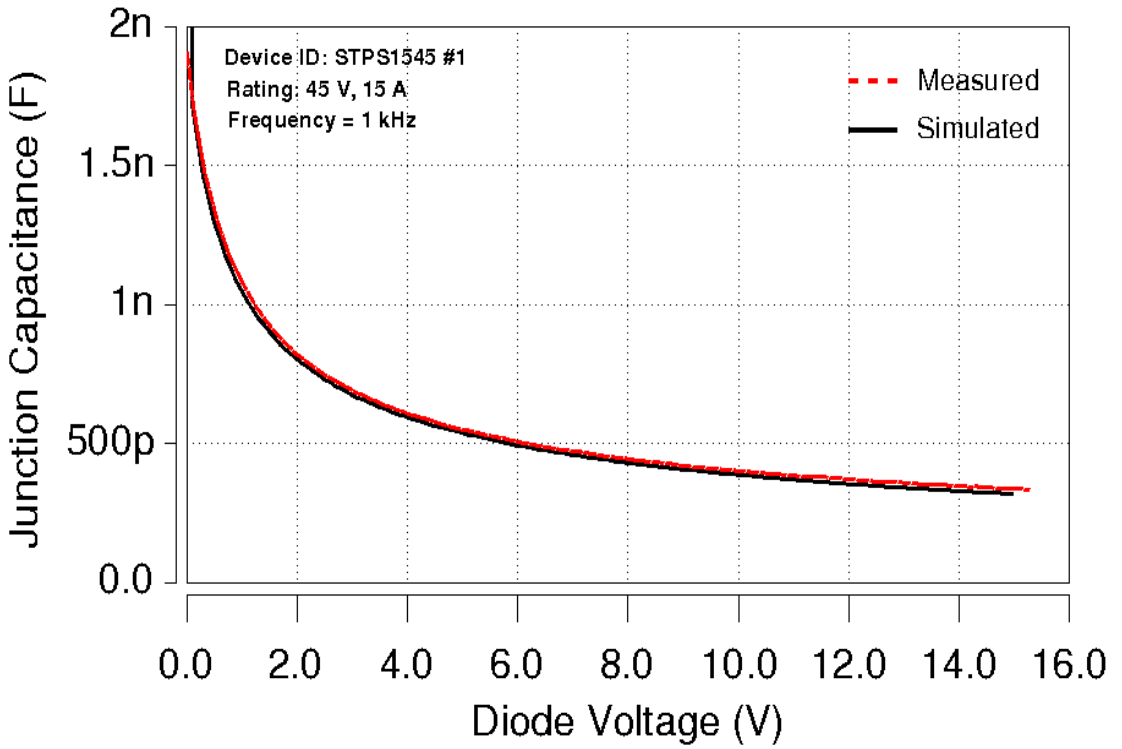


Figure 4-20 Comparison of measured (red dashed) and simulated (black solid) junction capacitance for a 45 V, 15 A Si Schottky diode

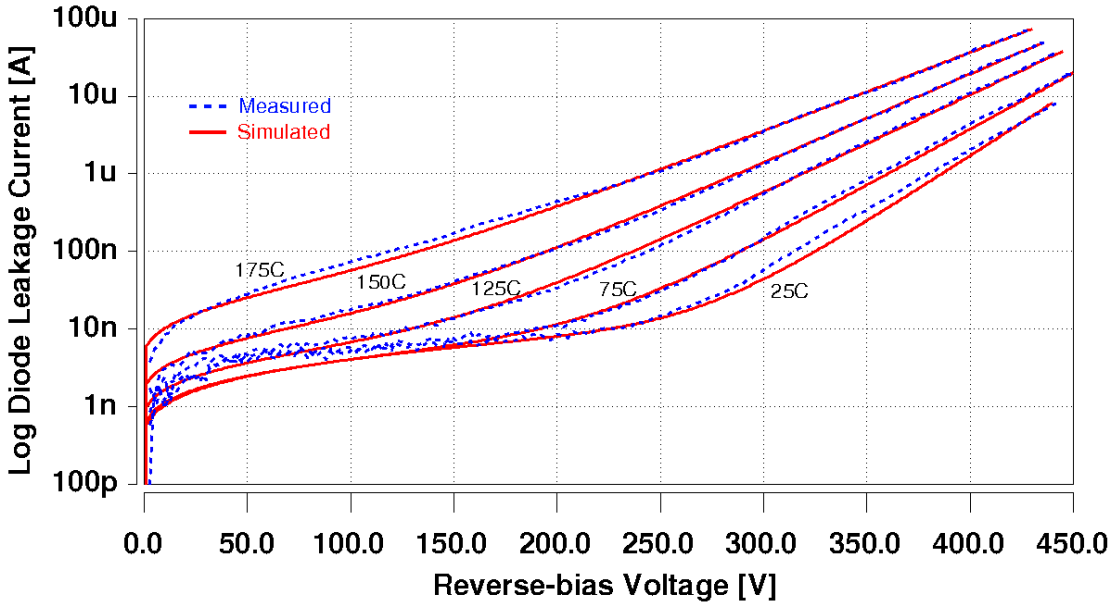


Figure 4-21 Measured (dashed) and simulated (solid) reverse-biased leakage for a 600 V, 6 A SiC Schottky diode in log scale at 25 ^{o}C, 75 ^{o}C, 125 ^{o}C, 150 ^{o}C and 175 ^{o}C

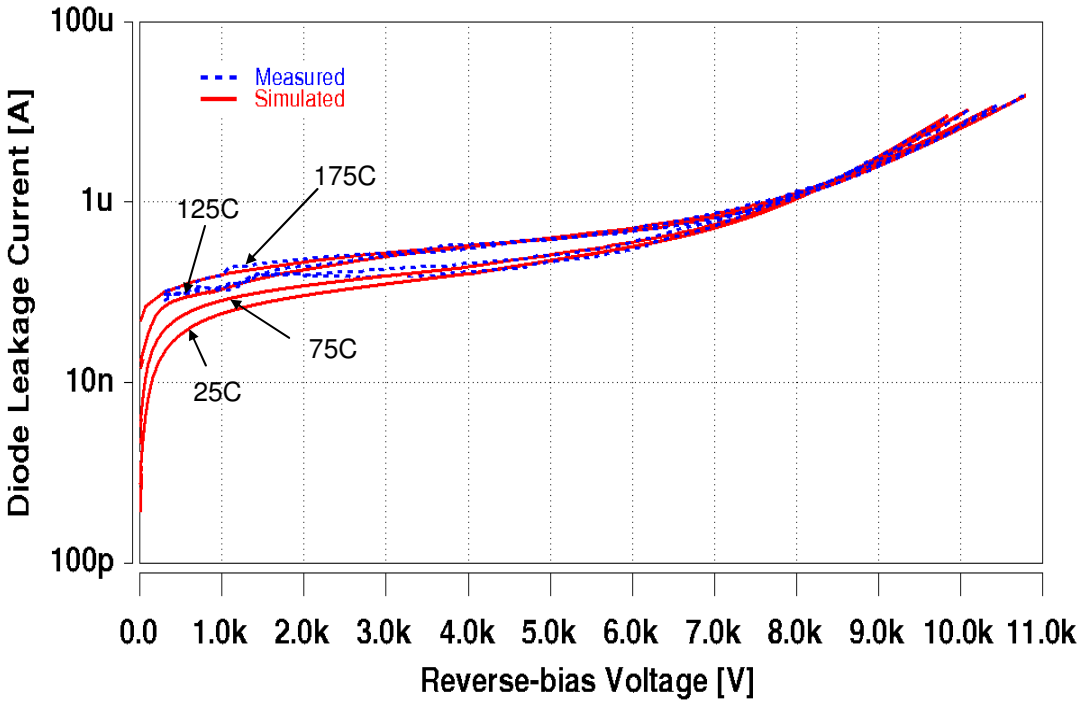


Figure 4-22 Measured (dashed) and simulated (solid) reverse-biased leakage for a 10 kV, 5 A SiC Schottky diode in log scale at 25 °C, 75 °C, 125 °C, and 175 °C

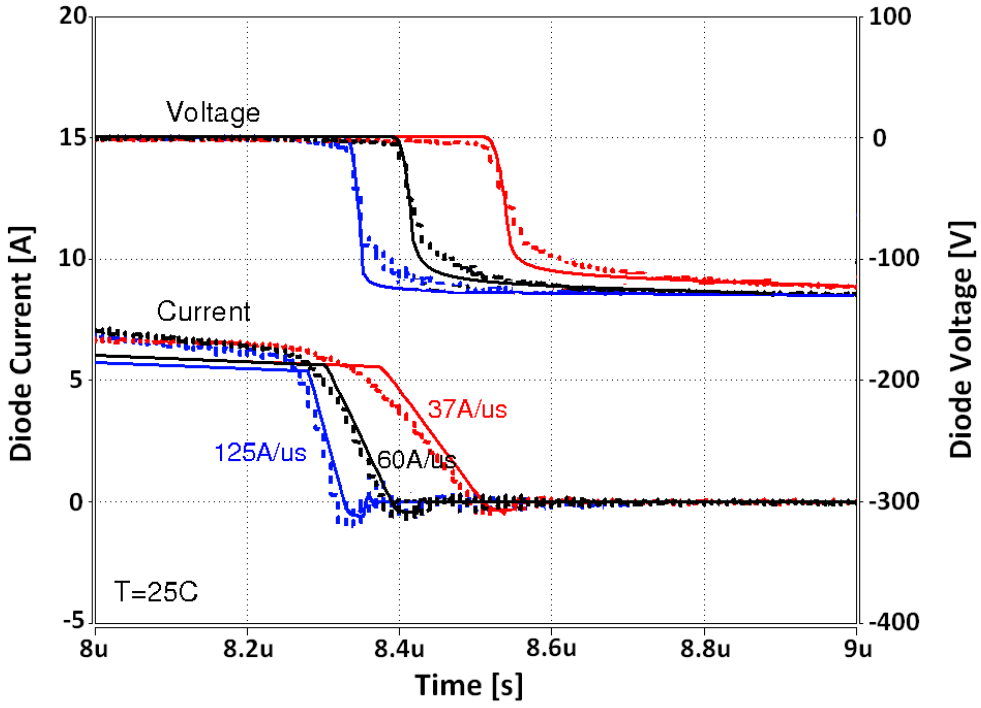


Figure 4-23 Comparison of measured (dashed) and simulated (solid) reverse recovery at 25 °C for a 600 V, 6 A SiC Schottky diode

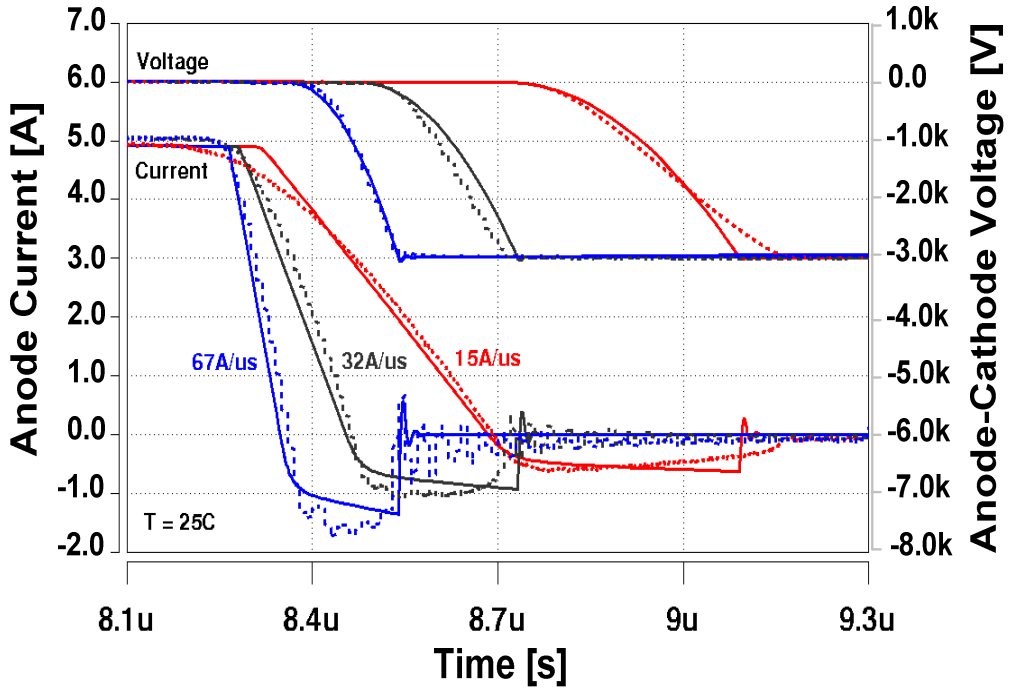


Figure 4-24 Comparison of measured (dashed) and simulated (solid) reverse recovery at 25 °C for a 10 kV, 5 A SiC JBS diode

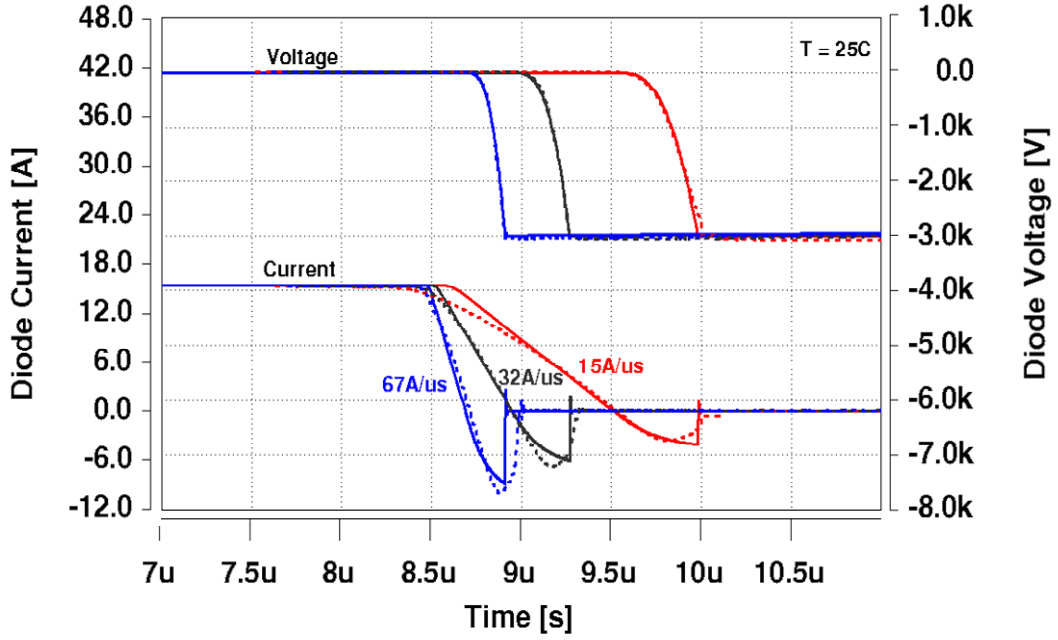


Figure 4-25 Comparison of measured (dashed) and simulated (solid) reverse recovery at 25 °C for a 10 kV, 20 A SiC PiN diode

4.5 Summary

In this chapter, the power diode models for Schottky/JBS and PiN diodes are presented, along with their parameter extraction using automated software called Diode Model Parameter Extraction Tools (DIMPACT), which consists of three programs: JBSMSR, MPSMSR, and PiNMSR. This program provides a method to automatically extract model parameter sets and rapidly construct power diode models for JBS, MPS, and PiN diodes.

The model theory for the reverse blocking characteristics of Schottky/JBS diodes is enhanced by adding physics-based equations. In the current power diode model in the Saber circuit simulator, an empirical approach was used to describe the low-bias reverse blocking region by introducing an effect called "conduction loss," a parameter that causes a linear relationship between the device voltage and current at low bias voltages, with no physics meaning [32]. Furthermore, this term is not sufficient to accurately describe the changes to the device characteristics as the junction temperature is varied. A more accurate model is required in order to adjust different systems, to fine tune the parameters of the energy management system, and to design power electronics system [33]. In this chapter, a new physics-based model of the reverse blocking characteristics for power Schottky/JBS diodes was developed by including the thermionic-emission mechanism in the low-bias range and was implemented in the Saber circuit simulator as an enhancement to the current power diode model. Comparison result between measured data, simulated data using current power diode model, and simulated data using enhanced power diode model shows the enhanced model achieves better accuracy than the current model.

The model validation results are demonstrated for a 600 V SiC Schottky diode, a 10 kV SiC JBS diode, a 10 kV SiC PiN diode, and a 600 Si PiN diode. The good agreements between measured data and simulated data prove the accuracy of the model parameters extracted using DIMPACT.

Chapter 5 Power MOSFET

The power MOSFET was developed in 1970s, which is widely used for medium power, fast-switching applications. With the availability of more advanced semiconductor material such as SiC, power MOSFETs could be used in high power application. Unlike BJT which has minority carrier modulation in its drift region, the power MOSFET is a unipolar device with current conducting via transport of majority carriers in the drift region, which will make power MOSFET suffer from high conductance loss. In this chapter, a new superjunction concept of MOS structure will be presented along with conventional vertical power MOSFET.

5.1 Vertical Power MOSFET

In Figure 5-1, the typical structure for a vertical power MOSFET is shown. The structure consists of a backside ohmic drain contact to an N+ substrate, a voltage-blocking epitaxial N- drift region, a p-base diffusion, an N+ source diffusion, gate oxide, a polysilicon gate, and source metallization. This device is often called a Double-diffused MOSFET (DMOSFET), because the p-base region and the N+ source regions are both diffused through a common window defined by the edge of the polysilicon gate.

As seen from Figure 5-1, for the conventional MOS transistor the pressure of the reverse-bias voltage will be sustained by the drift layer. In the case of conventional power MOSFET, the blocking capability is determined by the thickness and the doping concentration of the drift layer. There exists a tradeoff between on-resistance and voltage

blocking capability in the device design, and so the width and doping profile in the drift region vary with blocking voltage capability.

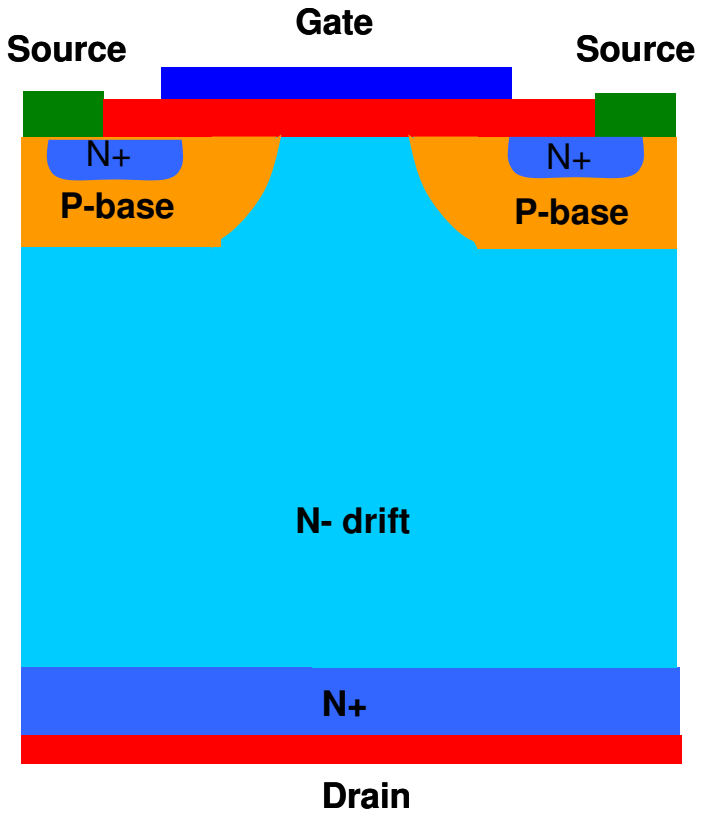


Figure 5-1 Cross-section of a conventional vertical power MOSFET

It can be seen from Figure 5-1 that there is a built-in diode inside the MOS structure which is recognized as body diode. This built-in body diode is in an anti-parallel configuration with the MOSFET between the source and drain. The body diode is formed by the p-base region (P), and the N- drift region (N). In some circuit design, the designer will use this body diode as a free-wheeling diode when operating the device in half- and full-bridge power circuits. Also, when fabricating the power MOSFET device, there is an inherent p-base contact to the source metallization. This design will prevent built-in

parasitic NPN bipolar transistor formed by N+ source, p-base, and N- drift region, which can slow MOSFET switching and lead to second breakdown.

The device operating principles of a vertical power MOSFET are similar to a low-voltage lateral MOSFET as described in [34]. When the device is under forward conducting condition, a MOSFET channel is formed at the semiconductor interface under the gate area; and electrons are flowing from the source region through the conducting channel, and down through the N- drift region to the drain contact. In this conducting process, the voltage drop across the N- drift region contributes the most to the total on-resistance.

Figure 5-2 illustrates the energy band diagram for a MOS structure with a P-type semiconductor. In Figure 5-2, E_C represents energy level of the conduction band, E_i represents the intrinsic energy level, E_V represents energy level of the valance band, $E_{F,M}$ is the Fermi level in the metal, $E_{F,S}$ is the Fermi level in the semiconductor, ϕ_M is the metal work function, χ and χ_0 are the semiconductor and oxide electron affinities, ϕ_B is the barrier height between the metal and the oxide, ψ_S is the surface potential in the semiconductor, and ψ_B is the potential difference between the intrinsic and Fermi levels in the semiconductor. In Figure 5-2 (a), the MOS energy band diagram is shown under flatband conditions. Under flatband conditions, band bending does not exit as there is no influence from gate bias.

Figure 5-2 (b) shows the accumulation mode obtained by applying a negative gate bias. With a negative gate bias, positive charges are attracted to the channel surface creating an accumulating of positive charges in the P-type semiconductor region, which forces the edge of the valence band to be bent closer to the Fermi level.

Figure 5-2 (c) depicts the energy band diagram for the case of a small positive gate bias applied to the gate such that positive charges are repelled from the semiconductor surface. Under this condition, the whole region will got depleted and a surface depletion layer will form under the gate area. The condition described in Figure 5-2 (c) represents the P-base region shown in Figure 5-1.

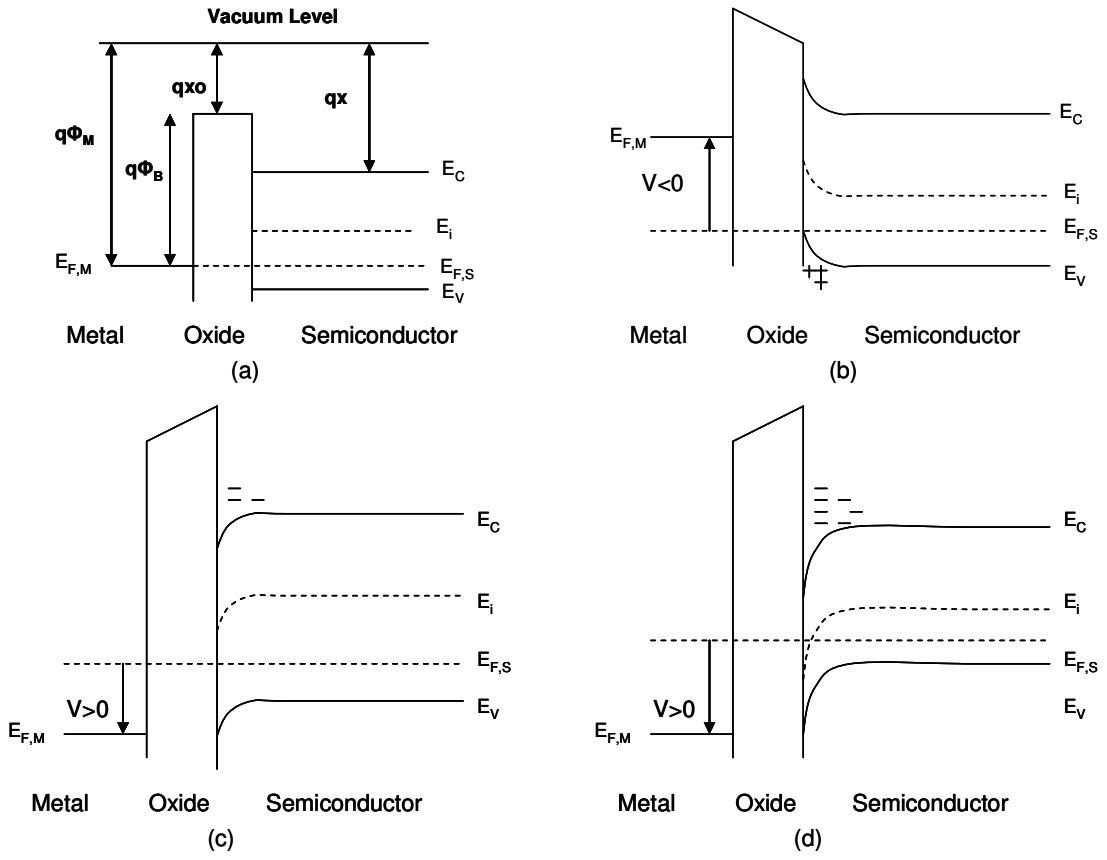


Figure 5-2 Energy band diagram for a MOS structure with a P-type semiconductor under flatband condiction (a), negative gate bias or accumulation mode (b), under positive gate bias forming a depletion layer in the channel (c), and for increased positive gate voltage forming an inversion layer in the channel (d)

Figure 5-2 (d) illustrates the energy band diagram for larger gate biases, such that enough electrons are attracted to the surface to form an inversion layer. When this happens, the band bending increases to an end where the intrinsic level is now below the

Fermi level at the surface, which is expected for an N-type region. When the electron density is low, the intrinsic level is close to the Fermi level in the semiconductor, and the condition is know as weak inversion, whereas further separation of the intrinsic level and Fermi levels results in a high electron density and strong inversion.

5.1.1 On-state Characteristics

Figure 5-3 shows the cross-section view of a vertical power MOSFET under forward conduction condition. It can be seen that electrons are conducting in most part of the drift region below the P-base. Typical output characteristics of the power MOSFET are shown in Figure 5-4, which consist of the cutoff-region, linear region, and a saturation region.

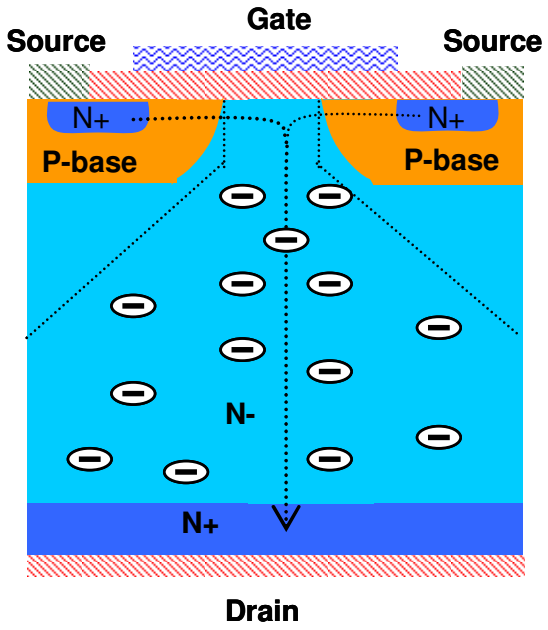


Figure 5-3 Cross-section view of a vertical power MOSFET when forward conducting

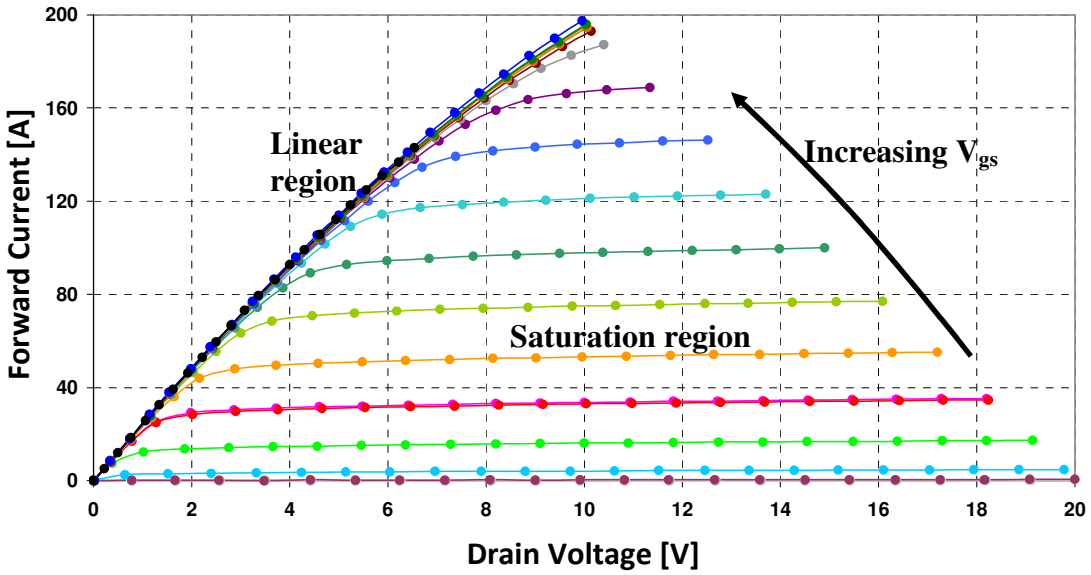


Figure 5-4 Typical on-state characteristics of a power MOSFET

The linear region occurs for low values of V_{ds} and $V_{gs} \geq V_T$ (Threshold voltage). In this region, the channel starts in weak inversion and then progresses to strong inversion as V_{gs} increases. In general, the channel is now highly conductive, as electrons can flow from the source through the drift region to the drain region. The series resistance encountered by the electrons is depicted in Figure 5-5 [18]. In high-voltage power devices, the linear region is mainly dominated by the voltage drop across the drift region due to the thickness and the low doping properties in this region. There are other resistances that contribute to the total on-resistance include the contact resistances; the resistance in the N+ source region, in the conducting channel, and in the N+ substrate; and the JFET resistance from the pinch-off effect due to adjacent depletion regions.

When V_{ds} increases, the current starts to saturate without increasing. Higher V_{gs} tends to have higher saturation current as shown in Figure 5-4.

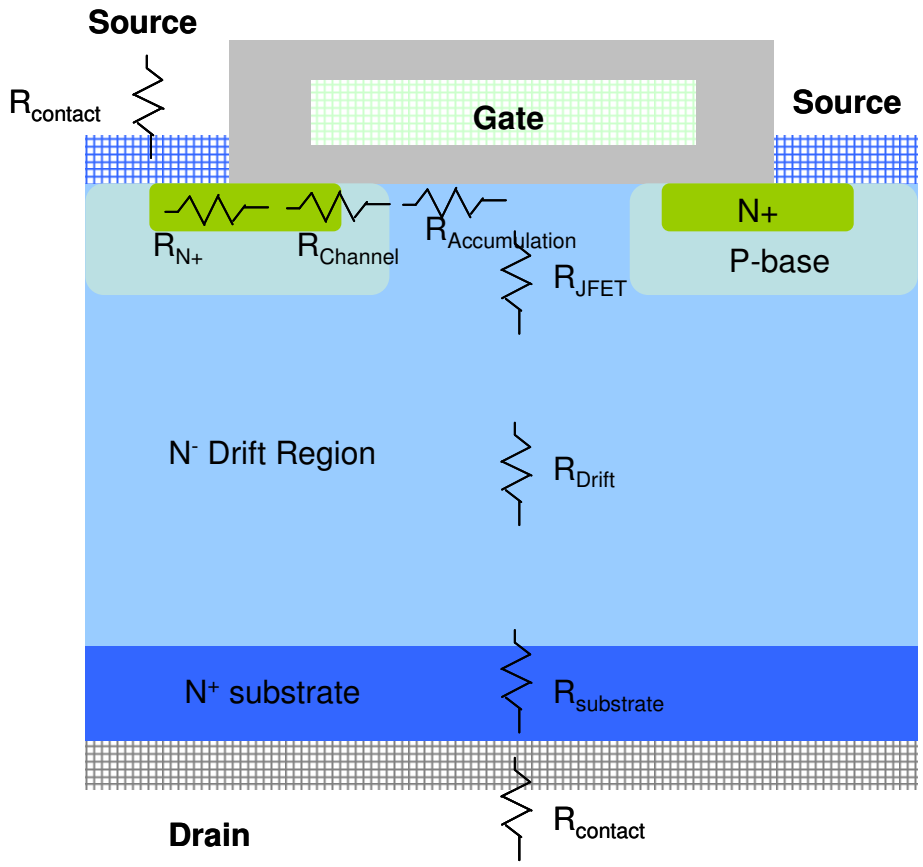


Figure 5-5 On-state series resistances or vertical power MOSFET

5.1.2 Transient Characteristics

The inter-electrode capacitances of power MOSFET type devices are very important in modeling its switching behaviors accurately, especially when investigating the effect of the variation of the gate-drain capacitance (C_{gd}), which dominates the output switching waveforms due to the "Miller" effect. At NIST, a new test system was built to measure all three inter-electrode capacitances: C_{gd}, the gate-source capacitance (C_{gs}), and the drain-source capacitance (C_{ds}) with both gate-sweeping and drain-sweeping [39].

The circuit layout for the HV CV apparatus is shown in Figure 5-6. Figure 5-6 (a) shows the main CV system, which attaches to the circuit shown in Figure 5-6 (b) at

terminals CM1 and CM2. The main CV system consists of six connection terminals (CM2', DUT1, SG, VdRef, Drain, and DUT2) that are used to generate the three capacitance measurement configurations for C_{gd}, C_{ds}, and C_{gs}.

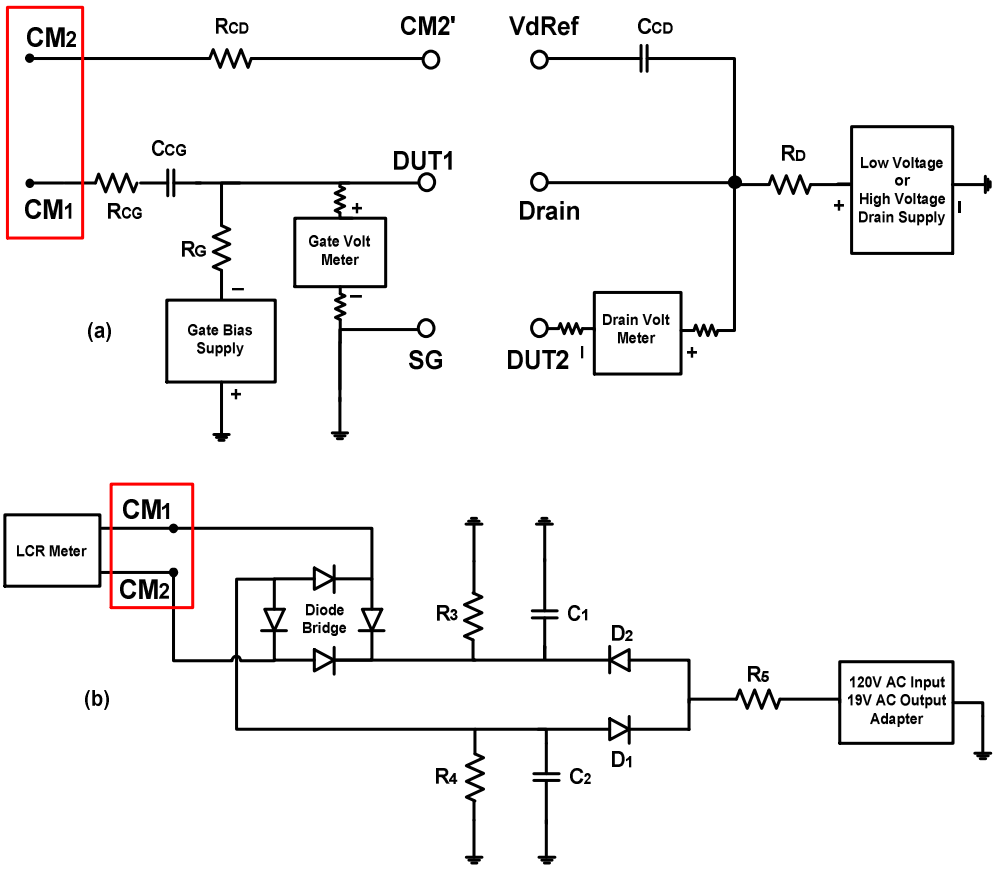
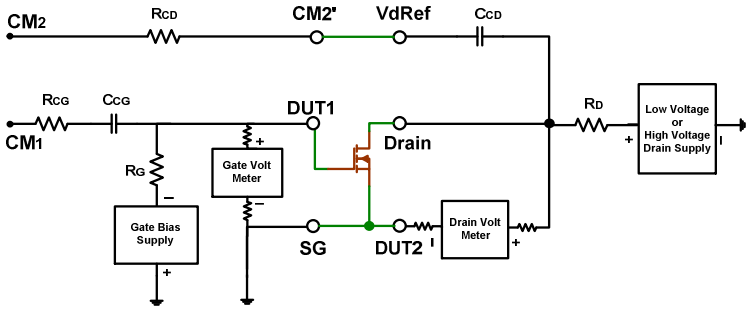
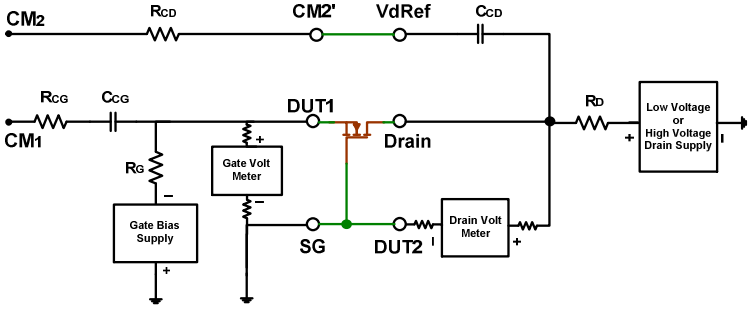


Figure 5-6 High voltage C-V circuit: main circuit showing terminal points, voltage supply, voltage meter and DC blocking capacitors (a); hookups to LCR meter and bridge rectifier (b)

Figure 5-7 shows the three capacitance measurement configurations, including (a) C_{gd}, (b) C_{ds}, and (c) C_{gs}, respectively. These three configurations enable the flexibility to accurately measure three different forms of capacitance in three terminal devices with a high impedance switch input.



(a)



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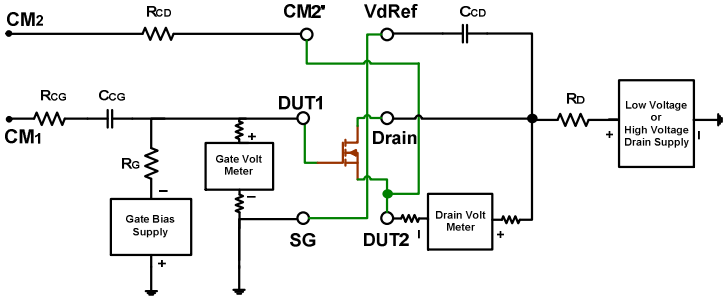
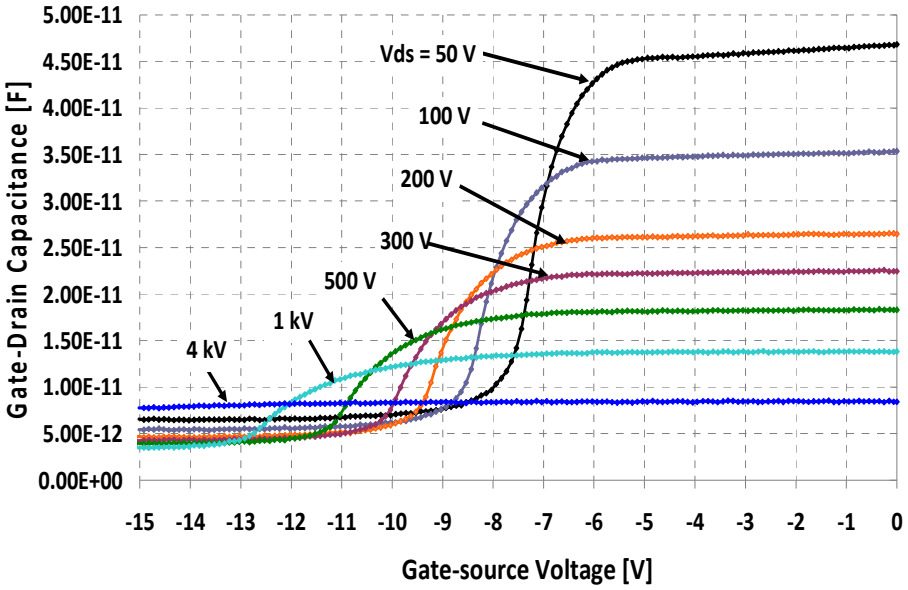


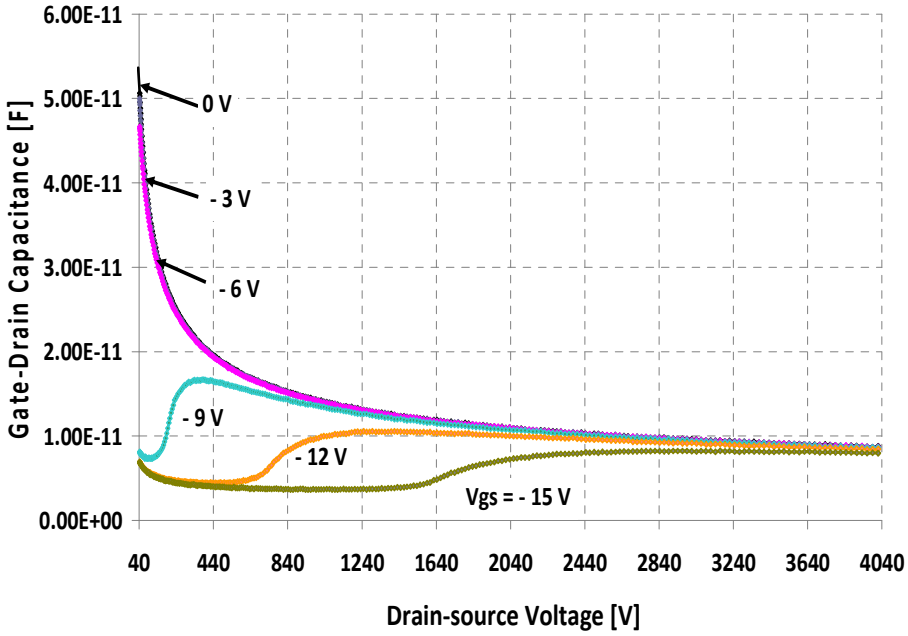
(c)

Figure 5-7 The three capacitance measurement configurations: C_{gd} (a), C_{ds} (b), and C_{gs} (c)

Figure 5-8 (a) shows the measured C_{gd} versus V_{gs}; and Figure 5-8 (b) shows the measured C_{gd} versus V_{ds} for a 10 kV SiC power MOSFET.



(a)



(b)

Figure 5-8 Measured gate-drain capacitance versus gate-source voltage (a); versus drain-source voltage (b) for a 10 kV SiC power MOSFET

Figure 5-9 shows the measured C_{ds} versus V_{ds} for a 10 kV SiC power MOSFET. Figure 5-10 shows the measured C_{gs} versus V_{gs} by stepping V_{ds} for a 10 kV SiC power MOSFET.

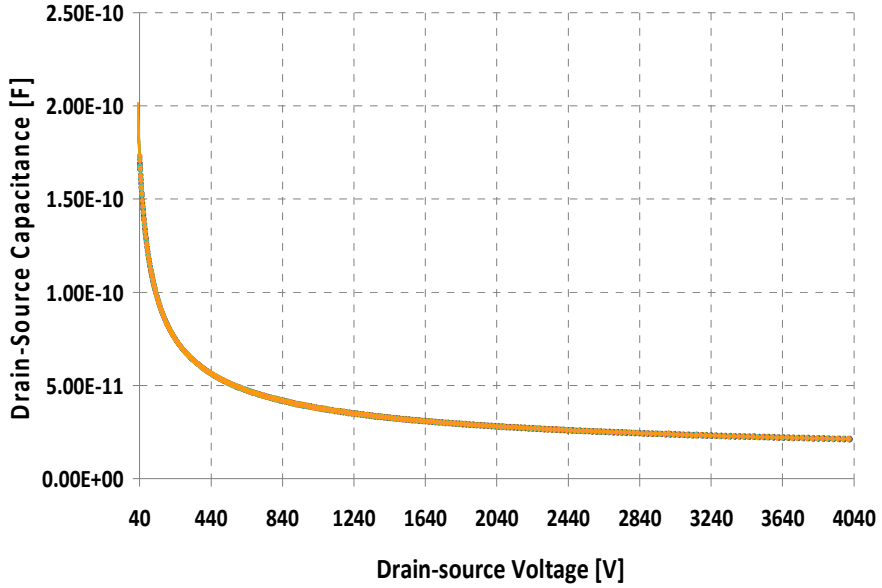


Figure 5-9 Measured drain-source capacitance versus drain-source voltage for a 10 kV SiC power MOSFET

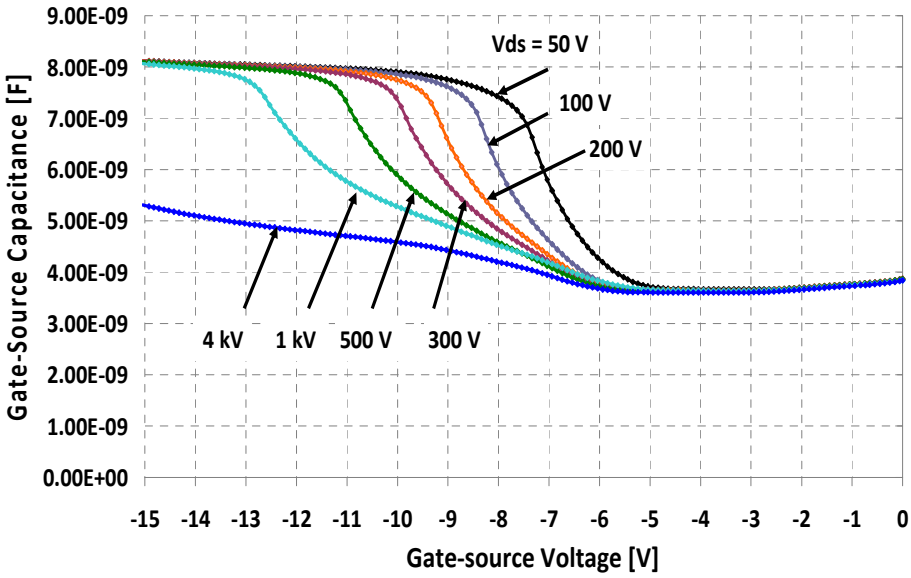


Figure 5-10 Measured gate-source capacitance versus gate-source voltage for a 10 kV SiC power MOSFET

5.2 CoolMOS™ Transistor

A new device concept named the superjunction device, CoolMOS™ has been proposed [40]. The CoolMOS™ transistor was introduced as an alternative device to provide the fast switching speed of power MOSFETs while also reducing the on-resistance by a factor of 5 [40] compared to conventional MOSFETs in the 500 V to 1200 V range. CoolMOS™ virtually combines the low switching losses of a MOSFET with the on-state losses of an IGBT. Figure 5-11 shows the cross-sectional drawing of the CoolMOS™ transistor and includes a diagram of the internal capacitances of the device. As shown in Figure 5-11, the drift region of the CoolMOS™ transistor is formed with a combination of vertical n- and p- strips [40, 41] rather than the constant n- region of the conventional power MOSFET. CoolMOS™ transistors serve as the main switching devices in many high efficiency soft-switching converter applications [42, 43]. Utilization of a CoolMOS™ device rather than an IGBT also allows synchronous rectification during the reverse conducting period and achieves fast turn-off without tail current. Recent work also considers a hybrid soft switching module approach consisting of an IGBT in parallel with a CoolMOS™ transistor.

Not only has the new technology achieved breakthrough at reducing on-resistance, but new benchmarks have also been set for the device capacitances. Due to chip shrink and novel internal structure, the technology shows both, a very small input capacitance as well as a strongly nonlinear output capacitance.

Due to the advantages described above, the CoolMOS™ transistor is employed in the inverter design of the electrical vehicle project as one of the main switches.

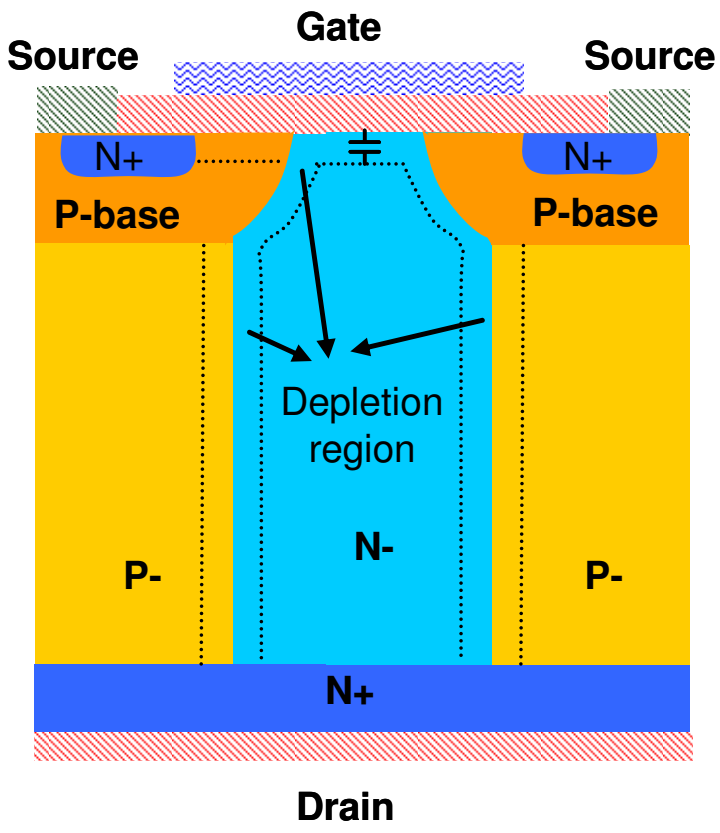


Figure 5-11 Cross-section of the CoolMOS™ transistor

5.2.1 IV - characteristics

Like the conventional power MOSFET, in the on state, electrons flow from the source, under the gate electrode, through the conduction channel, and through the drift region, to the drain terminal as shown in Figure 5-12. Also, for CoolMOS™ due to the presence of p-strips, the current conducting channel in the drift layer is confined between the p-strips as depicted in Figure 5-12. Although the conducting channel in the drift layer is narrower than the one in conventional power MOSFET. The on-resistance for CoolMOS™ is much lower than the one for regular power MOSFET because of the high doping concentration in the drift region. The unique super junction structure of CoolMOS™

makes it possible to have high doping concentration in the drift layer without sacrificing the blocking capability as limited in the conventional power MOSFET.

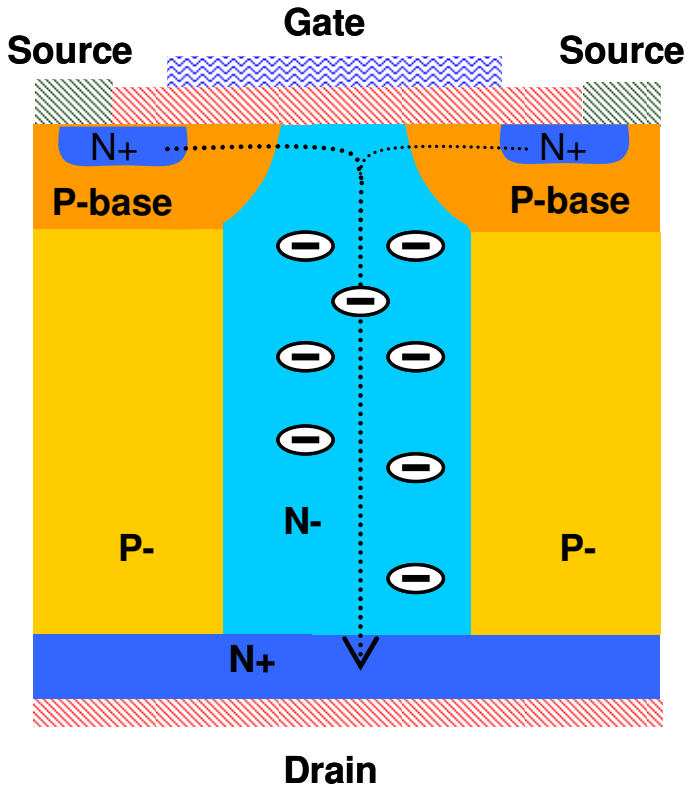


Figure 5-12 Cross-section view of forward conducing conduction

The output characteristics of the power MOSFET are shown in Figure 5-13, which consist of the cutoff-region, linear region, and a saturation region which are similar to the conventional power MOSFET. For higher V_{gs}, the current does not saturate completely, but undergoes a "partial" saturation and rises slowly with V_{ds}. It is also seen that, in this region, there is hardly any increase in the current with increasing V_{gs} (between $V_{gs} = 7V$ and $V_{gs} = 20V$ in Figure 5-13).

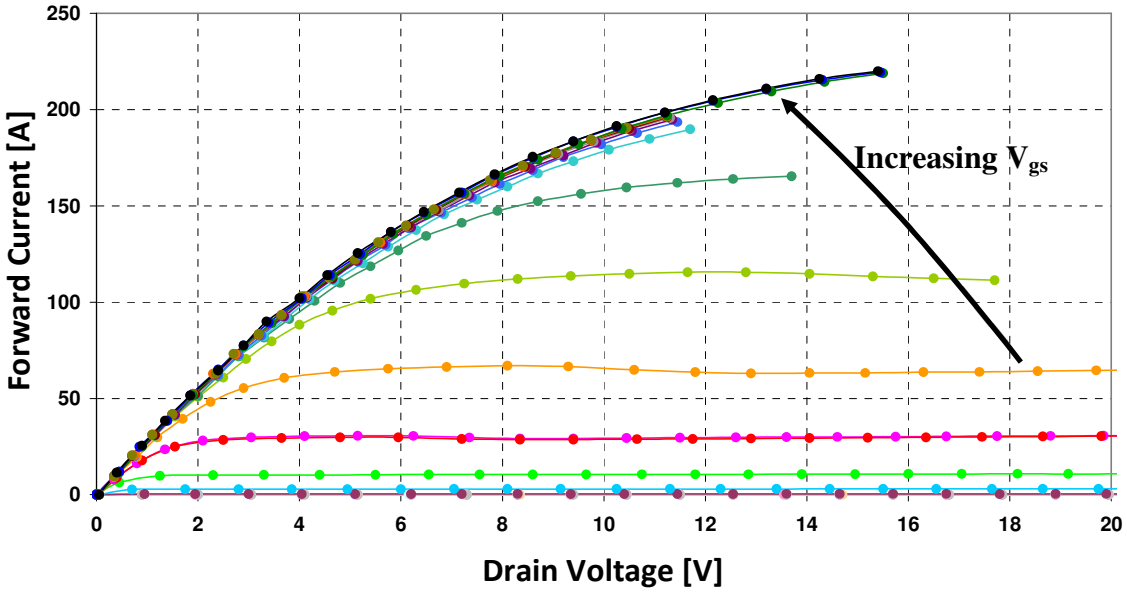


Figure 5-13 Forward conduction characteristics of 600 V Si CoolMOS

5.2.2 Transient characteristics

As described in the conventional power MOSFET, the inter-electrode capacitances of power MOSFET type devices are very important in modeling its switching behaviors accurately, especially C_{gd} which is also known as gate-transfer capacitance, which dominates the output switching waveforms. When the transistor is reverse biased, a lateral electric field is built up, which drives the charge towards the contact regions. Take a 600 V CoolMOS^{TM} device as an example, the space charge layer builds up along the physical pn-junction line and spreads at a voltage around 50 V across the whole p-/n-striped structure. The drift zone is now completely depleted and acts like the voltage sustaining layer of a PiN-structure. Due to this lateral depletion, the doping of the drift layer is rised by roughly one order of magnitude without sacrificing the blocking capability, which is a big improvement compared to the standard MOS transistor. Figure

5-14 illustrates cross-section of the CoolMOS™ transistor superimposed with inter-electrode capacitances.

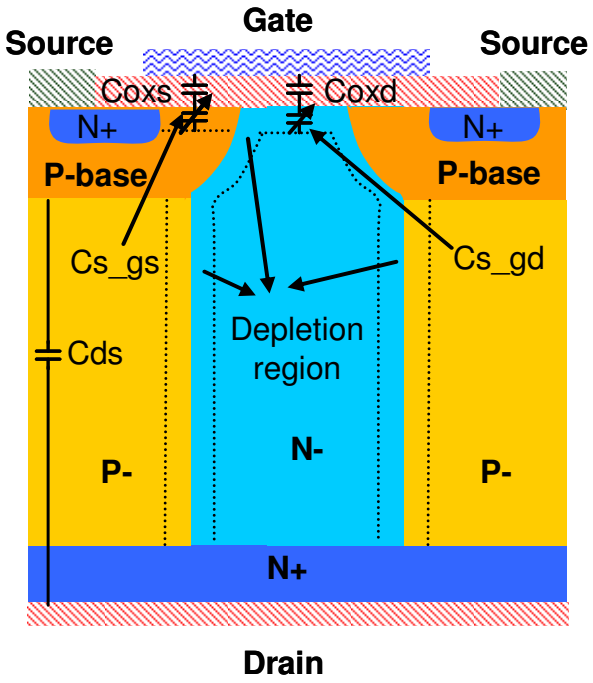


Figure 5-14 Cross-section of the CoolMOS™ transistor with inter-electrode capacitances model topology superimposed

The nonlinear spread of the space charge layer as a function of voltage can easily be observed in the characteristic output capacitance. Its main contribution is the drain/source capacitance (see Figure 5-15) [40]. Because the p strips are inserted into the drift region, the internal surface of the pn-junction is increased, which causes a large value of the capacitance at small voltages. By applying reverse bias voltage, the internal p/n- strips starts to deplete along the vertical depletion line as shown in Figure 5-14. When it starts to deplete, the surface area of the pn-junction will reduce and the depletion width will expand, both of which lead to a strongly nonlinear behavior of the output capacitance.

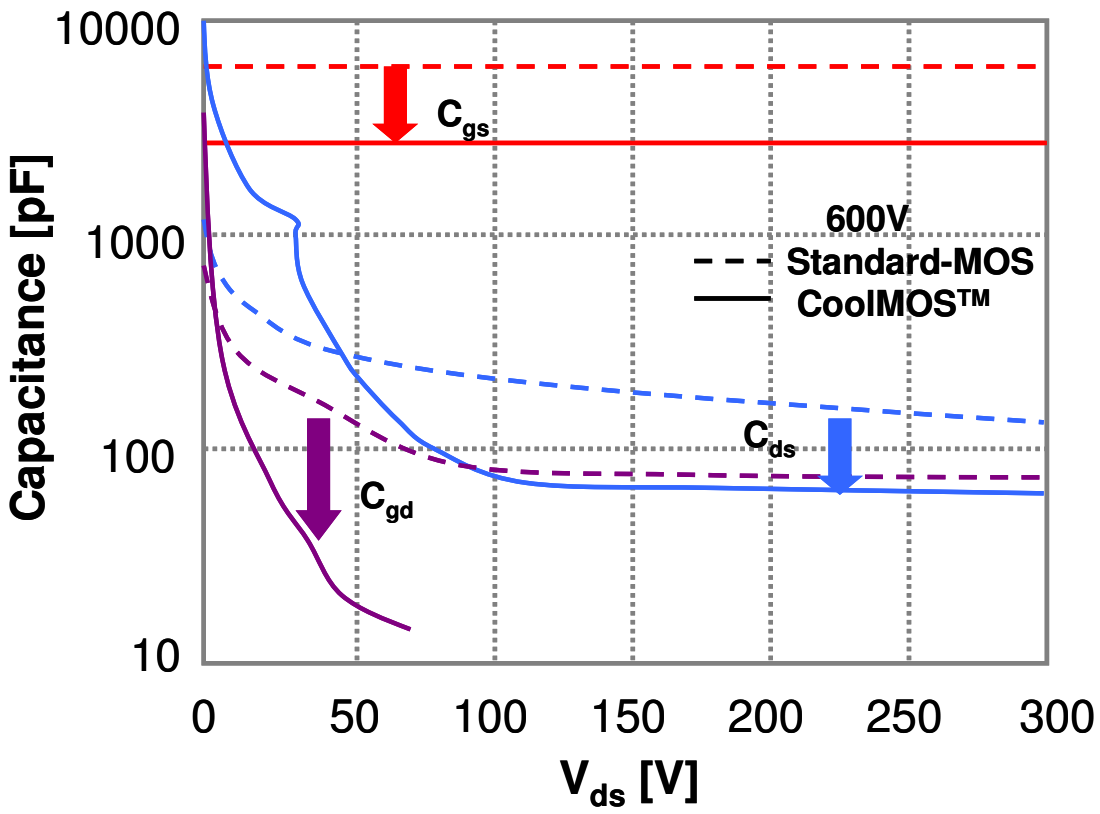


Figure 5-15 Inter-electrode capacitances comparison between CoolMOS™ and standard-MOS

Due to the immense reduction in the chip area, the CoolMOSTM transistor exhibits very low gate charge values in comparison with conventional technology which has the same on-resistance. As shown in equation (5-1), the gate charge Q_g is a measure of the driver power P_g required at a certain switching frequency f_{sw}: [40]

$$P_g = Q_g \cdot V_{gs} \cdot f_{sw} \tag{5-1}$$

As mentioned earlier, the output switching waveforms are determined by the charging process of the gate-transfer capacitance C_{gd} through the "Miller" effect. The lower the gate charge, the lower the switching losses. It can be seen from Figure 5-16, there is a drastic reduction of the gate charge for the CoolMOS™ technology resulting in low control power and high switching frequency.

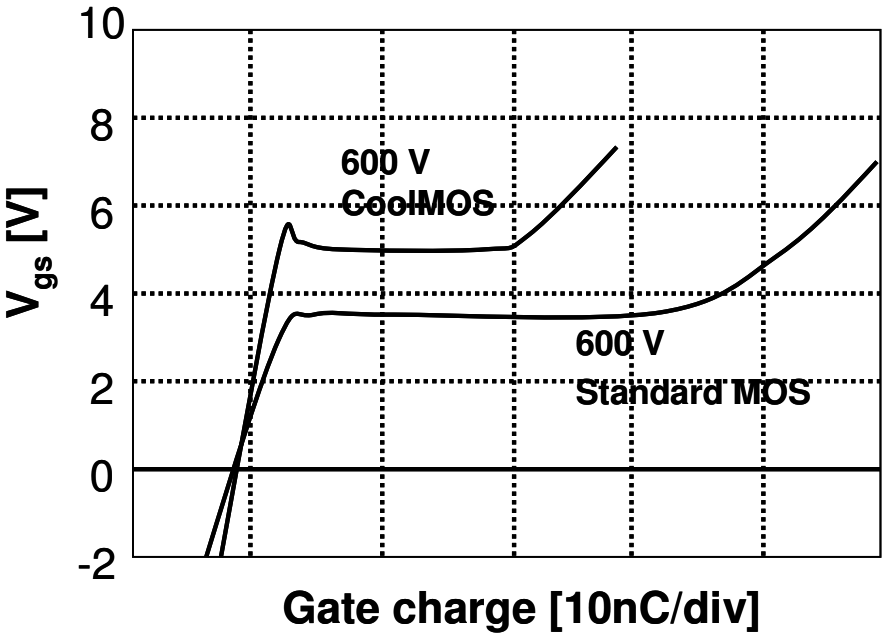


Figure 5-16 Gate charge characteristics of a 600mΩ CoolMOSTM compared to a 900mΩ standard MOSFET

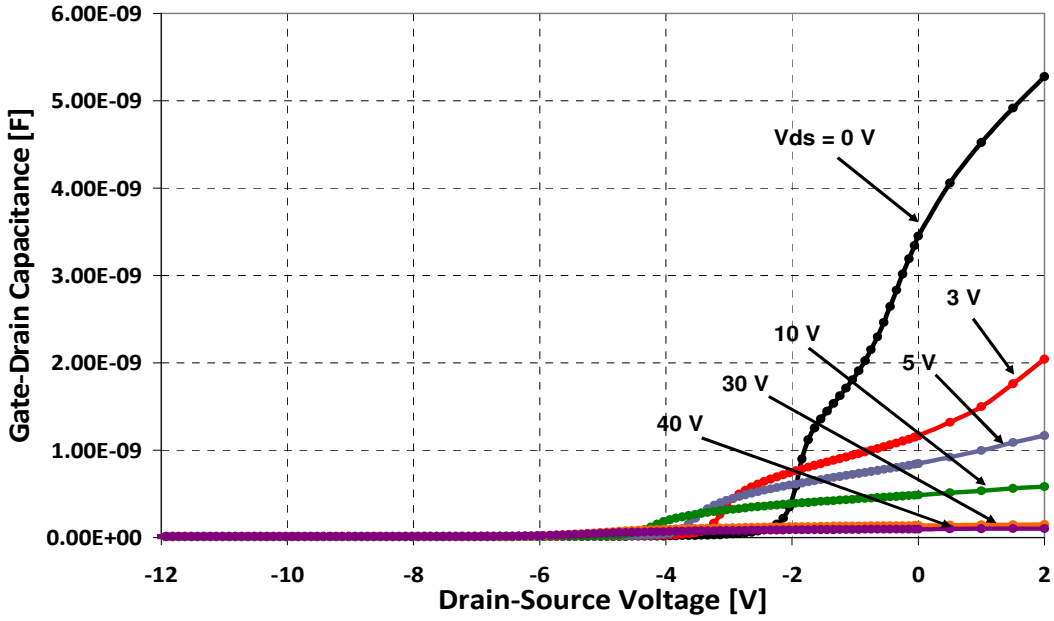
From circuit point of view, at low voltages, C_{ds} behaves like a turn-off relieve network. However, it is very important to have low energy stored in the output capacitance in order to have low switching losses given as [40]:

$$E_{ds} = \int C_{ds}(V) \cdot V \cdot dV \tag{5-2}$$

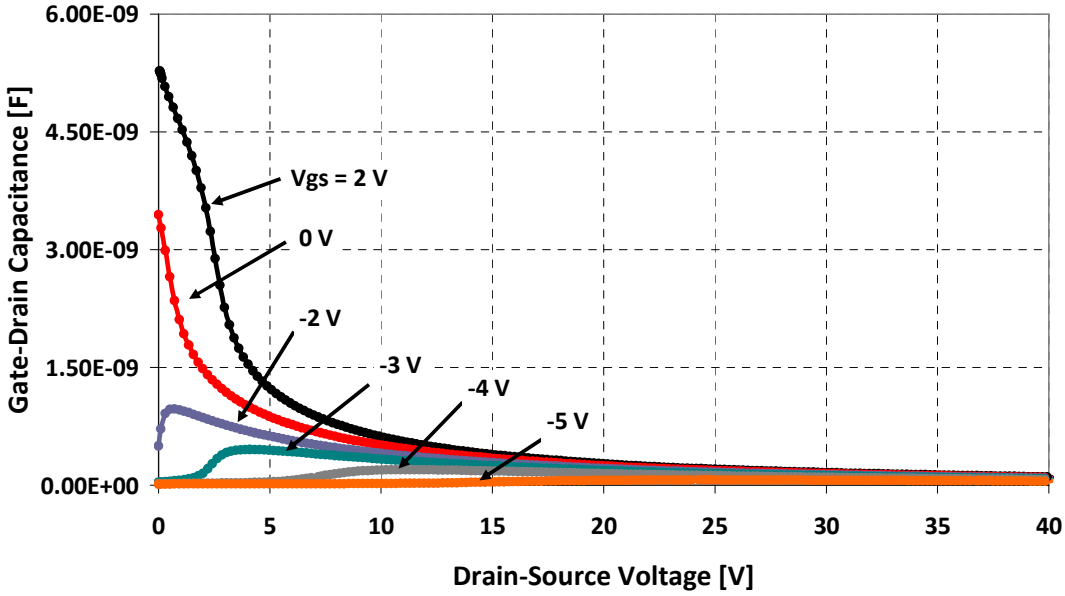
The energy lost in the switching process will convert into heat which will increase the chip temperature and affect the performance of the whole circuit. Due to the drastic reduction in the on-resistance and the stored output energy, the CoolMOSTM transistor has superior properties than the conventional power MOSFET for both static and transient characteristics.

In order to model the switching waveforms of the CoolMOS^{TM} transistor employed in the electrical vehicle project, the inter-electrode capacitances of the device have to be measured as a first step. Using the NIST customized C-V test system; the three inter-

electrode capacitances are measured with both gate-sweeping and drain-sweeping.



(a)



(b)

Figure 5-17 Characterization of C_{gd} versus V_{gs} by stepping V_{ds} (a); C_{gd} versus V_{ds} by stepping V_{gs} (b)

Figure 5-17 (a) shows the measured results of C_{gd} by sweeping the gate voltage from -12 V to 0, and stepping the drain voltage from 0 to 40 V; and (b) shows the measured results of C_{gd} by sweeping the drain voltage from 0 to 40 V, and stepping the gate voltage. These two plots are interchangeable. Figure 5-17 (b) exhibits some ripple behavior for some gate voltages (-2V~-5V) at low drain voltages. This can be explained from Figure 5-17 (a) where cross curves are seen in the range of $V_{gs} = -2V \sim -5V$. The capacitance value tends to peak at non-zero V_{ds} when V_{gs} falls in the range of $V_{gs} = -2V \sim -5V$. These cross curves are be further explained by considering the variation of the flat band voltage (V_{FB}) at different V_{gs}.

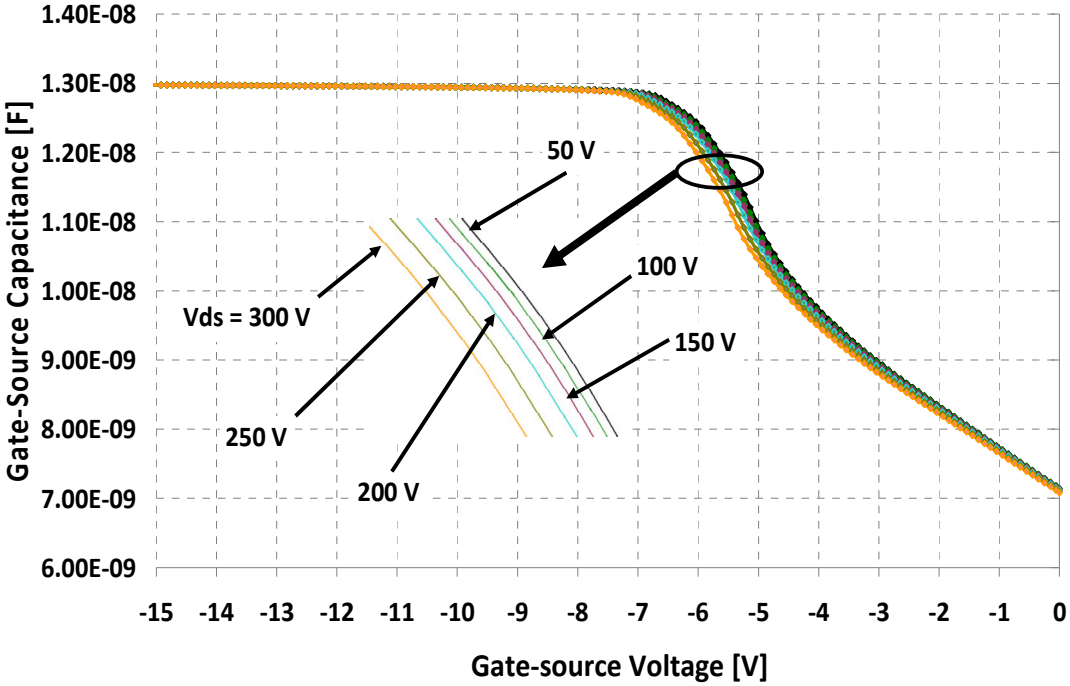


Figure 5-18 Characterization of C_{gs} versus V_{gs} by stepping V_{ds}

Figure 5-18 shows the measured results of C_{gs} by sweeping the gate voltage from -15 V to 0, and stepping the drain voltage from 50 V to 300 V. The zoomed-in feature shows

more details. The curves stay very close with each other, which imply that C_{gs} does not change with V_{ds}.

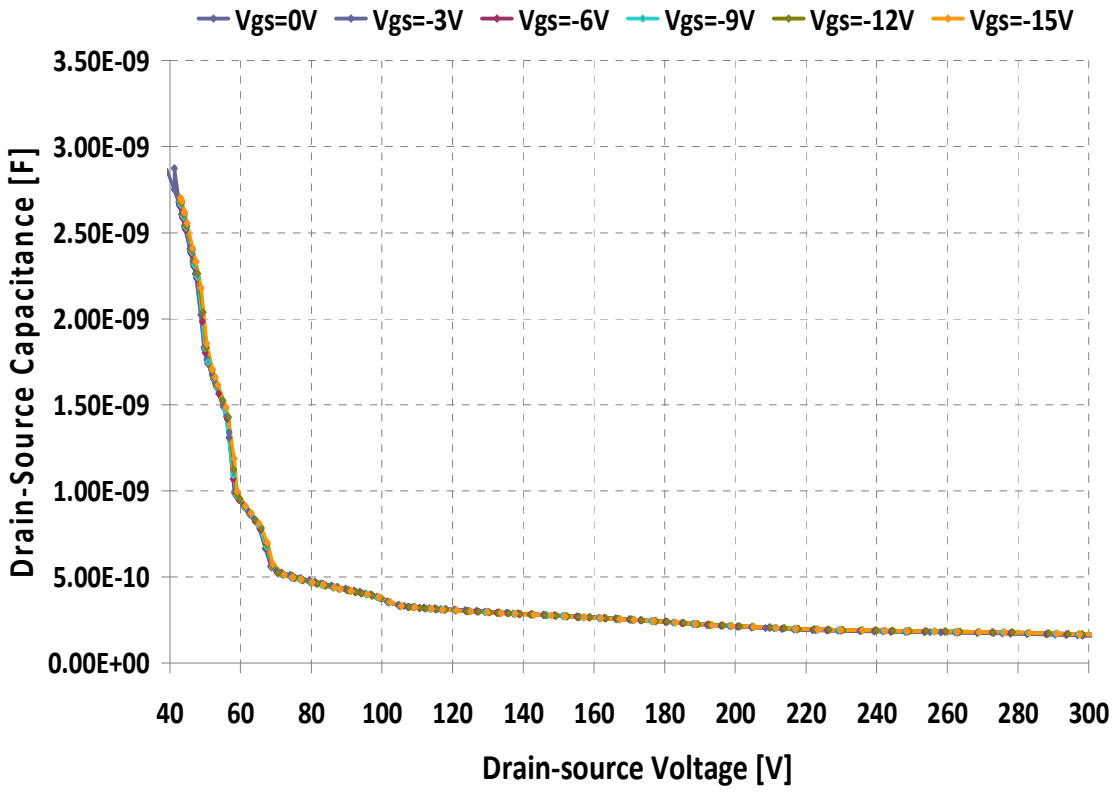


Figure 5-19 Characterization of C_{ds} versus V_{ds} by stepping V_{gs}

Figure 5-19 shows the measured results of C_{ds} by sweeping the drain voltage from 40 V to 300 V, and stepping the gate voltage from -15 V to 0. Also, it can be seen that the curves overlap with each other and does not change with V_{gs}. In the next chapter, a new approach for modeling the inter-electrode capacitances of the CoolMOS™ transistor will be presented. This new modeling approach features continuous curves, high accuracy, and good model flexibility.

Chapter 6 Modeling of CoolMOS™ and Model Parameter Extraction

There are several available MOSFET models available for circuit simulation [44]-[49]. Some have been macromodels, which consist of a subcircuit implemented in SPICE to capture the internal physics of the power MOSFET structure [45]-[48]. These models tend to be complex with a narrow range of accuracy, produce discontinuous C-V curves, have convergence problems and complex parameter extraction routines or none at all. There is only one publication found which is discussing power MOSFET model in the Saber simulator [50]. This model features continuous and accurate curves for all three inter-electrode capacitances. The model equations are derived from the charge stored on two internal nodes and the three external terminals. However, this model approach is not very flexible and straightforward. Model parameters can not be extracted directly from C-V measurement but from gate-charge plot.

Both static and transient characteristics are modeled with high accuracy for the CoolMOS™ transistor in this paper. The MOSFET model developed here is based upon the latest version of the power MOSFET formulation utilized in the Hefner IGBT model [51]. This model has the important quality that the implementation is relatively simple, and thus easily understood. Also, since it is based on the IGBT model, parameter extraction software was readily available to transition to the MOSFET [52]. The MOSFET channel current expressions used in the model are unique in that they include: (1) the channel regions at the corners of the square or hexagonal cells that turn on at lower gate voltages and (2) the enhanced linear region transconductance due to diffusion

in the nonuniformly doped channel. Note that unlike convention power MOSFET, for the CoolMOS^{TM} transistor, only the region in between the p strips is the conducting channel as described in chapter 5. This will result in some little change of model equations, which will be covered later in this chapter.

However, this basic model is found not sufficient enough to interpret the nonlinear C-V behavior of the CoolMOS^{TM} transistor. Plus, model equations can not be used to plot out capacitance versus gate voltage because V_{gs} only appears in the boundary condition.

$$C_{GD} = \begin{cases} C_{oxd} & V_{DS} \le V_{GS} - V_{TD} \\ C_{oxd} C_{s\_gd} / \left(C_{oxd} + C_{s\_gd}\right) & V_{DS} > V_{GS} - V_{TD} \end{cases} \tag{6-1}$$

where

$$C_{s\_gd} = \frac{A_{GD} K_s}{\sqrt{\frac{2K_s\left(V_{DS} + V_{TD}\right)}{qN_d}}} \tag{6-2}$$

Also, model equations can not explain the ripple behavior of C_{gd} at some gate voltages as discussed in chapter 5. Thus, a new modeling approach has been developed to model the inter-electrode capacitances of CoolMOS^{TM}. Using the new modeling approach, plotting C-V with V_{gs} as the horizontal axis is doable, and the ripple behavior is well exhibited. Model parameters can be directly extracted from C-V measurement.

6.1 CoolMOS^{TM} On-state Characteristics

The basic model topology is shown in Figure 6-1. In Figure 6-1, R_b is the resistance in the drift region, R_s is the resistance in the substrate region, C_{oxs} is the constant gate-source overlap oxide capacitance, C_{s_gs} is the gate-source semiconductor capacitance, C_{oxd} is the

constant gate-drain overlap oxide capacitance, C_{s_gd} is the gate-drain semiconductor capacitance, and C_{ds} is the drain-source capacitance.

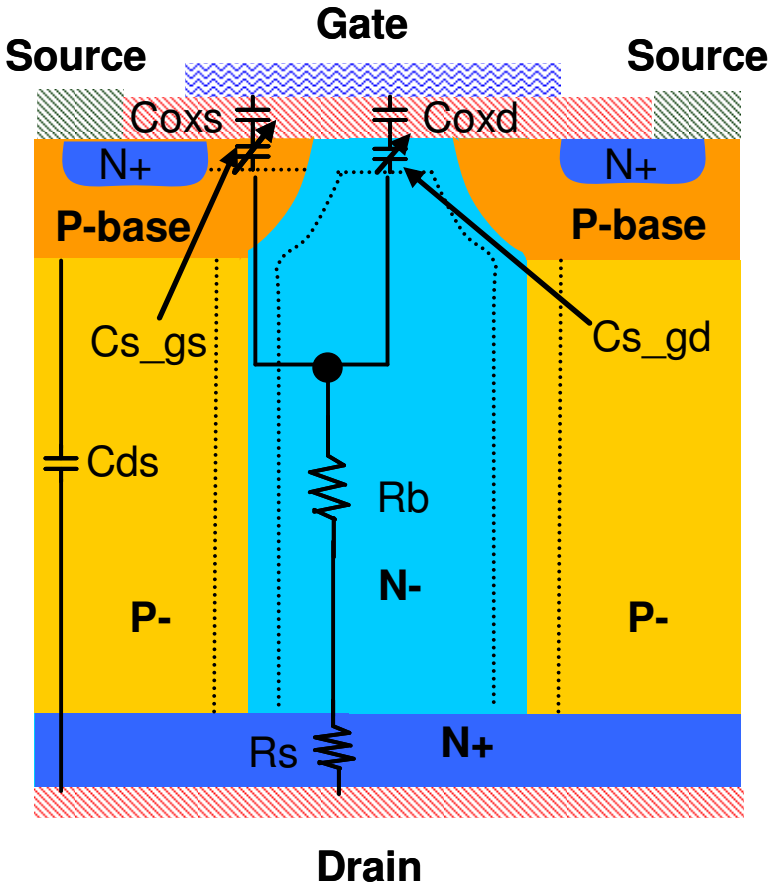


Figure 6-1 Basic model topology for the Si CoolMOS™ transistor

In the model, the MOSFET channel current I_{mos} is composed of two MOSFET channels in parallel, where

$$I_{mos} = I_{mosh} + I_{mosl} \tag{6-3}$$

such that one channel dominates in the very low current region, I_{mosl}, due to conduction at the corners of the MOSFET cells and the other channel dominates in the high current region, I_{mosh}, due to the main portion of the MOSFET cells [53]. The corner regions have a lower threshold voltage and transconductance than the main channel resulting in a "soft

threshold" effect. Therefore, it is necessary to assign each channel unique parameters to model the soft threshold effect

$$V_{Tl} = V_T - dV_{Tl} \tag{6-4}$$

$$V_{Th} = V_T + \frac{K_{fl}}{1 - K_{fl}} dV_{Tl} \tag{6-5}$$

where V_{Tl} and V_{Th} are the threshold voltages for the low and high current regions, and the transconductance factors K_{fl} and dV_{Tl} determine the threshold voltage for each channel. The expressions for V_{Tl} and V_{Th} are formulated to simplify parameter extraction and to allow the model to recycle the same set of parameter in the high current region with or without the soft threshold effect.

The linear region expression for I_{mosl} is given in the form of

$$I_{mosl} = \frac{K_{fl} K_f K_p \left[\left(V_{gs} - V_{Tl}\right) V_{ds} - \frac{P_{vf}^{y-1} V_{ds}^{y} \left(V_{gs} - V_{Tl}\right)^{2-y}}{y} \right]}{\left(1 + \theta\left(V_{gs} - V_{Tl}\right)\right)} \tag{6-6}$$

for $V_{ds} \le \frac{V_{gs} - V_{Tl}}{P_{vf}}$ where

$$y = \frac{K_f}{K_f - \frac{P_{vf}}{2}} \tag{6-7}$$

and the linear region expression for I_{mosh} takes the form

$$I_{mosh} = \frac{\left(1 - K_{fl}\right) K_f K_p \left[\left(V_{gs} - V_{Th}\right) V_{ds} - \frac{P_{vf}^{y-1} V_{ds}^{y} \left(V_{gs} - V_{Th}\right)^{2-y}}{y} \right]}{\left(1 + \theta\left(V_{gs} - V_{Th}\right)\right)} \tag{6-8}$$

for $V_{ds} \le \frac{V_{gs} - V_{Th}}{P_{vf}}$.

The above expressions for I_{mosl} and I_{mosh} in the linear region include the effect of carrier diffusion in the channel due to nonuniform channel dopant density. This effect will cause the transconductance to have different values in the linear region and the saturation region. The model presented here incorporates this effect and use a transconductance parameter K_p in the saturation region and a transconductance factor K_f in the linear region, where K_f is the ratio of the linear region transconductance parameter to the saturation region transconductance parameter. The pinch-off voltage parameter P_{vf} further refines the transition between the saturation and the linear region. Note that the expressions for I_{mos} and y in the linear region are written in a way that the current and its first derivative are continuous at the pinch-off voltage.

The expressions for the saturation region are in the form of

$$I_{mosl} = \frac{K_{fl} K_p \left(V_{gs} - V_{Tl}\right)^2}{2\left(1 + \theta\left(V_{gs} - V_{Tl}\right)\right)} \tag{6-9}$$

for $V_{ds} > \frac{V_{gs} - V_{Tl}}{P_{vf}}$ and

$$I_{mosh} = \frac{\left(1 - K_{fl}\right) K_p \left(V_{gs} - V_{Th}\right)^2}{2\left(1 + \theta\left(V_{gs} - V_{Th}\right)\right)} \tag{6-10}$$

for $V_{ds} > \frac{V_{gs} - V_{Th}}{P_{vf}}$.

Also, the parameter θ is included in current expressions of both linear region and saturation region to depict the effect of charge mobility reduction due to the high transverse electric field for high gate voltages.

There are two series resistance R_b and R_s as shown in Figure 6-1. In the model, the total drain-source terminal voltage V_{dst} consists mainly of the voltage drops across the two series resistances and the voltage across the MOSFET channel V_{ds}, as given by

$$V_{dst} = V_{ds} + I_d\left(R_b + R_s\right) \tag{6-11}$$

6.2 CoolMOS™ Transient Characteristics

The inter-electrode capacitances of power MOSFET type devices are very important in modeling its switching behaviors accurately, especially when investigating the effect of the variation of C_{gd}, which dominates the output switching waveforms due to the "Miller" effect. This paper describes an approach for modeling the inter-electrode capacitances that accounts for the actual charge distribution inside the CoolMOS™ capacitors [54] and uses this approach to derive the presented Saber-compatible model. Linearization of the key model equation was also employed to simplify the numerical complexity while retaining the functional accuracy of the device capacitances. Model equations were implemented in Saber which was used to validate the CoolMOS™ model static and dynamic behaviors.

6.2.1 Equivalent Circuit

The basic device structure and model topology for an n-type CoolMOS™ transistor is shown in Figure 6-1. The equivalent circuit in the non-conducting state is derived as shown in Figure 6-2. C_{gd} consists of the gate-drain overlap oxide capacitance (C_{oxd}) and the gate-drain junction capacitance (C_{s_gd}) in a relationship given by

$$\frac{1}{C_{gd}} = \frac{1}{C_{oxd}} + \frac{1}{C_{s\_gd}} \tag{6-12}$$

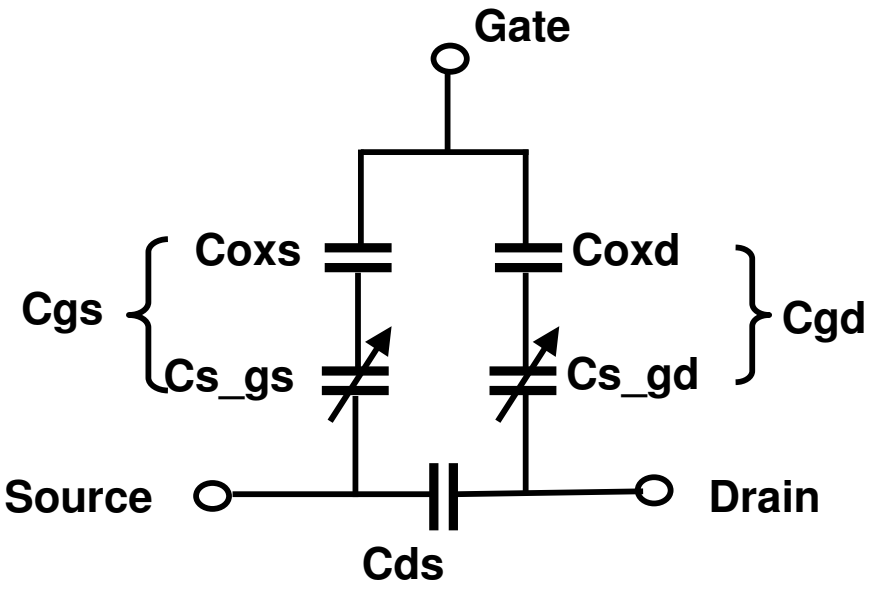


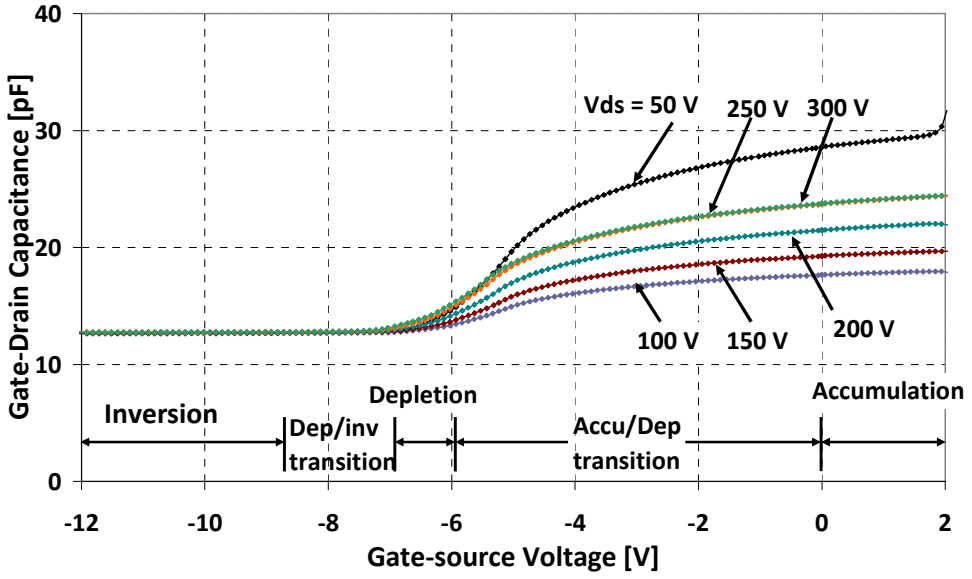
Figure 6-2 The simplified equivalent circuit of the CoolMOS^{TM} transistor in the non-conducting state

Similarly, C_{gs} consists of the gate-source oxide capacitance (C_{oxs}) and the gate-source junction capacitance (C_{s_gs}) in the same form as (6-12).

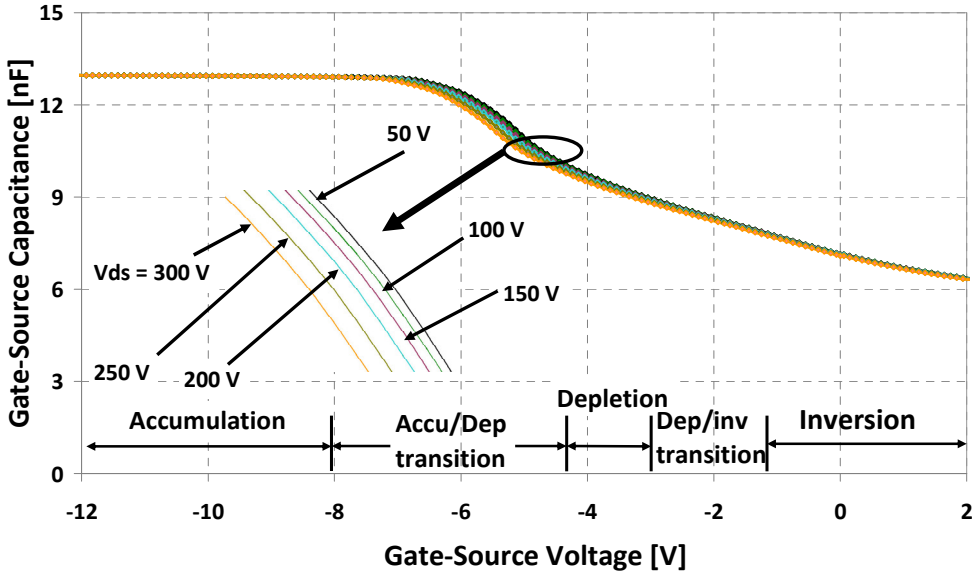
6.2.2 Gate-voltage Transition Analysis

For an n-type MOSFET, when $V_{gs} > 0$, the gate-drain overlap is in *accumulation* (see Figure 6-3 (a)). Upon applying a small amount of negative gate voltage, the gate-drain overlap will move from *accumulation* to *depletion*. As V_{gs} decreases towards -12 V, it will eventually go to *inversion* where the number of minority carriers remains fixed. This explains why the capacitance value for C_{gd} stays constant as shown in Figure 6-3 (a). It can be explained from a charge standpoint, the positive V_{gs} draws the negative charges toward the semiconductor-insulator interface forming a majority carrier accumulation in the n- drift region. The application of small negative V_{gs} will soon decrease and deplete the concentration of the accumulated majority carrier known as depletion. Finally, as V_{gs} becomes more and more negative, the surface electric field will be strong enough to draw

the minority carriers – holes close to the semiconductor-insulator interface, increase the hole concentration systematically and start to form an inversion layer. Notice that the curves overlap for V_{ds}= 250*V* and *300V*.



(a)



(b)

Figure 6-3 Transition from the region of accumulation to depletion and then inversion of C_{gd} with decreasing V_{gs} (a); transition from the region of accumulation to depletion and then inverstion of C_{gs} with increasing V_{gs}

On the other hand, due to the overlap between the gate and the p-base, the behavior of C_{gs} is the opposite of that of C_{gd} as a function of the gate bias V_{gs} as shown in Figure 6-3 (b). As V_{gs} decreases from 2 V to -12 V, the p-base surface goes from *inversion* to *depletion* and eventually to *accumulation*.

6.3 Derivation of Model Equations

In many publications, model equations used to calculate capacitances usually take V_{ds} as the independent variable (x-axis), with V_{gs} as a parameter which only appears in the boundary conditions [53, 55]. Thus, it is not possible to calculate capacitances as a function of V_{gs} using these model equations. Furthermore model validation is even less practical. V_{gs} must be explicitly included in the model equations of inter-electrode capacitances rather than accounted for as a boundary condition. In this work, a new approach has been developed by combining the simple delta-depletion and the exact calculation in order to model the nonlinear behavior of the inter-electrode capacitances of CoolMOS^{TM} based on the gate voltage bias condition. This new approach is generic and can apply to other power MOSFETs that have metal-oxide-semiconductor interface.

6.3.1 Simple Delta-depletion Model

It is relatively easy to establish a simple model based on the delta-depletion formulation [24]. This is demonstrated in Figure 6-4; the dotted curve represents the simulation result from the first-order delta-depletion theory by assuming the depletion threshold voltage (V_{TD}) set to 4 V. The simple model works well in the inversion region by assuming a constant capacitance value; but it is rather crude in the neighborhood of the transition points when going from accumulation to depletion.

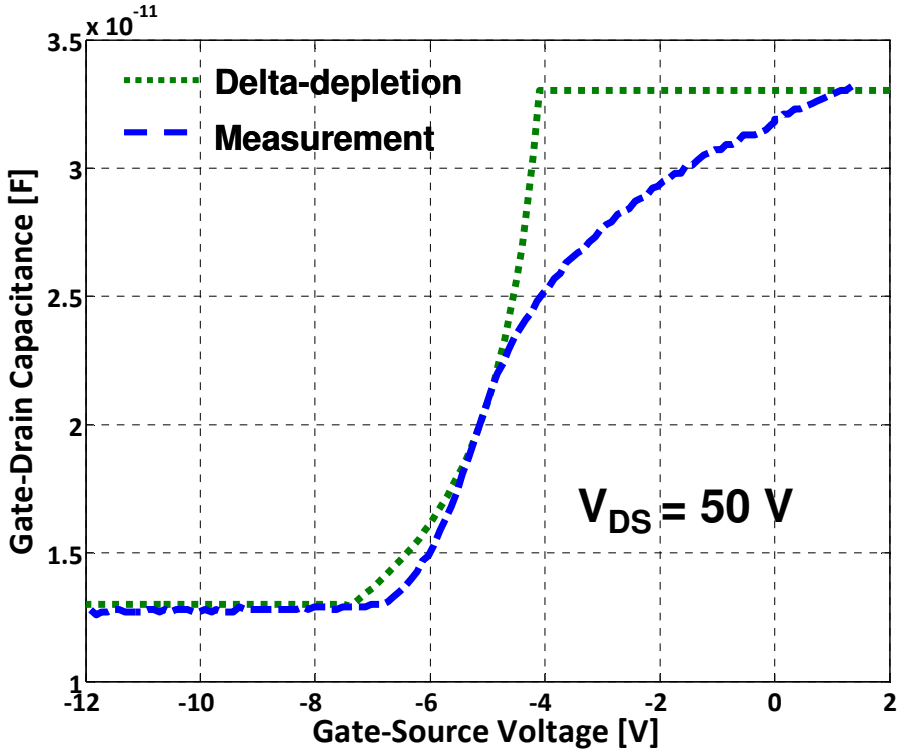


Figure 6-4 Comparison of the delta-depletion model (dotted) and the measured (dashed) C_{gd} versus V_{gs} of a 650 V CoolMOS™ for V_{ds} = 50 V

$$C = \begin{cases} C_o & \text{...acc} \quad (6\text{-}13) \\ \dfrac{C_o}{1+\dfrac{K_o W}{K_s t_{ox}}} & \text{...depl} \quad (6\text{-}14) \\ \dfrac{C_o}{1+\dfrac{K_o W_T}{K_s t_{ox}}} & \text{...inv} \quad (6\text{-}15) \end{cases}$$

The above equations are model equations for delta-depletion approach written in different forms based on the gate bias. It is seen from (6-15) that the depletion width W is assumed to be a constant W_T in the inversion layer. And the simulation result matches very well with the measured data in that region. The physics explanation will be

presented in the later section. However, this constant approximation will be used in the development of Saber model.

6.3.2 Numerical Model

The model presented in this paper is based on deriving the actual charge distribution inside the MOS transistor. The general capacitance formula including the a.c. inversion layer polarization effect was derived by Brews [54]. Model equations employed here are generic and applicable to all insulator-semiconductor systems [56].

6.3.2.1 Device Physics

The expressions for the charge density, electric field, and potential as a function of position inside the semiconductor are obtained by solving Poisson's equation in one dimension [24, 54]. The physical parameters used in the calculation including doping concentration in the drift region (N_d) and oxide layer thickness (t_{ox}) were extracted as a first step using the Hefner model [53]. The capacitance-voltage (C-V) relationships for an ideal n-type MOS transistor are given as:

$$C = \frac{C_{ox\_eff}(V_{ds})}{1 + \left(\frac{K_o W_{eff}}{K_s x_o} \right)} \tag{6-16}$$

where C_{ox_eff} is the effective oxide capacitance as a function of V_{ds}, and the effective depletion width is given as

$$W_{eff} = \begin{cases} \hat{U}_s A_D L_D \left[\dfrac{2F(U_s, U_F)}{e^{U_F}\left(1 - e^{-Us}\right) + e^{-U_F}\left(e^{Us} - 1\right)} \right] & \ldots\text{acc/depl} \quad (6\text{-}17) \\ \dfrac{\sqrt{2} A_D L_D}{\left(e^{U_F} + e^{-U_F}\right)^{1/2}} & \ldots\text{flat band} \quad (6\text{-}18) \\ \hat{U}_s A_D L_D \left[\dfrac{2F(U_s, U_F)}{e^{-U_F}\left(1 - e^{Us}\right) + e^{U_F}\left(e^{-Us} - 1\right)/(1+\Delta)} \right] & \ldots\text{depl/inv} \quad (6\text{-}19) \end{cases}$$

where A_D is a fitting parameter for W_{eff}, and

$$\Delta = \frac{\left(e^{-Us} + U_s - 1\right) / F(U_s, U_F)}{\int_{Us}^{0} \dfrac{e^{-U_F}\left(e^{U} - 1\right)\left(e^{-U} + U - 1\right)}{2F^3(U, U_F)} dU} . \quad (6\text{-}20)$$

The dimensionless semiconductor surface electric field $F(U_s, U_F)$ is defined by

$$F(U_s, U_F) = \sqrt{e^{U_F}\left(e^{-U_s} + U_s - 1\right) + e^{-U_F}\left(e^{U_s} - U_s - 1\right)} . \quad (6\text{-}21)$$

U_s and U_F are the normalized potentials, defined by $U_s = q\phi_s / kT$ and $U_F = q\phi_F / kT$, where ϕ_s is the surface potential and $\phi_F = (kT/q)\ln(n_i / N_d)$ is the Fermi potential. The symbol $\hat{U}_s$ is defined by $\hat{U}_s = 1$, for $U_s > 0$; and $\hat{U}_s = -1$, for $U_s < 0$. The intrinsic Debye length L_D is given as

$$L_D = \sqrt{K_s \varepsilon_0 kT \Big/ 2q^2 n_i} \quad (6\text{-}22)$$

where K_s is the dielectric constant for Si, and ε_0 is the permittivity of free space. The gate voltage is related to the oxide voltage, the surface potential, and the flat-band voltage V_{FB} through the relationship

$$V_{GS} = V_{FB} + \phi_s + \hat{U}_s \frac{kTK_s t_{ox} F(U_s, U_F)}{qK_o L_D} \quad (6\text{-}23)$$

where K_O is the dielectric constant for the oxide and t_{ox} is the thickness of the oxide layer.

It should be noted that equation (6-19) and (6-20) are only valid for n-type semiconductors, which are used to calculate C_{gd} for the n-drain CoolMOS^{TM} transistor in this paper. These two equations need to be modified to be used for p-type devices, and the modified equations must be used to calculate C_{gs} for the CoolMOS^{TM} transistor due to the presence of p-bases in the source region [24], given as

$$W_{eff} = \begin{cases} \hat{U}_s A_D L_D \left[\dfrac{2F(U_s, U_F)}{e^{U_F}\left(1 - e^{-Us}\right) + e^{-U_F}\left(e^{Us} - 1\right)} \right] & \ldots\text{acc/depl} \quad (6\text{-}24) \\ \dfrac{\sqrt{2} A_D L_D}{\left(e^{U_F} + e^{-U_F}\right)^{1/2}} & \ldots\text{flat band} \quad (6\text{-}25) \\ \hat{U}_s A_D L_D \left[\dfrac{2F(U_s, U_F)}{e^{U_F}\left(1 - e^{-Us}\right) + e^{-U_F}\left(e^{Us} - 1\right)/(1+\Delta)} \right] & \ldots\text{depl/inv} \quad (6\text{-}26) \end{cases}$$

where A_D is a fitting parameter for W_{eff}, and

$$\Delta = \frac{\left(e^{U_s} - U_s - 1\right) / F(U_s, U_F)}{\int_0^{U_s} \dfrac{e^{U_F}\left(1 - e^{-U}\right)\left(e^{U} - U - 1\right)}{2F^3\left(U, U_F\right)} dU}. \quad (6\text{-}27)$$

6.3.2.2 Numerical Model for CoolMOS^{TM}

The above equations were first implemented in Matlab^{TM} to compare the model predictions with measured data in order to evaluate their accuracy and applicability to the CoolMOS^{TM} transistor. The capacitance cannot be expressed explicitly as a function of V_{gs} as shown in equations (2) to (7). In Matlab^{TM}, a numerical method has to be used to solve the problem by assuming a set of U_s values.

In Figure 6-5, the dash-dotted curve shows the simulated curve of C_{gd} using the numerical approach for $Vds = 50$ V. It exhibits better agreement with the measured data especially in the neighborhood of the transition points going from accumulation to

depletion where simple delta-depletion analysis fails. This validates the accuracy of the theoretical equations derived from the exact charge distribution analysis. However, it does not work as well as the simple delta-depletion model in the inversion region

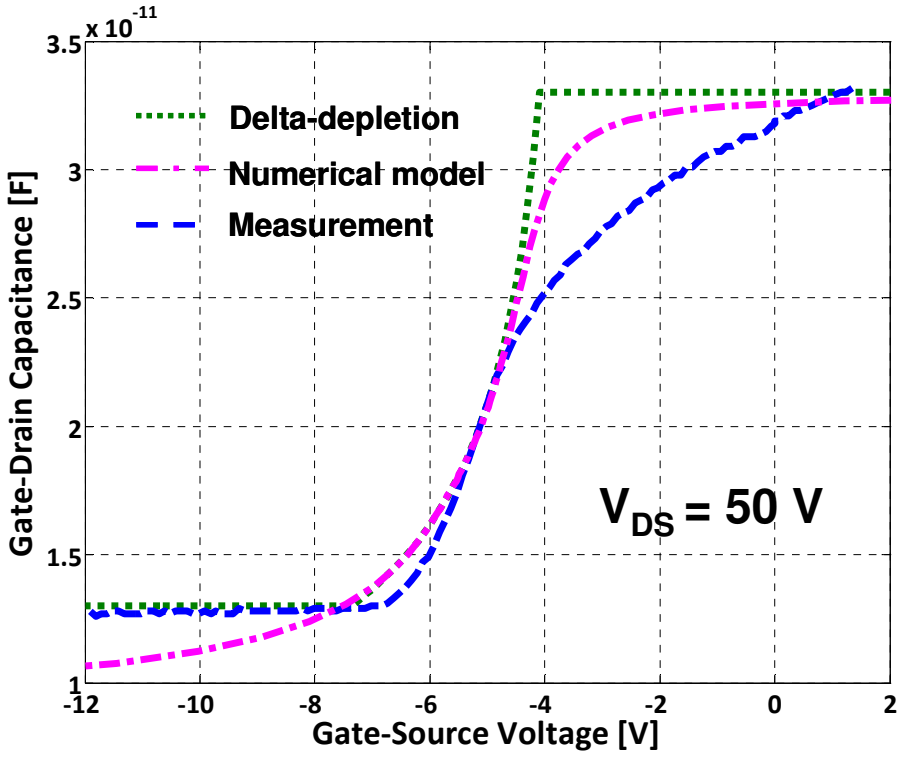


Figure 6-5 Comparison of the delta-depletion model (dotted), the numerical model (dash-dotted), and the measured (dashed) C_{gd} versus V_{gs} of a 650 V CoolMOS™ for V_{ds} = 50 V

6.3.3 Saber Model

Although the above theoretical equations were validated using Matlab™ through comparison with experiment, they are not ready to be implemented in Saber for circuit simulation due to the mathematical complexity of some of the model equations. Simplification and linearization need to be performed to reduce the numerical complexity while improving the functional accuracy of the device capacitances with the help of some free parameters. Furthermore, the analysis is conducted for accumulation, depletion and, inversion, respectively.

6.3.3.1 *Linearization Process*

From the circuit perspective, V_{gs} is the voltage reference that circuit designers use. However, from the device physics point of view the surface potential U_s, is the one used in the above equations to calculate capacitances. These two variables are related through equation (6-23) but in an implicit form through the function $F(U_s, U_F)$, which depends on U_s in both exponential and linear form described in equation (6-21). The linearization of $F(U_s, U_F)$ is critical in order to express equation (6-23) in an explicit form that can be coded into Saber.

A typical variation of $F(U_s, U_F)$ as a function of U_s is shown in Figure 6-6 for the CoolMOS™ transistor in the n-drain region with N_d = 1e15 cm^{-3}. U_F is calculated to be -11.5 with this N_d. In the accumulation region, the values of U_s are positive (see Figure 6-6) and $V_{gs} > V_{FBD}$. With negative U_F and positive U_s, the term $e^{-U_F}\left(e^{U_s} - U_s - 1\right)$ is much larger than the other term $e^{U_F}\left(e^{-U_s} + U_s - 1\right)$ in equation (6-23). So, in the accumulation region, $F(U_s, U_F)$ can be written as

$$F(U_s, U_F) \approx \sqrt{e^{-U_F}\left(e^{U_s} - U_s - 1\right)}. \tag{6-28}$$

However, there are still both exponential term and linear term exit in equation (6-28), which makes it not explicit for linearization. The exponential term (e^{U_s}) in (6-28) can be expressed through Taylor series for further linearization in the form of

$$e^{U_s} = 1 + U_s + \frac{U_s^2}{2!} + \cdots \frac{U_s^n}{n!} \quad . \tag{6-29}$$

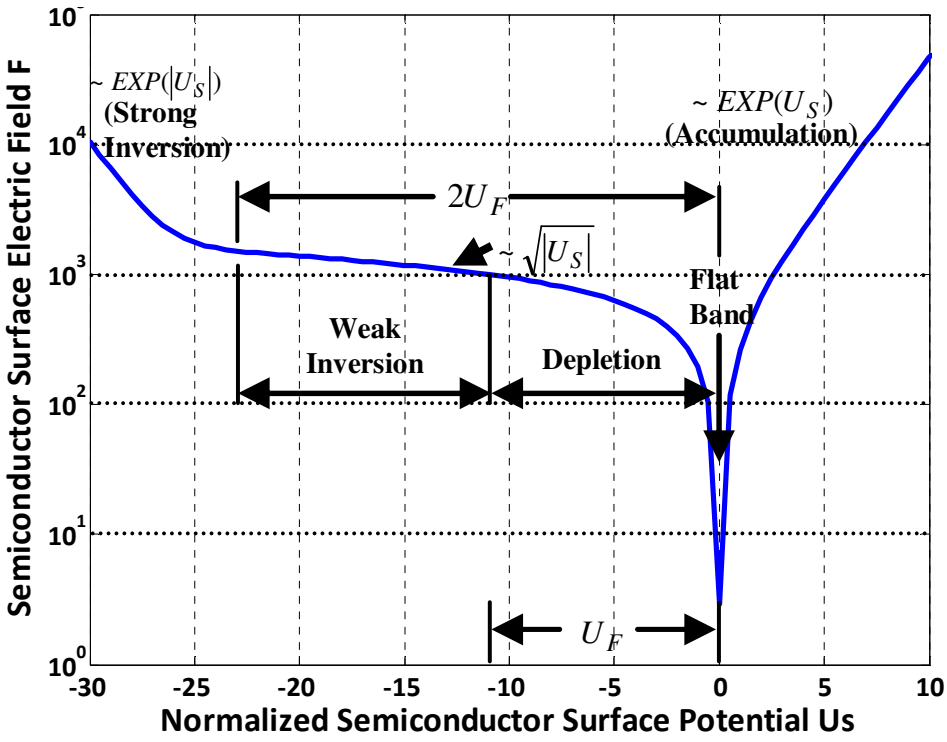


Figure 6-6 Relationship between the dimensionless semiconductor surface electric field F and the normalized semiconductor surface potential U_s in log scale for n-drain device

By combining equations (6-28) and (6-29) (first three terms only), $F(U_s, U_F)$ can be linearized and then substituted into equation (6-23) which is reorganized as

$$U_s = \frac{V_{gs} - V_{FB}}{B_D\left(\frac{kT}{q}\right)\left(1+\frac{P_P}{\sqrt{2}}\right)} \tag{6-30}$$

where $P_P = \frac{K_s \cdot t_{ox}\sqrt{e^{-U_F}}}{K_o \cdot L_D}$ is a constant value parameter, and B_D is the fitting parameter in the linearization process.

6.3.3.2 Refinement Process

The above linearization is conducted for the accumulation and the transition from accumulation to depletion regions where $U_s > 0$ (or $V_{gs} > V_{FBD}$). Through equation (6-30),

a set of U_s values can be calculated corresponding to the measured V_{gs} values, instead of assuming a set of predefined U_s values in the numerical model. Equation (6-17) was employed to find the values of W_{eff} which were used to calculate the capacitance values through equation (6-16) for the accumulation case. It should be noted that at $U_s = 0$ (or $V_{gs} = V_{FBD}$), equation (6-18) must be employed to calculate W_{eff_FB} which only depends on constant physical parameters (i.e., U_F and L_D).

Once V_{gs} drops below V_{FB}, the n-drain surface changes to depletion/inversion with negative U_s. It can be seen from the measured data (dashed curve (d)) in Figure 6-7 that the capacitance remains constant in the depletion/inversion region. This is because the relatively sluggish generation-recombination process will not be able to supply or eliminate minority carriers in response to the applied a.c. signal. The number of minority carriers in the inversion layer therefore remains fixed at its d.c. value, and W_{eff} simply is well approximated by constant W_{eff_FB} [16]. This makes $C(inv) = C(FB) =$ constant by having a constant W_{eff} for all depletion/inversion biases. The above analysis simplifies the equation used in the numerical model and reduces the numerical complexity of solving equation (6-19), which requires integration.

The above discussion and development of the model equations is focused on calculation of C_{gd} for the CoolMOS™ transistor with an n-type drift region. It should be noted that the behavior of C_{gs} is opposite to C_{gd} as a function of U_s. For C_{gs}, it is in accumulation, when $U_s < 0$ (or $V_{gs} < V_{FBS}$), and moves to depletion/inversion, when $U_s > 0$ (or $V_{gs} > V_{FBS}$). Therefore, some modifications are needed before applying

the same approach and linearization technique which was used for C_{gd} to calculate values for C_{gs}.

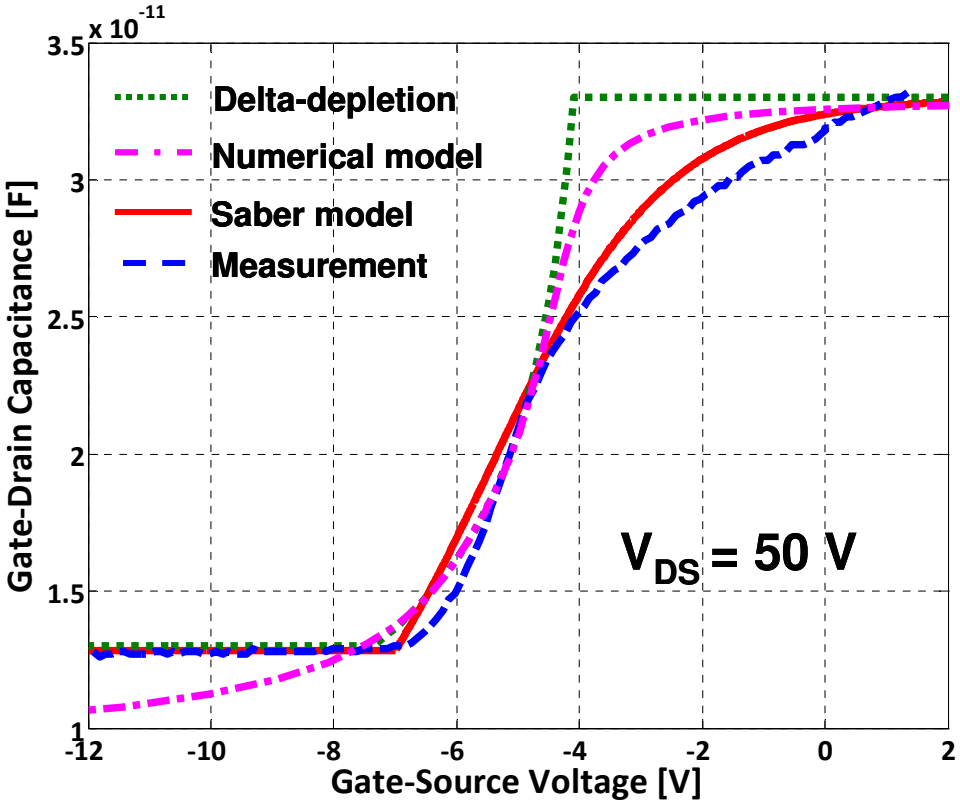


Figure 6-7 Comparison of the delta-depletion model (dotted), the numerical model (dash-dotted), the Saber model (solid), and the measured (dashed) C_{gd} versus V_{gs} of a 650 V CoolMOS™ for V_{ds} = 50 V

C_{ds} is modeled by the standard delta-depletion because it simply changes with V_{ds}, given as

$$C_{ds} = \frac{C_{jo}}{\left(1 - \frac{V_{ds}}{V_{\delta}}\right)^{m}} \tag{6-31}$$

where C_{j0} is the zero-bias junction capacitance, V_{δ} is the junction potential, and m is the grading coefficient.

An overall Saber-compatible model can now be constructed by combining the results of the foregoing analysis of accumulation, depletion, and inversion regions. In Figure 6-7, the solid line shows the simulated curve of C_{gd} using the Saber model for V_{ds} = 50 V, which exhibits excellent agreement in the full range with the measured data. Notice that the Saber model obtained much better accuracy than the numerical model in the neighborhood of the transition points going from accumulation to depletion. This is due to the inclusion of fitting parameters A_D, A_S, B_D, and B_S give the Saber model more flexibility to better match the measured data.

6.3.3.3 Saber Model Parameters

Table 6-1 lists the primary model parameters that were used for modeling the inter-electrode capacitance for CoolMOS™ in Saber. These parameters are derived and extracted from measurements. Parameters C_{oxd_eff} and C_{oxs_eff} are the effective gate-drain and gate-source oxide capacitances, which decrease monotonically with increasing V_{ds} because of the depletion region developed by the gate-to-drain voltage. And their capacitance values can be extracted directly from the measured CV curves at small positive V_{gs} values. U_{FD} and U_{FS} are physical parameters which can be calculated from the semiconductor doping concentration.

The two fitting parameters: A_D and A_S are employed to correct a deviation in the lateral depletion behavior that is caused by the n- and p- super-junctions in the drift region. The CoolMOS™ transistor exhibits very nonlinear behavior in the non-conducting state [40]. This is a result of the lateral electric field that builds up, which drives the charge towards the contact region. Therefore, extreme care must be exercised when extracting model parameters, because they must make the simulation curves work

continuously under all bias conditions. As described earlier, another two fitting parameters B_D and B_S are employed because of the linearization of equation (6-23) for C_{gd} and C_{gs}, respectively.

Table 6-1 Primary model parameters used for inter-electrode capacitances

	Model Parameter	Comments
C_{gd}	C_{oxd_eff}	Gate-drain effective oxide capacitance
	V_{FBD}	Drain flat band voltage
	A_D	Effective depletion width fitting parameter for drain
	B_D	Linearization fitting parameter for drain
	U_{FD}	Normalized Fermi potential for drain
C_{gs}	C_{oxs_eff}	Gate-source effective oxide capacitance
	V_{FBS}	Source flat band voltage
	A_S	Effective depletion width fitting parameter for source
	B_S	Linearization fitting parameter for source
	U_{FS}	Normalized Fermi potential for source
C_{ds}	C_{j0}	Zero-bias junction capacitance
	V_δ	Junction potential
	m	Grading coefficient

6.4 Parameter Extraction Software

A software package called IGBT Model Parameter ExtrACtion Tools (IMPACT) was introduced in [57] to automate laboratory instrument control and parameter extraction for Si IGBTs. IGBTs have more complicated structure than MOSFETs and IGBTs are minority carrier devices. Therefore, the original IMPACT program consists of five subprograms to fully extract model parameters for IGBTs. For the case of power MOSFETs, they are majority carrier devices and the extraction subprograms are reduced to three. A switch ring bar was added onto the main panel as an enhancement to provide the selection between the punchthrough IGBT, non-punchthrough IGBT, and MOSFET extraction algorithms. Also, the program was further enhanced by adding material properties for SiC [53]. The three programs used in power MOSFET parameter extraction

are demonstrated in Table 6-2. This table lists the symbol and name of the model parameters, as well as program and extraction characteristic.

Table 6-2 Software programs and extraction characteristics for power MOSFET model

Parameter symbol	Parameter name	Program	Extraction Characteristic
A	Device active area		Chip Size
V_T	Threshold voltage	SATMSR	Saturation current vs. Vgs
$K_p = K_{psat}$	Saturation region transconductance		Saturation current vs. Vgs
θ	Transverse electric field parameter		High saturation current vs. Vgs
K_{fl}	Low current transconductance factor		Low saturation current vs. Vgs
dV_{Tl}	Low current threshold voltage differential		Low saturation current vs. Vgs
$K_{plin} = K_p \cdot K_f$	Linear region transconductance parameter	LINMSR	On-state voltage vs. Vgs
R_s	Drain series resistance		On-state voltage vs. Vgs
N_b	Drift region dopant density		On-state voltage vs. Vgs
C_{gs}	Gate-source capacitance	CAPMSR	Gate charge at low gate voltage
C_{oxd}	Gate-drain overlap oxide capacitance		Gate charge at high gate voltage
A_{gd}	Gate-drain overlap area		Gate-drain charge
V_{Td}	Gate-drain overlap depletion threshold		Gate-drain charge
F_{xibe}	Gate-drain overlap depletion charge factor at edge		Gate charge vs. negative Vgs
F_{xibm}	Gate-drain overlap depletion charge factor at middle		Gate charge vs. negative Vgs

Figure 6-8, shows the material type switch and some important temperature dependent physical properties. Based on the input temperature and material, this panel will calculate out the values of the listed physical properties.

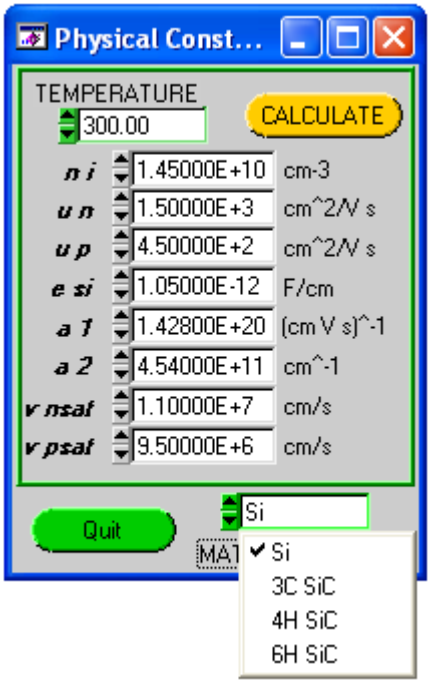


Figure 6-8 Panel of physical parameters

The three subprograms used for power MOSFETs are SATMSR, which measures the saturation current versus gate voltage to extract $K_{psat} \equiv K_p, V_T, \theta, K_{fl}$, and dV_{Tl}; LINMSR, which measures the linear region on-state voltage versus gate voltage for a constant drain current to extract $K_{plin} \equiv K_p K_f, R_s$, and N_b; and CAPMSR, which measures gate and gate-drain charge characteristics to extract $C_{gs}, C_{oxd}, A_{gd}, V_{Td}, F_{xjbm}$, and F_{xjbe}. The active area A should be acquired before the extraction and the width of the drift layer can be calculated out from the device voltage rating. The model parameter extraction needs to be performed in the sequence: SATMSR, LINMSR, and CAPMSR.

6.4.1 Saturation Region Parameter Extraction Using SATMSR

The SATMSR front panel is shown in Figure 6-9. A commercial curve tracer is used to measure the saturation current versus gate voltage which is used to extract the MOSFET model parameters in the saturation region including the transconductance parameter K_{psat}, the high current region θ, the low current region K_{fl} and dV_{Tl}, and the threshold voltage V_T. To perform the extraction, the measured MOSFET saturation current I_{mos}^{sat} versus gate voltage is converted into square root of I_{mos}^{sat} versus gate voltage (see bottom-left of Figure 6-9) which is used to extract the model parameters. The curve tracer (Tektronics 371 A) used to aid the extraction process is the type of instrument that uses the collector voltage as the sweep variable and the gate voltage as the step variable. The auto program not only can perform parameter extraction but also has the function that can take the IV measurement which uses the gate voltage offset voltage and the cursor readout to generate the continuous graph of current versus gate voltage.

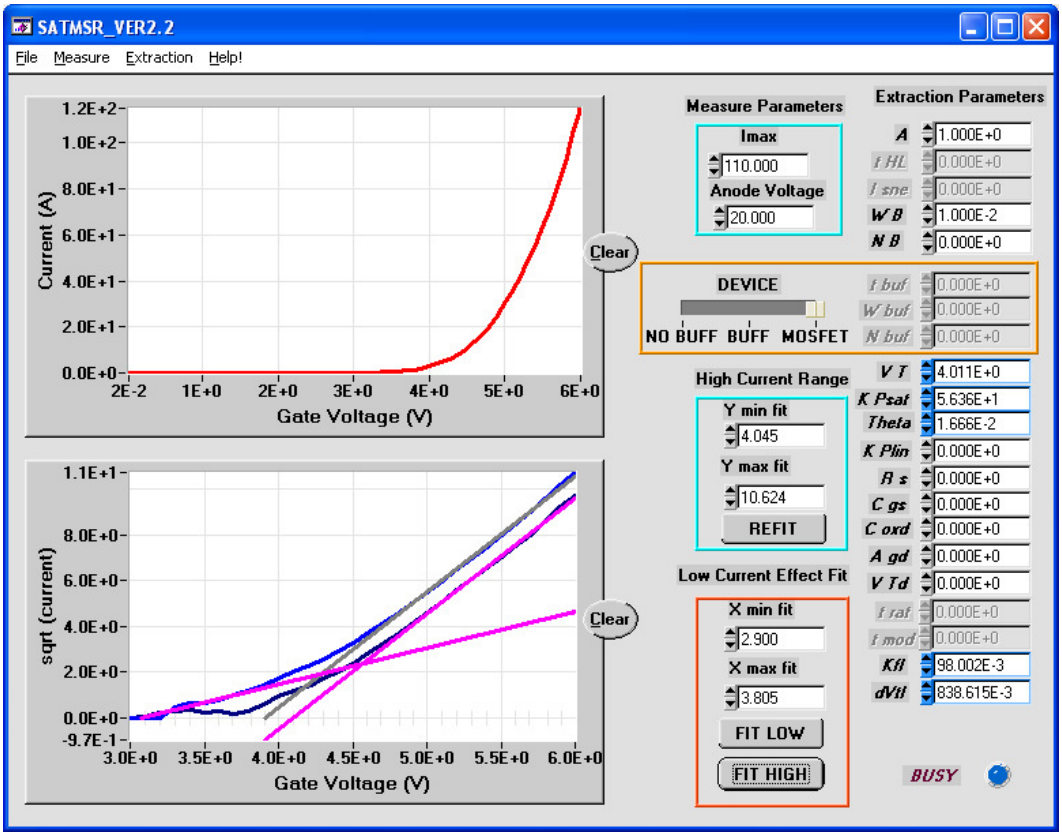


Figure 6-9 SATMSR front panel showing extraction of K_p, V_T, θ, K_{fl}, and dV_{Tl}

The SATMSR program incorporates several pull-down menus that allow the user to perform different measurement functions according to the device characteristics and the curve tracer required for the current range of interest. The program also allows the user to define the maximum allowable device current I_{max} during the measurement and the anode voltage of interest V_{anode}.

The extraction process starts by clicking "Extraction" from the pull-down menu. The first step takes a least squares fit to the simplified model equation

$$\sqrt{I_{mos}^{sat}} = \sqrt{\frac{K_{psat}}{2}}\left(V_{gs} - V_T\right). \tag{6-32}$$

The extracted K_{psat} and V_T are displayed on the right side of the panel in the parameter list. Next is to extract the high-current parameter θ and refine the extracted value of K_{psat}

using the "Refine K_{psat} and θ" option from the extraction pull-down menu. The "Fit Low" and "Fit High" buttons are clicked for several times in order to get good curve fit and extract K_{fl} and dV_{Tl}. These buttons perform a least-mean-square fit to the saturation region's low- and high-current equations which are (6-9) and (6-10), respectively. The program will automatically estimate the low- and high-current ranges for the fits but the user is also able to adjust them. Figure 6-10 illustrates the final fit of the square-root of the MOSFET saturation current in the saturation region, which demonstrates there are different slopes in the high- and low-current regions.

The model parameters extracted from SATMSR will be used to calculate model parameters in the other two programs which will be described later in details.

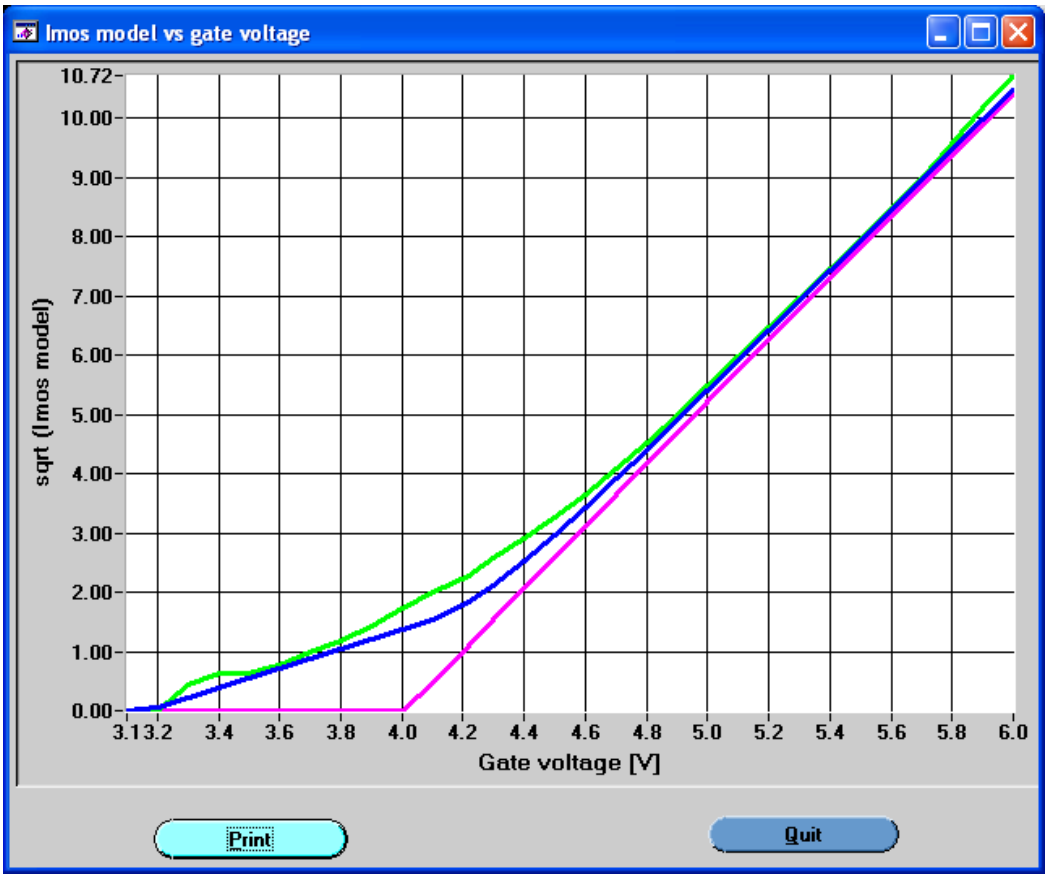


Figure 6-10 SATMSR final fit window demonstrating low- and high-current fit

6.4.2 Linear Region Parameter Extraction Using LINMSR

Figure 6-11 shows the front panel of the LINMSR program. The LINMSR uses the measurement of drain voltage versus gate voltage at a constant diode current to extract the parameters in the linear region including the transconductance K_{plin}, the series resistance R_s, and the base doping concentration N_b. These values are calculated from the model equations that are valid for the linear region where the values of the parameters extracted from the previous extraction steps (those from the SATMSR program) are used as known values in the equations.

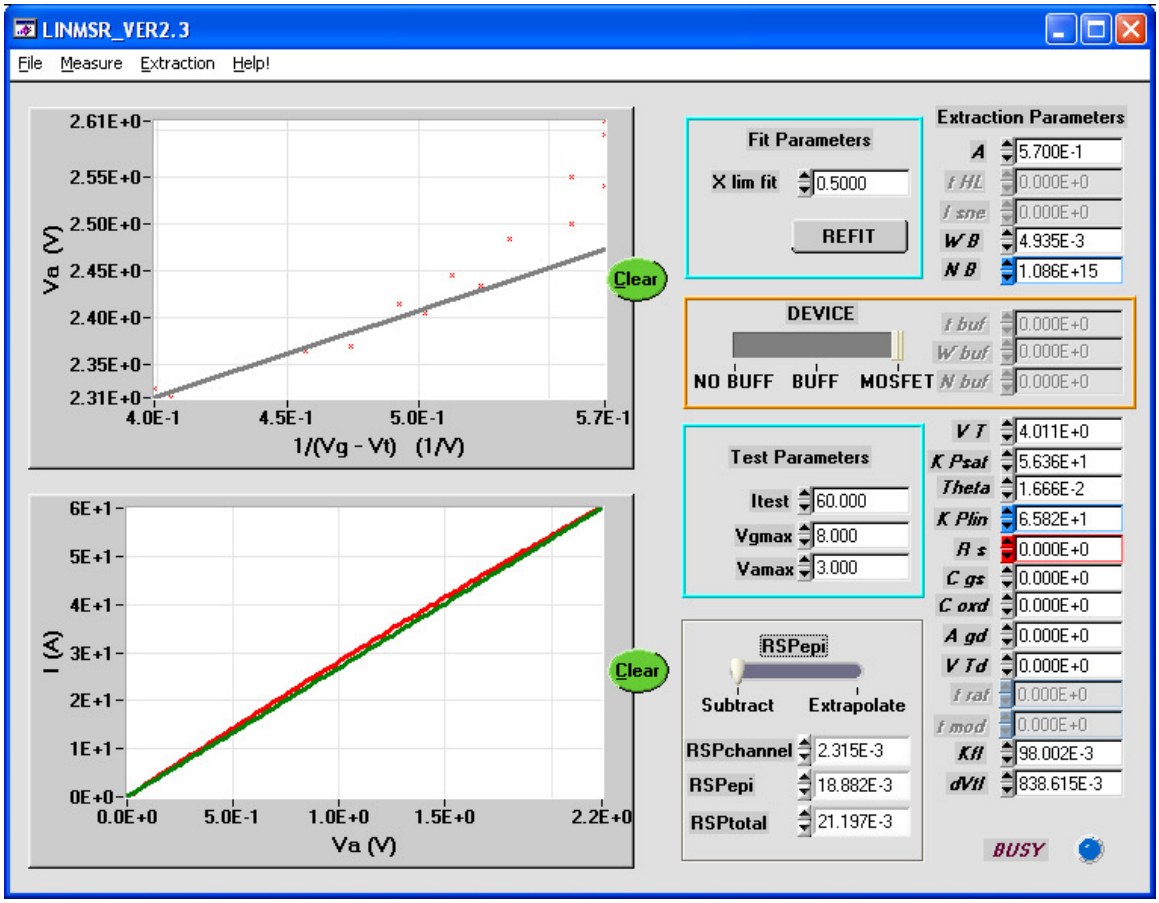


Figure 6-11 LINMSR front panel showing extraction of K_f, R_s, and N_b

LINMSR program can take measurement by clicking the "Measurement" from the menu. The user needs to input the test current I_T, the maximum gate voltage V_{gmax}, and the maximum anode voltage V_{amax} on the panel under the label of "Test Parameters". The same curve tracer is used to take the measurement to be used in the LINMSR program. LINMSR uses an iteration algorithm to establish the constant drain test current as described in [58], which results in measuring the on-state drain voltage that acquired at the selected test current I_T for each gate voltage.

Model parameters are extracted by using a least-mean-squares fit through model equations that is valid in the linear region in the form of

$$V_{on} = V_r + \frac{I_T}{K_{plin}\left(V_{gs} - V_T\right)} \tag{6-33}$$

where

$$V_r = \left(R_b + R_s\right)I_d + \frac{I_d\theta}{K_{plin}} \tag{6-34}$$

As seen from equation (6-33), K_{plin} can be calculated out from the slope and V_r is the y-intercept. The value of R_b can be calculated using equation (6-34) by substituting in V_r and other parameters extracted from the previous steps. Therefore, the value of N_b is calculated through the expression for R_b given as

$$R_b = \frac{W}{qAN_b\mu_n} \tag{6-35}$$

The above newly extracted model parameters are displayed in the list of parameters on the right side of the panel in Figure 6-11.

6.4.3 Gate Charge Characteristics Extraction Using CAPMSR

A test system was built to take the gate charge characteristics and the measured waveforms are captured by the oscilloscope. The drain voltage is clamped as a constant value and a -15 V is added to the gate in the beginning. An additional voltage source is used on the gate to change the gate voltage during the gate charge characteristics. The captured waveforms are transferred to the CAPMSR program as shown in the top graph of the front panel (see Figure 6-12). The CAPMSR program is used to extract model parameters including the gate-source capacitance C_{gs}, the gate-drain overlap oxide capacitance C_{oxd}, the gate-drain overlap area A_{gd}, and the gate-drain overlap depletion threshold V_{Td}.

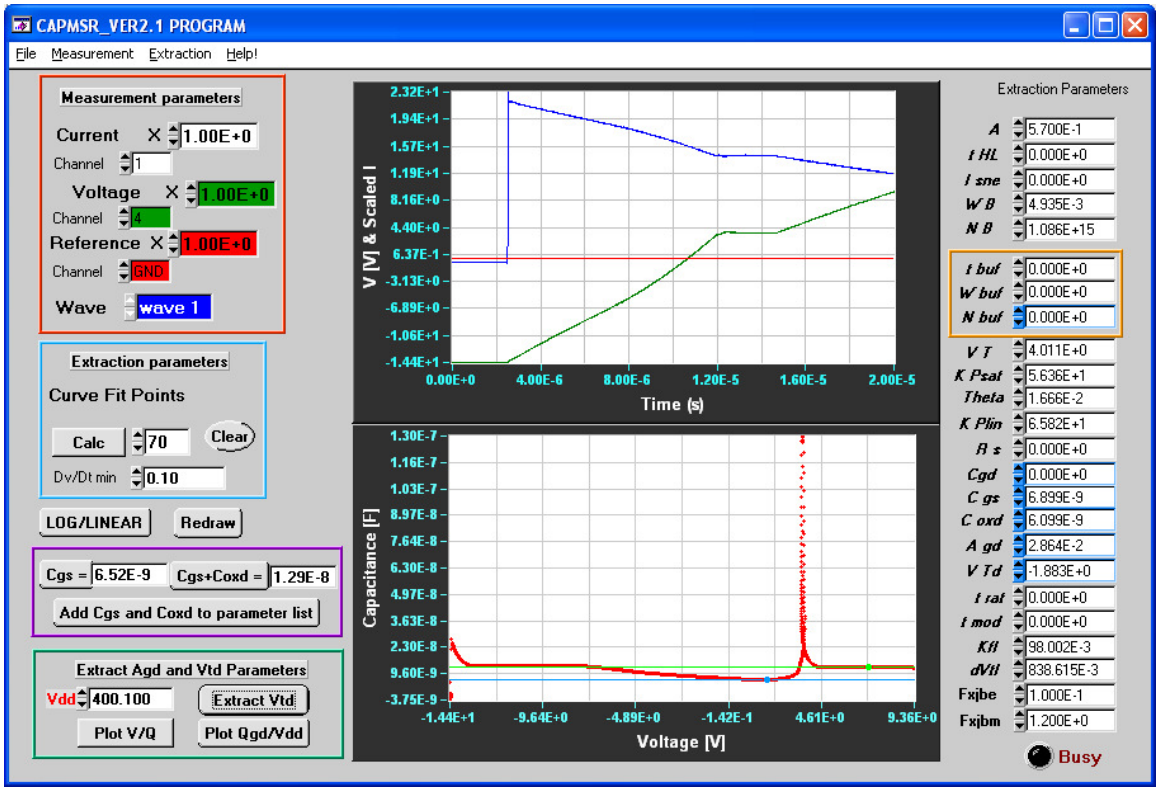


Figure 6-12 CAPMSR front panel demonstrating the extraction of C_{gs}, C_{oxd}, A_{gd}, and V_{Td}

$$C(V) = \frac{I}{dV/dt}. \tag{6-36}$$

Using equation (6-36), the program calculates *C(V)* versus voltage curve and plots the calculated values in the bottom graph on the front panel in Figure 6-12. The user controls the minimum value of *dV/dt* and the number of derivative points for each calculation. The values of C_{gs} and C_{oxd} are determined from *Ig* and dV_{gs}/dt during the positive voltage portion of gate charge curve. For positive values of gate voltage, there are essentially three distinct phases in the gate voltage waveform. During the fist phase, the gate current will charge the relatively small gate-source capacitance C_{gs} and V_{gs} increases with a fixed slope. Hence, C_{gs} can be extracted from this portion of the waveform by dividing the value of the gate current by the value of the derivative of gate voltage.

During the second phase or plateau region, V_{gs} stops increasing and stays constant. Meanwhile, the drain voltage decreases as the gate current starts to charge the large gate-charge capacitance C_{gd}. So, C_{gd} is extracted through equation (6-36) using the same approach which is used to extract C_{gs}. This provides a second method to extract C_{gd} and can be compared with the value of C_{gd} extracted from C-V measurement. A_{gd} and V_{Td} are also extracted from the second phase.

During the third phase, V_{gs} starts to rise again and the drain voltage remains constant. The gate current starts to charge both C_{gs} and C_{oxd}. Therefore, C_{oxd} can be extracted by subtracting out the value of C_{gs} which is extracted from the previous step.

As the last step, the values of Fxjbm and Fxjbe are calculated from equations

$$V_{Tdi} = V_{Td} - V_{bigd} - \frac{F_{xjbm} A_{gd}}{C_{oxd}} \sqrt{2\varepsilon_{semi} q N_b \left(V_{bigd} + V_{ds}\right)} \tag{6-37}$$

$$V_{Tdiedge} = V_{Td} - V_{bigd} - \frac{F_{xjbe} A_{gd}}{C_{oxd}} \sqrt{2\varepsilon_{semi} q N_b \left(V_{bigd} + V_{ds}\right)} \tag{6-38}$$

by utilizing the I_g and dV_{gs}/dt data for negative gate voltage and different drain voltages.

6.5 Body Diode of CoolMOS™

In order to get a more accurate device model for the CoolMOS™ transistor, the body diode also needs to be characterized. The on-state and the C-V characteristics are measured for the body diode of CoolMOS™ by shorting the gate terminal and the source terminal. Figure 6-13 demonstrates the forward IV characteristic of the body diode of the 650 V Si CoolMOS™ transistor. Figure 6-14 shows the C-V characteristic of the body diode of the 650 V Si CoolMOS™ transistor.

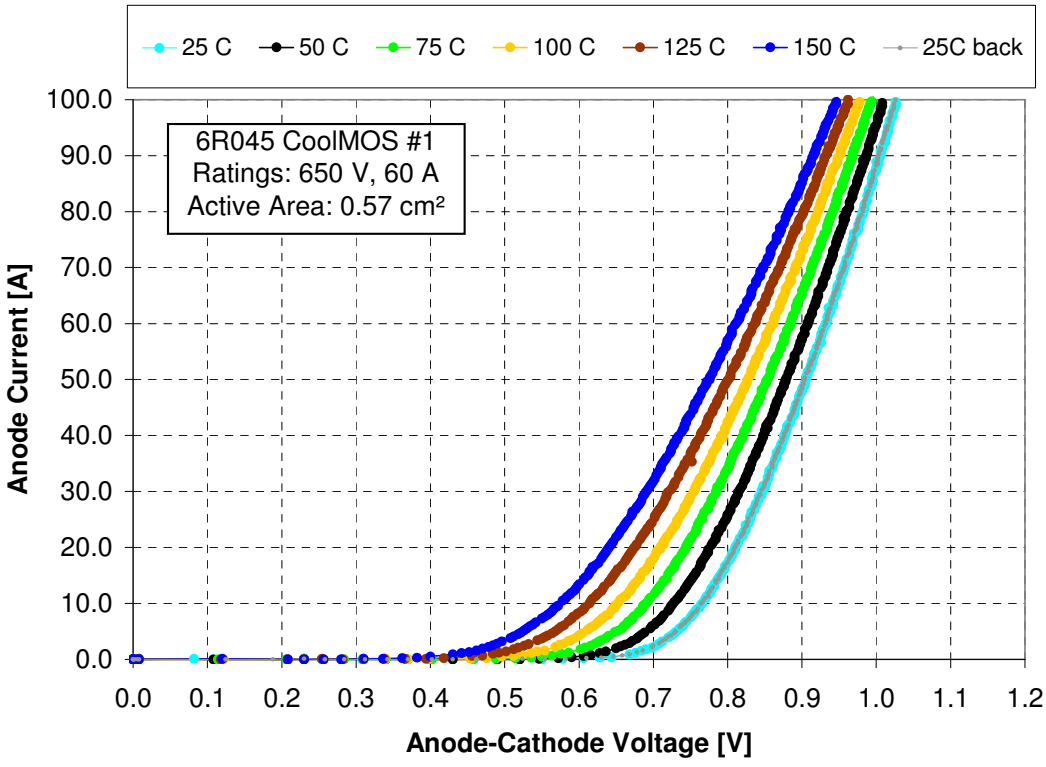


Figure 6-13 Forward conduction characteristics for the body diode of CoolMOS™

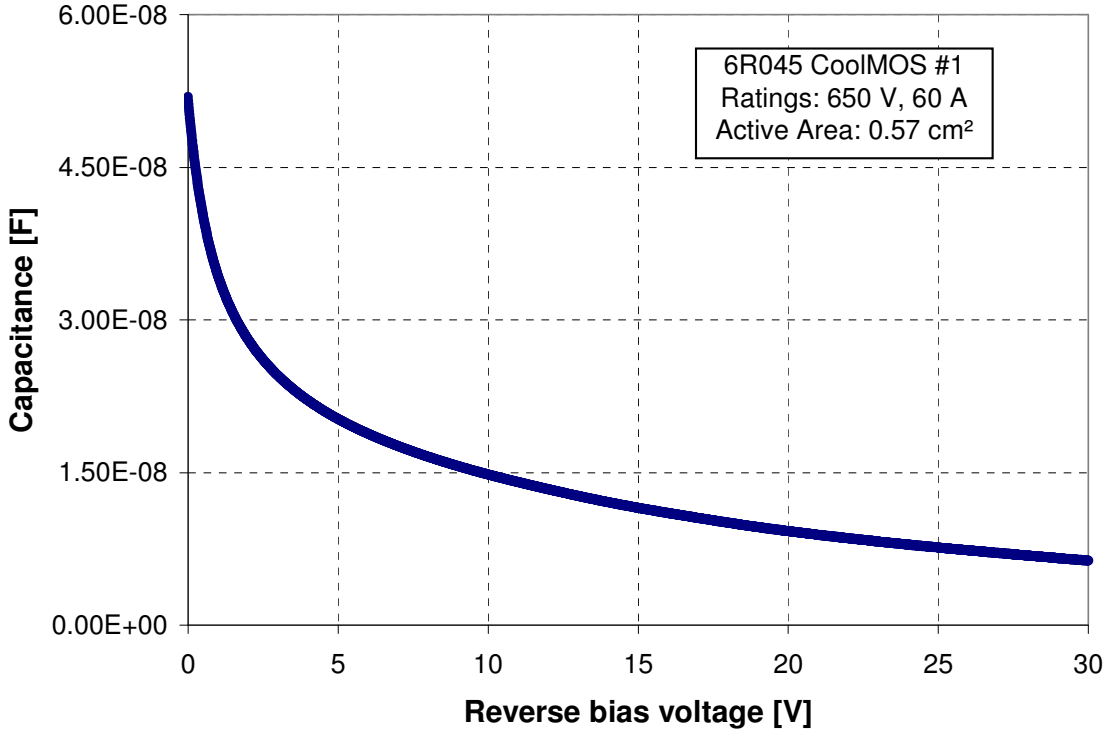
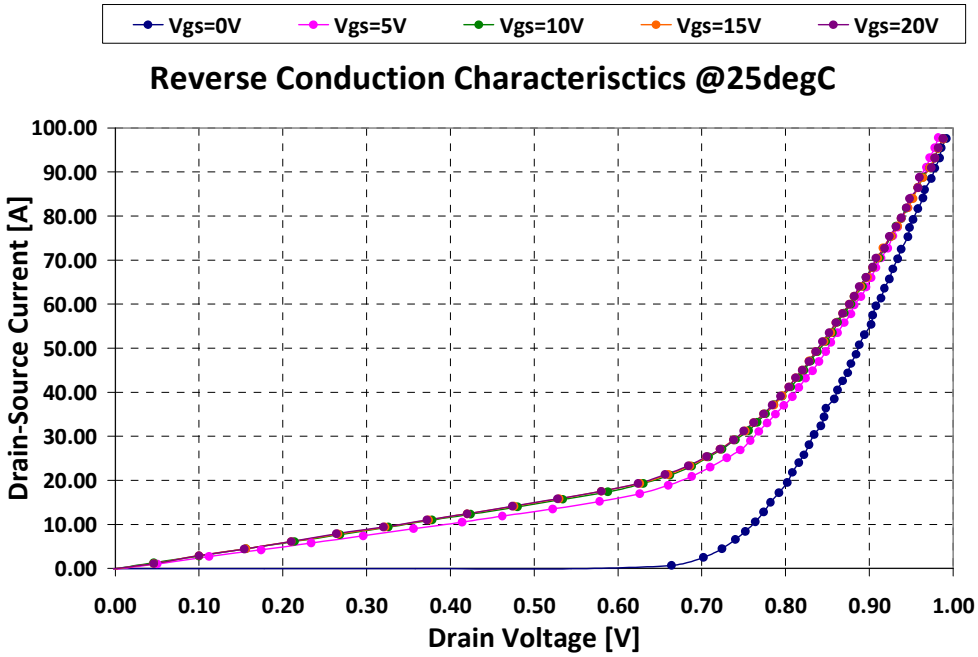


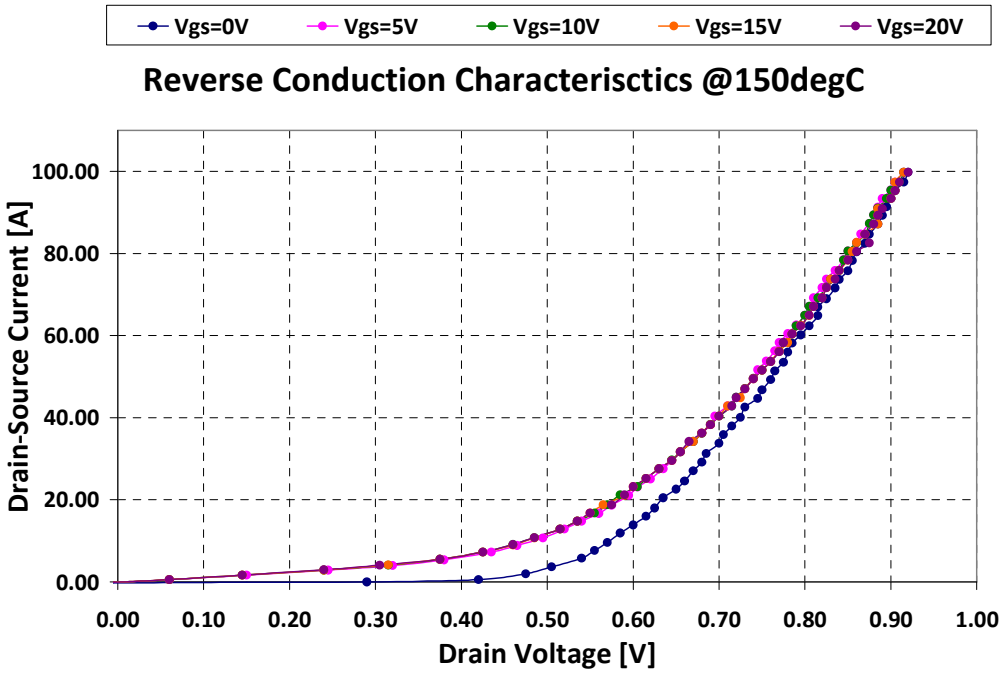
Figure 6-14 C-V characteristics for the body diode of CoolMOS™

6.6 Reverse Conduction of CoolMOS™

Theoretically, MOSFETs can conduct in both directions once the channel is formed. In the circuit design, the CoolMOS™ transistor is also considered for reverse conducting. Utilization of a CoolMOS™ device rather than an IGBT also allows synchronous rectification during the reverse conducting period and achieves fast turn-off without tail current. Therefore, it is important to measure the reverse conduction characteristics at various temperatures. Figure 6-15 demonstrates the reverse conduction characteristics of the CoolMOS™ transistor at 25°C (a) and 150°C (b). At high temperature, for the same diode voltage, there is more diode current flowing. Therefore, the power loss increases as temperature increases.



(a)



(b)

Figure 6-15 Reverse conduction characteristics for CoolMOS^{TM} at 25^{o}C (a), and at 150^{o}C (b)

6.7 Input, Output and Reverse Transfer Capacitances

The power MOSFET input capacitance C_{iss}, reverse transfer capacitance C_{rss}, and output capacitance C_{oss} will all affect the power conversion circuit. In hard switching, C_{oss} is used to calculate the additional power dissipation due to discharging this output capacitor every switching cycle. In soft switching circuits, C_{oss} may be used to calculate the resonant frequency or transition time, which is critical in establishing ZVS and/or ZCS conditions. Figure 6-16 depicts the typical circuit capacitances (C_{iss}, C_{oss}, and C_{rss}) for the CoolMOS™ transistor when the gate-source voltage is 0 V. The relationships between the inter-electrode capacitances (Cgd, Cgs, and Cds) and the circuit capacitances are demonstrated in Figure 6-16. The value of C_{iss} stays constant, whereas, the values of C_{oss} and C_{rss} vary non-linearly as a function of V_{ds}.

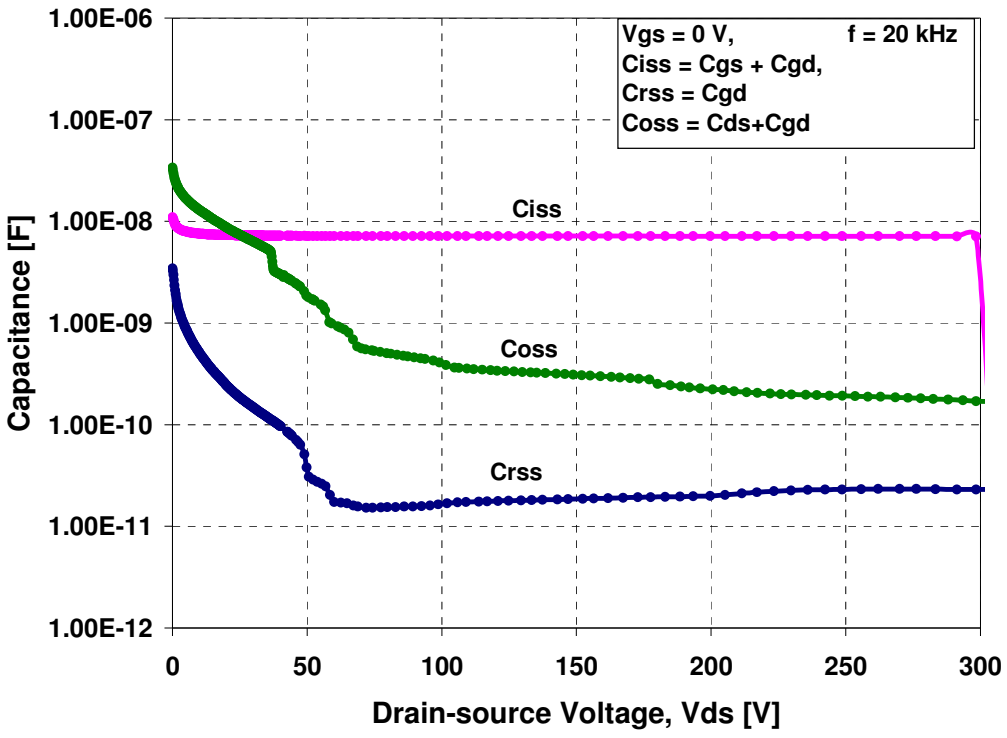


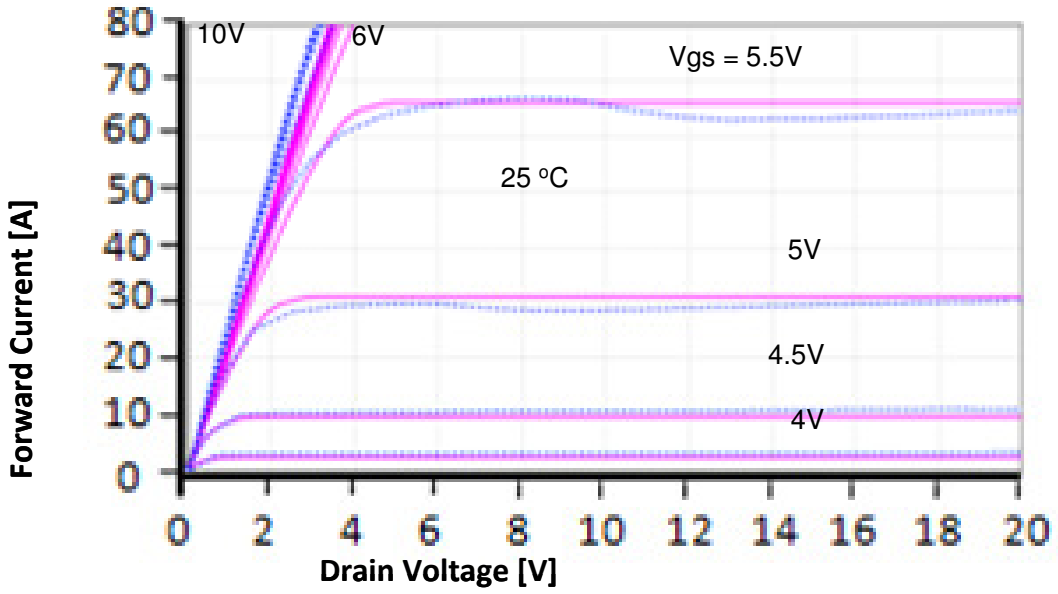
Figure 6-16 Typical circuit capacitances versus Vds

6.8 Model Validation Results

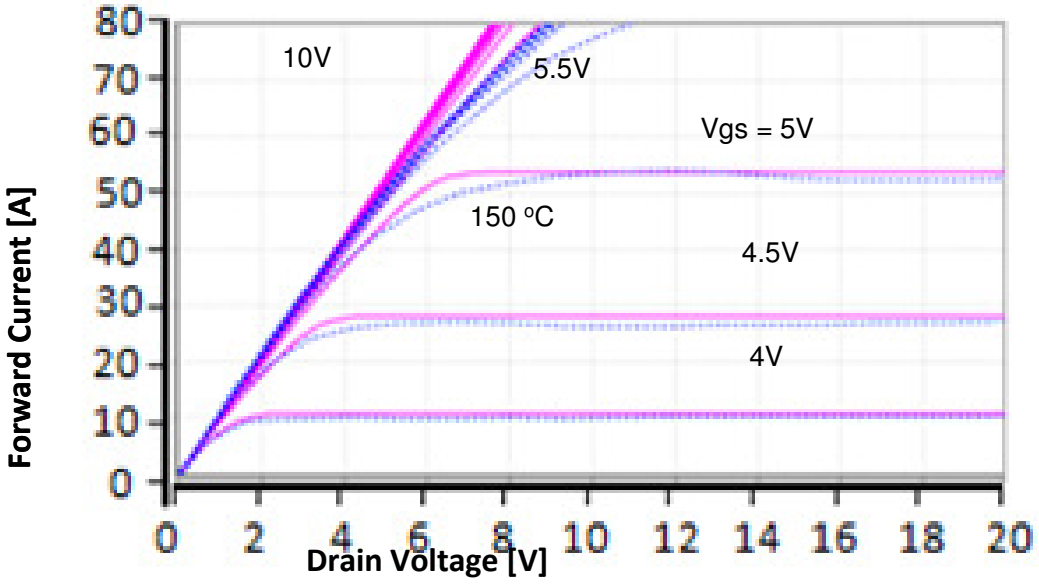
Both static and transient validations of the Si CoolMOS^{TM} transistor and its body diode are demonstrated. The results illustrate a very good agreement between the measured data and the simulated results as shown below.

6.8.1 On-state Characteristics Validation

Figure 6-17 demonstrates the forward IV characteristics of the CoolMOSTM transistor at 25^{o}C (a), and 150^{o}C. The comparisons between the measured and simulated curves demonstrate good agreement. Therefore, the model has been validated in the forward conduction range. Figure 6-18 shows the comparison between the measured data (dashed) and simulated curve (solid) for the body diode of CoolMOS^{TM} at various temperatures from 25 ^{o}C to 150 ^{o}C.



(a)



(b)

Figure 6-17 Comparison between measured data (dotted) and simulated data (solid) for a 650 V Si CoolMOS^{TM} at 25°C (a), at 150°C (b)

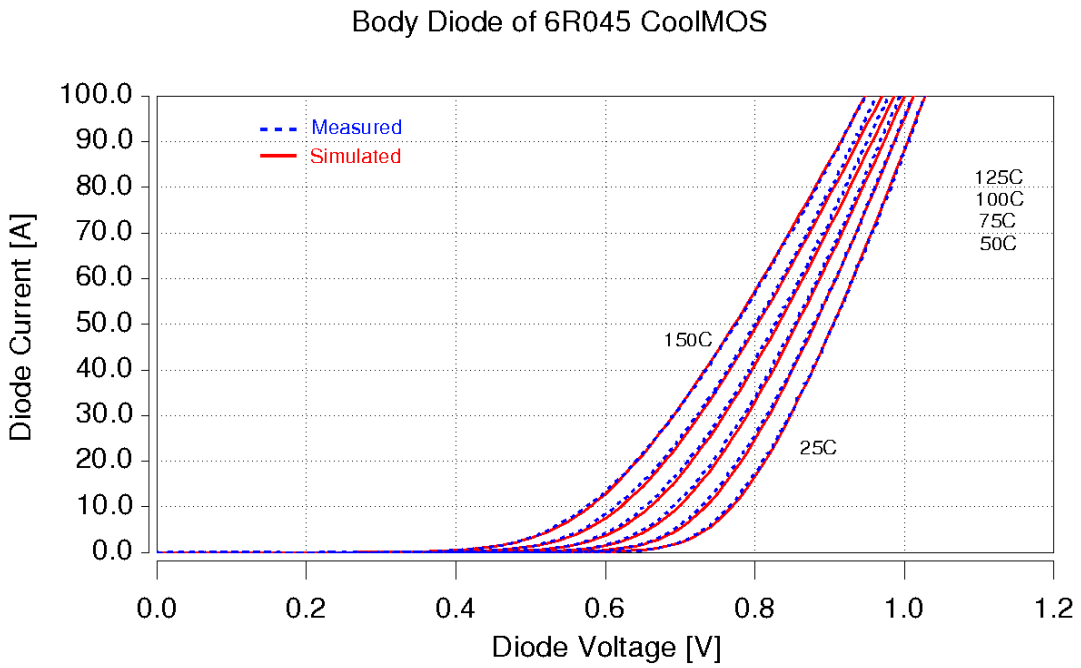


Figure 6-18 Comparison between measured data (dashed) and simulated data (solid) for the body diode of a 650 V Si CoolMOS^{TM} at 25 °C, 50 °C, 75 °C, 100 °C, 125°C and 175 °C

6.8.2 C-V Characteristics Validation

The results for the measured and modeled C_{gd} values are plotted versus V_{gs} with V_{ds} as a parameter in Figure 6-19. The good agreement over such a large range of bias conditions validates the accuracy of the new modeling approach as seen from Figure 6-19 (a) where V_{ds} ranges from 0 V to 40 V; and (b) where V_{ds} ranges from 50 V to 300 V. For a particular small positive V_{gs} value, C_{gd} decreases monotonically with increasing V_{ds}, due to the depletion region developed by the gate-to-drain voltage [45].

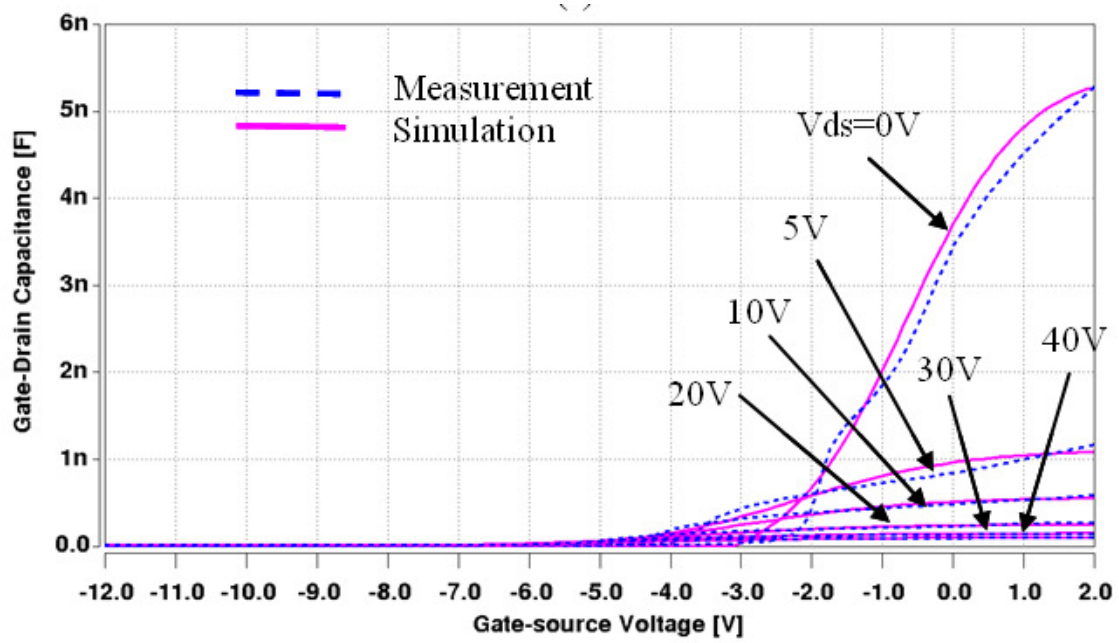
Figure 6-20 shows the model (solid) and measured (dashed) C_{gd} curves with V_{ds} on the horizontal axis and V_{gs} as the stepping parameter. Because the curves remain consistent for the high-bias range, they are condensed for V_{ds} between 60 V to 300 V in order to show more details in the low-bias range as seen from Figure 6-20. Notice that the C_{gd}

curve peak at non-zero V_{ds} for $V_{gs} \le -3$ V. This feature is due to the variation of V_{FB} for different V_{ds} (see Figure 5-17).

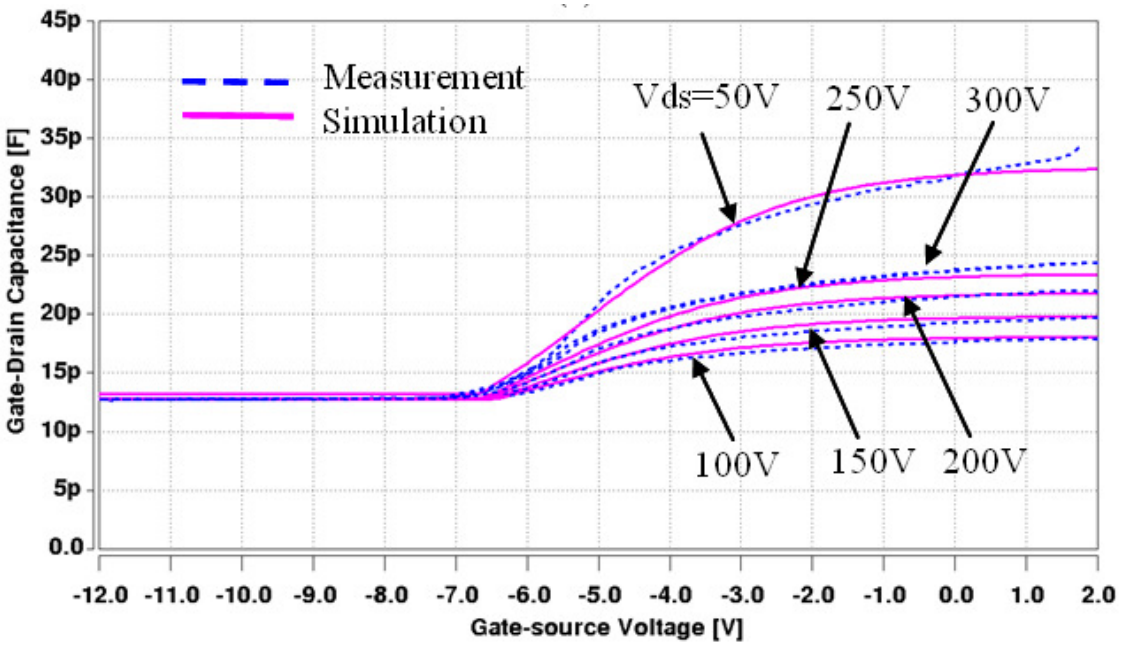
Figure 6-21is a comparison of the measured (dashed) and simulated (solid) C_{gs} values over a range of bias conditions that were obtained by sweeping V_{gs} from 2 V to -12 V and stepping V_{ds} from 50 V to 300 V. In this plot the onset of drain inversion at negative V_{gs} results in a large increase of C_{gs} as is expected from standard MOS theory [45].

Figure 6-22 shows simulated (solid) and measured (dashed) C_{ds} curves as a function of V_{ds}. Measured results indicate that C_{ds} does not vary much with V_{gs}. The step in the measured data is reproduced in the simulation data at approximately the same V_{ds}. Most likely, this step feature is due to the full depleted in the p strip.

Figure 6-23 shows the comparison between the measured data and the simulated data of the junction capacitance of the body diode of CoolMOS™.



(a)



(b)

Figure 6-19 Gate-Drain capacitance versus gate-source voltage of the 650 V, 60 A (0.57 cm^2) CoolMOS^{TM} at 25 ^{o}C for drain-source voltage (a) at 0 V, 5V, 10 V, 20 V, 30 V, and 40 V; and (b) at 50 V, 100 V, 150 V, 200 V, 250 V, and 300 V

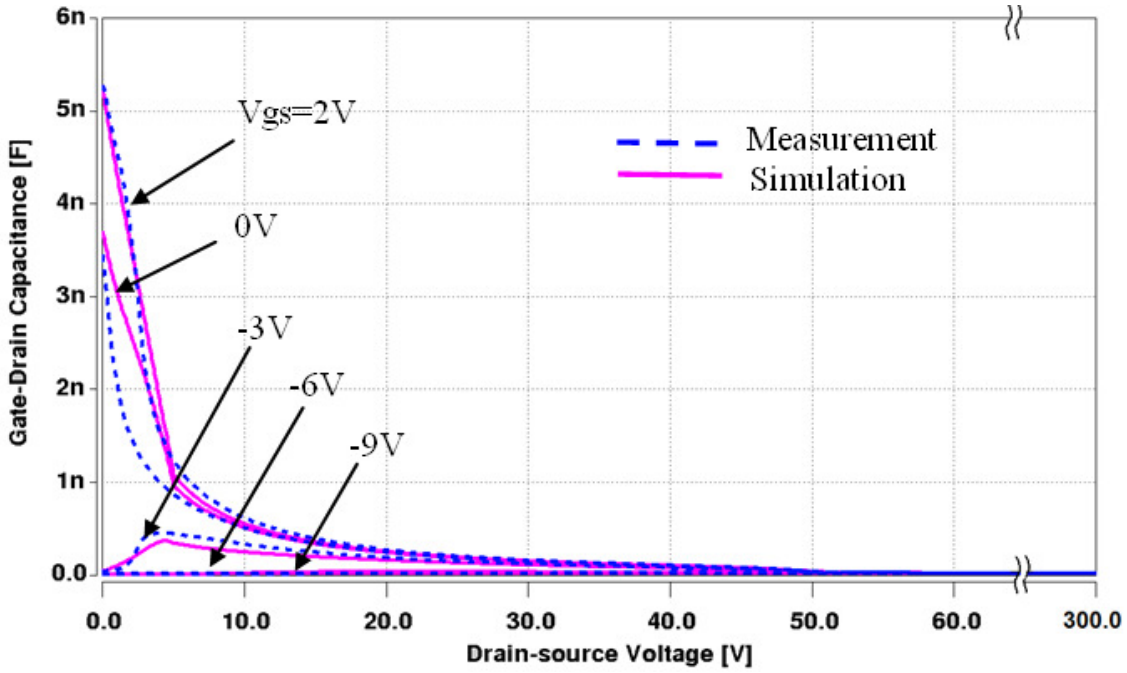


Figure 6-20 Gate-Drain capacitance versus drain-source voltage of the 650 V, 60 A (0.57 cm^2) CoolMOS^{TM} transistor at 25 ^{o}C for drain-source voltage sweeping from 0 V to 300 V by condensing V_{ds} between 60 V to 300 V

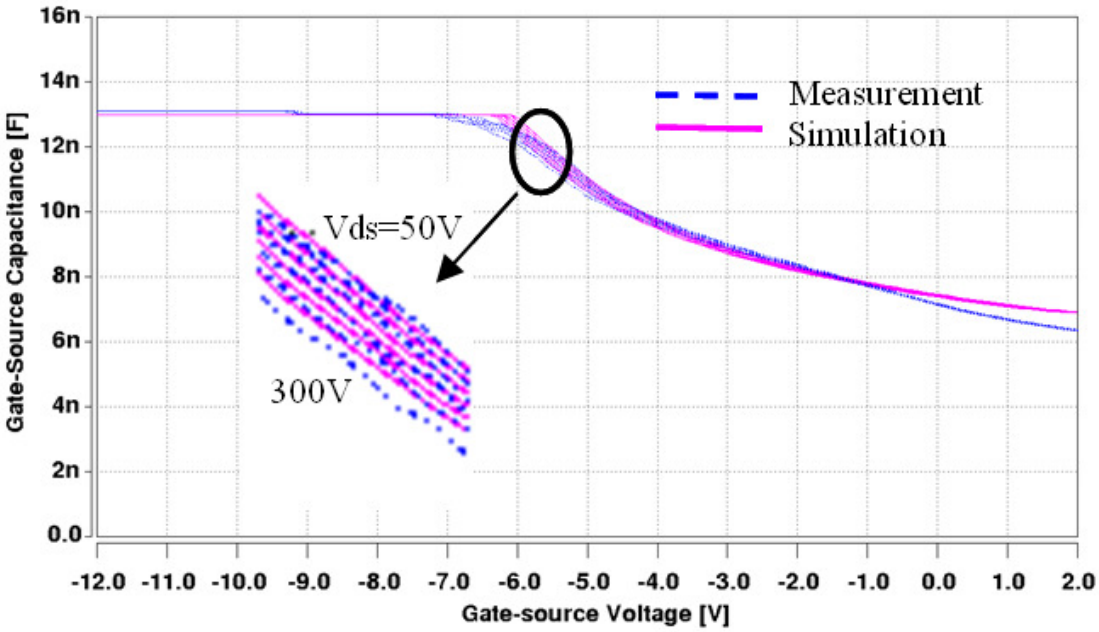


Figure 6-21 Gate-Source capacitance versus gate-source voltage of the 650 V, 60 A (0.57 cm^2) CoolMOS^{TM} transistor at 25 ^{o}C for drain-source voltage at 50 V, 100 V, 150 V, 200 V, 250 V, and 300 V with zoomed-in plot

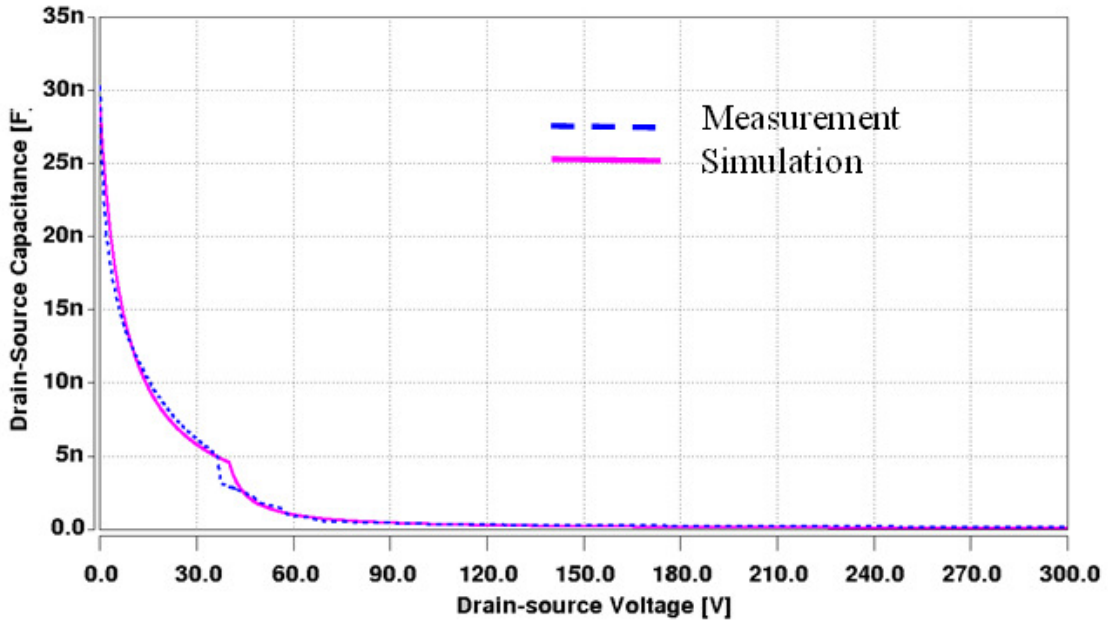


Figure 6-22 Drain-Source capacitance versus drain-source voltage of the 650 V, 60 A (0.57 cm^2) CoolMOS^{TM} transistor at 25 ^{o}C

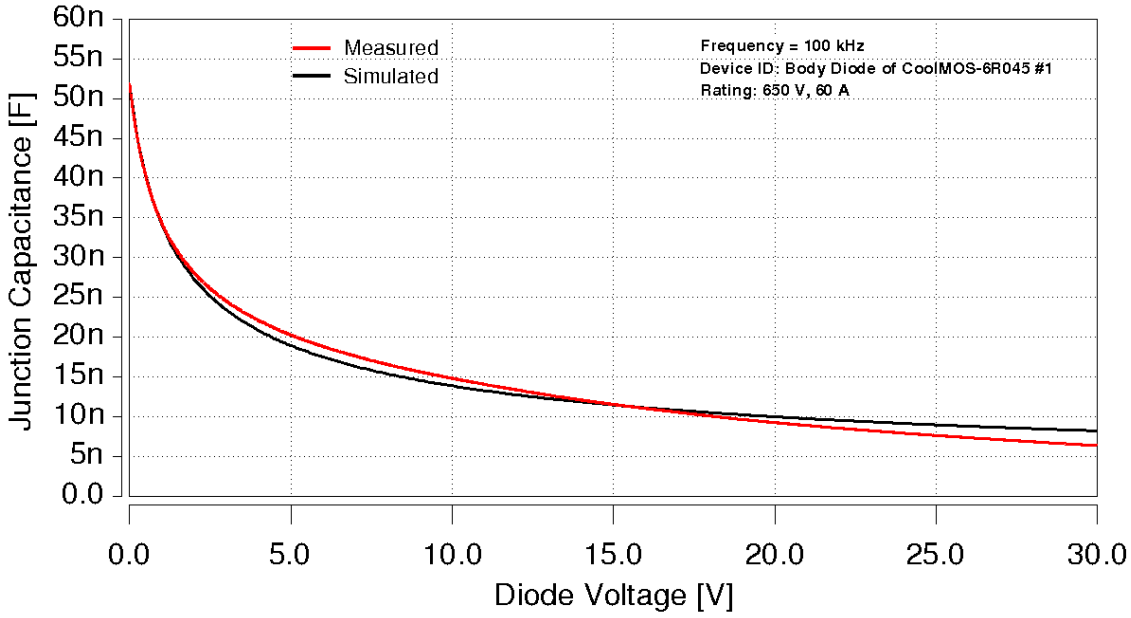


Figure 6-23 Comparison of junction capacitance of CoolMOS^{TM} body diode

6.8.3 Gate Charge Characteristics

The previous results have mainly demonstrated the model validation in the non-conducting state. Figure 6-24 shows the comparison between measured data and the simulated data for gate charge characterization.

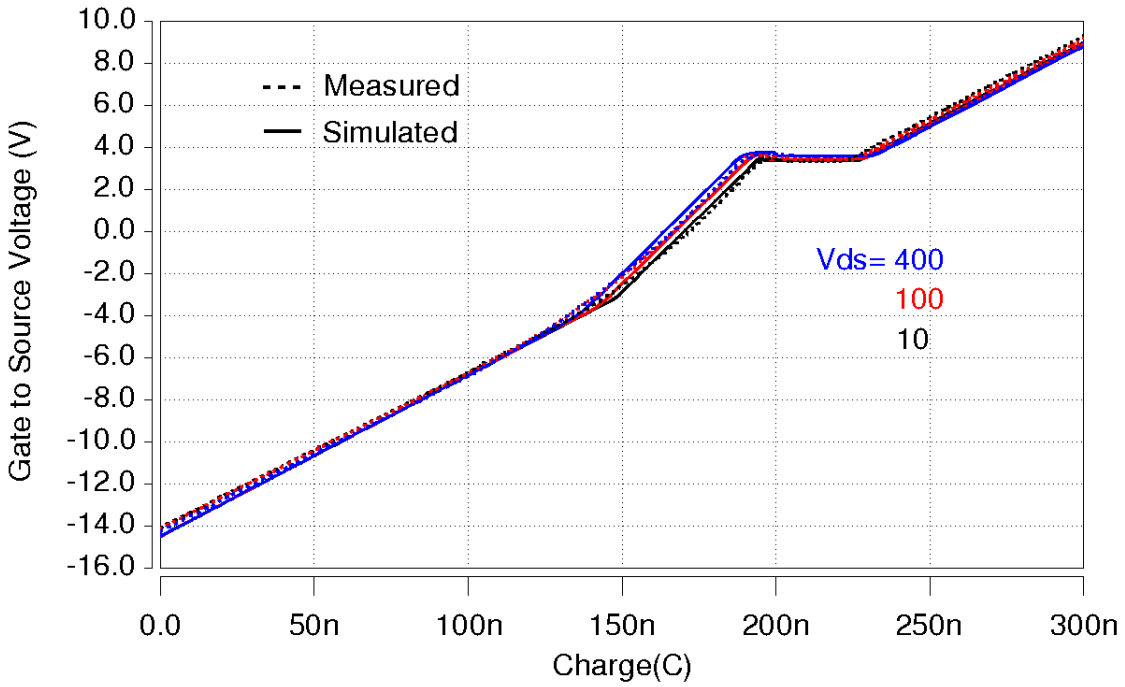


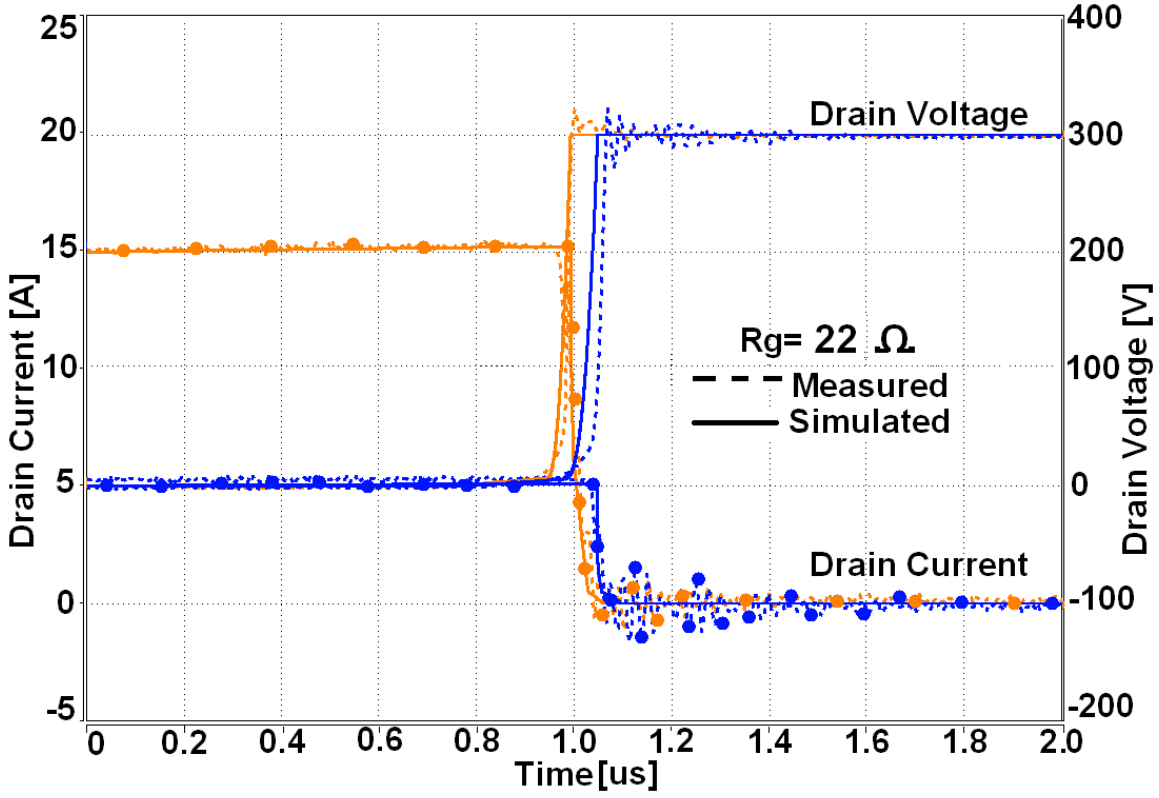
Figure 6-24 Gate charge results of the 650 V, 60 A (0.57 cm^2) CoolMOS^{TM} transistor at 25 ^{o}C

6.8.4 Inductive Switching Tests

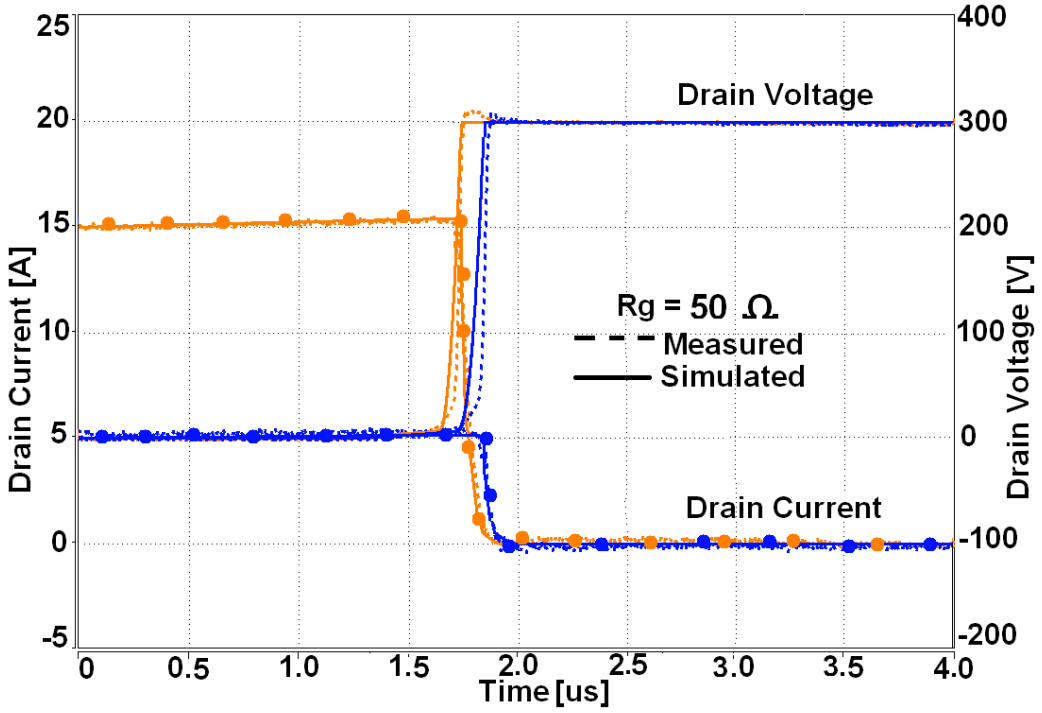
Inductive switching tests were performed using a well-characterized double-pulse test system. In the beginning, the CoolMOS^{TM} body diode was used as the freewheeling diode in the test circuit. However, it introduced excessive noise during device turn-on, which eventually damaged both devices unexpectedly when the test was being performed beyond the 100 V level. A commercial Si Schottky diode (600 V, 55 A) was then

employed as the freewheeling diode, and it performed adequately for the rest of the switching tests.

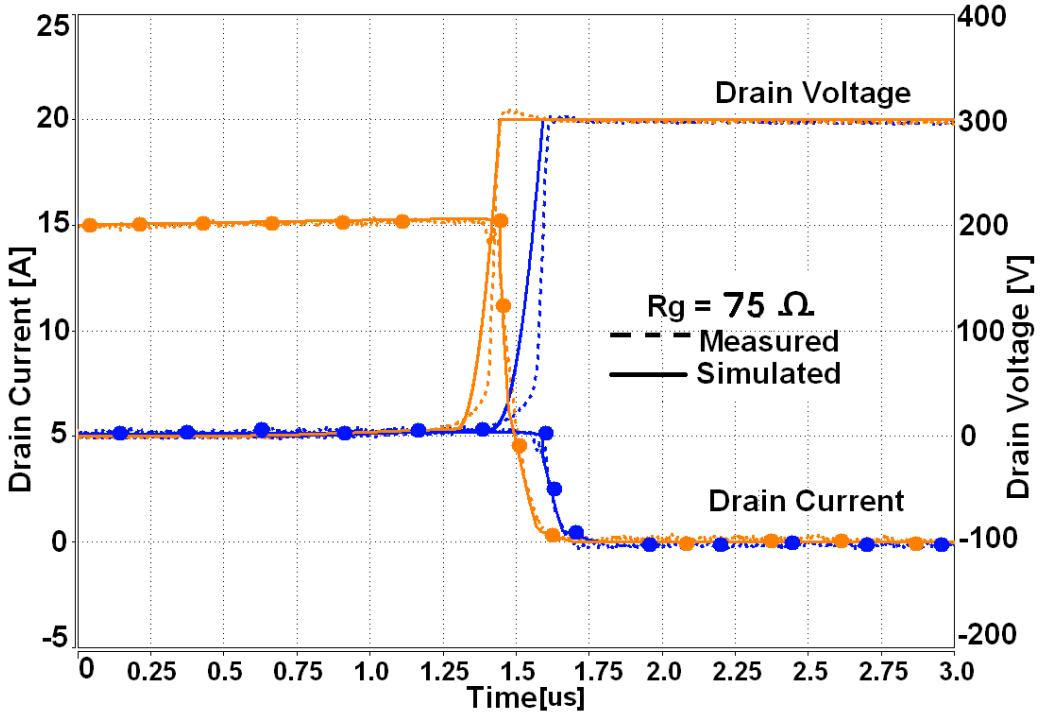
The gate resistor R_g was varied to provide different turn-off speeds for the devices. Figure 6-25 shows the simulated (solid) and measured (dashed) inductive switching turn-off waveforms of the drain current (with dots) at 5 A and 15 A, respectively, and the drain voltage clamped at 300 V at 25 ^{o}C for (a) R_g = 22 Ω; (b) R_g = 50 Ω; and (c) R_g = 75 Ω. Figure 6-26 illustrates the comparison between the measured data and the simulated data for the gate voltage (top) as well as the drain current at 15 A and the drain voltage at 300 V (bottom) using three different R_g (22 Ω, 50 Ω, and 75 Ω) at 25 ^{o}C.



(a)



(b)



(c)

Figure 6-25 Simulated (solid) and measured (dashed) inductive switching turn-off waveforms of drain current (dotted) and drain voltage at 25 °C for (a) R_g = 22 Ω; (b) R_g = 50 Ω; and (c) R_g = 75 Ω

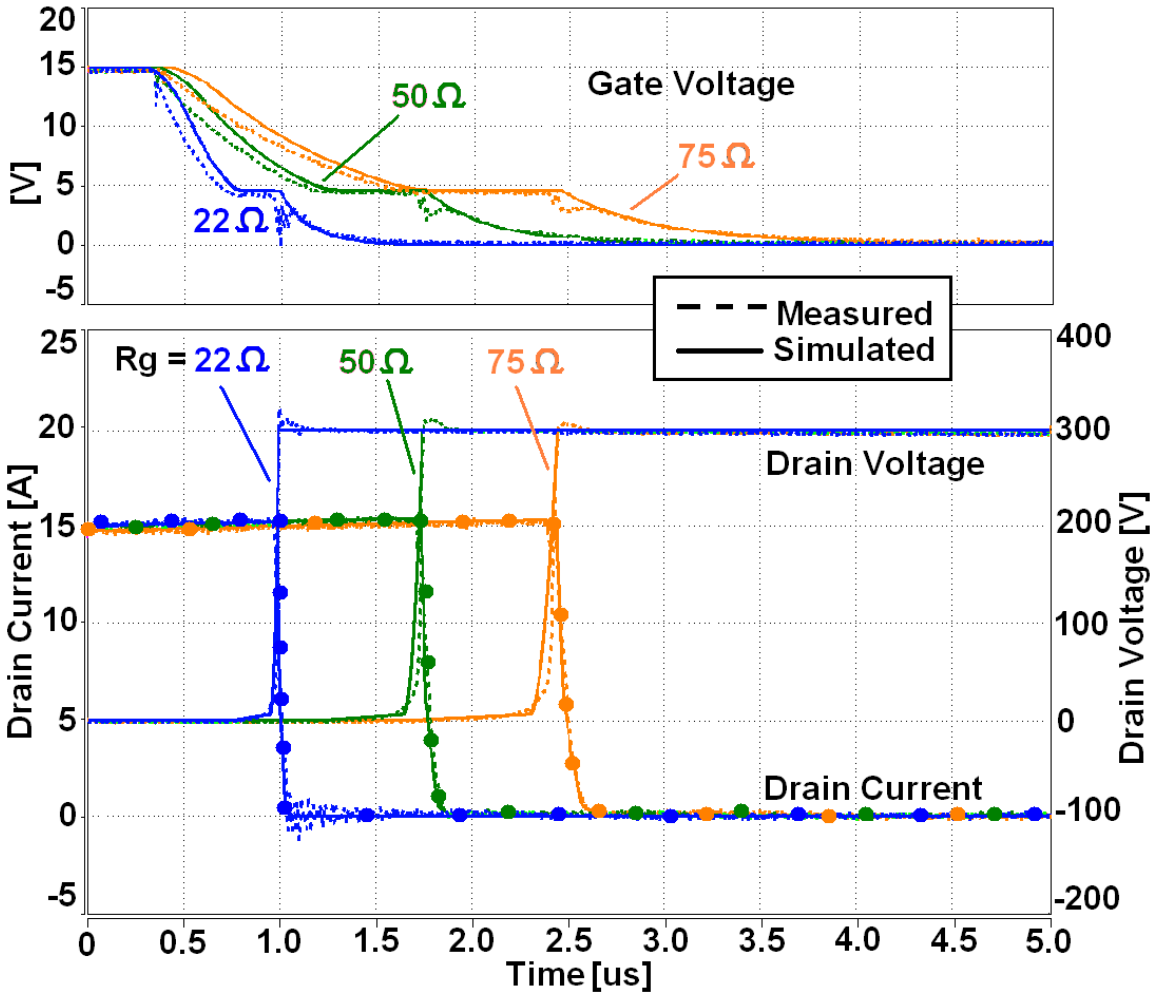


Figure 6-26 Simulated (solid) and measured (dashed) inductive load switching waveforms of gate voltage (top); and drain current at 15 A (with dots) and drain voltage at 300 V for R_g = 22 Ω, 50 Ω, and 75 Ω at 25 °C

Chapter 7 Conclusions and Future Work

This chapter summarized the entire dissertation and discusses some ideas for the future work.

7.1 Conclusions

This work presents device models for power diodes and the power CoolMOS^{TM} transistor. The power diodes studied in this work are the 10 kV SiC JBS diode, the 45 V Si Schottky diode, the 10 kV SiC PiN diode, the 600 V SiC Schottky diode, and the 600 V Si PiN diode. The first two power diodes (10 kV SiC JBS and 45 V Si Schottky) are employed in the DARPA HPE projects; and the last two devices (600 V SiC Schottky and 600 V Si PiN) are employed in the Electrical Vehicle project. The 600 V Si CoolMOS^{TM} transistors are also employed in the Electrical Vehicle project as main switches paralleled with IGBT.

For the power diode model, model equations along with the parameter extraction sequence applicable to Schottky/JBS, and PiN diode were presented. A new physics-based model of the reverse blocking characteristics for power Schottky/JBS diodes was developed by including the thermionic-emission mechanism in the low-bias range. The new model was implemented in the Saber circuit simulator as an enhancement to the current power diode model. An automated software package called DIode Model Parameter extrACtion Tools (DIMPACT) was developed by incorporating the power diode model equations. This software tool enables rapid development and validation of device component models in Saber for various types of Si and SiC power diodes. It

provides a method to extract the necessary modeling parameters for four classes of power diodes: (a) Schottky diodes, which offer high switching speed but suffer from high leakage current; (b) PiN diodes, which offer low leakage current but suffer from slow reverse recovery switching characteristics; (c) Junction barrier Schottky (JBS) diodes, which take advantage of p-n grids and offer low leakage current; and (d) Merge PiN Schottky (MPS) diodes, which combine the advantages of Schottky and PiN diodes to offer Schottky-like on-state and switching characteristics and PiN-like off-state characteristics. The enhanced power diode models constructed using the extracted parameters from DIMPACT are validated over temperature for both static and transient characteristics.

The power MOFET model applicable to the CoolMOS^{TM} transistor was presented in this work. The CoolMOS^{TM} transistor demonstrates similar on-state performance to that of the conventional power MOSFET while having a much lower on-resistance without sacrificing the blocking capability. Model parameters were extracted in sequence using the IGBT model parameter ExtrACtion tools (IMPACT) software. An enhanced method for modeling the inter-electrode capacitances of super-junction power MOSFET devices has been developed and validated with experimental results. By working with the actual charge distribution inside the CoolMOS^{TM} capacitors, a numerical model was established as a first step. Further simplifications and linearization were then performed to transfer the numerical model into a Saber-compatible model that even improves the accuracy, especially in the transition range from *accumulation* to *depletion*. Newly derived model equations were implemented in Saber which was used to validate the CoolMOS^{TM} model dynamic behaviors. The comparison between the simulated data with the measured

results validates the accuracy of the new physical model. The model was also validated for the forward conduction here over a wide temperature range. The results demonstrate good agreement between the model and experiment.

7.2 Future Work

The device models for the 600 V Si PiN diode, the 600 V SiC Schottky diode, and the 650 V Si CoolMOS^{TM} are being used in the inverter in the Electrical Vehicle project. Future work listed in the following can be carried out.

- There is another important power device (Si IGBT) needs to be modeled in order to perform the complete circuit simulation in the Saber simulator. This IGBT is used in parallel with CoolMOS^{TM} as the other main switch as described in chapter 1.
- This dissertation presents the electro model of the power devices. The compact device model needs to combine the electro model with the thermal model to get a complete device model in order to perform the circuit simulation.
- After acquiring the electrothermal device models in the Electrical Vehicle project, a circuit and system level simulation needs to be performed using these device models to test their accuracy and applicability.
- Apply the model developed for the CoolMOS^{TM} transistor to other superjunction power MOSFETs.

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