High Temperature SiC Embedded Chip Module (ECM) with Double-Sided Metallization Structure

by

Jian Yin

Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical and Computer Engineering

Dr. Jacobus Daniel van Wyk, Chair
Dr. Zhenxian Liang, Committee Member
Dr. Willem G. Odendaal, Committee Member
Dr. Guo-quan Lu, Committee Member
Dr. Elaine P. Scott, Committee Member

December, 2005
Blacksburg, Virginia

Keywords: High temperature, embedded chip module, electronic packaging, thermal analysis, thermo-mechanical analysis, integrated power electronics module, 3-D

High Temperature SiC Embedded Chip Module (ECM) with Double-sided Metallization Structure

Jian Yin

Abstract

The work reported in this dissertation is intended to propose, analyze and demonstrate a technology for a high temperature integrated power electronics module, for high temperature (e.g those over 200^{o}C) applications involving high density and low stress.

To achieve this goal, this study has examined some existing packaging approaches, such as wire-bond interconnects and solder die-attach, flip-chip and pressure contacts. Based on the survey, a high temperature, multilayer 3-D packaging technology in the form of an Embedded Chip Module (ECM) is proposed to realize a lower stress distribution in a mechanically balanced structure with double-sided metallization layers and material CTE match in the structure.

Thermal and thermo-mechanical analysis on an ECM is then used to demonstrate the benefits on the cooling system, and to study the material and structure for reducing the thermally induced mechanical stress. In the thermal analysis, the high temperature ECM shows the ability to handle a power density up to 284 W/in^3 with a heat spreader only 2.1x2.1x0.2cm under forced convection. The study proves that the cooling system can be reduced by 76% by using a high temperature module in a room temperature environment.

Furthermore, six proposed structures are compared using thermo-mechanical analysis, in order to obtain an optimal structure with a uniform low stress distribution. Since pure Mo cannot be electroplated, the low CTE metal Cr is proposed as the stress buffering material to be used in the flat metallization layers for a fully symmetrical ECM structure. Therefore, a chip area stress as low as 126MPa is attained.

In the fabrication process, the high temperature material glass and a ceramic adhesive are applied as the insulating and sealing layers. Particularly, the Cr stress buffering layer is successfully electroplated in the high temperature ECM by means of the hard chrome

plating process. The flat metallization layer is accomplished by using a combined structure with Cr and Cu metallization layers.

The experimental evaluations, including the electrical and thermal characteristics of the ECM, have been part of in the study. The forward and reverse characteristics of the ECM are presented up to 250^{o}C, indicating proper device functionality. The study on the reverse characteristics of the ECM indicates that the large leakage current at high temperature is not due to the package surrounding the chip, but chiefly caused by the Schottky junction and the chip passivation layer. Finally, steady-state and transient measurements are conducted in terms of the thermal measurements. The steady-state thermal measurement is used to demonstrate the cooling system reduction. To obtain the thermal parameters of the different layers in the high temperature ECM, the transient thermal measurement is applied to a single chip ECM based on the temperature cooling-down curve measurement.

Acknowledgement

I would like to express my deepest gratitude to my academic advisor Prof. J. Daan van Wyk for providing me with a great research opportunity. Without his unconditional guidance and support, this dissertation would never have come into existence. I am indebted to my doctoral committee members: Dr. Zhenxian Liang, Dr. W. G. Odendaal, Dr. Guo-quan Lu and Dr. Elaine P. Scott. I owe them a special note of appreciation for their thoughtful guidance and constant encouragement.

I am grateful to Center for Power Electronics Systems (CPES) at Virginia Tech for funding this research and providing research facilities. Special thanks are due to our lab manager Dan Huff for his continuous supports throughout my research projects, as well as my research group fellows: Rengang Chen, Lingyin Zhao, Jinggen Qian, Jing Xu, Michelle Lim, Yan Liang, Chucheng Xiao, Johan Strydom, Ning Zhu and Wenduo Liu.

Many thanks to the people for their great help and invaluable advises: Yingfeng Pang, Manu Mital, Zhiye Zhang, Mo Wu, Bryan Dickerson, Sihua Wen, John Bai, Bing Zhang, and Yu Meng. I also need to thank all my other CPES friends for their friendship and help.

I owe my sincere appreciation to my family and relatives who have supported and encouraged me over the years. I am sincerely grateful to my wife Ju Wang for her inspired love and constant support during all these years. Finally, I want to extend my profound appreciation to my beloved parents for their love, affection, and invaluable support.

Table of Contents

Nomenclature

A	Area, m^2
c	Specific heat, J/Kg-K
d	Thickness, m
I	Current, A
k	Thermal conductivity, W/m-K
Q	Power loss, W
R_E	Electrical resistance, Ω
R_{Th}	Thermal resistance, °C/W
t	Time, s
T	Temperature, °C
V	Voltage, V
ρ	Density, Kg/m^3
ν	Poisson's ratio
σ	Stresses, MPa

Acronyms

AC	Alternative current
CPES	Center for power electronics systems
CTE	Coefficient of thermal expansion
DBC	Direct bonded copper
DC	Direct current
ECM	Embedded chip module
ESC	Electronic System Cooling
FEM	Finite element method
GaN	Gallium nitride
HDI	High density interconnect
HFET	Heterostructure field effect transistor
IC	Integrated circuits
IGBT	Insulated gate bipolar transistor
IPEM	Integrated power electronics module
MEMS	Micro electro mechanical systems
MOCVD	Metal organic chemical vapor deposition
MOSFET	Metal oxide semiconductor field effect transistor
POL	Power overlay
PSD	Particle size distribution
SiC	Silicon carbide

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Current Trends in High Temperature Power Electronics Packaging

There has been a growing demand in recent years for high temperature power electronics suited to the harsh environments encountered around combustion engines in automobile and aircraft environments.[1] When a module has a high temperature capability, it is not only suitable for a harsh thermal environment, but this will also lead to a reduction in cooling requirements to a room temperature ambient. The availability of silicon carbide (SiC) and Gallium Nitride (GaN) devices have expanded the possibilities for high temperature, hybrid circuit designs. However, the packages supporting such devices are inadequate in electrical interconnection, thermal management and reliability under high-temperature operations/environments. So the advancement of packaging technology tailored for high temperature applications is a necessity. Although conventional packaging technologies, such as wire bond technology and pressure contact technology, pushed the temperature up to 350^{o}C, these technologies employ the unbalanced structure or CTE mismatch materials, which introduces high mechanical stresses in the structure and can cause failure or reliability problems. Additionally, these technologies, due to their discrete packaging structure have reached their limits to reduce parasitic inductance, enhance efficiency and improve thermal performance. Therefore, it is necessary to develop a three-dimensional high temperature module with a mechanically balanced structure, as well as match the CTE of the materials in the package for improving its long-term reliability performance. The three-dimensional multilayer packaging technologies has the potential to break the existing limits. Since the three-dimensional structure provides flexibility to design the multilayer module and also shortens the electromagnetic and thermal paths attributed to wire bond, it has evident improvements in thermal performance, operating frequency and power density.

1.2 Aim of the Study

1.2.1 High Temperature Embedded Chip Module (ECM) Technology

While the mechanically balanced structure, as well as the material CTE match, is a necessity at high temperature and three-dimensional multilayer packaging technologies are the trend of the high temperature power electronics packaging, this study will develop a high temperature, multilayer 3-D packaging technology in the form of an Embedded Chip Module (ECM), to realize a lower stress distribution in a mechanically balanced structure with double-sided metallization layers and material CTE match in the structure. In addition, the single chip can be properly packaged for universal high temperature applications by means of ECM structure.

1.2.2 Research Work Covered in this Dissertation

In this dissertation, the survey of packaging technologies for high temperature including the wire bond technology, pressure contact technology and flip chip technology will be introduced in chapter 2. Three-dimensional multilayer packaging technologies are only introduced for normal temperature applications, since no high temperature 3-D technology is found. The reason to choose the high temperature Embedded Chip Module (ECM) technology is stated.

In chapter 3, the proposed high temperature Embedded Chip Module (ECM) is introduced with the essential improvements required for high temperature applications. After the introduction of the functions and requirements for high temperature applications, the sealing and insulation materials, metallization materials, chip and substrate selections of the high temperature Embedded Chip Module (ECM) are carefully investigated.

Chapter 4 presents the thermal analysis and theoretical behavior analysis of a packaged SiC chip at high temperature. The one-dimensional model as well as the three-dimensional FE model is introduced, and IDEAS simulation is employed to analyze the EMC at a room temperature ambient. Then the theoretical reverse characteristics of the SiC chip are given by analyzing the Schottky junction properties.

The thermo-mechanical analysis for a high temperature ECM is described in Chapter 5. The optimal structure for low mechanical stress in the package is obtained in this chapter.

The different structures with Cu metallization layers are compared to the case with Mo metallization layers. Although Mo is a good metallization layer candidate for high temperature EMC, pure Mo can not be implemented in the module by means of an electroplating process. To solve this problem, a Cr metallization layer is introduced as a buffering layer to reduce the mechanical stress, while the Cu metallization layer is used for the lateral current conduction. A fully symmetrical structure with combined use of Cr and Cu metallization layers are presented to achieve low mechanical stress in the chip area.

The eight-step fabrication process of the high temperature ECM is illustrated in chapter 6, including layout design, laser cutting process, screen printing process, sputtering process, photo masking process, electrical plating process, etching process and final cutting and assembling process.

Experimental evaluations in chapter 7, including electrical and thermal tests, are described. The electrical tests show the forward and reverse characteristics of the high temperature ECM. This module has been tested up to 267^{o}C. The module leakage currents at high temperature, due to the passivation layer, Schottky junction and package around the chip, are also studied. To obtain the thermal characterization and improve the thermal performance, the high temperature steady and transient thermal measurements are proposed and investigated.

Finally, a recommendation and conclusion are given in chapter 8. Suggested work for further improvement is presented as well.

Chapter 2

Survey of Packaging Technologies for High Temperature

2.1 Introduction

The survey of packaging technologies for high temperature will be introduced in this chapter to show the current status of the high temperature packaging technology. The wire bond technology, pressure contact technology, flip chip technology and normal temperature 3-D multilayer packaging technologies are investigated. And the reason to choose the high temperature embedded chip module technology is stated.

2.2 Current Packaging Technologies for Power Electronics Modules for High Temperature Applications

2.2.1 Wire-bond Technology

The wire-bond technology is the most widely used in chip packaging for high temperature applications [2]-[8]. For the normal temperature applications, large diameter Al wire bonding is used with Si power devices. However, at high temperatures the mechanical strength of Al decreases. Also, Al would be incompatible with the Au wire bond pads used on SiC die due to inter-metallic formation and Kirkendall voiding at high temperature. Large diameter (10mil) Au and Pt wire bonding is available for high temperature applications. Both require substrate heating. Au wire provides higher conductivity than Pt, but Pt has higher mechanical strength at high temperatures. Large diameter Au wire has been successfully bonded to both pads on the die and to the thick Au/Ni/Cu substrate metallization. At this point, Pt wire is only bondable to the substrate metallization [3].

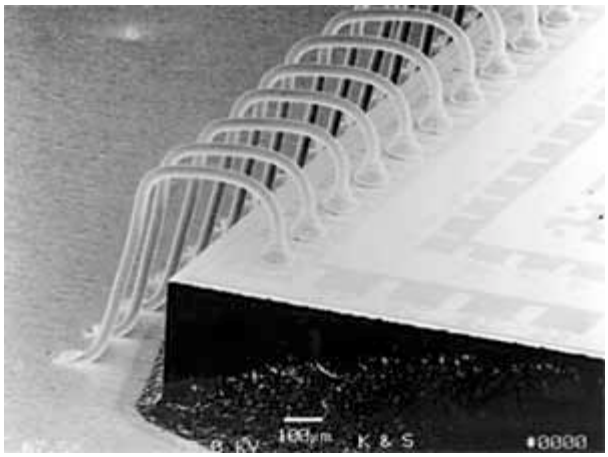
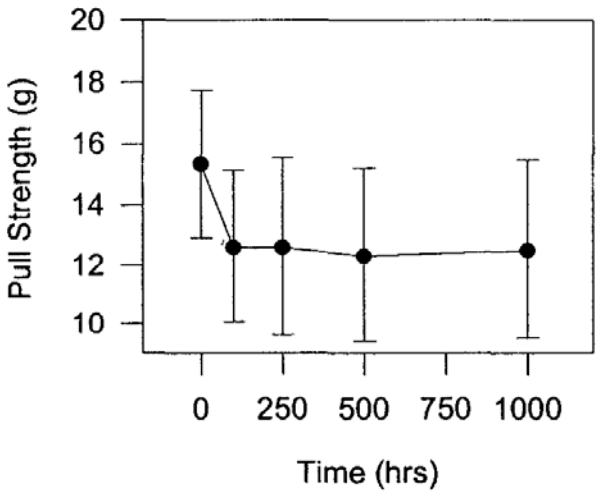


Fig. 2.1 25µm gold wire ball/wedge bonds as produced by a fully automatic production machine, bonding speeds approx. 5 wires/second

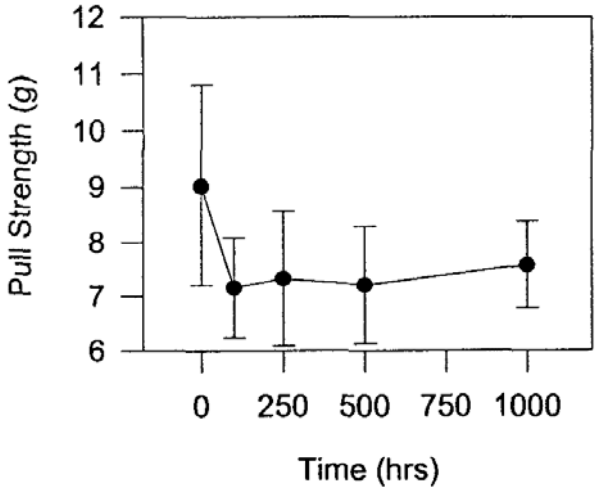
High temperature applications can weaken both the wire and the wire bond by annealing the wire and causing inter-metallic reactions at the bond site, respectively. Annealing increases the grain size in the wire, reducing the wire's strength and fatigue resistance. Inter-metallic reaction can lead to the formation of voids and brittle compounds that cause fatigue fracture at the bond interface. Inter-metallic formation is most often seen at temperatures exceeding 125 °C in Au wire/aluminum (Al) bond pad interconnects [2]. Other wire bond systems, such as Al wire/nickel (Ni) bond pad, have a slower rate of inter-metallic formation, and thus a higher allowable use temperature [6]. Temperatures in excess of 300 °C require monometallic wire-bond systems such as Au wire/Au bond pad.

Three different types of wire bonds were evaluated in [2] for use in silicon carbide based hybrid circuits at 500^{o}C. Small diameter (0.001") gold and platinum wires were tested for small signal applications and large diameter (0.010") platinum wire for high current carrying applications. Small diameter platinum wire was included in the study as an alternative to gold because of its higher tensile strength. The large diameter platinum wire was used in place of the more traditional large diameter aluminum wire. In both the platinum and gold wire a decrease in pull strength over time was experienced. This was not due to a weakening of the first or second bond but the annealing of the metal wire that

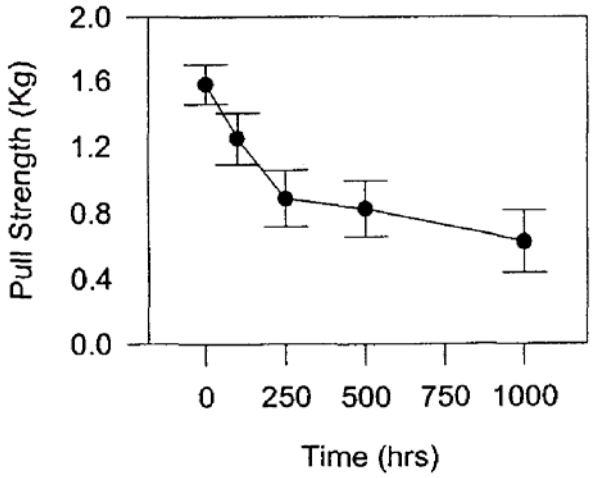
occurs at elevated temperatures (Fig. 2.2(a) and (b)). Pull tests on the large diameter wire bonds yielded strengths several times greater than conventional large diameter aluminum bonds, as shown in (c). However, due to the contact pad metallization stack-up, all circuit assemblies failed in about 250 hours. The contact pad in (d) shows where the contact metal has lifted from beneath a wire bond.



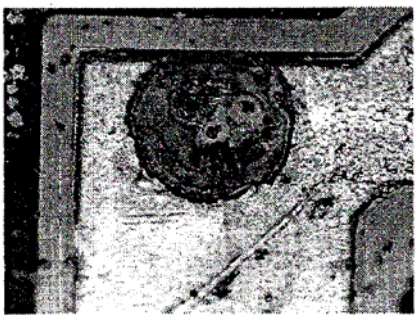
(a) Average pull strength of **1** mil gold wire bonds. Error bars are two standard deviations.



(b) Average pull strength of **1** mil platinum wire bonds. Error bars are two standard deviations.



(c) Average pull strength of **10** mil platinum wire bonds. Error bars are two standard deviations.



(d) Contact metal lifted from beneath a wire bond

Fig. 2.2 Pull strength comparisons for different wire bonds

Thick film metallization based wire-bond also is used in [3] for high temperature (up to 500°C) chip level packaging. Small diameter gold wire (0.001") was bonded to gold thick film printed pads by thermal-press wire bonding technique. The electrical resistance was studied at room temperature and 500°C versus accumulated testing time as shown in Fig.2.3. Although the resistances under all these conditions were desirably low and slightly decreased at an average rate of 2.7% over 1500 hour testing period, the wire-bond resistance under 500°C is about 2.5 times higher than the resistance at room temperature. This will limit its applications in high current and high temperature conditions.

Although the wire bond technology is well known and low-cost interconnect method, suitable for discrete device packaging, its unbalanced mechanical structure composed of the wire bonds at the top and the die attachment material at the bottom may produce high differential stress to cause failure at high temperature. In high temperature applications, the reliability of the wire bond technology is still a challenge and the resistance of the wire bond increases appreciably, which limits its applications for high current use. Additionally, its unbalanced mechanical structure leads to unbalanced thermal paths and limits the thermal cooling path from the wire-bond side, thus leading to a bulky package. For high frequency applications, the parasitic inductance due to the bond wires may be problematic.

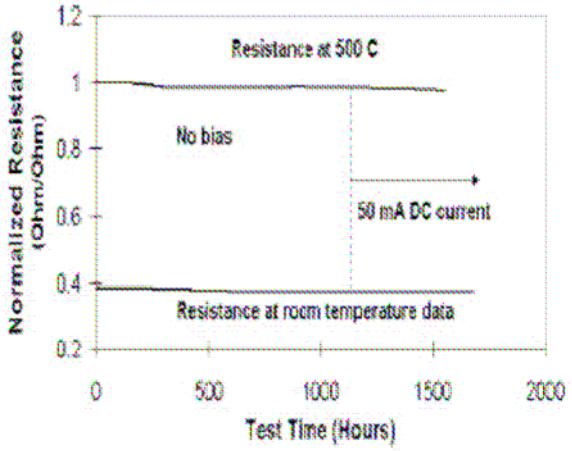
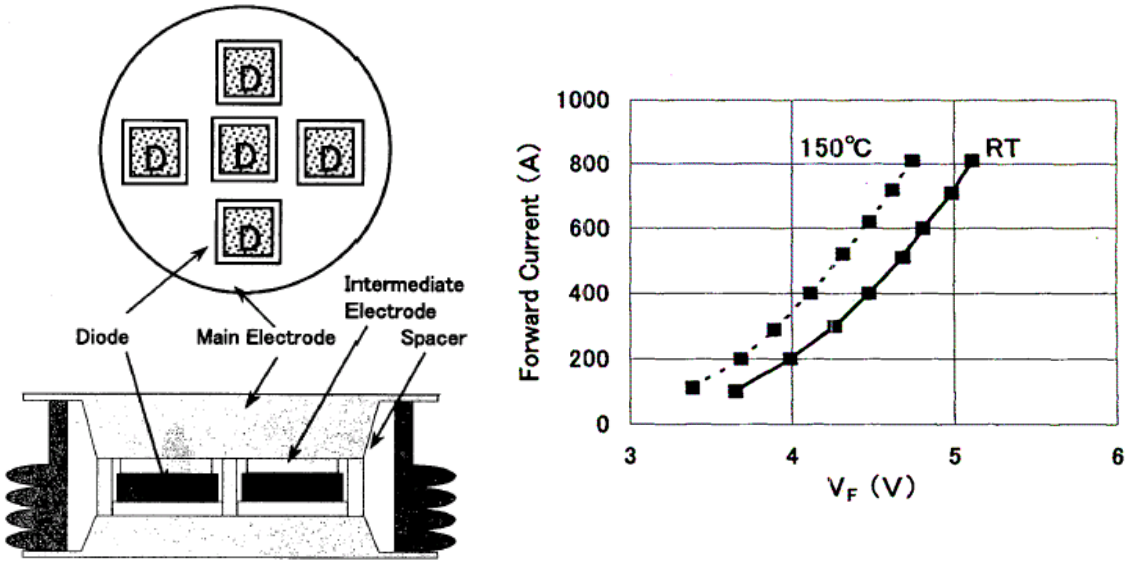


Fig. 2.3 Electrical resistance of 1 mil wire bond on room temperature and 500oC

2.2.2 Pressure Contact Technology

Pressure contact technology is another packaging technology for high temperature applications as in [9] - [12].

A 3kV 600A 4H-SiC high temperature diode module was developed in [9] by employing the pressure contact technology. Fig. 2.4 (a) shows a top and a cross-sectional view of a designed pressure contact flat package diode module, which includes 5 diode chips. Both cathode and anode main electrodes are composed of copper alloy, and the intermediate electrodes are composed of molybdenum, which acts to reduce the thermal expansion coefficient difference between SiC and copper alloy electrodes. Spacers are used for accurate chip arrangement and are composed of ceramics. The 5-diode module showed the low leakage current and forward voltage, however, the module was only tested up to 150°C as shown in Fig.2.4 (b) and the long-term reliability characterization was not considered in this paper.

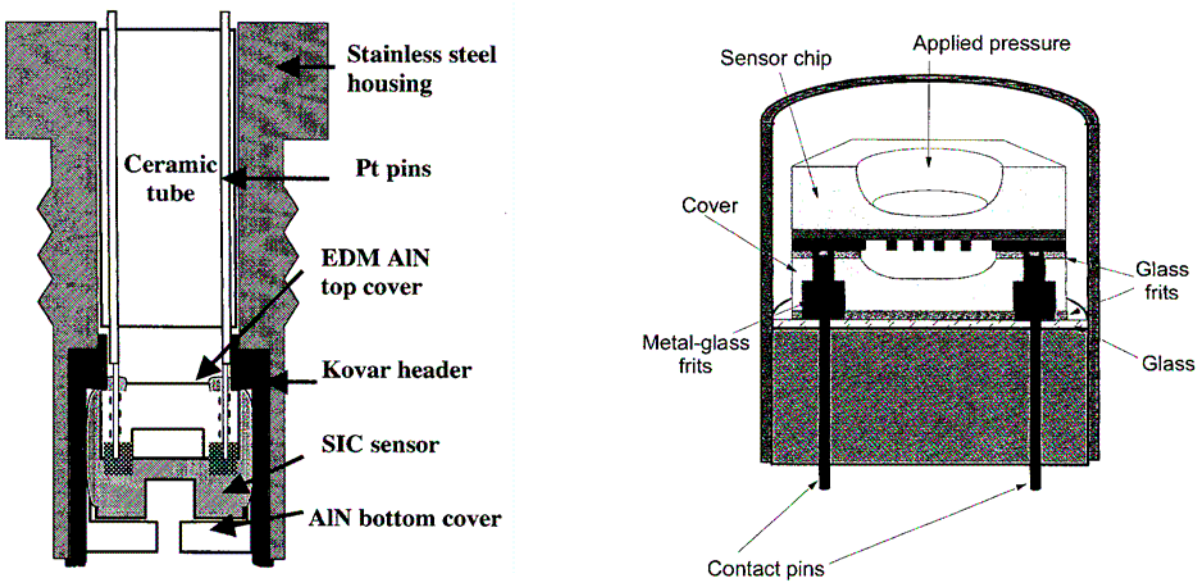


(a) Experimental setup (b) Module testing results

Fig. 2.4 Top and cross-sectional views of a designed pressure contact flat package diode module

A hermetic 6H-SiC pressure sensor package was introduced in [10] and [11]. The structure of the pressure sensor package in [10] is shown in Fig. 2.5 (a). An AlN substrate at the bottom serves as a receiving platform for the SiC sensor. The bottom AlN substrate also serves as the first level of protection of the sensor from harmful particulates in the

high temperature environment. The bottom substrate, together with the top substrate, which is also made from the AlN, forms a sandwich construction to protect the sensor. Because the top and bottom substrates are made of the same material (AIN) with thermo-mechanical properties similar to that of the SiC sensor, the mechanical stresses due to the thermal expansion mismatch between the substrates and the die are significantly reduced to harmless levels. The packaging technique allows a die (or a die array) to be intimately attached to next level of metallization via a through-hole in the substrate. This approach eliminates wire bonds, which are known to be the weakest links, and makes the packages more reliable. The packaged SiC MEMS pressure sensor was operated at 600^{o}C and 200psi, however, the long-term reliability characterization hasn't been performed. A Similar structure of the 6H-SiC pressure sensor package [11] is shown in Fig.2.5 (b). The wire bonds were avoided in the structure and electrical contacts were made using a metal-glass frits mixture. This pressure sensors packaged with this method were tested for pressures up to 1000psi and at temperatures up to 500°C, however, the reliability characteristics was not given.



(a) (b)

Fig. 2.5 Schematic drawing of the packaged sensor structure

Despite the merits, the largest disadvantage of pressure contact technology is its higher manufacturing cost and the more complicated mounting arrangement to maintain pressure. Also, limited research work has been published on the effects of thermo-mechanical stresses on these pressure contacts during actual operation of the devices and hence, the reliability of these modules is still under investigation. Finally, the pressure contact technology can only package the active components and is one type of discrete packaging technology.

2.2.3 Flip Chip Technology

Flip chip technology [13] [14] is another available technology for high temperature applications. The key material in the structure is the solder balls, which should be a high temperature material. The gold bump used in the GaN based microwave power amplifiers [13] to replace the solder ball shows one possible approach to enable the flip chip technology to be used for higher temperature applications. As shown in Fig.2.6, the HFET epilayers structures in this study were grown over basal plane sapphire or insulating SiC substrates using the low-pressure metal organic chemical vapor deposition (MOCVD) technique. The devices were then FC bonded onto 500-m-thick AlN substrate using gold bumps. No-flow epoxy underfill was then used to fill the air gap between the chip and the AlN substrate. This module operated at the maximum active region temperature of 250^{o}C. However, the GaN based structure is not purposely designed for high temperature applications and its maximum temperature is limited by the epoxy underfill material. Although the gold bump can be used to replace the solder ball for high temperature applications, the gold bump requires a process temperature up to 1000 ^{o}C and the high cost is another large concern for it.

Another high temperature flip chip example is shown in Fig. 2.7. [14] Two SiC PIN diodes were flipped over and attached to AlN substrate, with the metal leads for topside connections. The high temperature solder was used for leads and die attachment materials. The module was operated up to 250^{o}C; however, the heat dissipation ability was reduced due to the long lead connections and the insulating silicone material. The long term reliability test has not been performed in this research.

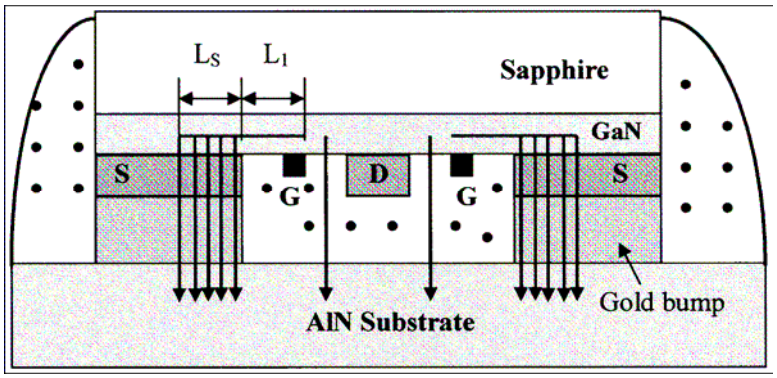


Fig. 2.6 GaN based flip chip structure

Simplified Diode Package in Oil

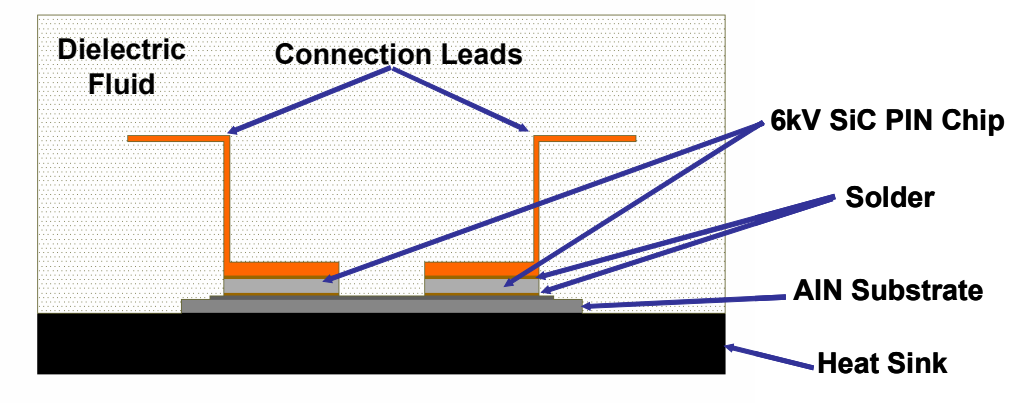


Fig. 2.7 12KV SiC PIN diodes with high voltage, high temperature packaging

The unbalanced mechanical structure at the top and bottom sides of the chip may cause high thermally induced differential stress in high temperature applications. Both the gold pump and high temperature solder as chip attachments have much higher CTE than the SiC chip. So the CTE mismatch and unbalanced mechanical structure in the module can cause high mechanical stress and finally result in reliability problems. The high process temperature for both cases is also a disadvantage. Besides, this technology is still one type of discrete packaging technology.

2.2.4 Candidates of Three-dimensional Multilayer Packaging Technologies for High Temperature Applications

2.2.4.1 Power Overlay (POL) Technology

The Power Overlay (POL) Technology, developed at General Electric Company, is a high-density-interconnect (HDI) process for the interconnection of multichip modules. This technology has an interconnect layer built on top of the semiconductor devices and base plates. The schematic shown in Fig. 2.8 illustrates the section view of the POL design concept. [15] - [17]

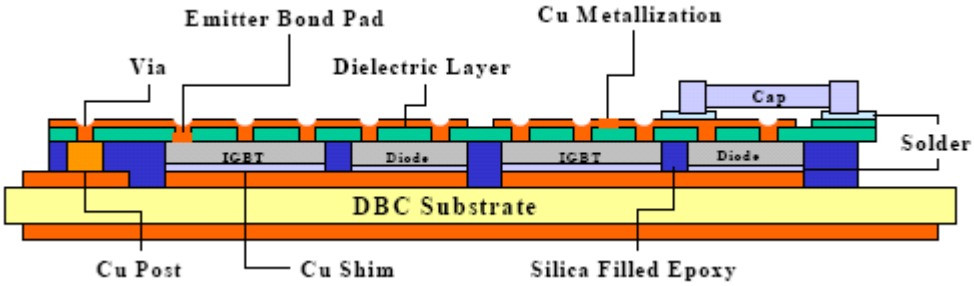


Fig. 2.8 A cross-sectional schematic of a GE-POL structure [15]

Some of the anticipated advantages of the POL structure are described as follows:

- Elimination of wire bonds with metallurgical interconnections improving reliability;
- Better electrical performance through reduced interconnection parasitics;
- Improved thermal performance via reduced numbers of thermal interfaces and two sided heat removal;
- Reduced profile and more flexible packaging options for stacking additional circuits;
- Limited number of processing steps compared with other 3d packaging options; and
- Low cost.

The POL process utilizes power semiconductor devices (IGBT, MOSFET, and diode) that are mounted to the backside of a dry polymer film, which is a suitable dielectric material, such as Kapton. The Kapton tape has pre-formed vias with specific pitch and size. These vias serve as electrical paths for circuit functioning. Metallization on the vias (making contact to the devices) and the polymer dielectric is achieved through a combination of sputtering and plating process. First, a barrier and adhesion layer of Ti (typically 1000Å) is sputtered followed by a seed layer of copper (1000Å). On top of the

seed copper layer, a five mil thick copper layer is deposited by electroplating. This thick copper layer provides a low-loss interconnection of the power devices. Finally, a thick photoresist is applied on the thick copper to pattern etch conductor pads on the electroplated metallization. DBC substrates are attached on the backside of devices through soldering. More layers can be built up repeatedly to realize a multilayer interconnect structure. Low profile passive components can also be embedded into the overlay. The inherent multiplayer nature of POL will facilitate the integration of gate drive and other circuits into a three-dimensional package.

However, GE-POL structure has not been successfully tested for high-power applications; furthermore, the key material, Kapton, is not a high temperature material and will fail at about 250^{o}C. Therefore, POL technology is difficult to push to high temperature.

2.2.4.2 The Flip-chip on Flex Technology for the Construction of 3-D Packaged IPEMs

The flip-chip technology firstly emerged in IC as low-cost, high density, and reliable interconnections [18] [19]. This technology eliminates wire-bonds and utilizes solder joints that are capable of carrying large currents for interconnecting devices. The low-profiled solder joints introduce smaller parasitic inductance and capacitance than conventional wire-bond connections. Also, the use of an underfill dielectric material between the devices and substrate helps to achieve protection and stress reduction in the devices as well as improve heat transfer. The flip-chip on flex technology extends flip-chip and flex circuitry technologies to power electronics packaging and takes advantages of these two technologies. [20] - [23]

As shown in Fig.2.9, the bottom layer of this multilayer structure, a direct-bond copper (DBC) substrate, is used to attach the power chips. The DBC substrate serves three purposes: providing a thermal path for flip-chip devices; providing an electrical path and completing the electrical layout; and supporting the robust assembly of the module. The top layer of the structure is a doubled-sided flexible copper-clad laminate, which is an adhesiveless composite of polyimide film bonded to copper foil. A novel triple-stacked solder bumping technique is used to connect the power chips to the flexible substrate with

a circuit pattern for gate-drive components. The devices are encapsulated in underfill polymer materials to reduce the thermo-mechanical stresses imposed on the solder joints. Finally, gate drivers and control circuits are built on top of the flex circuitry using either flip-chip or surface-mount technology. The structure would reduce the package and wire bond parasitics, and permit higher-frequency operation with increased conversion efficiency. The structure would also minimize thermal rise and completely encapsulate the chips and interconnection structure for a robust integrated module.

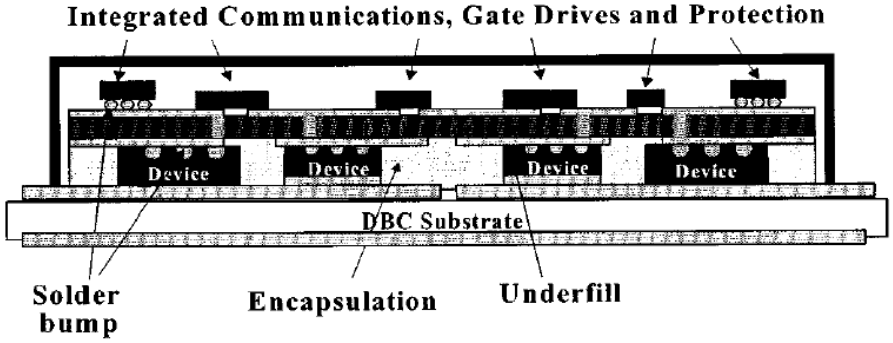


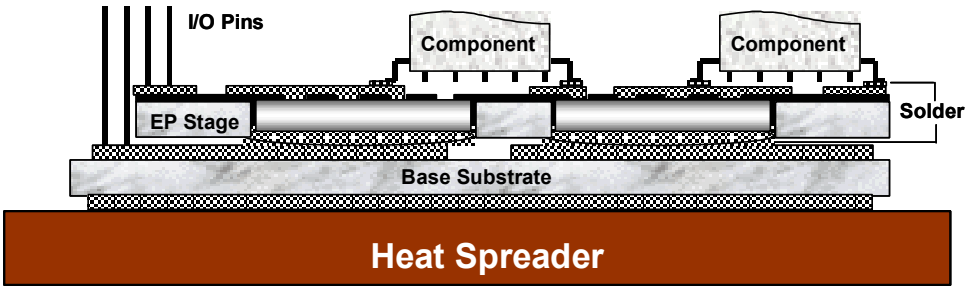
Fig. 2.9 Flip-chip on flex technology for the construction of 3-D packaged IPEMs

The flip-chip on flex technology realizes a three-dimensional structure and eliminates the wire bond connections to achieve smaller parasitic inductance. However, this technology relies on the solder balls for connections, which are not suitable for higher temperature (more than 350^{o}C) applications, even though the application of the solder ball is the main advantage in flip-chip on flex technology.

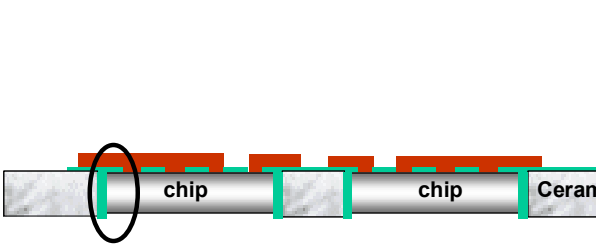
2.2.4.3 Embedded power technology

The main features of this integration technology, which differs from the other 3-dimensional packaging approaches are that the power chips are embedded in a special encapsulate structure, as well as all interconnections are metallgurically deposited. The main element is a MCM multilayer structure with compact metallization interconnects. It offers higher power density and performance. In the view of the process technology, low temperature hybrid techniques are developed to fabricate all structural layers. In addition,

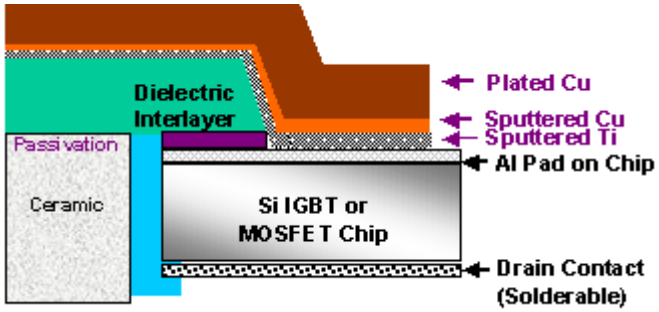
it has the capability of packaging all multilayer power electronics components such as hybrid drive/control circuits and integrated capacitors/ inductors. [24] - [26]



(a) Assembly of top components and bottom base substrate



(b) Integrated power chips stage



(c) Zoom-in cross-section view

Fig. 2.10 Embedded power technology

The embedded power stage, shown in Fig. 2.10 integrates multiple power chips into one compact component with further interconnection. It is composed of a flat ceramic frame, embedded bare power chips, dielectric interlayer and deposited metallization interconnection. This multilayer coplanar stacking construction provides not only the chip-level interconnect through metallurgical contact to aluminum pads on Si chips, but also carries the wiring for the top electronic circuitry. The ceramic frame or multichip carrier is provided with openings. The chips are mounted in these openings with adhesive polymer surrounding the chip edges. Such a flat surface provides a platform for the planar processing that is to follow. The interlayer dielectric is a kind of printed polymer with designed pattern screen, i.e., via holes corresponding to the Al pads of the chips. The deposited Cu pattern is employed as interconnect layer. As shown in Fig. 2.10 (c), the

metallization such as Ti-Cu or Cr-Cu deposited layers on Al pads of the semiconductor chip and polymer provide low film stress with good adhesion and electrical/thermal conduction. For carrying high current, a thick electro-plated (>5mils) Cu layer is deposited on the sputtered Cu seed layer. Then, the metallization layer is patterned to form the power and the control circuits and their I/O pads.

This integrated power chips stage provides a vertical interconnect structure due to the vertical semiconductor construction of the power chips (MOSFET and IGBT) in Fig.2.10 (b). The bottom sides of the chips, as drain or collector electrodes are usually metallized with a final solderable metal layer such as Ag or Au, and can be directly interconnected through soldering. The topside of the stage is of built interconnection which is designed to incorporate other electronic components through soldering (or surface mount).

Thus, a 3-D assembly structure, as shown in Fig.2.10 (a), is obtained. As in conventional multichip modules, a DBC (direct-bond-copper) base substrate is employed to provide a good electrical connection and excellent thermal path beneath the power chips. This substrate will be directly mounted on the heat spreader or/and heat sink for the necessary thermal management. After completing all interconnections the whole assembly will be encapsulated in a plastic case.

The technology features the building-up of interconnections on co-planar power chips embedded in a ceramic frame. Thus, an integrated power stage similar to integrated circuits (ICs) is fabricated through a thin- and thick- film approach, which is actually an extension of wafer level process technology. This compact interconnection eliminates the bond wires and one side contact interface (less packaging levels). In addition, the other components can be directly mounted on this stage. Therefore, a solid, 3-D power electronics subassembly is obtained. These are benefits to the reduction of electrical inductance and improvements on thermal behavior in the packaging structure. The embedded power technology leads to the reduced size of the geometric footprint, the parasitic capacitance and the peak junction temperature as compared to the discrete module.

2.3 Evaluations for Current High Temperature Packaging Technologies

Based on the survey of the current high temperature packaging technologies, the wire bond, pressure contact and flip chip technologies are available for applications. Although the wire bond technology is a low-cost interconnect method, suitable for discrete device packaging, the high differential stress due to its unbalanced mechanical structure and material CTE mismatch may cause failure at high temperature. Besides, the severe wire resistance increase at high temperature will limit its applications for high current use. Pressure contact technology is another usually high temperature technology. Although a balanced structure may be used in the structure, the stress due to the pressure is still under investigation. High cost is another disadvantage for pressure contact technology. The flip chip technology is used less compared to other technologies, chiefly due to the high processing temperature of the die attachment material. The material CTE mismatch and its mechanically unbalanced structure are also other reasons. Therefore, these current high temperature technologies have clear limits at high temperature due to their asymmetric structure, materials and CTE mismatch in the structure, thus normally leading to the reliability problem. Additionally, all current high temperature technologies are still discrete packaging technologies, and thus can only package the active components.

3-D multilayer packaging technologies are the trend of the power electronics packaging and show the potential ability to reduce parasitic inductor, enhance efficiency, improve the thermal performance and shrink the packaging volume. In the Power Overlay (POL) technology, the kapton tape as the adhesive and alignment layer in the structure is not an appropriate material for high temperature and is difficult to be replaced with an alternative high temperature material while keeping a similar structure. A similar problem happens in the flip-chip on flex technology. The key connection material, the solder ball, is used only for temperature up to 350^{o}C. Although the gold bump could replace the solder ball, the high process temperature up to 1000^{o}C makes it impractical. Therefore, the Power Overlay (POL) technology and the flip-chip on flex technology are difficult to develop for high temperature applications.

In the embedded power technology, the ceramic layer is used as the alignment and carrier layer and the metallization layer is employed for connections. All these key

materials are suitable for high temperature while some materials such as polyimide and epoxy can be replaced with proper high temperature materials. These properties of the embedded power module provide the potential capability to work at high temperature.

Therefore, for high temperature applications, our proposed high temperature Embedded Chip Module (ECM) should have these features:

-- High temperature material and interaction with semiconductor dies and surrounding materials;

-- Proper processing technologies for implementation of selected materials;

-- Low mechanical stress and the associated thermal expansion coefficients (CTE's);

-- Balanced structure with the low CTE metallization material;

-- 3-D multilayer packaging structure appropriate to high temperature operation.

2.4 Summary

The survey of packaging technologies for high temperature includes wire-bond interconnect and solder die-attach, flip-chip and pressure contact technologies. The three-dimensional multilayer packaging technologies working at normal temperature environments are introduced, including power overlay, flip chip on flex and embedded power technologies. However, current high temperature technologies have clear limits at high temperature due to their asymmetric structure, materials and CTE mismatch in the structure, thus normally leading to reliability problems. Additionally, no high temperature 3-D technology is existing and all current high temperature technologies are still discrete packaging technologies.

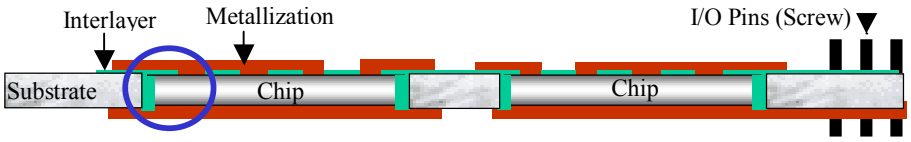
After detailed studies and comparisons in the current 3-D multilayer packaging technologies, the requirements and features of the desired high temperature module are presented.

Chapter 3

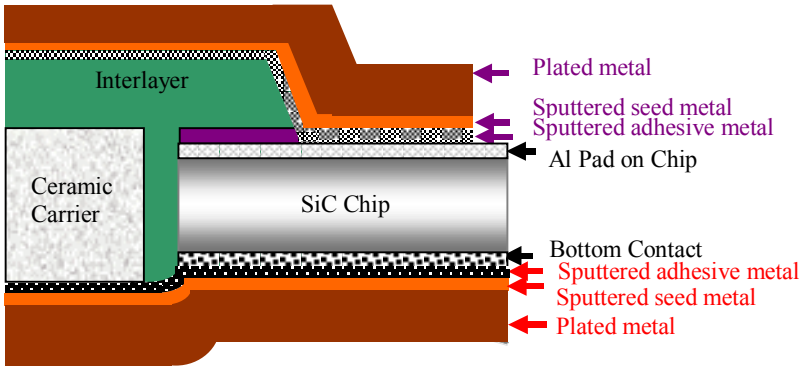
Proposed Embedded Chip Module (ECM) for High Temperature

3.1 Introduction

3.1.1 Proposed Embedded Chip Module (ECM) for High Temperature



(a) Proposed high temperature embedded power module



(b) Detailed cross section of the module

Fig. 3.1 Proposed embedded chip module(ECM) with double-sided metallization structure

The embedded power technology shown in Fig. 2.9 shows the potential ability to work at high temperature since this technology makes use of the ceramic carrier as the alignment layer (compared to POL technology) and the metallization layer as the inter-connections (compared to Flip chip on flex technology). However, this technology still requires essential improvements for high temperature applications.

The components or materials in the embedded power technology shown below are not suitable for high temperature applications:

-- Epoxy material;

-- Organic dielectric material;

-- Ceramic substrate due to the CTE mismatch;

-- Silicon chip;

-- Cu metallization material due to its high CTE;

-- Low temperature solder attachment.

Therefore, based on the required features of the current high temperature technology, the proposed high temperature embedded chip module (ECM) is shown in Fig. 3.1. The schematic cross sectional view of the module structure is presented in Fig. 3.1(a). Metallization layers on both sides are proposed for connections to replace wire bond/solder or metallization/solder. This double-sided metallization structure provides a mechanically balanced structure to reduce the mechanical stress at high temperature as well as enables double-sided cooling for better thermal performance. Additionally, it may incorporate integrated functional components, while the embedding of components into a flat ceramic carrier makes a multilayer high density interconnect system possible, by using integrated planar processing.

An important aspect of the design for this high temperature ECM is to select the proper materials and their combinations for high temperature applications. Fig. 3.1(b) presents a zoom-in of the different layers in the ECM. Four different layers are found on both sides of the chip. A thin passivation layer, usually thin-film Si_3N_4, is deposited on top of the chip during the chip fabrication process (not shown). This layer provides protection against damage from processing and is chosen by the chip manufacturer. Due to the high mechanical stress at high temperature, CTE match is an important issue in material selection to reduce this stress, so that the substrate material as the backbone of the structure should be chosen as a low CTE material similar to the semiconductor device material, leading to a material such as AlN. The adhesive layer between the chip and the substrate is designed to assemble multiple chips in one carrier. High temperature

materials with CTE similar to chip and substrate such as glass or ceramic adhesive are good candidates for the adhesive layer in the high temperature module. The interlayer is designed for planarization of the whole assembly after embedding multiple components. It is applied by screen printing or spin-coating. Via holes are formed to connect the metallization pattern to the metal pads on the chips. High temperature materials such as glass are proposed as the interlayer. The metallization layers on both sides, which are composed of a sputtered adhesive metallization layer, a sputtered metal layer and a plated metal layer, reduce the interconnection resistances and parasitic inductance dramatically. A pressure contact connection is used for I/O pins.

The high temperature ECM technology could also apply to a single chip packaging for general purpose use. An example showing how to package a MOSFET chip using ECM technology is presented for general purpose use including normal and high temperature applications in Fig. 3.2. The packaged single chip using ECM technology is flipped over with gate and source terminals on the bottom side. A high temperature die-attach material, such as Nanoscale silver [54] or high temperature thermal grease, is used for heat conduction between the base substrate and the active ECM part. Since the top metallization provides a large area as the drain terminal, the heat sink or other cooling systems could be connected here to realize double-sided cooling. Pressure contacts such as screws can be used for connecting the drain terminal to base substrate as well as for applying the pressure to fix the ECM part to the base substrate. Therefore, the proposed universal ECM combines the benefits of reduced parasitic inductance, enhanced efficiency, improved thermal performance and reduced packaging volume with ease of assembly.

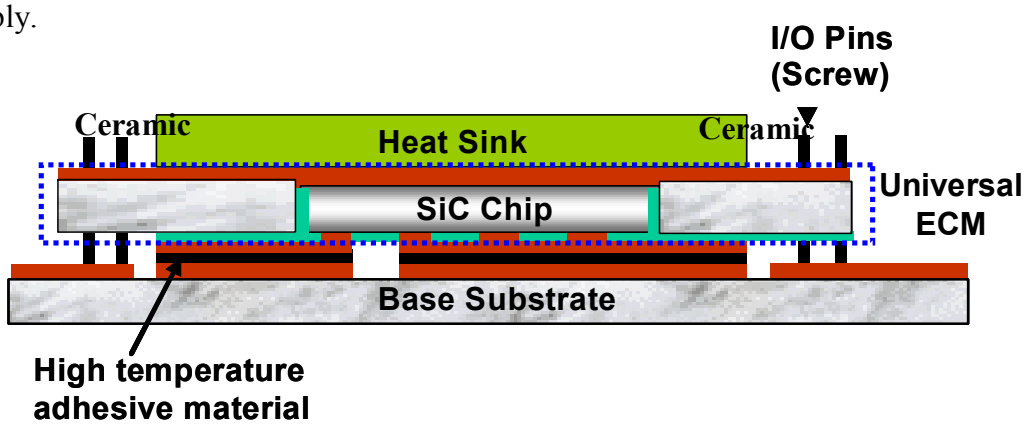


Fig. 3.2 An example for packaging the proposed universal ECM

3.1.2 Functions and Requirements for High Temperature Applications

Essential improvements are required to realize a 3-D module for high temperature applications, so further study on the functions and requirements for high temperature applications becomes necessary. High-temperature power electronics packaging is a system problem, not just a problem for discrete and integrated circuits. As temperatures increase, some materials, such as epoxy and dielectric, fail at high temperatures. Semiconductor devices are limited to high temperatures due to the limitation imposed by their material properties and traditional packaging technology. Mechanical stresses caused by thermal expansion mismatches between different materials severely increase under high-temperature environments. Therefore, the keys to successful high-temperature integrated power electronics modules are the availability of stable high-temperature electronics components and the packaging of these components using the proper materials. Interconnect materials such as glass and new die-attach materials, are expected to be used in the high-temperature module to replace the epoxy, dielectric and solder. Silicon carbide (SiC) and Gallium Nitride (GaN) have long been viewed as potentially useful semiconductors for high temperature applications. However, only SiC has been considered in this study. To minimize the mechanical stress due to the CTE mismatch, material with a similar CTE to the SiC chip, such as AlN or Si_3N_4, will be applied to replace the alumina substrate. Because of its good electrical resistivity, Cu metallization is widely used in the module working at normal environmental temperature. However, it is no longer a good candidate for high temperature applications due to its large CTE of 16.5ppm/^{o}C, so new solutions to implement the low CTE metallization are necessary in the high temperature module.

3.2 Selection of Sealing and Insulating Materials

3.2.1 Glass Material

3.2.1.1 Glass properties

Glass is a high temperature material with good chemical stability and high electrical resistance. It is composed of oxides, such as SiO_2, B_2O_3, Al_2O_3, ZnO, MgO, CaO, BaO,

PbO, Li_2O, Na_2O and K_2O. The different oxides have different contributions on the glass properties, such as durability, density, viscosity, and CTE.

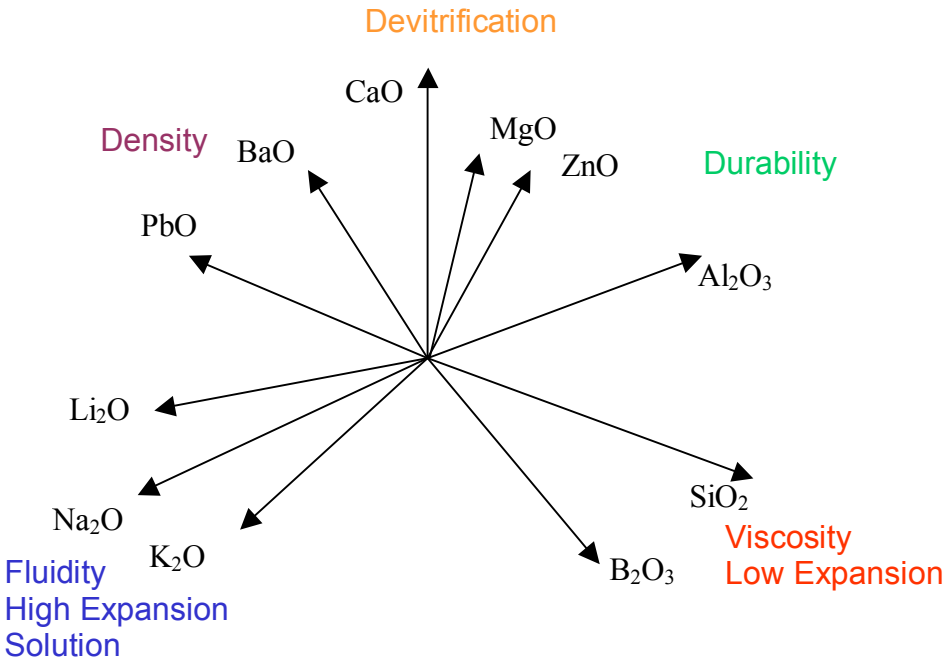


Fig. 3.3 Glass properties

In the scheme of Fig.3.3, three lines are drawn at angles of 120 degrees to each other. Toward the lower right is the line indicating the effect of silica. This oxide gives molten glass viscosity and cold glass its essential vitreous character. Silica contributes least to the thermal expansion of glasses. Soda appears toward the lower left. Soda promotes fluidity of the melt and expansibility of the glass. It is also the oxide chiefly responsible for the attack of water on glasses, which may be labeled, for want of a better term, solubility. In the third direction, we have lime, characterized by its effect in providing the durability of glasses against attack by water and also promoting diversification, or the tendency of glasses to crystallize out of the vitreous condition. Potash is like soda to a lesser degree, so its line is accordingly drawn in the same general direction. We may include Lithia in this category, and draw its line a little to the left of the soda line. Boric oxide must be given an intermediate position between soda and silica. It has some fuxing power, but at the same time its melts are viscous, that is, the borates the expansion of glasses. Alumina must be placed between lime and silica because it increases the viscosity of molten glasses more viscous than does an equal amount of lime, may be

placed farther to the right. Lead oxide, on the contrary, forms a rather low melting silicate and promotes the fluidity and subsequent workability of the molten glass when it is used as the base to give the mixture durability. It belongs well to the left of the lime position. Finally, barium oxide, whose behavior or effect upon physical properties is intermediate in character, may be placed between lime and lead oxide.

This scheme suffers from oversimplification because these effects cannot be clean-cut, and the oxide cannot be sharply differentiated from each other in their influence on the behavior and properties of glass. However, an idea of the compromises which are necessary to adapt the available oxides to the production of fusible, workable, and durable commercial glass may perhaps be obtained from a study of their respective position on the chart. [27]

Glass should be selected to provide optimum compatibility with the device requirements and usage, as well as the application technique used to apply it. The most critical characteristics of glass are:

- Type of glass
- Coefficient of Thermal Expansion at the glass set point
- Transformation Temperature (Tg)
- Particle Size Distribution (PSD)
- Glass flow and wettability at the processing temperature
- Compatibility of the glass composition with the application

3.2.1.2 Glass paste and glass firing profile

Glass powders can be applied to substrates and parts with a variety of techniques: screen-printing, doctor blade, electrophoreses, spin-coating, preforming, etc. This typically involves the mixing of the glass powder in a liquid vehicle to form a glass paste. The vehicle using to apply the glass is typically composed of a binder, which is used to promote adhesion and green strength, and a solvent. The higher the binder content of the vehicle the greater the green strength and the higher the viscosity of the vehicle, and subsequently, the viscosity of the glass slurry. [28]

Glass slurry viscosity is controlled by the ratio of glass powder to vehicle, and by the particle size distribution of the glass. The finer the glass powder is, the higher the slurry viscosity for the same ratio and the more difficult it is to remove the binder.

For a typical glass paste firing process shown in Fig. 3.4, the solvent is removed during a drying stage by heating in air at 120 °C for 10 - 20 minutes.

The binder is then removed during a separate binder burnout stage at 295 °C. The binder decomposition is most efficiently done in air, at a temperature below the transformation temperature Tg of the glass. Insufficient binder burnout can lead to excessive porosity and possible reduction of any heavy metal components, such as Pb, present in the glass. The time and temperature required is dependent on the binder selected, thickness of the glass layer, and the particle size distribution of the glass. A binder burnout profile, sometimes called a glazing profile shown in Fig.3.4.

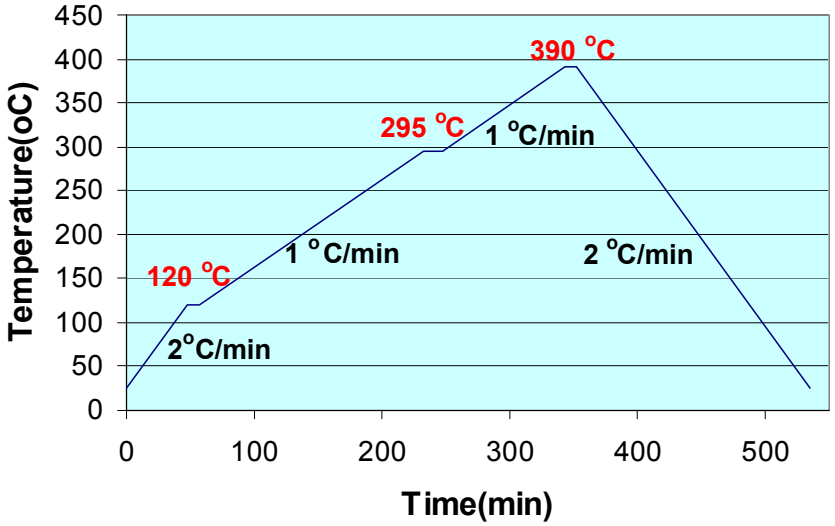


Fig. 3.4 Glass firing temperature profile

Final firing should typically be done in an oxidizing atmosphere, or if necessary to prevent oxidation of metal parts, in a neutral atmosphere such as Nitrogen. Reducing atmospheres can cause reduction of heavy metals from the glass. Fig.3.4 shows the firing process is performed at 390 °C with 15 – 20 minutes.

Heating rates are generally determined by part size, configuration, and thermal conductivity and should assure that the substrate/parts and the glass are in equilibrium. Devitrifying glasses are particularly sensitive to heating rates. Cooling rates are similar to heating rates, except within the annealing range of the glass. The fired unit should be cooled as slow as possible from the Annealing Point (T_a) to the Strain Point (T_{st}). Rates should be less than 5°C/min or less than 3°C/min for large parts, or where CTE mismatch between glass and substrate are present.

3.2.1.3 Disadvantages of the glass

The glass firing temperature is very high, normally more than 400 °C. Since a high firing temperature during the glass firing process can damage the device or change the device properties, the glass composition has to be changed for low temperature firing. Unfortunately, it is not practical to form a glass paste with a firing temperature lower than 350°C while keeping a low CTE similar to the SiC chip.

Glass normally has a high Coefficient of Thermal Expansion (CTE) more than 7ppm/°C when the glass firing temperature is about 400 °C. Since other materials in the ECM have relatively low CTEs about 3 – 4ppm/°C, the CTE mismatch will result in the high stress in the module and cause a module failure.

Table 3.1 Physical properties of glass

Typical uses	*Alumina*
Usual screen mesh	*80*
Peak glazing temperature	*380-440^oC*
Peak sealing temperature	*400-420^oC*
Thermal expansion coefficient, (x $10^{-7}/^oC$) (20-250^oC)	*64*
Density, grams/cc	*5.4*
Dilatometer softening point	*375^oC*
Dielectric constant (1kHz)	*15*
Dissipation factor (% @1kHz)	*0.7*
Volume resistivity, ohm-cm@25^oC	*>1013*
Breakdown voltage DC Volts/mil	*>300*

As discussed, the glass paste contains binder, which is burned out during the firing process. However, if the glass sealing layer is too thick, it has the potential problem of the insufficient binder burnout, which could cause small holes in the surface and gas bubbles in the glass. Additionally, it can also lead to possible reduction of heavy metal components. Both of these could reduce the glass voltage insulation rating. Fig. 3.5 illustrates voids in the glass due to the binder burnout process. Fig. 3.5(a) shows a simple test structure with a hole in AlN substrate filled by glass only and (b) presents the structure of a SiC chip embedded inside an AlN substrate by means of a glass sealant. Both structures show the voids and small bubbles in the glass. A voltage breakdown measurement demonstrated that the voids in the glass reduce the glass voltage rating severely and could lead to a voltage rating that was too low(less than 100V).

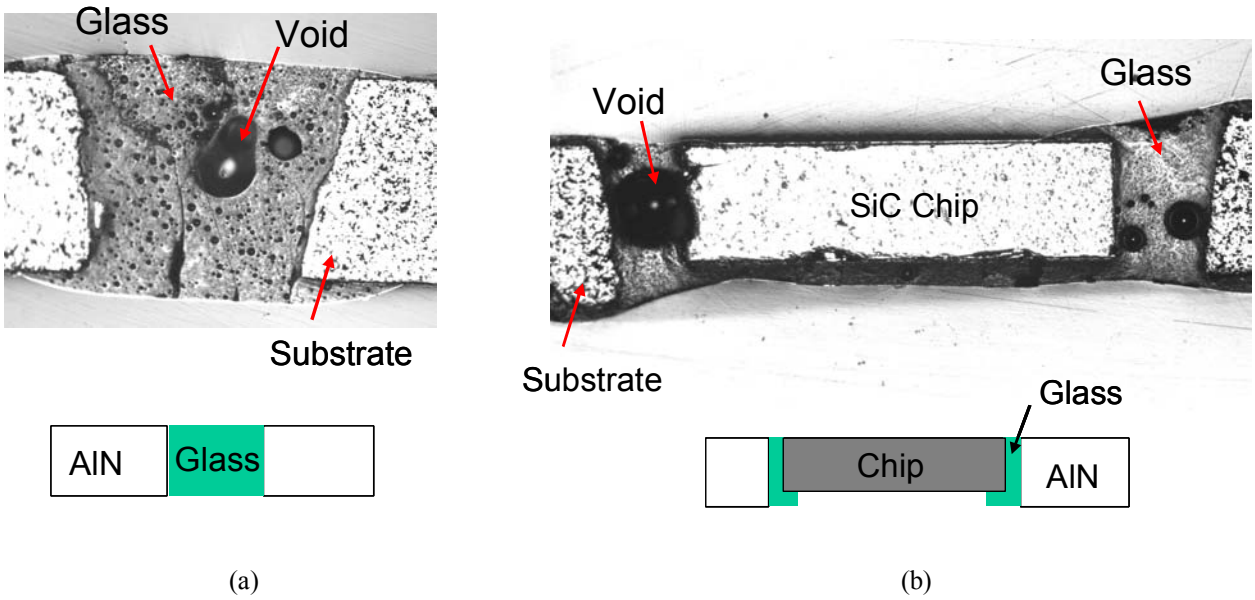


Fig. 3.5 Voids in the glass due to the binder burn out

3.2.2 Other Materials

3.2.2.1 Resbond material

Since repeated experiments using glass paste as an adhesive sealant for chip location (see Fig. 3.1(b)) consistently showed up low breakdown voltage due to the voids/bubbles, it was clear that another high temperature sealing material is needed to replace it. The

commercial ceramic adhesive material Resbond 919 was selected as a good candidate for high temperature applications.

Resbond 919 was formulated with the use of the specific ceramic binders to offer an adhesive with exceptionably high electrical resistance. [29] These special binders maintain their high electrical resistance and dielectric strength even when exposed to temperatures up to 2800ºF. The detailed applications are listed as bellows:

-- Bonds electrode rods into electrically insulating ceramic tubes and protects them from voltage breakdown and corrosive atmospheres;

-- Seals light bulb fixtures, insulating them with out cracking when exposed to heat and thermal cycling;

-- Forms protective tubes for fiberglass covered extension wires. Protect against heat and corrosion.

Resbond 919 can be used for electrical insulation in potting, sealing, coating, ingnitors, heating coils, instrumentation, thermocouples and in all electrical applications.

Table 3.2 Physical properties of adhesive material

Continuous Use Temp. ^{o}F	*2800*
Base	*Mg0-ZrO_2*
Form	*Paste*
Compressive Strength (psi)	*4500*
Flexural Strength (psi)	*450*
Thermal Expansion ($x10^{-6}/^{o}C$)	*4.5*
Thermal conductivity (W/m.K)	*0.577*
Dielectric Strength (V/mil)	*270*
Volume Resistivity (ohm cm)	*10^{11}*
Components	*2*

The physical properties of this material are shown in Table 3.2. Resbond 919 has a very similar CTE of 4.5ppm/^{o}C to SiC and AlN, so it is compatible within the structure, giving low stress at high temperature. Additionally, it provides a dielectric strength of 270volts/mil and a volume resistivity of 10^{11} ohm-cm (at room temp). It is easily incorporated into the production process.

The resbond ceramic paste is prepared by mixing 10g water and 50g ceramic adhesive powders. Then the paste is put to the sealing gap between the chip and the AlN carrier carefully. The curing process may take up to 24 hours at room temperature; however, curing process can be accelerated by keeping at 65^{o}C for 4 hours.

3.3.2.2 Polymer material

Polymer materials are known for the following characteristics: inertness, gas phase deposition, pinhole free, adherence to metals, composites, plastics, elastomers and ceramics and excellent barrier properties. Polymer materials available to the current market have so far been found to be useful only up to 300^{o}C. Parylene HT is a new fluorinated variant of Parylene polymer that provides thermal stability up to 450^{o}C. [30] In addition, it offers other improved properties such as low dielectric constant, low coefficient of friction etc.

Organic vapor-deposited Parylene HT, a new fluorinated variant of Parylene, is suited for electrical and environmental protection of power electronic components, printed circuit boards, microelectronics, automotive parts and medical devices; thereby enhancing their reliability without hermeticity. It is also suitable for contamination and corrosion control, dry lubrication and as an interlayer dielectric in manufacturing high density and high-speed integrated circuits. Parylene HT offers a solution to many existing polymer conformal coating challenges in part because of its low dielectric constant, thermal stability at higher temperatures, low moisture absorption values and dry lubricity. In addition to its excellent and exceptional thermal and electrical properties, new Parylene HT also shares important properties with traditional Parylenes (Parylene N, C and D) including freedom from solvents, lack of shrink-generated stress, excellent gap fill capability and uniform pinhole free coverage. However, for higher temperature applications of more than 400^{o}C, this material isn't suitable.

3.3 Metallization Material Selections

3.3.1 Candidates of Metallization Material

For high temperature applications, it is important to achieve the low stress in the module by choosing proper materials with similar CTEs. Copper metallization has a CTE 16.5ppm/^{o}C, which is 4 times larger than the CTE of the SiC chip. With such a large CTE mismatch at high temperature, the module will normally fail due to chip crack or metallization peeling. Therefore, to obtain the low stress for protecting the chip, it is necessary to replace copper metallization with a type of metal that has a similar CTE to the SiC chip. Additionally, for the power electronics module, it is required to have the thick metallization trace for carrying high currents, thus proper approaches such as the electrical plating process are used to implement the metallization and obtain the thick trace.

Mo is the most widely used metal in electrical contact for high temperature applications. The mechanical stress using Mo metallization is very low, due to its similar CTE to the SiC chip, so it is a good candidate for high temperature applications. However, it is impracticable to implement pure Mo to the high temperature ECM directly through the electrical plating process. The Ni and Mo alloy can be electrodeposited [31] - [33] although the electrical plating process is still under investigation and the Ni/Mo alloy may still have a much larger CTE compared to the SiC chip. Therefore, we still need to find a good candidate used for high temperature EMC.

Table 3.3 lists all candidate metals, which could be implemented with the electrical plating process. Except for Mo and Cr, other materials with CTE below 10ppm/^{o}C, such as Ru, Rh and Pt, are too costly and normally used for jewelry decorative purpose. In these candidates, Chromium (Cr) shows a very similar CTE to the SiC chip while its electrical resistivity is much higher than Cu. However, we can obtain the proper electrical resistivity in the high temperature module by a combined use of thin Cr layer and thick Cu layer, which means that Cr layer plays only as a stress buffer layer to protect the chip and the Cu layer as the main current carrying layer. Therefore, it is possible to achieve both the low mechanical stress and the low electrical resistivity in the high temperature module by finding an optimal module structure to implement the Cr and Cu metallization.

Table 3.3 Candidates for replacing the Cu metallization [34]

	CTE (ppm/oC)	*Electrical resistivity (uohm.cm)*
Mo	*4.8*	*5*
Chromium (Cr)	*4.9*	*12.7*
Ruthenium (Ru)	*6.4*	*7.1*
Rhodium (Rh)	*8.2*	*4.3*
Platinum (Pt)	*8.8*	*10.6*
Palladium (Pd)	*11.8*	*10*
Nickle (Ni)	*13.4*	*7*
Gold (Au)	*14.2*	*2.2*
Copper (Cu)	*16.5*	*1.7*
Silver (Ag)	*18.9*	*1.6*
Zinc (Zn)	*30.2*	*5.9*

Chromium is a good candidate in the high temperature module and has many good advantages:

1. Similar CTE to the SiC material;
2. Good adhesion material;
3. Easy to be electrically plated;
4. Low cost;
5. Wear resistance, lubricity and oil retention.

Disadvantages:

1. High electrical resistivity compared to Cu;
2. Highly toxic plating solution could cause the problem of health hazards.

3.3.2 Combination of Cu and Cr for metallization layer

Chromium is a good candidate for use in the high temperature module; however, it has a large electrical resistivity of 12.7uohm.cm, which is 7.5 times that of Copper. For power electronics applications, the large carrying current is normally applied to the

metallization layer, thus the resistance of the metallization is required to be small enough, in order to avoid a large voltage drop and high power loss. By combining Cu and Cr as the metallization, it is possible to achieve both a low mechanical stress and good electrical conductivity. The chromium as the buffering layer should be kept as thin as possible due to its high resistivity, while should have enough thickness to achieve the low stress for protecting the chip. The copper layer as the main current carrier should have a fixed thickness, which is sufficient for carrying currents. Therefore, it is important to choose the proper thicknesses for both Cu and Cr to get the optimal tradeoff.

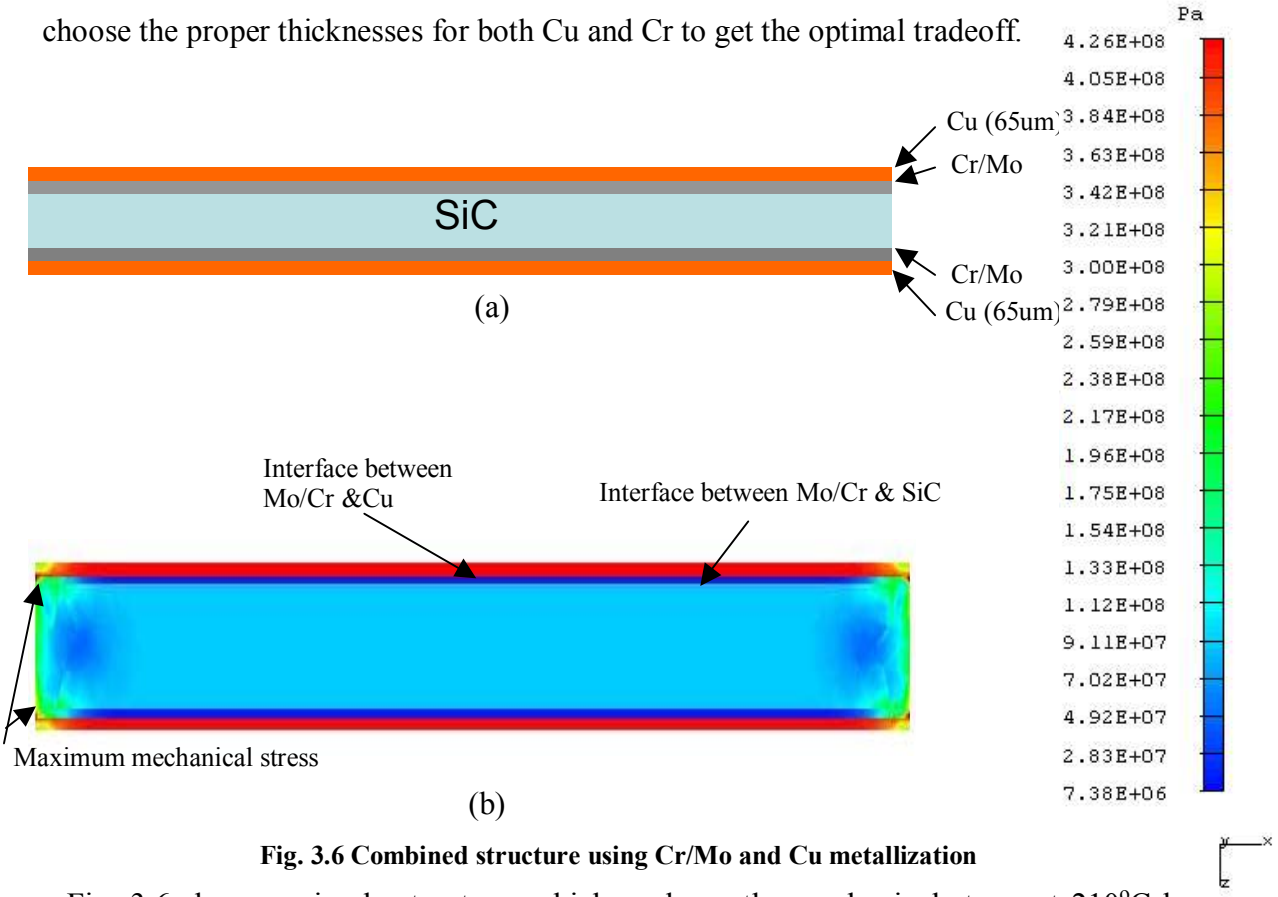
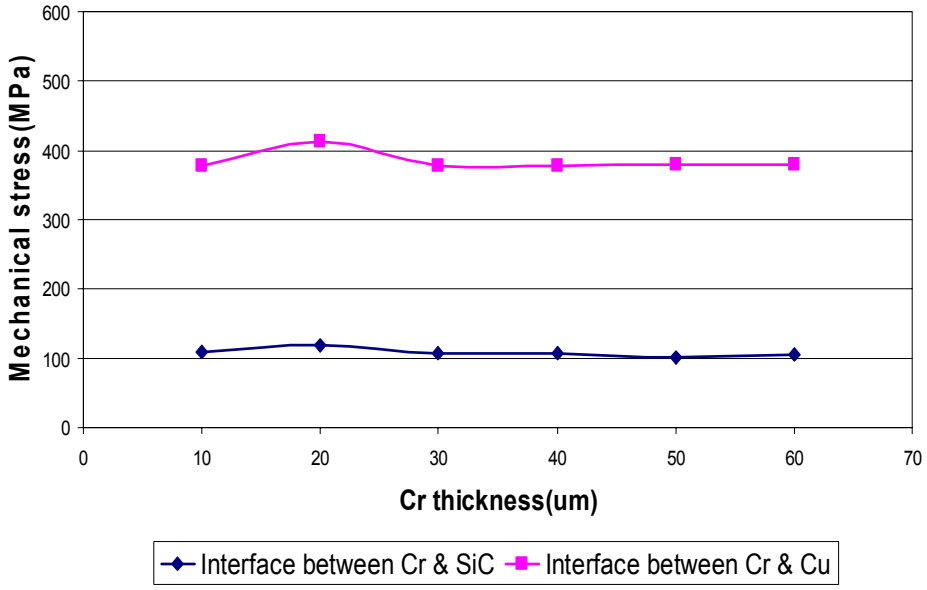


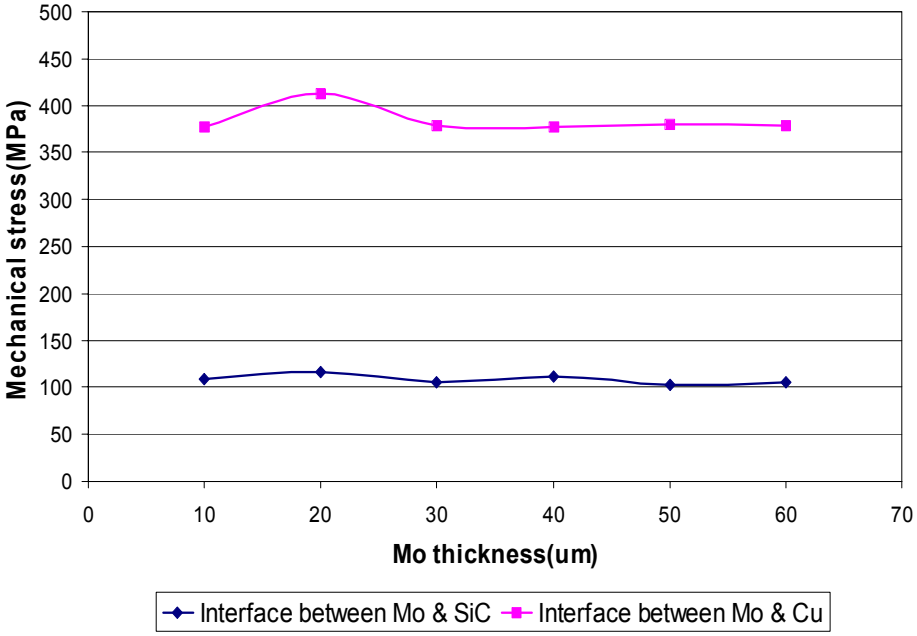
Fig. 3.6 Combined structure using Cr/Mo and Cu metallization

Fig. 3.6 shows a simple structure, which analyzes the mechanical stress at 210°C by using the Cu and Cr/Mo metallization layers. It is a symmetrical structure in Fig. 3.6(a) with the SiC layer covered by the Cr/Mo layer, which is under the Cu layer. Since the copper layer is the current carrier, the thickness of Cu is fixed at 65um, which is thick enough for carrying currents. By adjusting the Cr/Mo layer from 10um to 60um, the mechanical stress can be simulated by using I-DEALS software. Fig. 3.6(b) shows a specific case of the simulation results. The maximum stress occurs at the edge of the interface between the Mo/Cr and Cu layers, while the stress distributions are almost

horizontally uniform in the middle part. The maximum stress, which is at the edges of the interface between the Mo/Cr and the Cu layers, is chiefly caused by the sharp corner and large CTE difference between Cr and Cu. Since this maximum stress is far from the chip and can be released to a harmless level using the edge termination technology (it will be introduced later), we only consider the interfaces in the uniform stress part between Mo/Cr & Cu and between Mo/Cr & SiC for analysis.



(a) Cr case



(b) Mo case

Fig. 3.7 Mechanical stress analysis for different thickness of Cr/Mo

The simulation results for different Cr/Mo thickness are shown in Fig. 3.7. Both cases for Mo and Cr show similar simulation results, although the stresses of Cr case shown in Fig. 3.7(a) is slightly smaller than the Mo case shown in Fig.3.7(b). The interface stresses between Cr/Mo and Cu in the middle part are almost unchanged. It means that the uniform stresses in the middle part have no relationship with the Cr/Mo thickness. Although the uniform stress at the interface between Mo/Cr & Cu is high at 400MPa, the low stress about 100MPa is achieved at the interface between Mo/Cr & SiC. This illustrates that the high stress interface has shifted away from the chip surface to the interface between the Mo/Cr & SiC by using Cr/Mo layer as the stress buffering layer. Since the interface between the metal and semiconductor has the weakest bonding in the structure, the stress between the SiC chip and the metallization should be reduced to a harmless level. However, the larger interface between chromium and copper presents a metal-to-metal bonding, which can be resistant to much higher stresses than the interface between metal-to-semiconductor.[58]

3.3.3 Chrome Plating Process

3.3.3.1 Chrome plating types

The chromium can be implemented to the high temperature ECM as the buffering layer through chrome plating process. The electrical plating of hard chromium is a recognized means of prolonging the life of all types of metal parts subjected to wear by corrosion, friction and abrasion. Hare chromium, because it has a low surface energy, is more often deposited on sliding or revolving parts and is therefore used on moving components of engines, pumps, compressors, hydraulic and air operated plant, presses, etc. The chromium deposit is also highly resistant to corrosion, and a large number of applications where it is used to protect parts from corrosion are in popular demand. Another attribute is that the process is a relatively cold one and can therefore be used to import a very hard surface to delicate parts without fear of distortion. With these attractive properties and because it can be applied with perfect adhesion to numerous base metals, this specialized form of electroplating has assumed such an important position in the engineering and

allied industries today. [35]-[37] There are mainly two types of chrome plating: decorative chrome plating and hard chrome plating.

Decorative chrome plating is sometimes called nickel-chrome plating because it always involves electroplating nickel onto the object before plating the chrome. It sometimes involves electroplating copper on the object before the nickel, too. The nickel plating provides the smoothness, much of the corrosion resistance, and most of the reflectivity. Decorative chromium plating provides a durable coating with a pleasing appearance and is usually deposited in a thickness range of 0.002 to 0.020 mils. Common items with decorative chrome include appliances, jewelry, plastic knobs, hardware, hand tools, and automotive trim.

When chromium is applied for any other purpose, or when appearance is a lesser feature, the process is commonly referred to as hard chromium plating, or functional chromium plating. Hard chromium plating typically ranges from 0.1 to 10 mils thickness. Hard chromium plating is chrome plating that has been applied as a fairly heavy coating (usually measured in thousandths of an inch) for wear resistance, lubricity, oil retention, and other 'wear' purposes. Some examples would be hydraulic cylinder rods, rollers, piston rings, mold surfaces, thread guides, gun bores, etc. It is not really harder than other chrome plating, it is just called hard chromium because it is thick enough that a hardness measurement can be performed on it, whereas thinner plating will break like an eggshell if a hardness test is conducted. Hard chrome plating is almost always applied to items that are made of steel, often hardened steel. It is metallic in appearance but is not particularly reflective or decorative.

Chromium plating provides excellent hardness (typically 700-1,000 Vickers), bright appearance with no discoloration, and resistance to corrosive environments; it is easily applied and has a low cost. However, hexavalent chromium plating suffers from low cathode efficiency, poor metal distribution, lack of coverage around holes, and is very difficult to use in barrel plating. It is also a worker- and environment-unfriendly process.

To reduce the mechanical stress and act as a buffering layer, the thickness of the chromium layer should be between 10 um to 60 um. So only the hard chrome plating is a proper method for high temperature ECM applications.

3.3.3.2 Anode and solution

Lead, or its alloys, is used as the anode material: this oxidizes anodically to lead peroxide, so that during electrolysis an anode of the latter material is always present. The chief anode process consists in the evolution of gaseous oxygen. Cr^{3+} ions also present in the electrolyte are oxidized to chromic acid at the same time, so that ultimately equilibrium is established during the electrolysis in which as much trivalent chromium is oxidized at the anode as enters the electrolyte from the cathode. If the anode area is too small, and the anode current density therefore becomes high, the re-oxidation of trivalent chromium takes place at lower current efficiency, so that it gradually increases in the electrolyte and may ultimately be harmful to the operation. Conversely, too large an anode area may result in a reduction of the Cr^{3+} content, although no evidence is to be found that this condition has any adverse effect in practice.

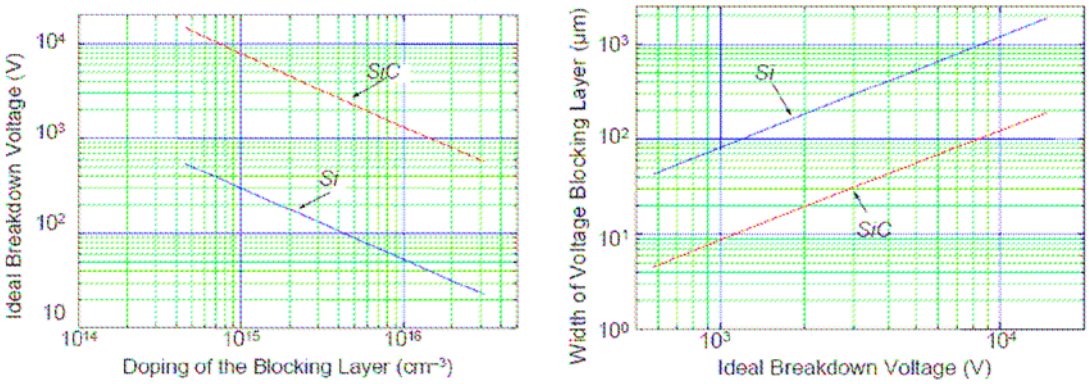
3.4 Chip selection

Silicon Carbide (SiC) power devices are expected to show superior performance compared to devices made with other semiconductors as shown in Table 3.3. This is primarily because 4H-SiC has an order of magnitude higher breakdown electric field (2 – $4X10^6$ V/cm) and higher temperature capability than conventional Silicon (Si) materials. The high breakdown electric field allows the design of SiC power devices with thinner and more highly doped voltage blocking layers. A comparison of the ideal breakdown voltage versus blocking layer-doping concentration is shown in Fig. 3.8(a). The more highly doped blocking layer (more than 10 times higher) provides lower resistance for SiC devices because more majority carriers are present than for comparably rated Si devices. A comparison of the voltage blocking layer thickness for a given breakdown voltage is shown in Fig. 3.8(b). The thinner blocking layer of SiC devices (1/10th that of Si devices) also contributes to the lowering of the specific on-resistance by a factor of 10. The combination of 1/10th the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si devices. Because SiC has a larger band gap, SiC devices can be

made to operate reliably at much higher temperatures than their Si counterparts (300°C for SiC vs. 150°C for Si).[38][39]

Table 3.4 Physical properties of semiconductors

	Silicon	GaAs	AlGaAs	GaP	SiC	Diamond
Band Gap (eV)	1.1	1.3	1.9	2.34	2.9	5.5
Breakdown Field (kV/cm)	250	300	500	—	2500	10,000
Thermal Conductivity (W/cm •K)	1.5	0.5	0.1	0.8	4.9	20
electron mobility, R.T. $cm^2/v\text{-}s$	1400	4000	3000	350	250	2200
hole mobility, R.T. $cm^2/v\text{-}s$	600	400	—	100	50	1600
electron sat. velocity 10^7 cm/s	1.0	1.0	1.0	—	2.0	2.7
dislocation energy (eV)	13	9	9	—	22	—
melting temp. (°C)	1412	1238	1304	1470	2700 (4 kpsi?)	—



(a) (b)

Fig. 3.8 Comparison of for SiC and Si

3.5 Substrate selection

3.5.1 Alternative substrate materials

The substrate as the chip carrier and the backbone of the structure is a highly important layer. The selection of substrate material should be carefully considered for high-

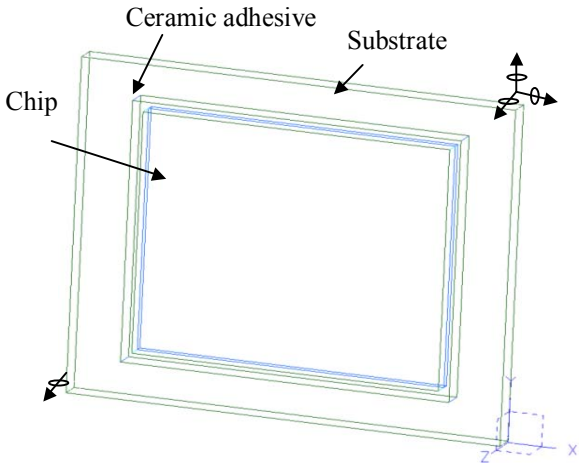
temperature applications, since the CTE mismatch between the substrate, adhesive and chip could cause severe cracks. Three types of substrate materials were compared: Al_2O_3, AlN and Si_3O_4. Their thermal and mechanical properties are shown in Table 3.4.

As shown in Table 3.4, aluminum nitride (AlN) has the highest thermal conductivity and a CTE only slightly higher than SiC. Silicon nitride (Si_3N_4) has a near CTE to SiC, however, it has a low thermal conductivity similar to Alumina (Al_2O_3). It is also important to have a low CTE for the sealing material compared to the SiC chip and the substrate. Therefore, a simulation with a structure composed of the SiC chip, substrate and ceramic adhesive is necessary to for the substrate selection.[40]

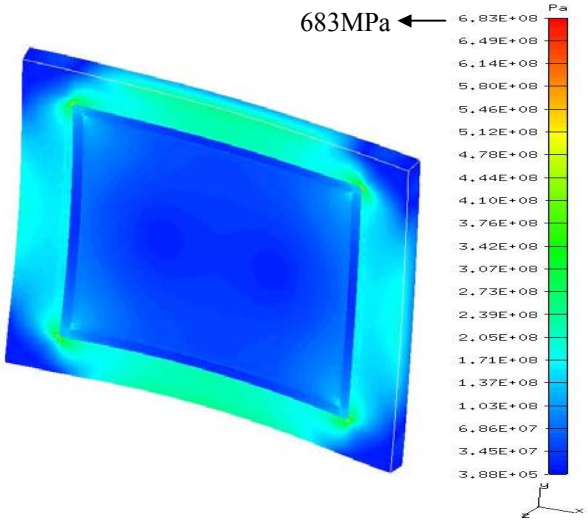
Table 3.5 Material properties

Properties	*Adhesive*	*Al_2O_3*	*AlN*	*Si_3N_4*	*SiC*
Modulus of Elasticity (GPa)	*70*	*370*	*330*	*304*	*420*
Thermal Conductivity (W/mK)	*2.16*	*26*	*170*	*30*	*120*
CTE (ppm/oC)	*4.6*	*7*	*4.5*	*3.3*	*4*

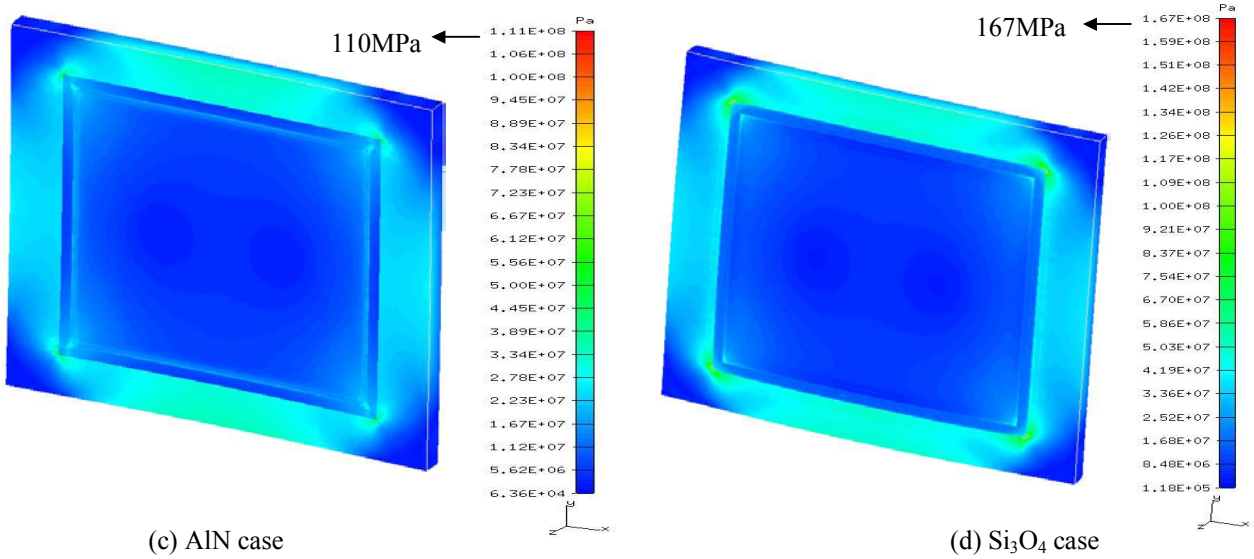
3.5.2 Substrate Selection



(a) Model structure



(b) Al_2O_3 case



(c) AlN case (d) Si_3O_4 case

Fig. 3.9 Substrate material selections

A simple structure shown in Fig.3.9 (a) was chosen with the chip assembled in the substrate by resbond material sealing. IDEAS software was employed to study the simple model and three displacement restraints at three different points were defined as shown in Fig. 3.9 (a). The stress-free temperature is set at 390^{o}C, which is the glass paste firing temperature. The mechanical stress results of the Al_2O_3, AlN and Si_2O_3 substrate material structure were respectively presented in Fig. 3.9 (b), (c) and (d). The largest mechanical stress of 683MPa and the strain displacement were detected in case (b), which uses Al_2O_3 as the substrate material. The case using Si_3N_4 substrate has a maximum stress 167MPa. AlN proved to be a good CTE match with the chip and had the lowest mechanical stress of 110MPa and the strain displacement in all three cases. Additionally, AlN had the highest thermal conductivity, which potentially improved the heat dissipation ability of the module. Therefore, AlN was chosen as the substrate material in our applications.

3.6 Summary

In this chapter, the high temperature ECM is proposed with a mechanically balanced structure with double-sided metallization layers and material CTE match in the structure. High temperature materials, such as the glass and Resbond adhesive, are proposed for the insulating and sealing layers. The voltage rating problem due to the air bubble in the sealing glass is studied. To achieve the low stress in the chip area, the combined use of Cr and Cu metallization layers are proposed. The optimal structure with the low stress is obtained by changing the thickness of the Cr buffering layer. The hard chrome plating process can be a proper processing approach to implement the Cr buffering layer to the high temperature ECM. For high temperature applications, the SiC device shows a good candidate by the comparisons with the Si device. In the substrate selections, the AlN substrate is finally chosen since it has the lowest stress in the structure compared to the Al_2O_3 and Si_3N_4 substrates.

Chapter 4

Analysis of a High Temperature Embedded Chip Module (ECM)

4.1 Introduction

The high temperature in the module could be caused by either the environmental temperature encountered around combustion engines, such as the automobiles and aircrafts, or the high heat generation from the components in the module. Under high environmental temperature, the high temperature ECM has a cooling system similar to the Si based "normal" temperature module, because both of them have a similar temperature difference from junction to ambient. Therefore, in this chapter, we focus on the EMC working at an ambient temperature of 24^{o}C with an economic cooling system. Due to the increasing device density, the Si based module has to survive with complicated thermal design and bulky cooling system, which limits the device density to increase further. Fortunately, the high temperature module can operate at higher temperature with the same environmental temperature as the Si based module, which thus simplifies the thermal design, eliminates the bulky cooling system and finally increases the power density. Therefore, it is necessary to show the cooling system reduction by using a high temperature ECM working at an ambient temperature of 24^{o}C, while keeping its maximum temperature at a safe operating level.

Thermal models such as 1-D, 2-D, and 3-D, can facilitate analysis of the steady- and transient-state thermal behavior of an ECM. The 3-D model [41] [42] introduces a digital model for the analysis of the electro-thermal behavior to offer better optimization of thermal losses due to the complication of the semiconductor device. The thermal model is described by the 3D finite difference and allows consideration of the heat distribution dissipated in the device components. This model, which always uses a three-dimensional finite element method (3-D FEM), is highly accurate. The 2-D model [43] [44] presents the use of the boundary element method (BEM) to investigate the transient thermal response of electronic packages consisting of dissimilar materials. Although 3-D FEM is commonly used for predicting the temperature distribution in such devices, it suffers from

poor accuracy in the calculation of the flux field. However, the BEM formulation considers both the temperature and flux fields through the internal equations. This permits an accurate prediction of sharp temperature gradients over the domain. Although the 3-D FEM and 2-D BEM deliver very accurate results, their usage is limited by constraints on computational time in arbitrary load cycles and the available computer memory. However, the 1-D model quickly offers insight into the physical layers of the components, providing useful information in a few minutes for arbitrary or periodic power waveforms. In this chapter, two types of thermal models, a 1-D thermal model employing an equivalent RC thermal network and a 3-D FEM thermal model, will be used to analyze the high temperature behavior of the proposed module.

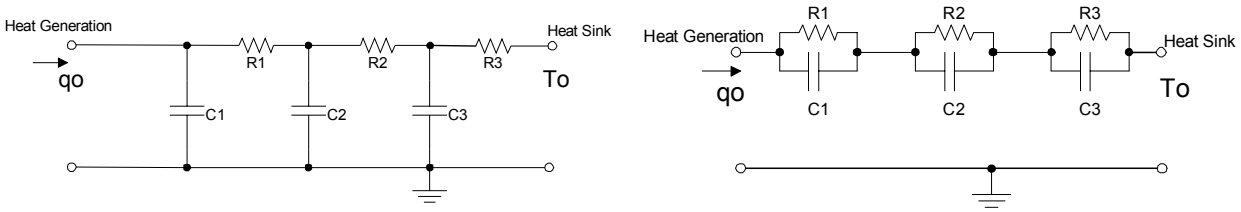
In the high temperature SiC ECM, the leakage current of the SiC device used, due to the Schottky junction, increases dramatically at high temperature. A leakage current that is too high will destroy the module and limit the module in high temperature applications. Therefore, the theoretical SiC chip reverse characteristics are analyzed in this chapter to predict the leakage current trend at high temperature.

4.2 Thermal Model of the Embedded Chip Module

4.2.1 One-dimensional Thermal Model

Compared to 2-D and 3-D thermal models, one-dimensional thermal model can quickly offer insight into the physical layers of the components and provide the accurate thermal parameters with short computable time. More importantly, 1-D thermal model can be directly applied to electrical simulations by combining the thermal and electrical analysis to obtain more realistic simulation results. The RC thermal equivalent model, which is always used in the 1-D model, is investigated to extract thermal resistances and time constants for a thermal network. The uniqueness of the RC model is its introduction of the time constants based on the Elmore delay, which represents the propagation delay of the heat flux through the physical geometry of each layer. [46] The dynamic behavior predicted by the thermal network is equivalent to numeric solutions of the 3-D FEM. RC model can quickly provide physical identifications for different layers of the structure. Therefore, this approach enables a system designer to obtain the thermal parameters,

identify the physical meanings of these parameters and quickly optimize the thermal system by adjusting the physical structure, while simultaneously couple the thermal prediction with a circuit simulator to analyze the electro-thermal behavior of a module system.



(a) (b)

Fig. 4.1 Candidate models for representing the experimental system:
(a) Cauer-equivalent circuit and (b) Foster-equivalent circuit

The candidate 1-D RC thermal equivalent model of Fig. 4.1 suggests an idealized discrete network representing the packaged module. The current generator q_0 corresponds to the thermal power in the heat source, the ideal voltage generator T_0 represents the heat sink, and the electrical ground is the environmental temperature. Since the electronic network is 1-D, its thermal property is nearly satisfied when the thermal losses in its environment, either by radiation or convection through the lateral walls or the top surface of the packaging, are negligible in comparison with the 1-D heat flow that occurs due to the conduction mechanism.

Although both thermal equivalent circuits can uniquely represent the semiconductor packaging, it must be pointed out that the only circuit that is suitable for faithfully representing the system from the physical standpoint is the Cauer network. The passive elements of the Cauer-equivalent model, the thermal resistance and capacitors, have a real physical meaning: each RC cell represents the contribution to the thermal impedance of a given part of the whole system. And the value of each resistance R_i is generally determined by the material thermal conductivity of the given part and by its size, while the capacitor C_i is related to the mass and to the specific heat of the sector. [47]

For dynamic problems, each layer has to be subdivided into one or several cells in order to accurately represent the heat conduction mechanism. There are two popular cell types:

R-C cell and R-C-R cell (T-type), shown in Fig.4.2 (a) and (b). The R-C cell is a simplified structure, which is only composed of one R and one C. However, to further significantly increase the accuracy of the model, the R-C-R cell is a better choice. Especially, while each layer is represented by one cell, the R-C-R cell structure can be corresponded to the physical structure more clearly, therefore, describe the physical structure more accurately.

In one-dimensional thermal model, the R-C-R cells as shown in Fig. 4.2 (b) are used to represent the contributions of the physical sectors in the thermal system. For each cell, the thermal resistance and thermal capacitance are physically related to the shapes and lengths of the solid parts representing this cell. Since each cell could include the contributions of more than one layer, or vice versa, identification of the contributions of each layer in terms of an R-C-R cell is required to obtain the accurate thermal characteristics for thermal design. Furthermore, the thermal parameters relating to the physical structure can be applied to obtain other important information of the physical structures, such as the interface thermal resistance and the failed layer in the structure.

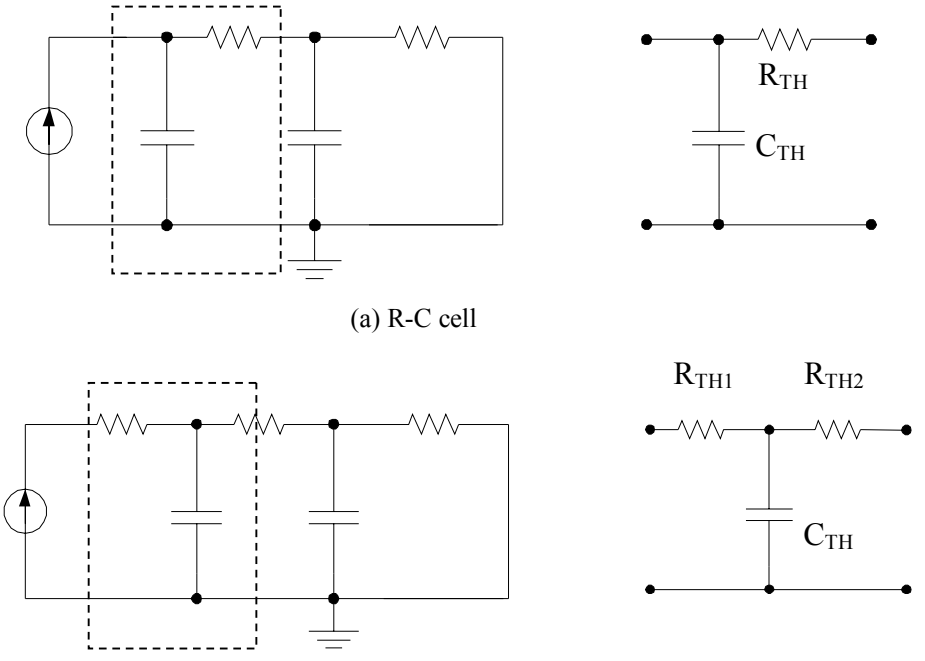


Fig. 4.2 Cell types: (a) R-C cell and (b) R-C-R cell

To represent each layer in the thermal system, thermal resistance and thermal capacitance are calculated by knowing the physical information of each layer including the material properties, shapes and lengths. In the R-C and R-C-R cells, the calculated thermal resistance R_{TH1}, R_{TH2}, R_{TH}, capacitance C_{TH} can be expressed in equation (4.1), (4.2) and (4.3).

$$R_{TH} = \frac{h}{k \cdot S} \tag{4.1}$$

$$C_{TH} = c \cdot \rho \cdot V \tag{4.2}$$

$$R_{TH1} = R_{TH2} = \frac{R_{TH}}{2} \tag{4.3}$$

where h -- Thickness of one layer S -- Cross-section area

k -- Thermal conductivity c -- Specific heat

ρ -- Density V-- Volume

4.2.2 Model for FE Analysis

The 3-D finite element models were created using commercial software, I-DEAS. I-DEAS provides a solid modeler to model solid geometry and electro-system cooling (ESC) solver for thermal simulations. ESC allows conjugate heat transfer analysis with comprehensive 3D computational fluid dynamics (CFD) solutions. In addition, ESC combines finite element modeling (FEM) based analysis with control volume formulation to achieve accurate solutions. The fluid flow and thermal model are solved iteratively. This powerful technique conveniently couples dissimilar fluids and thermal models by introducing a thermal couplings methodology to the thermal network. More information on the capabilities of ESC can be found in [48].

The ESC solver allows for conductive, convective, and/or radiative analysis. In this study, radiation was assumed negligible, and both conductive and convective modes were used. Conduction is a process of heat transfer from a solid-solid interface due to the atomic or molecular activity. A general conduction rate equation is known as Fourier's Law and can be expressed as follows:

$$q'' = -k \cdot (i\frac{\partial T}{\partial x} + j\frac{\partial T}{\partial y} + k\frac{\partial T}{\partial z}), \tag{4.4}$$

where q" is the heat flux, k is the thermal conductivity, and T is the temperature. It can be observed from Eq. 4.1 that the heat flux is a directional quantity.

The process of heat transfer from a solid-fluid interface due to fluid motion is known as convection. The overall effect of convection heat transfer is known as Newton's law of cooling and can be expressed as follows:

$$Q = h \,.\, A \,.\, (Tw - Ta), \tag{4.5}$$

where Q is the quantity of the heat convection, h is the heat transfer coefficient in W/m^2-K, A is the convection surface area, T_w is the temperature of the convection wall, and Ta is the ambient fluid temperature.

4.3 Simulation

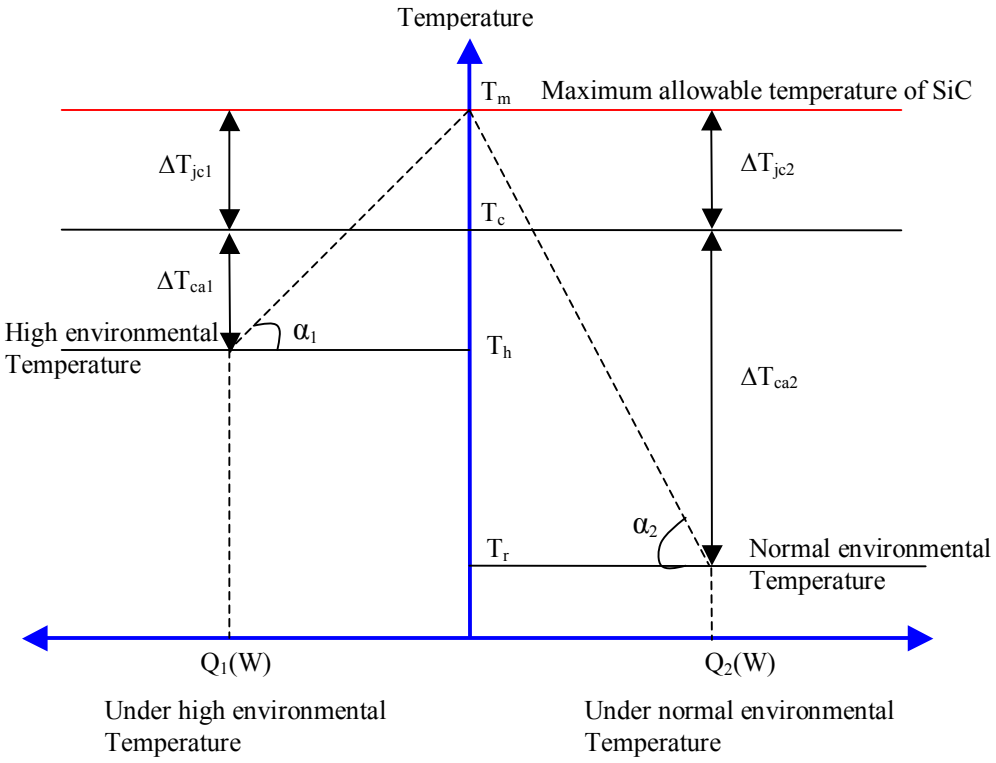


Fig. 4.3 Comparisons of a SiC module working under high and normal environmental temperature

The high temperature in the module could be chiefly caused by the environmental high temperature. Besides, when the module works under normal environmental temperature (room temperature), high temperature may caused by the heat dissipation generated from the module. As shown in Fig. 4.3, it illustrates the different thermal designs for a high temperature ECM, when the module works at high and normal environmental temperature. In Fig. 4.3, the horizontal axis represents the heat dissipations from the module, while the vertical axis shows the related temperature. For both cases, the maximum allowable temperature of the SiC chip T_m is fixed at a safe level and the heat dissipations is assumed to be equal. Since both cases have the similar heat paths from the chip junction to the heat sink (or heat spreader), the junction-to-case temperature ΔT_{jc1} under high environmental temperature is almost equal to the junction-to-case ΔT_{jc2} under normal temperature. That is:

$$\Delta T_{jc1} \approx \Delta T_{jc2}$$

However, the case to ambient temperature ΔT_{ca1} and ΔT_{ca2} are different for both cases due to the different ambient temperatures. It is obvious that:

$$\Delta T_{ca1} < \Delta T_{ca2}$$

So it is easy to know that the module working at high environmental temperature requires a much smaller thermal resistance from the case to ambient than that of the module working at normal environmental temperature. In other words, a larger heat sink (or heat spreader) is required for the module working at high environmental temperature to achieve a lower thermal resistance from the case to ambient. The angles of α_1 and α_2 can represent the total thermal resistance of the junction to ambient, thus the module working under normal environmental temperature has a larger thermal resistance.

Fig. 4.4 compares the thermal designs for the Si and SiC based modules. Both modules work at normal environmental temperature and have the same heat dissipations. The junction-to-case temperatures for both are similar. That is:

$$\Delta T_{jc2} \approx \Delta T_{jc3}$$

Since the maximum allowable temperature of the SiC chip is much larger than the Si based chip, the case to ambient temperature ΔT_{jc2} of the SiC based module is much higher than the temperature ΔT_{jc3} of the Si based module. So:

$$\Delta T_{ca3} < \Delta T_{ca2}$$

The required thermal resistance of the SiC based module from the case to ambient is much larger than the Si based module, so the SiC based module requires a smaller cooling system than the Si based module.

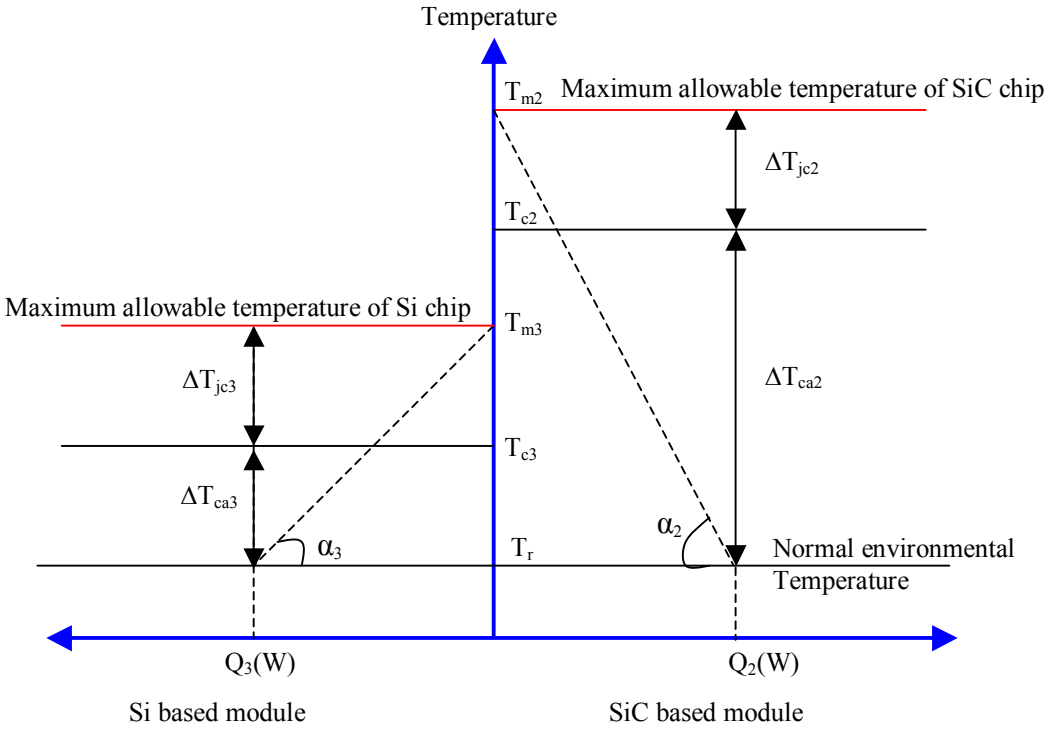


Fig. 4.4 Comparisons between the Si and SiC based modules

Therefore, from the comparisons, the SiC based module working under normal environmental temperature only requires the simplest cooling system in three cases. To demonstrate the cooling system reduction, the high temperature SiC ECM will be simulated using IDEAS software under high and normal environmental temperature respectively. Then the Si based module will be compared with the SiC based module under normal environmental temperature.

4.3.1 Under High Environmental Temperature

Table 4.1 Physical properties of different components

Item	*Material*	*Characteristic Thickness (mm)*	*Thermal Conductivity (W/m-K)*
Diode Chip	*SiC*	*0.425*	*120*
Substrate	*AlN*	*0.508*	*170*
Sealing material	*Glass/adhesive*	*0.508*	*0.96/0.577*
Screen-printing layer	*Glass*	*0.125*	*0.96*
Metallization layer	*Cu*	*0.075*	*380*

Any component level thermal analyses must consider the details of the power electronics package. Understanding the physical structure of the package is the first step in the analysis process. [49] The basic model of the high temperature single ECM are shown in Fig. 4.3. The finite element models included 2D linear triangle shell elements and 3D linear tetrahedron solid elements. To improve the accuracy of the simulation results, all available physical details, such as material properties and structure dimensions, were included in the models. Due to the thin layer of the interface materials, interface conditions within the modules were specified as equivalent thermal resistances, which are assumed to be zero in the simulation.

The ESC solver in the IDEAS software was employed in the simulations. The physical characteristics including thickness and thermal conductivity are shown in Table 4.1. Heat generation of 15W in the SiC chip was assumed to be uniform. The ambient temperature was chosen as 200^{o}C, since the used SiC Schottky diode is not suitable for temperature larger than 200^{o}C due to its large forward drops and leakage currents. One important heat path within the high temperature module was from the heat sources to the top metallization layer through the copper fillets as shown in Fig. 4.5. The heat path from the heat source through the adhesive sealant to the ceramic carrier or the top metallization layer is not important, since the adhesive has thermal resistance that is appreciably higher than AlN and metal. At the top surface of the metallization layer, heat was then transferred to ambient air through convection and the convection was assumed to have a

heat transfer coefficient at 20 or 80 W/m^2-K. Another important heat path is from the heat source to the bottom metallization layer. The bottom surface of the metallization layer was supposed to attach to a heat spreader or a heat sink. A reasonable thermal resistance between the environment and the bottom metallization layer is assumed as 0.67^{o}C/W, so the temperature difference between the bottom copper to the ambient is about 10^{o}C. Therefore, the boundary condition of the bottom surface of the metallization layer was at constant temperature of 210^{o}C.

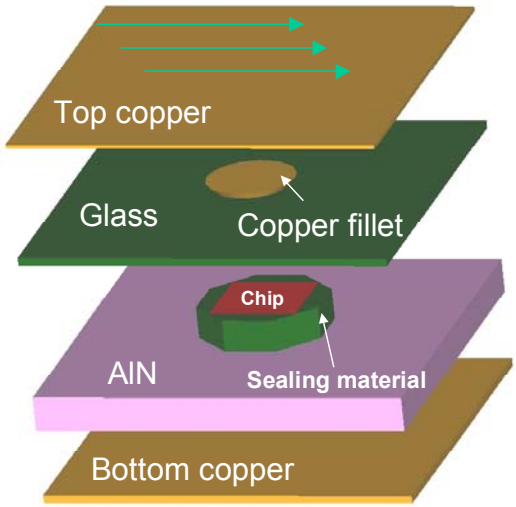


Fig. 4.5 Physical structure of a single chip ECM

The temperature distribution of four different layers in the high temperature ECM is shown in Fig.4.6. The heat is generated in the SiC chip, so the maximum temperature 224^{o}C is detected in the chip area. Since the sealing adhesive has very low thermal conductivity, the heat flux flows from the copper fillet to top copper layer almost in one dimenstional heat path. The heat dissipation from the top copper layer due to the convection could be calculated using equation 4.2,

$Q = h .A. (Tw - Ta) = 20 (36x10^{-6})(220-200) = 0.0144$ W

where the heat transfer coefficient h is 20 W/m^2-K, the convection surface area A is 36mm^2, the temperature of the top surface Tw is 220^{o}C, and Ta is the ambient temperature.

Therefore, due to the poor cooling on the top surface, 99.904% of the heat generated from the chip is dissipated from the bottom heat path.

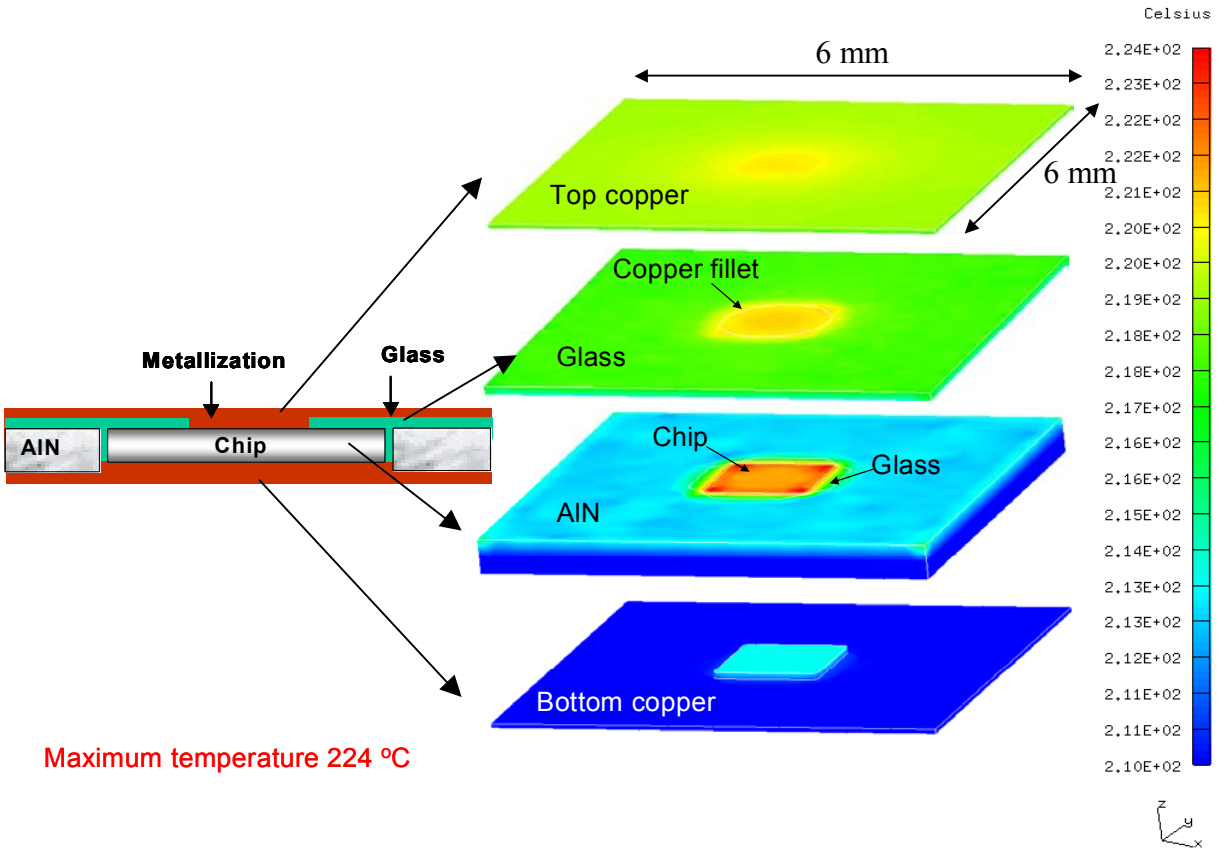


Fig. 4.6 Temperature distributions of a singe chip ECM with a 15W heat dissipation

4.3.2 Comparison to a Si Based module

Compared to the Si based power electronics module, the high temperature module can operate at a higher temperature with the same environmental temperature, thus eliminating the bulky cooling system and increasing the power density. The thermal analysis for high temperature applications is to keep the temperature at a safe operating level while minimizing the cooling system.

A one-dimensional thermal model can be used to describe the single chip ECM shown in Fig.4.5. Four thermal resistances are employed to describe the heat path shown in Fig.4.7. The heat is generated in the chip and flows through the metal fillet to the top and bottom metal surface (R_{jt} and R_{jb}) then dissipates to the air (R_{ta} and R_{ba}). In this thermal model, R_{jt} is the thermal resistance between the junction to top metal surface, R_{ta} is the thermal resistance between the top metal surface to ambient, R_{jb} is the thermal resistance between the junction to bottom metal surface, and R_{ba} is the thermal resistance between the bottom copper surface to ambient.

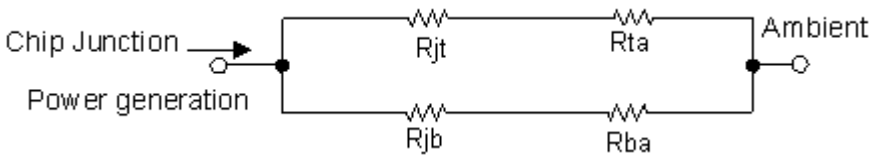


Fig. 4.7 One-dimensional thermal model for single ECM

We assume that the maximum safe temperature in ECM is 224°C and the environment temperature is 24°C. The dissipated heat from the chip is 15W. Due to the poor heat dissipation caused by the small top surface as discussed previously, we only consider the heat path from the bottom side to the air and all heat generation is assumed to be dissipated from bottom side. As shown in Fig. 4.7, the resistance R_{jb} is composed by half of the chip resistance R_{chip} and the copper fillet resistance R_{fillet}. Therefore, we can calculate the R_{jb} using equation 4.1 and 4.3, then we know the copper surface temperature Tw is 207.78°C. So we can know the required surface area for heat dissipation under convection at 20 and 80 W/m^2-K [45] using equation 4.7.

$$R_{jb} = R_{chip} + R_{fillet} = 0.946 + 0.1356 = 1.0816 \ ^{o}\text{C/W} \tag{4.6}$$

$$A = \frac{Q}{h(T_w - T_o)} \tag{4.7}$$

Table 4.2 Comparison of a Si based module and a high temperature ECM

Convection Condition	h=20 W/m^2-K		h=80 W/m^2-K	
Maximum safe operating temperature (oC)	84	224	84	224
Heat transfer coefficient (W/m^2-K)	20	20	80	80
Required heat dissipated area (cm^2)	171.3	40.8	42.825	10.2
Length of 2mm thick heat spreader(cm)	9.1	4.33	4.43	2.08

If the Si based module has the same structure and dimension as the high temperature ECM shown in the Fig. 4.5, Table 4.2 shows the enormous reduction on the cooling system by applying high temperature ECM in the environment temperature 24°C. Under both convection conditions, the high temperature ECM only requires 23.81% heat

dissipation areas of the Si based module as shown in Fig.4.8. Under forced convections with h at 80 W/m^2-K, the high temperature ECM shown in Fig. 4.5 only requires a heat spreader with the size of 2.08 x 2.08 x 0.2 cm to dissipate 15W heat generation.

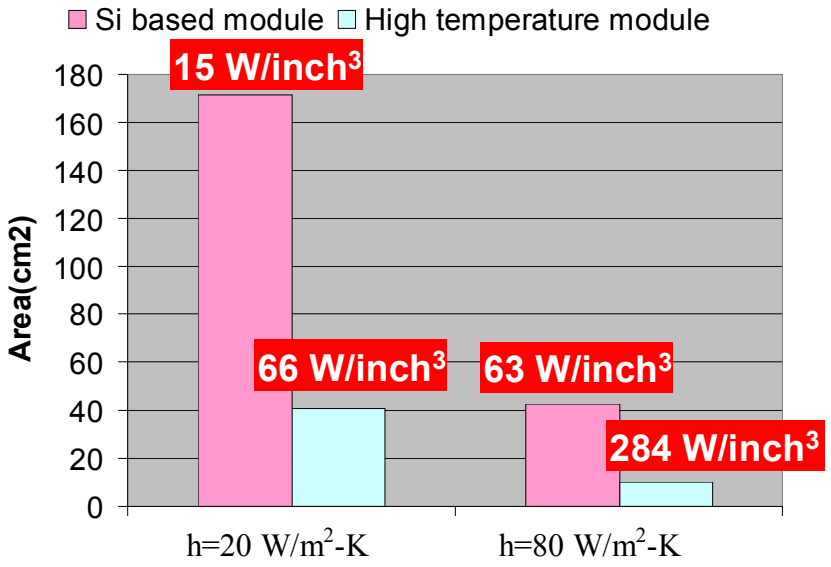


Fig. 4.8 Comparisons of the required dissipation areas

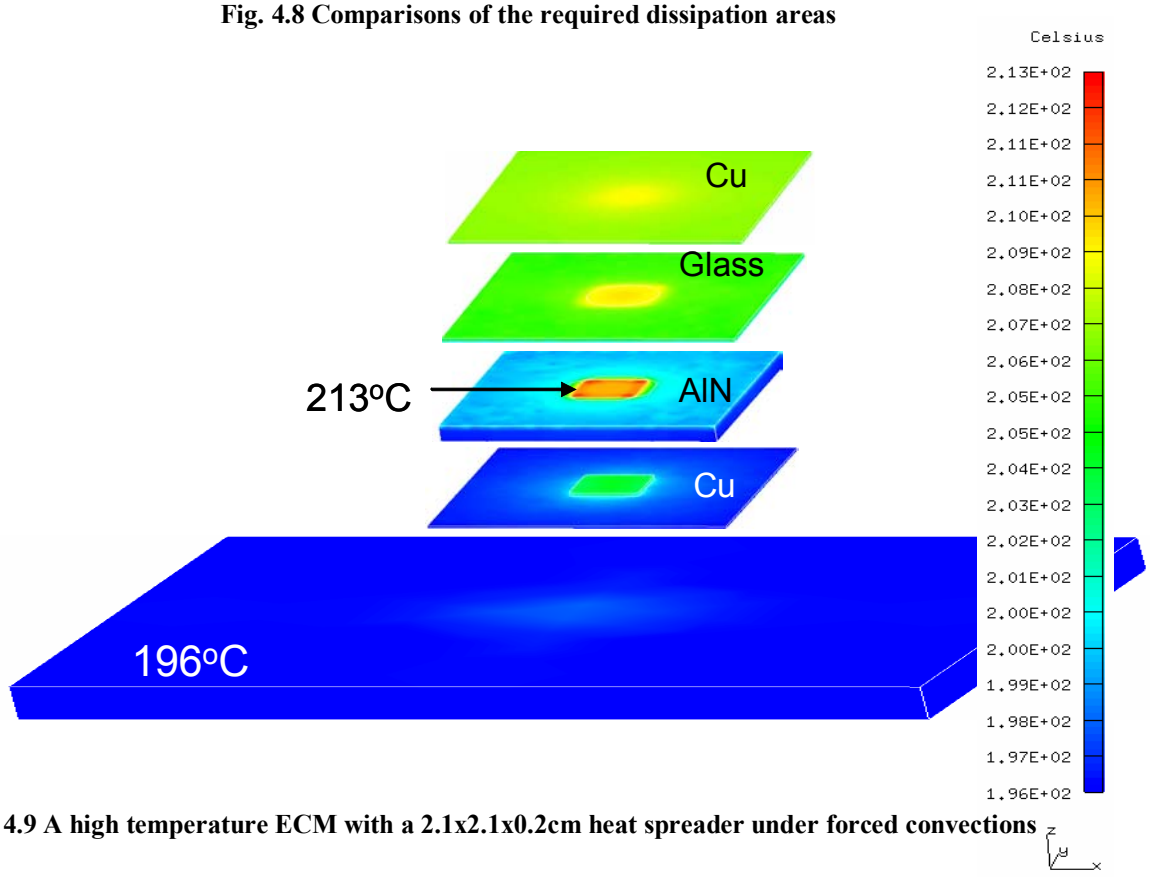


Fig. 4.9 A high temperature ECM with a 2.1x2.1x0.2cm heat spreader under forced convections

Fig. 4.9 presents an example to show the cooling system for an ECM under forced convections with h at 80W/m^2-K. The ECM is attached to a heat spreader with 2.1 x 2.1 x 0.2cm at environment temperature 24^{o}C. The maximum junction temperature in the ECM is 213^{o}C, which is under the designed safe operating temperature 224^{o}C.

4.4 Theoretical Behavior of SiC Chip Reverse Characteristics at High Temperature

The reverse characteristics are important for high temperature applications, since the Schottky leakage current increases dramatically as the temperature climbs higher than 200^{o}C. A leakage current that is too large will decrease the voltage rating, or even destroy the device and limit the device applications. The leakage current of Schottky rectifiers consists of the space charge generation current from the depletion region, the diffusion current from the semiconductor neutral region, and the thermionic current across the barrier. The first two components are the same as those observed in P-i-N rectifier. The third component is substantially greater than that for P-i-N rectifiers. This has been an important limitation to the high temperature performance of Schottky rectifiers. [50] [51]

When a reverse bias voltage V_R is applied to the Schottky barrier, the leakage current density can be expressed as below:

$$J_R = AT^2 e^{-(q\phi_{bn}/kT)}[e^{-(qV_R/kT)} - 1] \tag{4.8}$$

Where A is the effective Richardson constant A/(cm^{2}K^2), T is the device temperature (K), q is electron charge, Φ_{bn} is the barrier height between the metal and semiconductor (eV), and k is Boltzmann's constant.

For the material 4H-SiC, equation 4.8 can be drawn in Fig. 4.10 at 100^{o}C, 150^{o}C, 190^{o}C and 236^{o}C. The leakage current at a certain temperature is almost constant with the reverse voltage increasing, while becoming larger with the temperature increasing. The leakage currents at 100^{o}C and 150^{o}C are too small to be seen in Fig. 4.10.

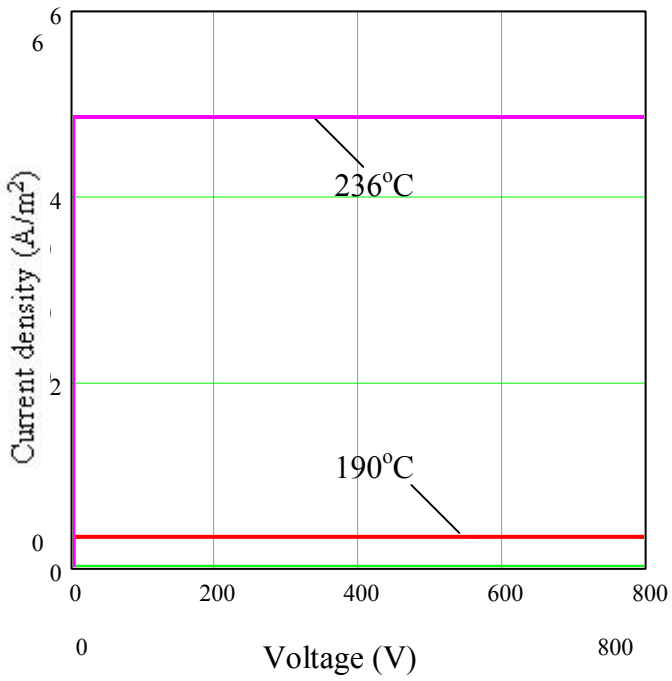


Fig. 4.10 Reverse characteristics without barrier lowing

In Eq. 4.8, the barrier height is given as a constant. Under the application of the reverse bias voltage, it has been found that there is a reduction in the Schottky barrier height due to image force lowering. This image force lowering is caused by the positive mirror image charge of the same magnitude in the metal, when an electron in the semiconductor approaches the metal.

The reduction in the barrier height due to image force lowering, indicated as $\Delta\Phi_b$, is given by:

$$\Delta\Phi_b = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}} \tag{4.9}$$

where ε_s is the SiC dielectric constant. The maximum electric field E_m is related to the applied reverse bias V_R by:

$$E_m = \sqrt{\frac{2qN_d}{\varepsilon_s}(V_R + V_{bi})} \tag{4.10}$$

where N_d is the drift region doping concentration ($1/cm^3$).

Although the reduction in barrier height is a small change, it is an important phenomenon which contributes to an increase in the reverse leakage current with increasing reverse bias voltage because the leakage current is an exponential function of the barrier height. Therefore, the reverse leakage current including the Schottky barrier lowering effect is given by:

$$J_R = AT^2 e^{-(q(\phi_{bn}-\Delta\Phi_b)/kT)}[e^{-(qV_R/kT)} - 1] \tag{4.11}$$

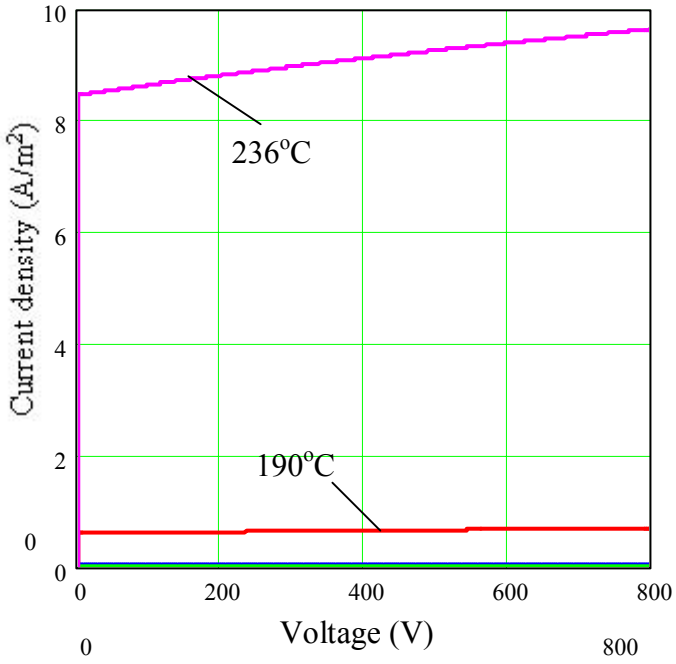


Fig. 4.11 Reverse characteristics with barrier lowing

In addition, the leakage current of the Schottky rectifier contains the space charge generation component (which increases with reverse bias voltage) and the diffusion component. These components to the leakage current represent only a small fraction of the total leakage current, which can usually be neglected. The calculated leakage of the 4H-SiC diode can be shown as in Fig. 4.11. Due to the barrier lowering effect, the leakage currents will increase slowly as the reverse bias voltages increase.

In order to account for the larger reverse leakage current at high reverse bias voltages, it is necessary to take into account the pre-avalanche multiplication of carriers at the high electric fields when the applied reverse bias approaches close to the breakdown voltage. The impact ionization process can be treated as a purely electron initiated process using

the electron current injected across the metal-semiconductor interface by thermionic emission. The total electrons that reach the edge of the depletion region will be larger than those injected at the metal-semiconductor interface by a factor M_n, the electron multiplication factor. Then this multiplication coefficient M_n can be given by:

$$M_n = \frac{1}{1-1.52(1-e^{\frac{-4.33\times10^{-24}E_m^{4.93}W}{1+n}})} \tag{4.12}$$

where W is the thickness of the depletion region.

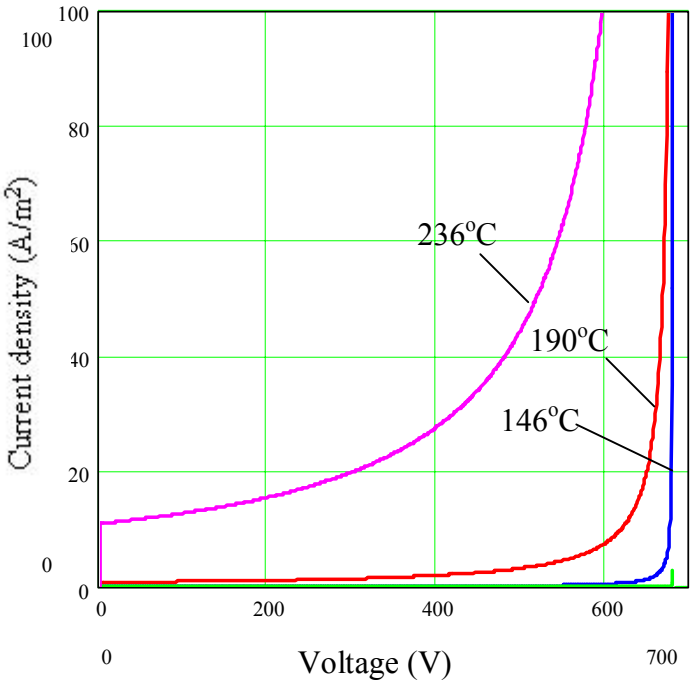


Fig. 4.12 Reverse characteristics with barrier lowing and multiplication

So the reverse characteristics of the 4H-SiC Schottky diode are shown in Fig. 4.12 by considering the barrier lowering effect and the pre-avalanche multiplication. As shown in Fig. 4.12, when the temperature is below 200°C, the leakage currents are relatively low while the reverse voltage is below the breakdown voltage 600V. However, as the temperature becomes higher more than 200°C, the leakage current increases dramatically, even when the reverse voltage is below the break down voltage.

4.5 Summary

In this chapter, thermal models, including the 1-D and 3-D FEM, are introduced to analyze the high temperature ECM. Under high environmental temperature with 15W heat generation, the junction temperature of the SiC chip is 24^{o}C higher than the environmental temperature and it has a similar cooling system to the Si based module. However, an enormous reduction in the cooling system is obtained using the high temperature ECM under normal environmental temperature. The high temperature ECM only requires 23.81% heat dissipating areas compared to the Si based module, while it only requires a heat spreader with a size of 2.08 x 2.08 x 0.2cm to dissipate 15W heat generation and finally achieves a power density of 284 W/inch^{3}. The theoretical SiC Schottky reverse characteristics are analyzed with considerations of the barrier lowering and the pre-avalanche multiplication effects. The predicted curves show that the leakage current increases dramatically when the temperature increases more than 200^{o}C.

Chapter 5

Thermo-mechanical Analysis of a High Temperature Embedded Chip Module (ECM)

5.1 Thermo-mechanical Model of the Embedded Chip Module (ECM)

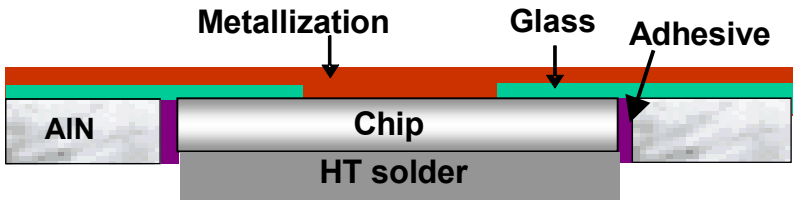
Thermo-mechanical stress due to the thermal mismatch in the high temperature ECM will affect long-term reliability. The temperature difference inside the chip, which is caused by power dissipation, as well as the environmental temperature change, will produce thermo-mechanical stress. During the packaging process, residual stress will be introduced to the chip because of the sandwich structure of the packaging, due to the difference of the material characteristics such as Young's modulus, linear expansion coefficient and thermal conductivity. [52]-[54] The residual stress and thermo-mechanical stress will fracture the chip, make cracks on the ceramic substrate or result in a metallization failure. In this chapter, thermo-mechanical stress due to temperature changes in the high temperature module, from the room temperature to the operating temperature about 210^{o}C, is studied.

Table 5.1 shows the mechanical properties of the different parts and materials in the ECM. For high temperature applications, the thermo-mechanical stress caused by temperature change is severe. In this respect, it also has to be taken into account that the different materials in the structure have different temperatures of zero stress. For solder it is the melting temperature, for an electroplated layer it is approximately room temperature, while for example for glass or sintered layers it is again different. Therefore, the proper material selection to attain CTE match in the ECM is important. To choose suitable materials and obtain the lowest stress at high temperature, six cases in Fig. 5.1 are compared with different structures and materials, taking all the different stress free temperature into account. The first case, which is shown in Fig. 5.1 (a), is a bench mark with an unbalanced structure. The copper metallization is only used for the topside connections, while a high temperature solder Au80Sn20 is employed as the die

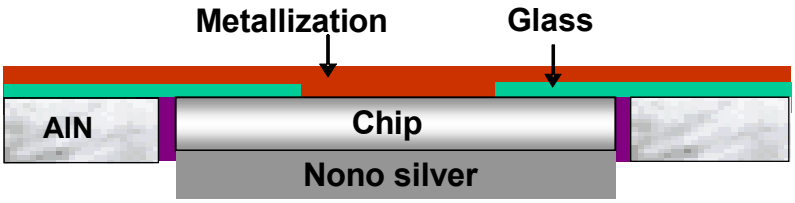
attachment material. Case 2 has a similar unbalanced structure, while nanoscale silver [55] is used to replace the high temperature solder as die attachment material. Case 3 shows another unbalanced structure with only one side Cu metallization layer and no material under the chip to present the extreme case of very soft die-attach material. Case 4 presents the proposed balanced structure using the bottom metallization layer to replace the die attachment materials in case 1 and 2. Since it may cause a bending effect due to the thicker AlN substrate as compared to the SiC chip in the module shown in Table 5.1, we change the thickness of the AlN substrate to the same value as the SiC chip in case 5. To further reduce the stress, the proposed low CTE metal Mo in case 6 is applied to replace the Cu metallization layer, which has a high CTE of 16.5ppm/^{o}C.

Table 5.1 Important properties of different parts and materials

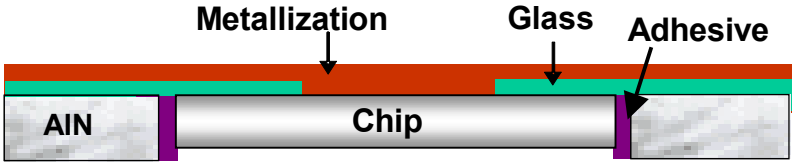
Item	*Material*	*Characteristic Thickness (mm)*	*CTE (ppm/oC)*	*Module of Elasticity (GPa)*	*Stress-free Temperature (^{o}C)*
Diode Chip	*SiC*	*0.425*	*4*	*420*	*25*
Substrate	*AlN*	*0.508*	*4.5*	*329.7*	*25*
Sealing material	*Resbond*	*0.508*	*4.5*	*70*	*25*
Screen-printing layer	*Glass*	*0.125*	*6.4*	*70*	*400*
Metallization layer	*Cu*	*0.075*	*16.5*	*124*	*25*
Metallization layer	*Mo*	*0.075*	*4.8*	*329*	*25*
High temperature solder	*Au80Sn20*	*0.085*	*16.5*	*136*	*390*
Nanoscale silver	*Ag*	*0.085*	*19*	*10*	*390*



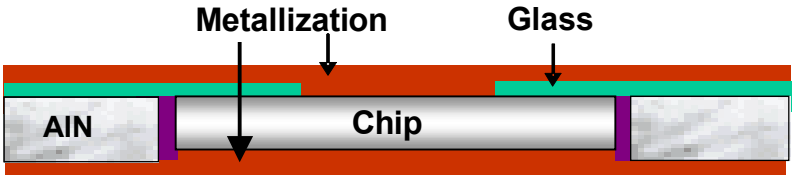
(a) Case 1 with high temperature solder attachment



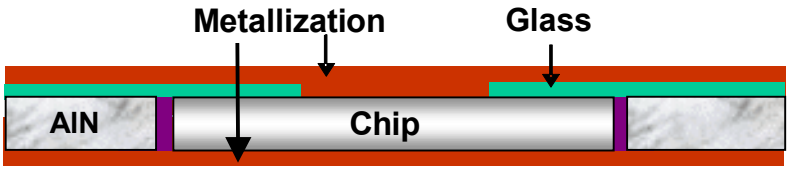
(b) Case 2 with Nanoscale silver attachment



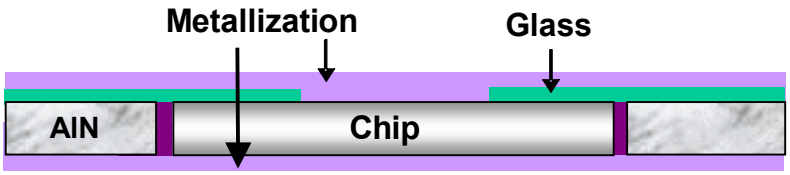
(c) Case 3 with no material under the chip



(d) Case 4 with double-sided metallization



(e) Case 5 with the same thickness of chip and AlN substrate



(f) Case 6 with Mo metallization layer

Fig. 5.1 Comparison to obtain the optimal structure

5.2 Simulation

The stress simulations were conducted using the structural analysis within the IDEAS software. Since different materials require different processing temperature during fabrication, this will affect the stress in the different layers. For example, due to the high firing temperature up to 400^{o}C during the glass fabrication process, if we assume that its mechanical stress at firing temperature is zero, high stress will occur at low temperature between the glass and other layers. However, other materials, such as copper and ceramic adhesive, are applied at room temperature; therefore, we set the room temperature as the stress free temperature for these materials. The temperature of the structure was increased from 25°C to about 210°C and the temperature distribution from thermal simulation is used as the input for the stress simulation to obtain the mechanical stress distribution. The type of element used for the stress simulations is solid parabolic tetrahedron. Also, we assume that the stress and strain always have a linear relationship, so we can compare and optimize module structures evidently even when the mechanical stress is over the material's yield stress.

The displacement constraint of the structure is shown in Fig. 5.2. The point A located at the corner of the bottom surface of the metallization layer was fully constrained (translational and rotational) in all directions, while the second point B located at another corner of the metallization layer illustrated in Fig. 5.2 was constrained in the x and y direction. The third point C at the corner of the metallization layer was constrained only in the z direction. The cutting plane presents the mechanical-stress distributions is in the middle of the ECM module at section T-T as shown in Fig 5.2.

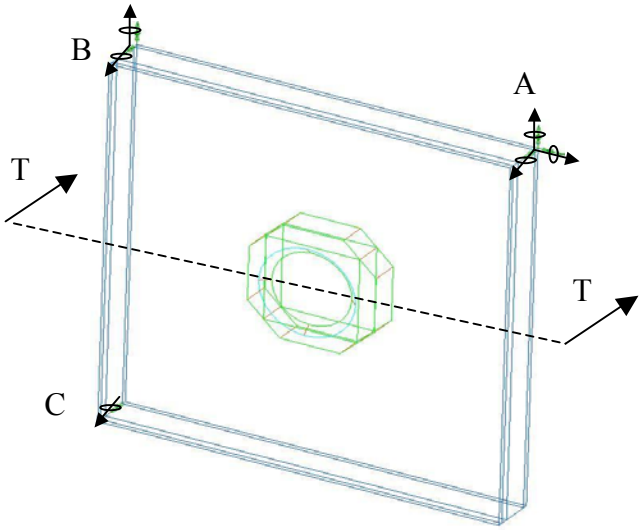
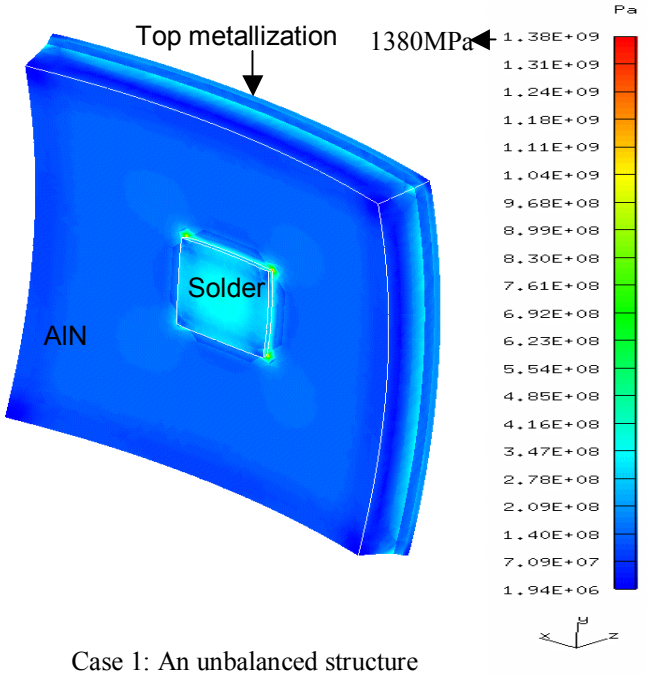
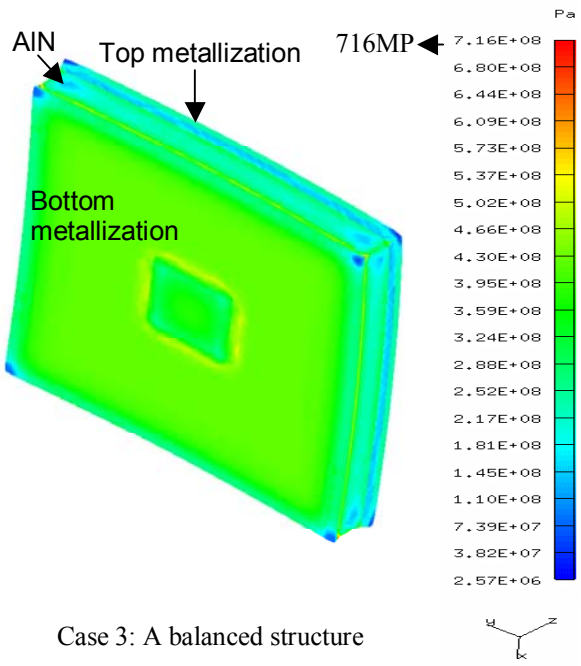


Fig. 5.2 The ECM structure with displacement constraints

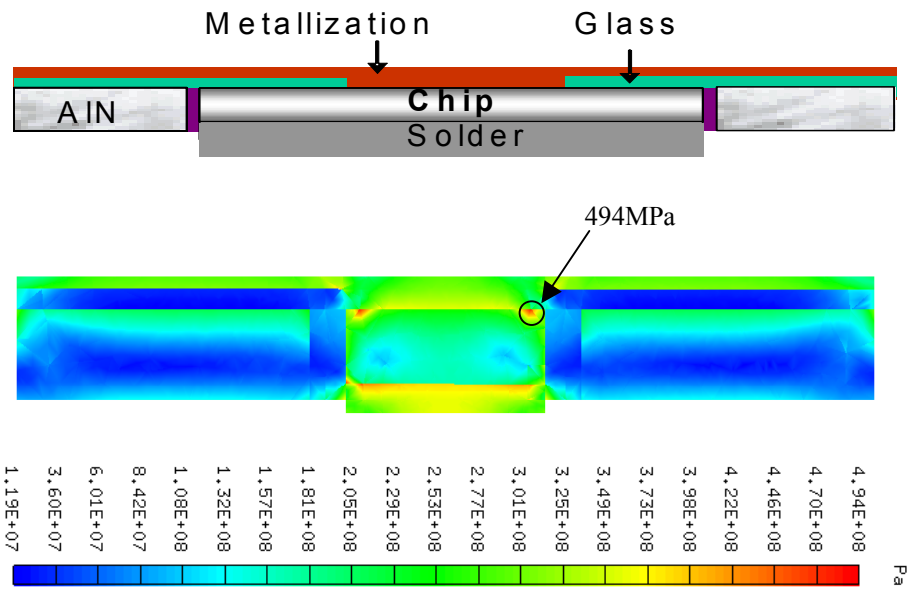


Case 1: An unbalanced structure

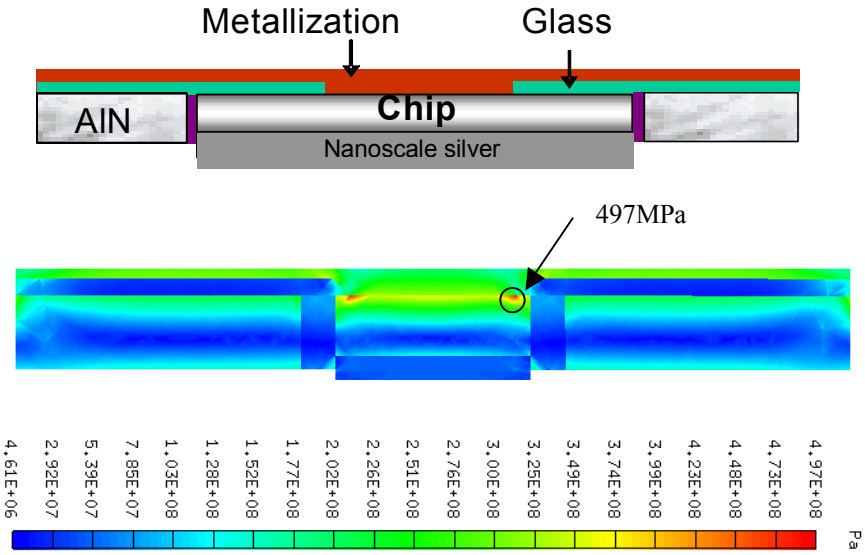


Case 3: A balanced structure

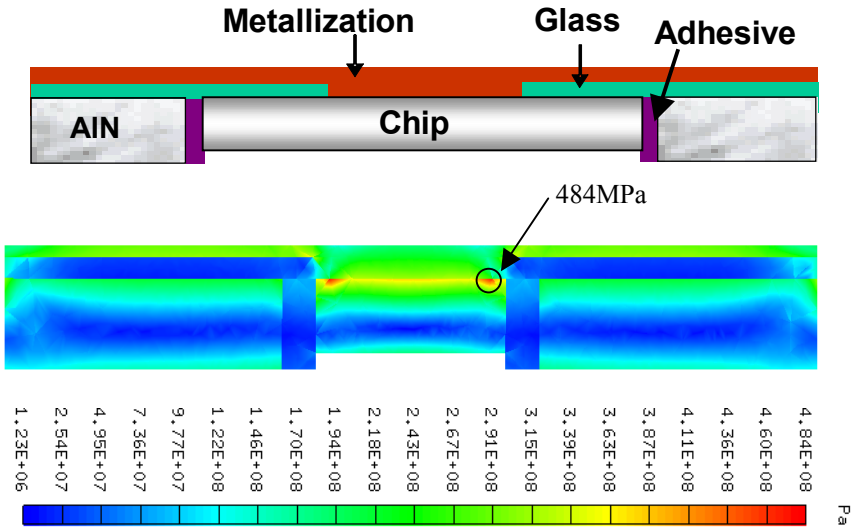
(a) Structure comparisons



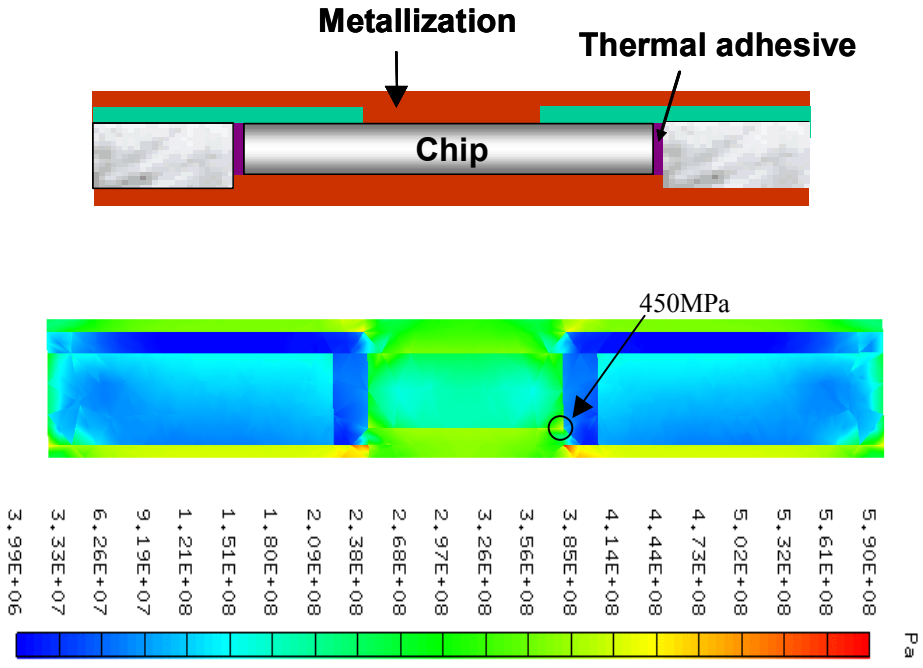
(b) Case 1



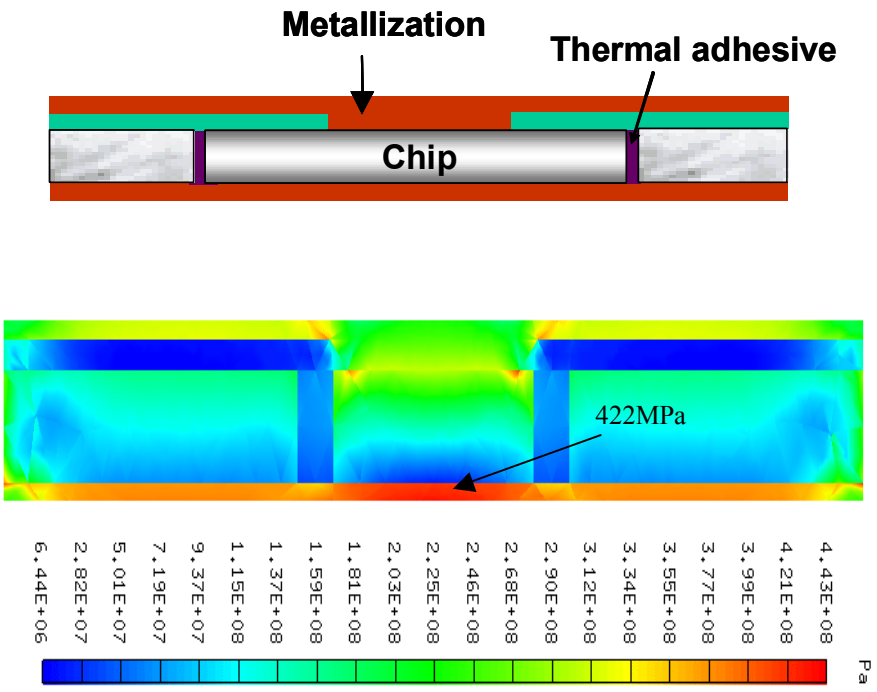
(c) Case 2



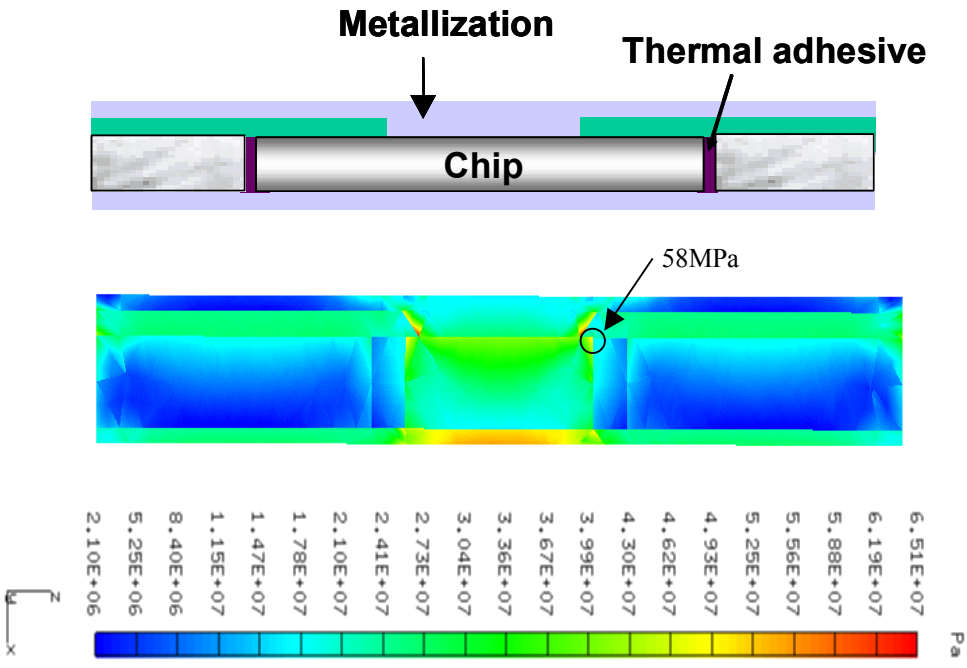
(d) Case 3



(e)Case 4



(f)Case 5



(g) Case 6

Fig. 5.3 Mechanical stress comparisons

For case 1 of the unbalanced structure shown in Fig. 5.1(a), the stress simulation result is shown in Fig. 5.3(a), by assuming the linear relationship between the stress and strain. The maximum stress 1380MPa occurs between the solder and the AlN substrate due to the large bending effect caused by the mechanically unbalanced structure. The yield stress of the high temperature solder Au80sn20 is 270MPa [56]. The stress simulation result of the proposed balanced structure case 3 is also shown in Fig. 5.3(a). The maximum stress 716MPa is located between the ceramic adhesive and the Cu metallization layer. The yield stress of plated Cu is in the range of 260-440MPa [57]. Although the balanced structure still has a large stress in the module, its stress distribution is more uniform and the maximum stress is reduced by 48.1% compared to the unbalanced structure case 1. Additionally, almost no bending is found in the balanced structure.

Since the maximum stress in the module normally occurs at the sharp edges or corners, which are impractical in the real case, we only consider the stress distributions in the cutting plane presented in Fig. 5.2. Fig. 5.3 shows the mechanical stress distributions of case 1 to 6. Since the nanoscale silver has much lower elastic modulus than the high temperature solder in case 1, the stress between the chip and the attachment in case 2 is reduced largely compared to case 1. However, both cases have the maximum stress of about 495MPa between the chip and Cu metallization due to the bending effect, which is caused by their unbalanced structures. Since the nanoscale silver is a very soft material, the simulation results of case 2 is similar to case 3, which has only topside metallization and no material under the chip. Therefore, from case 1 to 3, the bending effect due to the mechanically unbalanced structure causes a larger stress in the chip area in comparison to the balanced structure.

As a balanced structure, case 4 has the chip area maximum stress at 450MPa. However, it still has the internal imbalance caused by the thicker AlN substrate compared to the chip, so the high stress point 590MPa in case 4 is detected at the bottom copper layer near the ceramic adhesive due to the bending effect. To further reduce this stress, the AlN substrate is chosen as the same thickness as the chip in case 5, shown in Fig. 5.3 (f). Thus, a more uniform stress distribution is achieved at the bottom copper layer, although the maximum stress is still high up at 443MPa due to the large CTE of the copper. The chip

area maximum stress in case 5 is 422MPa. In case 6, by employing a low CTE metal Mo, a uniform stress distribution with the highest stress 65MPa is shown in Fig. 5.3(g).

5.3 Comparisons and improvements

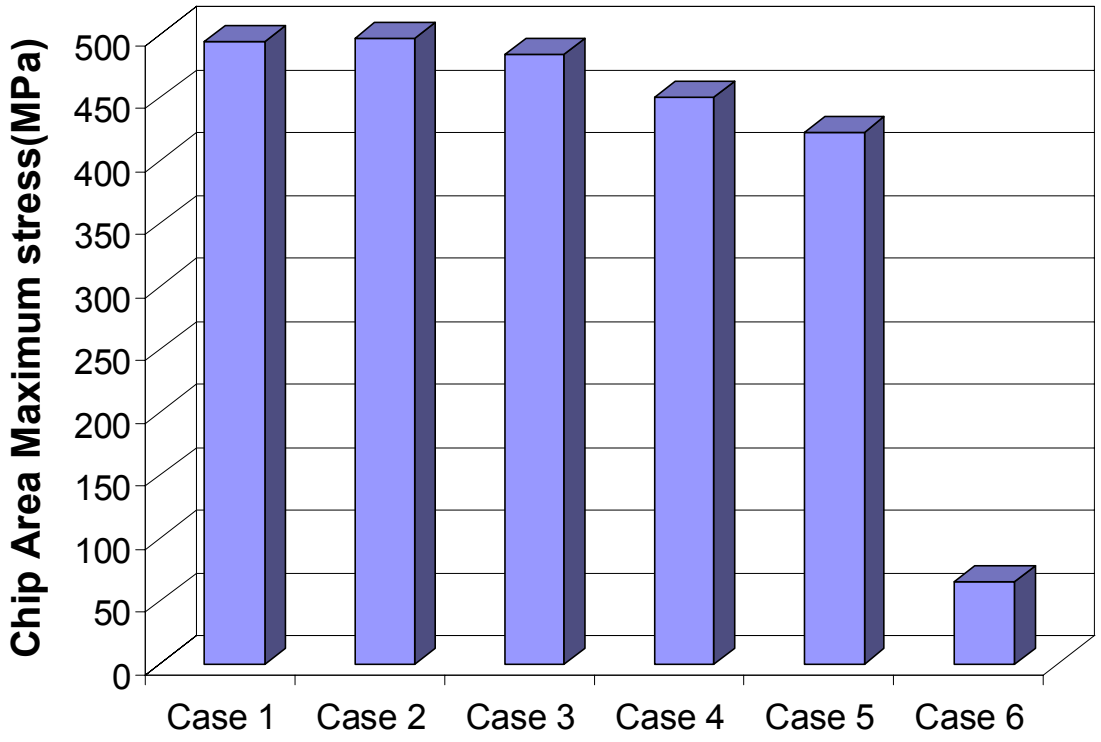


Fig. 5.4 Maximum stress comparisons

The chip area maximum stress is located at the interface between the metal and the SiC chip, which is the weakest bonding in the structure. So the chip area stress should be considered carefully and reduced a harmless level. In Fig. 5.4, the chip area maximum stresses of six different cases are compared by changing the materials and structure in the high temperature ECM. Since the mechanically balanced structure is important for high temperature applications, case 1 to 3 show the high maximum stress about 500MPa due to the bending effect, which is caused by their unbalanced structures. Even in the balanced structures, the internal balance is still important for reducing the stress. By removing the internal imbalance due to the thicker substrate, case 5 reduces the chip area

maximum stress to 422MPa from 450MPa in case 4. Thickness match avoids a bending effect in the structure, thus enables the double-sided metallization to achieve a mechanically balanced structure for both sides. The CTE match is another key concern in high temperature applications. Due to the high CTE of copper metallization, both case 4 and 5 have CTE mismatch problems, so they still have large stresses in the structure. By choosing a low CTE metal, such as Mo, case 6 has almost similar CTEs for different materials, thus achieves a low stress 58MPa and leads to a uniform stress distribution in the structure.

The advantage of avoiding the high CTE of the copper metallization is shown by using the metal Mo for the metallization layers. The maximum stress in case 6 decreases dramatically to only 58MPa and is reduced by 88% compared to case 1. The uniform stress in the structure will achieve a robust configuration and improve the long-time module reliability.

From the comparison of Fig. 5.4, the stress is very high using the Cu metallization layer and the high stress of about 500MPa normally occurs at the interface between the chip and Cu metallization layer. Such a high mechanical stress will cause module failure quickly. Therefore, in order to achieve a good CTE match and an excellent long term reliability performance, the high CTE Cu metallization must be replaced by a metal with a similar CTE to the SiC chip. Although Mo seems like a very good candidate for the metallization layer, pure Mo can not be electroplated. [31]-[33] Only the alloys of Mo and the iron family metals such as Ni and Fe can be electroplated. However, the CTE of the alloys is unknown and maybe very high due to the high CTE of the iron family metals. Therefore, as stated in 3.3.2, to reduce the stress, we can use a combined metallization layer with a low CTE-metal that can be electroplated as a stress buffering layer and Cu for the current carrying layer. Such a metal is chromium as will be discussed subsequently.

To implement the combined metallization layers and achieve an optimal structure, we changed two variables in the module, one is the thickness of the Cr layer d and the other one is the Cr layer angle α, as shown in Fig. 5.5(a). Fig. 5.5(b) shows the stress distributions of the cross-sectional area for a specific case. The Cu metallization layers at both sides are fixed at a constant thickness 65um, which is adequate for carrying currents.

We checked two mechanical stresses in the cross-sectional area: the chip area maximum stress and the maximum stress between the Cr and Cu. The chip area maximum stress is in the chip top surface under the edge of the Cr layer, on which the maximum stress between the Cr and Cu occurs. The chip area maximum stress is located at the interface between the metal and the SiC chip, which is the weakest bonding in the structure, thus should be reduced to a harmless level less than 200MPa. The larger interface between chromium and copper presents a metal-to-metal bonding. It is reasonable to expect this interface to be resistant to much higher stresses than the metal-to-semiconductor interface.[58]

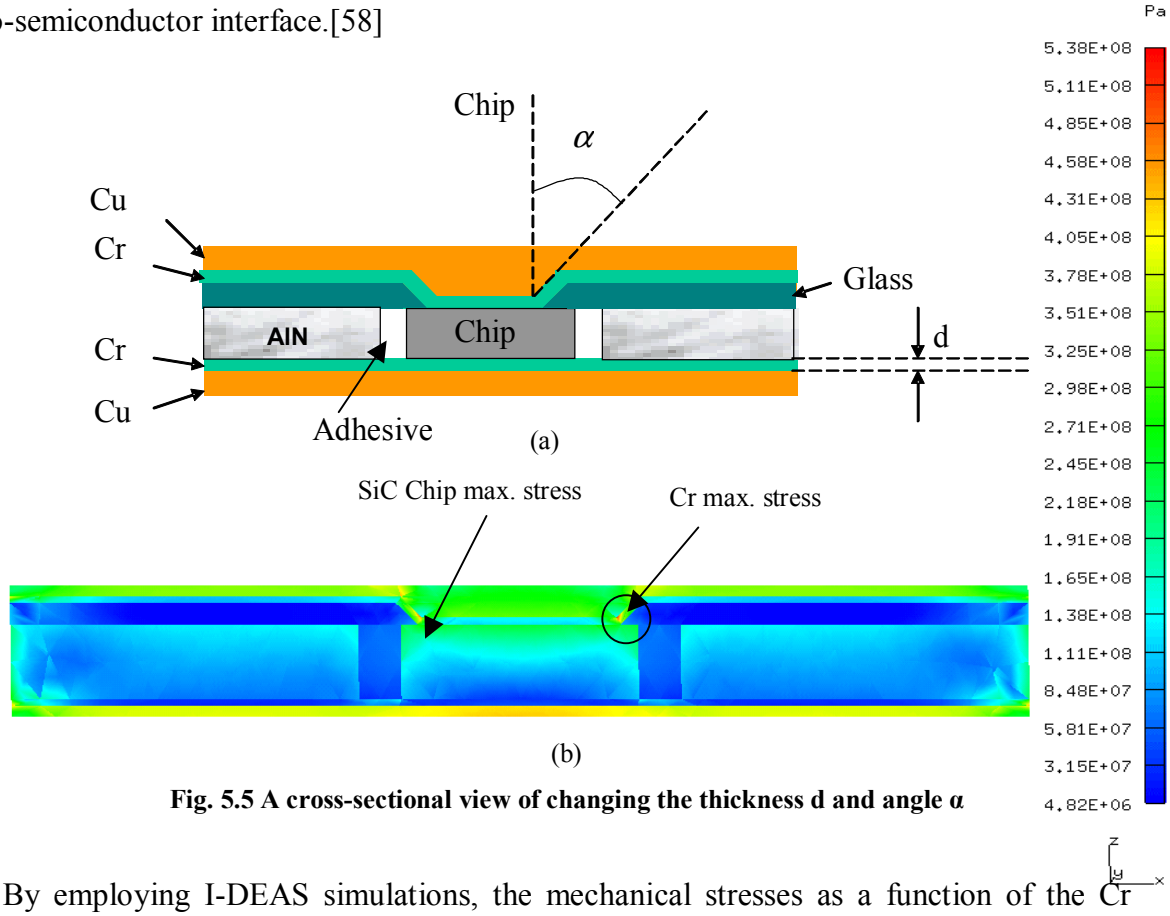


Fig. 5.5 A cross-sectional view of changing the thickness d and angle α

By employing I-DEAS simulations, the mechanical stresses as a function of the Cr layer thickness d are presented in Fig. 5.6. As the Cr thickness increases to 50um, all three mechanical stresses decrease very linearly. However, the mechanical stresses become almost constant when the thickness is larger than 50um. Therefore, 50um is the desired Cr thickness for the stress buffering layer. At this thickness, the module can attain the minimum stress while keeping Cr thickness as thin as possible to reduce the vertical electrical resistance. The chip area maximum stress shown in Fig. 5.6 is still very high

between 250MPa to 390MPa, so it is difficult to achieve the desired stress by only changing the Cr thickness.

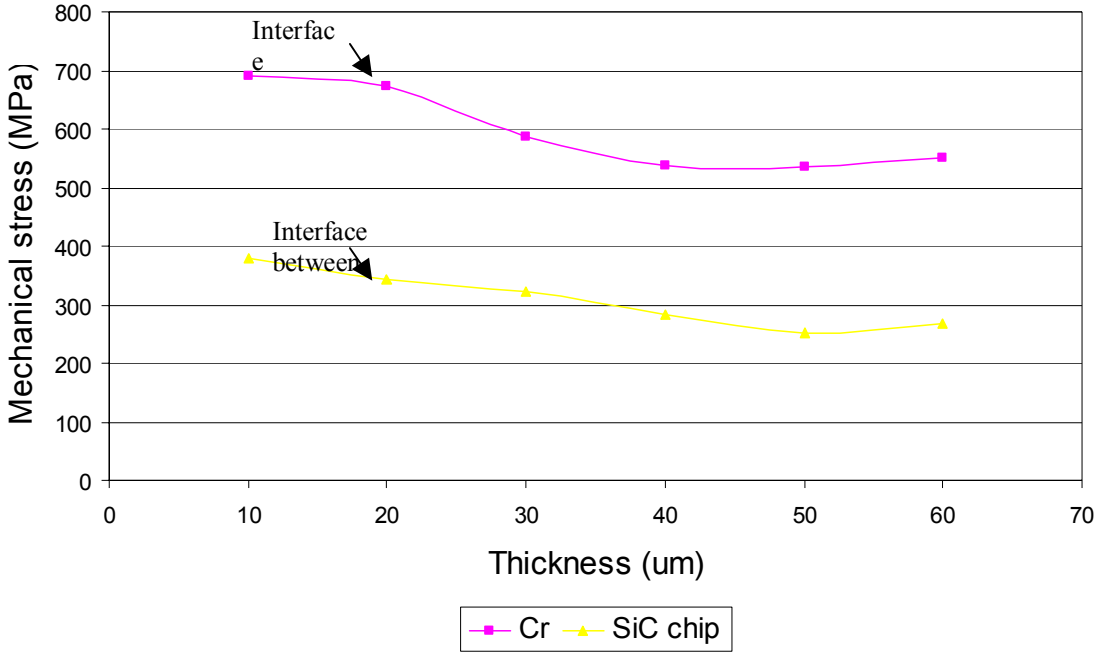


Fig. 5.6 Mechanical stresses changed with Cr thickness d

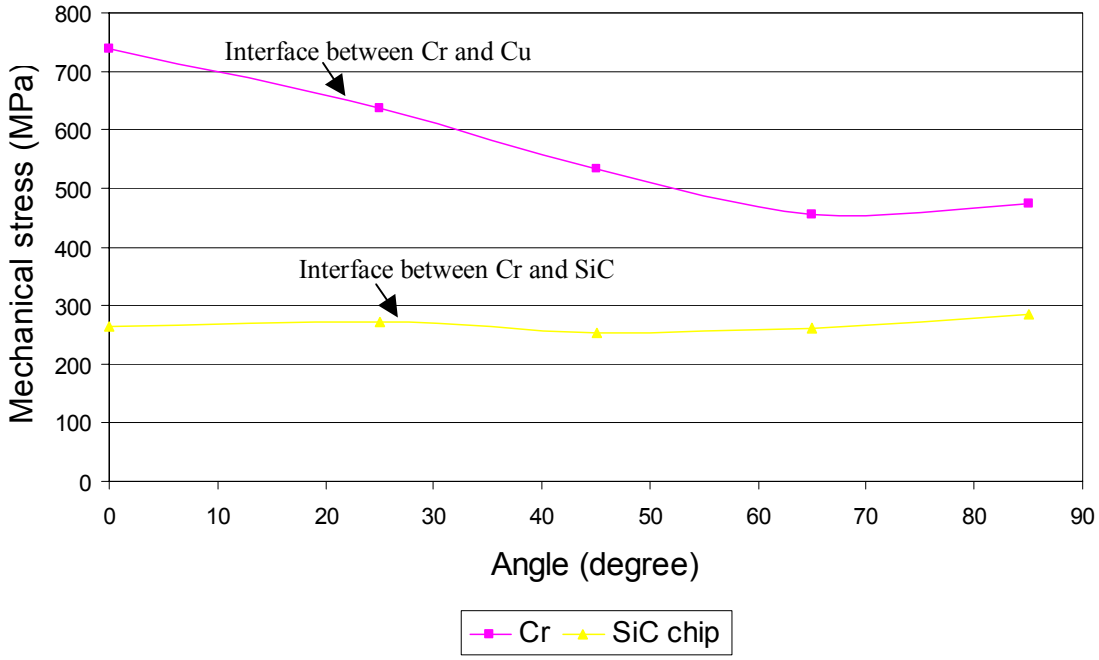


Fig. 5.7 Mechanical stresses changed with Cr layer at 50um and as a function of angle α

While keeping the desired Cr thickness at 50um, we changed the Cr layer angle α above the chip from 0^o to 85^o. The simulation results are shown in Fig. 5.7. As the angle α becomes larger, the metallization layer structure is closer to a flat metallization layer, thus the stress between Cr and Cu becomes smaller. However, the maximum stress of the chip area has no relationship with the angles and is almost unchanged at about 260MPa. Therefore, we can't reduce the maximum chip area stress to a harmless level by changing the angle of the Cr layer. Further adjusting on the metallization structure should be considered for the chip area stress reduction.

Due to the CTE mismatch between the Cu and Cr layers, the sharp corners or uneven metallization layers could cause high stress distributions. By using the flat metallization layers shown in Fig. 3.7(a), the maximum stress of the chip area can be reduced to a very low level around 100MPa. So we chose the flat metallization structure shown in Fig. 5.8 to further reduce the stress of the chip area. In this structure, we choose the desired Cr layer thickness at 50um and the Cu layer thickness at 65um. The interface between the Cu and Cr metallization layers is kept planer to avoid stress crowding. The simulation results in Fig. 5.8 are very similar to the flat metallization layer simulations shown in Fig. 3.7(a). The maximum stress occurs at the edges, while the stress distributions are almost horizontally uniform in the middle part. The chip area maximum stress has been reduced to 163MPa and the Cr maximum stress above the chip to 147MPa. Although the Cu metallization layer shows relatively high mechanical stress about 400MPa, the metal-to-metal bonding is robust, thus the higher stress between Cr and Cu is considered acceptable.

Although the stress can be reduced to an acceptable level by using the Cr buffering layer, additional electrical resistance could be introduced in the current flow path due to the high electrical resistivity of the Cr layer. As shown in Fig. 5.8(a), to attain the flat metallization layers, a Cr fillet, which has a thickness 100um identical to the glass layer has to be filled on the chip top surface. Therefore, the additional resistance caused by this Cr fillet as well as the flat Cr metallization layer should be considered carefully. For the worst case, the current flows from the chip to the Cu metallization layer only through the Cr cylinder, which has a thickness h and a diameter D as shown in Fig. 5.8(a). So the additional resistance due to the use of Cr can be calculated as:

$$R = \frac{\rho \cdot h}{\pi(\frac{D}{2})^2} = 2.427 \times 10^{-5}\,\Omega$$

where ρ is the Cr electrical resistivity at 12.7uΩ.cm, h is the thickness of the Cr cylinder 150um and D is the diameter of the Cr cylinder 1mm.

The additional resistance for the worst case due to the use for the Cr layer is only 24.27uΩ, so this demonstrates that the resistance increase due to the Cr buffering layer can be neglected in the electrical design.

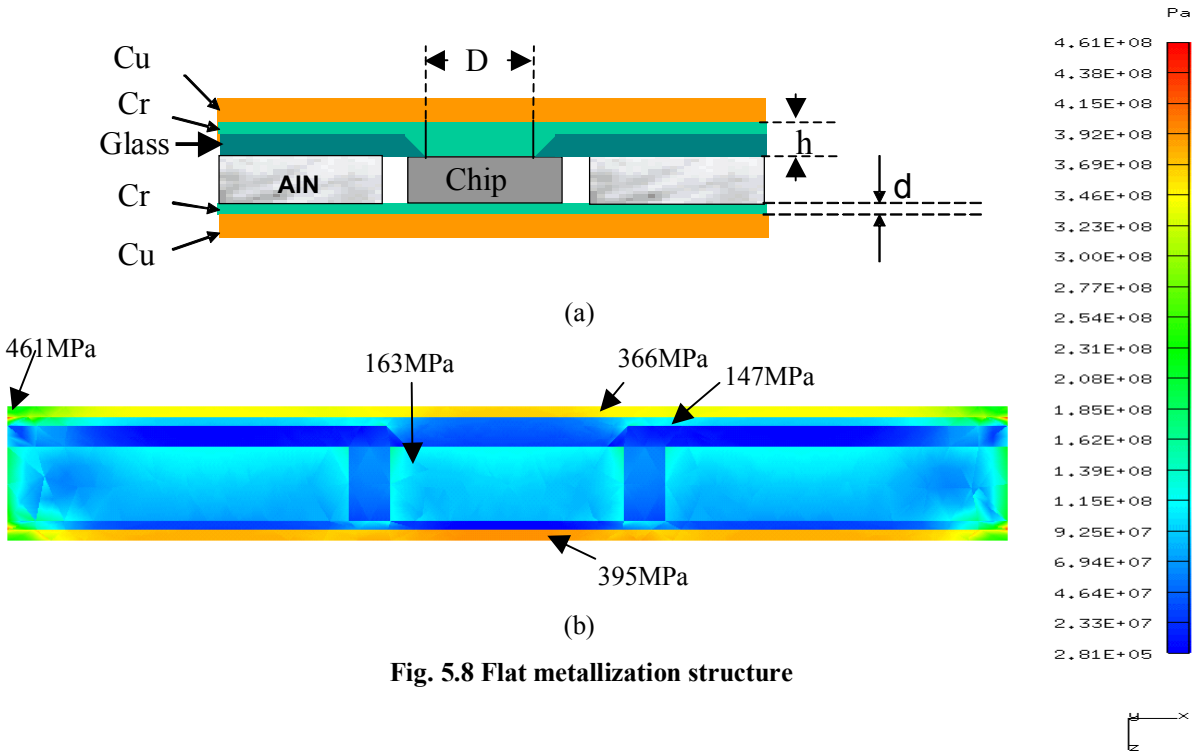


Fig. 5.8 Flat metallization structure

The structure shown in Fig.5.8 is not a fully symmetrical structure, so the mechanical stress at the top half part is slightly higher than the bottom part due to the bending effect. By adding another glass layer at the bottom side of the AlN substrate, a fully symmetrical structure is shown in Fig. 5.9(a). The mechanical stress in the fully symmetrical structure as shown in Fig. 5.9(b) is further reduced, with the maximum chip area mechanical stress 126MPa and the Cr maximum stress above the chip 122MPa.

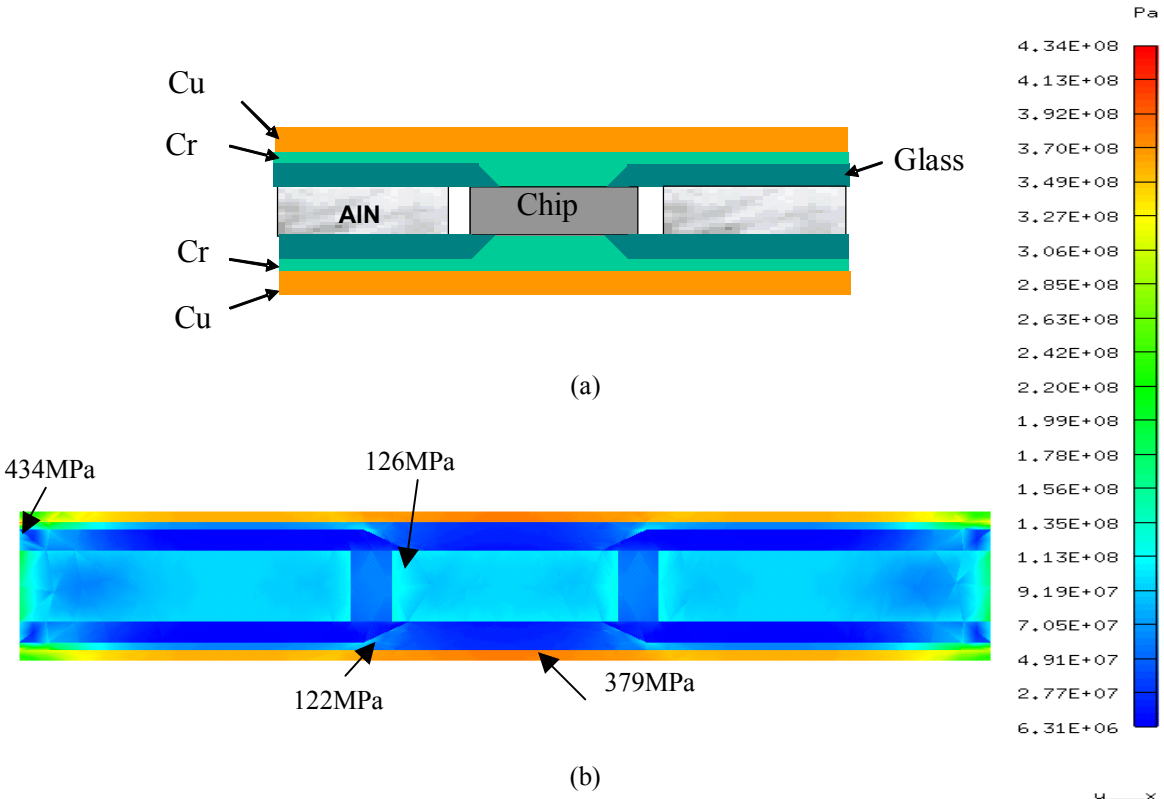


Fig. 5.9 Fully symmetrical structure

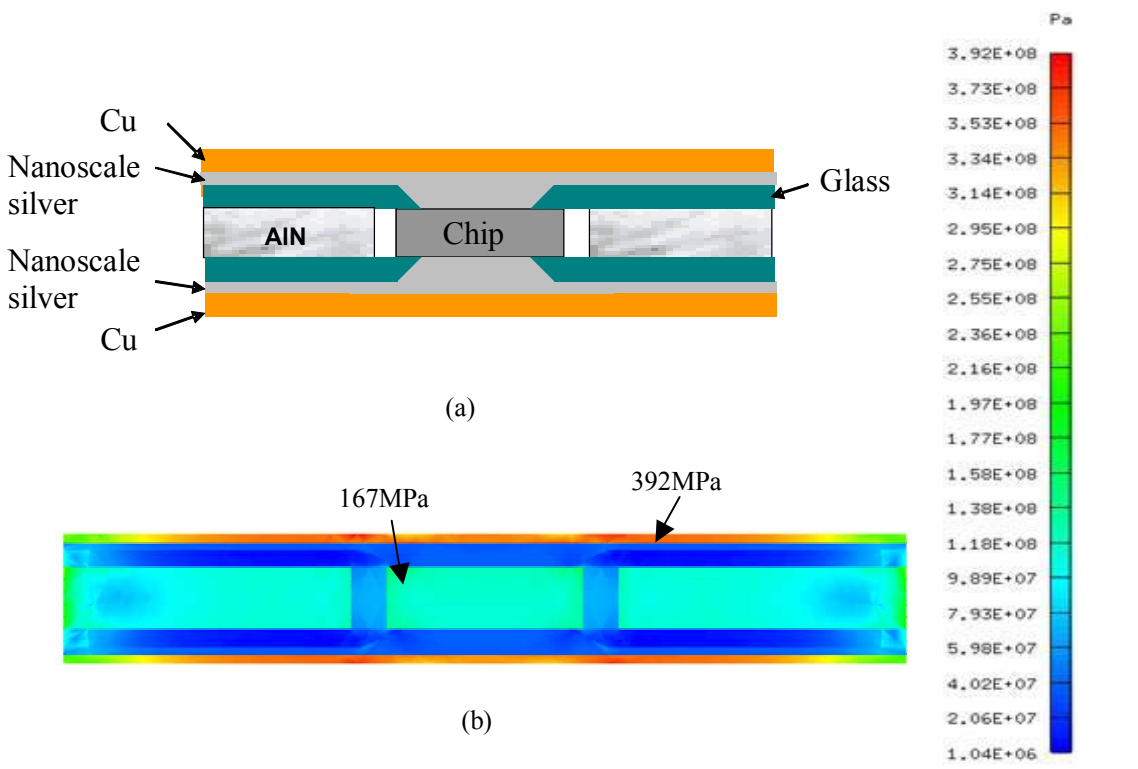


Fig. 5.10 Fully symmetrical structure using nanoscale silver

Since nanoscale silver material is a good candidate for high temperature and its elastic modulus is low at about 10GPa, it can also be used as the buffering layer similar to Cr in the fully symmetrical structure. Fig. 5.10 shows this structure using nanoscale silver to replace the Cr layers as the buffering layers. The chip area maximum stress 167MPa shown in Fig. 5.10(b) is slightly higher than the case of the Cr buffering layer as shown in Fig. 5.9, while the maximum stress 392MPa in the structure is lower than Cr case.

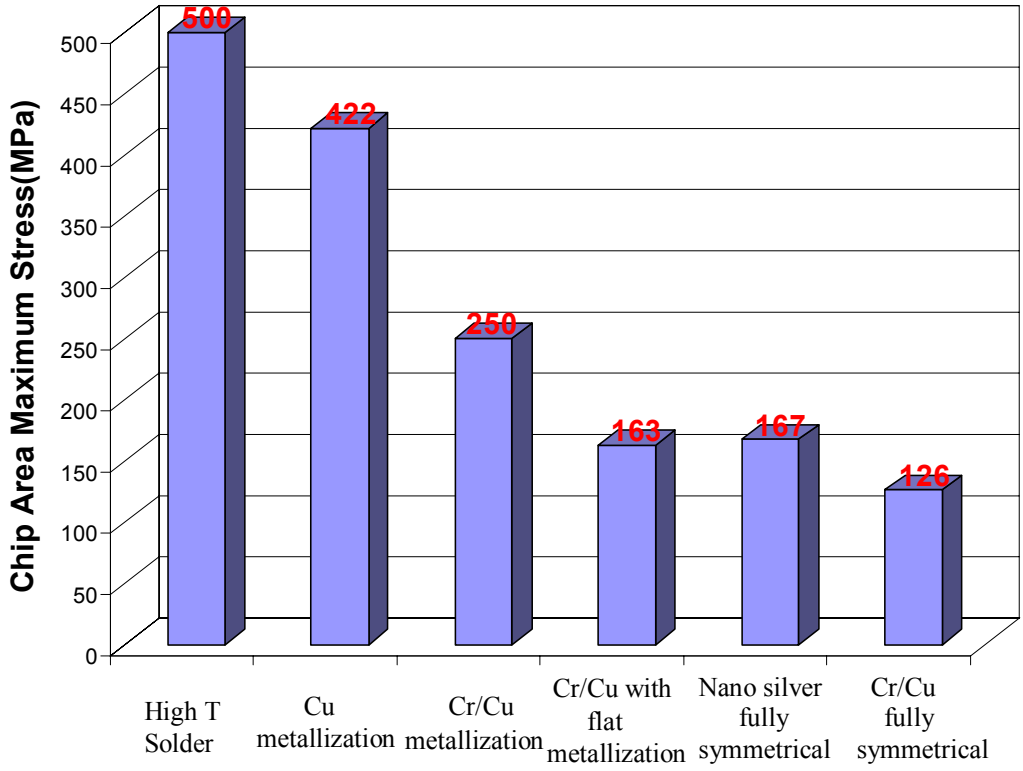


Fig. 5.11 Improvements by using Cr stress buffering layer

By the combined implementation of Cr and Cu metallization layers, the EMC structure is optimized to achieve the minimum mechanical stress. The improvements of the chip area maximum stress are shown in Fig.5.11. When a balanced structure with only Cu metallization is used, the maximum chip area mechanical stress reduced to 422MPa from 500MPa, which is in an unbalanced structure using high temperature solder. While the Cr layer is applied as the stress buffering layer and the Cu layer as the lateral current carrying layer, the chip area maximum stress is further reduced from 250MPa to 163MPa by using flat metallization layers. When a fully symmetrical structure is employed, the stress can be reduced to as low as 126MPa by using the Cr buffering layer and 167MPa

for the nanoscale silver buffering layer. The final improved stress 126MPa is reduced by 74.8% compared to case 1 and this stress is even lower than the Si based module, which works at lower environmental temperature of about 25°C. Therefore, by using the fully symmetrical structure shown in Fig.5.9, the mechanical stress can be appreciably reduced and the module reliability is expected to be highly improved.

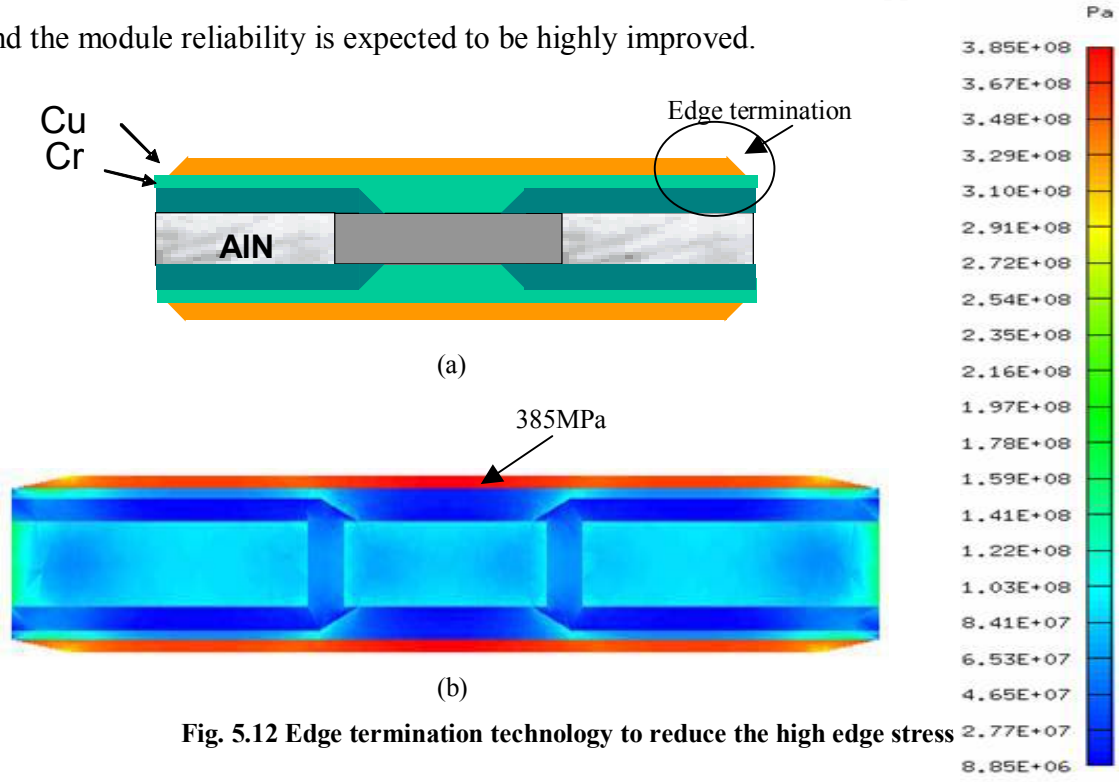


Fig. 5.12 Edge termination technology to reduce the high edge stress

Although the mechanical stress of the chip area has been reduced to an acceptable level, the edges of the interfaces between the Cr and Cu layers still have large mechanical stresses, about 450MPa as shown in Fig.5.9. The high stresses at the edges can be released by using an edge termination technology as shown in Fig.5.11. The copper metallization can be intentionally designed as a thin thickness at edges (shown in Fig. 5.11(a)) instead of a uniform thickness, so the high edge stress can be evenly distributed at edges to avoid stress crowding. Fig. 5.11(b) shows the simulation results using the termination technology. The maximum stress of 385MPa in the cross section occurs in the middle part of the Cu metallization layer instead of at edges. The maximum stress at edges is only 378MPa.

Additionally, the metal-to-metal bonding has a fully different bonding mechanism from the metal-to-SiC bonding. The metal-to-metal bonding is more robust, thus has larger yield strength compared to the metal-to-SiC bonding. [58]

5.4 Summary

The thermo-mechanical model is introduced in this chapter. Six cases of an ECM with different materials and structures are simulated to compare the mechanical stress. The Cu metallization cases show high stresses due to the high CTE of Cu, although the mechanical stress can be reduced by using a structure with the AlN substrate as thick as the SiC chip. Since pure Mo can not be implemented to the ECM structure using the electroplating process, a low CTE metallization such as Cr is employed as the stress buffering layer for high temperature applications, since this metal can be electroplated. To achieve a low stress, the Cr layer is optimized by changing its thickness and angle, although the maximum chip area stress is still relatively high at 250MPa. To further reduce the high stress occurring in the chip area, a fully balanced structure with identical flat metallization layers on top and bottom is applied to the EMC structure. The chip area maximum stress is finally reduced to 126MPa, which is even lower than the Si based module, which works at a lower environmental temperature of 25^{o}C. By calculations, the additional electrical resistance caused by one side Cr layer is only 24.27uΩ, so the Cr buffering layer doesn't introduce a high electrical resistance to the EMC module. Although the high stresses at the edges are a concern, the edge termination technology can be applied to release the edge stress. Additionally, the edges have a strong metal-to-metal bonding at the interface between Cr and Cu layers, thus can tolerate the high stress. These thermal-mechanical analyses will provide a reference for further improvements in the ECM.

Chapter 6

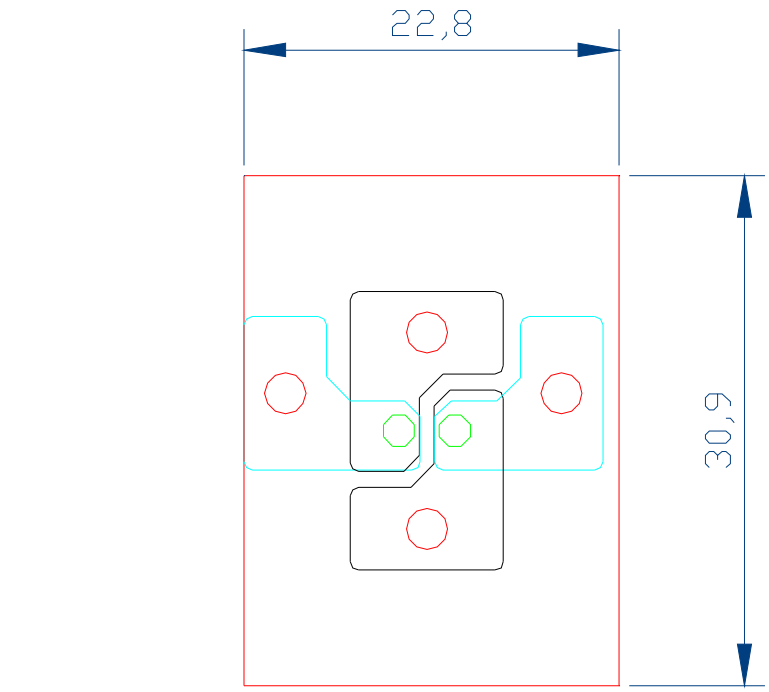
Design and implementation of a High Temperature Embedded Chip Module (ECM)

6.1 Introduction

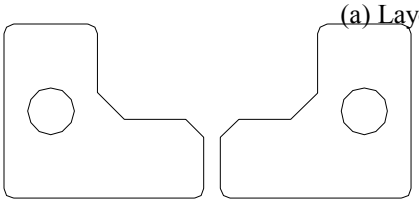
After the component selection, thermal and thermo-mechanical analysis, the structure of the high temperate embedded chip module is determined. To fabricate the high temperature module, eight steps are required in the manufacturing process, including layout design, laser cutting process, screen printing process, sputtering process, photo masking process, electrical plating process, etching process and final cutting and assembling process.

6.2 Layout design

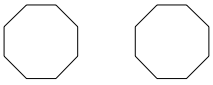
The layout design is used to organize the whole process and prepare the different layers of the embedded chip module for further fabrication process. The detailed size information for the different layers is required and careful consideration from the system level is necessary in the layout design process. Fig. 6.1 shows the embedded chip module layout design. This module is fabricated on a piece of AlN substrate with 2 x 2 inches shown in (a), and all layers including top metallization layer (b), chip layer (c), bottom metallization layers (d), and cutting layer (e), are associated in (a) with different colors. The four cutting holes in (e) are designed for I/O pins using screw connections.



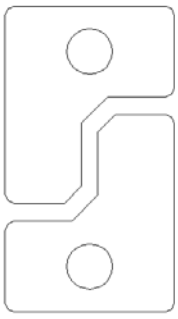
(a) Layout design



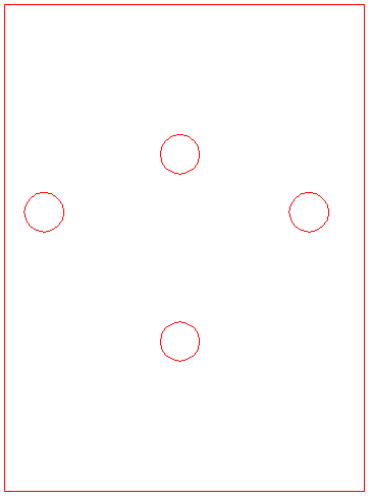
(b) Top copper layer



(c) Chip layer



(d) Bottom copper layer



(e) Cutting layer

Fig. 6.1 Layout design

6.3 Laser cutting process

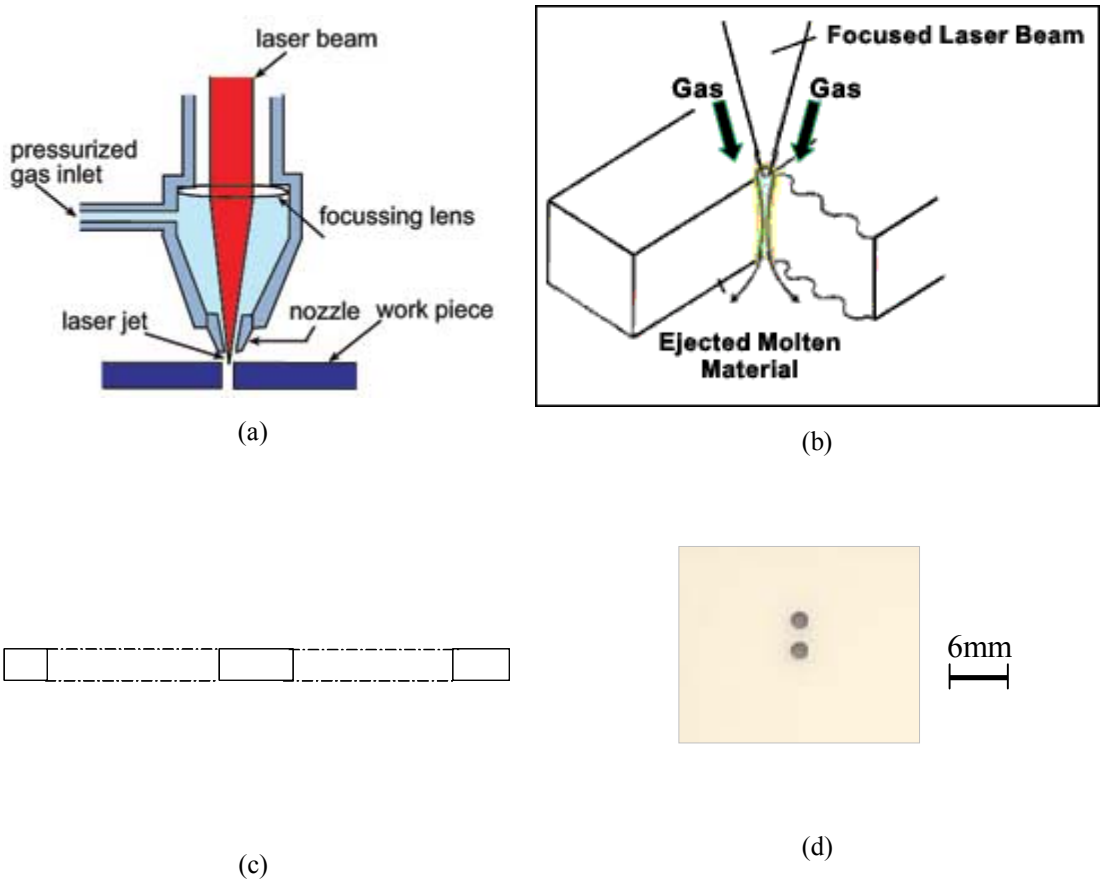


Fig. 6.2 Laser cutting process

Laser cutting is a mostly thermal process in which a focused laser beam is used to melt material in a localized area. As shown in Fig. 6.2(a), during the laser cutting process, a beam of high-density light energy is focused through a tiny hole in the nozzle. When this beam strikes the surface of the work piece, the material of the work piece is immediately cut. A co-axial gas jet is then used to eject the molten material from the cut and leave a clean edge as shown in Fig. 6.2(b). Laser cutting machines can accurately produce complex exterior contours and can be complementary to the CNC/Turret process. Laser cutting takes direct input in the form of electronic data from a CAD drawing to produce flat form parts of great complexity. With a 3-axis control, the laser cutting process can profile parts after they have been formed on the CNC/Turret process. Lasers work best on materials such as carbon steel or stainless steels. Metals such as

aluminum and copper alloys are more difficult to cut due to their ability to reflect the light, as well as absorb and conduct heat. The advantages of laser cutting are: [59]

- High quality cut - no finishing
- Flexibility - simple or complex parts
- Non contact - no marks
- Quick set up - small batches
- Low heat input - low distortion
- Virtually any material can be cut

In the fabrication process, the laser cutting is employed to cut the AlN substrate with the profile shown in the Fig. 6.1(c) and (e).

6.4 Adhesive Sealing and Screen printing process

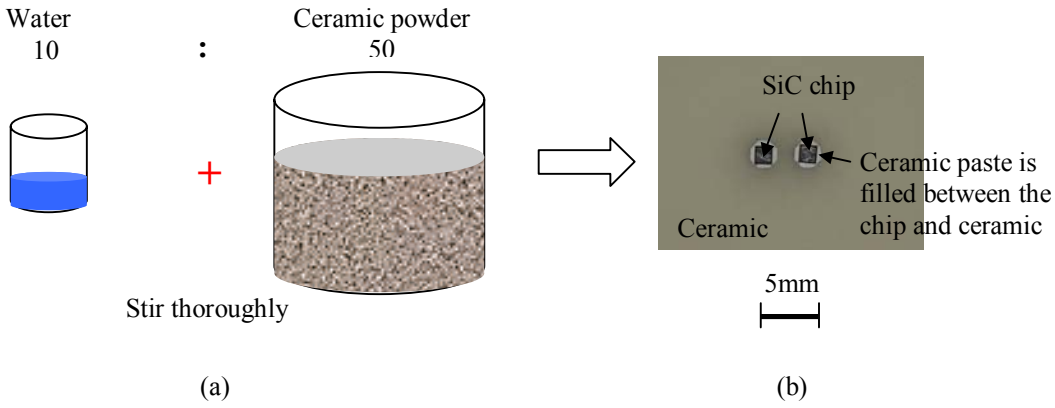
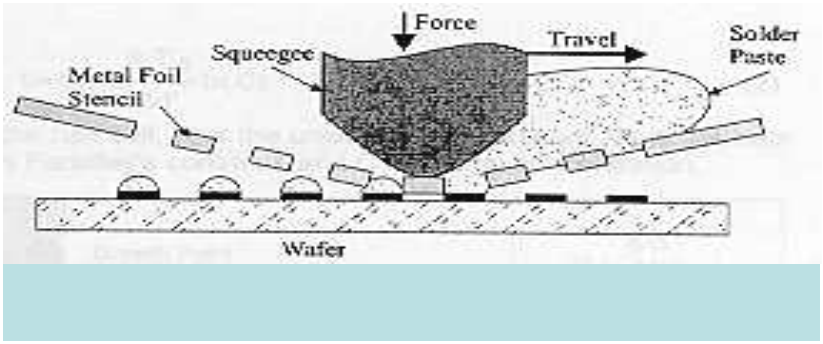
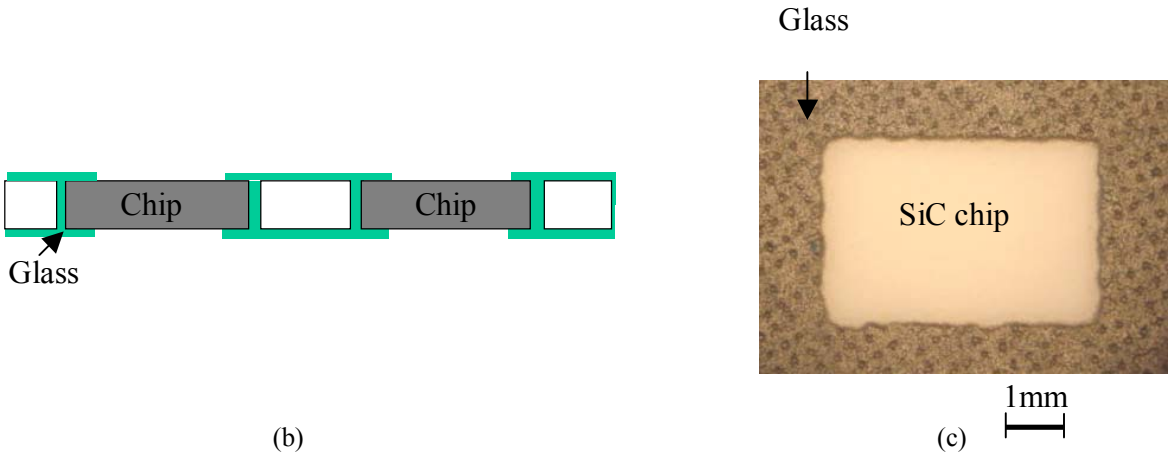


Fig. 6.3 Preparation of Resbond material

Rebond material is applied as the adhesive sealing material to fix the chip in the ceramic carrier. As shown in Fig.6.3 (a), the resbond ceramic paste is prepared by mixing 10g water and 50g adhesive powders. Then the prepared paste is carefully filled in the gap between the chip and ceramic using a needle, as shown in Fig. 6.3(b). The fixed SiC chips with the ceramic are put in the oven for curing. The curing process may take up to 24 hours at room temperature; however, curing can be accelerated by keeping at 65^{o}C for 4 hours.



(a)



(b) (c)

Fig. 6.4 Screen-printing process

The detailed screen-printing process is shown in Fig. 6.4. The equivalent of the printing plate for the screen printer is the SCREEN - a wooden or aluminum frame with a fine nylon MESH stretched over it as shown in Fig. 6.4(a). The screen is fitted on the press and is hinged so it can be raised and lowered. The substrate to be printed is placed in position under the screen and glass paste is placed on the topside of the screen. A rubber blade gripped in a wooden or metal handle called a SQUEEGEE is pulled across the top of the screen; it pushes the glass paste through the mesh onto the surface of the substrate. To repeat the process the squeegee floods the screen again with a return stroke before printing the next impression. [60] The glass screen-plating layers are implemented to both sides of the substrate to achieve a symmetrical structure. Then the glass layer is put in the oven for glass firing, which follows the firing profile shown in Fig. 3.4. Fig. 6.4(c) shows the glass layer after firing.

6.5 Sputtering process

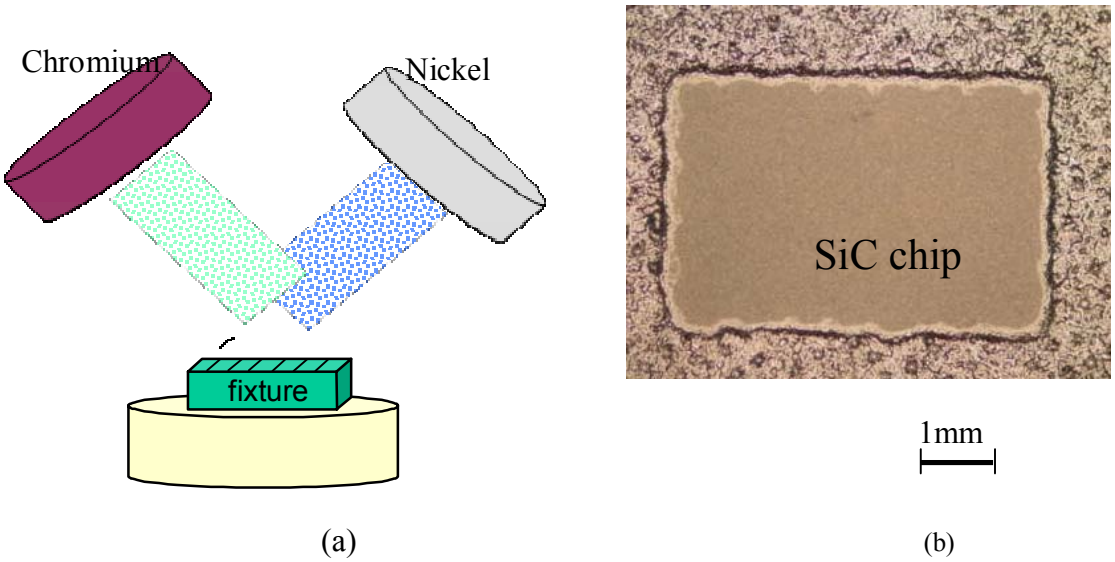


Fig. 6.5 Sputtering process

Sputtering is a momentum transfer process in which atoms from a cathode/target are driven off or sputtered by bombarding ions. In this process the momentum of bombarding ions is more important than their energy. For example, a hydrogen or helium ion accelerated to 3,000eV will cause very little sputtering compared to an ion of argon (which is chemically inert) with the same 3,000eV energy. This is simply because the lighter hydrogen or helium ion has much less momentum. Sputtered atoms travel until they strike a substrate, where they deposit to form the desired layer. As individual atoms they are chemically active and readily form compounds with the ions and atoms of the bombarding gas. For this reason inert argon is used as the bombarding gas. When argon ions strike the target their electrical charge is neutralized and they return to the process as atoms. If the target is an insulator, the neutralization process results in a positive charge on the target surface. This charge may reach the level where bombarding ions are repelled and the sputtering process stops. To continue the process the polarity must be reversed to attract enough electrons from the discharge to eliminate surface charge. This periodic reversal of polarity is done automatically by applying RF voltage onto the target assembly (hence the term RF sputtering). [61]

To achieve a seed layer for the Cr electroplating process, a Cr layer is sputtered to the substrate surface. This is a long process for about 2-3 hours since Cr is a very hard material. However, this process can be reduced by sputtering a Ni layer for 30 minutes following a Cr sputtering for 20 minutes.

6.6 Photo masking process

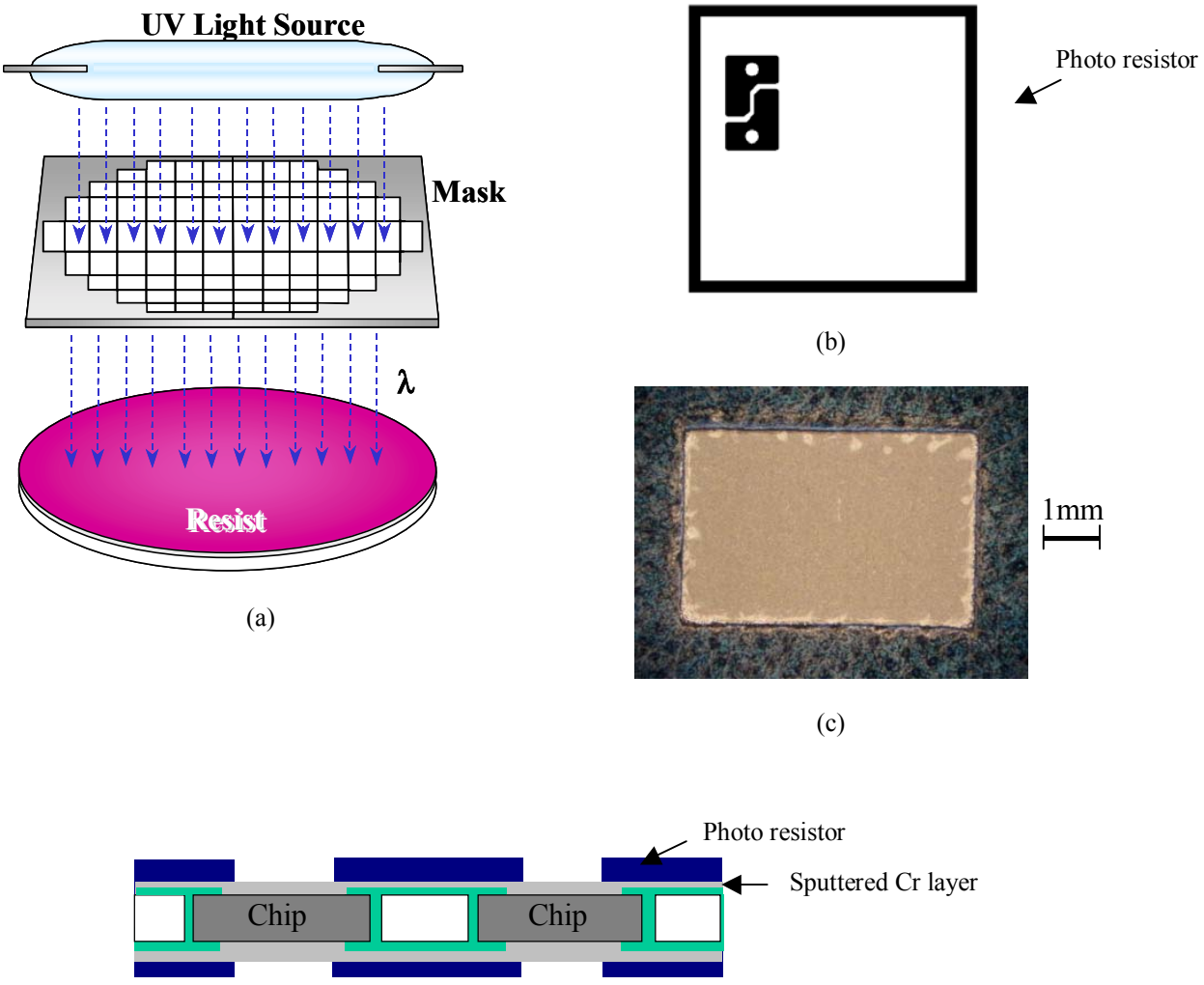
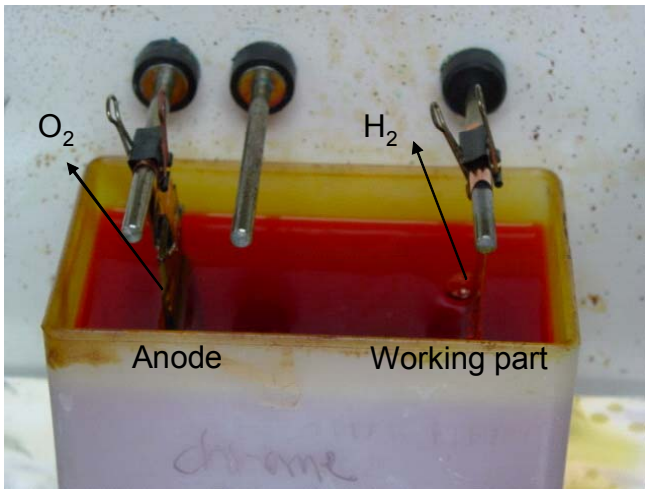


Fig. 6.6 Glass firing temperature profile

Photo masking is used to protect one area of the sputtering layer while working on another. The photo-resistor film is applied to the sputtering layer, giving it characteristics similar to a piece of photographic paper. A photo aligner aligns the substrate to a mask and then projects an intense light through the mask, exposing the photo-resistor with the mask pattern as shown in Fig. 6.6(a). Then the exposed sample is placed into the developer solution and the soluble areas of the photo-resistor are dissolved by developer chemical. Fig. 6.6 (b) show the top side mask, while (c) presents that the photo-resistor covers on the sputtering layer with other areas open for electroplating. [62]

6.7 Electroplating process for Cr

(a) Lead anode

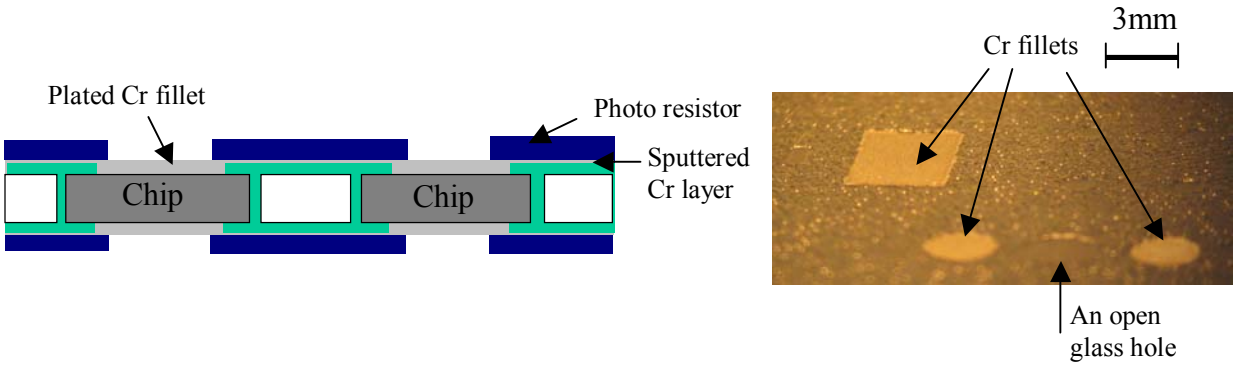


(b) Hard chrome plating setup

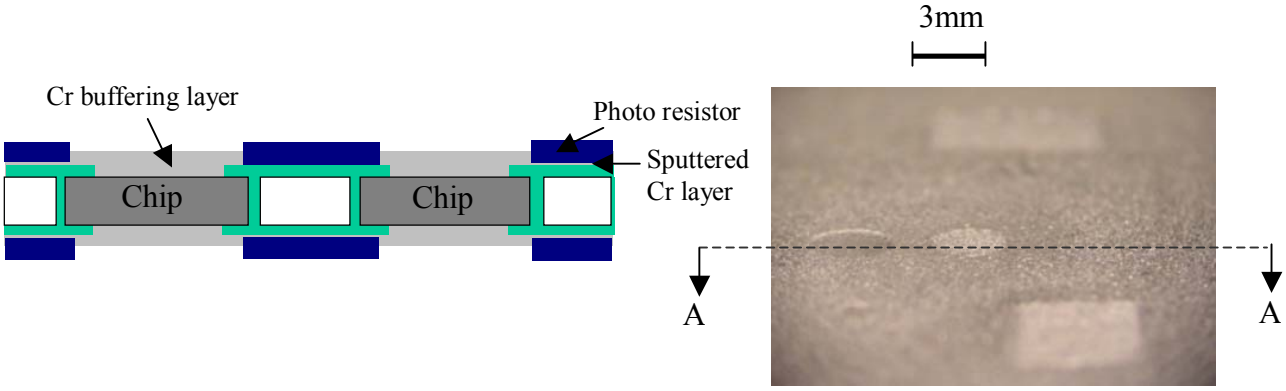
Fig. 6.7 Hard chrome plating

Two types of chrome plating processes are available: decorative chrome plating and hard chrome plating. Since the requirement for Cr thickness in the high temperature EMC is more than 50um, hard chrome plating process is employed in the module fabrication. To make the electroplating solution, we add 16 fl. Oz of distilled water to the tank, 1 kg of chromium crystals (CrO_3) to the water and 10 milliliters of sulfuric acid (98%). The plating solution is sensitive for the concentration of the sulfuric acid. [63] A lead anode as shown in Fig. 6.7(a) is employed and the toxic mist containing chromium acid may form during the plating process as shown in Fig. 6.7(b). So it is essential to do the chromium electroplating process in a fume hood. The plating current is much higher than other plating process, such as Cu plating and Ni plating. The normal plating current density is about 300mA/cm^2 and 25um thickness can be obtained using this current density about one hour.

To realize a flat metallization structure as simulated and shown in Fig. 5.9, the Cr fillets need to be filled in the open glass holes on the chip topside. As shown in Fig. 6.8(a), the Cr fillets have to be electroplated to the same thickness as the glass layer before the Cr buffering layer can be applied. The picture in Fig. 6.8(a) shows how three Cr fillets are formed in the glass holes. To identify the difference after the plating, a glass hole is left open in the picture. After the Cr fillets are formed in the open glass holes, a new photo resist layer needs to be developed with the designed pattern for the metallization layer. Fig. 6.8(b) shows the cross-sectional view with the Cr buffering layer. The picture showed in Fig. 6.8(b) indicates the flat surface in the structure. Therefore, it is necessary to have a two-step Cr electroplating process to form the flat metallization layers.



(a) First step to form Cr fillets



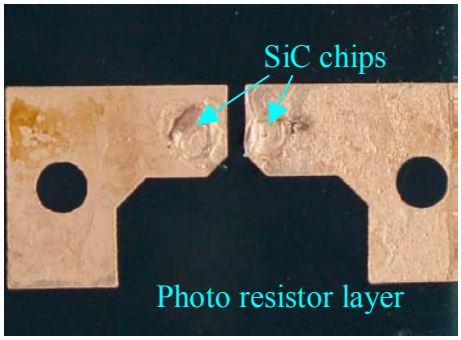
(b) Second step to form the Cr buffering layer

Fig. 6.8 Two-step Cr plating process

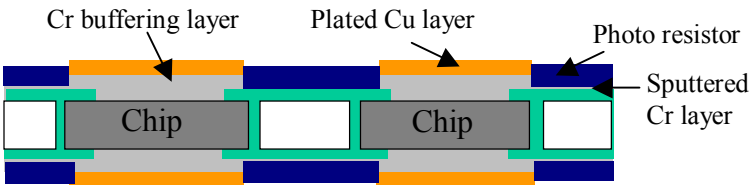
6.8 Electroplating process for Cu

The Cu electrical plating process is to increase the thickness of the designed metallization layer for carrying currents laterally in the structure. The sample to be coated is placed into a container containing a copper plating solution and the sample is connected to an electrical circuit, forming the cathode of the circuit. [64] When an electrical current is passed through the circuit, metal ions in the solution are attracted to the sample. The result is an evenly-coated layer of metal around the item. The Cu anode is always used in the Cu plating process. The normal current density is about 20mA/cm^2 and 25um can be obtained using this density after one hour. Fig. 6.9(b) shows the Cu is plated on the designed open areas, which are not covered by a photo resist layer. Fig. 6.9 (c) presents the desired cross-sectional view after the Cu electroplating process.

(a)

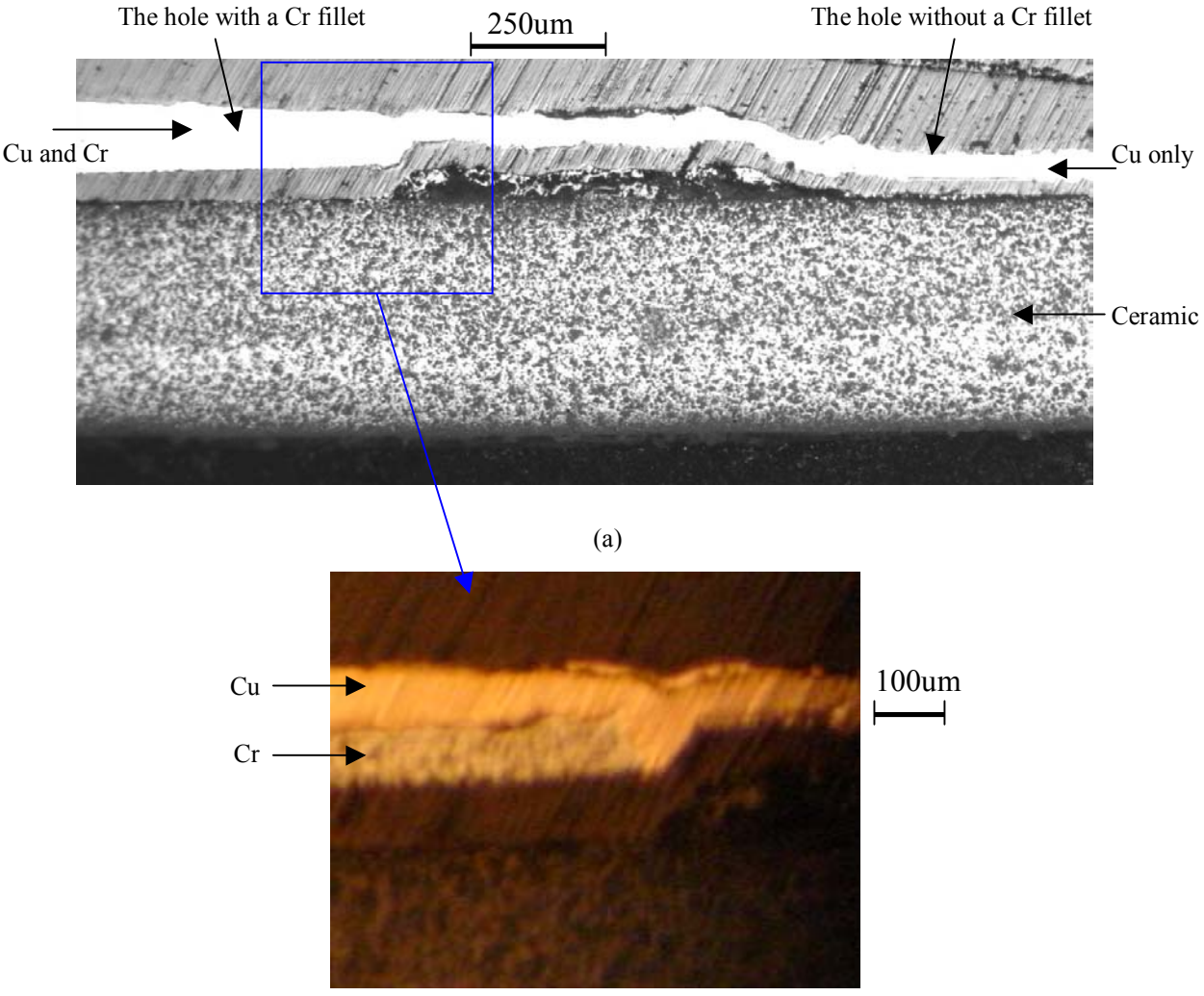


(b)



(c)

Fig. 6.9 Cu electrical plating



(a)

(b)

Fig. 6.10 Cross-sectional view of the sample

To demonstrate the flat metallization layers in the structure, we cut the sample following a line across two glass holes, one is filled with a Cr fillet and another has no Cr

fillet as shown in the picture of Fig.6.8 at section A-A. The cross sectional view of two glass holes is shown in Fig. 6.10. As shown in Fig. 6.10(a), the flat metallization is achieved in the hole with a Cr fillet, while the metallization layer is uneven in the hole without the Cr fillet. The zoom-in cross-sectional view in Fig. 6.10(b) clearly shows the Cr fillet, which is under the Cu metallization layer.

6.9 Etching process

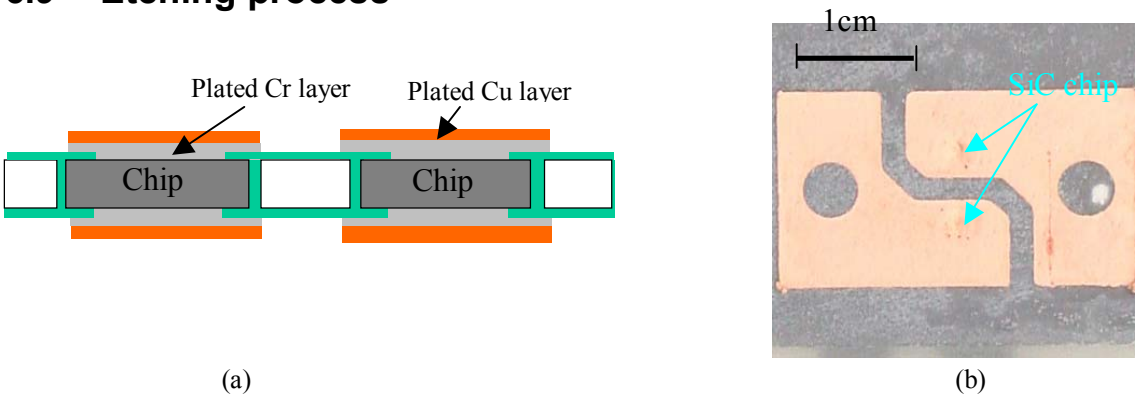
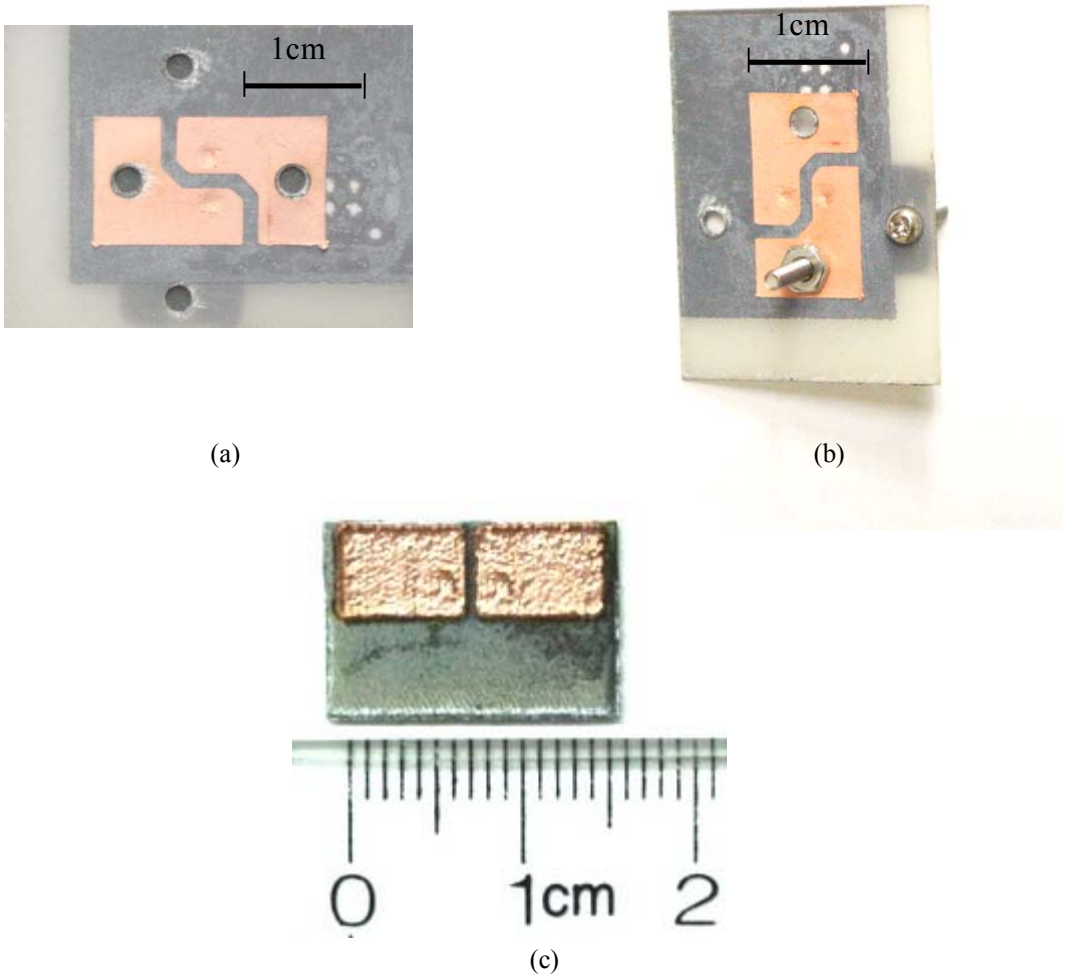


Fig. 6.11 Etching process

The etching process is designed to remove the excess sputtering layer and develop the final metallization pattern for both sides of the module. The copper etching solution is used to remove the sputtered copper layer and the chromium etching solution removes the sputtered chromium layer. Since it is a micro-etching process, the electrical-plated chromium and copper layers are too thick to be etched while the excess sputtering layer is removed. Fig. 6.11(b) shows the designed pattern is kept while the unnecessary sputtering layers are removed.

6.10 Final cutting and assembling process

In this final step, the whole substrate will be cut to the designed pattern for the final assembling process. Laser cutting is employed again in this step and the final sample after cutting sample is presented in Fig. 6.12(a). The four holes in the profile are designed for I/O pins using screw connections as shown in Fig. 6.12(b).



(a) (b)

(c)

Fig. 6.12 Final cutting and assembling process

In total, two kinds of modules were manufactured for testing, i.e.

- a module with SiC diode and only Cu electroplated metallization as shown in Fig. 6.12(a) and (b);
- a module with a buffering layer of Cr and Cu for lateral current conductor as shown in Fig. 6.12 (c).

6.11 Summary

The fabrication process of the high temperature ECM is covered. Two SiC diodes are packaged in one module. The new glass material is successfully applied as a screen-printing material and resbond material is used as the sealing material. The Cr buffering layer is implemented through a hard chrome plating process and a flat Cr metallization layer is formed through a two-step Cr plating process. The double-sided metallization layers are realized with the sputtering process followed by the electrical plating process for both sides. Pressure contact connection using screws is employed for I/O connections. The high temperature ECM is ready for experimental evaluations.

Chapter 7

Experimental Evaluation

7.1 Introduction

After the design and implementation of a high temperature embedded chip module, the experimental evaluations for the high temperature module, including electrical and thermal tests, will be introduced in this chapter. The electrical test shows the forward and reverse characteristics of a high temperature ECM, in order to demonstrate its proper device functionality at high temperature. The leakage currents of the module at high temperature are studied as well. The thermal test, including steady-state and transient measurements, is conducted to evaluate the thermal performance of a high temperature module. The stead-state thermal measurement is employed to show its capability to reduce the cooling system. To optimize the thermal design of the module structure, the transient thermal parameter analysis method is proposed, which is based on a temperature cooling-down curve measurement. The transient analysis process is described in this chapter to obtain the thermal parameters of a high temperature EMC. Ultimately, the electrical and thermal tests provide a comprehensive overview for the characteristics of a high temperature ECM and offer a useful reference for further improvements.

7.2 Electrical test

7.2.1 Experimental setup

The high temperature embedded chip module was packaged with two 1.4 X 1.4 mm^2 silicon carbide Schottky diodes (SIDC02D60SIC2). For the high temperature applications, two screws were employed as I/O pins, which were connected through two clips for measurement. A schematic of the experimental setup is shown in Fig. 7.1(a). The ECM was put into a heating chamber, and in order to test the module in a thermal equilibrium environment, a thermocouple was attached to the module to measure the chamber temperature. The module was measured with only one voltage pulse of 200us to avoid too much power input. Here, one pulse means that the power curve tracer only generates one

voltage pulse to measure the forward voltage drop through the die when the whole device is in thermal equilibrium. This is important in this experiment because any large amount power input will change the thermal environment equilibrium. [65]

This low power level can also be proved by calculations of the temperature increase under the maximum current 6A. As the device is measured using a single pulse, which is only 200us, the temperature increase of the chip is calculated as follows, assuming that the whole input energy is used to heat up the die region:

$$q = -c \cdot \rho \cdot V \cdot \frac{dT}{d\tau}, \tag{7.1}$$

$$\text{Temperature increase } \Delta T = \frac{1}{c \cdot \rho \cdot V} \int_0^t q d\tau = 2.065^{\circ} C$$

where density (kg/m^3) ρ is 3100, pulse period T is 2E-4, specific heat capacity (J/kg.K) c is 750, chip volume (m^3) V is 8.33E-10, input power (W) q is 20, sensing current (A) I is 6.

Since the maximum temperature increase is only 2.065°C using a single pulse, it is proved that the one-pulse heat input is relatively low and doesn't greatly change the thermal environment equilibrium.

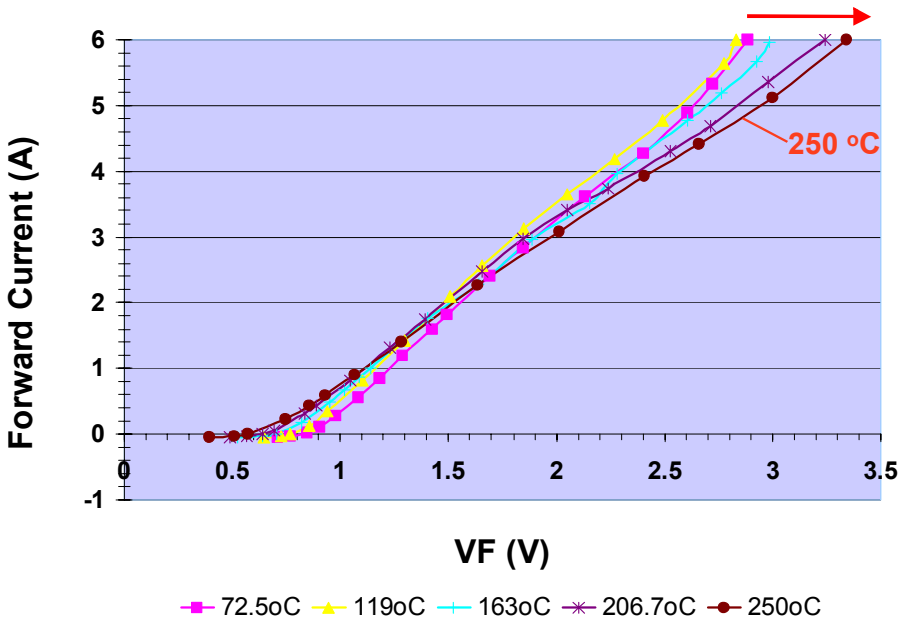
Fig. 7.1 Experimental setup

7.2.2 Forward characteristics

During the experiment, the device is unheated except for the heat generated by the sensing current, which is generally insignificant. When the component is in a constant-temperature environment, any point on the component case will eventually reach the same temperature as the component junction, assuming the heat generated by the sensing current is very small. Under these conditions, the component is said to be in a thermal equilibrium with its surrounding environment. Measurement of the forward voltage and the associated chamber temperature comprises one data point for construction of the forward characteristics.

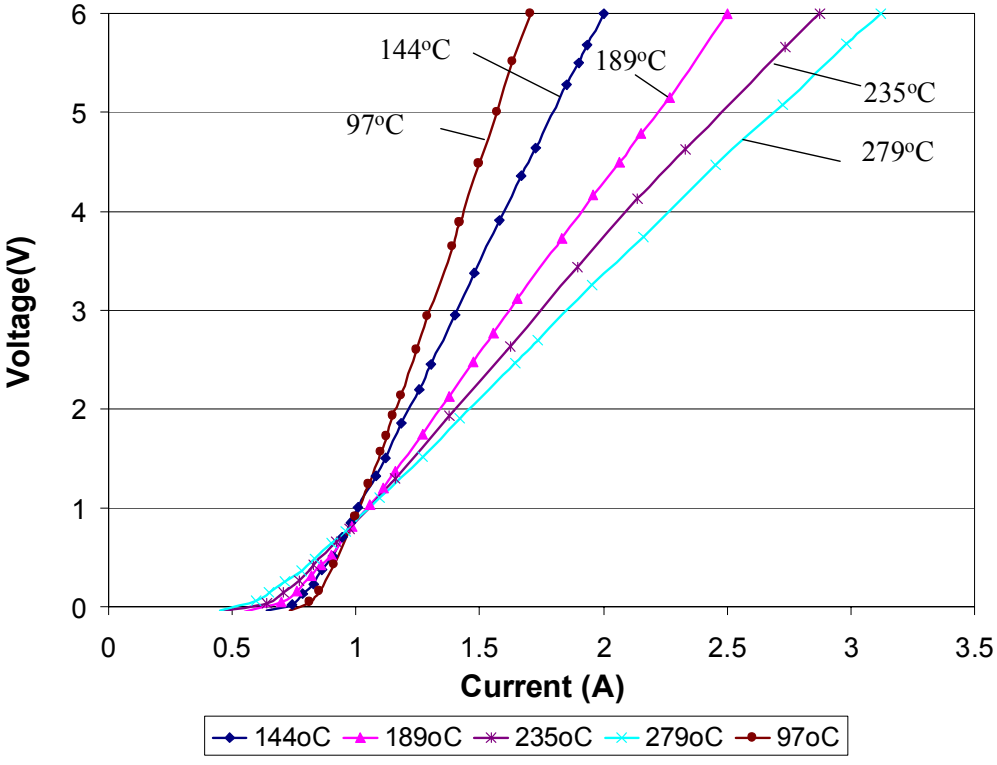
In the forward testing, the connection from the DBC board to the power curve tracer uses four-wire technology, which means the voltage difference across the temperature-sensing junction should not include the voltage drops across the wires that carry the sense current to the sense junction. This method minimizes the voltage drop measurement error and improves the experimental accuracy. The whole device is heated in the chamber so that a thermal equilibrium is attained, and a thermocouple is placed on the bottom of the module to measure the case temperature.

The forward characteristics of two high temperature ECMs, which are specified in Fig. 6.12, are shown in Fig. 7.2. The curves represent the typical forward characteristics from room temperature up to 279^{o}C. Fig. 7.2(a) shows the forward characteristics of a high temperature ECM using only Cu metallization layers. The forward voltage drop decreases as the temperature increases below the current of about 2.5A, while the forward voltage drop increases as the temperature increases. The characteristics of the positive temperature coefficient at the high current more than 2.5A. Fig. 7.2(b) presents the updated forward characteristics with Cr and Cu combined metallization layers. The positive temperature coefficient can be observed at currents more than 1A. The forward voltages in (b) are much smaller than (a), thus the EMC using the Cr and Cu combined metallization layers shows a better forward conduction performance.



The module has been tested up to 250 °C

(a) ECM with only Cu metallization layers



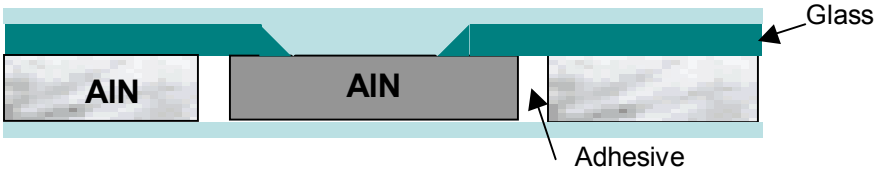
(b) ECM with Cr and Cu combined metallization layers

Fig. 7.2 Forward characteristics

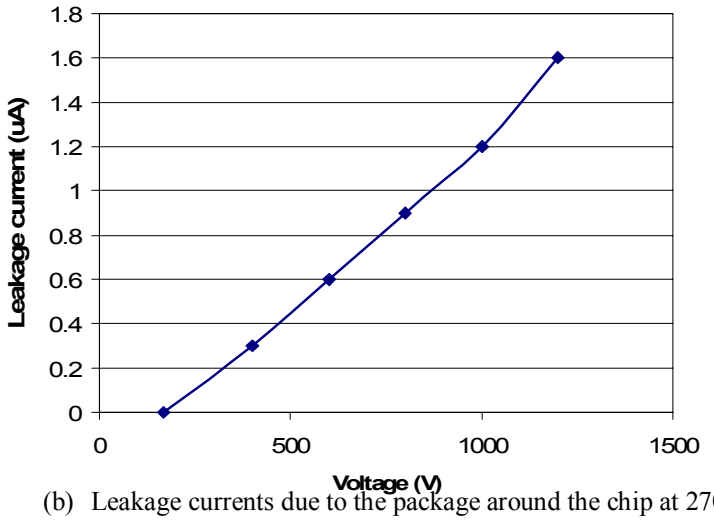
In the test of the high temperature ECM only using Cu metallization layers, we found that the forward voltage became larger after only several power cycles at the same environmental temperature. This indicates that the delamination becomes larger at the interface between the chip and Cu metallization. Finally, after the module was cooled down from 250^{o}C to room temperature, the module could not be tested functionally, which indicated a module failure. All these tests show that the Cu metallization is not suitable for attaching to the chip surface directly, since high stress occurs at the interface between the chip and Cu metallization. Due to the delamination, the curves in Fig. 7.2(a) don't show an apparent positive temperature coefficient at high currents, since an additional large voltage is dropped on the interface between the chip and metallization layer. However, for a high temperature ECM using the combined Cr and Cu metallization layers, the curves in Fig. 7.2(b) show lower forward voltages and the positive temperature coefficient can be observed at a lower current. These improvements are due to the good adhesion between the Cr metal and chip at high temperature, since the low thermally induced stress occurs in the chip area by using the Cr buffering layer.

7.2.3 Reverse characteristics

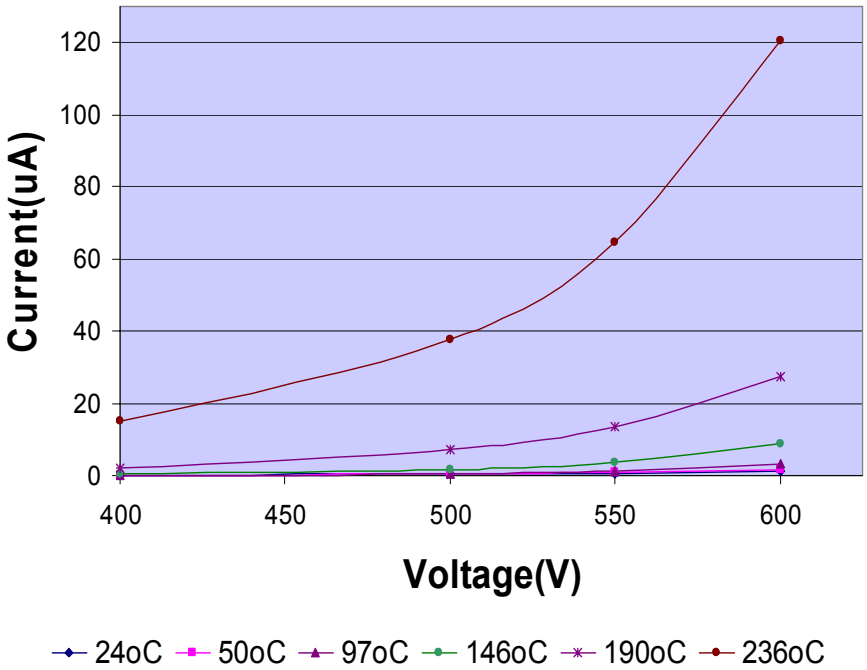
Both high temperature ECMs, which are shown in Fig. 6.12, presents similar reverse characteristics given in Fig. 7.3(c). The six curves represent the reverse characteristics from room temperature to 236^{o}C. The reverse leakage current increases as the temperature increases. As the temperature exceeds 200^{o}C, the leakage current increases dramatically. This leakage current in Fig. 7.3(c) may come from three sources: the package around the chip, the passivation layer and the Schottky junction. To study the leakage current due to the package, we used a chip-sized AlN substrate in a structure shown as in Fig. 7.3(a) to replace the SiC chip in the ECM structure. So the leakage current measured from this structure is chiefly from the leakage of the glass and the resbond material. This reverse measurement for this structure was done at 270^{o}C using the same setup shown in Fig. 7.1. Fig. 7.3(b) shows that the package leakage current is measured up to 1.6uA with the forward voltage high up to1200V. Since the measured leakage current is extremely small below 0.6uA at 600V, the leakage current at high temperature due to the package around chip can be neglected



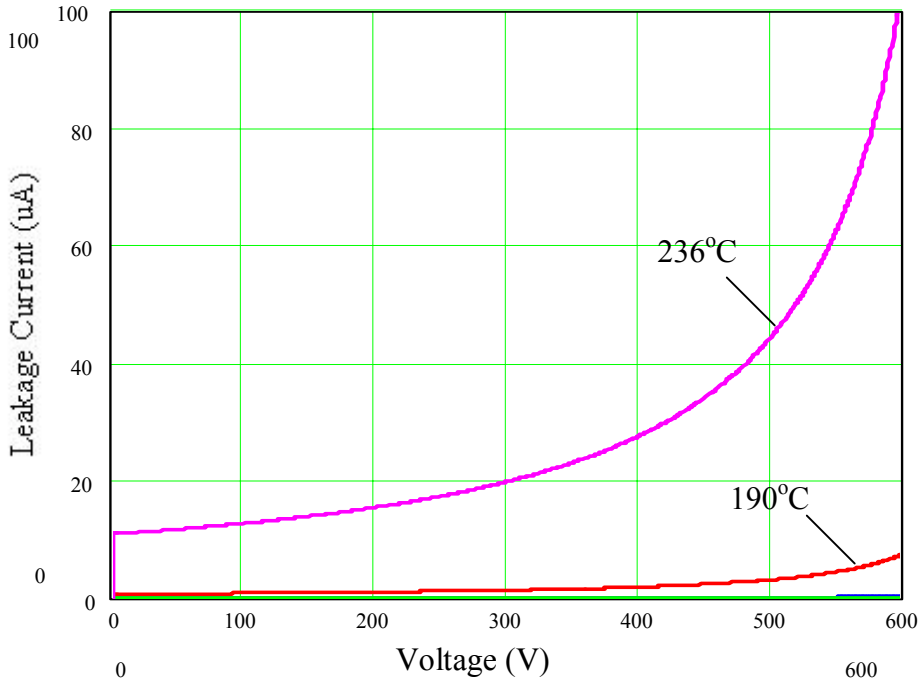
(a) A structure to measure the package leakage current



(b) Leakage currents due to the package around the chip at 270°C



(c) Measured reverse characteristics of a high temperature ECM



(d) Theoretical reverse characteristics of the Schottky junction

Fig. 7.3 Reverse characteristics study

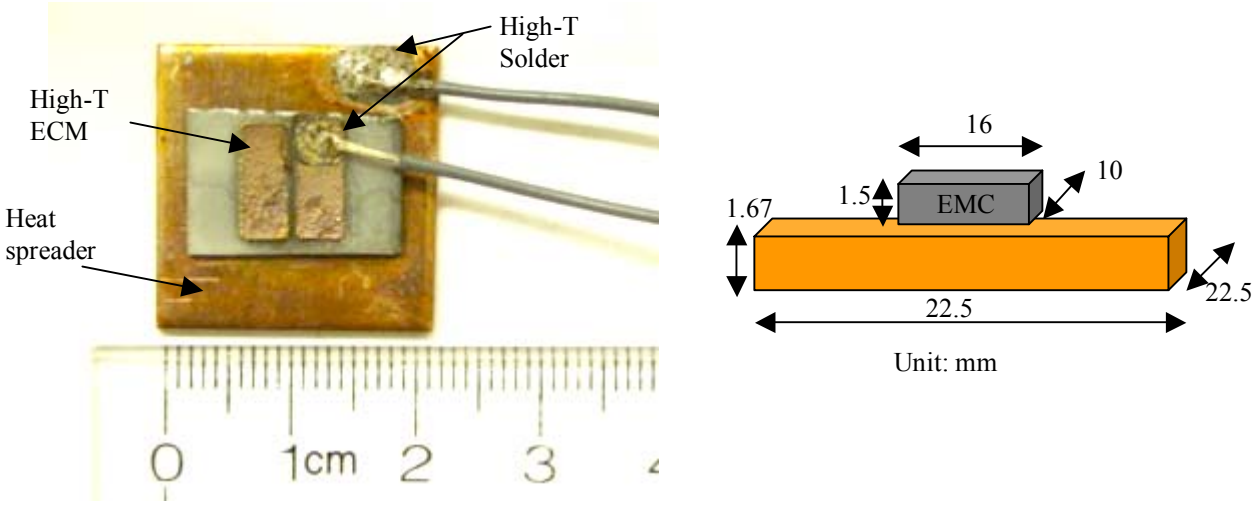
The theoretical reverse characteristics of the Schottky junction have been discussed in 4.3. So if the cross-sectional area of the SiC Schottky junction we used is 1x1mm^2, the theoretical leakage currents of the SiC Schottky junction can be obtained at different temperatures as shown of Fig. 7.3(d). Since the detailed parameters of the SiC diode are still unknown due to the confidential policy of the chip manufacturer, Fig. 7.3(d) can only show the trends of the reverse characteristics of the SiC Schottky diode we used. From the comparison with the measured leakage currents in Fig. 7.3(c), the trends of the theoretical curves are in good agreement with the measured curves, while the theoretical leakage currents are still smaller than the measured curves of the high temperature ECM. This leakage current difference may be caused by the passivation layer, which can decompose at high temperature, thus the passivation leakage current may become large at high temperature. The photo-imide material is used as the passivation layer in the SiC chip under test.[28]

7.2.4 Summary

The electrical test presents the forward and reverse characteristics of the high temperature module. The forward and reverse characteristics of the ECM are presented up to 270^{o}C indicating proper device functionality. The ECM using the Cr and Cu combined metallization layers shows a better conduction performance compared to the ECM using only Cu metallization layers. The study on the reverse characteristics of the ECM indicates that the large leakage current at high temperature is not due to the package around the chip, but chiefly caused by the Schottky junction and the chip passivation layer.

7.3 Steady State Thermal Measurement

Since the high temperature embedded chip module can reduce the bulky cooling system and improve the power density in normal temperature environments, the steady state thermal measurement is designed to demonstrate these capabilities. Fig. 7.4 shows the measurement set up with a high temperature EMC using the proposed simple cooling system, which is only a copper heat spreader.



(a) (b)

Fig. 7.4 Steady-state thermal measurement setup

It is a similar setup to Fig.4.7. As shown in Fig. 7.4(a), the high temperature EMC packaged with two SiC Schottky diodes was attached to a small piece of heat spreader

with the size of 22.5x22.5x1.67mm using a high temperature solder (Sn10Pb88Ag2). Two thin wires were employed as the electrical connections and attached to the pads using the high temperature solder as well. A thermocouple was attached at the bottom side of the heat spreader to monitor the case temperature. The detailed package size information is presented in Fig. 7.4(b) as the EMC and heat spreader are considered in the package profile.

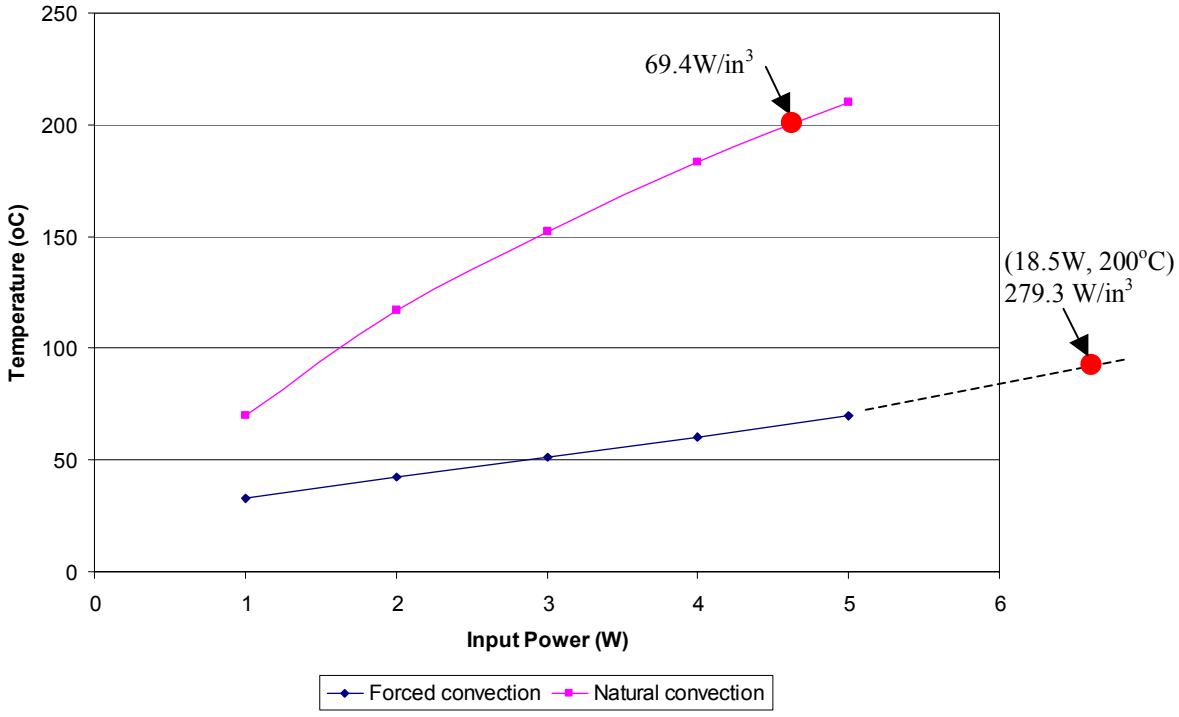


Fig. 7.5 Case temperature with natural and forced convections

The ECM was heated up with the constant voltages and currents to a steady state, while the case temperature was recorded at each steady state. Fig.7.5 shows the relationship between the input power and case temperature under natural and forced convection. The ECM was running up to 210°C (case temperature) with the input power at 5W under natural convection, while the case temperature is still very low at 70°C with the same input power under forced convection. By knowing the package profile information shown in Fig. 7.4(b), the power density can be calculated as 69.4W/in^3 at case temperature 200°C under natural convection. For forced convection, we can't measure the power density at case temperature 200°C because the required large input power is impractical

for the measurement. So a linear relationship between the case temperature and the input power is assumed by ignoring the radiation heat at high temperature. By calculations, the power density of 279.3W/in^3 at 200^{o}C is obtained with the power input at 18.5W.

7.4 Transient thermal parameter measurement

7.4.1 Introduction

Since the trend in power electronics is toward greater packaging density, speed and high power dissipation, improvements in the thermal management of power semiconductor devices are becoming more and more important. Good thermal characteristics in transient conditions could provide a good tool to design and optimize the power packaging modules for high efficiency and high power density. [66]

As discussed in 4.2.1, although three-dimensional finite element method (3-D FEM) delivers very accurate results, its usage is limited by an imposed computation time in arbitrary load cycles. Therefore, a one-dimensional thermal network is investigated to extract thermal resistances and thermal capacitors. The dynamic behavior predicted by the thermal network is equivalent to numeric solutions of the 3-D FEM. More importantly, the one-dimensional thermal network can be used directly in the software for electrical design, such as Saber and Pispice. So the system designer can couple the thermal prediction with a circuit simulator to analyze the electro-thermal behavior of module system, simultaneously. This is also help the designer to identify and improve the one-dimensional network in a few minutes with the arbitrary or periodic power waveforms, and finally provide a reference to optimize the physical system for improving its thermal performance.

The usual way to obtain the thermal characteristics is to get the thermal resistance -- the ratio of thermal gradient to the heat flux density for one-dimensional heat conduction. This always generates a total value of the whole thermal system without any information about the contributions of the various layers of the system and the dynamic behavior of the device temperature. Since this type of information is helpful for a designer, a simpler method, which can give accurate characterizations, is necessary. Employing the 1-D

thermal model shown in Fig. 4.1(a), the transient thermal parameter analysis method for evaluation of thermal resistances and capacitances is based on an experiment using the temperature cooling-down curve measurement. This method allows both the accurate determination of thermal parameters of a power device and the observation of the physical meaning of the calculated thermal resistance contributions. [67]-[69]

This method has been successfully applied to a single chip embedded power module to obtain its thermal transient characteristics at normal temperature environments [70]. For high temperature applications, some material properties, such as the thermal conductivity and specific heat, may alter with the temperature. So in the transient thermal parameter for the high temperature EMC, the temperature dependent parameters need to be considered.

The flow chart shown in Fig. 7.6 describes the detailed steps of the transient thermal parameter analysis method. The one-dimensional equivalent thermal network is obtained from careful analysis of the high temperature ECM structure and the thermal parameters of this one-dimensional network are calculated by knowing the physical information of the single-chip module. However, since the calculated thermal network is not accurate due to the inadequacy of physical information, further steps to adjust the calculated parameters are required to obtain the accurate equivalent network.[70] As shown in the flow chart, the calculated equivalent thermal network is input into the saber simulation to get a temperature cool-down curve of the chip. Then this simulated cool-down curve is compared to another temperature cool-down curve, which is obtained by the experimental measurement. To get the accurate equivalent thermal network, the thermal parameters in the calculated equivalent thermal network are adjusted until the simulated cool-down curve finally matches the experimental cool-down curve. Therefore, the accurate thermal parameters can be obtained in the finally adjusted thermal network after the comparison of the two cool-down curves.

In this part, the transient thermal parameter analysis method will be introduced by focusing on a high temperature ECM. First, as outlined in the explanation of the experimental setup, the temperature cool-down experiment, including the control scheme and analysis process, is explained. The experimental characterizations, which are

obtained by comparing the experiment and simulation cool-down curves, are then discussed. Finally the accurate thermal parameters of the ECM are given and analyzed.

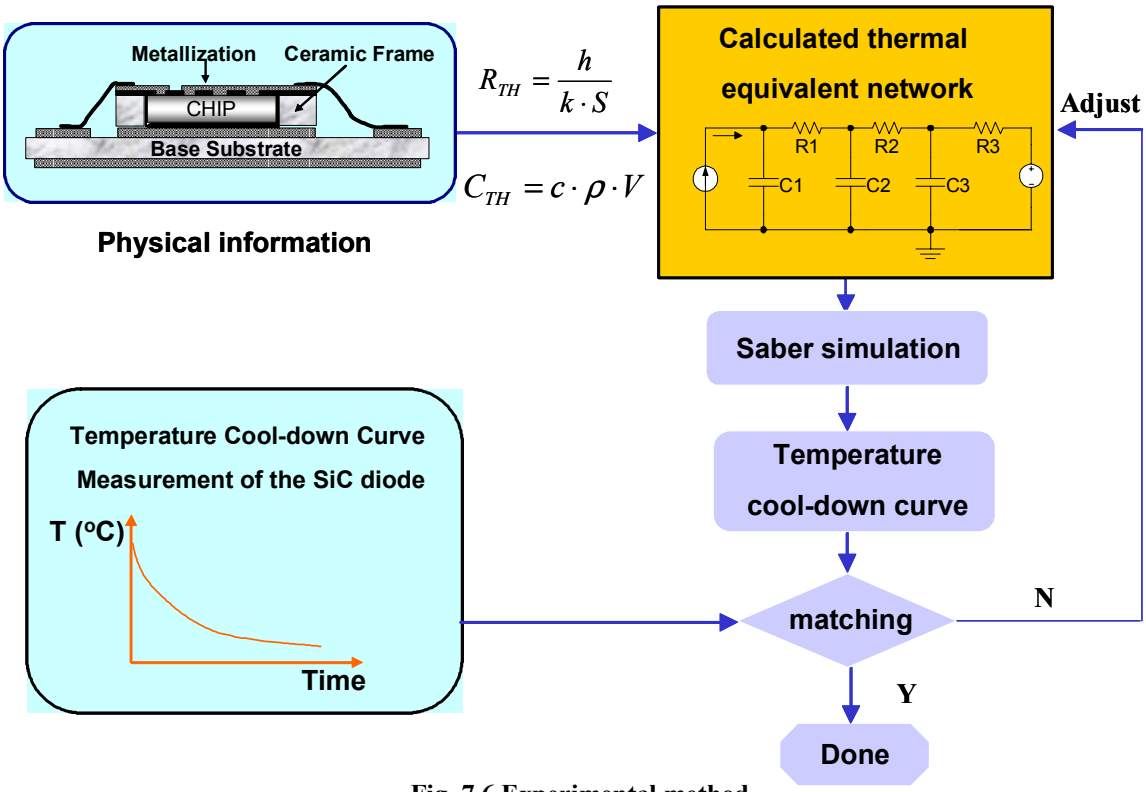


Fig. 7.6 Experimental method

7.4.2 Experimental setup

The proposed measurement setup for a high temperature transient test is shown in Fig. 7.7. In this setup, a high temperature ECM was attached on three layers of alumina and one layer of the Cu heat spreader using the high temperature thermal grease. The whole setup is put on the hot plate, which can be controlled at a constant temperature 180°C. Since the alumina has a relatively low thermal conductivity, three alumina ceramic layers are intentionally inserted under the EMC, so as to increase the thermal resistance from the chip junction to the hot plate. With the large thermal resistances in the heat flow path, a higher temperature difference from the chip junction to hot plate can be achieved for better measurement during the high temperature cooling-down test.

To employ the 1-D thermal model shown in Fig. 4.1(a), the necessary boundary conditions and initial states are required. Firstly, we assume that the heat generated from

ECM only flows to the hot plate through the ceramics and heat spreader, and that there is no heat leakage from the top and other sides. To achieve this, the whole setup shown in Fig. 7.7 was insulated with fiberglass material and put within two metal boxes, which were sited on the hot plate. Ideally, there would be no heat flow between two metal boxes if the two metal boxes had the same temperatures as the hot plates, thus it is a perfect insulation. However, due to the thermal resistances of the metal boxes, the temperature distributes evenly over the metal boxes and the actual temperatures of two metal boxes are lower than the hot base plate. The purpose of using two boxes is to reduce the heat flow from the inside box to outside, thus a high temperature on the inside box, which is close to the hot plate, can be obtained. The possible leakage heat can be reduced by decreasing the temperature difference from the chip junction to the inside box.

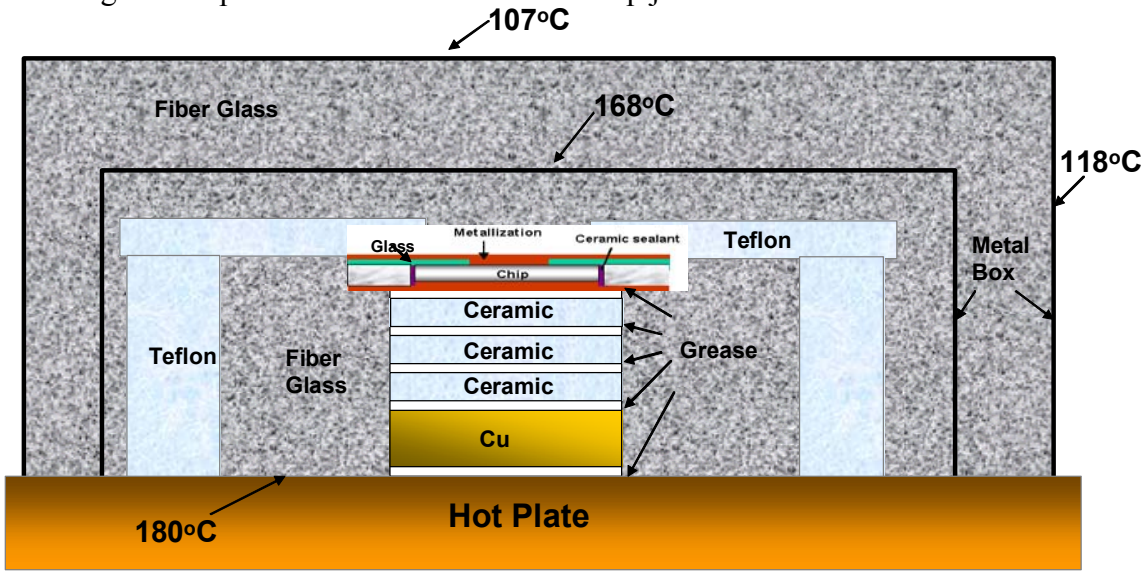


Fig. 7.7 Experimental setup for the high temperature transient measurement

To prove the low heat leakage from the setup, we measured the box temperatures as shown in Fig. 7.7. The inside box has a temperature 168^{o}C that is close to that of the base plate, while the outside box has a side temperature 118^{o}C and a topside temperature 107^{o}C. We assume that the uniform temperature distribution is at the setup from the EMC to the Cu heat spreader and the highest temperature of this setup is 235^{o}C. So the thermal resistance R_{th} from the setup to the inside box and the related leakage heat I_{th} can be calculated as below:

$$R_{th} = \frac{L}{KS^2}$$
$$I_{th} = \frac{T}{R_{th}} \qquad (7.2)$$

where K is the thermal conductivity of the fiberglass 0.04W/m.K, L is the distance from the setup to the inside box, S is the cross section area of the heat flow, T is the maximum temperature difference between the setup and the inside box at 62°C.

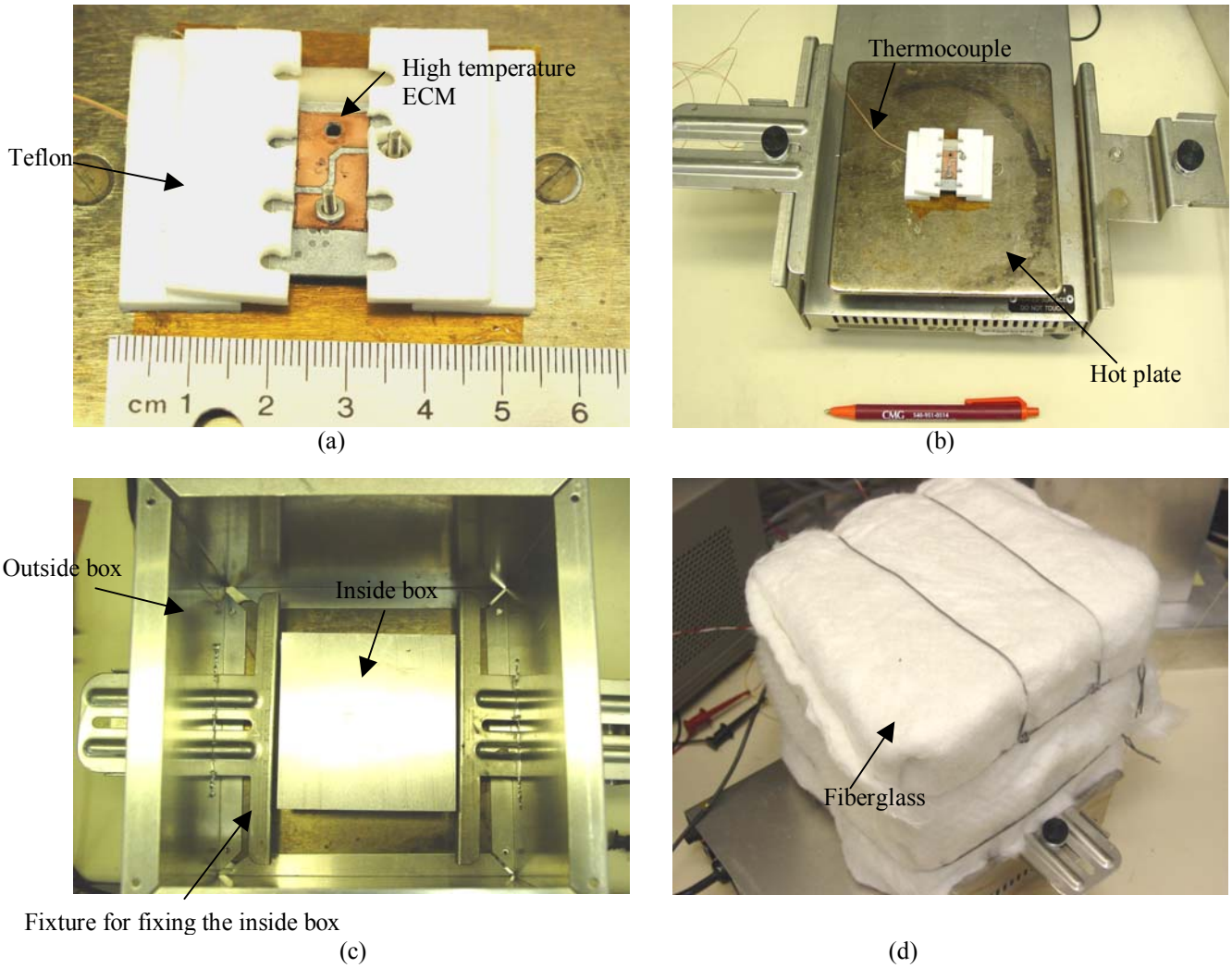


Fig. 7.8 Experimental setup of the cool-down temperature curve

From equation 7.2, the thermal resistance from the setup to the topside of the inside box is 757.6°C/W and the possible heat leakage from the topside is below 0.08W. The thermal resistance from the setup to the sides of the inside box is even higher at 1250°C/W and

the possible heat leakage is below 0.025W. Therefore, the total maximum heat leakage from the setup is below 0.105W. This low leakage is acceptable since the total input power for heating up the EMC is about 8.5W.

The physical experimental setup is shown in Fig. 7.7. As shown in Fig. 7.8(a), the adjustable D.U.T with several ceramic layers was carefully attached above the heat spreader using Teflon fixtures, because of their favorable thermal characteristics. The whole setup was built on a temperature controllable hot plate and a thermocouple was attached to the hot plate with kapton tape to monitor the temperature of the bottom side of the heat spreader, shown in Fig. 7.8(b). Then in Fig. 7.8(c), two metal boxes were employed for the good insulation purpose with their bottom sides attached to the hot plate. The insulating material fiberglass was filled into the two metal boxes due to its good thermal insulation properties. Finally, as shown in Fig. 7.8(d), the outside box was covered by the fiberglass to prevent the heat from flowing to the environment.

The device under test (D.U.T) in the setup is an adjustable fixture shown in Fig. 7.7, so it is a universal experiment setup designed for different packaging samples.

7.4.3 Measurement of the cool-down temperature curve

7.4.3.1 Calibration

a. Introduction

The measurement of chip temperature is essential to the evaluation of thermal performance for the design, application and manufacture of the module. The electrical testing method for the temperature measurement is widely used. It is a direct, non-contact technique, since it utilizes the chip itself as the temperature sensor. Although methods such as infrared and liquid crystal sensing can be used to measure chip temperatures, their application is limited to visible surfaces. In contrast, the electrical method can be performed at a distance without introducing a sensor, using only the electro-temperature properties of semiconductor junctions. It is used extensively for direct component characterization measurements.

The calibration is used to set up the relationship between the temperature and the electrical parameter. This relationship can be measured and used to compute the semiconductor temperatures.

For diodes, the diode forward voltage is always chosen as the electrical parameter to build the relationship with the temperature since it has a linear association with the temperature.

For the estimation of the diode junction temperature using the forward voltage drop, it is necessary to analyze the characteristics of the diode. The forward voltage drop is a function of (1) Junction temperature and (2) forward current [71] [72]. When (2) is constant, the forward voltage drop will have a linear relationship with the temperature.

b. Experimental setup and results

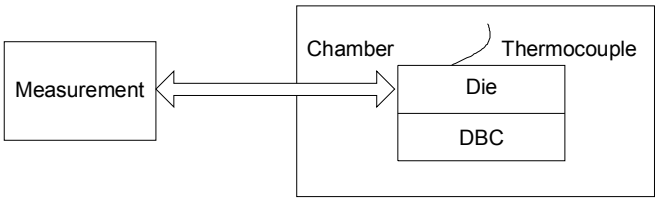


Fig. 7.9 Calibration setup

Fig.7.9 shows the calibration experimental setup. In this setup, the whole sample is put in a temperature controlled chamber to reach a thermal equilibrium state. The electrical parameters are measured with a very low sensing current, because any large amount of power input will change the thermal equilibrium environment. In this calibration, we employed the same experimental setup shown in Fig. 7.7 as the cooling-down measurement. By doing this, the system differential error between two measurements can be avoided. In Fig.7.7, the whole setup is well insulated with two metal boxes, so the leakage heat from the setup is negligible and a thermal equilibrium state can be achieved easily. The equilibrium temperature can be controlled by the hot plate from room temperature to 300^{o}C. The sensing pulse is at 1 KHz with a small duty cycle at 0.075 to avoid too much power input. This low power level can also be proved by calculations of the temperature increase under one pulse input by assuming the heat will not accumulate

during each pulse. Then assuming that the whole input power is used to heat up the die region, the chip temperature increase is calculated as follows:

$$q = -c \cdot \rho \cdot V \cdot \frac{dT}{d\tau}, \tag{7.3}$$

$$\text{Temperature increase } \Delta T = \frac{1}{c \cdot \rho \cdot V} \int_0^t q d\tau = 0.01936^{\circ} C$$

where density (kg/m^3) ρ is 3100, pulse period T (S) is 7.5E-5, specific heat capacity at (J/kg.K) c is 750, chip volume (m^3) V is 8.33E-10, input power (W) q is 0.5, sensing current (A) is 0.5.

So the temperature increase due to the input power is only 0.01936°C. It proves that the heat input is low enough not to heat up the junction or greatly change the thermal equilibrium environment.

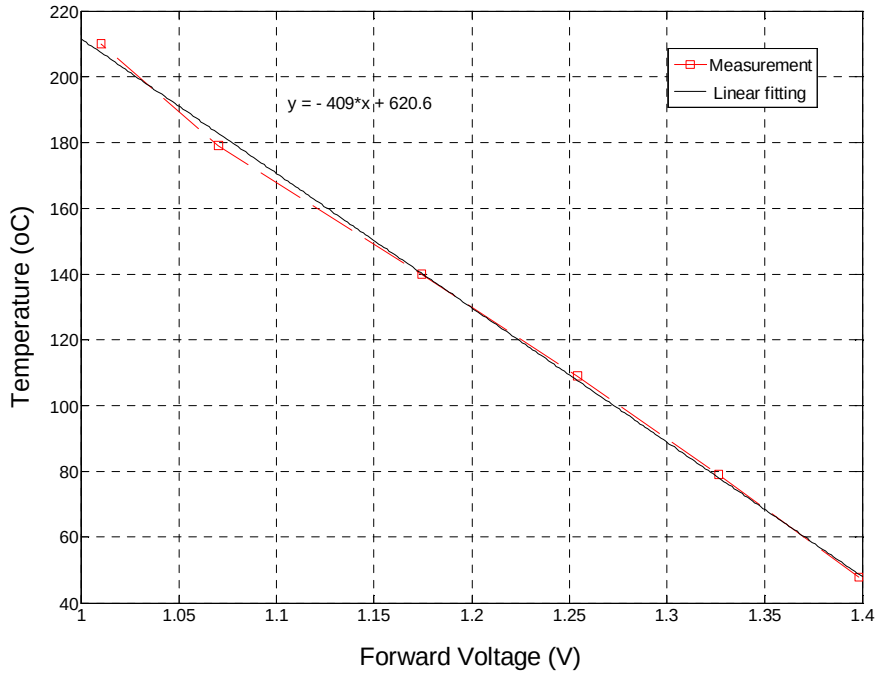


Fig. 7.10 Calibration result

With the calibration setup shown in Fig.7.6, the forward voltage of the SiC diode was measured from 80°C to 220°C with the sensing current at 0.5A. Fig. 7.10 illustrates the linear relationship between the forward voltage and the temperature and shows a negative

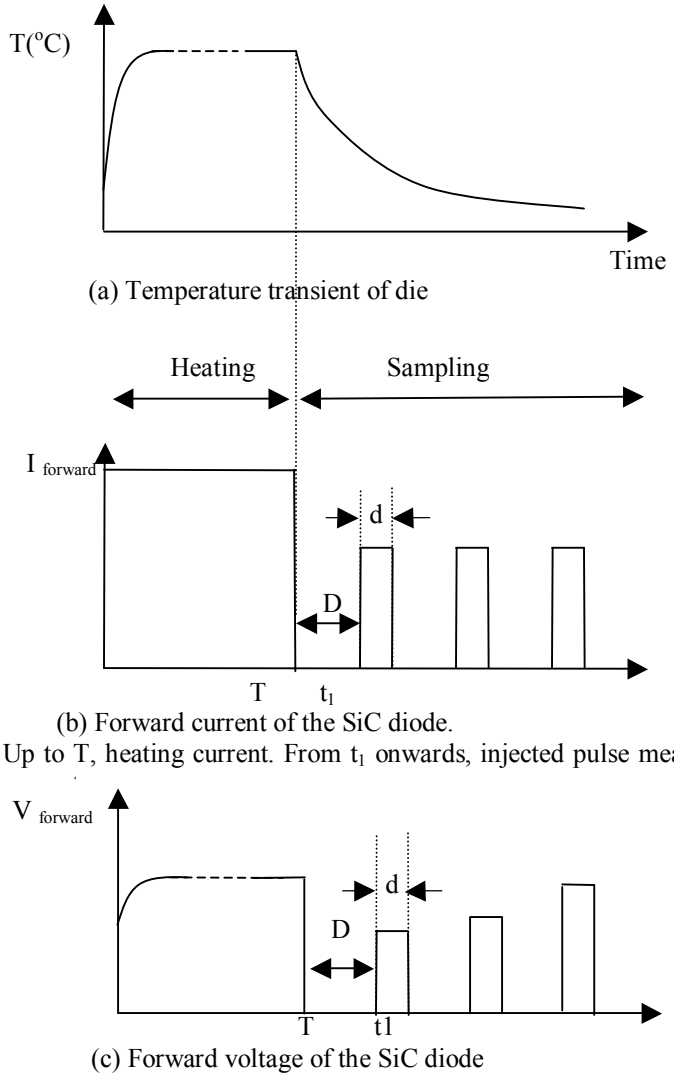
temperature coefficient at low forward currents. The curve fitting using MATLAB software shows the relationship can be represented by:

$$Y = -409.0\,X + 620.6 \qquad (7.4)$$

where x is the forward voltage, y is the related temperature.

7.4.3.2 Cool-down temperature measurement

The cool-down temperature curve is measured by setting a given power level on the diode to heat it up to a stable temperature, rapidly switching off the electrical power while simultaneously recording the forward voltage drop with the time evolution by injecting measurement current pulses as explained previously.



(a) Temperature transient of die

(b) Forward current of the SiC diode.
Up to T, heating current. From t_1 onwards, injected pulse measurement

(c) Forward voltage of the SiC diode

Fig. 7.11 Heating and cooling control

To take a good measurement of the high temperature cool-down curve, the device needs to be heated up to a constant temperature, which is much higher than the temperature of the base hot plate. So enough input power and necessary thermal resistances between the chip and the hot plate are required to obtain this high temperature difference between the chip and the hot plate. In this experiment, we chose the input power as 8.47W and added three layers of Al_2O_3 ceramics between the chip and the hot plate as discussed. After the setup reaches the steady state, the heating input needs to be removed. Then sensing pulses are employed to measure the diode forward voltage with a low power input to avoid heating up the device. The sensing pulses employed here are the same as in the calibration test. The pulses are at 1 kHz and the sensing current is at 0.5A, so the temperature increase due to each pulse is only 0.01936°C, which has been calculated in equation 7.3. This proves that the input power is low enough not to heat up the device.

The detailed control scheme to measure the temperature cooling-down curve is shown in Fig. 7.11. Two different actions occur during the experiment. Before time T, the high temperature ECM is heated up by conducting the high forward current 2.94A through the SiC diode. The heating continues until the DUT reaches a steady thermal state as shown in Fig.7.11(a). After time T, the ECM is allowed to cool down by removing the high forward current. At time t_1, it is turned on for a short duration d, and a low sense current is applied to the SiC diode. The temperature-sensitive, forward voltage $V_{forward}$ of SiC diode is then measured during each pulse as shown in Fig. 7.11(c). During this sampling interval, the chip junction is heated until the sense current is removed. However, as shown when properly executed, the heating is minimal and can be further reduced to a negligible level with faster data acquisition.

To realize the control scheme shown in Fig. 7.11, an experimental control circuit was built as shown in Fig. 7.12. Two MOSFETs were employed to control the heating and cooling processes and an oscilloscope was used to measure the diode forward voltage drop $V_{forward}$. During the heating period, both MOSFETs were turned on as shown in Fig. 7.12(b). The resistor R1 was shorted by the MOSFET D2 and the high forward current 2.94A would flow through MOSFET D2 to heat up the ECM. After the setup reached the steady state, the MOSFET D2 was turned off to let the setup cool down. A series of 1kHz pulses generated by a signal generator were applied to control the MOSFET D1. The

sensing current was reduced as low as 0.5A, since R1 was added to the measurement circuit during the cooling-down period. The diode forward voltage was then recorded by an oscilloscope during each pulse, which has a period at 75us. To ensure the forward current as a constant during the cooling-down measurement, the voltage source should be much larger than the diode forward voltage during each pulse. We selected 18.3V as the source voltage, which was much larger than the diode forward voltage of 0.9V at temperature 180^{o}C.

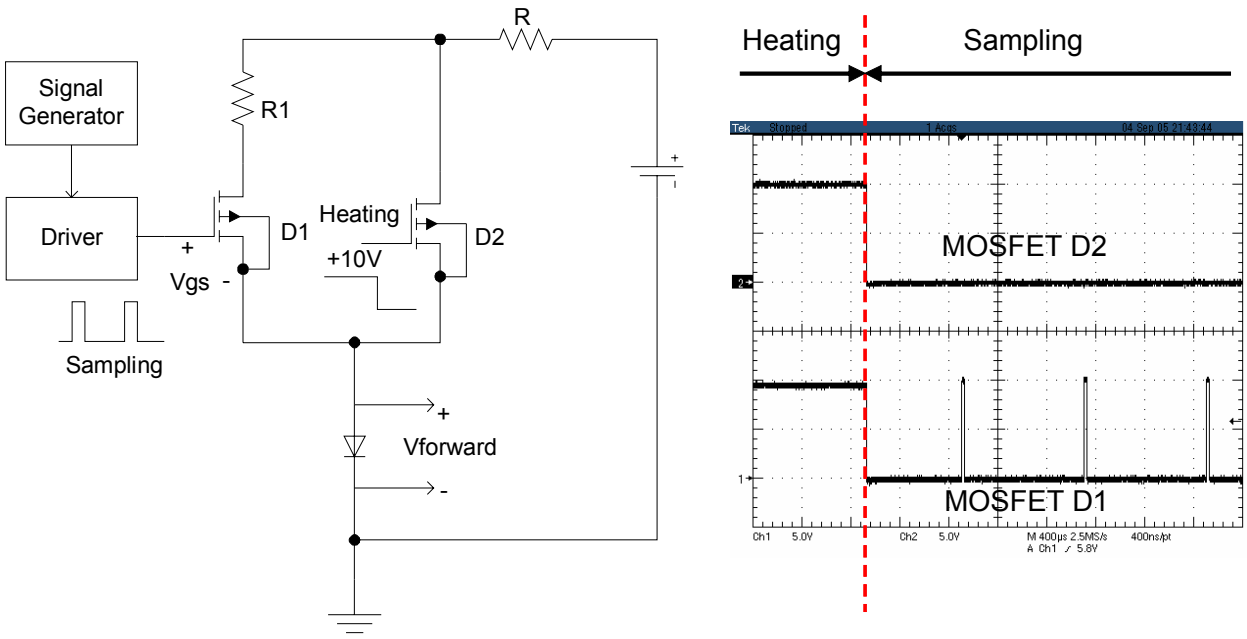


Fig. 7.12 Experimental circuit for measuring the cool-down temperature curve

With the control scheme shown in Fig. 7.11, the diode forward voltage drop at each pulse was recorded by setting the forward current (about 0.5A). To get an accurate forward voltage, hundreds of sampling data was taken during each pulse and then averaged through the MATLAB program shown in Appendix III. The diode forward voltage versus time during the cooling-down period is shown in Fig. 7.13. The small variations of the forward voltage curve up to 3mV are caused by the recording errors of the oscilloscope; however, these small variations are negligible since the temperature

variation caused by 3mV is only 1.227°C according to the calibration relationship of 0.409°C/mV.

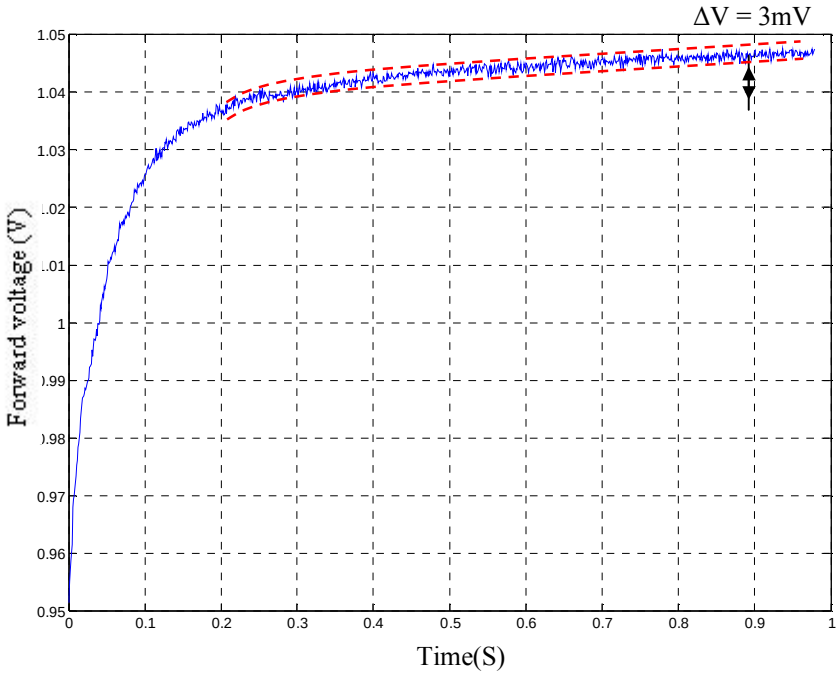


Fig. 7.13 Forward voltage recording during cool-down period

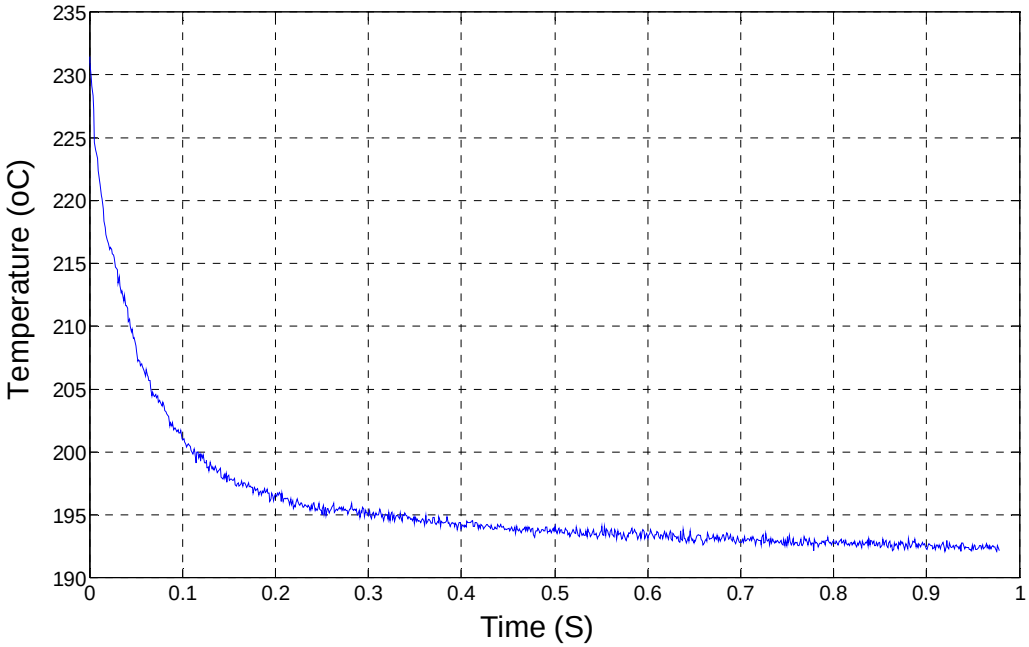


Fig. 7.14 Temperature cool-down curve recording

Using the calibration relationship stated in the equation 7.4, the forward voltage curve with time shown in Fig. 7.13 can be converted to a transient temperature curve shown in Fig. 7.14. This process used the MATLAB program shown in Appendix III. In this experiment, since the temperature cooling-down curve was recorded with the hot plate temperature at 180^{o}C, the temperature change of the chip was more than 50^{o}C. The temperature dependent parameters of the materials should be considered with such a large temperature change. This cooling-down temperature curve shown in Fig. 7.14 is decided by the thermal properties of the different physical parts on the heat flow path. So by building a thermal model, which includes the physical information of these parts, it is possible to obtain the same temperature cooling-down curve as the experimental curve. In other words, by comparing the simulated curve from the thermal model and experimental curve, the thermal model can be identified to accurately represent the real packaging structure. So it is necessary to build a thermal model to represent the physical structure.

7.4.4 Equivalent thermal network

7.4.4.1 Introduction

The key step to apply the transient thermal parameter analysis method is to build up a thermal model, which can describe the thermal behavior of the high temperature ECM including the transient and steady states. As discussed in 4.1.1, one-dimensional thermal model quickly offers insight into the physical layers of the components, providing useful information in a few minutes as well as presenting relatively accurate results. Therefore, a one-dimensional thermal model is employed in the transient thermal parameter analysis method to describe the thermal characterizations of a high temperature ECM. The characterization results can then be applied in a design for more efficient power device packages.

7.4.4.2 Equivalent thermal network analysis

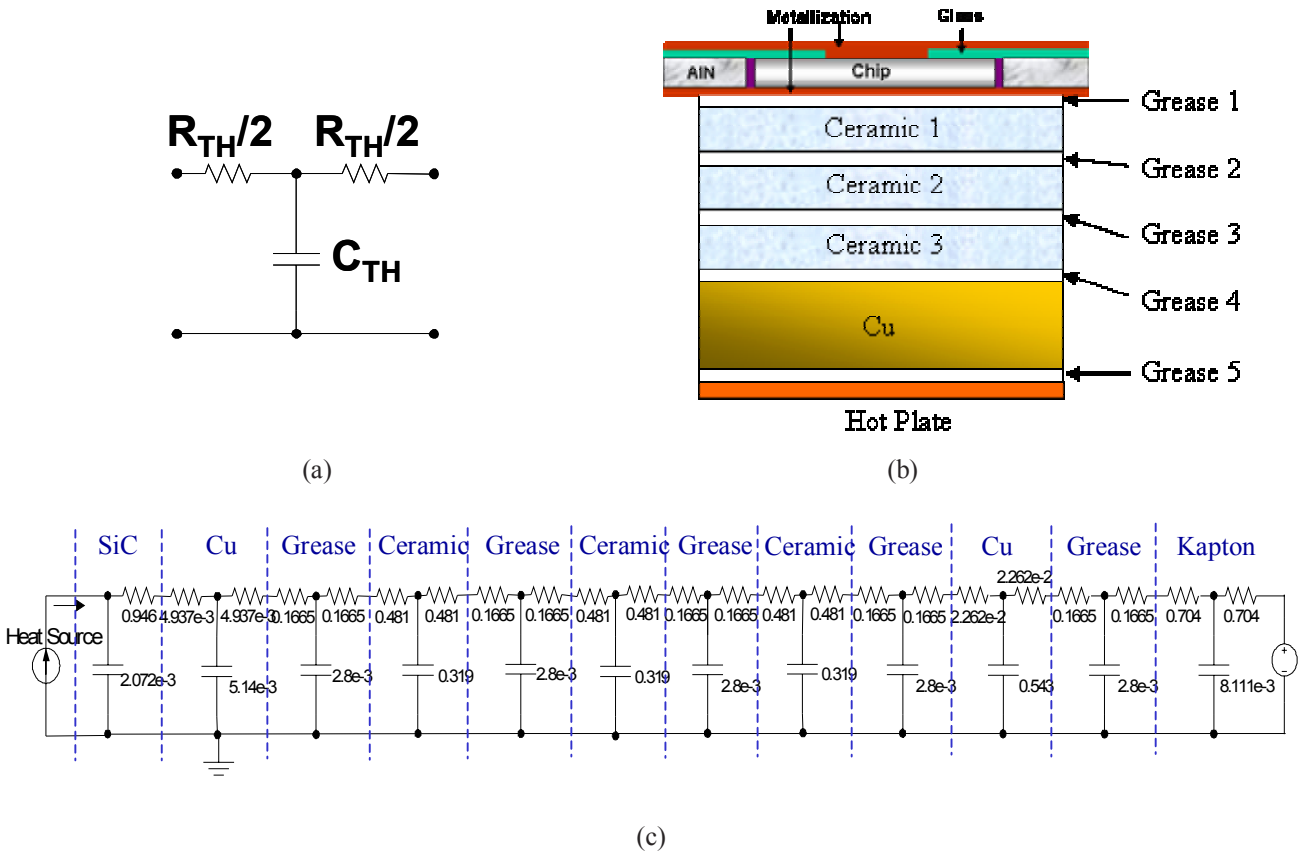


Fig. 7.15 Equivalent thermal network

To set up a one-dimensional thermal network, the thermal parameters of each layer need to be calculated through equation 4.1-4.3 based on the physical structure. An R-C-R cell shown in Fig. 7.15(a) is employed to represent each layer in the structure. With the calculated thermal resistances and capacitance of each layer, an equivalent thermal network can be obtained to have a direct physical correspondence to Fig. 7.15(b). Fig. 7.15(c) shows the calculated equivalent thermal network, which physically represents the high temperature ECM system shown in Fig. 7.15(b).[65]

As shown in Fig. 7.15(c), the heat is generated from the SiC diode, which is represented by a heat source. Since the bottom-side temperature of the heat spreader is kept constant, a voltage source is employed to characterize this controlled constant temperature. This step can eliminate the complicated cooling system under the heat spreader and simplify

the thermal model. The generated heat can flow from both top and bottom sides. The heat path to bottom side is as follows: metallization, thermal grease 1, ceramic1, thermal grease 2, ceramic2, thermal grease 3, ceramic3, thermal grease 4, heat spreader, thermal grease 5, and kapton. Compared to the heat path on the bottom side, the topside of the EMC is well insulated, so the thermal system is considered as a one-sided cooling system. Since chip temperature decrease is more than 50^{o}C in the cool-down temperature curve, the temperature dependent parameters including the thermal conductivity and specific heat are considered necessarily. In the ECM system as shown in Fig. 7.15(b), only three materials Al2O3, SiC and copper shown in Table 7.2, which have large thickness, are considered to be dependent on the temperature change.

Table 7.1 Temperature dependent parameters [73]

Material	*Thermal conductivity K*	*Specific heat C*
Al2O3	$K= 2 X 10^{-4} T^{2} -0.12 T + 34$	*C= 0.73(T-200)+1060*
SiC	$K= 1.55 X 10^{-3} T^{2} -1.11 T + 285$	*C=1.28(T+23)+600*
Copper	*Constant*	*Constant*

Although the identification of the physical correspondence could be obtained directly through the calculated thermal equivalent circuit, many factors limit the accuracy of the calculated thermal parameters. One of the most important factors is the interface resistance. The interfaces formed between the contacting surfaces can play a major role in the determination of the thermal network established between the source and sink [74]. In the structure of the EMC system of Fig. 7.15 (b), eleven interface thermal resistances are detected; however, these interface thermal resistances are difficult to obtain by calculations, although they play an important role in the heat path. Another important factor is the heat-spreading angle, which could affect the calculation results seriously, since heat flow is not pure 1-dimensional or a pure lateral. The 45^{o} spreading approximation is shown to provide the reasonable accuracy in thermal calculations for components in which the size of the heat source area is greater than the component

thickness. If the source width W is equal to or smaller than the thickness H, then the calculation errors compared with the FEA solution are more than 15% and increase with the decrease of the source width. [75] Since we measure the cool-down temperature curve in the experiment, the thermal capacitances with the stored heat from the steady state play as heat sources during the cooling period. So it is difficult to accurately describe the cooling thermal behavior only using the calculated thermal parameters. Other practical factors could cause unexpected errors in the calculations including solder voids, metallization delamination, measurement errors of thin film (such as solder and grease layer) and so on. Since the calculated thermal equivalent network shown in Fig. 7.15(c) can't represent the physical structure accurately, further steps are required to adjust the calculated parameters in the equivalent network.

7.4.4.3 Saber simulation

Since the calculated equivalent thermal network isn't accurate, the experimental method is required to adjust the thermal parameters in the equivalent network. The experimental cooling-down temperature curve is employed as a reference for adjusting. The calculated equivalent thermal network can be input into the Saber software by setting the same initial and boundary conditions as the experiment. So another cool-down temperature curve of the SiC diode can be obtained through simulations. Theoretically, there is only a unique equivalent network for a given physical structure. [61] Therefore, by comparing the experimental and simulated cool-down curves, the calculated thermal network can then be adjusted.

7.4.4.4 Comparisons

To set up an accurate physical correspondence, the calculated thermal network adjusted by the experimental thermal measurement is a practical method.

As shown in Appendix II of thermal parameter calculations, the total thermal resistance can be obtained by equation 7.2, if the input heat is known as 8.74W and the temperature increase of the diode is 53^{o}C.

Therefore:

R_{total}= 52^{o}C / 8.47W = 6.12 ^{o}C/W

In the preliminary calculations, a 45^{o} heat spreading angle is assumed and the total thermal resistance of $6.12^{o}C/W$ is a prerequisite. By setting the same initial conditions as the measurement, the calculated equivalent thermal network can be simulated to obtain a temperature cooling-down curve, which is shown as the smooth curve in Fig. 7.16. The measured SiC diode temperature cool-down curve is shown as the "noisy" curve. Fig.7.16 shows that the simulated cool-down curve from the preliminary calculated network can't match the experimental curve. So further adjusting is required based on fully understanding the thermal transient behaviors as well as the physical structure in the EMC system.

In Fig.7.16, the measurement curve can be divided into two parts: very small time constants part 1 and large time constants part 2. The small time constants are related to the diode spreading domain and the large time constants are related to the ceramics and copper plate domain. As explained in Fig. 7.17, during the cool-down process, the heat first spreads from the chip to the region 1 of the die spreading domain, following the $45^{o}C$ spreading angle. As time goes on, the large time constants decided by the ceramics and the copper plate become dominant, so the stored heat in the region 2, which is from the whole area of the ceramics and copper plate, plays the major role over a longer time. In Fig.7.16, the simulated curve from the preliminary calculated parameters has larger time constants than the experimental curve in the diode spreading domain, however, it has smaller time constants during the ceramics and copper plate domain. Therefore, the preliminary calculations should be adjusted as follows:

1. Adjust the thermal resistances and thermal capacitances of the ceramic 2 and 3 based on the full area (increase the time constants of part 2);
2. Adjust the thermal resistances and capacitances of the different layers in the die spreading area, which includes the metallization and ceramic 1. (decrease the time constants of part 1);
3. Provide more accurate thermal resistances for each layer. Due to the $45^{o}C$ heat spreading angle, the top half-part resistance will be larger than the bottom half-part resistance in each layer as shown in Fig.7.15(a).

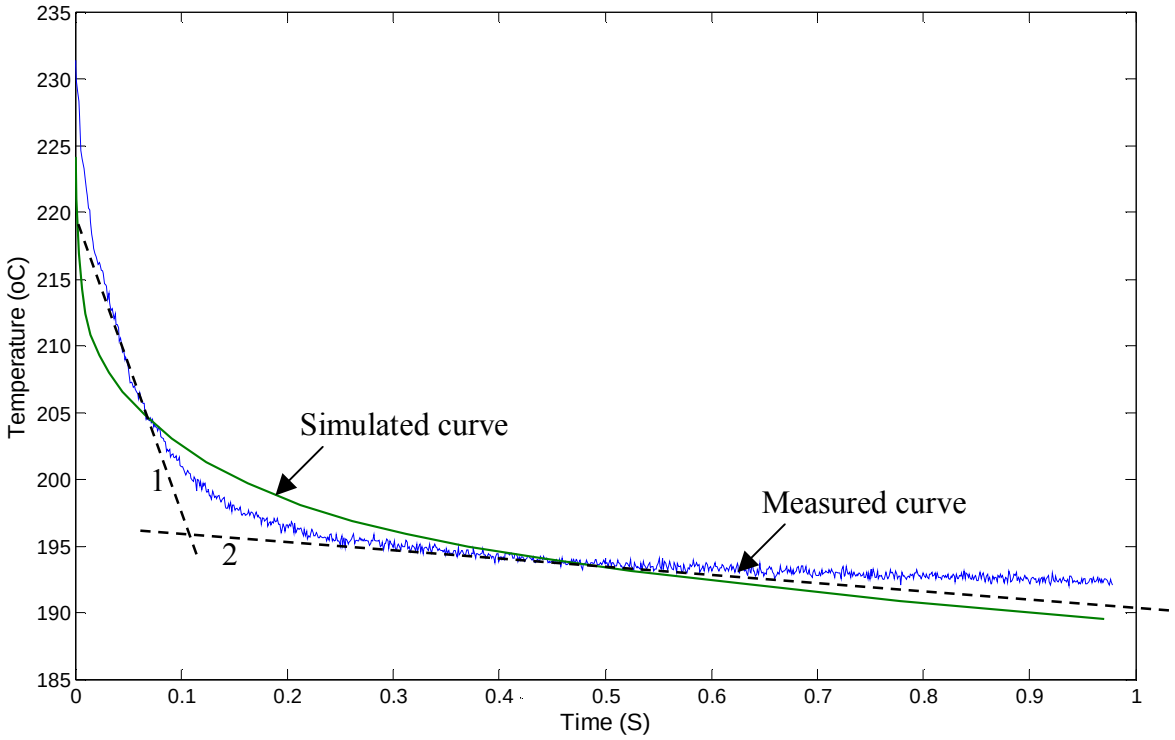


Fig. 7.16 Simulated curve direct from the calculated equivalent curve

The cool-down curve is very sensitive to the thermal parameter change, which means the parameters can be adjusted to accurately fit the experimental curve. Also, the thermal parameter change of the different layers will change the different part of the curve, since the time constants of the different layers become larger on the heat path. For example, if the thermal parameters of the ceramic layer are increased, the middle part of the cool-down curve will be higher than the experimental curve. Therefore, the calculated thermal parameters can be modified to get a simulated cool-down curve to fit the measured curve by adjusting the thermal parameters of every layer. An experimental based identification on the thermal contributions can be performed by combining the physical structure information and the experimental measurement.

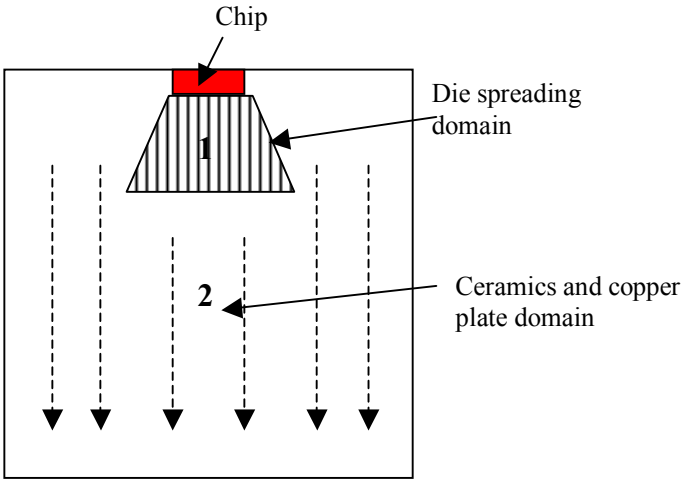


Fig. 7.17 Thermal behaviors during the cool-down process

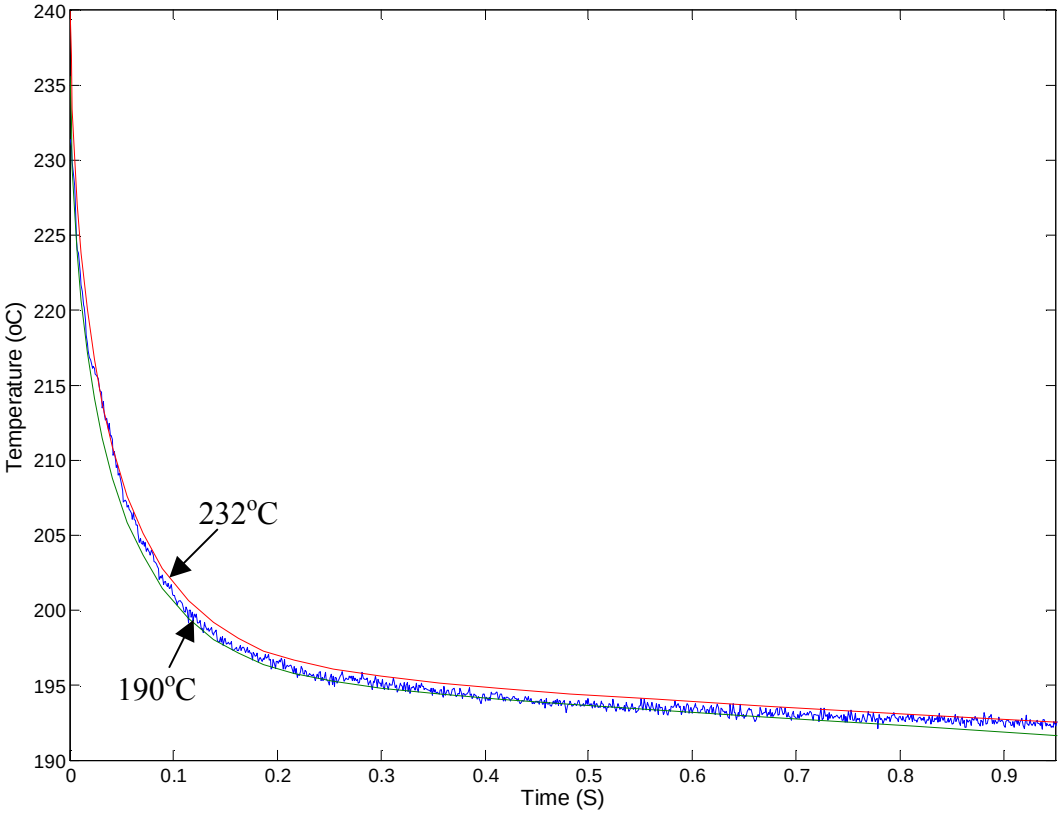


Fig. 7.18 Comparisons by considering the temperature dependent parameters

After the adjusting, two simulated curves are shown in Fig. 7.18 with the temperature dependent parameters considered at 190°C and 232°C respectively. The measured

temperature cool-down curve is shown as the "noisy" curve, which is located between the two simulated curves. These shows that the large temperature change in the system will result in the material thermal properties alteration, finally affect the thermal behaviors in the system.

To match the measurement curve, the temperature dependent properties of different materials, including the thermal conductivity and specific heat, are averaged using the parameters at 190°C and 232°C. The averaged parameters are then input to the equivalent thermal network for simulations. The final matching result is shown in Fig. 7.19. The simulated temperature curve from the average thermal properties shows as the smooth curve, which matches the measured curve very well. The thermal parameters employed in the final matched thermal network are shown in Table 7.3.

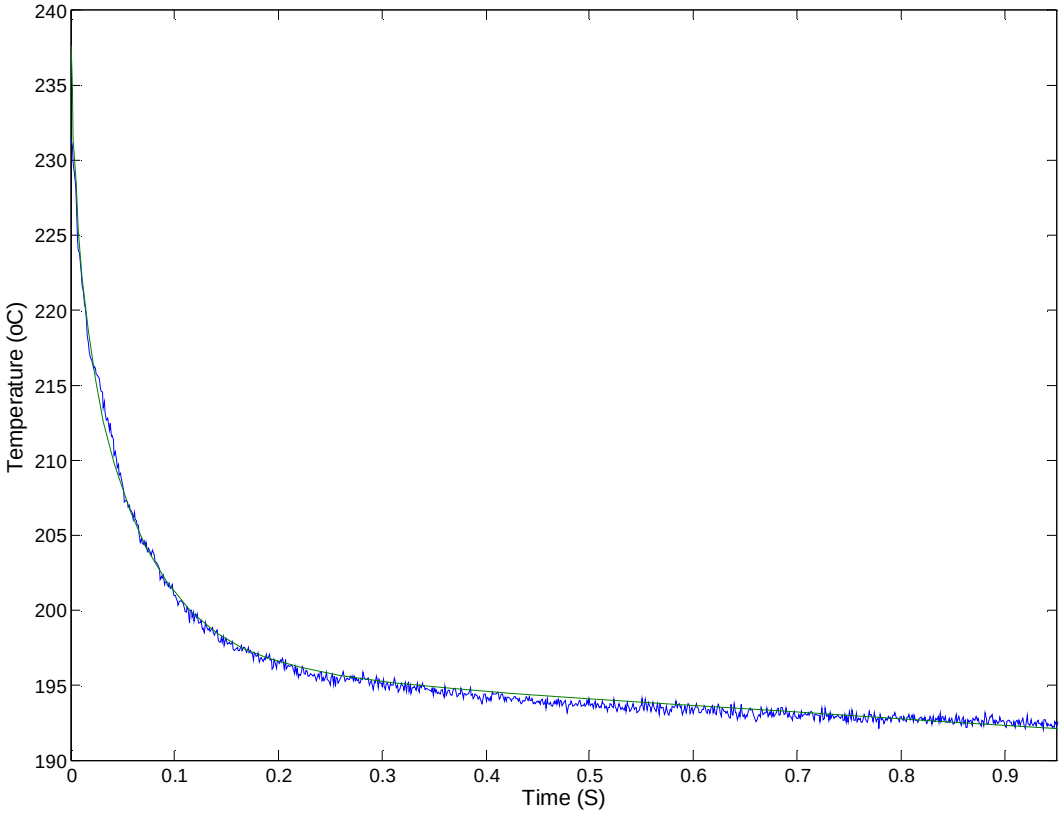


Fig. 7.19 Matched results with the average physical properties

Table 7.2 Thermal parameters of different layers after adjusting

	Thermal Resistance ($^oC/W$)	*Thermal Capacitance (J/K)*
SiC chip	*0.939*	*$2.423x10^{-3}$*
Metallization	*0.020*	*$2.56x10^{-3}$*
Thermal grease	*0.631*	*$1.061x10^{-3}$*
Al_2O_3 ceramic	*1.953*	*0.017*
Thermal grease	*0.362*	*$1.848x10^{-3}$*
Al_2O_3 ceramic	*0.857*	*0.065*
Thermal grease	*0.070*	*0.010*
Al_2O_3 ceramic	*0.294*	*1.030*
Thermal Grease	*0.070*	*0.010*
Heat Spreader	*0.0452*	*0.543*
Thermal grease	*0.0694*	*0.010*
Kapton	*1.504*	*0.0081*

The transient thermal measurement shown here is only applied to a high temperature ECM using Cu metallization layers, not to a high temperature ECM using combined Cr and Cu metallization layers yet. Because of the thin thickness of the Cr buffering layer and the relatively high thermal conductivity of Cr at 94W/m· K, the measurement results of a high temperature ECM, which uses combined Cr and Cu metallization layers, may be similar to the results shown in Table 7.3. To explain it clearly, we consider a combined metallization module shown in Fig. 5.8, which has a similar structure to the ECM under test only using Cu metallization, which is shown in Fig. 7.15(b). The thermal resistance of a Cr buffering layer in the heat path can be calculated as below:

$$R_{Cr} = \frac{d}{\lambda \cdot A} = 0.054\,^{o}\text{C/W}$$

where d is the thickness of the Cr buffering layer at 50um, λ is the thermal conductivity of Cr and A is the cross-sectional area at 9.85mm^2.

Therefore, due to the large thermal resistance from the junction to ambient in the heat path, the thermal resistance of the Cr buffering layer can be neglected in the thermal design.

7.4.5 Summary

Experimental evaluation for the high temperature ECM is introduced in this chapter, including the electrical and thermal testing. Forward and reverse characteristics of the ECM are presented and the ECM has been operated up to 267^{o}C. Then the steady-state thermal measurement is presented with a simple cooling system under natural and forced convection. The calculated and experimental results are in good agreement. The power density attained under forced convection is 279W/in^3 by running the module at more than 200^{o}C. Finally, a high temperature transient thermal experiment is described to get the transient thermal parameters of a unique Cauer-equivalent thermal circuit. The temperature calibration, experimental setup, control circuit, temperature cool-down curve and curve fitting are presented. Physical identification of the contributions can be performed by combining the physical structural information and experimental measurement**.** The temperature dependent parameters are considered in the transient thermal measurement. The experimental results can be applied with a view to adopt the packaging technology for more efficient high temperature packages.

Chapter 8

Conclusions

8.1 Contributions

I. Development of a High Temperature 3-D Embedded Chip Module (ECM) With A Mechanically Balanced Structure

a. ***The studies show that the material CTE match and the mechanically balanced structure are important for high temperature applications.***

Most current high temperature technologies have reliability problems due to the material CTE mismatch and the unbalanced structure. The high mechanical stress occurs at the interface between the CTE mismatch materials and distributes at one side of the module due to the bending effect caused by the mechanically unbalanced structure.

b. ***This research develops a three-dimensional multilayer structure for high temperature applications.***

The three-dimensional structure has a low profile, better electrical performance and improved thermal performance. Since no 3-D high temperature module has been studied before, the research in dissertation is very important for the future research.

c. ***The high temperature embedded chip module has been measured up to 270^{o}C.***

The forward and reverse characteristics of the high temperature module were measured up to 270^{o}C. Additionally, the steady-state thermal testing demonstrates that the module can be run at a very high case temperature of over 200^{o}C.

II. Implementations of New Material for High Temperature Applications

a. ***Glass is used in the high temperature module.***

This research studies the relationship of the glass CTE and the glass firing temperature. The study shows that the reduction of the glass CTE can lead to a high glass firing

temperature. Thus by changing the glass composition, it is impractical to match the CTE of the SiC chip at 4ppm/^{o}C, while keeping the firing temperature below 400^{o}C. So a glass with CTE of 6.4ppm/^{o}C is finally applied in the module. The proper method is successfully developed to implement the glass to the high temperature module.

b. ***Resbond material is successfully implemented to solve the reverse breakdown problem.***

This research examines the SiC chip and the materials around it, in order to resolve the breakdown problem of the high temperature module. It shows that the small holes and air bubbles in the sealing glass layer around the embedded semiconductor chip, which is due to the glass binder burnout in the firing process, cause the voltage breakdown. "Resbond" material is implemented to solve the breakdown problem successfully, since this material does not have the binder burnout problem.

c. ***Chromium metallization is implemented using a hard chrome plating process.***

Studies show that the Cu metallization layer can cause high mechanical stress and lead to module failure at high temperature. The low CTE metal, chromium, is introduced and successfully electroplated as a buffering layer in the high temperature module using the hard chrome plating process.

III. Development of a New Packaging Structure to Achieve the Low Mechanical Stress

a. ***Combined metallization structure by using Cr and Cu.***

Due to the high electrical resistivity of the chromium metal, a new combined metallization structure by using Cr and Cu is developed, in which Cr acts as the stress buffering layer and Cu as the lateral current carrying layer.

b. ***Development of a fully symmetrical structure with flat metallization.***

To implement the combined metallization structure for reducing the mechanical stress, different packaging structures are studied and compared. The mechanical stress is finally

reduced to 126MPa in the chip area by employing a fully symmetrical structure with flat metallization.

c. ***Demonstration of the packaging process of the new packaging structure.***

The packaging process of the new packaging structure is successfully developed including implementation of chromium, the fully symmetrical structure and the flat metallization.

IV. Understanding of the Cooling System Reduction in the Normal Temperature Environments and the Reverse Behaviors of the High Temperature ECM at High Temperature

a. ***The study shows that the cooling system can be reduced by 76% using a high temperature module.***

Studies show that the high temperature EMC can handle the power density of 284W/in^3 under the forced convections with a small pieced of heat spreader with 2.1x2.1x0.2cm, while the power density of the normal temperature module is only 68W/in^3. The high temperature ECM only requires 23.81% of the heat dissipated areas of a normal temperature module.

b. ***The reverse characteristics of the high temperature ECM are studied.***

The reverse behaviors of the high temperature EMC are studied through the investigation of the SiC Schottky junction, the high temperature module package and the passivation layer. The theoretical reverse characteristics of the SiC junction are built up by considering the barrier lowering and the pre-avalanche multiplication effects. The studies show that the leakage current at high temperature is caused by the SiC Schottky junction and the passivation layer, not by the high temperature module package.

V. Development of an Experimental Method to Obtain the Transient Thermal Characteristics of the High Temperature Module

a. ***High temperature measurement by using the forward voltage of the high temperature module.***

The calibration is set up by using the relationship of the forward voltage of the ECM and the temperature. The high temperature cool-down measurement is successfully measured from 230^{o}C to 180^{o}C.

b. ***The temperature dependent parameters were considered in the analysis***

The temperature dependent parameters such as thermal conductivity and specific heat are examined to make the results more accurate.

c. ***A method was developed to obtain the transient thermal characteristics of the high temperature module.***

The method includes the high temperature cool-down measurement, the thermal parameter calculations, development of the thermal network, simulations and comparisons of the calculated and experimental curves. The transient thermal characteristics of the high temperature EMC are developed using this method.

8.2 Recommendation

8.2.1 Module Improvements

From the simulation results shown in Chapter 5, the thickness match between the SiC chip and AlN substrate is important to reduce the thermally induced mechanical stress. However, the thin AlN layer is prone to fracture during thermal cycling due to its low flexural strength and fracture toughness. Silicon nitride (Si_3N_4) is a good candidate for thin layer applications, since it has an intermediate thermal conductivity, a close CTE match to SiC and 2.4 times of the AlN fracture toughness. The thermal studies have shown that the high thermal conductivity of AlN is not of primary importance in this application.

For further practical applications in the system, the ECM requires attachment material for the cooling system. This material can be nanoscale silver paste, phase change material or even high temperatue thermal grease. Furter investigations are necessary to demonstrate the system applications.

8.2.2 Reliability Test

Although the ECM has been tested up to 250^{o}C in the chamber for both forward and reverse characteristics, the long-time reliability test has not been finished. Further experimental setup and reliability analysis are essential to qualify the ECM's realistic applications.

REFERENCES

[1] Jeffrey B. Casady, William C. Dillard, R. Wayne Johnson, and U. Rao, "A Hybrid 6H-Sic Temperature Sensor Operational from 25°C to 500°C," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 19, pp. 416-422, Sept. 1996.

[2] J.S. Salmon, R.W. Johnson, M. Palmer, "Thick film hybrid packaging techniques for 500°C operation**,"** High Temperature Electronics Conference, HITEC 1998 Fourth International, 14-18 pp. 103-108, June 1998.

[3] R. Wayne Johnson, Michael Palmer, Cai Wangand Yi liu, "Packaging Materials and Approaches for High Temperature SiC Power Devices," Advancing Microelectronics, Jan/Feb 2004, pp. 8-11.

[4] F.P. McCluskey, R. Jain, N. Tiwari, R. Grzybowski, J. Benoit, S. Lin, "Die attach and wirebond systems for high temperature electronics," High Temperature Electronics, 1999. HITEN 99. The Third European Conference, 4-7 July 1999, pp. 63-67.

[5] F. P. McCluskey, D. Das, J. Jordan, L. Condra, T. Torri, J. Fink, and R. Grzybowski, "Packaging of Electronics for High Temperature Environments," International Journal of Microcircuits and Electronic Packaging, Vol. 20, No. 3, p. 409, Third Quarter 1998.

[6] J. Benoit, S. Chin, R. Grzybowski, S. Lin, R. Jain, and P. McCluskey, "Wire Bond Metallurgy for High Temperature Electronics," Proceedings of the 4th International High Temperature Electronics Conference, held in Albuquerque, NM, June 1998, p. 109.

[7] M. Mahaney, M. Shell, R. Strode, "Use of the in-process bond shear test for predicting gold wire bond failure modes in plastic packages," Reliability Physics Symposium, 1991, 29th Annual Proceedings, International 9-11 April 1991, pp. 44 – 51

[8] H. K. Charles Jr. and G. V. Clatterbaugh, "Packaging Considerations for High Temperature Operation," Proceedings of the Second International High Temperature Electronics Conference, June 1994, p. IX-3.

[9]Y. Sugawara, D. Takayama, K. Asano, "3 kV 600 A 4H-SiC high temperature diode module," Power Semiconductor Devices and ICs, 2002. Proceedings of the 14th International Symposium, June 2002, pp. 245 – 248.

[10] E.Savrun, "Packaging considerations for very high temperature Microsystems," Sensors, 2002. Proceedings of IEEE, Vol. 2 , 12-14 June 2002, pp. 1139 – 1143

[11]F. Masheeb, S. Stefanescu, A.A. Ned, "Leadless sensor packaging for high temperature applications," Micro Electro Mechanical Systems, 2002. The Fifteenth IEEE International Conference on 20-24 Jan. 2002, pp. 392 – 395

[12] R.S. Okojie, A.A. Ned, and A.D. Kurtz, "Operation of a(6H)-SiC pressure sensor at 500°C ", Sensors and Actuators, A-Physical, v. 66, no. 1-3, 1998, pp. 200-204

[13] Jie Sun, H. Fatima, A. Koudymov, A. Chitnis, "Thermal management of AlGaN-GaN HFETs on sapphire using flip-chip bonding with epoxy underfill," Electron Device Letters, IEEE , Vol. 24 , Issue: 6 , June 2003. pp. 375 – 377.

[14] B. Charboneau, B. Geil, W. Tipton, "12KV SiC PiN Diodes with High Voltage, High Temperature Packaging," CPES seminar, 2005.

[15] B. Ozmat, C.S. Korman, P. McConnelee; M. Kheraluwala, E. Delgado; R. Fillion, "A new power module packaging technology for enhanced thermal performance," Thermal and Thermomechanical Phenomena in Electronic Systems, 2000, The Seventh Intersociety Conference on Vo. 2, May 2000, pp. 287-296

[16] R. Fisher, R. Fillion, J. Burgess, W. Hennessy, "High frequency, low cost, power packaging using thin film power overlay technology," Applied Power Electronics Conference and Exposition, 1995. APEC'95. Conference Proceedings 1995, Issue 0, 5-9 March 1995 pp. 12 – 17

[17] B. Ozmat, C.S. Korman, R. Fillion, "An advanced approach to power module packaging," Integrated Power Packaging, IWIPP 2000, International Workshop on 14-15 July 2000, pp.8 – 11

[18] J. H. Lau, Flip Chip Technologies. New York: McGraw Hill, 1995.

[19] R. R. Tummala, E. J. Rymaszewski, and A. G. Klopfenstein, Microelectronics, Packaging Handbook. New York: Chapman & Hall, 1999.

[20] Xingsheng Liu; S. Haque, Guo-Quan Lu, "Three-dimensional flip-chip on flex packaging for power electronics applications", Advanced Packaging, IEEE Transactions on, Vol. 24, Issue 1, Feb 2001, pp. 1 –9.

[21] J.G. Bai, Guo-Quan Lu, Xingsheng Liu, "Flip-chip on flex integrated power electronics modules for high-density power integration," Advanced Packaging, IEEE Transactions on, Vol. 26, Feb. 2003, pp. 54 – 59

[22] P. Clot, J.-F. Zeberli, J.-M. Chenuz, F. Ferrando, D. Styblo, "Flip-chip on flex for 3D packaging," Electronics Manufacturing Technology Symposium, 1999. Twenty-Fourth IEEE/CPMT 18-19 Oct. 1999, pp. 36 – 41

[23] H.N. Shah, Y. Xiao, T.P. Chow, R.J. Gutmann, E.R. Olson, "Power electronics modules for inverter applications using flip-chip on flex-circuit technology," Industry Applications Conference, 2004. 39th IAS Annual Meeting, IEEE, vol. 3, Oct. 2004, pp.1526 – 1533.

[24] Zhenxian Liang, F.C. Lee, G.Q. Lu, D. Borojevic, "Embedded power-a multilayer integration technology for packaging of IPEMs and PEBBs," Integrated Power Packaging, 2000. IWIPP 2000. International Workshop on 14-15 July 2000, pp. 41 – 45.

[25] Z. Liang, J. D. van Wyk, "Functional integration in active IPEM by using a planar integration technology," Applied Power Electronics Conference and Exposition, 2005, Twentieth Annual IEEE, vol. 1, 6-10 March 2005 pp.375 - 381

[26] J. Yin, J.D. van Wyk, W.G. Odendaal, Z. Liang, "Design and optimization of embedded power chip modules for double-sided cooling," Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE, Vol. 3, Oct. 2004, pp. 1545 – 1551.

[27] Fay V. Tooley, "The handbook of glass manufacture : a book of reference for the plant executive, technologist, and engineer," 3rd New York : Books for the Glass Industry Division, Ashlee Pub. Co.

[28] www.ferro.com, "Glass assembling with sealing technology".

[29] www.cotronics.com, "Datasheet of electrically resistance adhesives".

[30]R. Kumar, D. Molin, "New high temperature polymer thin coating for power electronics," Applied Power Electronics Conference and Exposition, 2004. Nineteenth Annual IEEE, vol.2, pp.1247 – 1249.

[31] E. J. Podlaha and D. Landolt, "Induced codeposition I. an experimental investigation of Ni-Mo alloys", the Electrochemical Society, March 1996 vol. 143, no.3.

[32] E. J. Podlaha and D. Landolt, "Induced cocleposition II. a mathematical model describing the electrodeposition of Ni-Mo alloys", the Electrochemical Society, March 1996 vol. 143, no.3.

[33] E. J. Podlaha and D. Landolt, "Induced codeposition III. molybdenum alloys with Nickel, Cobalt, and Iron", the Electrochemical Society, March 1997, vol. 144, no.5.

[34] Data from www. webelements.com

[35] R. Weiner and A. Walmsley, "Chromium plating", Finishing Publications, 1980.

[36] J.K. Dennis, T.E. Such., "Nickel and chromium plating", Butterworths, 1986.

[37] J. D. Greenwood, "Hard chromium plating: a handbook of modern practice," Portcullis Press, 1981.

[38] P.L. Dreike, D.M. Fleetwood, "An overview of high-temperature electronic device technologies and potential applications," Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on, vol. 17, Issue 4, Dec. 1994, pp.594 – 609.

[39] A.R. Hefner, Jr. R. Singh, Lai Jih-Sheg, "SiC power diodes provide breakthrough performance for a wide range of applications," Power Electronics, IEEE Transactions on vol. 16, Issue 2, March 2001, pp. 273 – 280.

[40] J. Yin, Z. Liang, J.D. van Wyk, "High temperature embedded power module," Proceeding of Applied Power Electronics IEEE, 2005, pp. 334-339.

[41] J.-M. Dorkel, P. Tounsi, and P. Leturcq, "Three-dimensional thermal modeling based on the two-port network theory for hybrid or monolithic integrated power circuits," Components, Packaging, and Manufacturing Technology, Part A, Vol. 19 Issue 4 , Dec. 1996, pp. 501 –507.

[42] N.-E. Benhissen, A. Skorek, A. Lakhsasi, "Parallel modeling of the IGBT electrothermal behavior," Industry Applications Conference, 1999, Thirty-Fourth IAS Annual Meeting, Conference Record of the 1999 IEEE, Vol. 2, 1999, pp. 1403 –1407.

[43] M.S. Fan, A. Christou, M.G. Pecht, "Two-dimensional thermal modeling of power monolithic microwave integrated circuits (MMICs)," Electron Devices, IEEE Transactions on, Vol. 39, Issue 5 , May 1992, pp. 1075 –1079.

[44] I. Guven, Cho Lik Chan; E. Madenci, "Transient two-dimensional thermal analysis of electronic packages by the boundary element method," Advanced Packaging, IEEE Transactions on, Vol. 22, Issue 3, Aug. 1999, pp. 476 –486.

[45] A. Bejan, A. D. Kraus, "Heat transfer handbook," Published by N.J. Hoboken, 2003.

[46] P.E. Bagnoli, C. Casarosa, M. Ciampi, "Thermal resistance analysis by induced transient (TRAIT) method for power electronics devices thermal characterization-part I: Fundamentals and theory," IEEE Trans. Power Electron., vol. 13, pp.1208-1219.

[47] P.E. Bagnoli, C. Casarosa, M. Ciampi, "Thermal resistance analysis by induced transient(TRAIT) method for power electronics devices thermal characterization-part II: Practice and Experiments," IEEE Trans. Power Electron., vol. 13, pp.1220-1228.

[48] I-DEAS Electronic System Cooling User's Guide (Plano: UGS PLM Solutions Inc., 2004).

[49] Y.F. Pang, "Assessment of Thermal Behavior and Development of Thermal Design Guidelines for Integrated Power Electronics Modules," Dissertation of Virginia Polytechnic Institute and State University, 2005.

[50] B. J. Baliga, "Power semiconductor devices," PWS Publishing Co., Boston, 1996.

[51] V. Benda, J. Gowar and D. A. Grant, "Power semiconductor devices: theory and applications,"

[52] Yangang Wang, Yajie Wang, Xueqing Cui, Wuchen Wu, "A study on thermal stress of power IC die bonding," Solid-State and Integrated-Circuit Technology, 2001. Proceedings. 6th International Conference on vol 1, 22-25 Oct. 2001 pp. 109 – 112.

[53]M. Joodaki, G. Kompa, T. Leinhos, "Simulation and measurement of thermal stress in quasi-monolithic integration technology (QMIT)," Electronic Components and Technology Conference, 2001, Proceedings 51st, 29 May-1 June 2001, pp. 715 – 720.

[54] D.E. Riemer, "Thermal-stress analysis with electrical equivalents," Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [see also IEEE Trans. on Components, Packaging, and Manufacturing Technology, vol. 13, Issue 1, March 1990, pp. 194 – 199.

[55] G.Q. Lu, J.N. Calata, Z. Zhang; J.G. Bai, "A lead-free, low-temperature sintering die-attach technique for high-performance and high-temperature packaging," High Density Microsystem Design and Packaging and Component Failure Analysis, 2004. HDP'04, Proceeding of the Sixth IEEE CPMT Conference on June, 2004, pp. 42 – 46.

[56] M. W. Beranek, M. Rassaian, "Characterization of 63Sn37Pb and 80Au20Sn Solder Sealed Optical Fiber Feedthroughs Subjected to Repetitive Thermal Cycling," IEEE TRANSACTIONS ON ADVANCED PACKAGING, VOL. 24, NO. 4, NOVEMBER 2001

[57] W. H. Safranek, "The Properties of Electrodeposited Metals and Alloys- A Handbook," Second ediction, Published by the americanelectroplaters and surface finishers society.

[58] O. Milton, "The materials science of thin films," Academic press, Inc. 1992.

[59] J. Powell, "CO_2 laser cutting," New York, Springer-Verlag, 1993.

[60] R. Adam and carol Robertson, "Screenprinting", W W Norton & Co Inc, 2004

[61] D. M. Mattox, "Handbook of physical vapor deposition (PVD) processing," Noyes Publications, New Jersey, 1998.

[62] W. Bellingham, "Photomask and next-generation lithography mask technology," SPIE, 2000, v.4066, pp77.

[63] Complete Plating Manual, Caswell inc.

[64] N. Kanani, "Electroplating and electroless plating of copper & its alloys," Materials Park, Ohio, Finishing Publications, 2003.

[65] J. Yin, J. D. van Wyk, W.G. Odendaal and Z. Liang, "Comparison of transient thermal parameters for different die connecting approaches", Industry Applications Conference, 2003, 38th IAS Annual Meeting, vol. 1, pp. 222 –226.

[66] J.D. Van Wyk, F.C. Lee, "Power electronics technology at the dawn of the new millenium-status and future", power Electronics Specialists Conference, 1999. PESC99. 30th Annual IEEE, Aug 1999, vol.1, pp. 3 –12.

[67] E. Farjah, C. Schaeffer, and R. Perret, "Experimental thermal parameter extraction using nondestructive tests," in Proc. EPE'95 Conf. Sevilla, Spain, vol. 1, pp. 1.245 - 1.248.

[68] J. W. Sofia, "Analysis of thermal transient data with systemized dynamic models for semiconductor devices," in Proc. SEMITHERM'94, San Jose, CA, pp. 78 -85.

[69] P.E. Bagnoli, C. Casarosa, E.Dallago, G. Venchi, "Thermal Analysis of Packaged Power Devices", in Proc. EPE'99 Conf., Lausanne, Switzerland.

[70] J. Yin, J.D. van Wyk, W.G. Odendaal, Z. Liang, "Design and optimization of embedded power chip modules for double-sided cooling," Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE, vol. 3, 3-7 Oct. 2004, pp. 1545 – 1551.

[71] Yong-Seok Kim, Seung-Ki Sul, "On-line Estimation of IGBT Junction Temperature Using On–state Voltage Drop" IEEE Industry Applications Conference, 1998, vol.2, pp. 853-859.

[72] C.-S. Yun, P. Malberti, "Thermal Component Model for Electrothermal Analysis of IGBT Module Systems" IEEE Transactions on Advanced Packaging, 2001, vol 24, pp. 401-406.

[73] C. A. Harper, "Electronic Packaging and Interconnection Handbook", Fourth edition, McGraw-hill Company, 2005.

[74] B. M. Guenin, "Calculation corner: the 45^{o} heat spreading angle – an urban legend? " ElectronicsCooling, vol. 9, no. 4, Nov. 2003, pp. 10 –12.

[75] E. Marotta and J. Norley, "Thermal joint conductance", ElectronicsCooling, vol. 8, no. 3, Aug. 2002, pp. 16 –20.

Appendix I Data Sheet for the SiC Schottky Diode

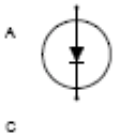
Preliminary

SIDC02D60SIC2

Silicon Carbide Schottky Diode

FEATURES:
- Worlds first 600V Schottky diode
- Revolutionary semiconductor material - Silicon Carbide
- Switching behavior benchmark
- No reverse recovery
- No temperature influence on the switching behavior
- Ideal diode for Power Factor Correction
- No forward recovery

Applications:
- SMPS, PFC, snubber



Chip Type	V_{BR}	I_F	Die Size	Package	Ordering Code
SIDC02D60SIC2	600V	6A	1.4 x 1.4 mm^2	sawn on foil	Q67050-A4162-A1
SIDC02D60SIC2	600V	6A	1.4 x 1.4 mm^2	unsawn	Q67050-A4162-A2

MECHANICAL PARAMETER:

Raster size	1.4 x 1.4	mm
Anode pad size	1.08 x 1.08	
Area total / active	1.742 / 1.191	mm^2
Thickness	401	µm
Wafer size	50	mm
Flat position	0	deg
Max. possible chips per wafer	867 pcs	
Passivation frontside	Photoimide	
Anode metalization	3200 nm Al	
Cathode metalization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond	Al, ≤ 250µm	
Reject Ink Dot Size	Ø = 0.3 mm	
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month	

Edited by INFINEON Technologies AI PS DD HV3, L4814A, Edition 1, 01.10.2001

Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Repetitive peak reverse voltage	V_{RRM}		600	V
Surge peak reverse voltage	V_{RSM}		600	
Continuous forward current limited by T_{jmax}	I_F		6	A
Single pulse forward current (depending on wire bond configuration)	I_{FSM}	T_C =25°C, t_p =10 ms sinusoidal	21.5	
Maximum repetitive forward current limited by T_{jmax}	I_{FRM}	T_C = 100°C, T_j=150°C, D=0.1	28	
Non repetitive peak forward current	I_{FMAX}	T_C =25°C, tp=10µs	60	
Operating junction and storage temperature	T_j , T_{stg}		-55...+175	°C

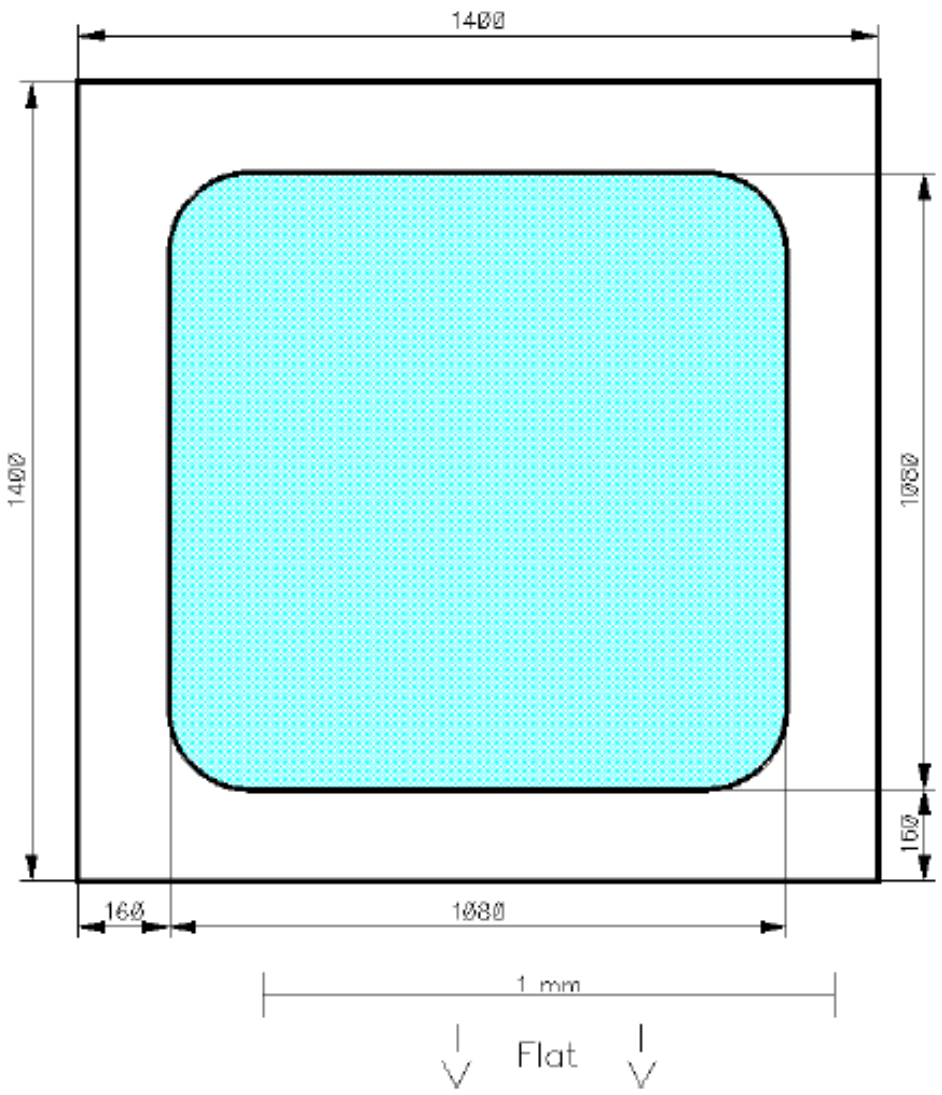
Static Electrical Characteristics (tested on chip), T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions		Value			Unit
				min.	Typ.	max.	
Reverse leakage current	I_R	V_R=600V	T_j=25°C		20	200	µA
Forward voltage drop	V_F	I_F=6A	T_j=25°C		1.5	1.7	V

Dynamic Electrical Characteristics, at T_j = 25 °C, unless otherwise specified, tested at component

Parameter	Symbol	Conditions		Value			Unit
				min.	Typ.	max.	
Total capacitive charge	Q_C	I_F=6A di/dt=200A/µs V_R=400V	T_j = 150 °C		21		nC
Switching time	t_{rr}	I_F=6A di/dt=200A/µs V_R= 400V	T_j = 150 °C		n.a.		ns
Total capacitance	C	I_F=6A di/dt=200A/µs T_j=25°C f=1MHz	V_R=0V		300		pF
			V_R=300V		20		
			V_R=600V		15		

CHIP DRAWING:



Edited by INFINEON Technologies AI PS DD HV3, L4814A, Edition 1, 01.10.2001

Appendix II Thermal Parameter Calculations

A2.1 Introduction

A one-dimensional thermal network is employed to analyze the high temperature ECM system shown in Fig. A2.1. The simulation results based on this network is compared to the experimental results to obtain the accuracy thermal parameters in the thermal network.

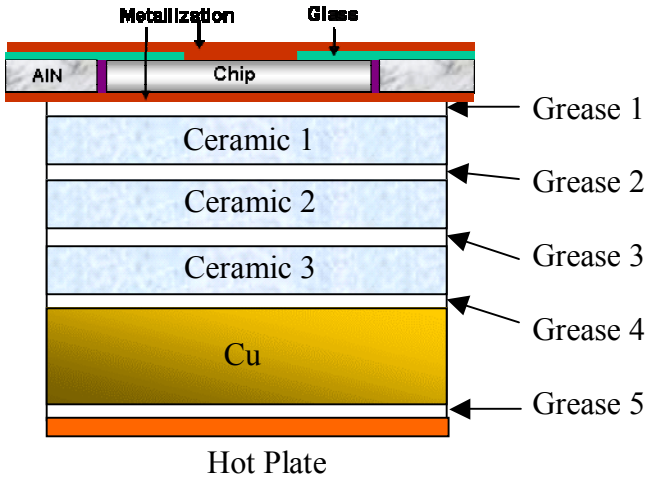


Fig. A2.1 Cross-sectional view of the measurement setup

A2.2 Calculations for the thermal parameters of the bottom side of the die

The thermal effect of the AlN carrier for embedding the chip is negligible because the ceramic adhesive surrounding the chip has a low thermal conductivity. So the layers under the bottom side of the die are: SiC, copper metallization, thermal grease1, Al_2O_3, thermal grease 2, Al_2O_3, thermal grease 3, Al_2O_3, thermal grease 4, heat spreader, thermal grease 5 and kapton tape layers, as shown in Fig. A2.1.

The total thermal resistance can be calculated by equation A2.1, since the input heat is 8.74W and the temperature increase of the diode from the measurement is 53°C.

Therefore:

$$R_{total} = 53^{o}C / 8.47W = 6.12\ ^{o}C/W \qquad (A2.1)$$

To match the total resistance, each layer in the structure needs to be analyzed as below:

1. SiC layer

Consider that the thickness of SiC chip is 0.445mm and the thermal conductivity is 120 W/^{o}C-m.

Thickness: d = 0.445 mm

Thermal conductivity: λ = 120 W/ ^{o}C.m

Area: $A = 1.4^2 = 1.96$ mm^2

Specific heat: c = 750 J/Kg.^{o}C

Density: ρ = 3100 Kg/m^3

Thus:

Thermal resistance $R_{SiC} = \frac{d}{\lambda \cdot A} = 1.892$ ^{o}C/W

Thermal capacitor $C_{SiC} = c \cdot \rho \cdot V = 2.027x10^{-3}$ J/K

2. Copper metallization layer

Consider that the thickness of the metallization layer is 0.075mm and the thermal conductivity is 380 W/^{o}C-m. To match the total thermal resistance, the conductivity area of Cu is chosen as 19.7 mm^2, because of the high thermal conductivity of the Copper.

Thickness: d = 0.075 mm

Thermal conductivity: λ = 380 W/ ^{o}C.m

Area: A = 19.7 mm^2

Specific heat: c = 385 J/Kg.^{o}C

Density: ρ = 8900 Kg/m^3

Thus:

Thermal resistance $R_{Cu} = \frac{d}{\lambda \cdot A} = 0.01$ ^{o}C/W

Thermal capacitor $C_{Cu} = c \cdot \rho \cdot V = 5.14 \times 10^{-3}$ J/K

3. Thermal Grease 1

Consider that the thickness of the thermal grease is 0.02mm and the thermal conductivity is 3 W/^{o}C.m.

Thickness: d = 0.02 mm

Thermal conductivity: λ = 3 W/ ^{o}C.m

Area: A=19.7mm^2

Specific heat: c = 2092 J/Kg.^{o}C

Density: ρ = 2400 Kg/m^3

Thus:

Thermal resistance $R_{grease} = \frac{d}{\lambda \cdot A} = 0.333\ ^{o}\text{C/W}$

Thermal capacitor $C_{grease} = c \cdot \rho \cdot V = 0.002$ J/K

4. Al_2O_3 ceramic 1

Consider that the thickness of the Al_2O_3 is 0.5mm and the thermal conductivity is 26W/^{o}C.m. The 45^{o}C heat spreading angle is assumed in the calculations for this layer.

Thickness: d = 0.5 mm

Thermal conductivity: λ = 26 W/ ^{o}C.m

Area: $A = \frac{19.7 + 29.6}{2} = 24.6$ mm^2

Specific heat: c = 800 J/Kg.^{o}C

Density: ρ = 3985 Kg/m^3

Volume: V= Ax0.5=12.3mm^3

Thus:

Thermal resistance $R_{Al2O3} = \frac{d}{\lambda \cdot A} = 0.7692\ ^{o}\text{C/W}$

Thermal capacitor $C_{Al2O3} = c \cdot \rho \cdot V = 0.03985$ J/K

5. Thermal Grease 2

Consider that the thickness of the thermal grease is 0.02mm and the thermal conductivity is 3 W/^{o}C-m.

Thickness: d = 0.02 mm

Thermal conductivity: λ = 3 W/ ^{o}C-m

Area: A=30mm^2

Specific heat: c = 2092 J/Kg.^{o}C

Density: ρ = 2400 Kg/m^3

Thus:

Thermal resistance $R_{grease} = \frac{d}{\lambda \cdot A} = 0.222\ ^{o}\text{C/W}$

Thermal capacitor $C_{grease} = c \cdot \rho \cdot V = 3.012x10^{-3}$ J/K

6. Al_2O_3 ceramic 2

Consider that the thickness of the Al_2O_3 is 0.5mm and the thermal conductivity is 26 W/^{o}C-m.

Thickness: d = 0.5 mm

Thermal conductivity: λ = 26 W/ ^{o}C-m

Area: $A = \frac{30+42}{2} = 36$ mm^2

Specific heat: c = 800 J/Kg.^{o}C

Density: ρ = 3985 Kg/m^3

Volume: V= (42+30)0.5/2=18 mm^3

Thus:

Thermal resistance: $R_{Al2O3} = \frac{d}{\lambda \cdot A} = 0.5342$ ^{o}C/W

Thermal capacitor: $C_{Al2O3} = c \cdot \rho \cdot V = 0.05738$ J/K

7. Thermal Grease 3

Consider that the thickness of the thermal grease is 0.02mm and the thermal conductivity is 3 W/^{o}C.m.

Thickness: d = 0.02 mm

Thermal conductivity: λ = 3 W/ ^{o}C.m

Area: A=42mm^2

Specific heat: c = 2092 J/Kg.^{o}C

Density: ρ = 2400 Kg/m^3

Thus:

Thermal resistance: $R_{grease} = \frac{d}{\lambda \cdot A} = 0.1587$ ^{o}C/W

Thermal capacitor: $C_{grease} = c \cdot \rho \cdot V = 4.217x10^{-3}$ J/K

8. Al_2O_3 ceramic 3

Consider that the thickness of the Al_2O_3 is 0.5mm and the thermal conductivity is 26 W/^{o}C.m.

Thickness: d = 0.5 mm

Thermal conductivity: λ = 26 W/ ^{o}C.m

Area: $A = \frac{42+56}{2} = 49$ mm^2

Specific heat: c = 800 J/Kg.^{o}C

Density: ρ = 3985 Kg/m^3

Volume: V= (42+56)0.5/2=24.5 mm^3

Thus:

Thermal resistance: $R_{Al2O3} = \frac{d}{\lambda \cdot A} = 0.3925$ ^{o}C/W

Thermal capacitor: $C_{Al2O3} = c \cdot \rho \cdot V = 0.0781$ J/K

9. Thermal Grease 4

Consider that the thickness of the thermal grease is 0.02mm and the thermal conductivity is 3 W/^{o}C.m.

Thickness: d = 0.02 mm

Thermal conductivity: λ = 3 W/ ^{o}C.m

Area: A=49mm^2

Specific heat: c = 2092 J/Kg.^{o}C

Density: ρ = 2400 Kg/m^3

Thus:

Thermal resistance: $R_{grease} = \frac{d}{\lambda \cdot A} = 0.1361$ ^{o}C/W

Thermal capacitor: $C_{grease} = c \cdot \rho \cdot V = 4.92x10^{-3}$ J/K

10. Copper layer

Consider that the thickness of one fillet is 1.65mm and the thermal conductivity is 380 W/^{o}C.m.

Thickness: d = 1.65 mm

Thermal conductivity: λ = 380 W/ ^{o}C.m

Area: A = 12x8 = 96 mm^2

Specific heat: c = 385 J/Kg.^{o}C

Density: ρ = 8900 Kg/m^3

Thus:

Thermal resistance: $R_{Cu} = \frac{d}{\lambda \cdot A} = 4.523x10^{-2}$ °C/W

Thermal capacitor: $C_{Cu} = c \cdot \rho \cdot V = 0.5428$ J/K

11. Thermal Grease 5

Consider that the thickness of the thermal grease is 0.02mm and the thermal conductivity is 3 W/°C.m.

Thickness: d = 0.02 mm

Thermal conductivity: λ = 3 W/ °C.m

Area: A=96mm^2

Specific heat: c = 2092 J/Kg.°C

Density: ρ = 2400 Kg/m^3

Thus:

Thermal resistance: $R_{grease} = \frac{d}{\lambda \cdot A} = 0.0694$ °C/W

Thermal capacitor: $C_{grease} = c \cdot \rho \cdot V = 9.64x10^{-3}$ J/K

12. Kapton

Consider that the thickness of kapton is 0.05mm and the thermal conductivity is 0.37 W/°C.m.

Thickness: d = 0.05 mm

Thermal conductivity: λ = 0.37 W/ °C.m

Area: A = 12x8 = 96 mm^2

Specific heat: c = 1190 J/Kg.°C

Density: ρ = 1420 Kg/m^3

Thus: Thermal resistance: $R_{kapton} = \frac{d}{\lambda \cdot A} = 1.4077$ °C/W

Thermal capacitor: $C_{Cu} = c \cdot \rho \cdot V = 8.111x10^{-3}$ J/K

Appendix III MATLAB Programs

```
clear;
home
load h11v.txt                          %plot the voltage figure

V=h11v;
x=0;
for i=3:7812500-2
    if (V(i)>0.0001) & (V(i-1)<0.0001) & (V(i-2)<0.0001)          % sum
 %      m=V(i+8);
       q=0;
       n=0;
       m=69;
    for c=1:104
        if (V(i+m+c)<1)                    %delete the wrong number
            continue
        elseif(V(i+m+c)>2)
                continue
            end
        q=q+V(i+m+c);                      % get the sum of the voltage
        n=n+1;
    end
    %if (V(i+2+c)>1)
    i
    i+m+c
    n
  %  h=i+3+c;
  %  end
    x=x+1;
    A(x)=x*1e-3-1e-3;
    B(x)=q/n;
   % C(x)=q/n;
    end
end
    plot(A,B)
  % for z=1:x
   %     temp(z)=68.061*B(z)-67.111;
   % end
    %plot(A,C)
    %plot(A,temp)
 %plot(A,temp,'--rs','LineWidth',2,...
    %         'MarkerEdgeColor','k',...
     %    'MarkerFaceColor','g',...
        % 'MarkerSize',10)
  %save('Z:\research\waveform\only wire
bond\total\temp100_230ms.txt','temp','-ASCII')
  %save('Z:\research\waveform\12_19\total\A360ms.txt','A','-ASCII')
```

Appendix IV Fabrication Process and Material Properties

A3.1 Fabrication Process

Cleaning

Type of cleaning: *NaOH (5%): 2 hr; H_2SO_4 (5%): 2 hr; Acetone; air dried*
Full name/information of materials used: *NaOH (5%), H_2SO_4 (5%), Acetone*
Duration of process: *> 4hr*
Temperature: *Room temperature*
Size of substrate: *2''* x *2''*
Drying procedure: *Air dried*

Laser Cutting

Temperature: *Room temperature*
Size of substrate: *2''* x *2''*
Speed and power levels used:
power level at 120W is used for the AlN substrate cutting process. The cutting program requires to be repeated 3 times for a finished substrate, due to the high thermal conductivity of AlN.

Chip Embedding

Full name/information of materials used: *Resbond 919 material from Cotronics Corp.*
Temperature: *Room temperature*
Size of substrate and dies:
Substrate: 2'' x *2''*
SiC die: 1.4mm x 1.4mm

Notes: *The resbond paste is prepared by mixing 10g water and 50g resbond powders. Then the paste is put into the sealing gap between the chip and the AlN carrier carefully. The curing process may take up to 24 hours at room temperature.*

Screen printing

Temperature: *Room temperature*

Full name/information of materials used: *Glass paste 1191Hz from Ferro Corp.*

Glass: 120℃/10min→275℃/15min→390℃/10min; temperature rise: 1℃/min.

Size of substrate: *2''* x *2''*

Sputtering

Vacuum: $< 2 \times 10^{-6}$

Type & Duration of Sputter:

Cr: 30 min

Ni: 30 min

Cr: 30 min

Size of substrate: *2''* x *2''*

Notes: *Before sputtering, surfaces of each module were cleaned.*

Photo resisting:

Duration of process:

Soft bake: 85℃/45min;

Exposure: exposed under ultraviolet light for 20 minutes (exposed part can't be washed by developer);

Developer: the ratio of water and D4000 is 1: 20;

Soak the sample into the developer to wash away the unneeded photo resist for 20 minutes.

Temperature: *Room temperature*

Size of substrate: *2''* x *2''*

Cr Electroplating

Duration of process:

Plating current: 300mA/cm^2

Plating time: 1.5 hr

Temperature: *Room temperature*

Spacing and sizes of materials: *200 mm^2*

Full name/information of materials used: *Chromium crystals from Caswell Corp.*

Size of substrate: *2''* x *2''*

Notes:

The hard plating solution is prepared with 16 fl. Oz of distilled water, 1 kg of chrome crystals (CrO_3) and 10 milliliters of sulfuric acid (98%).

Cu Electroplating

Duration of process:

Plating current: 20mA/cm^2

Plating time: 3 hr

Temperature: *Room temperature*

Spacing and sizes of materials: *200 mm^2*

Full name/information of materials used: *Cu_2SO_4*

Size of substrate: *2''* x *2''*

Etching

Duration of process: *20-30 minutes for each module*

Full name/information of materials used: *Ni and Cr micro-enchants*

Size of substrate: *2''* x *2''*

A3.2 Material Properties

A3.2.1 Glass paste

FERRO
ELECTRONIC MATERIALS

Mems & Sensor Materials

1161HZ
Dielectric

Description: Ferro low temperature compositions are screen printable thick film glass pastes for hermetic sealing of alumina ceramic packages, glass optoelectronic displays and many other sealing applications. The compositions contain glasses, which have very low softening points, in the range of 340-375°C. The low softening points permit using a low peak temperature during glazing and sealing operations. This feature is particularly important in sealing operations involving packages containing thermally sensitive semiconductor devices. The low temperature feature also eliminates bowing of the glass panels during sealing of large area displays.

Ferro's 1161HZ sealing glass features a large particle size for sealing alumina ceramics, such as Cerdip package lids. Offers low alpha emission, good chemical resistance and hermeticity.

Processing Recommendations

Printing: Stainless steel screens with any mesh openings that will accommodate the particle size of the paste may be used. Generally, thick seals will require large screen openings, such as 80 mesh and thin seals will call for similar screen openings such as 200 mesh. Screen emulsion may be varied from about 0.5 mils to 5.0 mils, depending on seal height desired.

Paste Storage & Shelf Life: The paste should be stored in tightly capped containers, in a cool, dry place away from direct sunlight. Properly stored material will have a shelf life in excess of 6 months.

Drying: Wet prints can be dried up to 150°C in a convection or forced-air oven, or in a belt dryer with either conventional or infrared heating.

To better control print definition or slump, slower initial drying at a lower temperature, e.g. 80° to 100°C, is recommended, followed by a period at 150°C to insure complete solvent removal.

Thinning: Thinning is not recommended, since the paste is supplied at the correct viscosity for application. Contact your local Ferro Representative for appropriate solvent details, should thinning become necessary to replace solvent lost through evaporation.

Glaze Cycle: The vehicle in 1161HZ low temperature sealing compositions will be removed during the glaze cycle at about 280°C. The glasses begin to sinter and lose particle identity at about 340°C. To avoid vehicle entrapment, a furnace time-temperature profile should be used that produces a plateau region in the first half of the glaze cycle at about 280°C. This is followed by a temperature increase to 380-400°C, in the last half of the cycle. The actual peak temperature selected depends on substrate mass and final application. Some experimentation in selecting a peak glazing temperature will be required which produces a glaze free of air bubbles and vehicle binder. The peak temperature is not limited to 400°C, or the eventual peak temperature used during the seal cycle; it may be lower or higher.

Rev:1200

FERRO
ELECTRONIC MATERIALS

1161HZ
Dielectric

Seal Cycle: The object during the seal cycle is to simply re-soften the glaze which has been applied to one, or both surfaces to be sealed. This requires a peak temperature, occurring mid-way in the cycle, as low as 400°C. A peak temperature lower than 400°C may be used with some compositions when weights are used to apply pressure. The peak temperature should be held for just a few minutes (2-5), long enough to re-flow the glazed surfaces and accomplish the seal.

Typical Properties	
Typical Uses:	Alumina
Usual Screen Mesh:	80
Peak Glazing Temperature:	380-440°C
Peak Sealing Temperature:	400-420°C
Thermal Expansion Coefficient, ($x10^{-7}$/°C) (20-250°C)	64
Density, grams/cc	5.4
Dilatometer Softening Point	375°C
Alpha-Particle Emission (counts/hour/cm²)	<1
Dielectric Constant (1kHz)	15
Dissipation Factor (% @ 1kHz)	0.7
Volume Resistivity, ohm-cm @ 25°C	$>10^{13}$
Breakdown Voltage DC Volts/mil	>300

A3.2.2 Resbond material

ELECTRICALLY RESISTANT ADHESIVES

Room Temp. Cure - Use to 3000ºF

2800ºF - RESBOND 919

Electrically Resistant Adhesive

Resbond 919 was formulated with the use of Cotronics' proprietary ceramic binders to offer an adhesive with exceptionably high electrical resistance.

These special binders maintain their high electrical resistance and dielectric strength even when exposed to temperatures up to 2800°F.

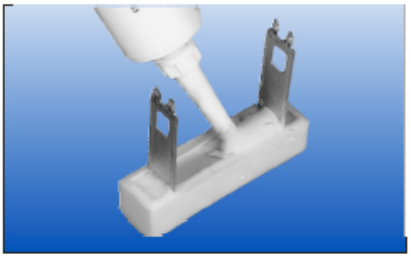
Resbond 919 has a dielectric strength of 270 volts/mil and a Volume Resistivity of 10^{11} ohm-cm (at room temp.).

Just mix the 919 powder to a creamy paste, apply and dry at room temperature.

Users Report:

- Bonds electrode rods into electrically insulating ceramic tubes and protects them from voltage breakdown and corrosive atmospheres.
- Seals light bulb fixtures, insulating them with out cracking when exposed to heat and thermal cycling.
- Forms protective tubes for fiberglass covered extension wires. Protecting against heat and corrosion.

Use Resbond 919 for electrical insulation in potting, sealing, coating, ingnitors, heating coils, instrumentation, thermocouples and in all electrical applications.



Applying 919 to Secure a Hi-Power Resistor

Resbond	919	920
Continous Use Temp. °F	2800	3000
Base	$MgO\text{-}ZrO_2$	Al_2O_3
Form	Paste	Paste
Compressive Strength (psi)	4500	4500
Flexural Strength (psi)	450	450
Thermal Expansion ($x10^{-6}$ /°F)	2.6	4.5
Thermal Conductivity*	4	15
Dielectric Strength (volts / mil)	270	270
Volume Resistivity (ohm cm)	10^{11}	10^{11}
Components	2	2
Color	Tan	White
Consistency	Paste	Paste

*BTU in / Hr °F Ft^2

A3.2.3 Hard chrome plating

PREPARING CASWELL HARD CHROME SOLUTION

Preparation of Solution

To make approx _ gal of CASWELL Hard Chrome Solution:

Add 5.5 US Pints (16 fl oz) of DISTILLED WATER to the tank.

Add 1 can of CASWELL Chrome Crystals to the water. (1kg)

Add 30 milliliters (1 fl oz. or approx 3 teaspoons of BATTERY ACID

To make up larger quantities, multiply the figure accordingly.

Therefore a 4 gallon setup would need 22 pints (4 x 5.5) DISTILLED WATER.

4 cans of CASWELL Chrome Crystals (4 x 1kg)

120 milliliters (4 fl oz or 12 teaspoons) of BATTERY ACID

Evaporation. Water loss by evaporation takes place in the mixed Caswell Hard Chrome solution as a result of contact with the atmosphere. It is recommended that solution level be checked daily and the necessary amount of water added each day to maintain the original level. Daily evaporation loss is small, but may be minimized by keeping the plating tank covered when not in use. To avoid damage to glass heaters, only raise the level when they are cold.

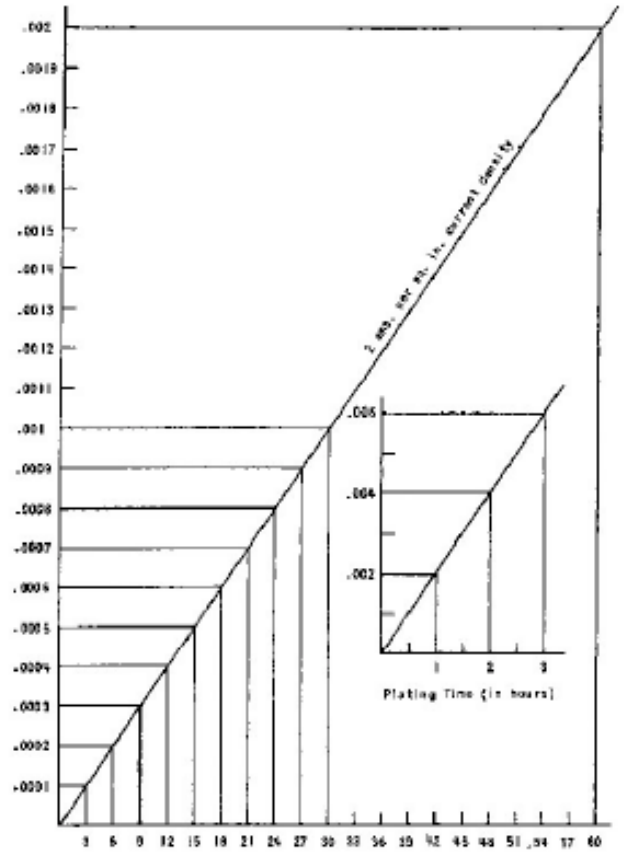
Contamination. Caswell Hard Chrome solution is designed to minimize the effects of contamination. Non-ferrous metals such as brass, bronze, copper and zinc., etc., if allowed to remain in the solution for long periods of time, either being stripped, or not electrically connected may cause contamination of the Caswell Hard Chrome, thereby reducing the efficiency of the solution or shortening its effective life. DO NOT STRIP NON-FERROUS METALS (Brass, copper, bronze, etc.) in Caswell Hard Chrome Solution.

See procedure for cleaning and plating non-ferrous metals.

Your Caswell Chrome setup should be located where atmosphere is free of heavy dust or oil mist. If the solution is covered with an oil film, the oil will tend to cling to the tool or part when. It is immersed into the solution and cause plating failures.

Temperature Caswell Hard Chrome solution is designed for operation at room temperature (65-90F). In cases where the room temperature drops, lowering the temperature of the Caswell Hard Chrome solution to below 65F, the solution must be brought up to plating temperature before use. For optimum results, set your tank heater thermostats to approx 80 F

RATE OF DEPOSITION CHART



Rate of Deposition Chart

Values given are based on the recommended current density of 2 amps per sq. in. Solution temp 80 deg f

fig 3

The Rate of Deposition Chart illustrates the thickness of Chrome plate deposited on the surface of the base metal in any given time, based on the recommended current density of 2 amps. per sq. in. For example, should you want to increase the diameter of a plug gage by 0.001", approximately 15 minutes plating time at the standard current density of 2 amps. per sq. in. would be necessary in order to deposit .0005" on the surface of the plug gage.

In the GENERAL HARD CHROME PLATING INSTRUCTIONS (p 92), notice that an initial plating action (after stripping) is based on a current density of 1 amp. per sq. in., and that the instructions call for this lower current density to be maintained for 1 minute, after which the current density is then increased to the higher rate of 2 amps. per sq. in.

IMPORTANT -

ALL TIMING CALCULATIONS REFERRED TO IN THE RATE OF DEPOSITION CHART ARE BASED ON THE 2 AMP PER SQ.IN.

CURRENT DENSITY AND TIMING REQUIRED FOR THE DESIRED DEPOSIT THICKNESS SHOULD START WHEN THE 2 AMP.PER SQ.IN.CURRENT DENSITY STARTS.

Current Densities

Current density is defined as the amperage (current) applied to one sq. in. of surface to be plated with your setup.

Tools and parts are always plated at the current density of 2 amps. per sq. in. As an example of how to arrive at the proper ammeter reading for tools or parts to be plated, assume a cutting tool with 5 square inches of surface to be plated. During plating, the ammeter would be set to read 10 amps. (After the initial stripping and plating procedure has been followed) the ammeter reading would remain at 10 amps until the desired deposit thickness is attained.

Appendix V Theoretical Calculation for SiC Schottky Junction [50] [51]

Effective Richardson constant: $A := 146 \cdot 10^{4}$ A.m-2.K-2 (4H-SiC)

Boltzmann's constant: $k := 8.617 \cdot 10^{-5}$

Barrier height between the metal and semiconductor: $\Phi_B := 1.1$ ev for Ti/4H-SiC

SiC dielectric constant: $\varepsilon := 9.6$ $\varepsilon o := 8.854 \times 10^{-12}$ F/m

Electron charge: $q := 1.6 \cdot 10^{-19}$ Q

Doping concentration: $Vb := 60$ V

Ideality factor: $n := 1.2$

Thickness of depletion region: $W := 0.24 \cdot 10^{-9}$ m

Drift region doping concentration: $N_d := 7.1 \cdot 10^{18}$ 1/m^3

Barrier lowing effect due to image force lowing:

$$\Delta\phi_b := \sqrt{\frac{q \cdot \sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}}{4 \cdot \pi \cdot (\varepsilon \cdot \varepsilon o)}} \qquad E_m := \sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}$$

Multiplication coefficient
Due to avalanche breakdown:

$$Mn := \frac{1}{1 - 1.52 \cdot \left[1 - e^{\frac{-4.33 \cdot 10^{-24} \left[\sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}\right]^{4.93} \cdot W}{1+n}}\right]}$$

A4.1 Only consider the SiC Schottky junction

Temperature (K): $T := 463$ $T1 := 423$ $T2 := 373$ $T3 := 509$

Current density:

$$J_L(Vr) := -A \cdot T^2 \cdot \left(e^{\frac{-Vr}{k \cdot T}} - 1\right) \cdot e^{\frac{-(\Phi_B)}{k \cdot T}}$$

$$J_{L1}(Vr) := -A \cdot T1^2 \cdot \left(e^{\frac{-Vr}{k \cdot T1}} - 1 \right) \cdot e^{\frac{-(\Phi_B)}{k \cdot T1}}$$

$$J_{L2}(Vr) := -A \cdot T2^2 \cdot \left(e^{\frac{-Vr}{k \cdot T2}} - 1 \right) \cdot e^{\frac{-(\Phi_B)}{k \cdot T2}}$$

$$J_{L3}(Vr) := -A \cdot T3^2 \cdot \left(e^{\frac{-Vr}{k \cdot T3}} - 1 \right) \cdot e^{\frac{-(\Phi_B)}{k \cdot T3}}$$

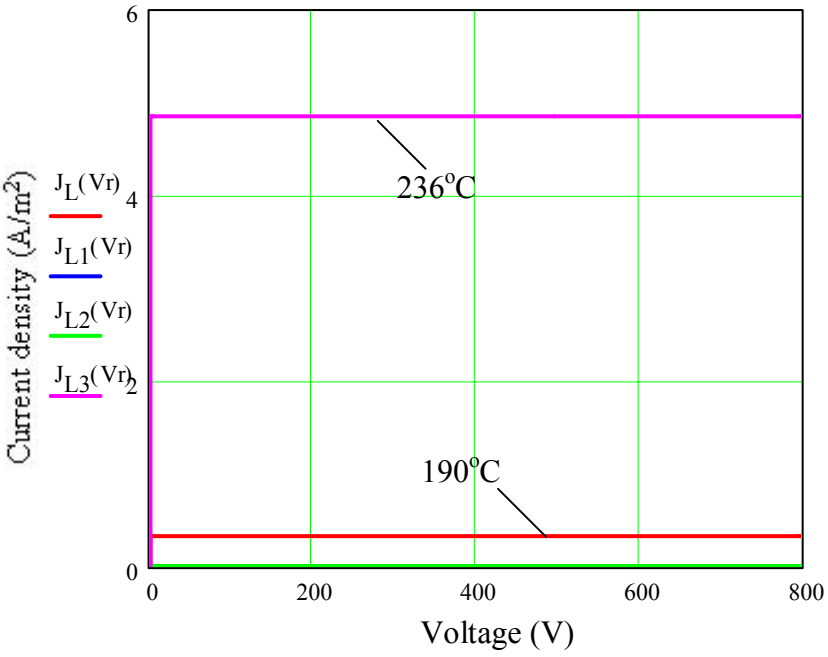


Fig. A4.1 Reverse characteristics without barrier lowing

A4.2 Consider the barrier lowering effect

Current density:

$$J_{L3}(Vr) := -A \cdot T^2 \cdot \left(e^{\frac{-Vr}{k \cdot T}} - 1 \right) \cdot e^{\frac{-\left[\Phi_B - \sqrt{\frac{q \cdot \sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}}{4 \cdot \pi \cdot (\varepsilon \cdot \varepsilon o)}} \right]}{k \cdot T}}$$

$$J_{L1}(Vr) := -A \cdot T1^2 \cdot \left(e^{\frac{-Vr}{k \cdot T1}} - 1 \right) \cdot e^{\frac{-\left[\Phi_B - \sqrt{\frac{q \cdot \sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}}{4 \cdot \pi \cdot (\varepsilon \cdot \varepsilon o)}} \right]}{k \cdot T1}}$$

$$J_{L2}(Vr) := -A \cdot T2^2 \cdot \left(e^{\frac{-Vr}{k \cdot T2}} - 1 \right) \cdot e^{\frac{-\left[\Phi_B - \sqrt{\frac{q \cdot \sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}}{4 \cdot \pi \cdot (\varepsilon \cdot \varepsilon o)}} \right]}{k \cdot T2}}$$

$$J_{L4}(Vr) := -A \cdot T3^2 \cdot \left(e^{\frac{-Vr}{k \cdot T3}} - 1 \right) \cdot e^{\frac{-\left[\Phi_B - \sqrt{\frac{q \cdot \sqrt{\frac{2 \cdot q \cdot N_d}{\varepsilon \cdot \varepsilon o} \cdot (Vr + Vb)}}{4 \cdot \pi \cdot (\varepsilon \cdot \varepsilon o)}} \right]}{k \cdot T3}}$$

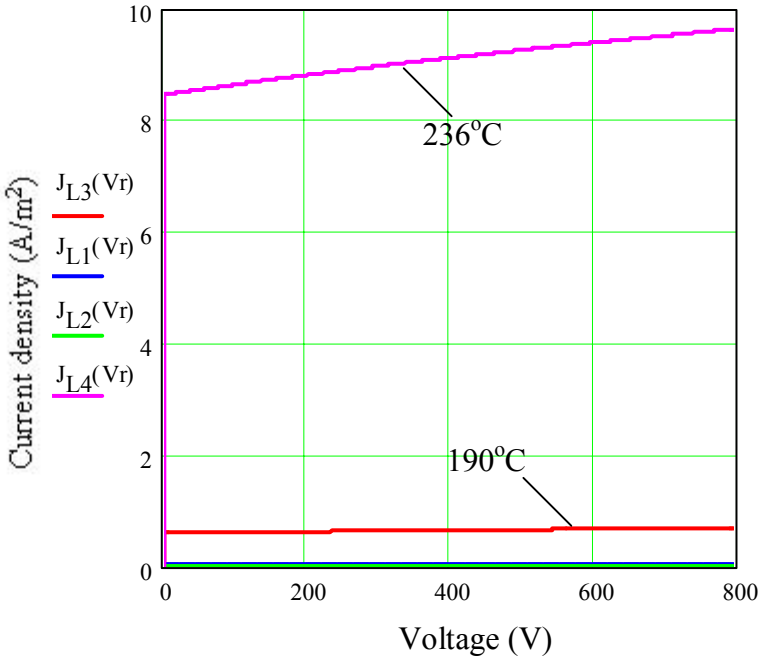


Fig.A4.2 Reverse characteristics with barrier lowing

A4.3 Consider the multiplication coefficient due to avalanche breakdown

Current density:

$$J_{L1}(Vr) := -A\cdot\left[\frac{1}{1-1.52\left[1-e^{\frac{-4.33\cdot10^{-24}\left[\sqrt{\frac{2\cdot q\cdot N_d}{\varepsilon\cdot\varepsilon o}\cdot(Vr+Vb)}\right]^{4.93}\cdot W}{1+n}}\right]}\right]\cdot T1^2\cdot\left(e^{\frac{-Vr}{k\cdot T1}}-1\right)\cdot e^{\frac{-\left[\Phi_B-\sqrt{\frac{q\cdot\sqrt{\frac{2\cdot q\cdot N_d}{\varepsilon\cdot\varepsilon o}\cdot(Vr+Vb)}}{4\cdot\pi\cdot(\varepsilon\cdot\varepsilon o)}}\right]}{k\cdot T1}}$$

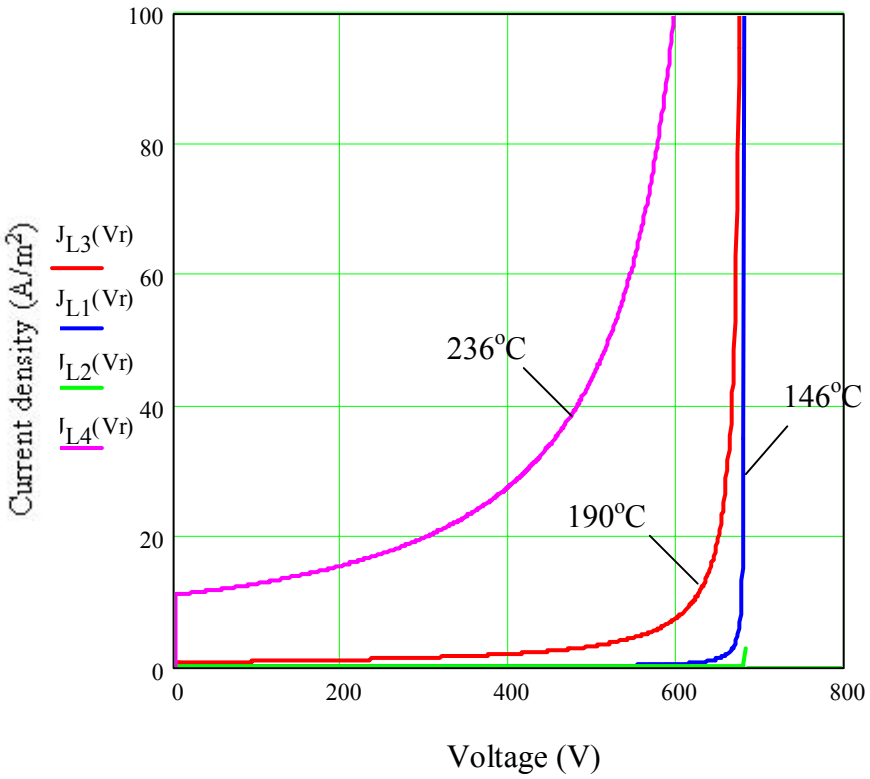


Fig. A4.3 Reverse characteristics with barrier lowing and multiplication

Vita

Jian Yin was born in P.R. China. In September 1998, he received his degree in Bachelor of Science in Electrical Engineering at Nanjing University of Aeronautics and Astronautics (NUAA). And he received his Master of Science in Electrical Engineering in Spring 2001 from NUAA as well. In September 2001, he became a Ph.D student under supervision of Dr. J. D. van Wyk in Blacksburg, Virginia Tech. His research topic focused on the development of high temperature modules for power electronic applications.