A Test Planning System for Functional Validation of VHDL DSP Models

by

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(ABSTRACT)

Validating DSP circuits modeled in VHDL involves generating test data, creating VHDL test benches, and simulating the test benches including models under test (MUTs). This is a laborious and time-consuming process. Therefore, it is desirable to develop a high level approach to automating and planning these tasks.

This dissertation presents a high level test planning system for functional validation of VHDL DSP models. The system requirements parameterized from the specifications constitute the input space and serve as generics of test benches. Library-based test benches are developed using high level design tools. A test planning framework uses a goal tree structure as a vehicle of planning and documenting the testing activities. In a goal tree, test goals are given based on the specifications and test groups are defined to satisfy the test goals. Test groups partially constrain the system requirements and thus partition the input space into smaller and more manageable subspaces. A set of test strategies are then applied to the test groups for efficient test case design. Each test case is mapped to a configuration declaration of the test bench. The test bench is then simulated to generate

test vectors against which the MUT is tested. The MUT response is compared with the gold response by a comparator and verdicts are reached by test oracles. An integrated test planning software system has been developed for test planning and test automation based on this approach. As an illustration of this approach, this dissertation uses the Synthetic Aperture Radar system as a case study. Completeness and effectiveness of the generated test set are evaluated.

This dissertation also discusses approaches to hierarchical faulty module isolation for hierarchical circuits. Exposability is proposed to measure the extent that signal values are revealed to the tester and is used as the cost function for the faulty module search problem. An expanded goal tree which explores the functional and structural aspects of a hierarchical circuit is also presented.