

**ELECTRICAL, THERMAL, AND EMI DESIGNS OF
HIGH-DENSITY, LOW-PROFILE POWER SUPPLIES**

by

Michael Tao Zhang

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy
in
Electrical Engineering

APPROVED:

Fred. C. Lee, Co-Chairman

Milan M. Jovanović, Co-Chairman

Dušan Borojević

Lay N. Chang

Dan Y. Chen

Douglas J. Nelson

February 17, 1997

Blacksburg, Virginia

ELECTRICAL, THERMAL, AND EMI DESIGNS OF HIGH-DENSITY, LOW-PROFILE POWER SUPPLIES

by

Michael Tao Zhang

Fred. C. Lee, Co-Chairman

Milan M. Jovanović, Co-Chairman

Electrical Engineering

(ABSTRACT)

This work presents the analyses and designs of high-density, low-profile power supplies, including the electrical, thermal, and EMI aspects. Emphasis is placed on forward and flyback converters.

The efficiency improvements of employing synchronous rectification are theoretically derived and experimentally verified in forward and flyback converters. The performances of synchronous rectifiers in forward converters are analyzed with regards to transformer reset and SR driven method. The effectiveness of synchronous rectification in flyback converters is evaluated in various operation modes and control schemes. The paralleling techniques utilized to realize high-density, low-profile power conversion are presented. Current sharing in transformer paralleling is addressed and evaluated in forward topology. The performance and the operation principles of one-choke and two-choke interleaved forward converters are analyzed.

The thermal management of high-density power supplies in sealed enclosures is optimized using computational fluid dynamics simulations. The theoretical limit of power density

due to thermal constraint is determined. In addition, the thermal-design optimization guidelines are given and verified experimentally.

A systematic methodology is developed to facilitate the analysis and design of conducted EMI problems in high-density power supplies. Partial element equivalent circuit method is employed for parasitic parameter extraction. Layout and packaging are optimized to minimize conducted EMI noises. Noise predictions by Saber simulations are confirmed by experimental measurements.

To my wife

Lily

ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my advisors, Dr. Fred C. Lee and Dr. Milan M. Jovanović, for their guidance, encouragement, and continuous support through the course of this work. The extensive knowledge, vision, and creative thinking of Dr. Lee have been the source of inspiration for me throughout this work. Many detailed and in-depth discussions with Dr. Jovanović have invaluable shaped the course of this work.

I am very grateful to my doctoral committee members, Dr. Dušan Borojević for many helpful suggestions, Dr. Lay N. Chang for introducing me to the power electronics field, Dr. Dan Y. Chen for his constant encouragement, and Dr. Douglas J. Nelson for his help in the thermal designs.

It has been a great pleasure associating with the excellent faculty, staff, and students at the Virginia Power Electronics Center. The friendships, enlightening discussions, and the overall atmosphere center spirit have made my stay at VPEC pleasant and enjoyable. Special thanks are due to my fellow students Dr. Guichao Hua, Mr. Wei Chen, Dr. Ning Dai, Dr. Yiming Jiang, Mrs. Qiong Li, Dr. Glenn Skutt, Mr. Richard Zhang, and Mr. Wilson Zhou.

I am especially indebted to the members of Delta Power Electronics Lab for their support over the years. I would like to thank Mr. David Crow, Dr. Laszlo Huber, and Dr. Yungtaek Jang, for their help.

My heartfelt appreciation goes toward my parents, Ji-Sui Zhang and San-Nan Sun, for their love and support in my pursuing higher education.

Finally I would like to thank my wife, Lily, for her love, understanding, support, and sacrifice during the course of my Ph.D. study.

This work was supported under Delta fellowship, provided by Delta Electronic Ind. Co., Ltd., Taiwan.

TABLE OF CONTENTS

1. INTRODUCTION	1
1.1. Background.....	1
1.2. Objectives and Dissertation Outline	6
1.2.1. Synchronous Rectification	7
1.2.2. Paralleling Techniques	7
1.2.3. Thermal Management and Packaging Considerations.....	8
1.2.4. Minimization of Conducted EMI.....	8
1.2.5. Conclusions and Concurrent Design Concept.....	8
2. SYNCHRONOUS RECTIFICATION	9
2.1. Synchronous Rectification in Forward Converter.....	11
2.1.1. Synchronous Rectifier Implementations	12
A. Forward Converter with RCD Clamp and Self-Driven SRs	12
B. Forward Converter with Active Clamp and Self-Driven SRs	16
C. Forward Converter with Control-Driven SRs.....	19
2.1.2. Efficiency Limits of Synchronous Rectification.....	21
2.1.3. Evaluation Results.....	27
2.1.4. Summary	40

2.2. Synchronous Rectification in Flyback Converter.....	41
2.2.1. Synchronous Rectifier Implementations	43
A. Constant-Frequency (CF) Continuous-Conduction-Mode (CCM)	45
B. CF Discontinuous-Conduction-Mode (DCM).....	47
C. Variable-Frequency (VF) DCM.....	50
D. VF Zero-Voltage-Switched (ZVS) DCM	52
2.2.2. Efficiency Limit of Synchronous Rectification.....	54
2.2.3. Evaluation Results.....	59
A. CF CCM.....	60
B. CF DCM.....	64
C. VF DCM and ZVS DCM	67
2.3. Summary.....	72
3. PARALLELING TECHNIQUES	73
3.1. Transformer Paralleling	75
3.1.1. Direct Paralleling	75
3.1.2. Paralleling With Separate Forward Diodes.....	78
3.1.3. Paralleling with Common Heat Sink.....	81
3.1.4. Experimental Evaluations.....	86
3.2. Interleaved Converters	89

3.2.1. Analysis of Operation of Interleaved Forward Converters.....	91
A. Two-Choke Approach.....	91
B. One-Choke Approach.....	91
3.2.2. Component Size and Loss Comparisons	100
A. Magnetic Component Size Comparisons	100
B. Loss Comparisons	103
3.3. Experimental Evaluations	105
3.4. Summary.....	112
4. THERMAL MANAGEMENT AND PACKAGING CONSIDERATIONS.....	114
4.1. Power Density Limits.....	117
4.2. Loss Distribution Analysis - Example : Flyback Adapter.....	124
4.3. Component Selection, Packaging, and Thermal Management - Example: Flyback Adapter	129
4.4. Summary.....	144
5. MINIMIZATION OF CONDUCTED EMI.....	146
5.1. Parasitic Parameter Extraction - Example: Flyback Adapter	147
5.1.1. Layout Inductance Calculation	148
5.1.2. Packaging Capacitance Calculation	152
5.2. Circuit Modeling and EMI Analysis - Example: Flyback Adapter.....	153

5.2.1. Power Transformer Modeling	153
5.2.2. Modeling of LISN	154
5.2.3. EMI Analysis.....	158
5.3. EMI Noise Suppression - Example: Flyback Adapter	160
5.3.1. Layout Improvement	160
5.3.2. Input Filter Design	164
5.4. Performance Evaluation and Experimental Verification - Example: Flyback Adapter	168
5.5. Summary.....	171
6. CONCLUSIONS AND FUTURE WORK	173
References	177
Appendices	185
I. Dynamic Current Sharing for Paralleled Transformers.....	185
II. Electro-Thermal Analysis of Current Sharing	191
III. Partial Element Equivalent Circuit Method.....	195
Vita.....	198

LIST OF ILLUSTRATIONS

Figure 1.1. Important design aspects of high-density, low-profile power supplies.....	3
Figure 2.1. Forward voltage comparison between synchronous rectifier and diode rectifier.....	10
Figure 2.2. Forward converter with RCD clamp and self-driven SRs	13
Figure 2.3. Forward converter with active-clamp and self-driven SRs	17
Figure 2.4. Forward converter with control-driven SRs	20
Figure 2.5. Efficiency limits of forward converter with self-driven SRs and active-clamp reset and control-driven SRs with small gate-drive timing delay and magnetizing current.....	26
Figure 2.6. Efficiency limits of forward converter with self-driven SRs and RCD-clamp reset for $D_{dead} = 0.2$	28
Figure 2.7. Measured efficiencies of forward-converter power stage with self-driven SRs	30
Figure 2.8. Measured and calculated efficiencies of forward-converter power stage with RCD-clamp reset and control-driven SRs for $T_{delay} = 0.25 \mu s$	33
Figure 2.9. Oscillogram of key voltage waveforms of forward converter with RCD-clamp and control-driven SRs	35
Figure 2.10. Blown-up voltage waveforms from Fig. 2.9 during dead time	36
Figure 2.11. Measured efficiencies of forward converter power stage with RCD-clamp reset and control-driven SRs with different delay times.....	39
Figure 2.12. Synchronous rectifier in flyback converter used as post regulator in multiple- output applications.....	42
Figure 2.13. Flyback converter with synchronous rectifier	44
Figure 2.14. Key waveforms of CF CCM flyback converter with SR	46
Figure 2.15. Key waveforms of CF DCM flyback converter with SR.....	48
Figure 2.16. Key waveforms of VF DCM flyback converter with SR.....	51
Figure 2.17. Key waveforms of VF ZVS DCM flyback converter with SR	53

Figure 2.18. Theoretical efficiency estimates.....	58
Figure 2.19. Control and drive circuit for VF DCM flyback converter with SR	61
Figure 2.20. Measured efficiencies of CF CCM implementation with SR and Schottkies rectifier at full power	62
Figure 2.21. SR turn-off waveforms of CF CCM converter with SR	63
Figure 2.22. Measured waveforms of CF DCM converter with SR at $V_{in} = 250$ Vdc.....	65
Figure 2.23. Measured efficiency of CF DCM implementation with SR and Schottky at full power	66
Figure 2.24. Measured waveforms at $V_{in} = 250$ Vdc, $V_o = 15$ V, $I_o = 2.4$ A.....	68
Figure 2.25. Measured efficiencies of VF DCM implementations with SR and Schottky, and ZVS-DCM implementation at full power	69
Figure 2.26. Switching frequency comparison of VF DCM implementations with SR and Schottky, and ZVS-DCM implementation.....	71
Figure 3.1. Direct transformer paralleling	76
Figure 3.2. Equivalent circuit and key waveforms of direct transformer paralleling.....	77
Figure 3.3. Transformer paralleling using separate forward diodes	79
Figure 3.4. Equivalent circuit and key waveforms of transformer paralleling with separate forward diodes.....	80
Figure 3.5. Thermal equivalent circuit for two diodes in parallel	83
Figure 3.6. Current unbalance as a function of device deviation d and thermal coupling resistance R_c (and spacing, d , between two diodes).....	84
Figure 3.7. Four experimented configurations for current sharing measurement.....	87
Figure 3.8. Interleaving implementations.....	90
Figure 3.9. Key waveforms of two-choke interleaved forward converter	92
Figure 3.10. One-choke interleaved forward converter.....	93
Figure 3.11. Key waveforms of one-choke interleaved forward converter.....	94
Figure 3.12. Equivalent topological stages.....	96

Figure 3.13. Experimental $V_{DS(Q1)}$ and $V_{DS(Q2)}$ waveforms of two-choke implementation for $V_{IN} = 50$ V	108
Figure 3.14. Experimental $V_{DS(Q1)}$ and $V_{DS(Q2)}$ waveforms of one-choke implementation for $V_{IN} = 50$ V	109
Figure 3.15. Measured full-load efficiencies of one-choke and two-choke implementations as functions of input voltage	110
Figure 4.1. Importance of thermal management	115
Figure 4.2. Permissible power dissipation for enclosure of given volume ($V = 10$ in ³) as a function of the aspect ratio w/l and h/l as a parameter	120
Figure 4.3. Maximum achievable power as a function of enclosure volume and its cross-sectional aspect ratio w/h	123
Figure 4.4. Mechanical design and placement of key components in packaging design ❶	126
Figure 4.5. Efficiency and total internal power loss of flyback adapter	127
Figure 4.6. Calculated adapter power-loss breakdown at 90 Vac	128
Figure 4.7. Simulation and experimental results of transformer temperatures with different rubber arrangements and different MOSFET case styles	130
Figure 4.8. Two package styles used to evaluate thermal behavior of primary MOSFET	132
Figure 4.9. Simulation and experimental results of semiconductor junction temperatures with different thermal rubber arrangements and different MOSFET case styles	134
Figure 4.10. Temperature maps of top surface of adapter	135
Figure 4.11. Transformer core shapes	137
Figure 4.12 Mechanical design and placement of key components in packaging design ❷	138
Figure 4.13. Mechanical design and placement of key components in packaging design ❸	140
Figure 4.14. Comparisons of temperatures of critical components for three packaging designs for $T_{amb} = 40$ °C	141
Figure 4.15. Temperature map of top surface in packaging design ❹	143
Figure 5.1. PCB layout of flyback converter	150

Figure 5.2. Equivalent circuit of parasitic elements in layout and packaging	151
Figure 5.3. Reduced equivalent circuit of power transformer	155
Figure 5.4. Comparison of power transformer impedance measurement and modeling	156
Figure 5.5. Circuit diagram of LISN.....	157
Figure 5.6. Simulated conducted EMI noises at $V_{in} = 265$ Vac.	159
Figure 5.7. Improved PCB layout of flyback converter.....	161
Figure 5.8. Simulated conducted EMI noises for improve layout and packaging at $V_{in} = 265$ Vac.	163
Figure 5.9. Comparison of common-mode choke (L_1) impedance measurement and modeling	165
Figure 5.10. Comparison of common-mode choke (L_2) impedance measurement and modeling	166
Figure 5.11. Attenuation of designed EMI filter.....	167
Figure 5.12. Simulated conducted EMI noises at $V_{in} = 265$ Vac	169
Figure 5.13. Measured conducted EMI noises at $V_{in} = 265$ Vac.....	170
Figure 5.14. Flow chart of conducted EMI analysis.	172
Figure 6.1 A concurrent approach for high-density power supply design	175
Figure III.1. A rectangular shaped loop described with PEEC method.....	196

LIST OF TABLES

Table 2-I. Power loss comparisons of flyback converters with diode (DR) rectifier and synchronous rectifier (SR)	55
Table 3-I. Parameters and current sharing in four tested configurations.....	88
Table 3-II. Component list of power stages of two-choke and one-choke implementations.....	106
Table 4-I. Comparison of analytically and numerically calculated permissible power dissipation for an enclosure with volume of $V = 10 \text{ in}^3$	122