Residual Stress Effects on Power Slump and Wafer Breakage in GaAs MESFETs

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(ABSTRACT)

The objectives of this investigation are to develop a precise, non-destructive single crystal stress measurement technique, develop a model to explain the phenomenon known as “power slump”, and investigate the role of device processing on wafer breakage. All three objectives were successfully met.

The single crystal stress technique uses a least squares analysis of X-ray diffraction data to calculate the full stress tensor. In this way, precise non-destructive stress measurements can be made with known error bars. Rocking curve analysis, stress gradient corrections, and a data reliability technique were implemented to ensure that the stress data are correct.

A theory was developed to explain “power slump”, which is a rapid decrease in the amplifying properties of microwave amplifier circuits during operation. The model explains that for the particular geometry and bias configuration of the devices studied in this research, power slump is linearly related to shear stress at values of less than 90 MPa. The microscopic explanation of power slump is that radiation enhanced dislocation glide increases the kink concentration, thereby increasing the generation center concentration in the active region of the device. These generation centers increase the total gate current, leading to a decrease in the amplifying properties of the device.

Passivation layer processing has been shown to both reduce the fracture strength and increase the residual stress in GaAs wafers, making them more susceptible to wafer breakage. Bare wafers are found to have higher fracture strength than passivated wafers. Bare wafers are also found to contain less residual stress than SiON passivated wafers, which, in turn, are found to have less stress than SiN passivated wafers. Topographic imaging suggests that SiN passivated wafers have larger flaws than SiON passivated wafers, and that the distribution of flaw size among SiN passivated wafers is wider than the distribution of flaws in SiON passivated wafers. These flaws are believed to lead to breakage of the device during processing, resulting in low fabrication yield.

Both the power slump model and the wafer breakage data show that these phenomena are dependent on residual stress developed in the substrate during device fabrication. Reduction of process-induced residual stress should therefore simultaneously decrease wafer breakage rates and reduce power slump during device fabrication and operation.

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Chapter 1
Introduction

In the last several years, GaAs device processing technology has become competitive with silicon technology in many areas of microelectronic fabrication. Although GaAs technology does not currently match the miniaturization scale attainable with silicon, the inherent advantages of higher mobility make GaAs the preferred choice for building high frequency devices, such as those used in the microwave communications industry. Whether the application is high-speed logic, microwave signal amplification, or high-speed analogue detection, the vast majority of GaAs ICs use metal-semiconductor field effect transistors (MESFETs) as the active elements of the circuit.

The devices under study in this investigation are MESFETs configured as microwave power amplifiers. These ICs are used in such devices as cellular telephones and satellite transponders, both of which require long-term, reliable power amplification. As the demand for higher operational frequencies at higher output power increases, the technological challenge of producing higher performance microwave amplifiers at a low cost must be met.

1-1 STATEMENT OF THE PROBLEM

Two problems are addressed in this research; power slump and wafer breakage. Power slump affects device lifetime and reliability, while wafer breakage affects fabrication yield, and therefore, device cost.

POWER SLUMP

GaAs MESFET microwave amplifiers produced at ITT-GTC in Roanoke, Virginia experience a rapid decrease in the output power of the device at high bias voltages. The high bias voltages are required to attain the power output desired from the chip, but the degradation experienced under such bias conditions renders the devices useless after a few days of operation. This degradation is known as "power slump" and is an industry-wide problem.

WAFER BREAKAGE

Fabrication yield is a dominant factor in the ultimate cost of the device, and wafer breakage is a major contributor to low fabrication yield. Wafer breakage occurs when the sum of the applied and residual stresses exceeds the fracture strength of the material. High residual process-induced stress may be partially responsible for high wafer breakage rates and will be addressed in this research.

1-2 OBJECTIVES OF THE RESEARCH

The objectives of this research are as follows:

1. Develop methods to measure single crystal stress in GaAs wafers and devices,
2. Develop a model to explain the power slump phenomenon, and
3. Investigate the role of process-induced stress on wafer breakage.

A successful outcome of the first objective will give the entire semiconductor industry a new tool to investigate the effects of stress on single crystal materials. There is growing demand for such capability, since the effects of mechanical stress on device performance and yield become more pronounced as devices are fabricated at the submicron scale.

A successful outcome of the second objective will give the III-V semiconductor industry an explanation of a phenomenon which currently has no comprehensive explanation. A model of power slump would provide guidance in developing improved device, material, and fabrication designs, and perhaps ultimately lead to development of low cost devices operating at frequencies and power outputs not currently obtainable.

A successful outcome of the third objective will allow manufacturers of any types of devices, including GaAs MESFETs, a better understanding of how process-induced stress affects wafer breakage. By identifying those processes which contribute to wafer breakage, improved methodologies may be developed to maximize fabrication yield, ultimately leading to reduced product cost.

1-3 SCOPE OF THE RESEARCH

This research will develop non-destructive methods of precisely measuring stress in single crystal materials. More specifically, methods to measure both macrostress and film-edge stress will be developed. Computer models and X-ray topographic imaging will be used to verify the stress measurement techniques, and methods will be developed to assure data reliability and correct for the effects of stress gradients on macrostress data.

A model to explain the power slump will be developed. This model will explain how residual stress and high bias voltage contribute to device performance degradation, and will at least qualitatively, predict the degree and conditions of power slump for various operating conditions and stress states. It is beyond the scope of this investigation to actually produce devices which do not power slump, or exhibit reduced power slump, as such an undertaking would be prohibitively expensive, given the many factors which must be controlled to produce such devices[*]. However, recommendations for improved device and materials design will be developed.

Data concerning wafer breakage as a function of process-induced stress will be collected. These data will be interpreted in the context of the conclusions of the single crystal stress investigation. Crack nucleation points will be identified, fabrication steps which contribute to wafer breakage will be identified, and suggestions to reduce process-induced wafer breakage will be made. It is beyond the scope of this study to optimize the fabrication process, as this would be prohibitively expensive and time consuming. As will be shown, optimization of the fabrication process is expected to both reduce power slump and wafer breakage by reducing a common contributor to both problems - residual stress.

[*] As will be shown, an extensive design of experiment (DOE) must be implemented to actually produce non-slumping or reduced slumping devices.

Chapter 2
MESFET Device Physics

This chapter presents basic concepts of metal semiconductor field effect transistor (MESFET) device physics and the general layout of the devices under investigation in this research. Also included in this chapter is a description of the power slump phenomenon and the derivation of equations that describe the electronic nature of the power slump.

2-1 MESFET BASICS

GaAs MESFETs are used as the active component of the microwave power amplifiers studied in this investigation. High frequency devices, such as microwave amplifiers, require a material that has a very high electron mobility so that the electronic carriers can propagate the signal. GaAs is such a material, and is therefore used for the active region of the device. Compared to silicon[*], GaAs is more brittle and more susceptible to defect formation during the crystal growing process, which has important ramifications with regard to device degradation and fabrication yield, as will be shown.

Several terms used throughout this document are defined in Table 2-1.

[*] The overwhelming majority of microelectronic devices use either silicon or GaAs technology, with far more silicon devices produced than GaAs devices. The comparison to silicon is made to keep the reader who is familiar with silicon technology mindful of the differences between silicon and GaAs materials properties.

Table 2-1: Definitions of terms used in this document.

Term	Meaning in this document
Active region of the device	The region of a MESFET that includes the depletion region and the channel.
The depletion region	The region depleted of carriers under the gate.
The "channel"	The region through which current flows.
The "device"	An individual MESFET.
FET	FET and MESFET will be used interchangeably.
The "amplifier"	The complete circuit, including 8 FETS and other structures on the chip.
Chip	The circuit and the substrate on which the circuit is built.
Die	An unmounted chip.
Wafer	The GaAs substrate on which devices are fabricated. After fabrication, the wafer is cut into die.

MESFET FABRICATION

The basic steps of MESFET fabrication are shown in Figure 2-1. The first step is to deposit a layer of SiON by plasma enhanced chemical vapor deposition (PECVD). This layer minimizes surface damage during ion implantation and acts as an anneal

cap during annealing (arsenic would diffuse out of the GaAs surface layers if no anneal cap was present).

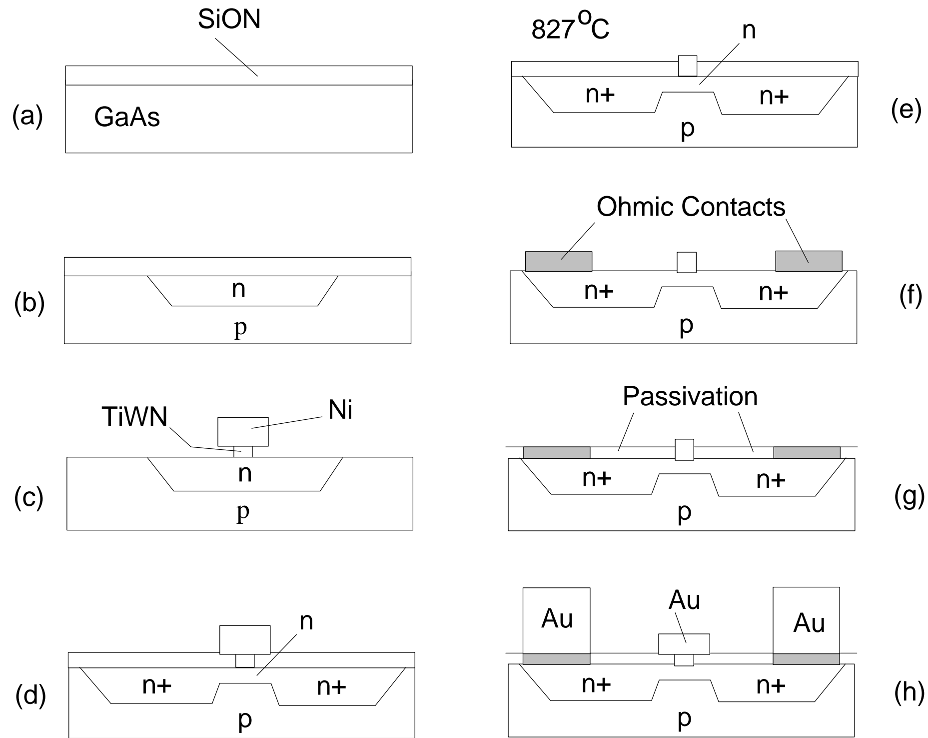

Figure 2-1: Steps in MESFET fabrication

Second, Mg and Si are co-implanted to form a deep p-type layer and a shallow n-type layer, respectively. The n-type layer will ultimately serve as the channel of the device and the p-type layer will more precisely define the bottom of the channel and provide electrical isolation from adjacent devices. Third, the anneal cap is removed and a TiWN layer is sputtered onto the bare GaAs to form a Schottky contact. An over-layer of nickel is deposited and serves to pattern the TiWN layer. The T-gate structure (refer to Figure 2-1 (c)) is formed by selective etching. Fourth, photoresist is patterned onto the wafer and the Si implant is repeated, forming two separate highly conductive

regions in the channel, where later the source and drain will be located. The photoresist and nickel layers are stripped and SiON is again deposited. Fifth, the wafer is annealed to electrically activate the implanted ions. In the devices under study, the wafers were furnace annealed to 827°C. The current process uses rapid thermal annealing (RTA) at 925°C to activate the implants. Sixth, the SiON anneal cap is removed and ohmic metal is sputtered to form the source and drain contacts. Seventh, a SiN passivation layer is deposited by PECVD and etched to expose the metallization tracks, gate metal, and source and drain ohmic contacts. The passivation layer provides electrical isolation between the gate, source, and drain, prevents electromigration of metallic ions across the GaAs surface, and protects the device from environmental degradation (moisture, salt, etc.). Finally, gold is plated to form the metallization interconnection layer and the entire device is passivated with SiN.

In the devices under study, additional processing is performed on the backside of the wafer. First, the wafer is mounted on a sapphire carrier using wax. Wax is used so that the wafer can be easily removed after backside processing is complete. Second, the wafer is thinned to 125 μm by mechanical grinding and polishing to improve heat transfer out of the substrate during device operation. Third, vias are etched through the substrate to connect the source contact pads on the front-side of the wafer (the top) to the backside of the wafer (the bottom). In this way, the heat sink on which the die will be mounted can also act as the grounding plane for the source, eliminating the need for wire bonding on the front side source contacts. Fourth, a titanium adhesion layer and a plated gold layer are deposited on the backside of the wafer and the wafer is removed from the carrier.

The wafer is then mounted onto tape, scribed and broken into dice. Each die is attached to a brass heat sink (or carrier) using an indium based solder. The devices in this study were mounted on the carrier manually using a hot stage. Lifetesting was

then performed in an environmental chamber. (The gate and drain contacts would normally be wire bonded and the device is hermetically sealed. The devices studied in this work did not undergo final packaging.)

MESFET GEOMETRY and DEVICE OPERATION

During depletion-mode operation[†], a positive voltage is applied at the drain contact, a negative voltage is applied at the gate contact, and the source contact is grounded (see Figure 2-2 and Figure 2-3). This biasing configuration causes the majority carrier

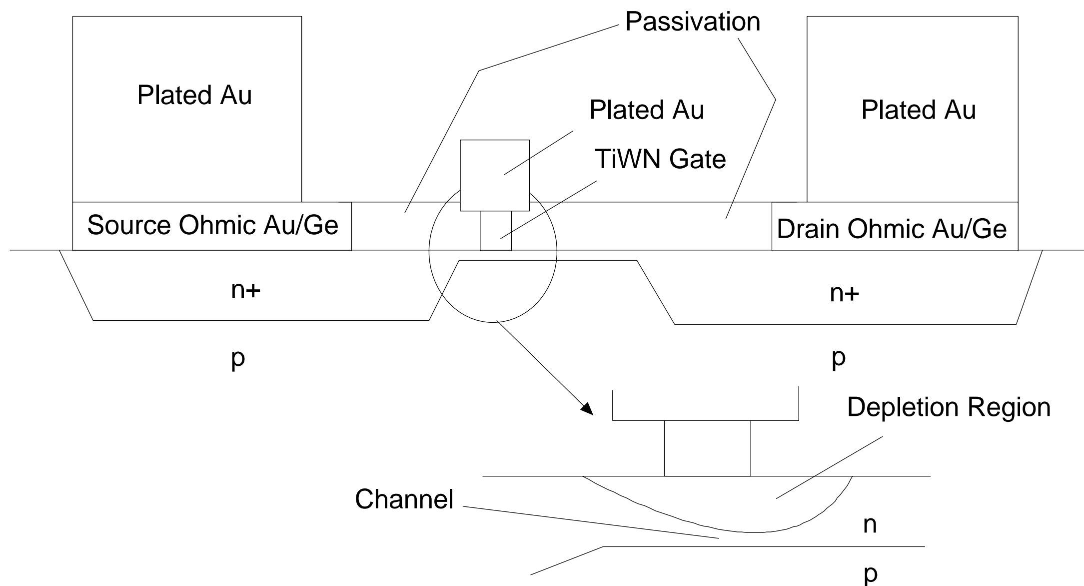

Figure 2-2: Cross-sectional view of a MESFET.

[†] "Depletion mode" refers to the manner in which the drain current is modulated. In depletion mode, the channel is open when the gate voltage is zero and narrows as the negative gate bias is increased. (As opposed to enhancement mode in which the channel is initially closed and positive gate bias opens it.)

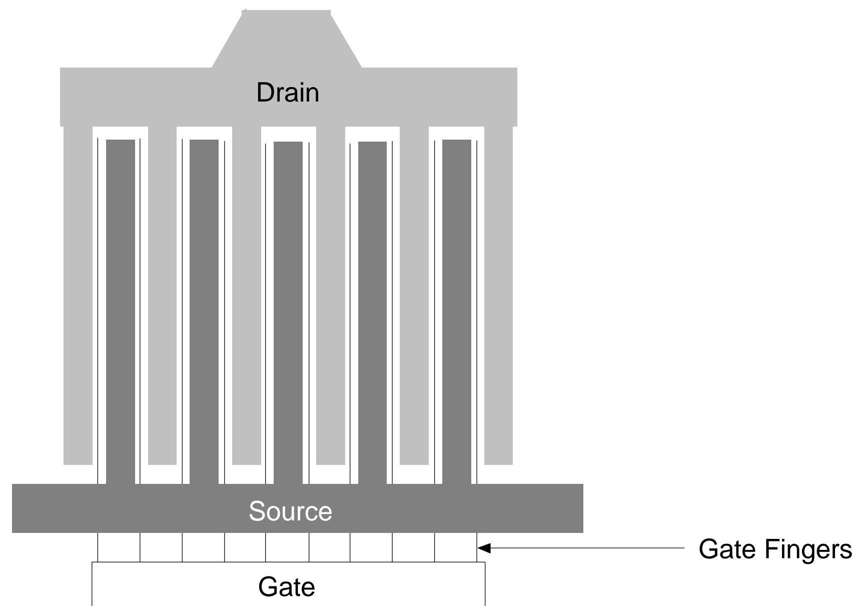

Figure 2-3: Top view of a MESFET. This device represents one of eight FETs on the amplifier.

(electrons in an n-type device) to flow from the source to the drain. The refractory TiWN alloy, which serves as the gate contact, forms a Schottky barrier at the metal/semiconductor junction. The depletion region formed in the semiconductor by the metal/semiconductor junction narrows the channel when negative bias is applied to the gate.

2-2 SCHOTTKY BARRIER GATE CONTACT

The Schottky barrier formed at the junction between the gate metal and GaAs is associated with a depletion region in the semiconducting material. The negative voltage applied at the gate reverse-biases the gate contact, increasing the size of the depletion region. As the depletion region under the gate increases, the width of the conducting channel decreases, confining the current flowing from the source to the drain to a smaller cross-sectional area. In this way, drain current can be modulated by

an applied gate signal, which is the basis for amplification in this device. The DC power gain is described by

Equation 2-1

$$G = \frac{V_D \cdot I_D}{V_G \cdot I_G}$$

where V_D and V_G are the drain and gate voltages and I_D and I_G are the drain and gate currents. For the devices studied in this research, V_D and V_G are fixed bias values (with a superimposed signal on the gate bias during AC operation).

The MESFET's refractory gate allows a small, but significant gate current to flow through the depletion region under reverse bias. This current, which is formed by thermionic emission over the Schottky barrier, acts to decrease the power output of the device, as is evident by Equation 2-1. The total current flowing through the depletion region under the gate is determined by the sum of the thermionic emission current and the generation current in the depletion region, as shown in Equation 2-2 [1].

Equation 2-2

$$I_G = ZLA^{**}T^2e^{-q\Phi/kT} + I_{gen}$$

where Z is the gate width, L is the gate length, ϕ is the potential barrier height, and I_{gen} is the generation current in the depletion region. A^{**} is the modified effective Richardson's constant, given by Equation 2-3 [2].

Equation 2-3

$$A^{**} = Am^{*}/m_o \frac{f_p \cdot f_Q}{1 + f_p \cdot f_Q \cdot \frac{v_R}{v_D}}$$

where, A is the Richardson-Dushman constant for a free electron (120 A/cm^2K^2), m^* is the effective mass of an electron in the conduction band, m_o is the free-electron mass, f_p is the probability that an electron will be backscattered over the barrier by optical phonon scattering, f_Q is a factor related to quantum mechanical reflection of electrons at the junction, v_R is the recombination velocity in the semiconductor side of the contact, and v_D is the diffusion velocity. Under high electric fields, such as those experienced in the gate region during device operation (>10^4 V/cm), A^{**} has been determined [2] experimentally to be 144 A/cm^2K^2.

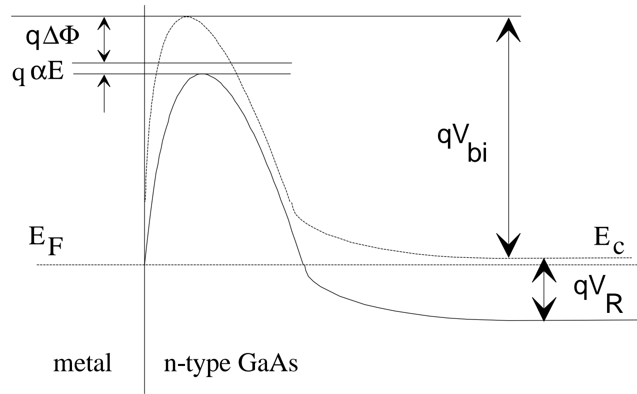

Figure 2-4: Band diagram of a Schottky barrier. Band bending near the metal-semiconductor interface is due to the combined effects of the applied field and image charge formation.

The potential barrier of Equation 2-2 is given by Equation 2-4 [1],

Equation 2-4

$$\Phi = qV_{bi} - \Delta\Phi - \alpha E,$$

where $\Delta\Phi$ is the decrease in the barrier height due to image force effects (refer to Figure 2-4), α is an empirical factor related to the quantum mechanical effects of the wave functions in the metal (approximately 0.2 nm for TiWN on GaAs), E is the applied electric field, and V_{bi} is the built-in potential of the Schottky barrier given by Equation 2-5 (assuming n-type GaAs),

Equation 2-5

$$V_{bi} = \frac{kT}{q} \cdot \ln\left(\frac{N_D}{n_i}\right)$$

where N_D is the donor concentration and n_i is the intrinsic carrier concentration. For the devices under investigation, $N_D = 5 \text{ X } 10^{17}$ /cc, $n_i = 9.98 \text{ X } 10^{7}$ /cc, and $V_{bi} = 0.67$ V at
T = 75°C.

The decrease in the potential barrier due to the image force (see Equation 2-4) is caused by the formation of a positive charge on the metal surface, induced by the proximity of the electric field from the approaching electron. The resulting attractive force lowers the potential barrier by an amount [2]

Equation 2-6

$$\Delta\phi = \sqrt{\frac{q \cdot E}{4 \cdot \pi \cdot \varepsilon_r \cdot \varepsilon_o}}$$

where E is the applied electric field, ε_r is the relative permittivity (13.1 for GaAs), and ε_o is the permittivity of free space. As an example, for V_{DG} = 24 V, E = 1.6 x 10^6 V/cm, and $\Delta\phi$ = 0.133 eV, which represents an appreciable change in the barrier height.

The thermionic current under low field operation is calculated to be 6.7 nA, which is consistent with measured values of gate current under low-field conditions. At an operating field of 1.2 x 10^6 V/cm (V_{DG} = 18 V), the thermionic current is calculated to be 320 nA. This value is much smaller than measured values, which show the reverse gate current (high field) to be between 1000 and 2000 μA at V_{DG} = 18 V. Deviations between the measured and calculated values are likely due to the degree of perfection of the metal-semiconductor interface, as evidenced by the significant variability in the measured values of the gate current, and the magnitude of the generation current in the depletion region due to electrically active defects.

As the drain voltage is increased beyond 18 V, the measured increase in the gate current does not match the increase in the gate current predicted by thermionic emission calculations. For example, the measured gate current increases from 1500 μA to 3500 μA when the applied voltage changes from V_{DG} = 18 V to V_{DG} = 24 V. For the same voltage increase, the thermionic emission current should increase from 320 nA to
760 nA. Again, this appears to indicate the presence of a significant generation current in the depletion region of the device. The nature of this generation current is discussed in the next section.

2-3 GENERATION CURRENT

Energy states near the middle of the bandgap can act as generation centers under reverse bias conditions. The depletion region under the gate could therefore give rise to a generation component of the gate current if defects exist in that region, and those defects have energy states near the middle of the bandgap.

Within the depletion region of the gate, energy states near the center of the bandgap may act to create electron/hole pairs. The generation rate of carriers, U, is described by Equation 2-7 [3] as

Equation 2-7

$$U = N_{GC} \cdot \sigma \cdot v_{TH} \cdot N_C \cdot e^{-\left(\frac{E_C - E_{GC}}{kT}\right)}$$

where σ is the effective capture cross-section of the generation center, v_{TH} is the thermal velocity of the carriers, N_{GC} is the number of generation centers per unit volume, E_{GC} is the energy level of the generation center, and E_C is the conduction band edge. The thermal velocity for GaAs is reported to be $v_{TH} = 2.32 \times 10^8$ cm/s and the density of states in the conduction band is calculated to be $N_C = 4.7 \times 10^{17}$ /cc. The assumption made for Equation 2-7 is that the generation centers have an energy level at E_i (the Fermi level of the intrinsic material) and that the capture cross sections of holes and electrons are equal.

If the centers are not at an energy level E_i, then electron-hole pairs are less likely to form, since either the energy required to promote an electron to the conduction band will increase, or the energy required to promote a hole to the valence band will increase. In the middle of the bandgap, the energy required to promote a hole or an electron to the conduction or valence band (respectively) is the same, and therefore, an equal probability exists for electron or hole promotion.

The effective capture cross section is given by $\sigma = \sigma_o X$, where σ_o is the intrinsic capture cross-section and X represents the combined effects of temperature, applied electric field, and the entropy change due to the emission process. For GaAs, σ_o is experimentally determined [3] to be on the order of 10^{-13} cm^2. X is given by Equation 2-8.

Equation 2-8

$$X = \frac{g_o}{g_1} \cdot e^{\frac{\Delta S}{k}} \cdot e^{\frac{\Delta E}{kT}}$$

where g_o is the degeneracy of the generation center not occupied by an electron, g_1 is the degeneracy of the generation center occupied by one electron, ΔS is the entropy change associated with emission of an electron, and ΔE is an energy factor related to the presence of an electric field. The degeneracy factors are not well known for deep level impurities in GaAs. For shallow donor impurities, the ground state degeneracy in GaAs is 2, since the donor can accept an electron with either spin or can have no electron. For shallow acceptor states, there are two degenerate valance bands at $k = 0$, making $g_o = 4$. As an estimate, the ratio of g_o:g_1 is taken to be 2. The change in entropy associated with an electron emission is estimated to be on the order of a few k

(Boltzman's constant), but again, is unknown for deep levels in GaAs. As an estimate, ΔS is taken to be 3k. Experimentally determined values of X, under conditions of low applied field, suggest X is between 10 and 100 for deep level impurities in GaAs [3].

ΔE is due to the attractive force experienced by the electron (or hole) due to an applied electric field. Figure 2-5 shows the effect of the applied electric field on the potential barrier for electron emission.

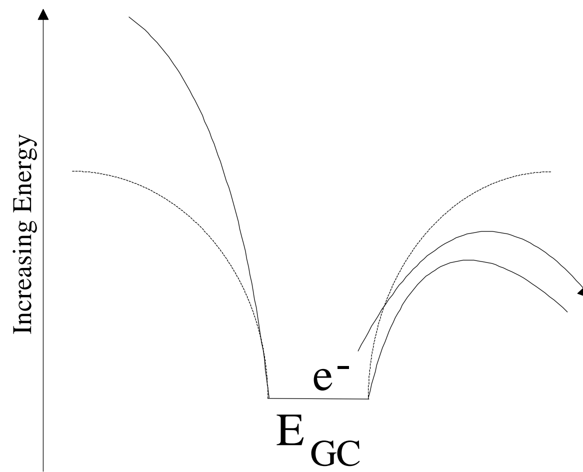

Figure 2-5: Energy diagram for a generation center under no bias (dotted lines) and under reverse bias (solid lines). E_{GC} is the energy level of the generation center; the trapped electron needs less energy under reverse bias to escapee from the generation center.

The attractive force between the generation center and an electron is given by Equation 2-9.

Equation 2-9

$$F = \frac{-q^2}{16 \cdot \pi \cdot \varepsilon_r \cdot \varepsilon_o \cdot z^2}$$

The potential energy as a function of distance from the generation center is given by [3]

Equation 2-10

$$PE(z) = \int_{\infty}^{z} F\,dz = \frac{q^2}{16\cdot\pi\cdot\varepsilon_r\cdot\varepsilon_o\cdot z}$$

If an external field, E, is applied,

Equation 2-11

$$PE(z) = \frac{q^2}{16\cdot\pi\cdot\varepsilon_r\cdot\varepsilon_o\cdot z} - q\cdot E\cdot z$$

The maximum in the barrier (on the side that is lowered) is found by taking the derivative and setting the result equal to zero. The result is the same form as Equation 2-6, which represents the reduction in the potential barrier due to image force lowering of the Schottky barrier.

Having defined all of the terms in Equation 2-7 to determine the generation rate, the generation current is given by Equation 2-12

Equation 2-12

$$I_{gen} = qUZYh,$$

where Z, Y, and h are the gate width, depletion region length, and depletion region width [3].

Generation centers exist in the depletion region as a consequence of point defects, surface states, and dislocations. Since the gate current at V_D = 12V and V_G = -6V is typically 1500 μA, and the parameters for the thermionic current are known, the pre-power slump value for N_{GC} is calculated to be on the order of 10^{18} /cc, assuming that all generation centers are located at the center of the bandgap and that no leakage current exists[‡]. Using $N_{GC} = 10^{18}$ /cc, the calculated value of the gate current is 1450 μA at V_{DG} = 18 V and 2622 μA at V_{DG} = 24 V, in agreement with measured values.

As will be shown in chapter 7, the number of generation centers necessary to cause power slump is on the order of 10^{19} /cc, an order of magnitude higher than the pre-power slump value. In the next few chapters, it will be shown that the generation centers responsible for power slump are likely to be kinks on dislocations, which form as a consequence of high shear strain in the gate region, high electric field, and high doping levels.

[‡] In fact, 10^{18} /cc is a relatively large number of generation centers in GaAs, suggesting that large leakage currents are probably present in these devices (in addition to the generation current).

2-4 CHAPTER REFERENCES

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Chapter 3
X-Ray Topography

X-ray topography, also known as X-ray microscopy, can be used to image defects and strain fields in nearly perfect single crystal materials. For all topographic techniques, only crystals with dislocation densities less than 10^6 /cm^2 and a relatively large subgrain structure are suitable. Since several X-ray topographic techniques exist, it is important to select the method which will provide the best images for a particular sample type. The samples used in this investigation are either 125 µm thick devices or 650 µm thick wafers, both with an average subgrain diameter of 60 µm. In addition to sample thickness and subgrain structure, it is also important to consider the information which is hoped to be obtained by the experiment. For this investigation, a topographic technique which can image strain fields and defect structures as a function of depth and at a resolution of 1 µm is desired.

The Berg-Barrett method, the Lang method, the Borrmann method, and Laue imaging are discussed [1]. The first three techniques are the traditional methods of topographic imaging, and use characteristic K_α radiation (single wavelength). The Laue technique has found limited use in the investigation of semiconductor devices primarily because this technique requires white radiation, which is not practical for routine materials investigation*.

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* White radiation is impractical because of the long film exposure times when using a low-flux X-ray tube. A high flux source of white radiation (such as an X-ray synchrotron) is not practical for routine measurements because of the limited availability of such facilities.

3-1 X-RAY TOPOGRAPHY METHODS

The overwhelming majority of topographic investigations of GaAs materials use the Berg-Barrett method. The Lang method and the Borrmann method have found only limited application for GaAs imaging. Laue imaging, which apparently has not been previously used in GaAs microelectronic investigations, is also discussed. By assessing all topographic techniques, it will be shown in this section that Laue imaging is the best technique for this investigation.

THE BERG-BARRETT METHOD

The Berg-Barrett method uses K_{α} radiation in reflection mode to produce a topograph of the sample surface on a photographic plate (see Figure 3-1). Regions of the specimen which are highly perfect will diffract, causing the corresponding region on the photographic plate to darken. Regions which have lower extinction than neighboring regions, will appear darker. Regions which do not satisfy the Bragg condition will appear lighter. Therefore, since regions around subgrain boundaries contain non-uniform strain, such defects can be identified as darker regions on the topograph. Microcracks, dislocation structures and regions of different phase will appear white.

This technique requires a highly parallel incident beam. The maximum resolution of this technique (using a double crystal diffractometer) is 5 - 10 μm, primarily due to beam divergence. A major restriction is that the 2θ angle must be near 90° to prevent distortion of the image. For GaAs, this limits the investigation to defects which can be imaged on strongly reflecting planes with a Bragg angle near 45°.

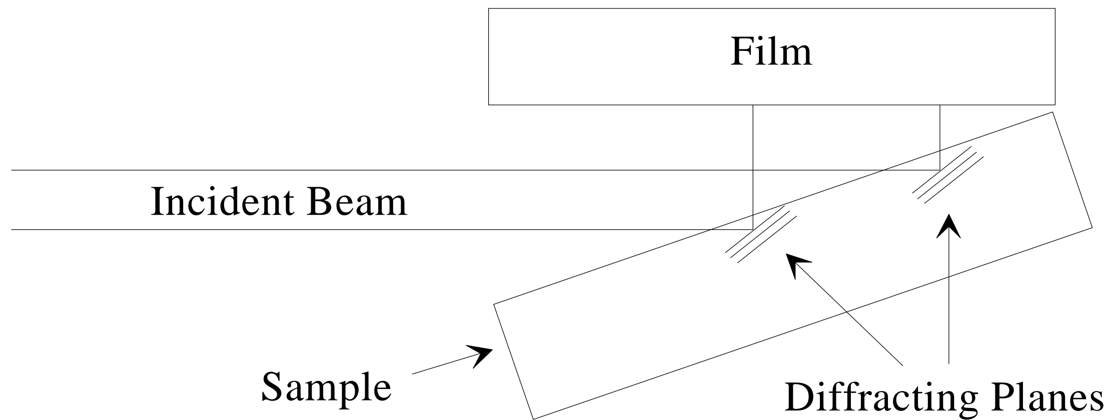

Figure 3-1: Geometry for Berg-Barrett topography.

Unfortunately, the Berg-Barrett method requires that the sample under investigation to be a nearly perfect single crystal, with very large, very low-angle subgrains. The ideal case for Berg-Barrett imaging would be no subgrain structure, which would maximize extinction contrast between the background and dislocation structures. The GaAs samples used in this investigation contain a very dense subgrain structure, which expected to significantly reduce strain field contrast (for non-parallel beam optics).

Since a primary objective of the topography measurements is to image strain fields in the device, both around dislocation structures and device structures, the Berg-Barrett method is not optimal for our purposes. Also, the Berg-Barrett method cannot provide information about the three-dimensional distribution of defects.

LANG METHOD

The Lang method is a transmission technique and is only suitable for samples which have a thickness satisfying the condition that $\mu t \sim 1$, where μ is the linear absorption coefficient for X-rays and t is the sample thickness. Put simply, the specimen must be thin enough for sufficient intensity to emerge from the crystal, but thick enough so that sufficient volume exists for diffraction.

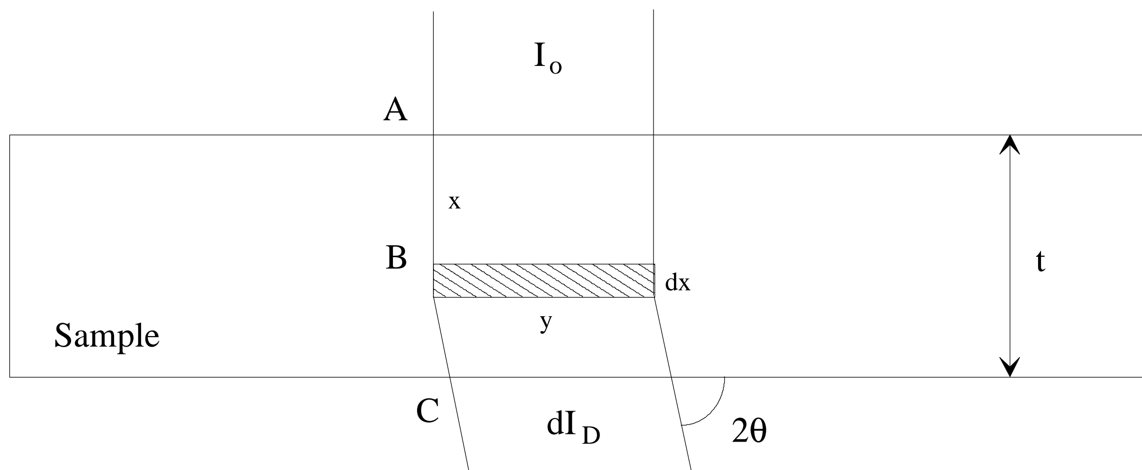

Figure 3-2: Geometry for the calculation of the optimal sample thickness for the Lang method.

Using the geometry defined in Figure 3-2, Cullity shows [2] that the total diffracted intensity outside the sample, originating in a layer of thickness dx at a depth x, is given by

Equation 3-1

$$dI_D = \varepsilon y I_o e^{-\mu (AB+BC)} dx$$

where ε is the fraction of the incident energy diffracted by the differential volume, AB = x and BC = (t - x) for small Bragg angles. By integrating from x = 0 to x = t, the diffracted intensity of the beam is determined to be

Equation 3-2

$$I_D = \varepsilon y t I_o e^{-\mu t}$$

By differentiation,

Equation 3-3

$$dI_D/dt = \varepsilon y I_o e^{-\mu t} - \varepsilon y t \mu I_o e^{-\mu t}$$

Setting $dI_D/dt = 0$, the maximum diffracted intensity occurs when $t = 1/\mu$ (assuming a small value of θ). To illustrate the required thickness which would be suitable for Lang topography, values are calculated for $Cr_{K\alpha}$ (2.29 Å) and $Mo_{K\alpha}$ (0.711 Å) radiation. For GaAs, $\mu = 1096\ cm^{-1}$ for $Cr_{K\alpha}$ radiation, requiring the sample thickness to be approximately 9 µm. For $Mo_{K\alpha}$, $\mu = 355\ cm^{-1}$, requiring the sample to be approximately 30 µm. Since our samples are either 125 µm for fully processed devices, or 625 µm for wafers, the Lang technique is not suitable for our purposes.

THE BORRMANN METHOD

The Borrmann method relies on anomalous transmission of X-rays to image defects through the bulk of the sample. Anomalous transmission is a dynamical diffraction phenomenon in which X-rays propagate through the sample parallel to the diffracting planes. Contrary to classical X-ray diffraction theory, anomalous transmission is not affected by absorption. However, it is very sensitive to disruptions in the periodic nature of the crystal lattice and cannot occur in crystals which contain significant mosaic structure. Since GaAs has dense subgrain structure, anomalous transmission will not occur to any appreciable extent. Therefore, the Borrmann technique is unsuitable for our purposes.

LAUE IMAGING

When highly parallel white radiation is incident on a single crystal, planes satisfying the Bragg and structure factor conditions will diffract. If X-ray sensitive film is placed near the diffracting crystal, each diffracted beam will produce a spot on the film, creating a Laue pattern. Since diffraction is a function of wavelength and Bragg angle, crystalline defects may be studied on several different planes with a single radiation, or on the same plane with a wide range of wavelengths. The advantage of investigating a single plane with several wavelengths is that absorption is a function of wavelength, so the near-surface layers may be studied as a function of depth.

Since a synchrotron source is used for this technique, several other advantages are realized. First, since the incident beam is highly parallel, resolution of this technique

is greater than other techniques which use non-parallel optics. In this case, it is the grain size of the X-ray film that is the limiting factor for resolution. For standard X-ray film the maximum resolution is approximately 3 μm. For nuclear emulsions, the maximum resolution is approximately 1 μm. Another advantage of synchrotron radiation is that the incident beam is very intense over a broad range of wavelengths. This allows relatively short film exposure times for any wavelength used, and increases the information available regarding defect distribution as a function of depth.

3-2 THE LAUE TECHNIQUE

The geometry for the Laue technique is shown in Figure 3-3. For a given α, diffraction will occur at those angles for which Bragg's Law is satisfied. Thus, each plane, having a unique d-spacing, will diffract only at a particular wavelength, since θ is fixed.

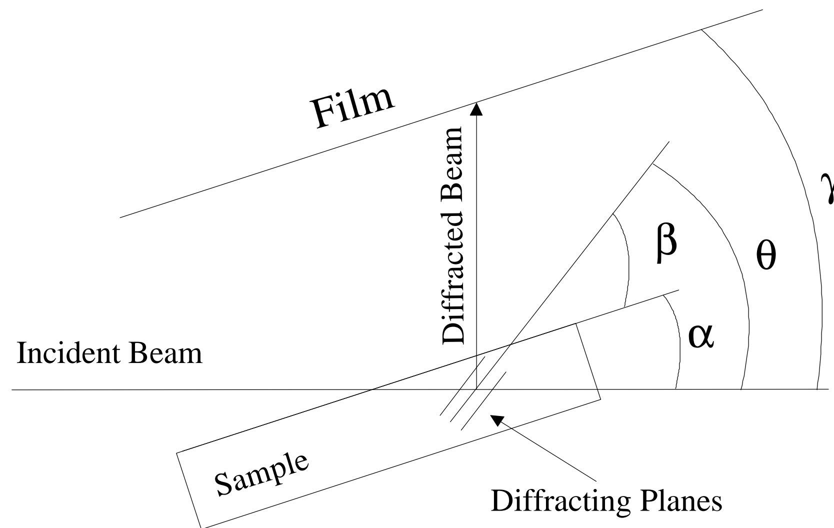

Figure 3-3: Geometry for Laue imaging.

As discussed previously (Lang topography), transmission experiments are not suitable for the samples used in this investigation. Therefore, Laue imaging in reflection mode is used. Noteworthy experimental details of Laue imaging include:

1. To eliminate parallax, a single emulsion film should be used. Double emulsion films create double images unless the exposing beam is normal to the film surface (which is rather difficult to achieve for any one spot and impossible to achieve simultaneously for the entire pattern using standard flat X-ray film or nuclear emulsion plates).

2. To image the entire Laue pattern, either a very large, curved strip of film must be used, or the angle γ must be varied in such a way that different regions of the pattern can be imaged on successive films. The latter technique is used for this investigation.

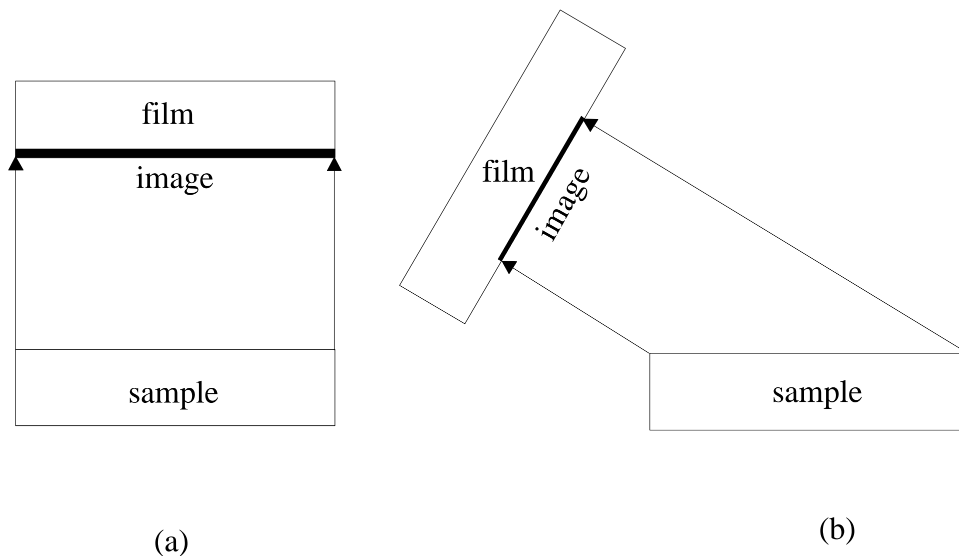

Figure 3-4: Image compression when diffracted X-rays are (a) normal to the sample surface and (b) oblique to the sample surface.

3. To image a particular plane as a function of wavelength, γ is held constant and α is varied (thus varying θ). By varying α (and thus θ), different wavelengths will satisfy the Bragg condition. The position of the diffraction spot on the film will not change (if γ is fixed); only the wavelength producing the spot will change.

4. To minimize compression of the surface image (and therefore loss of resolution), the diffracted beam must leave the sample surface as close to 90° as possible and strike the film at 90°, as shown in Figure 3-4 (a). This requires that the sample surface and the film be parallel, which fixes $\gamma = \alpha$. If the diffracted beam leaves the sample surface at an oblique angle, the image appears compressed, as shown in Figure 3-4 (b). This reduces the effective resolution of features on the image since the diffracted beams from adjacent defects blur together as the image is compressed. Therefore, for a particular hkl plane, there is only one wavelength which gives the proper Bragg angle satisfying the condition for maximum resolution, $\lambda = 2d \sin(90^{o} - \beta)$, corresponding to $\alpha = 90 - 2\beta$. Fortunately, small changes in α only compress the image by a small percentage, while allowing for a significant change in wavelength. So, although resolution is not optimized as wavelength is changed, acceptable results are still obtainable.

3-3 DEPTH OF PENETRATION CONSIDERATIONS FOR TOPOGRAPHIC IMAGING IN GaAs

X-ray absorption is the primary factor which defines the sampling volume of most X-ray techniques. Since Laue imaging allows use of a variety of wavelengths, the depth of penetration can be controlled to some extent, thus allowing information about the defect structure as a function of depth to be obtained. Absorption is also important when considering fluorescence, which can act to decrease resolution of topographic images.

LINEAR ABSORPTION

The figure of merit that defines absorption characteristics is the linear absorption coefficient, μ. The linear absorption coefficient represents the relationship between the transmitted and absorbed portions of an X-ray as it interacts with matter in a homogeneous medium. From Beer's Law,

Equation 3-4

$$I_x = I_o e^{-2\mu x},$$

where I_x is the intensity of the transmitted beam, I_o is the intensity of the incident beam, x is distance through the sample, and the factor of 2 accounts for the beam path into and out of the sample.

Empirically, the linear absorption coefficient for any element follows a relationship given by [2]:

Equation 3-5

$$\mu = k\rho\lambda^3 Z^n,$$

where ρ is the density of the material, λ is the wavelength of the X-ray, and Z is the atomic number. The coefficients k and n are constants, where k is different for different quantum shells and n is a number between 2 and 3. The linear absorption coefficient for a compound is given by [2]

Equation 3-6

$$\mu_{GaAs} = \mu_{Ga} \cdot w_{Ga} + \mu_{As} \cdot w_{As}$$

where w is the weight fraction of an element in the compound.

Normally, X-ray analysis is typically performed using X-ray tubes with targets of either Mo, Cu, Co, Fe, or Cr. For these characteristic radiation wavelengths, the *International Tables for X-Ray Crystallography* [3] give mass absorption coefficients (μ/ρ) for most elements. From this data, the linear absorption coefficient may be calculated for any material. For GaAs, with a density of 5.32 g/cc, Table 3-1 is calculated:

Table 3-1: Linear absorption coefficients for GaAs at selected wavelengths

Radiation (Å)	Mo (0.711)	Cu (1.54)	Co (1.79)	Fe (1.94)	Cr (2.29)
μ (cm^{-1})	327	368	556	695	1097

This investigation uses white synchrotron radiation for topographic investigations. Since white radiation is continuous, the linear absorption coefficient of GaAs for a wide range of wavelengths must be calculated. The data of table 3-1 are used to calculate regression coefficients for k and n. The regression analysis shows that for the K-shell branch, $k_{As} = 0.003770$, $k_{Ga} = 0.004031$, $n_{As} = 2.533$, and $n_{Ga} = 2.580$. For the L-shell branch, $k_{As} = 0.000645$, $k_{Ga} = 0.000631$, $n_{As} = 2.74$, and $n_{Ga} = 2.77$. From these data, the plot shown in Figure 3-5 is obtained.

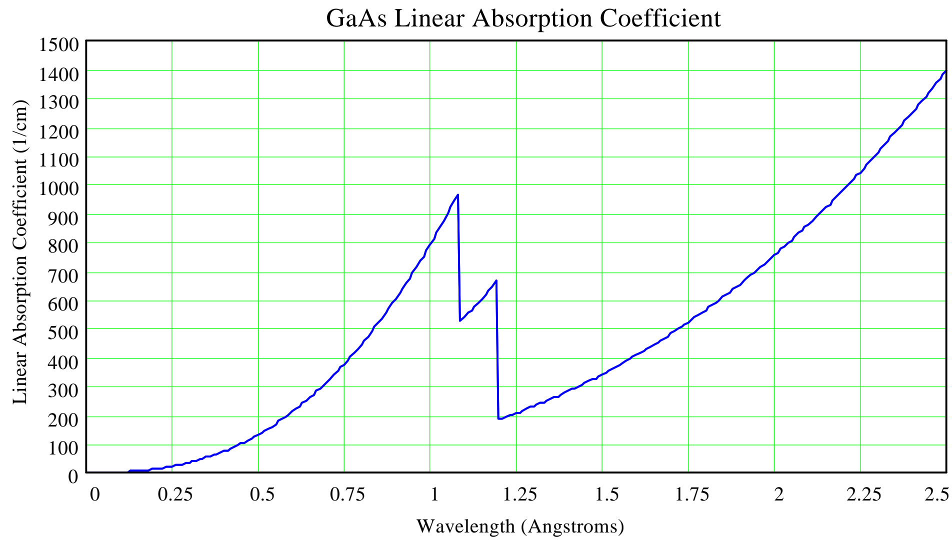

Figure 3-5: Calculation of the linear absorption coefficient for GaAs.

Absorption affects the depth of penetration, and thus the relative intensity of the diffracted beam from a given location below the sample surface. The depth of penetration is given by [4]:

Equation 3-7

$$G_z = 1 - e^{-\mu z \cdot \left(\frac{1}{\sin(\alpha)} + \frac{1}{\sin(\beta)}\right)}$$

where G_z is the fraction of the total diffracted intensity originating from the sample surface to a depth z below the surface (it is generally accepted that the depth of penetration is defined when $G_z = 0.95$). Therefore, a crystallographic plane which is imaged, using a wavelength that corresponds to a small μ, will provide information about defects farther below the surface than a wavelength that corresponds to a larger μ. For example, if the 533 plane is imaged using $\alpha = 9.4^o$, then $\lambda = 1.3157$ Å. For this wavelength, Table 3-1 shows a value of $\mu = 220$ /cm which corresponds to a depth of penetration of 19 μm. If the 533 plane is imaged using $\alpha = 1.0^o$, then $\lambda = 1.1386$ Å, corresponding to $\mu = 550$ /cm and a depth of penetration of approximately 0.93 μm.

By imaging a particular plane as a function of depth of penetration, information about the distribution of defects in the z-direction can be obtained. Shallow penetration depths will only image surface defects, while deeper penetration depths will image defects farther below the surface (assuming the concentration of surface defects is reasonably small).

ATTENUATION

Another consideration affecting the depth of penetration is attenuation. When a highly parallel beam is incident on a material, and the mosaic structure is such that a significant portion of the diffraction is subject to primary and secondary extinction, attenuation of the beam due to secondary and higher order reflections must be considered. The attenuation coefficient is given by Warren [4] as

Equation 3-8

$$\tau = 0.5\pi(q^2/mc^2)N\lambda F$$

where q is the electronic charge, m is electron mass, c is the speed of light, N is the number of unit cells in the material per unit volume, λ is the wavelength, and F is the structure factor given by (for GaAs):

$F^2_{hkl} = 0$	for hkl mixed
$F^2_{hkl} = 16(f_{Ga} + f_{As})^2$	for $h + k + l = 4n$
$F^2_{hkl} = 16(f_{Ga} - f_{As})^2$	for $h + k + l = (2n + 1)2$
$F^2_{hkl} = 16(f_{Ga}^2 + f_{As}^2)$	for hkl all odd

where n is an integer greater than zero and f is the atomic scattering factor.

When attenuation is significant, the linear absorption coefficient, μ, should be replaced in Equation 3-7 by the attenuation coefficient τ. The attenuation coefficient acts to reduce the effective depth of penetration considerably; as much as 3 orders of magnitude in some instances. This would, for example, reduce the effective depth of penetration for 0.711 Å radiation from 30 µm to approximately 30 nm in GaAs.

The influence of the atomic scattering factors, f_{Ga} and f_{As}, are important when interpreting defect structures as a function of depth below the surface. The atomic scattering factor is inversely proportional to radiation wavelength, and has different values for Ga and As atoms. Thus, topographic images which are created using longer wavelengths will have smaller attenuation coefficients than images created using short wavelengths. Likewise, images created using reflections from planes[†] with a structure factor $F^2_{hkl} = 16(f_{Ga} - f_{As})^2$ will have smaller attenuation coefficients than reflections from other planes. A smaller attenuation coefficient corresponds to a deeper depth of penetration, which must be considered when determining the location of a defect below the surface.

[†] such that $h + k + l = 2(2n + 1)$

Most crystals, including the GaAs crystals used in this investigation, are neither ideally perfect nor ideally imperfect, but somewhere in-between. Thus, topographic images do not represent diffraction from a uniform depth of penetration. Near subgrain boundaries and other large-scale defects such as lineages, extinction will be minimized. In these regions, it is expected that the depth of penetration will be greater since attenuation effects will be minimal. In the interior of the subgrains, attenuation should be significant, resulting in a more shallow depth of penetration. Since the subgrain boundaries are relatively narrow (with respect to the interior of the subgrain) most of the image can be interpreted using depth of penetration calculations based on the attenuation coefficient. The presence of different absorption characteristics can create some unusual phenomena in topographic images. For example, as shown in Figure 3-6, when strain fields from device structures overlap large scale defects and subgrain boundaries, the differences in the nature of X-ray absorption make the strain fields appear “wavy”.

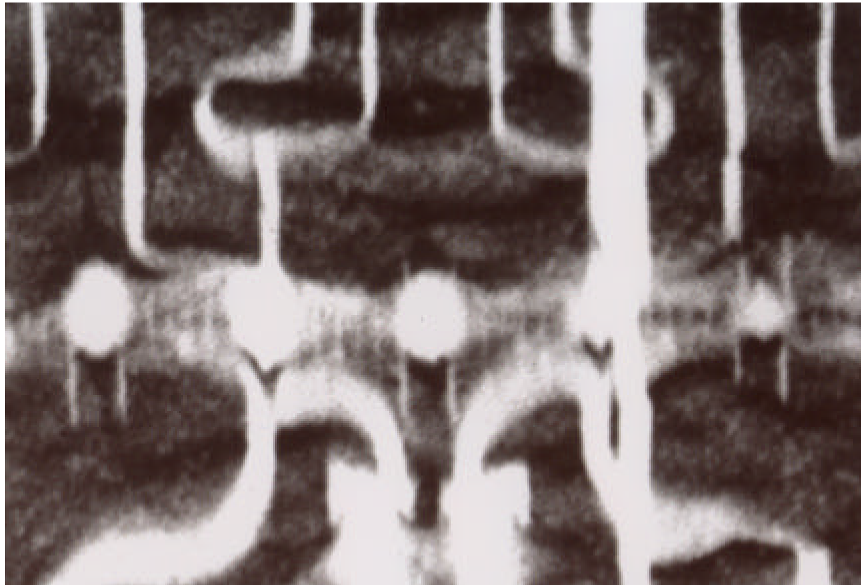

Figure 3-6: X-ray topograph showing linear absorption and attenuation. The white regions are strain fields, made "wavy" near subgrain boundaries due to differences in absorption characteristics.

FLUORESCENCE

The information in Figure 3-5 is also important when determining at which wavelengths X-ray fluorescence may occur. Fluorescence will affect the resolution of the topograph by "fogging" the film, and is therefore an important parameter to consider when designing the topographic experiment. From Figure 3-5, it is shown that the K-edge of Ga is located at a wavelength of 1.1958 Å. Below this wavelength, significant absorption will occur, increasing the intensity of fluorescence. Above approximately 2.37 Å, absorption is also high, causing fluorescence to occur from the L-shell of As. Thus, the optimal range of wavelengths to use for topographic imaging is in the range of 1.20 Å to 1.95 Å, where absorption is relatively low.

3-4 CHAPTER REFERENCES

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[3] International Union for Crystallography, *International Tables for X-Ray Crystallography*, Kynoch Press, Birmingham, England, v. 4, pp. 61 - 66.

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Chapter 4
Theories and Equations of Stress

This chapter presents the relevant theories and equations of stress and strain induced by thin films on thick substrates; specifically, macrostress due to bending moments and film-edge stress due to force continuity requirements. Computer models are developed and applied for the materials and device structures under investigation using a distributed force approximation. X-ray topographs are used to verify the accuracy of the computer models.

The complete state of stress in the wafer and near device features consists of two components - macrostress and film-edge stress. Theories for both types of stress are required for the investigation of power slump, which is believed to be a function of shear stress in the active region of the device, and for the investigation of wafer breakage, which is believed to be related to high normal stress near passivation edges.

It is demonstrated that measured shear stress in the gate-to-drain region theoretically exceeds the magnitude required by our model to induce power slump. It is also shown that measured normal stresses exist which theoretically exceed the magnitude necessary to induce microcracking and fracture of the wafer.

4-1 MACROSTRESS DUE TO BENDING MOMENTS

When an adherent film is deposited on a relatively thick substrate, bending moments often arise due to mismatch in thermal expansion coefficients. This occurs as the film and wafer cool from relatively high deposition temperatures to room temperature. For

the cases of a SiON or SiN film on a GaAs substrate, the films have a smaller thermal expansion coefficient than does the substrate, creating a tensile stress in the film and a compressive stress in the substrate surface (adjacent to the film) upon cooling.

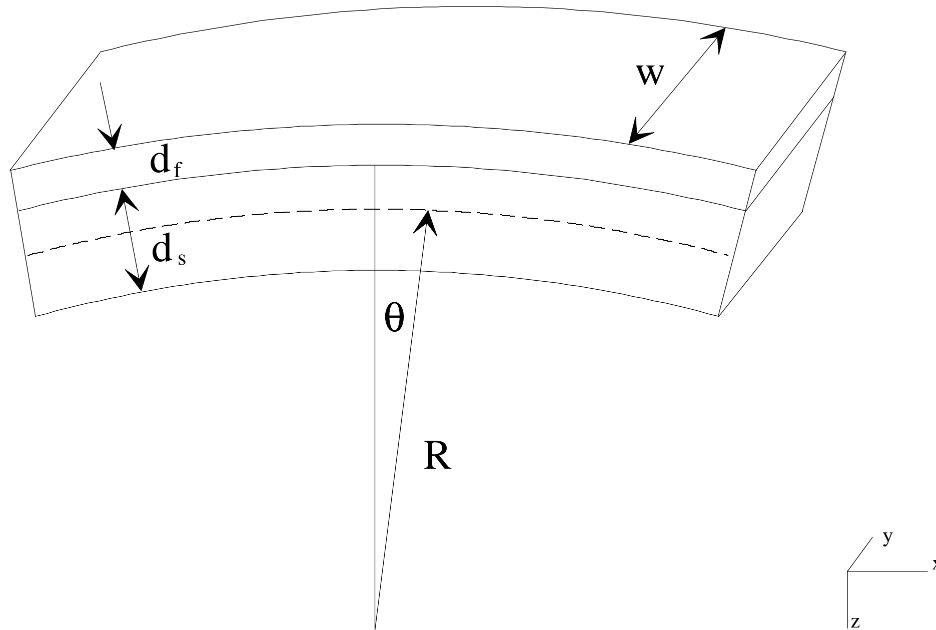

Figure 4-1: Geometry for the bending plate approximation. R is the radius of curvature, d_f and d_s are the thickness of the film and subtrate, and w is the plate width.

Figure 4-1 shows the geometry and definitions of terms used in the derivation of surface stress equations for the bending plate approximation of a thin film on a thick substrate. First, the equations of stress for an unconstrained, bare rectangular substrate will be derived. Using these equations, the equations of stress for the case of a thin film on a rectangular substrate will be derived. The result is the Stoney formula [1], which is commonly used to calculate bending stresses. Second, a more rigorous derviation of bending stresses by Röll [2] will be presented. This model will be applied to the cases of SiON or SiN on GaAs. Computer simulations will also be

presented which show the distribution of stress in the substrate due to bending moments.

STONEY FORMULA

For an elastically bent, bare ($d_f = 0$), rectangular substrate,

Equation 4-1

$$\varepsilon = \frac{\Delta L}{L} = \frac{(R + z)\cdot\theta - R\theta}{R\theta}$$

where z = d/2 represents the strain on the top surface and z = -d/2 represents the strain on the bottom surface. Using Hooke's Law,

Equation 4-2

$$\left|\sigma_{max}\right| = \frac{E_s \cdot d_s}{2\cdot R}$$

where E_s is the elastic modulus of the substrate in the bending direction. The sign of the stress is positive for tensile stress (on the top surface in Figure 4-1) and negative for compressive stress (on the bottom surface in Figure 4-1).

The induced moment is calculated to be the force generated in the substrate (F_s) by the internal stress multiplied by the moment arm, which is taken to be at the center of the substrate. This assumption is valid if the center of the stress distribution is at the

midpoint of the substrate, which is reasonable for symmetrically distributed stresses. Thus, as the substrate is bent,

Equation 4-3

$$M_s = \frac{F_s \cdot d_s}{2}$$

The substrate is now assumed to have an adherent film such that $d_f \neq 0$ and is initially held flat. Conservation of moments requires that

Equation 4-4

$$\Sigma M = 0$$

And thus,

Equation 4-5

$$M_s + M_f = 0$$

If the substrate is then released (implying $M_s \neq -M_f$),

Equation 4-6

$$\frac{F_s \cdot d_s}{2} + \frac{F_f \cdot d_f}{2} = M_s + M_f$$

Since F_s and F_f must be equal at the interface (due to conservation of force requirements), we have the result that

Equation 4-7

$$M_s + M_f = F_s \cdot \left(\frac{d_s + d_f}{2} \right)$$

The moment in the film (or the substrate) is given by,

Equation 4-8

$$M = \int_0^{\frac{d}{2}} \sigma \cdot y \, dA$$

By substituting $dA = w \cdot \frac{y}{\left(\frac{d}{2}\right)} \cdot dy$, where A is the cross-sectional area of the film (or substrate),

Equation 4-9

$$M = 2 \cdot \int_0^{\frac{d}{2}} \sigma \cdot y \cdot w \cdot \frac{2 \cdot y}{d} \, dy = \frac{\sigma \cdot w \cdot d^2}{6}$$

By substituting Equation 4-2 into Equation 4-9,

Equation 4-10

$$M = \frac{E \cdot d^3 \cdot w}{12 \cdot R}$$

By substitution of Equation 4-2 and Equation 4-10 (applied for both the substrate and the film) into Equation 4-7, the magnitude of the substrate surface stress is determined to be,

Equation 4-11

$$\sigma_s = \frac{1}{6 \cdot R \cdot d_s} \cdot \frac{1}{d_s + d_f} \cdot \left[\left(\frac{E_f}{1 - \nu_f} \right) \cdot \left(d_f \right)^3 + \left(\frac{E_s}{1 - \nu_s} \right) \cdot \left(d_s \right)^3 \right]$$

where E is replaced by $E/(1-\nu)$ to account for the biaxial state of stress [3] (ν_f and ν_s are the Poisson's ratios of the film and substrate, respectively).

Equation 4-11 should give rise to a residual stress in the substrate of approximately 320 kPa for a typical film stress of 200 MPa in a 125 μm GaAs substrate with a 2000 Å adherent SiN thin film. However, our X-ray strain measurements consistently show stresses which are two orders of magnitude greater than those which should exist due bending moments.

RÖLL'S EQUATIONS OF BENDING PLATE STRESS

The preceding equations were derived under the assumption of homogenous, isotropic stresses, which do not exist in our case. A more rigorous derivation is given by Röll [2], who shows that,

Equation 4-12

$$\sigma_{xx} = \alpha_{xx} + \beta_{xx}\xi$$

and

Equation 4-13

$$\sigma_{yy} = \alpha_{yy} + \beta_{yy}\xi$$

where α is the dilatation stress, β is the deviatoric (deformation) stress, xx is the stress in the x-direction due to bending in the xz plane, yy is the stress in the y-direction due to bending in the yz plane, and ξ is the distance from the substrate/film interface in the z-direction. Using a linear approximation for the case that the film is much thinner than the substrate,

Equation 4-14

$$\left(\sigma^{o}\right)_{xx} = \frac{-\left(d_s\right)^2}{6 \cdot d_f} \cdot \left[\kappa_s \cdot \frac{\delta}{\delta x} \cdot \left(\frac{\delta W}{\delta x}\right) \cdot \left(1 + \frac{4 \cdot \kappa_f \cdot d_f}{\kappa_s \cdot d_s} - 2 \cdot \frac{C_{xx}}{d_s}\right) + \lambda_s \cdot \frac{\delta}{\delta y} \cdot \left(\frac{\delta W}{\delta y}\right) \cdot \left(1 + 4 \cdot \frac{\nu_f \cdot d_f}{\nu_s \cdot d_s} - 2 \cdot \frac{C_{yy}}{d_s}\right) \right]$$

and

Equation 4-15

$$\left(\sigma^{o}\right)_{yy} = \frac{-\left(d_s\right)^2}{6 \cdot d_f} \cdot \left[\kappa_s \cdot \frac{\delta}{\delta y} \cdot \left(\frac{\delta W}{\delta y}\right) \cdot \left(1 + \frac{4 \cdot \kappa_f \cdot d_f}{\kappa_s \cdot d_s} - 2 \cdot \frac{C_{yy}}{d_s}\right) + \lambda_s \cdot \frac{\delta}{\delta x} \cdot \left(\frac{\delta W}{\delta x}\right) \cdot \left(1 + 4 \cdot \frac{\nu_f \cdot d_f}{\nu_s \cdot d_s} - 2 \cdot \frac{C_{xx}}{d_s}\right) \right]$$

and

Equation 4-16

$$\left(\tau^{o}\right)_{xy} = \frac{-\left(d_s\right)^2}{6 \cdot d_f} \cdot \mu_s \cdot \frac{\delta}{\delta x} \cdot \left(\frac{\delta W}{\delta y}\right) \cdot \left(1 + 4 \cdot \frac{\mu_f \cdot d_f}{\mu_s \cdot d_s} - 2 \cdot \frac{C_{xy}}{d_s}\right)$$

where σ^o and τ^o are the film stresses, κ, μ, and λ are modified Lamé coefficients, d_s or d_f is the thickness of the film or substrate, ν is Poisson's ratio, and C is the center of the stress distribution in the thin film or the substrate. The parameters α and β in the x-direction are given by:

Equation 4-17

$$\alpha_{xx} = \frac{-4 \cdot d_f \cdot \left(\sigma^0\right)_{xx}}{\nu_s \cdot d_s} \cdot \left(1 - 4 \cdot \frac{\nu_f \cdot d_f}{\nu_s \cdot d_s} + \frac{3}{2} \cdot \frac{C_{xx}}{d_s}\right)$$

and

Equation 4-18

$$\beta_{xx} = \frac{-6 \cdot d_f \cdot \left(\sigma^o\right)_{xx}}{\nu_s \cdot \left(d_s\right)^2} \cdot \left(1 - 4 \cdot \frac{\nu_f \cdot d_f}{\nu_s \cdot d_s} + 2 \cdot \frac{C_{xx}}{d_s}\right)$$

and similar equations exist for α_{yy} and β_{yy}. These equations were used as the basis for a computer model to calculate the stress due to bending moments in a wafer. For the 650 μm wafers used in this research, Figure 4-2 was obtained.

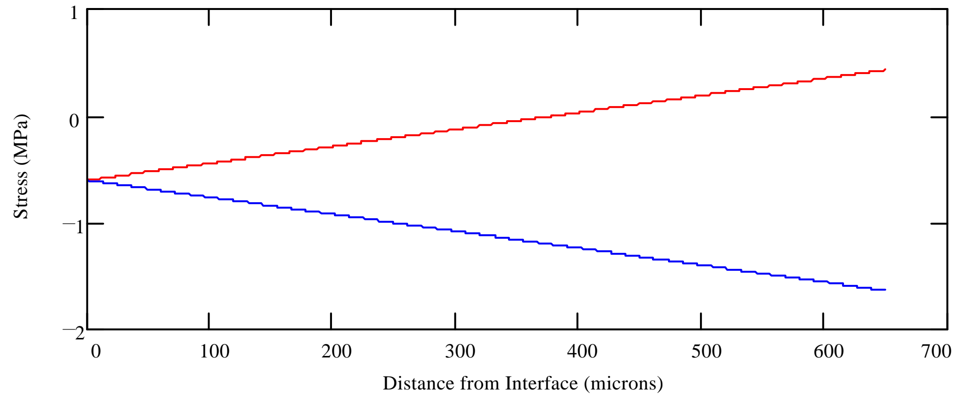

Figure 4-2: Computer plot of normal stress distribution in a wafer due to bending moments. Blue (lower line) is the x-direction and red (upper line) is the y-direction.

Still, these equations do not predict an appreciable strain in the wafer for the passivation layers under investigation. The maximum stress in the x-direction is 1.7 MPa, compressive, and 0.5 MPa, tensile in the y-direction. Therefore, it appears that the stresses measured by X-ray analysis are, for the most part, not due to bending moments from the film.

Since the residual stress from the crystal growing process are typically between 10 MPa and 30 MPa (as will be shown in Chapter 8), and it has been shown in Figure 4-2 that stress due to bending moments is not appreciable, the remaining stress must be due to modification of the surface during processing or film-edge stress (or both). An investigation of substrate surface modification during PECVD deposition and other fabrication processes of SiN and SiON thin films is beyond the scope of this study. Film-edge stress is discussed in the section 4-2.

4-2 FILM-EDGE STRESSES

Film edge stresses exist near discontinuities in adherent thin films due to force continuity requirements at the film edge. For the GaAs MESFETs under investigation, the film edge stresses developed under the gate, source, and drain edges are of primary importance. Calculation of these stresses involve the TiWN gate metal and the SiN or SiON passivation between the gate and drain and gate to source. The total stress in any region of the device will be the superposition of the stresses developed at the various film edges, the macrostress due to bending moments, and the residual stress developed in the substrate during crystal growth and processing.

Most authors use the concentrated force approximation when characterizing film edge stresses. The concentrated force approximation assumes that the initial stress in the film is uniform through the bulk of the film and becomes zero at the film edge, following a step function. Hu [4] has derived the edge stress components in the substrate using the concentrated force approximation:

Equation 4-19

$$\sigma_x = \frac{-2 \cdot F_x}{\pi} \cdot \frac{x^3}{\left(x^2 + z^2\right)^2}$$

Equation 4-20

$$\sigma_z = \frac{-2 \cdot F_x}{\pi} \cdot \frac{x \cdot z^2}{\left(x^2 + z^2\right)^2}$$

Equation 4-21

$$\tau_{zx} = \frac{-2 \cdot F_x}{\pi} \cdot \frac{x^2 \cdot z}{\left(x^2 + z^2\right)^2}$$

where the forces are in units of force per unit length. This approximation is valid for soft films on relatively hard substrates [4] (e.g., ohmic metal on GaAs), but becomes invalid as the magnitude of the elastic modulus of the thin film becomes close to, or exceeds, the modulus of the substrate (as is the case with SiN, SiON, or TiWN on GaAs). While these equations are valid for the initial description of stress distribution in the substrate, they ignore the effects of strain relaxation, leading to an inconsistency in the description of stress. The inconsistency is that as strain is developed in the substrate, a corresponding amount of strain relaxation must occur in the film. As the film stress near the edge is relaxed, it can no longer be unformly distributed, leading to errors in the concentrated force approximation. Therefore, a more sophisticated model is required.

Hu has shown that a distributed force can be described by:

Equation 4-22

$$\frac{\delta F_x}{\delta x} = d_f \cdot \frac{\delta \sigma_{f,x}}{\delta x}$$

where d_f is the thickness of the adherent film and $\sigma_{f,x}$ is the film stress in the x-direction. By convolution, the stress components in the film, as described by the distributed force model, are:

Equation 4-23

$$\sigma_x = \frac{-2 \cdot d_f}{\pi} \cdot \int_0^{\infty} \frac{(x-u)^3}{\left[(x-u)^2 + z^2\right]^2} \cdot \frac{\delta \sigma_{f,x}}{\delta u} \, du$$

Equation 4-24

$$\sigma_z = \frac{-2 \cdot d_f}{\pi} \cdot \int_0^{\infty} \frac{(x-u) \cdot z^2}{\left[(x-u)^2 + z^2\right]^2} \cdot \frac{\delta \sigma_{f,x}}{\delta u} \, du$$

Equation 4-25

$$\tau_{zx} = \frac{-2 \cdot d_f}{\pi} \cdot \int_0^{\infty} \frac{(x-u)^2 \cdot z}{\left[(x-u)^2 + z^2\right]^2} \cdot \frac{\delta \sigma_{f,x}}{\delta u} \, du$$

For wafer breakage problems, we are interested in the normal stress component σ_x, when it is tensile at the surface (z = 0). For the substrate surface stress,

Equation 4-26

$$\sigma_x = \frac{-2 \cdot d_f}{\pi} \cdot \int_0^{\infty} \frac{1}{(x-u)} \cdot \frac{\delta \sigma_{f,x}}{\delta u} \, du$$

which can be solved by the method of finite differences [5]. This method requires formulation of a grid to accurately characterize the integral. Since the initial

conditions of stress distribution is assumed to be a delta function, it is anticipated that the stress distribution in the distributed force model will be sharper closer to the film edge. Thus, a non-linear grid is most appropriate. The grid elements can be described by:

Equation 4-27

$$x_i = q \cdot \left(\frac{p^i - 1}{p - 1} - 0.5 \right)$$

which contains more elements closer to the film edge than far from it. The parameter q is related to the precision of the solution and has been determined to be sufficient at q=0.00005 for our purposes. The value of p is related to the magnitude of the finite difference, which has been determined to be p=1.2 for a sufficiently accurate solution at reasonable number of iterations.

NORMAL STRESS

The stress normal to the film edge, under the film is shown in Figure 4-3. For example, 300 Angstroms from the film edge, and under the film, the substrate surface stress is compressive, with a magnitude of approximately 100 MPa for a film stress of 200 MPa. It should be noted that within 50 Angstroms, the continuum approximation becomes increasingly less valid closer to the film edge. In this region, an atomic force model would be required to accurately describe the local stress. However, for the purposes of this research, knowledge of the magnitude of stress beyond 50 Angstroms from the film edge is sufficient. The biaxial stress distribution is symmetric about the film edge, with a corresponding tensile stress in the substrate developed on the side which is not covered by the film.

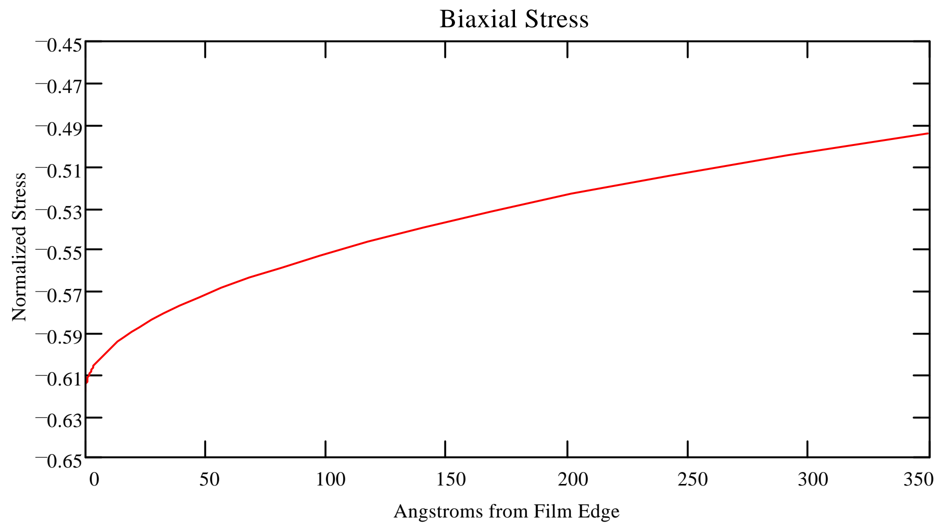

Figure 4-3: Biaxial Stress in a GaAs Substrate due to a SiN Film Edge, using d_f = 2000 Å, E_f = 200 GPa, ν_f = 0.5, E_s = 89 GPa, and ν_s = 0.244. Normalized stress = σ_s / σ_f.

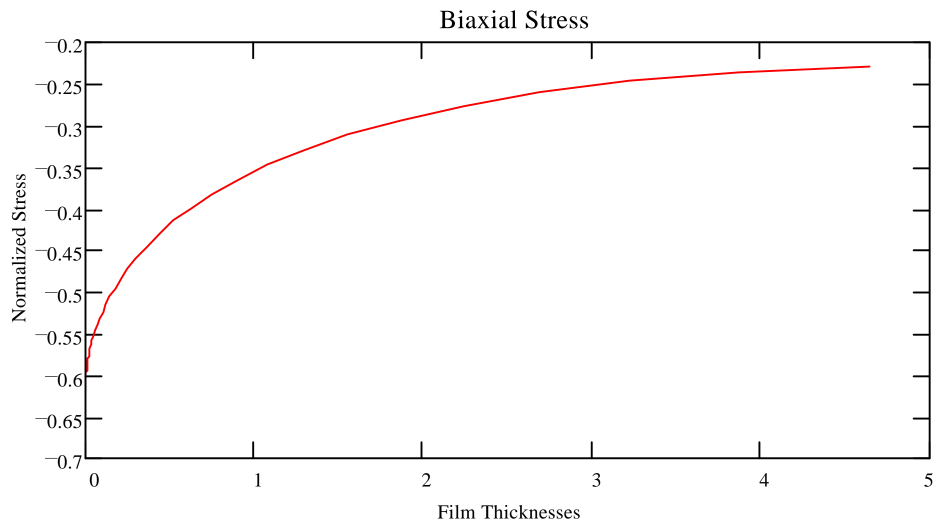

Figure 4-4: Biaxial Stress in a GaAs Substrate due to a SiN Film Edge, using E_f = 200 GPa, ν_f = 0.5, E_s = 89 GPa, and ν_s = 0.244. Normalized stress = σ_s / σ_f.

Superposition of stresses in the active region of the device requires that stress from film edges relatively far from the passivation gate edge be evaluated, since the model

predicts that film edge effects may extend several microns. Figure 4-4 represents the model for normal stress out to about 1 micron, in terms of film thicknesses. Even at 1 micron (for a 2000Å SiN film), the film edge stress is 20% of the film stress. By superimposing all stress from nearby device structures, the total normal stress in the active region of the device is 40% of the film stress, or about 80 MPa. This suggests that the local value of the normal residual stress from all sources (as-grown residual stress ≅ 35 MPa, film edge-stress ≅ 80 MPa, and bending stress ≅ 1 MPa) is about 116 MPa.

NORMAL STRESS DISTRIBUTION NEAR THE GATE

A plot of the superimposed normal stresses, as calculated from our computer model, is shown in Figure 4-5. The edge stress is represented by a red line for the SiN on the left side of the gate, by the green line for the TiWN gate metal, by the blue line for the SiN on the right side of the gate, and by the black line for the superposition of all stresses. The stress is given in units of "normalized stress" so that this plot can be applied to any state of film stress. The materials constants used in this calculation are: E_{SiN} = 200 GPa, ν_{SiN} = 0.5, E_{GaAs} = 89 GPa, and ν_{GaAs} = 0.244, E_{TiWN} = 590 GPa, and ν_{TiWN} = 0.35. The film thicknesses used are: d_{TiWN} = 700Å and d_{SiN} = 2000Å. This plot does not include the contributions from as-grown residual stress and bending moments, which are additive macrostresses. They have the effect of moving the entire plot toward the tensile side for net tensile macrostress and toward the compressive side for net compressive macrostress.

SHEAR STRESS

For dislocation generation and motion, we are interested in the shear stress component, τ_{zx}. In the computer simulation shown in Figure 4-6, the red line represents the stress distribution at 0.2 μm, the blue at 0.1 μm, and the green at 0.05 μm below the surface.

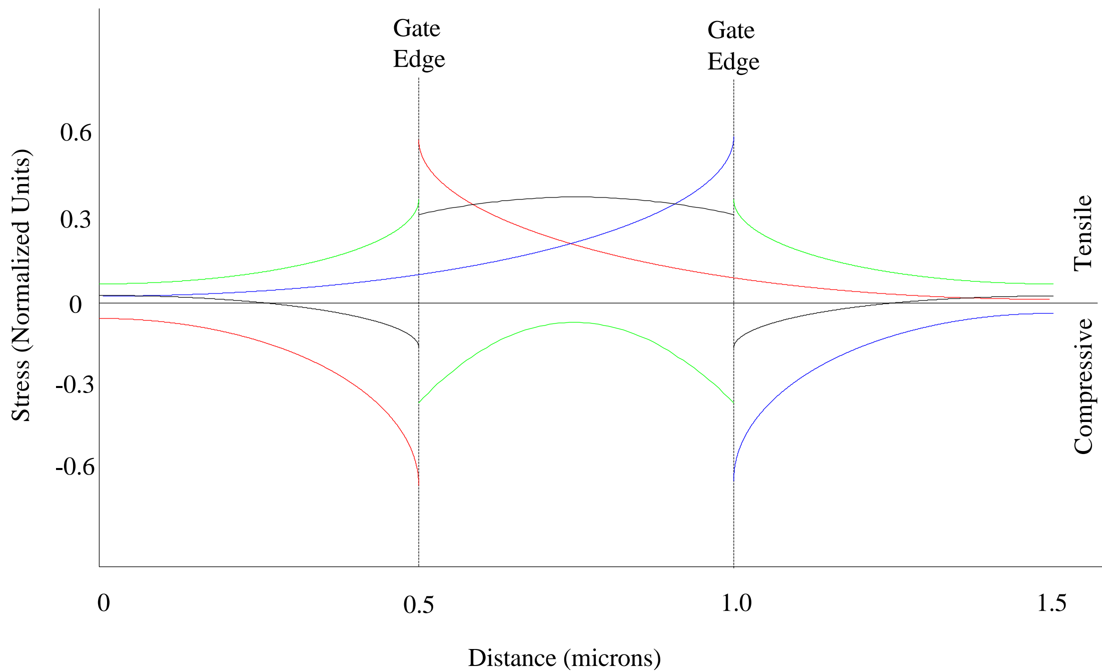

Figure 4-5: Superposition of normal strains in gate-to-drain region. Normalized stress = σ_s / σ_f.

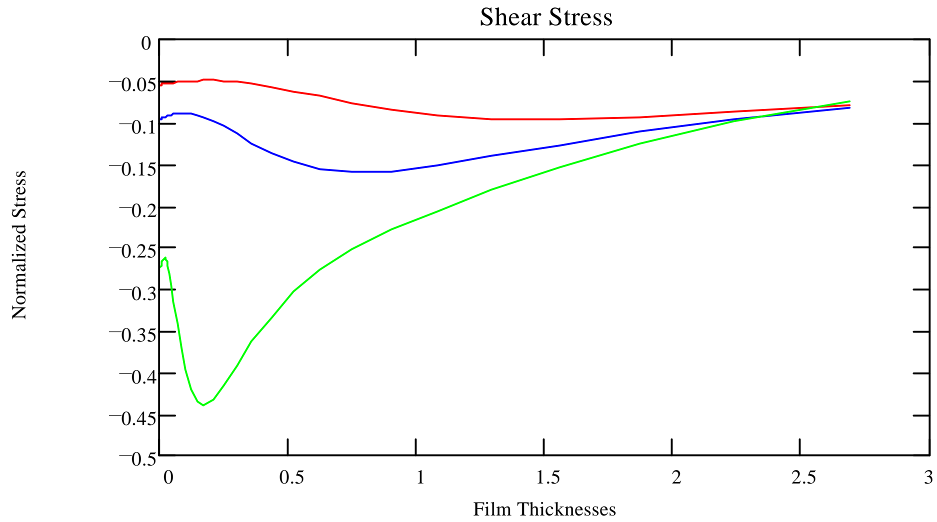

Figure 4-6: Shear stress in a GaAs substrate due to SiN and TiWN film edges, using E_f = 200 GPa, ν_f = 0.5, E_s = 89 GPa, and ν_s = 0.244. Normalized stress = σ_s / σ_f.

The importance of the shear stress is not only in its magnitude, but also in its distribution. The presence of an appreciable shear strain extending several thousand Angstroms from the film edge is necessary for the dislocation and kink motion, as hypothesized by our power slump model. The distributed force model shows that this shear stress is concentrated between 0.1 and 0.6 microns from the film edge at a depth of 0.2 microns below the surface (the depth of the active region). For a typical SiN film stress of 200 MPa, this corresponds to a shear stress between 10 MPa and 16 MPa in the region of interest. This magnitude of shear stress developed in the region near the passivation edge is sufficient to cause dislocation motion in the active region of the device.

4-3 VERIFICATION OF THE STRESS COMPUTER MODELS

Computer models which accurately and precisely describe the state of stress are vital to this investigation (see Chapter 7). Therefore, X-ray topography experiments were performed to independently verify the conclusions of the stress models.

As shown in Chapter 5, rocking curves verify that the GaAs substrates used in these devices are “ideally imperfect”, with respect to their crystalline substructure. Therefore, the width of the region (in terms of 2θ) between no reflected intensity and maximum reflected intensity of the Bragg peak is very narrow, according to dynamical diffraction theory (on the order of 10 seconds of arc). For the GaAs crystals used in this investigation, strains over 87 ppm (a stress of 9.6 MPa) will appear as white regions [6], since this magnitude of strain will cause the local lattice to no longer satisfy the Laue conditions. This contrast is used to verify the computer models of strain distribution near device features.

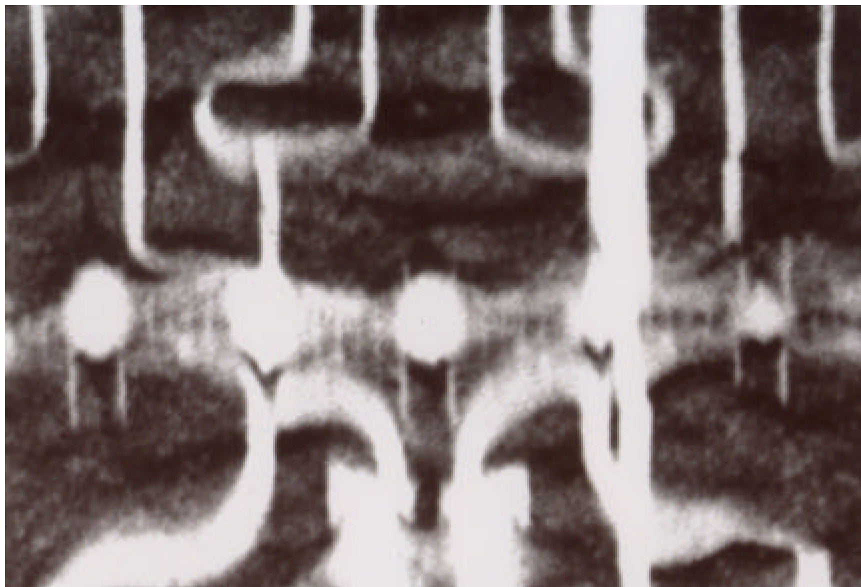

Figure 4-7: Topograph of stress fields around device features. The white regions are stress fields exceeding 10 MPa. The white region running vertically across the image is a crack.

Since the white region of the topograph extends from the device edge until the stress is less than 9.8 MPa, for the film stress of 78 MPa (as measured for this sample), the contrast edge exists in the topograph at a normalized stress of 0.125. As shown in Figure 4-4, our computer model predicts that the strain field in the GaAs substrate from a SiN film edge should extend 4.6 film thicknesses, or 0.92 +/- 0.1 μm. As shown Figure 4-7, the width of the strain field extending from the passivation edge is 0.95 μm. Thus, the topograph verifies the accuracy of the computer simulation, within the uncertainty of the strain field measurement. The same analysis was performed on all devices in this investigation, with similar results. Thus, the computer models used to calculate the stress distribution in the GaAs substrate due to film edge stresses are believed to be accurate.

4-4 CHAPTER REFERENCES

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Chapter 5
Single Crystal X-ray Strain Measurements

Since both device degradation and wafer breakage are believed to be dependent on residual stress, it is critical that a suitable method of stress measurement for single crystal GaAs be found or developed. After an exhaustive literature search, it was found that current methods of stress/strain measurement either cannot be used to study stress as a function of processing, cannot be used to study stress on fully processed devices, or lack the precision required for this work. For example, strain gauge measurements are only suitable for measuring flat surfaces and cannot be used for process-induced stress measurements. This precludes their use on fully processed devices, since the metallization and other structures on the device would interfere with the measurement. Furthermore, the harsh conditions of device fabrication, such as RTA and PECVD, prevent the use of strain gauges for process-induced stress measurements since the device would be altered or destroyed in the process. Plate bending measurements, which use phenomena such as birefringence or light reflection to determine strain, are unsuitable for fully processed chips (due to their small size) and some only provide semi-quantitative information. Other non-contact methods of strain measurement, such as laser reflectivity or acoustic measurements, are generally second order measurements of strain[*] and therefore are subject to fairly large errors (typically exceeding 10 percent of the measured value [1]). These methods become increasingly inaccurate in the presence of non-uniform strains (strain gradients), which are expected to be present in the samples under investigation. Since only a limited number of samples are available, a method of stress characterization with a high degree of precision is desired to ensure statistical significance.

[*] These methods typically measure a materials parameter, such as changes in the index of refraction or the velocity of sound, to deduce strain.

It is well known that X-ray methods provide a first-order method of strain measurement and therefore must provide a higher degree of precision relative to second order methods. Using a typical diffraction geometry and single crystal samples, stresses may be measured using a spot size of 2 mm or less, allowing X-ray diffraction to evaluate stress on a localized scale. However, no suitable technique for measuring the complete state of stress in a single crystal material by X-ray diffraction was found. Strain interpretation by line shape analysis cannot be used for single crystal strain measurements because the peak broadening effect of non-uniform strain only exists for polycrystalline materials. Determining the peak shift of a diffraction line can measure uniform stress, but only represents strain in the direction normal to the crystallographic plane measured. X-ray topographic imaging can be used to qualitatively study the distribution of non-uniform stress, but is not suitable for quantitative evaluation of uniform stress since the angular range over which diffraction occurs is extremely narrow[†]. (Refer to Chapter 3 for more information about imaging strain fields using X-ray topography.)

Due to the lack of a suitable strain measurement technique for single crystals, one was developed as part of this research [2]. Our single crystal strain measurement technique is non-destructive, characterizes the entire stress tensor, measures the near-surface state of stress, and has a precision of 5% or better of the measured value of strain.

The Phi Analysis [3], a technique to insure reliable residual stress data for polycrystalline materials, was adapted to the case of single crystal materials and incorporated into this research. The Phi Analysis was used to insure that the data were not influenced by non-stress effects, such as alignment errors or subgrain misorientation.

[†] Since the Bragg condition is met in only a very narrow angular range for single crystal materials, all but the smallest strains will not result in any diffracted intensity.

Since a suitable technique for measuring uniform and non-uniform strain in the single crystal GaAs samples cannot be found, such a technique was developed as part of this research. The X-ray strain measurement technique for single crystal materials involves several steps:

1. An *assessment of crystalline quality* is used to determine the misorientation between subgrains and the degree of perfection in the single crystal sample using rocking curves. Large subgrain misorientation will result in larger errors by introducing uncertainty in the orientation of the crystallographic planes used to determine strain.

2. An *experimental design* is performed to select the proper combination of diffracting planes. Strain must be determined in a minimum of 6 independent directions, but these independent directions cannot be selected arbitrarily.

3. *Data acquisition* is performed to determine diffraction peak shifts from the stress free value. Profile fitting is used to determine peak location.

4. A *determination of data reliabilty* is performed to determine whether the stress tensor is consistent with strain distribution models and whether the data are affected by non-stress effects. This quality assessment of the data uses the Phi Analysis, modified for the case of single crystals.

5. *Strain gradient corrections* are performed to improve stress distribution interpretation. These corrections are based on the strain distribution models presented in Chapter 4 and on strain distribution models used in polycrystalline residual stress theory.

5-1 ASSESSMENT OF CRYSTALLINE QUALITY

Prior to strain measurements, an assessment of crystalline quality is performed to insure the accuracy of the strain study. Specifically, rocking curve data are generated to determine whether substructure in GaAs single crystals would significantly affect strain measurements. Subgrains may be misoriented relative to one another by as much as ten degrees across the width of the sample. Large subgrain misorientation will cause significant errors in the determination of the stress tensor, because it introduces an error in the true value of the sample orientation relative to the diffraction vector. The reader is referred to a paper by Jo and Hendricks [4], in which this error is derived.

A study was performed to determine substructure effects on the stress characterization of the samples used in this investigation. This study was performed using bare wafers. To extend these results to other samples, the assumption must be made that the subgrain boundaries of the samples are immobile so that the substructure is not affected by the processing conditions endured by the wafer during device fabrication. This is reasonable when one considers that these crystals are ionic/covalent in the nature of their atomic bonding, making the free energy required to move or change the nature of the substructure very large [5][‡].

As shown in Figure 5-1, a rocking curve is obtained by orienting the sample for a Bragg reflection and rotating the crystal about the omega axis. As each subgrain in brought into the proper orientation for Bragg reflection, a plot of intensity versus omega is produced. A crystal with no subgrain misorientation would have a very narrow diffraction peak with a FWHM of less than a few seconds of arc [6]. However, since our diffraction system (a Scintag PTS) uses non-parallel beam optics, the minimum width of the rocking curve may be determined by the detector slit width.

[‡] It will be shown, however, that individual dislocations can move through the crystal lattice under very special circumstances. This does not affect the size or distribution of subgrains, however.

For the 0.01 mm and 0.02 mm slits on the detector, the width of the diffraction peak due to divergence is 0.057 degrees, or 3.42 minutes of arc. Thus, the minimum subgrain misorientation that our system can detect is 0.057 degrees. (Subgrain misorientation does not become significant until it reaches a maximum value of approximately 1.0 degrees, assuming that the subgrains are randomly oriented about the surface normal direction and are small relative to the spot size of the incident beam.)

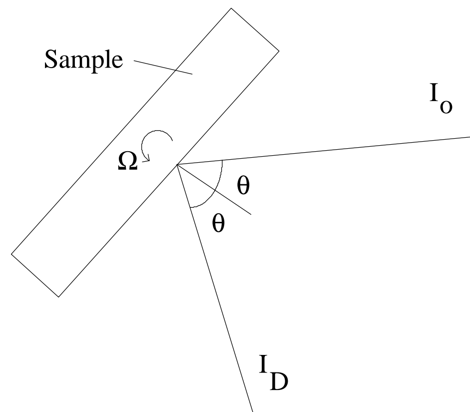

Figure 5-1: Diffraction Geometry for Rocking Curves. I_o = incident beam, I_D = diffracted beam, θ = Bragg angle, Ω = rocking angle.

As long as the maximum subgrain misorientation is less than 0.057 degrees, and is randomly distributed, then at least during some portion of the rocking curve, the entire diffracted intensity from all of the subgrains will be incident on the detector. In this region, the intensity profile as a function of rocking angle will be constant, assuming a uniform intensity distribution from the source. If the intensity distribution from the X-ray source is not uniform, as is usually the case, variation in the otherwise constant intensity region of the rocking curve will be observed. This variation is primarily due to the polycrystalline nature of the target and the use of non-parallel beam optics. Thus, even if the subgrain structure is perfectly randomly distributed with respect to misorientation, intensity variation will be observed in the rocking curve. The variation

of intensity from the incident beam can be distinguished from true subgrain effects since the variation from the source will be the same for all samples.

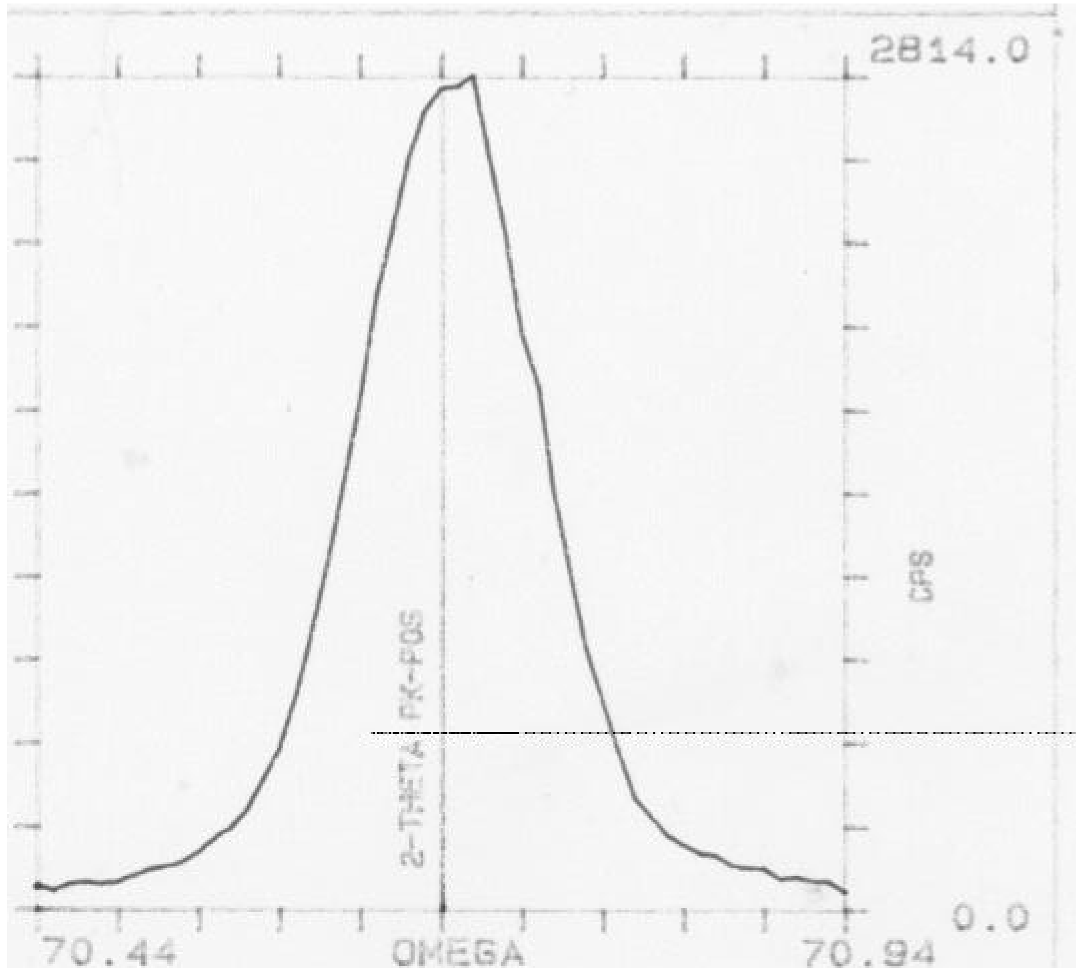

Figure 5-2: Typical Rocking Curve Data for the GaAs samples used in this investigation.

All rocking curves measured for a variety of bare and passivated samples are identical to Figure 5-2. The rocking curve width of Figure 5-2 shows that the subgrains in all samples measured are not sufficiently misoriented to cause significant error in macrostrain calculations. As previously discussed, the small variations in the regions of maximum intensity are due to intensity variation from the source.

In addition to the rocking curve measurement, a measurement of the diffracted integrated intensity relative to the incident beam was made. This information, in combinaiton with topographic data, can be used to determine the degree of perfection in the single crystal, and therefore, determine the effective sampling volume of the stran measurement technique. The goniometer was moved to $\theta = 0$ so that the incident beam directly entered the detector, and the incident intensity was measured. A GaAs sample was then placed in the sample holder and the goniometer moved to $2\theta=126.65^o$, which is the Bragg angle for the 533 plane. The data for the experiment are shown in Table 5-1. Relatively large detector slits were used to insure that the entire diffracted beam was measured.

Table 5-1: Data for Diffracted Intensity Experiment. I_d is the diffracted intensity from the 533 plane and I_o is the intensity from the incident beam ($Cu_{K\alpha}$). Slit widths: source side, 0.2 mm, 0.1 mm, detector side: 0.5 mm, 0.3 mm.

SAMPLE	Passivation	I_D/I_o
1	Bare	0.45
2	Bare	0.39
3	Bare	0.41
4	Bare	0.50
5	Bare	0.41
6	2000Å SiN	0.35
7	2000Å SiN	0.38
8	2000Å SiN	0.55
9	2000Å SiN	0.42
10	2000Å SiN	0.46

The data show that the value of I_d/I_o is 0.43 ± 0.04, and that there is no significant difference between the bare and passivated wafers, with respect to diffracted intensity.

Theoretically, the diffracted intensity from an ideally imperfect crystal is 100% of the incident beam. The diffracted intensity from an ideally perfect crystal is approximately 10% of the diffracted beam. The value for our crystals is approximately 43% of the incident beam, indicating that primary or secondary extinction is occurring. The

topograph in Figure 5-3 shows that the average subgrain size is approximately 70 μm. This is a relatively large subgrain size, indicating that primary extinction is likely to occur. Since the misorientation of the grains is known to be less than 3.4 minutes of arc by our rocking curve data, it is likely that secondary extinction is not as great a factor as primary extinction.

Figure 5-3: Topographic Image of Typical Substructure for GaAs.

Since primary extinction is apparently significant, the diffracting volume is limited to the near surface region of the material (less than roughly one micron) by attenuation in the dynamically diffracting regions. In the regions near subgrain boundaries,

kinematical diffraction theory applies, meaning that the sampling volume of the measurement is roughly 20 microns. The subgrain boundary width, as seen in Figure 5-3, is typical around 3 μm. Since the subgrain radius is about 35 μm, the percent of kinematical diffraction in the diffracted beam should be about 8%. Thus, approximately 92% of the diffracting volume depth is determined by attenuation. This effectively limits the surface stress measurement to a depth of about 0.2 μm for GaAs.

5-2 EXPERIMENTAL DESIGN FOR STRAIN MEASUREMENTS IN SINGLE CRYSTAL GaAs

Strain is determined by measuring the location of the diffraction peak for an hkl plane and subtracting the measured value from the stress free value. After applying the appropriate direction cosines, the data from several hkl planes are used to calculate the strain tensor.

To maximize peak shift sensitivity to strain, high θ angles should be used. This can be shown by differentiating of Bragg's Law and finding the maximum value of $\Delta\theta$.

$$\lambda = 2d \sin\theta,$$

$$0 = 2\Delta d \sin\theta - 2d\Delta\theta\cos\theta,$$

therefore,

$$\Delta\theta = \Delta d/d \tan\theta = \varepsilon\tan\theta$$

For a given strain, $\Delta\theta$ becomes larger as $\tan\theta$ becomes larger. With this in mind, high index planes were selected for strain measurement. Table 5-2 shows the planes selected to determined the strain tensor for all samples in this investigation.

Table 5-2: Goniometer angles for various planes in a (100) oriented crystal

Plane	2θ	χ	Φ
(444)	141.406	54.74	45
(4-44)	141.406	54.74	135
(44-4)	141.406	54.74	225
(4-4-4)	141.406	54.74	315
(533)	126.653	40.32	45
(5-33)	126.653	40.32	135
(53-3)	126.653	40.32	225
(5-3-3)	126.653	40.32	315
(620)	119.048	18.43	0
(6-20)	119.048	18.43	90
(260)	119.048	71.565	180
(2-60)	119.048	71.565	270

Although 6 independent directions must be measure to determine the 6 values of the strain tensor (in cubic systems), the planes must be selected such that the strain tensor is calculated from data representative of the normal and shear strains. For example, if the planes were selected such that all phi values were n + 90°, where n is an integer, then only strain in orthogonal directions is represented. In this case, the shear strains would not be correctly calculated. To minimize errors, at least one third of the planes selected should be different from the others by 45° in the phi direction.

The number of planes which must be measured beyond the minimum (6 for cubic systems) is a function of the goniometer and sample alignment precision, and the counting statistics error. For the instrument used in this study, goniometer and sample

alignment uncertainty were not found to cause significant error. Reflections of the higher order peaks were of sufficient intensity to make the counting statistics error 7 ppm or better. The excellent separation of $K_{\alpha 1}$ and $K_{\alpha 2}$ for all diffraction peaks measured made a Stokes correction unnecessary, thus improving peak position calculations. Due to the shape of the diffraction peaks, a Pearson-VII profile fitting routine was used to determine peak position.

A total of 12 independent directions were measured (see Table 5-2), resulting in a maximum mean error of 5.3% of the value of any component in the strain tensor. It was determined experimentally that the improvement in precision by measuring more than 12 planes did not warrant the additional time required to run the experiment. Analysis of the data was performed on a personal computer using routines developed by the authors in the software package MathCad 6.0.

As part of these computer analyses, the least squares method [7] was used to calculate the strain matrix. For a set of *n* linear equations, the following matrix notation may be used:

$$\mathbf{F}_{n,1} = \mathbf{A}_{n,m}\mathbf{X}_{m,1} + \mathbf{E}_{n,1}$$

where $\mathbf{F} = \varepsilon_{33}$ in the laboratory coordinate system, $\mathbf{A}$ is the design (transformation) matrix, $\mathbf{X}$ is a vector representing the six components of the strain tensor, and $\mathbf{E}$ represents measurement error. The components of the design matrix are the terms in the well-known strain equation given by Noyan and Cohen [8]:

$$\varepsilon'_{33} = (\varepsilon_{11}\cos^2\Phi + \varepsilon_{22}\sin^2\Phi + \varepsilon_{12}\sin 2\Phi)\sin^2\Psi + (\varepsilon_{13}\cos\Phi + \varepsilon_{23}\sin\Phi)\sin 2\Psi + \varepsilon_{33}\cos^2\Psi$$

Thus, $\mathbf{A}_{11} = \cos^2\Phi \sin^2\Psi$, and so forth. For the special case of single crystals, the design matrix is determined by the crystallographic orientation of the measured planes, rather than the reflections obtained from randomly oriented grains and goniometer

position, as is the case for polycrystalline measurements. However, if significant substructure had been found in the rocking curve measurements, then the design matrix would have to include the measured deviations, $\Delta\Psi$ and $\Delta\Phi$, due to subgrain misorientation - similar to the polycrystalline case. The greater the subgrain misorientation, the greater the error in calculating macrostrain, as the microstrain measurement of significantly misoriented subgrains no longer approximates macrostrain. Fortunately, the wafers measured in this study did not show significant subgrain misorientation, as previously discussed.

To determine the estimates of strain using the least squares treatment,

$$\mathbf{X} = (\mathbf{A}^T\mathbf{P}\mathbf{A})^{-1}\mathbf{A}^T\mathbf{P}\mathbf{F}$$

which requires calculating the inverse of a function of the design matrix ($\mathbf{P}$ is the weight matrix[§]). This leads to the aforementioned point about the selection of planes used to determine strain: a combination of planes must be selected such that all components of the strain tensor are represented. If this is not the case, a column of zeros exists in the design matrix, which results in a singularity when the design matrix is inverted. Thus, planes must be selected such that for all {hkl}planes measured, the Φ direction is different by 45° for at least one third of the planes. For example, although the {444} and {533} planes are not different in Φ in the kl plane, the {620}planes are, resulting in a representative design matrix.

5-3 DATA ACQUISITION (AN EXAMPLE)

The example given in this section is representative of all single crystal strain measurements performed in this research. The presentation and analysis of these data

[§] The data are assumed to be normally distributed with equal variances, and thus $\mathbf{P} = \mathbf{I}$.

is given in Chapters 7 and 8 in the context of the wafer breakage and device degradation studies.

Table 5-3 is raw data from a SiON passivated GaAs sample. Stress-free values were obtained from the JCPDS card file.

Table 5-3: Stress Measurement Example Data

Plane	Stress-free 2θ	Measured 2θ	χ	Φ
(444)	141.406	141.463	54.74	45
(4-44)	141.406	141.472	54.74	135
(44-4)	141.406	141.328	54.74	225
(4-4-4)	141.406	141.337	54.74	315
(533)	126.653	126.681	40.32	45
(5-33)	126.653	126.599	40.32	135
(53-3)	126.653	126.677	40.32	225
(5-3-3)	126.653	126.584	40.32	315
(620)	119.048	119.101	18.43	0
(6-20)	119.048	119.003	18.43	90
(260)	119.048	119.111	71.565	180
(2-60)	119.048	119.021	71.565	270

The resulting stress tensor is:

$\sigma_{11} = 20$ $\sigma_{12} = 1.2$ $\sigma_{13} = 2.3$

$\sigma_{21} = 1.2$ $\sigma_{22} = -21$ $\sigma_{23} = -1.7$

$\sigma_{31} = 2.3$ $\sigma_{32} = -1.7$ $\sigma_{33} = 5.0$

where all values are in MPa.

The stress tensor is found by multiplying the strain tensor by the stiffness coefficient tensor [9]. These elastic constants have less than a 5% error on any one value, which is not incorporated into the calculation of the error matrix. A 5% maximum error in the elastic constants result in an 8% maximum error in the stress tensor, which is suitable for our purposes.

5-4 DETERMINATION OF DATA RELIABILITY

The Phi Error Analysis for single crystals was applied to the data. The Phi Error for the previous example was found to be 1.3 MPa. Care was taken to properly align the sample and goniometer, which indicates that the main contribution to the phi error is from a non-representative diffracting volume. It is believed that the differences in the effective depth of penetration between the regions of the crystal which dynamically and kinematically diffract are the primary contributor to the Phi Error.

It should be noted that the magnitude of the Phi Error is not related to the error bars of the measurement. It is only an indicator of the differences in the quality of stress measurements among samples. In this investigation, the Phi Error is consistently between 8 and 14 MPa, indicating that all samples are aligned to the same degree and that it is reasonable to compare stress data between any two samples. If a large variation in the Phi Error were to be found, that would indicate that the samples are either not consistently and properly aligned or that the nature of the material changes significantly (e.g., different subgrain structures among wafers).

The stress tensor calculated in the example of the previous section indicates a compressive stress in one direction and a tensile stress in the other. This hyperbolic

paraboloid shape (i.e., a potato chip shape) is found in nearly every wafer measured. This stress distribution has also been qualitatively observed by other experts in the industry (I. C. Noyen, private communication), and is due to residual stress from wafer processing.

5-5 STRESS GRADIENT CORRECT IONS

Since the measurement presented in this chapter was performed such that the diffracting volume was in the middle region of the wafer, no film edge effects are expected for this sample. Therefore, the only stress gradients expected are from bending moments in the wafer (refer to Chapter 4). Since the majority of the diffracting volume has been determined to be within the first 0.2 μm due to attenutation effects, the stress gradient from bending moments will not significantly alter the stress data. In this case, the assumption made is that the variation in stress within the diffracting volume is minimal.

However, as shown in Chapter 4, stresses can vary quite significantly within the first 0.2 μm of the sample surface in the vicinity of device features due to film edge stresses. The stress distribution in these regions can create stress gradients in the x-y plane as well as in the z-direction. Correcting the data for the presence of these gradients requires introducing a additional terms into the stress equation [10].

$$\varepsilon'_{33} = \varepsilon_{ij}\ (z=0) + K_{ij}\tau^{n_{ij}}$$

where K and n are constants related to the magnitude and variation of the stress distribution and τ is the effective depth of penetration of the X-ray beam. For dynamically diffracting regions, τ is the attenuation coefficient. Since the depth of penetration for dynamically diffracting regions is small, gradients in the z-direction

will not vary significantly, making the value of K small, and therefore having a minimal effect on the stress tensor. Gradients in the x-y plane, however, may substantially affect the results.

The effect of strain gradients is determined by integrating, over the diffracting volume, the difference between the measured strain (uniform strain plus strain gradient effects) and the strain gradient calculated by theory. The distribution of stress gradients around device features, and the topographic technique to verify the accuracy of the computer models, was previously described in Chapter 4.

Since the device structures are the same for all fully processed chips, the strain graident distributions should be the same (this does not imply, however, that the magnitude of the stresses will be the same). Thus, once the correction for strain gradient effects is made, it can be applied to all devices if the absolute value of the stress gradient is known. The absolute value of the stress gradient can be determined by topographic imaging, as described in Chapter 4. For the devices measured in this investigation, the change in stress in the normal direction (Φ=0) is typically 12% of the measured value. The change in the stress in the shear direction is typically 15% of the measured value for the same conditions of beam size and location. All stress values presented in Chapters 7 and 8 are corrected for the stress gradient effect, where appropriate.

5-6 CHAPTER REFERENCES

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Chapter 6
Dislocation Motion in GaAs

This chapter presents the theories of dislocation structure and motion in GaAs relevant to this research. It is shown that, even near room temperature, rapid dislocation motion is possible under certain conditions. High doping levels, high electron flux, and high shear strain reduce the energy barrier to kink formation and motion, increasing the velocity of dislocations and forming deep levels in the bandgap of GaAs. These deep level energy states are hypothesized to be the generation/recombination centers described in Chapter 2. Experimental values presented in this chapter are from several independent studies of dislocation behavior in GaAs which investigate such phenomena as the effects of doping on the hardness of GaAs wafers [1], the influence of photon flux on LED and laser degradation [2, 3], and the effects of applied stress on dislocation structures [4]. While this investigation does not attempt to repeat these well-established results, it does assimilate these findings into the new theories proposing that wafer breakage and device degradation are dependent on the behavior of dislocations during passivation processing and device operation.

A key element missing from the literature is a correct evaluation and interpretation of the stresses which exist in the active region of the devices under investigation. Because the literature investigations are mostly scientific research (rather than engineering research), the results are presented in terms of general trends of dislocation behavior as a function of stress. This generalization of the results is primarily due to lack of knowledge of the state of stress in a particular device structure or materials interface and the need to make the results universally applicable. Since the state of stress in the wafers and devices under investigation has previously been discussed, imaged, modeled, and measured in Chapters 3, 4, and 5, the results of the

literature investigations can be interpreted more exactly in the context of power slump and wafer breakage, which will be presented in Chapters 7 and 8.

6-1 DISLOCATION STRUCTURES IN GaAs

Normally, dislocations form in GaAs primarily as a result of the thermal stresses developed during processing of the single crystal boule and the subsequent sawing, grinding, and polishing operations used to create the wafer. Several investigations [5, 6, 7] have identified that the stable dislocations in GaAs are 60° dislocations with a Burgers vector of <110>. These dislocations are known to dissociate into 90° and 30° Shockley partials, which is typical of other materials which have the FCC structure (refer to
Figure 6-1). Dislocations primarily move on the glide set of the {111} family of planes. Because GaAs is a compound, two types of dislocations exist, α and β dislocations, with the α-dislocations ending on a plane of Ga atoms, and the β-dislocations ending on a plane of As atoms.

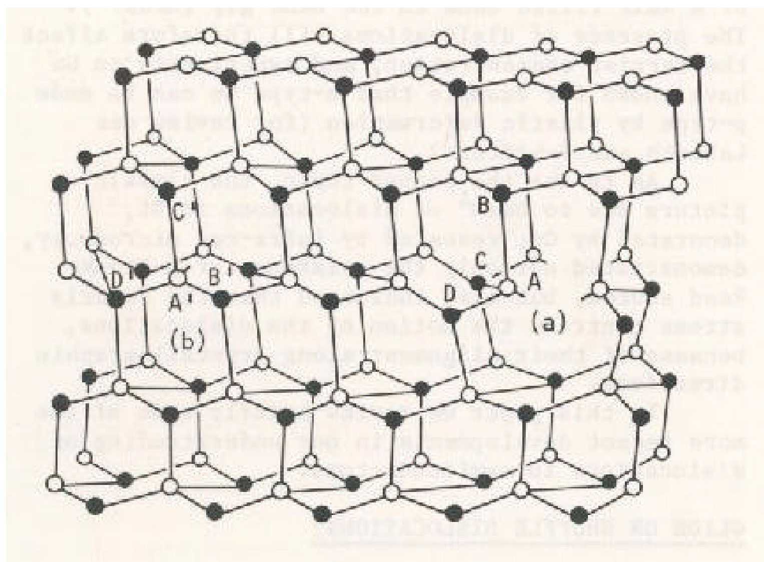

Figure 6-1: Dislocation structures in GaAs; (a) a 90° partial, (b) a 30° partial [1].

6-2 DISLOCATION MOTION IN GaAs

Dislocations in GaAs move through the lattice by overcoming the Peierls barrier [8]. This barrier can be effectively reduced in the presence of an applied stress, high electron flux, and high doping levels. This section will discuss these phenomena in the context of the devices and wafers under investigation.

STRESS EFFECTS ON THE EFFECTIVE PEIERLS BARRIER

Dislocation motion in GaAs, for temperatures less than approximately $0.6T_m$, is determined by the Peierls potential energy barrier. As a dislocation attempts to move along a glide plane, it periodically encounters rows of like atoms which repel the moving dislocation by electrostatic force. To continue motion in the same direction, the dislocation must overcome this electrostatic repulsion, which is the basis for the Peierls barrier.

In FCC lattices, a dislocation can reduce its free energy by dissociating into Shockley partials; in this case, a 60° dislocation will dissociate into 90° and 30° partials. Because these partials are separated, they will encounter the Peierls potential at different times during movement over the barrier [9]. If the partials are separated by an integer number of the distance between the maxima in the Peierls potential, both partials will attempt to surmount the barrier at the same time, requiring twice the energy of the Peierls potential. Thus, the effective Peierls barrier has been increased. Conversely, if the partials are separated by a distance equal to $a(n + 1/2)$, where a is the distance between the maxima of the Peierls potential, as one partial moves down the potential barrier, the other partial moves up, thus forming a saddle point in the effective Peierls potential (refer to Figure 6-2). Thus, because of the formation of

Shockley partials, the effective Peierls barrier is reduced, resulting in increased dislocation velocity*.

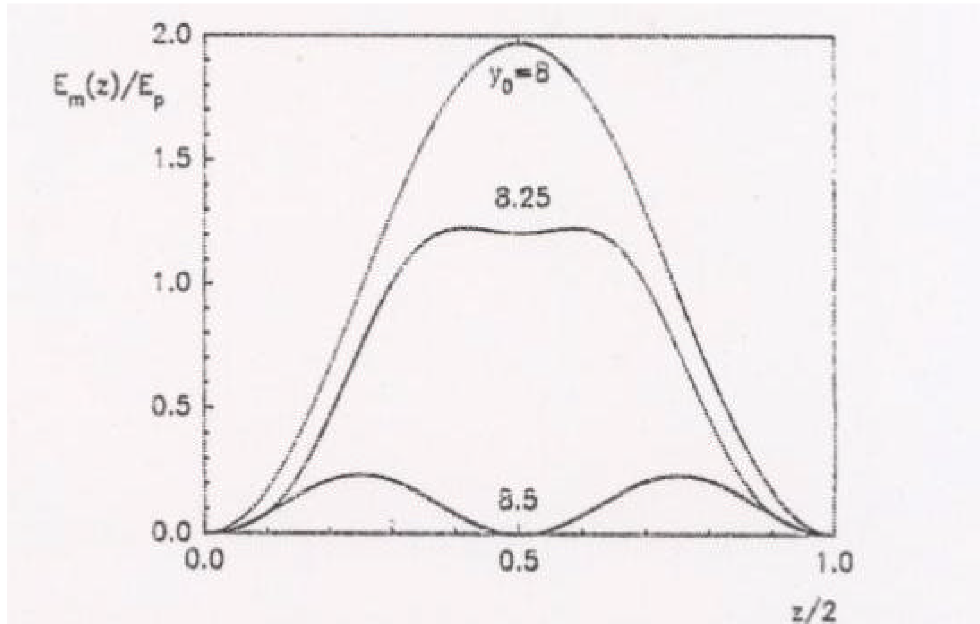

Figure 6-2: Energy diagram of the effective Peierls potential as a function of separation distance between Shockley partials in a covalently bonded FCC crystal. E_p is the Peierls potential and E_m is the effective Peierls potential, z/2 is the position of the dislocation as it moves from one Peierls valley to another, and y is the separation distance between partials [8].

Schoek [8] has shown that the separation distance of the partials can be changed in covalently bonded materials (such as GaAs) when the applied stress is greater than 10^{-4} μ, where μ is the shear modulus (47 GPa for GaAs). Unfortunately, no data is available for the separation distance in GaAs. This is not surprising since the change in separation distance is on the order of half the Burger's vector of the dislocation, which in this case, is only 2 Å. Even the most sophisticated experiments have difficulty in resolving changes in the separation distance of partials on this scale.

* As will be discussed later, an increase in dislocation velocity also corresponds to an increase in the kink formation rate in materials such as GaAs. This is important for the power slump model discussed in Chapter 7.

However, although the exact separation distance is unknown, it is estimated by Shoeck [9] that if the applied shear stress is greater than 4.7 MPa in GaAs, the separation distance between partials will be changed by at least one-half the distance between the valleys of the periodic potential. This implies that in a region which contains a stress gradient varying from zero to 4.7 MPa, the effective potential barrier will be reduced below the Peierls potential at some location in the region. For example, referring to Figure 6-2, the maximum of the effective potential barrier is twice the Peierls barrier for the stress-free separation distance (corresponding to $y = 8.0$ Å and $z/2 = 0.5$). For an applied stress of $\tau = 4.7$ MPa, the separation distance should increase by half the distance between Peierls valleys, corresponding to a separation distance of $y = 8.5$ Å. The effective potential barrier reaches a maximum of approximately 1/4 the Peierls barrier at $z/2 = 0.25$ for this partial dislocation separation distance. Thus the effective barrier to dislocation motion has been reduced by a factor of 8. In the devices under study, between 0.01 and 0.2 μm from a SiN film edge, shear stress values typically exceed 4.7 MPa from the surface to a depth of 0.15 μm. This implies that the potential barrier to dislocation motion (which is approximately equal to the kink formation energy) is reduced by approximately a factor of eight somewhere in the channel region within 0.2 μm from a SiN film edge.

KINK FORMATION AND MOTION IN GaAs

Since it is unlikely that an entire dislocation line will attain enough energy to overcome the Peierls barrier at every point along its length, the dislocation moves in a piecemeal fashion by the formation of double kink pairs. The segment of the dislocation line that has surmounted the effective Peierls barrier will attempt to increase its length parallel to the dislocation line by kink motion in this direction, as shown in Figure 6-3. Thus, both kink nucleation and kink motion contribute to the velocity of the dislocation through the crystal.

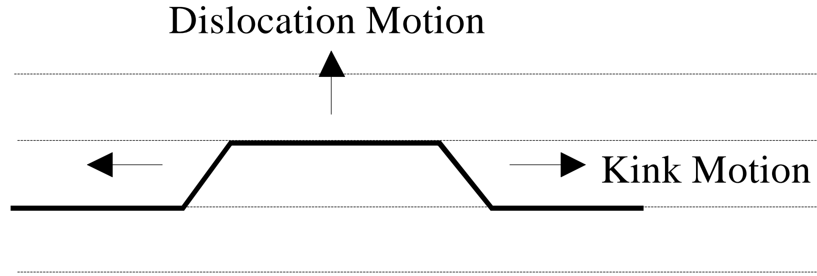

Figure 6-3: Dislocation motion by kink pair nucleation and motion [1].

Kink nucleation and movement involve only a few atomic rearrangements, and thus can be modeled using diffusion theory. Kink velocity is given by [10]

Equation 6-1

$$v_k = \mu\tau ab/kT$$

where μ is the kink mobility, τ is the stress, a is the lattice period, and b is the Burgers vector. The kink mobility is given by

Equation 6-2

$$\mu = \kappa aD/E_k$$

where κ is the "line tension" of the dislocation, D is the atomic diffusion coefficient, and E_k is the energy of the kink. The line tension is given by

Equation 6-3

$$\kappa = \frac{\mu_o \cdot b^2}{4 \cdot \pi} \cdot \left(\frac{1+\nu}{1-\nu} \cdot \ln\left(\frac{\lambda}{3.56\pi \cdot \rho^c} \right) - 0.5 \right)$$

where μ_o is the shear modulus, ν is Poisson's ratio, λ is the distance between Peierls valleys, and ρ^c is the dislocation core parameter given by

Equation 6-4

$$\rho^c = \frac{1}{2} \cdot d \cdot e^{-\frac{3}{2}}$$

where d is the core diameter. The value of d is estimated to be $d = b(1-\nu)/2$. E_k in Equation 6-2 is given by

Equation 6-5

$$E_k = \frac{2 \cdot \kappa \cdot D}{\nu_D \cdot b} \cdot e^{\frac{E_{km}}{k \cdot T}}$$

where E_{km} is the energy barrier to kink motion, also known as the secondary Peierls potential. The velocity of the dislocation is given by

Equation 6-6

$$v_D = b \cdot \sqrt{J \cdot v_k}$$

where J is the kink nucleation rate given by

Equation 6-7

$$J = \frac{2 \cdot \nu_D \cdot \tau \cdot b^2}{k \cdot T} \cdot e^{\left(\frac{-E_{kf}}{k \cdot T}\right)}$$

where ν_D is the Debye frequency and E_{kf} is the energy of kink formation, which is equal to the Peierls barrier under stress-free conditions. Under applied stress, the kink formation energy is modified as

Equation 6-8

$$E_{KF} = (E_{KF})_{\tau=0} - (\mu_o \tau b^3 d^3 / 2\pi)^{1/2}$$

where d = b(1-ν)/2 and τ is the applied shear stress. Solving for v_D,

Equation 6-9

$$v_D = \frac{\nu_D \cdot \tau \cdot b^4}{k \cdot T} \cdot e^{-\left(\frac{E_{kf} + E_{km}}{2 \cdot k \cdot T}\right)}$$

For ionic/covalent materials, such as GaAs, the dislocation velocity is primarily determined by the kink nucleation rate, as the barrier to kink motion is rather high (approximately 2 eV [11]).

DOPING EFFECTS ON DISLOCATION VELOCITY

Dislocation velocity increases as a function of doping level in many semiconducting materials, including GaAs. Other investigations [10, 14] have shown that the effect is not dependent on the dopant used, but rather, on the resulting position of the Fermi energy. The increase in dislocation velocity is believed to be due to the change in the electrostatic force between charged kinks and atoms in the lattice. For the case of n-type GaAs, it is assumed that the concentration of positively charged kinks is negligible, and the ratio of negatively charged kinks to neutral kinks follows Fermi-Dirac statistics as shown by Equation 6-10,

Equation 6-10

$$\frac{c^{neg}}{c^{o}} = \exp\left(\frac{E_F - E_{kink} - eV}{kT}\right)$$

where E_F is the Fermi energy, E_{kink} is the energy level associated with kinks that trap electrons, and eV is the electrostatic energy of the charged dislocation. Thus, the concentration of charged kinks is dependent on the doping level via the Fermi energy. At high stresses and/or low temperatures (<0.6 T_m), the velocity of the dislocation is controlled by the concentration of kink pairs, and therefore,

Equation 6-11

$$\frac{v^{neg}}{v^{o}} = \exp\left(\frac{E_F - E_{kink} - eV + \Delta E}{kT}\right)$$

where ΔE is the difference in the energy of migration of kinks on the dislocation between neutral and negatively charged kinks. For n-type GaAs, the activation energy for Equation 6-11 was found to be 1.0 eV for α-dislocations [1, 14]. Here, the values for eV and ΔE are not reported, but thought to be small. Under different experimental conditions, eV is found to have different values, making an exact determination difficult. For E_F = 1.42 eV, and E_{kink} on α-dislocations = 0.7 eV, ΔE is determined to be approximately -0.58 eV. The increase in dislocation velocity due to doping effects is approximately a factor of 10^2 for $N_D = 5 \times 10^{17}$ /cc. Using a dislocation velocity of 5×10^{-10} cm/s for the intrinsic material, this corresponds to a dislocation velocity of 5.3×10^{-8} cm/s for n-type doping.

It should be noted that the dissociation of 60° dislocations into partials requires that separate E_{kink} values be considered for kinks on 30° and 90° partials. For α-dislocations, E_{kink} for both types is thought to be near the center of the bandgap, giving an average value of approximately 0.7 eV . However, for β-dislocations, E_{kink} is thought to be small for 90° partials. Since the energy level for the kink is not near the center of the bandgap, it is not an efficient trapping center, thus making the doping effect on β-dislocations negligible [10].

6-3 RADIATION ENHANCED DISLOCATION GLIDE

Radiation enhanced dislocation glide (REDG) is a well-studied phenomenon [11, 12, 13, 14] in which dislocation velocity is increased in certain semiconducting materials when these materials are exposed to high electronic or photonic flux. Since this effect is only known to occur in covalent or ionic/covalent semiconductors, the dominant mechanism for the observed increase in dislocation velocity is thought to involve the formation of kinks.

Experimentally, the dislocation velocity is described by Equation 6-12 [14].

Equation 6-12

$$v_{disl} = v_D + \eta v_R \exp(-(U-\delta E)/kT)$$

where the first term represents the velocity of dislocations due to thermal energy, η is an efficiency factor (<1), v_R is the recombination rate, and δE is the energy released upon capture of a carrier inducing defect motion. Microscopically, the second term in Equation 6-12 represents a mechanism in which carriers are captured at a potential kink site and the absorbed energy is transferred to the local lattice, thereby reducing

the effective energy barrier to kink nucleation. This model makes two major assumptions. First, it is assumed that the energy level of the kink exists near the middle of the bandgap so that the carrier capture process is highly efficient. Second, the energy absorbed by the capture process can be efficiently transferred to the lattice in the specific vibrational modes to influence kink motion. Regarding the first assumption, the energy level for kinks on α-dislocations in GaAs is 0.7 eV, satisfying the requirement for the presence of a mid-bandgap energy level associated with the defect. Regarding the second assumption, Sumi [cited in 14] solved the complex problem of the distribution of vibrational modes around a defect in III-V compounds using numerical methods, and found that for GaAs (and several other semiconductors) are well suited for such an energy transfer. Thus, the second assumption is also satisfied.

Experimentally, several investigators have found a linear relationship between dislocation velocity and irradiation intensities. Some consistent findings of these investigations are [14]:

1. Dislocation velocity enhancement is only present during the irradiation. Thus, the REDG effect does not permanently change the nature of the material.

2. The reduction in activation energy is not a function of irradiation intensity. This implies a fixed amount of energy transfer occurs to cause the effect. This is consistent with the supposition that the energy absorbed by the trapping center reduced the effective energy barrier to dislocation motion.

3. The dislocation velocity increase due to irradiation is not a function of doping levels. (However, this does not imply that doping levels cannot reduce the energy barrier to kink motion by other mechanisms.)

4. Only kink formation is enhanced by irradiation, not kink motion.

For the conditions found in the devices and wafers under investigation, the REDG effect has been shown to increase dislocation velocity linearly with electron flux intensity by more than 5 orders of magnitude. For the devices under investigation, even the gate generation current of typically 2000 μA is sufficient to increase the dislocation velocity in the depletion region of the device by 5 orders of magnitude at a shear stress of 26 MPa. This corresponds to a remarkably high dislocation velocity of 10^{-2} cm/s. The magnitude of the channel current density is even higher, and therefore dislocation velocity in the channel must be even higher than in the depletion region [†].

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[6] Ibid., Hirsch, pp. 343 - 344.

[7] Kovacs, I. and Zsoldos, L., *Dislocations and Plastic Deformation*, Permagon Press, New York, 1973, pp. 168 - 183.

[†] The REDG effect must saturate when the electron flux provides more carriers than can be trapped at dislocation sites, so it is unlikely than the linear relationship between dislocation velocity and electron flux holds in the channel where current densities are several orders of magnitude higher than in the depletion region.

[8] Schoeck, G. and Püschl, W., “Dissociated Dislocations in the Peierls Potential,” Materials Science and Engineering, A189, 1994, pp. 61 - 67.

[9] Ibid.

[10]Maeda, K., et. al, “Radiation Enhanced Dislocation Glide and Rapid Degradation,” Mat. Res. Soc. Symp. Proc., v. 184, 1990, pp. 69 - 80.

[11]Ibid., Hirsch.

[12]Ueda, O., “Device Degradation in III-V Semiconductor Lasers and LEDs,” Mat. Res. Soc. Symp. Proc., v. 184, 1990, pp. 125 - 134.

[13]Chu, S.N.G., “Defect Mechanisms in Degradation of Long Wavelength Laser Diodes,” Mat. Res. Soc. Symp. Proc., v. 184, 1990, pp. 135 - 143.

[14]Ibid., Maeda.

Chapter 7
Power Slump Model

A model to explain power slump is developed in this chapter. Ideality measurements, X-ray topographic images, and stress analysis are used to support the model. Comparisons between the predicted power slump and the measured power slump show that the model is accurate within the error bars of the predicted values.

7-1 EVIDENCE OF GENERATION CENTERS BY IDEALITY MEASUREMENTS

The output power of the devices under investigation is stable up to a critical value of the gate-to-drain bias voltage. Beyond this critical voltage, the device exhibits power slump. Electrical tests for several devices have shown that the major symptom of power slump is an increase in the current flowing from the gate region, as depicted in Figure 7-1.

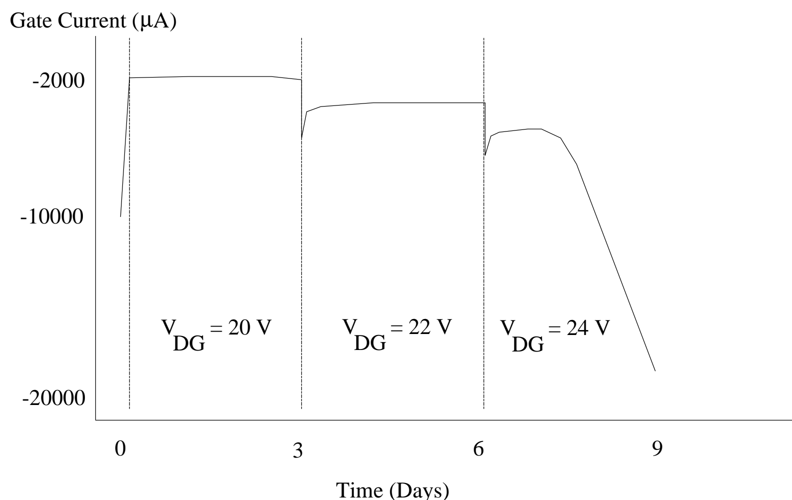

Figure 7-1: Gate current of a typical device during lifetesting. The rapid increase in the magnitude of the gate current in the region labeled V_{DG}=24 V is the major symptom of power slump.

In the power slump region, the thermionic current should be constant and the generation component should initially be approximately 2000 μA, based on calculations presented in Chapter 2. However, it is observed that after an initial transient region, the magnitude of the generation component of the gate current increases linearly with time, implying that the number of generation centers must increase linearly with time. A typical power slumping device shows an increase in the gate current by 6000 μA over 64 hours. This requires the formation of roughly 10^{19} /cc new generation centers during the power slump test - a number five orders of magnitude greater than the estimated pre-power slump value. It is difficult to explain how such a large value of new generation centers could be produced if the generation centers are point defects, especially since the energy level of these generation centers must be near the center of the bandgap, as discussed in chapter 6. It is also difficult to explain such a large value of new generation centers from an increase in the surface state concentration (as other authors have suggested [1, 2]), since the value of the surface state concentration would have to be approximately 10^{18} /cm^2. (The surface concentration of atoms is approximately 10^{15} /cm^2.)

The ideality factor, η, is related to the type of current flow through the depletion region formed in the semiconductor by the junction under forward bias. In the ideal case, $\eta = 1$, which represents no carrier recombination in the depletion region. As $\eta \rightarrow 2$, the recombination current becomes dominant. The recombination current is given by Equation 7-1:

Equation 7-1

$$I_{rec} = q\sigma v_{TH} N_t n_i Z L (e^{qV/2kT} - 1),$$

where σ is the effective capture cross-section of the recombination center, v_{TH} is the thermal velocity of electrons, N_t is the number of traps, n_i is the intrinsic carrier

concentration, Z is the gate length, and L is the gate width. The total current under forward bias can be expressed as the sum of the thermionic emission current (refer to chapter 2) and the recombination current, as shown in Equation 7-2.

Equation 7-2

$$I_G = ZLA^{**}T^2e^{(-q\phi_b/kT)}\,(e^{qV/kT} - 1) + q\sigma\nu_{th}N_tn_iZL(e^{qV/2kT} - 1)$$

Although Equation 7-2 cannot be factored, the gate current can be written empirically as,

Equation 7-3

$$I_G = I_o\,(e^{qV/\eta kT} - 1),$$

where $I_o = ZL(A^{**}T^2e^{(-q\phi b/kT)} + q\sigma\nu_{th}N_tn_i)$ and η is a factor (the ideality factor) related to the weighted average of the thermionic and recombination current. Considering only thermionic and recombination current*,

Equation 7-4

$$\eta = 1 + I_{rec}/(I_{rec} + I_{thermionic})$$

such that when $I_{rec} = 0$, $\eta = 1$ and when $I_{thermionic} << I_{rec}$, $\eta = 2$. Comparing this equation to the ideality current equation, the ideality factor thus represents the relative contribution to the forward current of the normal forward current and the recombination current. In other words, η is a number between 1 and 2; the closer to 2, the more recombination is occurring. Therefore, if the power slump is a function of carrier trapping induced by defects in the active region of the device (which includes

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* Other factors, such as quantum mechanical tunneling and edge leakage effects, make an analytical expression for the ideality factor difficult to formulate. In practice, the ideality factor can only be empirically determined.

the channel and the depletion region under the gate), the ideality factor should increase as the power slump occurs.

Electrical measurements show that an increase in the ideality factor occurs in 80% of the devices which exhibit power slump. An increase in the ideality factor occurs in only 9% of the devices which did not exhibit power slump. These results are summarized in
Table 7-1.

Of the ten devices shown in Table 7-1 that did slump, only two SiON devices (1070, 1073) did not have a significant change in the ideality factor. Of the eleven devices that did not slump, only one SiON device (1014) had a significant increase in the ideality factor (1.23 to 1.31) during lifetesting. The two sample t-test used to analyze the data indicates a significant increase in the ideality factor after power slump, as shown in Table 7-2.

The increase in the ideality factor associated with power slump indicates that it is likely that new recombination centers are forming during power slump and that these centers are electrically active, thereby increasing the recombination current component of the gate current. As is the case with generation of carriers, the process of carrier recombination is most efficient for energy states near the middle of the bandgap. Thus, the changes in the ideality factor are consistent with the hypothesis that an increase in the concentration of generation centers is responsible for the power slump, since energy states that would act as recombination centers under forward bias would also act as generation centers under reverse bias.

Table 7-1: Ideality factor and power slump.

Sample (Passivation)	Ideality Factor Pre-power slump (± .05)	Ideality Factor Post-power slump (± .05)	Power Slump (μA/h)
1007 (SiN)	1.23	1.36	272
1009 (SiN)	1.22	1.28	40
1011 (SiN)	1.21	1.35	260
FX7 (SiN)	1.12	1.35	13
FX10 (SiN)	1.19	1.44	3527
FX20 (SiN)	1.20	1.36	119
FX22 (SiN)	1.19	1.36	48
FX28 (SiN)	1.19	1.23	11
1070 (SiON)	1.24	1.23	14
1073 (SiON)	1.24	1.23	16

Table 7-2: Statistical analysis for ideality data.

F-Test Two-Sample for Variances			t-Test: Two-Sample Assuming Unequal Variances		
	Post-slump	*Pre-slump*		*Post-slump*	*Pre-slump*
Mean	1.32	1.20	Mean	1.32	1.20
Variance	0.0052	0.0012	Variance	0.0052	0.0012
Observations	10	10	Observations	10	10

F	4.18		df	13	
P(F<=f) one-tail	0.022		t Stat	4.56	
F Critical one-tail	3.18		P(T<=t) one-tail	0.00026	
			t Critical one-tail	1.77	
			P(T<=t) two-tail	0.00053	
			t Critical two-tail	2.16	

7-2 RESIDUAL STRESS AND POWER SLUMP

Twenty two devices were electrically stressed under the same conditions by ITT personnel to characterize power slump. We then determined the state of stress using our X-ray stress measurement technique and made X-ray topographs at SSRL for each device. This section provides the experimental details of the investigation, presents data for devices which did not exhibit power slump, and finally, presents data for devices which did exhibit power slump. The magnification for all topographs in this chapter is 53X.

EXPERIMENTAL DETAILS

X-ray strain measurements were made on 29 power amplifier circuits using the single crystal X-ray strain measurement technique discussed in Chapter 5. An optical micrograph of a typical device is shown in Figure 7-2. The measurements were performed on a Scintag XDS 2000 PTS diffraction system using Cu K_α radiation, and 0.01 mm and 0.02 mm detector slits. The (533), (444), and (620) families of planes were used to determined the strain tensor. Peak positions were determined using the profile fitting routines of Scintag's DMS software. The samples were manually positioned to bring them into the appropriate diffracting positions.

Rocking curves of all of the samples were measured to verify that the subgrain misorientation was sufficiently low to allow the assumption of linear elasticity. All samples had minimal subgrain misorientation. A typical rocking curve is shown in Figure 5-2. The rocking curve data are verified by the excellent separation of the $K_{\alpha 1}$ and $K_{\alpha 2}$ doublet in all samples measured. Significant subgrain misorientation would cause broadening of the K_{α} peak, and poor separation (if any) of the doublet.

Once the positions of the $K_{\alpha 1}$ peaks for each plane measured were determined, these data were entered into a computer program written to calculate the stress tensor. The stress tensors and the error matrices were calculated for each sample and transformed to determine the octahedral shear stress (coincident with {111} for GaAs).

Presented with the stress data are X-ray topographs of each die. These topographs were created using the Laue technique described in Chapter 3. The (533) planes were used to image these devices at a wavelength of $\lambda = 1.1386$ Å. The corresponding absorption coefficient is $\mu = 550\ cm^{-1}$ with a depth of penetration of approximately 0.93 μm, using
$\alpha = 1.00^{o}$. In dynamically diffracting regions, the depth of penetration is approximately 9 nm due to attenuation. As explained in chapter 3, the regions which are kinematically diffracting are regions where high dislocation densities exist. Therefore, the images which show large dislocation densities are effectively sampling a deeper volume than those images which show very few dislocation structures. In this way, increases in dislocation densities are more pronounced than would be expected if the depth of penetration was constant for all images.

The light regions which appear to be device structures are in fact the strain fields caused by the overlying metallization and film edge stresses. The topograph in Figure 7-3 is of a die which has not been mounted to a heat sink. The formation of

dislocations, though minimal, is evident in the FET regions of the circuit, as pointed out by the white arrows in the figure. The presence of pre-existing dislocations in the region under the FET is consistent with our theory of power slump.

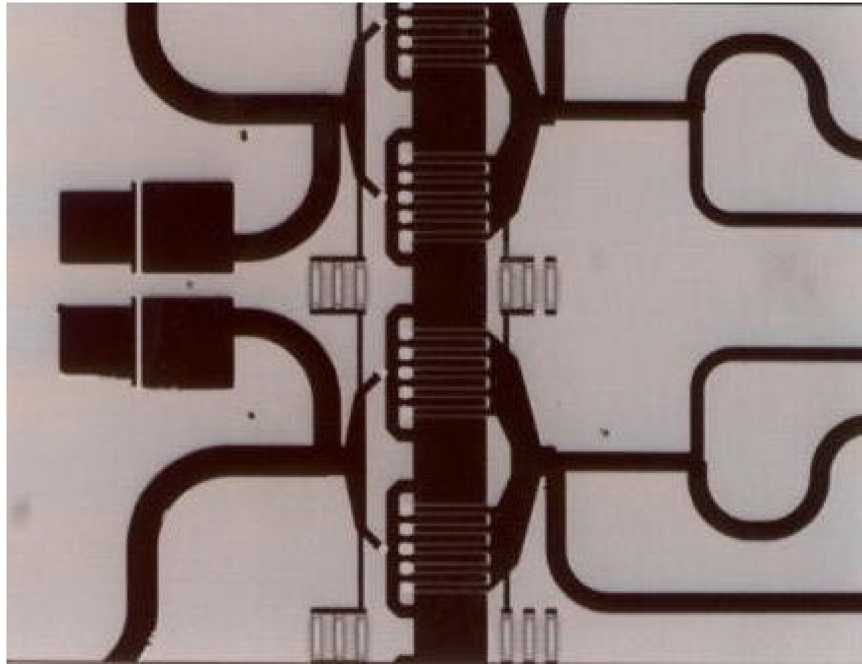


Figure 7-2: Optical micrograph of the devices under investigation.

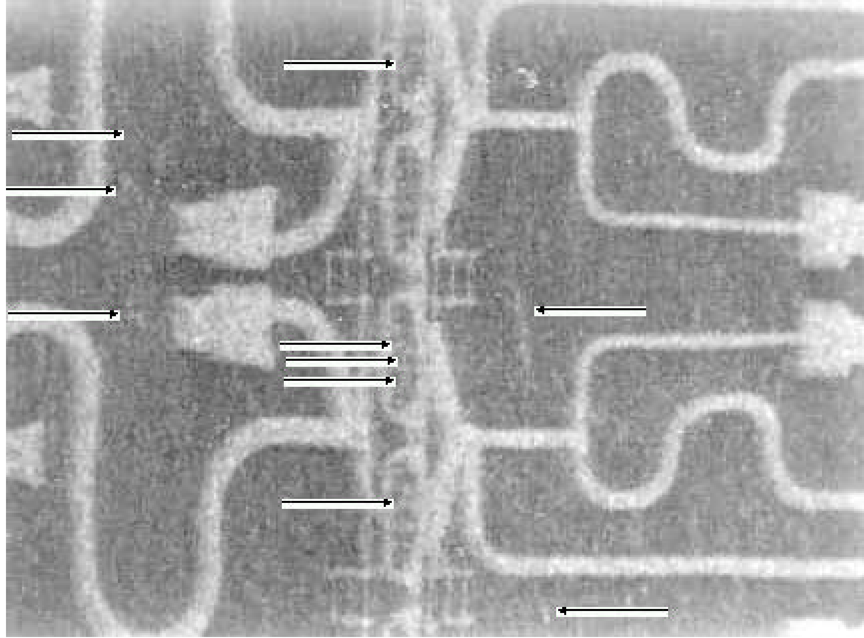


Figure 7-3: X-ray topograph of unmounted die. The arrows point to dislocation structures.

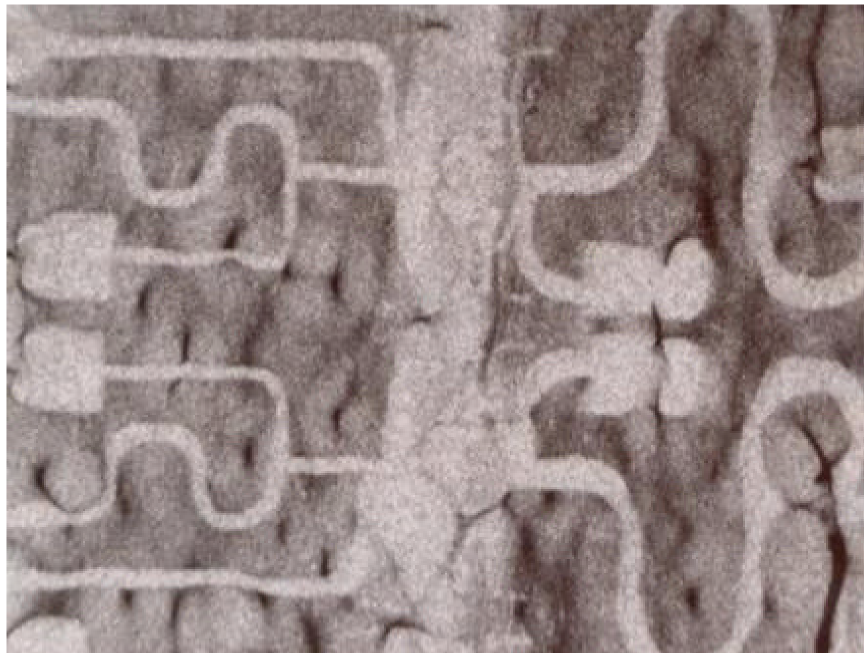


Figure 7-4: X-ray topograph of circuit after die-attach (SiN passivated). This image represents the most pronounced strains from the die attach process.

Images of the devices tested have a background contrast pattern due to strains developed during the die attach process. Figure 7-4 shows a die that has been attached to a heat sink by an indium based solder. The pattern that appears to be in the background is due to the microstrains from the grain structure of the solder on the backside of the chip. Lighter regions are strain fields, while the darker regions, which correspond to the position of the grain boundaries of the solder, are regions which are unstrained. The effect of these uneven strain fields on the strain fields around the FETs is to enhance the strain field in some areas (brighter regions) and decrease the strain field in others (darker regions). Note that in the topographic images throughout the remainder of this chapter, there is a wide variation in the presence of the strain fields due to the die attach process. This is possibly due to variability introduced by human operators who manually solder the die to the heat sink.

DEVICES NOT EXHIBITING POWER SLUMP

Thirteen of the twenty two devices tested did not exhibit power slump. Table 7-3 shows the stress data for these devices. Figure 7-5, Figure 7-6, Figure 7-7, and Figure 7-8 are typical topographs of the non-power slumping devices. For later comparison, note the clear imaging of the gate fingers in the FET region of the chip. The clear image indicates both a small strain field and relatively few dislocations.

Table 7-3: Shear stress data for devices showing no power slump (V_{DG}=24 V).

Sample and Passivation Type	Residual Shear Stress (+/- 2 MPa)
FX8 (SiN)	13
FX31 (SiN)	12
1017 (SiON)[#]	8
1014 (SiON)	8
1010 (SiN)	7
1018 (SiON)	6
1071 (SiON)	4
1079 (SiON)	4
1072 (SiON)	3
1019 (SiON)	0
1076 (SiON)	0
1077 (SiON)	0
1079 (SiON)	0

[#]It should be noted that device 1017 failed during testing. The topograph of this device shows that the die is fractured (Figure 4-9). It is unknown whether residual stress played a role in the destruction of this device and was relieved after fracture. The device did not exhibit power slump. It is assumed that the device failed testing as a result of the fracture.

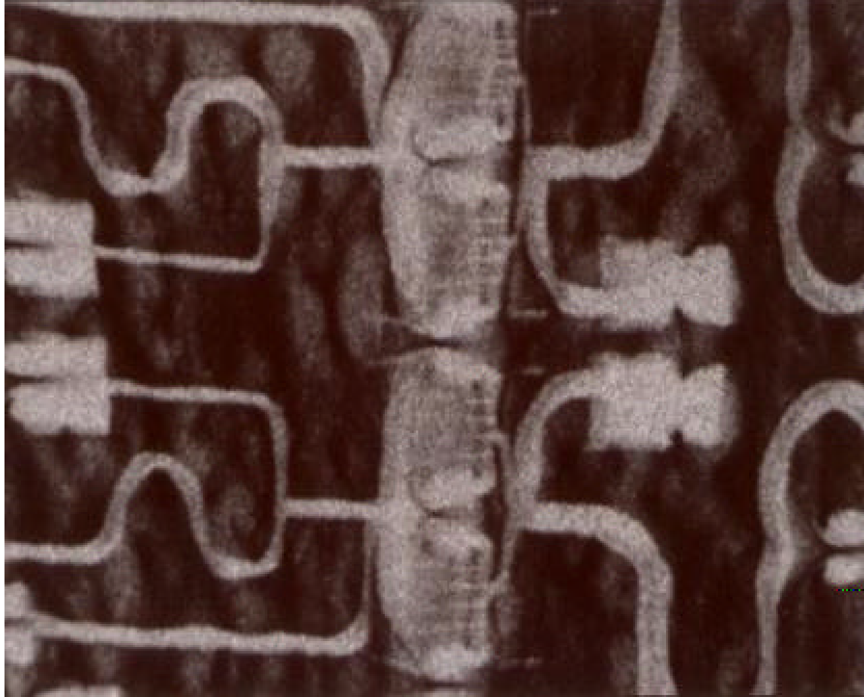


Figure 7-5: Topograph of device FX8; SiN passivated, no power slump. Notice that the strain fields associated with the gate regions are clearly imaged (horizontal white lines in the FET region).

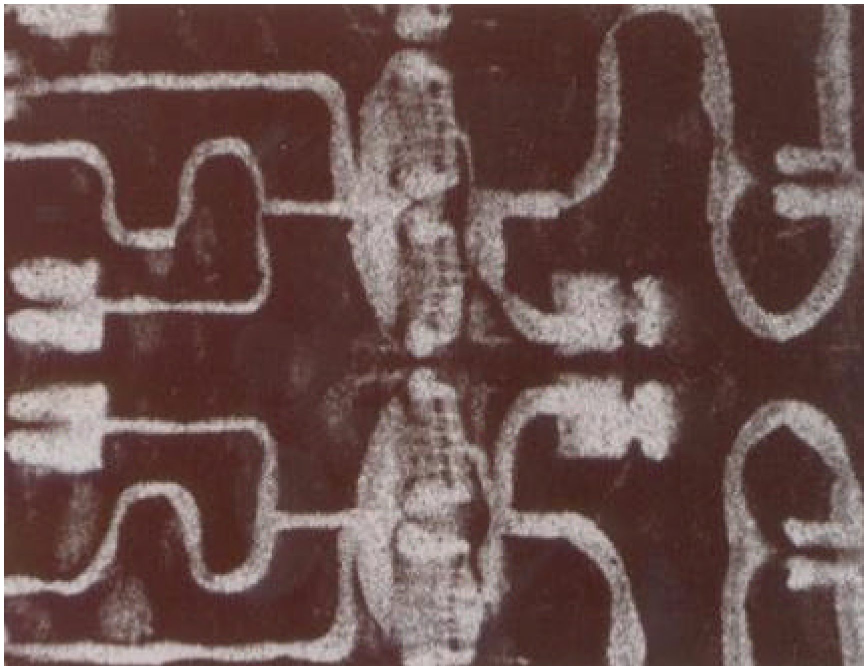


Figure 7-6: Topograph of device 1019; SiON passivated, no power slump.

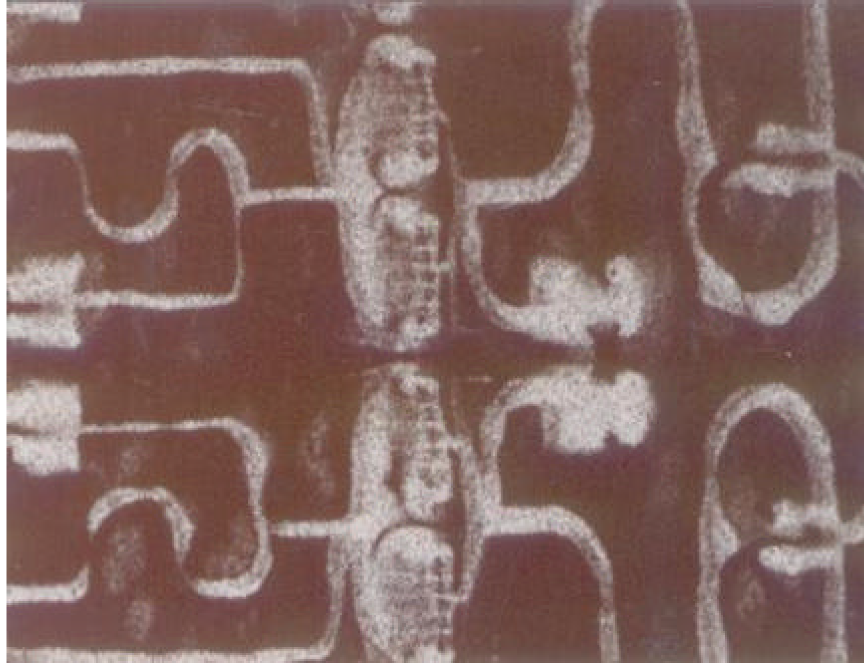


Figure 7-7: Topograph of device 1076; SiON passivated, no power slump.

Figure 7-8: Topograph of device 1077; SiON passivated, no power slump.

DEVICES EXHIBITING POWER SLUMP

The data in Table 7-4 and Figure 7-9 show the linear relationship between residual shear stress and power slump. Note that the value of R^2 is 0.92, indicating very good linearity in the data ($R^2 = 1.0$ would represent a perfect linear fit to the data). It should also be noted that devices 1007 and 1011 exhibited power slump at a lower applied bias than other devices. At 22 V_{DG}, absolute power slumps of 5.1 and 4.5 μA/h, respectively, were measured. Other devices did not exhibit power slump until V_{DG} = 24 V.

Comparing Table 7-3 and Table 7-4, it is apparent that the non-slumping devices had much lower residual stress than the devices that did slump[†]. As will be shown in the next section, a model to describe power slump explains the linear relationship between power slump and shear stress.

Table 7-4: Residual Shear Stress (τ) and Power Slump at 24 V_{DG}.

Sample and Passivation Type	Residual Shear Stress (MPa)	Normalized Power Slump (μA/h)
1007 (SiN)	80	272
1011 (SiN)	75	260
FX20 (SiN)	57	119
FX22 (SiN)	50	48
1009 (SiN)	36	40
FX7 (SiN)	32	13
FX28 (SiN)	25	11
1070 (SiON)	35	16.5
1073 (SiON)	25	13.6

[†] Device FX10 was not included in the above analyses because its value of power slump was extreme (3527 μA/h). It is likely that this device experienced normal power slump, then overheated, causing additional failure modes to occur.

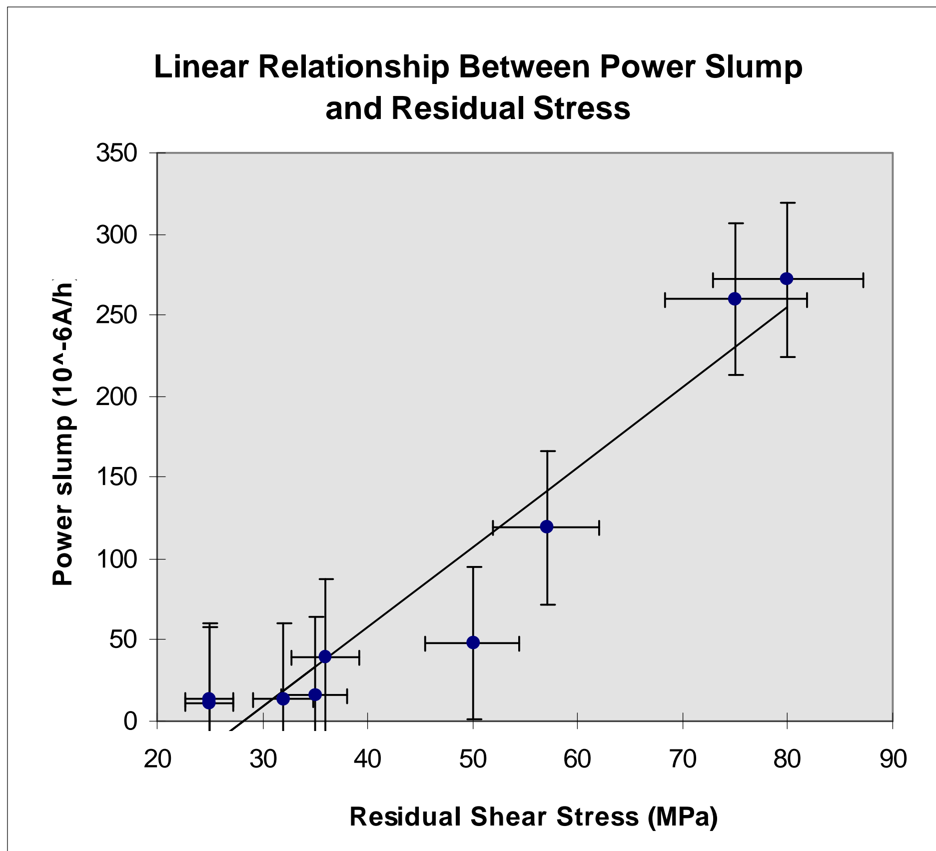


Figure 7-9: Chart showing the relationship between residual shear stress and power slump.

Figure 7-10, Figure 7-11, and Figure 7-12 show stress tensors and topographs representative of large, medium, and small values of power slump, respectively. Figure 7-10 shows a device with a shear stress of 80 MPa and a high dislocation density in the FET region. The high strain fields in this device are evident by the large areas of white contrast, as discussed in chapter 3. The small white lines in the FET region are dislocation structures. Figure 7-11 shows a device with a medium strain field, and a moderate dislocation concentration, compared to Figure 7-10. This is consistent with the assertion that lower shear stresses in the active region of the device will result in a smaller dislocation density. Figure 7-12 has a relatively small strain field and even fewer dislocations compared to Figure 7-10 and Figure 7-11. However, it does have more

Sample 1007

$$\sigma = \begin{bmatrix} -17 & -80 & 3.0 \\ -80 & -17 & -3.0 \\ 3.0 & -3.0 & 28 \end{bmatrix} \qquad E = \begin{bmatrix} 0.3 & 2.7 & .02 \\ 2.7 & 0.3 & .02 \\ .02 & .02 & 0.1 \end{bmatrix}$$

Figure 7-10: X-ray topograph of a device exhibiting a large value of power slump.

Sample FX22

$$\sigma = \begin{bmatrix} -10 & -50 & 2.0 \\ -50 & -10 & -2.0 \\ 2.0 & -2.0 & 18 \end{bmatrix} \qquad E = \begin{bmatrix} 0.2 & 2.2 & .02 \\ 2.2 & 0.2 & .02 \\ .02 & .02 & 0.1 \end{bmatrix}$$

Figure 7-11: X-ray topograph of a device exhibiting a medium value of power slump.

Sample 1073 (SiON)

$$\sigma = \begin{bmatrix} -5.0 & -25 & 1.0 \\ -25 & -5.0 & -1.0 \\ 1.0 & -1.0 & 9.0 \end{bmatrix} \qquad E = \begin{bmatrix} 0.2 & 1.2 & .02 \\ 1.2 & 0.2 & .02 \\ .02 & .02 & 0.1 \end{bmatrix}$$

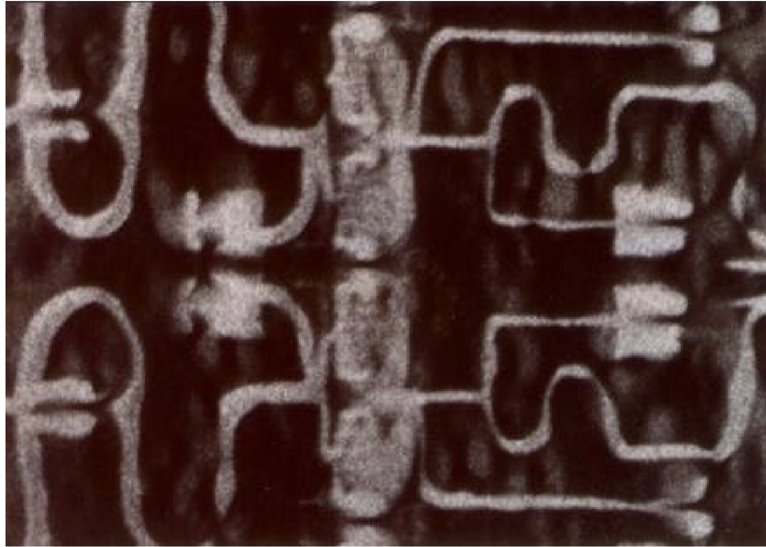


Figure 7-12: X-ray topograph of a device exhibiting a small value of power slump.

dislocations than the non-power slumping devices shown in Figure 7-5 through Figure 7-8.

7-3 POWER SLUMP MODEL

Data have been provided in section 7-1 which show a statistically significant relationship between the increase in the ideality factor and the degree of power slump, implying that generation centers are created in the depletion region during power slump. The apparent increase in dislocation density associated with power slump, shown in the topographs of section 7-2, supports the contention that these generation centers are related to dislocations. Since the mechanism of dislocation formation and motion in GaAs is primarily kink formation, and since kinks are efficient generation centers in GaAs due to the proximity of their energy level to the center of the bandgap, it is suggested that the generation centers are kinks on dislocations. To complete the

model, a relationship between process-induced film edge stress and power slump is now presented.

Summarizing the results presented in Chapters 2 and 6,

$$I_G = I_{therm} + I_{gen}$$

$$I_{therm} = ZLA^{**}T^2e^{-q\Phi/kT} \qquad \text{(Equation 2-2)}$$

$$I_{gen} = qZYhU \qquad \text{(Equation 2-12)}$$

$$U = \sigma v_{TH}N_Ce^{-(E_C-E_{GC})/kT}\, N_{GC} \qquad \text{(Equation 2-7)}$$

$$J = (2\nu_D\tau b^2/kT)e^{-E_{kf}/kT} \qquad \text{(Equation 6-7)}$$

where, the terms of these equations are defined in Table 7-5.

Power slump is defined (in this work) as the change in gate current as a function of time. Since the thermionic emission terms contains no time-dependent values, the value of power slump is given by the time rate of change in the generation current, as shown in Equation 7-5.

Equation 7-5

$$\partial I_G/\partial t = \partial I_{gen}/\partial t$$

Taking the time derivative of Equation 2-13,

Equation 7-6

$$\partial I_{gen}/\partial t = qZYh\, \partial U/\partial t$$

Table 7-5: Summary of terms used in power slump model.

Symbol	Term	Value	Reference
Z	Gate width	180 μm	ITT-GTC
L	Gate length	0.5 μm	ITT-GTC
A**	Effective Richardson Constant	144 A/cm^2K^2	calculated, chapter 2
T	Absolute temperature	75 ^oC	ITT-GTC
Φ	Effective Schottky barrier height (typical)	0.57 eV @ 24V_{DG}	calculated, chapter 2
Y	Depletion layer width normal to gate direction	1 μm	estimated
h	Depletion layer width normal to surface	0.15 μm	ITT-GTC
σ	Effective capture cross-section	3×10^{-15} cm^2	Schroder [2]
v_{TH}	Thermal velocity	2.32×10^8 cm/s	calculated, chapter 2
N_C	Density of states in conduction band	4.7×10^{17}/cc	Sze [3]
E_C	Conduction band energy	1.43 eV	Sze [3]
E_{GC}	Generation center energy level	0.71 eV	Schroder [2]
ν_D	Debye frequency	6.9×10^{13} /s	calculated
b	Burgers vector [110]	3.99 Å	calculated

The change in the generation rate per unit volume as a function of time can be expressed as Equation 7-7.

Equation 7-7

$$\partial U/\partial t = \sigma v_{TH} N_C\, e^{-(E_C-E_{GC})/kT}\, \partial N_{GC}/\partial t$$

Assuming a one-to-one correspondence between kinks and generation centers, the change in the number of generation centers as a function of time is equal to the kink nucleation rate per unit volume, J, as shown by Equation 7-8.

Equation 7-8

$$\partial N_{GC}/\partial t = J = (2\nu_D \tau b^2/YZkT)e^{-E_{kf}/kT}$$

Substituting Equation 7-6, Equation 7-7, and Equation 7-8 into Equation 7-5, an equation to describe power slump is given as Equation 7-9.

Equation 7-9

$$\text{Power slump} = \partial I_G/\partial t = \{2h\sigma v_{TH} \nu_D b^2 N_C e^{-(E_C-E_{GC})/kT} \tau\, e^{-E_{kf}/kT}\}/kT$$

or more simply,

$$\text{Power slump} = C\, \tau\, e^{-E_{kf}/kT}$$

where C is a function of applied bias (V_{DG} and V_{DS}) via the depletion layer width (h), temperature (T), and the effective capture cross-section (σ). The kink formation energy is partially a function of the REDG effect, which depends on bias via the drain

to source current and the gate current. However, since all of the terms which define C are assumed to be the same for all devices which are biased at the same voltages and operated at the same temperature, the only parameters that vary among the devices tested are the shear stresses in the active region of the device and the kink formation energy (which also varies with shear stress). For the bias conditions used in the electrical characterization of power slump, and converting to power slump units of μA/h for 80 FETs per chip,

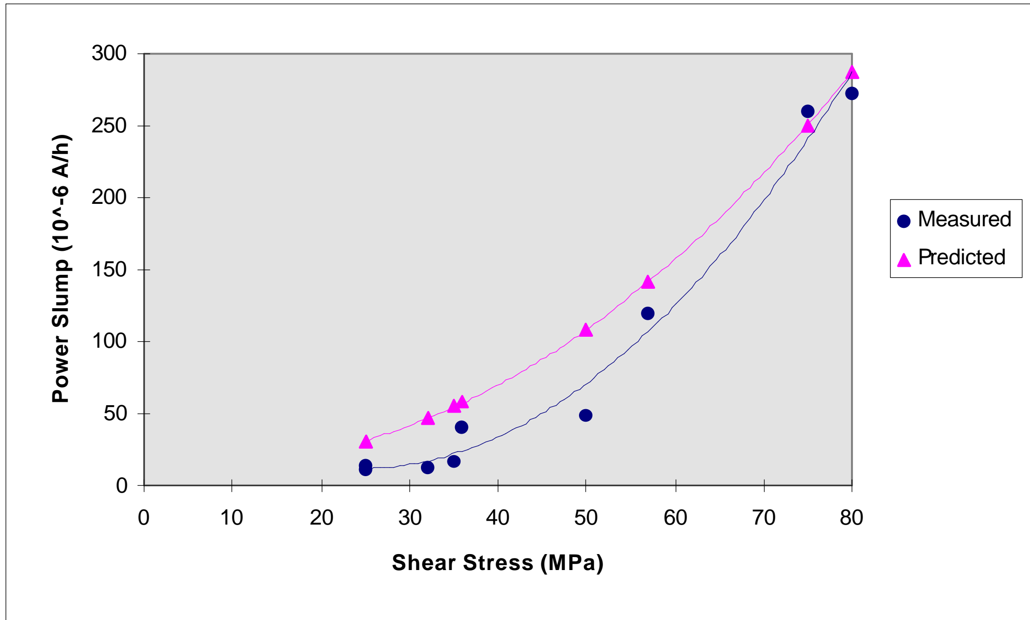
C = 390 μA/Pa•h.

The effective kink formation energy as a result of the REDG effect is estimated to be 0.63 eV for this device at V_{DG} = 18 V, based on the data reported by Maeda [4]. As the applied voltage increases, the applied field increases, thus increasing the REDG effect and further reducing E_{kf}. As the kink formation energy decreases, the number of kinks increase, thus increasing the number of generation centers in the depletion region. In this way, the generation current increases, thus increasing the total gate current, and decreasing gain.

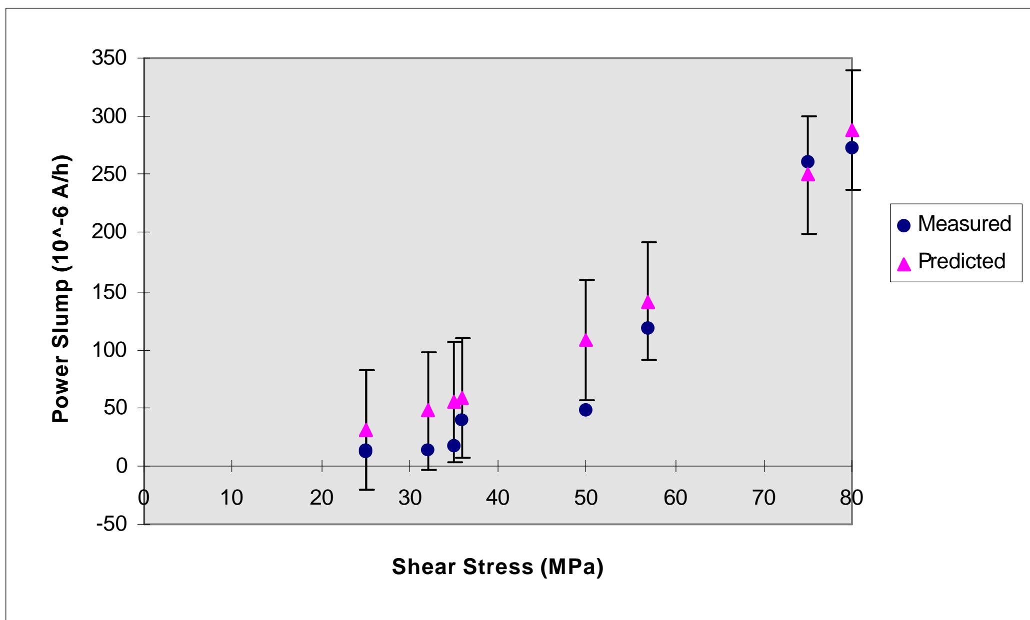
Table 7-6: Comparison of measured and predicted power slump values.

Sample and Passivation Type	Residual Shear Stress (MPa)	Predicted Power Slump (μA/h)	Measured Power Slump (μA/h)
1007 (SiN)	80	288	272
1011 (SiN)	75	250	260
FX20 (SiN)	57	141	119
FX22 (SiN)	50	108	48
1009 (SiN)	36	58	40
FX7 (SiN)	32	47	13
FX28 (SiN)	25	31	11
1070 (SiON)	35	55	16.5
1073 (SiON)	25	31	13.6

The accuracy of the power slump model is dependent on the accuracy of the stress measurements (approximately 5% error due to uncertainty in the single crystal elastic



(a)



(b)

Figure 7-13: Comparisons of measured and predicted power slump values.

constants), the gate and drain currents in the channel (well characterized), and the initial defect density (generally not well known, but small). Table 7-6 and Figure 7-13 compare the model with actual data.

The error bars in Figure 7-13 (b) represent the standard error of the predicted power slump value (error bars on measured power slump values are shown in Figure 7-9). These error bars were determined by considering the precision of the values obtained from the literature, and the errors bars calculated for the stress measurements (as discussed in chapter 5). The trendline in Figure 7-13 (a) shows that there is a small error in the calculation of E_{kf}, since the curvatures of the trendlines are not quite the same. However, for shear stresses less than approximately 90 MPa, despite the error in E_{kf}, the model still gives reasonable results since the measured values are (for the most part) within the standard error of the predicted values, as shown in Figure 7-13 (b). In other words, at stresses below approximately 90 MPa, the dominant term in the power slump equation is the shear stress, which is consistent with the observation that the relationship between power slump and shear stress is almost linear.

Only one device (FX10) showed power slump well in excess of the predicted value. The predicted value was 985 μA/h, while the measured value was 3527 μA/h. As discussed in section 7-1, this anomalous power slump value may be due to other failure modes arising as a consequence of Joule heating in the active region of the device.

Since the power slump model predicts that the degree of power slump is essentially linearly related to the shear stresses in the depletion region of the device at low stresses (<90 MPa), and exponentially related to the shear stress via the kink formation energy at high stresses (>90MPa), reducing (or eliminating) the shear stress in the depletion region should reduce (or eliminate) power slump. Power slump can therefore be reduced by decreasing the passivation film edge stress, which has been shown in

chapters 3 and 4 to be the major contributor to shear stress near the gate. As discussed in Chapter 8, measurements have shown that SiON induces less film edge stress than SiN, which explains why 85% of the devices produced with SiON passivation did not show power slump (and the other 15% showed minimal power slump). This statement does not imply that devices which did not power slump would never do so. However, it does suggest that higher bias voltages are necessary to lower the kink formation energy via the REDG effect‡, in order to create kinks at lower shear stresses and induce power slump.

7-4 SUMMARY

A model has been presented that describes the power slump phenomenon. It explains the bias voltage dependence and the dependence of the passivation type (via the shear stress) on the observed power slump characteristics. The model proposes that the increase in gate current associated with power slump is due to the increase in the kink concentration in the depletion region. The increase in kink concentration is a complicated function of the applied bias, and a linear function of the shear stress in the active region of the device. The model is supported by topographic imaging which shows an higher dislocation density in the active region, and by ideality measurements which suggest that an increase in the number of generation/recombination centers occurs in power slumped devices.

We have shown that power slump appears to involve an increasing concentration of dislocations in the active region of the device. We hypothesize that kinks on dislocations are by far the most likely source of the increased generation current in the depletion region. It should be noted, however, that other dislocation features such as

‡ As discussed in chapter 6, large values of shear stress reduce the kink formation energy significantly. To force SiON devices (which have low shear stress) to power slump, the REDG effect must also compensate for the absence of the shear stress reduction in the kink formation energy term.

jogs or the dislocation core could produce generation centers in the depletion region of the device. Whether the generation centers are kinks, jogs, or some other dislocation structure, is left to be determined by future research.

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Chapter 8
Wafer Breakage

This chapter presents an investigation to determine whether process-induced residual stress may be a significant factor in high wafer breakage rates. Residual stress is measured in bare, SiON passivated, and SiN passivated GaAs wafers using the single crystal stress measurement technique described in Chapter 5. Fracture data is obtained using the 3-point bend technique to determine whether passivation processing decreases fracture stress. By determining residual stress and fracture stress, the amount of applied stress tolerated by a wafer as a function of passivation type can be calculated. It is assumed that wafers which tolerate less applied stress are more likely to break during device fabrication, thus leading to increased wafer breakage rates. Data is also presented that demonstrates the nucleation of sub-critical cracks near film edges. The magnification for all topographs in this chapter is 159X.

8-1 PROCESS-INDUCED RESIDUAL STRESS

From a production standpoint, wafer breakage is generally attributed either to human and machine handling errors or to poor quality wafers from the wafer vendor. To address the latter problem, mechanical bending measurements are performed on a representative number of wafers before accepting the boule for device fabrication. The role of process-induced residual stress is not generally considered when determining the cause of high wafer breakage rates and was therefore measured as part of this investigation.

RESIDUAL STRESS ANALYSIS OF BARE AND PASSIVATED WAFERS

Residual stresses in twenty bare, twenty 700 Å SiON, and twenty 2000 Å SiN passivated 3" GaAs wafers were measured using the techniques developed in Chapter 5. The SiON and SiN films were deposited using the same PECVD parameters used in device production; $T_{deposition}$ = 250 ^{o}C, applied field = 2 kV/cm at 13.5 MHz, carrier gas flow rate = 2000 sccm. Concentrations of oxygen in the SiON films is unknown, but less than 10%, and the hydrogen content of SiON and SiN films is unknown, but believed to be small. Variation in oxygen and hydrogen content between depositions is also unknown. The passivation films are amorphous.

The means testing in Table 8-1[*] shows extremely strong evidence that SiN passivated wafers have more residual stress than SiON wafers, which have more residual stress than bare wafers. The mean values of stress, are found to be 25 ± 7 MPa for bare GaAs wafers, 35 ± 6MPa for SiON passivated GaAs wafers, and 62 ± 10 MPa for SiN passivated GaAs wafers.

MACRO-RESIDUAL PROCESS-INDUCED STRESS

An experiment was performed to determine the origin of process induced macro-stress in devices[†]. Only processes that affect the wafer stress on a macroscopic scale were considered in this experiment (refer to Chapter 2 for device processing steps). Thus,

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[*] F-tests are performed to determine whether the t-test should assume equal variances. If the value of F exceeds the "F critical" value, then the variances are assumed to be unequal. The t-tests are used to determine if the mean value of residual stress is different between two groups. If the magnitude of the t-Stat is greater than the value of "t-Critical", then the means are different. A negative t-Stat indicates the mean of the first group is less than the mean of the second group. The P value is the significance of the test; the smaller P is, the less chance that the test gives an incorrect conclusion.

[†] Macro-residual stress as opposed to process-induced film edge stress.

Table 8-1: Statistical Analysis of residual stress data.

F-Test Two-Sample for Variances			**t-Test: Two-Sample Assuming Equal Variances**		
	Bare	**SiON**		**Bare**	**SiON**
Mean	24.9	35.4	Mean	24.9	35.4
Variance	49.6	44.6	Variance	49.6	44.6
F	1.11		t Stat	-4.84	
P(F<=f) one-tail	0.41		P(T<=t) two-tail	2.19E-05	
F Critical one-tail	2.17		t Critical two-tail	2.02	
F-Test Two-Sample for Variances			**t-Test: Two-Sample Assuming Unequal Variances**		
	SiON	**SiN**		**Bare**	**SiN**
Mean	35.4	62.4	Mean	24.9	62.4
Variance	44.6	110	Variance	49.6	110
F	2.46		t Stat	-13.30	
P(F<=f) one-tail	0.028		P(T<=t) two-tail	8.25E-15	
F Critical one-tail	0.46		t Critical two-tail	2.03	
F-Test Two-Sample for Variances			**t-Test: Two-Sample Assuming Unequal Variances**		
	Bare	**SiN**		**SiON**	**SiN**
Mean	24.9	62.4	Mean	35.4	62.4
Variance	49.57	110	Variance	44.57	110
F	2.21		t Stat	-9.73	
P(F<=f) one-tail	0.045		P(T<=t) two-tail	4.35E-11	
F Critical one-tail	0.46		t Critical two-tail	2.04	

processes, such as the channel implants which only affect the GaAs wafer in the 180 μm x 10 μm active region of the device, are not included in the investigation.

Five bare wafers were measured to determine the residual stress generated during the crystal growth process and subsequent sawing, grinding and polishing operations used to form the wafer. These wafers were then passivated with 700 Å of SiON using PECVD, and the residual stress was measured again. The wafers were then subjected to RTA at 925 ^{o}C to simulate the activation of the channel implant and the residual stress was measured again. The wafers were then subjected to the "damage" or "isolation" implant and the residual stress was measured again. The SiON was stripped, 2000 Å of SiN was deposited, and residual stress was measured again. Finally, the SiN was stripped and the residual stress of the bare wafers measured again.

Figure 8-1 shows that the greatest increase in residual stress occurs after the RTA process. Significant increases in residual stress also occur after SiON and SiN passivation. These increases in the residual stress cannot be due to bending moments in the wafer, as discussed in Chapter 4. Therefore, these stresses must be due to modification of the GaAs surface during PECVD and RTA. The fact that high residual stress continues to exist in the GaAs wafer after the SiN is removed (after the complete processing cycle) supports the contention that surface modification, rather than bending moments, are the cause of the stress.

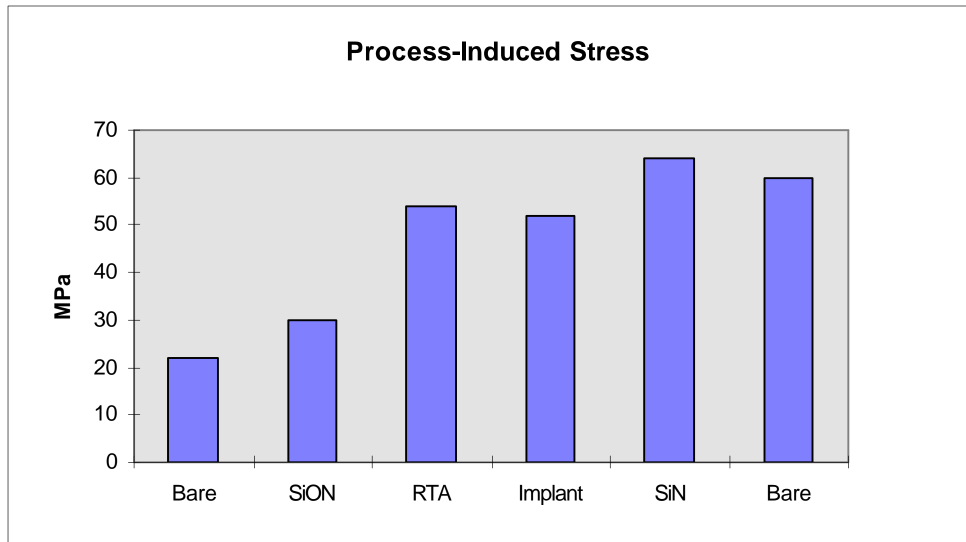

Figure 8-1: Residual stress (σ_{11}) as a function of various processing steps (Error bars = ± 5%).

As discussed in Chapter 3, since a large fraction of the X-ray beam used to determine stress is dynamically diffracting, much of the sampling volume of the crystal is a only few atomic layers deep (approximately 9 nm for 533 reflections). Thus, the single crystal stress measurement technique would be sensitive to surface modification. A possible explanation for the increased measured residual stress (other than plastic deformation of the near surface layers) is that preferential loss of As atoms into the passivation layer may occur during RTA (or furnace annealing), causing a composition-strain gradient in the near surface layers. Similar loss of As may occur during SiON and SiN deposition, but to a lesser degree since these processes are carrier out at much lower temperatures (250 ^{o}C compared to 925 ^{o}C for RTA or 827 ^{o}C for furnace annealing). Since oxygen can react with Ga to form a weak diffusion barrier of GaO, it is possible the diffusion of As into the passivation layer is reduced for SiON films compared to SiN films, resulting in less process-induced stress for SiON films. It should be noted that the stress values reported in Table 8-1 and Figure 8-1 for SiN films are consistent (62 MPa and 65 MPa, respectively). However, the SiN wafers represented in Table 8-1 did not undergo RTA. It is apparent that future

research should address the microscopic mechanism of macrostress formation during these processes, so that this stress may be minimized.

8-2 FRACTURE STRENGTH OF GaAs WAFERS

The theories of fracture in GaAs have been well-established [1, 2, 3], but there is a surprising lack of fracture data in the literature for GaAs devices. No data were found to determine whether PECVD decreases GaAs wafer fracture strength, although one study [4] presented evidence of reduced fracture strength in GaAs wafers due to MOCVD of metallic films. No data were found regarding the relationship between the presence of microelectronic device structures and fracture strength on GaAs wafers. As shown in Chapter 4, film edges can significantly increase the stresses near device features, causing dislocation motion and accumulation in these regions at elevated processing temperatures (as discussed in Chapter 6). Accumulation of dislocations can nucleate sub-critical microcracks, which can lead to fracture of the wafer during handling and thermal cycling. The effects of PECVD processing and device film edges on fracture strength of GaAs wafers is explored in this investigation.

EXPERIMENTAL PROCEDURE

Specimens were created from 3.5" wafers by a standard scribe and break technique in which a diamond stylus was used to scratch the surface, and the wafer cleaved such that the large edge of the sample was parallel to [110]; the direction normal to the sample surface is [001]. The samples were cleaved to approximately 1 cm x 6 cm and are 650 μm thick. Specimens dimensions were measured after cleavage. Residual stress was measured in the samples, using the technique discussed in Chapter 5. The

samples were then placed in a 3-point bend apparatus, built in-house (refer to Figure 8-2), and the deflection of the bent sample determined at fracture [5]. From the deflection, the applied stress at fracture was calculated for a rectangular sample using Equation 8-1.

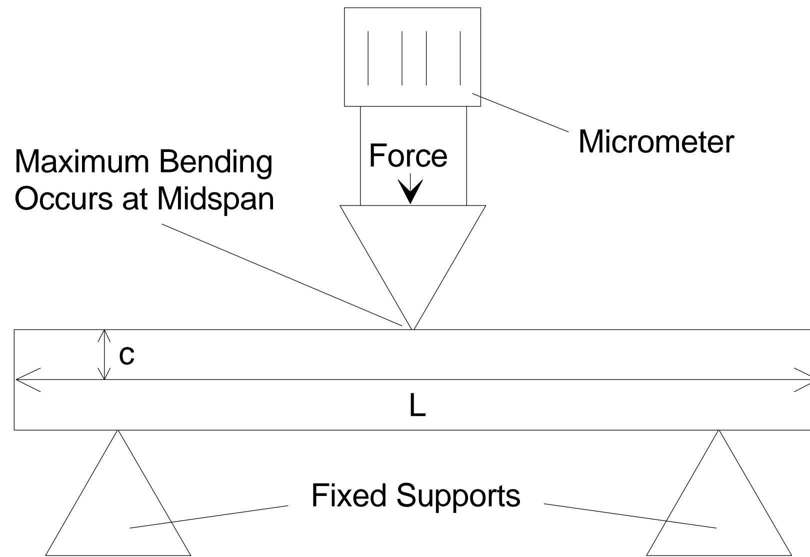

Figure 8-2: Schematic of 3-point bend apparatus.

Equation 8-1

$$\sigma_f = 12Ecd/L^2$$

where $E = E_{110}$ = 114 GPa, L = 6 cm, c = 312.5 µm, and d is the deflection at mid-beam. Twenty samples each taken from four bare, four SiON passivated, and four SiN passivated 3” wafers were measured (5 samples per wafer). These data are presented in Table 8-2 (bare GaAs samples), Table 8-3 (SiON passivated GaAs samples), and Table 8-4 (SiN passivated GaAs samples).

Table 8-2: Breakage test for bare wafers.

Sample	Residual Stress (MPa, σ_{11})	Applied Stress (MPa, σ_{11})
1	25	70
2	30	82
3	15	67
4	18	85
5	16	80
6	21	62
7	21	66
8	24	76
9	26	72
10	45	50
11	27	47
12	30	60
13	18	78
14	28	69
15	24	74
16	21	81
17	32	72
18	25	75
19	19	80
20	33	57

Table 8-3: Breakage test for SiON passivated wafers.

Sample	Residual Stress (MPa, σ_{11})	Applied Stress (MPa, σ_{11})
1	38	54
2	40	56
3	42	49
4	27	55
5	23	58
6	29	60
7	35	60
8	29	55
9	34	63
10	35	67
11	38	42
12	26	58
13	33	52
14	38	48
15	45	33
16	39	40
17	50	42
18	36	52
19	31	56
20	40	49

Table 8-4: Breakage test for SiN passivated wafers.

Sample	Residual Stress (MPa, σ_{11})	Applied Stress (MPa, σ_{11})
1	52	18
2	49	10
3	52	10
4	55	22
5	60	13
6	48	17
7	65	15
8	76	22
9	80	28
10	58	17
11	52	20
12	62	28
13	67	8
14	70	11
15	50	7
16	77	5
17	68	14
18	59	25
19	72	16
20	77	5

ANALYSIS AND DISCUSSION OF FRACTURE TESTS

The data were subjected to statistical analysis to determine whether there is a difference in the mean fracture strength among the groups tested (bare, SiON passivated, and SiN passivated). The fracture stress was calculated as the sum of the residual and applied stress at fracture, using the assumption that no plastic deformation occurred during the bend tests.

The generally accepted representation of fracture data uses Weibull statistics [3], which assumes the "weakest link" approach to data analysis. The weak link in this case is the largest flaw in the crystal, which upon application of high stress, initiates catastrophic fracture of the crystal. This theory assumes that the material under test exhibits no plastic deformation before fracture, which is the case for GaAs at room temperature. Weibull frequency plots of the data obtained in this investigation are presented in Figure 8-3, Figure 8-4, and Figure 8-5.

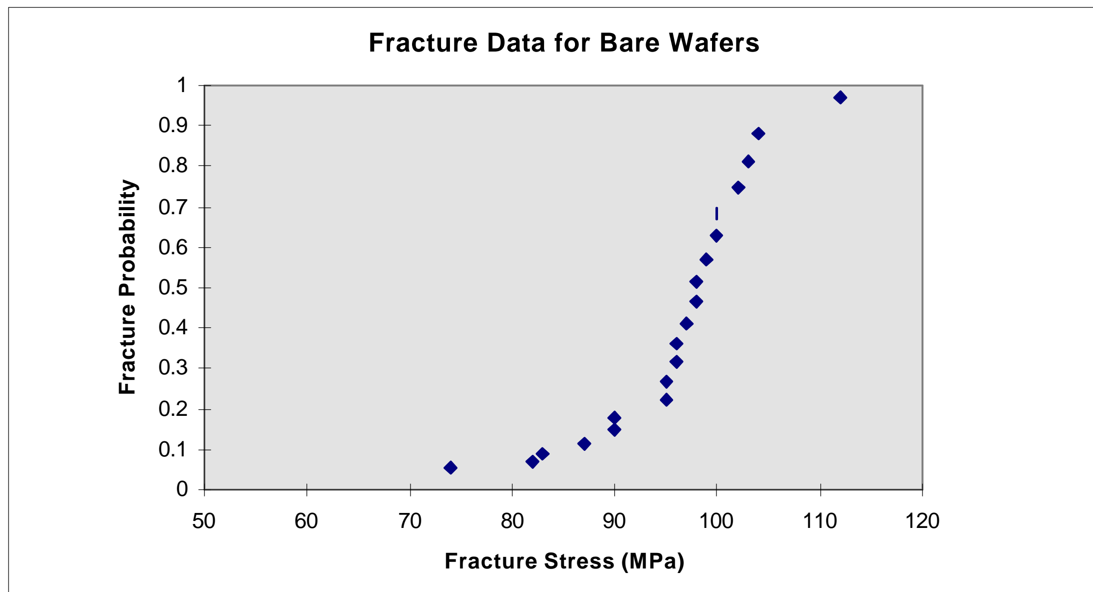

Figure 8-3: Frequency distribution plot of fracture in bare GaAs samples.

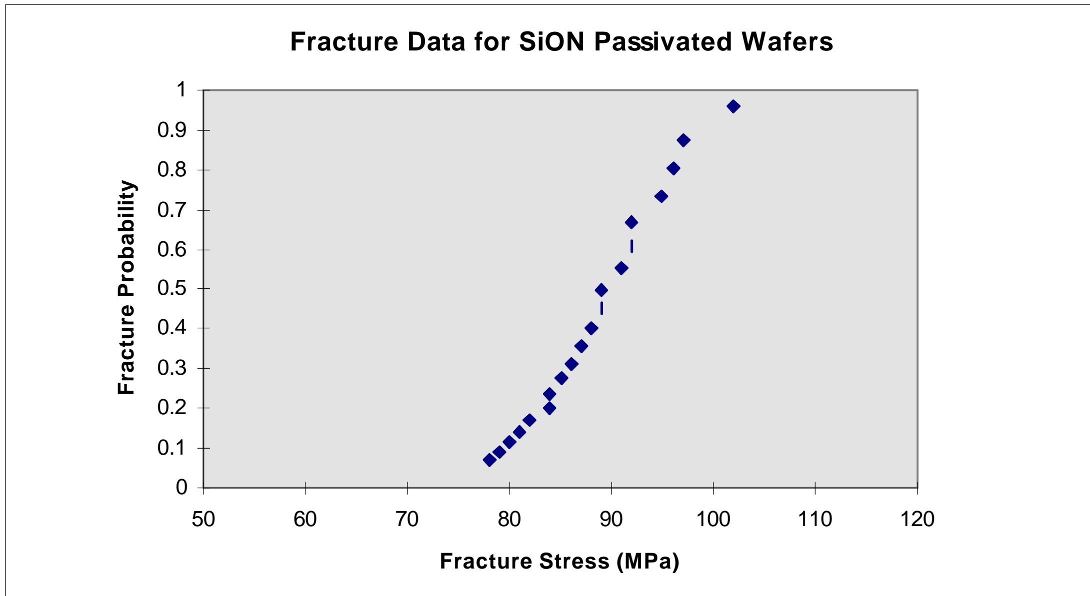

Figure 8-4: Frequency distribution plot of fracture in SiON passivated GaAs samples.

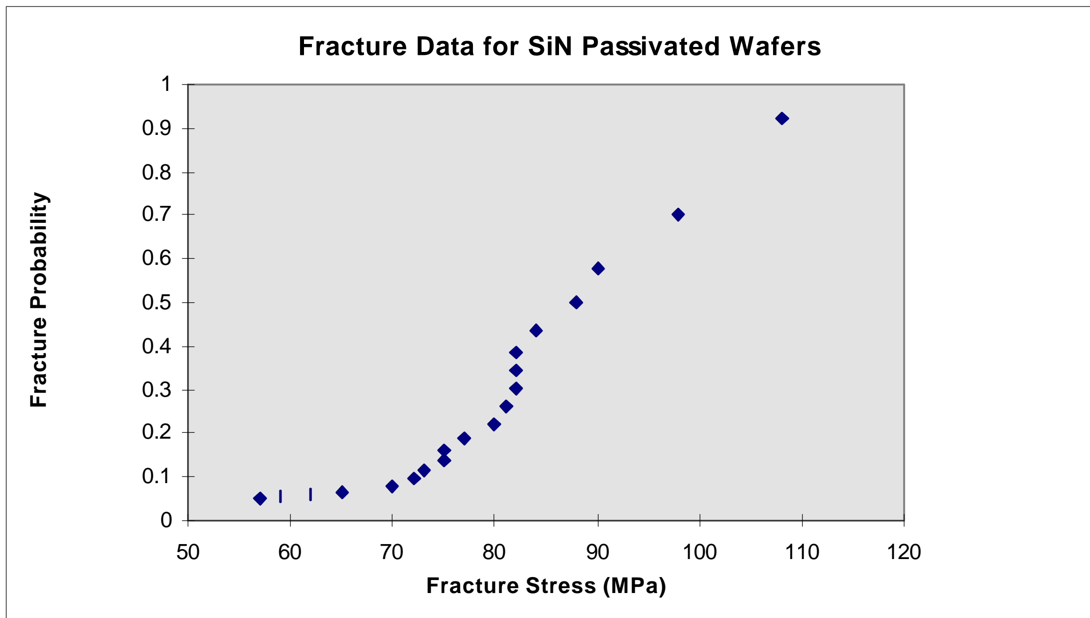

Figure 8-5: Frequency distribution plot of fracture in SiN passivated GaAs samples.

The probability of failure, according to Weibull statistics, is given by Equation 8-2.

Equation 8-2

$$G = 1 - e^{-\left(\frac{\sigma - \sigma_{min}}{\sigma_{max} - \sigma_{min}}\right)^{b}}$$

where σ is the stress of interest, σ_{min} is the stress below which no fracture occurs, σ_{max} is the stress above which all samples fracture, and b is the Weibull modulus. The Weibull modulus is related to the slope of the distribution, and is a direct measure of the distribution of flaws in the sample. A shift in the Weibull distribution to the left of the above plots is interpreted as an increase in the critical flaw size. In other words, larger flaws (sub-critical cracks) are present in the crystal, resulting in a lower fracture stress. To calculate the Weibull modulus for each sample type, the Weibull plots of Figure 8-6, Figure 8-7, and Figure 8-8 were produced.

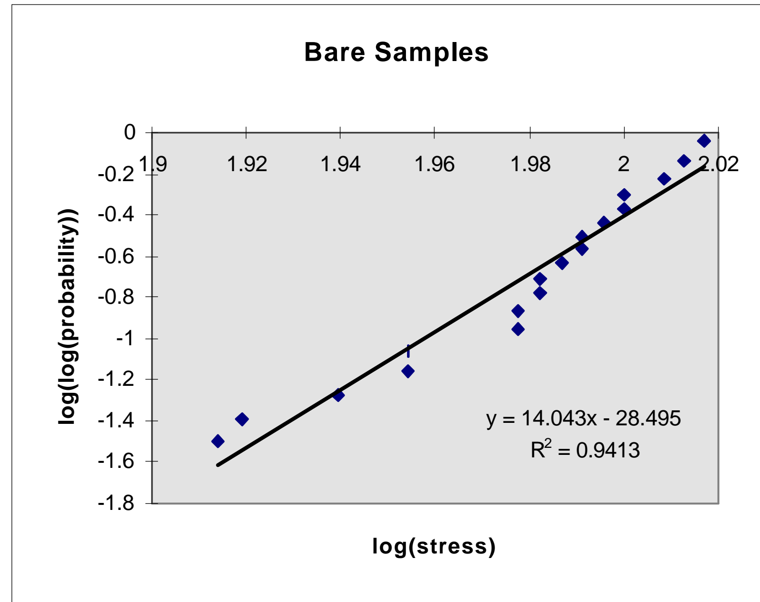

Figure 8-6: Weibull plot for bare GaAs samples.

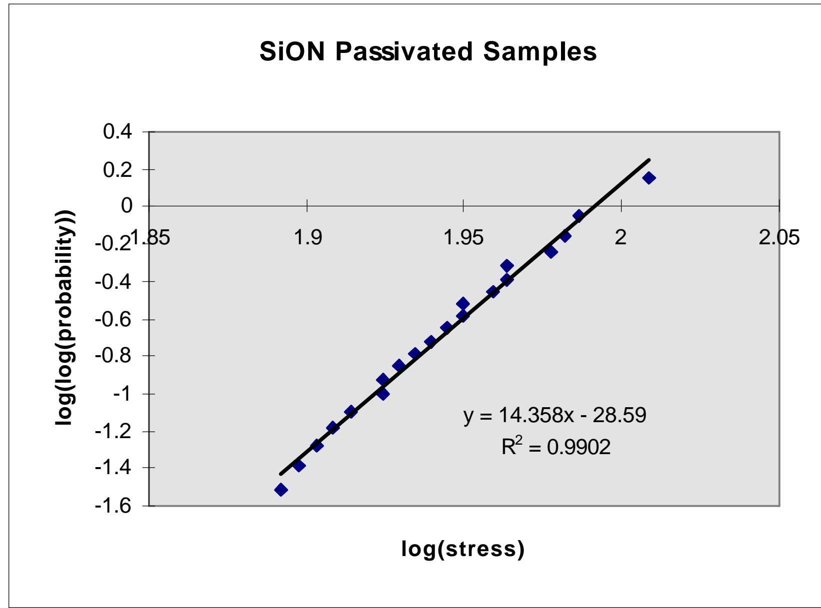

Figure 8-7: Weibull plot for SiON passivated GaAs samples.

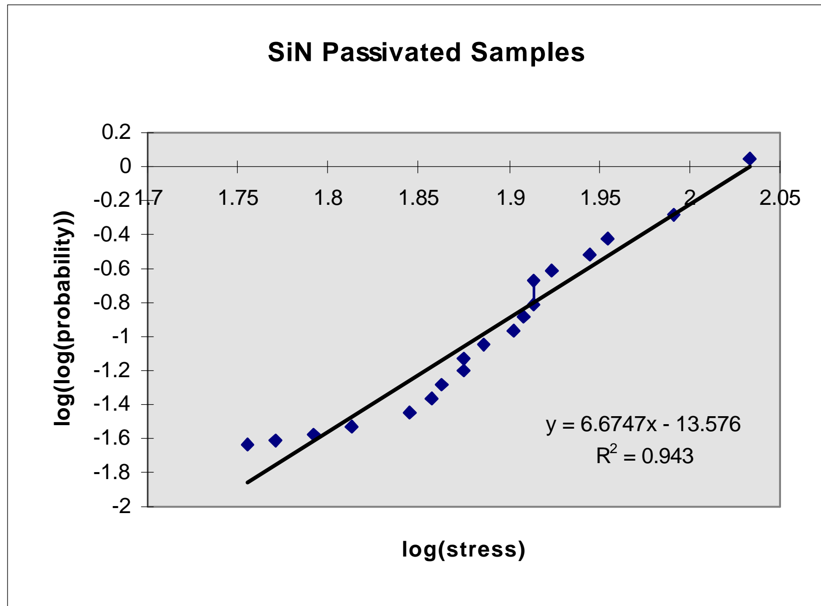

Figure 8-8: Weibull plot for SiN passivated GaAs samples.

The Weibull moduli for the data are found to be: bare samples, b = 14.0, SiON passivated samples, b = 14.3, and SiN passivated samples, b = 6.7. These Weibull data indicate that a wider distribution in flaw size exists for SiN passivated samples compared to bare and SiON passivated samples.

Additionally, according to analysis of the Weibull plots, larger critical flaws exist on average in SiN passivated GaAs samples (fracture probability = 0.5 at 88 MPa) than SiON passivated GaAs samples (fracture probability = 0.5 at 89 MPa) [‡], and larger flaws exist in SiON passivated GaAs samples than in bare GaAs samples (fracture probability = 0.5 at 98 MPa).

Topographic imaging supports the contention that larger sub-critical flaws exist in the passivated samples compared to the bare wafers and that larger sub-critical flaws exist in SiN passivated samples than in SiON passivated samples. The topographic images are from different samples than those used in the fracture tests.

Figure 8-9 and Figure 8-10 show topographs of wafers with SiN and SiON passivation. Note the microcracks (white lines). Since none of the bare wafers showed these features, it is assumed that the PECVD process introduced these flaws. The flaws in Figure 8-9 appear to be larger than those in Figure 8-10, consistent with the Weibull data which show that a larger critical flaw size is to be expected from SiN passivated wafers.

[‡] Although the mean fracture stresses of SiN and SiON passivated samples are nearly equal, 16 of the 20 SiN samples tested fall below the mean value of the SiN sample population. Thus, the Weibull plot for the SiN samples is more heavily weighted toward larger critical flaw sizes, compared to the SiON plot. Non-normal population distributions are to be expected for fracture data.

Figure 8-9: Typical X-ray topograph of sub-critical crack formation in a SiN passivated wafer (the largest flaw in this topograph is 35 microns in the longitudinal direction).

Figure 8-10: Typical X-ray topograph of sub-critical crack formation in a SiON passivated wafer.

Dowling [7] shows that the ultimate strength (in tension) of a sample with an internal flaw of size a_i is given by Equation 8-3,

Equation 8-3

$$\sigma_{ut} = K_c\,(\pi a_i)^{-1/2}$$

where K_c is assumed to be K_{IC} (representing the worst case scenario for fracture) and a_i is half the crack length in the longitudinal direction. K_{IC} for GaAs is reported in the literature [5] as 310 $kN/m^{3/2}$. Using the fracture data of Figure 8-3, Figure 8-4, and Figure 8-5, the ranges of flaw sizes are calculated to be 2.8 to 4.5 μm for bare samples, 3.1 to 4.9 μm for SiON passivated samples, and 2.7 to 5.9 μm for SiN passivated samples, using fracture probabilities of 0.1 to 0.9 as the lower and upper bounds to calculate the range. The topographs of Figure 8-9 and Figure 8-10 show flaws that are 35 μm for the SiN passivated sample (corresponding to a fracture strength of 30 MPa) and 19 μm for the SiON passivated sample (corresponding to a fracture strength of 40 MPa). Thus, the wafers imaged by X-ray topography appear to have fracture strengths of approximately half the value of the samples used in the 3-point bend tests.

The inconsistency between the topographic images and the fracture data is likely due to the relatively small number of samples used in the 3-point bend tests and variation among wafers in the distribution of flaw sizes imaged by X-ray topography. Since the fracture samples were from different wafers than those imaged by X-ray topography, it is very possible that the fracture samples have a different flaw size distribution than those imaged. Furthermore, only 2 wafers were imaged, and it is very possible that the flaw size distributions in these wafers are not representative of all wafers processed in the same manner. Therefore, although both the fracture data and topographic imaging indicate that SiN passivated wafers have larger flaws (and therefore lower fracture strength) than SiON passivated wafers, the data cannot be considered conclusive until

a larger sample size of wafers for both fracture and topographic imaging are studied. However, it does appear that PECVD processing of the passivation films does act to reduce fracture strength relative to the bare wafers, requiring a more stringent proof test to be implemented on the bare wafers prior to device processing.

8-3 MICROCRACK FORMATION DU E TO FILM EDGE STRESSES

Since silicon has a higher fracture toughness than GaAs (K_{IC} for GaAs of 310 kN/m$^{3/2}$ on the {110} cleavage planes, compared to a minimum K_{IC} for silicon wafers of 820 kN/m$^{3/2}$ on {111}), processing and film edge stresses generally do not induce fracture in silicon substrates, thus, the lack of historical concern for process-induced stress. However, as shown in Chapter 4, film edge stresses can become quite large in the active region of sub-micron GaAs devices which have adherent nitride films (TiWN, SiON, and SiN films for the devices investigated in this research). Therefore, an X-ray topographic investigation was performed to determine whether film edge stress is the primary nucleation point for large sub-critical flaws. A 700 Å SiON film was deposited and patterned on a 4" GaAs wafer to simulate the edge stresses in the active region of MESFETs. The width of the openings in the film is 3 μm.

Topographic images show the accumulation of dislocations and formation of microcracks at various stages in a test sample. (The features are from different areas of the same test wafer). This sample was processed at a deposition temperature of 250 ^{o}C. The elevated temperature and possibly the REDG effect from the plasma may contribute to dislocation motion, as discussed in Chapter 6.

The topographic images show microcrack formation where large film edge stresses exits (refer to Chapter 4). Figure 8-11, Figure 8-12, and Figure 8-13 show concentrations of dislocation structures near film edges. Figure 8-14 shows how these dislocations appear to coalesce into relatively large scale lineage features. Figure 8-15 shows how these lineages can grow into microcracks. The microcracks observed near film edges are

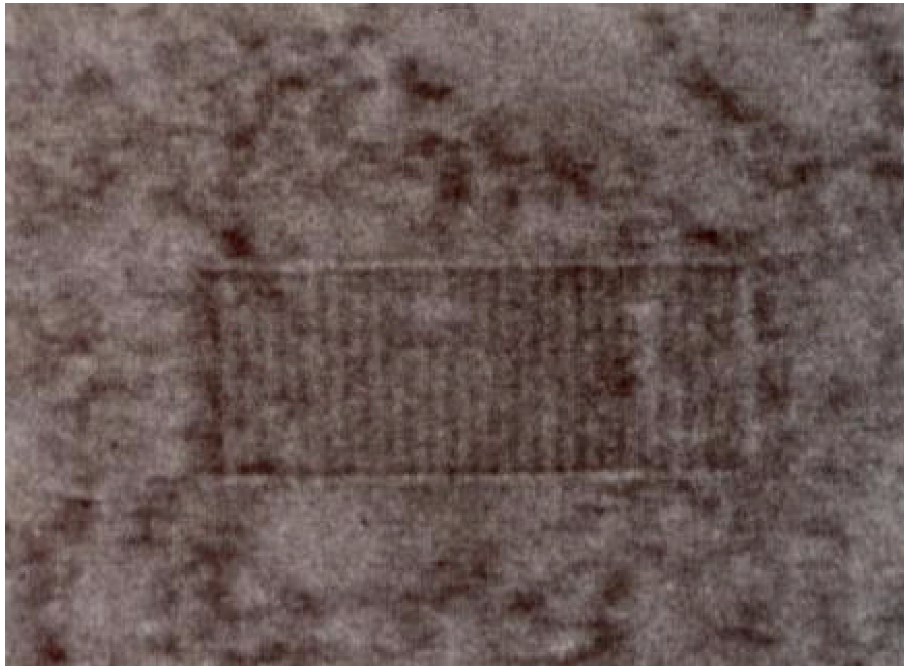

Figure 8-11: Dislocation accumulation (a small amount) near device features (the distance between the vertical white lines representing the strain field from each passivation edge is 3 microns).

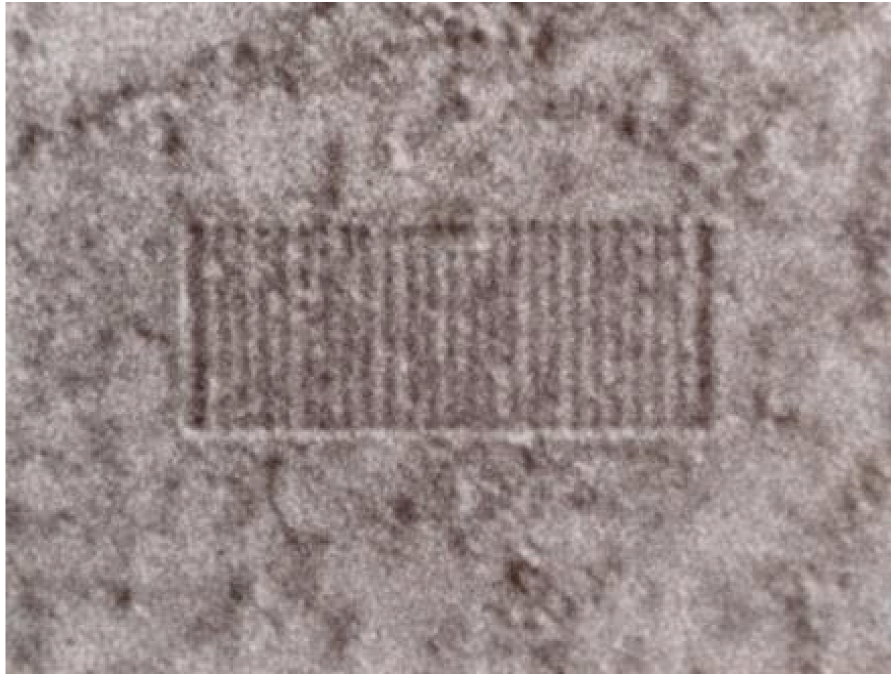

Figure 8-12: Dislocation accumulation (greater than previous figure) near device features.

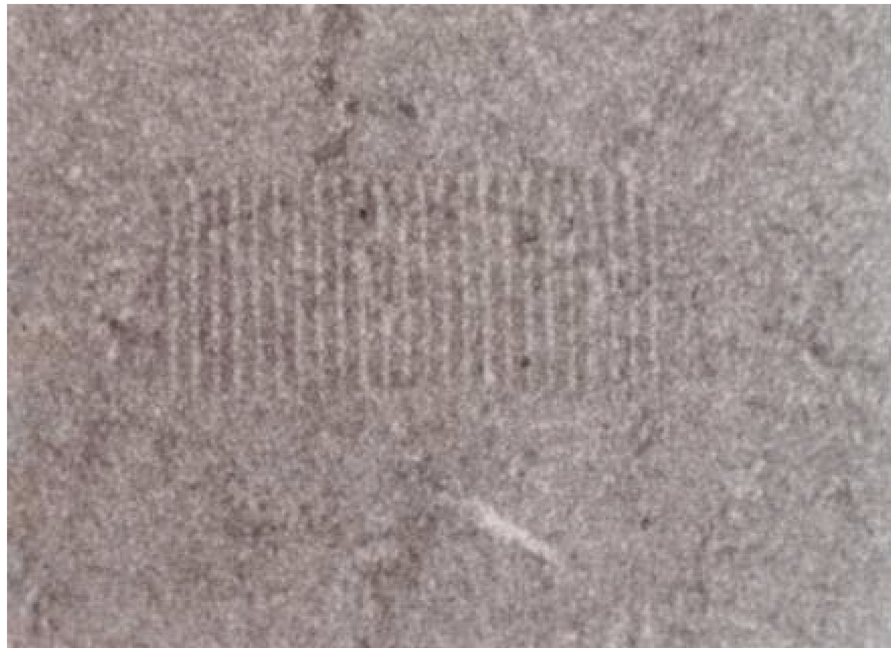

Figure 8-13: Dislocation accumulation (lineage formation) near device features.

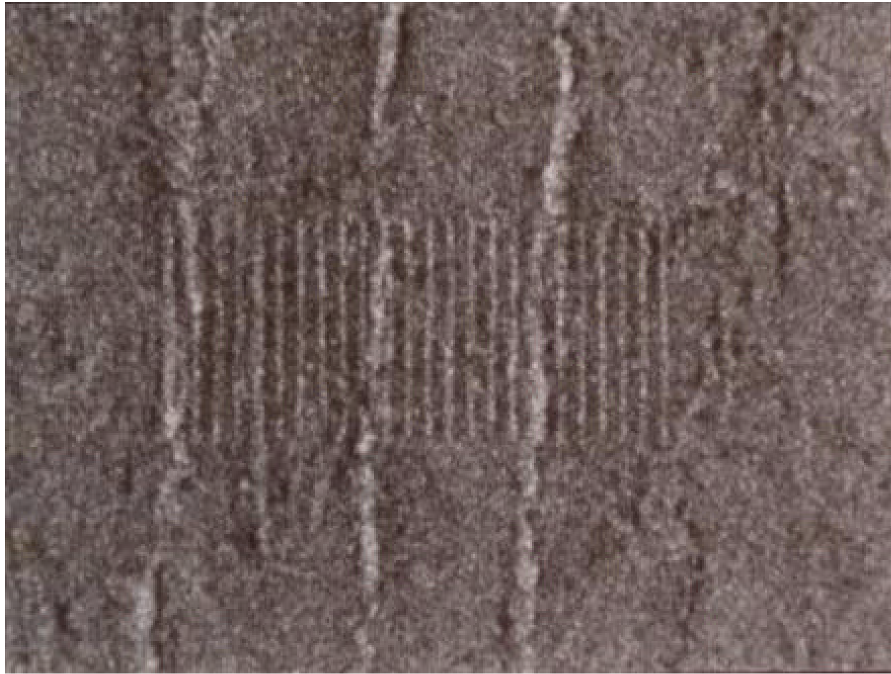

Figure 8-14: Dislocation accumulation (lineage formation) near device features.

Figure 8-15: Microcrack near device features.

typically much larger than those observed to form as a consequence of the PECVD process (refer to Figure 8-9 and Figure 8-10), and thus, are likely to be the initiation point of fracture in wafers during device fabrication.

8-4 SUMMARY

SiN passivation causes higher residual stress in GaAs wafers than SiON passivation, and passivated GaAs wafers contain more stress than bare GaAs. RTA was found to increase residual stress more than passivation processing. Passivation processing also was shown to decrease the fracture stress of GaAs wafers, both by fracture test data and indirectly by topographic imaging. Film edge stresses were shown by topographic imaging to nucleate microcracks.

SiN passivation processing both increases residual stress and decreases fracture strength, resulting in a reduction in the amount of applied stress that the wafers can tolerate. Thus, devices with SiN passivation would seem more likely to fracture during processing. SiON passivated wafers contain less residual stress and a less severe decrease in fracture strength compared to SiN passivated wafers, suggesting that SiON passivated wafers would withstand higher applied stress before fracturing. Since the film stress of SiON is typically less than the film stress of SiN, edge stress will also be reduced in SiON passivated devices, resulting in a reduction in microcrack nucleation near device features. By all indications, SiN passivated devices would appear to be more susceptible to breakage than SiON passivated wafers. This implies that wafer breakage rates for SiON passivated wafers should be lower than for SiN passivated wafers. Additionally, the ability to predict wafer breakage is better for SiON passivated devices, as evidenced by the higher Weibull number for SiON

fracture data. Therefore, higher fabrication yield is to be expected for devices fabricated with SiON passivation.

8-5 CHAPTER REFERENCES

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Chapter 9
Conclusions and Recommendations

9-1 CONCLUSIONS

The objectives of this research have been met as follows:

1. Methods have been developed to measure single crystal stress in GaAs wafers and devices,

2. a model has been developed to explain the power slump phenomenon, and

3. the role of process-induced stress on wafer breakage has been investigated.

SINGLE CRYSTAL STRESS TECHNIQUE

The successful outcome of the first objective gives the entire semiconductor industry a new tool to investigate the effects of stress on single crystal materials. This technique uses X-ray diffraction to measure peak positions in single crystal materials. These data are processed using an algorithm which calculates the full stress tensor and the associated error matrix. Before measurements, the technique requires that rocking curves are generated to insure that substructure in the sample does not make the assumption of linear elasticity invalid. After measurements, the Phi Error Analysis and stress gradient corrections are applied to the data using mathematical models developed in this research. Stress gradient calculations were verified using X-ray topographic imaging.

THE POWER SLUMP MODEL

The successful outcome of the second objective gives the III-V semiconductor industry an explanation of a phenomenon which currently has no comprehensive explanation. The model of power slump provides an explanation of the observed changes in ideality, increased gate current, and the effects of different passivation materials on the magnitude and threshold of power slump.

According to the power slump model, kinks form and migrate into the depletion region of the device when the kink formation energy is reduced in the presence of a large shear strain. These kinks act as efficient generation centers which are responsible for the increase in gate current. The increase in gate current causes a decrease in gain, and therefore a decrease in the output power of the device. The mechanism by which the kink formation energy decreases has been shown to be a function of shear strain and the degree of radiation enhanced dislocation glide. Since the REDG effect is dependent on drain to source current, which is a function of applied bias, the voltage threshold at which power slump occurs has been explained.

Shear strain has been shown, by the strain measurements developed in this research, to be a function of passivation layer composition, and thus explains the observed differences in the power slump behavior of SiN and SiON passivated devices. Increases in dislocation density have been qualitatively shown to increase by X-ray topographic imaging, as a function of power slump. The model predicts that for shear stresses less than 90 MPa, power slump will correlate approximately linearly with shear stress, and at shear stresses greater than 90 MPa, power slump will correlate exponentially with shear stress via the energy of kink formation term, which is stress dependent.

For higher bias voltages, the model predicts that the kink formation energy will decrease due to an increase in the REDG effect, thus reducing the “critical stress” that defines the transition between the linear and exponential behavior of power slump with stress. In any case, the entire power slump characteristic has been shown to be dependent only on bias voltage and shear stress, implying that the composition of the passivation layer has no effect on power slump, except indirectly, in that SiON films induce less shear stress in the substrate than SiN films. Therefore, to reduce power slump in the GaAs MESFETs studied in this investigation, it is necessary to reduce the stress of the passivation film and the gate metal.

The shear stress measured in the FET is the superposition of edge stresses and macrostresses, which implies that reducing macroscopic shear stress should also reduce power slump. As shown in the topographic images, a significant shear strain is developed during the die attach process, which undoubtedly exacerbates the power slump. Therefore, minimizing stresses developed during the die attach process is also recommended as future work.

With regard to reliability, the stress and topographic data indicate that there is great variability in the amount of stress developed in any one device due to variation in the film and die attach stress. This variability in the process makes it very difficult to predict which devices will power slump and which devices won’t, forcing the manufacturer to either make unreliable devices or operate devices reliably at reduced power levels. Even if the average value of process-induced stress cannot be reduced, better control of the process will allow production of more reliable devices. To this end, we suggest that manufacturer better control the PECVD parameters for passivation layer deposition and automate the die attach process, to ensure more uniformity in the stresses developed during device processing.

WAFER BREAKAGE

The successful outcome of the third objective provides a better understanding of how process-induced stress affects wafer breakage. X-ray strain measurements, developed in this research, have demonstrated that stress in the near-surface layers under the passivation contain a higher degree of stress than bare wafers. Furthermore, SiN passivation has a higher stress than SiON passivation. Stress measurements as a function of processing show that deposition of SiON, rapid thermal annealing, and SiN deposition are the primary causes of process-induced residual stress. Of these, RTA apparently causes the greatest increase in stress.

Fracture stress measurements indicate that the fracture stress of bare wafers is significantly greater than passivated wafers, and that the fracture stress of SiON is significantly greater than SiN wafers. X-ray topographic imaging has provided some evidence that PECVD introduces, or increases, the size of subcritical flaws, thus reducing fracture strength. The combination of increased process-induced stress and decreased fracture strength reduce the tolerance of the wafer to applied stress. This reduction in the tolerance of applied stress almost certainly causes increases wafer breakage rates and therefore reduces fabrication yield.

This research has also shown that film edge stress can nucleate sub-critical cracks around device features. These subcritical cracks are larger than those observed in the wafer with no device features, and are therefore expected to make wafers which are in-process even more fragile after device features are constructed.

9-2 RECOMMENDATIONS

Several recommendations as a result of this research are suggested.

1. A Taguchi or central composite design (CCD) should be implemented to determined the optimal passivation layer processing conditions to minimize film and process-induced stress (including die attach). Reduction of passivation stress will reduce the magnitude and delay the onset of power slump, according to the power slump model. Reduction of passivation stress will should increase the amount of applied stress which the wafers can tolerate by reducing residual stress in the wafer and reducing edge stress near device features. By minimizing passivation film stress, both the problems of power slump and wafer breakage should be simultaneously reduced.

2. Research is recommended to investigate how PECVD and other deposition methods modify the surface of GaAs wafers. Knowledge of how the surface is modified will provide insight into the microscopic causes of the near-surface strain gradient measured in this research, and possibly provide processing solutions to minimize this stress.

3. Additional investigation regarding the formation of kinks in the depletion region is recommended. Understanding the distribution and concentration of kinks in the depletion region as a function of stress and applied bias will allow refinement of the model developed in this research and verify the data obtained by other authors. Sectioning lifetested devices and performing transmission electron microscopy is likely the best method for investigating kink behavior in these devices, although

advanced sectioning processes will likely have to be developed for investigations at the sub-0.1-micron scale.

4. DTLS measurements should be performed in conjunction with the recommended TEM measurements to determined the exact energy levels of the kinks thought to act as the generation centers responsible for the power slump. This will provide insight into the solid state physics of crystallographic defects in semiconducting devices.

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Vita

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Other important accomplishments by Allan Ward during his nearly 10 years at Virginia Tech include receiving his private pilot's license, teaching courses as an instructor for the MSE department, building the Electrical and Optical Materials Teaching Laboratory for the MSE department, working as a process engineer at ITT-GTC, Roanoke, VA, and working as a failure analysis engineer at Electro-Tec, Blacksburg, VA. As of the date of this writing, Allan has 6 publications in the scientific literature, has presented his research at 4 conferences, and has written user's manuals for two commercial diffraction equipment vendors.