

Chapter 5

Design Examples of High Density High Efficiency Low Voltage Power Supplies

This chapter presents several design examples of high-density, high-efficiency (HDHE), low-voltage power supply using the proposed IM circuits. The theoretical results derived from the previous chapters are applied. The following examples will be used to demonstrate the design of high density modules using the proposed IM technique.

- For 70V input and 2.5V/140A output, at the switching frequency of 100kHz, a greater than 87% efficiency was achieved.
- For 48V (+/-10%) input and 1.2-1.8V/70A output, at the switching frequency of about 120kHz, an efficiency of greater than 81% was obtained.
- With 60V input and 3.3V/30A output, at the switching frequency of 500kHz, a power density of 130W/in³, a profile of 0.21", and an efficiency of about 90% were obtained.

The first two examples employ the FI²M circuit while the third example uses HBI²M circuit.

5.1. Design of Low Voltage High Current Power Supplies with Forward Circuit with Improved Integrated Magnetics (FI²M)

In this section, the designs of several applications using the FI²M are presented. The selection of the integrated magnetic core and the design of the PCB windings are addressed in detail. The stability issues of the FI²M are briefly discussed. A simple solution was provided.

Example 5-1

Input: 68-71V

Output: 2.5V/140A

Switching frequency: 100KHz

Efficiency: >87%

3+1 redundancy

Example 5-1 is used to demonstrate the design of the magnetic device and the power stage components for the FI²M circuit.

5.1.1. Electrical Design

Because of the redundancy requirement, four modules are paralleled to provide the required output current. Figure 5-1 shows the proposed block diagram. Four modules are interleaved. Each individual module is designed to provide 35A nominal and 47A maximum load current and to have its own local peak current mode control loop. Because four modules also share the same voltage feedback loop, the load current is automatically balanced among the four modules.

The power stage of each module is shown in Figure 5-2. Compared to the principle circuit shown previously, this diagram adds R_d and C_d . These two additional devices are intended to alleviate the noise stability problems, as will be discussed later. For synchronous rectifiers, the gate drive adopts Scheme 3A from the previous chapter, as shown in Figure 5-2. Based on the maximum allowable device stress, the steady-state maximum duty cycle is chosen to be 0.55. Therefore, the primary-to-secondary turns ratio can be estimated to be

$$N = \frac{V_{in,min} (D_{max} - \Delta D) \cdot \text{Eff}}{V_o},$$

Eq. 5-1

where DD is the duty cycle loss caused by the switching transient. At 100KHz, DD is assumed to be 0.01.

In this example, $N=12.8$. As the output current is relatively high, the single-turn secondary configuration is employed. Then the primary winding has 12T. So $N=12$. The resulting duty cycle range is about 0.49-0.52. The maximum voltage stress on the primary side is about 150V. The primary side MOSFETs use 200V devices: IRF640. On the secondary side, two MTP75N03HDLs are paralleled for each SR. Since the output voltage is only 2.5V, the secondary transformer waveform amplitude barely exceeds 5V. To guarantee a full turn-on of MTP75N03HDL, additional gate drive windings is used as shown in Figure 5-2(b).

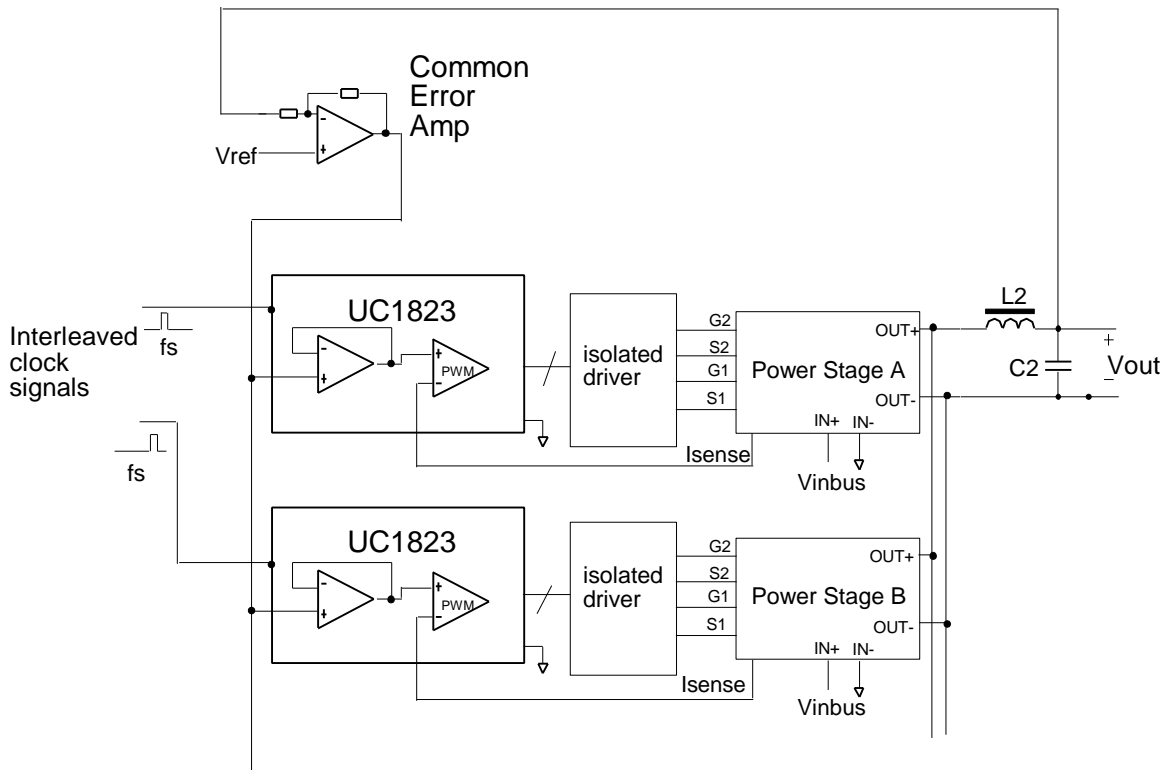
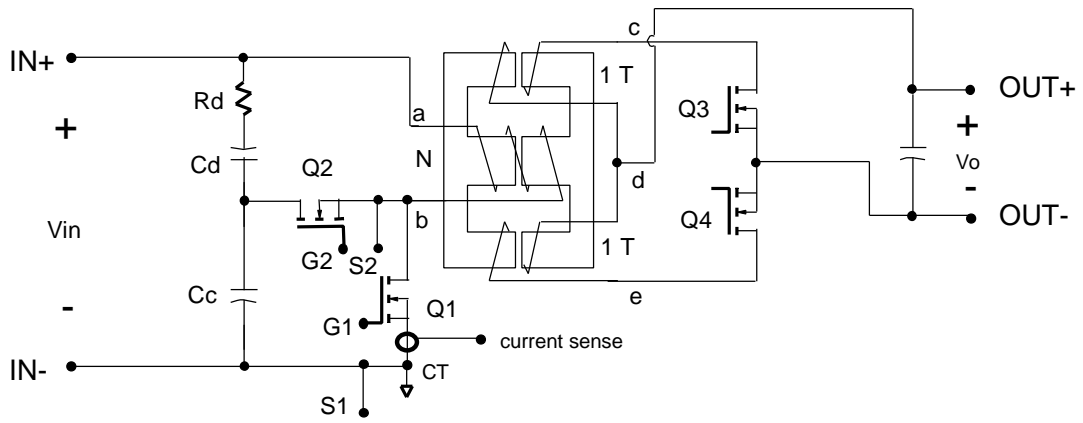
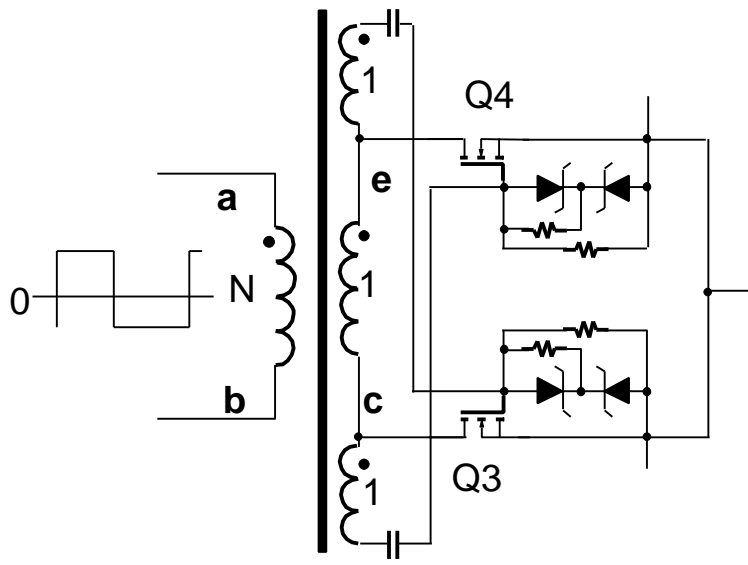


Figure 5-1 Proposed block diagram of power supply for 2.5V/140A output



(a)



(b)

Figure 5-2 Power stage schematic for Example 5-1, (a) main power train, (b) gate drive scheme for SR

5.1.2. Design of Magnetic Device

If the core loss density is chosen to be $P_c=100,000 \text{ W/m}^3= 100 \text{ mW/cm}^3$, the ac flux density for the 3F3 material at 100°C core temperature is about: $B_m=0.1\text{T}$. The required core cross-sectional areas are then estimated to be:

Core Leg 1: $A_{1\min}=68\text{mm}^2$

Core Leg 2: $A_{2\min}=66\text{mm}^2$

Center Post: $A_c=131\text{mm}^2$

Since $D_{\min}=0.496$ and $D_{\max}=0.517$, A_1 and A_2 are almost equal. The off-the-shelf planar E-core can be used. If we choose $J_{\max}=10\text{A/mm}^2$, and the winding filling factor K_f to be 0.2, the area for both core windows is estimated to be 25.7mm^2 .

For the E32/6/20-3F3 and PLT3220/3.2-3F3 cores, Philips Magnetic Products Catalogue lists the core cross-sectional areas for each core leg as: $A_1=71\text{mm}^2$, $A_2=71\text{mm}^2$ and $A_c=129\text{mm}^2$. This E-I combination yields a window areas of 29mm^2 . All of these areas are close to the calculation results. So these cores were eventually selected.

The saturation flux density for the 3F3 materials is about $B_{\text{sat}}=0.35\text{T}$. If the center post is not gapped, the required outer leg gapping are estimated to be 0.20mm (refer to Eq. 3-55).

The PCB planar winding is adopted. Four winding arrangements, as shown in Figure 5-3 were investigated. Case 1 and Case 2 employ the eight-layer PCB winding. Case 3 and Case 4 employ four-layer PCB winding for twelve-turn primary winding and separate copper foil for the secondary winding. The purpose of the Case-3 and Case-4 winding structure is to use fewer layers of PCB and to reduce costs.

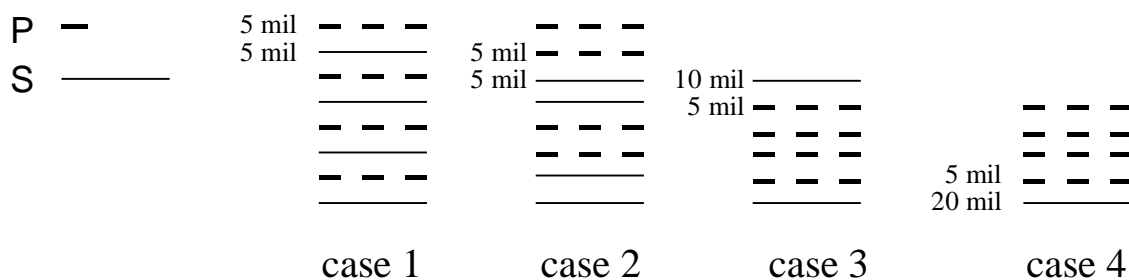


Figure 5-3 Four winding arrangements

Table 5-1 Comparison of AC winding loss and leakage inductance for the winding arrangements shown in Figure 5-3. 2-D FEA solver was used to obtain this result (fs=100KHz)

	Case 1	Case 2	Case 3	Case 4
AC winding loss (W)	0.23	0.26	0.24	0.38
Leakage inductance (nH)	72	232	354	1072

It can be seen from Table 5-1 that Case 1 has the minimum ac winding loss as well as the minimum leakage inductance. As discussed previously, the leakage inductance may affect the output ripple voltage and complicate the choice of capacitor, it is desirable to minimize the leakage inductance of windings. Therefore, the Case 1 winding arrangement was adopted.

The complete piece of winding consists of one power winding and one auxiliary gate-drive winding. The power winding is an eight-layer board, 4oz copper on an FR4 substrate. The complete assembly is shown in Figure 5-4.

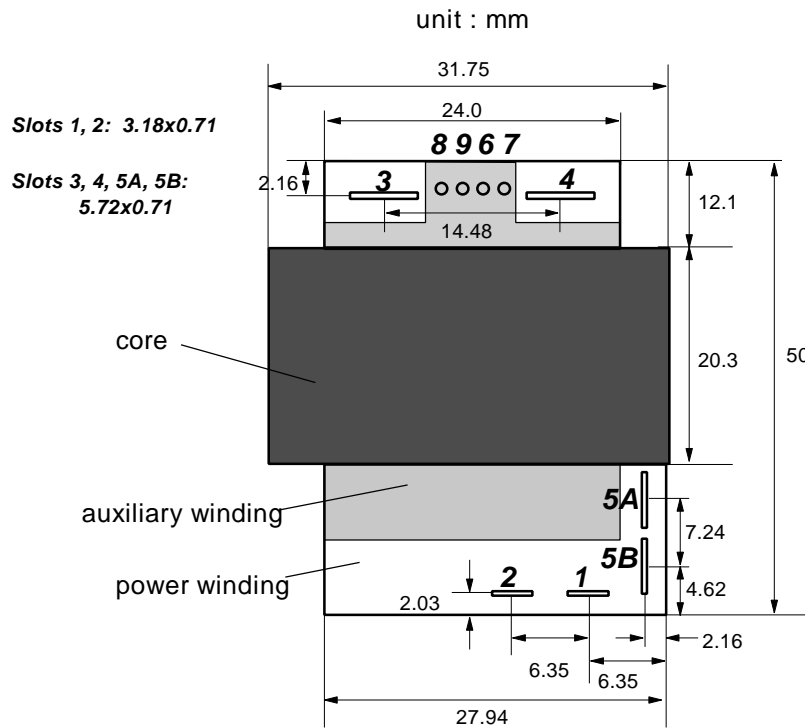


Figure 5-4 Mechanical outline of complete magnetic device

5.1.3. Stability Issues

Because of the existence of C_c on the primary side, the small signal model of the proposed FI²M circuit is a fourth-order system, as analyzed in Appendix 2. The average circuit model is shown in Figure 5-5(b), with all the variables and parameters defined in Appendix 2. Though this circuit model includes three equivalent inductances, these three inductors form a loop, and therefore, only two inductor currents are independent variables.

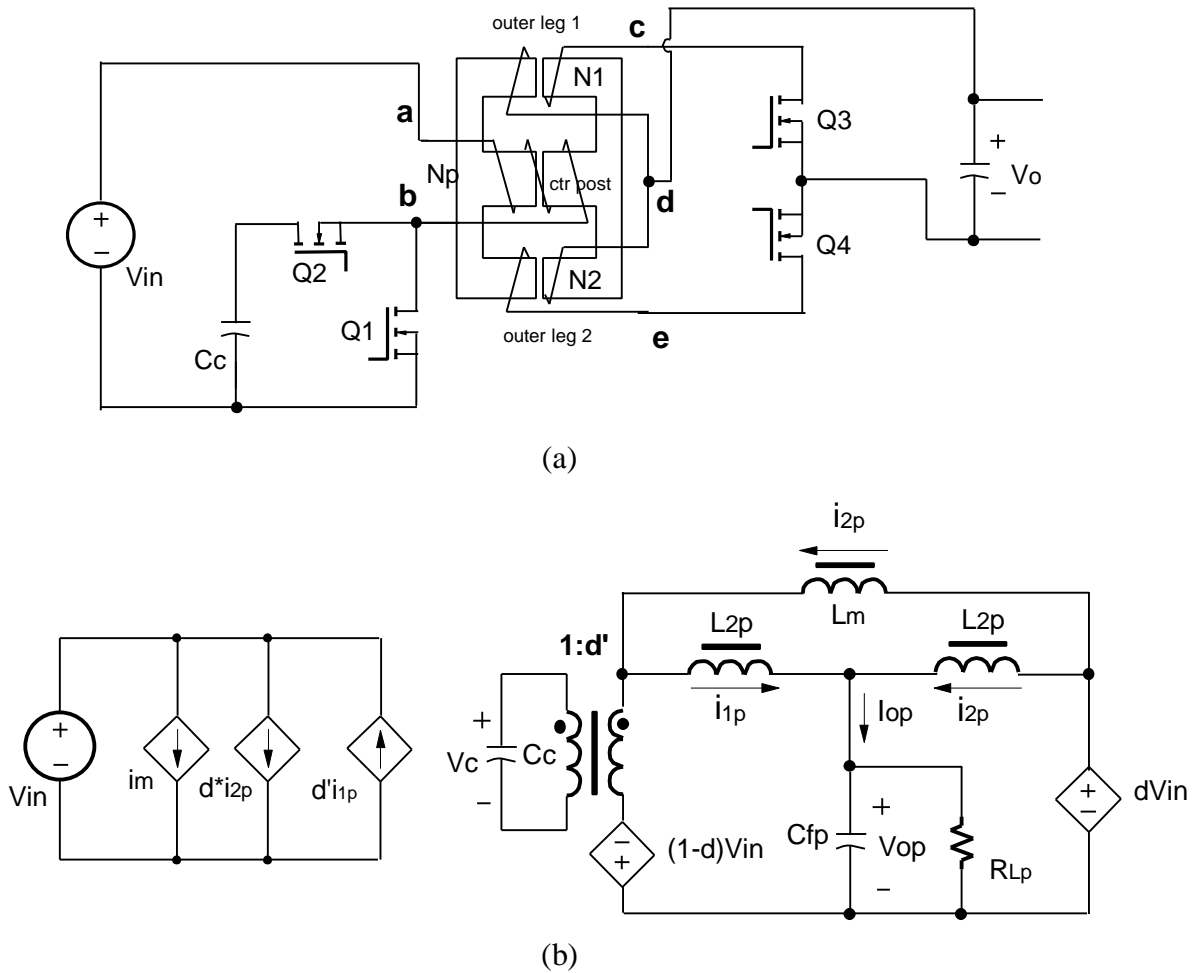


Figure 5-5 Average circuit model for power stage (a) power stage, (b) average circuit model

The Control to Output transfer function is expressed as

$$G_{oc} = \frac{\hat{V}_o}{\hat{V}_{con}} = G_{od} \cdot FM \quad \text{Eq. 5-2}$$

where FM is the PWM modulation gain. G_{od} , the duty-cycle-to-output transfer function, is derived to be [Appendix 2]:

$$G_{od} = \left. \frac{\hat{V}_o}{\hat{d}} \right|_{\hat{U}=0} = \frac{1 + s^2 \left(C_c L_{1p} L_m - C_c L_{2p} L_m \frac{D}{D'} \right) / \left[D'^2 (L_{1p} + L_{2p} + L_m) \right]}{\Delta(s)} \frac{V_{in}}{N}$$

Eq. 5-3

where D is the steady state duty cycle, $D' = 1 - D$, and

$$\Delta(s) = 1 + s \frac{L_{2p} (L_{1p} + L_m)}{R_{LP} (L_{1p} + L_{2p} + L_m)} + s^2 \left[\frac{L_{2p} (L_{1p} + L_m) C_{fp}}{L_{1p} + L_{2p} + L_m} + \frac{L_m (L_{1p} + L_{2p}) C_c}{(L_{1p} + L_{2p} + L_m) D'^2} \right] + s^3 \frac{C_c L_{1p} L_{2p} L_m}{R_{LP} D'^2 (L_{1p} + L_{2p} + L_m)} + s^4 \frac{C_c L_{1p} L_{2p} L_m C_{fp}}{D'^2 (L_{1p} + L_{2p} + L_m)}$$

Eq. 5-4

The control-to-output function consists of two pairs of double-poles and two zeroes. All of the poles are duty cycle dependent. A detailed discussion can be found in Appendix 2. The worst-case design for the control loop is the light load, minimum line (or high duty cycle) condition. In order to avoid the double-pole peaking and the low frequency pole, the compensator must be able to make the loop gain cross 0dB well before the first low frequency pole.

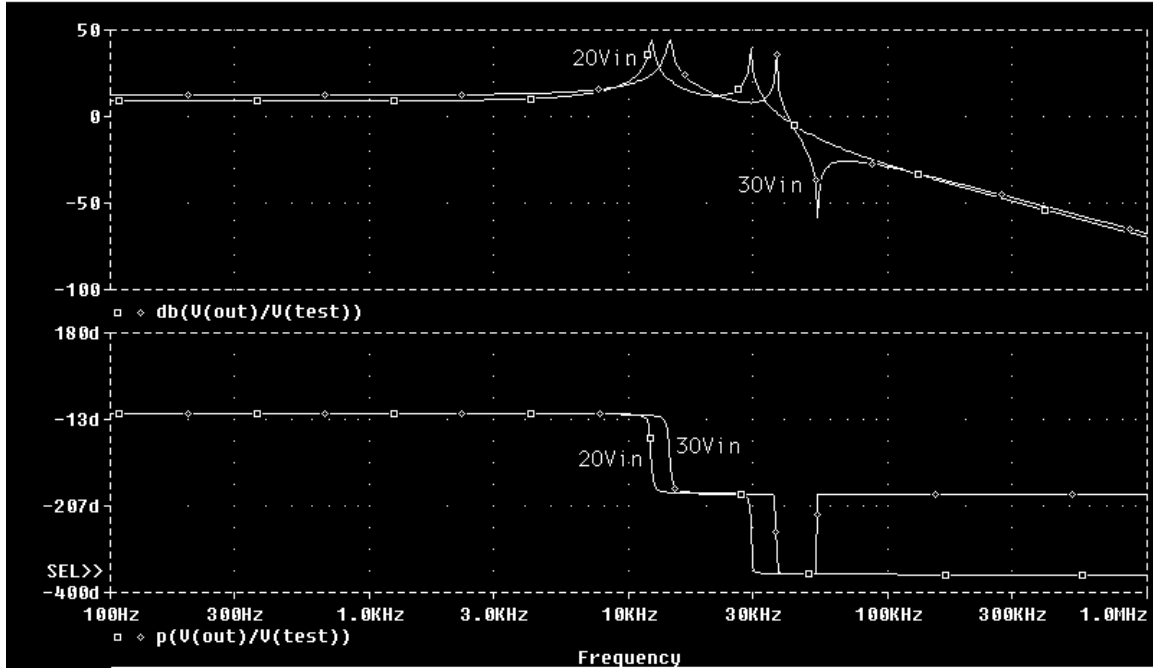


Figure 5-6 Control-to-output function under different duty cycle. In this plot: at 20Vin, $D > D_{crit}$; at 30Vin, $D < D_{crit}$. In this plot, $V_{in}=20-30V$, $V_o=2.8V$, $I_o=1A$, $f_s=200kHz$, $N=4:1$, $L_m=47\mu H$ (measured from the primary side), $C_c=0.68\mu F$, $L_1=L_2=1.9\mu H$ (measured from the secondary side), $C_f=110\mu F$ MLC (measured from the secondary side)

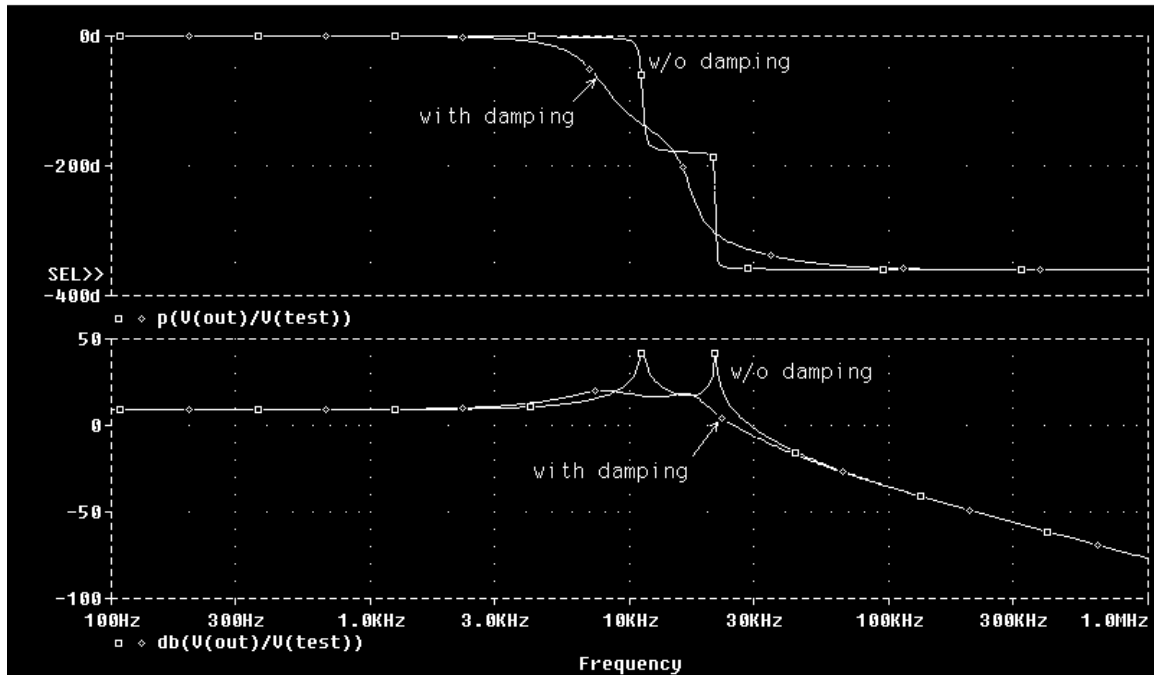
However, the peaking at the double pole is usually very high. Any noise near that frequency can easily ignite an oscillation problem. In particular, when several modules are in parallel, the modules tend to oscillate during the large signal transient (line or load transient). In practice, these oscillations usually result in damage to semiconductor devices.

The origin of the problem can be traced from the average circuit model shown Figure 5-5(b): C_c resonates with the inductors and introduces additional double-poles and double zeros compared to the Buck-type converters. As the duty cycle changes, the equivalent C_c present in the average circuit also varies. This causes the moving poles and zeroes. Since there is no resistance across C_c , there is high Q peaking at two double-pole positions. To alleviate the problem, a simple damping branch may be added to minimize the effect of C_c , as shown in Figure 5-2(a).

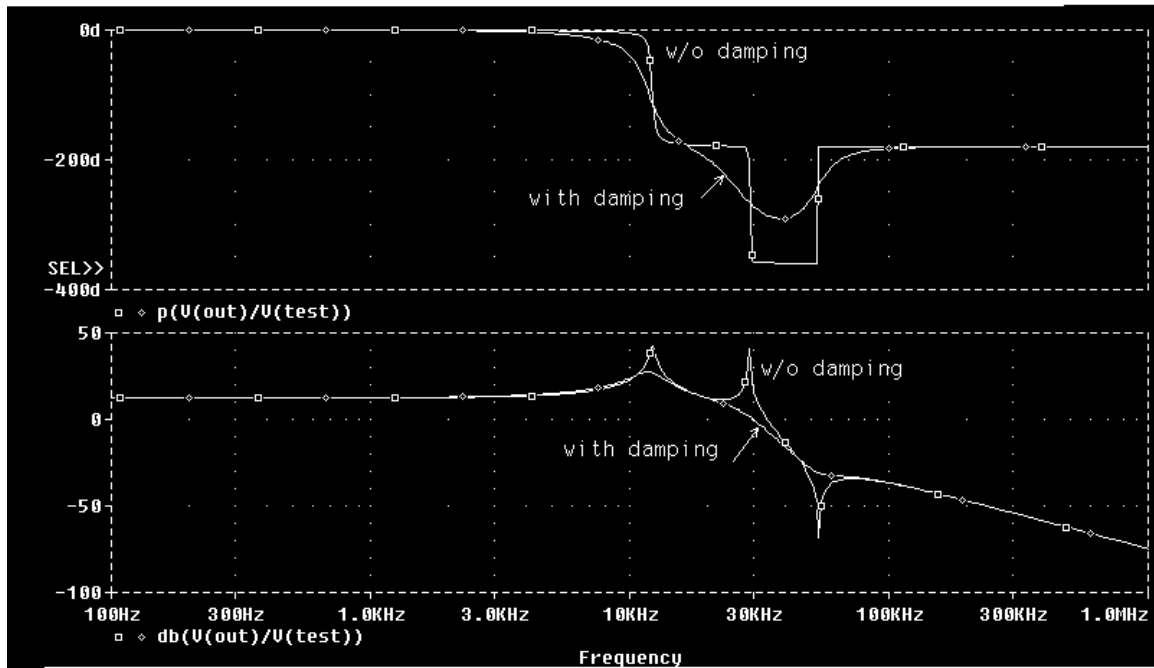
Figure 5-7 shows the plots of the control-to-output function with and without the damping branch. It can be seen that each pair of poles and zeroes are damped by this

branch. Compared to the control loop design without the damping branch, the control loop with the damping branch is more stable around the second pair of poles because of the reduced peaking at this point.

Practice has proved that damping branches can effectively solve the oscillation problems in the FI²M circuit during large signal transients. The immunity to noises also improves for the multi-module parallel operation.



(a) $D > D_{crit}$



(b) $D < D_{crit}$

Figure 5-7 Plots of control-to-output function with and without damping branch: $C_d=3C_c$, $K_r=4$ (a) $20V_{in}$, $D > D_{crit}$ (b) $30V_{in}$, $D < D_{crit}$

5.1.4. Experimental Results

Figure 5-8 shows the measured power stage efficiency of the breadboard prototype. Because each MOSFET uses only a TO-220 heat sink, a bench fan was used. Efficiency was measured after the circuit operated for 15 minutes. As the load current varies from 10% to 100% of full load current, the efficiency was always higher than 87%. In most of the load range (4A-24A), an efficiency of higher than 90% was measured.

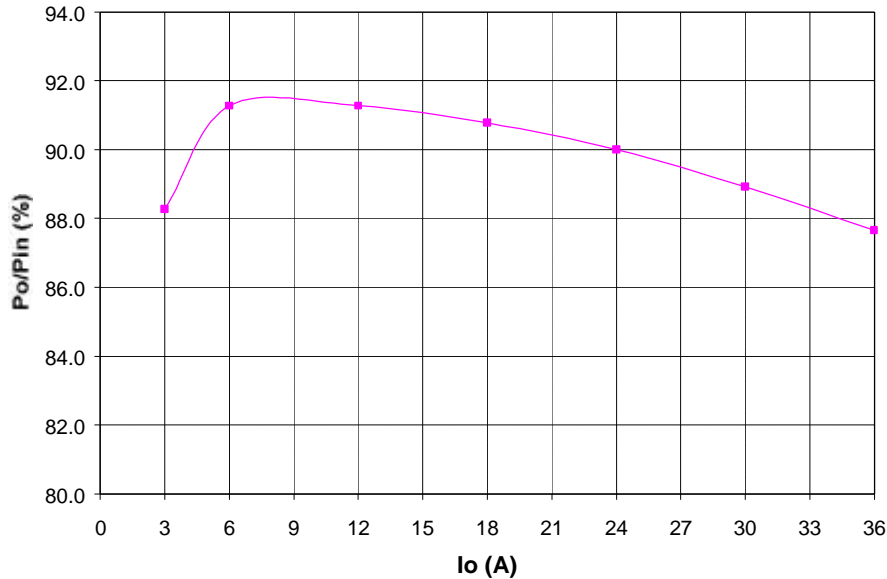


Figure 5-8 Measured power stage efficiency vs. load current, $V_{in}=70V$, $V_o=2.55V$

The following shows another example of applying the FI²M circuit .

Example 5-2 The electrical requirements of this power module are specified as follows:

Input: 48V (+/-10%)

Output: 1.2-1.8V/70A

Efficiency: >80% for $V_o=1.2-1.8V$

Because there is no redundancy requirement, it is desirable to use only one converter instead of several interleaved converters to minimize cost. Several low-voltage MOSFETs are paralleled to implement each synchronous rectifier because of the requirement of the high output current. The relatively large gate charges and slow reverse recovery speed of the body diodes within these MOSFETs usually limit the practical frequency range to a couple of hundred KHz. Under these constraints, the proposed integrated magnetic circuit appears to be a perfect topology to minimize the size of the overall circuit, especially the size of the capacitor and magnetic components.

The preliminary design employs the FI²M circuit shown Figure 5-2. The IRF3415 (150V MOSFET) is used to implement the main switch Q1, and IRF630 is adopted for the

auxiliary switch Q2. On the secondary side, four MTP75N03HDLs are paralleled for each synchronous rectifier. The gate-drive technique for the SR is the same as that shown in Figure 5-2(b). The turns ratio of the transformer is 12:1. The single-turn secondary configuration is adopted. The auxiliary gate-driving winding is one turn. As a result, the gate of Q3 sees the reflected input voltage, about 8V. The gate voltage of Q4 varies from 8V to 11V as the load changes from light load to full load. The integrated magnetic core is a modified planar E/I core (E32 from Philips) with outer legs gapped by 0.34mm and the center post gapped by 0.1mm. The purpose of adding the gap into the center post is to obtain ZVS for Q1. Otherwise, because each SR utilizes four MOSFETs with huge gate capacitance in parallel, the gate-driving loss of SR will be significant if Q1 is not turned on at zero voltage. The power winding is a PCB planar winding made by 5 mil Cu on an FR4 substrate. The complete winding consists of 8 layers of copper: 4 primary layers in series and 4 secondary layers in parallel. Each primary layer consists of three turns and each secondary layer only one turn. The primary and secondary layers are interleaved as “3P-S-3P-S-3P-S-3P-S” to minimize leakage inductance and ac high-frequency loss.

Figure 5-9 shows the measured power stage efficiency with the preliminary breadboard design. The efficiency is always higher than 81% throughout the output voltage range: 1.2-1.8V. Because the breadboard layout was intended for the 30A-output application, the conduction loss on the negative output trace alone accounts for about 2% of the efficiency drop. By optimizing the layout packaging design, the worst case overall efficiency can be improved further.

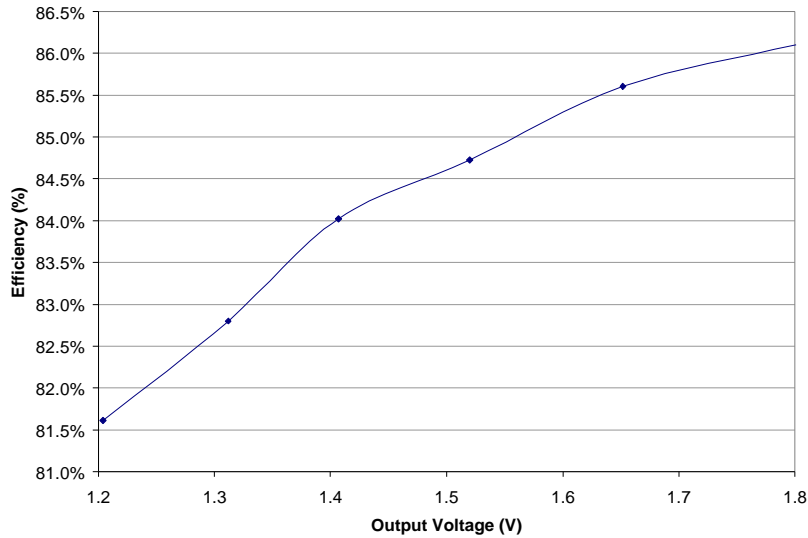


Figure 5-9 Measured efficiency with 1.2-1.8V output

5.2. Design of HDHE Low Voltage, High Current Power Supplies Using HBI²M Circuit

HBI²M circuit can achieve the smallest size, the lowest profile, and the best performance if the duty cycle range is always near 50%. The following application, which was intended for an aircraft distributed power system, is a perfect example for implementing this circuit [C27].

Example 5-3

Input: 60Vdc (well regulated)

Output: 3.3V/100W

Efficiency: 90%

Ultimate Goal of Profile: 0.18"

Ultimate Goal of Footprint: 1.5"x1.5"

For the given input and output voltage, an HBI²M with turns ratio of 4:1 is a perfect fit because the duty cycle can be close to 50%. The worst-case voltage and current stress on the semiconductor devices can be minimized.

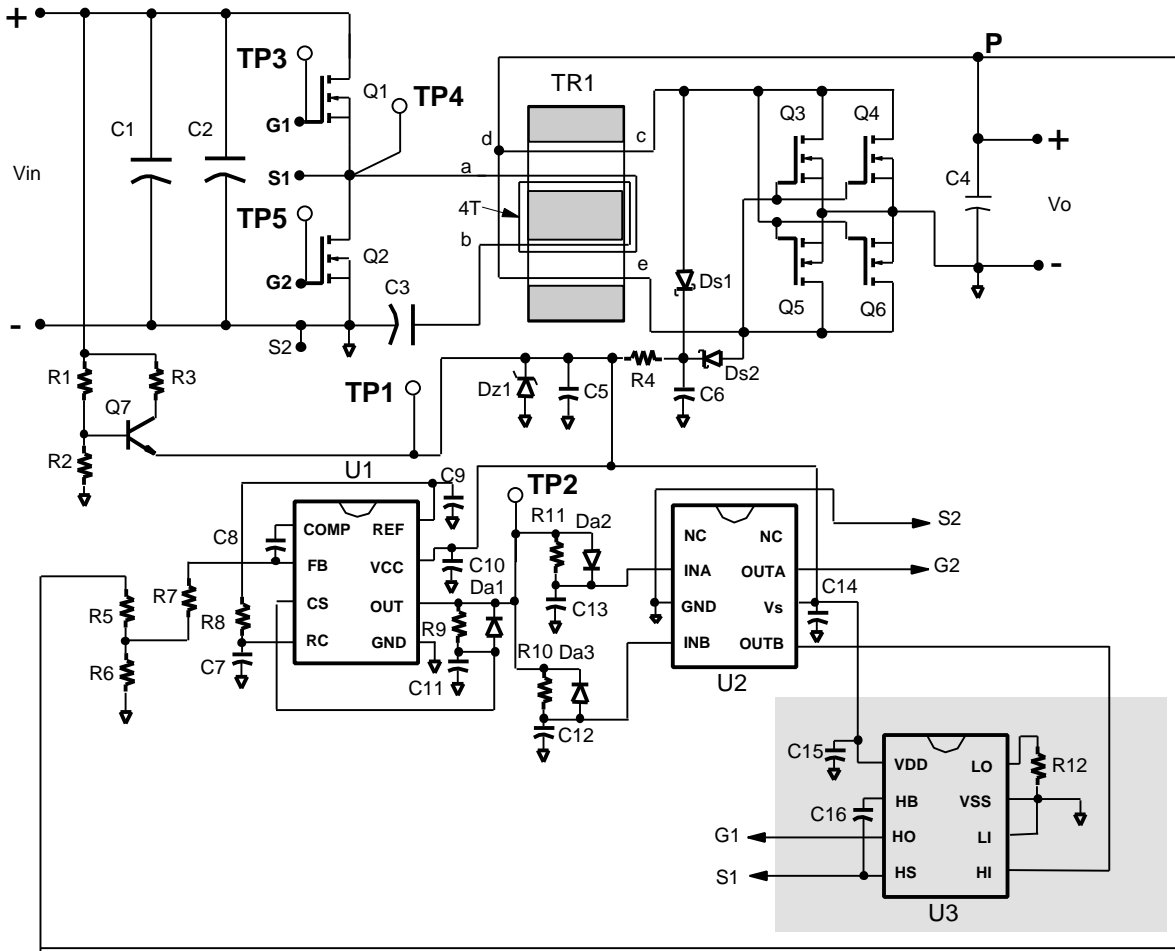


Figure 5-10 Complete schematic of HDHE hybrid module using HBI²M topology

5.2.1. Electrical Design

The complete schematic is shown in Figure 5-10. In this design, the steady state duty cycle at full load is about 45% to allow some room for the load regulation. The switching frequency is chosen to be 500 kHz. The primary switches chosen are IRL540, which are logic-level devices. The reason for using a logic-gate device is to reduce the gate-drive losses, which are not negligible at 500 kHz. Each of the secondary-side synchronous rectifiers consists of two logic-level MOSFETs (MTP75N03HDL) in parallel. Because these MOSFETs are directly driven by the secondary-side voltage waveform, the on-voltage applied on the gate of the MOSFETs is lower than 10V. Choosing the logic-gate MOSFET to implement the synchronous rectifiers ensures the proper turn-on of these devices. Because the body diode of the MTP75N03HDL is very fast, the reverse recovery

problem of the body diode is not severe. Therefore, no Schottky diodes are used to parallel with Q3 and Q4.

5.2.2. Magnetic Design

The gap in the center post decreases L_m and may help achieve the ZVS of the primary switches at lighter load. However, the primary conduction loss increases if the gap in the center post is too big. In this design, there was a minimal gap in the center post, which is caused by the interface of I-core and E-core; 3F4 material is selected, for which $B_m=60$ mT, resulting in a loss density of $300\text{mW}/\text{cm}^3$ at 500 kHz [D5]. By choosing $N_s=1$, the cross-sectional area of each core leg is calculated to be $A_{1\text{min}}=38\text{ mm}^2$, $A_{2\text{min}}=30\text{ mm}^2$, $A_c=69\text{ mm}^2$. These dimensions are close to those of a commercially available core (E22/5.7/16-3F4), where $A=A_1=A_2=40\text{ mm}^2$, $A_c=80\text{ mm}^2$. Therefore, the E22 planar EI structure is chosen for this design. To simplify the design, the gaps in the two outer legs are chosen to be equal.

By choosing $B_{\text{sat}}=0.3\text{ T}$, $N_p=4$, $I_{\text{in,dc}}=1.9\text{ A}$, the required gap is computed to be $l_{g,\text{min}}=0.083\text{ mm}$, according to the equations in Ch. 4. So $l_g=0.09\text{ mm}$ was chosen.

Three types of winding arrangements were investigated, as shown in Table 5-2. The FEA simulation (2-D) results showed that in Case 1, the “2P-S-2P-S” winding arrangement gives minimum power loss at 500kHz. The fully-interleaving structure helps reduce the leakage inductance and the ac resistance of windings [D1, D6].

Table 5-2 Winding power loss with different winding arrangement obtained by FEA 2-D simulation, E22 Core, $I_o=30\text{ A}$, $f_s=500\text{ kHz}$.

	Case 1	Case 2	Case 3
Winding Arrangement	2P-S-2P-S	S-2P-2P-S	2P-2P-S-S
Leakage inductance (nH)	16	23	58
AC winding loss (W)	0.36	0.41	0.75

Note: “2P” stands for two primary winding turns in one layer, “S” represents one secondary winding turn in one layer

The Case 1 winding configuration was, therefore, adopted. Two layers of primary windings are in series to form four turns; two layers of secondary windings are paralleled to share the current. The PCB winding is made of four-ounce copper on one-mil thick flex material. The outline of the winding featured two primary terminations and three secondary terminations.

5.2.3. Packaging Design

A preliminary hybrid module, including the power stage, control circuit, and self-bias circuit, was developed. The power stage has been fabricated with 8-mil direct bond copper on a ceramic substrate. Every component was reflow soldered onto the board. The MOSFETs, PWM controller, and MOSFET driver are in bare die form; the capacitors are in a surface-mounted package. The primary-side MOSFETs (IRL540) source connections use single 5-mil aluminum wire bond. The secondary-side MOSFET source connections use two 15-mil aluminum wire bonds. The choice of the wire bond was made to minimize the power loss. The E22/5.7/16-3F4 core was milled down and gapped 0.09mm at the outer legs. The profile of the whole magnetic component is 0.18 inch. The control circuit is fabricated on a separate small board, which is placed above the output trace to minimize the footprint of the whole module.

5.2.4. Experimental Results

An overall efficiency of close to 90% was achieved at 500 kHz, 3.3 V, and 100 W output. Figure 5-11 shows the experimental waveforms of Q2 in the power stage. Because the leakage inductance of the primary winding and the circuit trace was utilized, the ZVS turn-on of primary switches was accomplished by properly adjusting the gate timing. Figure 5-12 shows a picture of the preliminary hybrid module. The footprint of the preliminary module measures 2.0"x1.6" and its height is 0.21". The resulting power density is about 130W/in³. Although still lower than the ultimate goal, it is much higher than the state-of-art power density of a commercial power supply for the same output requirement. Further improvement on the power density can be made by integrating all the control circuitry into one chip and improving the layout design. The efficiency can be improved further with the utilization of better MOSFET devices.

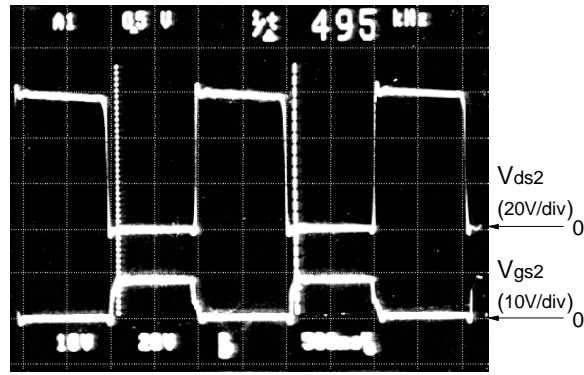


Figure 5-11 Experimental waveforms on Q2

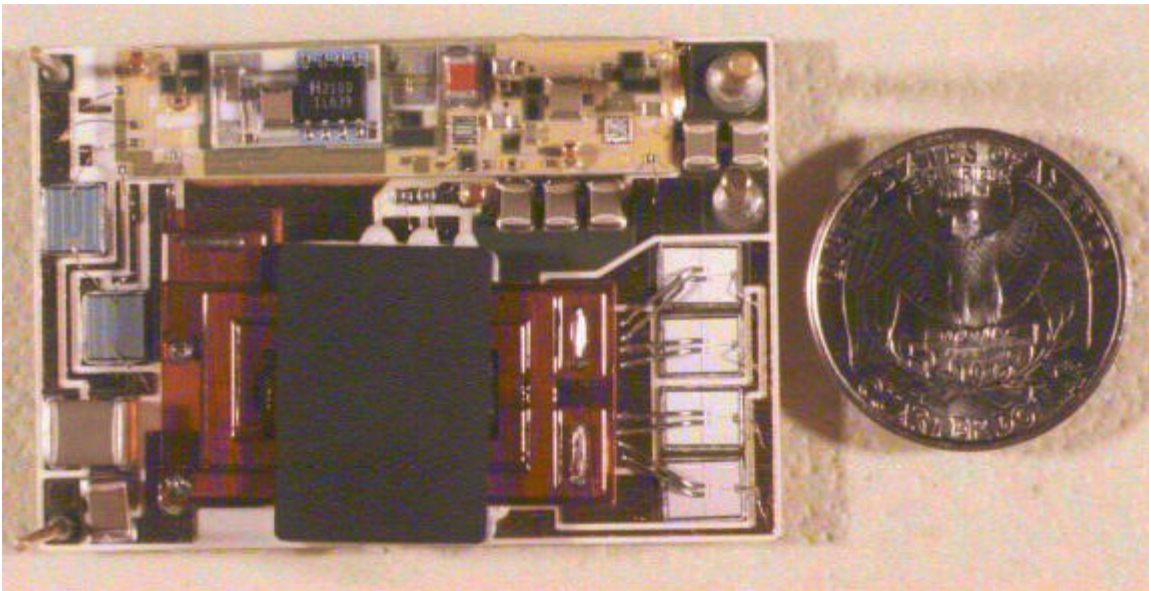


Figure 5-12 Picture of the preliminary hybrid module