

9. APPENDIX

9.1 Appendix A

Appendix A consists of outlines of the derivations of key design equations developed in Sections 3.3 and 3.6.

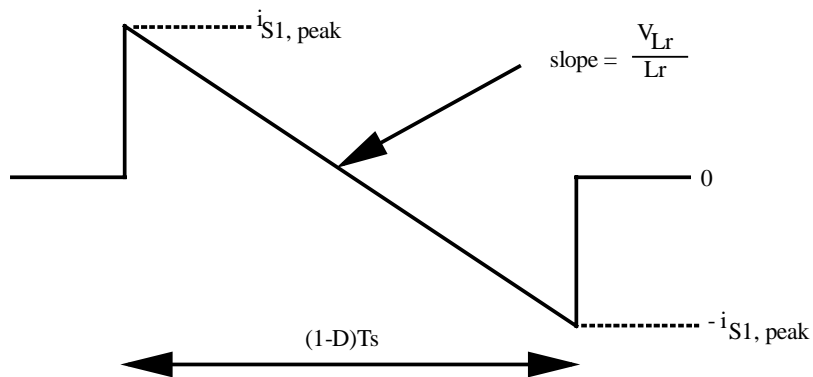
9.1.1 Derivations for Section 3.3

For the derivations in this section, the following simplifying assumptions are made:

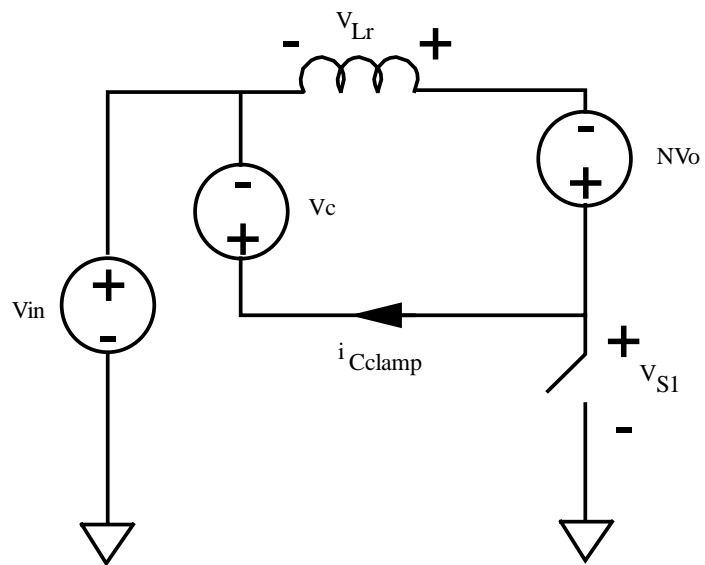
- the clamp current is piece-wise linear instead of quasi-sinusoidal,
- clamp capacitor voltage is constant (i.e. clamp capacitor is assumed infinite in value),
- the duration of the intervals $T_1 - T_2$ and $T_4 - T_6$ shown in Fig. 3.3 is short enough compared to the duration of interval $T_1 - T_6$ to allow them to be neglected,
- $D = D_{\text{eff}} = D_{S1}$,

Eq. 3.6: Figure A.1 shows the idealized clamp current waveform and the simplified circuit topology during switch S1's "off" time. The switch voltage is given by:

$$V_{S1} = V_{in} + V_{Lr} + NV_O = V_{in} + \frac{2L_r i_{S1,peak}}{(1-D)T_S} + NV_O. \quad (\text{A.1})$$



(a) Idealized clamp capacitor current waveform.



(b) Simplified topological state - S1 "off", S2 "on."

Fig. A.1 Idealized clamp current and topological state during S1 "off."

The peak switch current (which is equal to the peak magnetizing current and peak resonant inductor current) is determined by applying the principle of power balance to the converter. Under the assumptions stated above, the expression for the peak switch current is the same as that obtained for a non active-clamp CCM flyback. This is simply the average inductor current plus one-half of the peak-to-peak inductor ripple current, and is given by Eq. (3.9). Substituting Eq. (3.9) into Eq. (A.1) results in Eq. (3.6).

Eq. 3.7: Referring to Fig. A.2, the duration of the interval ΔDT_s is given by:

$$\Delta DT_s = \frac{L_r}{V_{in} + NV_O} (i_{Lm,peak} + i_{Lm,valley}). \quad (A.2)$$

We now need an expression for the second factor in Eq. (A.2) in terms of D_{S1} . Resorting to power balance and assuming $\Delta D \ll D_{S1}$ yields:

$$i_{Lm,peak} + i_{Lm,valley} = \frac{2P_O}{V_{in}D_{S1}}. \quad (A.3)$$

Substituting Eq. (A.2) into Eq. (A.3) yields the second part of the expression given in Eq. (3.7).

Eqs. (3.8) and (3.10): Eq. (3.8) follows directly from Eq. (3.5). Equation (3.10) is complicated by the fact that the resonant capacitor voltage is a function of the resonant inductor voltage, which is given by the middle term in Eq. (A.1). However, under the assumption of small duty cycle loss, $V_{Lr} \ll V_{in} + NV_O$ during clamping portion of the switching cycle. Therefore, for ZVS of S1:

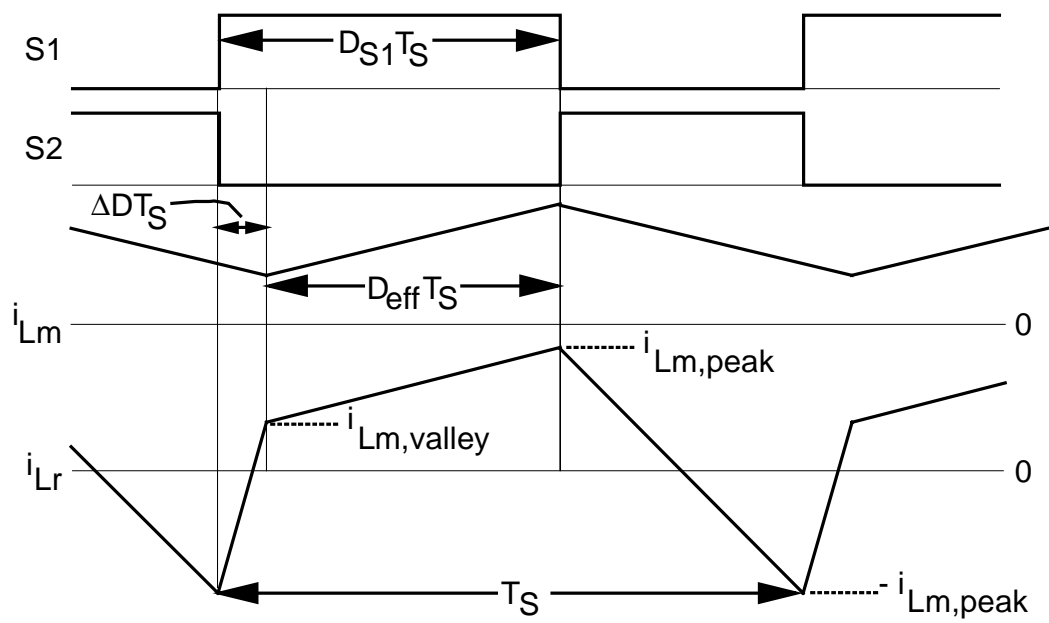


Fig. A2 Idealized waveforms for computing the effective duty cycle.

$$\frac{1}{2} L_r \overline{i_{L_r}^2} \Big|_{@ S2 \text{ turn-off}} \geq \frac{1}{2} C_r V_{C_r}^2 \Big|_{@ S2 \text{ turn-off}} . \quad (\text{A.4})$$

For $V_{C_r} \approx V_{in} + NV_O$ Eq. (A.4) can be solved for L_r to yield Eq. (3.10).

Eq. (3.11): The RMS current flowing in the resonant inductor can be calculated with the aid of Figs. 3.4 and A.2. If we assume negligible duty cycle loss, the slope of the resonant inductor current becomes infinite during the $T_4 - T_7$ interval shown in Fig. 3.4 (i.e., the duration of the $T_4 - T_7$ interval is zero). The RMS value of the current can then be more easily approximated using two piece-wise linear intervals over a switching cycle:

$$I_{L_r, RMS} \cong \sqrt{\frac{1}{T_S} \int_0^{DT_S} i_{L_r}^2(t) dt + \frac{1}{T_S} \int_{DT_S}^{T_S} i_{L_r}^2(t) dt} . \quad (\text{A.5})$$

Integrating Eq. (A.5) yields an expression for the RMS current in terms of the peak switch current. Equation (3.9) can then be used to obtain Eq. (3.11).

Eqs. (3.12) and (3.13): Both of these equations can be derived with the aid of Fig. A.1. It is assumed the body diode of S2 will conduct the positive portion of the clamp current and the MOSFET will conduct the negative portion. With a linear clamp current waveform and equal but opposite endpoint values, this implies each “part” of S2 will conduct for half of the $(1-D)T_S$ interval. Therefore, the average body diode current is:

$$I_{S2 \text{ body diode, avg}} \cong \frac{1}{T_S} \int_0^{(1-D)T_S/2} i_{Cclamp}(t) dt = i_{S1, peak} \frac{1-D}{4} . \quad (\text{A.6})$$

The MOSFET RMS current is obtained in a similar manner:

$$I_{S2,MOSFET,RMS} \cong \sqrt{\frac{1}{T_S} \int_0^{(1-D)T_S/2} i_{Cclamp}^2(t) dt} = i_{S1,peak} \sqrt{\frac{1-D}{6}}. \quad (A.7)$$

Eqs. (3.14) through (3.16): Equation (3.14) results from the resonance between L_r and C_{clamp} . We want half the resonant period to be greater than $S1$'s maximum off-time:

$$\frac{T_{Lr,Cclamp}}{2} = \pi \sqrt{L_r C_{clamp}} \gg (1-D)T_S. \quad (A.8)$$

Eq. (A.8) can be solved for C_{clamp} to yield Eq. (3.14). Once an expression is found for the resonant inductor voltage during the clamping cycle (middle term of Eq. (A.1)), the derivation of Eq. (3.15) is straightforward. Equation (3.16) can be derived from Fig. A.1:

$$I_{Cclamp,RMS} \cong \sqrt{\frac{1}{T_S} \int_0^{(1-D)T_S} i_{Cclamp}^2(t) dt} = i_{S1,peak} \sqrt{\frac{1-D}{3}}. \quad (A.9)$$

Eqs. (3.17) through (3.19): Equations (3.17) through (3.19) can be derived with the aid of Fig. A.3. As shown in the figure, the diode current waveform has been approximated as piece-wise linear. This reflects the assumption that the clamp capacitor

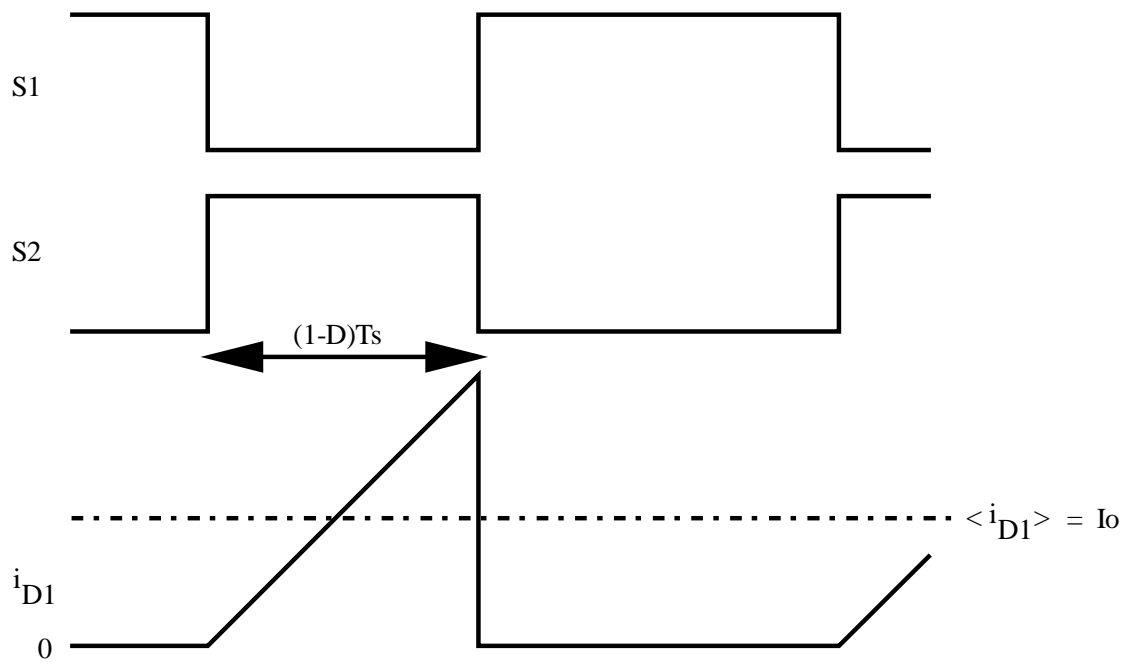


Fig. A.3 Simplified output rectifier waveform.

current is linear during the clamping interval. Once again, if it is assumed $L_r \ll L_m$, the rectifier turn-off current slope can be approximated as infinite. The peak diode current can be obtained from knowledge of the average rectifier current:

$$\frac{P_O}{V_O} = I_O = \frac{I}{2T_S} (1-D)T_S i_{DI,peak} . \quad (\text{A.10})$$

The output capacitor ripple current is equivalent to the output rectifier RMS current with the DC portion of the current removed. Therefore, two intervals of integration have to be considered:

$$I_{Co,RMS} = \sqrt{\frac{I}{T_S} \int_0^{DT_S} \left(i_{DI}(t) - \frac{P_O}{V_O} \right)^2 dt + \frac{I}{T_S} \int_{DT_S}^{T_S} \left(i_{DI}(t) - \frac{P_O}{V_O} \right)^2 dt} . \quad (\text{A.11})$$

Integrating Eq. (A.11) and using the result of Eq. (3.17) yields Eq. (3.18). The transformer secondary is in series with the output rectifier, so their RMS currents are identical. Since the DC component of current is present we have:

$$I_{sec,RMS} = \sqrt{\frac{I}{T_S} \int_0^{(1-D)T_S} i_{DI}^2(t) dt} . \quad (\text{A.12})$$

Integrating Eq. (A.12) and using the result of Eq. (3.17) yields Eq. (3.19).

9.1.2 Derivations for Section 3.6

The derivations of all the equations given in Section 3.6 make use of the following assumptions:

- unity power factor operation with $F_S \rightarrow \infty$ (compared to F_{line}),
- flyback “transformer” leakage inductance is small enough to neglect its effects on circuit operation,
- the clamp and output capacitors are infinite in value,
- no delay between the turn-off of S2 and turn-on of S1.

Figure A.4 shows the idealized converter waveforms over a switching cycle under the constraints imposed by the assumptions listed above.

Eq. (3.24): For component selection purposes, it is necessary to know the clamp capacitor RMS current averaged over half of the line cycle (120 Hz). Compared to averaging over a switching cycle, line cycle averaging considerably complicates the derivation, necessitating a further simplification of the clamp capacitor waveform. The simplified version is shown in Fig. A.5. I_C is selected so that the ideal and simplified waveforms have the same positive and negative areas. Therefore:

$$I_C = \frac{I}{2} i_{S1} \Big|_{peak} . \quad (A.13)$$

Since the averaging is done over half of the line cycle I_C is time dependent (a function of S1’s peak switch current which is in turn a function of the converter duty cycle). Therefore, S1’s peak switch current needs to be determined as a function of where the

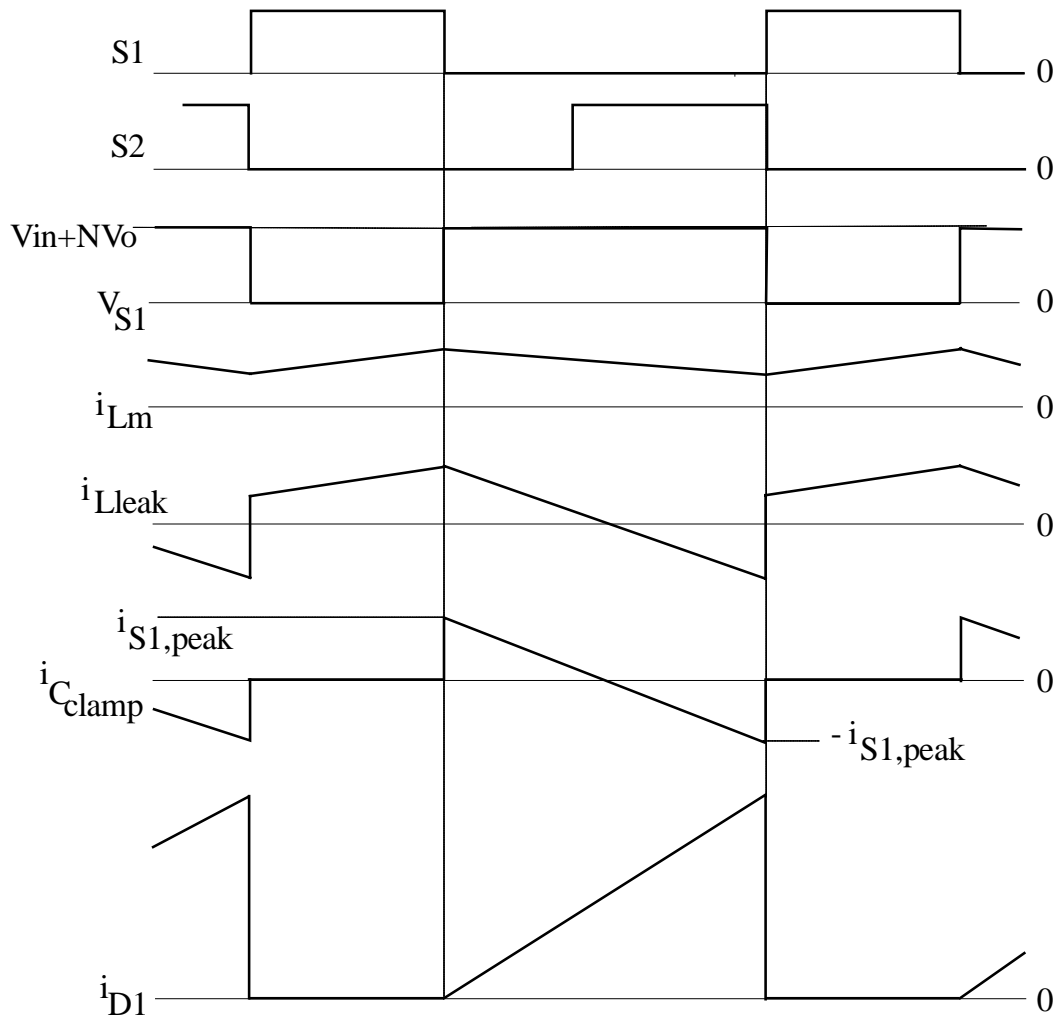


Fig. A.4 Switching cycle active-clamp flyback ideal waveforms.

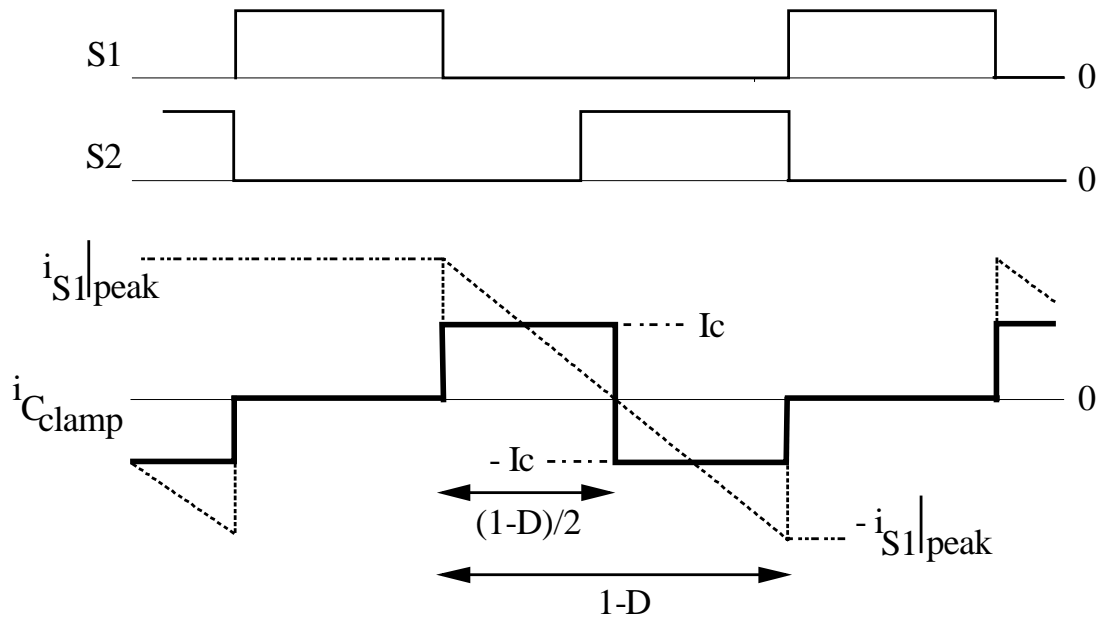


Fig. A.5 Simplified clamp capacitor current waveform.

instantaneous operating point is on the input line cycle ($T_s \rightarrow 0$ compared to the line cycle period). Neglecting ripple current in the switch:

$$I_{S1}(\phi) = \frac{I_{AVG}(\phi)}{D(\phi)}. \quad (\text{A.14})$$

In Eq. (A.14) the one-half the line cycle period is considered to be normalized to the interval $[0, \pi]$ and ϕ is an arbitrary point on that interval. $I_{AVG}(\phi)$ is the average input line current and is given by:

$$I_{AVG}(\phi) = \frac{\sqrt{2}P_O}{\eta V_{RMS}} \sin(\phi). \quad (\text{A.15})$$

The instantaneous duty cycle is:

$$D(\phi) = \frac{V_O}{V_O + \frac{\sqrt{2}V_{RMS}}{N} \sin(\phi)}. \quad (\text{A.16})$$

Neglecting inductor ripple current, $I_{S1}(\phi) = I_{S1}(\phi)|_{\text{peak}}$, and Eqs. (A.14) through (A.16) can be combined and substituted into Eq. (A.13) to yield an expression for I_C that is a function of the instantaneous operating point on the input line. The amplitude (I_C) of each ‘‘pulse’’ shown in Fig. A.5 is now known as a function of ϕ , but to calculate the RMS value the pulse area is required:

$$RMS\ value = \sqrt{\frac{1}{\pi} \sum_{line\ cycle} (\text{area of each pulse with amplitude squared})}. \quad (A.17)$$

From Fig. A.5 the pulse area is simply given by:

$$area = I_C^2(\phi)[1 - D(\phi)]. \quad (A.18)$$

Therefore, the estimated value of clamp capacitor 120 Hz ripple current can now be calculated:

$$I_{Cclamp,RMS} \approx \sqrt{\frac{1}{\pi} \int_0^{\pi} \frac{P_0^2}{2\eta^2 V_{RMS}^2} \sin^2(\phi) \left[\frac{1 - D(\phi)}{D(\phi)} \right] d\phi}. \quad (A.19)$$

Carrying out the integration called for in Eq. (A.19) yields Eq. (3.24).

Eq. (3.25): The active-clamp flyback transformer primary RMS (120 Hz) current is the root-sum-of-squares (RSS) combination of the clamp capacitor RMS current (Eq. (3.24)) and the RMS value of the primary switch current:

$$I_{pri,RMS} = \sqrt{I_{SI,RMS}^2 + I_{Cclamp,RMS}^2} = \sqrt{\frac{1}{\pi} \int_0^{\pi} I_{SI}^2(\phi) d\phi + I_{Cclamp,RMS}^2}. \quad (A.20)$$

Equation (A.20) is valid because the two current waveforms that comprise the transformer's primary current are non-zero over mutually exclusive intervals (over a switching cycle - see Fig. A.4). Substitution of Eqs. (A.14) and (3.24) into Eq. (A.20) yields Eq. (3.25).

Eq. (3.26): The flyback transformer's secondary is in series with the output rectifier and so has the idealized current waveform (i_{D1}) shown in Fig. A.4. Both the clamp capacitor and transformer secondary current waveforms share similar properties, hence, to make the mathematics tractable, the secondary current waveform will be simplified in an analogous manner. The simplified version is shown in Fig. A.6. I_{sec} is chosen so that the average value of the output rectifier's simplified "pulsed" current waveform yields the correct value of average rectifier current. Of course, this average is function of the line cycle, therefore:

$$I_{sec}(\phi) = \frac{\frac{2P_O}{V_O} \sin^2(\phi)}{1 - D(\phi)}. \quad (\text{A.21})$$

The RMS value is then calculated using Eq. (A.17) and an expression for the area calculated over a switching cycle:

$$area = I_{sec}^2(\phi)[1 - D(\phi)]. \quad (\text{A.22})$$

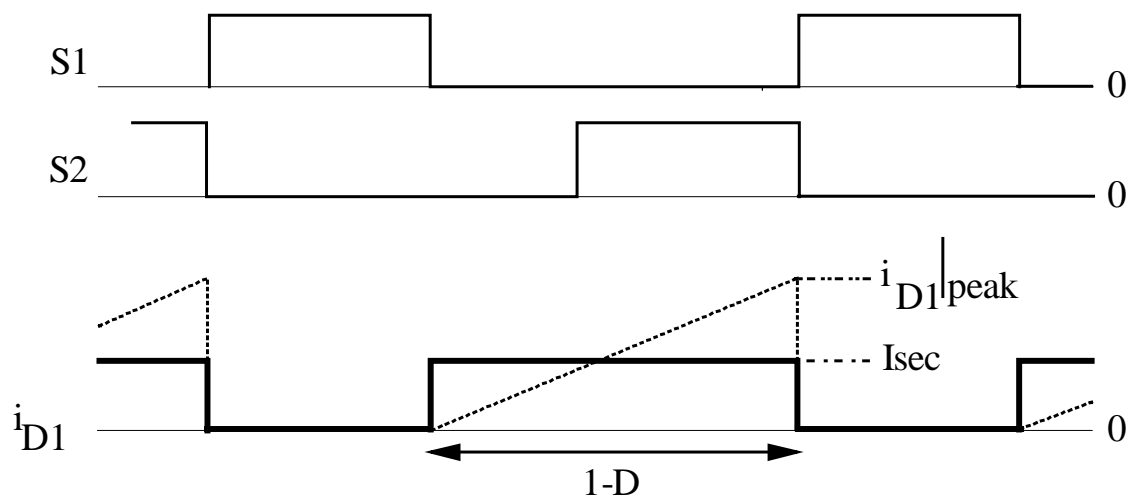


Fig. A.6 Simplified output rectifier current waveform.

Combining Eqs. (A.16), (A.21) and (A.22) and substituting into Eq. (A.17) yields Eq. (3.26).

9.2 Appendix B

Appendix B contains the netlists for the PSPICE simulations of Section 5.2.

9.2.1 Sinewave system, maximum load

LCC-SRR System Simulation for maximum load (400W total, 100 W each)

```
.PARAM Fs=300KHz, Ts={1/Fs}, D=0.4625 phi={(1-D)*Ts/2} td=117ns
.PARAM Lo = 31.1uH ;Lo for 300kHz = 28.14477uH; max. load: 31.1uH; min. load: 40uH
```

```
Vin boost 0 DC 380V
```

* Bridge Switches:

```
S1 boost 2 101 0 SW_ideal
```

```
D_S1 2 boost D_Ideal
```

```
C_S1 boost 2 133pF
```

```
S3 2 0 103 0 SW_ideal
```

```
D_S3 0 2 D_ideal
```

```
C_S3 2 0 133pF
```

```
S2 6 9 102 0 SW_ideal
```

```
D2 0 6 D_ideal
```

```
D_S2 9 0 D_ideal
```

```
S4 boost 7 104 0 SW_ideal
```

```
D4 6 boost D_ideal
```

```
D_S4 7 6 D_ideal
```

```
.model D_ideal D(Is=10uA)
```

```
.model SW_ideal VSWITCH(Ron=1m)
```

* Bridge Switch Control:

```
V_S1cntrl 101 0 PULSE(0V 1V {td} 10ns 10ns {Ts/2-td} {Ts})
```

```
R_S1cntrl 101 0 1
```

```
V_S3cntrl 103 0 PULSE(1V 0V 0s 10ns 10ns {Ts/2+td} {Ts})
```

```
R_S3cntrl 103 0 1
```

```
V_S2cntrl 102 0 PULSE(0V 1V {phi+td} 10ns 10ns {Ts/2-td} {Ts})
```

```
R_S2cntrl 102 0 1
```

```
V_S4cntrl 104 0 PULSE(1V 0V {phi} 10ns 10ns {Ts/2+td} {Ts})
```

```
R_S4cntrl 104 0 1
```

* Resonant Tank:

```
Cs 2 4 4510pF
```

```
Cp 4 5 4960pF
```



```

L 5 6 90uH

* isolation XFMR:
Lpri 4 5 1mH
Lsec bus+ bus- 62.5uH
K_isoxfmr Lpri Lsec 1
Rbus+ bus+ 0 10MEG
Rbus- bus- 0 10MEG

* SRR post-regulators:
X_SRR1 bus+ bus- Vo1 0 SRR
Rload1 Vo1 0 0.25
X_SRR2 bus+ bus- Vo2 0 SRR
Rload2 Vo2 0 0.25
X_SRR3 bus+ bus- Vo3 0 SRR
Rload3 Vo3 0 0.25
X_SRR4 bus+ bus- Vo4 0 SRR
Rload4 Vo4 0 0.25

.SUBCKT SRR +IN -IN Vo Vo_rtn
Lo +IN 1 {Lo}
Co 1 2 0.01uF
Lpri 2 -IN 64mH
Lsec1 3 Vo_rtn 1mH
Lsec2 Vo_rtn 4 1mH
K Lpri Lsec1 Lsec2 1
D1 3 Vo D_ideal
D2 4 Vo D_ideal
.model D_ideal D(Is=1mA)
Cf Vo Vo_rtn 150uF
.ENDS SRR

.TRAN 1us 100ms 99.9ms 10ns
.FOUR 300kHz 49 V([bus+],[bus-]) I(Lsec)
.OPTIONS RELTOL=0.01 ABSTOL=10uA
.PROBE

.END

```

9.2.2 Sinewave system, minimum load

LCC-SRR System Simulation for minimum load (80W total, 20 W each)

```

.PARAM Fs=300KHz, Ts={1/Fs}, D=0.246 phi={{(1-D)*Ts/2} td=117ns
.PARAM Lo = 40uH ;Lo for 300kHz = 28.145uH; max. load: 31.1uH; min. load: 40uH

Vin boost 0 DC 380V

* Bridge Switches:
S1 boost 2 101 0 SW_ideal

```

```

D_S1 2 boost D_ideal
C_S1 boost 2 133pF
S3 2 0 103 0 SW_ideal
D_S3 0 2 D_ideal
C_S3 2 0 133pF

S2 6 9 102 0 SW_ideal
D2 0 6 D_ideal
D_S2 9 0 D_ideal
S4 boost 7 104 0 SW_ideal
D4 6 boost D_ideal
D_S4 7 6 D_ideal
.model D_ideal D(Is=1mA)
.model SW_ideal VSWITCH(Ron=1m)

* Bridge Switch Control:
V_S1cntrl 101 0 PULSE(0V 1V {td} 10ns 10ns {Ts/2-td} {Ts})
R_S1cntrl 101 0 1
V_S3cntrl 103 0 PULSE(1V 0V 0s 10ns 10ns {Ts/2+td} {Ts})
R_S3cntrl 103 0 1
V_S2cntrl 102 0 PULSE(0V 1V {phi+td} 10ns 10ns {Ts/2-td} {Ts})
R_S2cntrl 102 0 1
V_S4cntrl 104 0 PULSE(1V 0V {phi} 10ns 10ns {Ts/2+td} {Ts})
R_S4cntrl 104 0 1

* Resonant Tank:
Cs 2 4 4510pF
Cp 4 5 4960pF
L 5 6 90uH

* isolation XFMR:
Lpri 4 5 1mH
Lsec bus+ bus- 62.5uH
K_isoxfmr Lpri Lsec 1
Rbus+ bus+ 0 10MEG
Rbus- bus- 0 10MEG

* SRR post-regulators:
X_SRR1 bus+ bus- Vo1 0 SRR
Rload1 Vo1 0 1.25
X_SRR2 bus+ bus- Vo2 0 SRR
Rload2 Vo2 0 1.25
X_SRR3 bus+ bus- Vo3 0 SRR
Rload3 Vo3 0 1.25
X_SRR4 bus+ bus- Vo4 0 SRR
Rload4 Vo4 0 1.25

.SUBCKT SRR +IN -IN Vo Vo_rtn
Lo +IN 1 {Lo}
Co 1 2 0.01uF
Lpri 2 -IN 64mH

```

```

Lsec1 3 Vo_rtn 1mH
Lsec2 Vo_rtn 4 1mH
K Lpri Lsec1 Lsec2 1
D1 3 Vo D_ideal
D2 4 Vo D_ideal
.model D_ideal D(Is=1mA)
Cf Vo Vo_rtn 150uF
.ENDS SRR

.TRAN 1us 100ms 99.9ms 10ns
.FOUR 300kHz 49 V([bus+],[bus-]) I(Lsec)
.OPTIONS RELTOL=0.01 ABSTOL=10uA
.PROBE

.END

```

9.2.3 Square-wave system, maximum load

Square-wave System Simulation (max load)

```
.PARAM Fs=300kHz, Ts={1/Fs}, Td=150ns tt=175ns tblock=-70ns ff=100ns
```

```
V1 boost 1 DC 190V
V2 1 0 DC 190V
```

* Bridge Switches:

```

S1 boost 2 101 0 SW_ideal
D_S1 2 boost D_ideal
C_S1 boost 2 133pF
S2 2 0 102 0 SW_ideal
D_S2 0 2 D_ideal
C_S2 2 0 133pF
.model SW_ideal VSWITCH(Ron=1m)
.model D_ideal D(Is=10uA)

```

* Bridge Switch Control:

```

V_S1cntrl 101 0 PULSE(0V 1V 0s 10ns 10ns {Ts/2-Td} {Ts})
R_S1cntrl 101 0 1
V_S2cntrl 102 0 PULSE(0V 1V {Ts/2} 10ns 10ns {Ts/2-Td} {Ts})
R_S2cntrl 102 0 1

```

* isolation XFMR:

```

Lpri 2 1 878.9uH ;for 15:4 turns ratio as compared to 16:4 for sinewave topology
Lsec bus+ bus- 62.5uH
K_primary_xfmr Lpri Lsec 1
Rbus+ bus+ 0 10MEG
Rbus- bus- 0 10MEG

```

* PWM magamp post-regulators:

```
X_PWM1 bus+ bus- Vo1 0 PWM
```

```

Rload1 Vo1 0 0.25
X_PWM2 bus+ bus- Vo2 0 PWM
Rload2 Vo2 0 0.25
X_PWM3 bus+ bus- Vo3 0 PWM
Rload3 Vo3 0 0.25
X_PWM4 bus+ bus- Vo4 0 PWM
Rload4 Vo4 0 0.25

.SUBCKT PWM +IN -IN Vo Vo_rtn
Rpri +IN +IN_a 10u ;to break inductor loop formed with other post-regs
Lpri +IN_a -IN 64mH
Lsec1 1 Vo_rtn 1mH
Lsec2 Vo_rtn 4 1mH
K Lpri Lsec1 Lsec2 1
SR1 1 2 101 0 ideal_SR
.model ideal_SR VSWITCH(Ron=10u)
V_SR1 101 0 PULSE(0V 1V {tt/2+tblock} 10ns 10ns {Ts-(tt+ff+tblock)}) {Ts})
R_VSR1 101 0 1
D1 2 3 D_ideal
SR2 4 5 102 0 ideal_SR
V_SR2 102 0 PULSE(1V 0V {Ts/2-(tt/2+ff)} 10ns 10ns {tt+ff+tblock-10ns}) {Ts})
R_VSR2 102 0 1
D2 5 3 D_ideal
.model D_ideal D(Is=1mA)
Lf 3 Vo 0.5uH
Cf Vo Vo_rtn 15uF
.ENDS PWM

.TRAN 1us 2ms 1993.333us 10ns
.OPTIONS RELTOL=0.01 ABSTOL=10uA
.PROBE

.END

```

9.2.4 Square-wave system, minimum load

Square-wave System Simulation (min load)

```

.PARAM Fs=300kHz, Ts={1/Fs}, Td=150ns tt=175ns tblock=-23ns ff=100ns

V1 boost 1 DC 190V
V2 1 0 DC 190V

* Bridge Switches:
S1 boost 2 101 0 SW_ideal
D_S1 2 boost D_ideal
C_S1 boost 2 133pF
S2 2 0 102 0 SW_ideal
D_S2 0 2 D_ideal
C_S2 2 0 133pF
.model SW_ideal VSWITCH(Ron=1m)

```

```

.model D_ideal D(Is=10uA)

* Bridge Switch Control:
V_S1cntrl 101 0 PULSE(0V 1V 0s 10ns 10ns {Ts/2-Td} {Ts})
R_S1cntrl 101 0 1
V_S2cntrl 102 0 PULSE(0V 1V {Ts/2} 10ns 10ns {Ts/2-Td} {Ts})
R_S2cntrl 102 0 1

* isolation XFMR:
Lpri 2 1 878.9uH ;for 15:4 turns ratio as compared to 16:4 for sinewave topology
Lsec bus+ bus- 62.5uH
K_primary_xfmr Lpri Lsec 1
Rbus+ bus+ 0 10MEG
Rbus- bus- 0 10MEG

* PWM magamp post-regulators:
X_PWM1 bus+ bus- Vo1 0 PWM
Rload1 Vo1 0 1.25
X_PWM2 bus+ bus- Vo2 0 PWM
Rload2 Vo2 0 1.25
X_PWM3 bus+ bus- Vo3 0 PWM
Rload3 Vo3 0 1.25
X_PWM4 bus+ bus- Vo4 0 PWM
Rload4 Vo4 0 1.25

.SUBCKT PWM +IN -IN Vo Vo_rtn
Rpri +IN +IN_a 10u ;to break inductor loop formed with other post-regs
Lpri +IN_a -IN 64mH
Lsec1 1 Vo_rtn 1mH
Lsec2 Vo_rtn 4 1mH
K Lpri Lsec1 Lsec2 1
SR1 1 2 101 0 ideal_SR
.model ideal_SR VSWITCH(Ron=10u)
V_SR1 101 0 PULSE(0V 1V {tt/2+tblock} 10ns 10ns {Ts-(tt+ff+tblock)} {Ts})
R_VSR1 101 0 1
D1 2 3 D_ideal
SR2 4 5 102 0 ideal_SR
V_SR2 102 0 PULSE(1V 0V {Ts/2-(tt/2+ff)} 10ns 10ns {tt+ff+tblock-10ns} {Ts})
R_VSR2 102 0 1
D2 5 3 D_ideal
.model D_ideal D(Is=1mA)
Lf 3 Vo 0.5uH
Cf Vo Vo_rtn 15uF
.ENDS PWM

.TRAN 1us 2ms 1993.333us 10ns
.OPTIONS RELTOL=0.01 ABSTOL=10uA
.PROBE

.END

```

9.3 Appendix C

9.3.1 PSPICE netlist for parallel-plate bus structure

Shown below is the PSPICE netlist used to generate the FEA results that are compared with the experimental results derived from the test bed. As the bus structure is modified, the component values and network topology of the subcircuit "pplate" is modified according to the FEA results. These networks (with their component values) are shown in Fig. 5.13 and in Sections 9.3.2 and 9.3.3.

```
System Simulation - parallel plate PCB testbed

.PARAM Fs=300KHz, Ts={1/Fs}, Td=700ns

Vin1 boost 1 DC 190V
Vin2 1 boost_rtn DC 190V
Riso boost_rtn 0 10MEG

* Bridge Switches:
X_S1 boost g_S1 2 irfp460
C_S1 boost 2 1fF IC=0V ;470pF
X_S2 2 g_S2 boost_rtn irfp460
C_S2 2 boost_rtn 1fF IC=380V ;470pF

* Bridge Switch Control:
V_S1cntrl 101 2 PULSE(0V 12V 0s 20ns 20ns {Ts/2-Td} {Ts})
Rgate_S1 101 g_S1 10
V_S2cntrl 102 boost_rtn PULSE(0V 12V {Ts/2} 20ns 20ns {Ts/2-Td} {Ts})
Rgate_S2 102 g_S2 10

* isolation XFMR:
R_Cu_pri 2 3 0.03
Lpri 3 1 79uH
Lsec 4 bus- 5.61778uH
R_Cu_sec 4 bus+ 0.01
K_isoXFMR Lpri Lsec 0.999

* Coupled Bus and Logic Networks:
X_Network logic_src logic_src_rtn logic_rcv logic_rcv_rtn bus+ bus- busout+ busout- pplate
Rbus busout- 0 10u

* Bus Loads:
X_postreg1 busout+ busout- Vo1 0 post_reg
RL1 Vo1 0 0.6667
```

```
X_postreg2 busout+ busout- Vo2 0 post_reg
RL2 Vo2 0 0.6667
```

```
* Logic Terminations:
```

```
X_Logic logic_src logic_src_rtn logic_rcv logic_rcv_rtn Logic
Rlogic_src logic_src_rtn 0 10u
Rlogic_rcv logic_rcv_rtn 0 10u
```

```
.TRAN 1us 200us 192us 10ns UIC
.OPTIONS RELTOL=0.01 ABSTOL=1nA
.PROBE
```

```
*****
```

```
.SUBCKT pplate logic_src logic_src_rtn logic_rcv logic_rcv_rtn bus+ bus- busout+ busout-
```

```
* bus:
```

```
R11 bus+ 1000 0.00278
L11 1000 busout+ 0.255uH
R22 bus- 2000 0.00278
L22 2000 busout- 0.255uH
C12 busout+ busout- 700pF ;2603pF
```

```
* logic:
```

```
R33 logic_src 3000 0.551
L33 3000 logic_rcv 0.318uH
R44 logic_src_rtn 4000 0.552
L44 4000 logic_rcv_rtn 0.320uH
C34 logic_rcv logic_rcv_rtn 0.454pF
```

```
* Cross Capacitance:
```

```
C13 busout+ logic_rcv 17.8pF ;30.4pF
C14 busout+ logic_rcv_rtn 17.8pF ;30.4pF
```

```
* Mutual Inductance:
```

```
K12 L11 L22 0.99825
K13 L11 L33 0.89429
K14 L11 L44 0.8906
K23 L22 L33 0.89262
K24 L22 L44 0.88893
K34 L33 L44 0.80795
```

```
.ENDS pplate
```

```
*****
```

```
.SUBCKT Logic src src_rtn rcv rcv_rtn
```

```
Vcc Vcc src_rtn DC 2V
Rds_on Vcc src 85
Dposclamp rcv Vcc int_diode
Resd rcv CMOS 90
Dnegclamp1 rcv_rtn rcv int_diode
Dnegclamp2 rcv CMOS int_diode
.model int_diode D(Is=1fA Cjo=0.01pF Rs=0.01)
R_cmos CMOS rcv_rtn 300MEG
```

C_cmos CMOS rcv_rtn 15pF

.ENDS Logic

.SUBCKT post_reg IN+ IN- Vo Vo_rtn

R_Loop IN+ IN+_a 10u ;breaks inductor loop formed with other post-reg

Lpri IN+_a IN- 500uH

Lsec1 1 Vo_rtn 7.8125uH

Lsec2 Vo_rtn 4 7.8125uH

K_XFMR Lpri Lsec1 Lsec2 0.997 ;models XFMR leakage

SR1 1 2 101 0 magamp

D1 2 3 Dschottky

SR2 4 5 102 0 magamp

D2 5 3 Dschottky

DFW Vo_rtn 3 Dschottky

Lf 3 Vo 6uH IC=7.5A

Cf Vo Vo_rtn 10uF IC=5V

V_SR1cntrl 101 0 PULSE(1V 0V 2.62us 20ns 20ns 490ns 3.3333us)

R_SR1cntrl 101 0 1

V_SR2cntrl 102 0 PULSE(1V 0V 900ns 20ns 20ns 520ns 3.3333us)

R_SR2cntrl 102 0 1

.model magamp vswitch(ron=1m)

.model Dschottky D(Is=200uA Rs=1.4m Cjo=300pF)

.ENDS post_reg

.SUBCKT irfp460 1 2 3

* Model format: SPICE3

* External Node Designations

* Node 1 -> Drain

* Node 2 -> Gate

* Node 3 -> Source

M1 9 7 8 8 MM L=100u W=100u

* Default values used in MM:

* The voltage-dependent capacitances are

* not included. Other default values are:

* RS=0 RD=0 LD=0 CBD=0 CBS=0 CGBO=0

.MODEL MM NMOS LEVEL=1 IS=1e-32

+VTO=3.854 LAMBDA=0.0101851 KP=29.2045

+CGSO=4.20555e-05 CGDO=1e-11

RS 8 3 0.0282736

D1 3 1 MD

.MODEL MD D IS=1e-17 RS=0.00908038 N=0.70113 BV=500

+IBV=0.00025 EG=1.00085 XTI=1.00002 TT=0

+CJO=6.16104e-09 VJ=1.30742 M=0.9 FC=0.5

RDS 3 1 2e+07

RD 9 1 0.244129

RG 2 7 2.96914

D2 4 5 MD1

* Default values used in MD1:


```

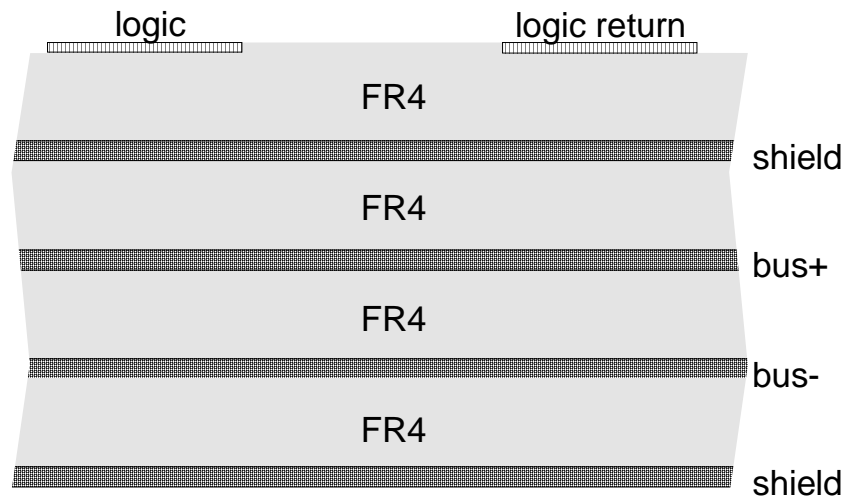
* RS=0 EG=1.11 XTI=3.0 TT=0
* BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=2750pF VJ=1.83303 M=0.9 FC=1e-08 ;CJO=5e-09
D3 0 5 MD2
* Default values used in MD2:
* EG=1.11 XTI=3.0 TT=0 CJO=0
* BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=1 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 5e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
* EG=1.11 XTI=3.0 TT=0 CJO=0
* RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=1
.ENDS
*****

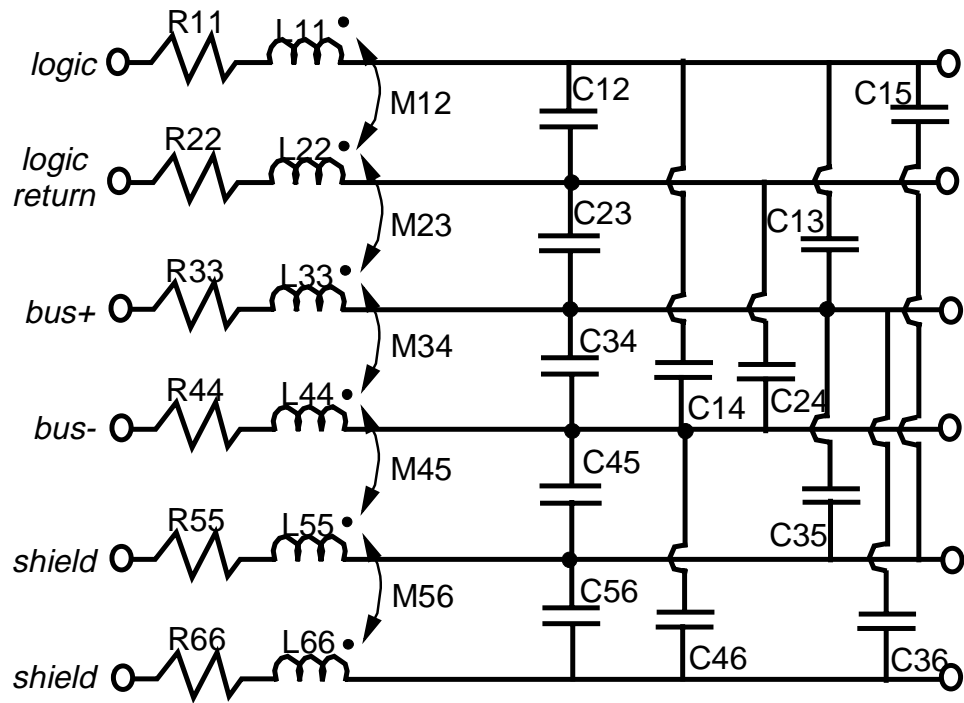
.END

```

9.3.2 Parallel-plate with shield layers

FEA results for this bus structure are shown below.





$$L_{ij} = \begin{bmatrix} 1.448 & 1.304 & 1.248 & 1.245 & 1.25 & 1.243 \\ & 1.441 & 1.248 & 1.245 & 1.25 & 1.243 \\ & & 1.251 & 1.249 & 1.249 & 1.247 \\ & & & 1.251 & 1.247 & 1.249 \\ & & & & 1.251 & 1.245 \\ & & & & & 1.251 \end{bmatrix} \mu\text{H}/\text{m}$$

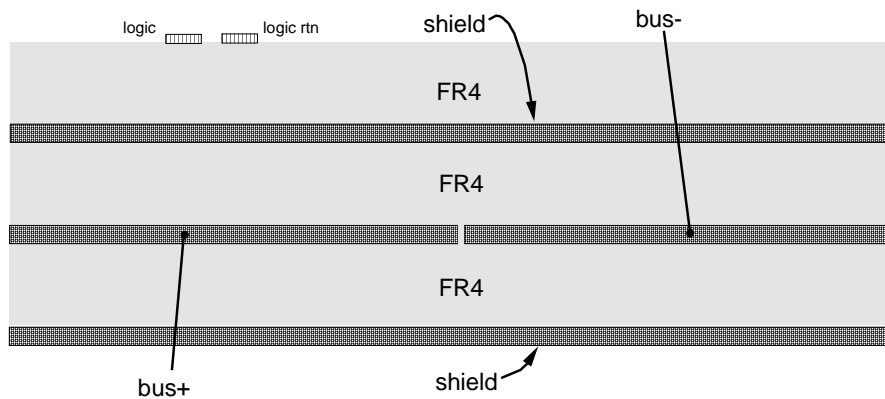
$$k_{ij} = \begin{bmatrix} 1 & 0.9026 & 0.9269 & 0.9252 & 0.9287 & 0.9235 \\ & 1 & 0.9291 & 0.9273 & 0.9308 & 0.9256 \\ & & 1 & 0.9983 & 0.9983 & 0.9964 \\ & & & 1 & 0.9964 & 0.9983 \\ & & & & 1 & 0.9946 \\ & & & & & 1 \end{bmatrix}$$

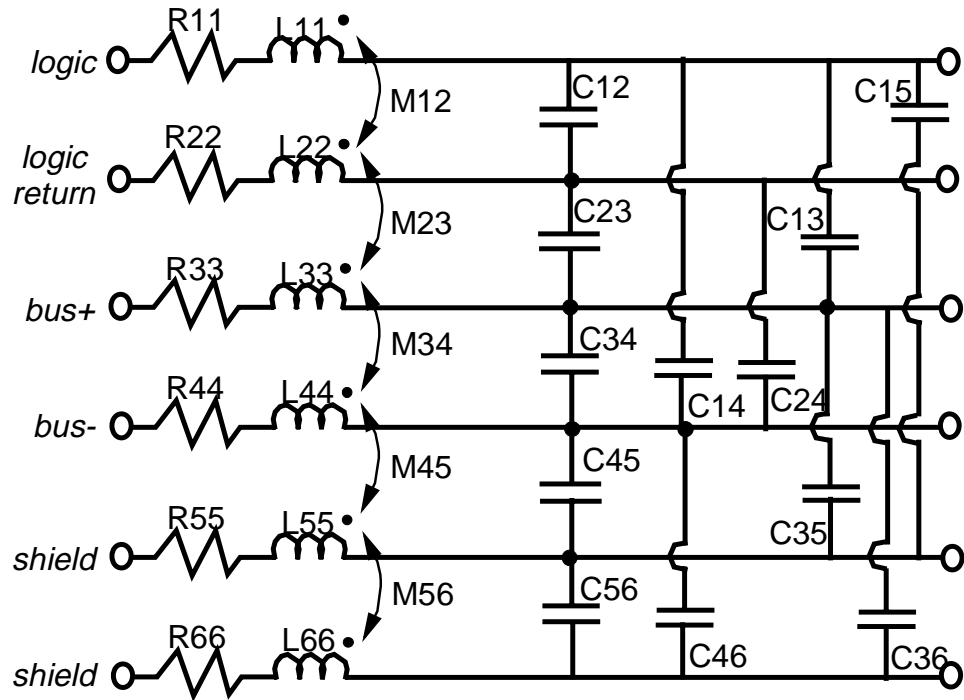
$$C_{ij} = \begin{bmatrix} 366.9 & -97.8 & -0.00113 & -0.00113 & -269 & -0.117 \\ & 365.4 & -0.0011 & -0.0011 & -267.5 & -0.114 \\ & & 26532 & -13266 & -13266 & -0.153 \\ & & & 26532 & -0.149 & -13266 \\ & & & & 13815 & -12.47 \\ & & & & & 13279 \end{bmatrix} \text{ pF/m}$$

$$R_{ij} = \begin{bmatrix} 2.65 & & & & & \\ & 2.647 & & & & \\ & & 0.01277 & & & \\ & & & 0.01277 & & \\ & & & & 0.01273 & \\ & & & & & 0.01273 \end{bmatrix} \Omega/m$$

9.3.3 Single-layer with shield

FEA results for this bus structure are shown below.





$$L_{ij} = \begin{bmatrix} 1.59 & 1.273 & 1.249 & 1.249 & 1.252 & 1.247 \\ & 1.573 & 1.249 & 1.249 & 1.252 & 1.247 \\ & & 1.255 & 1.251 & 1.251 & 1.251 \\ & & & 1.255 & 1.251 & 1.251 \\ & & & & 1.253 & 1.249 \\ & & & & & 1.253 \end{bmatrix} \mu\text{H}/\text{m}$$

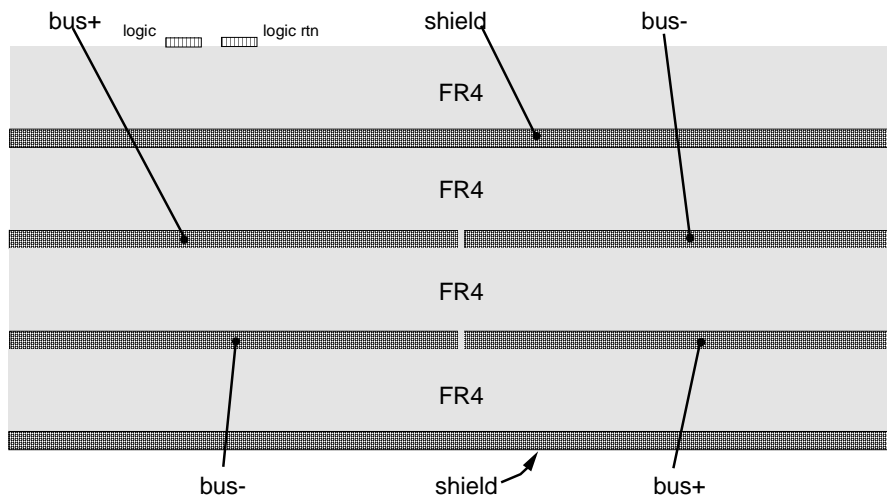
$$k_{ij} = \begin{bmatrix} 1 & 0.8048 & 0.8842 & 0.8843 & 0.8867 & 0.8834 \\ & 1 & 0.8890 & 0.8891 & 0.8915 & 0.8882 \\ & & 1 & 0.9965 & 0.9974 & 0.9974 \\ & & & 1 & 0.9974 & 0.9974 \\ & & & & 1 & 0.9964 \\ & & & & & 1 \end{bmatrix}$$

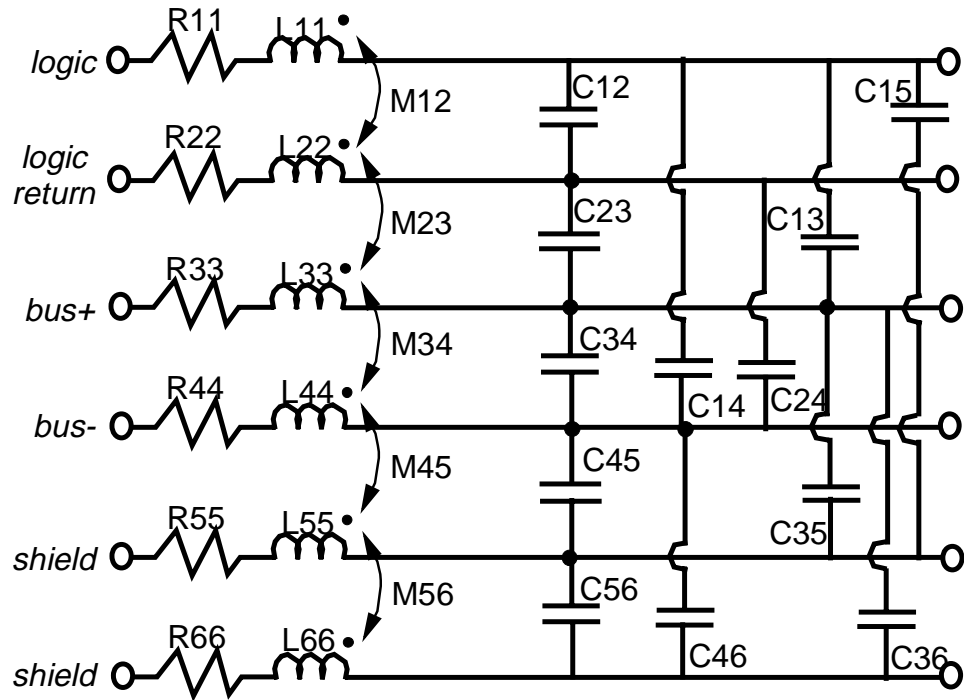
$$C_{ij} = \begin{bmatrix} 367.2 & -98 & -0.00067 & -0.00046 & -269.1 & -0.117 \\ & 365.7 & -0.00065 & -0.00047 & -267.6 & -0.115 \\ & & 13188 & -0.825 & -6593.8 & -6593.8 \\ & & & 13188 & -6593.8 & -6593.8 \\ & & & & 13771 & -46.32 \\ & & & & & 13234 \end{bmatrix} \text{pF}/m$$

$$R_{ij} = \begin{bmatrix} 2.71 & & & & & \\ & 2.70 & & & & \\ & & 0.0278 & & & \\ & & & 0.0278 & & \\ & & & & 0.0130 & \\ & & & & & 0.0130 \end{bmatrix} \Omega/m$$

9.3.4 Two layer w/shield, 4 conductor structure

FEA results for this bus structure are shown below.





$$L_{ij} = \begin{bmatrix} 1.573 & 1.275 & 1.249 & 1.248 & 1.251 & 1.245 \\ & 1.572 & 1.248 & 1.248 & 1.251 & 1.245 \\ & & 1.252 & 1.251 & 1.249 & 1.249 \\ & & & 1.252 & 1.249 & 1.249 \\ & & & & 1.253 & 1.246 \\ & & & & & 1.253 \end{bmatrix} \mu\text{H}/\text{m}$$

$$k_{ij} = \begin{bmatrix} 1 & 0.8889 & 0.8895 & 0.8843 & 0.8815 & 0.8869 \\ & 1 & 0.8897 & 0.8892 & 0.8918 & 0.8871 \\ & & 1 & 0.9986 & 0.9975 & 0.9975 \\ & & & 1 & 0.9975 & 0.9975 \\ & & & & 1 & 0.9949 \\ & & & & & 1 \end{bmatrix}$$

$$C_{ij} = \begin{bmatrix} 366.9 & -97.8 & -0.00113 & -0.00113 & -269 & -0.117 \\ & 365.4 & -0.00111 & -0.00111 & -267.5 & -0.114 \\ & & 26370 & -13163 & -6603.4 & -6603.4 \\ & & & 26370 & -6603.4 & -6603.4 \\ & & & & 13767 & -23.25 \\ & & & & & 13230 \end{bmatrix} \text{pF}/m$$

$$R_{ij} = \begin{bmatrix} 2.70 & & & & & \\ & 2.71 & & & & \\ & & 0.0132 & & & \\ & & & 0.0132 & & \\ & & & & 0.0136 & \\ & & & & & 0.0136 \end{bmatrix} \Omega/m$$

Vita

Bob Watson was born in Indianapolis, Indiana, around the time of the second Eisenhower administration. He received the B.S. degree from Purdue University in 1982, and the M.S. degree from the University of Arizona in 1986, both in electrical engineering. He has thirteen years of industrial experience, first with Hughes Aircraft and later with Allied-Signal Corporation and Virginia Power Technologies (now know simply as “VPT”). He became a member of the Virginia Power Electronics Center in 1992, first as a graduate research assistant and was later promoted to research associate. Following his successful completion of the Ph.D. degree requirements, he will be employed with Thomson Consumer Electronics in Indianapolis, Indiana, where he will finally learn how to fix a TV.