1. INTRODUCTION

This dissertation presents new power conversion architectures that can significantly improve the cost, reliability, and efficiency of state-of-the art electronic equipment. These architectures include:

1) New power conversion techniques that substantially simplify the design of power-factor correction front-end converters in DC distributed power systems, and
2) new high-frequency AC power distribution techniques that significantly simplify the entire distributed power system.

1.1 Background and Motivation

Power conversion systems are becoming an increasingly costly component in the design of state-of-the-art electronic equipment. For information technology equipment (i.e., computer systems), the evolution of digital logic technology continues to impose decreasing supply voltage requirements with increasing supply current needs. This trend is especially evident in the area of microprocessor and computer memory design [1, 2]. Further complicating power conversion system design issues are present and emerging requirements for the management of computing system power consumption through microprocessor control [3]. System power management allows for manipulation of the computing system energy consumption as a function of the system activity level. However, transitions from minimum to maximum power levels are of large magnitude

and very short duration [4, 5, 6, 7, 8], severely impacting the design of the power supply system.

As this evolutionary process in digital logic and computer systems technology continues, the typical power system "architecture" used in present-day computers (Fig. 1.1) is becoming less capable of meeting performance goals. The most apparent example of this is the issue of maintaining tight transient point-of-load (POL) voltage regulation for the system microprocessor(s). Stand-alone "silver box" designs are unable to meet transient voltage regulation requirements, so post-regulators (known as voltage regulator modules or "VRMs") are being developed. The power processing *combination* of the silver box and VRM is used to meet a microprocessor's stringent power quality requirement [6]. However, VRM performance (e.g., efficiency and transient response) is constrained to the limitations imposed by the silver box outputs. This is illustrated by considering a VRM design based on an input voltage of 48 Vdc instead of the more usual 5 Vdc (or possibly 12 Vdc). With a 48 Vdc input, VRM efficiency can be improved by as much as 3 % [9]. Not only is the VRM efficiency improved, there is an accompanying decreased I^2R loss in distributing power to the VRM from the silver box.

Also, a power processing structure where there are several conversion steps in "series" tends to lead to an inefficient overall power system design. As shown in Fig. 1.1 three to four conversion steps are required to process power from the AC line to the loads. A target area for reducing the power system cost is to eliminate and/or simplify as many conversion steps as possible. This is especially true in light of the more stringent power system performance objectives that lie in future computer system designs [3, 7].

An additional drawback to the power system architecture shown in Fig. 1.1 is its inflexibility. A particularly important issue for high-availability/fault-tolerant computing systems (e.g., workstations and servers), this inflexibility manifests itself in two ways [10, 11, 12, 13, 14]:

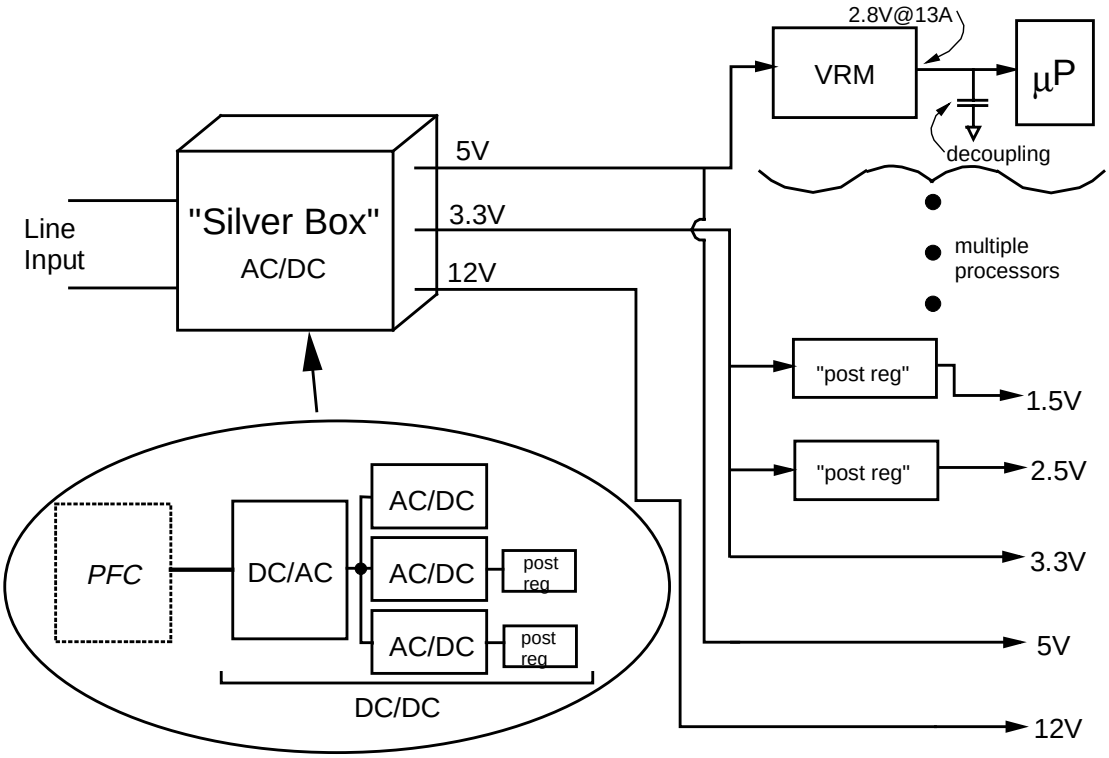


Fig. 1.1 Typical present-day PC/workstation/server power supply architecture.

1) As system power level requirements increase, the distribution of multiple low-output voltages becomes less practical. Silver box efficiency suffers and the resolution of low-voltage/high-current distribution issues consumes a greater percentage of the overall power system cost target. Also, as a direct result of the low distribution voltage levels, post-regulators are typically not isolated. This may reduce costs, but leads to potential difficulties with ground loops, load-fault isolation, and system noise levels. Switched-mode post regulators (such as the VRMs) require large input filters because of the high input currents they switch.

2) Providing a power backup function from the output side of the silver box in the power system shown in Fig. 1.1 is complicated, primarily because there is no common output "bus." Each output would have to be serviced from an individual backup circuit. Utilization of an uninterruptible power supply (UPS) is a possible solution, but a failure in the silver box still brings the entire power system down. A fault-tolerant system design would resolve this issue, but requires a redundant silver box. This implies individual pairs of each of the silver box outputs would need to be configured for parallel operation.

Solutions to these problems can be realized by simplifying the silver box design, as shown in Fig. 1.2. In this power system architecture, the silver box is reduced to a single output "front-end" converter and the post regulators evolve to "DC/DC" converters. The distribution bus voltage is typically 48 Vdc, but other values are used as well [14]. This silver box design simplification typically requires that *all* system loads now be fed directly from DC/DC converters. Therefore, Fig. 1.2's power system architecture will have an increased DC/DC converter component count. However, the issues raised at the end of the previous section regarding the inflexibility of Fig. 1.1's power system architecture are more easily resolved.

Although the front-end design is now simplified, the power architecture shown in Fig. 1.2 still requires three conversion steps to process power from the AC line to the system

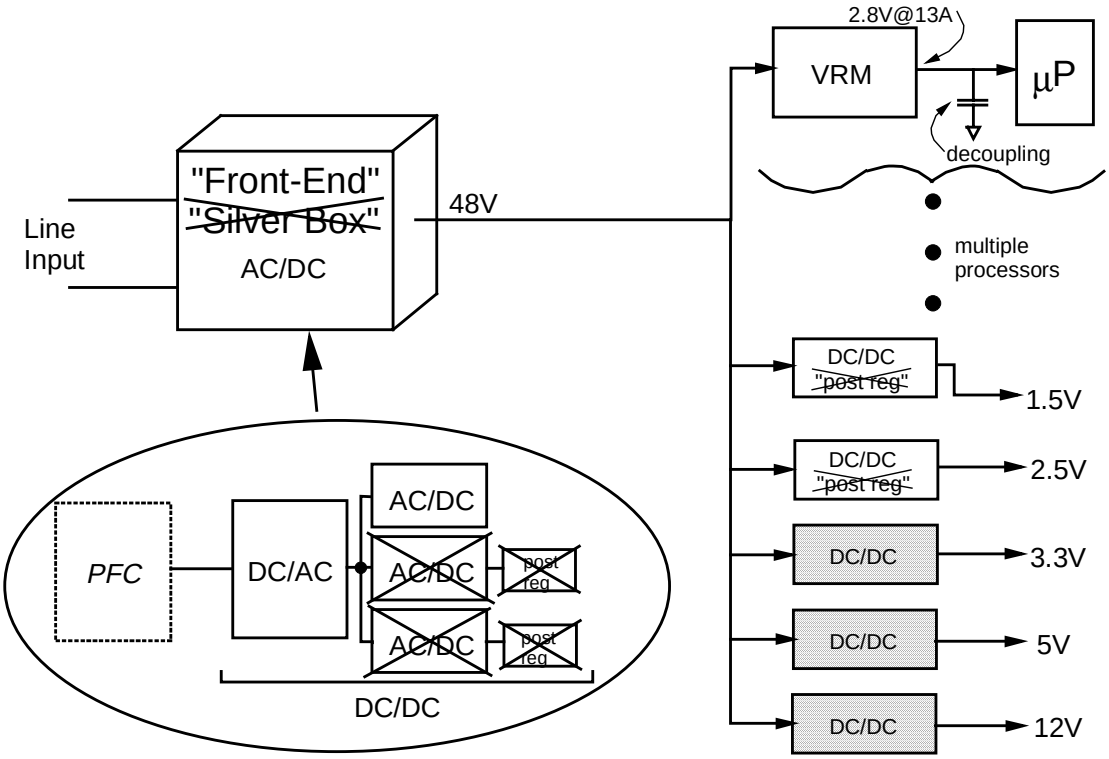


Fig. 1.2 PC/workstation/server power supply architecture with a simplified silver box design.

loads. Two of these conversion steps reside within the front-end converter. Therefore, it becomes a natural target for further simplification [15, 16, 17, 18, 19, 20] and is the subject of Part I of this dissertation.

The complexity of the DC distributed power system (DPS) shown in Fig. 1.2 can also be further reduced as shown in Fig. 1.3. As illustrated in Fig. 1.3, the elimination of inverter and rectifier functions allows for one conversion step to be eliminated. As a result, the "DC" method of power distribution changes over to an "AC" power distribution technique. The AC DPS eliminates the rectification/filtering step performed at the output of the front-end DC/DC converter and the inversion step performed at the input of *every* DC/DC post-regulator present in the system. An AC DPS has a lower parts count and higher efficiency.

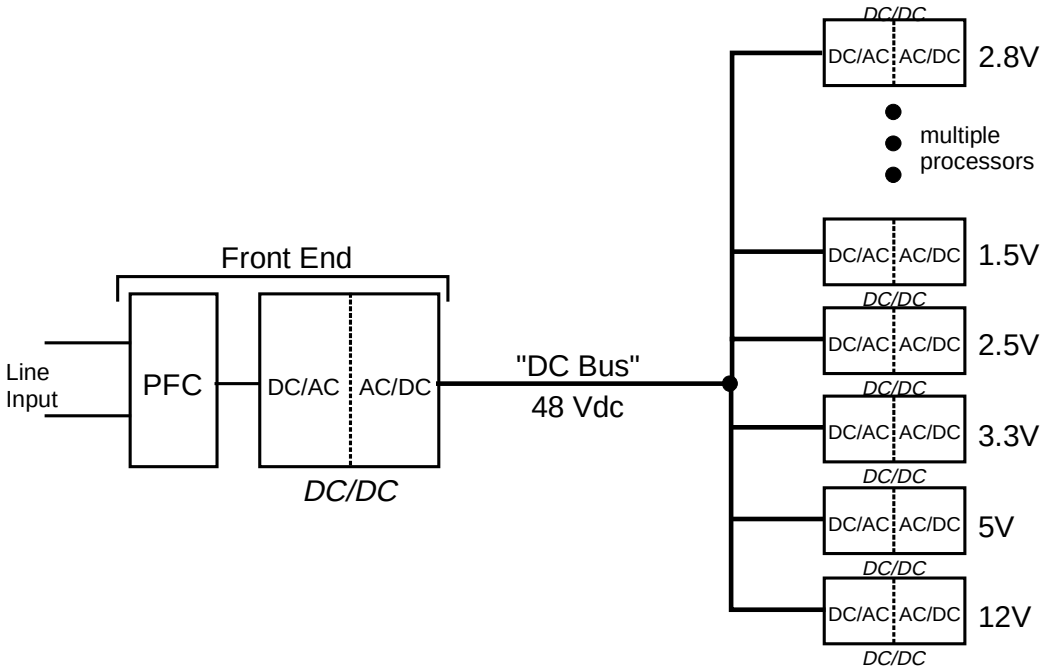
However, there are three major technical challenges confronting the deployment of an AC DPS:

1) *Power system layout, particularly with respect to electromagnetic interference (EMI) and noise induced into the host computing system* -

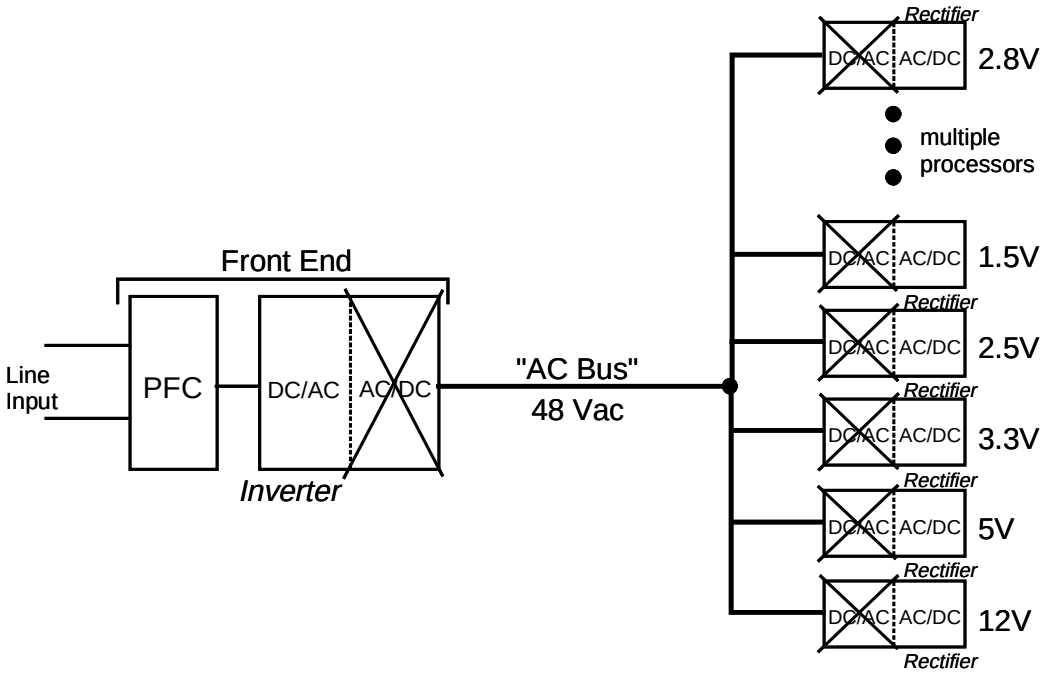
   The ramifications of distributing high voltage, high-frequency waveforms throughout a host computing system need to be determined.

2) *The choice of bus voltage and current waveshapes and their impact on the design and performance of the front-end and post-regulator converters* -

   There are two "extremes" of bus waveform shapes available for consideration - sinewave type and square-wave type. Sinewave type bus voltage *and* current waveforms will realize minimum harmonic distortion. This would seem to be an important consideration with respect to the EMI generated by this power system architecture. However, the potential burden placed on the design of converter topologies required to generate and process high-frequency (HF) sine wave voltages and currents has to be considered. Research has been reported in the literature regarding sinewave type AC bus systems as applied to investigations into power



a) DC DPS.



b) AC DPS.

Fig. 1.3 Conceptualization of the derivation of an AC distributed power systems.

system architectures for the international space station [21, 22, 23, 24, 25, 26]. But the results of this research has limited applicability to the computing system power architectures being considered here. The bus distribution dimensions for the space station are on the order of 100 meters with power levels of tens of kilowatts. This can be contrasted with the requirements of workstations and low to mid-range servers where bus dimensions would be on the order of one-third of a meter with power levels below one kilowatt [27]. Also, reactive energy issues that accompany resonant type converter topologies need to be effectively dealt with in a power system environment where there are very fast and large load changes. At the other extreme, the use of square-wave type bus waveforms imply that EMI issues can be effectively dealt with and the advantages of conventional pulse-width-modulation (PWM) techniques can be utilized [28, 29].

3) *Point-of-load post-regulator design* -

Consideration of POL regulation exposes the third unique issue with respect to AC DPSs - how are the AC DPS post-regulators designed to provide good point-of-load regulation, dynamic behavior, and efficiency?

1.2 Dissertation Outline and Major Results

This dissertation is organized into two general sections. Part I consists of Chapters 2, 3, and 4 and investigates simplifications and performance improvements in two-stage PFC/DC-DC front-end designs for DC distributed power systems (see Fig. 1.4):

Chapter 2 simplifies the two stage front-end design by presenting the analysis, design, and experimental results for an improved zero-voltage-switched (ZVS) full-bridge DC/DC converter. This converter's ZVS characteristic is extended to a wide load range by utilization of the isolation transformer's magnetizing inductance as an energy storage element. It is demonstrated how controlled switching on the converter's secondary accomplishes this task. Integration of the control of these switches for ZVS with control

of the switches to maintain DC bus voltage regulation is then described. This integration of functions has the benefit of simplifying the methods used for maintaining control and isolation of the DC bus. The converter's primary is switched in a very simple manner with constant duty cycle. Experimental results are provided for a 1 kW breadboard.

Chapter 3 discusses altogether eliminating the 2nd stage DC/DC converter in the two-stage front-end implementation. This forces transformer isolation to be incorporated into the PFC converter. The task of accomplishing precise and fast output voltage regulation is then placed on the post-regulators. In Chapter 3 the design of the PFC conversion stage is investigated through the utilization of a soft-switched active-clamp flyback topology. The behavior of the ZVS active-clamp flyback operating with unidirectional magnetizing current is analyzed and design equations based on this analysis are presented. Experimental results are then given for a 500 W prototype circuit, illustrating the soft-switching characteristics and improved efficiency of the converter. The design is then extended to 500 W single and 600 W interleaved active-clamp flybacks to be used in computing systems requiring PFC from a universal AC line input (90 Vac - 264 Vac). Several practical design issues, including the application of charge control, the use of mixed-technology power devices to increase the topology's power processing capability, and a solution to the hold-up time problem are discussed and experimentally verified.

Chapter 4 discusses front-end designs consisting of isolated PFC topologies, but for computing systems requiring higher power levels, such as higher-end servers [30]. A new full-bridge, active-clamp boost converter for single-phase high power PFC applications is detailed. It is shown how the active-clamp network serves to limit bridge switch turn-off voltage overshoot and enable the energy stored in the isolation transformer leakage inductance to be used for zero-voltage switching. Phase-shift control of the bridge switches is utilized to obtain zero-current switching (ZCS) for two of the four bridge switches. Analysis, design, and experimental results are presented for a 1 kW universal line input to 48 Vdc output are presented, verifying the principle of operation.

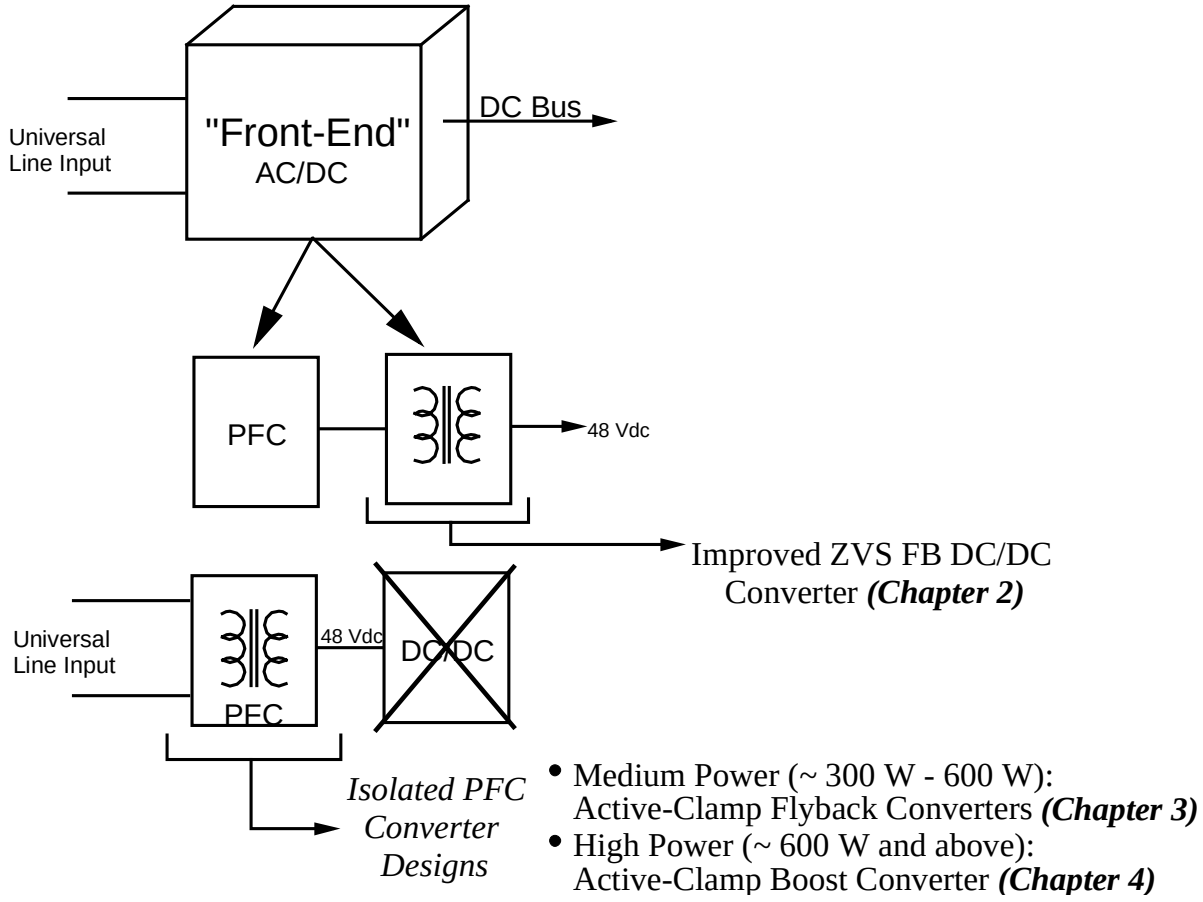


Fig. 1.4 Part I functional description.

A 3 % efficiency improvement over a two-stage front-end design is experimentally demonstrated.

Part II consists of Chapters 5 and 6 and details investigations into computer power system architecture simplification through the implementation of the AC DPS concept:

Chapter 5 details investigations into the AC DPS technical issues that were raised in Section 1.1. After the scope and specifications of the problem are outlined, two example AC DPS designs are detailed and compared. The results of this comparison clearly indicate the decreased system cost and complexity in utilizing square-wave bus waveforms. Theoretical and experimental data for a 300 kHz square-wave AC DPS are then provided. Solutions to the problems of induced noise ("crosstalk") and radiated noise are developed through a combination of unique printed circuit board (PCB) bus structure designs coupled with the use of noise cancellation techniques. It is demonstrated how the application of finite element analysis (FEA) methods to various bus structures results in excellent agreement between theory and experiment.

Utilizing the results of Chapter 5, Chapter 6 concentrates on an experimental comparison between identically configured DC and AC distributed power systems. The points of comparison are efficiency, radiated noise, complexity, and finally, cost. An AC DPS efficiency improvement of between 5 % and 8 % is demonstrated. Results with respect to radiated noise are presented and discussed. A crude piece-parts cost analysis indicates a cost savings of about 20 % for the AC DPS front-end design over its DC DPS counterpart, along with a corresponding 15 % per post-regulator cost savings.

Chapter 7 summarizes the major results of this work and contains suggestions for future investigations into the AC DPS concept.