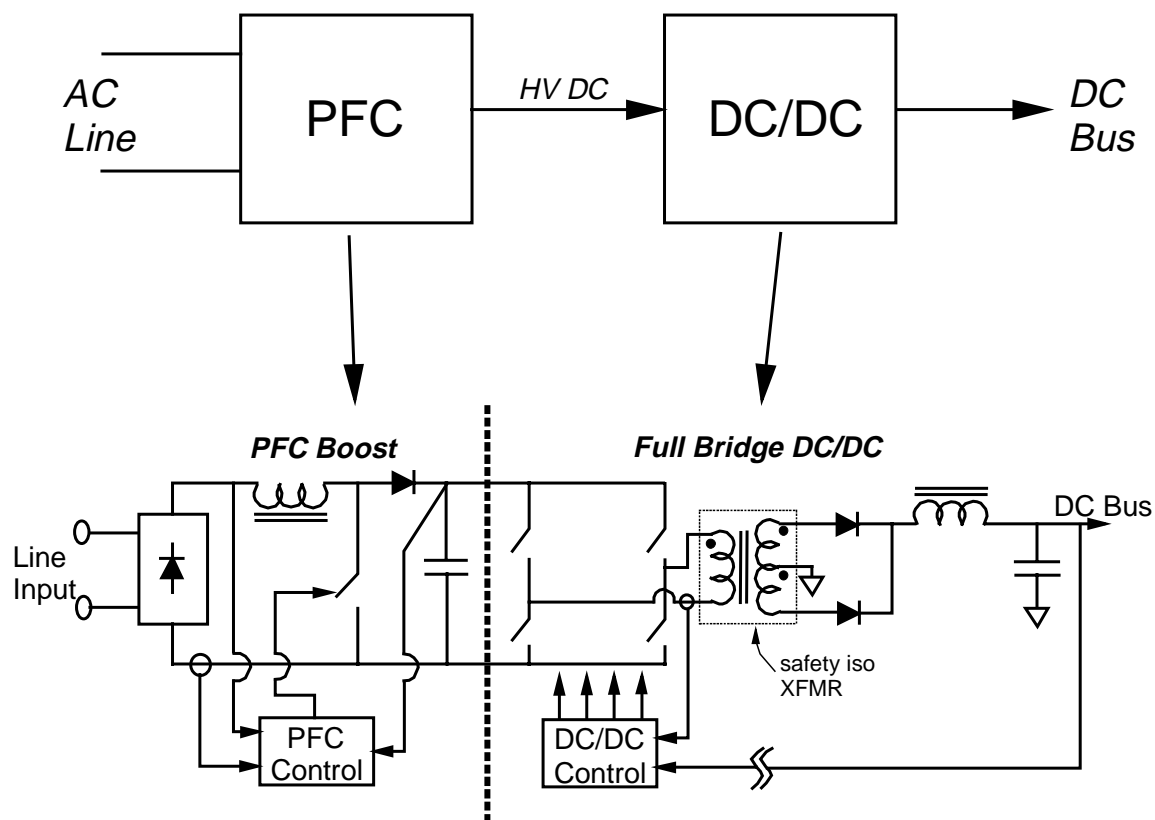


2. AN IMPROVED ZVS FULL-BRIDGE DC/DC CONVERTER

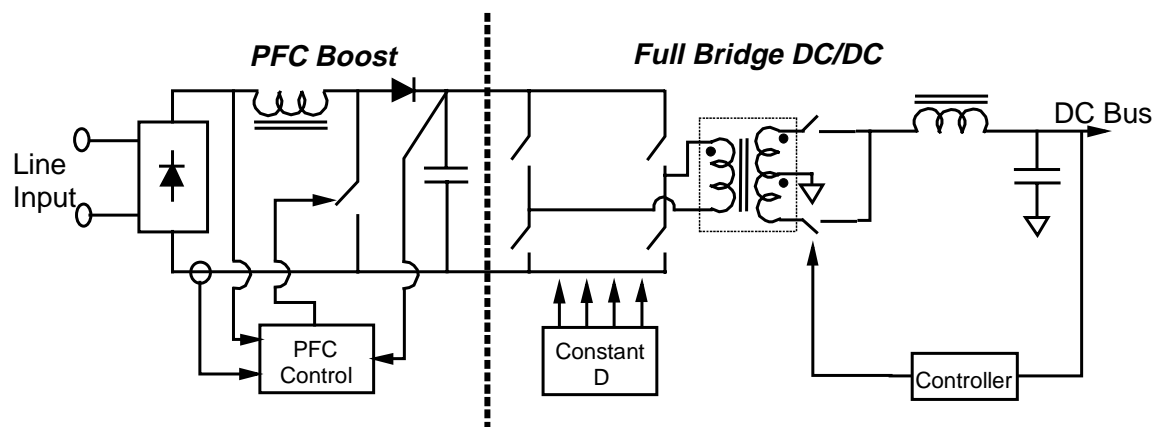
2.1 Introduction

Shown in Fig. 2.1(a) is the basic structure of a typical two-stage front-end converter for DC distributed power systems, often used in systems requiring power factor correction (PFC) and power levels above about 500 - 600 W. For universal AC input line applications, the intermediate voltage between the two stages is approximately 380 Vdc. Typically, the peak total change in this voltage due to variations in line, load, and the effects of the 120 Hz ripple current is within $\pm 5\%$. The closed-loop control of the DC/DC converter, conceptually shown in Fig. 2.1(a), prevents this voltage variation, along with the variations due to the losses in the DC/DC converter itself, from appearing on the output DC bus.

While the control "structure" for the PFC boost converter is necessitated by the need for power factor correction, the control concept utilized by the full-bridge DC/DC converter requires passing the output voltage control signal across the isolation boundary and then providing the necessary logic functions to pulse-width-modulate the four bridge switches based on this control signal. A much simpler method, at least conceptually, is to accomplish the necessary closed-loop regulation of the bus voltage entirely on the secondary, as shown in Fig. 2.1(b). Here secondary-side switches modulate the volt-seconds to the output inductor, thereby maintaining bus regulation without crossing the



(a) Traditional two-stage concept.



(b) Two-stage design with simplified secondary-side DC/DC control.

Fig. 2.1 Two-stage DC DPS front-end design.

isolation barrier. The bridge switches on the primary can now be switched with a constant duty cycle, greatly simplifying the overall control scheme.

Constant-frequency, phase-shifted operation of the primary side switches provides a convenient method for achieving zero-voltage turn-on of the switches, significantly reducing switching losses. Traditional methods utilized to achieve zero-voltage-switching in full-bridge, constant-frequency PWM converters typically rely upon either the energy stored in the isolation transformer leakage inductance and/or the inclusion of a resonant inductor in series with the transformer to act as a supplemental energy storage element. This stored energy is used to charge and discharge bridge switch capacitance during a freewheeling stage created by phase shifting the "on" times of opposite pairs of transistors in the bridge configuration. Assuming sufficient energy storage, the body diode of the switch is forced into conduction before that particular device is turned on, enabling loss-less switching. A drawback to this approach is the dependency of the zero-voltage-switching (ZVS) characteristic on load current. As the required output power decreases, ZVS is lost because not enough energy is stored in the resonant inductor to complete a charge/discharge cycle before device switching occurs. Also, this (relatively) large inductance resonates with the secondary-side rectifier junction capacitance, necessitating the addition of dissipative snubbers or active-clamp circuits to reduce the ringing to manageable levels [31].

A possible way of minimizing the ZVS load dependency is to utilize the energy stored in the isolation transformer magnetizing inductance, which is independent of the load current. However, normally, the magnetizing current becomes available to the bridge switches only when the reflected load current has decreased to the point where it is less than the magnetizing current. The difference is then available to charge and discharge the switch capacitances and enable ZVS. This difference may or may not be large enough to achieve ZVS. By gapping the transformer the useful ZVS range can be increased at light load at the expense of increasing the circulating energy in the converter [32, 33].

A more load independent situation for ZVS can be created by incorporating some form of switching action in the converter secondary [34, 35, 36]. In this scenario, secondary switches are used to prevent the magnetizing current from exiting the primary through the secondary. Consequently, all the magnetizing energy is available for capacitor charge and discharge. No external energy storage element is necessary and ZVS is obtained through the use of a minimum amount of circulating energy. In addition to achieving a more load independent ZVS characteristic, the use of controlled switching in the secondary simplifies the overall control structure of the DC/DC converter.

This chapter describes the analysis, design, and experimental evaluation of an improved 100 kHz, 1 kW, full-bridge, ZVS PWM converter employing secondary-side magamp control. The magamps fill the role of the secondary-side switches, simultaneously integrating the functions of output voltage regulation and utilization of the isolation transformer's magnetizing energy as a source to extend the FB switch ZVS range. As a result of regulation on the secondary, the primary is switched in a very simple constant-frequency, constant phase-shifted (i.e., constant duty cycle) fashion. Also, parasitic ringing between the transformer's leakage inductance and parasitic rectifier capacitance, apparent in previous designs [31, 32, 34], is eliminated without incorporating any additional components.

It should also be noted that the methods to be developed here that realize soft-switching of the FB switches will be applied to the high-frequency AC distributed power system half-bridge (HB) inverter/post-regulator topology examined in Chapter 5. As is discussed in that chapter, one of the chief advantages to soft-switching (using magnetizing energy) of the HB inverter switches is the "controlled" bus voltage slew rates that result.

2.2 Theory of Operation

The basic operation of pulse-width-modulated, (PWM) phase-shifted, full-bridge converter employing secondary-side switching is illustrated in Fig. 2.2. The switches on the same leg of the bridge are (ideally) switched with a 50 % duty cycle and are 180° out of phase. The switching time for one leg is then phase-shifted relative to the other. In the absence of the secondary-side switches, S5 and S6 (i.e., they are replaced with rectifiers), controlling the bridge phase shift (ϕ) varies the volt-seconds applied to the output inductor and hence the resulting DC output voltage, V_o . However, by incorporating S5 and S6 and modulating their turn-on time relative to the bridge switching cycle (θ , the shaded regions shown in Fig. 2.2), the volts-seconds applied to the output inductor can also be varied to maintain output voltage regulation. In this case the bridge can be switched with constant phase shift (duty cycle) and the output voltage regulation be accomplished completely on the secondary. The range of regulation is determined by the input voltage, transformer turns ratio, and output voltage. Since the secondary-side switches can only remove volt-seconds from the output inductor, for a given turns ratio and desired output voltage the minimum input voltage is then determined. Similarly, the maximum input voltage is limited by the maximum volt-seconds S5 and S6 can block (all else being equal).

Switches S5 and S6 also enable the isolation transformer's magnetizing inductance to extend the useful range for ZVS of the bridge switches. To illustrate this, Figure 2.3 shows a simplified schematic of a full bridge ZVS topology incorporating secondary switching (S5 and S6). The isolation transformer is shown with its leakage and magnetizing inductances reflected to the primary. For the purposes of simplifying the explanation of converter operation, the output filter inductor is assumed large enough so that it can be replaced by a current source equal in value to the load current. Because of the presence of switches S5 and S6, catch diode DFW is used to maintain a circulating path for the output inductor current on the secondary. For high-duty cycle designs

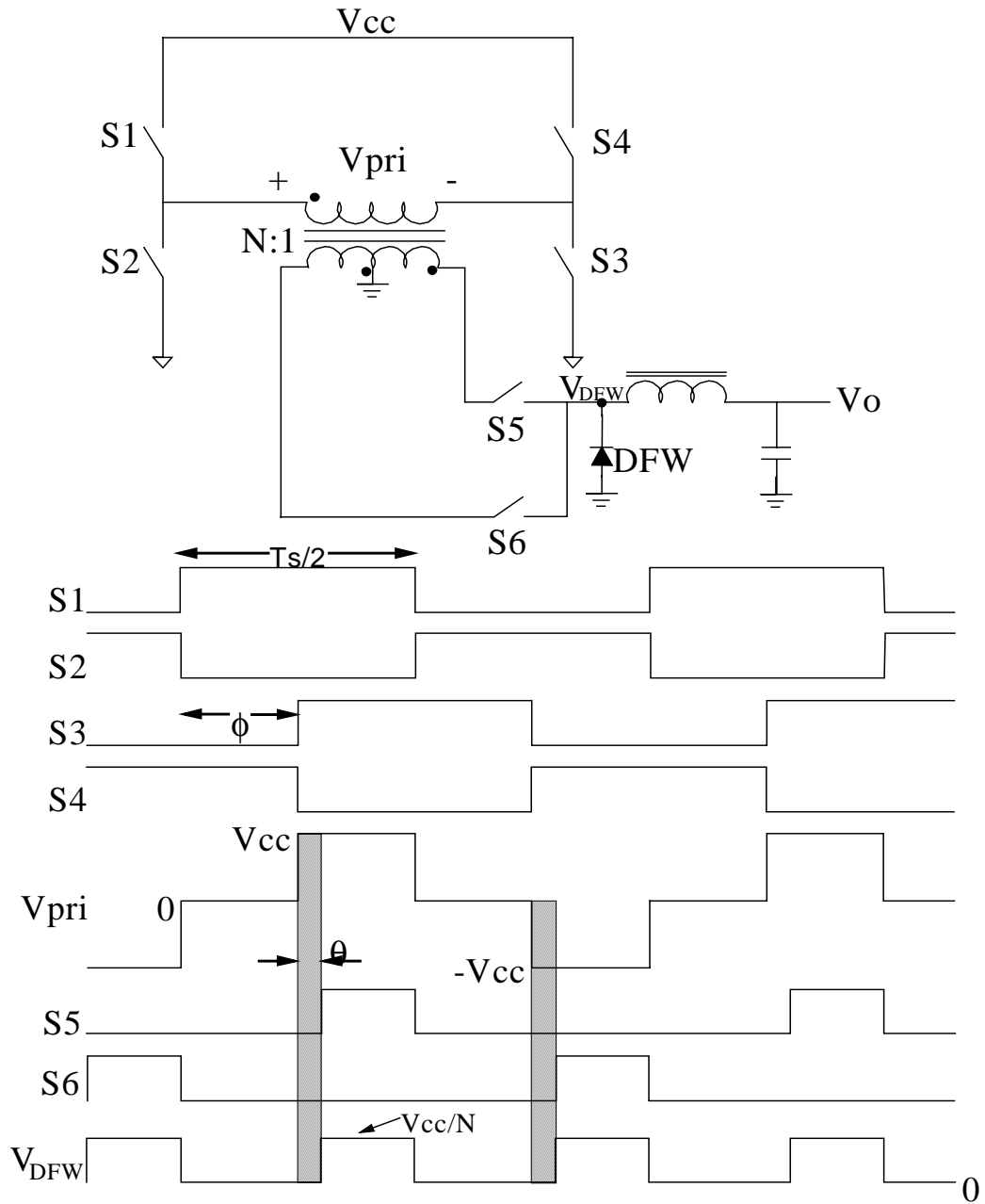


Fig. 2.2 PWM phase-shifted full-bridge converter with secondary-side control.

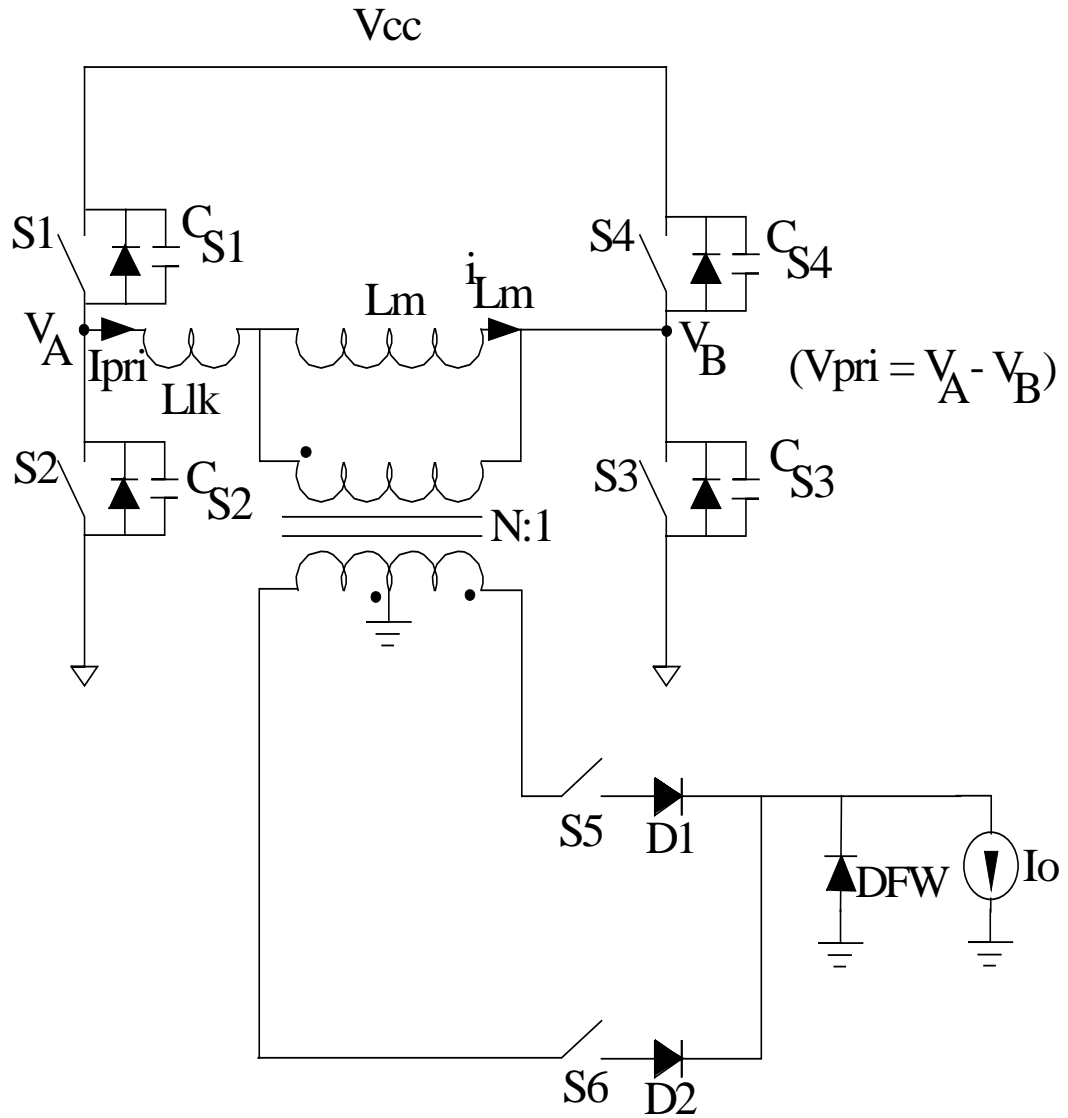


Fig. 2.3 Idealized ZVS-FB schematic with secondary-side switches.

circulating the freewheeling inductor current on the secondary, as opposed to the primary, tends to improve efficiency, with the penalty of the cost of the additional diode [37, 38]. Figure 2.4 shows the key waveforms and Fig. 2.5 the principle topological states. In Fig. 2.5, the darker lines in the secondary schematic indicate the load current path. For the description of the topological states, it is assumed the energy stored in the isolation transformer leakage inductance is insufficient to realize ZVS for S3 and S4, but the combination of leakage and magnetizing inductance energy will achieve ZVS for S3 and S4. (In addition, the delay between turn on and turn off of the complementary side switches in the bridge is sufficient to allow for ZVS as well). Considering all switching components to be ideal, the sequence of steady state topological modes over one-half of a full-bridge switching cycle is:

$T_0 - T_1$: At T_0 , S1 is turned off with S3 still on. D1 and S5 are conducting the load current while C_{S1} and C_{S2} are being charged and discharged, respectively, by $I_o/N+i_{Lm}$. Because the leakage inductance is much smaller than the magnetizing inductance, the decreasing transformer voltage is dropped primarily across the magnetizing inductance. Therefore, the primary current is relatively constant during this transition.

$T_1 - T_2$: At T_1 , the body diode of S2 starts conducting. Since the primary current has decreased to something slightly less than I_o/N , the difference on the secondary is picked up by the freewheeling diode, DFW (S6 is open). The slope of the primary current remains slightly negative since, ideally, the voltage across the magnetizing current is clamped to zero by the secondary. Sometime during this interval S2 can be turned on into zero volts.

$T_2 - T_3$: At T_2 , S3 is turned off. C_{S3} and C_{S4} are charged and discharged, respectively, by the energy stored in the leakage inductance. Because the voltage across the transformer's magnetizing inductance remains clamped at zero volts, the leakage inductance drops all of the decreasing primary voltage. As a result, the primary current decreases very rapidly. On the secondary, the freewheeling diode continues to make up

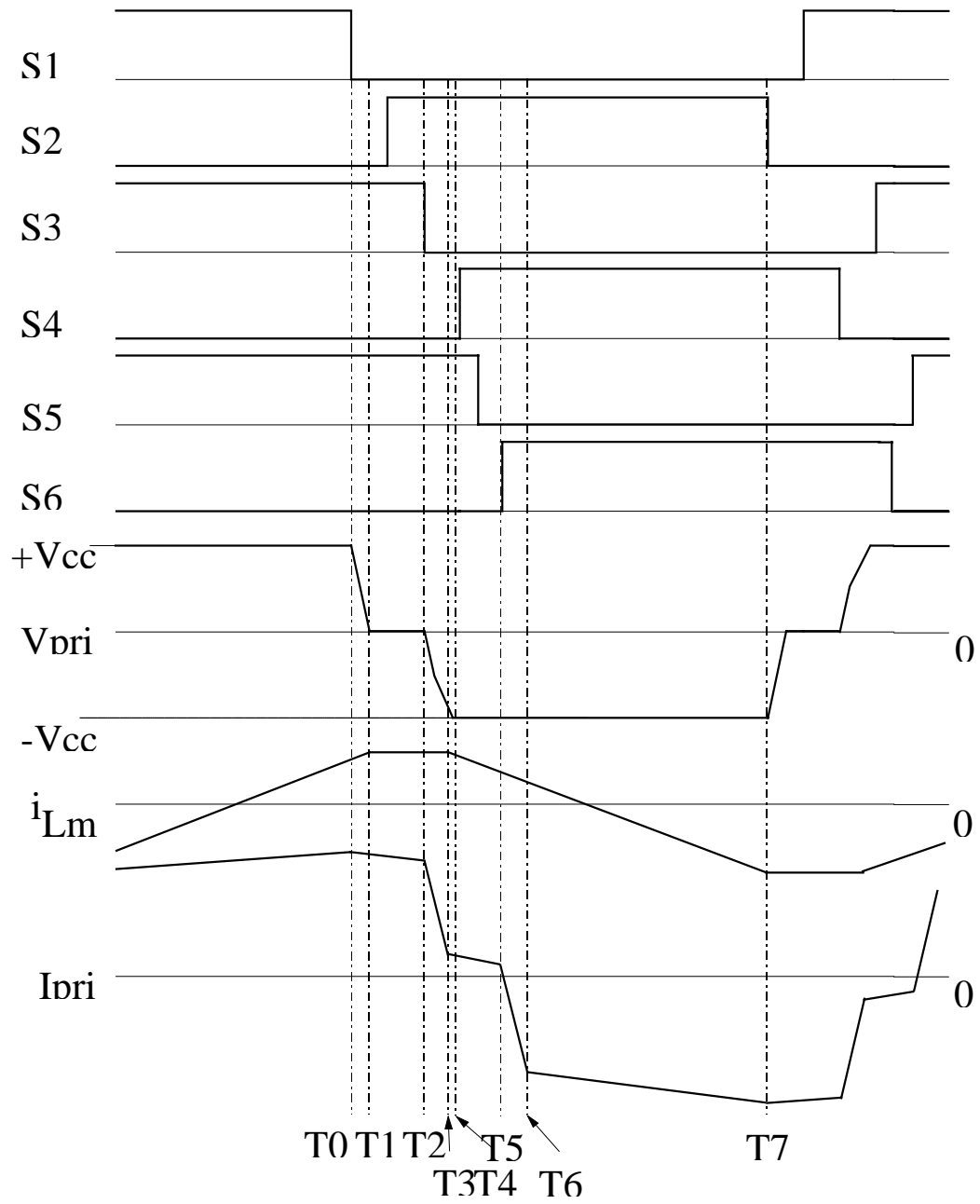


Fig. 2.4 Idealized ZVS-FB key waveforms.

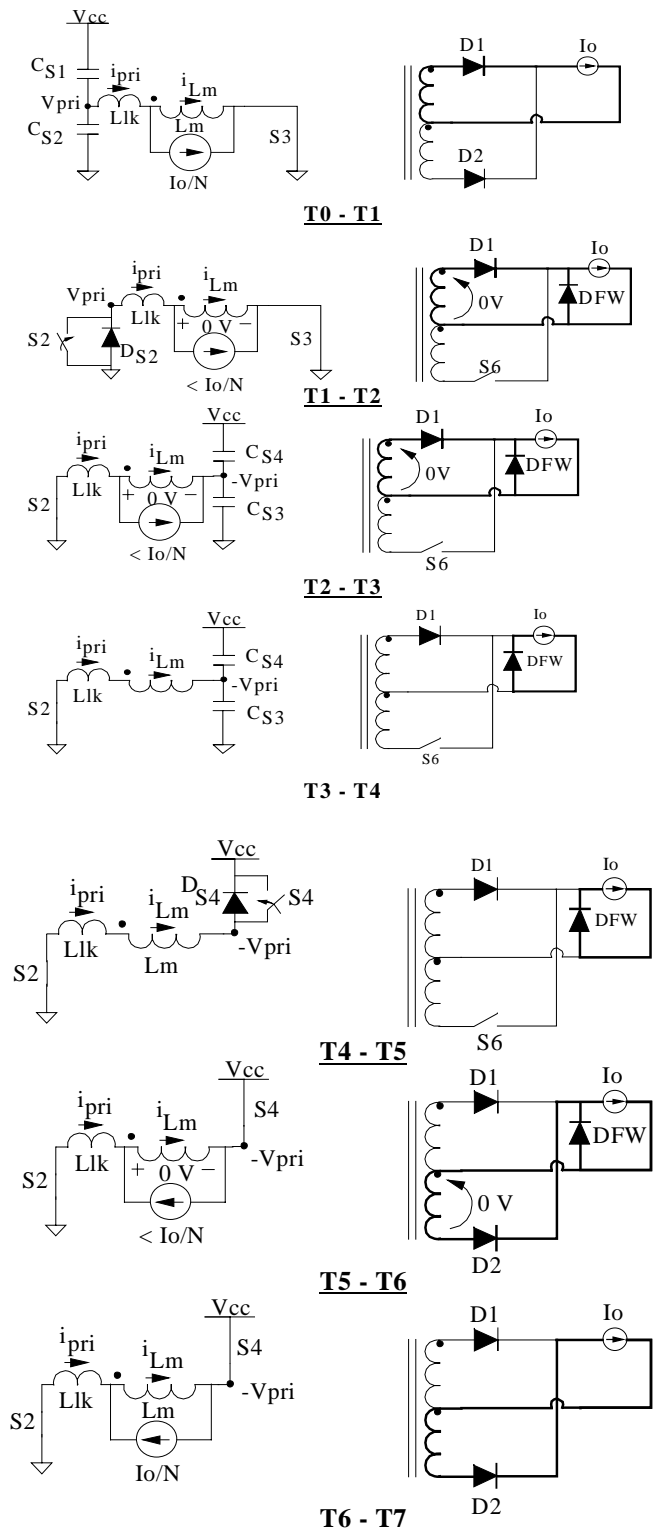


Fig. 2.5 Idealized ZVS-FB primary and secondary topological states.

the increasing difference between the reflected primary current and the load current, I_o .

$T_3 - T_4$: At T_3 , the leakage inductor current has decayed to the point where it is equal in value to the magnetizing current. D1 unclamps the secondary voltage and all of the load current commutes to the freewheeling diode. Because of the presence of S6 and the fact that it is open, the (very large) magnetizing inductance is now free to join the resonance with the switch capacitance. In this manner, the useful load range for ZVS is extended below that which could be obtained using only the leakage inductance.

$T_4 - T_5$: At T_4 D_{S4} is forced into conduction and S4 can then be turned on into zero volts.

$T_5 - T_6$: At T_5 , S6 is closed, allowing D2 to start conducting. This once again clamps the voltage across the magnetizing inductance to zero, and drops the supply voltage across the leakage inductance. The primary current starts decreasing very rapidly. The maximum time delay for the closing of S6 (i.e., the duration of intervals $T_3 - T_5$) is determined by the volt-seconds required by the output inductor to maintain the desired output voltage. The minimum delay is equal to the duration of the interval between the turn-off of S3 and the turn-on of S4. A quantitative analysis is given in Section 2.3.

$T_6 - T_7$: At T_6 , the primary current has decreased to the point where it equals the sum of the reflected load current and the magnetizing current. With DFW turning off, D2 now carries the full load current. During this interval positive volt-seconds are applied to the output inductor (in the normal manner for a buck converter). At T_7 , the cycle is repeated, except with the correspondingly opposite set of bridge transistors.

The presence of the secondary switches not only provide a mechanism through which the ZVS range can be increased, but, as mentioned previously, provides a means through which output voltage regulation can be accomplished in a very simple fashion. This can be done by modulating the turn-on time of S5 and S6, which in turn varies the applied volt-seconds to the output inductor. The primary advantages of secondary-side regulation are the removal of the need to pass a voltage feedback signal across the

isolation barrier and the subsequent elimination of control of the phase-shifting for the FB switches. Also, secondary-side control can have the capability to isolate load faults from the primary or, in the case of a multiple output converter, from other outputs (S5 and S6 could be left open for the duration of an output short).

The choice of the type of switch implementation for S5 and S6 depends on the application. If high output current is required, saturable reactors (magamps) make a good choice. The operation of an ideal square-loop core magamp acting as switch S6 is illustrated in Fig. 2.6. The operating point locations shown on the B-H curve in the figure correspond to the topological states outlined in Fig. 2.5, except for the point marked T_4^* . This is equivalent to the topological state starting at T_4 (as shown in Fig. 2.5) that occurs during the *opposite* half cycle of bridge operation, i.e., when D2 is turning off. Reset of S6 occurs between T_4^* and the turn off of S1 (which occurs at T_0).

2.3 Analysis of ZVS Range and Duty Cycle Loss

This section derives the conditions required to achieve zero-voltage-switching by utilizing the energy stored in the isolation transformer magnetizing inductance (L_m). To simplify the analysis, the following assumptions are made (refer to Figures 2.2 through 2.5):

- 1) $\phi \rightarrow 0$ (i.e., the primary side duty cycle approaches 100%),
- 2) the delay between turn on/turn off of switches on the same bridge leg is small compared to $T_s/2$,
- 3) $L_{lk} \ll L_m$, and
- 4) the energy stored in the leakage inductance (L_{lk}) is insufficient by itself to realize ZVS.

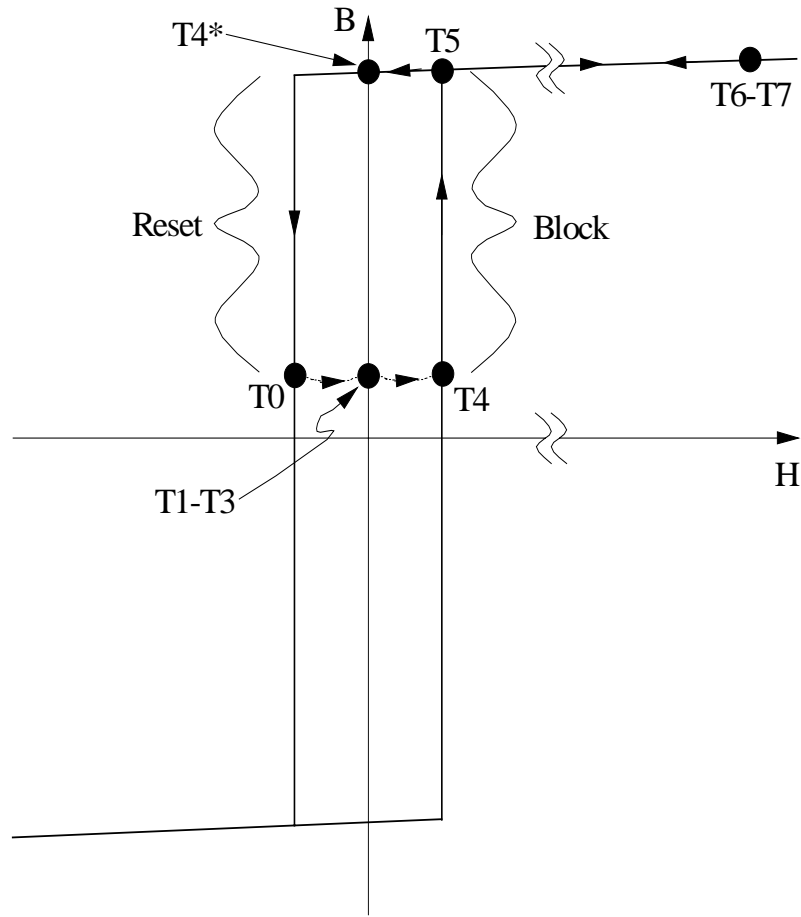


Fig. 2.6 Square-loop core operation of secondary switch S6.

First, for ZVS to be realized utilizing the energy stored in the magnetizing inductance the following inequality must be satisfied (this assumes leakage inductance is zero):

$$\frac{1}{2} L_m i_{Lm}^2 \Big|_{S3 \text{ or } S4 \text{ turn-off}} \geq \frac{1}{2} \left(\frac{8}{3} C_{oss} \right) V_{cc}^2 + \frac{1}{2} C_{xfmr} V_{cc}^2 = \frac{1}{2} C_{eq} V_{cc}^2, \quad (2.1)$$

where $C_{eq} = (8/3)C_{oss} + C_{xfmr}$. C_{oss} is the value of MOSFET output capacitance determined at a drain-to-source voltage of V_{cc} and C_{xfmr} is the isolation transformer's winding capacitance. The factor of 8/3 results from the fact that the value of output capacitance is a nonlinear function of the MOSFET drain-to-source voltage [31, 38]. At the point where S3 or S4 turns off, the magnetizing current is given by:

$$i_{Lm} = \frac{V_{cc} T_s}{4 L_m}, \quad (2.2)$$

where T_s is the switching period for the bridge switches. Solving Eqs. 2.1 and 2.2 for L_m yields:

$$L_m \leq \frac{T_s^2}{16 C_{eq}}. \quad (2.3)$$

For the power stage design described in Section 2.4, $C_{eq} \approx 400$ pF, resulting in a maximum magnetizing inductance of 15.6 mH, significantly greater than the 2.2 mH value used in the design.

For ZVS, in addition to the constraint required by Eq. 2.3, the duration of the $T_3 - T_4$ interval must be of sufficient length to allow the resonance of L_m and C_{eq} to reach the point where V_B (see Fig. 2.3) equals V_{cc} or ground. If S3 or S4 is turned on before the $T_3 - T_4$ interval is completed ZVS is lost. The duration of the interval is dependent on the value of V_B at T_3 and this in turn is dependent on the energy stored in L_{lk} and the duration of the $T_2 - T_3$ interval. The $T_2 - T_3$ interval terminates when the current in the leakage inductance decays to the point where it equals the magnetizing current. During this interval the voltage at V_B is given by:

$$V_B(t)|_{T_2-T_3 \text{ interval}} = \left(\frac{I_o}{N} + \frac{V_{cc}T_s}{4L_m} \right) \sqrt{\frac{L_{lk}}{C_{eq}}} \sin \frac{t}{\sqrt{L_{lk}C_{eq}}}. \quad (2.4)$$

The current in the leakage inductance during this interval is then:

$$i_{Llk}(t)|_{T_2-T_3 \text{ interval}} = \left(\frac{I_o}{N} + \frac{V_{cc}T_s}{4L_m} \right) \cos \frac{t}{\sqrt{L_{lk}C_{eq}}}. \quad (2.5)$$

Therefore, the duration of the $T_2 - T_3$ interval is

$$\Delta(T_2 - T_3) = \sqrt{L_{lk}C_{eq}} \cos^{-1} \frac{NV_{cc}T_s}{4L_mI_o + NV_{cc}T_s}. \quad (2.6)$$

The value of V_B at T_3 is then

$$V_B|_{T_3} = \left(\frac{I_o}{N} + \frac{V_{cc} T_s}{4L_m} \right) \sqrt{\frac{L_{lk}}{C_{eq}}} \sin \left[\cos^{-1} \left(\frac{NV_{cc} T_s}{4L_m I_o + NV_{cc} T_s} \right) \right]. \quad (2.7)$$

For the $T_3 - T_4$ interval the magnetizing inductance is free to resonate with C_{eq} . Therefore,

$$V_B(t)|_{T_3-T_4 \text{ interval}} = V_B|_{T_3} + \frac{V_{cc} T_s}{4L_m} \sqrt{\frac{L_m}{C_{eq}}} \sin \frac{t}{\sqrt{L_m C_{eq}}}. \quad (2.8)$$

For zero-voltage-switching, $V_B = V_{cc}$ and this marks the completion of the $T_3 - T_4$ interval. The duration of the $T_3 - T_4$ interval is then given by:

$$\Delta(T_3 - T_4) = \sqrt{L_m C_{eq}} \sin^{-1} \left(\frac{V_{cc} - V_B|_{T_3}}{\frac{V_{cc} T_s}{4L_m} \sqrt{\frac{L_m}{C_{eq}}}} \right). \quad (2.9)$$

Equations (2.3), (2.7), and (2.9) serve to define the conditions for achieving ZVS using the magnetizing inductance.

The total duration of intervals $T_2 - T_3$ and $T_3 - T_4$ also serves to set an upper limit on the conversion ratio by limiting the maximum duty cycle seen by the secondary. In particular, during the $T_3 - T_4$ interval the freewheeling diode (DFW, see Fig. 2.5) is conducting the output inductor current, so the longer the duration of this interval the greater the loss of secondary-side volt-seconds that could otherwise have been applied to the inductor. Of course, this assumes S6 (S5) was being controlled such that it would be

turned on simultaneously with the turn-on of S4 (S3) (i.e., the controller is commanding maximum output voltage). Practically speaking, a trade-off would normally need to be made with respect to the ZVS range and the maximum conversion ratio.

Under the assumptions outlined above, defining Δ to be the sum of the durations of the $T_2 - T_3$ and $T_3 - T_4$ intervals (Eqs. (2.6) + (2.9)), the maximum conversion ratio is:

$$\left. \frac{V_o}{V_{cc}} \right|_{\max} = \frac{1 - \frac{2\Delta}{T_s}}{N}. \quad (2.10)$$

The minimum conversion ratio is determined by the maximum blocking time of S5 and S6:

$$\left. \frac{V_o}{V_{cc}} \right|_{\min} = \frac{1 - \frac{2(\Delta + t_{block,max})}{T_s}}{N}. \quad (2.11)$$

The maximum blocking time of S5 and S6, $t_{block,max}$, is obtained from Eq. (2.13):

$$t_{block,max}(\text{sec}) = \frac{NA_e(2B_{sat})}{V_{block}}. \quad (2.12)$$

2.4 Circuit Design

2.4.1 Specifications

To provide experimental verification of the operating principles described in the previous sections, a 1 kW FB-ZVS converter was built to the following specifications:

- $V_{in} = 350 \text{ Vdc} - 450 \text{ Vdc}$,
- $V_O = 12 \text{ Vdc}$ at 83 A maximum ($P_o \text{ max.} = 1 \text{ kW}$), and
- $F_S = 100 \text{ kHz}$.

The input voltage range was selected to match the output range from a typical off-line, universal input voltage power factor correction (PFC) boost converter, as was discussed in Section 2.1. The output voltage was selected to be 12 Vdc at 1 kW in order to determine the utility of magamps as high current secondary-side switches. Although a 48 Vdc bus will be considered exclusively in Chapters 3 and 4, the exact value of the bus voltage is not important with respect to verifying the principles of operation of the converter being considered here. However, efficiency data for this converter with a 48 Vdc output at 1 kW is reported in [38]. Switches S5 and S6 are realized using magamps. Additionally, magamps are well suited for use in this particular application because of the relatively narrow range of input voltage. This reduces the range of volt-seconds required to be blocked, enabling the use of smaller cores. One disadvantage to using square-loop core magamps, however, is increased core loss as the switching frequency is increased. The switching frequency of 100 kHz was selected to help minimize this problem. A further discussion of this tradeoff is provided in Section 2.5.

2.4.2 Power stage design

The simplified schematic for the power stage and primary side control signals is shown in Fig. 2.7. Except for the magamp portion, the process of selecting the power stage

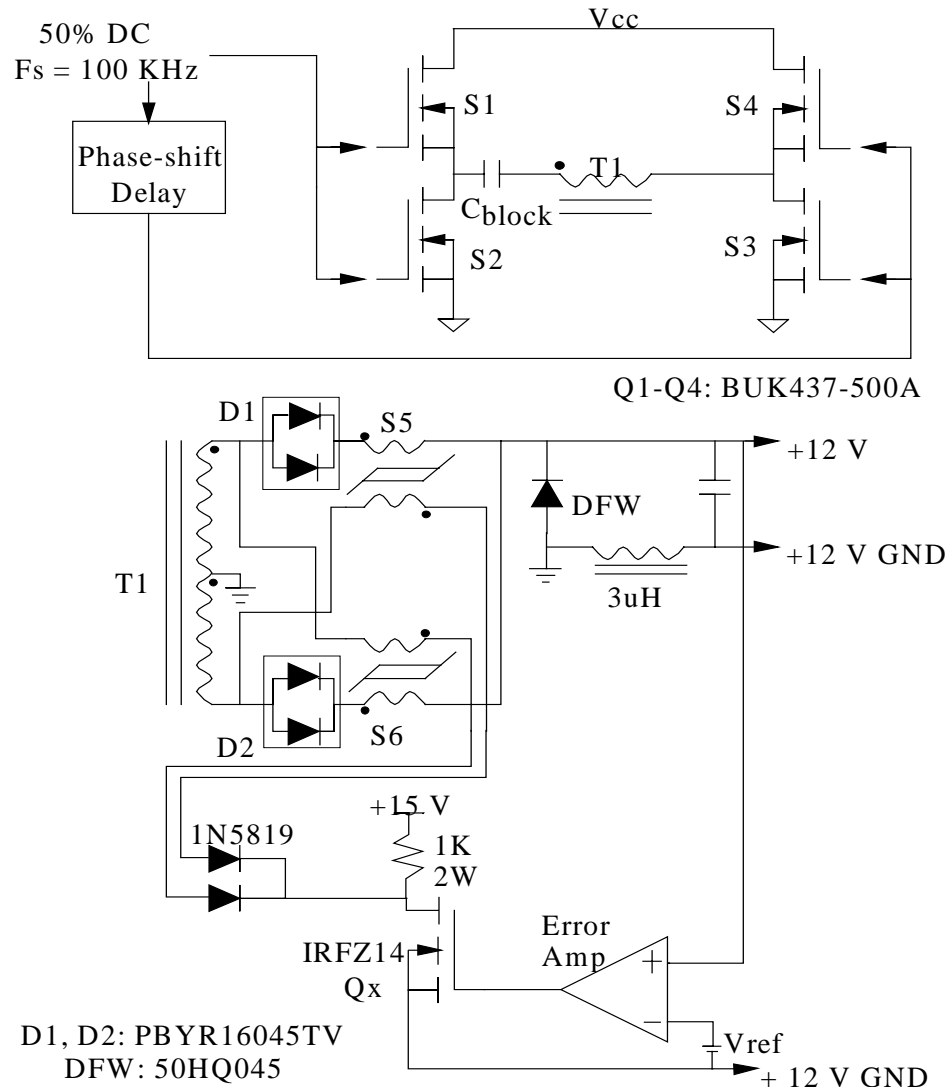


Fig. 2.7 Simplified schematic of the 1 kW FB-ZVS-PWM converter.

components is identical that which would be done for a standard phase-shift controlled full-bridge converter designed to similar power and voltage levels.

The isolation transformer (T1) design consists of the following:

core: Toshiba PC40ETD49-Z.

primary winding: 22 turns of 7 strands of 26 AWG.

secondary winding: 1 turn of 4 paralleled sheets of 5 mil x 1" wide Cu foil.

winding pattern: 1/2 primary - secondary - 1/2 primary (i.e., interleaved).

magnetizing inductance: 2.2 mH.

leakage inductance (referred to the primary): $\sim 4.2 \mu\text{H}$.

The transformer was wound with the intent of minimizing leakage inductance and the core was not gapped. Copper foil was used for the secondary winding due to the high output current.

Ideally, for phase-shifted, constant-frequency operation, the gate drive signals for the bridge transistors are operated with a 50% duty cycle and transistor pairs are switched 180° out-of-phase. However, as discussed in Section 2.2, in order to allow the resonant transitions to occur delays are deliberately introduced between the turn-on/turn-off of switches in the same bridge leg. This has the benefit of preventing cross-conduction problems but reduces the secondary-side maximum duty cycle (see Section 2.3). This delay circuitry is not shown in Fig. 2.7.

The "phase-shift delay" shown in Fig. 2.7 is used to introduce a delay in the drive signal of the S3, S4 transistor pair relative the S1, S2 pair. Since closed-loop control is accomplished entirely on the secondary side, this delay is held constant. Ideally, the delay would be near zero in order to maximize the primary-side duty cycle and hence, the transformer turns ratio. However, for experimental purposes the bridge transistors in the breadboard were switched with a duty cycle of about 85% to more clearly illustrate the

converter operation. Also, a high-frequency blocking capacitor is used to keep the volt-seconds on the transformer balanced.

2.4.3 Magamp circuit design

A simplified version of the secondary-side magamp and control circuitry is also shown in Fig. 2.7. Because of the physical layout of the secondary, the magamps were placed on the cathode side of the rectifier diodes. The MOSFET (Qx) pass transistor's "on" resistance is modulated by the control loop, providing the necessary amount of reset voltage to the magamps in order to maintain output voltage regulation. Magamp reset current flows through each output rectifier's RC snubber network (not shown in Fig. 2.7) and the transformer secondary. In the absence of rectifier snubber networks, diode parasitic capacitance can be used to complete the current path. As explained previously, individual core reset can occur only during the opposite half cycles of bridge operation.

Because of the high secondary current, the maximum number of primary turns available for the magamp core is one. This limits the maximum blocking time available from the core, which is given by:

$$t_{block}(\text{sec}) = \frac{NA_e(B_{sat} - B_{reset})}{V_{block}}, \quad (2.13)$$

where A_e is the core cross section (in m^2) and the flux density, B , is in Tesla. Maximum blocking time occurs at high-line, light load and is about $1.5 \mu\text{s}$ in this application. The magamp design implemented in the 1 kW breadboard is:

core: 2 x Allied Signal METGLAS #MP1906.

primary winding: 1 turn of 7 strands of 150/33 AWG Litz wire.

reset winding: 1 turn of 26 AWG.

To meet the maximum blocking time, two cores were required to realize a single magamp. Maximum core loss can be estimated from [39]:

$$P_{core} (W / Kg) \approx 9.93 \times 10^{-6} \cdot F_S^{1.57} \cdot \left(\frac{B_{sat} - B_{reset}}{2} \right)^{1.70}, \quad (2.14)$$

where B is in Tesla and the switching frequency, F_S , is in Hz. The loss is about 1.76 W maximum per magamp.

2.5 Experimental Results

Transformer primary voltage and current waveforms are shown superimposed in Fig. 2.8. Operation is at the maximum line and load condition under closed-loop output voltage regulation. ZVS is easily obtained at this operating point as demonstrated in the oscillogram. With the secondary-side switching, the ZVS range extends down to about 15% of full load (150 W) over the line range. As a comparison, if output voltage regulation is disabled (i.e., the secondary-side duty cycle seen by the output inductor is constant - no closed loop output voltage feedback is utilized) achieving ZVS requires approximately 60% of full-load current. This difference is illustrated in Fig. 2.9. Both oscillograms show the primary voltage waveform at identical input voltage and load current operating points. As illustrated by the bottom waveform of Fig. 2.9, closed-loop control allows the magnetizing inductance to join the leakage inductance resonant transition. This occurs at the instant the voltage due the leakage inductance resonance transition reaches its peak. ZVS could be extended to even less load by further delaying S3's turn-on/turn-off time (relative to the turn-off/turn-on time of S4, see Fig. 2.4). However, as discussed in Section 2.3, the effective duty cycle on the

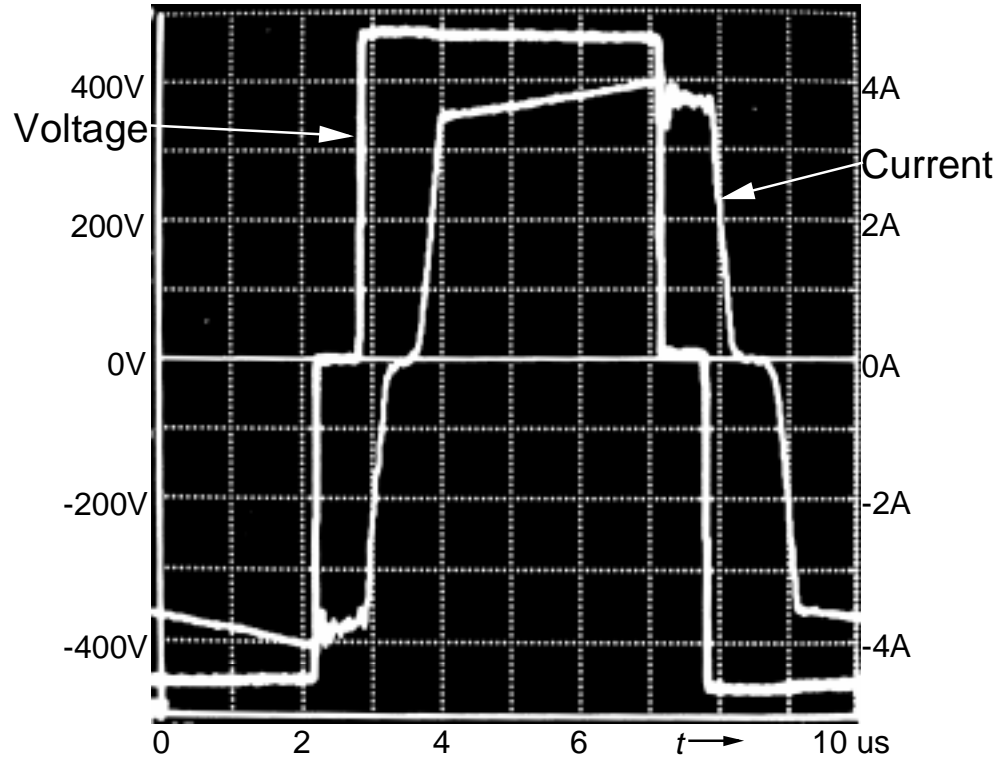


Fig. 2.8 Transformer primary voltage and current waveforms at $V_{in} = 450 \text{ Vdc}$ and $P_0 = 1 \text{ kW}$.

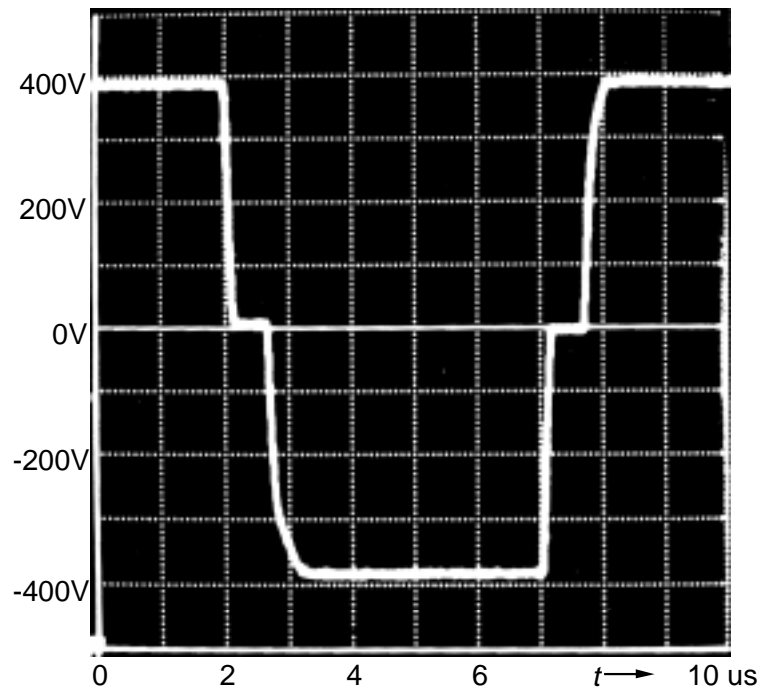
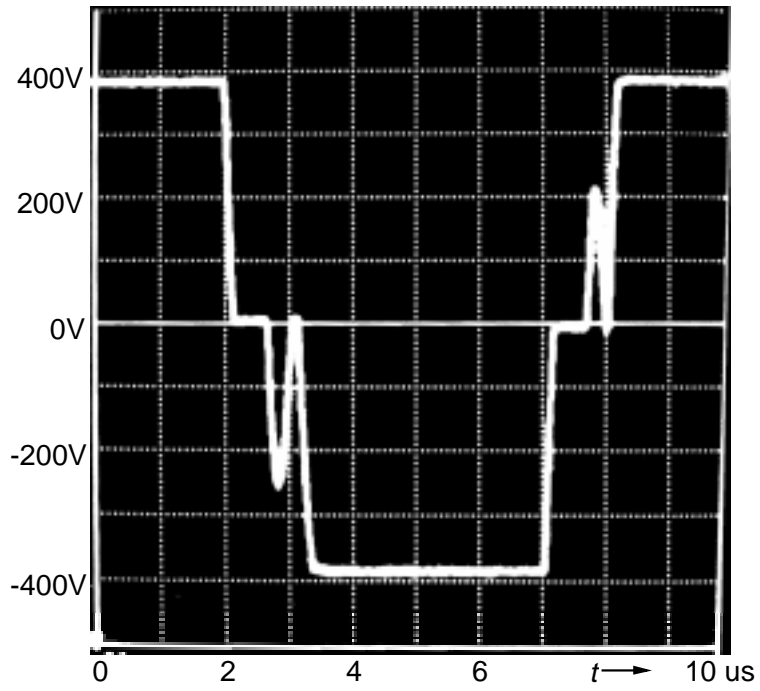


Fig. 2.9 Transformer primary voltage at $V_{in} = 375$ Vdc and $P_o = 150$ W. Top: "Open loop." Bottom: "Closed loop."

secondary is correspondingly reduced, potentially creating problems in obtaining closed-loop regulation during operation at low line, high load. For the breadboard constructed, regulation at full output power was lost when the input voltage dropped below about 360 Vdc.

Table 2.1 illustrates a comparison between the power dissipation savings incurred due to light-load ZVS of S3 and S4 versus the core loss introduced by the magamps used to realize the ZVS mechanism. A load current of 8 A (10% of full load) was used as the point of comparison. The table shows the losses as a function of both supply voltage and switching frequency. For the magamp loss calculations the induction level (ΔB) was held constant for the three different frequencies (although the volts-seconds required to be blocked increases as the switching frequency is decreased). As is shown in the table, the overall net gain in power dissipation is about break even until the switching frequency is increased to 200 kHz, at which point the high line magamp core loss will dominate. However, at 100 kHz and high-line a significant reduction in S3/S4 power dissipation can be had by shifting the transistor loss to the magamps. This would typically be desirable from the viewpoint of thermal management and reliability. The data in this table points out the importance of minimizing the volt-seconds the magamps have to block, particularly as the switching frequency is increased. For a constant load, the variation in magamp blocking time is a direct function of the variation in input voltage. This is a key reason why the method of achieving control and ZVS through the use of controlled switching on the secondary is so well suited as the second-stage front-end DC/DC converter - the input voltage variation from the PFC first stage is minimal.

Figure 2.10 shows experimental efficiencies vs. load at different input voltages. The efficiency decreases as the input voltage increases (the primary is switched with constant duty cycle, leading to increased circulating energy and magamp core loss as the input voltage increases). The disparity becomes more evident at lighter loads where the required volt-seconds to be blocked is greatest. These efficiency measurements do not

Table 2.1 Loss comparison - S3/S4 ZVS vs. magamp losses.

Fs	Vcc (V)	P_D Savings in S3 and S4 Due to ZVS	Magamp Core Loss Introduced
	450	2.6 W	2.1 W
50 kHz	400	1.9 W	2.1 W
	350	1.35 W	0.5 W
	450	5.2 W	6.2W
100 kHz	400	3.8 W	3.2 W
	350	2.7 W	1.5 W
	450	10.4 W	18.4 W
200 kHz	400	7.6 W	9.5 W
	350	5.4 W	4.4 W

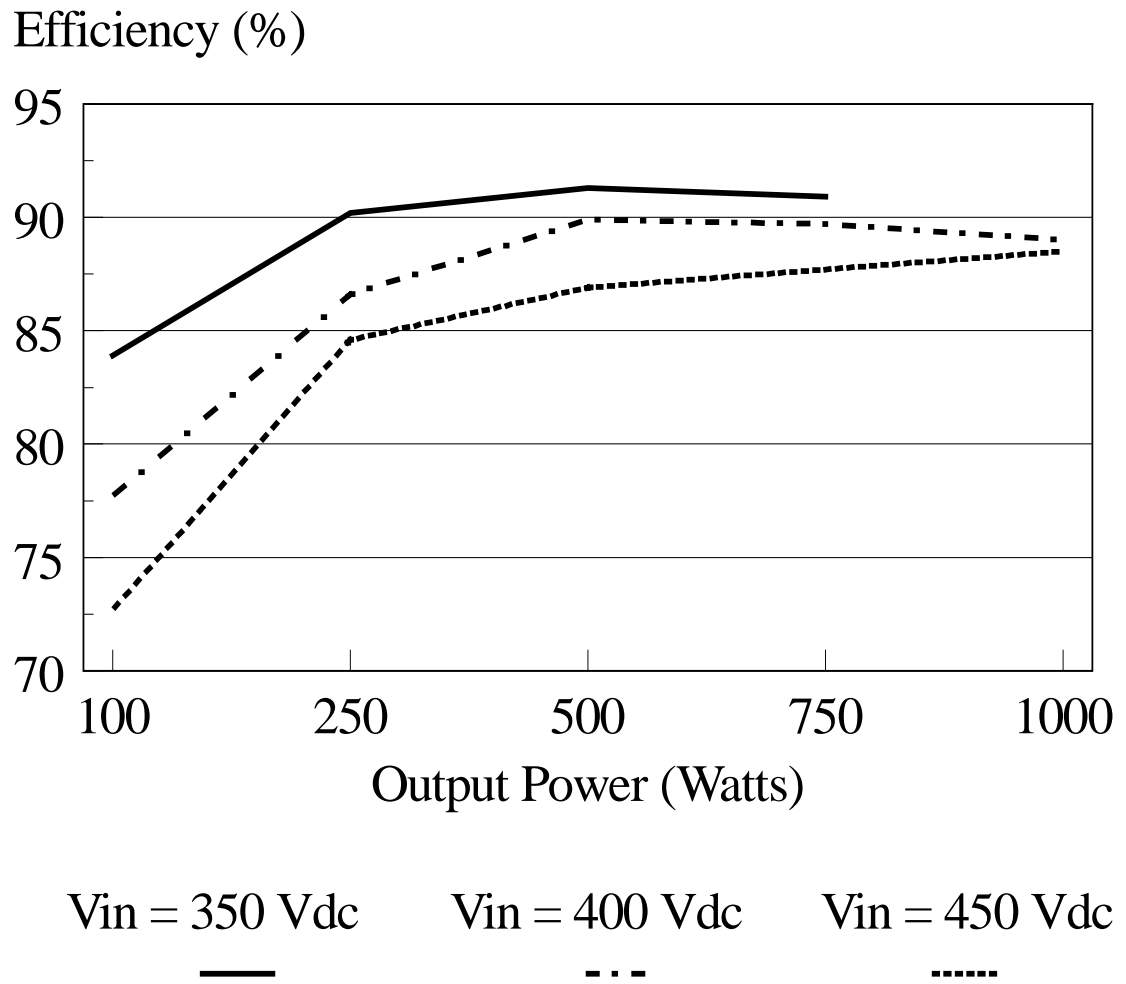


Fig. 2.10 Experimental efficiencies vs. output power.

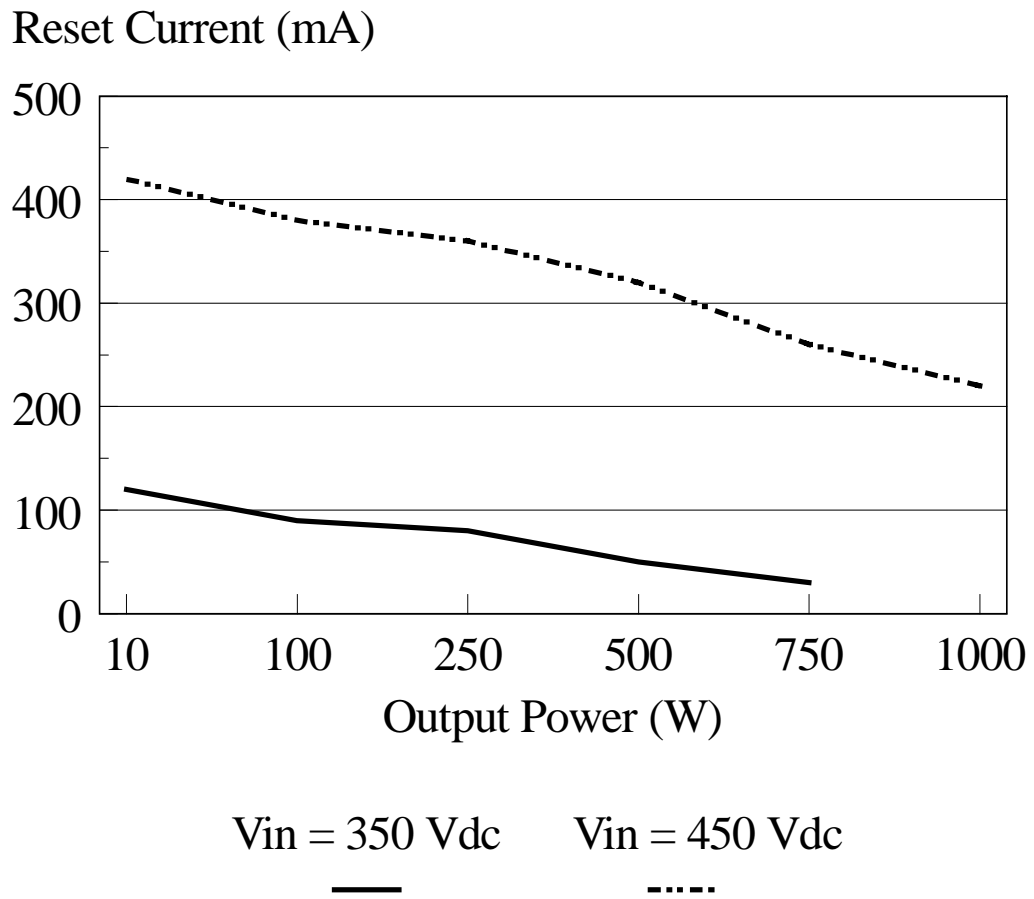


Fig. 2.11 Magamp reset current as a function of load and input voltage.

include the gate drive or magamp control circuitry power dissipations. The measured gate drive power dissipation was about 3 W. Figure 2.11 illustrates the required magamp control current as a function of line and load. These curves include both magamp reset currents.

Oscillograms showing the voltages across the output rectifier (D1) and magamp (SR1) (together with the primary current) are displayed in Figures 2.12 and 2.13. The rectifier voltage is very clean, with no overshoot at all. This marks a substantial performance departure from the more traditional ZVS FB converter, where parasitic oscillation between the resonant inductor (or, possibly just the leakage inductance) is a difficult issue to deal with. A comparative study of four different implementations of FB ZVS converters, including the circuit being described here, and of the parasitic oscillation problem, is reported in [38]. The exponential-like decay in the rectifier voltage (when the opposite rectifier is conducting) is due to the magamp reset current flowing through the parallel combination of the rectifier parasitic capacitance and RC snubber.

2.6 Summary

This chapter has described the analysis, design, and experimental results of an improved 100 kHz, 1 kW full-bridge, ZVS converter incorporating secondary-side control. Operation is from a 350 - 450 Vdc input with a 12 Vdc bus output voltage. Utilization of secondary-side switching accomplishes two important tasks: 1) extending the useful load range for zero-voltage-switching by enabling the transformer magnetizing inductance to join the resonance between the leakage inductance and the bridge switch capacitance, and 2) providing output voltage regulation for the secondary, which results in a simplified overall control scheme where the primary-side bridge switches are switched with a constant phase-shift (i.e., in an open loop fashion). For a low voltage,

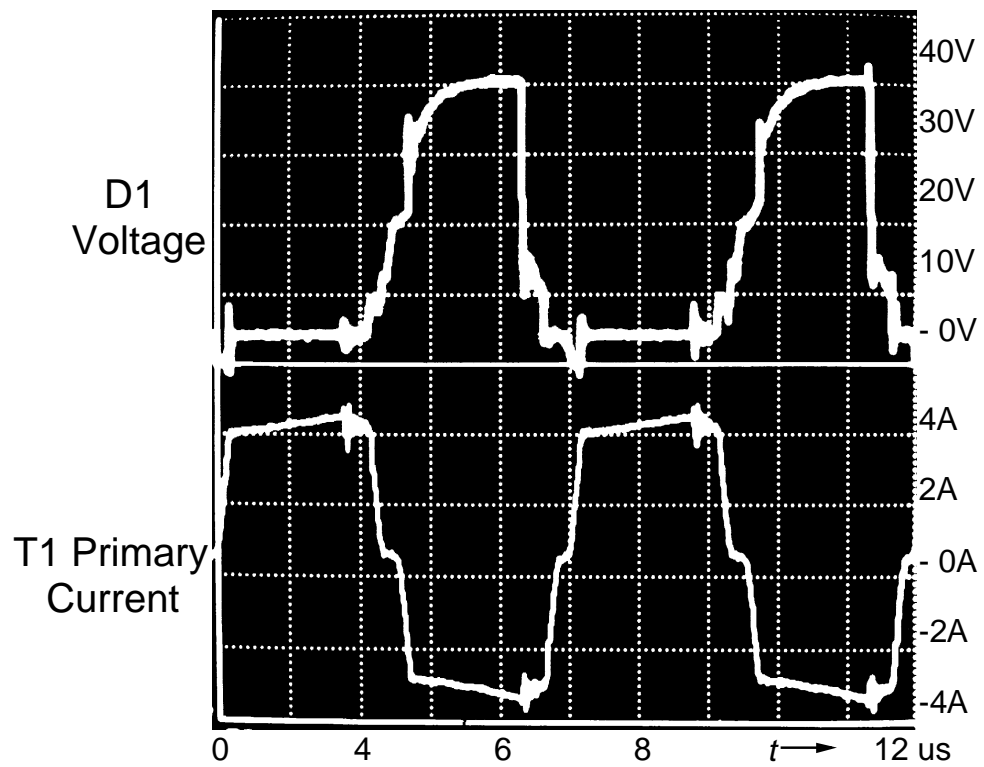


Fig. 2.12 Output rectifier D1 voltage and transformer primary current at $V_{in} = 450$ V, $P_o = 1$ kW.

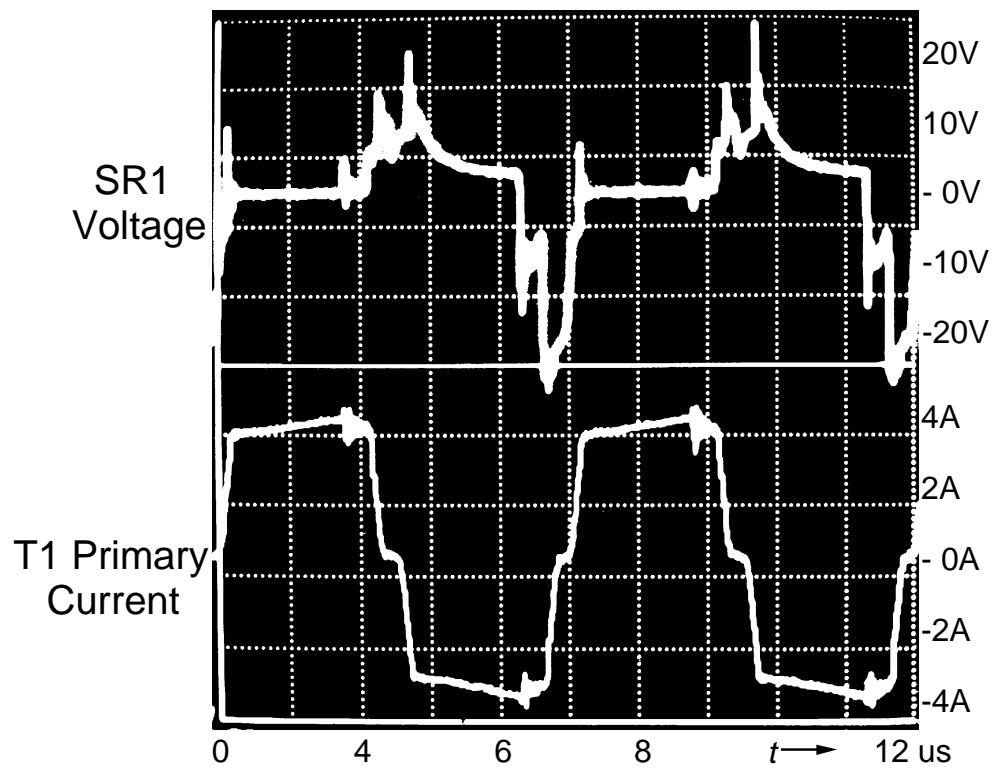


Fig. 2.13 Magamp SR1 voltage and transformer primary current at $V_{in} = 450$ V, $P_o = 1$ kW.

high current output magamps are the preferred choice for realizing the secondary switches.

Experimental results demonstrate the range of ZVS is extended from about 60% of full load without secondary switching to about 15% of full load when operating under closed-loop control (a factor of four improvement). Isolation transformer design is done to minimize leakage effects and it was not necessary to add any external resonant inductor in the primary. Experimental efficiencies between 85% and 91% were obtained above an output power of about 250 W.