5. SYSTEM SIMPLIFICATION

5.1 Conceptual Overview

As was discussed in Chapter 1, changing the "DC" method of power distribution to an "AC" power distribution technique can substantially mitigate the cost and complexity of the DC DPS. This was illustrated in Fig. 1.3. An AC DPS eliminates a conversion step in the chain of power flow. As will be demonstrated in Chapter 6, compared to an identically configured DC DPS, an AC DPS has increased power train efficiency and a decrease in power train complexity. Such fundamental improvements in a power system architecture begs the question as to why such a concept would not be universally adopted.

There are several perceived technical problem areas with respect to the development of an AC DPS that were introduced and briefly discussed in Section 1.1:

- Signal integrity issues with respect to the bussing of HF AC voltage and current waveforms.
- Poorly defined tradeoff issues between system component design and signal integrity.
- Post-regulator design in light of the absence of the traditional method of PWM control of the inverter switch.

The objective of this chapter is to investigate these issues, and where applicable, propose and verify resolutions. As a first step, however, it is necessary to provide a general overview of the type and physical layout of the system under consideration.

5.1.1 AC power distribution bus designs - problem assumptions/constraints

Before exploring AC distributed power system design details and issues, a rough concept of the physical dimensions and proposed type of bus structures for the type of computer system that would host such a power architecture should be outlined. Shown in Fig. 5.1 is a simplified description of the mechanical design and form-factor for a typical system board incorporated into a mid-range (300 W to 500 W) server [27]. Most personal computers and workstations exhibit similar system board dimensions to that shown in Fig. 5.1. The primary information to be gleaned from Fig. 5.1 is that, for the baseboard configuration shown, the HF AC power distribution bus would occupy dimensions on the order of that shown in the figure (≈ 12" diagonal dimension). Also, implied is the stipulation that the power distribution bus be an integral part of the system board printed circuit board (PCB), just as it is for the DC power systems designed into present-day computing systems (Fig. 1.1). The integration of the bus into the system board is shown in a simplified fashion in Fig. 5.2. Here the front-end converter is shown as being located on the system board, but this is for conceptual purposes only. A cross-section of a typical muti-layer system board PCB is shown in Fig. 5.3. Following standard industry practices, the typical PCB layer-to-layer spacing is about 6 mils. Depending on the total number of layers required, the spacing between the middle two layers is adjusted to achieve a total board thickness of between 62 and 70 mils, as indicated in the figure. For DC power systems, the inner two layers typically serve as the "power" and "ground" planes, and the same situation would be expected to be applied to an AC power distribution bus.

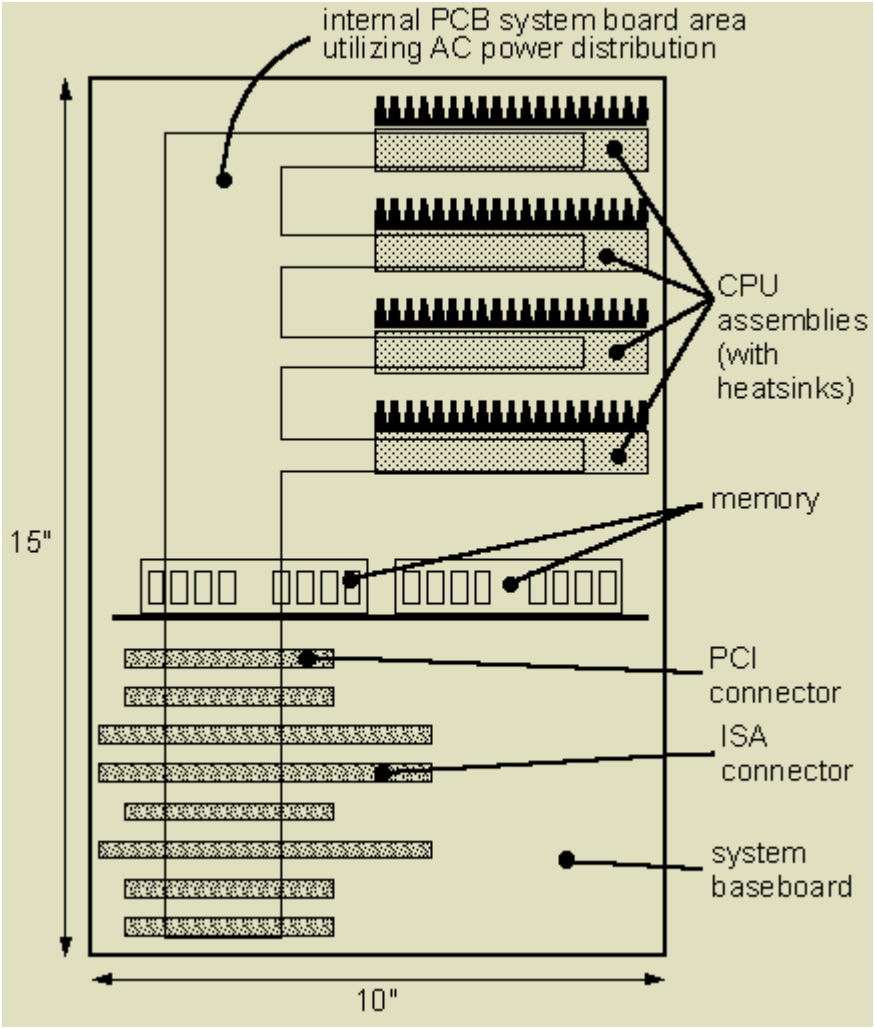


Fig. 5.1 Typical server system board physical layout, top view.

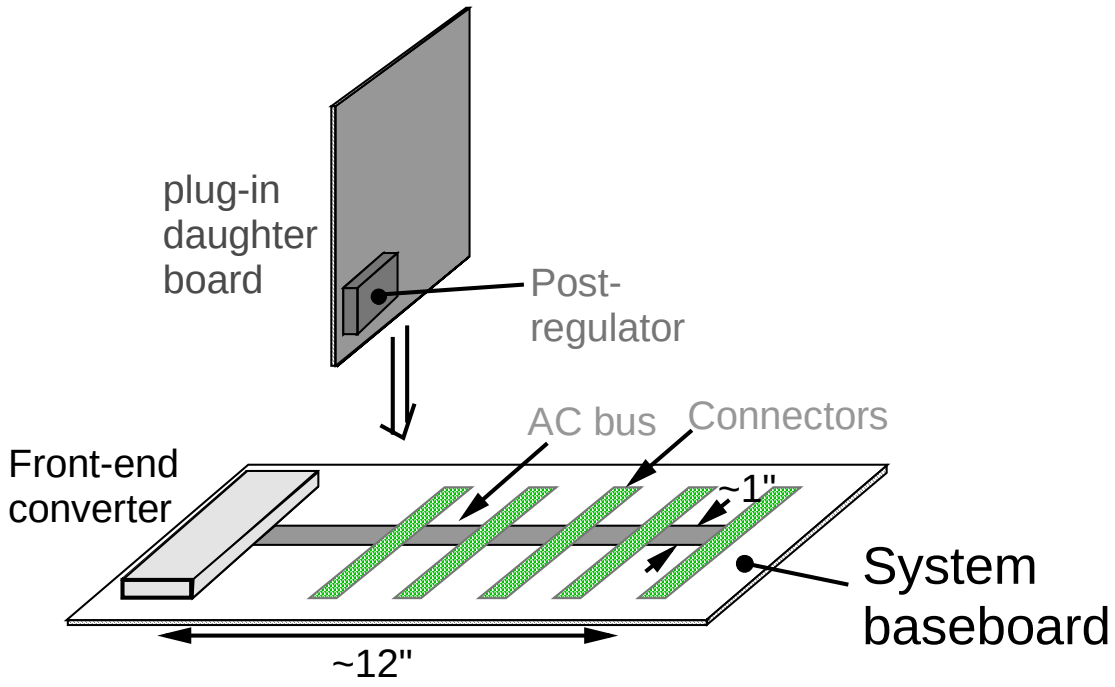


Fig. 5.2 Simplified concept of PCB AC power distribution bus.

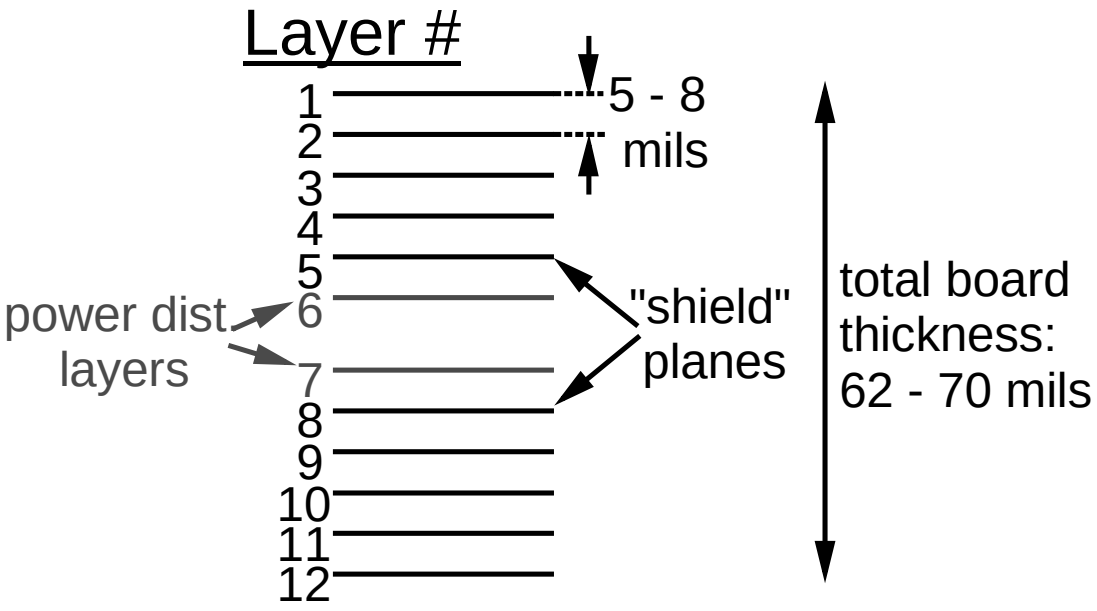


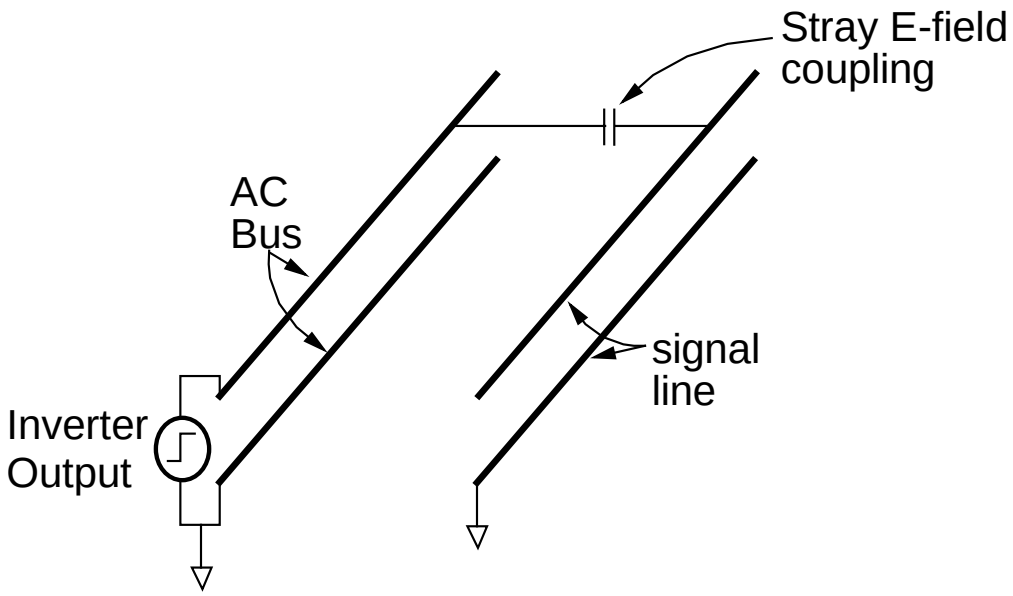
Fig. 5.3 Cross-section of a typical multi-layer baseboard PCB.

5.1.2 Physical bus design and the resulting implications to the host system

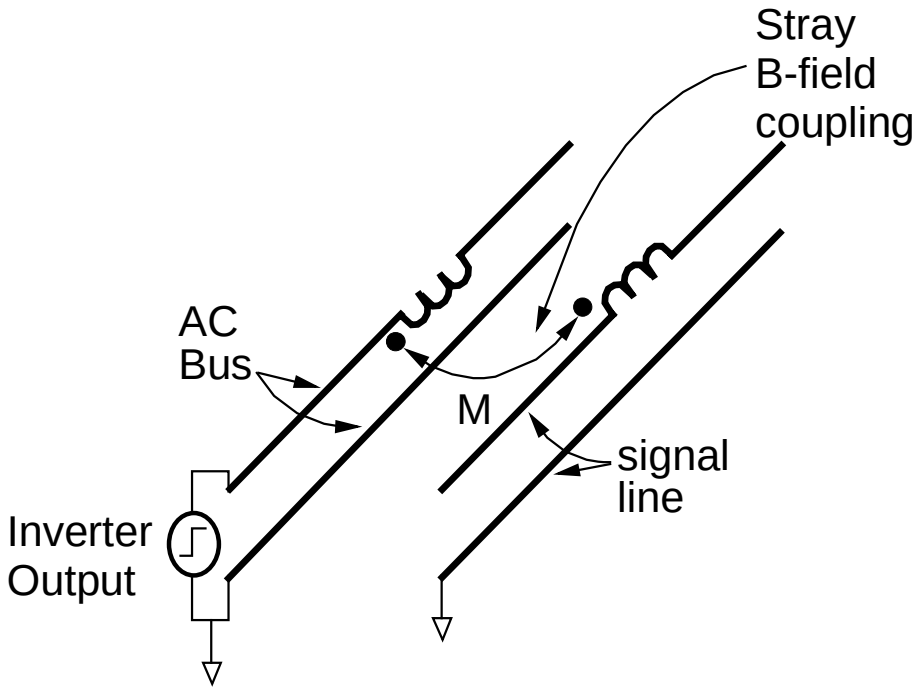
The implication that potential AC power distribution bus structures are limited to PCB implementations is that signal level PCB traces will necessarily be routed within very close physical proximity to the AC power distribution PCB routing. This is clearly illustrated by considering a signal level trace located on a PCB layer adjacent to the power distribution layers (see Fig. 5.3). In the absence of shield layers, if the trace were located immediately above or below the power distribution bus, a separation between the two of only five to eight mils would result. This is an advantage if high density/low-cost packaging of the system board functional components is desired, however, it is a distinct disadvantage when considering the possibility of the HF AC power distribution network injecting noise into the host system (crosstalk).

The phenomena of crosstalk can be modeled by the schematics shown in Fig. 5.4. Here it is assumed the crosstalk mechanisms are operating in the near field only, and, consequently, the electric and magnetic field effects can be treated separately (i.e., the electric or magnetic field properties are determined predominately by the characteristics of the source, not the propagation medium [53]). The transition region from near field to far field is defined as an approximate distance of $\lambda/2\pi$ from the electric or magnetic field source, where λ is the wavelength of the source under consideration. For example, for the transition region to reside within a distance of 12" from a source (the maximum circuit dimension being considered for this problem), and assuming a propagation medium of FR4 material (relative permittivity, ε_R, = 4.4 and relative permeability, μ_R, = 1), the highest significant harmonic present in the source would have to be greater than

$$f = \frac{c}{2\pi d\sqrt{\mu_r \varepsilon_r}} = 72 \text{ MHz.} \tag{5.1}$$



(a) Electric field.



(b) Magnetic field.

Fig. 5.4 Lumped circuit representation of parasitic electric field and magnetic field coupling for HF AC waveforms.

In Eq. (5.1) *c* is the velocity of light in meters/second and *d* is the distance from the source to the near field/far field transition region, in meters. FR4 material is probably the most common dielectric used in PCB manufacturing.

Another way of stating the near field/far field constraints is to stipulate that the dimensions of the circuits under consideration are to be much less than the wavelengths of the frequencies of interest. Again, assuming FR4 material, a maximum circuit dimension of 12" (or, for this calculation, one wavelength, λ) results in a frequency given by:

$$f = \frac{c}{\lambda\sqrt{\varepsilon_R \mu_R}} = 450 \text{ MHz.} \tag{5.2}$$

The value resulting from Eq. 5.2 is an order of magnitude greater than the highest frequencies that will be considered here, so lumped parameter approximations are well suited for subsequent analysis.

In Fig. 5.4(a), the effects of the time-varying electric field generated between the AC bus lines and subsequently being coupling to signal conductors can be modeled by inserting a capacitance between the respective conductors. The value of this capacitance is obtained from knowledge of geometry of the conductors and the permittivity of the material in which they are embedded. Any dv/dt appearing along the AC bus lines will result in current flow through the coupling capacitor. Depending on the signal line circuit impedances, a noise voltage will result that is proportional to the product of the injected noise current and the signal line Thevenin impedance.

In an analogous fashion, the effects of the time-varying magnetic field generated along the AC bus and subsequently being coupling to signal conductors can be modeled by coupling the respective conductors through a mutual inductance, M (see Fig. 5.4(b)).

The value of this mutual inductance is obtained from knowledge of geometry of the conductors, the permeability of the material in which they are embedded, and the source frequency. Any di/dt appearing along the AC bus lines will result in noise voltage coupling through the mutual inductance to the signal lines. This noise voltage appears in series with the signal line terminating impedances.

In light of the equivalent circuits shown in Fig. 5.4, it is easy to see why a DC power distribution bus would have reduced noise effects. For the DC system bus voltage dv/dt's and bus current di/dt's approach zero (ideally). In comparison with an AC system, even though the coupling mechanisms are identical, the crosstalk effects of the DC system should be greatly reduced.

However, for an AC DPS, given some fixed geometry, the magnitudes of the crosstalk effects are approximately directly proportional to the AC DPS bus waveform frequencies. For the case of coupled noise due to the stray electric field this assumes signal line termination impedances that are purely resistive and who have a value that is much less than the magnitude of the capacitor representing this stray electric field coupling. Assuming, for the moment, sinusoidal bus voltage and current waveforms, the amplitude of the noise voltage appearing between the signal line and its return (see Fig. 5.4) is given by:

$$V_{noise}\big|_{E-field} = j\omega_{bus} C R_t V_{bus}, \tag{5.3}$$

and

$$V_{Noise}\big|_{B-field} = j\omega_{bus} M I_{bus}, \tag{5.4}$$

where R_t is the signal lines' Thevenin terminating resistance. From Eqs. (5.3) and (5.4) it is clear the "efficiency" of both the electric and magnetic noise coupling mechanisms increase with increasing bus frequency. For non-sinusoidal bus waveforms harmonic content must be considered as well. The selection of bus frequency is analogous to the selection of switching frequency in DC/DC converter design for a DC DPS. It is common knowledge that reactive component and transformer size decrease with increased switching frequency (to some practical limit) but for an AC DPS higher bus frequencies will exaggerate induced system noise effects. For the analysis and experimental results that comprise the remainder of the chapter and all of Chapter 6, a 300 kHz bus frequency was selected as a reasonable compromise between converter size and potential noise effects.

5.2 Topology Considerations and Comparisons for HF AC Power Distribution

5.2.1 Introduction

Before giving further consideration to the issues of induced system noise and EMI in general, it needs to be determined, from a power converter topological perspective, what the tradeoffs are of processing various types of bus voltage and current waveforms. Although this issue is definitely not separate from the concerns of noise generated by the power system, if clear topological advantages to using some types of waveforms over others can be demonstrated, this must be taken into account as part of an effective overall system design. In order to put a practical limit on the number of bus waveform shapes that can be considered, the two "extremes" of waveshapes will be examined here - sinewave shapes and square-wave shapes.

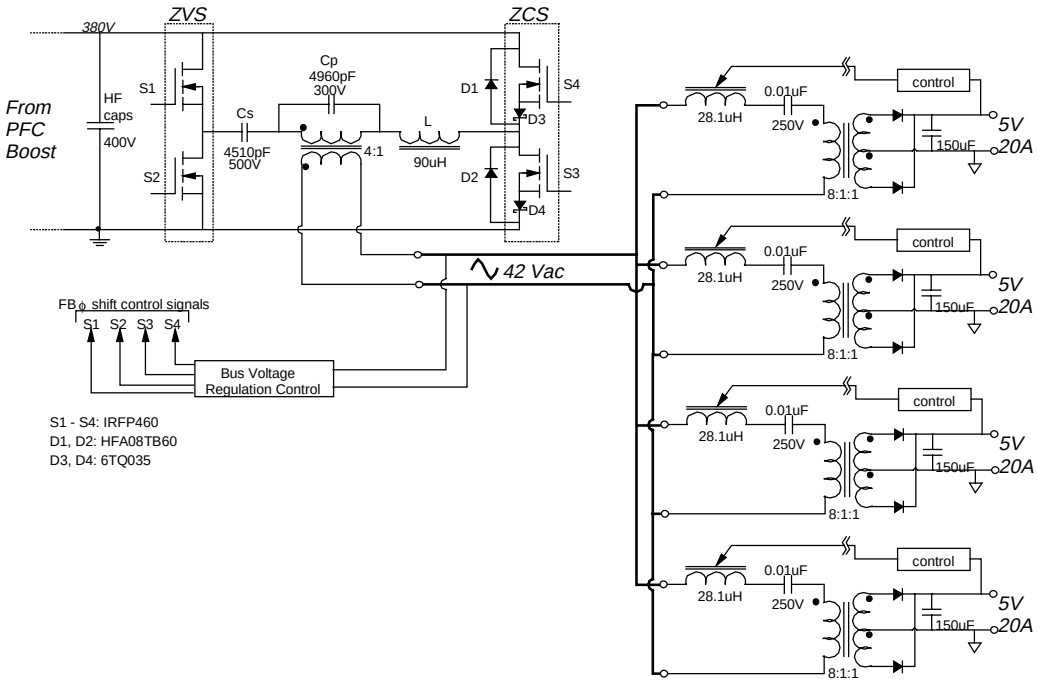
5.2.2 Power system design specifications and key design points

The power system designs that realize sinewave type bus voltage and current waveforms and square wave type waveforms are shown in Fig. 5.5. Both designs were completed to meet the following common system specifications:

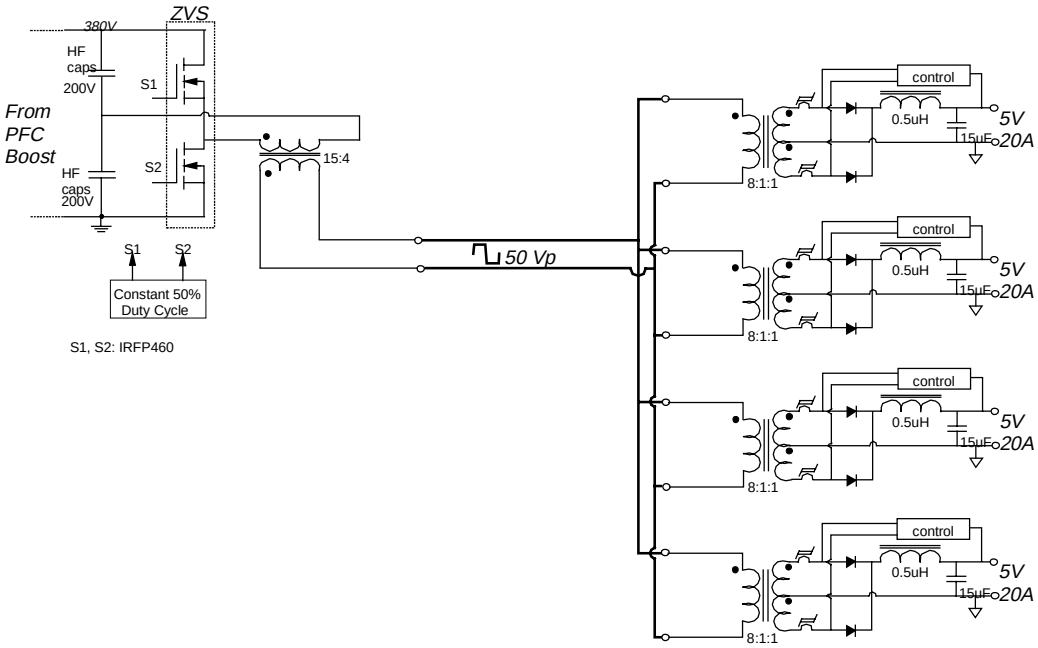
- The total output power is between 80 W and 400 W (20 % to 100 % load range) to approximate a typical mid-range server type of host computer system [27].
- Both front-end inverters are fed from identical PFC boost converters operating from a universal line input. Consequently, the designs will be compared only from the inverter DC input to the post-regulator DC outputs. The PFC circuits' output voltage will be considered constant as a function of line and load, with a value of 380 Vdc.
- Four post-regulators comprise the sum total of the power system load converters. Each is designed for a 5 Vdc output at 100 W maximum output power, with a 50 mVpp maximum output voltage ripple.
- The bus frequency is 300 kHz (fixed frequency) and the power distribution bus structure and power devices are considered ideal, i.e., any parasitic effects are ignored. For the sinewave system the bus voltage and current total harmonic distortion (THD) should be less than 10 %.

5.2.2.1 Sinewave power architecture design specifics

The sinewave power system, shown in Fig. 5.5 (a), consists of a full-bridge, clamped-mode, LCC resonant inverter [54, 55, 56, 57, 58, 59, 60] and series resonant rectifier (SRR) post-regulators [24, 25, 61, 62, 63]. The resonant inverter is responsible for generating a low harmonic distortion sinewave bus voltage waveform with the SRR post-regulators drawing low harmonic distortion sinewave currents from the inverter. In the inverter, S1 and S2 are switched with zero-voltage while S3 and S4 are switched with zero-current. This "mode" of



(a) Sinewave topology.



(b) Square-wave topology.

Fig. 5.5 Sine and square-wave AC DPS topologies used for comparison purposes.

operation was chosen to minimize the circulating energy in the inverter's tank components [54, 59]. The stipulation that S3 and S4 switch with zero current requires the application of blocking diodes (D3 and D4) and ultra-fast recovery rectifiers (D1 and D2) to prevent large reverse recovery losses from appearing in S3 and S4 due to the presence of their slow body diodes. With a switching frequency of 300 kHz, the practicality of ZCS for S3 and S4 is questionable due to potential reverse recovery losses in D1 and D2. The alternative is to switch all four bridge switches with zero voltage, with the penalty of increased tank circulating energy [56, 59].

The LCC tank components were selected based on the results in [59], with $Q_S = 2$, $C_n = 1.1$, and $\omega_n = 1.2$. The isolation transformer's turns ratio was selected as 4:1 (Np:Ns) to yield a reasonable duty cycle range for control of the bus voltage. Due to the nature of the voltage conversion ratio as a function of load for the LCC converter, the bus voltage must be closed-loop regulated (even with a fixed input voltage). The bus voltage is regulated at 42 Vrms, which, for a pure sinusoidal output yields a peak voltage of 59.4 V.

The SRR post-regulator design was accomplished by following the procedure outlined in [61]. As indicated in [61], higher values of Q for the series resonant network result in reduced bus current harmonics and increased power factor presented to the inverter, at the expense of higher resonant inductor and capacitor voltage stress and increased load transient response. Line and load regulation is accomplished through variable resonant inductor control [62, 63, 64]. Also, the transformer turns ratio for the post-regulators is indicated in Fig. 5.5(a).

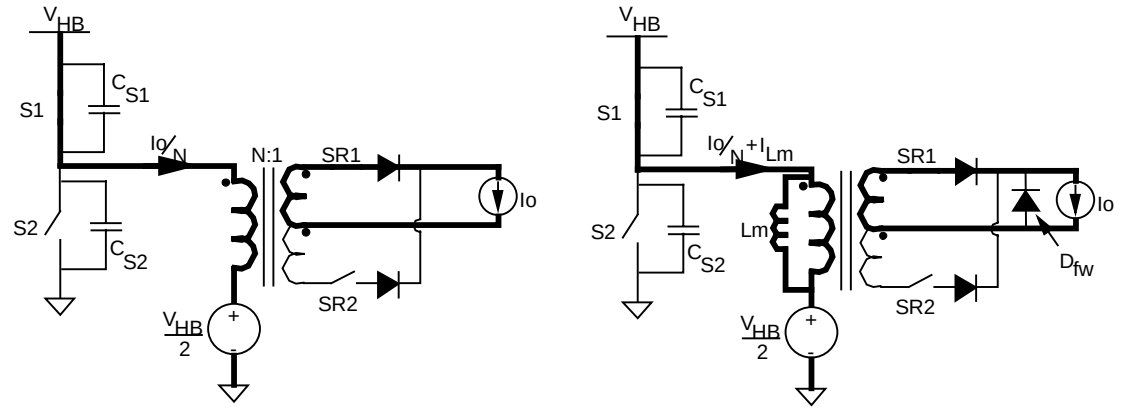
5.2.2.2 Square-wave power architecture design specifics

The square-wave power system, shown in Fig. 5.5(b), consists of a half-bridge (HB), ZVS inverter and magamp controlled, buck-derived post-regulators. The inverter is switched with constant duty cycle (ideally, slightly less than 50 %), and bus voltage regulation is achieved indirectly through the PFC boost converter's regulation of its 380

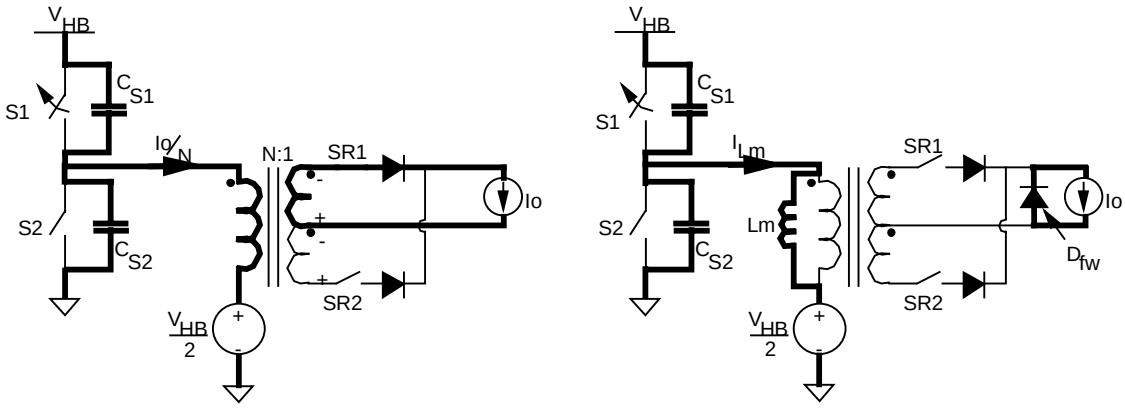
Vdc output. Experimental result indicate a typical steady-state variation of less that ± 5 % in the PFC converter's output voltage over the entire line and load range (at room temperature). Factoring in losses as a function of load for the HB inverter yields a steady-state bus voltage variation of less than ± 7 %, which is compensated for at the load by the magamp controlled post-regulators. This can be contrasted with the sinewave system, where a constant FB duty cycle "control" would result in a bus voltage variation range of almost 2:1 (entirely due to the 20 % to 100 % load range variation), placing a severe burden on the post-regulator designs.

Zero-voltage-switching of the HB inverter's two switches achieves two important goals; 1) controlling the bus voltage slew rates, and 2) reducing switching losses, which can be significant at 300 kHz. The importance of the first goal will be addressed later in this chapter. The mechanism for realizing ZVS is dependent on the configuration of the post-regulators, as shown in Fig. 5.6. The left-hand side equivalent circuits in Fig. 5.6 represent ZVS by utilizing reflected load current [37, 38]. Conversely, the right-hand side circuits represent ZVS by utilizing the HB isolation transformer's magnetizing inductance [35]. This is a similar concept to the FB ZVS mechanism described in Chapter 2. For the topological states shown in Fig. 5.6, the output inductor is idealized as a current source and the transformer's turns ratio, N:1, represents the total turns ratio from the post-regulator secondaries to the HB inverter primary (the power distribution bus is assumed ideal). Also, leakage inductance effects have been neglected.

Realizing ZVS through the reflected load current saves one diode (or, possibly a synchronous rectifier switch) in each post-regulator. It has the disadvantage of circulating reflected load current on the bus and in the inverter, but with a small duty cycle since the post-regulators are operated with very high duty cycles. In addition, with this ZVS method the bus voltage slew rate is more load dependent.



(a) S1 on, S2 off.



(b) S1 turns off.

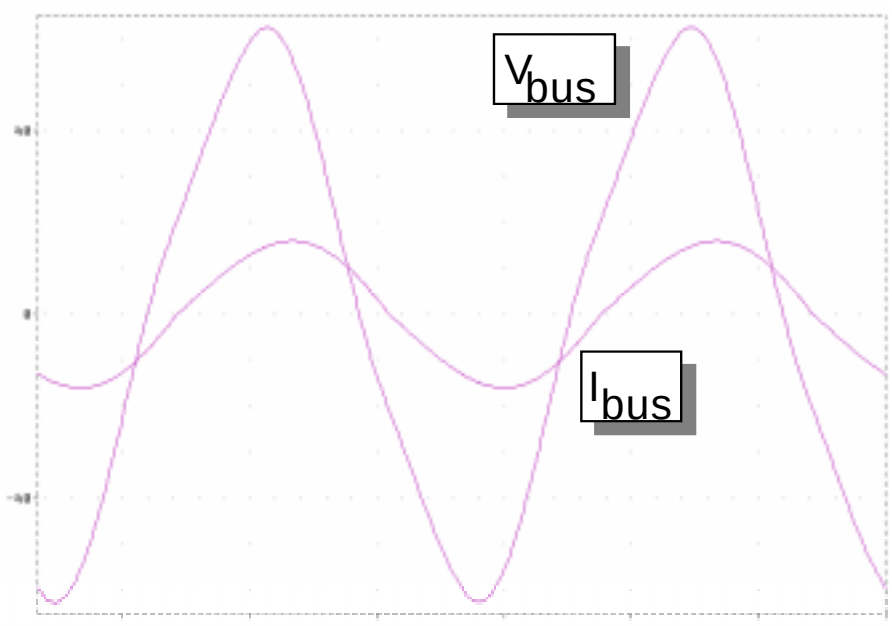
Fig. 5.6 HB ZVS mechanisms. Left side: through reflected load current; Right side: through magnetizing current.

5.2.3 Comparison results and conclusions

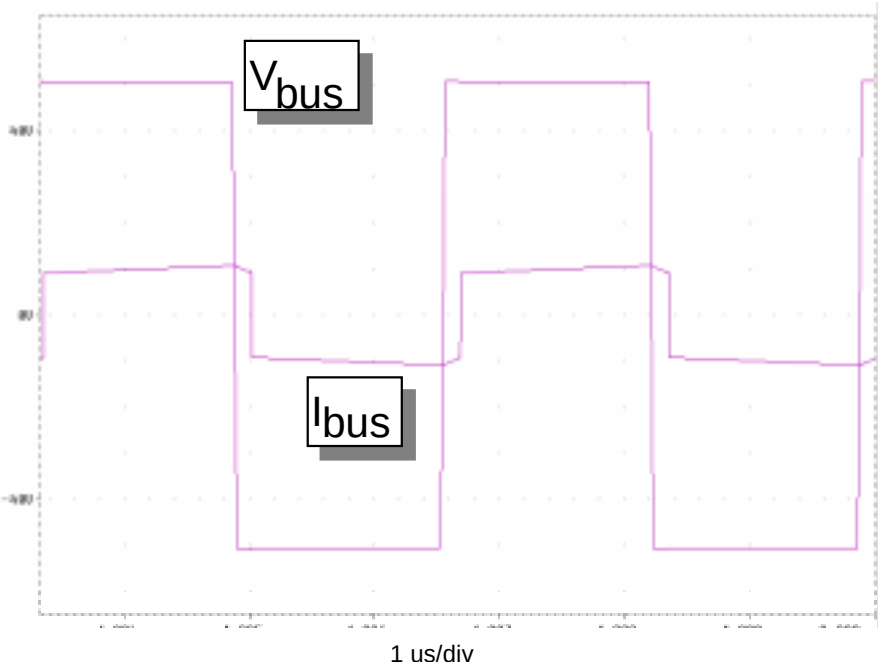
The comparison is based on the results from PSPICE [65] simulations of both power system architectures. Complete netlists for both simulations are given in Appendix B. Figure 5.7 shows the simulated bus voltage and current waveforms for each system, with both operating at maximum output power. Table 5.1 tabulates various operating parameters for each system, as determined from the simulations, each at maximum and minimum load. Several key conclusions can be drawn from the data presented in the table:

1) The sinewave FB LCC inverter overall losses as a function of load range will be higher than the square-wave HB inverter's, and not only because there are twice as many switches in the LCC inverter. Because of the necessity to realize low bus voltage THD in the face of a 20 % to 100 % load range, some amount of tank circulating energy is required. As can be seen in the table, S1's rms current in the sinewave case is 2.62 times higher at light load than it is for the square wave design. This translates to an increased power dissipation for this component of 6.87 times over the same component in the square-wave design, with both operating at minimum load. Therefore, in addition to being a more complex design than the square-wave inverter, the efficiency of the sinewave inverter will be less as well.

2) RMS bus currents are higher in the sinewave case as compared to the square wave case, resulting in about a 25 % increase in power dissipated in the bus, the secondary of the inverter isolation transformer, and the primaries of the post-regulator transformers (assuming the transformer resistances are the same for both designs).



(a) Sinewave topology bus voltage and current.



(b) Square-wave topology bus voltage and current.

Fig. 5.7 Simulated ideal sinewave and square-wave topology bus waveforms. Po = 400 W.

Table 5.1 Operating characteristics of sine and square wave AC DPS topologies.

Sinewave DPS			***Square-wave DPS***		
	max load, 403.2 W	**min load, 79.8 W**		**max load, 399.6 W**	**min load, 79.8 W**
RMS tank current	2.57 A	1.33 A			
S1 rms current	1.82 A	0.928 A	S1 rms current	1.905 A	0.413 A
S2 rms current	1.80 A	0.933 A	S2 rms current	1.9 A	0.413 A
S3 rms current	1.82 A	0.943 A			
S4 rms current	1.81 A	0.989 A			
Iso XFMR Lm	1 mH		Iso XFMR Lm	879 μH	
Cs peak voltage	412.8 V	226.8 V			
Cp peak voltage	249.5 V	234.5 V			
Tank D	0.418	0.249	S1, S2 D	0.458	0.458
pp bus voltage	124.8 V	117.8 V	pp bus voltage	101.3 V	101.3 V
RMS bus voltage	42 V	42.1 V	RMS bus voltage	50.35 V	49.5 V
Bus voltage THD	7.71 %	5.23 %			
pp bus current	31.9 A	6.78 A	pp bus current	21.6 A	5.61 A
RMS bus current	11.2 A	2.28 A	RMS bus current	10 A	2.06 A
Bus current THD	3.95 %	12.1 %			
SRR PF	0.904 (ind)	0.87 (ind)			
SRR L value	31.1 μH	40 μH	Post-regulator (P/R) effective D	0.902	0.875
SRR rectifier peak current	32 A		P/R rectifier peak current	21.5 A	
SRR output cap RMS current	9.83 A		P/R output cap rms current	0.955 A	

3) The peak and RMS currents in the SRR secondaries are considerably higher than for the square-wave post-regulators. In particular, output capacitor RMS currents are almost an order of magnitude greater in the SRR designs. As can be seen in Fig. 5.5(a), this results in a order of magnitude increase in the value of output capacitance required for the SRR designs. Also, the values shown are based on the use of ideal capacitors - including ESR and ESL effects will result in an even greater disparity between the sine and square-wave post-regulator designs.

Tables 5.2 and 5.3 present the results of a crude piece-parts cost analysis for the two power system architectures. From the tables it can be seen that the square-wave system has about a 40 % reduction in parts costs over the sinewave system.

The fundamental conclusion that can be drawn from this comparison of the two systems is that, from both a technical and economic perspective, the stipulation of the need for low bus voltage and current harmonic distortion sacrifices overall system efficiency, complexity, and cost. The perceived need for low bus waveform THD has its roots in the (unknown) potential system noise effects brought about by the bussing of HF AC waveforms throughout the host electronic system. Limiting the harmonic content of such waveforms certainly would reduce their effects, but as has been demonstrated, the overall power system architecture suffers. This is not meant to imply that an AC DPS employing sinusoidal bus waveforms should not ever be considered. For systems where the transmission dimensions are significant (e.g., the international space station [21, 22, 23, 24, 25, 26]) a sinewave AC DPS may be preferred. The inverter design described in [59] was intended for sending a 20 kHz, 100 W, 28 Vrms sinewave over a distance of several meters. In such instances, the use of squarewave bus waveforms (especially waveforms with frequencies on the order of several hundred kilohertz) is probably not appropriate. However, in cost sensitive, "short distance" applications, such as for the PC/workstation/server computer systems being considered here, sinusoidal AC DPSs are at a distinct disadvantage when compared with square-wave AC DPSs. Therefore, the

Table 5.2 Piece-parts costs for sine and square-wave topology inverters.

	Sine-wave	*Cost**	*Square-wave*	*Cost**
Transistors	**4 x IRFP460**	$5.78 ea	**2 x IRFP460**	$5.78 ea
Diodes	**2 x HFA08TB60**	$1.41 ea		
	2 x 6CTQ035	$1.55 ea		
Capacitors	**4510 pF, 500V**	$0.31		
	4960 pF, 300V	$0.29		
	2 x 0.47μF HF, 400V	$1.22 ea	**2 x 1 μF HF, 250V**	$1.77 ea
Magnetics	**Iso transformer**	$2.00	**Iso transformer**	$2.00
	2 x gate drv xfmr	$0.25 ea	**Gate drive xfmr**	$0.25
	Resonant L	$1.00		
Bus Reg Circuit	**ϕ-shift controller IC (UC3879?)**	$1.50		
	LM385 ref	$1.00		
	4N26 Optoisolator	$0.34		
	LM358 dual op-amp	$0.45		
Driver Circuit	**4 x TC4426 MOSFET driver**	$1.35 ea	**2 x TC4426 MOSFET driver**	$1.35 ea
			LM555	$0.24
			74AC74 Flip Flop	$0.51
Total Cost		**$44.27**		**$20.80**

*Based on quantity 100 piece price from Digi-Key Corporation's July-September, 1998 catalog (except for magnetic components).

Table 5.3 Piece-parts costs for sine and square-wave topology post-regulators.

	Sine wave	*Cost**	*Square wave*	*Cost**
Diodes	**40CPQ035**	$3.62	**32CTQ030**	$1.55
Capacitors	**0.014 μF, 200V**	$0.31		
	3 x 330 μF OS-CON, 6.3V	$1.20 ea	**68 μF OS-CON, 6.3V**	$0.79
Magnetics	**Transformer**	$1.50	**Transformer**	$1.50
	Resonant L	$1.00		
			Output L	$0.50
			2 x magamp	$1.38 ea
Output Reg Circuit		$2.50 (total)		$2.50 (total)
	4N26 Optoisolator	$0.34		
Total Cost		**$12.87**		**$9.60**

*Based on quantity 100 piece price from Digi-Key Corporation's July-September, 1998 catalog (except for magnetic components). OS-CON capacitor prices based on quantity 1000 pieces.

remainder of this chapter will be devoted to addressing the issues of induced system and radiated noise under the assumption the power system architecture is a square-wave type.

5.3 System Noise and Distribution Issues

5.3.1 Introduction and problem approach

This section attempts to answer the following fundamental question:

"What is the magnitude of the effects of crosstalk and radiated "noise" using square-wave bus voltage and current waveforms and can their effects be controlled while still maintaining the topological simplicity afforded by a square-wave AC DPS?"

The power system electrical design specifications are identical to those given at the beginning of Section 5.2.2. An additional mechanical "constraint" being imposed is that the power distribution bus structures are limited to PCB type implementations with dimensions and interlayer spacings on the order of those shown in Figs. 5.2 and 5.3.

Figure 5.8 shows the procedure that will be followed in order to attempt to answer the above question. Beginning with a baseline PCB bus structure and appropriately located signal traces, the application of finite element analysis (FEA) techniques [66] to the structure results in a lumped component network which accurately describes, at the frequencies of interest, the parasitic electric and magnetic field coupling of the bus structure to the signal traces. Also generated are the bus and signal trace self impedances (e.g., self inductance and trace resistance). The bus/signal trace network is then "plugged into" a PSPICE simulation which already includes models for both the FE inverter and the post-regulators. Detailed netlists are included in Appendix C. The results of the PSPICE simulation are then evaluated, and if desired, are verified against experimental results. The bus structure design can then be modified, and the entire process repeated. A by-product of the FEA outputs is theoretical magnetic field data.

In order to verify the theoretical analysis, an experimental "test bed" is used. One of the key functions of the test bed is to provide a platform where it is relatively easy to mimic a variety of PCB bus structures while maintaining the same FE and post-regulator configurations. This is accomplished by tightly sandwiching layers of the appropriate thickness copper (Cu) foil and insulator between two copper-clad vector boards. Figure 5.9 illustrates a simplified view of the system's physical setup. The total power distribution bus dimensions are maintained at a constant length of 8" and width of 2". The logic traces are located on the layer immediately above the uppermost bus layer, and run down the length of the as shown in the top view of Fig. 5.9. The bus structure depicted in Fig. 5.9 is a simple parallel-plate structure, and more complicated bus structures are created as necessary. However, the location of the logic traces relative to the overall dimensions of the bus remains constant.

The front-end is located at the opposite end of the bus from the post-regulators, as shown in Fig. 5.10. The logic traces are sourced and terminated with actual logic gates, as shown in the figure. The logic integrated circuits are powered from a battery, and an isolated, high-bandwidth differential probe (Tektronix P5205) is used to measure the effects of the square-wave bus waveforms on the induced noise into the logic traces (as measured at the input of U2). Although the system design specifications call for a maximum power output of 400 W, only two post-regulators, each with a 50 W maximum output, were constructed. However, all the essential operating details of the power system are able to be verified.

Figure 5.11 shows the simplified schematic of the experimental AC DPS, less the PFC boost converter. This is essentially the same design as was used for the sinewave/square-wave topology comparison carried out in Section 5.2. C_{S1} and C_{S2} are utilized to control the bus voltage slew rates and bus voltage regulation is maintained indirectly by the PFC converters' voltage loop.

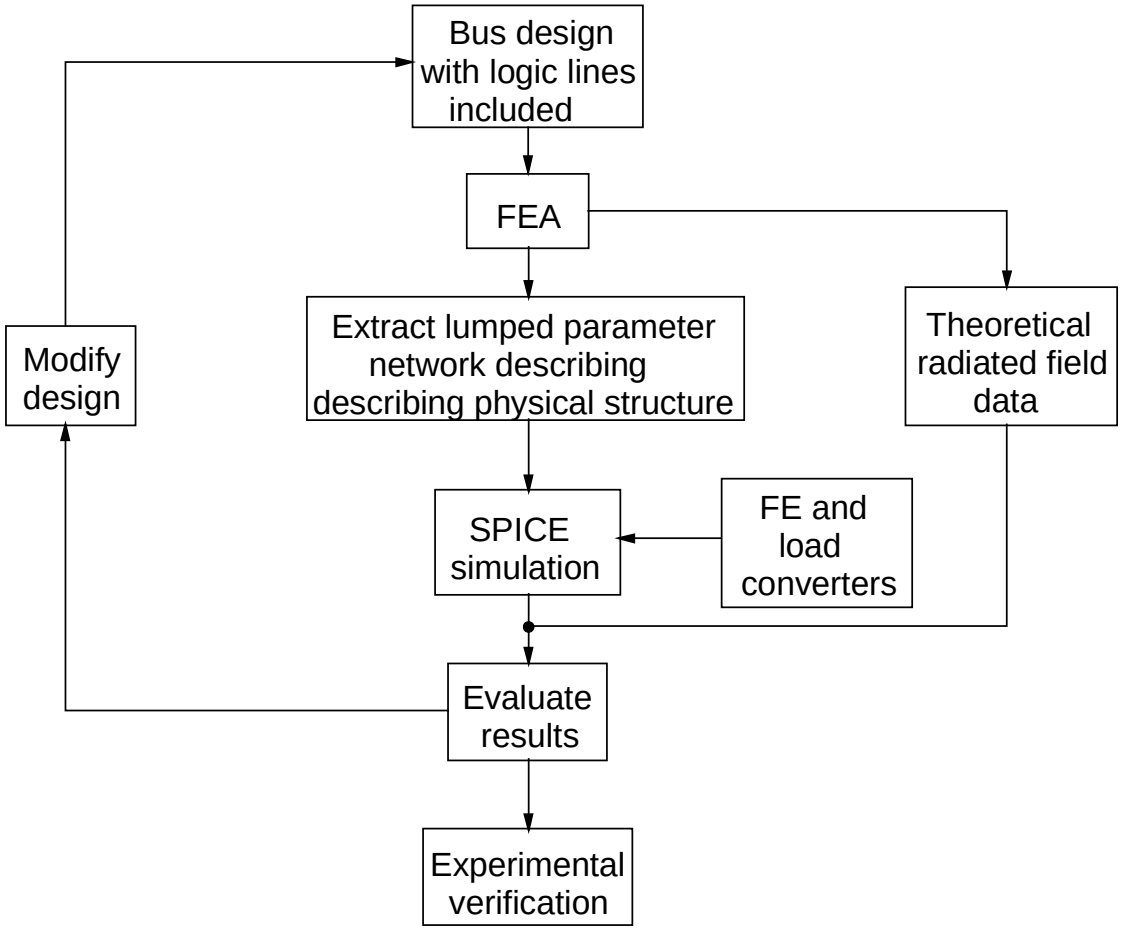


Fig. 5.8 Crosstalk/radiated noise analysis flowchart.

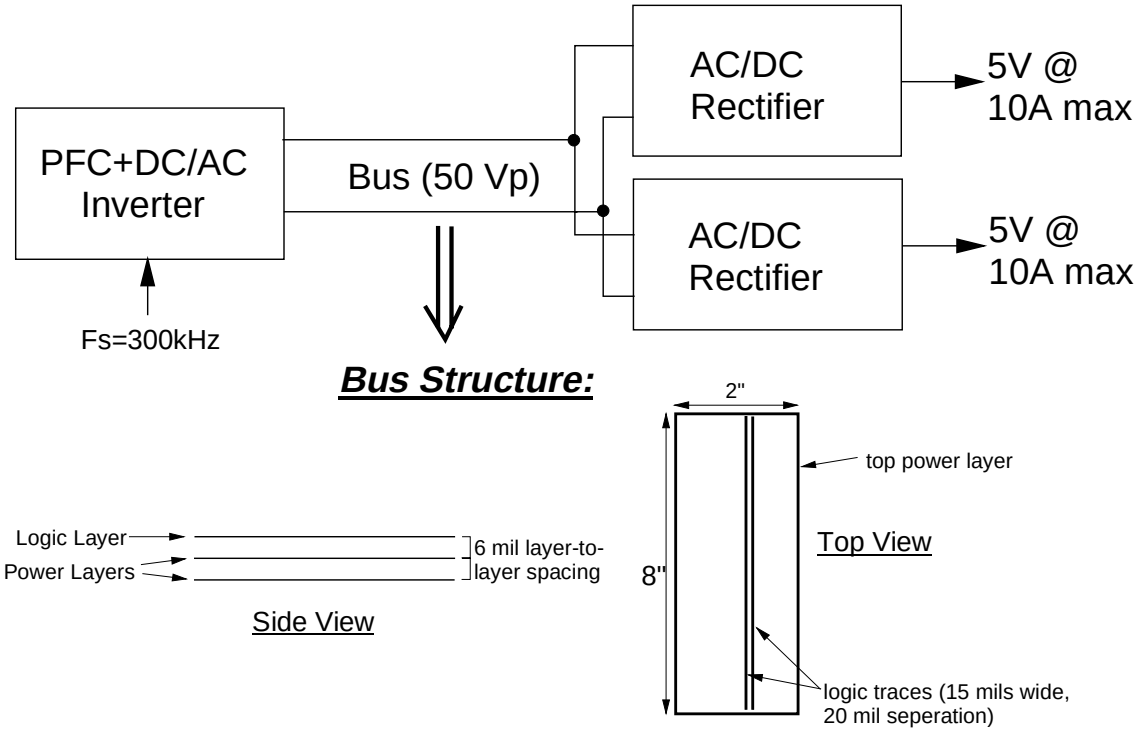


Fig. 5.9 Experimental verification test bed physical setup.

5.3.2 Printed-circuit board bus structure design

There are two basic qualitative properties any "good" bus structure design should possess: 1) low inductance, and 2) good copper utilization. These two items are not really independent, but low inductance also implies the structure has a small loop area. Small loop areas are desirable from the perspective that the strength of external (to the structure) magnetic fields generated by the bus currents are decreased. Good Cu utilization implies that HF losses in the bus structure are manageable. For reference, the skin depth of Cu at 300 kHz is 4.74 mils, and a frequency of 3.44 MHz is required for the thickness of 1 oz. Cu to be equal to one skin depth.

5.3.2.1 Performance of a simple "parallel-plate" (2 layer) PCB bus structure

As a starting point, probably the simplest PCB bus structure that can be concocted to potentially meet the above criteria is a parallel plate design, shown, along with the logic traces, in Fig. 5.12. The layer-to-layer spacing is 6 mils, with 1 oz. Cu being used for the bus conductors and 1/2 oz. Cu being used for the logic traces. From the figure it is easy to envision that tight coupling must exist between the power plane and the logic traces, due primarily to their extremely close physical proximity. The results from FEA of the structure confirms this suspicion, as shown in Fig. 5.13. The matrices shown in Fig. 5.13 are used to generate the values for the various circuit elements shown in the structure's lumped parameter schematic. The elements in the matrix of inductive coupling coefficients are defined as

$$k_{ij} = \frac{L_{ij}}{\sqrt{L_{ii} L_{jj}}}. \tag{5.5}$$

The values of the capacitances between the various conductors are given by the absolute values of the off-diagonal terms in the capacitance matrix.

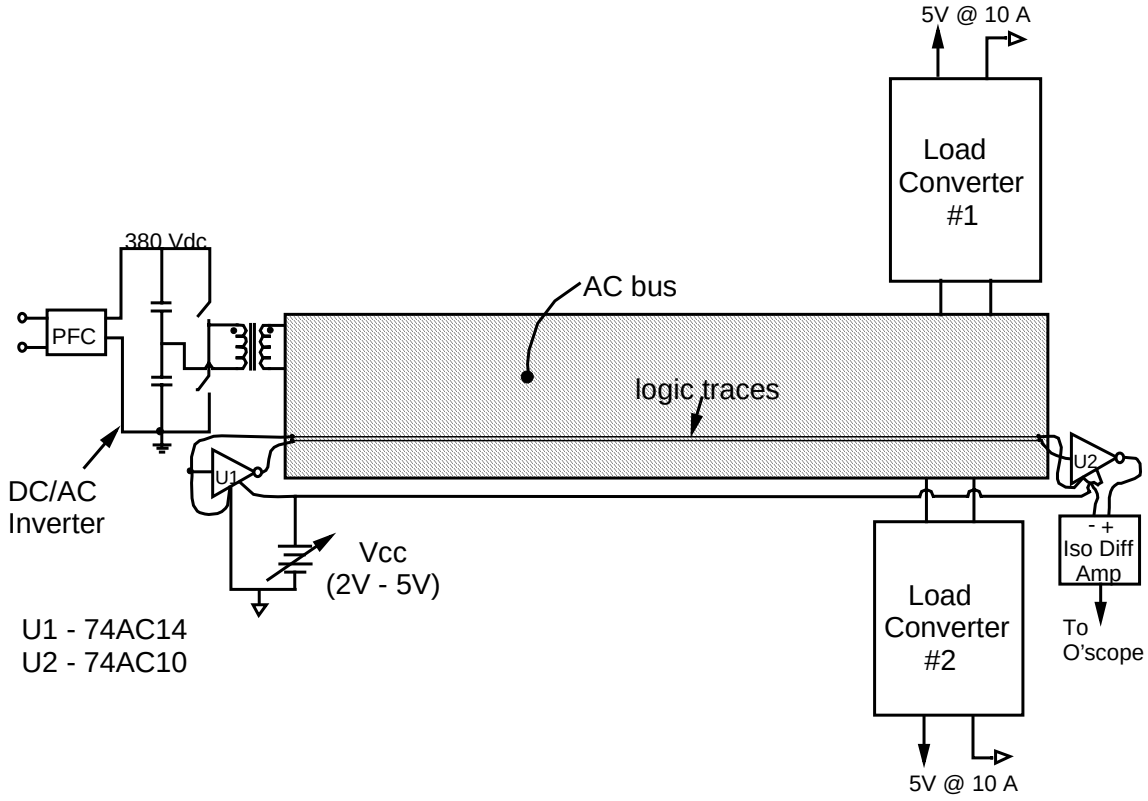


Fig. 5.10 Experimental verification test bed electrical setup.

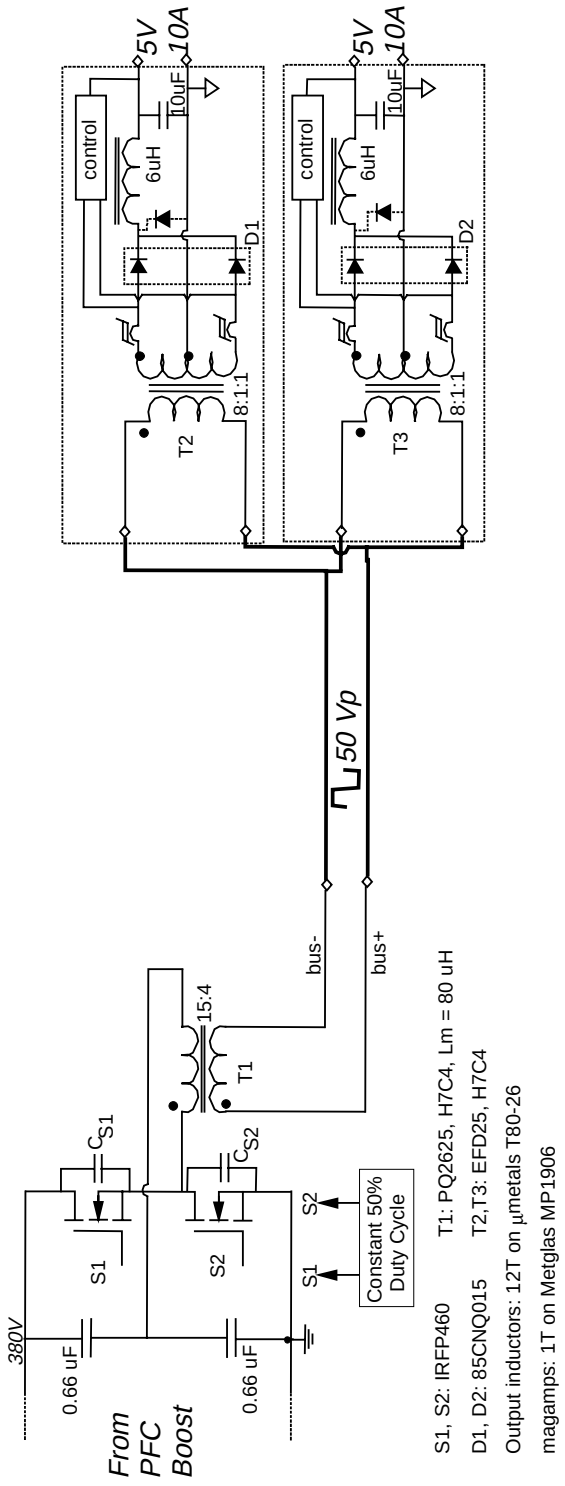


Fig. 5.11 Simplified experimental AC DPS schematic.

From the FEA results it can be seen that the parallel-plate structure results in very low bus inductance (on the order of a few nanohenries) and very high bus capacitance (≈ 2600 pF). Theoretical and experimental results of the induced logic noise for this structure are shown in Fig. 5.14. This data is taken under the following operating conditions: Vin = 110 Vac, Po = 75 W (split evenly between the two post-regulators), bus voltage rise/fall times ≈ 65 ns, and Vcc = 2 Vdc. There is excellent agreement between theory and experiment, however, the performance is clearly unacceptable. At the point of each bus voltage transition a large "spike," obviously capable of causing a change in the receiver's output state, is induced on the input of the receiver logic gate. Figure 5.15 shows the primary mechanism through which the logic noise is induced. Although C13 and C23 are nearly identical in value, the fact that logic return and bus- have no *AC* potential between them (simply indicated by a common ground connection in Fig. 5.15) effectively shorts out C23. During a bus voltage transition, current is injected through C13 and returns via the logic return/bus- connection to its source. Since Rs << |Zin| the resulting noise voltage appearing at the logic receiver's input is given by:

$$\Delta V_{logic} \approx \left(C_{13} \frac{dV_{bus+}}{dt} \right) R_S \tag{5.6}$$

5.3.2.2 Investigation into solutions to the induced logic noise problem

This sections describes potential solutions to the induced logic noise problem. In order of increasing solution complexity, they are:

1) Decrease Rs to decrease ΔV_{logic}, which would require logic circuit modifications.

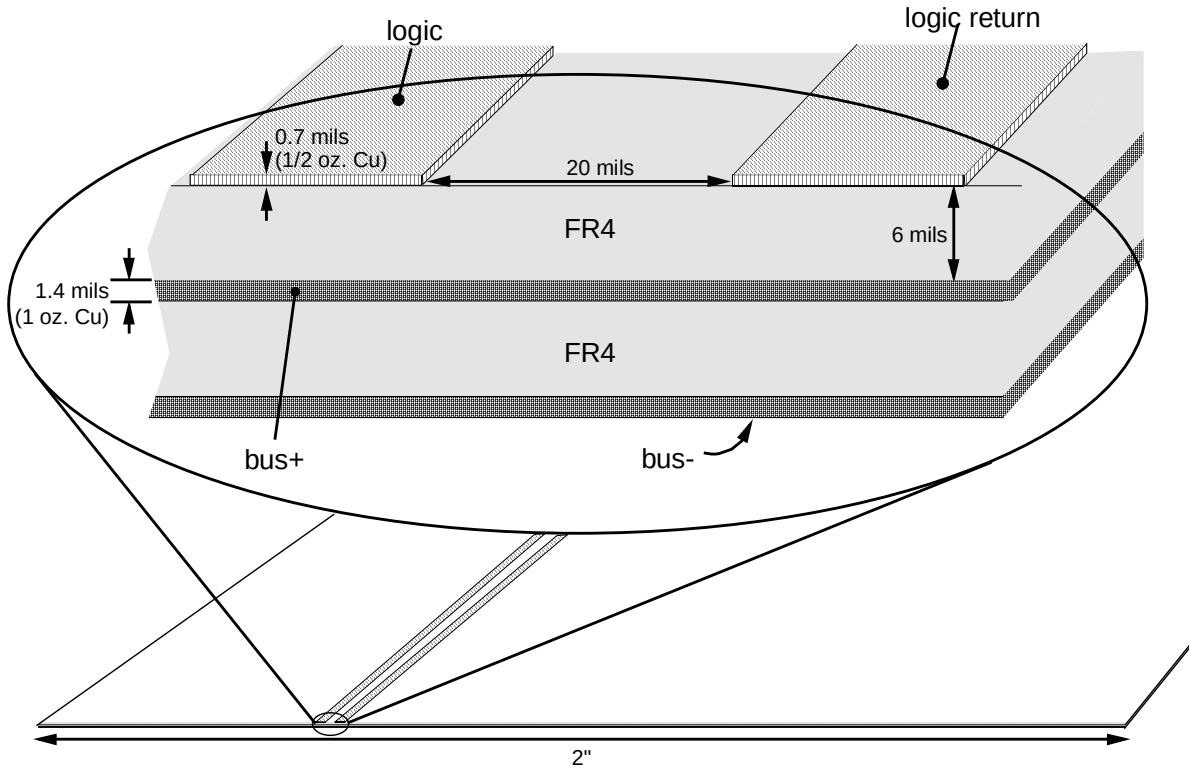
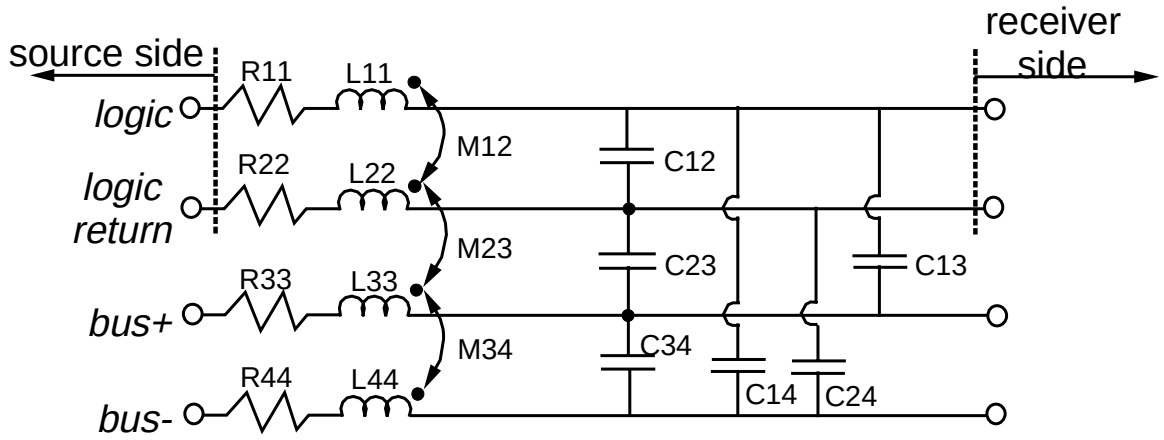


Fig. 5.12 End-view of the parallel-plate PCB bus structure

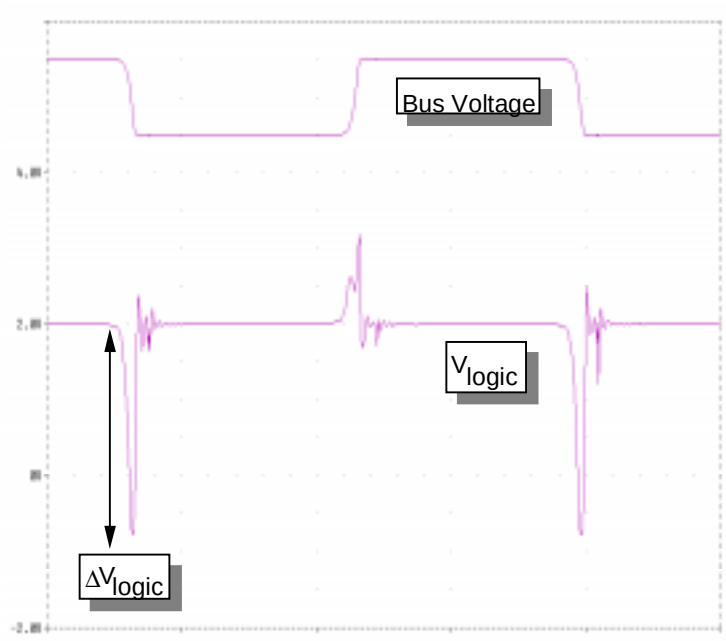


$$L_{ij} = \begin{bmatrix} 1.564 & 1.269 & 1.252 & 1.25 \\ & 1.577 & 1.252 & 1.25 \\ & & 1.253 & 1.251 \\ & & & 1.253 \end{bmatrix} \mu H/m \qquad k_{ij} = \begin{bmatrix} 1 & 0.808 & 0.894 & 0.893 \\ & 1 & 0.891 & 0.889 \\ & & 1 & 0.998 \\ & & & 1 \end{bmatrix}$$

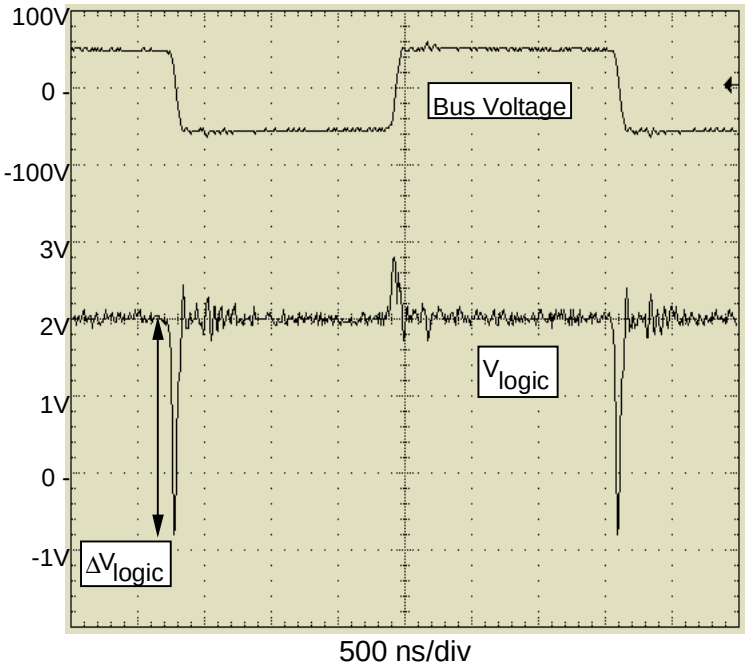
$$C_{ij} = \begin{bmatrix} 151.9 & -2.23 & -149.6 & -0.0853 \\ & 151.9 & -149.6 & -0.0819 \\ & & 13108 & -12809 \\ & & & 12809 \end{bmatrix} pF/m$$

$$R_{ij} = \begin{bmatrix} 2.711 & & & \\ & 2.716 & & \\ & & 0.01368 & \\ & & & 0.01368 \end{bmatrix} \Omega/m$$

Fig. 5.13 Results of FEA analysis on parallel plate PCB bus structure.



(a) Theoretical.



(b) Experimental.

Fig. 5.14 Induced noise into logic line for 2 layer PCB bus structure.

2) Increase the bus voltage rise/fall times, requiring circuit modifications in the inverter.

3) Fix the AC potential present between bus+ and the logic traces (i.e., add a shield). This requires PCB bus structure modifications.

4) Inject equal, opposite, and simultaneous "noise" currents through C13 and C23. This would require both bus structure and circuit modifications.

5.3.2.2.1 Decreasing Rs

Since the magnitude of the induced logic noise is directly proportional to the logic output's source resistance, decreasing its value will reduce the noise level. For CMOS logic, the $R_{DS,on}$ of the MOSFETs that comprise their complementary output stage decreases with increasing supply voltage. This is illustrated in Fig. 5.16(a). By increasing Vcc from 2 Vdc to 5 Vdc, the induced logic noise decreases dramatically, as shown in Fig 5.16(b) and (c). As an aside, the fact that the noise levels change as a function of the logic line terminating impedance verifies the idea that the coupling mechanism is predominately due to stray electric fields [53].

Although the improvement is substantial by increasing Vcc, this solution is probably not terribly practical from an overall computer system design point of view.

5.3.2.2.2 Increasing bus voltage rise and fall times

The induced logic noise is also directly proportional to the bus voltage slew rate. As discussed previously, the ZVS HB inverter used in this design provides a convenient method for modifying the bus voltage transition times. The effects of slowing the transition times is shown in Fig. 5.17. By increasing the rise and fall times from 65 ns to about 190 ns results in a significant decrease in the amplitude of the induced logic noise "pulse." Although the performance is still not good enough, increasing bus voltage rise/fall times will be shown to have benefits other than simply decreasing the induced logic noise levels. In addition, combining the concept of increased bus voltage transition times with modified PCB bus structures will be shown to be very effective as well.

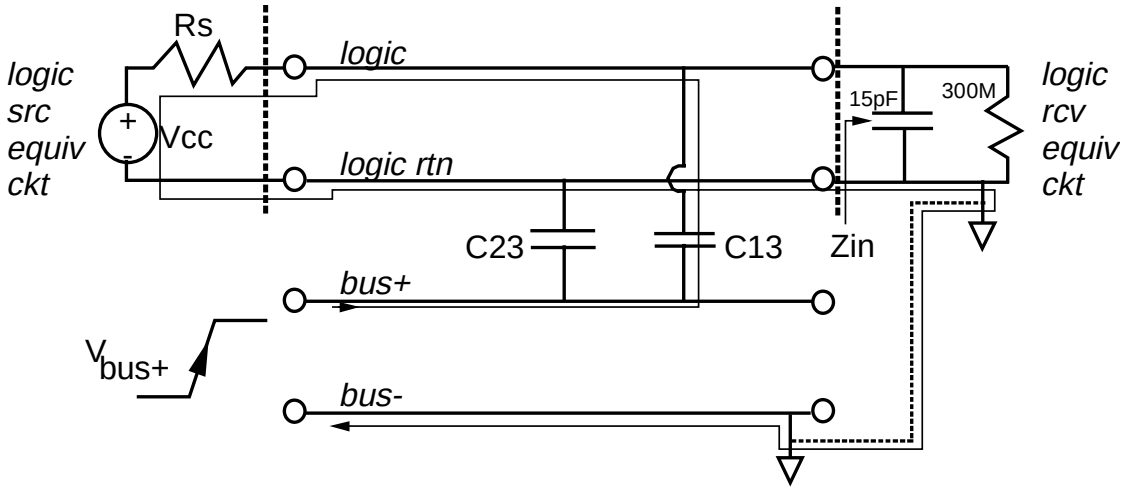
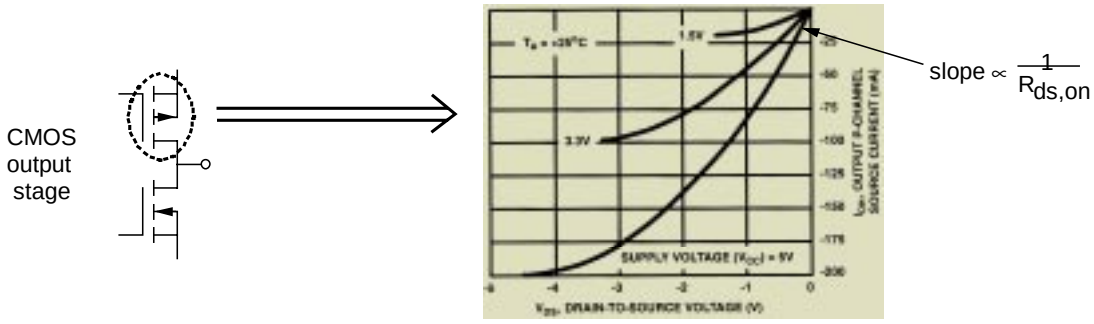
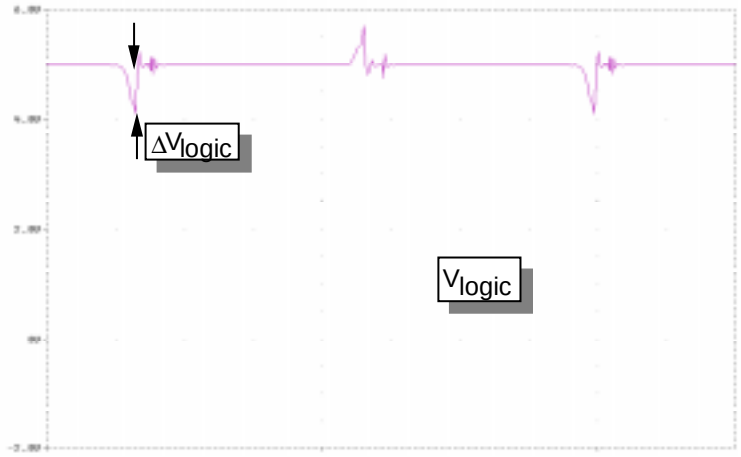


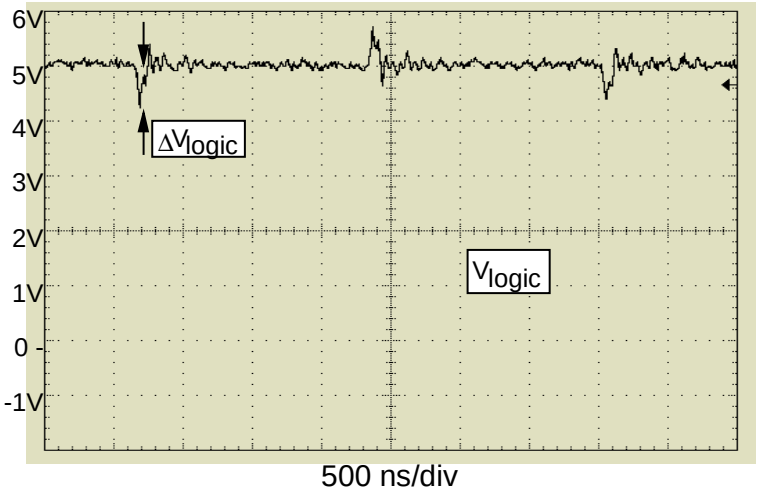
Fig. 5.15 Equivalent circuit for induced logic noise mechanism.



(a) CMOS logic $R_{DS,on}$ as a function of supply voltage.

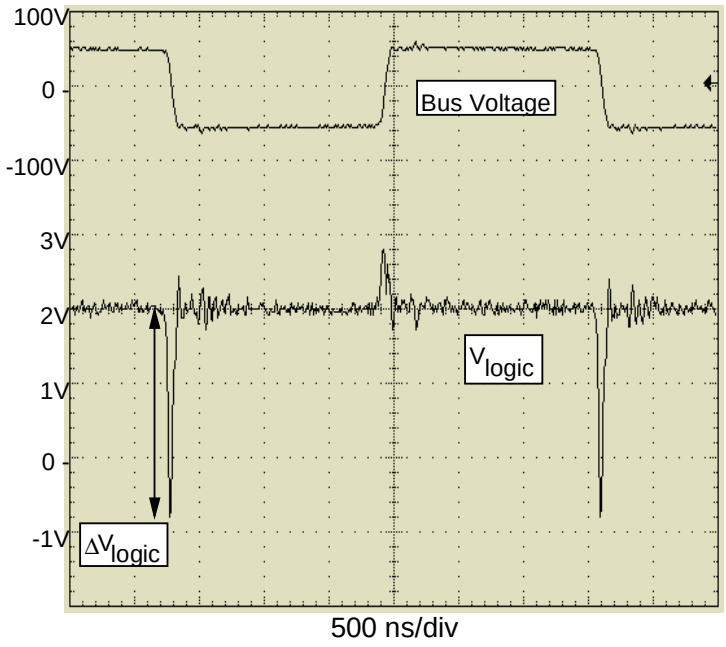


(b) Theoretical induced logic noise.

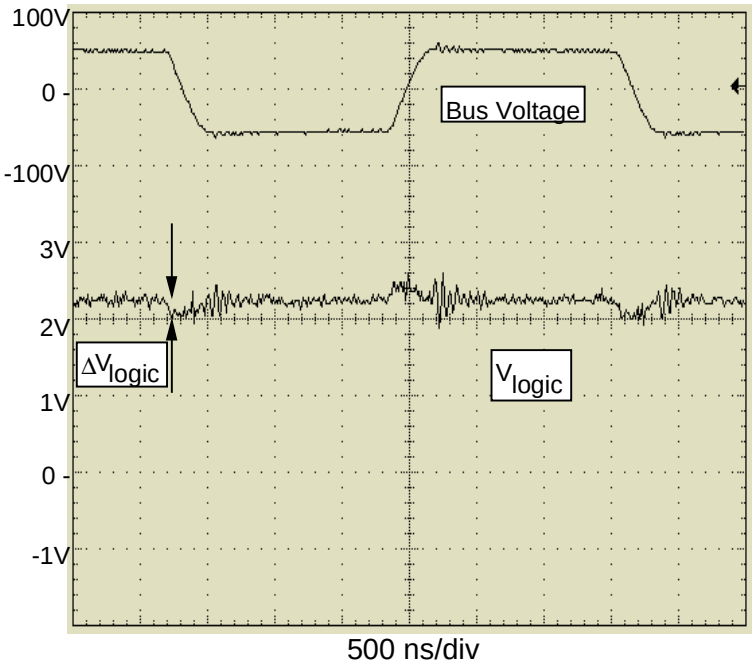


(c) Experimental induced logic noise.

Fig. 5.16 Induced logic noise as a function of supply voltage.



(a) $t_r/t_f \approx 65$ ns.



(b) $t_r/t_f \approx 190$ ns.

Fig. 5.17 Induced logic noise for different bus voltage rise and fall times.

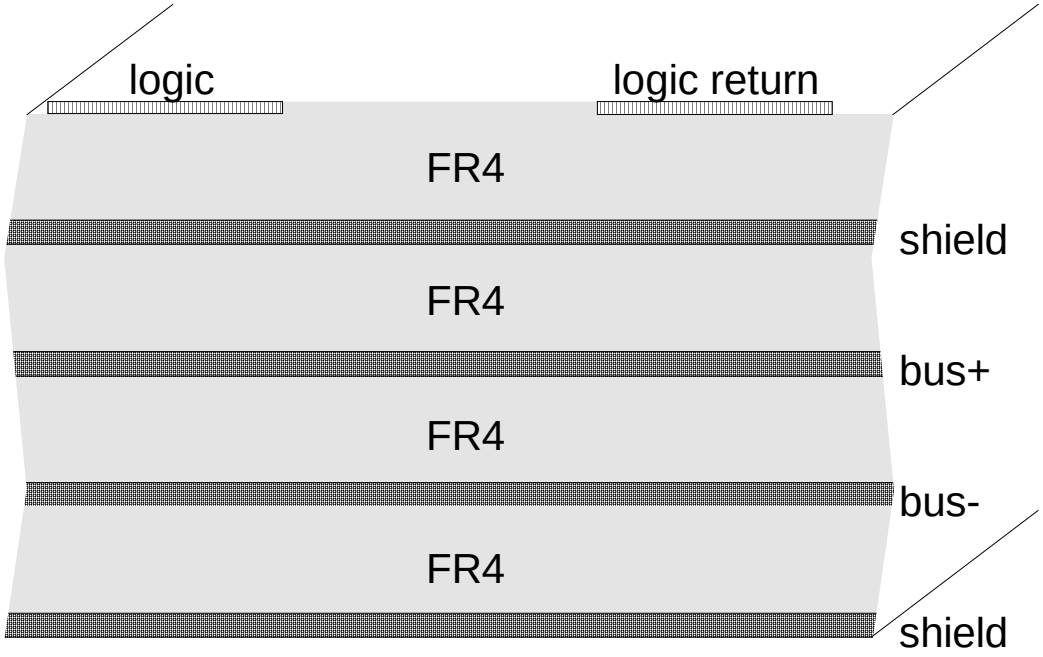
5.3.2.2.3 Two layer PCB bus structure with shield layers

In order to provide a "fixed" potential between the bus itself and the logic traces, shield layers can be added, as shown in Fig. 5.18(a). Figure 5.18(b) shows the equivalent lumped parameter network, with element values being given in Appendix C. The shield layers are tied to the same potential as the logic return trace, and, as before, it is assumed there is no AC potential difference between the bus- layer and logic return. The theoretical and experimental results for this bus structure are given in Fig. 5.19. Induced logic noise performance is the best yet, however, problems arise when consideration is given to the currents circulating in the shield, as indicated in the waveforms shown in Fig. 5.20. Again, there is excellent agreement between theory and experiment, providing ample validation for the accuracy of the analysis procedures, but significant pulses of shield current flow during bus voltage transitions. The shield currents arise from capacitive coupling from the bus+ layer to the shield layer immediately above it. The resulting current that flows through this capacitance during a bus voltage transition returns to its source through the common (AC) connection between the shield and bus- layers. Slowing the bus voltage slew rates improves the situation (see Fig. 5.21), but does not address the fundamental problem. There are three potential ramifications due to the presence of the shield currents:

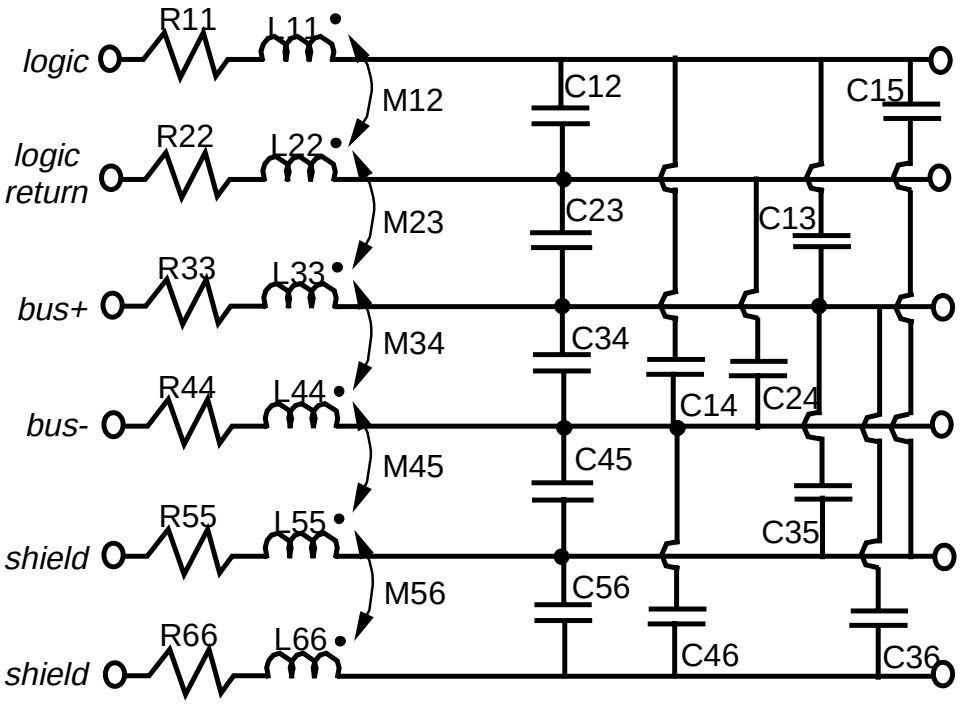
1) Because the shield currents return to their source through the bus- conductor, the bus+ and bus- currents are no longer equal and opposite down the length of the bus, resulting in an increased external (to the bus structure) magnetic field.

2) High shield current di/dt will tend to couple noise into adjacent circuitry through mutual inductive coupling.

3) Also, high shield current di/dt will cause noise voltage to appears along the shield due to the shield's non-zero impedance. The noise voltage typically manifests itself as common-mode radiation [53].

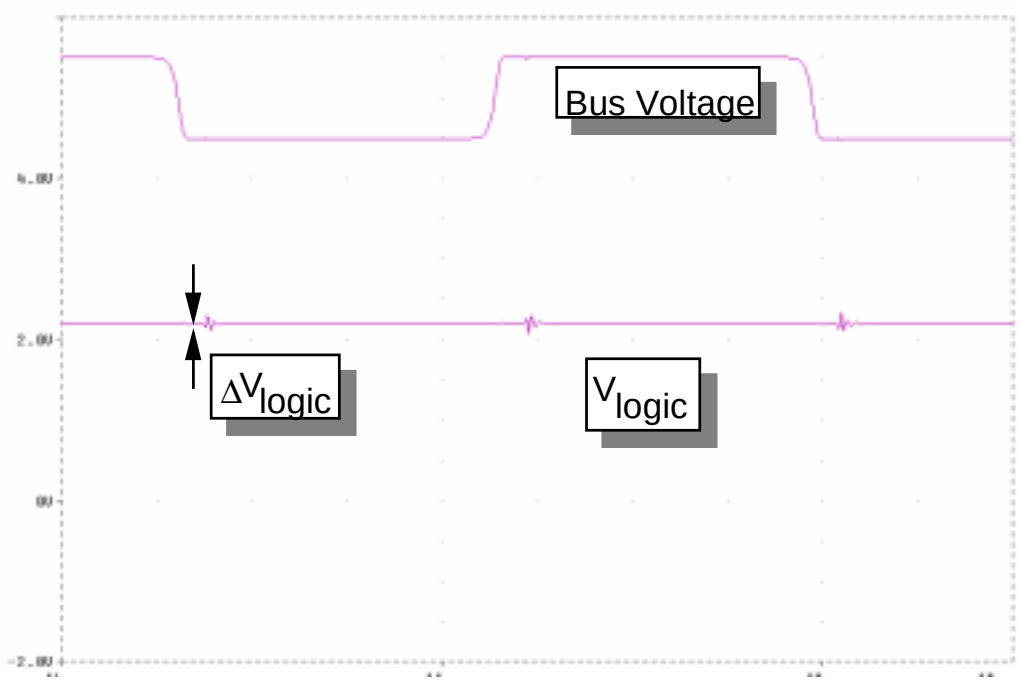


(a) End view.

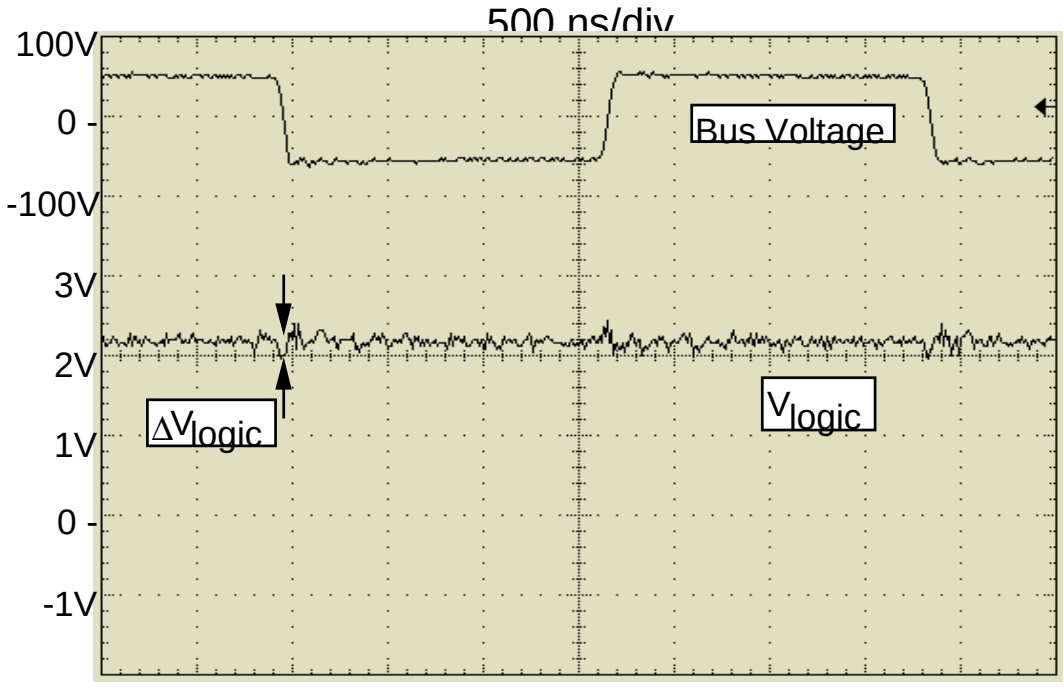


(b) Lumped parameter network.

Fig. 5.18 2 layer with 2 shield layers PCB bus structure.

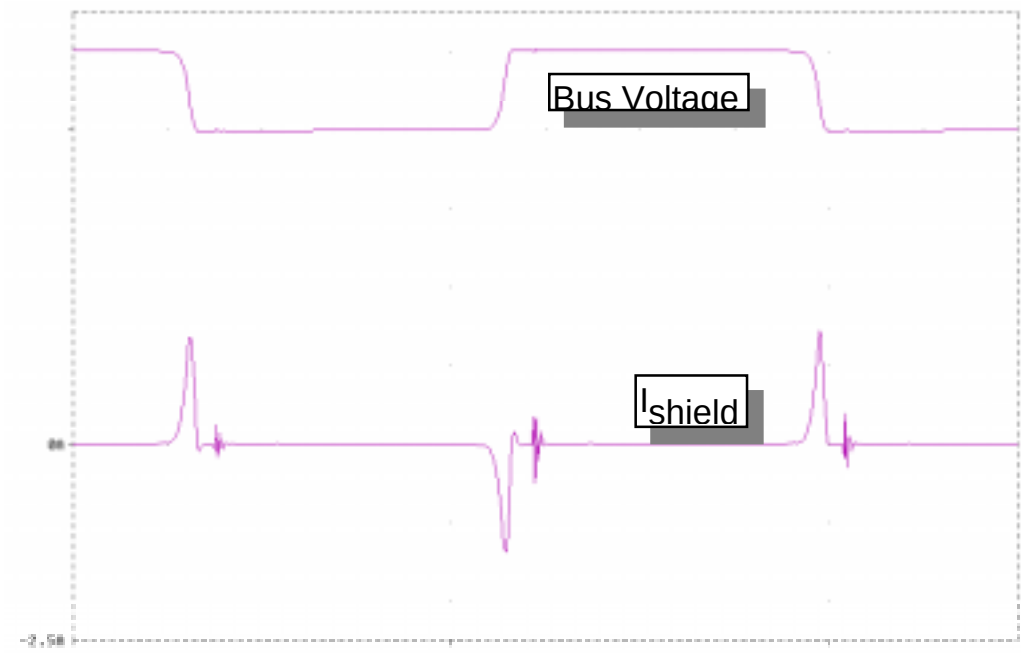


(a) Theoretical.

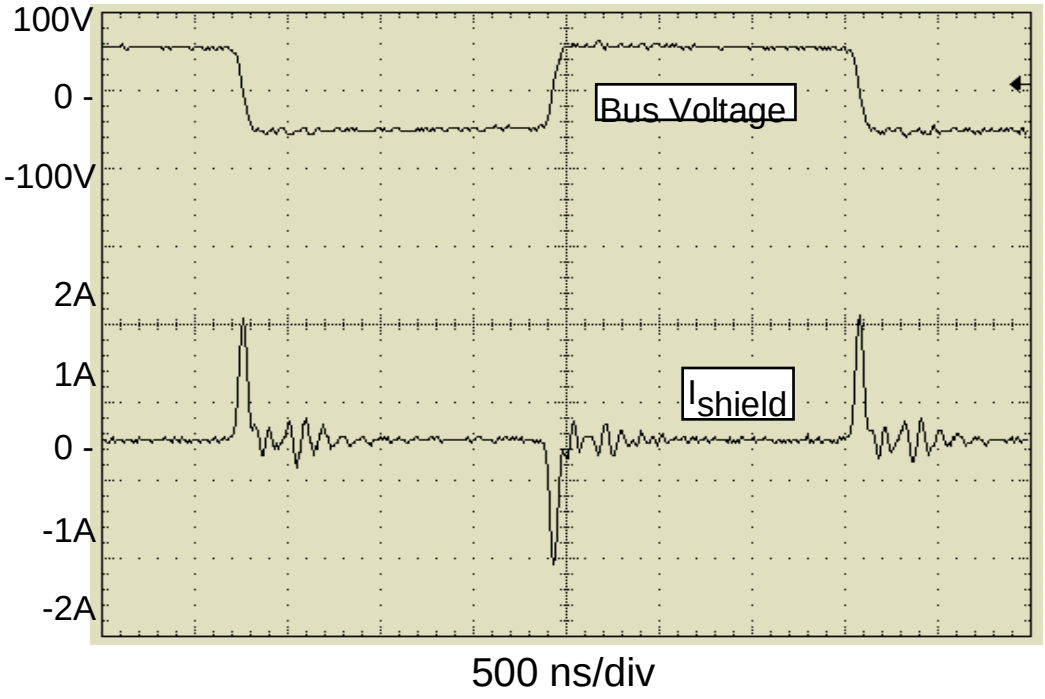


(b) Experimental.

Fig. 5.19 Induced logic noise for 2 layer with shield PCB bus structure.

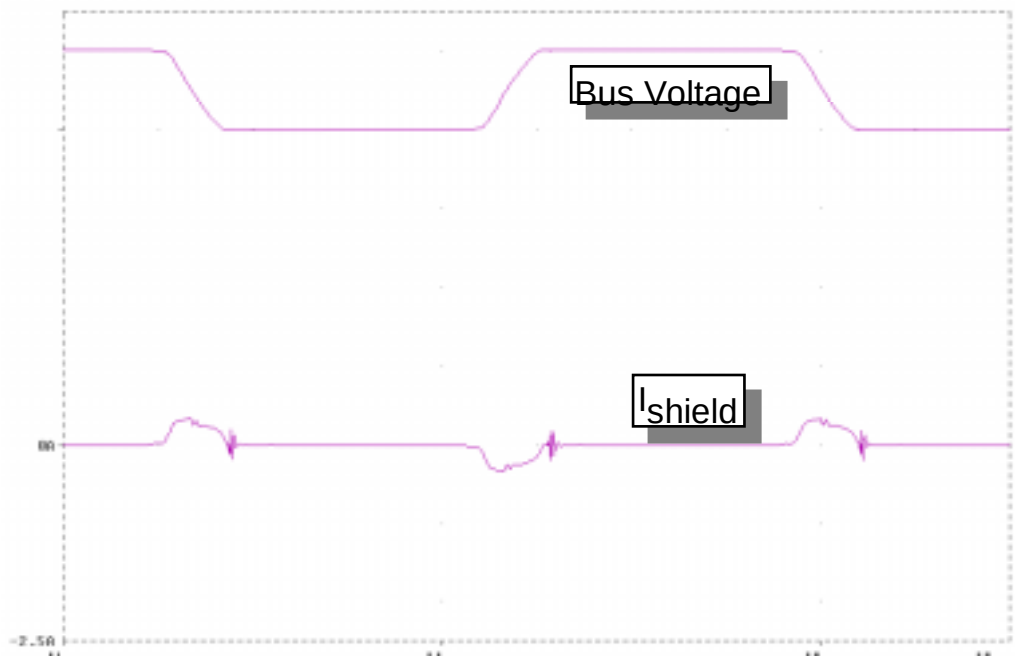


(a) Theoretical.

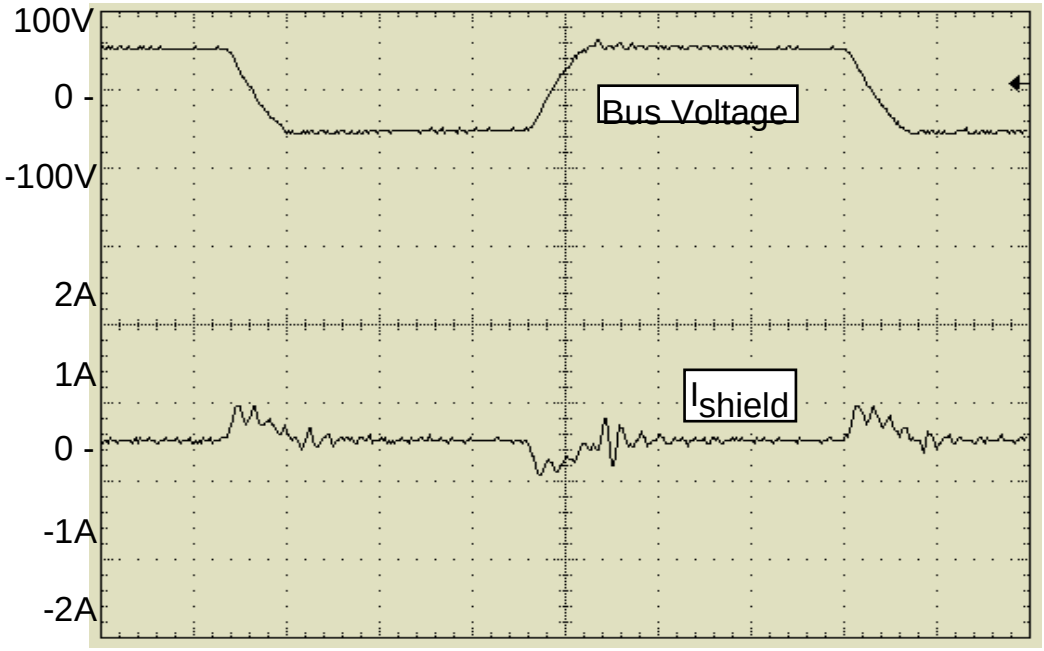


(b) Experimental.

Fig. 5.20 Shield currents for the 2 layer w/shield structure. Bus voltage $t_r/t_f \approx 65$ ns.



(a) Theoretical.



(b) Experimental.

Fig. 5.21 Shield currents for the 2 lyr w/shield structure. Bus voltage $t_r/t_f \approx$ 220 ns.

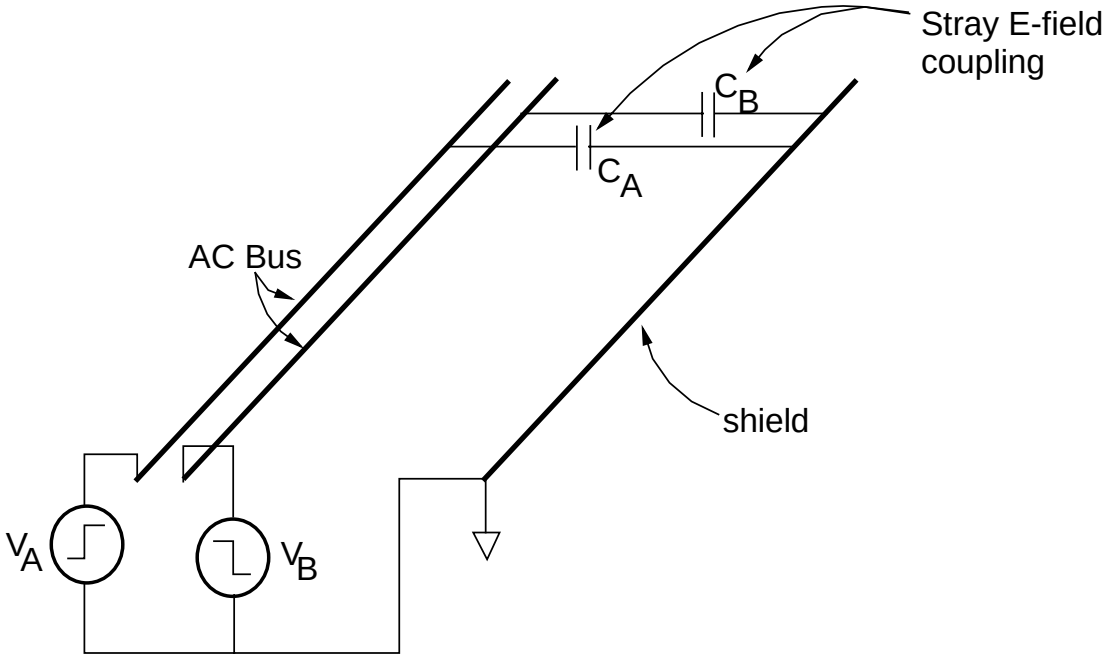
The solution to the shield current problem lies in applying "noise" cancellation techniques.

5.3.2.2.4 A simple solution to the shield current problem

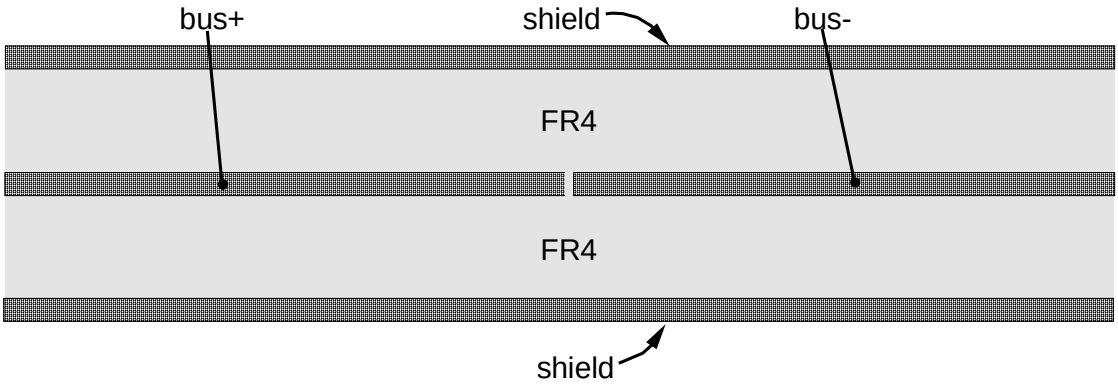
The location of the shield layers is strategic from the standpoint that they provide a Cu layer that is held at a fixed potential between the bus layers and the logic traces. These layers midigate the effects of the stray electric field on the logic traces generated by the bus. Since the shield layers are necessarily located on adjacent layers to the bus conductors, the key to eliminating the shield currents is to inject equal and simultaneous, but opposite currents into the shield. This is conceptually illustrated in Fig. 5.22(a). For this scheme to work, the slew rates for V_A and V_B must be equal and opposite, and the transitions must occur simultaneously. Further, the capacitances representing the electric field coupling from the bus conductors to the shield, C_A and C_B, must be equal. The stipulation of equal capacitances requires a symmetrical bus structure, such as that shown in Fig. 5.22(b).

The issue of generating the out-of-phase, equal slew-rate bus voltage waveforms is resolved simply by center-tapping the FE's isolation transformer, as shown Fig. 5.23(b). The transformer's center tap becomes the "shield" and no additional switches or circuitry are required to be added to the HB inverter. Also, the transformer's design is not complicated because the center-tap carries no net current, and the bus voltage transition times are simply and accurately matched.

Figure 5.24 shows the theoretical and experimental shield currents utilizing the PCB bus structure shown in Fig. 5.22(b) in conjunction with the center-tapped isolation transformer. As can be seen, the shield currents are virtually eliminated. Induced logic noise performance is also improved over the 2 layer with shield structure, as can be seen in Fig. 5.25. This additional improvement is due to the elimination of the shield currents and with them the resulting noise voltages that were impressed in series with the logic traces through stray magnetic field coupling.

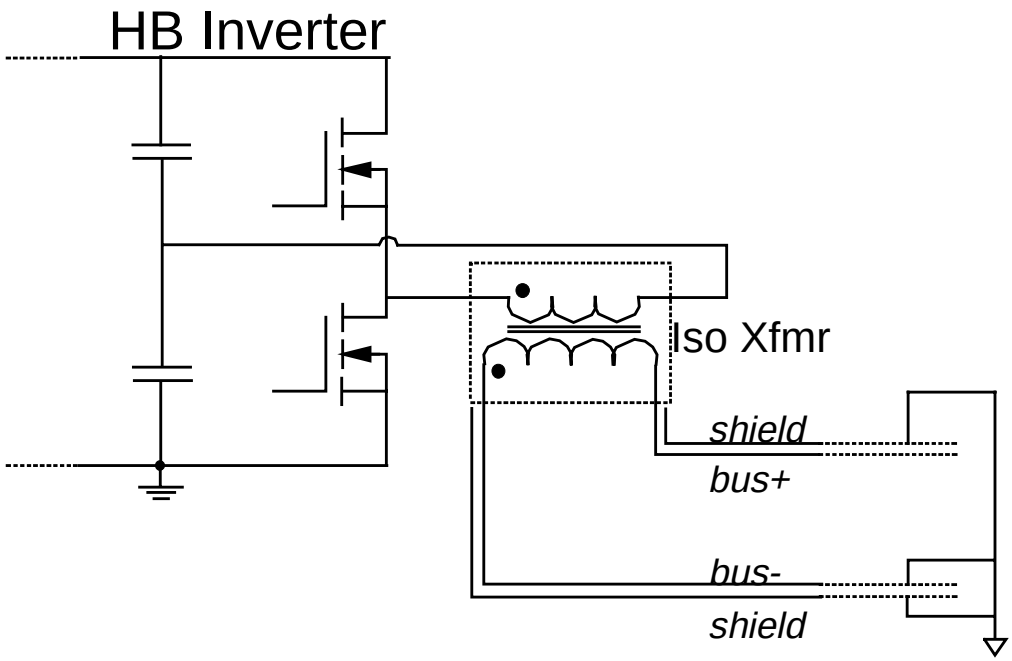


(a) Noise cancellation through the distribution of out-of-phase bus voltage waveforms.

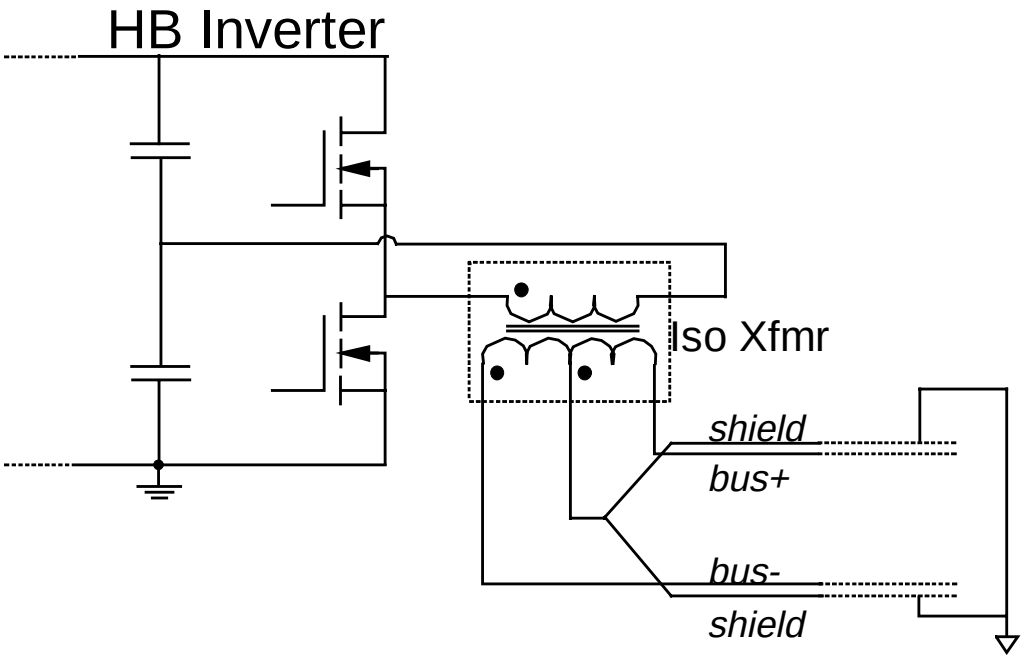


(b) PCB bus structure that implements the noise cancellation concept (1 lyr w/shield structure).

Fig. 5.22 Conceptual development of the solution to the shield current problem.

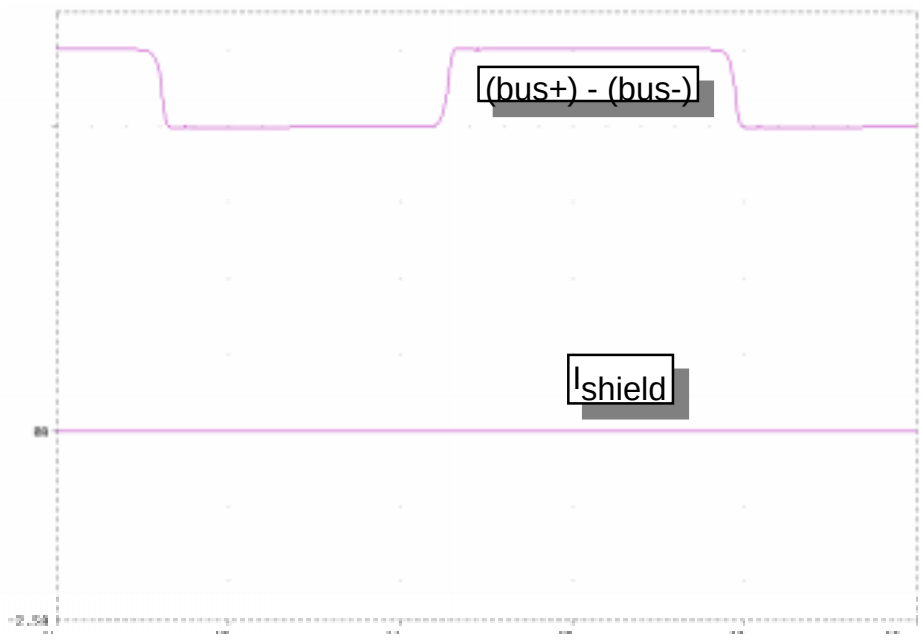


(a) Original single-phase design.

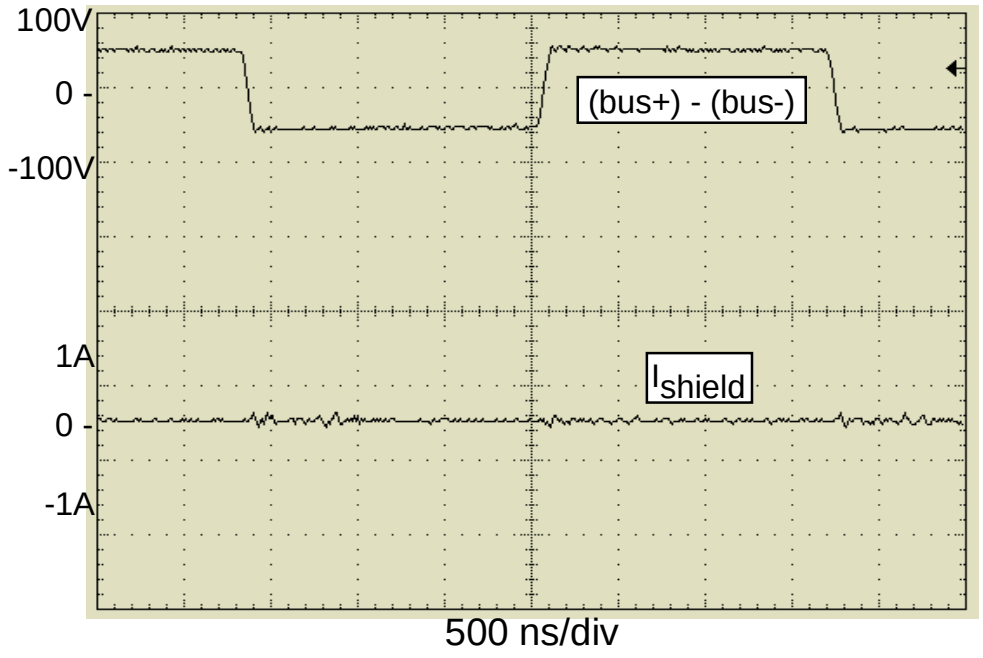


(b) Modified design for bi-phase operation.

Fig. 5.23 Modification of the front-end inverter to accommodate bi-phase bus voltage waveforms.

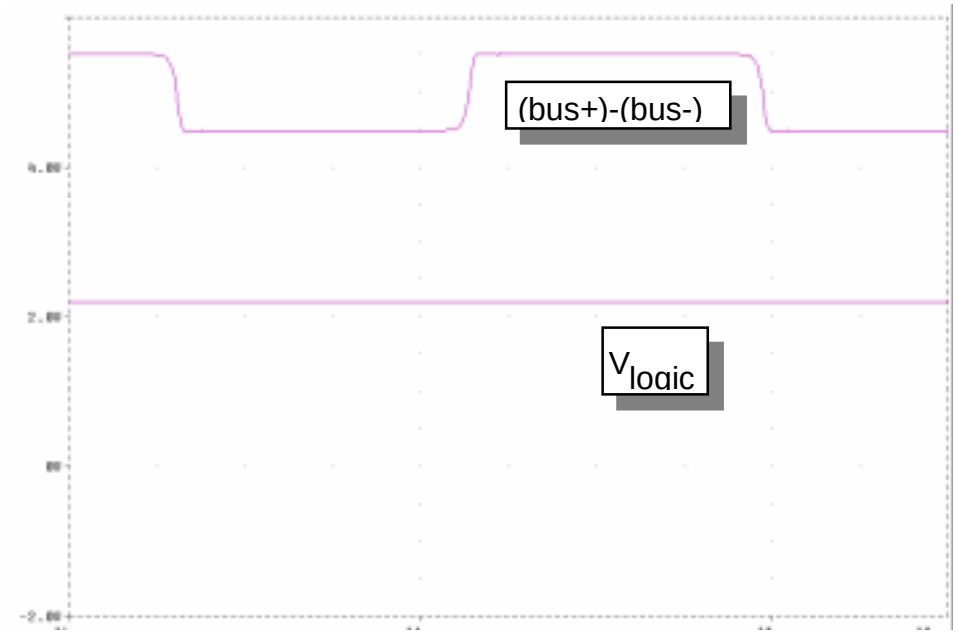


(a) Theoretical.

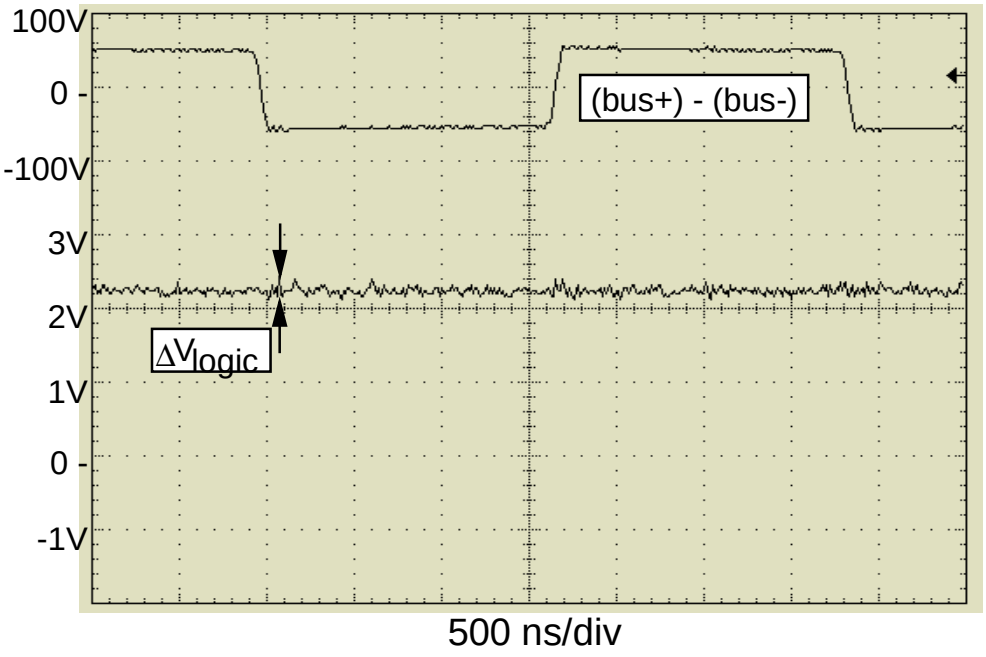


(b) Experimental.

Fig. 5.24 Shield currents for 1 lyr PCB bus structure and center-tapped FE transformer. Bus voltage $t_r/t_f \approx 65$ ns.



(a) Theoretical.



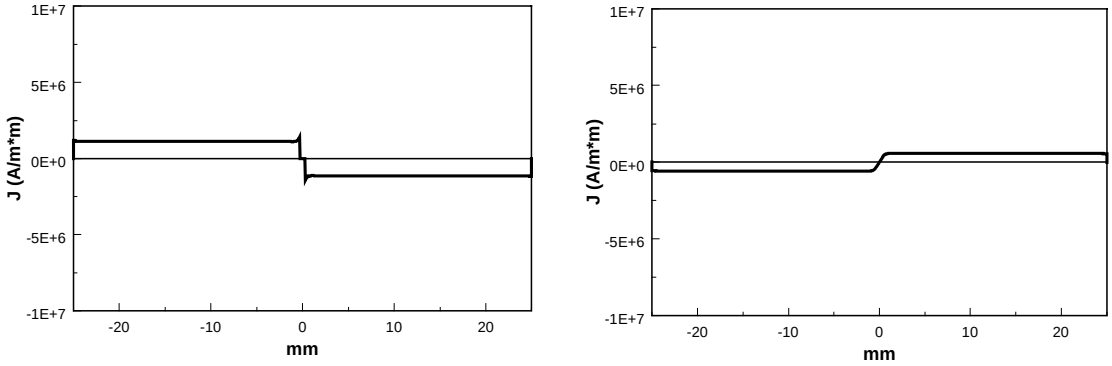
(b) Experimental.

Fig. 5.25 Induced logic noise for 1 lyr PCB structure with center-tapped FE transformer. Bus voltage $t_r/t_f \approx 65$ ns.

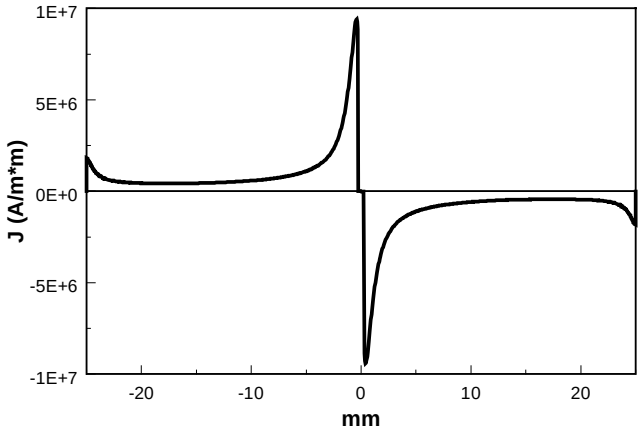
In addition to solving the shield current problem, the PCB bus structure shown in Fig. 5.22 displays a tremendous reduction in the density of the external (to the structure itself) magnetic field generated by the bus current (when compared with the 2 layer structures previously discussed). This will be demonstrated in the next section. However, this reduction in external magnetic field strength does not come without a price, an issue that is also addressed in the next section.

5.3.2.3 PCB bus structure optimization

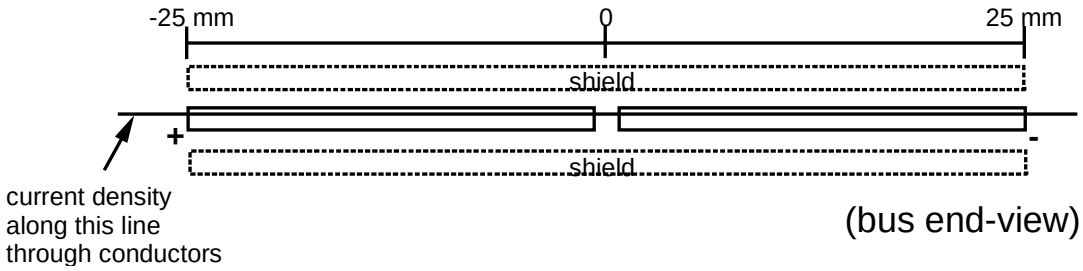
Compared to the simple parallel-plate structure, the 1 layer structure shown in Fig. 5.22(b) is fundamentally different in that the bus conductors are side-by-side carrying equal, but opposite currents. For DC and low-frequency applications this may be acceptable, but as the bus frequency is increased the bus currents tend to crowd toward the inside edges of the conductors, due to both eddy and proximity effects. This phenomena is illustrated in Fig. 5.26, which shows the conductor and shield current densities for the 1 layer structure. For this data, the spacing between the conductors was set at 20 mils, with the total layer width kept the same as for the parallel-plate structure (2"). However, because both the bus+ and bus- conductors are on the same layer, half the amount of copper is used when compared to the parallel-plate structure. Also shown is the current density for the 1 layer structure with the shield layers removed, illustrating the exaggerated proximity effects at the inside edge of the conductors and the (smaller) eddy current effects on their outside edges. As a point of reference, Fig. 5.27 shows the conductor and shield current densities for the parallel plate structure. In this case the proximity effects are not obviously visible, and this is due to the fact that this structure's "aspect ratio" completely different. For the single-layer structure (without the shield layers) the area of greatest magnetic field density is between the inside edges of the two conductors, with a direction that approaches being *perpendicular* to the top and bottom surfaces of the conductors. For the parallel-plate structure, the area of greatest magnetic field density is confined primarily to the area immediately between the "plates," and is



(a) Conductor (left) and shield current densities.

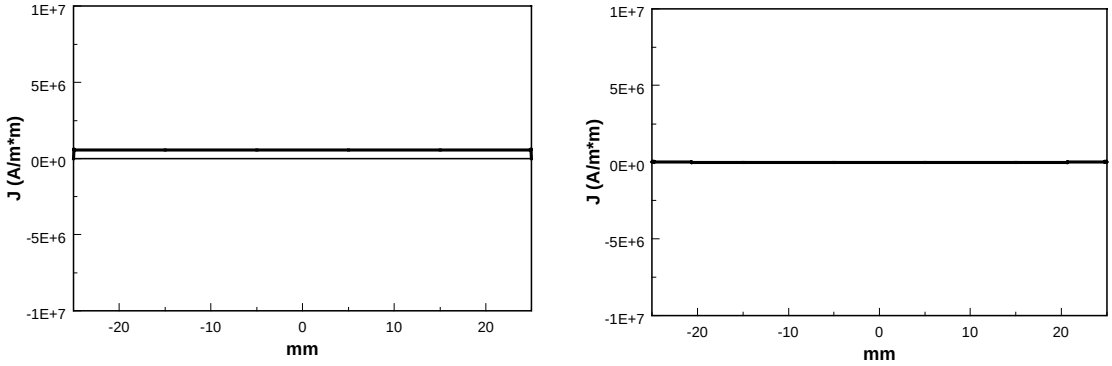


(b) Conductor current density without shield layers.

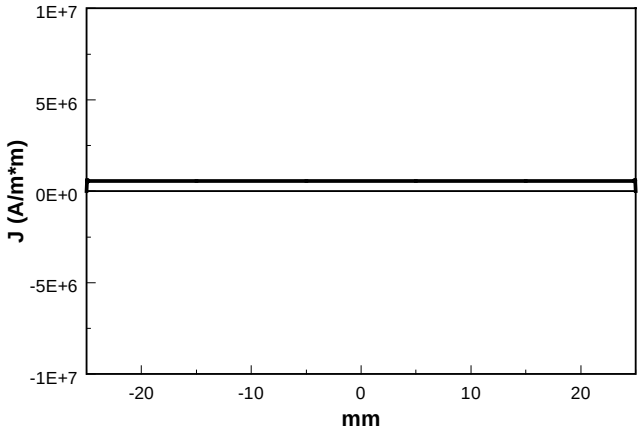


(c) Plot-line for conductor current density.

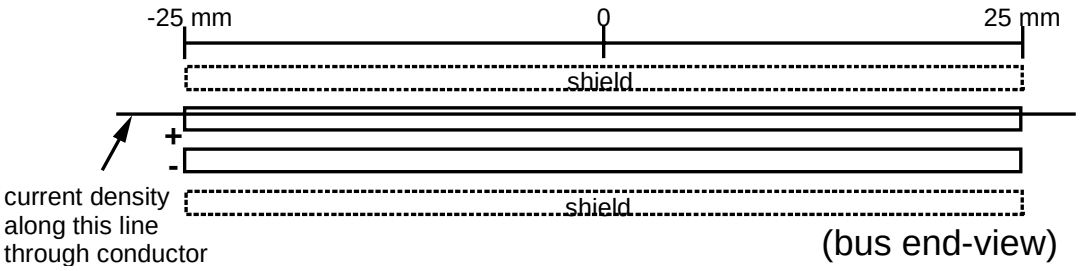
Fig. 5.26 300 kHz Cu utilization for the single layer bus structure.



(a) Conductor (left) and shield current densities.



(b) Conductor current density without shield layers.

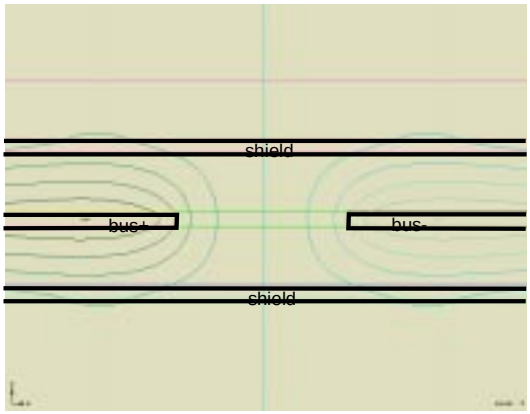


(c) Plot-line for conductor current density.

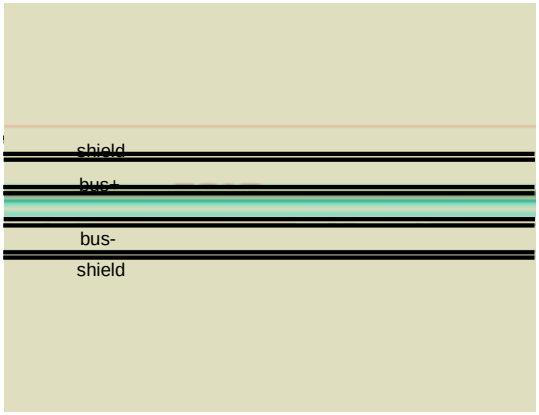
Fig. 5.27 300 kHz Cu utilization for the parallel-plate bus structure.

approximately *parallel* to the top and bottom surfaces. Figure 5.28 illustrates this by plotting lines of equal vector magnetic potential, derived from finite-element analysis, for both structures. Therefore, with respect to proximity effects, the conductor "thickness" of the 1 layer structure (without the shield layers) is 25 mm, whereas the conductor "thickness" for the parallel plate structure is the actual conductor thickness - ~ 1.4 mils for 1 oz. Cu. Hence the effect is much more pronounced for the single layer structure.

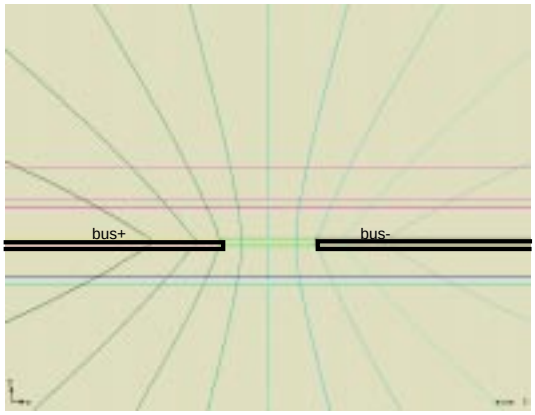
The addition of the shield layers to the single layer structure considerably modifies the proximity effect, as demonstrated by Figs. 5.26(a) and 5.28(c). Here the shield introduces proximity effects of its own, setting up currents that oppose the magnetic fields setup by the bus currents flowing in the side-by-side conductors (i.e., Lenz's Law). The net result is magnetic fields in the structure that now run approximately perpendicular to the top and bottom surfaces of the conductors - resulting in vector magnetic equipotential lines that are similar in shape to the parallel-plate structure. Hence conductor Cu utilization in the single-layer structure is much improved with the addition of the shield layers, as evidenced by the current density plots shown in Fig. 5.26(a). However, due to the losses introduced by the shield layers and some residual proximity effects at the inside edges of the conductors, the single layer structure still has higher loss than the parallel plate structure, even when the single layer structure is modified to give it the same "DC" copper area as the parallel-plate structure. A loss comparison (at 300 kHz) for the various structures discussed to this point is shown in Fig. 5.29. As mentioned above, the density of the "external" magnetic field (B field) generated by the single-layer with shield structure is significantly improved over the parallel-plate structure. Figure 5.30 compares the B field magnitudes along a 2" line that is perpendicular to the bus, extends 1" above and below the plane of bus, and crosses at the bus structure's origin. As can be seen from the plot, the magnetic field density is reduced by a factor of between 30 and 60 for the single layer with shield structure when compared with the parallel-plate structure, beyond a distance of about 0.4" above or below the plane of the bus structure.



(a) Single layer with shield.

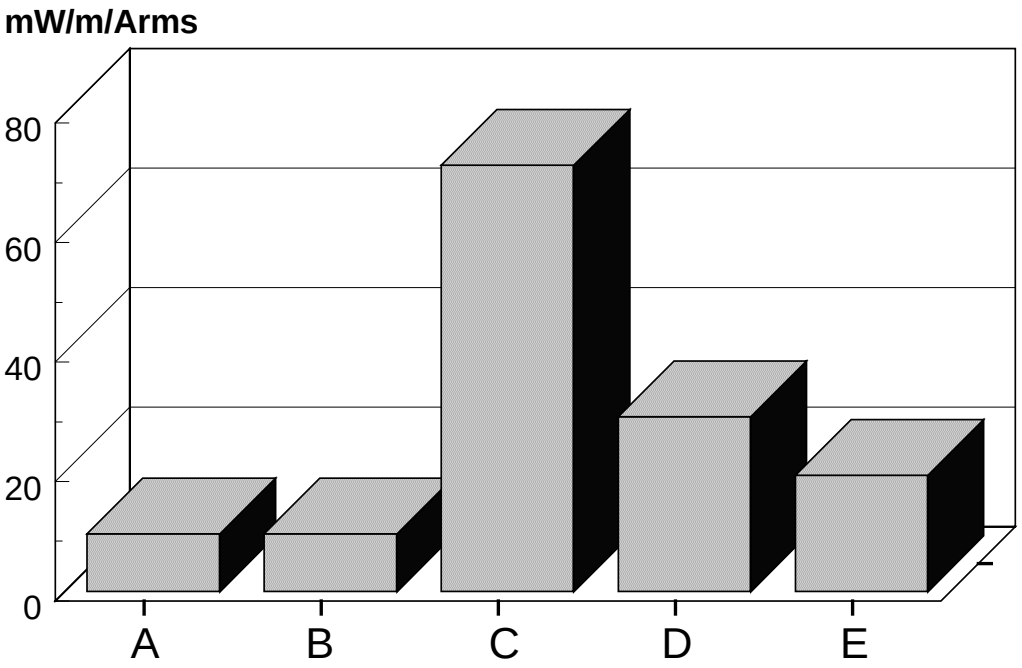


(b) Parallel plate.

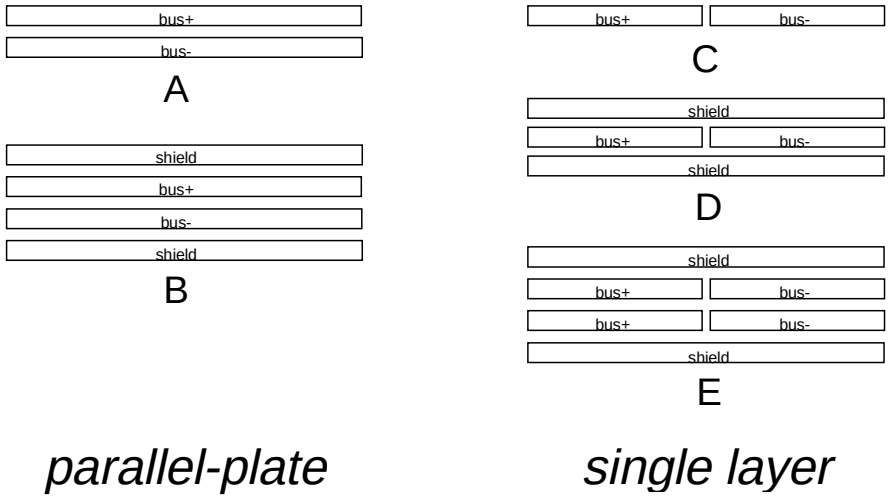


(c) Single layer without shield layers.

Fig. 5.28 Lines of equal vector magnetic potential for single layer and parallel-plate bus structures.



(a) Loss at 300 kHz.



(b) Bus structures.

Fig. 5.29 Loss comparison for parallel-plate and single layer structures.

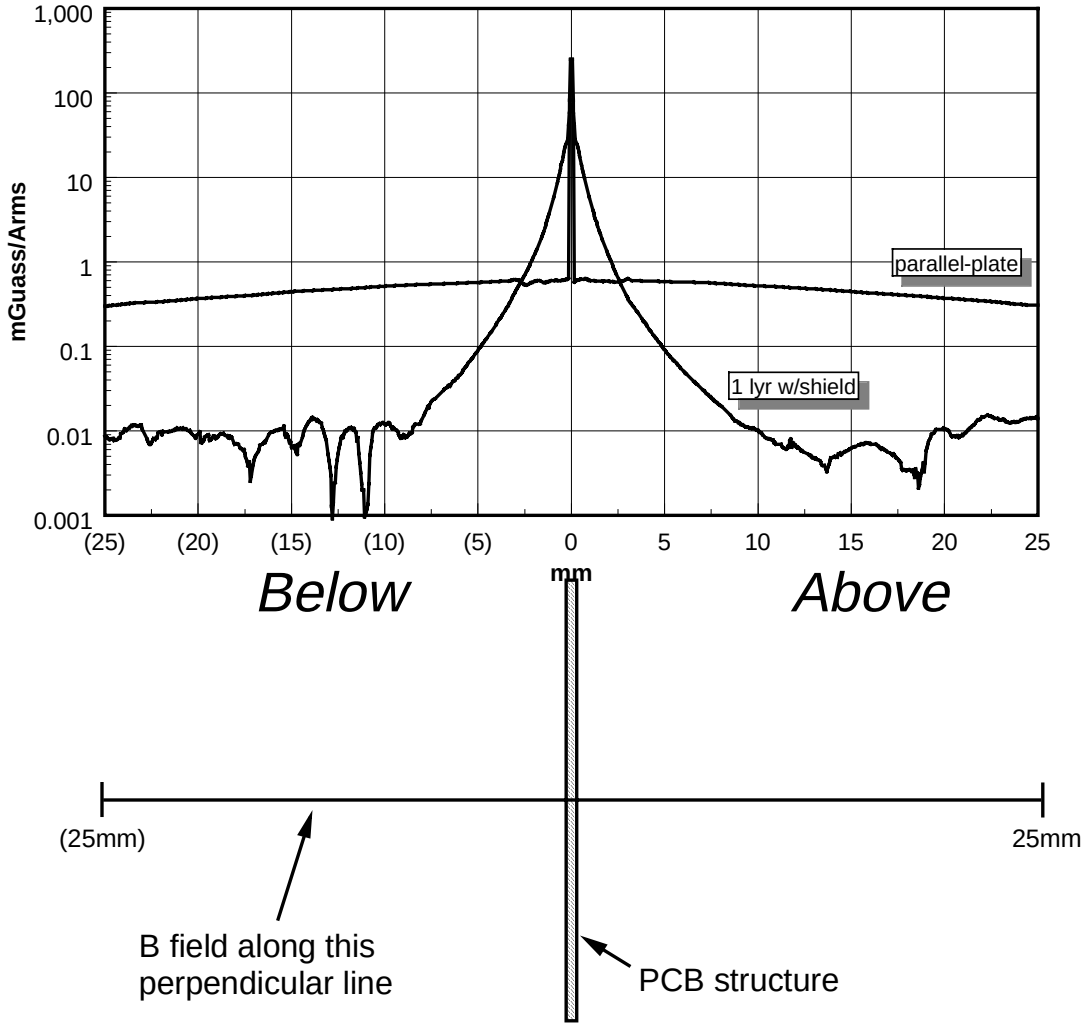


Fig. 5.30 Perpendicular-line B-field magnitudes for single layer and parallel-plate bus structures.

The results presented in Figs. 5.29 and 5.30 illustrate the tradeoff involved in selecting from the bus structures designs discussed to this point. While losses for the single-layer with shield structure are twice the parallel-plate design, its radiated B field characteristics are far superior. What would be desirable are bus structures designs that combine the desirable B field characteristics of the single layer structure with the reduced loss properties of the parallel-plate structure.

In order to minimize losses, it is preferred to avoid making use of the shield layers for magnetic field cancellation. Another method to reduce the "external" magnetic field is to place conductors carrying equal but opposite currents in as close a physical proximity as possible. To a degree, the parallel-plate structure already accomplishes this, since the bus+ to bus- spacing is 6 mils, with a conductor width of 2" (2000 mils). But by subdividing the conductors in the parallel-plate structure into separate conductors, as shown in Fig. 5.31, greater external B field reduction can be achieved relative to the parallel-plate structure, without the loss penalty incurred by the single layer with shield structure. The structures shown in Fig. 5.31 can be thought of as combining two or four one layer with shield structures, as indicated in the figure.

Figure 5.32 compares the conductor and shield Cu utilization for the single layer with shield and 2 layer with shield, 4 conductor structures. The spacing between conductors on the same layer is 20 mils for both structures. For the 2 layer with shield, 4 conductor structure, proximity effects are minimal and the induced shield current is small as well. Therefore losses are going to be similar to the parallel-plate structure. Figure 5.33 shows the lines of equal vector magnetic potential for the same two structures as in Fig. 5.32. The 2 layer with shield, 4 conductor structure has higher external B fields.

Further subdividing the 4 conductor structure into 8 conductors (see Fig. 5.31(b)) further reduces this external B field with virtually no additional loss. Figure 5.34 summarizes the B field data for the single layer and the 2 layer with 4 and 8 conductors perpendicular to the plane of the PCB. As the conductors in the 2 layer design are further subdivided, the B field magnitudes may approach the limits set by the single layer

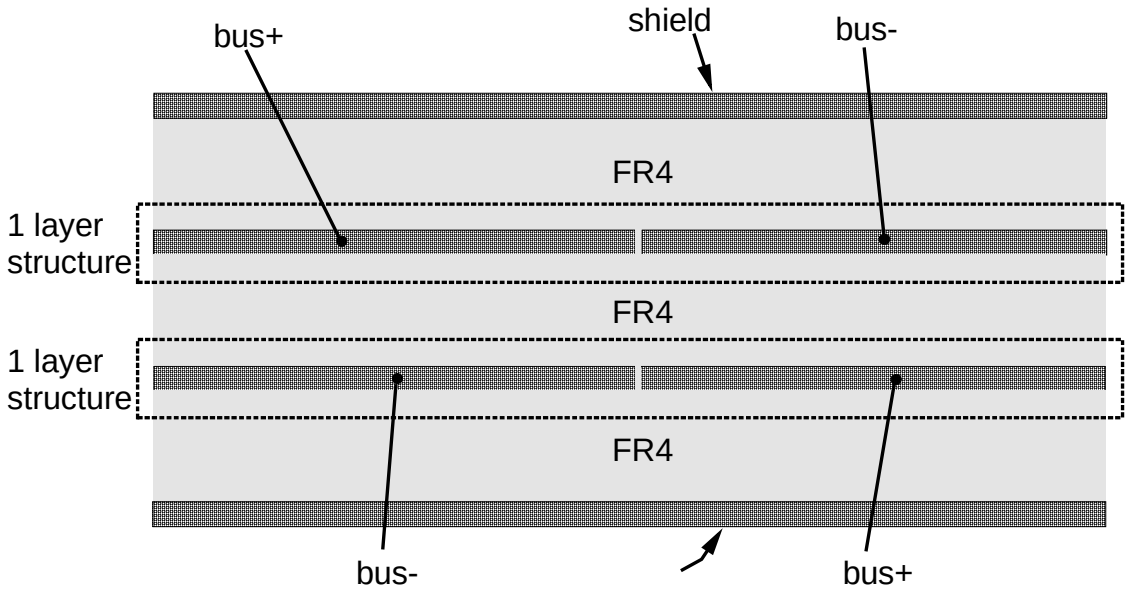
with shield design. A summary of the losses is shown in Fig. 5.35. The loss for the 4 and 8 conductor designs is about half of that for the single layer with shield design.

5.3.2.3.1 Experimental results for the 2 layer, 4 conductor structure

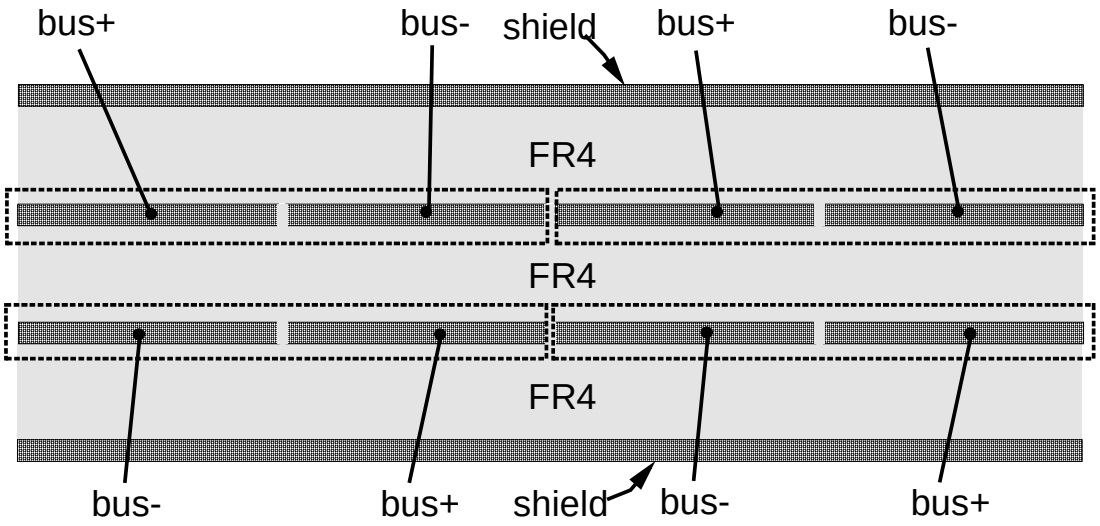
The 2 layer, 4 conductor structure was incorporated into the test bed to verify the induced logic noise and shield current performance and to compare simulation results based on FEA of the structure with experimental results. Figure 5.36 shows the theoretical bus waveforms alongside the ones obtained from the test bed. There is excellent agreement between the two, providing much confidence that the results from the analysis of even more complicated bus structures using finite element methods will be useful in providing design guidance. Figures 5.37 and 5.38 show the experimental results for induced logic noise and the shield currents. With respect to these two issues, the 2 layer, 4 conductor structure yields the best performance out of all the structures tested.

5.3.2.3.2 Bus structure optimization - summary

Figure 39 summarizes a comparison between the bus structures investigated. The criteria for comparison are Cu utilization, B-field performance (as measured along the line shown in Fig. 30), and induced logic noise. The tradeoff between loss and the reduction in the radiated magnetic field is apparent. For the power system specifications considered here (P_{max} ~ 400 W), the single-layer, 4 conductor with shield structure is probably the best choice.

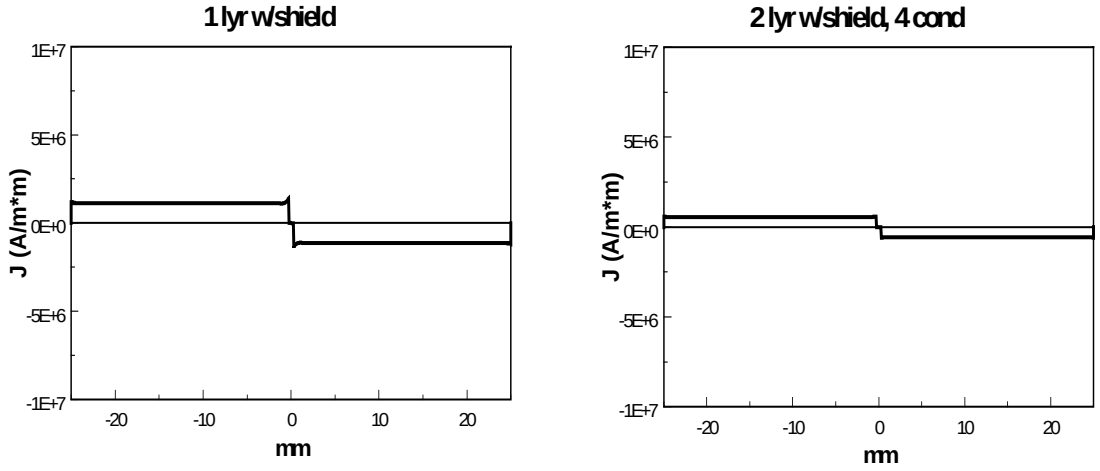


(a) 2 layer w/shield, 4 conductor.

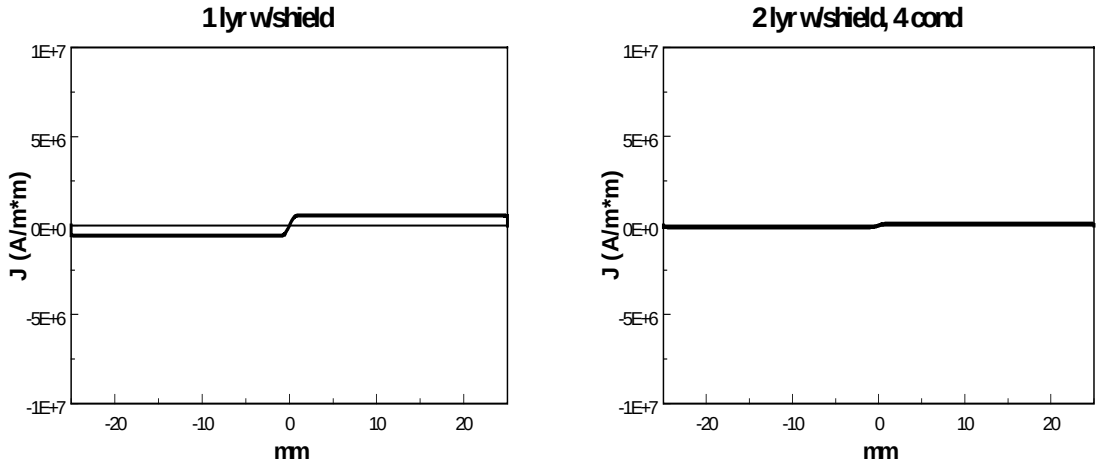


(b) 2 layer w/shield, 8 conductor.

Fig. 5.31 Design of the 2 layer w/shield, 4 conductor and 2 layer w/shield, 8 conductor PCB bus structures.

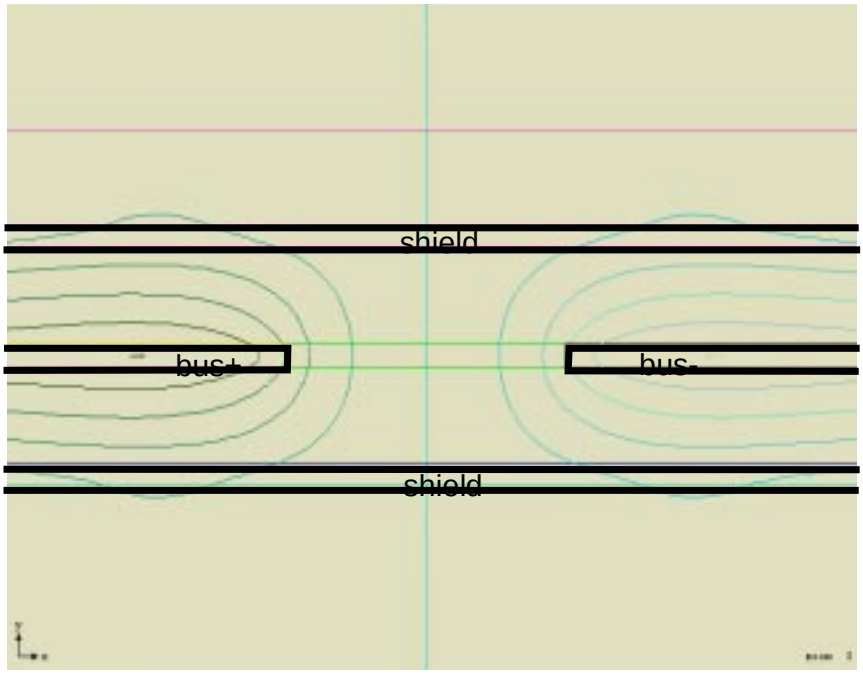


(a) Conductor current density

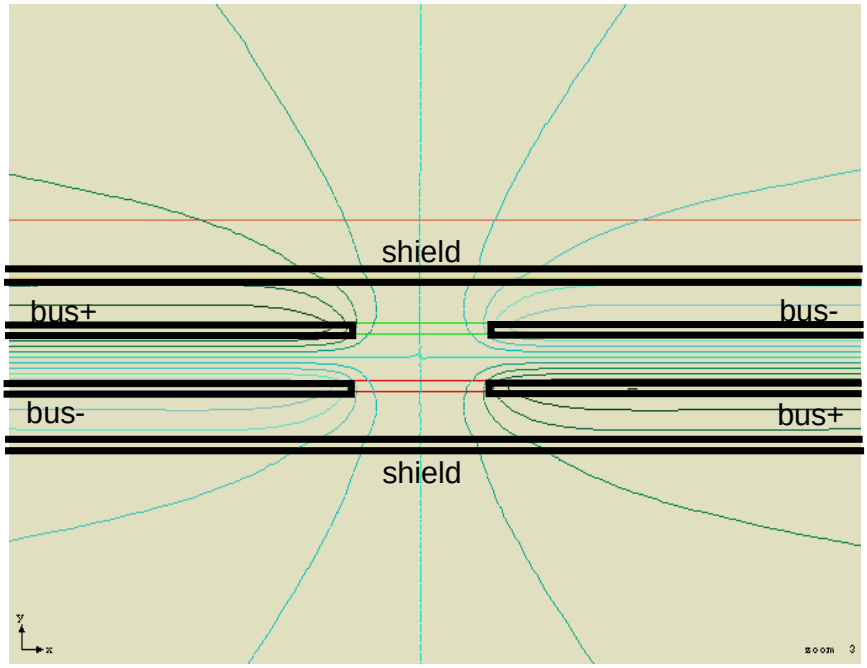


(b) Shield current density.

Fig. 5.32 1 lyr and 2 lyr conductor and shield Cu utilization.



(a) 1 layer w/shield.



(b) 2 layer w/shield, 4 conductor

Fig. 5.33 B-field characteristics for 1 lyr and 2 lyr PCB structures.

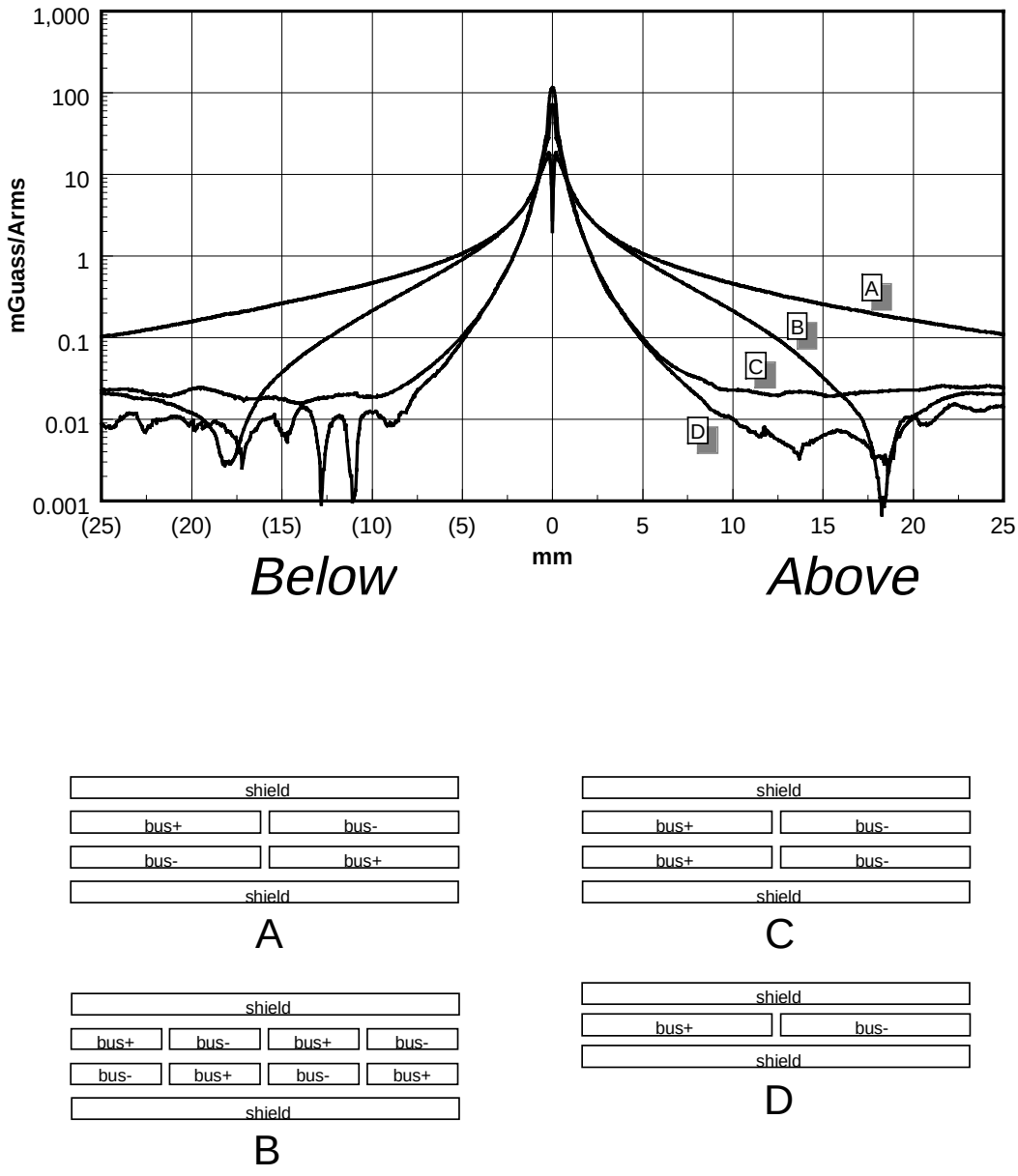


Fig. 5.34 Perpendicular line B field magnitudes for the bus structures shown.

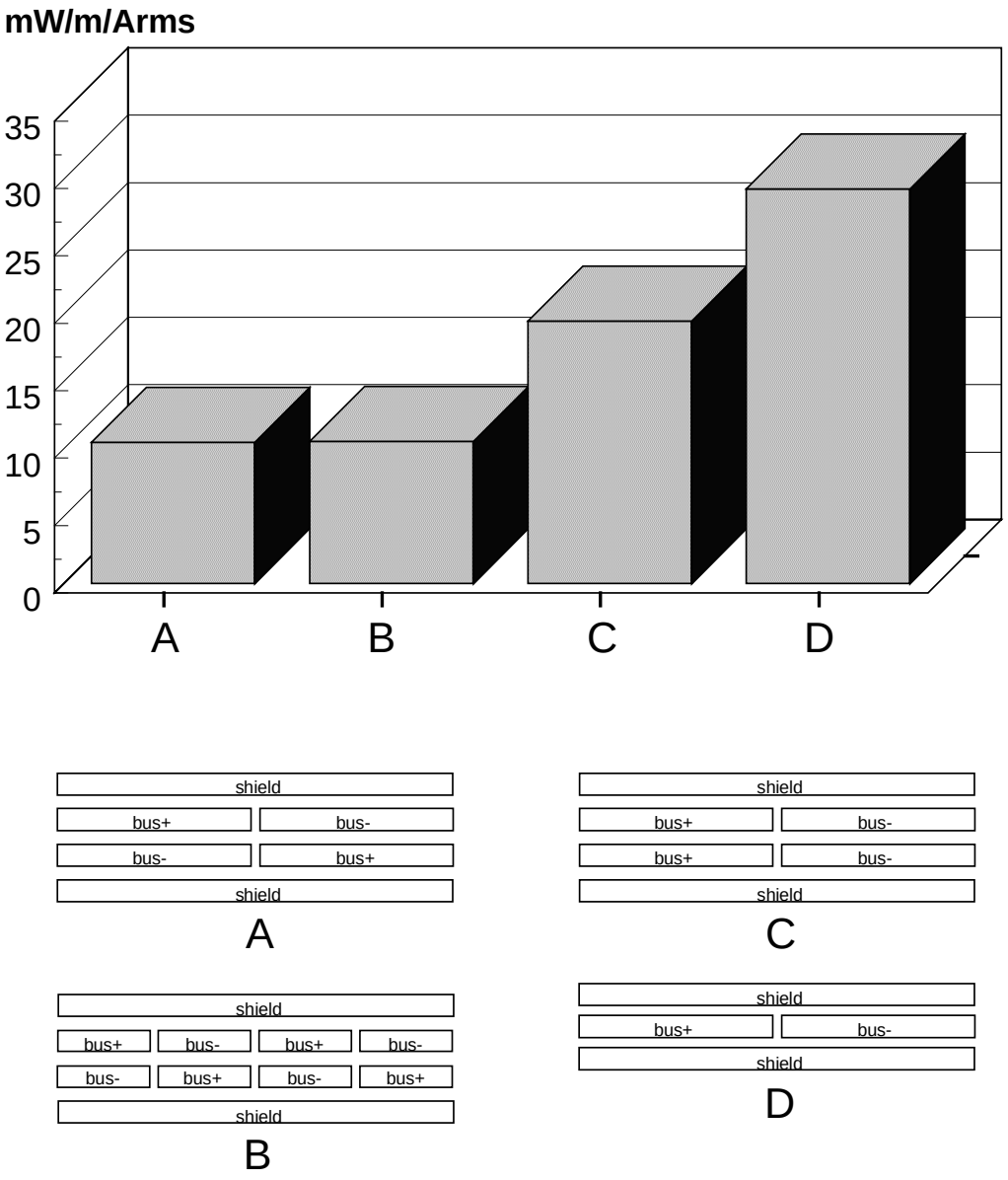
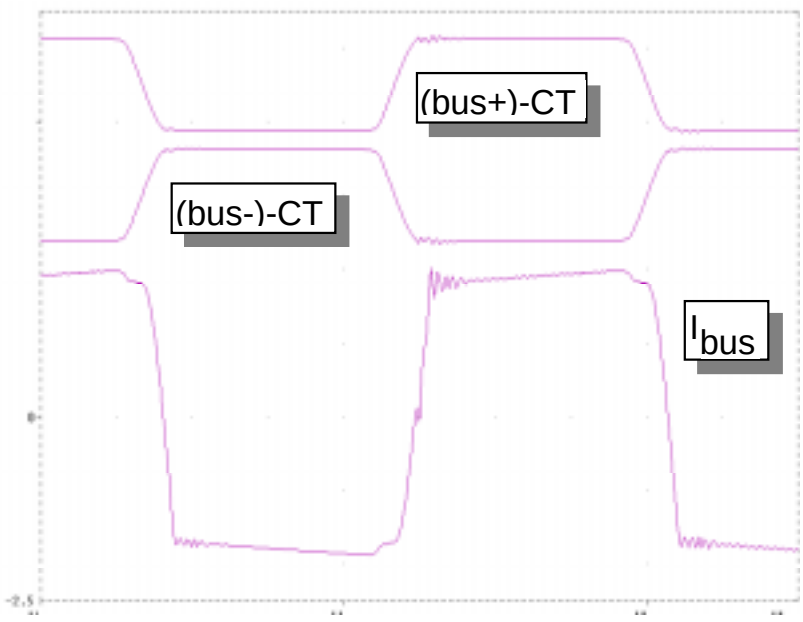
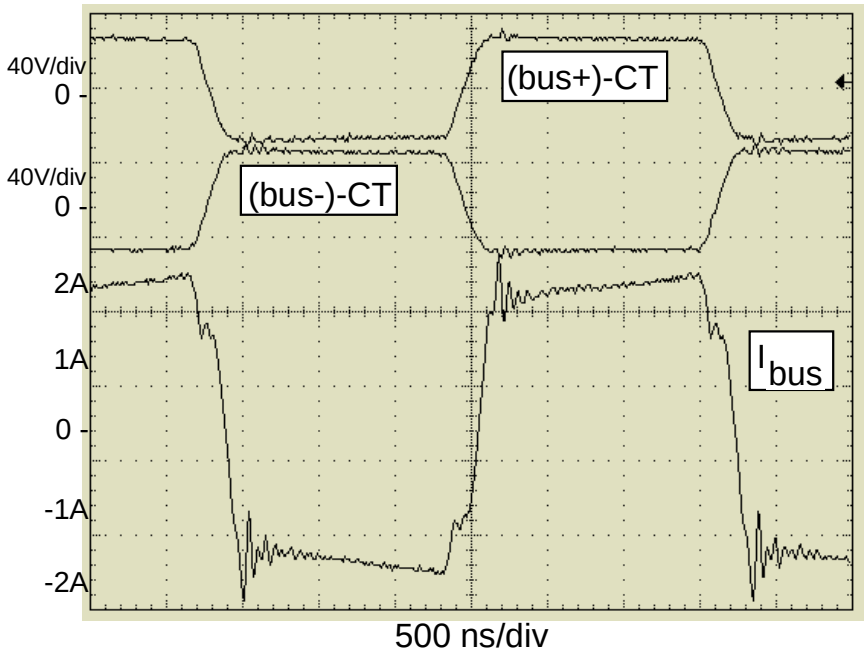


Fig. 5.35 Loss for 1 layer w/shield based structures.

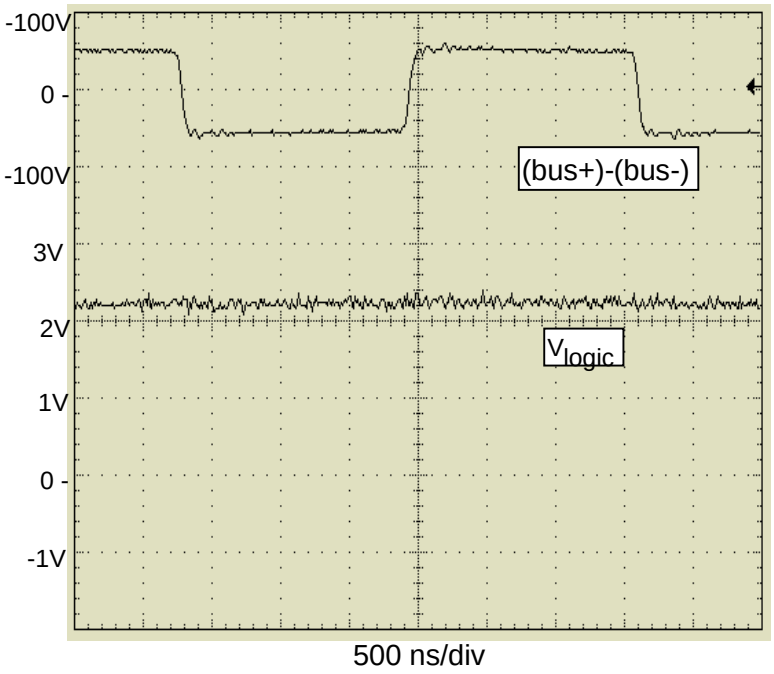


(a) Theoretical.

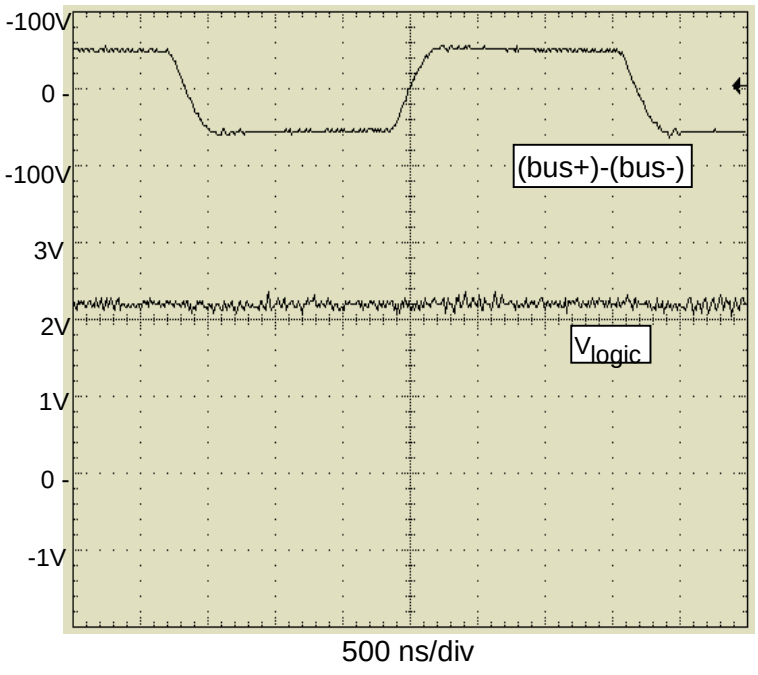


(b) Experimental.

Fig. 5.36 Bus voltage and current waveforms utilizing the 2 lyr w/shield, 4 conductor PCB bus structure. Bus voltage $t_r/t_f \approx 215$ ns.



(a) $t_r/t_f \approx 65$ ns.



(b) $t_r/t_f \approx 215$ ns.

Fig. 5.37 2 lyr, 4 conductor bus structure induced logic noise for Vcc = 2.2 Vdc.

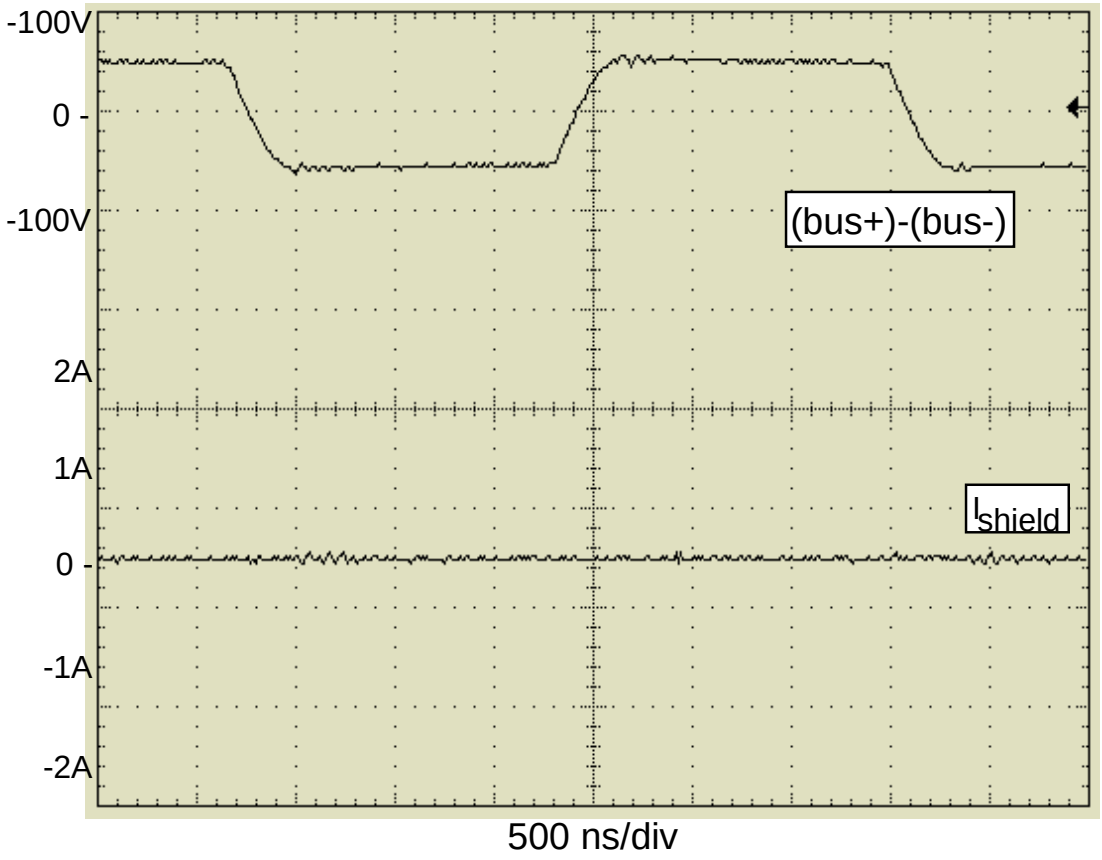


Fig. 5.38 2 lyr, 4 conductor bus structure shield current. $t_r/t_f \approx 215$ ns.

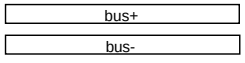
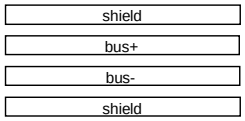
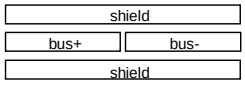
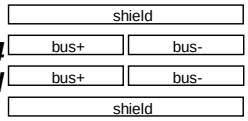
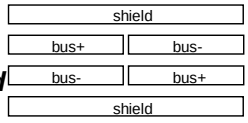
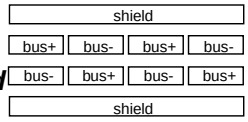
(1 - best, 4 - worst)		*Cu utilization (loss)*	*B-field*	*induced logic noise*
parallel-plate		1	4	4
parallel-plate w/shield		1	4	2
single-layer w/shield		4	1	1
single-layer, 4 cond w/shield		3	2	1
two-layer, 4 cond w/shield		1	3	1
two-layer, 8 cond w/shield		1	3	1

Fig. 5.39 Summary of bus structure optimization.

5.3.3 The effect of bus voltage rise/fall times on the electric field characteristics

Having solved the induced logic noise problem, which was demonstrated to be caused by stray electric field coupling from the bus power distribution layers (source) to the logic traces (receiver), it is instructive to take a look at the electric field characteristics at distances farther from the bus.

As was shown in Section 5.3.2.2.2, decreasing the bus voltage slew rates resulted in a reduction of the magnitude of the induced logic noise, all other factors being equal. The reason for this is easy to understand when viewing the phenomena from a circuit theory standpoint. From the perspective of field theory, specifically Maxwell's equations, the injected current is actually the displacement current, given by

$$I_{displacement} = \int_S \frac{d\varepsilon \mathbf{E}}{dt} \bullet d\mathbf{S}\,, \tag{5.6}$$

where **S** is an appropriately chosen surface over which to perform the integration. The important point regarding Eq. (5.6) is that the displacement current is a function of the time rate of change of the electric field, and that by lengthening the bus voltage transition times this current is decreased, for a given bus structure geometry.

For the near field electric field, the effects of bus voltage slew rates on the field intensity (as a function of frequency) can be determined experimentally. Referring to Fig. 5.40, it can be seen that as the bus voltage rise and fall times are increased, the relative (to a square wave) power contained in the waveform's harmonics decreases dramatically. It would be expected that the measured intensity of the E field harmonics should decrease as the bus voltage transition times are increased. The experimental setup to quantify the amount of decrease is shown in Fig. 5.41. An Electro-Metrics model

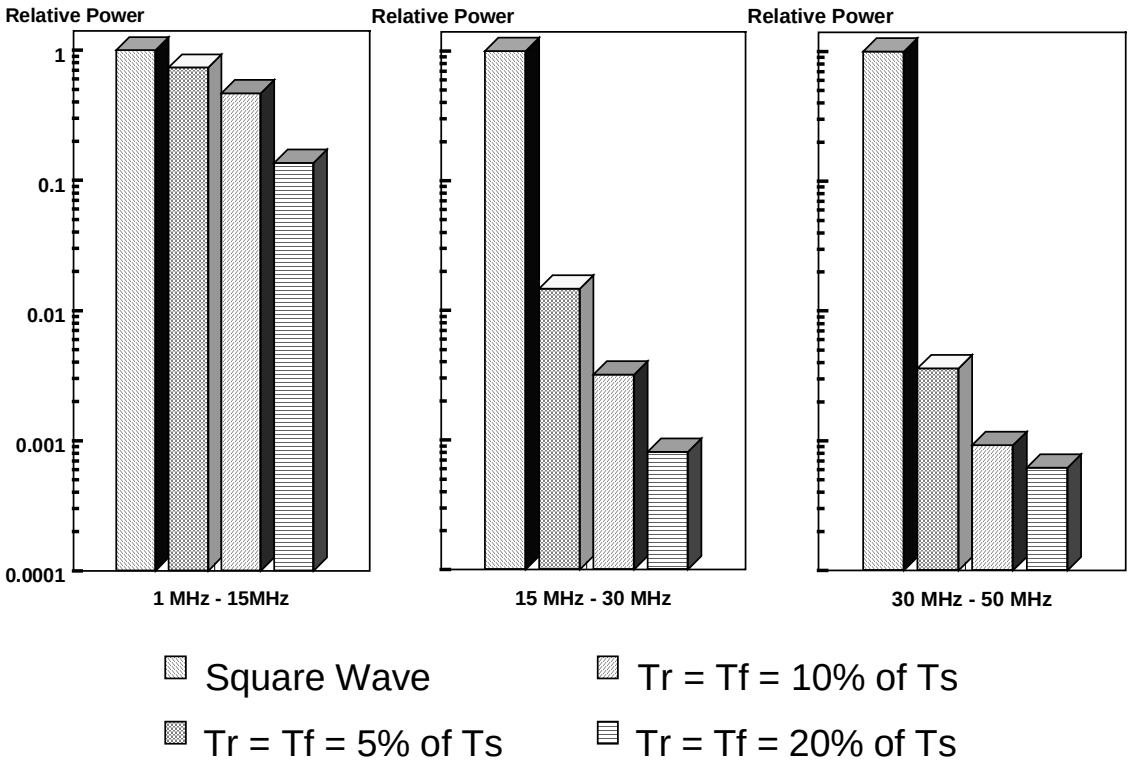


Fig. 5.40 Harmonic power as a function of bus voltage rise/fall times.

EM-6912 biconical antenna is located one meter from the AC DPS, approximately on the same horizontal plane. Although the response bandwidth of the biconical antenna only extends down to 20 MHz, comparative data can be taken at much lower frequencies.

The experimental results are shown in Figs. 5.42 and 5.43. Figure 5.42 is for the frequency range of 100 kHz to 10 MHz, and Fig. 5.43 covers the 10 MHz to 50 MHz range. The maximum frequency is limited to 50 MHz because it is approximately the frequency where the transition from near field to far field takes place at the antenna distance of 1 meter. For the 100 kHz to 10 MHz data, the bus voltage fundamental and first three harmonics are indicated. The data was taken utilizing the 2 layer w/shield, 4 conductor bus structure where Vin = 110 Vac and Po = 75 W. As can been seen, particularly in Fig. 5.42, there is a significant reduction in the strength of the E field's harmonics. Near 10 MHz some harmonics are reduced by 10 to 15 dB. A similar situation occurs between 20 and 30 MHz. Although it is difficult to correlate the data with Fig. 5.40, the experimental data demonstrate that modifying the bus voltage slew rates has a significant impact on the electric field intensity. As an aside, calibration data for the particular biconical antenna used to collect this data requires that approximately 17 dB be added to the Y axis scale in Fig. 5.43 over the frequency range of 20 to 50 MHz to convert the readings in dBμV to dBμV/meter.

Although noticeable reductions in E field intensity can be realized through decreased bus voltage slew rates, it is not clear what portion of the measured E field intensity is actually due to the power distribution bus, and what portion is due to the various dv/dt's present in the front-end converters (both the PFC boost, switching at 95 kHz and the HB inverter) and the post-regulators. For example, in the HB inverter, S2's drain voltage slews from near ground to approximately 380 V with the same transition time as the bus voltage. The drain voltage is significant because, for the breadboard circuit, the devices' heatsink, with its relatively large radiating area, maintains the same potential as S2's drain

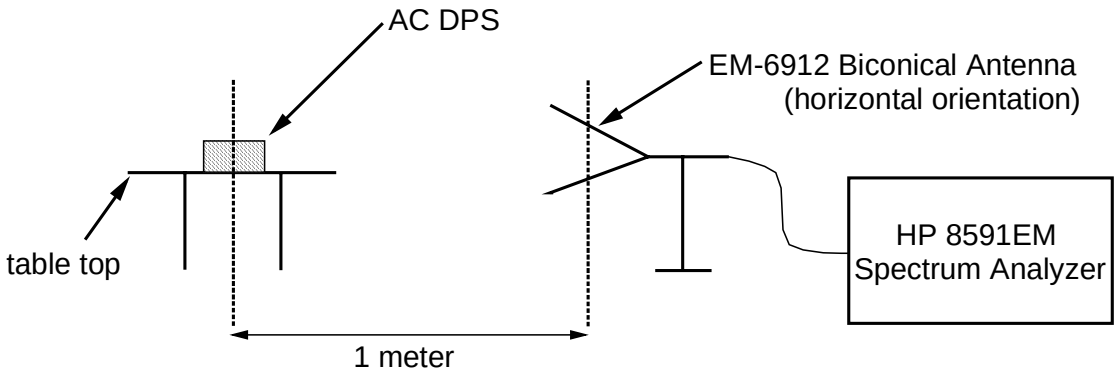
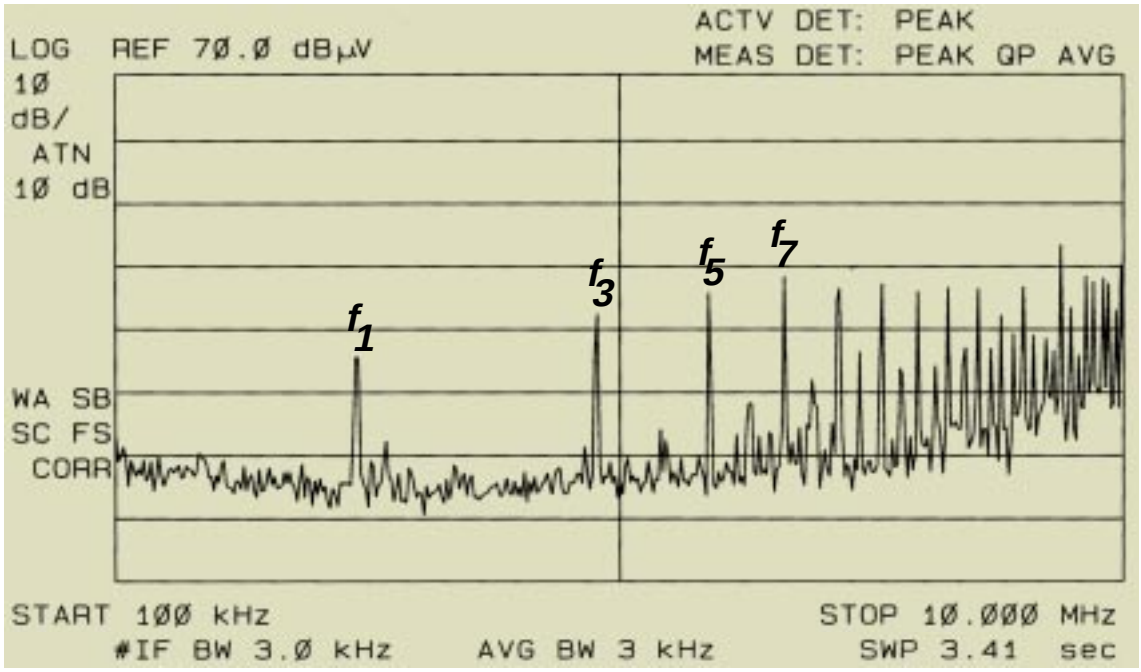
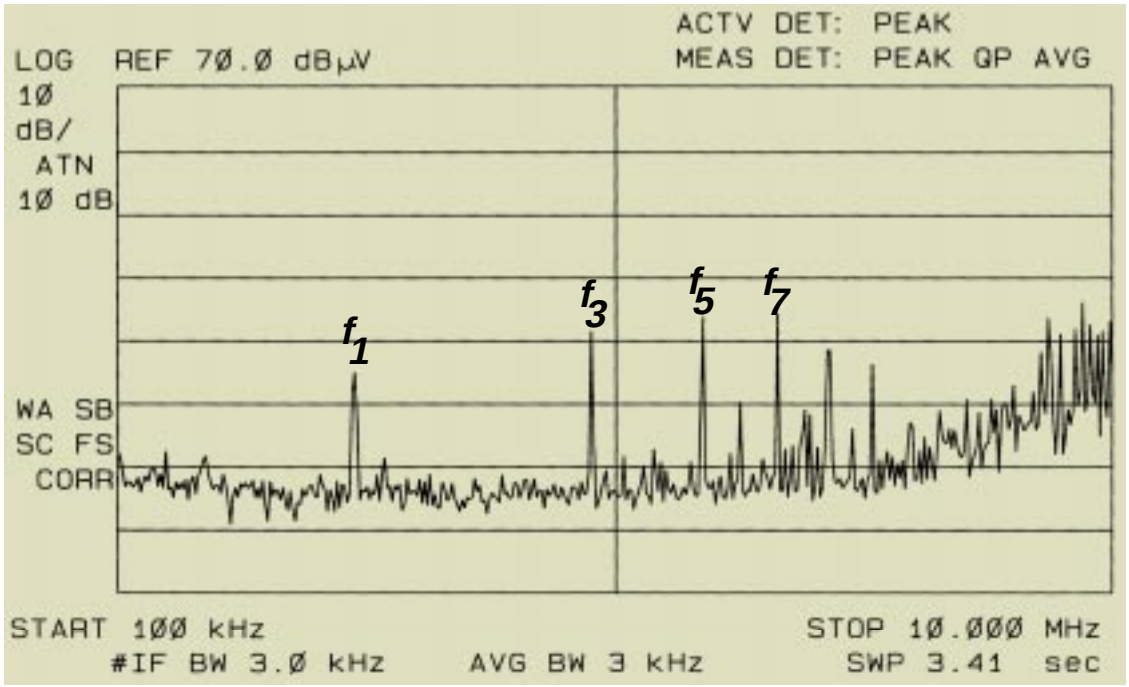


Fig. 5.41 Near field E field measurement experimental setup.

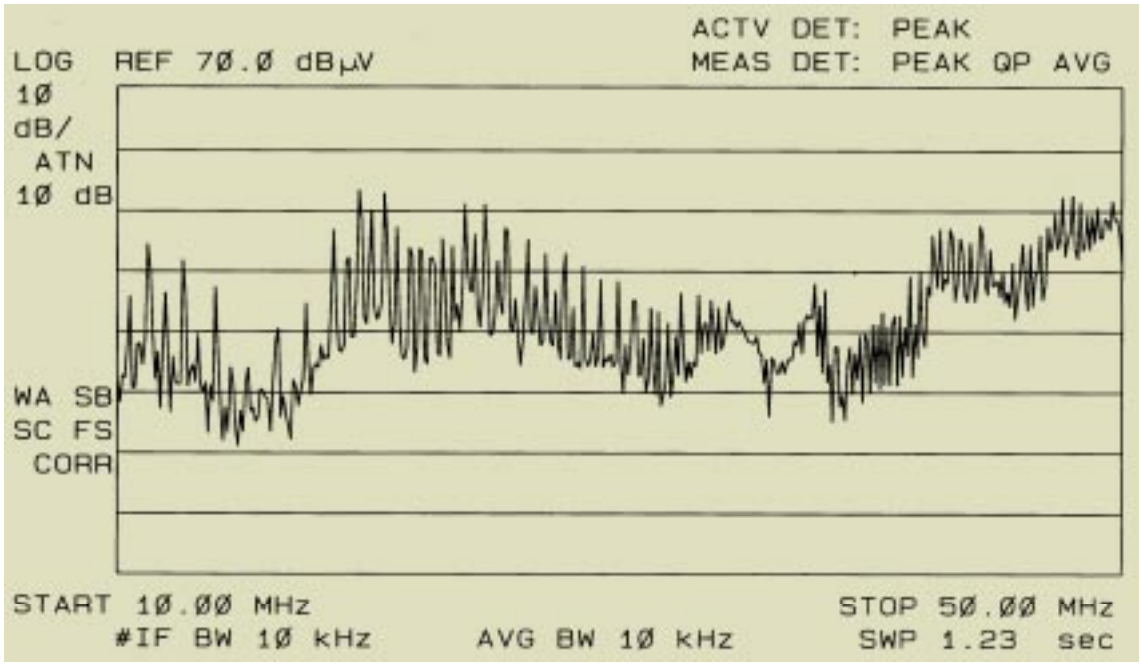


(a) $t_r/t_f \approx 65$ ns (~ 2 % of Ts).

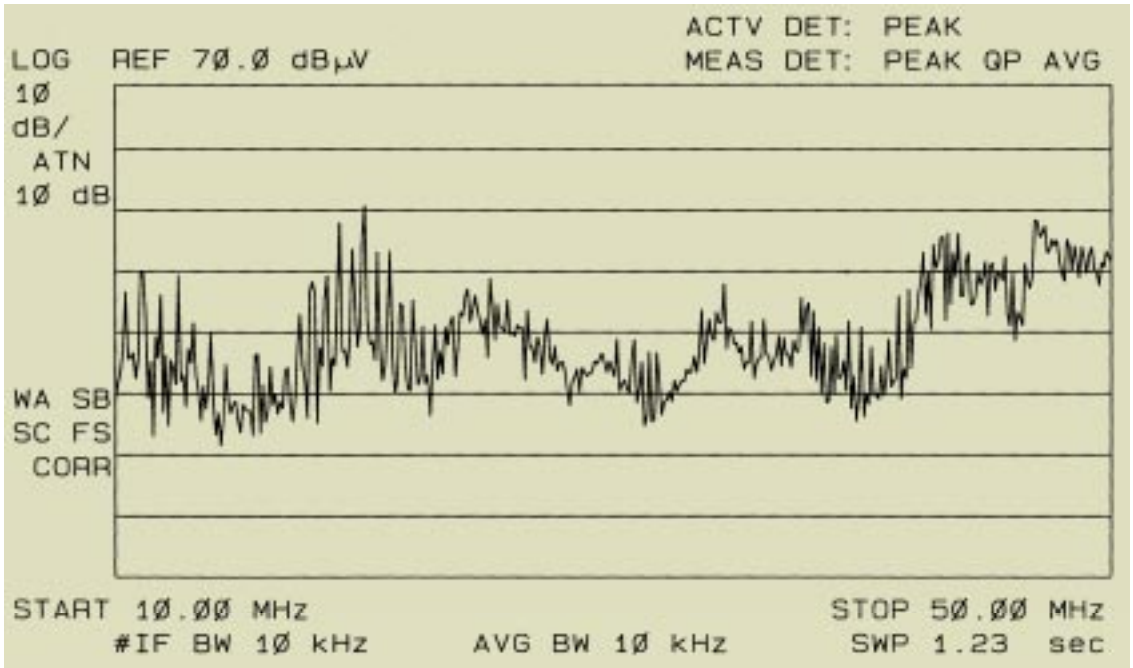


(b) $t_r/t_f \approx 190$ ns (~ 6 % of Ts).

Fig. 5.42 Experimental results, 100 kHz - 10 MHz.

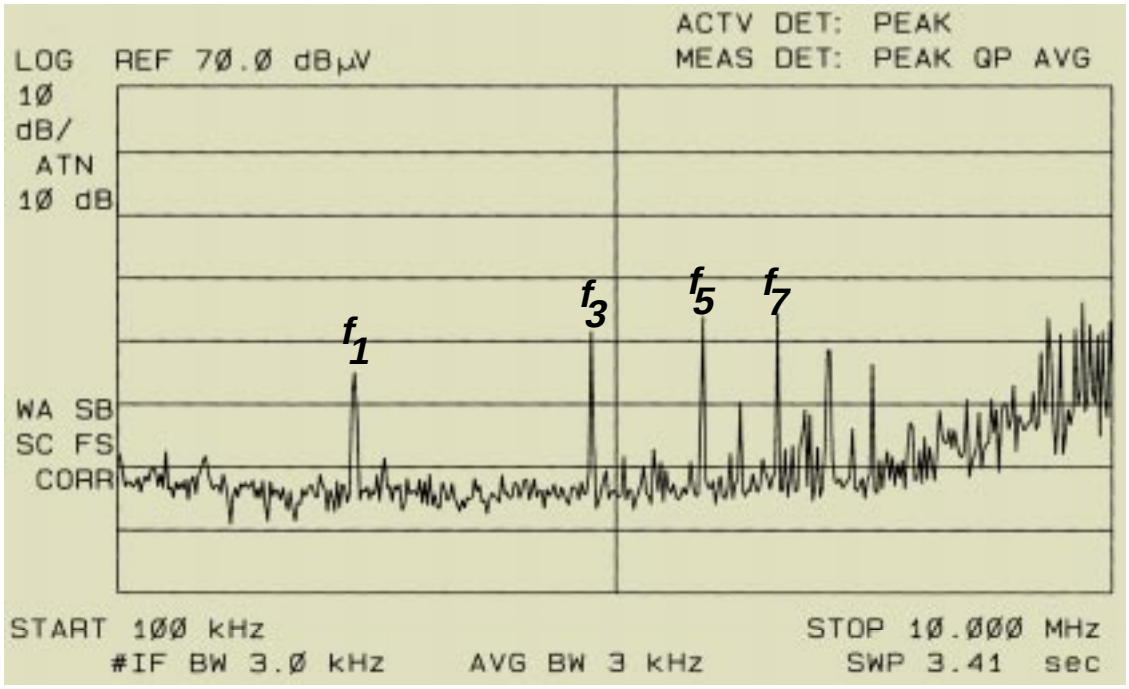


(a) $t_r/t_f \approx 65$ ns.

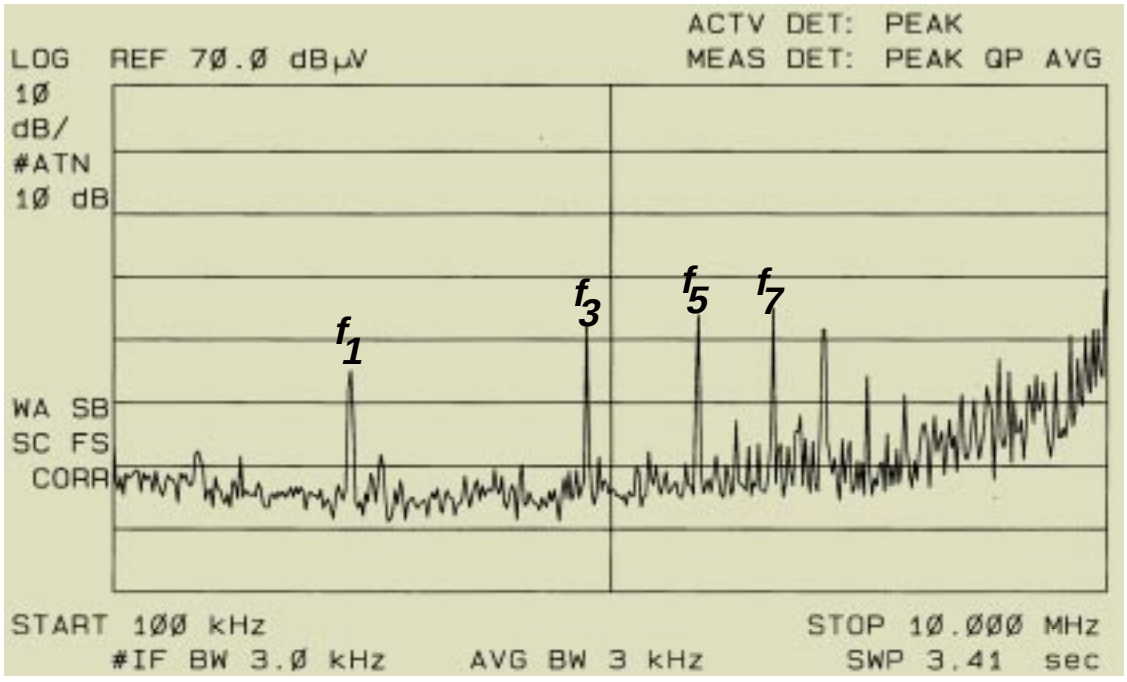


(b) $t_r/t_f \approx 190$ ns.

Fig. 5.43 Experimental results, 10 MHz - 50 MHz.



(a) With the bus.



(b) Without the bus.

Fig. 5.44 E field with and without the bus structure. $t_r/t_f \approx$ 190 ns for both plots.

voltage. Perhaps the simplest way to determine the bus structures' E field contributions is to measure the E field both with and without the distribution bus present. The results of these measurements are shown in Fig. 5.44. As can be seen the E field intensities are nearly identical with or without the bus. This result is really not very suprising, given the nature of the bus structure. The bus is essentially a large parallel plate capacitor - due to the very small layer-to-layer spacing relative to the overall bus dimensions. Results from the FEA confirm this as well. As a parallel-plate capacitor, the vast majority of the electric field generated by the bus is confined to the region between the "plates."

5.4 Summary

This chapter has addressed several fundamental issues with respect to the development of a HF AC distributed power system for computer system applications. These issues and their resolutions include:

1) The problem of determining the relative merits of choosing between sinewave and square-wave bus voltage and current waveforms from the perspective of power processing topology performance. A trade-off study, performed with the aid of computer simulation, attests to the notion that the use of square-wave bus waveforms leads to a simpler, more cost effective, and higher efficiency power system design. A crude piece-parts cost analysis indicates a 50 % reduction in inverter cost and a 25 % reduction in post-regulator cost (per regulator) for the square-wave system over the sinewave system.

2) The identification of the nature and magnitude of crosstalk and radiated noise effects caused by the bussing of HF AC power and the development of methods to mitigate these effects. After establishing the preference towards the use of square-wave topologies for the power system architecture, the primary induced noise mechanisms were first identified experimentally and then verified theoretically through the use of finite element analysis. Various solutions to the problem were

then proposed, verified, and compared. The optimal solution involves using a combination of bi-phase bus voltage waveforms with specific PCB bus structures - that result being canceled noise current due to stray electric field coupling from the bus to adjacent system circuitry. The bi-phase bus voltage waveforms are generated in a very simple manner, specifically by center-tapping the front-end inverter's isolation transformer. Trade-off issues involving the PCB bus structures, which utilize the bi-phase bus voltages, were identified as essentially as one of loss vs. external (to the bus structure itself) magnetic field reduction. Electric field experimental results verify that the distribution bus itself is a minor player in the determination of the overall near field E field characteristics of the power system.

Also, it should be noted that the pros and cons of the PCB bus structures developed in this chapter apply equally well to DC distributed power systems. In fact, the single layer with shield structure would not suffer from the disadvantage of increased loss if it where applied in a DC DPS, but would provide superior external magnetic field cancellation.