IMPACT OF LOT DEDICATION ON THE PERFORMANCE OF THE FAB

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ABSTRACT

Photolithography is the most complex of the operations involved in the fabrication of a wafer, and it requires the greatest precision. Photolithography is used to create multiple layers of circuit patterns on a chip. Traditionally, wafer fab operations, and in particular, those performed in the photolithography processing area, have always presented challenging scheduling and control problems. Some of the characteristics that make the photolithography processing area difficult to schedule are as follows: reentrant flow, unpredictable yield and rework time at critical operations, shared resources such as reticles, rapidly changing technologies, and lot dedication for steppers and scanners for critical layers. This processing area, where wafers are exposed using scanners or steppers, typically, comprises the bottleneck workstations. Also, the numbers of reticles available for a given layer of product type are limited. Consequently, it is important to develop appropriate schedules to ensure effective utilization of the tools involved.

In this study, a manufacturing line that is used to produce four dynamic random access memory (DRAM) products, requiring approximately 240 stages with 18 photolithography layers, is considered. The problem we propose to investigate can concisely be described as follows: Given a set of products to be processed in a photolithography area consisting of steppers and scanners (tools), with each product requiring a specific reticle type, determine the sequence in which to process the lots on

the tools loaded with requisite reticles, so as to minimize the cycle time. The reticles required for processing a product are known apriori and can be transferred from one tool to another. Also, the lot dedication requirement has to be met. This requirement pertains to the fact that some of the layers of a lot should be processed on the same tool. (Scanner or Stepper). The processing of other layers may not require lot dedication. These are handled accordingly. Some lots may enter into the system with the requirement of processing them urgently. (called hot lots). These are handled in the formulation of the problem as such.

Two solution methodologies are presented for the above stated problem. The first methodology uses a mathematical programming based approach. For the given routes and processing times of the product types, the entire problem is formulated as an Integer program. This integer program uses the start time of the jobs at various operations and the availability of reticles as variables, among others. The objective is to reduce the cycle time of the lots released into the system. The cycle time of a lot is defined as the time that a lot spends in the system. Results from the experimentation for integer program show that the computation time for solving small size problems is very high. A methodology is presented to solve this model efficiently.

The second methodology consists of the development of a new dispatching rule for scheduling lots in the photolithography processing area. This along with the other dispatching rules discussed in the literature are implemented using the Autosched AP software to study the impact that lot dedication makes on the performance of a fab. The performance measures that are considered include throughput, cycle time, WIP and utilization of tool sets. The results are presented for 1-level, 2-level and 3-level lot

dedication schemes. . It is shown that the 3- level lot dedication scheme performs the best under no preventive maintenance/breakdown case while, for the deterministic value of unscheduled breakdown times and preventive maintenance schedule used, 1-level lot dedication performed the best. Even though the 3- level lot dedication scheme is more flexible as compared to the 1 –level lot dedication scheme, yet for the values of unscheduled breakdown times and preventive maintenance schedule used, the performance of the 3- level lot dedication scheme is worse than that of the 1- level lot dedication scheme. For another set of break down time values and preventive maintenance schedule, the outcome can be different. We also compare the performance of the proposed procedure with that of the dispatching rules available with the AutoSched AP software. The results indicate that the proposed procedure is consistent in generating better solutions under different operating conditions.

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Chapter 1 Motivation and Problem Statement

1.1 Introduction

Traditionally, semiconductor manufacturing, and wafer fab operations in particular, have always presented challenging scheduling and control problems. The characteristics that make the semiconductor manufacturing difficult to schedule are as follows: reentrant flows, unpredictable yield and rework time at critical operations, batching, shared resources, high mix of products and rapidly changing technologies.

Recently fabs are adopting new technologies, which involve 300 mm wafer processing, which involves increased levels of automation. Hence, in order to control and co-ordinate these complex activities, efficient scheduling/dispatching tools need to be developed

Infineon Technologies, Richmond is part of Infineon Technologies (formerly Siemens Semiconductor Group), located at Sandston near Richmond VA. It has a fully integrated semiconductor-manufacturing site, which includes wafer fabrication, component probe, assembly and test, and module assembly and test.. The components and modules are primarily used as memory devices in the computer industry. Currently, this site is manufacturing 64M, 128M and 256M SDRAM and 256M DDR DRAM products-all product designs are manufactured below 0.20µm technology. Infineon Technologies, Richmond is ISO 9000 certified company and strives to be the benchmark for time –to –volume and cost –per-die in the manufacturing of high quality DRAMs.

1.2 Salient features of the Semiconductor Manufacturing Process

Traditionally, manufacturing systems can be classified as Flow shops and Job shops. Flow shops are generally known for low product mix and high volume of production. Machines are arranged in sequence and the jobs visit a machine only once in its entire route. Job shops can handle large product mixes and medium volume. They

have a variety of machine types. The routes of the jobs vary according to the operations to be performed on each product type. In job shops, a job may revisit a machine. The semiconductor manufacturing does not fit in to either of the above types. The flow in semiconductor manufacturing is reentrant in contrast to the unidirectional flow in flow shops, but the flow is structured and well defined as compared to that in the job shops.

1.3 Manufacturing Environment

Semiconductor wafer fabrication can be described as a multistage process with reentrant flow in which the equipment is arranged similar to a job shop. The operations include Chemical-Mechanical Polishing, Diffusion, Films deposition, Photolithography, and Implant (doping) and Etching. For each of the product type, a wafer goes through approximately 400 process steps over a period of a few weeks. Wafer fabrication planning and control is a complex task due to the large number of products and machines involved. It is further complicated by random disturbances; namely, reentrant flow of operations, set up issues due to the special nature of the operations, random machine breakdowns and random repair times. Improvements in scheduling and dispatching will make a dramatic difference in the performance of the semiconductor manufacturing facility (fab).

Infineon Technologies clean room manufacturing environment consists of 8 different areas. These are Chemical Mechanical Polishing, Diffusion, Etch, Films, Implant, Litho, Wets, and Ply.

1.Chemical mechanical Polishing: The purpose of the C.M.P process is to remove the previously deposited films by a combination of physical polishing and chemical reaction with the slurry.

2.Diffusion: The Diffusion area serves three basic functions:(i.) To deposit, (ii) to grow, and (iii) to anneal the films on the wafer surface to facilitate the creation of devices.

3..Etch: The purpose of the etching is to define the transistor by removing excess film material from the wafer surface through chemical and physical processes.

4.Films: The purpose of the Films processing area is to deposit thin film layers of conductive (oxides and metals) and non-conductive (insulators) materials on the wafer surface to control its electrical characteristics.

5.Implant: This area is responsible for doping materials and giving the semiconductor electrical characteristics.

6. Litho: The purpose of the Litho process is to create a pattern using ultraviolet light to transfer an image from a mask onto a wafer surface.

7.Wets: The wets area is responsible for cleaning the wafers by flushing chemicals on their surface and etching the unwanted materials on the wafer surface.

8.Ply: This area is concerned with checking and monitoring the inline defects.

1.4 Overview of the Photolithography Process

Photolithography is the most complex operation in wafer fabrication, and it requires the greatest precision. Photolithography is used to create multiple layers of circuit patterns on a chip. This area, where wafers are exposed using scanners or steppers, typically, comprises the bottleneck workstations. Also, the number of reticles available for a given layer of product type is limited. It is very important to develop schedules that ensure the maximum utilization of the equipment, in this processing area.

The main steps that a wafer has to undergo during a photolithography step are coating of the photo resist, exposure of the resist and the development of the resist. In the first step, the wafer is spun while the resist is deposited onto the wafer. The wafer is then baked to firm the photo resist and improve its adhesion to the wafer. The wafer is exposed to the UV light through the reticle, which contains the pattern for a few chips.

This alignment and exposure step is repeated until the whole wafer surface is exposed. The wafer is then sent to the developing step, where the exposed photo resist is removed with a chemical solvent, and then it goes through final bake to ensure that the unexposed photo resist adheres to the wafer.

The tool sets used in photolithography are characterized by the function they perform and by their limits on critical dimensions. The tool sets used in the model are the scanners and steppers. Scanners are used for processing critical layers as compared to steppers, which are used for processing non-critical layers. Processing of all layers of a lot on the same scanner or stepper ensures a better alignment of separate layers. So, it is a common practice to dedicate a lot to a scanner or a stepper. In this model, lot dedication is used for only the critical layers.

1.5 Objective

The motivation behind this research is to study the impact of lot dedication on the performance of various dispatching rules. The main areas for the analysis of this problem can be identified as follows:

- **Dispatching rules:** Use of dispatching rules constitutes the most common method for scheduling wafers in a wafer fab. Dispatching rules are easy to understand and implement. Proper dispatching rules need to be identified in order to reduce the cycle time.
- **Equipment utilization**: Utilization of a tool is critical from the throughput point of view. Greater utilization of a bottleneck tool will result in increased throughput.
- **Work-in-Process (WIP)**: Excessive WIP represents low efficiency of the operation. It also introduces variability in the throughput. It is necessary to keep WIP at a minimum level at each process step to reduce the holding cost and to ensure the smooth flow of jobs through the system.

1.6 Problem Statement

The problem that we address in this research can be defined as follows: Given a number of lots in a queue at a particular workstation, determine the lot to be

processed next so that the waiting time in the queue is minimized, which in turn results in an overall reduction of cycle time.

In this case, the jobs at different stages of production are queued up in front of a same tool. The issue then is which of these jobs to process next. This issue is further complicated by the fact that a job has to be processed at the same tool where it is processed for the first layer. This is an important requirement in the semiconductor manufacturing process, in order to achieve high quality fabricated wafers. Another issue is the dynamic environment in which the lots enter and exit the system periodically.

Thus, the objectives are:

(i) Determine how to allocate the scanners and steppers to different product types during their first visit, and (ii) decide when to make changeovers for setting up the tools for different product types and different layers during their subsequent visits, in order to utilize the tools efficiently in the Photolithography area as well as to reduce the overall cycle time under the following conditions.

a. There are different types of products in the system
b. There are different types of tools available, which can be used for a particular operation.
c. The type of flow is reentrant i.e. a lot can visit a given tool type many times during its production.
d. For critical layers, the lot has to visit the same tool on which its first layer is processed.
e. The tools are subjected to random breakdowns and preventive maintenance schedules.

Thus, the above problem can be viewed as a sequencing problem with special characteristics.

1.7 Proposed Methodologies

The, following are the two methodologies are suggested for the above problem.

1.Mathematical Programming Based Approach:

For the given routes and processing times of the product types, the entire problem is formulated as an Integer program. This integer program can be run by any commercial linear and integer programming software to give the optimal solution. The integer program uses the start time of the jobs at various operations and the availability of reticles at that time as variables. The objective function used in this formulation is to minimize mean cycle time. An effective solution methodology is proposed to solve this integer program.

2.Heurstic Algorithm based on a new Dispatching Rule:

The proposed approach is to reduce waiting time and increase utilization of the photolithography processing area, which would result in an overall cycle time reduction. This algorithm is written as a customized rule in C++ and is integrated into a simulation model of a facility using Autosched AP. The results of the performance of proposed algorithm is compared as against those of standard dispatching rules.

1.8 Thesis Outline

Chapter 1 describes the manufacturing environment characteristics and Provides an overview of the photolithography processing area. It also presents the statement of the problem addressed in the study along with its assumptions. Chapter2 provides a detailed literature review in the field of planning and scheduling of wafers in semiconductor manufacturing facility. Chapter 3 presents an analysis of various dispatching rules using characteristic curves. A new heuristic for scheduling lots on the photolithography area tools is presented. Furthermore a detailed analysis of the impact of lot dedication on the performance of various dispatching rules is described. Chapter 4 describes the mathematical based approach for scheduling lots on photolithography area tools. Finally, chapter 5 provides the conclusions and directions for future research.

Chapter 2 Literature Review

2.1 Introduction

In this research, we address the planning and scheduling of the photolithography processing area. The problem of scheduling the equipment in this processing area can be classified as that of scheduling with limited resources. As described above, for a wafer to be processed on a given tool, a reticle required for that layer must be present on that tool. The literature review includes work reported regarding the planning and scheduling of production in a semiconductor manufacturing facility and, in particular, the photolithography processing area.

In 1992 and 1994 Uzsoy, Lee and Vega [23] conducted an exhaustive survey of the work done regarding the planning and scheduling of production in semiconductor industry. They defined three types of planning and scheduling problems:

- Performance evaluation: Descriptive models employed to understand the system behavior.
- Production planning: Aggregate, long term production planning.
- Shop Floor Control: Short term control for the processing of orders.

The present review will focus on the following types of approaches used for the planning and scheduling problems in semiconductor manufacturing and, in particular, the photolithography processing area.

- Mathematical Programming based approaches.
  These can be further classified as Linear and Non-Linear programming approaches.
- Dispatching Rules

We also take a look at the simulation models, which are developed to evaluate the various performance measures.

2.2 Mathematical Programming based approach

Hung and Leachman [8] present a linear programming based planner and scheduler. The results given by the system are used as an input to a simulation model that validates the result. When the LP and simulation systems do not agree, the LP is reformulated until satisfactory agreement between the two models is obtained. The LP minimizes a weighted production cost and includes capacity, demand and processor availability. The use of two models ensures reliable results under varying conditions.

S.Kim, S.Yea and B.Kim [18] have proposed an approach for scheduling steppers in the photolithography area. They have developed a heuristic, two-phase algorithm for scheduling steppers for an 8-hour shift. In the first phase, to satisfy the given target cycle time within the fab, they determine target Work –In-Process (WIP) level at each layer. In the second phase, a mixed integer-programming model for allocating steppers is formulated. For this step, they have tested three heuristic algorithms for solving the machine allocation problem with the objective of keeping the actual WIP levels close to the target WIP levels after the current shift. They have claimed that one of the heuristics, using linear programming relaxation of MIP, generates schedules within 5% of the optimum values, on the average.

Glasssey, Shantikumar and Seshadri [6] address the job –release problem for a single product, high volume semiconductor fab. The objective is to minimize the cycle time. The linear control rules are based on intersecting hyperplanes and determine the time of release. These rules can be applied to the fab model developed by Wein[22]. Lou and Kager [12] worked along the same direction. They minimize the WIP while maintaining the output. The validation of their model is achieved by comparing its results to two other simulation based schedulers.

Jason McCune [14] has proposed a linear programming based model, which attempts to reduce the overall cycle time at the operation by reducing the range of tool utilization within the toolset. A secondary objective statement is used to include the

objective of minimizing the utilization range of the toolset and maximizing the layer load on preferred tools

Connors and Yao [4] paid attention to the total demand for a multi-product fab. The authors define numerous technological constraints and assume a random yield. The optimization of the production is achieved with the help of six linear programs. The main contribution of this work is the integration of the constraints that aim at reaching the expected demand set. The problem to meet production targets in an IBM facility motivated the design of this system.

Bai, Srivastsan and Gershwin [2] decompose the scheduling problem into a hierarchical structure to allow for the integration of non-linear and linear programming. The approach applies non-linear programming to establish long run values such as the set-up rate. At a lower level, the system executes a linear programming computation to find the production rate etc. The lowest level is controlled by different DRs that depend on the results previously obtained.

Mehta and Uzsoy [15] deal with the scheduling of several incompatible product families. The minimization of total tardiness appears to be NP-hard. Dynamic Programming (DP) optimally solves small size systems but larger problems cannot be treated within reasonable amount of time. By applying a decomposition algorithm to the large size problem, they divide it into smaller ones that can be solved using DP. The results of the heuristic are obtained quickly and are reported to be robust and near optimal.

2.3 Dispatching Rules

The dispatching rules (DR) are one of the most widely used tools to schedule the wafer manufacturing process. They are applied to select which job to process next on a particular tool. The use of the DR is often motivated by the fact that they are fast and simple to implement in the dynamic manufacturing environment.

Lu, Ramaswamy and Kumar [13] developed deterministic rules based on the Least Slack (LS) policy, in order to smooth out the mean and variance of cycle times. The proposed rules are as follows:

LS policy: $Slack_k$ = (Set Due Date) $_k$ – (Estimated Remaining Processing Time) $_k$

The highest priority is given to a lot k with the least slack.

FSVCT policy: S_k =(Release time of lot) $_k$ – (Estimated Remaining Processing Time) $_k$

The highest priority is given to a lot k with the least value of S.

FSMCT policy: S_k = ((n/λ) - (Estimated Remaining Processing Time) $_k$

Where n is the number of the lot and λ is the throughput rate.

The highest priority is given to a lot k with the least value of S_k.

Using simulation, the authors have compared the results of the above rules to those obtained using standard dispatching rules. They have found that the "fluctuation smoothing of variance of the cycle time (FSVCT)" policy efficiently reduces the variance of the cycle time. The fluctuation smoothing policy for mean cycle time (FSMCT) decreases the mean cycle time and tends to reduce its variance by avoiding bursting in the arrivals at buffers. It is also claimed that this rule reduces the cycle time by more than 20% and its variance by more than 40% compared to FIFO. However, the effects of these rules on other performance measures such as WIP and machine utilization are not known.

Hung and Yang [7] address the due date related criteria. They consider DRs like Expected Due Date (EDD), Shortest Remaining Processing Time (SRPT), Urgent Factor Index (UF), as well as other rules with the aim of balancing the line. These DRs are applied on a model of a wafer fab that includes a few machines and assume deterministic processing times. The efficiency of each DR is presented under different number of machines. The results presented are dependent on the model considered.

Kayton, Teyner, Schwartz, and Uzsoy [9] compare many common DR in a complete simulation study. They have taken into account the break down of the tools.

The authors outline the significant effect of non-bottleneck downtimes on the mean cycle time.

Wein[24] has reviewed 12 different DRs, simulated their applications using the available data of two existing fabs data under six common distributions. The extensive amount of result is clearly summarized to enable comparisons. It appears that no rules dominate in performance but the author observes that if the input distribution is known, some DR can be disregarded since they cannot perform better than others. The unique point of this paper is the number of rules considered and their application to real world data.

Ying –Jen Chen, et, [3] implemented the dispatching rules at Macronix's fab to reduce the cycle time. They developed a multi –criteria rule based on slack rule, next queue rule, lot grade and critical layer. This resulted in cycle time reduction of 31.3 % from May 1997 to July 1998.

Related to DR efficiency, the work of Kumar and Kumar [11] addresses the performance bounds of Markovian queuing network and DR. The DRs considered in the article are the First Buffer First Serve (FBFS), Last Buffer First Serve (LBFS). These DRs are specific to the reentrant flow. The authors analyzed the behavior of these policies under traffic conditions varying from light to very heavy. They observed that the efficiency of the FBFS and LBFS policies could be improved by the addition of constraints on buffer capacity. The authors have considered both open and closed queuing networks and have established performance bounds for different models. The computation of bound for such rules provides important information about DR limitations and enables one to select easily the most efficient policy for a particular system under a pre-defined traffic condition.

2.4 Simulation Model

A joint project between the JESSI/MST and SEMAECH in 1995 studied the single effect case studies conducted under the Measurement and Improvement of Manufacturing Project. The studies considers the effect due to alternative equipment, batching, breakdowns, dispatching/sequencing, end of shift, factory shutdown, hot lots/ engineering lots, inspection yield, level of operator cross training, lot sizes, mix, operator availability, order release/WIP limits, redundant equipment, reentrant flow, rework, setup and time bound sequences.

El Adl, Rodriguez and Tsakalis [5] focus their study on the hierarchical aggregation/disaggreation model of the facility. This decomposition yields smaller models that can be scheduled through discrete event simulation within a shorter amount of time. This strongly enhances the performance of the scheduler since excessive computation time is the main disadvantage of this type of system.

Thompson [22] describes the integration of simulation techniques in the semiconductor industry and presents the perspective given by the fast pace of development of the simulation program. The simulation tools presented in his paper aim at solving two of the main wafer fab problems: when to release lots into production and what each piece of equipment should work on next. The simulation system may be used in three different modes: offline policy development, predictive planning and reactive scheduling.

Schoemig [19], used simulation models to describe the influence of variability caused by machine and tool availability. These simulation models were built using Factory Explorer ™ simulation tool. The results of the simulation model indicate that reducing the variability in the manufacturing system leads to lower and predictable cycle times.

Schoemig and Mittler [20] use a simulation model to investigate the performance of dispatching rules in order to reduce the mean and standard deviation of cycle times using discrete event simulation. They conclude that fluctuation-smoothing policies FSMCT and FSVCT achieve best results.

2.5 Conclusions

Lot of research work has been carried out in the field of production planning and Scheduling of work in a wafer fab. There are various techniques and models that have been developed for solving these types of problems. There has been a lot of work done in the field of shop floor control.

Mathematical programming based models are useful because of their ability to provide optimal or near-optimal solutions to the scheduling problems. The main disadvantage of the mathematical programming models is that they fail to provide the solutions for large size problems in a relatively short time.

The shop floor control models based on the dispatching rules are most commonly used on the shop floor. They are simple to implement in a real life based environment. The main drawback of dispatching rules is that they do not guarantee an optimal solution. Various heuristic based approaches are also developed using a combination of dispatching rules.

Simulation based model have been extensively used for performance evaluation of a wafer fab. The reasons for this are the availability of sophisticated simulation software packages and improved computer hardware, which makes building simulation models easier and reduces the computational expense of the resulting models.

Very little work is carried out in the planning and scheduling of photolithography area as compared to the work done for the planning and scheduling of the overall wafer fabs. A study to determine the impact of lot dedication on the performance of various dispatching rules has not been reported.

Chapter 3 Dispatching Rules for the photolithography area

3.1 Introduction

In this chapter, we describe a methodology to analyze the performance of dispatching rules and develop a dispatching rule for the photolithography processing area. The chapter is divided into three sections. The first section of the chapter deals with the characteristic curve model approach for analyzing the performance of various dispatching rules. A simulation model for photolithography tools is built and the performance of dispatching rules are analyzed for different lot dedication schemes.

The second section of the chapter describes the proposed heuristic approach. The proposed heuristic is applied to photolithography tools and the all the other tools in the Fab are modeled as black boxes. The results of the performance of the proposed heuristic as against those of standard dispatching rules are presented. This section also investigates the impact of lot dedication on the performance of dispatching rules.

3.2 Dispatching rules

Dispatching rules ranks the jobs, waiting for processing, on the basis of various attributes of the lot or the tool or a combination of both. Dispatching rules have been proven useful in the industry for scheduling lots at a given tool. They are easy to implement and they can be applied in real time. Dispatching rules do not guarantee attainment of an optimal solution, but they find good solutions in a relatively short amount of time.

There are different ways to classify dispatching rules. One such way is in accordance with the type of information they are based upon. A local rule uses the information pertaining to the queue stationed in front of the tools, like for example, FIFO. On the other hand, a global rule uses information about the system outside of a given queue. An example of this rule is the LLA (Least lot ahead). This rule, when applied at a station, considers the lots present in the queues of stations to be visited for its next step of processing. This concept can be extended over several steps to be processed hence.

Generally, dispatching rules are useful for finding reasonably good schedules with respect to a single objective such as makespan or the total completion time. But, in a real

life environment, there is typically a combination of objectives that need to be achieved. Ranking of the lots based on only one criterion may not yield best results. Hence, there arises a need of a composite dispatching rule. A standard dispatching rule is based on a single attribute of a lot or a tool. A composite dispatching rule is a combination of standard dispatching rules. An attribute can be thought of as a property associated with a lot or a tool. For example, attributes of a lot may be priority, due date, or processing time. Examples of tool attributes are throughput rate, number of lots waiting in the queue to be processed. A composite dispatching rule, for example, would rank the lots based on their priorities first and then by due date and followed by the number of the lots ahead in the line.

3.3. Characteristic Curve

According to Little's Law, cycle time for a given production rate (i.e. the throughput rate), is proportional to the mean number of wafers in the plant. This definition of cycle time does not take into account the variability in the lot arrival times, process time variability, tool utilization and equipment downtime. In order to include the impact of variability, we use the concept of the characteristic curve. This characteristic curve concept is typically used for a single tool. However, for the problem on hand, we have extended this concept to the overall fab, which we will describe later.

The definition of Characteristic Curve is introduced by Fowler and Robinson [17]. It is also referred to in the literature as "operating curve methodology "by Aurand and Miller [1].

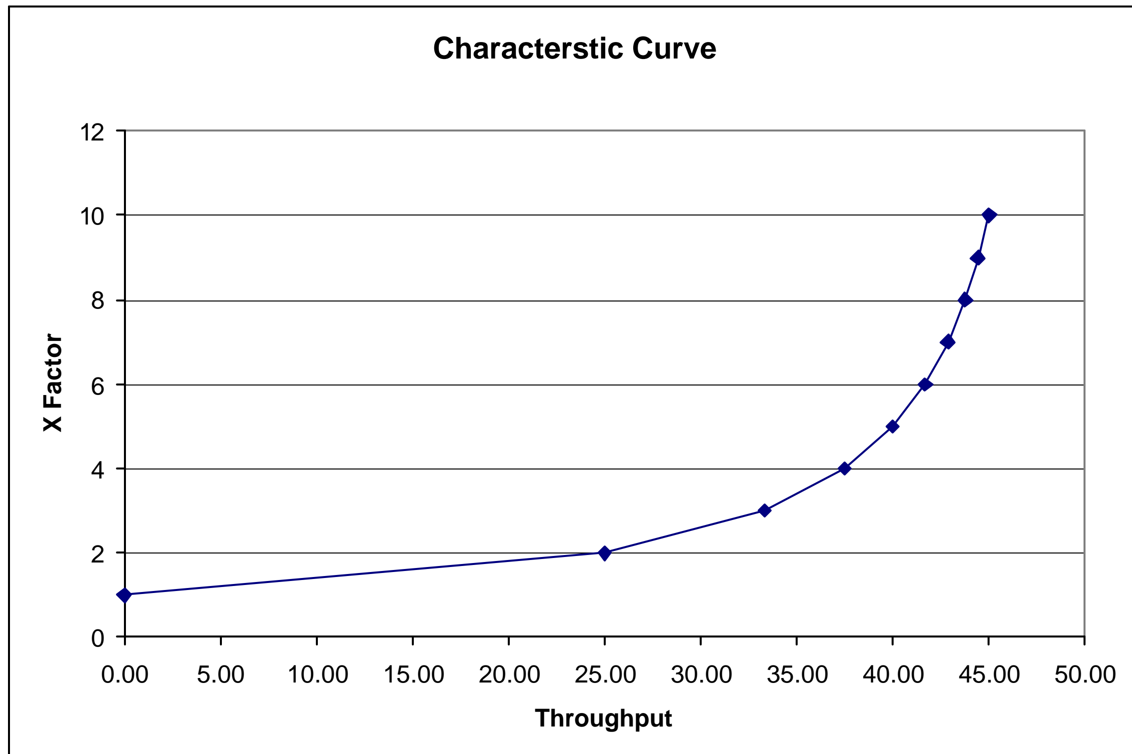
Characteristic curve is a plot of cycle time multiplier (X factor, which is the ratio of average cycle time to the theoretical cycle time.) versus the throughput rate.

These are related by the following expression [1]:

$$X \text{ Factor} = \propto U/(1-U) + 1 \qquad (1)$$

Here $\propto$ = coefficient of variability, which includes the variability in the arrival of the jobs at a tool, tool uptime variability and process variability, U= Utilization of the tool (in this case, the average utilization of all the tools is considered). Also, utilization, U = Throughput / Capacity. These formulae are used to construct the characteristic curve.

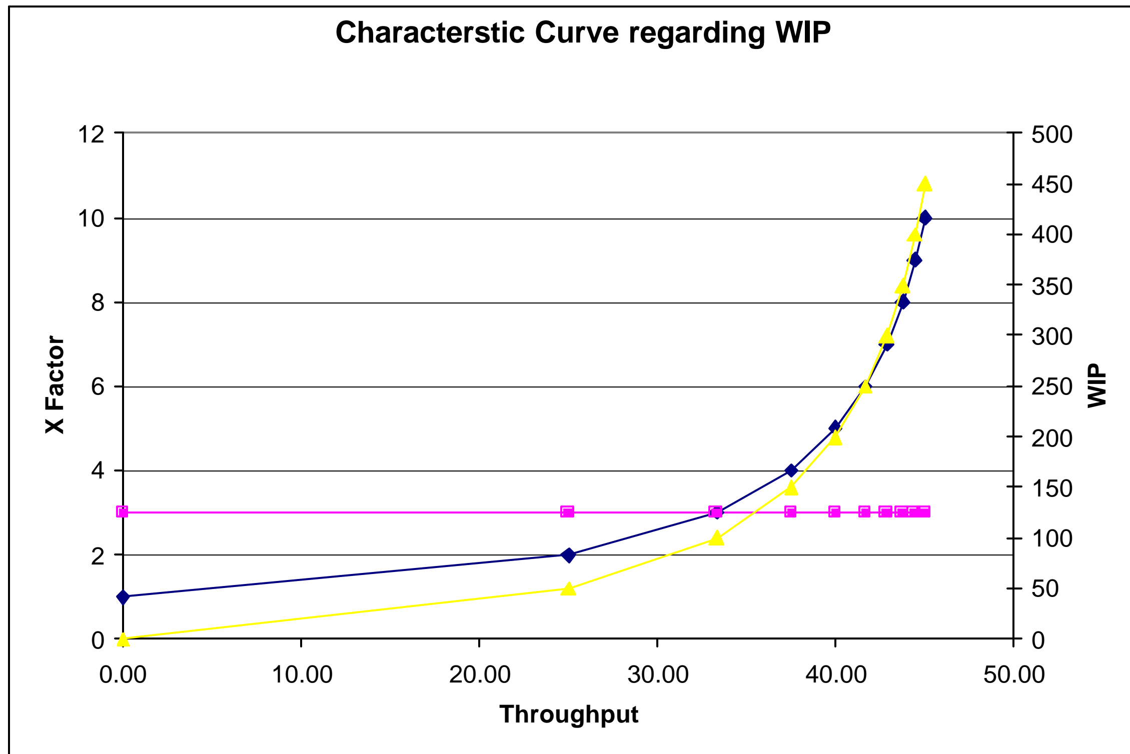
FIGURE3.1: CHARACTERISTIC CURVE



The graph in Figure1 is drawn for a tool having a capacity of 50 units/hr. The value of ∝ is assumed to be equal to 1. The shape of the curve is dependent of the value ∝ used. If the value of ∝ is increased, then the curve is less flat. So, for the same X factor if we increase utilization, then the throughput rate also increases but so does the WIP level. Hence, if we have a certain target cycle time, we can determine corresponding utilization and the throughput.

In the above graph, there is no representation of the WIP. So, using Little's Law, we substitute WIP/throughput for cycle time and determine WIP levels for the given throughput.

FIGURE 3.2: CHARACTERISTIC CURVE REGARDING WIP



The graph in Figure 2 shows the WIP levels associated with throughput. For the above graph, X Factor of 3 is achieved with a throughput of 34 units and with a WIP of 100 units. For the same capacity, if we want to achieve a higher throughput, there is an increase in the X factor and the WIP level. So, in the above case, to achieve a throughput of 38, there would be an increase in X factor by 1 and WIP level by 50 units.

3.4 Description of the Simulation Model

The simulation model for photolithography area was developed by using AutoSched AP 7.0 software distributed by Brooks- PRI Automation. The inputs to the simulation model are given using Microsoft Excel file format. The inputs contain various data files for factory resources, products and demand. There are different worksheets used for defining the various components of the simulation model. They are as follows:

1. The Orders Worksheet
2. The Parts Worksheet
3. The Routes Worksheet
4. The Stations Worksheet
5. The Generic Resources (Reticles) Worksheet
6. The Down Calendar Worksheet
7. The Preventive Maintenance Worksheet

1. The Orders Worksheet

This Worksheet defines lots and their starting time in the model. Lots consist of a number of pieces of a part defined in the part file. The Orders worksheet is attached in Appendix A.

2. The Parts Worksheet

This file defines the types of the products that are manufactured in the facility. The part file specifies the name of each part type and the route that it follows. The Parts worksheet is attached in Appendix B.

3. The Routes Worksheet

This file defines the processing steps that parts must go through to be manufactured. Each step in the route uses a resource. The Routes worksheets are attached in Appendix C.

4.The Stations Worksheet

This file defines the stations used in the factory. Each station can be a machine or a area in the factory. The Stations worksheet is attached in Appendix D.

5.The Generic Resources Worksheet

This file defines the reticles used in the fab. The Generic Resources worksheet is attached in Appendix E.

6.The Down Calendar Worksheet

This file defines the down time data for the stations. The Down Calendar worksheet is attached in the Appendix F.

7.The preventive maintenance worksheet

This file defines the preventive maintenance schedule followed by the stations. The preventive maintenance worksheet is attached in the Appendix G.

There are other worksheets, which define standard action lists, customized action lists to be performed at various steps, standard functions, classes, and non-standard scheduling rules.

The output of the simulation model can be viewed in the Microsoft Excel Format. There are different worksheets for statistics collected for different entities. These are as follows:

1. Lot Report
2. Station Report
3. Performance Report
4. Generic Resources Report

Using the statistics collected from the model, the characteristic curve is generated for each dispatching rule and the curve with the least slope is selected.

3.5 Results of the experimentation done to study the performance of various dispatching rules applied in the Photolithography processing area

3.5.1 Introduction

This experimentation is done to study the performance of dispatching rules under various lot dedication schemes.

3.5.2 Dispatching Rules

The following dispatching rules are used in the analysis.

1.FIFO: The lots are ranked in the order “first in and first out”. The lot that arrives the stage first is ranked first in the queue.

2.ESD: Earliest start date. The lots are ranked in the order of their start date. The lot with the earliest start is ranked first.

3.LLA: Least Lots Ahead. The lot that has the fewest lots (of any part type) at its next step is ranked highest.

4.LPR: Least Percent (of processing time) Remaining. The lots are ranked in order of the percentage of their remaining processing time.

(Percent remaining = remaining proc. Time /(actual proc. Time + remaining proc. Time))

The actual processing time is the processing time the lot has incurred up to the current step.

5.LTR: Least (processing) Time Remaining. The lots are ranked in order of their remaining processing time. The lot with the least remaining processing time is ranked first. Remaining processing time is the sum of processing times at all remaining steps.

3.5.3 Performance measures

The metrics for analyzing the performance of dispatching rules are described as below:

1.Lots completed: The number of lots that are completed during the simulation period.

2. Average Cycle time: The average cycle time for 4 products.

3. STD: standard deviation of the cycle time.

4.WIP: The average WIP in the system.

5.Utilization: The average utilization of the all the tools.

3.5.4 Experiment Design

The simulation model is based on “constant start”. i.e. the lots enter the in the fab at a predefined uniform interval. In this model, the following assumptions are made.

i. The number of reticles is kept constant

ii. There is no rework of lots.

iii. The lots are never split during the entire process.

Under these conditions, the model is run for 4 different levels of lot dedication.

The experimentation is a two – phase process.

a. Phase I: Warm-up Period

To make comparisons, the simulation of every scenario has to start from the same state. Since the warm-up period of each dry run may vary, we decided not to collect data when the system is empty; instead we always started to collect data from a steady state with an initial WIP. To obtain this steady state, we run a warm-up simulation for 50 days.

b. Phase II: Steady state period

With the initial WIP obtained, we run the simulation model for 50 more days and then the data is collected and the performance measures are calculated.

3.5.5 Results

The results regarding the performance of standard dispatching rules are compared under different level of lot dedication schemes considering two cases. In the first case, we assume tool breakdowns and preventive maintenance and, in the second case, we assume that there are no breakdowns or preventive maintenance. The product mix and the loading policy are kept the same in both the cases. The results are shown as below.

3.5.5.1 With PM and Breakdown

Case 1. 3-Level Lot Dedication

In this case a lot is grouped 3 times during its process flow. i.e. the lot, after being dedicated to a tool for first layer, can again be dedicated to some other tool after processing some of its critical layers. For the three level lot dedication this is done twice, after the first allocation. In this case, we assume that only 1 product has three levels of lot dedication while the other products have 2-level lot dedication due to processing requirements.

TABLE 3.1: COMPARISON OF DISPATCHING RULES FOR 3-LEVEL LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
LTR	1366	45.76	2.79	61.89	1668
LPR	1364	45.79	2.80	61.91	1668
LLA	1361	45.94	2.72	60.8	1675
ESD	1372	45.72	2.60	61.96	1665
FIFO	1345	45.93	1.55	60.57	1678

FIGURE 3.3: CHARACTERISTIC CURVE FOR 3-LEVEL LOT DEDICATION

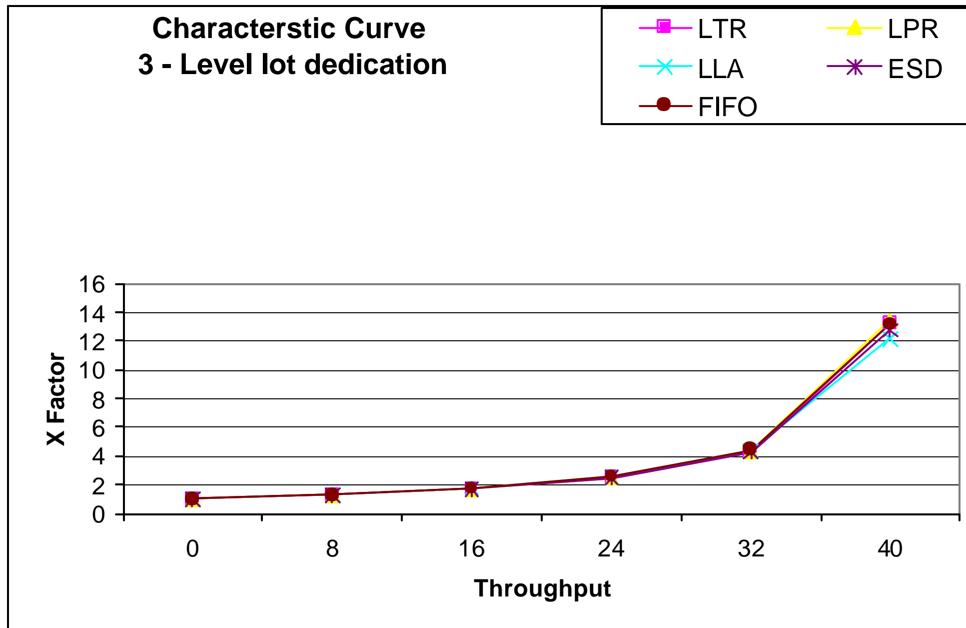
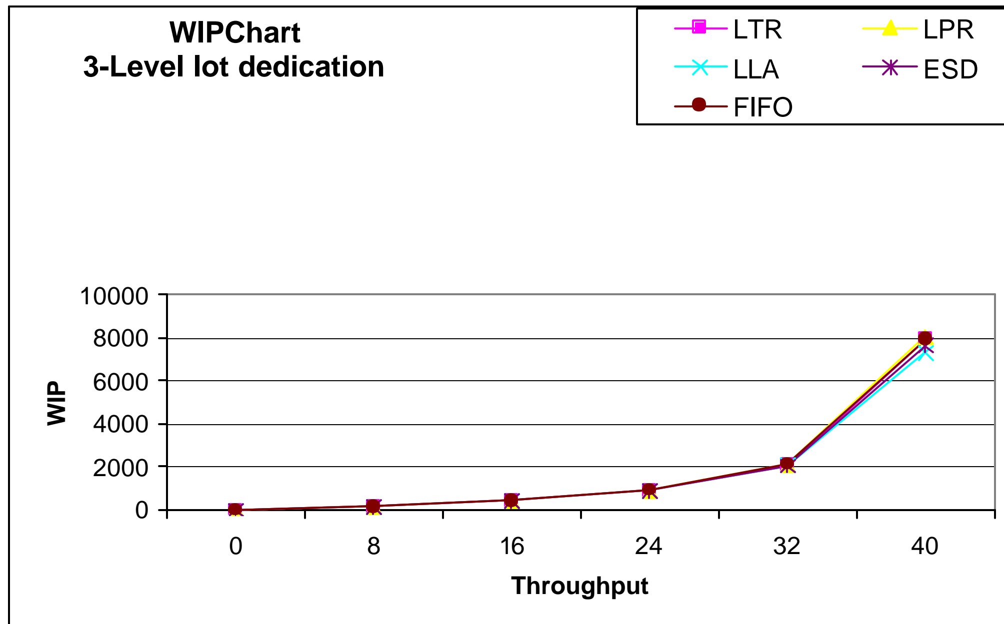


FIGURE 3.4: CHARACTERISTIC CURVE REGARDING WIP FOR 3 -LEVEL LOT DEDICATION



From Table 3.1, there does not appear to be a significant difference in terms of throughput and cycle time, also the performance of dispatching rule is similar under varying loading conditions as seen from Figure 3.3 and Figure 3.4.

Case 2. 2- Level Lot dedication

In this case, a lot is grouped twice during its process flow. i.e. the lot, after being dedicated to a tool for the first time, can again be dedicated to some other tool after processing some of its critical layers.

TABLE 3.2: COMPARISON OF DISPATCHING RULES FOR 2- LEVEL LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
LTR	1362	45.39	2.98	61.26	1658
LPR	1365	45.40	2.90	61.28	1658
LLA	1402	45.34	2.71	61.31	1657
ESD	1367	45.41	2.84	61.39	1657
FIFO	1413	45.36	1.71	61.34	1657

FIGURE 3.5: CHARACTERISTIC CURVE FOR 2- LEVEL LOT DEDICATION

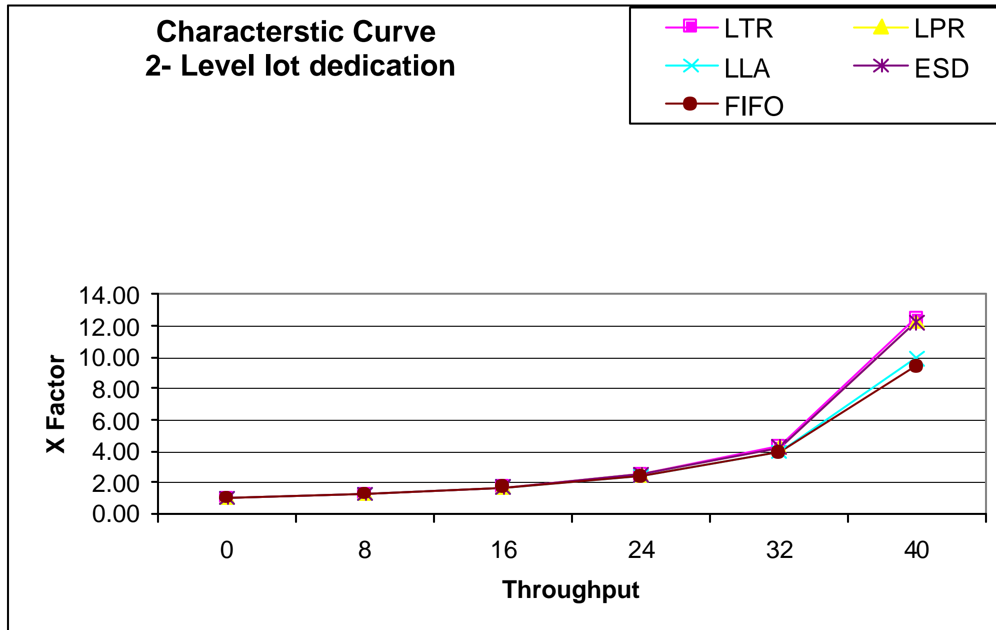
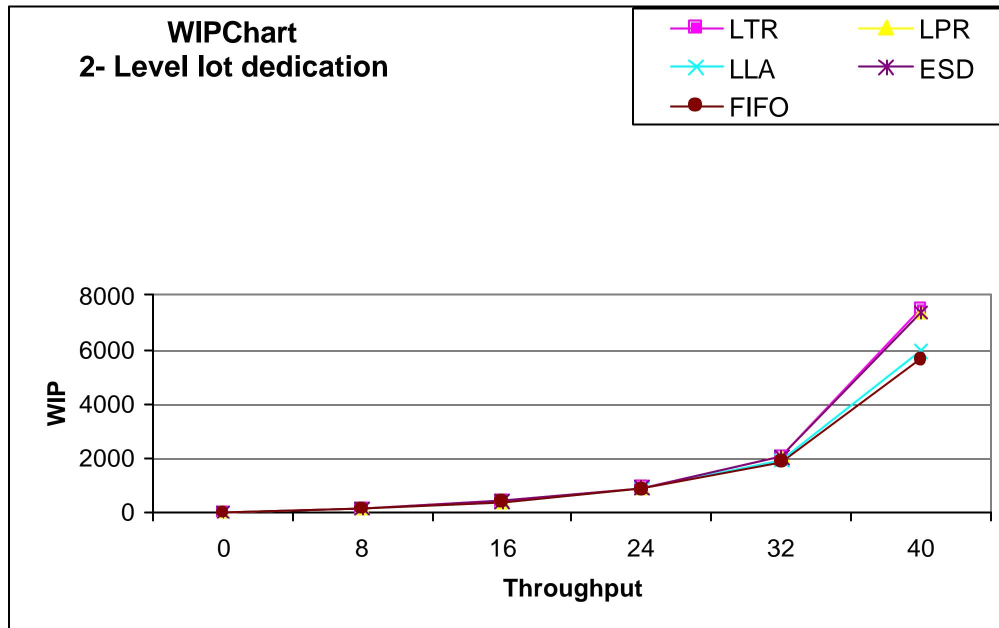


FIGURE 3.6: CHARACTERISTIC CURVE REGARDING WIP FOR 2 LEVEL LOT DEDICATION



From Table 3.2 we can see that FIFO performs the best in terms of throughput, cycle time and standard deviation of cycle time. Also from Figure 3.3, FIFO seems to have the least slope, which indicates less variability in terms of cycle time and better performance as compared to other dispatching rules under varying load conditions.

Case 3. 1- Level lot dedication

In this case, a lot is grouped only once during its process flow. i.e. a lot, after being dedicated to a tool for the first time, visits the same tool for processing all the critical layers.

TABLE 3.3: COMPARISON OF DISPATCHING RULES FOR 1- LEVEL LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
LTR	1401	45.93	2.90	62.39	1652
LPR	1402	45.94	2.94	62.51	1652
LLA	1452	46.32	2.53	63.55	1662
ESD	1404	46.04	2.61	62.3	1654
FIFO	1447	46.33	2.40	63.46	1662

FIGURE 3.7: CHARACTERISTIC CURVE FOR 1- LEVEL LOT DEDICATION

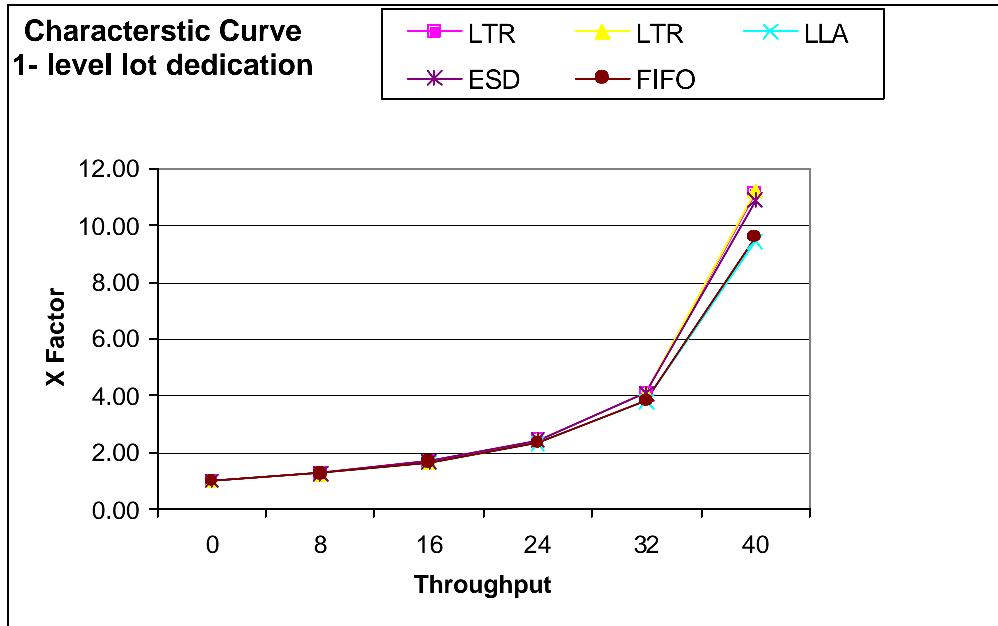
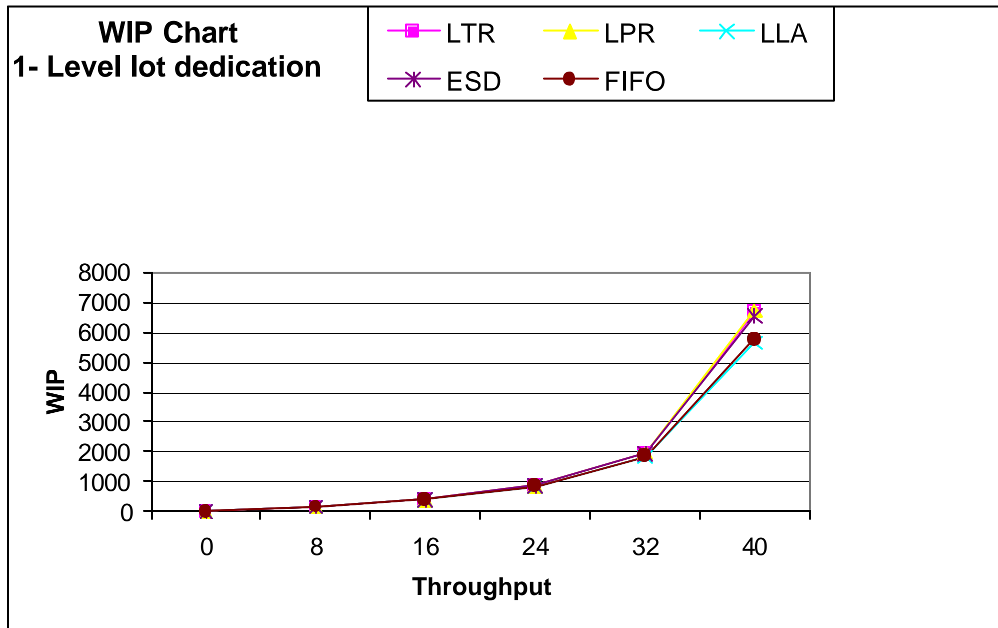


FIGURE 3.8: CHARACTERISTIC CURVE REGARDING WIP FOR 1 LEVEL LOT DEDICATION



From Table 3.3, we can see that LLA and FIFO give similar performances. They perform better than other dispatching rules in terms of throughput. Also, from Figure 3.7 and 3.8, we can see that they have flatter shaped curve as compared to those of other dispatching rules.

Case 4. No Lot dedication

TABLE 3.4: COMPARISON OF DISPATCHING RULES FOR NO LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
LTR	1498	45.07	3.46	63.26	1617
LPR	1491	44.97	3.43	62.32	1615
LLA	1391	48.69	4.75	63.71	1728
ESD	1486	45.90	4.11	61.7	1625
FIFO	1402	48.58	3.81	63.87	1716

FIGURE 3.9: CHARACTERISTIC CURVE FOR NO LOT DEDICATION

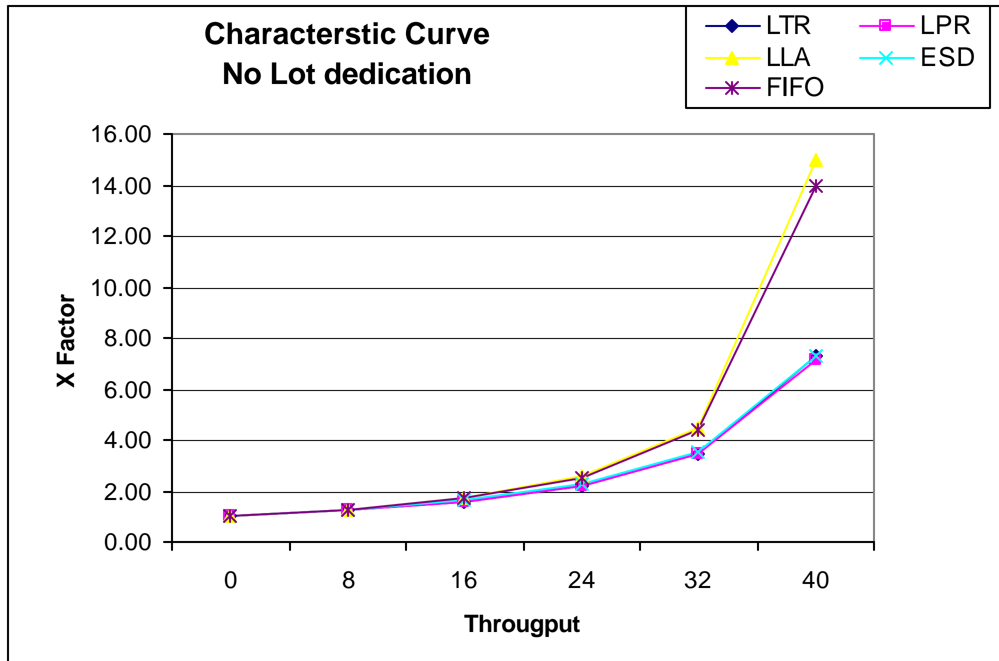
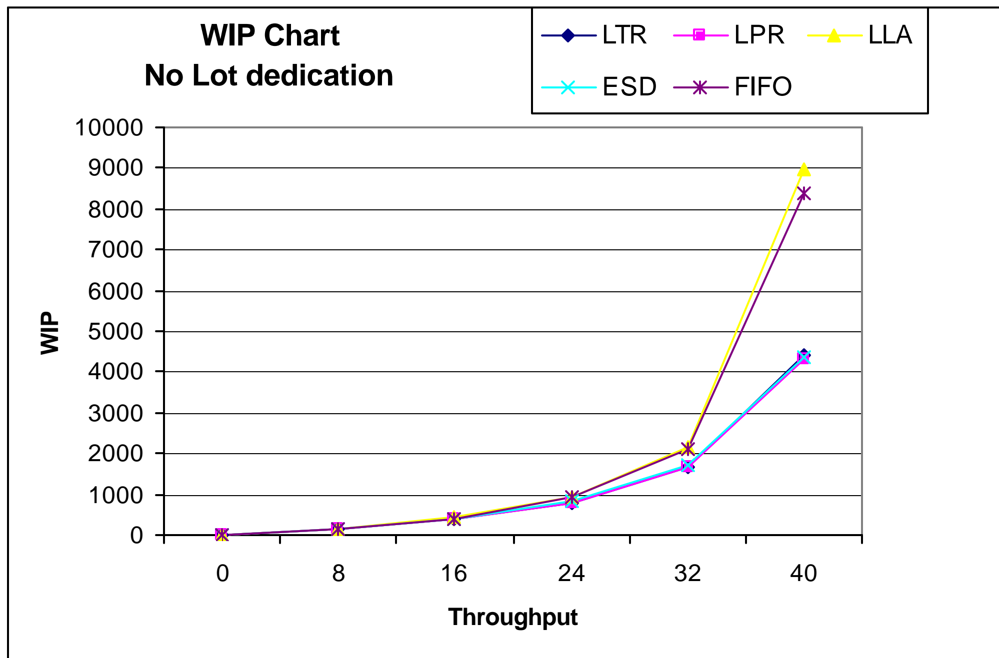


FIGURE 3.10: CHARACTERISTIC CURVE REGARDING WIP FOR NO LOT DEDICATION



From Table3.4, we can see that LTR, LPR and ESD give similar performances. They perform better than other dispatching rules in terms of throughput. Also, from Figure 3.9 and 3.10, we can see that they have a more flatter shaped curve as compared to those for the other dispatching rules.

3.5.5.2 Without PM and Break Down

Case 1. 3- Level lot dedication

TABLE 3.5: COMPARISON OF DISPATCHING RULES FOR 3- LEVEL LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
ESD	1481	46.06	3.21	64.39	1645
LTR	1475	46.03	3.16	64.31	1645
LPR	1475	46.04	3.12	64.32	1645
LLA	1471	46.01	2.87	64.37	1647
FIFO	1464	46.02	2.86	64.3	1648

FIGURE 3.11: CHARACTERISTIC CURVE FOR 3-LEVEL LOT DEDICATION (NO PM/BREAKDOWN)

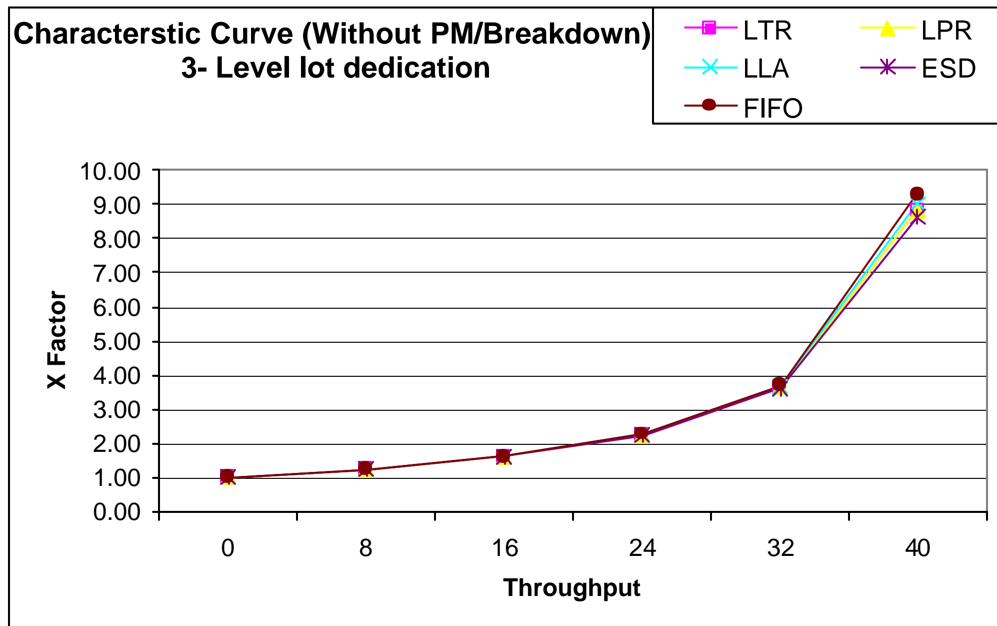
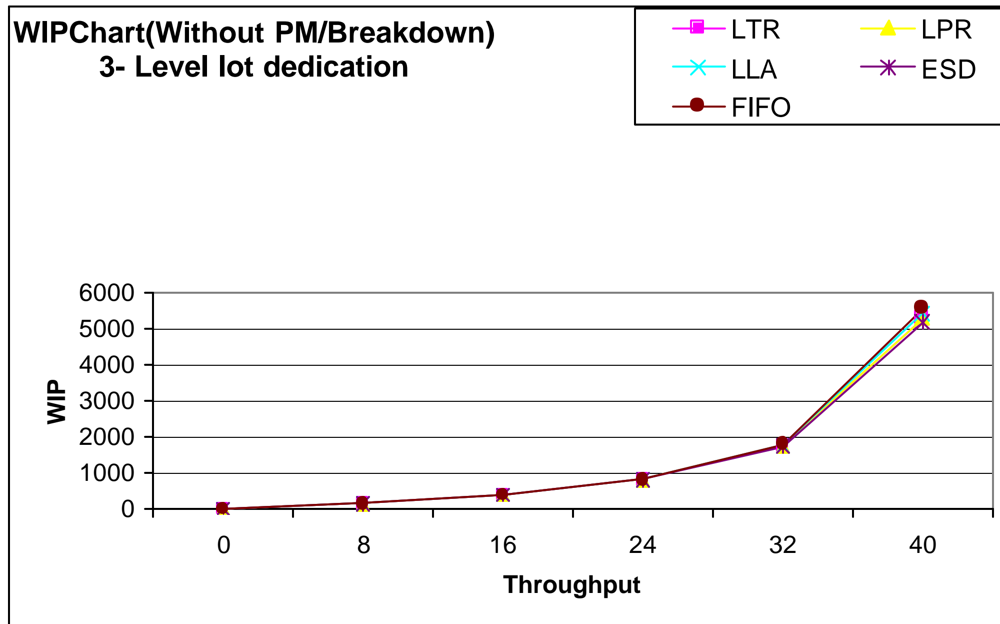


FIGURE 3.12: CHARACTERISTIC CURVE REGARDING WIP FOR 3- LEVEL LOT DEDICATION (NO PM/BREAKDOWN)



From Table 3.5, Figure 3.11 and Figure 3.12 we can infer that performance of all dispatching rules are identical. None of the dispatching rule dominates the other with respect to all performance metrics.

Case 2. 2- Level lot dedication

TABLE 3.6: COMPARISON OF DISPATCHING RULES FOR 2- LEVEL LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
ESD	1475	45.91	3.24	64.35	1640
LTR	1470	45.88	3.22	64.33	1641
LPR	1470	45.87	3.19	64.33	1641
LLA	1481	45.88	3.06	64.33	1642
FIFO	1479	45.82	2.97	64.29	1641

FIGURE 3.13: CHARACTERISTIC CURVE FOR 2- LEVEL LOT DEDICATION (NO PM/ BREAKDOWN)

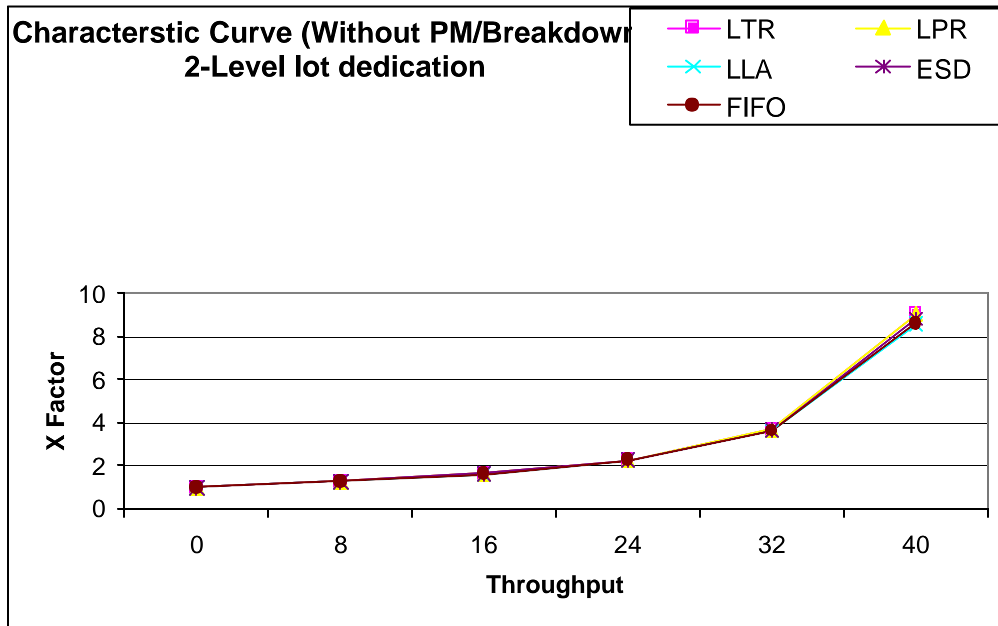
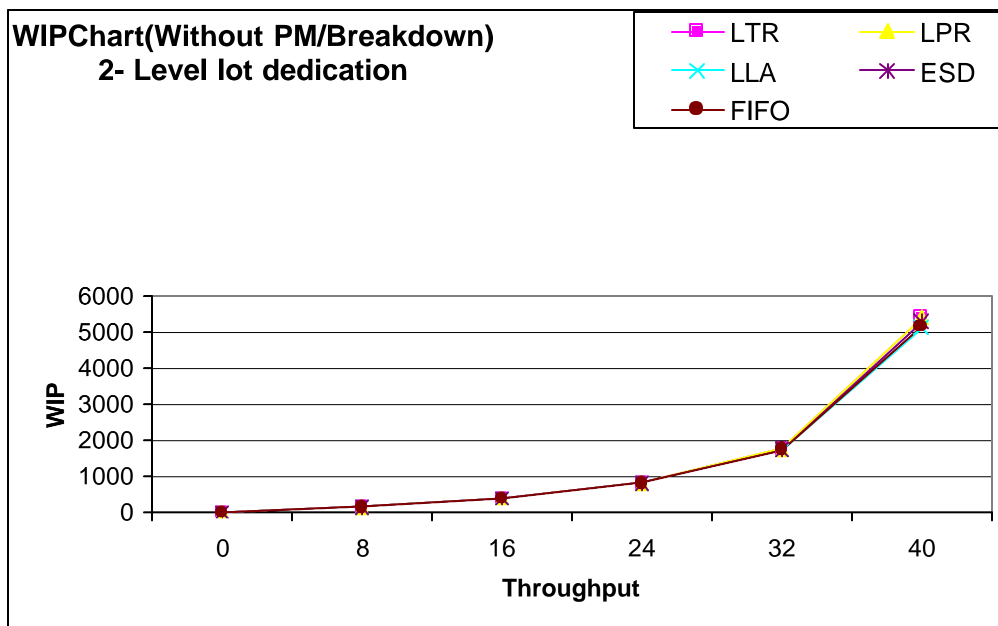


FIGURE 3.14: CHARACTERISTIC CURVE REGARDING WIP CHART FOR 2- LEVEL LOT DEDICATION(NO PM/BREAKDOWN)



In this case also as seen from Table3.6, Figure 3.13 and Figure 3.14, all the dispatching rules show similar performances with regard to throughput and cycle time.

Case 3. 1 Level lot dedication:

TABLE 3.7: COMPARISON OF DISPATCHING RULES FOR 1- LEVEL LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
ESD	1465	45.36	2.66	63.94	1624
LTR	1504	45.01	2.14	64.37	1616
LPR	1497	44.96	1.90	64.6	1615
LLA	1471	45.89	2.20	64.77	1646
FIFO	1464	45.87	2.32	64.78	1639

FIGURE 3.15: CHARACTERISTIC CURVE FOR 1- LEVEL LOT DEDICATION (NO PM/BREAKDOWN)

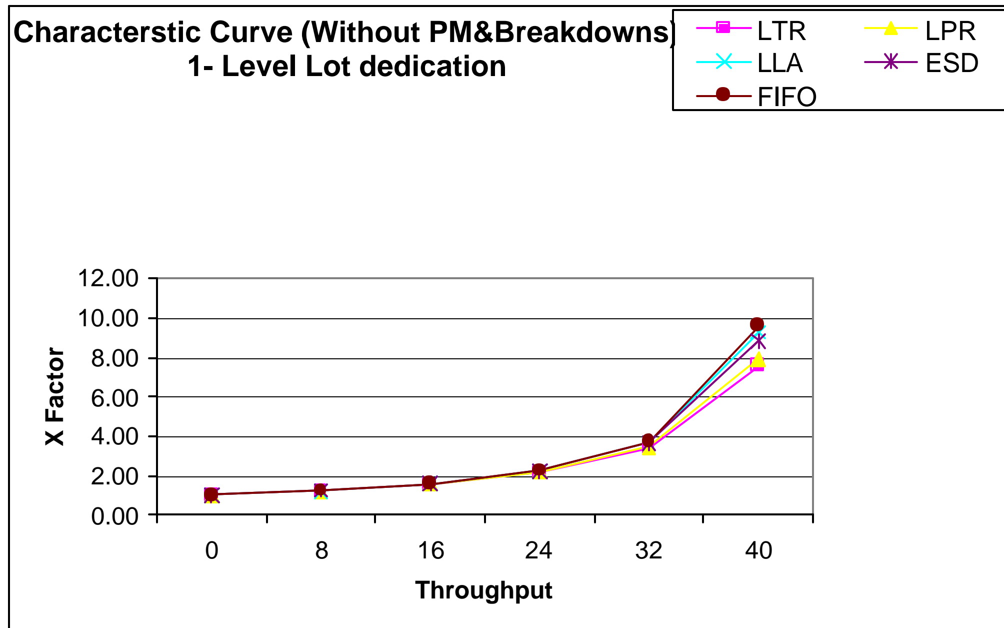
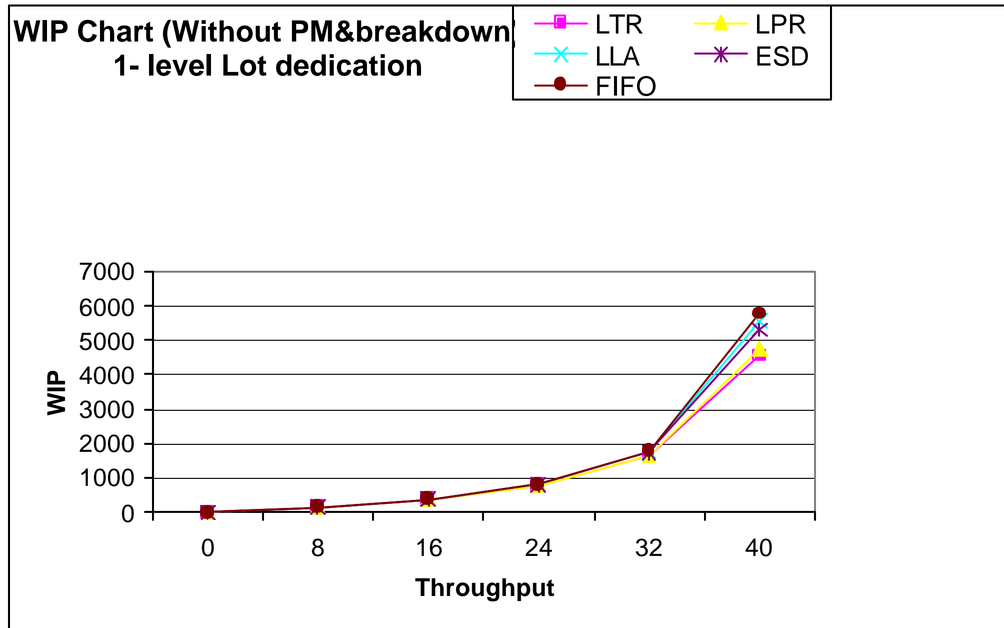


FIGURE 3.16: CHARACTERISTIC CURVE REGARDING WIP FOR 1- LEVEL LOT DEDICATION (NO PM/BREAKDOWN)



In this case as seen from Table 3.7 LPR and LTR out perform other dispatching rules in terms of throughput and cycle time. Figure 3.15 and 3.16 indicate that their performances are robust under different loading conditions.

Case 4. No Lot dedication

TABLE 3.8: COMPARISON OF DISPATCHING RULES FOR NO LOT DEDICATION

Rule	Lots Completed	Average Cycle Time	Std. Deviation of Cycle Time	Utilization %	Average WIP
LTR	1518	44.88	2.86	64.39	1602
LPR	1557	45.04	3.13	64.2	1601
LLA	1459	47.55	3.68	65.46	1683
ESD	1549	45.68	3.01	63.94	1609
FIFO	1471	47.44	2.78	65.67	1672

FIGURE 3.17: CHARACTERISTIC CURVE FOR NO LEVEL LOT DEDICATION (NO PM/BREAKDOWN)

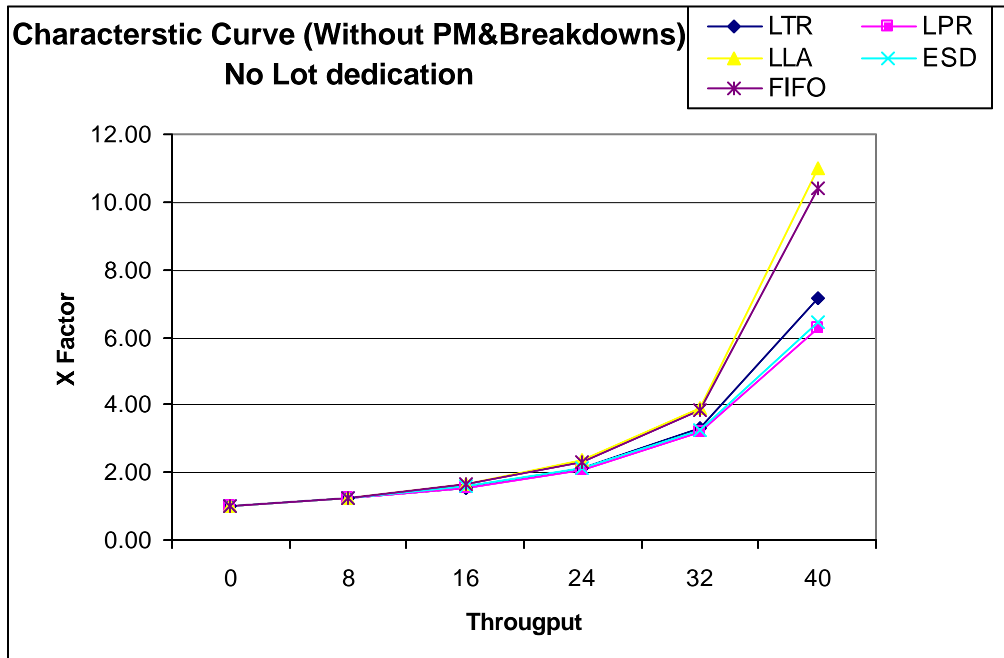
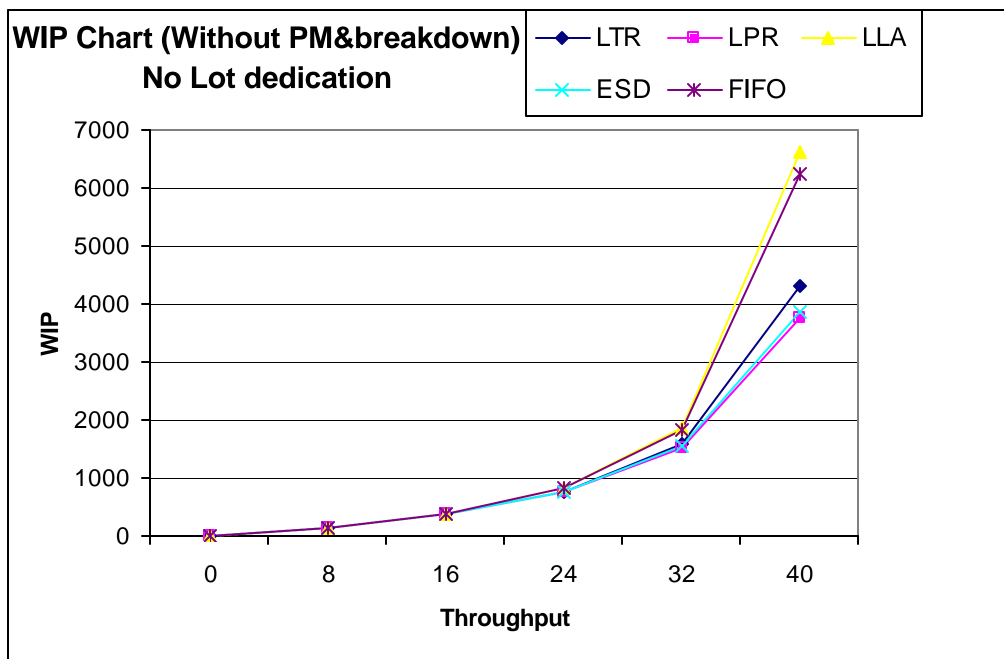


FIGURE 3.18: CHARACTERISTIC CURVE REGARDING WIP FOR NO LOT DEDICATION (NO PM/BREAKDOWN)



In this case LPR performs the best in terms of throughput as seen from Table 3.8. The cycle time for LPR is comparable to those of ESD and LTR. These rules perform better

than others as seen from Figure 3.17 and Figure 3.18. They have a flat shaped curve, which indicates less variability in the system.

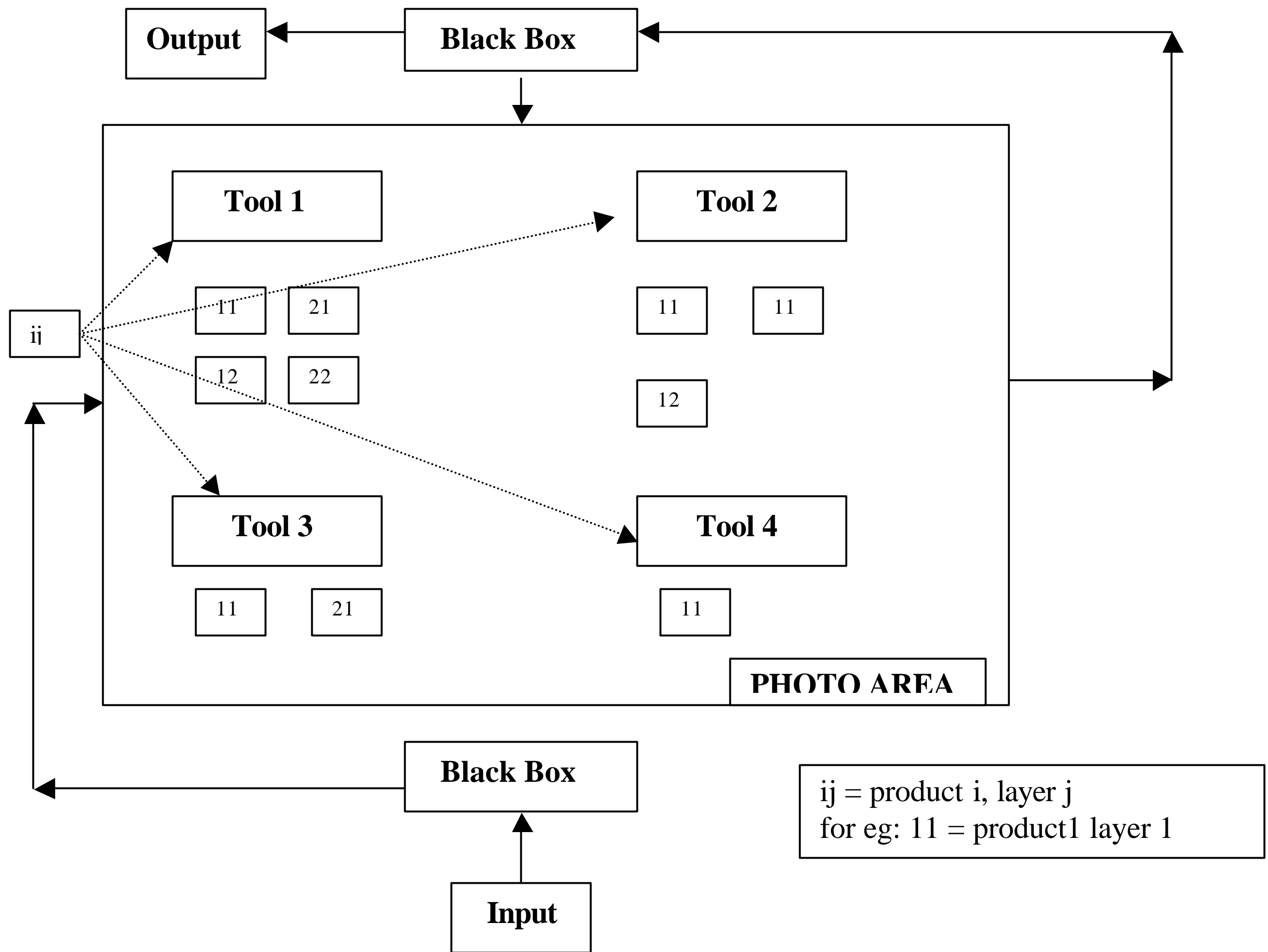
3.4.5.3 Summary of Experimentation

1. The performance of the dispatching rules were compared under the presence of PM/ breakdown of tools and in presence of no PM /Breakdowns.
2. FIFO rule gives the least standard deviation of Cycle time under both cases of PM/Breakdown and under different levels of lot dedication.
3. LTR and LPR rules show robust performance in terms of throughput and cycle time under different lot dedications levels
4. Best throughput performance is realized under no lot dedication level for both cases of PM /Breakdown.
5. The cycle time for all the dispatching rules is insensitive to lot dedication levels. i.e., it remains the same under all lot dedications level.
6. The impact of lot dedication on various performance metrics is more pronounced as we go from level 1 to level 2 or if we go from level 1 to level 3 dedication levels.

3.5 Motivation for a new heuristic

The idea behind the proposed heuristic is to use a combination of available dispatching rules. The standard dispatching rules rank the lots waiting in a queue, in front of a tool, based on some attribute of the lot or the tool. Typically, the lots are assigned to the tools randomly. The proposed heuristic uses the dispatching rules and also systematically allocates a lot to a given tool. The problem area can be depicted as follows:

FIGURE 3.19: LOT MOVEMENT THROUGH THE FAB.



A lot goes through some processing steps before reaching the first photolithography step. These steps are represented as a black box here. When it reaches the first step in the photo area, a decision has to be made as to allocate the lot to a given tool. Referring to Figure 3.19, a lot can be allocated to any of the 4 tools. The lot will visit the same tool during the subsequent photolithography steps due to lot dedication .The steps in between the photolithography steps are also depicted as a black box. There are different lots waiting in front of the tools of a photolithography area. These lots may be of different

product types or at different stages of processing. Referring to Figure 11, we can see that, in front of Tool 1, there are 4 lots, one lot of product 1 layer1, one lot of product1 layer2, one lot of product2 layer1 and one lot of product2 layer2. The problem that we are attempting to solve here is a high volume and low product mix type. Moreover, the processing times of the different products are not significantly different.

We are now faced with three questions: (1) where should a lot be allocated for processing its first photolithography layer, (2) which layer should be selected for processing at a tool, and (3) which lot of a given layer should be selected.

The ESD (Earliest start date) rule attempts to equalize the waiting times of the jobs, that is, to minimize the variance of the waiting times. So, we use this rule to rank the lots at a given tool. Now, since each tool feeds itself, i. e, the lots leaving the tool come back to the tool for the subsequent photo steps, we use LLA (least lots ahead) rule to select the layer. The combination of the ESD and LLA takes care of answering second and third questions.

To minimize the waiting time at a given tool, we allocate the lot to a tool with the least amount of lots associated with that tool. For this, we look at the lots waiting in front of the tool and the lots which are due to come back for the processing of subsequent layers.This algorithm does not guarantee optimal solution, but can be applied in a real life environment. This algorithm is coded in C++ and is integrated with the Autosched AP model developed for the photolithography area.

3.6. Proposed Algorithmic steps

Part A: **Allocation of Lot to a tool.**

During the first visit to a photolithography tool, the lots must be dedicated to one particular tool. This is achieved by summing up the work in progress for all the tools available. The work in progress at a tool includes the lots waiting in front of that tool and the lots, which are due to visit that tool during their subsequent visits. Consequently, a lot is allocated to the tool with the least amount of work in progress.

Part B: **Selection of a lot for processing at a given tool.**

Step1: First, the lots are sorted according to a priority. A lot with the higher priority is placed first in the queue. (The lower the rank, the higher the priority). The Priority of a lot is predetermined. If there is a tie, first break the tie using the ESD rule, and if tied again by the LLA rule.

Step 2: Schedule the first lot on that tool, and repeat for all the tools.

3.7 Results

The performance proposed heuristic approach is compared against those of the standard dispatching rules for 3- level, 2- level lot dedication and 1-level lot dedication scheme under two cases. In first case we assume that there are breakdowns and preventive maintenance, and, in the second case, we assume that there are no breakdowns and preventive maintenance. The product mix and the loading policy are kept the same in both the cases. The results are shown in Table 3.9 and Table 3.10.

1. Performance under PM's and Breakdowns

TABLE 3.9: PERFORMANCE OF THE PROPOSED AND OTHER DISPATCHING RULES UNDER 1- LEVEL, 2-LEVEL AND 3- LEVEL LOT DEDICATION.(WITH PM/BREAKDOWN)

Rules	Throughput			Average Cycle time			Average WIP			Utilization %		
Dedication	1	2	3	1	2	3	1	2	3	1	2	3
Proposed	**1464**	**1423**	**1446**	**46.81**	**46.02**	**46.57**	**1682**	**1705**	**1704**	**63.53**	**62.64**	**62.88**
LTR	1401	1362	1366	45.93	45.39	45.76	1652	1658	1668	62.39	61.26	61.89
LPR	1402	1365	1364	45.94	45.40	45.79	1652	1658	1668	62.51	61.28	61.91
LLA	1452	1402	1361	46.32	45.34	45.94	1662	1657	1675	63.55	61.31	60.8
ESD	1404	1367	1372	46.04	45.41	45.72	1654	1657	1665	62.3	61.39	61.96
FIFO	1447	1413	1345	46.33	45.36	45.93	1662	1657	1678	63.46	61.34	60.57

2. Performance under No breakdowns and PM's

TABLE 3.10: PERFORMANCE OF THE PROPOSED AND OTHER DISPATCHING RULES UNDER 1- LEVEL, 2-LEVEL AND 3- LEVEL LOT DEDICATION.(WITHOUT PM/BREAKDOWN)

Rules	Throughput			Average Cycle time			Average WIP			Utilization %		
Dedication	1	2	3	1	2	3	1	2	3	1	2	3
Proposed	**1533**	**1525**	**1536**	**46.42**	**46.48**	**46.55**	**1638**	**1642**	**1643**	**65.43**	**65.64**	**65.2**
LTR	1504	1470	1475	45.01	45.88	46.03	1616	1641	1645	64.37	64.33	64.31
LPR	1497	1470	1475	44.96	45.87	46.04	1615	1641	1645	64.6	64.33	64.32
LLA	1471	1481	1471	45.89	45.88	46.01	1646	1642	1647	64.77	64.33	64.37
ESD	1465	1475	1481	45.36	45.91	46.06	1624	1640	1645	63.94	64.35	64.39
FIFO	1464	1479	1464	45.87	45.82	46.02	1639	1641	1648	64.78	64.29	64.3

3.7.1Peformance of Heuristic against standard dispatching rules:

Case 1: With PM's and Breakdown

FIGURE 3.20:THROUGHPUT PERFORMANCE COMPARISON (WITH PM /BREAKDOWN)

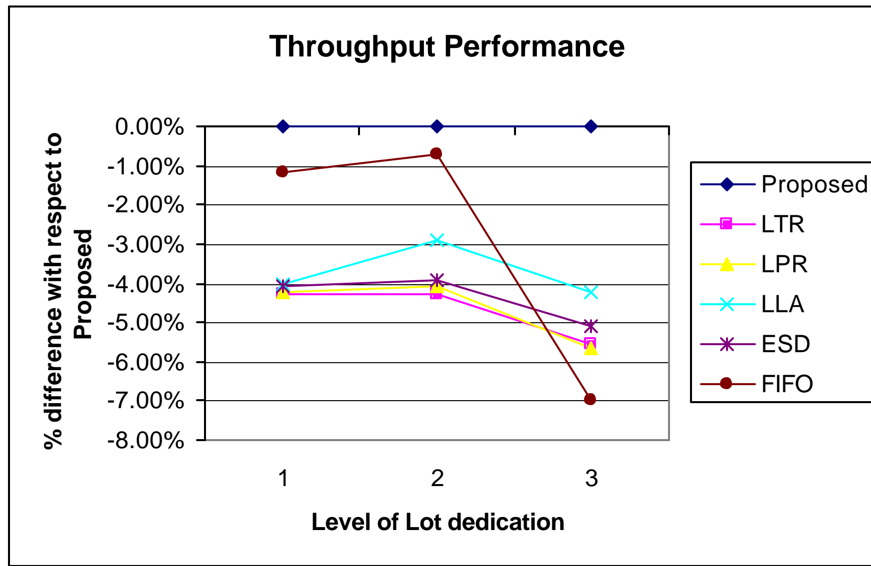


FIGURE 3.21: CYCLE TIME PERFORMANCE COMPARISON (WITH PM/ BREAKDOWN)

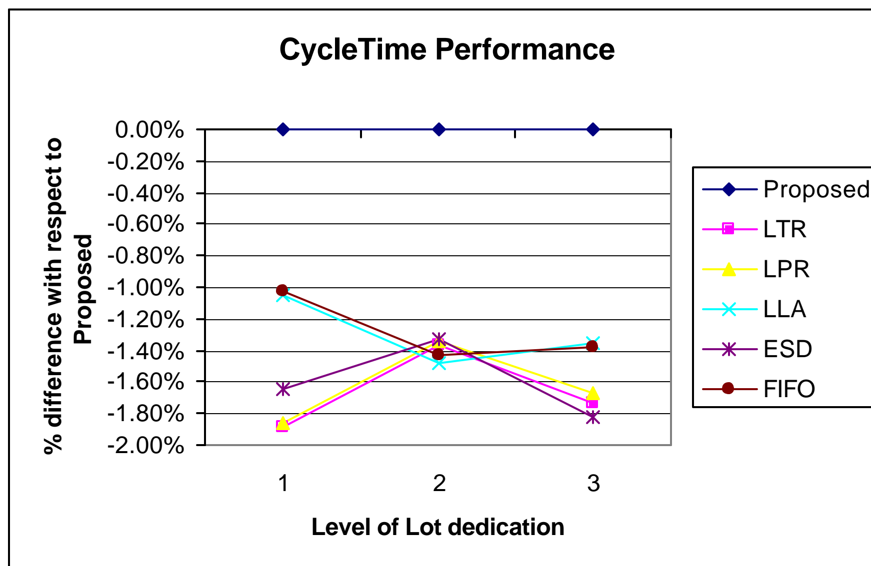


FIGURE 3.22: WIP PERFORMANCE COMPARISON (WITH PM/BREAKDOWN)

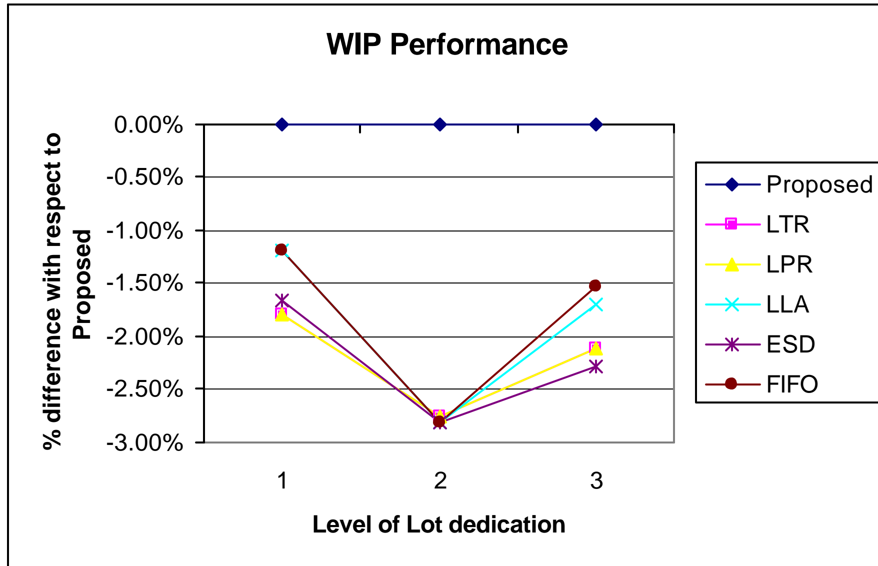
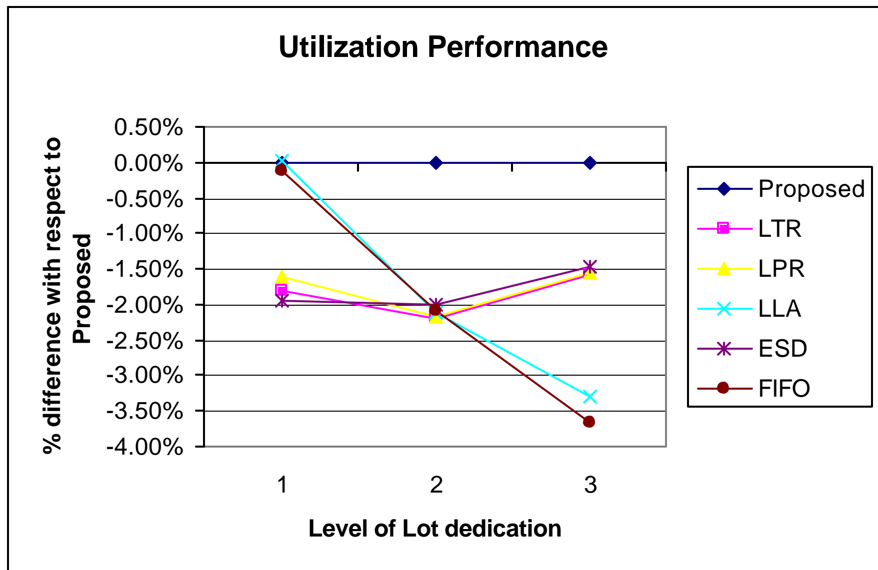


FIGURE 3.23: UTILIZATION PERFORMANCE COMPARISON (WITH PM/BREAKDOWN)



It is clear from Figures 3.20,3.21,3.22 and 3.23 that the throughput and utilization values are better for the proposed heuristic than those for the other dispatching rules. The cycle time and the WIP are little high for the Proposed heuristic but the percentage increase in throughput is more as compared to percentage decrease in WIP and cycle time.

Case 2: Without PMS and Breakdown

FIGURE 3.24: THROUGHPUT PERFORMANCE COMPARISON (WITHOUT PM /BREAKDOWN)

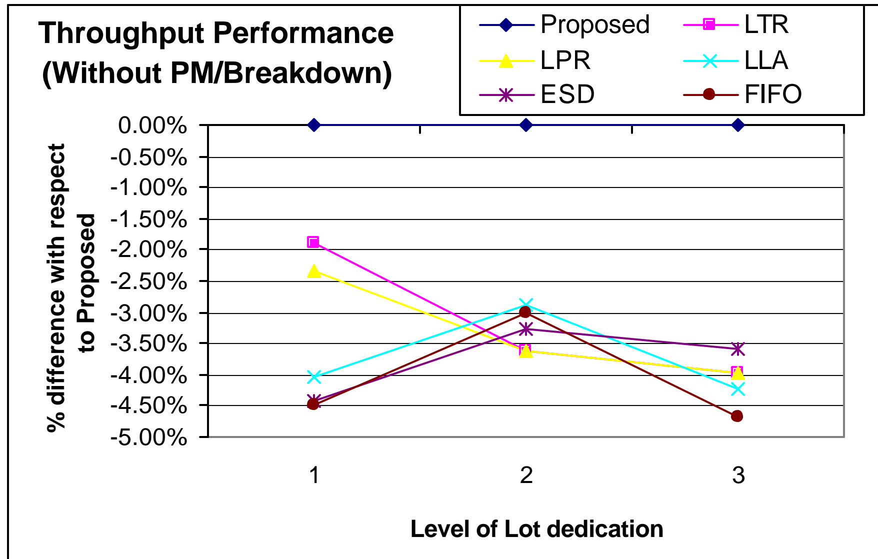


FIGURE 3.25: CYCLE TIME PERFORMANCE COMPARISON (WITHOUT PM/ BREAKDOWN)

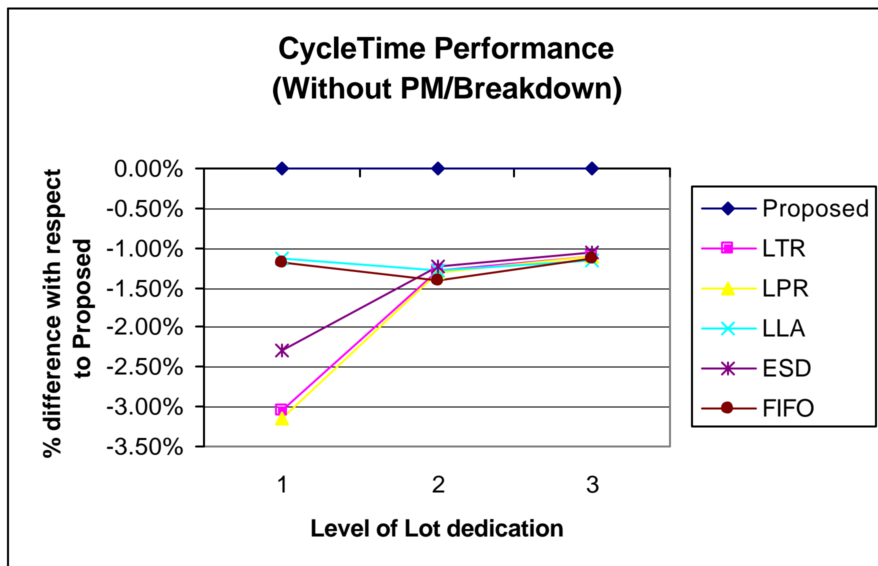


FIGURE 3.26: WIP PERFORMANCE COMPARISON (WITHOUT PM/BREAKDOWN)

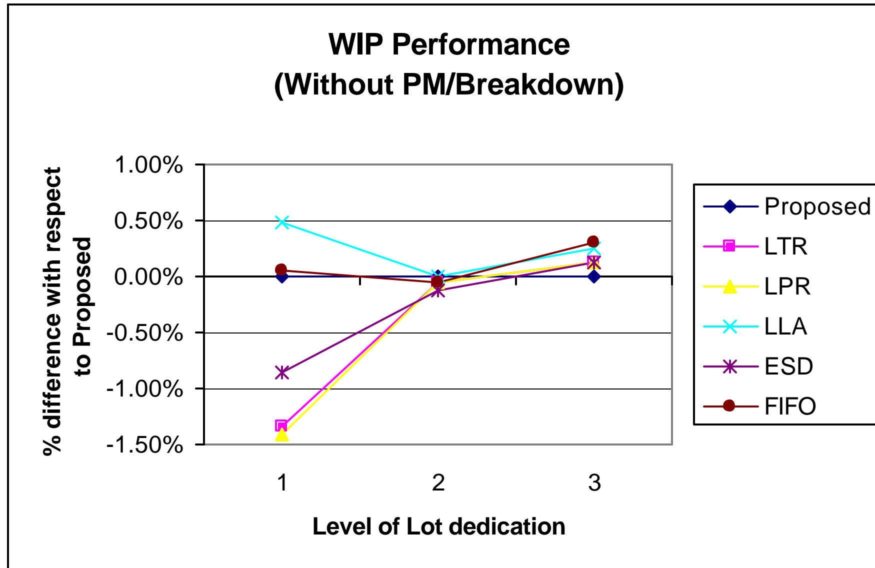
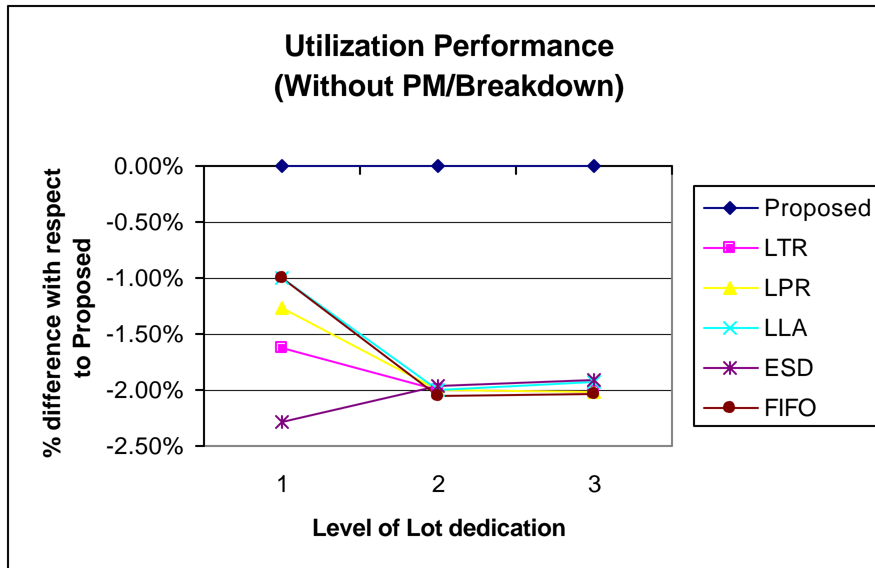


FIGURE 3.27: UTILIZATION PERFORMANCE COMPARISON (WITHOUT PM/BREAKDOWN)

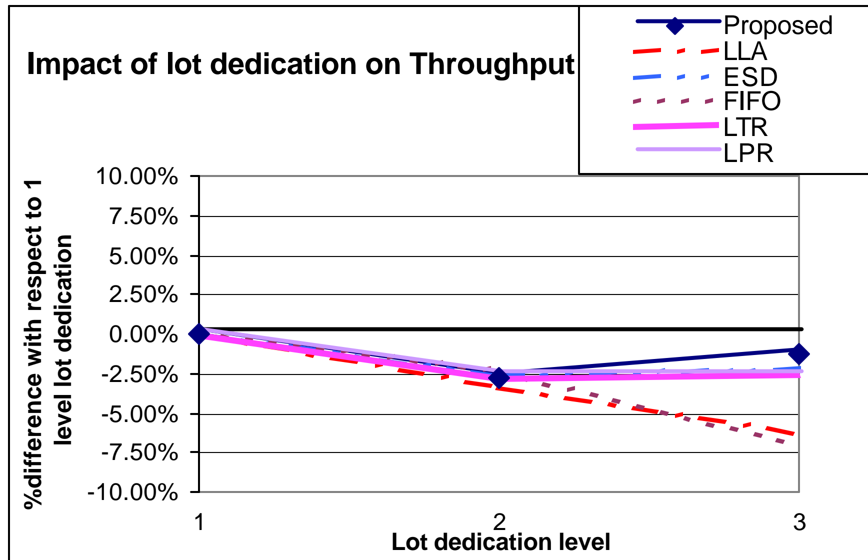


We can see from Figures 3.24,3.25,3.26 and 3.27 that the performance of the Proposed heuristic is best with regards to throughput and utilization as compared to those of the other dispatching rules. The WIP performance of the proposed heuristic is also good as compared to those of the other dispatching rules.

3.7.2 Impact of lot dedication

Case 1: With PM's and Breakdown

FIGURE 3.28: IMPACT OF LOT DEDICATION ON THROUGHPUT (WITH PM/BREAKDOWN)



From the above figure we can see that there is a drop in the throughput value for all the dispatching rules, from level1 to level3 lot dedication scheme.
However, the drop in the throughput value for the Proposed heuristic is the least.

FIGURE 3.29: IMPACT OF LOT DEDICATION ON CYCLE TIME (WITH PM/BREAKDOWN)

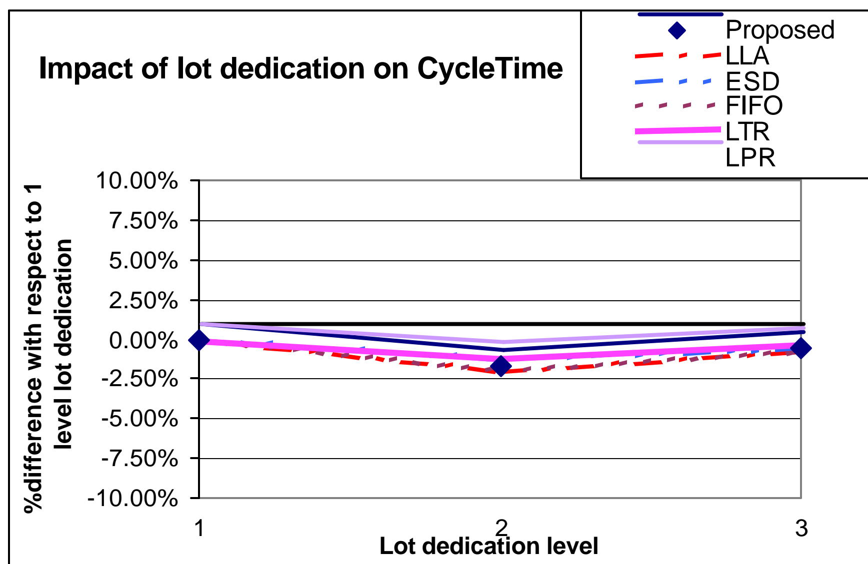
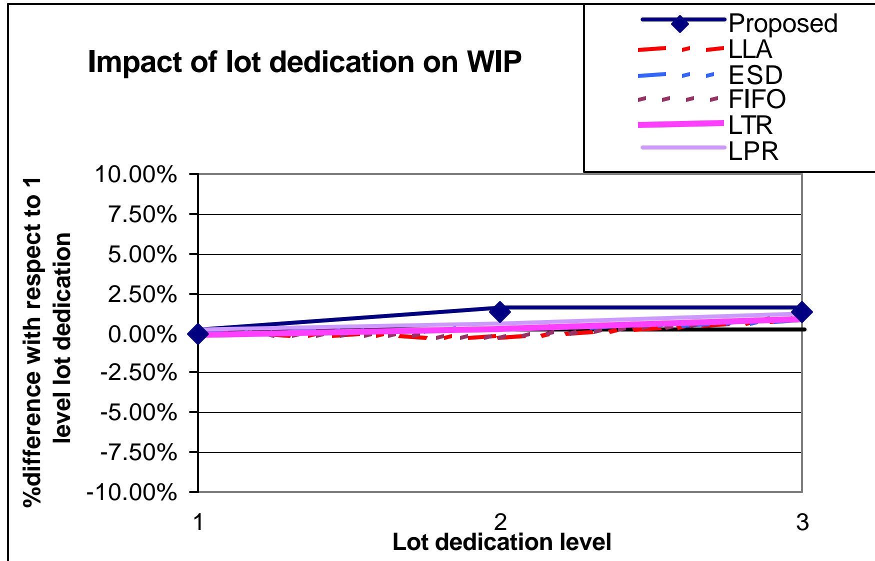


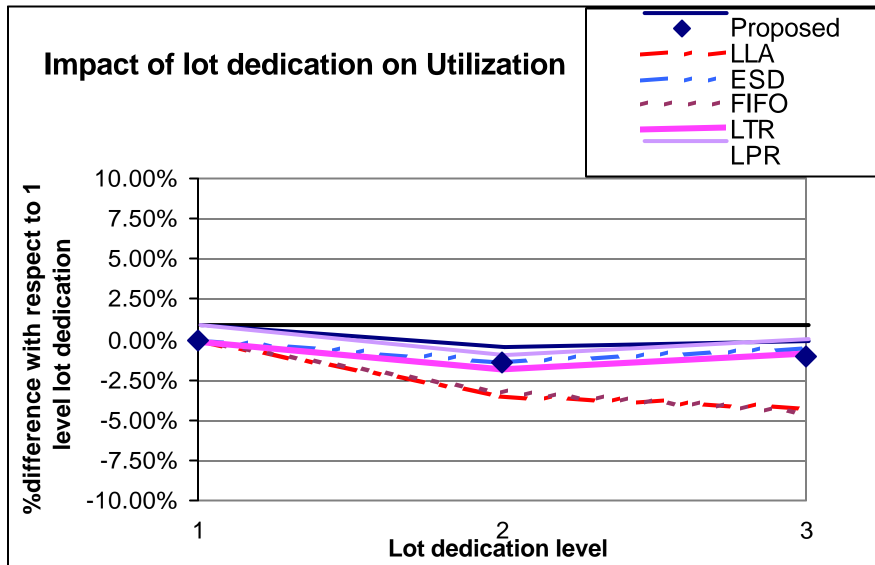
Figure 3.29 reveals that there is about 1% gain, on average, in the cycle time for all the dispatching rules as we move from 1- level lot dedication to 3- level lot dedication.

FIGURE 3.30: IMPACT OF LOT DEDICATION ON WIP (WITH PM/BREAKDOWN)



From Figure 3.30 indicates that there is increase in WIP as we go from 1- level lot dedication to 3 -level lot dedication

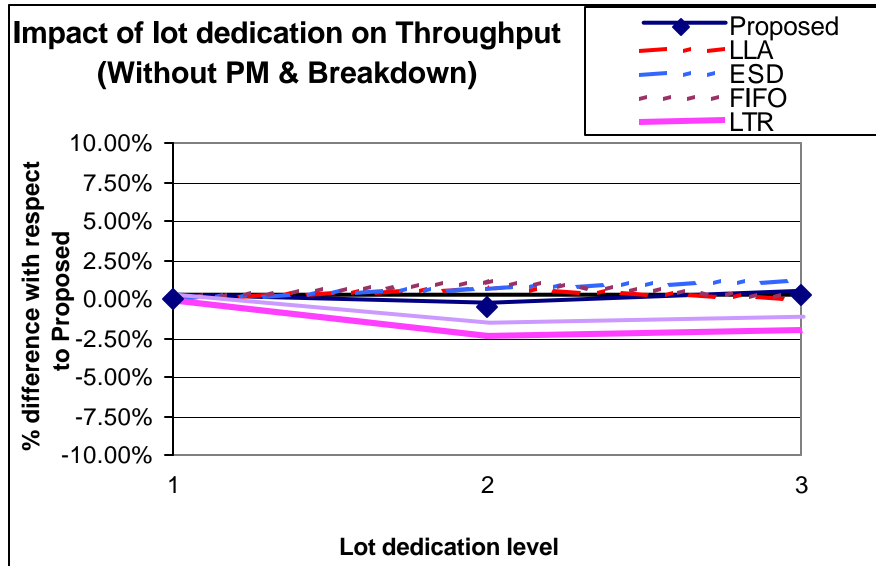
FIGURE 3.31: IMPACT OF LOT DEDICATION ON UTILIZATION (WITH PM/BREAKDOWN)



According to Figure 3.31 utilization decreases for 2- level and 3- level lot dedication level as compared to 1- level lot dedication

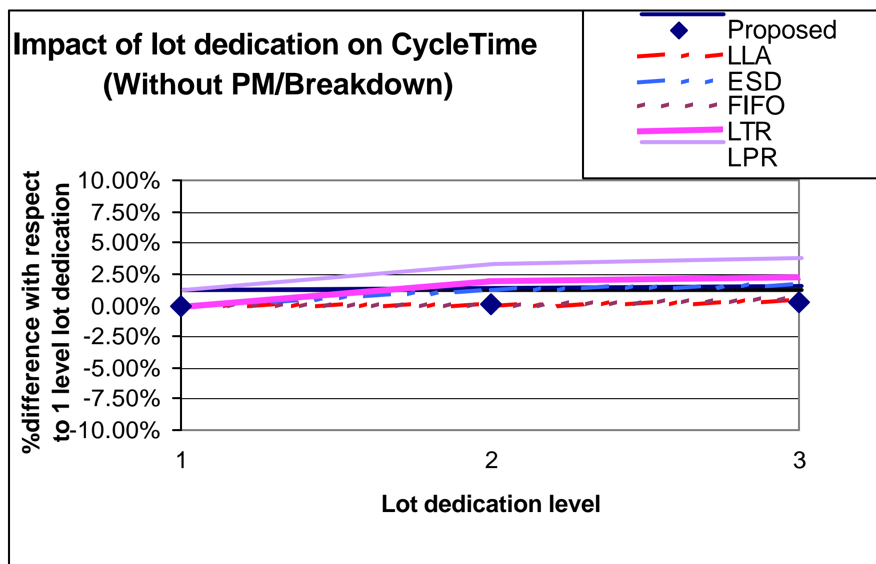
Case 2: Without PM's and Breakdowns.

FIGURE 3.32: IMPACT OF LOT DEDICATION ON THROUGHPUT (WITHOUT PM/BREAKDOWN)



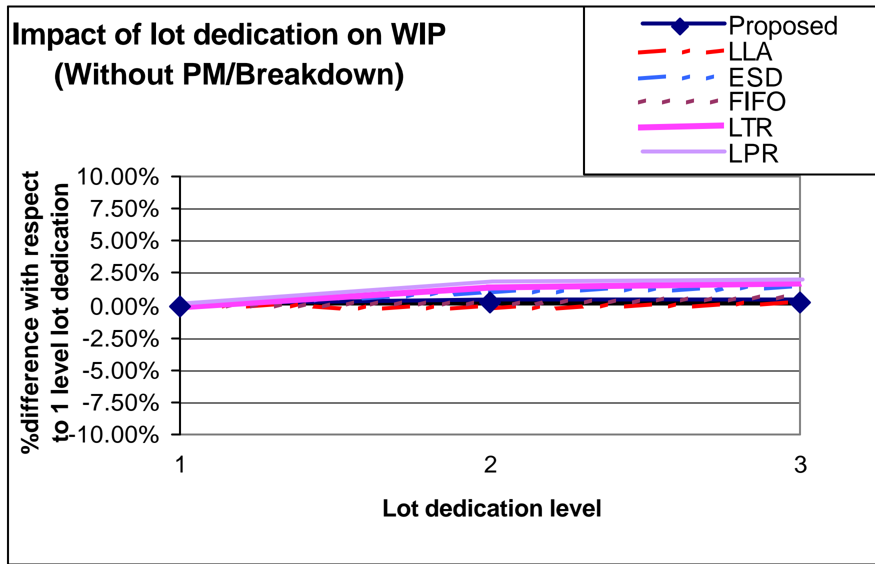
It appears from Figure 3.32 that LLA and ESD improve the throughput and Proposed, LTR and LPR rules reduce the throughput as we go from 1- level to 3 - level lot dedication scheme.

FIGURE 3.33: IMPACT OF LOT DEDICATION ON CYCLE TIME (WITHOUT PM/BREAKDOWN)



The cycle time increases as we go from 1-levelto 3-level dedication (Figure 3.33) . This is true for most of the dispatching rules.

FIGURE 3.34: IMPACT OF LOT DEDICATION ON WIP (WITHOUT PM/BREAKDOWN)



The WIP levels remain constant for all lot dedication levels for most of the dispatching rules (see Figure 3.34).

FIGURE 3.35: IMPACT OF LOT DEDICATION ON UTILIZATION (WITH PM/BREAKDOWN)

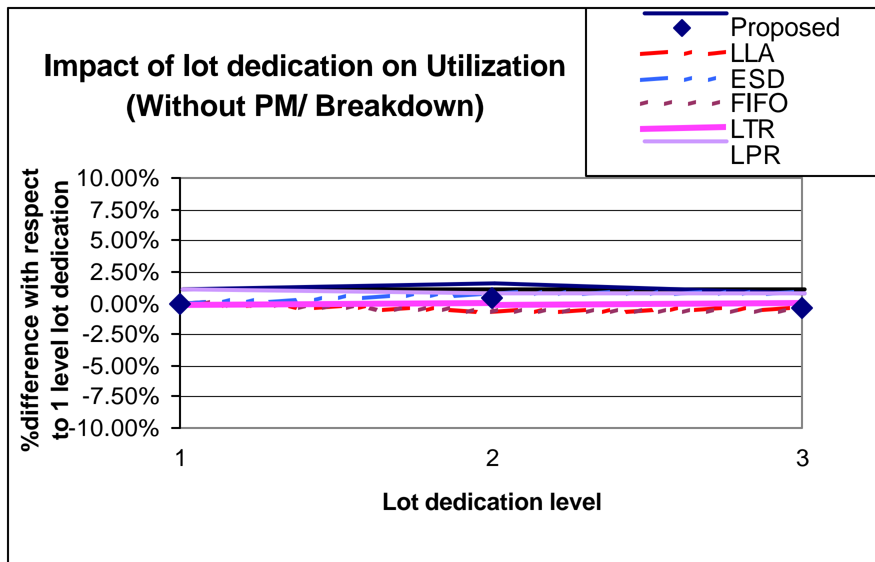


Figure3.35 reveals that utilization almost stays constant as we go from 1- level to 2-level lot dedication. However, there is a slight increase in utilization for 3- level lot dedication as compared to 2- level lot dedication.

3.8 Conclusions

1. A heuristic algorithm for scheduling and sequencing of wafers for photolithography tools is developed. The performance of the proposed heuristic is compared against those of the standard dispatching rules.
2. The proposed method performs the best in the throughput metric from among the dispatching rules tested for 3- level, 2 - level lot dedication, and 1- level lot dedication schemes with or without the PM's and breakdowns.
3. The Proposed heuristic performance metrics are least sensitive to the lot dedication level as compared to other dispatching rules.
4. All of dispatching rules show similar trend of performance for different levels of lot dedication.
5. The throughput and utilization of a tool is dependent on the availability of that tool. The availability of a tool is a function of the frequency and duration of unscheduled breakdowns and preventive maintenance schedule. For the deterministic value of unscheduled breakdown times and preventive maintenance schedule used, the 1- level lot dedication scheme performed better with respect to throughput and tool utilization as compared to the 2- level and the 3- level lot dedication schemes. Even though the 3- level lot dedication scheme is more flexible as compared to the 1 –level lot dedication scheme, yet for the values of unscheduled breakdown times and preventive maintenance schedule used, the performance of the 3- level lot dedication scheme is worse than that of the 1- level lot dedication scheme. For another set of break down time values and preventive maintenance schedule, the outcome can be different.

6. In the case where we do not have PM or breakdown, 3- level lot dedication scheme gives better performance regarding throughput (for most of the dispatching rules) as compared to 1- level and 2- level lot dedication schemes.
7. The impact of lot dedication is more visible if we compare 1- level lot dedication against 2- level or 3- level lot dedication schemes. It is less visible if we compare 2- level against 3- level lot dedication schemes.

Chapter 4 Mathematical Programming based Approach

4.1 Introduction

As presented in earlier chapters, dispatching rules do not provide optimal solutions. An attempt is therefore made to solve the problem on hand by formulating a mathematical model.

The main advantages a of mathematical programming based model are as follows:
(1). It can generate optimal solutions if solved to optimality. The optimal solutions, are of course, better than the schedules obtained using heuristics or dispatching rules.
(2). The objective function may be formulated for one performance measure or a combination of performance measures.

The main disadvantage of the mathematical programming models is their computational intractability.

We have formulated an integer-programming model for the photolithography area, which we describe later in this chapter.

4.1.1.Integer Programming modeling concepts

As described in [21], Integer linear programming (IP) models involve a linear objective function subject to a set of linear constraints, as in linear programming, but with the added complexity that a subset of variables can take on certain discrete values. In many cases, these discrete values are 0 or 1. These types of problems are often referred to an as class of 0 –1 mixed integer programming models. (MIP)

In order to solve a reasonably sized problem, the model formulated should have tight underlying linear programming representation so that the solutions lie in the neighborhood of the convex hull of integer feasible solutions. This also helps from computational point of view, since most of the commercially available software's use the LP relaxation within their solution methodology. Sometimes, it is worthwhile to include additional constraints in the model so as to improve its, solvability. The model should also exploit any special structures present in it during the process of model formulation and algorithmic development.

The most commonly used methodology for the solution of integer programming is the branch and bound methodology. This was first introduced by Land and Doig (1960),

and later extended by Dakin (1966). Branch and bound is an enumerative divide and conquer technique in which the feasible region is successively partitioned based on enforcing a finite set of alternative logical restrictions that must be satisfied at any stage. The integrality gap that exists between the value of LP relaxation of the integer problem, $\nu(LP)$, and that for the integer problem itself, $\nu(IP)$, given by $| \nu(LP) - \nu(IP) |$, determines the extent of branching required to determine the optimal integer solutions.

4.2 Integer programming model for the photolithography area

The aim is to develop a model to achieve minimal possible cycle time of the lots released into the system. The cycle time of a lot is the completion time of the last step in its route, which is the sum of the beginning time and process time. We assume the processing time of a lot at a given step to be a known constant.

There are several product types to be processed in photolithography processing area. A reticle is required for processing every layer of a wafer on a stepper or a scanner. It is necessary that all the critical layers of a wafer be processed on the same stepper or scanner. The underlying variables concerning the allocation of wafer of a product to a stepper or scanner as well as that of a reticle to that stepper or scanner .To that end we define the following notation:

X_{lijprt} = 1, if the layer l of lot i product type j is processed on tool p using reticle r starting at time t.
= 0, otherwise.

Y_{prt} = 1, if reticle r starts processing a lot on tool p at time t
= 0, otherwise.

T = Planning time horizon.

P = Set of all tools.

N_j = Number of lots of product type j.

J = Set of all product types.

L_j = Number of layers of product type j

R(r) = set of reticle type r.

M = set of all reticle types.

E_{ij} = Dummy layer of lot i of product type j. Dummy layer represents the processing step after the completion of all processing steps.

τ_{lj} = Processing time for layer l, product type j.

$\underline{v}_{lijprt}$ = a column vector with t elements. All elements of this column vector are zero's except for the elements at the locations from t to $(t+\tau_{lj}-1)$ which are one's. This vector represents the capacity of a reticle. A reticle will process only one lot on one tool during a designated time period.

$\underline{u}_{lijprt}$ = a column vector with t elements. All elements of this column vector are zero's except for the elements at the locations from t to $(t+\tau_{lj}-1)$ which are one's. This vector represents the capacity of a tool. A tool will process only one lot during a designated time period.

$\propto$ = hot lot multiplier.

Objective function:

$$\text{Min} \quad \sum_{j=1}^{J} \sum_{i \in Nj} \sum_{t=0}^{T} t.X_{Eijij00t}$$

$E_{ijij00t}$ denotes the dummy layer of lot I of product type j being processed at time t. 00 indicates that this layer does not require any tool or reticle.

Subject to:

1. (Tool Selection). At most one tool p can start processing with a reticle k at time t.

$$\sum_{p=1}^{P} Y_{pkt} \le 1 \qquad \text{For } k \in R(r),\ r \in M$$

$$t = 0,1,2 \ldots T$$

2. (Reticle Selection). At most one reticle can start processing on a tool at any given time.

$$\sum_{r\in M} \sum_{k\in R(r)} Y_{pkt} \leq 1 \quad \text{For p =1,2….P}$$

t = 0,1,2…..T

3. (Processing of a Layer). A layer of any lot i of product j is processed by only one tool, reticle pair and only once.

$$\sum_{p=1}^{P} \sum_{r\in M} \sum_{k\in R(r)} \sum_{t=0}^{T} X_{lijpkt} = 1 \quad \text{For l=1,2….}L_j$$

i = 1,2….N_j j=1…..J

4. (Allocation of Reticle-Tool). A reticle and a tool pair can work on at most one layer at a given time t.

$$\sum_{j\in J} \sum_{i=1}^{Nj} \sum_{l=1}^{Lj} X_{lijpkt} \leq Y_{pkt}, \quad \text{For p=1,2…P}$$

k ∈R(r), r∈M,

t=0,1,2..T

5. (Lot Dedication): Subsequent layers of a lot i of product type j are processed at a tool on which the first layer is processed.

$$\sum_{p=1}^{P} \sum_{r\in M} \sum_{k\in R(r)} \sum_{t=0}^{T} p.X_{1ijpkt} = \sum_{p=1}^{P} \sum_{r\in M} \sum_{k\in R(r)} \sum_{t=0}^{T} p.X_{lijpkt}$$

For j =1,2…J

i =1,2…N_j

l=2,3…Lj

6. (Precedence Constraint): This constraint ensures that the layers are processed in the correct processing order. i.e. layer l+1 is processed only after layer l is processed.

$$\sum_{p=1}^{P} \sum_{r\in M} \sum_{k\in R(r)} \sum_{t=0}^{T} (t + \boldsymbol{t}_{lj}) X_{1ijpkt} = \sum_{p=1}^{P} \sum_{r\in M} \sum_{k\in R(r)} \sum_{t=0}^{T} t..X_{(l+1)ijpkt}$$

For j =1,2…J

i =1,2…N_j l=2,3…Lj

7. (Capacity Constraint for tool).

$$\sum_{j \in J} \sum_{i=1}^{Nj} \sum_{l=1}^{Lj} \sum_{r \in M} \sum_{k \in R(r)} \underline{u}_{lipkt} . X_{lijpkt} \leq \underline{1}$$

For p=1,2….P   t=0,1,2…T

$\underline{1}$= Column vector with T elements consisting of one's.

8. (Completion Time of a Lot). The start time for the dummy layer should not exceed the time specified for hot lots..

$$\sum_{t} t . X_{Ejij00t} \leq \mathbf{a} . \sum_{l=1}^{Lj} \mathbf{t}_{lj}$$

For j=1,2…J   i=1,2….N_j

9. (Reticle's Processing of a Layer). A reticle can process only one layer of one lot of a product type j during a designated time period

$$\sum_{j \in J} \sum_{i=1}^{Nj} \sum_{l=1}^{Lj} \sum_{p=1}^{P} \underline{v}_{lijpkt} . X_{lijpkt} \leq \underline{1}$$

$k \in R(r)$, $r \in M$, t =0,1,…., T

$\underline{1}$ = Column vector with T elements consisting of one's.

10. (Reticle Allocation to a Tool). A reticle occupies at most one tool during the designated time period.

$$\sum_{j \in J} \sum_{i=1}^{Nj} \sum_{l=1}^{Lj} \sum_{p=1}^{P} \underline{v}_{lijpkt} . y_{pkt} \leq \underline{1}$$

$k \in R(r)$, $r \in M$, t =0,1,…., T

$\underline{1}$ = Column vector with T elements consisting of one's.

4.3.1 Methodologies to adapt to dynamic changes on the floor

The above model can be easily adopted to include the occurrence of dynamic changes on the shop floor.

1.**Unscheduled tool breakdowns**

A tool can breakdown unexpectedly due to various reasons. For each such reason, the average time it takes to repair the tools can be determined from the past data. When a tool breaks down, the model can be solved again, by taking into consideration the unavailability of the tool. The capacity of the tool is made equal to zero for the amount of time the tool is down.

2.**Preventive maintenance**

If the preventive maintenance schedule is known at the time of solving the problem, the capacity of the tool is put equal to zero during this time, so that no lot can be processed.

3.**Reticle Unavailability**

If a reticle is damaged during the process or is taken out for scheduled inspection, the historical time can be used to predict the time for reticle down time. For that time period, we can set the starting times of the reticle at all the tools equal to zero and solve the scheduling problem again.

4.4 Methodology to solve the integer problem

The above integer program is solved under a static lot release policy. Under this policy, the processing steps of the various lots are known a priori. The scheduling problem determines the time at which each lot should be scheduled at a particular tool with the appropriate reticle available at that tool.

An attempt is made to solve the above model, using the CPLEX 6.6 software. The problem we have formulated is a NP hard problem. The time required to solve the

problem is not a polynomial in the size of the problem. This model fails to provide a solution in reasonable computation time for even small size problems.

4.4.1 Experimentation

Experiment 1:

Input data for the above model is as follows:

Number of lots =2 Number of tools=2

Number of reticle families =4 Number of reticles in each reticle family =2

Priority of lots =3 Number of parts =1 Number of photo layers = 2

TABLE 4.1 RESULTS OF EXPERIMENT 1:

Lot	Start time of Layer1 (Photo layer)	Tool\reticle family\reticle number	Start time of Layer 2(Black box)	Start time of Layer 3 (Photo layer)	Tool\reticle family\reticle number	Start time of Dummy layer
1	0	1\11\2	1	3	1\12\1	5
2	0	2\11\1	1	3	1\12\2	5

Integer optimal solution = 10

Iterations = 159

Solution time = 1.69 sec.

Nodes = 5.

As seen in Table 22, lot 1 was started on tool1 using reticle family 11 and using reticle number 2 of reticle family 11 at time 0 for the first photo step.

The second layer of lot 1 is not a photo step and is considered as black box with 2 units of processing time.

The third layer of lot 1 is started on tool1 using reticle family 12 and using reticle number 1 of the reticle family 12 at time 3.

Layer 4 is a dummy layer; it is the layer after the last layer of a lot.

Experiment 2:

Input data for the math model is as follows:

Number of lots =4 Number of tools=2

Number of reticle families =4 Number of reticles in each reticle family =2

Priority of lots =3 Number of parts =2 Number of photo layers = 2

TABLE 4.2 RESULTS OF EXPERIMENT 2:

Lot	Start time of Layer1 (Photo layer)	Tool\reticle family\reticle number	Start time of Layer 2(Black box)	Start time of Layer 3 (Photo layer)	Tool\reticle family\reticle number	Start time of Dummy layer
1	0	1\11\2	1	3	1\12\1	5
2	0	2\11\1	1	3	2\12\2	5
3	1	1\21\2	3	5	1\22\1	6
4	1	2\21\1	3	5	2/21\2	6

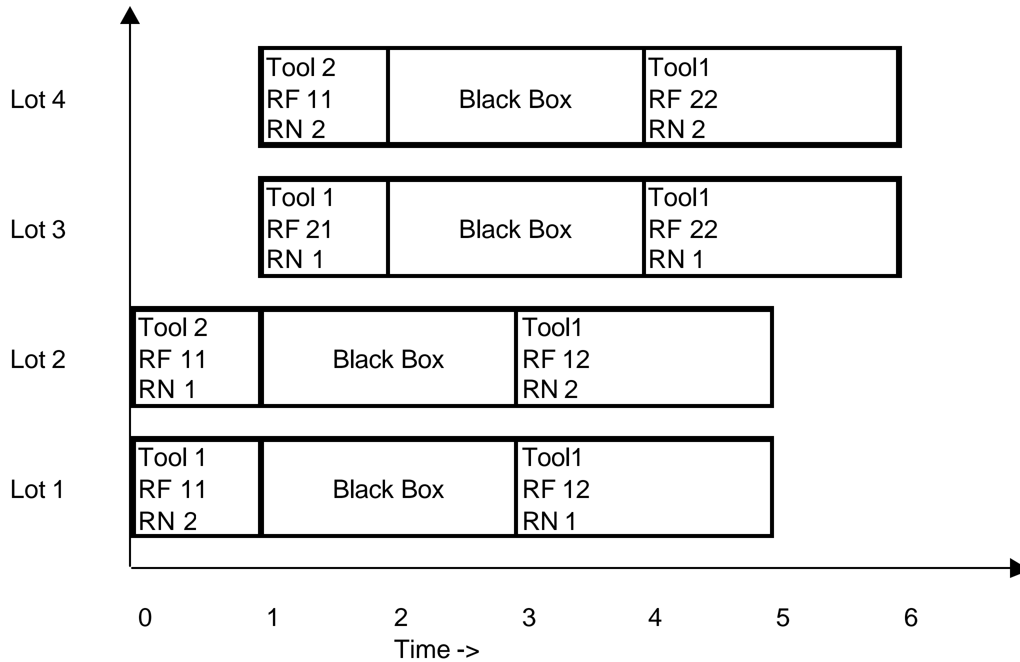
Integer optimal solution = 22

Iterations = 272

Solution time = 13.77sec.

Nodes = 30.

FIGURE 4.1 LOT MOVEMENT



RF: Reticle Family RN: Reticle number in a given reticle family.

Figure 4.1 depicts the lot movement as shown below.

X-axis represents the time at which a given lot was started using a given tool and reticle pair. Y-axis represents the given lot.

Lot **1,** first photo layer (layer1) was started processing on **Tool1** at Time 0 using reticle **2** of reticle family **R11** and its second photo layer (layer 2) was started processing on **Tool1** at Time 3 using reticle 1 of reticle family **R12**.

When the number of lots was increased to 5, the model could not solve the problem in reasonable amount of time. Hence, there is a need to develop an appropriate methodology to solve the above problem efficiently.

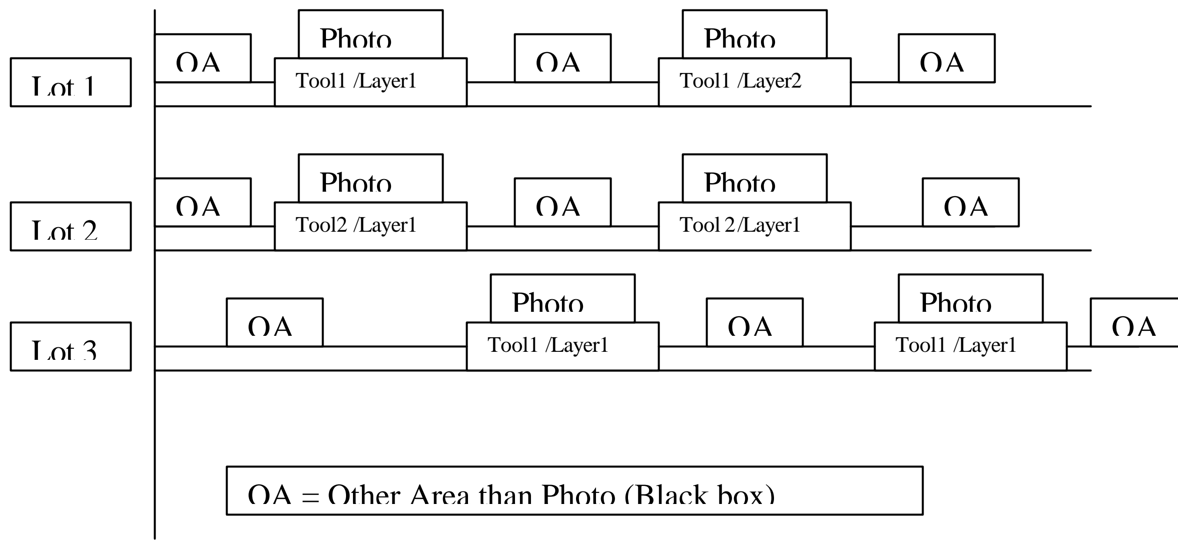
4.5 Proposed Methodology

In order to develop an efficient methodology to solve this problem at hand, it can be conceptualized as follows: The lot dedication requirement makes the lot be processed at the same tool for a certain number of critical layers. In between its visit to the same

tool, the lot goes through different areas within the facility.(denoted as black box in above discussion)

Thus, the visits of a product to the same tool in interspersed with voids as shown Figure 4.2:

FIGURE 4.2: PROPOSED METHODOLOGY



The minimum lengths of these voids are known, being equal to the processing time at the processing areas in the black box. Thus a lot can be viewed as a "string of jobs" with the intervening lengths of strings being greater than or equal to a known lower bound. The length of a string corresponding to a product can be viewed as flexible. The problem is then to schedule these strings (corresponding to the various lots to be processed) on the tools (scanners and steppers), with each string assigned to only one tool.

If all the tools are assumed to be identical, the above problem reduces to that of scheduling strings of lots on parallel processors to minimize the average cycle time. There are crucial differences of this problem from the classical m parallel processor mean flow time scheduling problem. One difference relates to the types of lots to be scheduled, which are strings with flexible lengths and not the ones with known and fixed processing times. The other difference is the requirement of a particular reticle for processing a layer of a lot. Thus, there is a reticle allocation problem superimposed on the

m – parallel processor, mean flow time problem of scheduling strings of jobs of flexible lengths.

The above conceptualization helps in determining a methodology to solve the photolithography planning and scheduling problem. The problem can now be decomposed as follows:

In the formulation presented above, we fix the y variables i.e. we first allocate the reticles appropriately to the tools. Note that this allocation has to take care of the lot dedication constraint. i.e. if we allocate a reticle for layer 1 to a given tool, then reticles for all the layers, for which the lot has to come back to the same tool, have to be allocated to this tool as well .The lot dedication constraint helps in reducing the problem size for the above sub-problem. It also limits the problem size of allocating the lot to a tool, because of reticle availability constraint.

So, once the allocation of lots to tools is determined, the remaining problem is to sequence the lots on individual tool subject to the priority lot constraint. i.e. the lots have to be finished before the time specified by the priority lot constraint.

Thus, from above, we can see that the problem can be decomposed into three sub-problems of relatively smaller sizes to obtain a solution in a relatively smaller amount of computational time. These sub problems are: allocation of a lot to a tool, allocation of appropriate reticles to the tools based on the allocation of lots to the tools, and then the sequencing of the lots on individual tools.

4.6 Conclusions*:*

1. An integer-programming model for the system is presented.
2. This integer-programming model is not able to solve even small sized problems efficiently.
3. A solution methodology is proposed that decomposes the problem into three subproblems, which are relatively easier to solve.

Chapter 5: Summary and Conclusions

5.1 Summary

Chapter 1 gives a brief introduction to semiconductor manufacturing and photolithography processing area. The problem that is addressed in this research is described.

Chapter 2 presents a detailed literature review for planning and scheduling of semiconductor manufacturing. The mathematical approach, Dispatching rules and Simulation modeling techniques are covered in detail.

Chapter 3 describes the characteristic curve approach used for determining the best dispatching rule. This chapter also presents the impact of lot dedication on the performance of the dispatching rules. A heuristic based dispatching rule is presented. It performs the best in terms of throughput rate in the presence of breakdowns and preventive maintenance or in the presence of no breakdowns and preventive maintenance. The proposed heuristic gives the most robust performance for different levels of lot dedication.

Chapter 4 presents a mathematical programming based approach for scheduling lots at the photolithography processing area. For the given routes and processing times of the product types, the entire problem is formulated as an Integer program. It is found out that this model can’t solve even a small sized problem efficiently and consequently, a solution methodology is proposed to solve the problem efficiently.

5.2 Directions for future research:

A. For Heuristic Based Dispatching rules:

1. The performance of the proposed heuristic can be to be compared under different conditions of preventive maintenance and breakdowns of the tool.
2. This heuristic needs to be incorporated in a Fab wide simulation model to determine the impact on overall fab performance.
3. One can also study the effect of number of reticles and rework on the performance of the heuristic.

B. Mathematical programming based approach:

1. Verification of the proposed solution methodology.
2. Consideration of stochastic processing times in between the photolithography steps: The model at present uses deterministic values for processing steps in between the photolithography steps. Incorporation of stochastic values in the model will increase its accuracy.
3. Incorporation of multiple level of lot dedications in the mathematical model.

BIBLOGRAPHY

[1] Aurand S., P.Miller, “The Operating Curve: A method to measure and benchmark manufacturing line productivity”, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 1997.

[2] Bai, X., Srivatsan, N., and Gershwin, S. B., “Hierarchical Real-Time Scheduling of a Semiconductor Fabrication Facility,” 1990 IEEE/CMPT International Electronics Manufacturing Technology Symposium, p. 312-317.

[3] Chen Ying, Shu.Y, Hong.M, Wang I “Real time dispatching reduces cycle time”

[4] Connors, D. P., and Yao, D. D., “Methods for Job Configuration in Semiconductor Manufacturing,” IEEE Transactions on Semiconductor Manufacturing, Vol. 9, No. 3, p. 401-411, August 1996.

[5] El Adl, M. K., Rodriguez, A. A., and Tsakalis K. S., “Hierarchical Modeling and Control of Re-entrant Semiconductor Manufacturing Facilities,” IEEE Proceedings of the 35th Conference on Decision and Control, Kobe, Japan, December 1996, p. 1736-1742

[6] Glassey, C. R., Shantikumar, J. G., and Seshadri, S., “Linear Control Rules for Production Control of Semiconductor Fabs,” IEEE Transactions on Semiconductor Manufacturing, Vol. 9, No. 4, p. 536-549, November 1996.

[7] Hung Y.F and Hung J.L “Scheduling job with machine dependant processing times”

1996 IEEE/CMPT International Electronics manufacturing Technology symposium, p.42 –58

[8] Hung, Y.-F., and Leachman, R. C., “A Production Planning Methodology for Semiconductor Manufacturing Based on Iterative Simulation and Linear Programming Calculations,” IEEE Transactions on Semiconductor Manufacturing, Vol. 9, No. 2, p. 257-269, May 1996

[9] Kayton D., Teyner.T, Schwartz.C and Reha Uzsoy “Effect of dispatching and down time on the performance of wafer fab operating under theory of constraints” 1996 IEEE/CMPT International Electronics manufacturing Technology symposium, p.49 –56

[10] Kumar P.R. “Scheduling semiconductor manufacturing plants” IEEE control systems, December 1994, p33-40

[11] Kumar.S and Kumar P.R. “Performance bounds for queuing networks and scheduling policies” IEEE transactions on Automatic control, vol 39, No 8, August 1994

[12] Lou, S. X. C., and Kager P. W., “A Robust Production Control Policy for VLSI Wafer Fabrication,” IEEE Transactions on Semiconductor Manufacturing, Vol. 2, No. 4, p. 159-164, November 1989

[13] Lu, S. C. H., Ramaswamy, D., and Kumar, P. R., “Scheduling Semiconductor Manufacturing Plants to Reduce Mean and Variance of Cycle Time,” 1993 IEEE/SEMI Advanced Semiconductor Manufacturing Conference. p. 83-85.

[14] McCune J. “Production Planning on Lithography tools in a multiproduct/ multi technology fab with tool qualification lead times”

[15] Mehta S.V. and Uzsoy.R “Minimizing total tardiness on a Batch processing machine with incompatible job families.” IIE Transactions (1998)30, p.165 -178

[16] Pinedo M. “Scheduling Theory, Algorithms and Systems”, Prentice Hall, New Jersey.

[17] Robinonson J.K., Fowler J.N., “Measurement and Improvement of Manufacturing Capacity (MIMAC), Project Final Report, SEMATECH technology transfer # 95062861,A-TR, Austin, TX.

[18] Sooyoung Kim, Seung-Hee Yea, Bakang Kim " Stepper Scheduling in Semiconductor Wafer Fabrication Process”, Proceedings of International Conference on Modeling and Analysis of Semiconductor Manufacturing (MASAM 2000), Pg 157-162.

[19] Schoemig A.,” On the corrupting influence of variability in semiconductor manufacturing”, Winter Simulation Conference 1999.

[20] Schoemig, Mittler, “Comparison of dispatching rules for reducing the mean and variability of cycle times in semiconductor manufacturing” Symposium on Operations Research, 1999.

[21] Sherali H.D., Driscoll P.J., ”Evolution and State of the Art in Integer Programming”, July 1999.

[22] Thompson M., “Simulation-Based Scheduling: Meeting the Semiconductor Wafer Fabrication Challenge,” IIE Solutions, V-28, N-5, p. 30-34, 1996.

[23] Uzsoy,R., Martin-Vega, L. A., Lee, C.-Y., and Leonard, P. A., “Production Scheduling Algorithms For A Semiconductor Test Facility,” IEEE Transactions on Semiconductor Manufacturing, Vol. 4, No. 4, p. 270-280, November 1991

[24] Wein L. M., “Scheduling Semiconductor Wafer Fabrication,” IEEE Transactions on Semiconductor Manufacturing, Vol. 1, No. 3, p. 115-130, August 1988.

APPENDIX A: ORDERS FILE

LOT	PART	PIECES	START	REPEAT	RUNITS	RPT#	DUE	TRACE
256M	256M_S17		07/01/99 00:00:00	1.25	hr	4000		
128M	128M_S17		07/01/99 00:00:00	6	hr	4000		
259M	259M_S17		07/01/99 00:00:00	4	hr	4000		
64M	64M_S17		07/01/99 00:00:00	4	hr	4000		

APPENDIX B: PARTS FILE

PART	ROUTEFILE	ROUTE	STDLTSZ
128M_S17	128_route.txt	128_route	25
256M_S17	256_route.txt	256_route	25
64M_S17	64_route.txt	64_route	25
259M_S17	259_route.txt	259_route	25

APPENDIX C: ROUTE FILE

SAMPLE ROUTE FOR 128M and 256M

ROUTE	STEP	STNFAM	PTIME	PTUNITS	PTPER	GENRESFAM	STNEXC1	STNEXC2	SVESTN
128_route	Blackbox	delay	57.09	hr	lot				
	L-DTEXPOSE	DUVZ1	1.09	hr	lot	128_DT	DUVZ12		yes
	L-DTOVLY	LOVRL	0.34	hr	lot				
	L-DTSEM	LCSEM	0.26	hr	lot				
	L-DTWSRT	LWSRT	0.09	hr	lot				
	L-DTSCOP	LSCOP	0.2	hr	lot				
	L-DTREJN	delay	0.1	hr	lot				
	Blackbox	delay	357.42	hr	lot				
	L-AAEXPOSE	DUVZ1	1.26	hr	lot	128_AA			
	L-AAOVLY	LOVRL	0.15	hr	lot				
	L-AASEM	LCSEM	0.21	hr	lot				
	L-AAWSRT	delay	0.1	hr	lot				
	Blackbox	delay	38.49	hr	lot				
	L-KVEXPOSE	LCILNZ	0.72	hr	lot	128_KV			
	L-KVSCOP	LSCOP	0.2	hr	lot				
	L-KVREJN	delay	0.1	hr	lot				
	Blackbox	delay	36.96	hr	lot				
	L-WNEXPOSE	LCILNZ	1.08	hr	lot	128_WN			
	L-WNOVLY	LOVRL	0.15	hr	lot				
	L-WNSEM	LCSEM	0.08	hr	lot				
	L-WNREJN	delay	0.1	hr	lot				
	Blackbox	delay	10.26	hr	lot				
	L-WPEXPOSE	LCILNZ	0.94	hr	lot	128_WP			
	L-WPOVLY	LOVRL	0.15	hr	lot				
	L-WPSEM	LCSEM	0.12	hr	lot				
	L-WPREJN	delay	0.1	hr	lot				
	Blackbox	delay	9.66	hr	lot				
	L-VNEXPOSE	LCILNZ	1.71	hr	lot	128_VN			
	L-VNOVLY	LOVRL	0.15	hr	lot				
	L-VNSEM	LCSEM	0.09	hr	lot				
	L-VNREJN	delay	0.1	hr	lot				
	Blackbox	delay	5.97	hr	lot				
	L-WBEXPOSE	LCILNZ	1.76	hr	lot	128_WB			
	L-WBOVLY	LOVRL	0.15	hr	lot				
	L-WBSEM	LCSEM	0.1	hr	lot				
	L-WBREJN	delay	0.1	hr	lot				
	Blackbox	delay	58.68	hr	lot				
	L-GCEXPOSE	DUVZ1	1.06	hr	lot	128_GC			
	L-GCOVLY	LOVRL	0.5	hr	lot				
	L-GCSEM	LCSEM	0.41	hr	lot				
	L-GCREJN	delay	0.1	hr	lot				
	Blackbox	delay	27.18	hr	lot				
	L-XNEXPOSE	LCILNZ	1.02	hr	lot	128_XN			
	L-XNOVLY	LOVRL	0.15	hr	lot				
	L-XNSEM	LCSEM	0.1	hr	lot				
	L-XNREJN	delay	0.1	hr	lot				
	Blackbox	delay	41.19	hr	lot				
	L-XPEXPOSE	LCILNZ	1.02	hr	lot	128_XP			
	L-XPOVLY	LOVRL	0.15	hr	lot				
	L-XPSEM	LCSEM	0.13	hr	lot				
	L-XPREJN	delay	0.1	hr	lot				
	Blackbox	delay	56.97	hr	lot				
	L-CBEXPOSE	DUVZ1	1.17	hr	lot	128_CB			
	L-CBOVLY	LOVRL	0.15	hr	lot				
	L-CBSEM	LCSEM	0.2	hr	lot				
	L-CBREJN	delay	0.1	hr	lot				
	Blackbox	delay	66.9	hr	lot				
	L-CSEXPOSE	DUVZ1	1.23	hr	lot	128_CS			
	L-CSOVLY	LOVRL	0.15	hr	lot				
	L-CSSEM	LCSEM	0.2	hr	lot				
	L-CSREJN	delay	0.1	hr	lot				
	Blackbox	delay	10.92	hr	lot				
	L-YNEXPOSE	LCILNZ	0.97	hr	lot	128_YN			
	L-YNOVLY	LOVRL	0.15	hr	lot				
	L-YNSEM	LCSEM	0.11	hr	lot				
	L-YNREJN	delay	0.1	hr	lot				
	Blackbox	delay	21.45	hr	lot				

	L-M0EXPOSE	DUVZ1	1.15	hr	lot	128_MO			
	L-M0OVLY	LOVRL	0.15	hr	lot				
	L-M0SEM	LCSEM	0.28	hr	lot				
	L-M0REJN	delay	0.1	hr	lot				
	Blackbox	delay	56.52	hr	lot				
	L-C1EXPOSE	DUVZ2	1.55	hr	lot	128_C1			yes
	L-C1OVLY	LOVRL	0.15	hr	lot				
	L-C1SEM	LCSEM	0.22	hr	lot				
	L-C1REJN	delay	0.1	hr	lot				
	Blackbox	delay	30.9	hr	lot				
	L-R1EXPOSE	DUVZ2	1.6	hr	lot	128_R1			
	L-R1OVLY	LOVRL	0.5	hr	lot				
	L-R1SEM	LCSEM	0.41	hr	lot				
	L-R1UVHD	LDUVHD	0.42	hr	lot				
	L-R1REJN	delay	0.1	hr	lot				
	Blackbox	delay	31.56	hr	lot				
	L-C2EXPOSE	LCILNZ	1.67	hr	lot	128_C2			
	L-C2OVLY	LOVRL	0.15	hr	lot				
	L-C2SEM	LCSEM	0.12	hr	lot				
	L-C2REJN	delay	0.1	hr	lot				
	Blackbox	delay	11.7	hr	lot				
	L-M2EXPOSE	LCILNZ	1.73	hr	lot	128_M2			
	L-M2OVLY	LOVRL	0.15	hr	lot				
	L-M2SEM	LCSEM	0.11	hr	lot				
	L-M2UVHD	LDUVHD	1.14	hr	lot				
	L-M2REJN	delay	0.1	hr	lot				
	Blackbox	delay	60.87	hr	lot				

ROUTE	STEP	STNFAM	PTIME	PTUNITS	PTPER	GENRESF	SVESTN
256_route	Blackbox	delay	57.09	hr	lot		
	L-DTEXPOSE	DUVC1	1.09	hr	lot	256_DT	yes
	L-DTOVLY	LOVRL	0.34	hr	lot		
	L-DTSEM	LCSEM	0.26	hr	lot		
	L-DTWSRT	LWSRT	0.09	hr	lot		
	L-DTSCOP	LSCOP	0.2	hr	lot		
	L-DTREJN	delay	0.1	hr	lot		
	Blackbox	delay	358.53	hr	lot		
	L-AAEXPOSE	DUVC1	1.26	hr	lot	256_AA	
	L-AAOVLY	LOVRL	0.15	hr	lot		
	L-AASEM	LCSEM	0.21	hr	lot		
	L-AAWSRT	delay	0.1	hr	lot		
	Blackbox	delay	35.58	hr	lot		
	L-KVEXPOSE	LCILNZ	0.72	hr	lot	256_KV	
	L-KVSCOP	LSCOP	0.2	hr	lot		
	L-KVREJN	delay	0.1	hr	lot		
	Blackbox	delay	36.96	hr	lot		
	L-WNEXPOSE	LCILNZ	1.08	hr	lot	256_WN	
	L-WNOVLY	LOVRL	0.15	hr	lot		
	L-WNSEM	LCSEM	0.08	hr	lot		
	L-WNREJN	delay	0.1	hr	lot		
	Blackbox	delay	10.26	hr	lot		
	L-WPEXPOSE	LCILNZ	0.94	hr	lot	256_WP	
	L-WPOVLY	LOVRL	0.15	hr	lot		
	L-WPSEM	LCSEM	0.12	hr	lot		
	L-WPREJN	delay	0.1	hr	lot		
	Blackbox	delay	8.97	hr	lot		
	L-VNEXPOSE	LCILNZ	1.71	hr	lot	256_VN	
	L-VNOVLY	LOVRL	0.15	hr	lot		
	L-VNSEM	LCSEM	0.09	hr	lot		
	L-VNREJN	delay	0.1	hr	lot		
	Blackbox	delay	6.42	hr	lot		
	L-WBEXPOSE	LCILNZ	1.76	hr	lot	256_WB	
	L-WBOVLY	LOVRL	0.15	hr	lot		
	L-WBSEM	LCSEM	0.1	hr	lot		
	L-WBREJN	delay	0.1	hr	lot		
	Blackbox	delay	57.78	hr	lot		
	L-GCEXPOSE	DUVC1	1.06	hr	lot	256_GC	
	L-GCOVLY	LOVRL	0.5	hr	lot		
	L-GCSEM	LCSEM	0.41	hr	lot		
	L-GCREJN	delay	0.1	hr	lot		
	Blackbox	delay	27.18	hr	lot		
	L-XNEXPOSE	LCILNZ	1.02	hr	lot	256_XN	
	L-XNOVLY	LOVRL	0.15	hr	lot		
	L-XNSEM	LCSEM	0.1	hr	lot		
	L-XNREJN	delay	0.1	hr	lot		
	Blackbox	delay	40.74	hr	lot		
	L-XPEXPOSE	LCILNZ	1.02	hr	lot	256_XP	
	L-XPOVLY	LOVRL	0.15	hr	lot		
	L-XPSEM	LCSEM	0.13	hr	lot		
	L-XPREJN	delay	0.1	hr	lot		
	Blackbox	delay	56.97	hr	lot		
	L-CBEXPOSE	DUVC2	1.17	hr	lot	256_CB	yes
	L-CBOVLY	LOVRL	0.15	hr	lot		
	L-CBSEM	LCSEM	0.2	hr	lot		
	L-CBREJN	delay	0.1	hr	lot		
	Blackbox	delay	69.06	hr	lot		
	L-CSEXPOSE	DUVC2	1.23	hr	lot	256_CS	
	L-CSOVLY	LOVRL	0.15	hr	lot		
	L-CSSEM	LCSEM	0.2	hr	lot		
	L-CSREJN	delay	0.1	hr	lot		
	Blackbox	delay	11.28	hr	lot		
	L-YNEXPOSE	LCILNZ	0.97	hr	lot	256_YN	
	L-YNOVLY	LOVRL	0.15	hr	lot		
	L-YNSEM	LCSEM	0.11	hr	lot		
	L-YNREJN	delay	0.1	hr	lot		
	Blackbox	delay	21.45	hr	lot		

	L-M0EXPOSE	DUVC2	1.15	hr	lot	256_MO	
	L-M0OVLY	LOVRL	0.15	hr	lot		
	L-M0SEM	LCSEM	0.28	hr	lot		
	L-M0REJN	delay	0.1	hr	lot		
	Blackbox	delay	57.33	hr	lot		
	L-C1EXPOSE	DUVC3	1.55	hr	lot	256_C1	yes
	L-C1OVLY	LOVRL	0.15	hr	lot		
	L-C1SEM	LCSEM	0.22	hr	lot		
	L-C1REJN	delay	0.1	hr	lot		
	Blackbox	delay	28.71	hr	lot		
	L-R1EXPOSE	DUVC3	1.6	hr	lot	256_R1	
	L-R1OVLY	LOVRL	0.5	hr	lot		
	L-R1SEM	LCSEM	0.41	hr	lot		
	L-R1UVHD	LDUVHD	0.42	hr	lot		
	L-R1REJN	delay	0.1	hr	lot		
	Blackbox	delay	34.53	hr	lot		
	L-C2EXPOSE	LCILNZ	1.67	hr	lot	256_C2	
	L-C2OVLY	LOVRL	0.15	hr	lot		
	L-C2SEM	LCSEM	0.12	hr	lot		
	L-C2REJN	delay	0.1	hr	lot		
	Blackbox	delay	9.72	hr	lot		
	L-M2EXPOSE	LCILNZ	1.73	hr	lot	256_M2	
	L-M2OVLY	LOVRL	0.15	hr	lot		
	L-M2SEM	LCSEM	0.11	hr	lot		
	L-M2UVHD	LDUVHD	1.14	hr	lot		
	L-M2REJN	delay	0.1	hr	lot		
	Blackbox	delay	60.87	hr	lot		

APPENDIX D: STATION FILE

STNFAM	STN	RULE	TRACE	FWLRANK	RWLRANK
DUVC1	DUVC04	rule_FIRST_A	both		
	DUVC05	rule_FIRST_A	both		
	DUVC09	rule_FIRST_A	both		
	DUVC10	rule_FIRST_A	both		
DUVC2	DUVC14	rule_FIRST_A	both		
	DUVC16	rule_FIRST_A	both		
	DUVC17	rule_FIRST_A	both		
DUVC3	DUVC18	rule_FIRST_A	both		
	DUVC19	rule_FIRST_A	both		
	DUVC20	rule_FIRST_A	both		
DUVZ1	DUVZ08	rule_FIRST_A	both		
	DUVZ12	rule_FIRST_A	both		
	DUVZ13	rule_FIRST_A	both		
	DUVZ15	rule_FIRST_A	both		
DUVZ2	DUVZ03	rule_FIRST_A	both		
	DUVZ11	rule_FIRST_A	both		
LCILNZ	ILNZ01	rule_FIRST_A	both		
	ILNZ02	rule_FIRST_A	both		
	ILNZ03	rule_FIRST_A	both		
	ILNZ04	rule_FIRST_A	both		
	ILNZ05	rule_FIRST_A	both		
	ILNZ06	rule_FIRST_A	both		
	ILNZ07	rule_FIRST_A	both		
	ILNZ08	rule_FIRST_A	both		
	ILNZ09	rule_FIRST_A	both		
	ILNZ10	rule_FIRST_A	both		
	ILNZ11	rule_FIRST_A	both		
	ILNZ12	rule_FIRST_A	both		
	ILNZ13	rule_FIRST_A	both		
	ILNZ14	rule_FIRST_A	both		
	INLZ15	rule_FIRST_A	both		
	ILNZ16	rule_FIRST_A	both		
	ILNZ17	rule_FIRST_A	both		
LCSEM	CSEM01	rule_FIRST	both		
	CSEM02	rule_FIRST	both		
	CSEM03	rule_FIRST	both		
	CSEM04	rule_FIRST	both		
	CSEM05	rule_FIRST	both		
	CSEM06	rule_FIRST	both		
	CSEM07	rule_FIRST	both		
	CSEM08	rule_FIRST	both		
	CSEM09	rule_FIRST	both		
LDUVHD	UVHD01	rule_FIRST	both		
	UVHD02	rule_FIRST	both		
	UVHD03	rule_FIRST	both		
	UVHD04	rule_FIRST	both		
LOVRL	OVRL01	rule_FIRST	both		
	OVRL02	rule_FIRST	both		
	OVRL03	rule_FIRST	both		
	OVRL04	rule_FIRST	both		
	OVRL05	rule_FIRST	both		
	OVRL06	rule_FIRST	both		
LSCOP	SCOP15	rule_FIRST	both		
	SCOP16	rule_FIRST	both		
	SCOP17	rule_FIRST	both		
	SCOP18	rule_FIRST	both		
	SCOP19	rule_FIRST	both		
LWSRT	WSRT18	rule_FIRST	both		
	WSRT19	rule_FIRST	both		

APPENDIX E: RETICLE FILE

GENRESFAM	GENRES	RULE	TRACE
64_DT	64_DT_1	rule_FIRST	
	64_DT_2	rule_FIRST	
64_AA	64_AA_1	rule_FIRST	
	64_AA_2	rule_FIRST	
64_KV	64_KV_1	rule_FIRST	
	64_KV_2	rule_FIRST	
64_WN	64_WN_1	rule_FIRST	
	64_WN_2	rule_FIRST	
64_WP	64_WP_1	rule_FIRST	
	64_WP_2	rule_FIRST	
64_VN	64_VN_1	rule_FIRST	
	64_VN_2	rule_FIRST	
64_WB	64_WB_1	rule_FIRST	
	64_WB_2	rule_FIRST	
64_GC	64_GC_1	rule_FIRST	
	64_GC_2	rule_FIRST	
64_XN	64_XN_1	rule_FIRST	
	64_XN_2	rule_FIRST	
64_XP	64_XP_1	rule_FIRST	
	64_XP_2	rule_FIRST	
64_CB	64_CB_1	rule_FIRST	
	64_CB_2	rule_FIRST	
64_CS	64_CS_1	rule_FIRST	
	64_CS_2	rule_FIRST	
64_YN	64_YN_1	rule_FIRST	
	64_YN_2	rule_FIRST	
64_MO	64_M0_1	rule_FIRST	
	64_M0_2	rule_FIRST	
64_C1	64_C1_1	rule_FIRST	
	64_C1_2	rule_FIRST	
64_R1	64_R1_1	rule_FIRST	
	64_R1_2	rule_FIRST	
64_C2	64_C2_1	rule_FIRST	
	64_C2_2	rule_FIRST	
64_M2	64_M2_1	rule_FIRST	
	64_M2_2	rule_FIRST	
128_DT	128_DT_1	rule_FIRST	
	128_DT_2	rule_FIRST	
	128_DT_3	rule_FIRST	
128_AA	128_AA_1	rule_FIRST	
	128_AA_2	rule_FIRST	
	128_AA_3	rule_FIRST	
128_KV	128_KV_1	rule_FIRST	
	128_KV_2	rule_FIRST	
	128_KV_3	rule_FIRST	
128_WN	128_WN_1	rule_FIRST	
	128_WN_2	rule_FIRST	
	128_WN_3	rule_FIRST	
128_WP	128_WP_1	rule_FIRST	
	128_WP_2	rule_FIRST	
	128_WP_3	rule_FIRST	
128_VN	128_VN_1	rule_FIRST	
	128_VN_2	rule_FIRST	
	128_VN_3	rule_FIRST	
128_WB	128_WB_1	rule_FIRST	
	128_WB_2	rule_FIRST	
	128_WB_3	rule_FIRST	
128_GC	128_GC_1	rule_FIRST	

	128_GC_2	rule_FIRST	
	128_GC_3	rule_FIRST	
128_XN	128_XN_1	rule_FIRST	
	128_XN_2	rule_FIRST	
	128_XN_3	rule_FIRST	
128_XP	128_XP_1	rule_FIRST	
	128_XP_2	rule_FIRST	
	128_XP_3	rule_FIRST	
128_CB	128_CB_1	rule_FIRST	
	128_CB_2	rule_FIRST	
	128_CB_3	rule_FIRST	
128_CS	128_CS_1	rule_FIRST	
	128_CS_2	rule_FIRST	
	128_CS_3	rule_FIRST	
128_YN	128_YN_1	rule_FIRST	
	128_YN_2	rule_FIRST	
	128_YN_3	rule_FIRST	
128_MO	128_M0_1	rule_FIRST	
	128_M0_2	rule_FIRST	
	128_M0_3	rule_FIRST	
128_C1	128_C1_1	rule_FIRST	
	128_C1_2	rule_FIRST	
	128_C1_3	rule_FIRST	
128_R1	128_R1_1	rule_FIRST	
	128_R1_2	rule_FIRST	
	128_R1_3	rule_FIRST	
128_C2	128_C2_1	rule_FIRST	
	128_C2_2	rule_FIRST	
	128_C2_3	rule_FIRST	
128_M2	128_M2_1	rule_FIRST	
	128_M2_2	rule_FIRST	
	128_M2_3	rule_FIRST	
256_DT	256_DT_1	rule_FIRST	
	256_DT_2	rule_FIRST	
	256_DT_3	rule_FIRST	
256_AA	256_AA_1	rule_FIRST	
	256_AA_2	rule_FIRST	
	256_AA_3	rule_FIRST	
256_KV	256_KV_1	rule_FIRST	
	256_KV_2	rule_FIRST	
	256_KV_3	rule_FIRST	
256_WN	256_WN_1	rule_FIRST	
	256_WN_2	rule_FIRST	
	256_WN_3	rule_FIRST	
256_WP	256_WP_1	rule_FIRST	
	256_WP_2	rule_FIRST	
	256_WP_3	rule_FIRST	
256_VN	256_VN_1	rule_FIRST	
	256_VN_2	rule_FIRST	
	256_VN_3	rule_FIRST	
256_WB	256_WB_1	rule_FIRST	
	256_WB_2	rule_FIRST	
	256_WB_3	rule_FIRST	
256_GC	256_GC_1	rule_FIRST	
	256_GC_2	rule_FIRST	
	256_GC_3	rule_FIRST	
256_XN	256_XN_1	rule_FIRST	
	256_XN_2	rule_FIRST	
	256_XN_3	rule_FIRST	
256_XP	256_XP_1	rule_FIRST	
	256_XP_2	rule_FIRST	
	256_XP_3	rule_FIRST	
256_CB	256_CB_1	rule_FIRST	
	256_CB_2	rule_FIRST	
	256_CB_3	rule_FIRST	
256_CS	256_CS_1	rule_FIRST	
	256_CS_2	rule_FIRST	
	256_CS_3	rule_FIRST	
256_YN	256_YN_1	rule_FIRST	
	256_YN_2	rule_FIRST	
	256_YN_3	rule_FIRST	
256_MO	256_M0_1	rule_FIRST	
	256_M0_2	rule_FIRST	
	256_M0_3	rule_FIRST	
256_C1	256_C1_1	rule_FIRST	
	256_C1_2	rule_FIRST	

APPENDIX F: STATION DOWN FILE

RESTYPE	RESNAME	CALTYPE	CALNAME
stn	DUVC04	down	DUVC04_down
	DUVC05	down	DUVC05_down
	DUVC09	down	DUVC09_down
	DUVC10	down	DUVC10_down
	DUVC14	down	DUVC14_down
	DUVC16	down	DUVC16_down
	DUVC17	down	DUVC17_down
	DUVC18	down	DUVC18_down
	DUVC19	down	DUVC19_down
	DUVC20	down	DUVC20_down
	DUVZ03	down	DUVZ03_down
	DUVZ08	down	DUVZ08_down
	DUVZ11	down	DUVZ11_down
	DUVZ12	down	DUVZ12_down
	DUVZ13	down	DUVZ13_down
	DUVZ15	down	DUVZ15_down
	ILNZ01	down	ILNZ01_down
	ILNZ02	down	ILNZ02_down
	ILNZ03	down	ILNZ03_down
	ILNZ04	down	ILNZ04_down
	ILNZ05	down	ILNZ05_down
	ILNZ06	down	ILNZ06_down
	ILNZ07	down	ILNZ07_down
	ILNZ08	down	ILNZ08_down
	ILNZ09	down	ILNZ09_down
	ILNZ10	down	ILNZ10_down
	ILNZ11	down	ILNZ11_down
	ILNZ12	down	ILNZ12_down
	ILNZ13	down	ILNZ13_down
	ILNZ14	down	ILNZ14_down
	INLZ15	down	ILNZ15_down
	ILNZ16	down	ILNZ16_down
	ILNZ17	down	ILNZ17_down
	CSEM01	down	CSEM01_down
	CSEM02	down	CSEM02_down
	CSEM03	down	CSEM03_down
	CSEM04	down	CSEM04_down
	CSEM05	down	CSEM05_down
	CSEM06	down	CSEM06_down
	CSEM07	down	CSEM07_down
	CSEM08	down	CSEM08_down
	CSEM09	down	CSEM09_down
	UVHD01	down	UVHD01_dowm
	UVHD02	down	UVHD02_dowm
	UVHD03	down	UVHD03_dowm
	UVHD04	down	UVHD04_dowm
	OVRL01	down	OVRL01_down
	OVRL02	down	OVRL02_down
	OVRL03	down	OVRL03_down
	OVRL04	down	OVRL04_down
	OVRL05	down	OVRL05_down
	OVRL06	down	OVRL06_down
	SCOP15	down	SCOP15_down
	SCOP16	down	SCOP16_down
	SCOP17	down	SCOP17_down
	SCOP18	down	SCOP18_down
	SCOP19	down	SCOP19_down
	WSRT18	down	WSRT18_down
	WSRT19	down	WSRT19_down

DOWNCALNAME	DOWNCALTYPE	MTTF	MTTFUNITS	MTTR	MTTRUNITS
DUVC04_down	mttf_by_proctime	28.94885	hr	3	hr
DUVC05_down	mttf_by_proctime	24.12678	hr	2.358925	hr
DUVC09_down	mttf_by_proctime	28.55128	hr	3.24845	hr
DUVC10_down	mttf_by_proctime	30.4686	hr	2.10145	hr
DUVC14_down	mttf_by_proctime	36.30673	hr	2.676779	hr
DUVC16_down	mttf_by_proctime	36.30673	hr	2.676779	hr
DUVC17_down	mttf_by_proctime	33.16688	hr	1.60135	hr
DUVC18_down	mttf_by_proctime	35.4499	hr	1.6417	hr
DUVC19_down	mttf_by_proctime	42.77058	hr	2.003025	hr
DUVC20_down	mttf_by_proctime	62.63323	hr	1.079375	hr
DUVZ03_down	mttf_by_proctime	42.77058	hr	2.003025	hr
DUVZ08_down	mttf_by_proctime	28.57703	hr	1.69715	hr
DUVZ11_down	mttf_by_proctime	52.51063	hr	1.82015	hr
DUVZ12_down	mttf_by_proctime	32.2502	hr	1.2902	hr
DUVZ13_down	mttf_by_proctime	37.74218	hr	1.203275	hr
DUVZ15_down	mttf_by_proctime	30.00095	hr	1.275425	hr
ILNZ01_down	mttf_by_proctime	81.4346	hr	1.341	hr
ILNZ02_down	mttf_by_proctime	106.2403	hr	1.31655	hr
ILNZ03_down	mttf_by_proctime	163.6902	hr	1.303025	hr
ILNZ04_down	mttf_by_proctime	139.763	hr	1.083325	hr
ILNZ05_down	mttf_by_proctime	121.3546	hr	1.110275	hr
ILNZ06_down	mttf_by_proctime	143.8507	hr	1.014	hr
ILNZ07_down	mttf_by_proctime	84.3619	hr	1.148225	hr
ILNZ08_down	mttf_by_proctime	86.2831	hr	1.445875	hr
ILNZ09_down	mttf_by_proctime	127.8204	hr	1.097575	hr
ILNZ10_down	mttf_by_proctime	115.6959	hr	0.976925	hr
ILNZ11_down	mttf_by_proctime	92.3027	hr	1.363125	hr
ILNZ12_down	mttf_by_proctime	123.6331	hr	1.462675	hr
ILNZ13_down	mttf_by_proctime	75.44033	hr	1.390225	hr
ILNZ14_down	mttf_by_proctime	107.4852	hr	1.54295	hr
ILNZ15_down	mttf_by_proctime	113	hr	1.014	hr
ILNZ16_down	mttf_by_proctime	123	hr	1.148225	hr
ILNZ17_down	mttf_by_proctime	127	hr	1.445875	hr
CSEM01_down	mttf_by_proctime	51.4174	hr	3.8694	hr
CSEM02_down	mttf_by_proctime	129.3419	hr	1.54155	hr
CSEM03_down	mttf_by_proctime	219.5279	hr	10.00105	hr
CSEM04_down	mttf_by_proctime	255.8224	hr	0.92795	hr
CSEM05_down	mttf_by_proctime	116.537	hr	4.4758	hr
CSEM06_down	mttf_by_proctime	59.96695	hr	9.28745	hr
CSEM07_down	mttf_by_proctime	86.3265	hr	2.1762	hr
CSEM08_down	mttf_by_proctime	86.9917	hr	2.7784	hr
CSEM09_down	mttf_by_proctime	125.7415	hr	4.382225	hr
UVHD01_dowm	mttf_by_proctime	401.9657	hr	1.20405	hr
UVHD02_dowm	mttf_by_proctime	253.0543	hr	1.265	hr
UVHD03_dowm	mttf_by_proctime	116.6921	hr	2.7317	hr
UVHD04_dowm	mttf_by_proctime	200	hr	2	hr
OVRL01_down	mttf_by_proctime	68.0639	hr	1.23025	hr
OVRL02_down	mttf_by_proctime	85.4272	hr	0.785	hr
OVRL03_down	mttf_by_proctime	64.14605	hr	0.8702	hr
OVRL04_down	mttf_by_proctime	88.70845	hr	1.04135	hr
OVRL05_down	mttf_by_proctime	100.8917	hr	1.3296	hr
OVRL06_down	mttf_by_proctime	81.44746	hr	1.05128	hr
SCOP15_down	mttf_by_proctime	200	hr	2	hr
SCOP16_down	mttf_by_proctime	210	hr	2	hr
SCOP17_down	mttf_by_proctime	185	hr	2	hr
SCOP18_down	mttf_by_proctime	193	hr	2	hr
SCOP19_down	mttf_by_proctime	189	hr	2	hr
WSRT18_down	mttf_by_proctime	220	hr	2	hr
WSRT19_down	mttf_by_proctime	212	hr	2	hr

APPENDIX G: PM FILE

PMCALNAME	PMCALTY	TRACE	MTBPM	MTBPMUN	MTTR	MTTRUNITS
DUVC1_pm	tbpm_by_cal		30	day	10	hr
DUVC2_pm	tbpm_by_cal		30	day	10	hr
DUVC3_pm	tbpm_by_cal		30	day	10	hr
DUVZ1_pm	tbpm_by_cal		30	day	10	hr
DUVZ2 _pm	tbpm_by_cal		30	day	10	hr
ILNZ_pm	tbpm_by_cal		30	day	10	hr
CSEM_pm	tbpm_by_cal		30	day	10	hr
UVHD_pm	tbpm_by_cal		30	day	10	hr
OVRL_pm	tbpm_by_cal		30	day	10	hr
SCOP_pm	tbpm_by_cal		30	day	10	hr
WSRT_pm	tbpm_by_cal		30	day	10	hr

RESTYPE	RESNAME	CALTYPE	CALNAME	FOADIST	FOA	FOAUNITS
stnfam	DUVC1	pm	DUVC1_pm	constant	30	day
	DUVC2	pm	DUVC2_pm	constant	30	day
	DUVC3	pm	DUVC3_pm	constant	30	day
	DUVZ1	pm	DUVZ1_pm	constant	30	day
	DUVZ2	pm	DUVZ2 _pm	constant	30	day
	LCILNZ	pm	ILNZ_pm	constant	30	day
	LCSEM	pm	CSEM_pm	constant	30	day
	LDUVHD	pm	UVHD_pm	constant	30	day
	LOVRL	pm	OVRL_pm	constant	30	day
	LSCOP	pm	SCOP_pm	constant	30	day
	LWSRT	pm	WSRT_pm	constant	30	day

VITA

Madhav R. Kidambi

Madhav Kidambi obtained the degree of Bachelor of Engineering in Mechanical Engineering from Nagpur University, India. After the completion of his undergraduate program he worked as a Trainee Engineer at Bajaj Auto Ltd. at Waluj, India for one and half years in Engine and Transmission division. During this period, he developed a keen interest in manufacturing systems and he decided to pursue his Masters in Industrial and Systems Engineering with concentration in Manufacturing Systems at Virginia Tech. During his M.S., he worked as a Research Assistant for Ericsson, Lynchburg, Virginia for nine months and for Infineon Technologies, Richmond, Virginia with Dr.S.Sarin as Principal Investigator. He also did three months internship at Infineon Technologies, Richmond, Virginia. He is Currently a Systems Engineer for Infineon Technologies, Richmond specializing in Fab simulation and Dispatching.