Chapter I Introduction

1.1 Importance of Packaging in Power Electronics

Power electronics, as defined by Thomas G. Wilson, is:" The technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form."[1] The goal of power electronics is to realize power conversion from an electrical source to an electrical load in a highly efficient, highly reliable and cost-effective way. The application of power electronics includes a variety of fields such as energy storage, transmission and distribution, pollution avoidance, communication, computer systems, propulsion and transportation[2]. Power electronics modules are key units in a power electronics system. As the integration of power switches, device gating, sensors, controls and actuators, power modules can be used to perform energy transfer, storage and conditioning.

Over the last twenty years, industrial and research efforts on electronic power conversion are making the move toward high-frequency synthesis,[2] which results in great improvement in converter performance, miniaturization in physical size and reduction of mass weight and cost. This is pushing the limits of existing control, packaging and thermal management technology. For example, when the switching performance of silicon devices improves, controlling and reducing losses from packaging materials in packages become increasingly important. For this reason, power conversion technology will more urgently demand the solutions to the challenges of reducing the packaging parasitic capacitance and inductance as well as efficient dissipation of ever-increasing heat rather than the semiconductor devices and circuit topology. Meanwhile, the long design cycle and labor-intensive, costly manufacturing process of power electronics systems reveal another major barrier: the striking lack of standardization, or more generically, system integration.

Power electronics packages provide mechanical support, device protection, cooling and electrical connection and isolation. The drive to reduce the fabrication cost and energy conservation has put increasing pressure on the energy density within the power

modules. This means more silicon chips must be placed into a more compact package. Therefore, thermal and mechanical designs are of significant importance.

In the scope of microelectronic packaging, the chip connection is evolving from the wire bond of 1970's, 1980's and 1990's to flip chip technology today and in the future.[3] As a consequence, the package interconnection developed from the very early PTH in the 1970's and the SMT in 1980's to the BGA SMT and CSP SMT in the 1990's. The earlier single-chip packaging evolution is predicted to lead to Single-Level Integrated Module (SLIM) Multichip Packaging in the next century (courtesy of Georgia Tech). Unlike microelectronic packaging technology, power electronics packaging has not kept pace with the development of semiconductor devices. Power devices underwent generation by generation improvements and can now handle significant power density. On the other hand, since the adoption of wire bonding technology in power modules, it remains the prevalent format for chip connections in power modules. This situation has not changed much during the past decades: A typical traditional package form is a single-packaged device soldered to the substrates, with embedded wire bond inside to interconnect the chip to the outside leads, and housed by a plastic encapsulation.

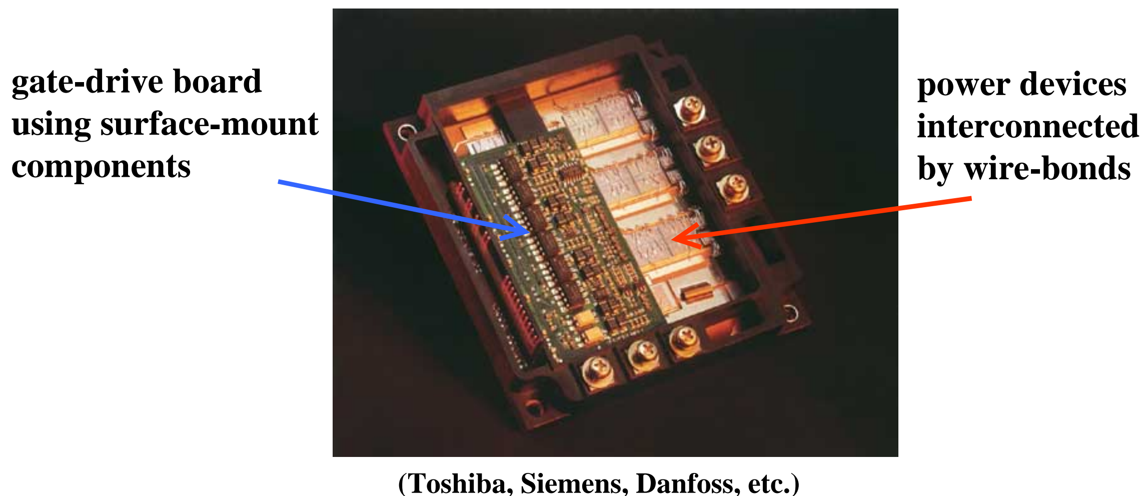
The fast-growing heat dissipation combined with the reduced package volume poses a challenge and is a vital barrier for current power packaging design. Sean C. O Mathuna, et al has given an example of why reducing DC resistance in the package interconnect is so important.[4] Using the requirement of the year 1997 to design a power supply (Vout = 2.5 V, Pout = 70W, Area = 35cm^2, Tj_{max} = 125°C, $Tair_{max}$ = 55°C), the thermal resistance of the power supply must be lower than 145°C/Wcm^2 if the output stage resistance is no more than 20mΩ. Keeping the thermal resistance at the same value, in the year 2001 (Vout = 1.5 V, Pout = 110W, Area = 28.5cm^2, Tj_{max} = 125°C, $Tair_{max}$ = 55°C), the related output stage electrical resistance has to be no more than 1mΩ to meet the above requirement. In this situation, even if the on-resistance of the MOSFET is reduced to zero, the conduction loss of the overall interconnections might still exceed the desired 1mΩ value. In current interconnect technology, for example, if using four parallel, 100µm (4mil) diameter, 5mm long aluminum bond wires, the DC-resistance is 6.8mΩ, which does not satisfy the power loss requirement. This is just one

of the many problems in concurrent power packaging design. The recent trend of exploring three-dimensional power packaging design shows great potential in addressing the above problems. Shorter interconnect, lower DC resistance and parasitic noise and better heat-removal capability and reliability is anticipated to be some of the new features using feasible 3-D packaging design. The implementation of 3-D power packaging, however, requires system design effort combining expertise in electronics, materials, mechanical engineering, manufacturing and system design to improve the overall packaging design.

1.2 Overview of Existing and Developing Techniques for Power Electronics Packaging

1.2.1 State-of-the-art Power Electronics Packaging

The state-of-the-art power electronics packaging, as shown Figure I-1, is formatted with two circuit layers. The bottom is a thick copper layer mounted on a heat sink, with the power devices soldered on the substrate. Usually a multilayer FR4 PCB is used for the driver, sensors, protection circuits and control circuitry, and is mounted on top of the power devices and connected to the power device circuitry via vertical pins. A silicone type material will be used to fill in the package, and a plastic case will house the whole package. The entire manufacturing process is cost and labor intensive, and the time-to-market delays for custom circuits are significant.



(Toshiba, Siemens, Danfoss, etc.)

Figure I-1 State-of-the-art Power electronics packaging

It is thus expected that many of the breakthrough gains in power conversion density and thermal management in the near future will come from the emerging packaging technologies, such as the chip-scale and three-dimensional packaging. Innovative interconnect techniques will revolutionize the traditional packaging methodology, bringing about the important benefits of lower interconnect resistance, less noise and parasitic oscillations, improved reliability, better thermal management, higher level of system integration of power devices, driver circuitry, controls, sensors and communication connections, and last, reduced cost.

1.2.2 Pressure Contact Assembly Structure:

In high-power applications such as HVDC, SVC, transportation systems and motor drives, the pressure contact approach to packaging high-power semiconductor devices such as diodes, thyristors, GTOs, etc., has been proved to be efficient and reliable.[5] Although aluminum wire bonding technology and soldering still dominate in medium- and low-power device packaging, plastic module IGBTs are now going to be used in higher-power applications such as traction and large motor drives. Thuss research interest has been raised in the study of a pressure contact assembly structure applied to IGBTs. The pressure contact concept, experienced through several stages, has now evolved to a sandwiched structure which includes anode-side Cu plate, anode-side thermal compensating metal disc Mo, silicon device, cathode-side thermal compensating metal disc and cathode-side grooved Cu post, as shown in Figure I-2.

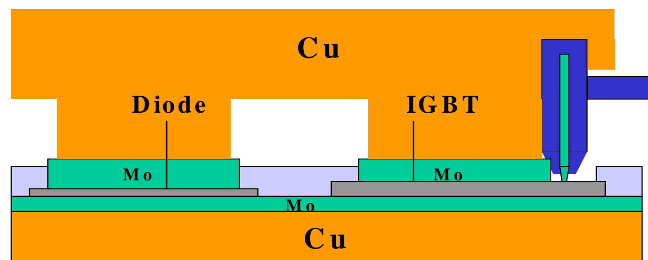


Figure I-2 Pressure Contact Assembly Structure

The wafer size has expanded from less than 60mm to 6 inches in diameter after entire removal of the solder layer. Since no soldering process is involved, this method eliminates the residual stress on each material, but also raises the concern of mechanical

damage caused by pressure force. Hideo Matsuda, et al has performed stress analysis and examined the electrical characteristics for both planar and trench gate structures under the pressed emitter electrode condition. There were no mechanical damages or changes in electrical characteristics observed. The stress analysis showed uniformity on the chips from the grooved Cu post structure.

1.2.3 GE's Thin-film Power Overlay Technology

The thin-film power overlay (POL) technology developed at General Electric is another approach aimed at reducing the cost of mass production and improving the reliability and efficiency of power electronics packages.

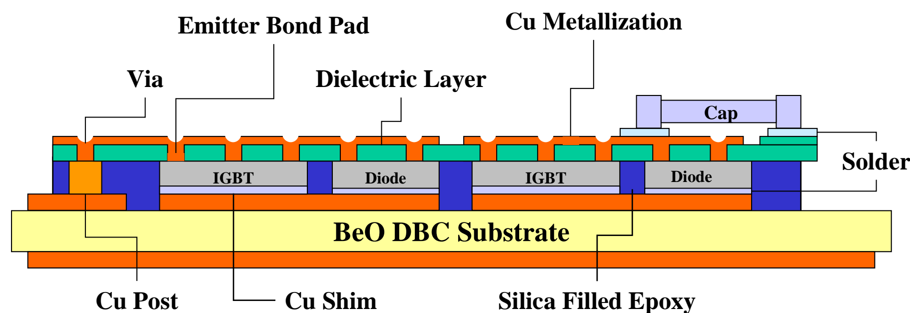


Figure I-3 GE's Power Overlay Technology

Figure I-3 shows a cross-sectional view of the POL design concept. Power semiconductor devices are soldered to a Direct Bonded Copper (DBC) substrate from the backside. Differences in device thickness are compensated by copper shims. A thin layer of polyimide sheet is laminated over the die after vias are laser machined or mechanically punched through the film. These vias provide openings for the power interconnect to the top layer. The whole top surface is then metallized (electro-plated) with copper. Circuit patterns are achieved by the application of photoresist and chemical etching processes. More layers can be built up repeatedly to realize a multilayered interconnect structure. Low-profile passive components can be embedded into the overlay flex. This technology has the following advantages:

- Elimination of wire bonds with metallurgical interconnections

- Higher performance---reduced interconnection parasitics allow higher frequency operation

- Improved thermal performance---minimizes numbers of thermal interfaces and allows two-sided heat removal

- Reduced profile and more flexible packaging options---allows innovative stacking approaches for circuit packaging; components such as capacitors can be mounted on top

- Low cost: Commercialized Power Overlay has a packaging cost of less than \$1.00 per in^2

The inherent multilayer nature of POL technology will facilitate the integration of gate drive and other circuits into the three-dimensional package of Power Electronic Building Blocks (PEBB) modules. Improved thermal management, reliability and performance are the potentially attractive features of POL technology.

1.2.4 Metal-Posts Interconnected Parallel-Plate Structure (MPIPPS)

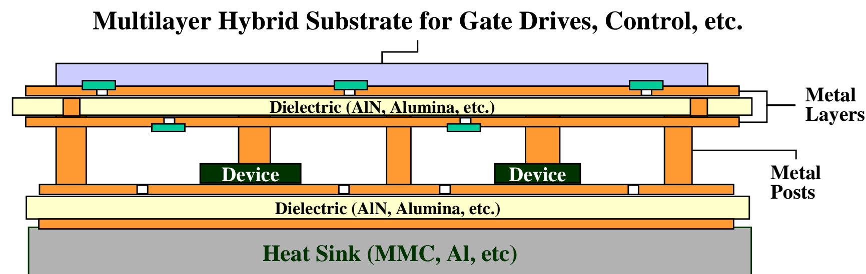


Figure I-4 MPIPPS Packaging Concept (Currently Being Developed at Virginia Tech)

Currently under development at Virginia Polytechnic Institute and State University, this is a three-dimensional packaging technique developed for power electronic building blocks, as shown in Figure I-4. Successfully demonstrated for simple building block circuitry, this technique uses direct copper bonding rather than wire bonding to interconnect power devices. The parallel-plate structure provides the potential for double-sided cooling, direct liquid cooling of the power devices between the plates, and integration of passive components in the module. The thick copper post interconnect has

lower DC-resistance than conventional aluminum wire bonding. It has also been concluded that the parasitic noise is much lower compared with the wire bonding technique, according to the work done by Kun Xing et al.[6]. Key processing step for this technology is the acquisition of solderable devices through metallization of the Aluminum contact, which can be done by thin film sputtering and subsequent electrolyte/electroless plating of Ti/Cr, Ni and Cu.

1.2.5 Multilayer Integration Technology[7]

Currently being developed at Virginia Tech, this technology features a four-layered structure: the substrate, power layer, dielectric, and conductive layer for the drive/control circuit, from bottom to top, as shown in Figure I-5.

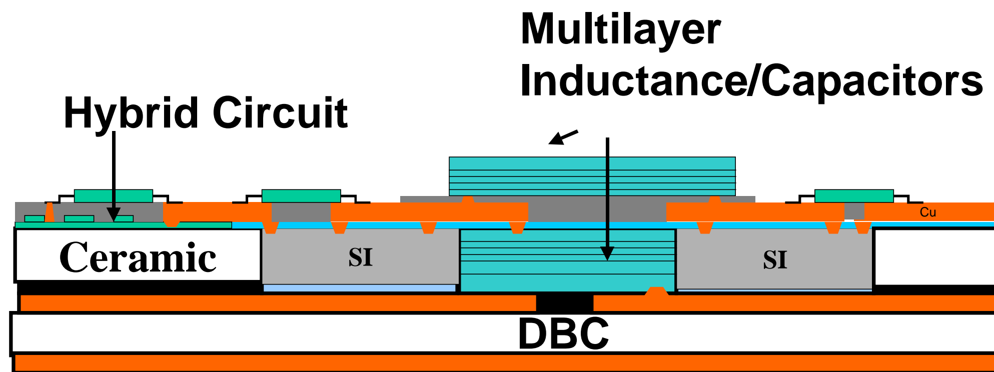


Figure I-5 Multilayer Integration Technology (Currently Being Developed at Virginia Tech)

An Aluminum Nitride (AlN) DBC is employed as the base substrate. The power devices are directly attached to the substrate by soldering. A ceramic plate with appropriate thickness is then bonded to the DBC using epoxy to embed the power devices. This is done by micro-machining openings on the ceramic substrate using laser beams. A dielectric material is then coated onto the power layer to flatten out the surface and serve as an electrical insulation layer. Via holes for power device pads are made by photoresist developing. The top surface is metallized with a solderable Cu layer, which will be patterned to form the driver circuit layout. Hybrid circuit technology can be used to fabricate the driver/control circuit. Thus, the resulting low-profile, low-parasitic noise power module with various integrated passive components constitute the attractive

features of this technique, although the implementation work needs to tackle some technical difficulties and its thermal management is yet to be evaluated.

1.2.6 Concept of the Future Integrated Power Electronics Module (IPEM) from Center of Power Electronics Systems, Virginia Tech

The Center for Power Electronics Systems (CPES), an NSF-funded research program, has teamed up expertise from five universities and covered virtually all the areas needed to advance the power electronics technologies. Advanced Power electronics packaging is a critical part of the CPES program. The goal of the CPES packaging subthrust is to achieve three-dimensional, high-level integrated power electronics modules (IPEMs), as shown in Figure I-6. Improvements will be made in thermal management, parasitics and electromagnetic noise reduction, integration of passive components, reliability against thermal cycling, and cost.

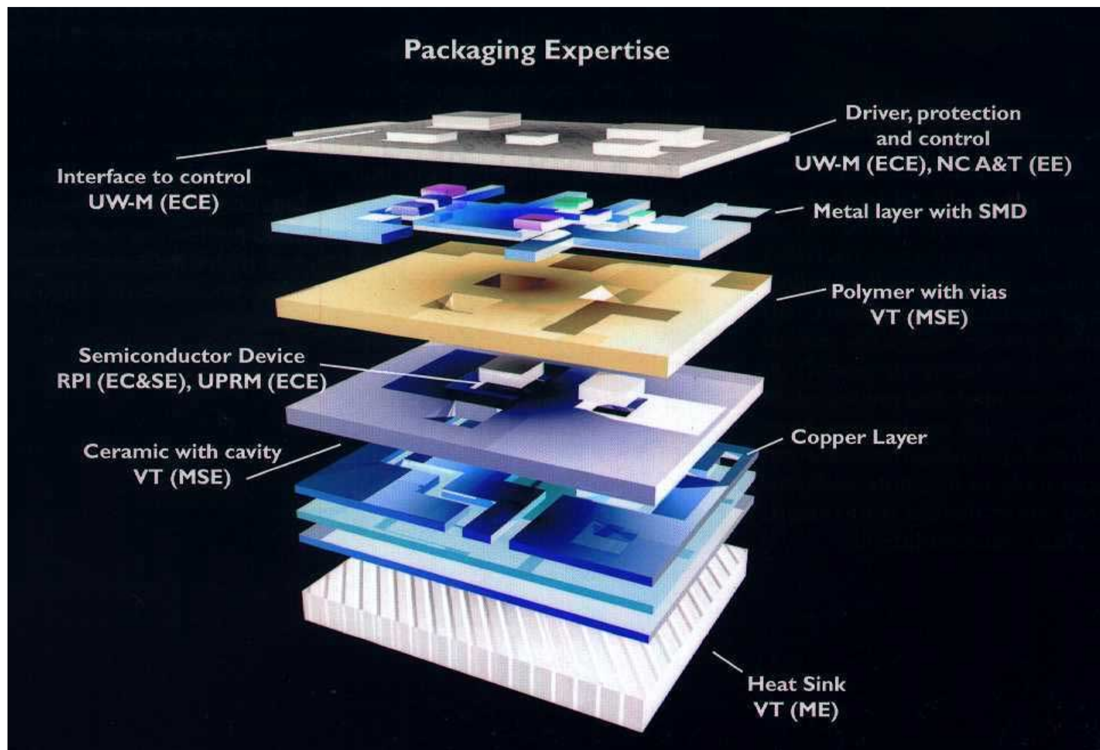


Figure I-6 Concept of IPEM at CPES

1.3 Motivation, Objectives, Approach and Outline

1.3.1 Motivation and Objectives

Due to their complex format, innovative 3-D packaging technologies have yet to be well understood. New power module package designs are required to provide semiconductor devices lifetime protection from adverse interactions with even severe environment. Such interactions include hostile gases, electro-chemical reactions and electrostatic discharge (ESD). Thermal fatigue, however, is an important failure mode that is intrinsic to electronic devices and packages. The fabrication stage might initiate the occurrence of micro defects, which will manifest as weak locations where, during thermal and power cycling, cracking or delamination most likely to occur. The turn-on and turn-off of devices will produce operation cycles in the modules. Therefore, temperature continues to be the most direct and influencing environmental factor affecting the performance of new power electronics modules. To some extent, the situation that contemporary power packaging engineers are facing is even more challenging. Electrical, thermal, and mechanical performance of the modules deteriorates dramatically when the temperature goes beyond the design boundary. The change in thermal environment, whether due to external or internal factors, has to be taken into account early in the design stage in order to maintain appropriate conditions and to ensure module functionality.

The tasks for thermal and thermo-mechanical analysis involve in-depth study using experimental techniques and computer simulation. This in-depth study helps in understanding key issues of thermal management and reliability in power electronics packaging, and allows for effective exploration of new packaging schemes to meet these challenges.

Thus the primary objectives of this work are (by parametric modeling and evaluation of the conventional and innovative 3-D high-power packaging technologies) to compare the strengths and weaknesses of each packaging design, to gain further understanding in thermal management and thermo-mechanical reliability evaluation, and to evaluate what effects three-dimensional packaging designs have on thermal and mechanical aspects in

high-density, low-profile and high-performance power modules before establishing processing guidelines.

1.3.2 Approach

Available approaches to evaluate thermal fatigue in packages vary from experimental methods to numerical methods. In the experimental approach, electrical, mechanical or thermal metric during thermal cycles will be monitored and inspected in many different ways. These methods include: the use of strain gauges and Moiré Interferometry for stress and strain measurement; Scanning Electron Micrography (SEM) to map microstructure and displacement in solder joints, interfaces and components; infrared thermal imaging system to characterize the surface temperature of packages; and thermal, mechanical, and power cycling to simulate the real service condition.

Numerical analysis in both thermo-mechanical and electrical aspect, however, has been overwhelmingly dominated by finite element modeling (FEM). FEM solves displacements and stresses in a structure by discretizing it into a finite number of regularly shaped elements. Constitutive and equilibrium equations are applied to each element, taking into consideration external thermal and mechanical loading and boundary constraints. The individual element behaviors will be obtained by solving the resultant huge sets of linear equations using high-speed computers. The summation of which produces the expected behavior of the actual structure. As a cost-effective and time-effective analytical approach, finite element method has proved itself to be a very powerful tool in prediction of the package response to environment during the pre-design stage, when the design of packaging scheme and component placement are most flexible. Steady-state or transient heat transfer analysis can help to establish thermal models and extract useful results for thermal management consideration. Thermal stress analysis and creep analysis, on the other hand, can give insight into the stress concentration that occurs due to the fabrication process and thermal loading, and can help to estimate the fatigue life of plastic deformation-involved structures.

1.3.3 Thesis Outline

This thesis includes primarily three parts: the methodology; thermal modeling and analysis, and thermo-mechanical modeling and analysis. Finite element modeling will be conducted to evaluate two packaging structures: the MPIPPS and the conventional wire bonding Technology. 3-D FEM meshes were built and various boundary conditions were applied. The resultant temperature distribution was used to serve as the thermal load during power module operation. Thermal stresses, inelastic response and material creep were given focus in this study. Thermal cycle-induced deformation of solder was also studied, which will lead to an estimate of fatigue life at some specific critical locations.

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