Chapter III Thermal Characteristics of the Wire bond module vs. the MPIPPS Module

3.1 Outline

To compare the two different packaging techniques a wire bond module and a single-side-cooled MPIPPS module are modeled and the results are compared. After that, the double-side-cooling capability of the MPIPPS module is evaluated using uniform equivalent convective transfer coefficient. The post height effect is also studied.

3.2 Thermal Modeling and Results of Wire Bond Model

3.2.1 3D FEM Mesh

The wire bond thermal model, shown in Figure III-1, includes a total of 71,437 elements and 27,126 nodes.

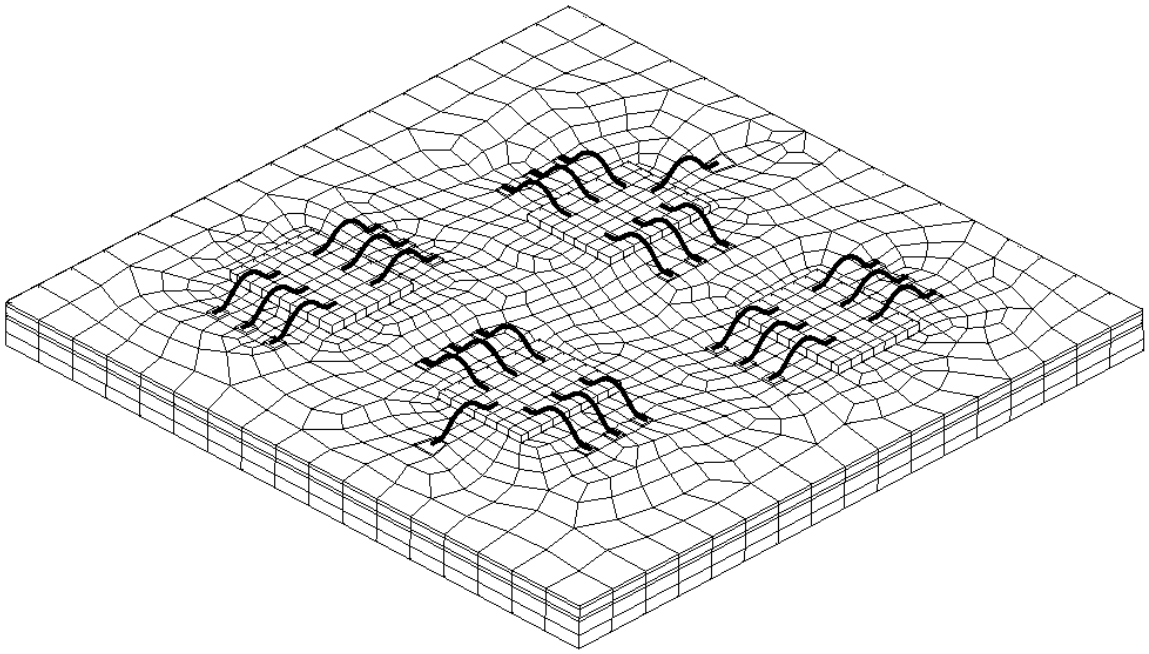

Figure III-1 FEM Model of the Wire Bond Module

A detailed wire bond model structure of the IGBT chip with wire bonds is shown in Figure III-2.

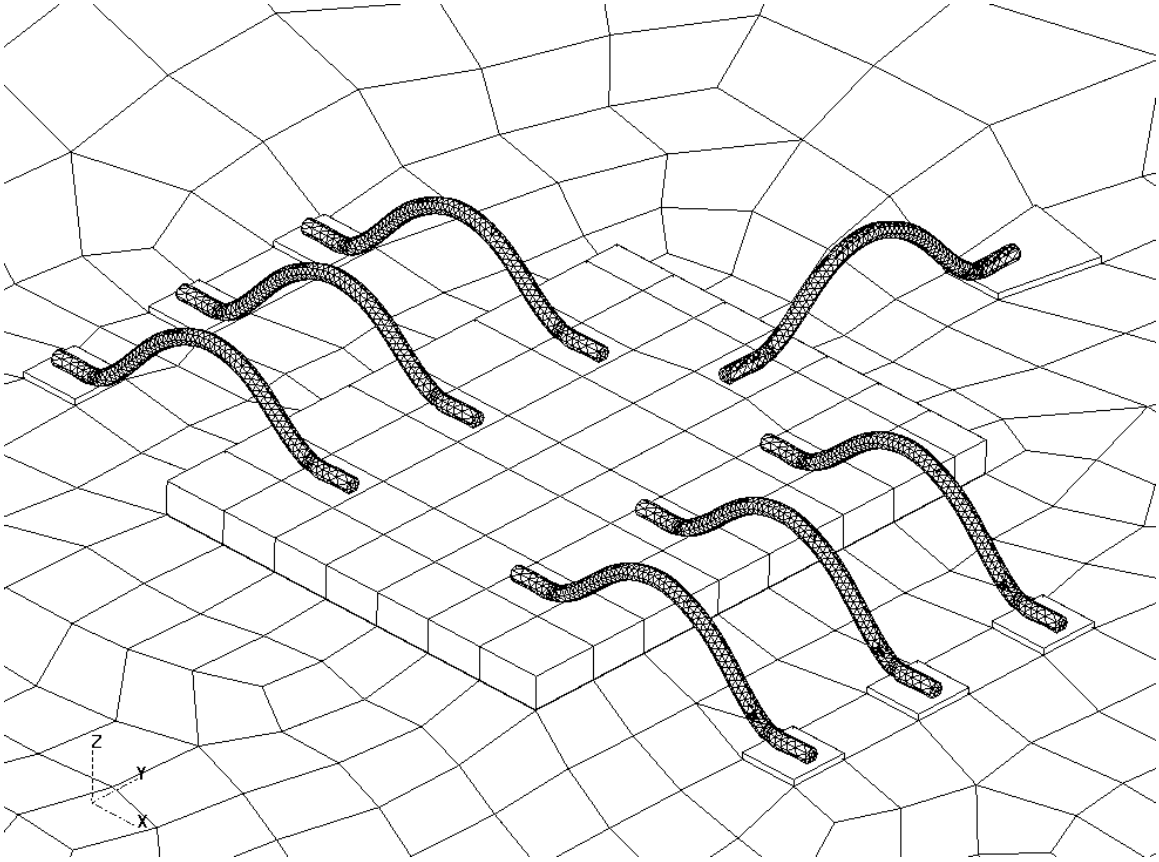

Figure III-2 Close-up View of Wire Bond Model

In order to keep the geometry of the aluminum wire bonds, tetragonal elements are used. The edge lengths for these elements are kept very short compared with the other components in the module. Consequently, care must be taken to avoid boundary discontinuity. Thermal gap elements are used to interface two different materials to realize heat conduction between them. These elements have a Gap Conductance of 1.0×10^9 W/m K, which is normally used in FEM analysis to characterize a defect-free, conductive interface between two solids.

In the wire bond model, the diameter of the aluminum wires is assumed to be 0.2mm (8mils). Length of the wires is approximately 2mm. Other dimensions, such as substrate size, solder thickness and device dimensions, are listed in Table III-1.

Table III-1 Some Important Dimensions in the Wire Bond Thermal Model

Diode (mm)	IGBT (mm)	DBC (mm)	Heat spreader (mm)	Die attach solder layer (mm)
7.0×9.0×0.508	7.0×9.0×0.508	50×50×1.143; Cu/AlN/Cu=10mil/25 mil/10mil	50×50×2	0.075 (3mil)

3.2.2 Temperature Distribution in the Wire Bond Model

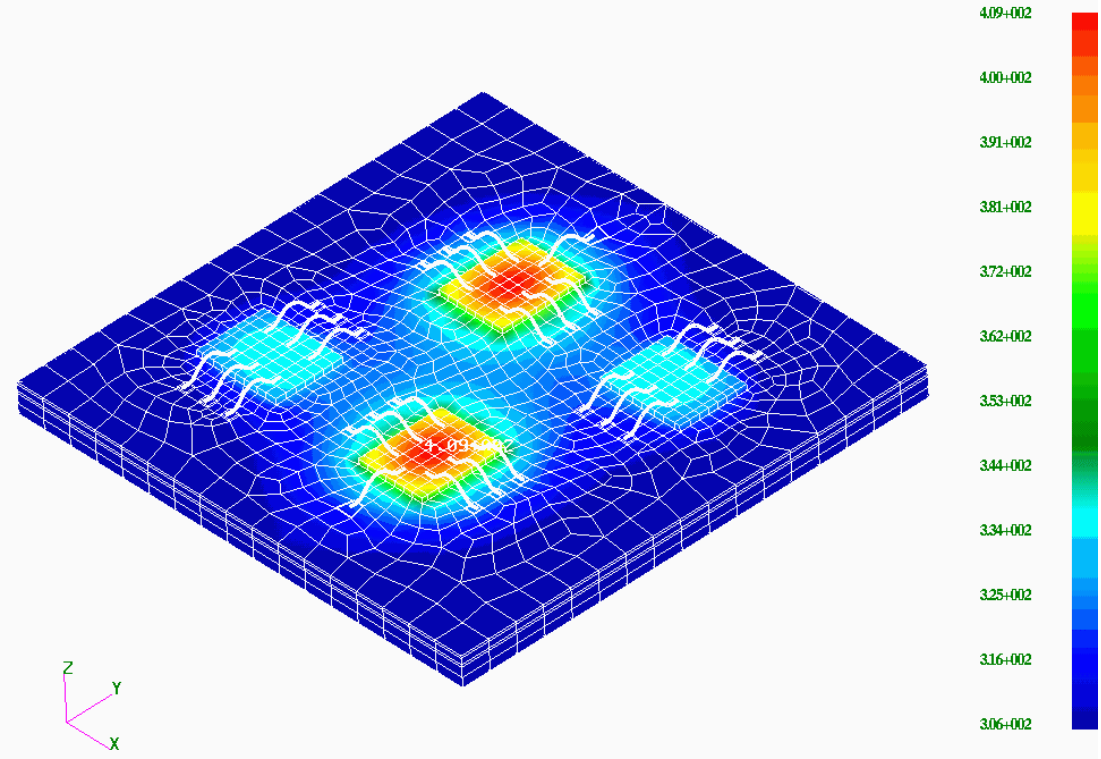

Figure III-3 Temperature Distribution in Wire Bond Model

Steady state heat transfer analysis is performed to give temperature and heat flux results. The temperature distribution of the wire bond model is shown in Figure III-3. The maximum temperature in the model is 136 ^{o}C, which is located in the IGBT chips. Diodes are much cooler than the IGBT chips, with an average temperature of 60 ^{o}C. The edge of the model has the lowest temperature at 33 ^{o}C.

3.3 MPIPPS Module Thermal Modeling

3.3.1 3D FEM Mesh

The MPIPPS thermal model with 1.27mm (50 mil) post height and the wire bonding thermal model are shown in Figure III-4. For clarity, the topside DBC in MPIPPS model is not shown. In MPIPPS model, there are 10,388 elements and 13,204 nodes in total.

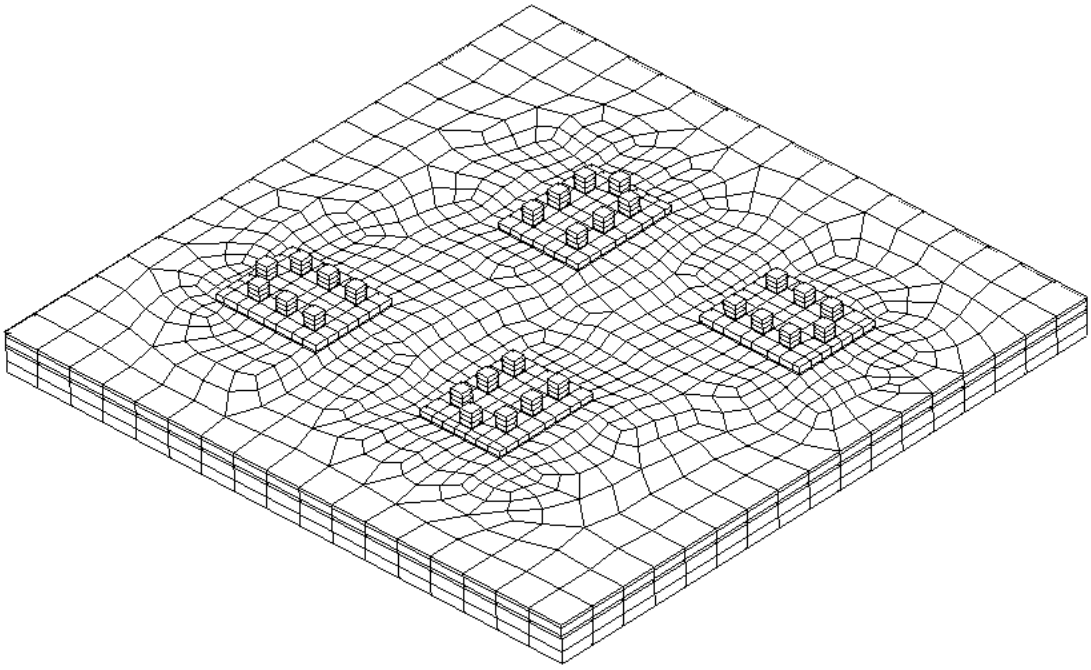

Figure III-4 FEM Model of MPIPPS Module

A detailed MPIPPS structure of the IGBT chip with posts is shown in Figure III-5.

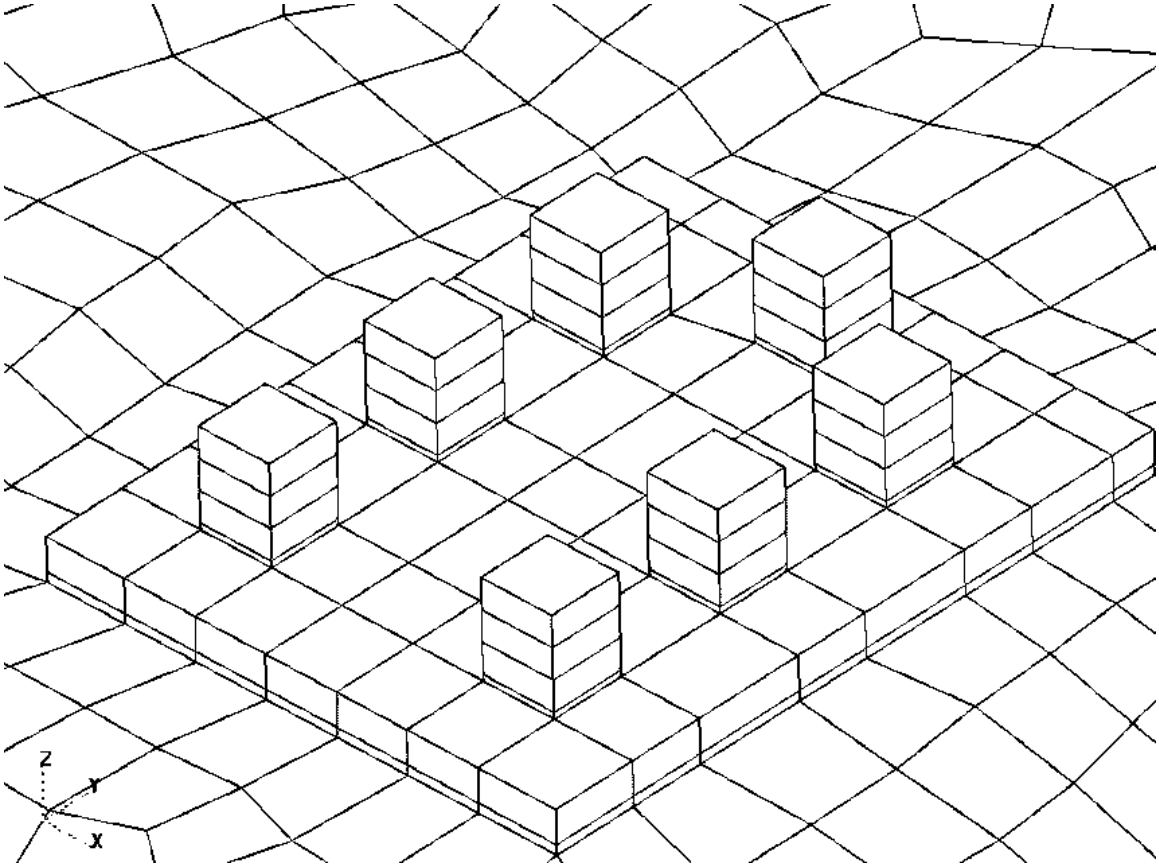

Figure III-5 Close-up View of the MPIPPS Model

The MPIPPS model dimensions are listed in Table III-2. The bottom substrate, the device and the device-to-DBC solder layer dimensions are identical as those of the wire bond model.

Table III-2 Some Important Dimensions in MPIPPS Thermal Model

Post height (mm)	IGBT (mm)	Diode (mm)	DBC (mm)	Heat spreader (mm)	Die attach solder layer (mm)	Post-attach solder layer(mm)
2.54 (100mil)	7.0×9.0×0.432	7.0×9.0×0.508	50×50×1.143; Cu/AlN/Cu=10mil/25mil/10 mil	50×50×2	0.075 (3mil)	0.05 (2mil)
1.27 (50mil)						

3.3.2 Temperature Distribution in the MPIPPS Model

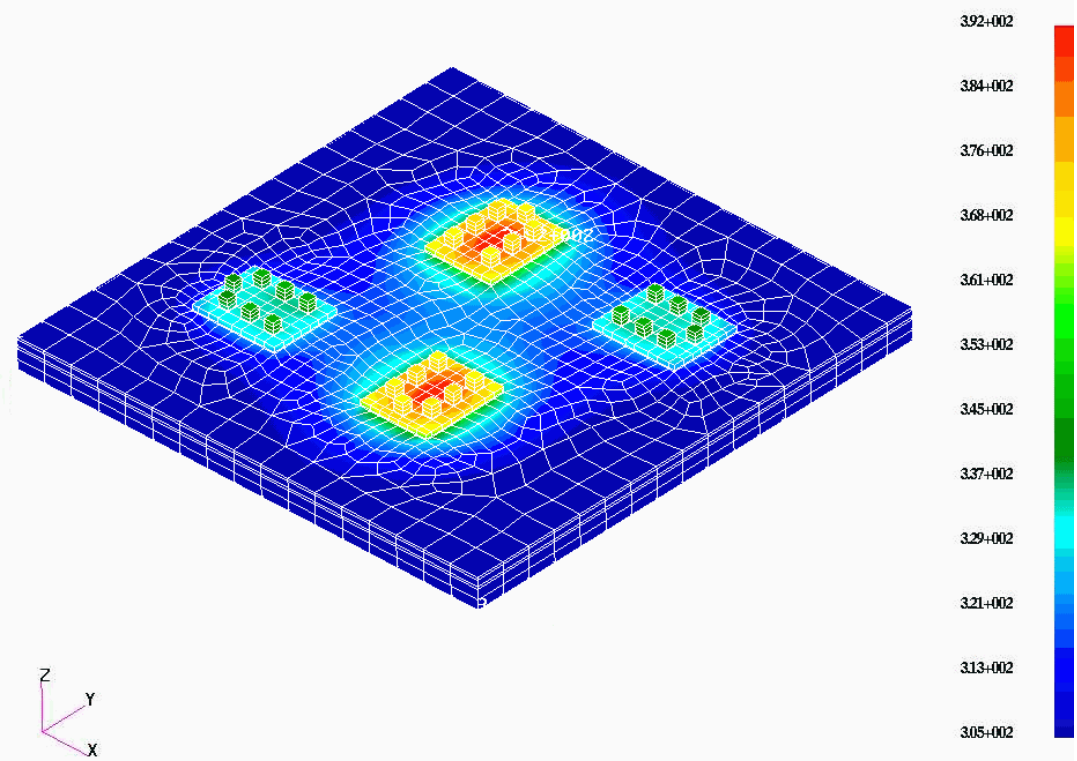

Figure III-6 Temperature Distribution in the MPIPPS Model

Steady state heat transfer analysis is performed to give temperature and heat flux results. The temperature distribution of the MPIPPS model is shown in Figure III-6. The maximum temperature in the model is 119 ^{o}C, which is reached in the IGBT chips. Diodes have an average temperature of 60 ^{o}C. The edge of the model has a temperature of 32 ^{o}C.

3.4 Discussion

3.4.1 Comparison of Heat Transfer in the Wire Bond Module and the MPIPPS Module

For both modules, as mentioned earlier, a uniform bottom boundary condition value of 20,000 W/^{o}Cm^{2} (equivalent to heat sink thermal resistance of 0.02 ^{o}C/W) is used; and the topside of each module is assigned a heat transfer coefficient value of 1 W/^{o}Cm^{2}.

The comparison of temperature distribution of the wire bond and MPIPPS models (Figure III-7) shows the difference between the maximum junction temperatures of these two models.

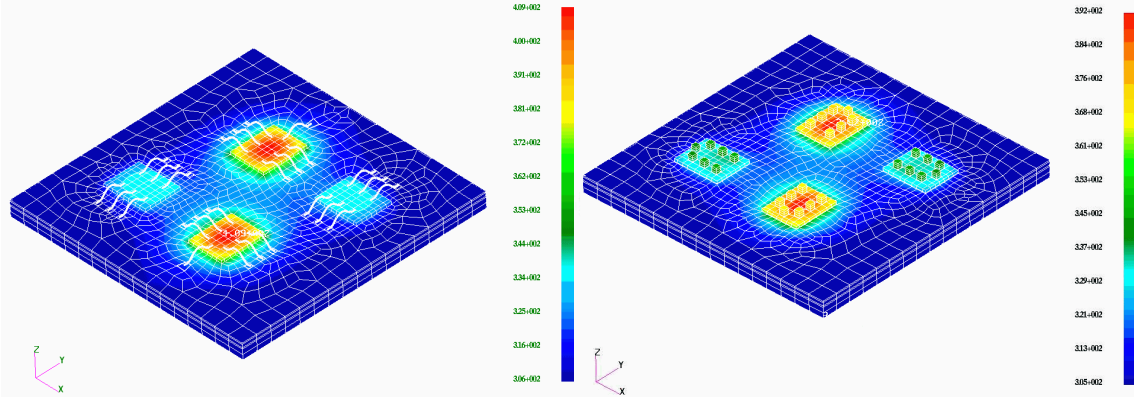

Figure III-7 Comparison of Temperature Distribution Between the Wire Bond Model and the MPIPPS Model

The maximum junction temperature in the wire bond module is 409 K (136 ^{o}C) which is 17 ^{o}C higher than that of the MPIPPS module. While the maximum temperature of the IGBT is different in these two models, the diode temperatures are similar. The temperature distribution is more uniform in the MPIPPS model than it is in the wire bond model. It is interesting to note that in both cases the thermal interfaces from the chip to the heat spreader and the boundary conditions are the same.

The reason for this seeming anomaly lies in the stacked-plate structure. With the heat sink attached to the bottom of the heat spreader, the top DBC also improves the thermal performance of the module. Since the heat dissipation of the IGBT chip is three times that of the diode chip, in the current cooling configuration, heat also takes the path from the IGBT chips to the top DBC through copper posts, then flows back down to the diode chips through copper posts. This is the reason that while the IGBT temperature in the wire bond module is 17^{o}C higher than that in MPIPPS module, the diode temperature is about the same as that of the MPIPPS module. In other words, cooling the stacked-plate structure power module is more efficient since the heat flow reduces the heat crowding at the IGBT region by redirecting the excessive heat to the diode chips.

To more clearly demonstrate this point, Figure III-8 and Figure III-9 show the local heat flux vector plot for the two models. Wire bonds make only a minimum contribution to the heat flow because they only deliver the heat to the area adjacent to the chips.

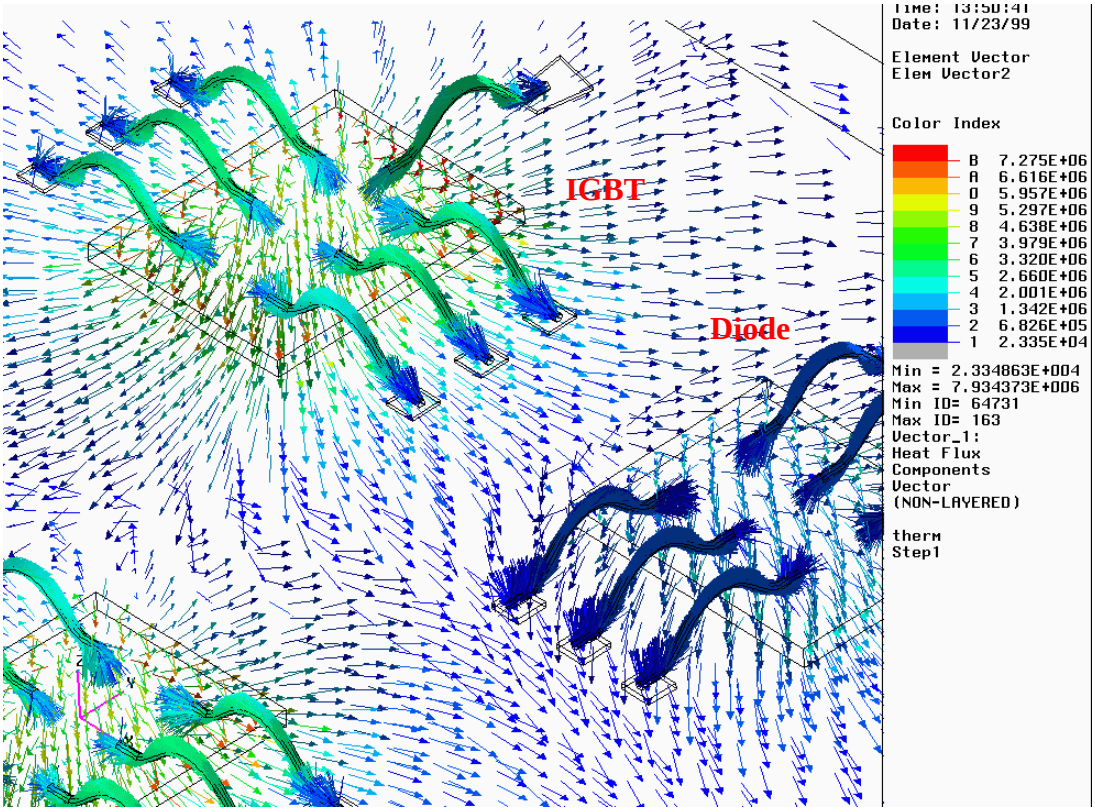

Figure III-8 Heat Flux Vector Plot in Wire Bond Model

While the copper posts help distribute heat flow more uniformly through the top heat flow path (Figure III-9).

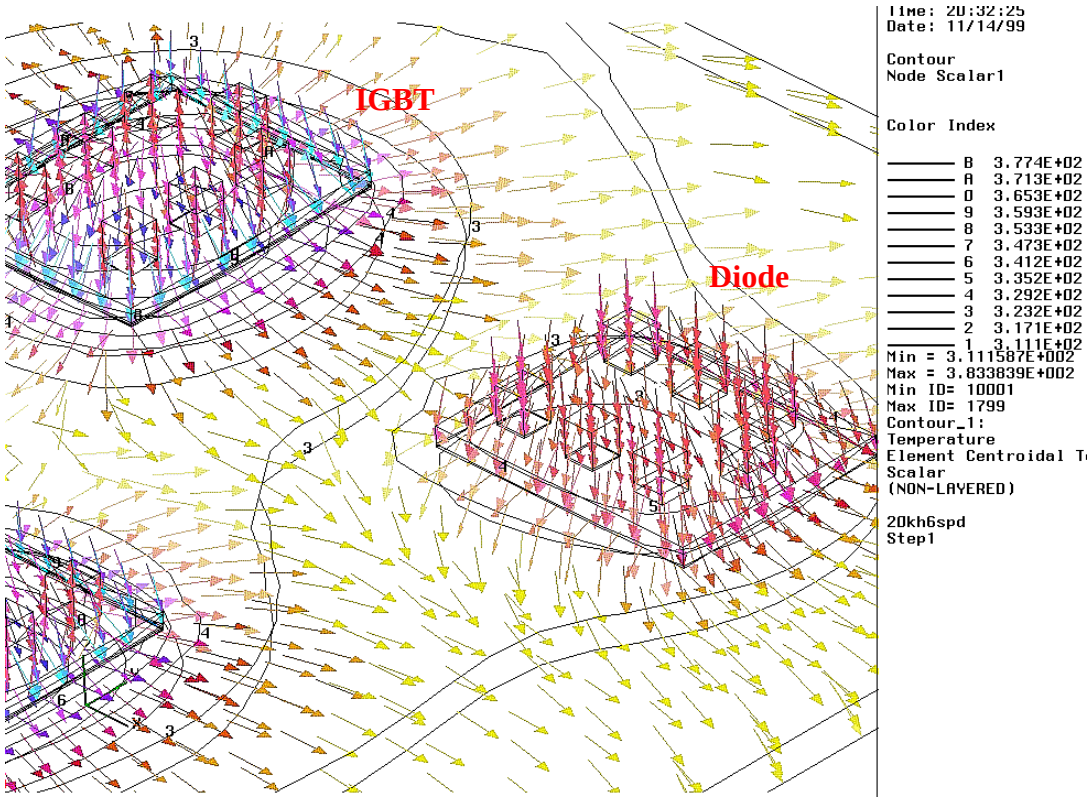

Figure III-9 Heat Flux Vector Plot in MPIPPS Model

The maximum heat flux in the wire bond model is 748 W/m^2, which is crowded around the IGBT device-to-DBC region. In the MPIPPS model, however, this value is reduced to 540 W/m^2.

With single side cooling of the MPIPPS module, there is only downward heat flow in diode posts, while in the IGBT posts, the heat flows upward. In the wire bond module, the heat flow is always in a single direction: from the chip-wire bonding interface to the wire-DBC bonding interface.

3.4.2 Double-sided Cooling vs. Single-sided Cooling for the MPIPPS Module

The stacked-plate structure has an added advantage over the conventional power module thermal design. Rather than a downward, single-direction thermal path through the bottom DBC substrate and heat sink, the stacked-plate power module enables double-sided cooling. As shown in the previous section, the top DBC reduces the maximum junction temperature significantly. Extrapolating these results, we have added another

heat sink on top. With an added heat sink (also has a thermal resistance of 0.02 ^{o}C/W) on the top DBC substrate, the case of double-sided cooling for the MPIPPS is modeled, and a significant reduction of junction temperature has been observed (Figure III-10). Maximum chip temperature (108 ^{o}C/381K) is 11 ^{o}C lower than that of the single-side cooled MPIPPS model.

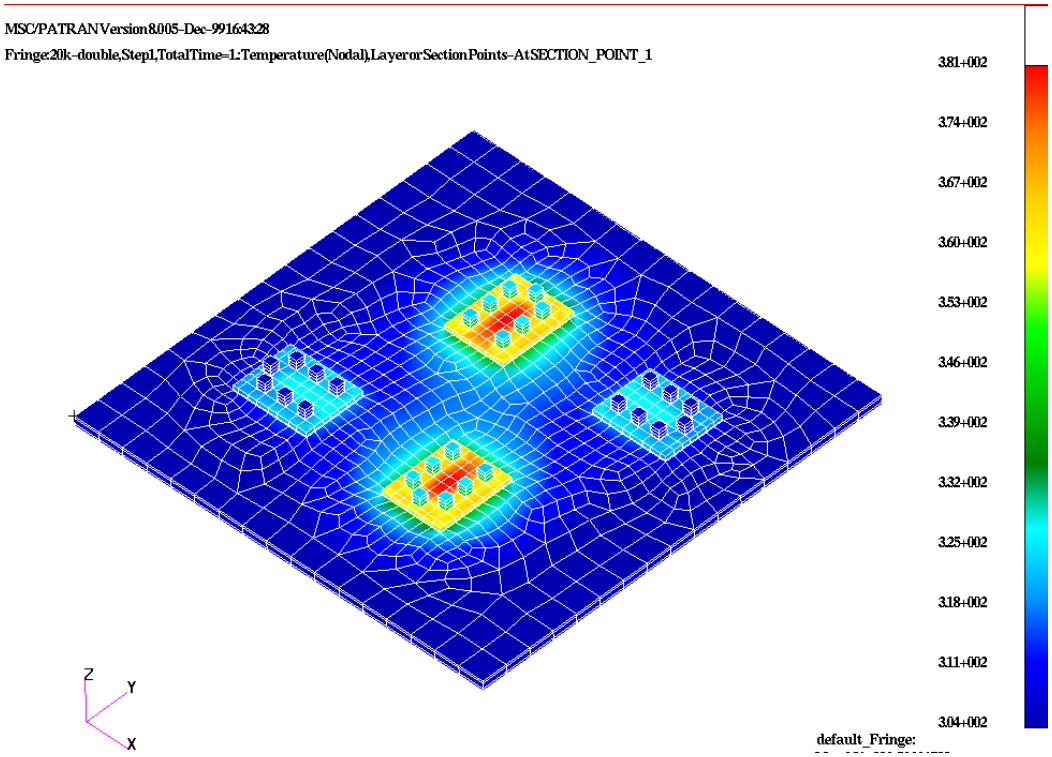

Figure III-10 Temperature Distribution of Double-sided Cooled MPIPPS Model

Figure III-11 shows how an added topside heat sink helps distributed the heat flow.

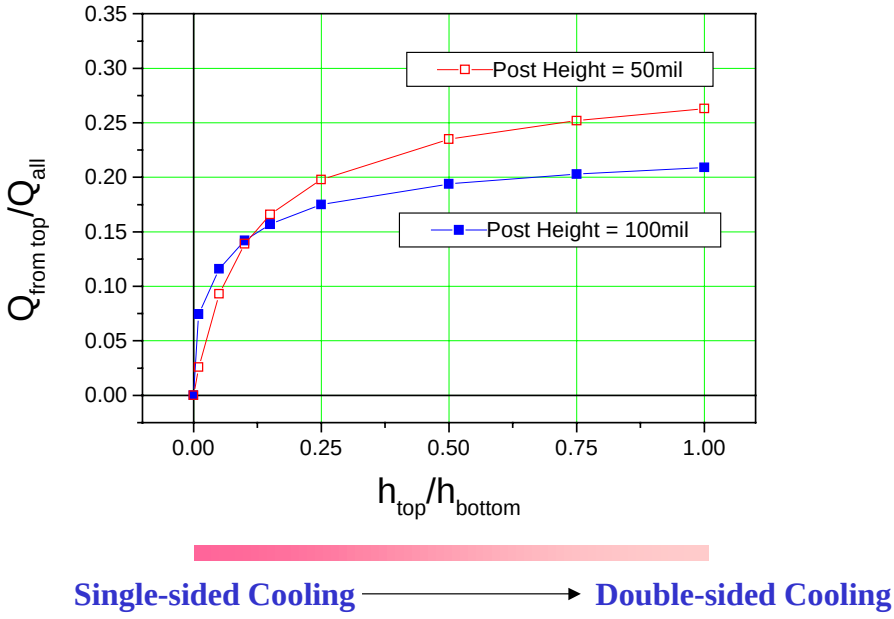

Figure III-11 Double-sided Cooling and Post Height Effects

A series of models have been studied to evaluate the effect of the additional heat sink on top. The modeled thermal resistance for the bottom heat sinks has been kept at 0.05 ^{o}C/W, and the top heat sink thermal resistance ranges from 0.05 ^{o}C/W to 5 ^{o}C/W. The percent of heat dissipated by the top heat sink shows an increasing trend when its thermal resistance approaches that of the bottom heat sink. But the rate of increase in top heat dissipation decreases as the ratio of h_{top}/h_{bottom} approaches unity.

The copper post height effects are also evaluated (Figure III-11). With the copper post (heat removal path) occupying only 10% of the overall heat generation area, 30% of total heat dissipation flows to the top plate. With decreased post height and increased section area of top heat flow path, close to 90% improvement of heat dissipation efficiency is anticipated.

3.5 Conclusion Remarks

Thermal modeling using Finite Element Method is performed on both the conventional wire bond power module and the stacked-plate structured The MPIPPS module. Modeling results have shown a significant improvement in thermal performance

using copper post interconnecting double DBC substrates. In the wire bond module, the heat dissipation path is only on a single side down to the bottom heat sink, so local heating is more severe. On the other hand, regardless of single- or double-sided cooling, heat generated in the MPIPPS module takes advantage of both the top heat flow path and the bottom dissipation path. Compared with the wire bond model, the maximum junction temperature in the MPIPPS module is reduced by 17 ^{o}C, which is due to more uniform temperature distribution and thus more effective cooling from the heat sink. An additional heat sink on top of The MPIPPS module will further lower the junction temperature. The effectiveness depends primarily on the post height and the size of post-device contact area. Shorter, thicker posts will improve the efficiency of double-sided cooling.