Investigation of High Performance AC/DC Front-End Converter with Digital Control for Server Applications

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ABSTRACT

With the development of information technology, the market for power management of telecom and computing equipment keeps increasing. Distributed power systems are widely adopted in the telecom and computing applications for the reason of high performance and high reliability. Recently industry brought out aggressively high efficiency requirements for a wide load range for power management in telecom and computing equipment. High efficiency over a wide load range is now a requirement. On the other hand, power density is still a big challenge for front-end AC/DC converters. For DPS systems, front-end AC/DC converters are under the pressure of continuous increasing power density requirement. Although increasing switching frequency can dramatically reduce the passive component size, its effectiveness is limited by the converter efficiency and thermal management. Technologies to further increase the power density without compromising the efficiency need to be studied.

The industry today is also at the beginning of transferring their design from analog control to full digital control strategy. Although issues are still exist, reducing components count, reducing the development cycle time, increasing the reliability, enhancing the circuit noise immunity and reducing the cost, all of these benefits indicate a great potential of the digital control.

This thesis is focusing on how to improve the efficiency and power density by taking the advantages of the digital control.

A novel π/2 phase shift two Channel interleaving PFC is developed to shrink the EMI filter size while maintain a good efficiency. A sophisticated power management strategy that associates with phase shedding and adaptive phase angle control is also discussed to increase the efficient for the entire load range without compromising the EMI filter size. The method of current sampling is proposed for π/2 phase shift two Channel interleaving PFC and multi-channel adaptive phase angle shift PFC is proposed to accurately extract the average total current information. A noise free current sampling strategy is also proposed that adjusting the sampling edge according to duty cycle information.

An isolated ZVS dual boost converter is proposed to be the DC/DC stage of the front-end converter. This PWM converter has similar performance as the LLC resonant converter. It has hold up time extension capability without compromising the normal operation efficiency. It can achieve ZVS for all the switches. The current limit and SR implementation is much easier than LLC. State plane method, which potentially can be extent to other complex topologies, is used to fully study this circuit. All the operation modes are understood through the state plane method. The best operation mode is discovered for the front end applications. Light load efficiency is improved by the proposed pulse skipping method to guarantee the ZVS operation meanwhile reduce the switching frequency. Current limit operation is also proposed to restrict a best operation

mode by fully taking the advantage of digital control that precisely control the circuit under the over current condition.

High efficiency high power density is achieved by new topology, innovative interleaving, and the sophisticated digital control method.

To grandma in heaven

A.Q. Zhu

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Chapter 1. Introduction

1.1 Research Background

With the fast growing information technology, telecom and computer systems become a large market for power supply industry. Moreover, because of the technology development of IC technology, computers and telecom equipments keep increasing their density and functionality. The increasingly functionality results in more power consumption, higher density requires smaller and higher efficiency on the power supplies. Therefore, the power supplies for the telecom and computer applications are required to be more compact and cost effective [1.1][1.2]. To meet these desired features, distributed power system (DPS) is widely adopted.

Instead of using a single bulky power supply to provide the final voltages required by the load, distributed power system distributed the power processing functions among many power processing unites. One typical DPS structure is the intermediate bus structure [1.3][1.4], as shown in Figure 1.1. In this system, the voltages that are needed for loads are generated through two stage approach. In the first stages, many front-end converters are parallel together to generate the intermediated bus voltage, which is normally 48V, or 12V. After that, the following load converters then transfer the intermediate bus voltage into the voltages that load needs.

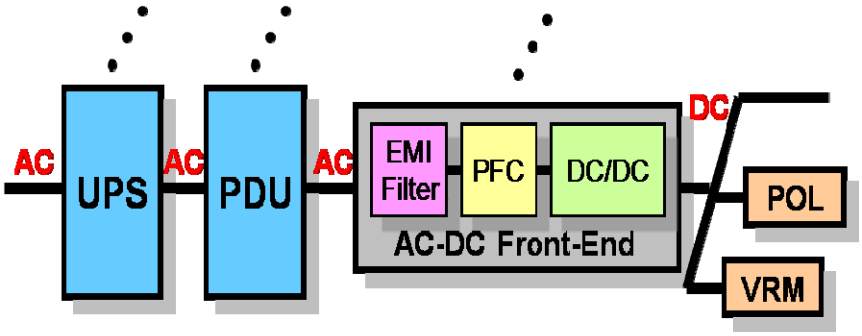

Figure 1-1 Distributed power system

As illustrated in Figure 1.2, which shows the power consumption of a typical large data center, for each Watt consumed by data processing, more than two Watts are wasted in power conversion and cooling. With steadily decreasing prices of datacom equipment, the cost of electricity over the equipment lifetime has become a significant fraction of the initial acquisition cost, especially for low-end equipment such as "blade", 1U, and 2U. As a result of the increasing impact of energy cost on the total cost of ownership, efficiency considerations have started to have a significant influence on equipment acquisition decisions [1.5].

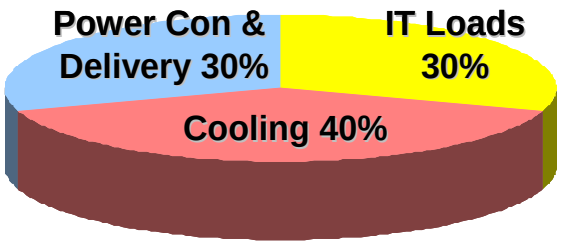

Figure 1-2 Power consumption of a typical large data center

The U.S. Environmental Protection Agency (EPA) announced the first draft of its proposed revision to the ENGERGY STAR specification in February 2005. The draft specification addresses efficiency requirements for lap top, desktop,

workstation and server computers including provisions for maximum allowable power consumption in standby mode sleep mode and idle state, and also proposes a minimum power supply efficiency of 80% for PCs and 75% to 83% for desktop derived servers. Recently, the emphasis of saving energy is further increasing. High efficiency requirement is not only targeting the full load condition but extents to the whole load range. 80 PLUS Initiative[1.6] certifies energy efficient computer power supply units to have more than 80% energy efficiency at 20%, 50% and 100% of rated load. Starting with the 2007 ENERGY STAR[1.7] requirements for desktops laptops, workstations and servers, the Climate Savers Computing Initiative[1.8] brings out a gradually increases the efficiency requirements over the next four years as follow: From July 2007 through June 2008, volume servers must have 85 percent minimum efficiency for the power supply unit (PSU) at 50 percent of rated output (and 81 percent minimum efficiency at 20 percent and 100 percent of rated output), and power factor of at least 0.9 at 100 percent of rated output. From July 2008 through June 2009 the standard increases to 89 percent minimum efficiency for the PSU at 50 percent of rated output (and 85 percent minimum efficiency at 20 percent and 100 percent of rated output). From July 2009 through June 2010, the standard increases to 92 percent minimum efficiency for the PSU at 50 percent of rated output (and 88 percent minimum efficiency at 20 percent and 100 percent of rated output. As a major player in computer server market, Dell specifies a more restrict high efficiency requirements for front-end AC/DC converters to have 75%, 85%, 92%,

94% and 92% separately at 5%, 10%, 20%, 50% and 100% load conditions. The summarized efficiency targets are shown in Figure 1-3.

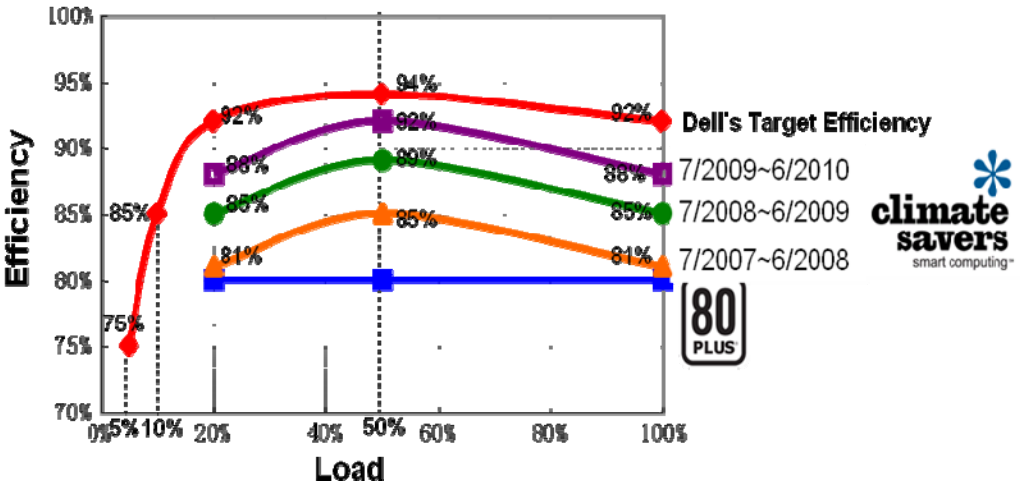

Figure 1-3 Efficiency targets for Front-end AC/DC converter

On the other hand, power density is still a big challenge for front-end AC/DC converters. For DPS systems, front-end AC/DC converters are under the pressure of continuous increasing power density requirement. As shown in Figure 1-4, the power density of front-end converter for server and telecom is continuously increasing [1.9]. At year 2000, the power density is only around 7~8W/in3. However, the power density reaches 20W/in3 at year 2005. And the power density of front-end converter is required to keep increasing.

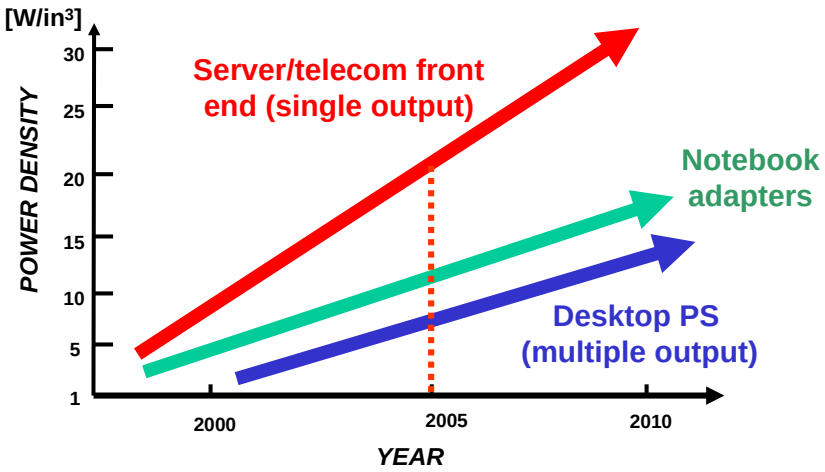

Figure 1-4 Power density trends for front-end AC/DC converters

Although increasing switching frequency can dramatically reduce the passive component size, its effectiveness is limited by the converter efficiency and thermal management. In present industry implementations, the PFC stage switching frequency is typically limited to 75 kHz to 150 kHz range. And DC/DC stage switching frequency is typically limited to 100 kHz to 200 kHz range. As the result, passive components take large portion of converter volume. Figure 1-5 shows a state of art AC/DC front-end converter, Its PFC stage uses single switch continuous conduction mode (CCM) PFC with average current mode control, and DC/DC stage uses phase shift full bridge (PSFB). Because of simple structure and smaller EMI filter size, single switch CCM PFC is wide adopted for power factor correction applications. Meanwhile, PSFB is able to achieve high efficiency with soft switching capability. Thus, it is popular for kilo-watt range power supply

designs. Because these circuit topologies have been existed for many years and they have been well understood and adopted by power supply industries.

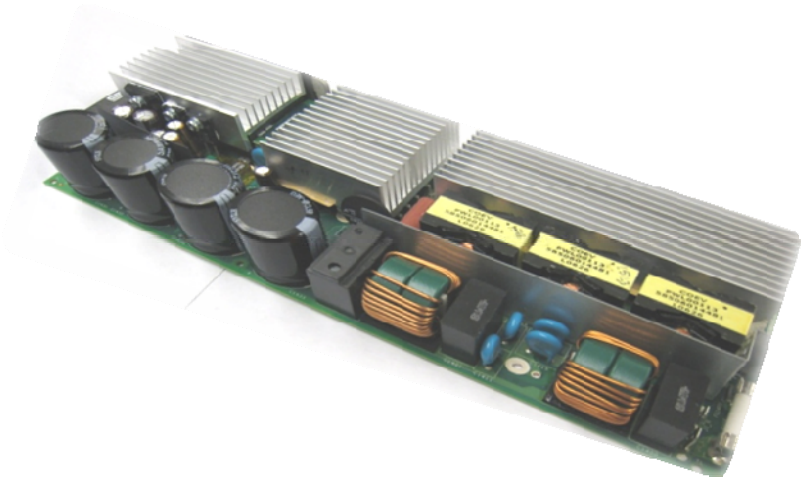

Figure 1-5 1800W front-end AC/DC converter

However, due to several limitations, it is difficult to further increasing the power density of the existing converters. A state of art front-end AC/DC converter is shown in Figure 1-5, although it can reach 18W/in^3 power density, several issues can still be observed [1.9].

PFC inductor and EMI filters takes about one third of the whole converter volume. PFC inductor is used to achieve power factor correction and shape the input current to be sinusoidal. To ensure smaller ripple current, PFC inductor is designed based on the switching frequency. It is desired to have higher switching frequency to achieve smaller PFC inductor size. However, due to the large switching loss caused by PFC stage, it is difficult to increase the switching frequency. Meanwhile, the EMI filter is used to attenuate the EMI noise generated

by the system. Because of stringent EMI standard requirement, large EMI filter is normally used in front-end converters. Since the relationship between EMI filter size and switching frequency is not clear for the industry, most PFC circuits in the real implementation are switching below 150 kHz [1.10].

Due to two-stage approach (PFC+DC/DC), system efficiency is low. Thus, large heat-sinks are required to maintain the thermal handling capability. To achieve higher power density, heat-sink size can be reduced by either improving the system efficiency or improve the system thermal design.

Another large component in front-end converter is the bulky holdup time capacitor. According to the specifications of server systems, front-end AC/DC converters are required to maintain regulated output voltage for more than 20mS when the input AC line is lost. During holdup time, all the energy transferred to the load comes from holdup time capacitor. Therefore, large holdup time capacitors are required to provide the energy during holdup time. Holdup time capacitor requirement is determined by the system power level and the input voltage range of DC/DC converter. Apparently, higher the system power level, more energy is required to transfer to the load. Thus, larger holdup time capacitor is required. On the other hand, wider the DC/DC stage input voltage range, more energy stored in the holdup time capacitor could be used during holdup time. Thus, less holdup time capacitor can be used. However, in the conventional front-end AC/DC converters, DC/DC stage employs PWM converter, and it is difficult

to achieve wide input range together with high efficiency. Therefore, to maintain high system efficiency, large holdup time capacitor has to be used [1.11].

Furthermore, it can be observed that the passive components and the heat sink in the DC/DC also have large size. Similar to the PFC stage, large switching loss prevents DC/DC stage operating at high switching frequency, and need large heat sink to deal with thermal problem [1.12].

The industry today is at the beginning of transferring their design from analog control to full digital control strategy by taking the advantage of reducing components count, reducing the development cycle time, increasing the reliability, enhancing the circuit noise immunity and reducing the cost. TDK announced the full digital control of its innovative EFE series brings a 25 per cent reduction in parts count to achieve a 45 per cent smaller and up to 56 per cent lighter design when compared to similar recently announced competitive products [1.13]. Through digital control, the working environment of the whole system can be better monitored. More sophisticated power management solutions are able to be applied. The operation characteristics can be better optimized by intelligently adjusting according to different conditions thus improves the efficiency. During abnormal situations, having precise control through proprietary algorithms better prevents device overstress, and longer life time of the power supply can be expected. However there is still some issues to be addressed for example the current sampling of multiphase PFC, the impact of digital delay and quantization effect, and etc.

1.2 Thesis outline

This thesis contains 4 chapters.

Chapter one gives an introduction to Front-end DC/DC converters in Distributed Power Systems that are widely adopted in telecom and computing equipment. The challenges and problems with state-of-the-art practice are also discussed.

In chapter two, digital controlled interleaving PFC is discussed as the first stage of the front-end converter. By change the phase shift anger from π/ to π/2 for two phases interleaving PFC, the EMI filter size can be greatly reduced for 75 kHz to 150 kHz switching frequency application. Sophisticated power management solution, phase shedding with adaptive phase anger control, is used to increase the PFC efficient especially at light load while not sacrificing the EMI filter size. Digital control is used to simplify the circuit for complex functionalities. Current sampling strategy for multi-phase interleaving PFC is proposed to accurately fetch the total average current information.

In chapter three, a high frequency isolated ZVS dual boost converter is proposed to be the DC/DC stage of the front-end converter. This PWM converter has a similar performance of LLC resonant converter that has the ability of hold up time extension while the efficiency of normal operation is not compromised. State plane analysis is applied to explore the possible operation modes of the proposed topology and through comparison. The best operation mode is decided

for front-end DC/DC application. Light load operation is proposed to improvement the light load efficiency by maintaining the ZVS operation and meanwhile decreasing the switching frequency. Current limit operation is also proposed to keep the most efficient operation mode through a large range of the load resistance. All the implementation of the complex power management solution is through a TMS320F2808 DSP. High efficiency and high power density is achieved.

In chapter four, a summary related to this topic is discussed. Since the phase shedding with adaptive phase angle control need at least two phases to guarantee a small EMI filter size, a burst mode operation of PFC is propose as the future work to further increase the efficiency of PFC during the light load.

Chapter 2. Digital Controlled Interleaving PFC

2.1 Introduction

The continuously increasing efficiency and power density requirement of the AC/DC front-end converter posed a big challenge for today's power factor correction (PFC) circuit design. The multi-channel interleaved PFC as shown in Figure 2-1 is a promising candidate to achieve the goals. By staggering the channels at uniform intervals, multi-channel interleaved PFC can reduce the input current ripple significantly due to the ripple cancellation effect. Smaller input current ripple indicates low Differential Mode (DM) noise. It is generally believed that the reduced DM EMI noise magnitude will make the DM filter smaller.

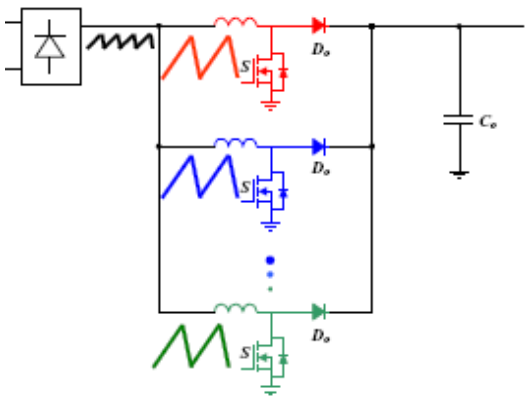

Figure 2-1 circuit diagram of multi-channel interleaved PFC

Multi-channel interleaving PFC has been studied by a lot of researchers in the past. The challenges of implementing the interleaving control has been well studied and analyzed [2.1]-[2.4], and several approaches have been proposed.

There are also studies tried to quantify the input current ripple reduction by interleaving technique [2.5] [2.6] [2.7]. A general method for analyzing interleaved converters to predict ripple amplitudes has be has been proposed for both CCM and DCM[2.7], and was demonstrated with 8- channel interleaving DCM PFC operating at 25 kHz. The EMI filter size reduction was verified by prototype. The high frequency input RMS current reduction by interleaving is also analyzed and quantified [2.7], and used to predict the EMI noise reduction.

2.2 Novel π/2 phase shift 2 phase interleaving PFC

75 kHz ~ 150 kHz is a quite popular switching frequency range for PFC circuit used by today's industry products. Paralleling two MOSFETs to handle the large current is a common practice for a kilo watt power rating PFC, so it is very likely to take this 2¬channel interleaving PFC solution running in this popular switching frequency range. Unfortunately, by using the conventional interleaving scheme, there will be no benefit on the EMI filter at all. 130 kHz switching frequency is one example of the 2-channel interleaved PFC that cannot benefit the EMI filter. Figure 6 (a) shows the measured DM noise of a non-interleaved PFC running at 130 kHz, a switching frequency used by some industry products today. The measured DM noise of a 2-channel interleaved PFC running at 130 kHz is shown in Figure 6 (b). Since the EMI standard starts the regulation from 150 kHz. For both the non-interleaving and the interleaving, the EMI filter is designed based the 260 kHz noise peak. If we compare 260 kHz noise peak, they have

exactly the same magnitude. So the EMI filter will be the same. There will be no benefit on the EMI filter at all. In this case, the interleaving does reduce the ripple current if we check the time domain input current waveform. However, the two ripple currents being compared are at not at the same frequency. Just comparing the ripple current magnitude is not enough to estimate the impact on the EMI filter.

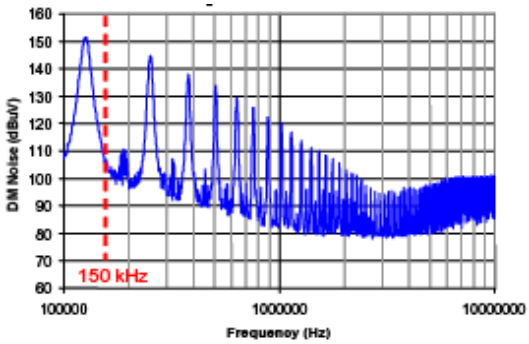

Figure 2-2 measured DM noise of a non-interleaved PFC running at 130 kHz

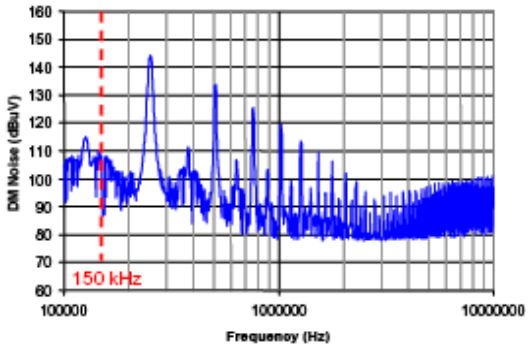

Figure 2-3 measured DM noise of a 2-channel interleaved PFC running at 130 kHz

However, in accordance with the basic principles of harmonics cancellation analysis, other phase shift angles between the PFC channels can provide cancellation or partial cancellation effects can provide benefits in regards to EMI

filter design for reduction of size and cost [2.8]. In this switching frequency range, a two-channel PFC operating with aπ/2 or 3π/2 phase shift can cancel the second order harmonic and reduce the third order harmonic, allowing the EMI filter to be designed based on the reduced third order harmonic noise; so that the filter size can be substantially reduced.

With the proposed π/2 phase shift for 2-channel PFC, the fundamental frequency component noise sources have π/2 phase shift, so the first order noise magnitude will be reduced 3dB. For the 2nd order harmonic, the noise sources are out of phase, so it gets cancelled. For the 3rd order harmonic, the noise sources has 3 π /2 phase shift, so again the magnitude will be reduced 3dB. For the 4th order harmonic, the noise sources are in phase, so they add together. The 4th order will keep the same magnitude as the non-interleaved PFC. The higher order harmonics will repeat in this pattern as shown in Figure 2-4. In summary, all the odd order harmonics reduced 3dB; the 2nd, 6th, 10th, 14th… order harmonics get cancelled; no impact on the 4th, 8th, 12th… order harmonic.

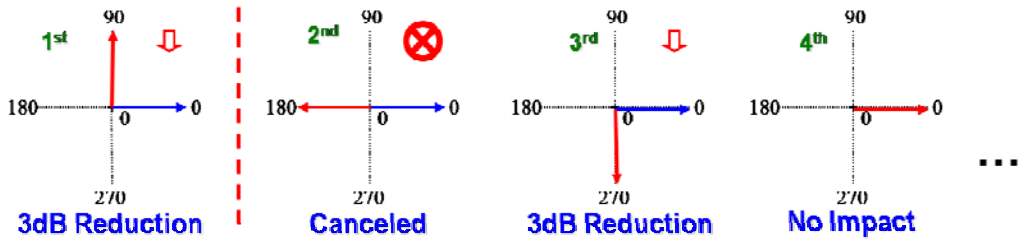

Figure 2-4 noise vector diagram

This π/2 phase shift 2-channel interleaving scheme is experimentally verified on a 2-channel PFC prototype. The measured DM noise for π/2 phase shift two-channel PFC is illustrated in Figure 2-5.

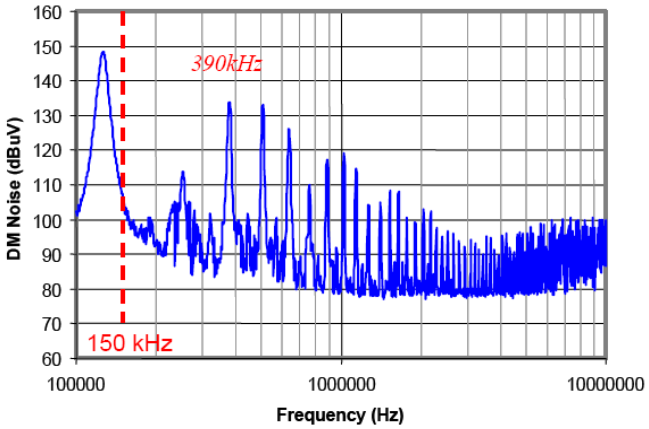

Figure 2-5 measured DM noise of a π/2 phase shift 2-channel interleaved PFC running at 130 kHz

For the DM noise, the 2nd order harmonic gets cancelled. The 3rd order harmonic reduced 3 dB, which is 10 dBuV lower than the original 2nd order harmonic. For the 2¬channel PFC withπ/2 phase shift, the DM filter is designed based the higher frequency noise with smaller magnitude, so the DM filter size will be smaller.

For the CM noise, the noise cancellation phenomenon is the same. The 2nd order harmonic also gets cancelled. The 3rd order harmonic reduced 3dB. The CM filter also can be reduced, as shown in Figure 2-6.

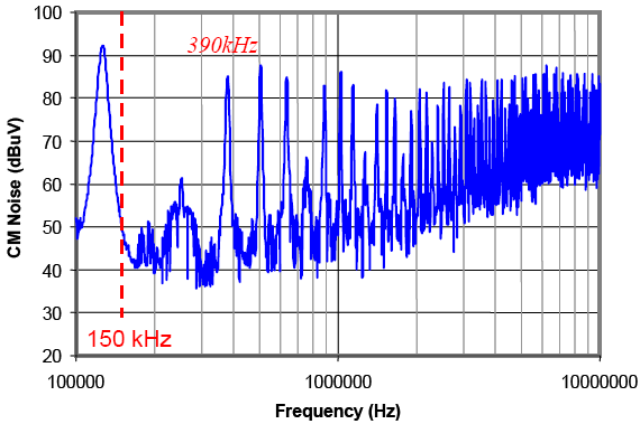

Figure 2-6 measured CM noise of a π/2 phase shift 2-channel interleaved PFC running at 130 kHz

The DM filter corner frequency for non-interleaving (1-Channel), conventional interleaving (2-Channel phase shift π) and the proposed π/2 phase shift are summarized and compared in Figure 3.3. Using the proposed π/2 phase shift scheme, the EMI filter corner frequency can be greatly improved. For a 2-channel PFC with π/2 phase shift, each channel running at 130 kHz switching frequency, the EMI filter size is equivalent to a conventional 2-channel interleaving PFC with 250 kHz switching frequency, and is equivalent to a single channel PFC with more than 600 kHz switching frequency.

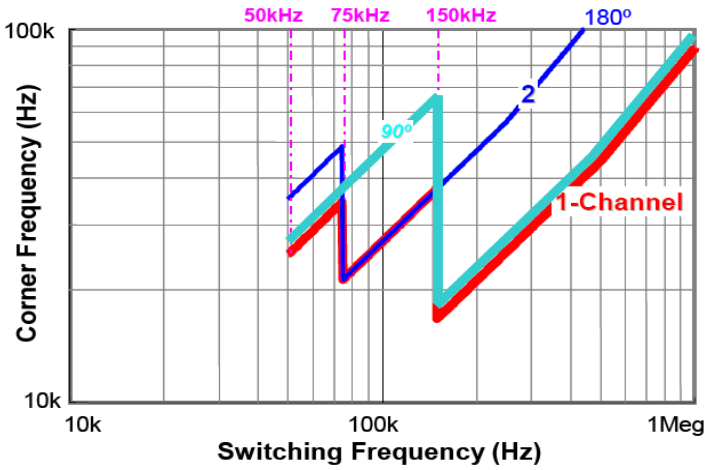

Figure 2-7 Relationship between the filter corner frequency and the switching frequency (DM Filter) for single channel, conventional 2-channel interleaving and 2channel With π/2 degree phase shift

The benefit on the EMI filter of the proposed interleaving scheme is demonstrated by the EMI filter prototype as shown in Figure 2-8 the a total 49% filter size reduction can be achieved by using π/2 phase shift interleaving.

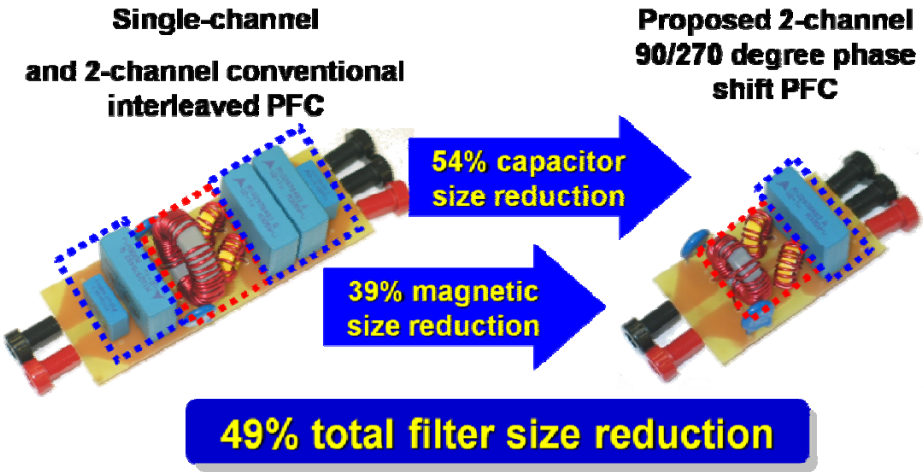

Figure 2-8 EMI filter size reduction

The phase angle control strategy can also be extended to other multi-channel interleaving PFC. The DM filter corner frequency for non-interleaving (1-Channel) and the optimized phase angle control strategy for switching frequency range from 75kHz to 150kHz are summarized and compared in Figure 2-9.

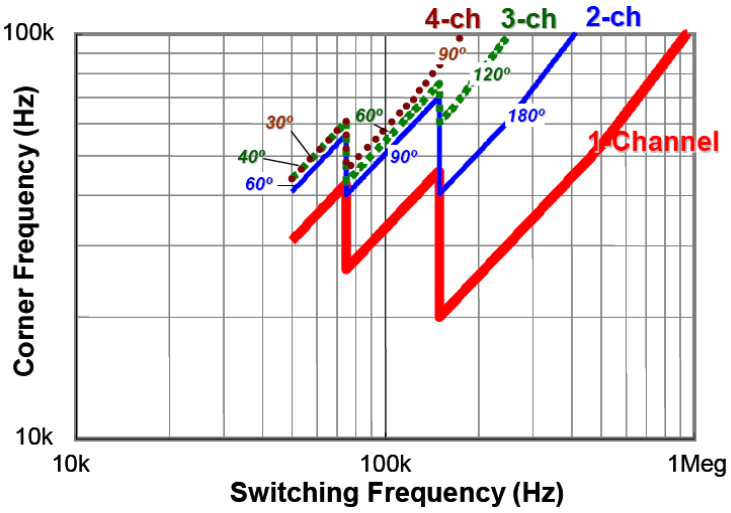

Figure 2-9 DM filter corner frequency v.s. switching frequency for multi-channel PFC with phase angle control

2.3 Power management – phase shedding with adaptive phase angle control

In a multi-channel configuration, it is possible to use phase-shedding to improve the light load efficiency. At heavy load, all channels are active and share the current so that high efficiency can be obtained. When the load becomes light, the power processed by each channel is actually dramatically reduced; if all the channels are still operating, the switching loss, reverse-recovery loss, inductor core loss, etc. still exist in all channels. Reducing the number of active channels

accordingly can result in an efficiency increase at light load [2.9]. Generally, phase-shedding can be used for any power converters with multi-channel configuration to improve the light load efficiency. It has actually already been widely used for the POL applications [2.10]. However, PFC circuit has its own challenges. Reducing the number of active channels can improve the light load efficiency, but it reduces the ripple cancellation effect as well, which will result in the EMI noise increase and losing the benefit on the EMI filter.

By adopting phase angle control strategy, the penalty on the EMI filter design due to the phase shedding can be minimized, as shown in Figure 2-10. At light load condition, two channels are operating with π/2 phase shift to keep both high efficiency and small EMI filter size.

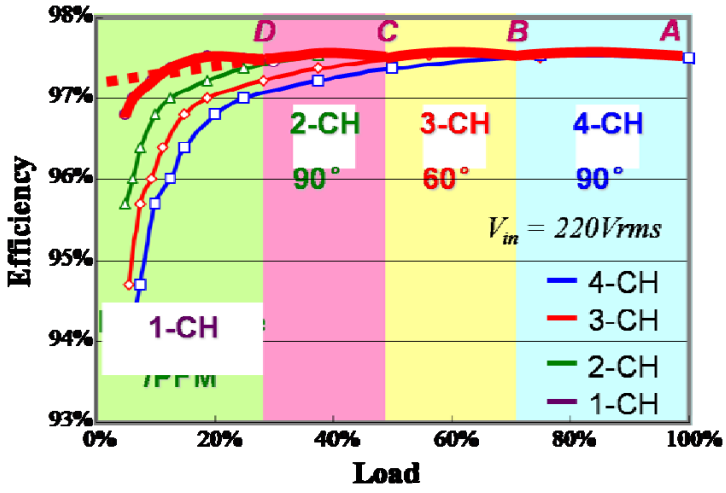

Figure 2-10 power management strategy: phase shedding with adaptive phase angle control

To meet the EMI standard, the filter will be designed based on the worst case, which is the 2-channel π/2 phase shift operation. As can be observed from Figure

2-9, the filter design criterion between 2-channel, 3-channel, and 4-channel operation is only slightly different. Thus, adopting such phase angle control strategy, the light load efficiency can be improved by phase shedding technique without compromising the EMI filter. This method also can be extended to other multi-channel PFC design with different switching frequencies and channel numbers.

Due to the complex power management strategy, implementation through conventional analog chips will increase the circuit complexity, and will be difficult for modification and functionality extension. Instead, TMS320F2808 DSP is used to implement all the functions including PFC and DC/DC, thus the control circuit become very simple. As shown in Figure 2-11. The whole prototype is also become more compact compare to previously analog board as.

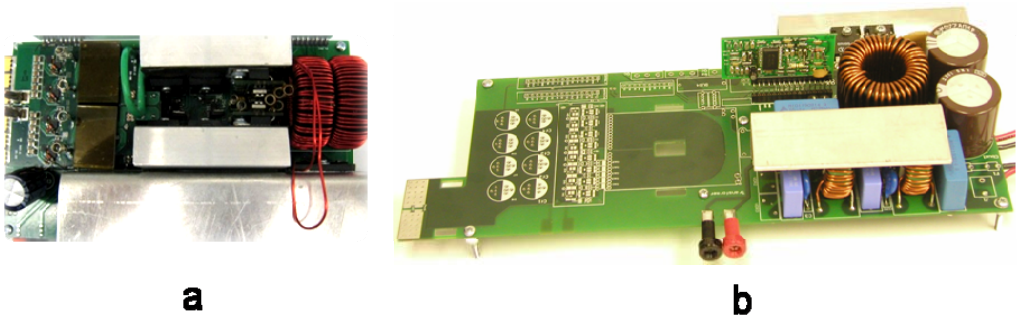

Figure 2-11 prototype comparison: a) digital prototype with π/2 phase shift two phase interleaving PFC. b) analog prototype with one phase PFC

2.4 Total current sampling strategy

Average current control is normally used for the current loop of boost type PFC circuits in nowadays industry products. For analog implementation, the inductor current can be sensed and due to the low bandwidth of current control loop, average current can be automatically obtained and controlled through the current loop. For digital implementation, the current information is discrete, so the sampled current must represent the average of total current in order to implement the average current control.

For one channel PFC, the average current can be always sampled at the middle point of the turn on period. If double edge is used as the modulation method, the sampling point can be always fixed at the point when the ramp counts to zero as shown in Figure 2-12.

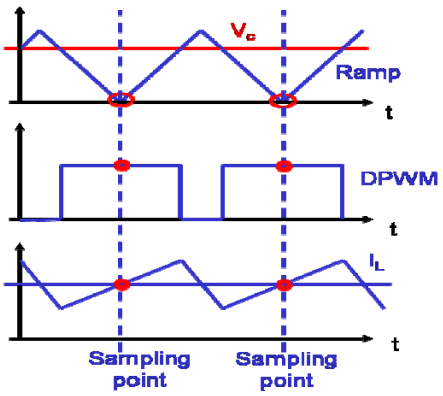

Figure 2-12 Current Sampling Strategy for One Channel PFC

For conventional two phases interleaving PFC, the circuit schematic for total current sensing is shown in Figure 2-13. And the same current sampling point can

be used as of the one channel PFC. As shown in Figure 2-14, the second ramp has a π phase shift to the first ramp. Because the point that the first ramp counts to zero is the middle point of the turn on period of the first phase while is also the middle point of the turn off period of the second phase, the total current sampled at this point can still represent the average value of the total current.

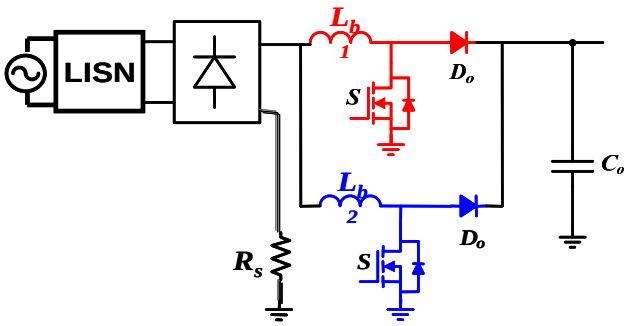

Figure 2-13 total current sensing schematic

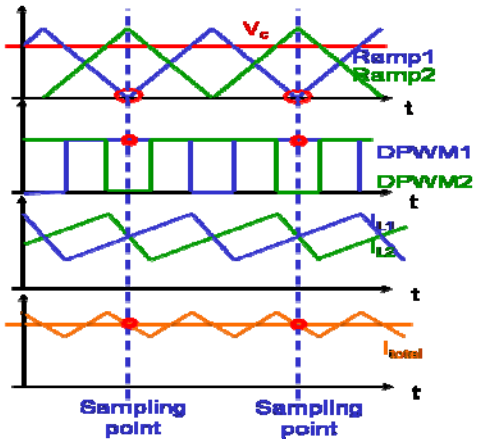

Figure 2-14 Current Sampling Strategy for conventional two Channel interleaving PFC

However, if the same sampling points are applied to the π/2 phase shift PFC, the total average current cannot be obtained. As shown in Figure 2-15, the zero point of ramp1 is the middle point of turn on period of first phase, but is not the

middle point of any period of the second phase, therefore the current sampled at this point cannot represent the average value of the total current. Instead, the current sampled at the middle point of the turn on point of the second channel and the turn off point of the first channel will represent the total average current. To locate this point, the delay between the sampling point and the ramp1 zero point need to be calculated.

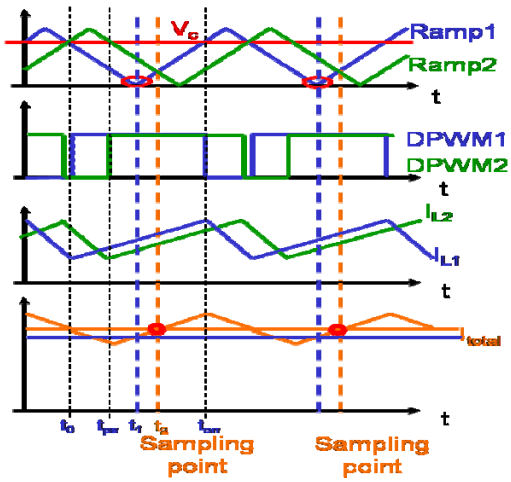

Figure 2-15 Current Sampling Strategy for π/2 phase shift two Channel interleaving PFC

Assume t_0 is the reference point, then t_1 can be written as:

$$t_1 = \frac{t_{on}}{2}$$

And t_2 can be written as:

$$t_2 = \frac{t_{on} - t_{ps}}{2}$$

where the t_{ps} is the phase shift time between the first channel and the second channel.

The delay between the sampling point and the ramp1 zero point then can be calculated:

$$t_2 - t_1 = \frac{t_{ps}}{2}$$

Therefore, the sampling point for π/2 phase shift PFC is $\frac{t_{ps}}{2}$ delay to the first channel zero point.

This sampling method can also be extended to multi-channel adaptive phase shift PFC. for n channel PFC, the current sampled at the middle point of the turn on point of channel 1 and the turn off point of channel n will represent the averaged total current. Same calculation can be used to find out the delay between the sampling point and the zero point of ramp1.

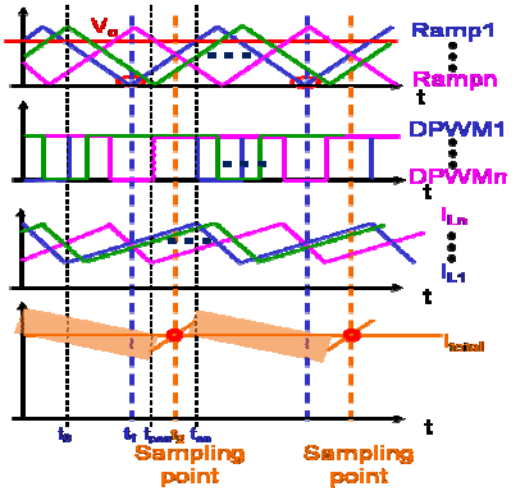

Figure 2-16 Current Sampling Strategy for multi-channel adaptive phase shift PFC

Assume t_0 is the reference point, then t_1 can be written as:

And t_2 can be written as: $t_1 = \frac{t_{on}}{2}$

$$t_2 = \frac{t_{on} - t_{psn}}{2}$$

where the t_{psn} is the phase shift time between channel 1 and channel n.

The delay between the sampling point and the ramp1 zero point then can be calculated:

$$t_2 - t_1 = \frac{t_{psn}}{2}$$

Therefore, the sampling point for any phase shift n channel PFC is $\frac{t_{psn}}{2}$ delay to the first channel zero point.

Another issue associates with digital implementation is the noise problem at the sampling point. As shown in Figure 2-17, the noise happens at the switching points of both channels. The positions of the noise points are determined by the phase shift, duty cycle, and the channel numbers.

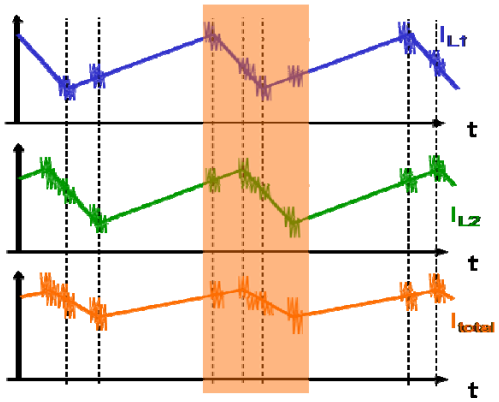

Figure 2-17 noise on the current waveform for π/2 phase shift two Channel interleaving PFC

If the sampling point is happened to be noised, the average current information will never be correctly obtained. Filter might be applied to deal with noise problem. But since the current waveform is triangle, which contains

significant high order of switching harmonics, clearly filter out the noise will destroy the current shape. Sampled current will no longer represent the average total current.

As mentioned the noise positions is related to duty cycle, the noised waveform of π/2 phase shift two Channel interleaving PFC for different duty cycle is studied as shown in Figure 2-18. For D=0.1 and D=0.3, the trailing edge of the total current is noised while the falling edge is noise free. For D=0.7, the falling edge of the total current is noised while the trailing edge is noise free. For D=0.5, both trailing and falling edges are noise free.

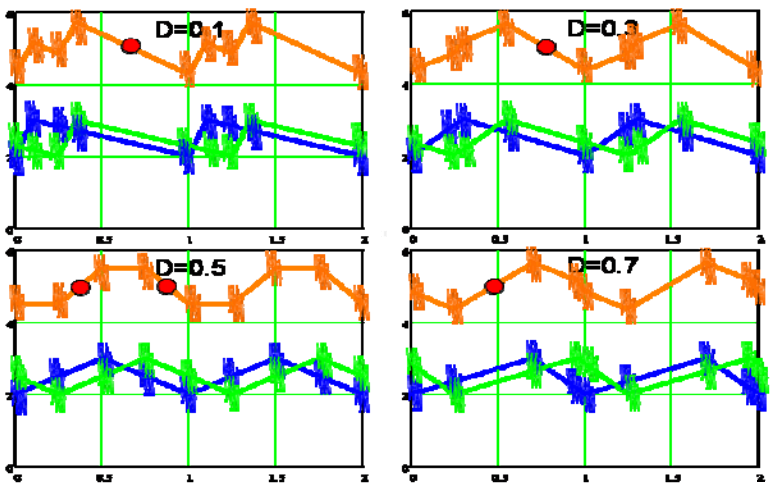

Figure 2-18 the noised waveform of π/2 phase shift two Channel interleaving PFC for different duty cycle

Therefore, a noise free sampling strategy is proposed to adjust the sampling edges according to the duty cycle information. And this method can be extent to

multi-phase PFC. When the PFC is running at low line condition, the duty cycle range is from 1 to 0.565 according to:

$$D_{\min} = 1 - \frac{120 \cdot \sqrt{2}}{390} = 0.565$$

The sampling edge can be stick to the rising edge of the total current.

For high line voltage input, the duty cycle range is from 1 to 0, the sampling point is set to the rising edge when the duty cycle is larger than 0.5; the sampling point is set to the falling edge when the duty cycle is smaller than 0.5. Because the duty cycle value is calculated in every switching cycle, the next sampling point is well determined at the present cycle. The switching of the sampling edge will not cause unstable issue.

2.5 Experiment result

π/2 phase shift two Channel interleaving PFC is implement with digital control as the first AC/DC stage. 130 kHz switching frequency is chosen considering both the efficiency and power density. The prototype is shown in Figure 2-11 (a). Figure 2-19 shows the experiment waveforms with 90 V AC input, 400 V output and running at 1200W power. Figure 2-20 shows the efficiency curve for 90 V input. About 95% peak efficiency can be achieved.

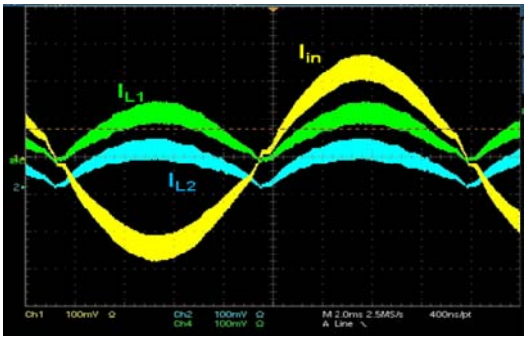

Figure 2-19 experiment waveforms of π/2 phase shift two Channel interleaving PFC

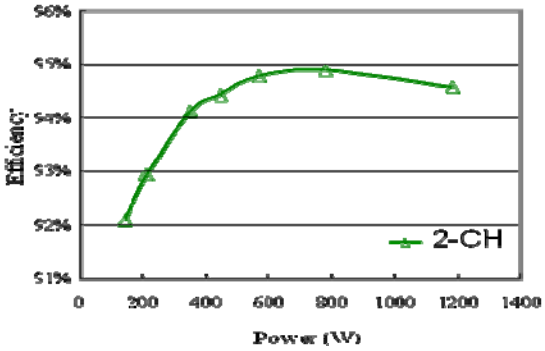

Figure 2-20 measured efficiency curve for π/2 phase shift two Channel interleaving PFC

Chapter 3. Digital Controlled High Frequency Isolated ZVS Dual Boost Converter

3.1 Introduction

With the development of power conversion technology, high efficiency for power management, especially in computer application, becomes the major challenge. The new efficiency targets specify high efficiency for the entire load range. For example, Dell specifies a high efficiency requirement for front-end AC/DC converters to have 75%, 85%, 92%, 94% and 92% separately at 5%, 10%, 20%, 50% and 100% load conditions.

On the other hand, power density is still a big challenge for front-end AC/DC converters. Although increasing switching frequency can dramatically reduce the passive component size, its effectiveness is limited by the converter efficiency and thermal management. In present industry implementations, DC/DC stage switching frequency is typically limited to 100 kHz range. As the result, passive components take large portion of converter volume.

Beside large passive component size, bulky holdup time capacitor becomes the bottleneck for further power density improvement. To ensure the digital system to have enough time to respond to power failure, the front-end converter is required to provide full power output for one AC line cycle which is at least 20ms. With a 1.2kW design, the energy needed to store in the system will be at

least 24 Joule to target the 20ms holdup time requirement. During the holdup time, all the energy is drawn from the bulky capacitor on the 400V DC bus until the allowable minimum input voltage of the DC/DC converter is reached and then the DC/DC stage shuts down and output voltage begins to drop as shown in Figure 3-1

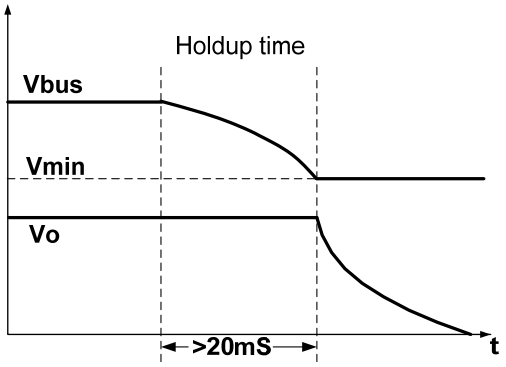

Figure 3-1 holdup time requirement for front-end AC/DC converters

The relationship between the allowable minimum input voltage of the DC/DC converter and the required holdup time capacitor is determined by the following equation:

$$E = \frac{1}{2}C\left(V_{bus}{}^{2} - V_{\min}{}^{2}\right)$$

For PFC stage, the output voltage is always set to 400V to ensure its capability of operates at highest input line. Therefore, to provide the required energy during holdup time, both large C with large $V_{\min}$ and small C with small $V_{\min}$ can meet the requirement. The relationship between the holdup time capacitor requirement and the minimum DC/DC stage input voltage for front-end AC/DC converter at different power levels is illustrated in Figure 3-2.It can be

seen that the holdup time capacitor requirement decreases with reducing DC/DC minimum input voltage. In order to achieve higher power density and lower cost, wide input range DC/DC converter is desired for the front-end AC/DC converters.

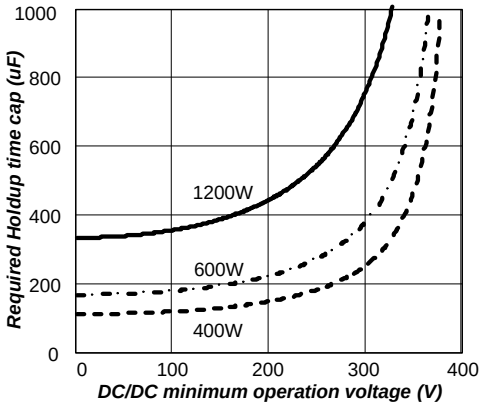

Figure 3-2 Holdup time capacitor vs. minimum DC/DC stage input voltage

However, for conventional PWM converters, it is difficult to achieve both high efficiency and wide operation range simultaneously. For instance, the asymmetrical half bridge converter is desired to operate with 50% duty cycle to achieve the maximum efficiency. But to ensure the holdup requirement with a small bulky capacitor, the converter has to operate in a wide operation range, and during normal operation, duty cycle has to be reduced to realize regulation capability. Thus the efficiency at the normal operation condition has to be compromised. In Figure 3-3, demonstrated a 1 kW, 48V output asymmetrical half bridge (AHB) is able to achieve 94.5% optimal efficiency at 200 kHz switching frequency when it is dedicatedly designed for 400V input and operates with 50% duty cycle. However, to achieve wide operation range from 300V to 400V, duty cycle at 400V input has to be reduced to 30%, which dramatically reduce the

converter efficiency. As shown in Figure 3-3, converter efficiency reduces to 92% when the wide operation range is realized.

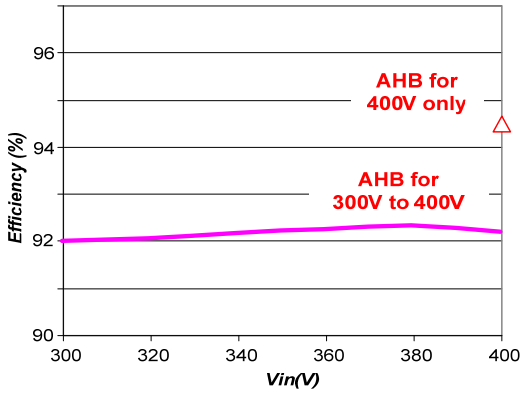

Figure 3-3 Asymmetrical half bridge efficiency

To help DC/DC stage accomplishing both wide operation range and high efficiency, different auxiliary circuit have been implemented [3.1][3.2]. Although these solutions could results in good circuit performance in the aspects of efficiency, due to the complex circuit structure, together with the concern of transient performance and the stability issues, these solutions are difficult to be adopted by industry.

LLC resonant converter becomes an attractive topology for DC/DC Front-end converter because it is able to achieve wide operation range without sacrificing the efficiency in normal operation condition. The LLC resonant converter topology and its gain curve are shown in Figure 3-4.

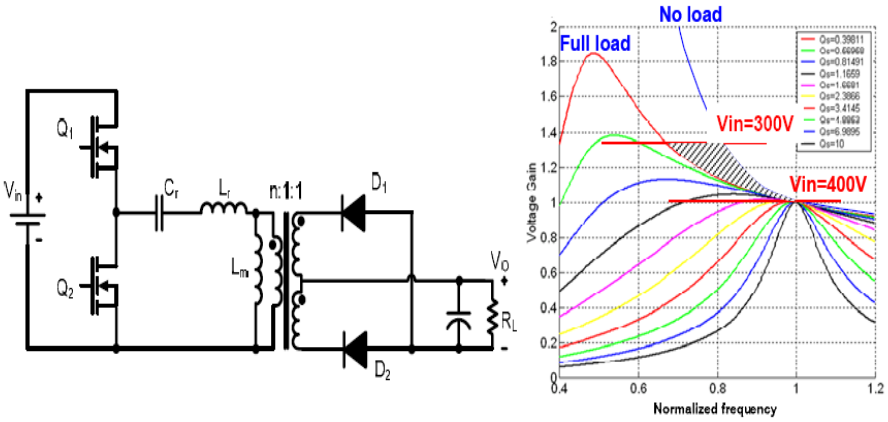

Figure 3-4 Resonant Converter and its gain curve

As illustrated on the gain curve, the LLC resonant converter can achieve both Buck mode and Boost mode operation. During the normal operation, its input is generated by PFC stage. Converter operates at its resonant frequency to minimize the conduction loss and switching loss. When the AC line drops, the energy is purely from the bulky capacitor. So the input voltage of LLC converter keeps decreasing, and switching frequency is reduced to realize Boost mode and keep the output voltage regulated.

Therefore, LLC resonant operate at resonant frequency and achieves maximum efficiency for most of the time. During the holdup time, circuit operates below the resonant frequency, and circuit has lower efficiency, but this condition only lasts for 20mS and will not cause thermal issue for the converter design.

However, to make commercial use of the LLC resonant converter, there are still some issues to be addressed. For example over current protection is one of the critical issues. Normally, there are three methods for over current protection

[3.3]. The first method is increasing the switching frequency when over-current occurs. It's simple, but the frequency becomes too high to keep acceptable current, which results in great losses on devices and brings more critical demand on thermal management. Another concern is that magnetic design will be greatly affected by this high switching frequency. The second method is a combination of varied-frequency control and pulse width modulation (PWM) control. With this method, a lower maximum frequency can be chosen compared to the first method. The PWM control is used to limit the current so that magnetic and semiconductor components don't need to be over designed. However, the primary switches will lose ZVS under over current protection mode. And the speed of mode transition between frequency control and PWM control is also an issue. The third method achieves the current limitation function by modifying the original LLC topology with splitting resonant capacitors and clamping diodes. The current can be automatically limited by clamping the voltage across the splitting resonant capacitors and ZVS of primary switches can still be achieved under current limit operation. The main problem of this method is that the current-limit point is a function of input voltage. While the primary current and voltage across resonant capacitors are larger at low line voltage than they are at high line voltage, the current-limit-point at high line voltage is much higher and loses the meaning of over current protection.

Other than over current protection, additional resonant components, variable switching frequency, and also synchronous rectifier driving are still the big

reasons that the industry companies are so hesitate to use LLC resonant topology in their products for sever and telecom applications.

Instead of using LLC topology, in this chapter, a PWM converter with similar performance as LLC resonant converter is proposed [3.4] for DC/DC Front-end converter. The proposed topology is shown in Figure 3-5, which is constructed by primary full bridge and secondary controlled rectifier, together with an inductor and isolation transformer.

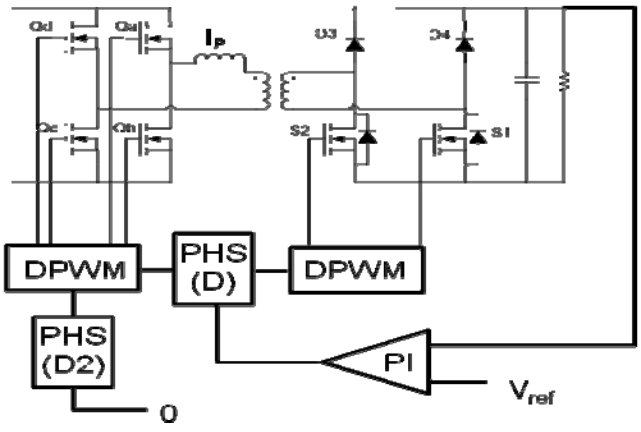

Figure 3-5 proposed isolated ZVS dual boost converter

In the proposed topology, primary side full bridge generates a square wave voltage and complementary 50% duty cycle PWM signals are used to control secondary side switches. By controlling the phase shift between primary side and secondary side voltages, the converter can achieve optimal efficiency at normal operation condition, when AC line exists. Additionally, the circuit has the capability of boost voltage gain, which can help extend the holdup time and reduce bulky capacitor requirement.

The other benefit of this proposed topology is its small switching loss. The primary side is full bridge structure so that ZVS can be achieved for all the four switches during heavy load condition. For the secondary side, the body diode of the bottom switch is always conducted first, so ZVS operation is also guaranteed. Traditional full bridge topologies normally lose ZVS at light load condition. Although the ZVS operation range might be extended, the converter will suffer a high circulating energy at heavy load, which compromised the efficiency at full load condition. This proposed topology operates burst mode during light load condition. Not only the effective switching frequency is reduced, but also maintains enough turn off current to realize ZVS operation for the primary side switches. Combining ZVS operation for all the switches and the burst operation mode during the light load, this proposed topology can achieve a promising high efficiency for the whole load range.

In this chapter, firstly, the proposed isolated ZVS dual boost converter is analyzed based on the normal operation and holdup time operation. Secondly, state plan method is applied to search for all the other possible operation modes. Then, burst mode operation is introduced to improve the light load efficiency. After that, current limit operation and start up method are discussed. Furthermore, this proposed isolated ZVS dual boost converter has been implemented using 260 kHz switching frequency to demonstrate the high frequency, high efficiency operation capability and verify the design process.

3.2 Operation principles of isolated ZVS dual boost converter

As shown in Figure 3-6, Qa and Qc are switching at same time with 0.5 duty cycle. Qb and Qd gate signals are not shown, because they are the same signal and complementary with Qa&Qc gate signals. So the output of full bridge at points ab generates a square wave voltage. The secondary side switches S1 and S2 are also driven by complementary 50% duty cycle PWM signals as shown in Figure 3-8. The phase shift between Qa and S1 is defined as equivalent duty cycle D that

$$D = t_1 / \frac{T_s}{2}$$

D1 is defined as a sub duty cycle where it is from current zero crossing point to S1 turn-on point, which is :

$$D_1 = t_1 - t_0 / \frac{T_s}{2}$$

D1 is used in calculation of voltage gain curve which will be discussed below. The primary current I_P is indicated as $i(\theta)$ because it is a function of phase shift. With such a driving scheme, the proposed topology can achieve both Buck mode and Boost mode operation, which means the voltage gain is lower or higher than 1.

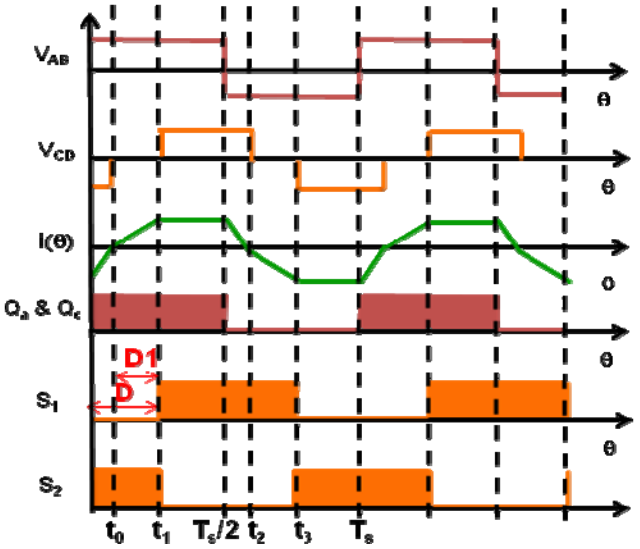

Figure 3-6 Critical waveforms of isolated ZVS dual boost converter

The equivalent circuits for each switching interval are shown in figure 3-9. Between time t0 and t1, Qa&Qb are conducting and inductor current begins to increase from zero. Because the primary side current is positive, body diode of S1 is conducting. Since S2 is still conducting, transformer secondary side is shorted by S1 body diode and S2. Therefore, the inductor is charged by the input voltage. Because body diode of S1 conducts first, S1 can be turned on at t1 with zero voltage switching (ZVS) turn on. At time t1, switch S2 is turned off. Transformer secondary current transfers from S2 to D2 automatically and the inductor begins to transfer energy to load. Between time t1 and t2, the slope of inductor current depends on the difference between input and output voltages, and it can be positive, negative or zero. At time t2, Q1&Q3 turn off and Q2&Q4 turn on with ZVS because inductor current is positive. At this moment, because the primary

side voltage polarity changes, inductor is discharged by both the input and output voltages, and keeps transferring energy to load. At the end of this half switching cycle, inductor current is reset to zero and then begins next half cycle. In this operation mode, all the primary side and secondary side switches can achieve ZVS turn on. Thus the switching loss can be minimized.

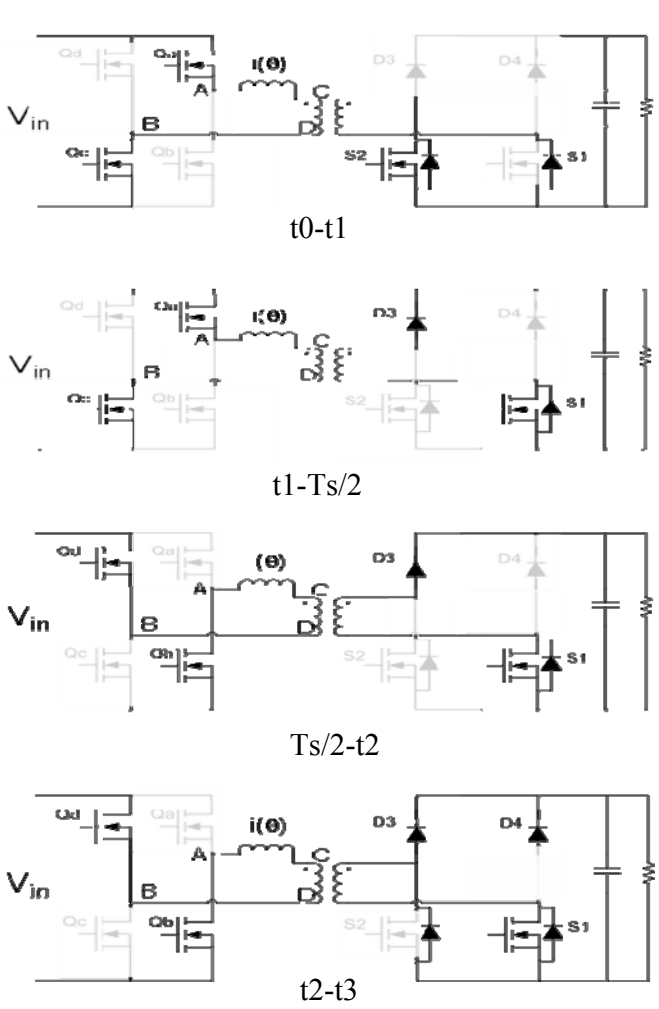

Figure 3-7 Equivalent circuits for each switching interval of isolated ZVS dual boost converter

According to the analysis above, from time 0 to t1, voltage across the inductor is input voltage Vin. Therefore, inductor current at time t1 can be calculated as

$$I_1 = \frac{V_{in}}{L} \cdot D_1 \cdot \frac{T_s}{2}$$

From time t1 to t2, voltage across the inductor is input voltage minus the output voltage reflected to primary side, which is Vin-nVo (In this equation n is transformer turns ratio.). Therefore, inductor current at time t2 can be calculated as

$$I_2 = I_1 + \frac{V_{in} - nV_o}{L} \cdot (1 - D_1) \cdot \frac{T_s}{2}$$

Between time t2 to T/2, inductor voltage is the sum of input and the output voltage reflected to primary side, which is -Vin-nVo. Because the inductor current is reset to zero at T/2, time between t2 and T/2 can be calculated as

$$\frac{T_s}{2} - t_2 = I_2 / \frac{V_{in} + nV_o}{L}$$

Because the time between t2 and T/2 is equal to the time between ta and 0,

$$D - D_1 = (\frac{T_s}{2} - t_2) / \frac{T_s}{2}$$

Once these currents at different time instances are calculated, the relationship between input and output voltage can be calculated accordingly.

If defining the voltage gain as

$$g = \frac{n \cdot V_o}{V_{in}}$$

From the volt-second balance on the inductor, it can be calculated as

$$D_1 + (1-g)\cdot(1-D) - (1+g)\cdot(D-D_1) = 0$$

Because from time t1 to T/2, the inductor current is transferred to the load, the average value of the transferred current should be the load current. Therefore,

$$\frac{1}{2}(1-D)\cdot(I_1 + I_2) + \frac{1}{2}(D-D_1)\cdot I_2 = \frac{n \cdot V_o}{R_L}$$

In this equation, R_L is the load resistance.

By combining previous equations, the relationship between the input and output voltage can be calculated.

The gain curve is shown in Figure 3-8. In these curves, the characteristic factor is defined as

$$Q = \frac{4 \cdot L}{n^2 \cdot R_L \cdot T_s}$$

Where L is the inductor value, n is transformer turns-ratio, R_L is load resistance and T is switching cycle. Comparing with conventional PWM converters, these gain curves are more similar to a resonant converter. The voltage gain is largely affected by both the phase shift and Q value.

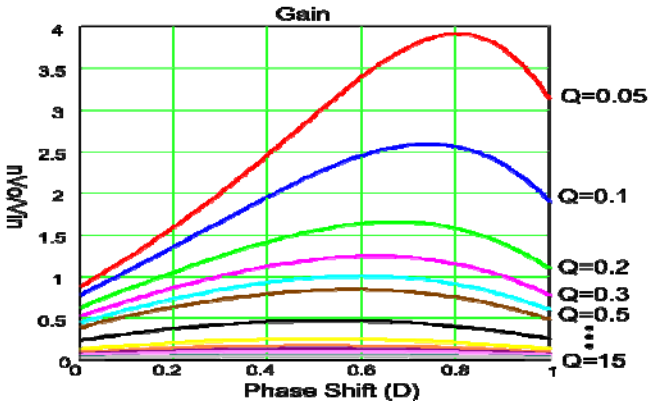

Figure 3-8 Gain curve of isolated ZVS dual boost converter

3.3 SR driving of isolated ZVS dual boost converter

For the low voltage, high current applications, synchronous rectification is desired because of its smaller conduction loss comparing with diode rectifiers. However, due to the capacitor filter structure, the proposed isolated dual boost couldn't achieve self-driven. Although using the current sensing on the synchronous rectifier (SR), SR can be controlled as the desired timing, due to the large load current and high di/dt of SR current, it is difficult to sense the current and adjust the timing. To address the issue, simple SR driving method has been proposed.

Isolated dual boost converter with SRs is shown in Figure 3-9. Both the switches and diodes on the secondary side are replaced with SRs. Considering the converter operating in CCM I mode for most of the time, SR driving scheme is mainly focus on this operation mode. The key waveforms are shown in Figure 3-10.

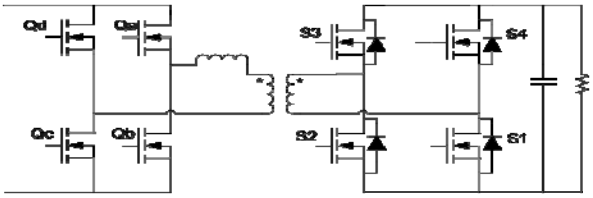

Figure 3-9 Isolated ZVS dual boost converter with synchronous rectification

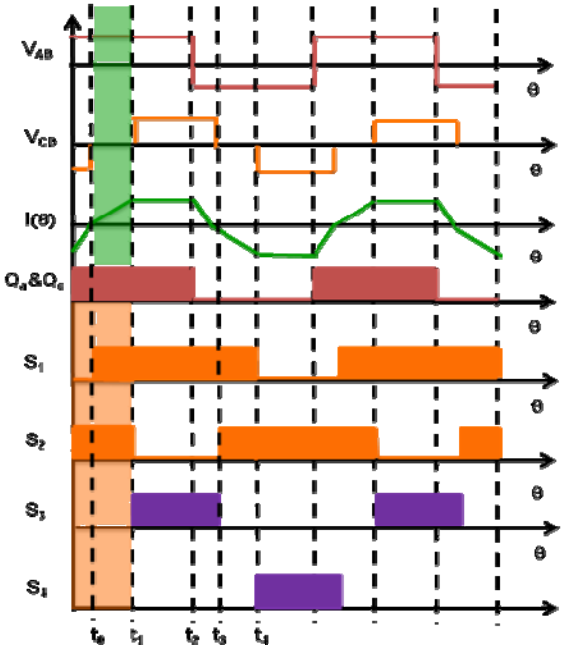

Figure 3-10 Isolated ZVS dual boost converter with synchronous rectification

From the Figure 3-10, it can be observed that, for SR S3, the desired conducting time should be between t1 to t3. For SR S2, its desired conduction time should be between t3 to t1, which is complimentary to S3 conduction. To get the desired gate signal, it is required to locate the time instances t1 and t3. Time instance t1 can be easily located, because it is delayed to rising time of Qa by the phase shift time D. However, time instance t3 is the inductor current zero-crossing point, which is very difficult to locate, if considering the current sensing and zero-

crossing detection. However, t2 can be easily located by the falling edge of signal Qa. If letting S3 conduct between t1 to t2 instead of t1 to t3, due to the short period (about 10ns) between t2 and t3, only extra 5W loss is generated on S3 because of the early turn-off, for 1200W output power. Thus, S3 can be controlled turn on between time t0 and t2 while still maintaining low conduction loss. Moreover, this signal can also be used to generate the gate signal for both S2 by employing commercial half bridge driver IC HIP6601 from Intersil. The driving circuit diagram is shown in Figure 3-11. For HIP6601, input PWM signal is used to control both the top and bottom switch. The gate driver input and output voltages are shown in Figure 3-12. At the rising edge of input signal, bottom switch is turned off and after a short delay to prevent shoot through, top switch is turned on. At the falling edge of input signal, top switch is turned off. Instead of turning on immediately after turning off of top switch, the bottom switch is turned on after its drain to source voltage dropping down below 0.5V, which means the body diode is going to conduct shortly. In this way, the body diode conduction time of bottom switch can be minimized. By using the driver IC, with S3 as the input signal, S3 can be turned on and off as desired time instances. Moreover, turning on of S2 can be automatically adjusted to time instance t3. Furthermore, SR S1 and S4 can be driven using the same scheme.

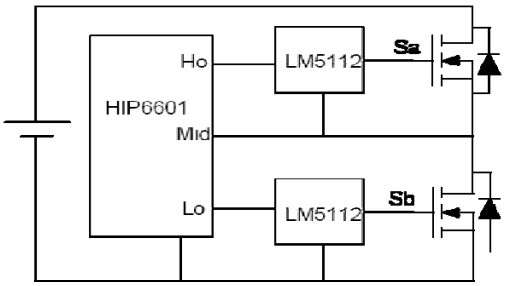

Figure 3-11 Synchronous rectification driving by HIP6601

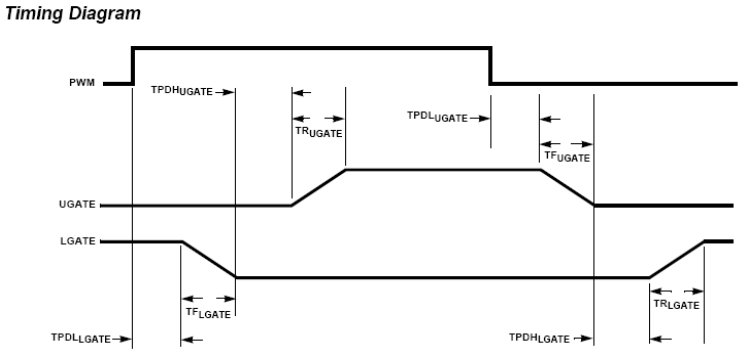

Figure 3-12 Timing Diagram of HIP6601

3.4 State plane analysis of isolated ZVS dual boost converter

According to the analysis of 3.2, the proposed converter can realized hold up time extension and have the feature of ZVS for all the switches. The current waveform is in a rectangular form thus has low current stresses on devices and relatively low RMS current. Thus this proposed converter is expected to be high power density and high efficiency if it can be guaranteed to be operated in the proposed mode.

Purely from topology point of view, this converter is constructed by 8 switches that two full bridge structures are on both primary and secondary sides

of an isolation transformer. The voltage waveform across the inductor could be either square waveform with any duty cycle, or phase shifted quasi-square waveform with any phase shift angle. It is questionable that the converter will run in the particular operation mode under all the condition without proper design. It is also unconfident to claim the proposed operation mode is the best mode for front-end DC/DC application without thoroughly exploration of all the possible operation modes for the proposed structure.

Conventional way to explore steady state operation of a newly proposed converter is typically through analysis on the waveform in time domain. For simple circuits like buck or boost that only contain two switches, the waveform analysis method is good enough to find out all the operation modes. But for more complex circuits contain more switches or contain some resonant tanks, people start to feel headache to looking at the operation modes through time domain by trying different waveforms without a systematical crew.

State plane analysis is a method used in the non-linear control system and is first introduced in power electronics field by T.G Wilson to study the dynamic performance of boost converter and introduced an alternative control strategy. It also has been used to tackle the unstable problem of series resonant converters (SRC) in the early stage of studying resonant converter and give people a clear view of dynamic and steady state operation of SRC from a new angle. The first time to use state plane analysis to identify different steady state operation modes is when people study the parallel resonant converters (PRC) whose operation is

much more complex than the SRC. Through state plane analysis, all the operation modes of PRC are uncovered by exam the possible equilibrium trajectories on the state plane. Some interesting operation modes that never been discovered before were discussed. After that, state plane analysis is used as a simple but powerful tool to study other type of resonant converters, like quasi-resonant converters and clamped mode resonant converters.

In this part, state plane is used as a tool instead of a traditional waveform analysis method to explore the operation mode of the isolated ZVS dual boost converter because this 8 switches structure is more complex than traditional two switches buck and using waveform analysis cannot guarantee a thoroughly exploration of its operation modes. After all the operation modes of the isolated ZVS dual boost converter has been identified. Comparison between those modes will be discuss to determine the best operation mode for front-end DC/DC application and the boundary between modes will be identified and the converter is designed to operate in the optimal points for all load conditions.

To construct a state plane for this 8 switches bridge type isolated converter, the topological modes of the converter need to be identified firstly. The switching combinations of primary side are shown in Figure 3-13. The first combination is when Qa and Qc turn on while Qb and Qd turn off. The input side of the inductor AB is connected to Vin. If define the positive current direction as the current flow from the input side to the load side, the source charges the inductor when the current is positive and discharges the inductor when the current is negative. The

second combination is when Qb and Qd turn on while Qa and Qc turn off. The input side of the inductor AB is connected to -Vin. The source discharges the inductor when the current is positive and charges the inductor when the current is negative. The third combination is when Qb and Qc turn on while Qa and Qd turn off. The input side of the inductor AB is shorted by the bottom switches. For the case when Qb and Qc turn off while Qa and Qd turn on, The input side of the inductor AB is shorted by the top switches. Because the voltage second applied to the inductor is same as both bottom switches turn on, this case is consider to be identical to the third combination and have not been listed separately. The fourth combination is when all the switches of primary side turn off that results the open circuit of the input side of the inductor.

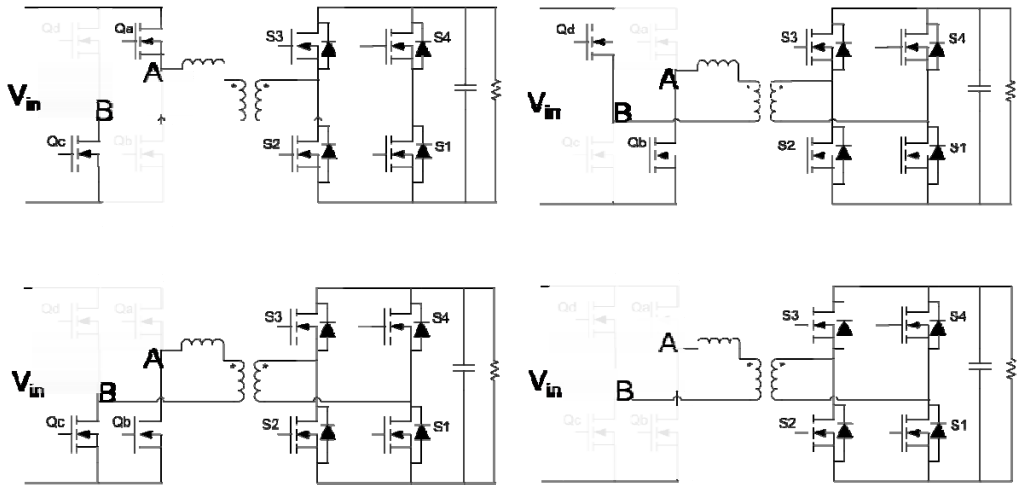

Figure 3-13 Switching combination of the primary side

The switch construction of the secondary side is the same as of the primary side. So the possible switching combinations will also be the same as of the primary side shown in Figure 3-14.

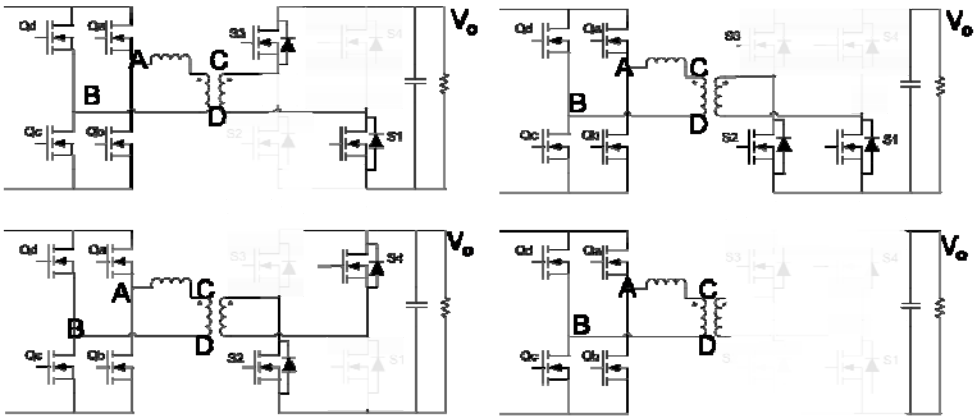

Figure 3-14 Switching combination of the secondary side

Combining the primary and the secondary and meanwhile considering the current direction, totally 22 topological modes are found for this 8 switches topology as shown in Figure 3-15. By observing these 22 topological modes, three normalized common equivalent circuits shown in Figure 3-16 are used to represent all the 22 modes in Figure 3-15.

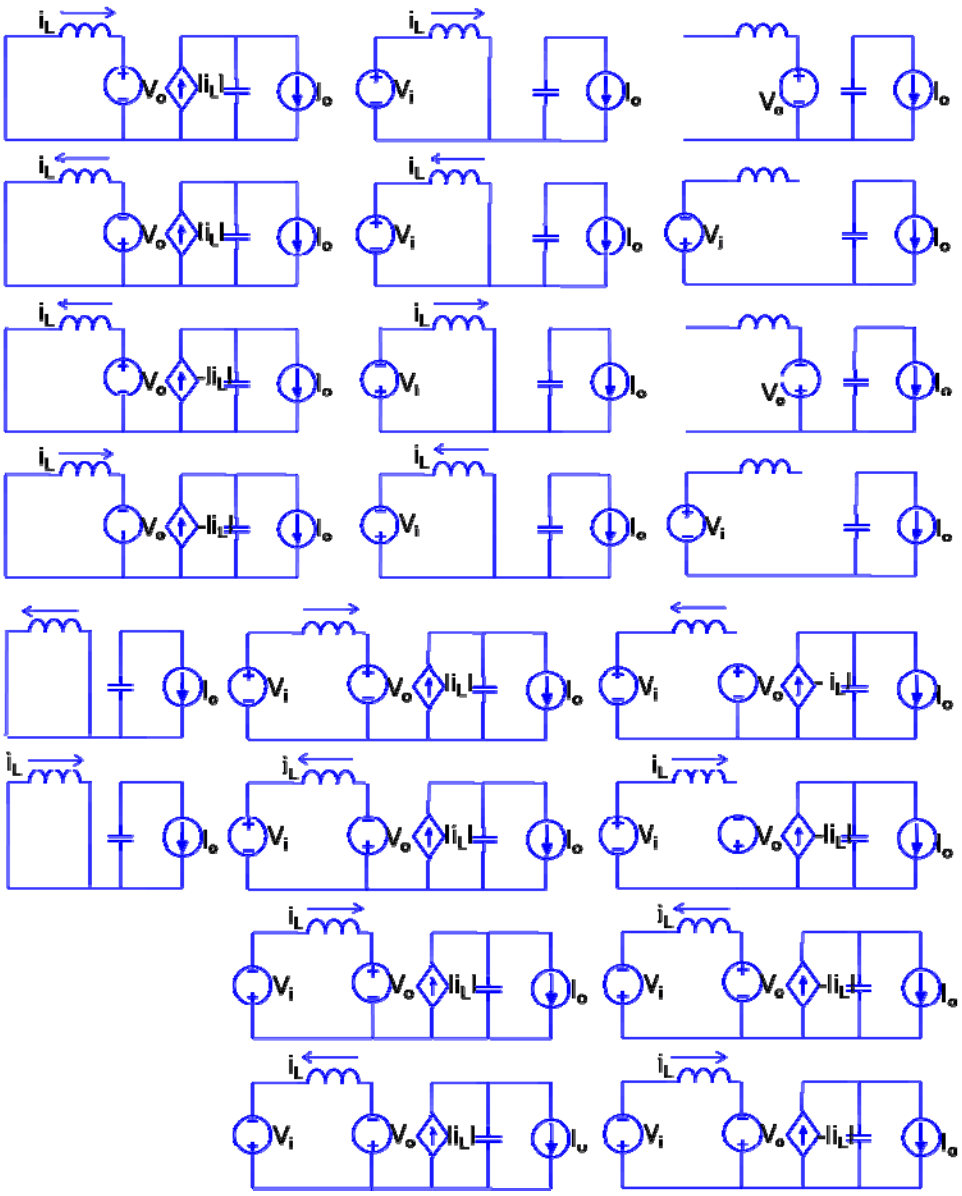

Figure 3-15 topological modes of isolated ZVS dual boost converter

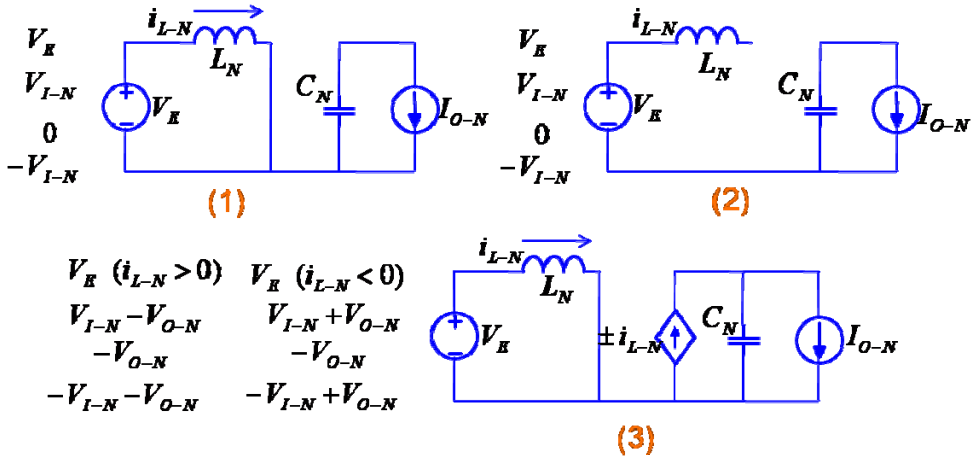

Figure 3-16 Normalized common equivalent circuits

The normalization rule is to normalize the voltage with output DC voltage and to normalize the current to the load DC current. The normalizations of inductance and capacitance are based on normalization of impedance to the load resistance. For example, the normalized impedance of an inductor can be written as

$$Z_{LN}(\omega) = \frac{Z_L(\omega)}{Z_R(\omega)} = \frac{j\omega \cdot L}{R}$$

And also can be written as

$$Z_{LN}(\omega) = L_N \cdot j \cdot \omega_N$$

So the inductance L can be solved that

$$L = \frac{R \cdot Z_{LN}(\omega)}{j\omega} = \frac{R \cdot L_N \cdot j \cdot \omega_N}{j\omega}$$

Because the normalized frequency ω_N can be expressed as

$$\omega_N = \frac{\omega}{\sqrt{LC}}$$

The normalized inductance can be solved that

$$L_N = \frac{L}{R \cdot \sqrt{LC}} = \frac{I_O}{V_O \sqrt{LC}} \cdot L$$

The normalization process for capacitance is in the same way as of inductance. All the normalization results are listed below:

$$L_N = \frac{I_O}{V_O \sqrt{LC}} \cdot L, C_N = \frac{V_O}{I_O \sqrt{LC}} \cdot C$$

$$V_{I-N} = \frac{V_I}{V_O}, V_{O-N} = \frac{V_O}{V_O}, I_{O-N} = \frac{I_O}{I_O}$$

$$i_{L-N} = \frac{i_L}{I_O}, v_{C-N} = \frac{v_C}{V_O}, t_N = \frac{t}{\sqrt{LC}}$$

The first circuit in Figure 3-16 represents the cases that secondary side of transformer is shorted. V_E could be either Vin, 0, and –Vin. The time domain expression of normalized inductor current and of normalized capacitor voltage can be written as

$$i_{L-N} = \frac{V_E}{L_N} \cdot t_N + i_{L-N}(t_N^0)$$

$$v_{C-N} = -\frac{I_{O-N}}{C_N} \cdot t_N + v_{C-N}(t_N^0)$$

And the state trajectory equation can be solve that

$$v_{C-N} = -\frac{L_N I_{O-N}}{C_N V_E} \cdot i_{L-N} + K_1$$

The secondary circuit represents the cases that secondary side of transformer is open circuit. V_E could also be either Vin, 0, and –Vin. The time domain expression of normalized inductor current and of normalized capacitor voltage can be written as

$$i_{L-N} = 0$$

$$v_{C-N} = -\frac{I_{O-N}}{C_N} \cdot t_N + v_{C-N}(t_N^0)$$

And the state trajectory equation can be solve that

$$i_{L-N} = 0$$

The third circuit represents the cases that energy is been transferred between source and the load. The V_E could be Vin-Vo, 0, or -Vin-Vo when the gain is larger than 1 and be Vin+Vo, 0, or –Vin+Vo when the gain is smaller than 1. The time domain expression of normalized inductor current and of normalized capacitor voltage can be written as

$$i_{L-N} = \frac{V_E}{L_N} \cdot t_N + i_{L-N}(t_N^0)$$

$$v_{C-N} = \frac{1}{C_N} \cdot [\frac{V_E}{2L_N} \cdot {t_N}^2 + i_{L-N}(t_N^0) \cdot t_N \pm I_{O-N} t_N] + v_{C-N}(t_N^0)$$

And the state trajectory equation can be solve that

$$v_{C-N} = \begin{cases} \frac{L_N}{2C_N V_E} \cdot ({i_{L-N}}^2 \pm 2I_{O-N} i_{L-N}) + K_2 & i_{L-N} \geq 0 \\ \frac{L_N}{2C_N V_E} \cdot (-{i_{L-N}}^2 \pm 2I_{O-N} i_{L-N}) + K_2 & i_{L-N} \leq 0 \end{cases}$$

According to the three state trajectory equations list above, a completed state portrait can be plotted as shown in Figure 3-17. The x-axis is normalized capacitor voltage and the y-axis is normalized inductor current. For a steady state operation mode presenting as a close loop, current stress and output voltage ripple can be directly read from the state plane.

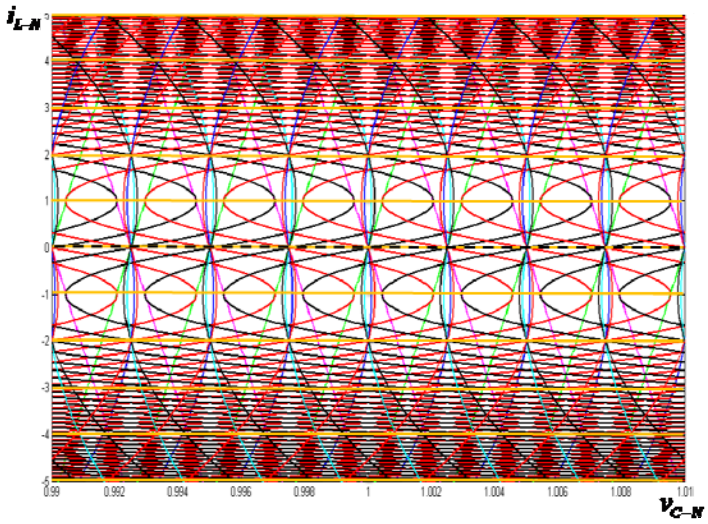

Figure 3-17 completed state portrait for the proposed topology

This state portrait looks complex because all the topological modes are included and all the possible operation modes can be found from the state portrait. Although the operation modes are finite, exhausting from such a complex portrait is still difficult and is not efficiency to study a circuit. Alternatively, customizing the state plane by excluding some topological modes that will never appear for the circuit to be studied will greatly reduce the complexity of the state plane and make the exhaustion of operation modes to be easier. Two methods have been indicated to customize the state plane as following. The first method is to indicate the waveform shape of both sides of the series inductor. And the second method is to specify the undesired functions.

Method 1:

As the first method, one can specify the voltage waveforms of both sides of the inductor to be square waveform, or specify the voltage waveform of left side

of the inductor to be square waveform and the right side of the inductor to be quasi-square waveform that as indicated in Figure 3-18, or specify the voltage waveform of left side of the inductor to be quasi-square waveform and the right side of the inductor to be square waveform.

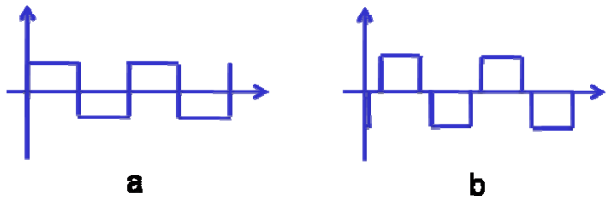

Figure 3-18 (a) square waveform (b) quasi-square waveform

The first case that specifying voltage on both sides of the inductor to be square waveform is taken as an example to show the customization of the state plane. As the restriction of square waveform, topological modes that associate a short circuit on either primary or secondary sides can be excluded, as well as topological modes appears open circuit on either primary or secondary sides. As the result, the 22 topological modes indicated in Figure 3-15 can be reduced to 8 as shown in Figure 3-19 and the state plane can be simplized as shown in Figure 3-20. Compared with the completed state plane shown in Figure 3-17, this customized state plane gives a much more clear picture and thus the thorough exploration of operation modes under the specific restrictionts becomes much easier.

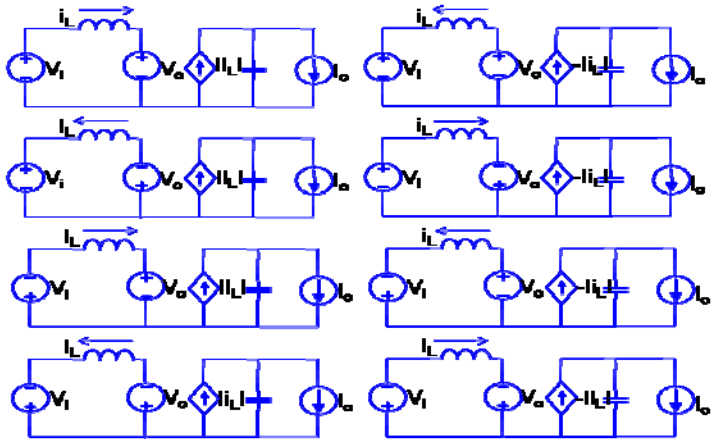

Figure 3-19 topological modes under restriction: square voltage waveform on both sides of inductor

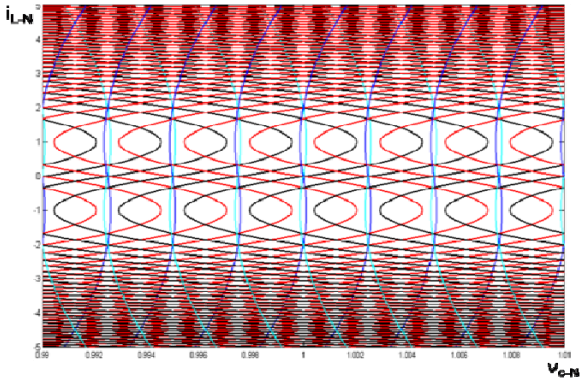

Figure 3-20 customized state plane under restriction: square voltage waveform on both sides of inductor

To search the possible operation modes, a starting point need to be set at where the normalized inductor current equals 0 and the normalized capacitor voltage equals 1. This point indicates an initial point with zero inductor current and capacitor voltage equals the DC value of the output voltage. Any close loop state portrait represents a steady state operation mode. A possible steady state operation mode can be found on the state plane as shown in Figure 3-21 (a) with

indicated inductor current ripple and output voltage ripple. After drawing the accordingly time domain waveform as shown in Figure 3-21 (b), one can find this operation mode has already been proposed by D.M. divan [3.5]. The circuit is shown in Figure 3-21 (c). This circuit features ZVS for all the MOSFETs and easy driving and control schemes that fixed duty cycle, fixed frequency, no phase shift on both the primary side and the secondary side of the transformer. The phase shift between the primary side and the secondary side is used to regulate the output voltage. The disadvantage of this circuit is large circulating energy and that the ZVS range is limited by the load condition and also the gain range.

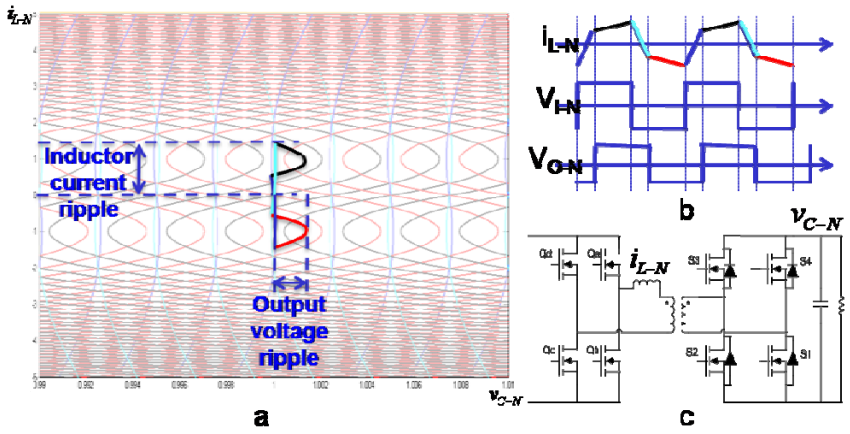

Figure 3-21 steady state operation mode 1 under restriction: square voltage waveform on both sides of inductor (a) state portrait (b) waveform (c) circuit

Another possible steady state operation mode is shown in Figure 3-22 (a) with the same sequence as of the one shown in Figure 3-21 but with asymmetrical shape. Compared with operation mode 1 under same condition, this circuit will have larger inductor current ripple and larger output voltage ripple. According to

the waveform, this circuit has been proposed by Dehong Xu [3.6]. The author modified the original DAB circuit by adding duty cycle as another control variable to extent the ZVS operation range, but also increased the control complexity as a penalty.

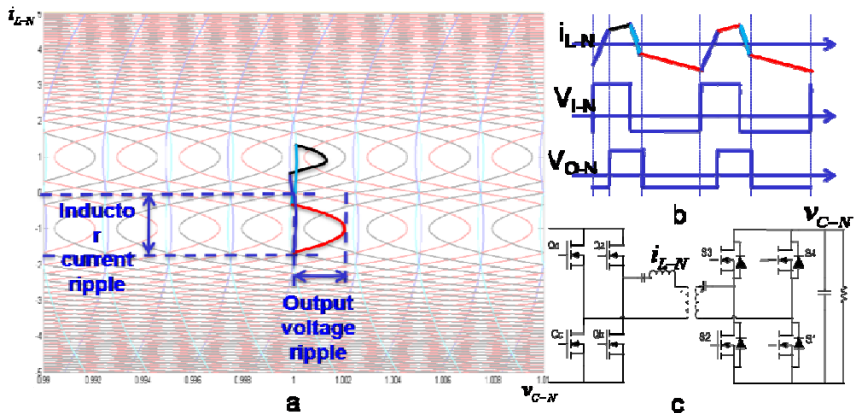

Figure 3-22 steady state operation mode 2 under restriction: square voltage waveform on both sides of inductor (a) state portrait (b) waveform (c) circuit

Other than these two steady state operation modes mentioned above, other operation modes that have not been discovered can be also found in the state plane. Figure 3-23 (a) shows a new steady state operation mode has been found and its waveform is shown in Figure 3-23 (b). The duty cycles of both sides are same. The gain of this discovered circuit is controlled by duty cycle. The driving scheme is a little bit strange that for every switching cycle the duty cycle need to switch between D and 1-D. The disadvantage of this circuit is still large circulation energy.

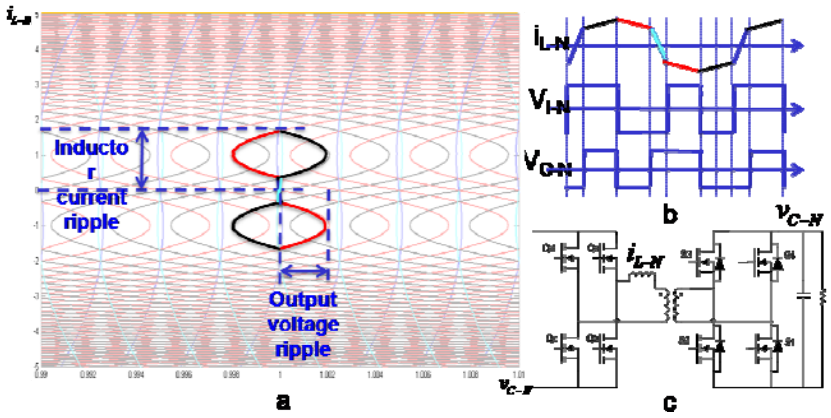

Figure 3-23 steady state operation mode 3 under restriction: square voltage waveform on both sides of inductor (a) state portrait (b) waveform (c) circuit

Method 2:

The second method that to specify the undesired function is from another angle of view to customize the state plane. For example, if the converter is expected to have minimum circulating energy, all the switching intervals that input discharges the inductor and that output charges the inductor are not desired. So all the topological modes that involves the functions that input discharges the inductor and that output charges the inductor need to be deleted from the complete state plane. The new customized state plane is shown in Figure 3-24. By avoiding these undesired topological modes, circulating energy can be minimized to the amount that is just enough to realize the ZVS function, which is only during the dead time.

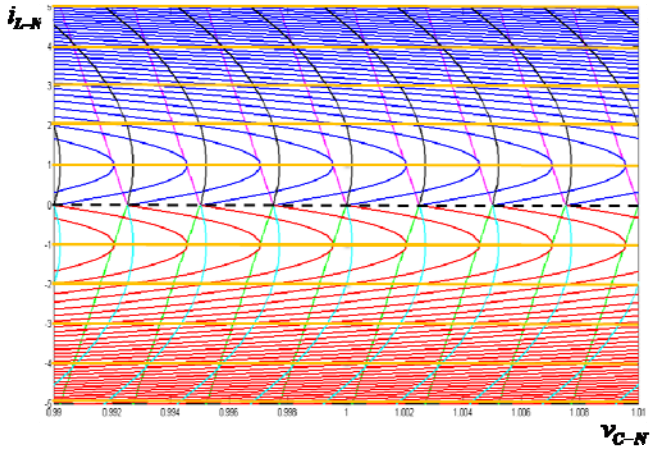

Figure 3-24 customized state plane under restriction: no switching intervals that input discharges the inductor and that output charges the inductor

The example steady state portraits are shown in Figure 3-25 and Figure 3-26 together with their waveforms and circuits.

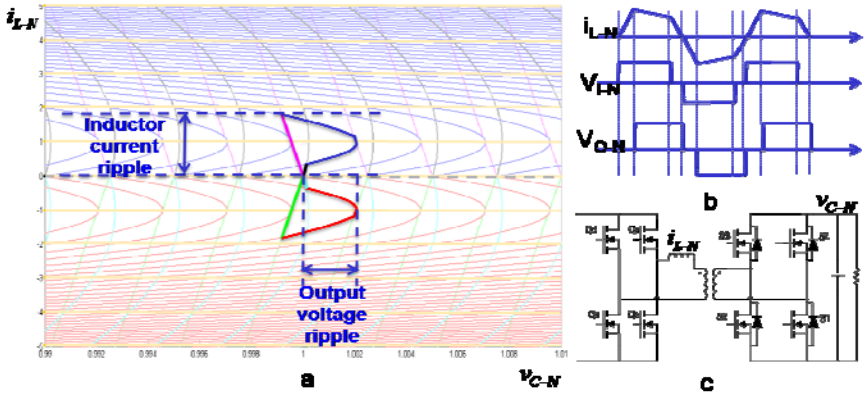

Figure 3-25 steady state operation mode 1 under restriction: no switching intervals that input discharges the inductor and that output charges the inductor (a) state portrait (b) waveform (c) circuit

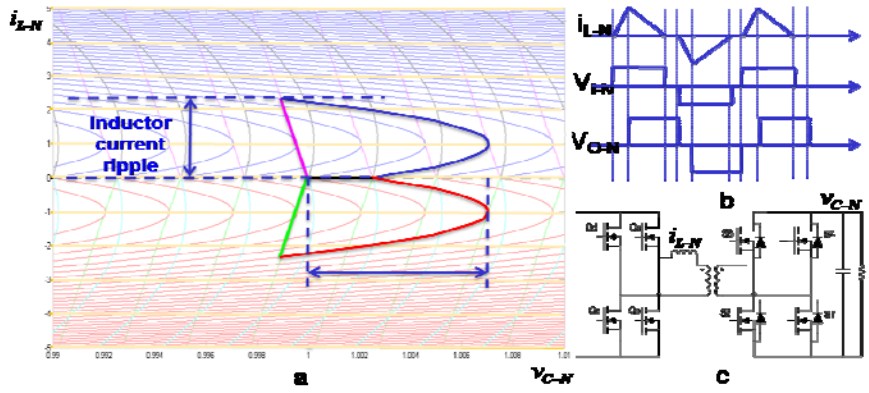

Figure 3-26 steady state operation mode 2 under restriction: no switching intervals that input discharges the inductor and that output charges the inductor (a) state portrait (b) waveform (c) circuit

For the operation mode 1 in Figure 3-25, the current waveform is rectangular. The voltage waveforms on both the primary and the secondary sides are quasi-square. Circulating energy is minimized by the selected topological modes. But the control and driving strategy is becoming complex because the undesired topological modes need to be purposely avoided. The phase shift between the primary side and the secondary side might used to regulate the output voltage and the phase shift of primary side itself or/and of secondary side itself might be used to guarantee the operation mode. For the operation mode 2 in Figure 3-26, the current waveform is triangular. All the primary side switches is ZCS turn off which is good for IGBT devices. But the current stress is larger than the operation mode 1 because the shape of the current waveform. Control and driving strategy for this operation mode will be as complex as the operation mode 1. These two operation modes have been proposed by N.Schilbli in his PhD thesis [3.7].

These two methods mentioned above are combined to generate the restrictions to study the proposed isolated ZVS dual boost converter. To restrict the function, it is specified to be unidirectional current flow because bidirectional current flow is not necessary for front-end converter applications. In addition to the functional restriction, primary side voltage waveform is specified to be 0.5 duty cycle square waveform to further eliminate the topological modes to simplify the analysis. With these two restrictions, the possible topological modes are reduced to 9 as shown in Figure 3-27.

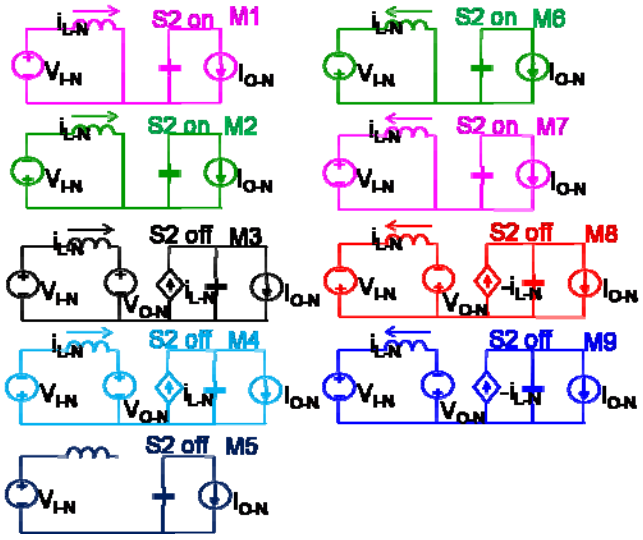

Figure 3-27 topological modes under restrictions: 1. unidirectional current flow, 2. 0.5 duty cycle square waveform of voltage on the primary side of transformer

And accordingly, the state plane is drawn in Figure 3-28, where the trajectories are with directions because the function of this converter is limited to unidirectional current flow. Figure 3-28 (a) is for the cases when the voltage gain is smaller than 1 and Figure 3-28 (b) is for the cases when the voltage gain is

larger than 1. The difference between (a) and (b) is the directions of the red and the black hyperbolic curves according to their state equations:

$$v_{C-N} = \begin{cases} \frac{L_N}{2C_N V_E} \cdot (i_{L-N}{}^2 \pm 2I_{O-N} i_{L-N}) + K_2 & i_{L-N} \geq 0 \\ \frac{L_N}{2C_N V_E} \cdot (-i_{L-N}{}^2 \pm 2I_{O-N} i_{L-N}) + K_2 & i_{L-N} \leq 0 \end{cases}$$

Where $V_E = V_{L-N} - V_{O-N}$

So V_E is positive when the voltage gain is smaller than 1 and vice verse.

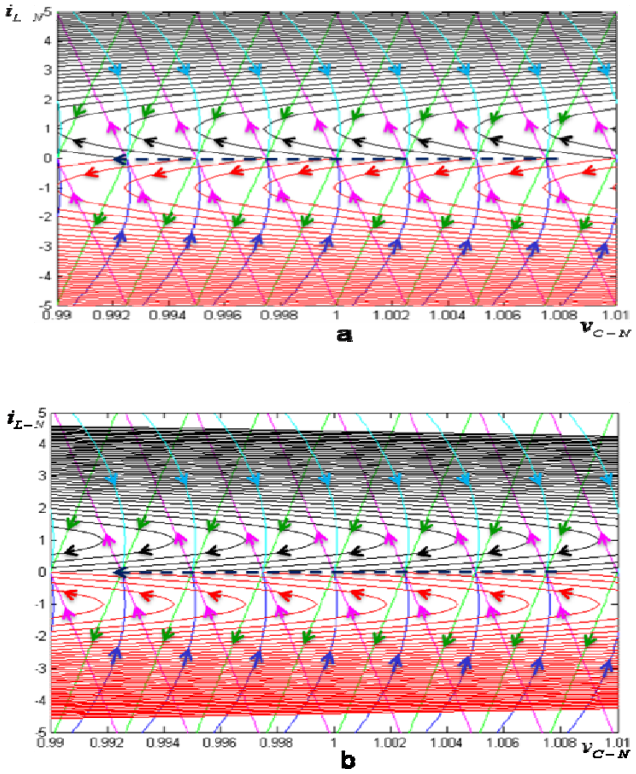

Figure 3-28 customized state plane under restrictions: 1. unidirectional current flow, 2. 0.5 duty cycle square waveform of voltage on the primary side of transformer. (a) for voltage gain < 1 (b) for voltage gain > 1

To guarantee a thorough exploration, the operation modes are categorized by switching intervals. For two switching intervals' operation modes, three steady state state portraits can be found in Figure 3-28 (a) for voltage gain < 1 case, which are M1M4M6M9, M3M4M8M9, and M3M2M8M7. And two steady state state portraits can be found in Figure 3-28 (b) for voltage gain > 1 case, which are M1M3M6M8 and M1M4M6M9. For three switching intervals' operation modes, six steady state state portraits can be found in Figure 3-28 (a) for voltage gain < 1 case, which are M1M4M2M6M9M7, M1M3M4M6M8M9, M3M4M2M8M9M7, M1M3M2M6M8M7, M3M2M4M8M7M9, and M1M2M4M6M7M9. And five steady state state portraits can be found in Figure 3-28 (a) for voltage gain > 1 case, which are M1M3M4M6M8M9, M1M3M2M6M8M7, M1M3M5M6M8M5, M1M2M4M6M7M9, and M1M4M2M6M9M7.

The relationship between two switching intervals operation and three switching intervals' operation is shown in Figure 3-29. The three switching intervals' operation is actually derived from the two switching intervals' operation by interrupting M3 and inserting M4. The switching actions which are overlapped in two intervals' operation are now separated in three switching intervals' operation. The four switching intervals' operation is thus derived from the three switching intervals' operation as shown in Figure 3-30. M3 is again interrupted and M2 is inserted. To realize this modification, additional switching actions must be generated because there is no overlapping switching actions in three switching interval's operation. Equivalently, the switch frequency is at least doubled for

four or more than four switching intervals' cases. Accordingly switching loss is increased. Therefore it is not necessary to study four or more than four switching intervals' cases for this converter because it will do no good from the efficiency point of view.

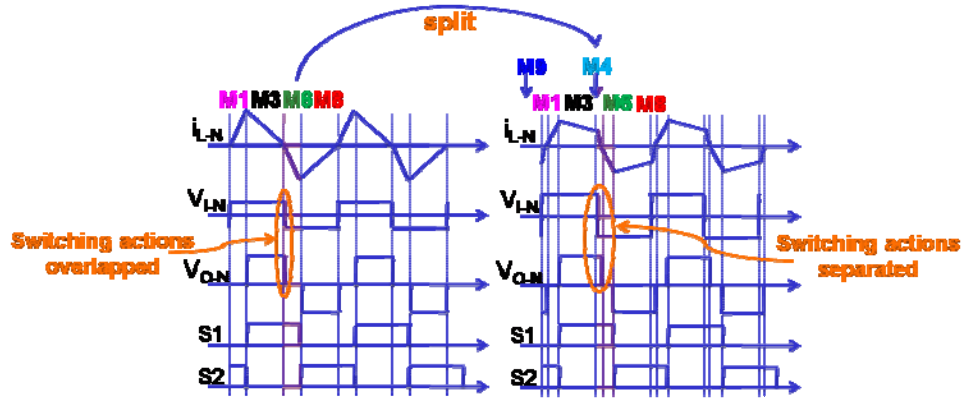

Figure 3-29 relationship between two switch intervals and three switch intervals transition

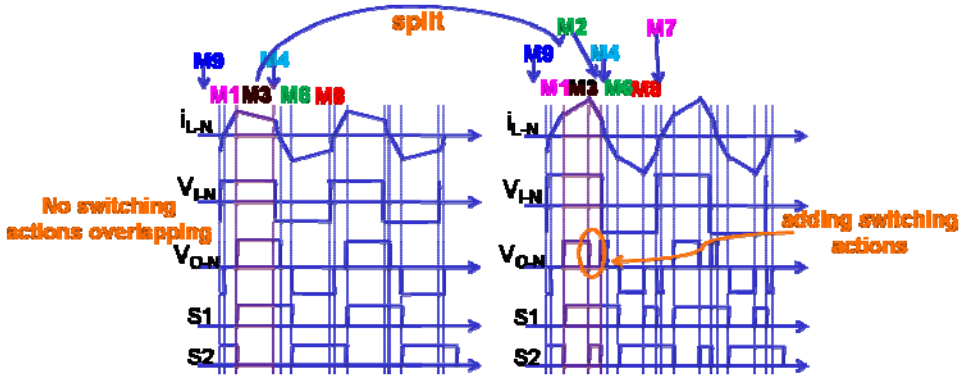

Figure 3-30 relationship between three switch intervals and four switch intervals transition

The exploration of operation modes for the isolated ZVS dual boost converter now is limited to two switching intervals and three switching intervals. For gain < 1 cases, three two switching intervals' operations and six three intervals'

operations are available. For gain >1 cases, two two switching intervals' operations and five three switching intervals' operations are available. However some overlaps are found in this category. For example M1M4M6M9 appears in both gain < 1 and gain > 1 case. After resorting, there are four steady state operation modes contain two switching intervals and seven steady state operation modes contain three switching intervals and are listed below:

Three switching intervals: M3M2M4M8M7M9, M1M3M2M6M8M7, M1M4M2M6M9M7, M1M3M4M6M8M9, M3M4M2M8M9M7, M1M2M4M6M7M9, and M1M3M5M6M8M5. Two switching intervals: M1M4M6M9, M3M4M8M9, M3M2M8M7, and M1M3M6M8;

One by one examination on these steady state operation modes will be conducted. The key waveforms of steady state operation mode M3M2M4M8M7M9 is shown in Figure 3-31. It is noticed that at the transition between topological mode M3 and M2, switching actions are overlapped. This is determined by the characteristics of topological modes M3 and M2 that the voltages on both sides of inductor are different as shown in Figure 3-32. So both the primary and the secondary side need to switch to complete the transition from M3 to M2. And as the result, additional switching actions have to be introduced to realize the three switching intervals' operation. This steady state operation is not interested because of unnecessary switching loss and is not possible to be one of the operation modes of our proposed converter because of its equivalent switching frequency.

Figure 3-31 key waveforms of steady state operation mode: M3M2M4M8M7M9

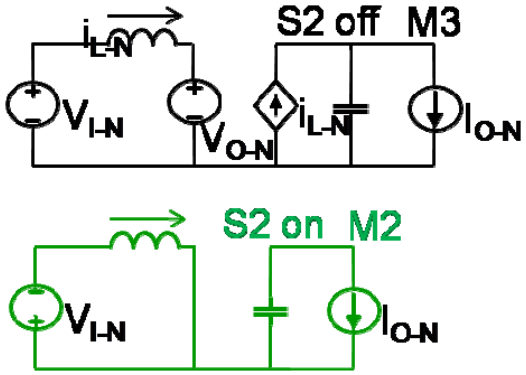

Figure 3-32 topological modes M3 and M2

The key waveforms of steady state operation mode M1M3M2M6M8M7 is shown in Figure 3-33. And its gain curve and normalized RMS current is shown in Figure 3-34. This operation mode features small current stress, small RMS current, and ZVS on all primary side switches. But it cannot be used for front-end converter application because its voltage gain is limited. The control strategy for this operation mode is that no phase shift between the primary side and the secondary side and only the duty cycle of the secondary side switches regulates the output voltage. It won't be a operation mode for our proposed converter because for our converter the duty cycle of the secondary side switches is fixed

and the phase shift between the primary side and the secondary side is used to regulate the output voltage.

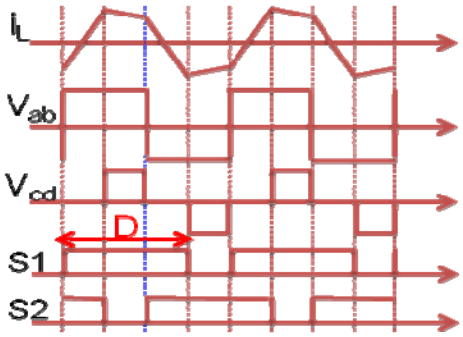

Figure 3-33 key waveforms of steady state operation mode: M1M3M2M6M8M7

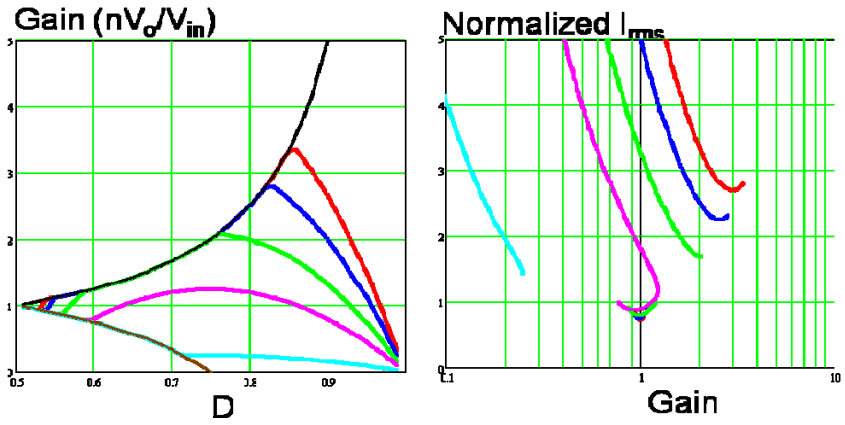

Figure 3-34 gain curve and normalized RMS current for operation mode: M1M3M2M6M8M7

The key waveforms of steady state operation mode M1M4M2M6M9M7 is shown in Figure 3-35. And its gain curve and normalized RMS current is shown in Figure 3-36. This operation mode is not good because of large current stress and large circulating energy. The control strategy is also to control the secondary

side duty cycle but no phase shift between the primary side and the secondary side. So this operation mode is not associated with the proposed converter.

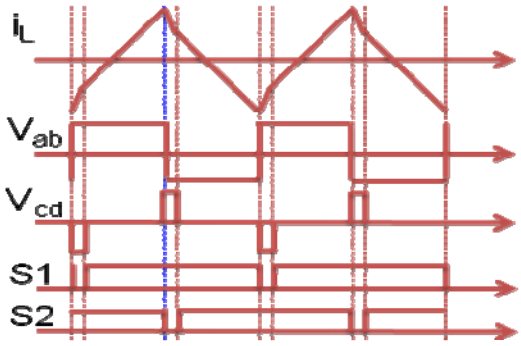

Figure 3-35 key waveforms of steady state operation mode: M1M4M2M6M9M7

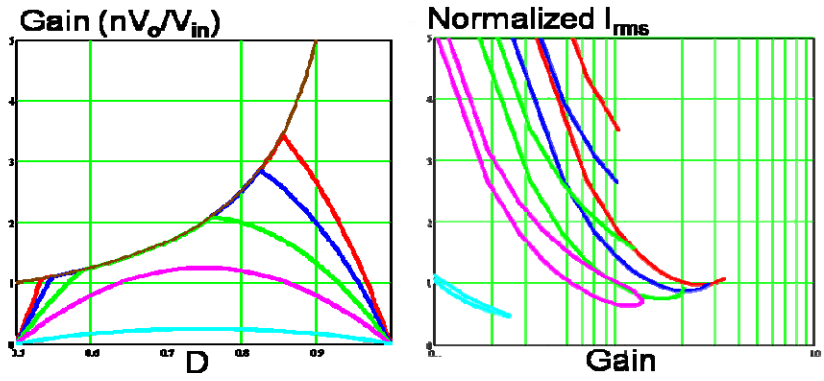

Figure 3-36 gain curve and normalized RMS current for operation mode: M1M4M2M6M9M7

The key waveforms of the rest four steady state operation modes M1M3M4M6M8M9, M3M4M2M8M9M7, M1M2M4M6M7M9, and M1M3M5M6M8M5 are shown in Figure 3-37. The CCM I mode -- M1M3M4M6M8M9 is what has been proposed in 3.2. All the other three operation modes are associated operation modes with the proposed converter

because they share the same control and driving strategy that has a fix 0.5 duty cycle on S1 and S2 and the phase shift between the primary side and the secondary side is used to regulate the output voltage.

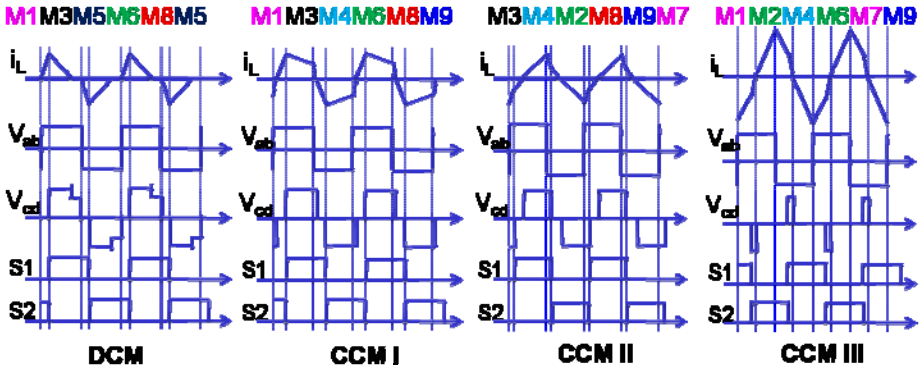

Figure 3-37 key waveforms of isolated ZVS dual boost operation modes

Comparing amount these four operation modes will be based on the ZVS operation, current stress, circulating energy and RMS current. For DCM ZVS can be realized on the secondary side switches but ZCS for all the primary side switches. For CCM I and CCM III ZVS can be realized on all the switches and ZCS on secondary side diodes. For CCM II ZVS can only be realized on the primary side. From the current stress point of view CCM I will have the smallest current stress because the inductor current is in rectangle shape while all the other three modes have a triangle current waveform. From the circulating energy of view CCM III is worst because the secondary side only conduct for a very short period. Although CCM III can realize ZVS for all the switches and ZCS for secondary side diodes which is as attractive as of CCM I mode, its disadvantage on circulating energy wipe it out of our interesting. The gain curve is shown in

Figure 3-38 and the normalized RMS current is shown in Figure 3-39. The detail calculation of RMS current will be described in 3.5. From the Figure 3-39one can find the smallest RMS current can be achieved when the gain is equal to one and from the Figure 3-38 one gain equal to one can only be realized in the range of CCM I. Therefore, CCM I is claimed to be the best operation mode for the proposed isolated ZVS dual boost converter. The design will restrain the operation to be CCM I.

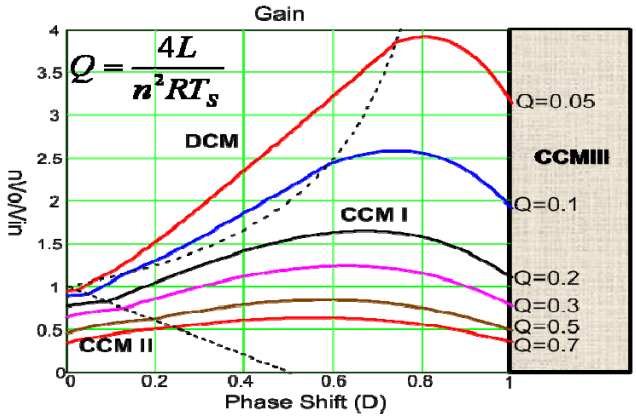

Figure 3-38 gain curve of isolated ZVS dual boost converter

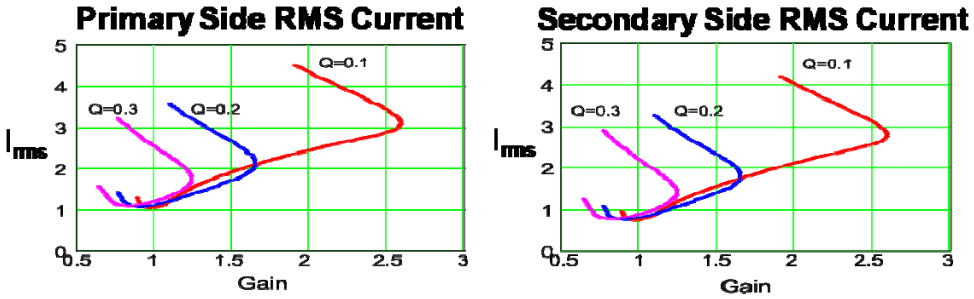

Figure 3-39 normalized RMS current of isolated ZVS dual boost converter

Two switching intervals' steady state operations are the boundaries of three switching intervals' cases or the special cases of the three switching intervals' operation, because if the duration of a switching interval in three switching intervals' operation becomes shorter and shorter and eventually becomes zero, the three switching intervals' operation will degrade to two switching intervals' case.

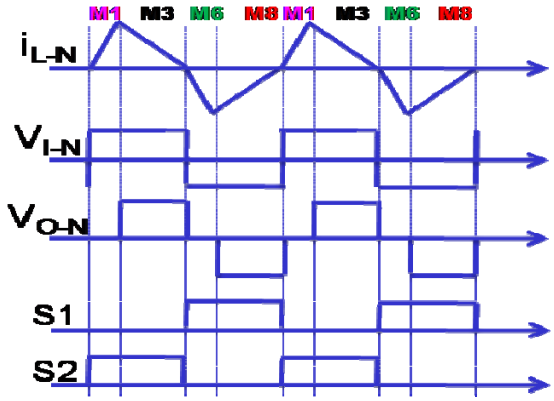

Figure 3-40 key waveforms of steady state M1M3M6M8

Figure 3-40 shows an example two switching intervals' operation M1M3M6M8 which is the boundary mode between DCM mode and CCM I shown in Figure 3-38 is the curve that g=1/(1-D). For the other three two switching intervals' operation, M1M4M6M9 is the boundary mode between CCM I and CCM III mode. M3M4M8M9 is the boundary mode between CCM I and CCM II. And M3M2M8M7 is a special case of CCM II when the phase shift between the primary side and the secondary side is zero.

3.5 Design of isolated ZVS dual boost converter

Because of the soft switching capability, the converter efficiency estimation should focus on conduction loss. Therefore, transformer primary side and secondary side RMS currents normalized with load current can be used as indicators of conduction loss.

As shown in Figure 3-41, for primary side current, the entire transformer current goes through primary, it should use the transformer current to estimate the primary RMS current, which can be expressed as:

$$Irms = \sqrt{\frac{\int_0^{D1\cdot\frac{Ts}{2}} \left(\frac{Vin}{L}t\right)^2 dt + \int_0^{(1-D)\frac{Ts}{2}} \left(\frac{Vin}{L}D1\cdot\frac{Ts}{2} + \frac{Vin - n\cdot Vo}{L}\cdot t\right)^2 dt + \int_0^{(D-D1)\frac{Ts}{2}} \left(\frac{Vin + n\cdot Vo}{L}\cdot t\right)^2 dt}{\frac{Ts}{2}}}$$

After normalized with load current, it can be written as:

$$\frac{\frac{Irms}{Vo}}{n\cdot R} = \frac{2}{g\cdot Q}\cdot\sqrt{\frac{1}{3}\cdot D1^3 + D1^2\cdot(1-D) + (1-g)\cdot D1\cdot(1-D)^2 + \frac{1}{3}\cdot(1-g)^2\cdot(1-D)^3 + \frac{1}{3}\cdot(1+g)^2\cdot(D-D1)^3}$$

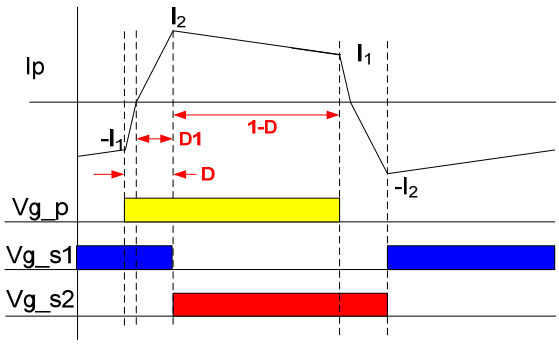

Figure 3-41 Current waveform through primary side switches

The current waveform of secondary side bottom switches is shown in Figure 3-42. And can be expressed as:

$$Irms\_S = \sqrt{\frac{2\cdot\int_0^{D1\cdot\frac{Ts}{2}}\left(\frac{Vin}{L}t\right)^2 dt + \int_0^{(1-D)\frac{Ts}{2}}\left(\frac{Vin}{L}D1\cdot\frac{Ts}{2} + \frac{Vin - n\cdot Vo}{L}\cdot t\right)^2 dt + \int_0^{(D-D1)\frac{Ts}{2}}\left(\frac{Vin + n\cdot Vo}{L}\cdot t\right)^2 dt}{Ts}}$$

Normalized to the load current and become:

$$\frac{Irms\_S}{\frac{Vo}{n\cdot R}} = \frac{\sqrt{2}}{g\cdot Q}\cdot\sqrt{\frac{2}{3}\cdot D1^3 + D1^2\cdot(1-D) + (1-g)\cdot D1\cdot(1-D)^2 + \frac{1}{3}\cdot(1-g)^2\cdot(1-D)^3 + \frac{1}{3}\cdot(1+g)^2\cdot(D-D1)^3}$$

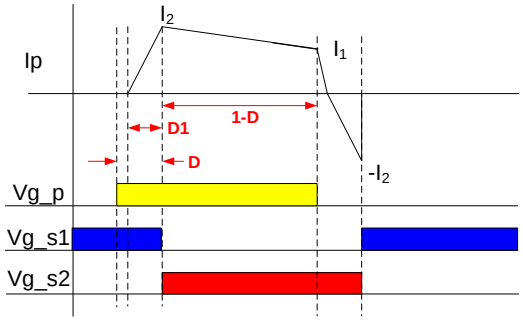

Figure 3-42 Current waveform through secondary side bottom switches

The current waveform of secondary side top diodes is shown in Figure 3-43. And can be expressed as:

$$Irms\_T = \sqrt{\frac{\int_0^{(1-D)\frac{Ts}{2}}\left(\frac{Vin}{L}D1\cdot\frac{Ts}{2} + \frac{Vin - n\cdot Vo}{L}\cdot t\right)^2 dt + \int_0^{(D-D1)\frac{Ts}{2}}\left(\frac{Vin + n\cdot Vo}{L}\cdot t\right)^2 dt}{Ts}}$$

Normalized to the load current and become:

$$\frac{\frac{Irms\_T}{Vo}}{n \cdot R} = \frac{\sqrt{2}}{g \cdot Q} \cdot \sqrt{D1^2 \cdot (1 - D) + (1 - g) \cdot D1 \cdot (1 - D)^2 + \frac{1}{3} \cdot (1 - g)^2 \cdot (1 - D)^3 + \frac{1}{3} \cdot (1 + g)^2 \cdot (D - D1)^3}$$

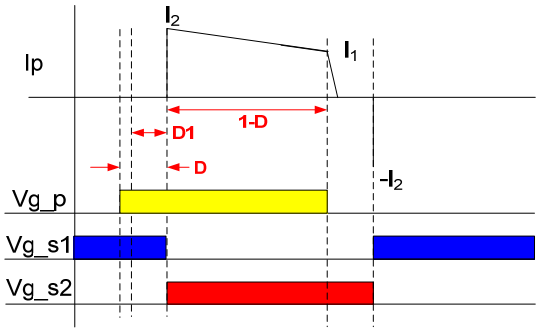

Figure 3-43 Current waveform through secondary side top diodes

The normalized primary side RMS current for different designs is shown in Figure 3-44. It shows that gain equal to one and smaller Q will minimize primary side conduction loss. Normalized secondary side RMS current for bottom switch and for top diode are shown in Figure 3-45 and Figure 3-46 respectively, similar trend as of the primary side can be observed.

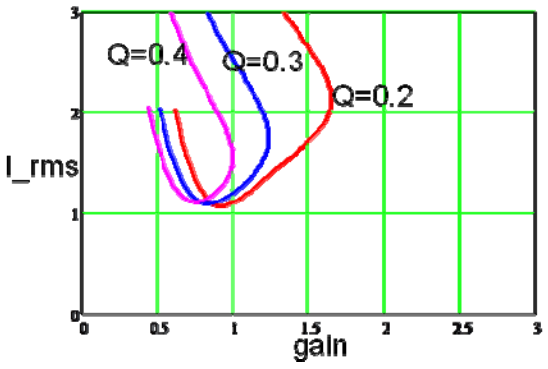

Figure 3-44 Normalized RMS current of primary side switch

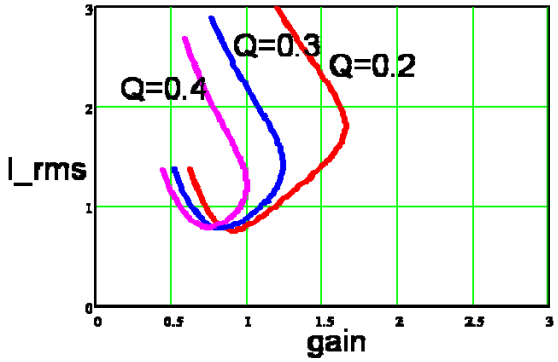

Figure 3-45 Normalized RMS current of secondary side bottom switch

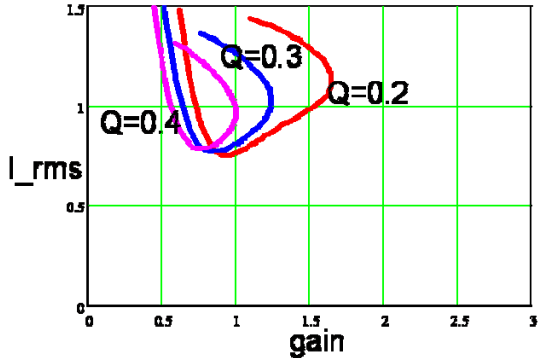

Figure 3-46 Normalized RMS current of secondary side top diode

To have a smaller Q value, smaller inductor value is required. However, smaller inductor will make the circuit difficult to be protected during over current condition. For instance, if the load is shorted, transformer is shorted on secondary side and smaller inductor could result in huge current and damage the converter. Therefore, considering the trade-off between efficiency and easy protection, Q=0.2 and gain equal to one is chosen as the design.

Because the proposed converter can be optimally operated at gain equal to one, this operation point can be designed as normal operation mode when input

AC line exists and DC/DC stage input voltage is the regulated 400V DC from PFC stage output. During holdup time, because of the decreasing input voltage, the phase shift between primary side and secondary side can be enlarged to increase the converter voltage gain and regulate output voltage. Thus, the extra voltage boost capability of the proposed topology enables maintaining regulating output voltage during holdup time. For instance, the peak gain of Q=0.2 is about 1.6. Thus, the proposed converter can operate with 400/1.6=250V input. Although choose Q=0.2 can easily make the converter operation down to 250V input, considering 400V input at normal operation, only 60% of the energy stored in holdup time capacitor is utilized. If the minimum input voltage can be further decreased, more energy stored in holdup time capacitor can be used, which means less holdup time capacitor and higher power density could be achieved.

For a designed isolated dual boost converter, primary side inductance and transformer turns-ratio are fixed. According to the gain characteristic curves, for certain load condition and switching frequency, the maximum gain that can be achieved is determined accordingly. Although the inductance and transformer turns-ratio are fixed, Q value can still be changed by adjusting the switching frequency. Form the gain curves, smaller Q can further increase the gain of converter and enlarge the DC/DC converter input voltage range. Therefore, during holdup time, converter switching frequency can be reduced to decrease Q value and increase peak gain. For instance, if the switching frequency is reduced to half, Q value decreases from 0.2 to 0.1. The converter peak gain can be easily pushed

up to 2.5 and the minimum DC/DC operation voltage could be as low as 160V. Thus, more than 80% energy stored in the holdup time capacitor can be used, and the holdup time capacitor can be reduced to 440uF for 1200W power level. Therefore, by using the proposed converter, holdup time capacitor can be minimized without using any auxiliary circuit. Although variable frequency control is used during holdup time, the proposed converter operates with constant frequency under normal operation condition.

3.6 Light load efficiency improvement of isolated ZVS dual boost converter

The proposed converter can achieve ZVS for all the eight switches. And the design is optimizing the RMS current to keep it at a low level during the normal operation mode. So the efficiency [3.8] can be achieved to 94.5% at full load as shown in Figure 3-47.

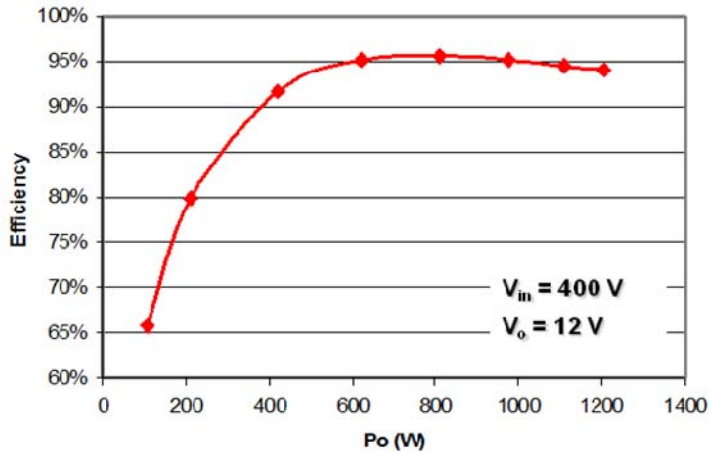

Figure 3-47 Measured efficiency curve w/o improvement

However, the efficiency sharply drops under the light load condition. Only 65.5% efficiency can be remained at 10% of full load. The main reason for the low efficiency is because the primary switches lose ZVS condition. Although the operation mode will not change during the light load which means if ignore the output capacitor of MOSFET, ZVS can be always achieved. But in the real case, this capacitance is about several hundreds pF. Take IRFP460A as an example, the effective C_{oss} is 140pF according to the datasheet [3.9]. The equivalent circuit for the ZVS transition is shown in Figure 3-48. During this period the inductor current discharges the effective C_{oss} to 0V. The energy stored in the inductor should be large enough to complete this process, so the turn off current should satisfy the equation:

$$\frac{1}{2}C_{oss}V^2 \le \frac{1}{2}L\cdot(\frac{1}{2}I)^2$$

Assume the inductance is 38uH, and IRFP460A is used as the primary switches, the turn off current is calculated to be at least 1.536A.

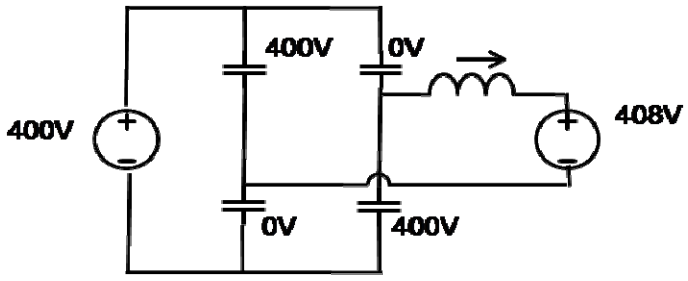

Figure 3-48 equivalent circuit for ZVS transition

The experiment waveforms for converter operating under light load condition are shown in Figure 3-49. It can be clearly observed the turn off current is too small to realized ZVS.

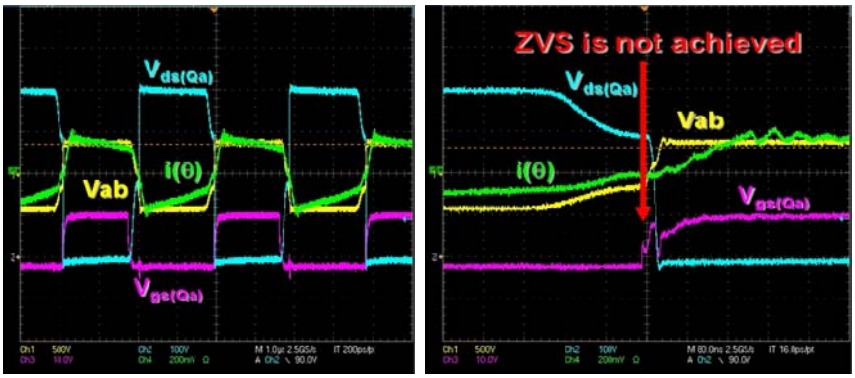

Figure 3-49 experiment waveforms during light load condition

So the strategy is to guarantee the turn off current to be large enough to realize ZVS. In order to reduce the inductor RMS current as the load become light, a skipping time t_D is introduced where the current is keeping zero and both the primary side and the secondary side are shorted as shown in Figure 3-50. Under this control strategy, the current runs a positive cycle and keeps zero for a skipping time t_D determined by the load, and then runs a negative cycle and keeps zero for another skipping time t_D. The skipping time t_D will become longer as the load become lighter. Under this control strategy the turn off current is always kept to a high level during the light load and ZVS can be always guaranteed.

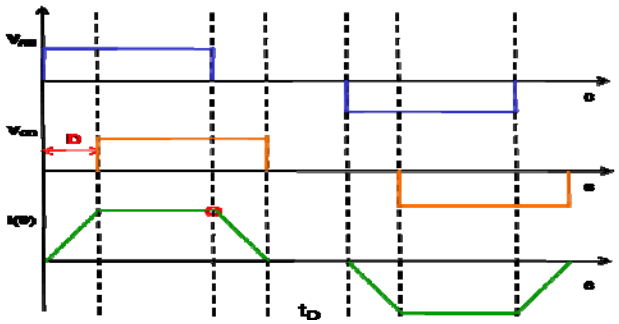

Figure 3-50 pulse skipping concept

To realize the pulse skipping concept, a very simple driving scheme is proposed where only frequency need to be controlled, while the phase shift of primary side switches is automatically adjusted as well as the duty cycle of the secondary side switches. As shown in Figure 3-51, duty cycle of the primary side switches is fixed to be 0.5. T_1 is the delay time from Qa to Qd and is always fixed, where $1/2T_1$ is the maximum switching frequency that happens during the heavy load operation. The secondary switches S1 still have a phase shift to the primary side switches Qa to regulate the output as the same function as in the heavy load, and turns off tighter with Qa. S2 always keep a 180 degree phase delay to S1. Therefore, when switching frequency reduces as the load decrease, phase shift on the primary side is automatically generated and the input side of the inductor is shorted. When the current goes to zero, the secondary side diode is turned off and the current keeps zero as no voltage is applied to the inductor and volt-second is zero during the skipping time t_D.

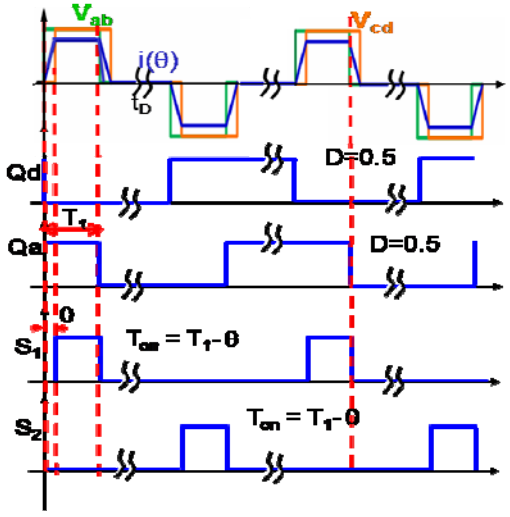

Figure 3-51 light load driving scheme

The control scheme is shown in Figure 3-52. There are two independent control loops. The voltage loop is a fast loop to regulate the output voltage by control the phase shift between the primary side and the secondary side. The current loop controls the switching frequency and is a much slower than the voltage loop so it cannot see the change of the current pulse's shape as the load changes. During the heavy load, the turn off current is larger than the reference current set. So the current loop is saturated that always output the maximum switching frequency as set to be 260kHz in our design. When the load become lighter and the turn off current is becoming smaller than the reference current, the current loop reduces the switching frequency to control the turn off current equal to the reference.

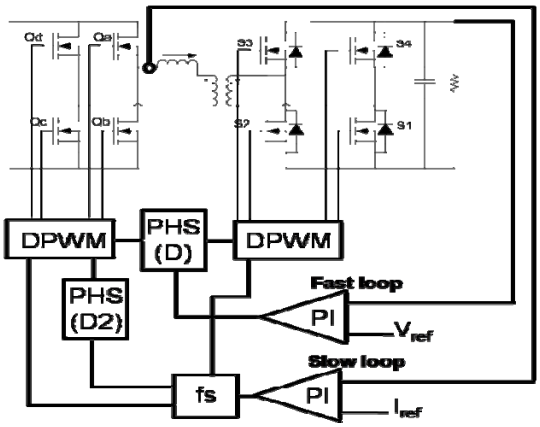

Figure 3-52 light load control scheme

The experiment waveforms are shown in Figure 3-53. The turn off current is kept to about 2A under the light load condition so ZVS can be always maintained. However, this turn off current is only for the top switches while the turn off current for the bottom switches is always zero and ZCS is achieved.

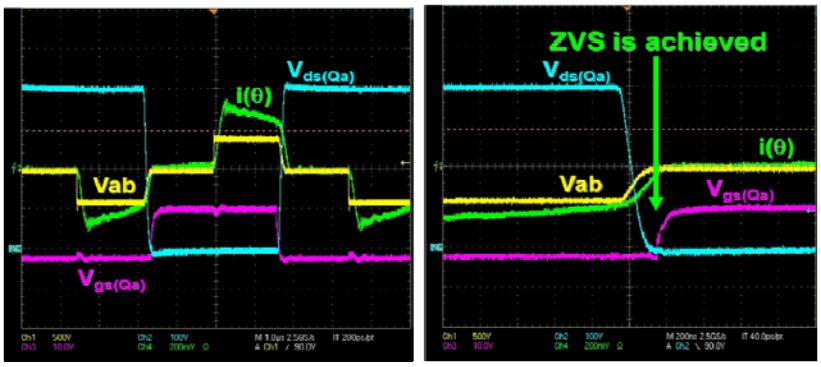

Figure 3-53 experiment waveforms of pulse skipping operation under light load

For MOSFET the switching loss for ZCS is larger than ZVS but still smaller than hard switching. Together with the reduced switching frequency the light load efficiency is improved to 89.5% for 10% load which is about 25% incensement, as shown in Figure 3-54.

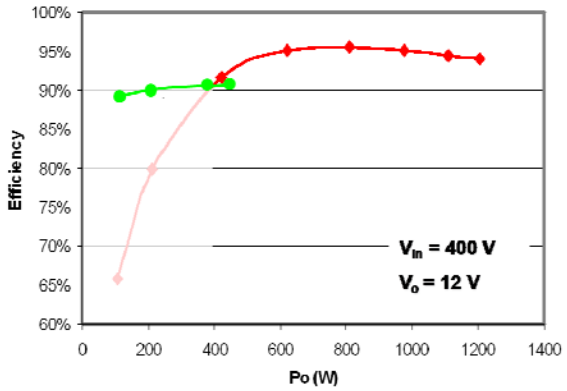

Figure 3-54 light load efficient improvement measurement results

3.7 Current limit operation of isolated ZVS dual boost converter

During the current limit operation, the load current is regulated to an allowed maximum value. The output voltage decreases as the load resistance decreases. Because:

$$I_o = \frac{V_o}{R_L}$$

$$g = \frac{n \cdot V_o}{V_{in}}$$

$$Q = \frac{4 \cdot L}{n^2 \cdot R_L \cdot T_s}$$

The relationship between g and Q can be obtained during the current limit operation where the output current is regulated.

$$g(Q) = \frac{4 \cdot I_o \cdot L}{V_{in} \cdot n \cdot Q \cdot T_s}$$

The gain function can also be written as g(D,Q) that is used to draw the gain curve in Figure 3-38, where D is the phase shift between the primary side and the

secondary side. If D can be always found to satisfy g(Q)=g(D,Q), same phase shift control as used in normal operation can be used to regulate the output current. Proper design of L is required to guarantee D can be found for the whole load range. The smallest inductance can be found under the extreme condition that output is shorted and the phase shift is 0. The key waveform under this condition is shown in Figure 3-55. If assume the input voltage to be 400V, turns ratio to be 34, switching frequency to be 260kHz, and the output current is regulated to 100A, the minimum inductance is calculated to be 32.7uH. From the waveform of i_{S3}, one can find only half of the switching period, the current goes to the load. Thus the peak inductor current for the S3 with be as large as $4I_o$.

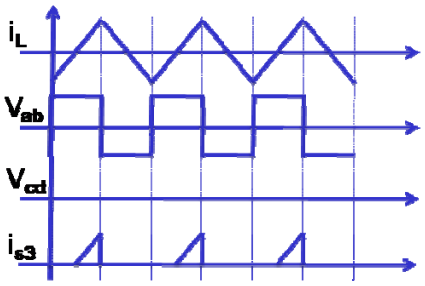

Figure 3-55 key waveforms for 0 phase shift and output short

Larger L can be used to reduce the current stress but will hurt normal operation efficiency. Instead, increase switching frequency together with phase shift control during the current limit mode can also help to reduce the current stress. The best it can do is to reduce the current stress of S3 to $2I_o$, while the switching frequency is increased to 500kHz. But high switching frequency increases the loss during current limit operation. And the thermal will be a

problem. The key waveforms of phase shift control together with frequency control for shorted load case are shown in Figure 3-56.

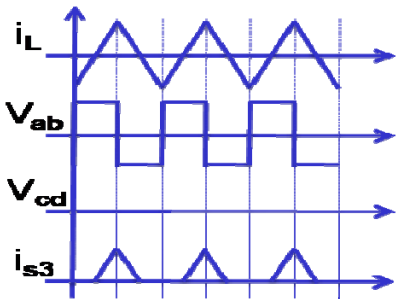

Figure 3-56 key waveforms of current limit operation with phase shift and frequency control for shorted load case

Instead of looking for the solution based on the existing control strategy, another variable, primary phase shift, is introduced to help the current limit operation. With primary side phase shift, current can be well limited as shown in Figure 3-57 for shorted load case.

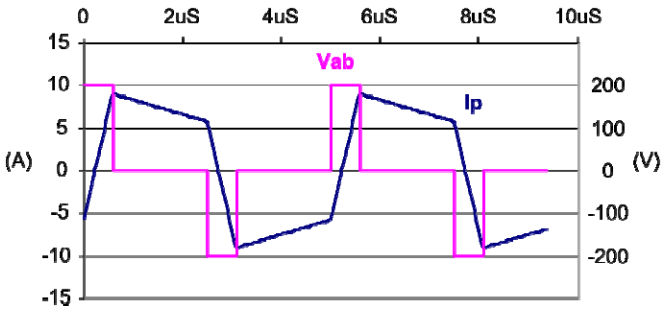

Figure 3-57 waveforms of proposed current limit operation for shorted load case

The control scheme is shown in Figure 3-58. Because either the change of primary phase shift or the change of the phase shift between the primary and the secondary will result the gain variation, a fixed relationship between these two

phase shifts is needed to get rid of one of the free variable. In Figure 3-58, phase shift is used to be the control variable in the current loop and the phase shift between the primary and the secondary changes according to the primary side phase shift.

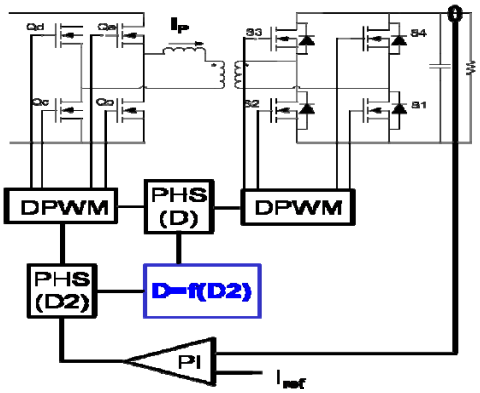

Figure 3-58 control scheme with primary side phase shift for current limit operation

For the normal operation mode, the converter has been designed to be soft-switching and operated under the minimum RMS current, as well as small current stress. For the current limit operation, those benefits are still desired to be kept as shown in Figure 3-59.

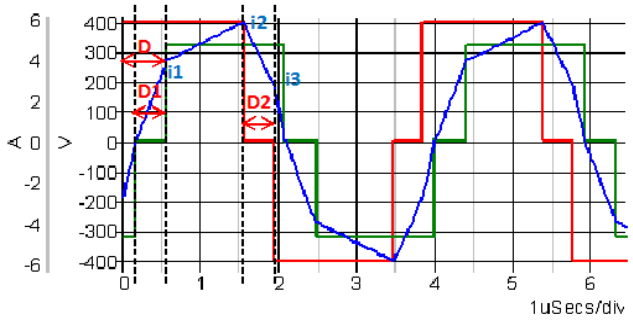

Figure 3-59 desired operation mode for current limit mode

However, if the function D=f(D2) is not proper designed, the circuit will easily run into some unexpected operation modes because the variation of gain is very large during the current limit operation. Arbitrarily choosing D=f(D2) as a constant value as same as the D value under the full load condition will result an unexpected operation mode when R_L is large. Figure 3-60 shows the simulation waveform of this operation mode that the primary side body diodes are hard turn off, which results very large voltage spikes. Arbitrarily choosing D=f(D2) as a constant value of the maximum D will result another unexpected operation mode where the RMS current is very large under the condition that R_L is small.

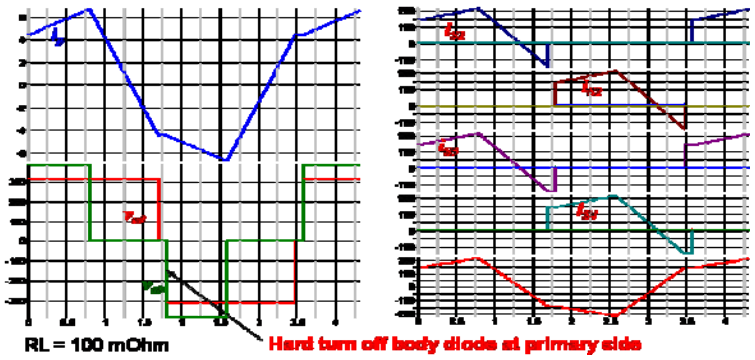

Figure 3-60 simulation result of undesired operation mode I

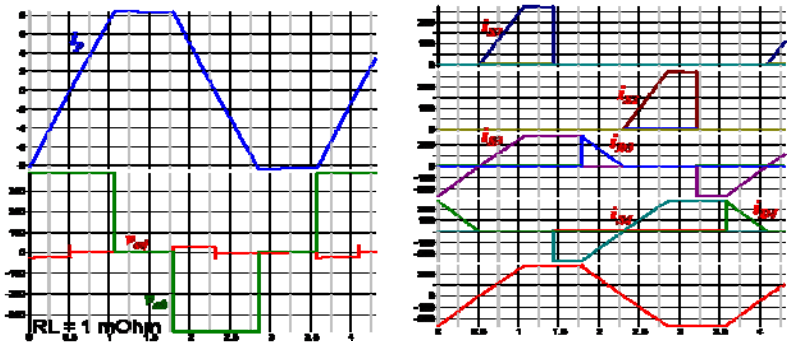

Figure 3-61 simulation result of undesired operation mode II

Therefore, looking for a function D=f(D2) that can guarantee the desired mode is the key for current limit operation. As shown in Figure 3-59, to avoid the mode transition, both i_1 and i_3 should be larger than 0. While in order to guarantee ZVS, i_1 and i_3 should be larger than a minimal value, which is a stronger restriction than the one for no mode transition. On the other word, as long as ZVS can be guaranteed the operation will be restricted to the desired mode. The ZVS boundary equations can be written:

$$i_3 = i_{3critical}$$

$$D1 + (1-g)(1-D-D2) - g \cdot D2 - (1+g)(D-D1) = 0$$

$$(-D2 \cdot D1 + D2 - 1 + 2D - 2D \cdot D1 + D1^2) \cdot g - 4 \cdot D \cdot D1 + 1 + 2 \cdot D1 - D2 + 2 \cdot D \cdot D2$$

$$-2 \cdot D2 \cdot D1 - 2 \cdot D + D1^2 + 2 \cdot D^2 = \frac{4 \cdot I_o}{n \cdot g \cdot Vin} \cdot \frac{L}{Ts} \cdot g$$

D can be solved as a function of D2 and is shown in Figure 3-62 as the red line. In the area below the red line, ZVS can be achieved for all the primary side switches.

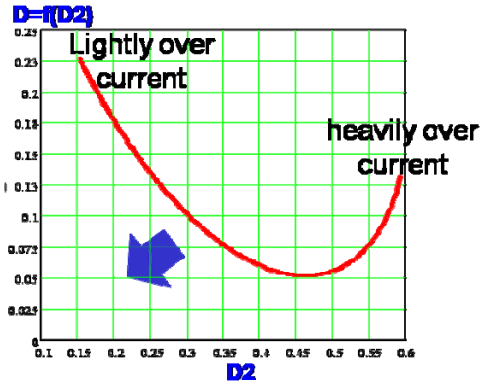

Figure 3-62 primary side ZVS range

The boundary equations for secondary ZVS can be obtained as the same way as of primary ZVS, which can be written as:

$$i_3 = i_{3critical}$$

$$(-D2 \cdot D1 + D2 - 1 + 2D - 2D \cdot D1 + D1^2) \cdot g - 4 \cdot D \cdot D1 + 1 + 2 \cdot D1 - D2 + 2 \cdot D \cdot D2 - 2 \cdot D2 \cdot D1 - 2 \cdot D + D1^2 + 2 \cdot D^2 = \frac{4 \cdot I_o}{n \cdot g \cdot Vin} \cdot \frac{L}{Ts} \cdot g$$

$$D1 + (1-g)(1-D-D2) - g \cdot D2 - (1+g)(D-D1) = 0$$

The boundary D is solved through the equations and is shown in Figure 3-63. In the area above the red line, the converter is able to realize the ZVS for the secondary side.

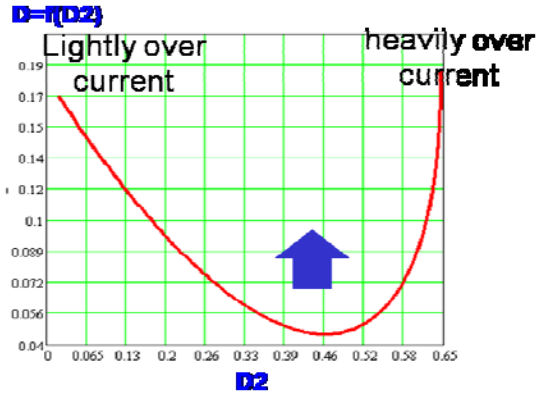

Figure 3-63 secondary side ZVS range

Combining these two boundaries together, the possible range for D is obtained shown in Figure 3-64. As long as the converter operates in the shadow range, the desired operation mode is maintained. ZVS for both the primary side and the secondary side is also guaranteed. Figure 3-65 shows the RMS current range for the whole R_L range. The largest RMS current will happen at shorted load condition and is about 1.3 times of the RMS current under the full load condition.

Figure 3-66 shows the secondary turn off current, where the largest turn off current is as same as the turn off current under the full load condition.

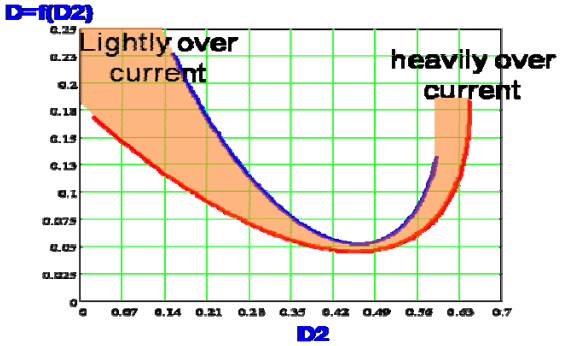

Figure 3-64 desired operation range

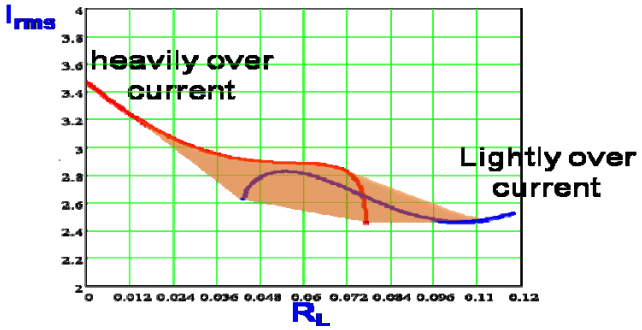

Figure 3-65 RMS current range

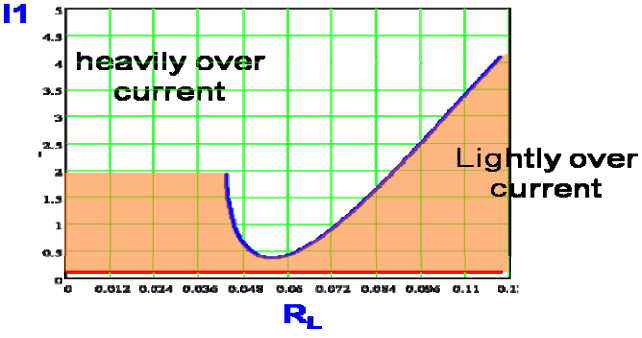

Figure 3-66 secondary turn off current range

Since the expression of a candidate curve is very complex if it is derived from the equations, curve fitting method is introduced to make up a curve for D=f(D2). As shown in Figure 3-67, when D2=0, D is chosen to be the same as the D under the full load condition. When D2=0.45, the shadow has a narrowest part, the center point in that part is chosen for D to eliminate the circuit running into other modes. The point (D2,D) under the shorted load condition is also specified to obtain the smallest RMS current during that load condition. Other point can be accordingly set to smooth the curve during the fitting process. Therefore, the object D function is:

$$f(D2) = 6.2907D2^4 - 5.7128D2^3 + 2.3838D2^2 - 1.003D2 + 0.28$$

as the green curve shown in Figure 3-67.

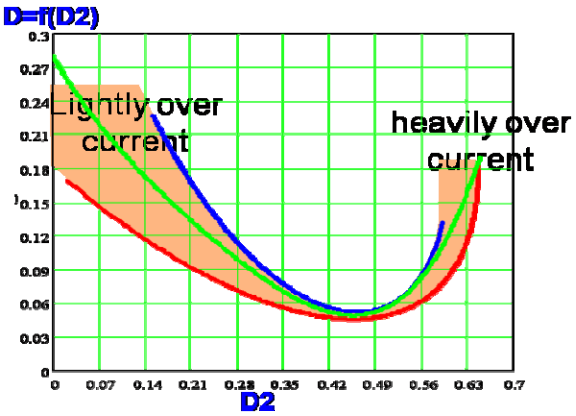

Figure 3-67 design of D=f(D2)

The implementation of this control is through DSP, and the experiment waveform is shown in Figure 3-68, where the input is 200V, output is 1V, and the load current is limited to 50A.

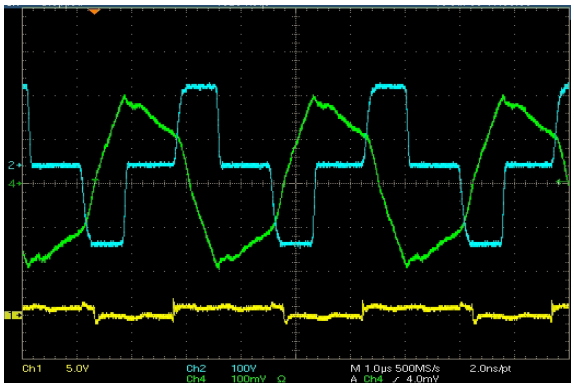

Figure 3-68 experiment waveform of current limit operation

3.8 Comparison with LLC converter

LLC resonant converter is an attractive topology for DC/DC Front-end converter because it is able to achieve wide operation range without sacrificing the efficiency in normal operation condition. During the normal operation, converter operates at its resonant frequency to minimize the conduction loss and switching loss. So high efficiency can be achieved.

A detail comparison between the proposed converter and the LLC converter is listed in Table 3-1 and Table 3-2 for 12V output application and 48V output application, separately.

	DAB	LLC
Primary Switch	IRFP460A	IRFP460A
Primary RMS Current	3.34A	3.8A
Primary conduction loss	6W	7.798W
Primary switching loss	13.52W	5.92W
Inductor	30.72uH	60uH
Capacitor	N/A	10nF (1000V)
Transformer	32:1	32:1:1
Secondary switch	IRF6609 X3	IRL1404ZL X3
Secondary RMS Current	76	79
Secondary conduction loss	17.28W	12.48W
Transformer Loss	18.6W	25.9W
Efficiency	95.6%	95.8%

Table 3-1 comparison with LLC for 12V output application

	DAB	LLC
Primary Switch	IRFP460A	IRFP460A
Rdson	0.27	0.27
Primary RMS Current	6.6875A	7.353A
Primary conduction loss	12.075W	14.598W
Inductor	7.68uH	15uH
Capacitor	N/A	42nF
Transformer	16:1	16:1:1
Secondary switch	IRF6609 X4	IRL1404ZL X1
Rdson	0.002/4	0.003
Secondary RMS Current	76	79
Secondary conduction loss	11.52W	37.45W

Table 3-2 comparison with LLC for 48V output application

3.9 Implementation of singer controller for both PFC and DC/DC stages

Because of the isolation of the DC/DC stage, conventionally, separated controllers are used for the PFC and DC/DC. The controller of PFC is grounded to the primary side of the isolation transformer, sharing the same ground to the sensing signals. The controller of DC/DC is normally at the secondary side of the isolation transformer, sharing the ground of the output signals.

Taking the advantage of digital control, in this novel implementation, only one DSP controller is used for controlling both the PFC and the DC/DC stages.

For PFC, there are totally three signals need to be sensed, which are the input voltage, the inductor current and the output voltage. For DC/DC, there are also three signals need to be sensed, which are the primary inductor current, the output voltage and the load current. Therefore, if placing the DSP controller on the secondary side of the isolation transformer, all the three signals of PFC stage and the primary inductor current information of DC/DC stage need to be sensed isolatedly. If placing the DSP controller on the primary side of the isolation transformer, only two signals, which are the load current and the output voltage of the DC/DC stage, need the isolated sensing. As the result, the controller is arranged at the PFC side.

Because both the load current and the output voltage contain DC bias, transformer cannot be employed as the isolation circuit. Optocoupler can transfer

the DC signal, but due to the processing limit, the tolerance of the component variation is too large to allow it to be used in sensing circuit for any product.

Alternatively, in this implementation, the analog sensing signal is first translated into a PWM signal by comparing with a triangle ramp. Then the PWM signal is isolated transmitted to the DSP through either transformer or the optocoupler. Because the information is carried by the duty cycle of the PWM signal rather than the amplitude, the loss of the sensed information is minimized during the transition. On the receiver side, the DSP monitors the duty cycle of the received PWM signals which represent the sensing information, and combined it with other sensed information to generate the command.

The achieved hardware of the total system is shown in Figure 3-69, where in the red box is the DC/DC part. Taking the advantage of the novel topology and the digital control, high efficiency and high power density are achieved. As shown in Figure 3-54, the efficiency is above 89% from 10% load to full load with 95.5% maximum efficiency. The power density is 22.3W/in^3 with 50% bulk cap reduction.

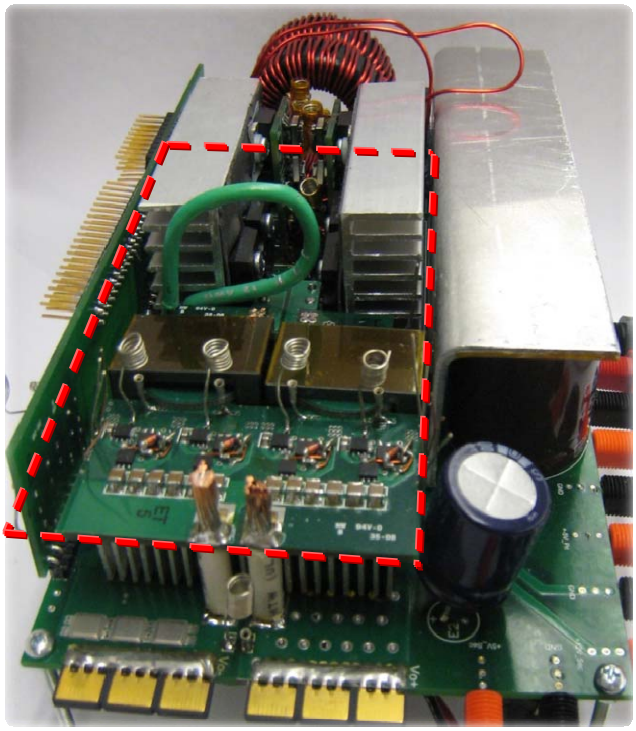

Figure 3-69 achieved hardware

Chapter 4. Summary and Future Work

4.1 Summary

Because of high performance, high reliability, and easy maintainability, distributed power systems (DPS) are widely adopted by telecom and high-end server applications. In recent years, with the development of information technology, demands for power management of telecom and server applications is keep increasing, which provides large market for DPS systems. Recently industry brought out aggressively high efficiency requirements for a wide load range for power management in telecom and computing equipment. High efficiency over a wide load range is now a requirement. On the other hand, power density is still a big challenge for front-end AC/DC converters. For DPS systems, front-end AC/DC converters are under the pressure of continuous increasing power density requirement. Although increasing switching frequency can dramatically reduce the passive component size, its effectiveness is limited by the converter efficiency and thermal management. Technologies to further increase the power density without compromising the efficiency need to be studied.

The industry today is also at the beginning of transferring their design from analog control to full digital control strategy. Although issues are still exist, reducing components count, reducing the development cycle time, increasing the reliability, enhancing the circuit noise immunity and reducing the cost, all of these benefits indicate a great potential of the digital control.

This thesis is focusing on how to improve the efficiency and power density by taking the advantages of the digital control.

In Chapter 2. , a novel π/2 phase shift two Channel interleaving PFC is developed to shrink the EMI filter size while maintain a good efficiency. A sophisticated power management strategy that associates with phase shedding and adaptive phase angle control is also discussed to increase the efficient for the entire load range without compromising the EMI filter size. The method of current sampling is proposed for π/2 phase shift two Channel interleaving PFC and multi-channel adaptive phase angle shift PFC is proposed to accurately extract the average total current information. A noise free current sampling strategy is also proposed that adjusting the sampling edge according to duty cycle information.

In Chapter 3. , an isolated ZVS dual boost converter is proposed, which has similar performance as the LLC resonant converter. It has hold up time extension capability without compromising the normal operation efficiency. It can achieve ZVS for all the switches. Also, the current limit and SR implementation is much easier than LLC. The best operation mode of the isolated ZVS dual boost is discovered through the state plane method, which potentially can be extent to other complex topologies. Light load efficiency is improved by the proposed pulse skipping method to guarantee the ZVS operation meanwhile reduce the switching frequency. Current limit operation is also proposed to restrict a best

operation mode by fully taking the advantage of digital control that precisely control the circuit under the over current condition.

4.2 Future work

In PFC application, the light load efficiency gains increasing attention recently. Phase shedding with adaptive phase angle control is a premising method to increase the PFC light load efficiency without compromising the EMI filter size. However, this method does not allow shedding to one phase, otherwise the EMI filter size suffers.

Burst-Mode operation is widely used in VR application. The basic concept for this method is to avoid light load operation for converters. When the load reduced, the converter switches between active mode and skipping mode to control the output voltage to be the desired value [4.1][4.2][4.3].

Burst mode operation can be employed after the PFC shedding its phases to two. The concept of burst-mode for PFC is the same as for VR application. The circuit switches between active mode and skipping mode from time to time, and the mode-switch criterion is the output voltage hysteresis [4.4][4.5]. The operation of burst-mode control for PFC is shown in Figure 4-1.

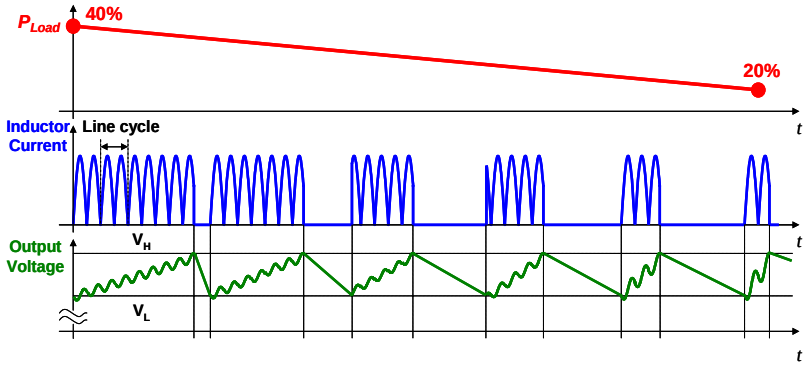

Figure 4-1 Burst-mode operation for PFC

In the digital implementation, normally the sampling frequency is set as high as the switching frequency. The calculation of duty cycle also normally finishes in a switching cycle. The control bandwidth is always designed to be much lower than the switching frequency, so the sampling will not affect the control performance. However, when with an extra high switching frequency, or the calculation is super complex, the calculation may need to be finish for several switching cycle. In the other words, the equivalent sampling frequency is reduced. When the sampling frequency is lower enough, the delay of the control can be easy observed.

A simple way to solve this problem is just to use a faster and more powerful DSP or MCU, but this will increase the cost.

Alternatively, if consider the effect from the sampling when design the compensator, stable loop can still be obtained. Exploring the limit of the sampling frequency will be a very interesting topic.

Dr. Yang Qiu studied the high-frequency modeling for buck converters[4.6], where the switching action introduce the side band effect and through the close loop, large phase drop can be predicted when the control bandwidth is very high or the switching frequency is very low.

The sampling effect is similar to Dr. Yang Qiu's case. Because the sampling frequency is much lower than the switching frequency and is close to the control bandwidth, the power stage can be treat as a linear system, the average model can be used. The effect of switching action can be ignored and the sampler will generate the side band, and affect on the phase and the magnitude through the close loop. Same analysis method can be used as Dr. Yang Qiu did, to predict the phase and the magnitude drops.

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