Three-Dimensional Heterogeneous Integration for RF/Microwave Applications

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(ABSTRACT)

High performance RF/mixed signal systems require new interconnect strategies to combine high frequency (microwave/mm-wave) circuitry with silicon mixed-signal and baseband digital processing. In such systems, heterogeneous vertical integration, in which circuits in different technologies can be stacked on top of each other within the system architecture, can reduce the overall system size and power consumption. Chip stacking also enables optimally-performing heterogeneous systems, because each level of the stack can consist of components fabricated in their most suited device or substrate technology. Two novel approaches for the vertical interconnection of heterogeneous integrated systems are proposed in this work. These approaches are related to flip-chip bonding techniques used in Radio-Frequency (RF)/microwave integrated circuits.

The first proposed approach involves an interlocking mechanical structure that supports flip-chip assembled Monolithic Microwave Integrated Circuits (MMICs). Photolithographically patterned thick-film SU-8 structures are applied to both the chip and the carrier such that the chip self-aligns into place and mates with the carrier. Gold bumps embedded within the structures electrically connect the chip pads to the carrier pads. This method is demonstrated through the assembly of a SiGe power amplifier MMIC onto a high resistivity silicon carrier.

The second proposed approach involves vertical interconnects consisting of room temperature liquid-state metals. The fluid nature of the liquid bumps allows them to be robust in the presence of thermo-mechanical stresses, such as Coefficient of Thermal Expansion (CTE) mismatch between the interconnected chips. SU-8 structures are used to form a shaping mold on the bottom carrier that contains the liquid metal. Gold posts are electroplated on the top chip, then mated with the SU-8 mold, thereby making contact with the liquid metal to form the electrical continuity.

For each of these proposed methods, design and fabrication considerations are discussed in detail. RF measurements on prototype structures up to Ka band are per-

formed to verify the functionality of the proposed methods. Given the results of these proof-of-concept efforts, electrical characteristics of the materials used in these methods are determined, and recommendations are provided for future improvements and refinements to these two techniques.

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Chapter 1

Introduction

The packaging of devices and components plays a significant role in the performance of an electronic system. Traditionally, the ability to create highly integrated electronic systems that incorporate various functional blocks requires advances in packaging. Packaging ensures that different blocks, particularly those fabricated in different substrate materials, can function optimally in the desired system environment. As electronic systems push towards millimeter-wave frequencies (30-300 GHz) to meet emerging military and commercial applications, the demand for high performance packaging strategies has become even greater. The millimeter wave spectrum opens up many new technological applications: automotive radar, remote sensing, wideband terrestrial and satellite communications, and high-resolution non-optical imaging [2]. Effective packaging allows high frequency components, such as antennas, amplifiers, frequency converters, and high-Q passives, to be intimately integrated with mixed-signal baseband and digital signal processing circuitry in a compact system implementation. A block diagram of such components in a simple heterodyne transceiver is shown in Figure 1.1. It should be noted that high resistivity silicon is progressively being used as an insulating substrate instead of traditional compound semiconductors in order to support high density integration.

Traditional packaging strategies in the microwave/mm-wave regime have been based on two-dimensional board-level or module integration. On the other hand, the integration strategies demonstrated in this work exploit the third dimension through multi-chip stacking. Chip stacking allows for higher density systems with intercon-

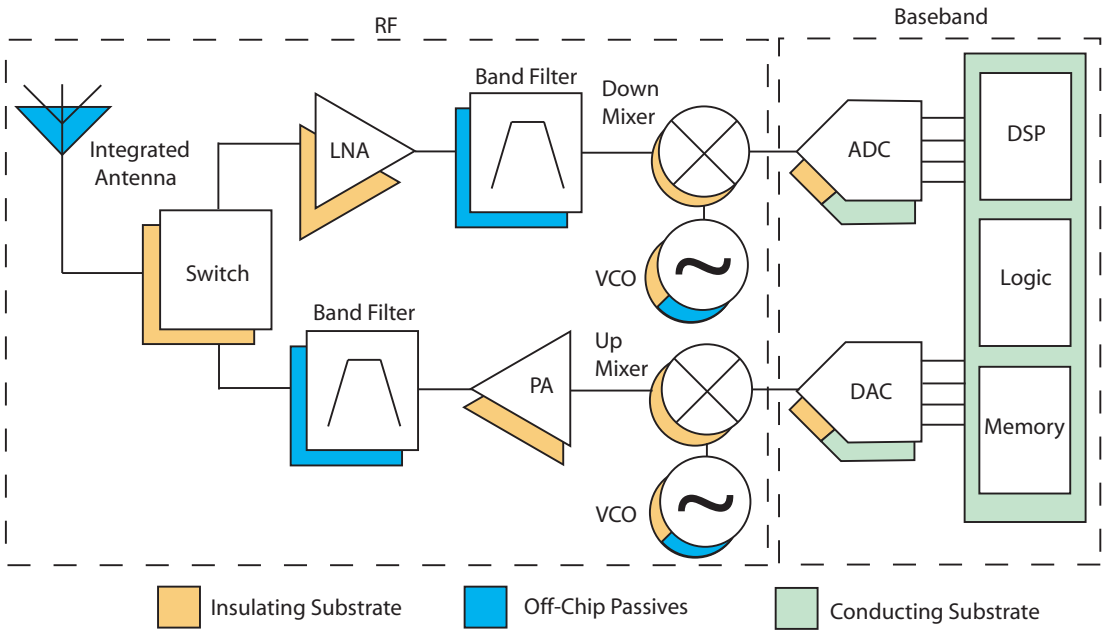


Figure 1.1: Heterodyne transceiver diagram showing RF and baseband system components. Colors show the distinctions in component technology.

nects that are more compact and require less driving power due to their short, vertical path lengths [3]. Figure 1.2 shows the difference in interconnect length between stacked 3-D systems and planar 2-D systems.

As an example, cell phones have been reduced considerably in size with the introduction of monolithic System On Chip (SoC) integration approaches that combine RF and baseband circuitry in a single chip. However, the need for additional functionality, such as multi-band, multi-mode operation with WLAN and video, has created the need for high-density stacked integration due to more extensive filtering, processing and memory requirements. This has led to the stacking of standard components vertically within a system. These stacked configurations not only benefit from high-density, low power interconnects, but the use of commodity components reduces cost and design time over embedded cores [4].

The advantage of using multiple technologies in the realization of an integrated system is that optimal performance can be achieved through the use of the optimal technology for each component. For example, RF components have traditionally been fabricated in III-V semiconductor technologies, such as GaAs, due to their semi-insulating nature. On the other hand, the low resistivity of CMOS silicon technologies causes

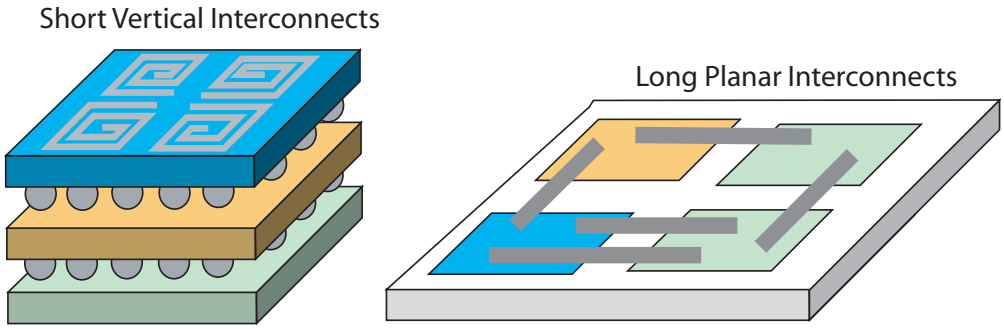


Figure 1.2: Stacked components with short, vertical interconnects vs. planar components with long interconnects

significant loss in RF circuits and low Q in on-chip passive components. This division between RF high-resistivity circuitry and baseband CMOS circuitry is shown in Figure 1.1. While SiGe and RF CMOS circuits are expanding the frequency range of silicon technologies into the microwave and mm-wave regime, the additional design and fabrication costs of integrating the high frequency components with the digital CMOS components with sufficient isolation in an integrated silicon system is an incentive for pursuing mixed, or heterogeneous, technology systems. In addition, the passive components that form filters, antennas, and tuning and matching networks are often optimized off-chip. Due to the three-dimensional nature of carrier-embedded passive structures, off-chip passives have at least an order of magnitude better Q factor than planar on-chip passives and do not occupy expensive semiconductor wafer area [5]. For these reasons, high-performance-oriented integrated systems generally exhibit some degree of heterogeneous integration.

Combining heterogeneous technologies in a chip stacking approach adopts the qualities of both high performance and small size in integrated systems. However, this presents a new set of challenges in terms of fabrication, electrical performance, thermal management, and mechanical stability from those of traditional two-dimensional integrated systems.

1.1 Scope of Thesis Work

This work focuses on vertical interconnections that carry RF signals between stacked chips in a heterogeneous integrated system. These interconnects are intended for microwave/millimeter-wave operation at Ka band (40 GHz and beyond). The design, structural and material considerations, fabrication, and electrical testing of two novel proof-of-concept approaches for vertical interconnects are discussed. The first approach involves an interlocking structural support mechanism that allows Monolithic Microwave Integrated Circuits (MMICs) to be assembled in a self-aligning, low-cost process referred to as the Mechanical Fit approach. The second approach, referred to as Liquid Metal Interconnect, involves using low melting point metals as flexible vertical interconnects that are more resistant to failure due to thermomechanically-induced stress. The development of these vertical interconnects involves novel processing and assembly techniques. Microwave and millimeter-wave measurements are performed to evaluate the electrical performance of these interconnect strategies.

While the vertical interconnects are the focus of this work, the context of their assembly within an integrated system must also be discussed. In this case, the vertical interconnects mate with standard planar transmission lines used on MMICs. Therefore, an introduction to both transmission line topologies and the integrated system architecture are included.

1.2 Organization of Thesis

This thesis explores the vertical integration of microwave/millimeter-wave electronic systems and the interconnection strategies that link diverse system blocks. This thesis consists of eight chapters.

Chapters 2-4 introduce integration technologies for microwave/millimeter-wave integrated systems. Chapter 2 discusses the different options for realizing integrated systems, both monolithic and heterogeneous. Vertically integrated systems are the focus of this chapter as they are the target of the proposed interconnect research. Chapter 3 discusses planar waveguides and transmission lines that carry RF signals on the chip level. Specifically, design considerations for coplanar waveguide (CPW)

implementation are included; CPW is used as the chip level transmission line structure throughout this work. Chapter 4 discusses chip assembly and alternative vertical interconnect approaches. The assembly of the approaches introduced by this thesis emphasize the use of flip-chip bonding.

Chapter 5 discusses the fabrication techniques and materials that enable the vertical integration strategies used in this work.

Chapter 6 presents the work on Mechanical Fit, an interlocking mechanical structure for flip-chip assembly of MMICs. This structure is demonstrated through the assembly of a SiGe power amplifier. Chapter 7 presents the work on Liquid Metal Interconnects including the design, fabrication, and testing of the liquid metal vertical transition.

Finally, the thesis is concluded in Chapter 8 with a brief summary of accomplishments and a discussion of future research directions.

Chapter 2

Electronic System Configurations

This chapter highlights the evolution of electronic system integration from traditional, single-level Multi-Chip Modules to high-density, multi-level System-on-Package architectures. The size and power consumption benefits of vertical integration are emphasized as they are motivating factors for this research. Also, the advantages of both monolithic and heterogeneous system integration approaches will be discussed.

Key parameters of electronic system integration are electrical performance, mechanical stability over temperature variations, size, and cost. The most common strategy for reducing cost and in many cases, improving performance, is to combine several system components into the same package or module. This is becoming an increasingly complicated task because modern electronic systems integrate active devices, passive components, Micro-Electro-Mechanical Systems (MEMS), optoelectronics, antenna arrays, etc.

2.1 Introduction

Traditional system integration followed board-level design approaches in which all of the components were mounted on a single two-dimensional plane. The development of Multi-Chip Module (MCM) integration reduced the parasitic packaging effects of individual chips by mounting bare die, along with miniaturized discrete passives, onto a common carrier that would be subsequently bonded within a single package. In or-

der to further miniaturize and reduce the parasitic effects of MCM integration, the System-on-Chip (SoC) integration approach was developed, in which all of the system components are fabricated within the same substrate technology. This further reduces the length of system level interconnects compared to MCMs as all functions are fabricated on-chip. This monolithic approach has been instrumental in the miniaturization of wireless devices, with RF circuitry, baseband processing, data conversion, signal processing, and cache memory within the same chip.

As performance requirements became more stringent, two-dimensional miniaturization transitioned into three-dimensional stacking. In RF systems, the 2-D monolithic approach bounds the performance of some components, particularly passives and RF components traditionally fabricated in compound semiconductors. This has led to the vertically-oriented System-in-Package integration approach, with shorter interconnects linking heterogeneous system components.

This chapter presents these different approaches to system integration, as well as introducing an emerging technology, System-on-Package, that combines the strengths of the other techniques previously mentioned.

2.2 Multi-Chip Module

MCM packaging allows each component to be fabricated in its optimal technology and then combines the components on a common substrate. For example, RF power amplifier circuits could be designed in GaAs or SiGe HBT technology, mixed signal and digital logic circuits designed in silicon CMOS, and passives in high performance surface-mount technology (as opposed to on-chip planar devices). Typical MCM carrier substrate materials include Low Temperature Co-fired Ceramic (LTCC), alumina, etc. This heterogeneous approach requires more complicated post-fabrication steps than an SoC, but does not suffer as significantly from parasitic substrate modes and cross-coupling between noisy digital circuitry and sensitive RF circuitry. However, the size of the system is quite large in the two dimensional plane due to the long, lateral interconnects between components on separate chips. Figure 2.1 shows typical MCM technology including surface-mount passives, wirebonded ICs, and embedded lateral interconnects.

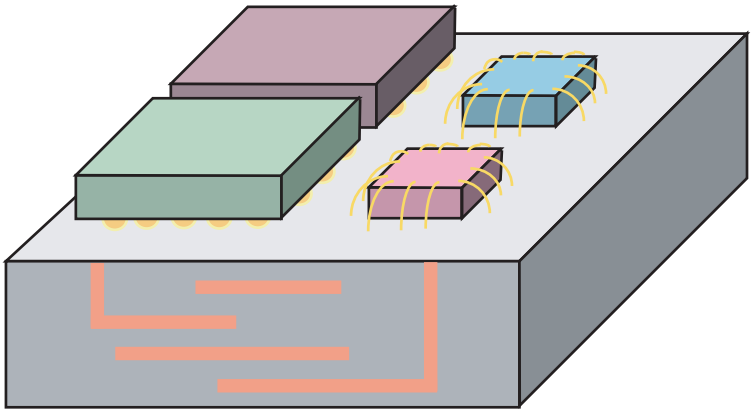


Figure 2.1: Multi-Chip Module

2.3 System-on-Chip

SoCs are fabricated in a single semiconductor IC technology, typically silicon CMOS or BiCMOS, on the same substrate as shown in Figure 2.2. This simplifies the integration process and allows intellectual property (IP) cores from standard silicon IC designs to be re-used to shorten design time; however, interconnection and routing between blocks on-chip can become complex, tending to increase design times in layout and verification [6]. No multi-chip assembly is necessary in SoC systems, which subsequently reduces the overall system size. This leads to SoC systems being the most compact and lightweight, and readily produced in high volume. Some of the shortcomings of the SoC approach are that a homogeneous technology may not be optimum for all of the individual component blocks' performance, and that electrical and thermal coupling between components can become a limiting factor [5]. Passive component performance, in particular, is sacrificed in silicon SoCs. In on-chip silicon, inductors generally have an order of magnitude lower Q factor than off-chip inductors and occupy valuable semiconductor area. Also, parasitic substrate modes and cross-coupling between noisy digital circuitry and sensitive RF circuitry become prevalent in SoC systems.

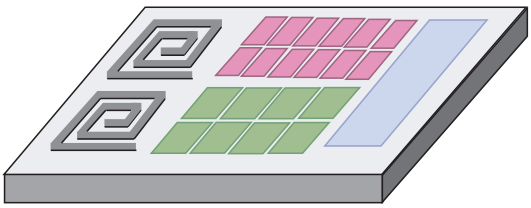


Figure 2.2: System-on-Chip

2.4 System-in-Package

System-in-Package progresses beyond the two dimensional framework of SoC and MCM technology to exploit the vertical dimension [3]. SiP stacks each component IC of the system vertically, minimizing the lateral area of the system as shown in Figure 2.3. The high density of SiP technology allows the vertical connections between components to be shorter than a lateral system such as SoC, mitigating the performance-compromising parasitics associated with long global wires [7]. The challenges of SiP technology include isolating adjacent levels, both thermally and electromagnetically, heat sinking through the stack, and mechanical reliability of the interconnects between the components. SiP can be optimized through new processing developments such as through-substrate vias (TSV) that allow electrical connection across the chip area through multiple levels of the stack. TSVs will be discussed further in Chapter 5. The International Technology Roadmap for Semiconductors predicts that stacks of high performance die will be 5 levels tall (14 levels tall for low cost Si die) by 2015 [8].

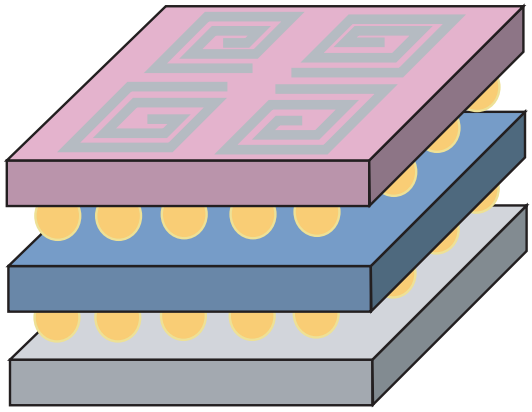


Figure 2.3: System-in-Package

2.5 System-on-Package

SoP is a packaging concept introduced by researchers at the Georgia Institute of Technology that seeks to leverage the advantages of each of the three previous system styles [9]. In an SoP configuration, each component of the system is fabricated and integrated in the most appropriate way to optimize the overall system performance. A carrier substrate is used to combine highly integrated SoC subsystems with three dimensional SiP stacks, while passives are fabricated in the carrier substrate itself to enhance their quality factor (similar to MCM)[10]; this configuration is shown in Figure 2.4. In an SoP RF front-end, the analog components, such as the power amplifier, low-noise amplifier, up and down conversion mixers, and voltage-controlled oscillator, are typically integrated in a high performance SoC, with the digital logic and memory in SiP stacks and the passives embedded within the carrier substrate.

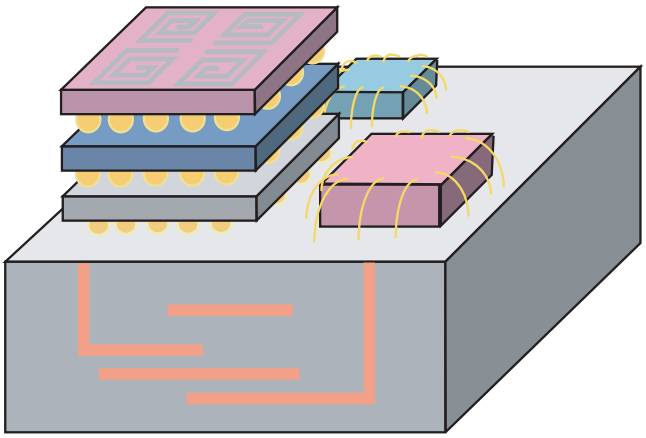


Figure 2.4: System-on-Package

2.6 Summary

The above integration technologies represent an evolution of research and development to increase efficiency in terms of size, electrical and mechanical performance, and cost. The design trade-offs of these integration technologies are summarized in Table 3.1.

Table 2.1: Summary of System Integration Implementations.

Integration	SoC	MCM	SiP	SoP
Size	Small	Large	Medium	Medium
Heterogeneous	No	Yes	Yes	Yes
Interconnect Length	Long on chip	Long on carrier	Short	Short
Optimized Passives	No	Yes	No	Yes
Component Coupling	High	Low	Medium	Medium
Design Time/Cost	High	Low	Medium	High

The work in this thesis is based on vertical stacking strategies that are best suited for use in SiP and SoP technologies. A critical consideration when adapting these integration technologies to the microwave/mm-wave regime is that the interconnects must function as low-loss electromagnetic waveguides, while maintaining high mechanical stability. In order to emphasize the transition from on-chip planar interconnects to off-chip vertical interconnects, an introduction to chip level waveguides and transmission lines is given in the next chapter.

Chapter 3

Integrated Waveguides and Transmission Lines

Waveguides and transmission lines are used to propagate high frequency signals in microwave/millimeter-wave systems. Planar waveguides, as discussed in this chapter, are fabricated at the chip level to connect the transistors and other elements within a MMIC. In order to develop vertical RF interconnects, it is necessary to understand the interconnects at the MMIC level to frame the design considerations for vertical transitions between planar transmission lines. This chapter introduces several popular 2-D integrated waveguides and then focuses on the type used throughout this work: coplanar waveguide (CPW).

3.1 Introduction

The distinction between the interconnects of RF systems and those of baseband and digital systems is that the wavelengths of the transmitted signals approach the dimensions of the interconnect. Wavelengths on the order of millimeters (chip scale) require the use of distributed elements (transmission lines) for intra-chip connections. Signal propagation is therefore dependent on the dielectrics and metallization schemes used within the chip and the package [11]. In a microwave/mm-wave system, the electrical performance can be determined by how well the traveling electromagnetic fields or waves propagate in the transmission media. For example, the wavelength of a guided

wave, λ_g, relative to the wavelength of the same wave traveling in vacuum, λ_0, is determined by the effective dielectric constant, ϵ_{eff}, of the waveguide, given by:

$$\lambda_g = \frac{\lambda_0}{\sqrt{\epsilon_{eff}}} \tag{3.1}$$

The effective dielectric constant is the ratio of the propagation speed of electric fields in a given medium compared to vacuum.

The effectiveness of transmission lines and waveguides can be specified by parameters such as return loss, insertion loss, and power handling capability. Return loss is a measure of the incident power reflected back from the input port as a result of improper impedance matching between the port and the preceding part of the system given by

$$\text{Return Loss} = -10 \cdot \log\left(\frac{P_R}{P_I}\right) \tag{3.2}$$

where P_R is the power reflected from the power and P_I is the total power introduced to the port. Ideally, a transmission line whose characteristic impedance Z_0 perfectly matches the port impedances will not reflect any power, and therefore will have no return loss (-∞ in dB)[12]. Insertion loss is a measure of the power transmitted from one port of the system to a different port given by

$$\text{Insertion Loss} = -10 \cdot \log\left(\frac{P_T}{P_I}\right) = -10 \cdot \log\left(1 - \frac{P_R + P_L}{P_I}\right) \tag{3.3}$$

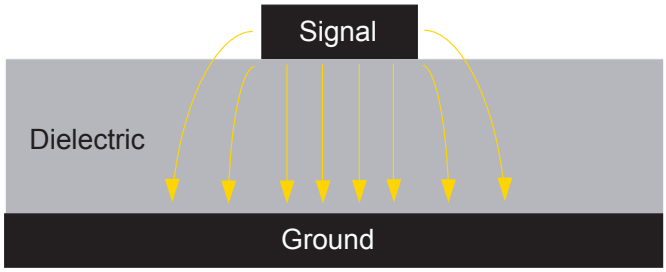
where P_T is the power transmitted through the system to the load and P_L is the power dissipated within the system. From 3.3, it is clear that insertion loss is a representative measure of both reflection effects, and the quality of the transmission line conductors and dielectric medium. Transmission lines should ideally have low insertion loss (close to 0 dB) meaning that most of the incident power from the input is transferred to the output. These loss considerations are discussed in the following section in terms of commonly used MMIC transmission lines.

3.2 Integrated System Waveguides and Transmission Lines

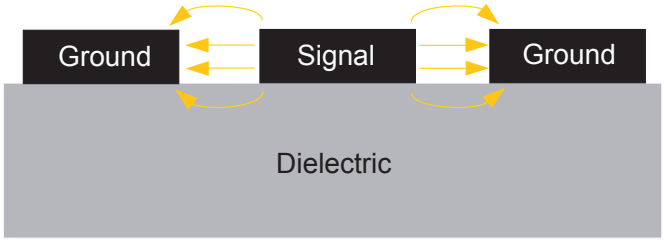
The main issues associated with microwave/mm-wave integration are the interconnect dimensions relative to the desired wavelengths, the radiation and cross-talk between nearby interconnects, and the power handling capability of the interconnects. The fabrication limits of the interconnect dimensions determine the frequency range that can be propagated through a integrated waveguide since larger dimensions increase the effective resistance, inductance, and capacitance and therefore reduce the upper frequency limit. In order to reduce cross-talk between adjacent transmission lines, the separation between the lines can be increased to reduce coupling as well as return path (ground) conductors can be brought closer to the signal conductor to concentrate the electromagnetic fields in the conductor gap. From a power handling standpoint, the breakdown voltage of the dielectric determines the maximum electric field that the line can support. While air has a lower permittivity than polymer and semiconductor dielectrics, its low dielectric strength limits its power handling capability. Therefore, high power transmission lines typically avoid air-filled dielectrics.

3.2.1 Planar Waveguides and Transmission Lines

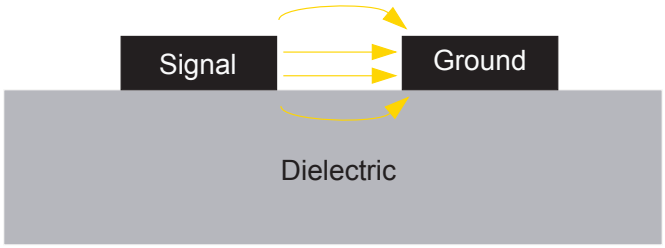
In typical MMIC technologies, only Micro-strip (Fig. 3.1(a)), Coplanar Waveguide (Fig. 3.1(b)) and Coplanar Stripline (Fig. 3.1(c)) are commonly used due to the available metal layers and thin Inter-Metal Dielectric (IMD) layers. The key difference between these structures is the relationship between the signal conductor and the ground planes that confine the traveling wave. Microstrip lines consist of a signal conductor on top of the dielectric substrate and a single ground plane on the bottom side. Coplanar waveguide (CPW) consists of a signal conductor with ground plane traces on either side, all on the top of the dielectric substrate. The dual of CPW is the Coplanar Stripline (CPS) which consists of a pair of differential traces on the top level of the substrate separated by a fixed width [13]. Since there are multiple dielectrics in each of these planar transmission lines, they do not support pure transverse electromagnetic (TEM) wave modes.



(a) Microstrip



(b) Coplanar Waveguide

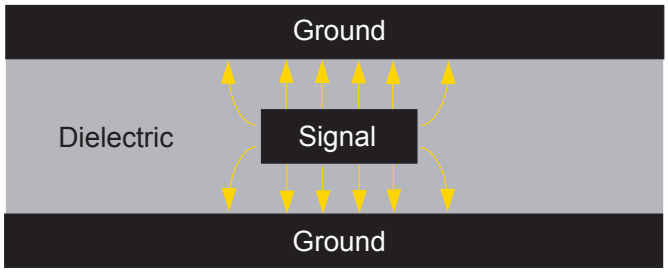


(c) Coplanar Stripline

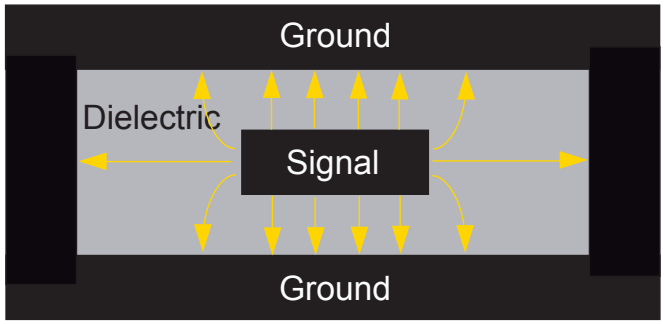
Figure 3.1: Planar Waveguides and Transmission Lines

3.2.2 Three-Dimensional Waveguides and Transmission Lines

Multilayer (3-D) fabrication techniques allow high performance TEM transmission lines to be created. These three-dimensional transmission lines include Stripline (Fig. 3.3) and Micro-Coaxial (Fig. 3.4). Stripline lines consist of a signal conductor sandwiched inside of a dielectric with ground planes above and below. Micro-coaxial lines consist of a suspended signal conductor surround on all sides by uniform dielectric and ground conductor. The need for at least three metal layers to construct these transmission lines generally limits their use to carrier-level integration (such as LTCC discussed in Chapter 5) where multiple layers are readily available. However in advanced IC technologies with multiple back-end metal layers, such structures can also be realized.



(a) Stripline



(b) Micro-Coaxial

Figure 3.2: Three-Dimensional Waveguides and Transmission Lines

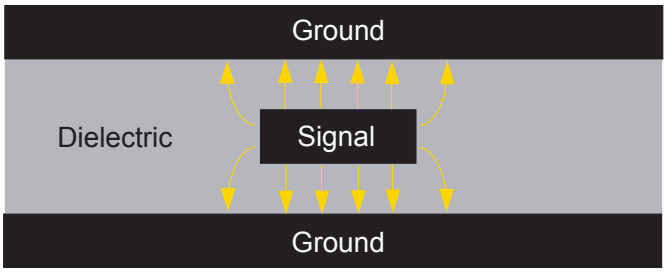


Figure 3.3: Stripline

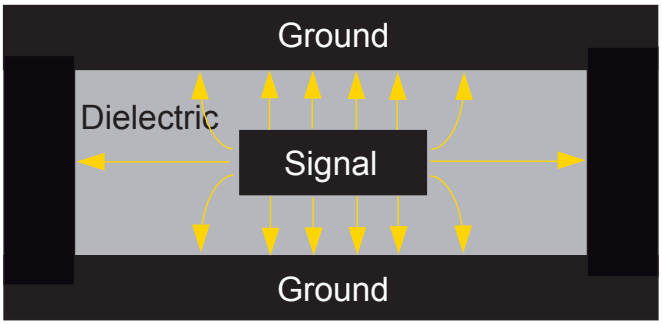


Figure 3.4: Micro-coaxial

3.2.3 Discussion

The choice of transmission line to be used in a given integration design is dependent on the trade-off between fabrication simplicity and performance.

From the fabrication standpoint, CPW and CPS are generally the easiest to fabricate in that both the signal and ground traces are on the same side of the substrate and therefore only require a single metal layer. This simplifies photolithography as well as direct bonding to those traces. Microstrip is slightly more difficult because, even though the topside signal traces can be patterned photolithographically, two metal layers are required and vias must be used to bring all of the conductors to the same plane for bonding. The additional metal layers required for Stripline and Micro-coaxial are generally prohibitive on the MMIC level; however high performance carrier level transmission lines are being developed through multiple layer stacking processes [14][15] that will be further discussed in Chapter 5. It is worth noting that the characteristic impedance of each of these lines can be changed through the geometrical dimensions of the conductors and dielectrics [12].

From the performance standpoint, micro-coaxial and stripline offer the best performance through their ability to support pure TEM wave modes. This means that these lines can support higher frequency operation without dispersion. Dispersion is a distortion effect in which the phase velocity of a signal changes with respect to frequency. Also, the strict wave confinement of the three-dimensional lines enhances their resistance to environmental radiation and cross-talk from nearby integrated devices. On the other hand, the exposure of the wave to multiple dielectric media, as is the case with microstrip, CPW and CPS, leads to non-TEM propagation and dispersion since waves travel at different speeds in different dielectrics.

The loss and isolation of microstrip, CPW, and CPS lines is determined by the proximity of signal to ground conductors. In microstrip, the wave primarily travels within the substrate, but with some fields above in the air. Therefore, it is critical for the substrate to have a high resistivity to prevent attenuation. Microstrip is also more susceptible to radiation noise since the signal trace is generally farther away from the ground plane. Surface wave radiation effects become more significant as dielectric constant increases. Since CPW lines are closer together on the same side of the substrate, more of the wave travels through the air (for CPW traces on the MMIC surface) in between the signal and ground traces compared to microstrip. This makes CPW less dependent on the substrate material and therefore less dispersive than microstrip. However, the effective dielectric constant is lower, so the line is longer per wavelength, adding size and attenuation. However, the close proximity of the ground traces helps isolate the wave from radiation effects.

As a balance between performance and fabrication simplicity, CPW is primarily used in this work; a more thorough discussion is given in the next section.

3.3 Coplanar Waveguide

As previously discussed, CPW transmission lines have the following qualities that make them desirable for this application:

- simplified fabrication due the signal and ground conductors on the same substrate surface, eliminating the need for through-substrate vias;

- reduced susceptibility to dispersion and interfering radiation compared to microstrip, allowing quasi-TEM operation into the millimeter-wave regime;
- ease of integration of active devices;
- common millimeter-wave on-wafer test probes are in Ground-Signal-Ground (GSG) orientation for easily measuring CPW-like structures; and,
- the characteristic impedance can be set by changing either the signal conductor width or the gap separation between signal and ground conductors, adding a second degree of freedom over microstrip.

Each of these features will be discussed further in the following sections.

3.3.1 Coplanar Waveguide Fabrication

In practice, there are two strategies for fabricating low-loss CPW interconnects: directly on top of low-loss III-V substrates or on top of dielectric layers above lossy Si substrates as shown in Figure 3.5. In MMIC design, CPW conductors can be placed directly on low-loss III-V substrates, significantly reducing fabrication cost by reducing the number of additional layers and masks. In Si RFIC design, additional dielectric layers (and often bottom ground planes) are needed to prevent unwanted signal attenuation in the low-resistivity substrate.

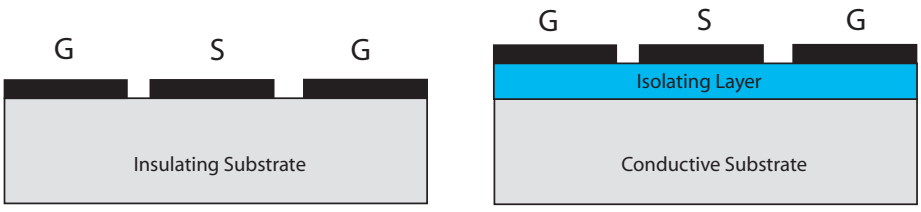


Figure 3.5: Cross-section comparison of CPW directly on an insulating substrate vs. on a isolating barrier on top of a lossy substrate

3.3.2 Dispersion and Isolation of Coplanar Waveguide

Dispersion in CPW lines can be reduced by using smaller gap widths, confining more of the fields in the gaps between conductors. The trade-off is that the reduced gaps lead to higher attenuation because the current travels closer to the conductor edge, effectively increasing the conductor resistance.

Since the signal line is on the same plane as the ground planes, traces can be routed close together with higher isolation than microstrip. This allows for compact differential signaling. Differential (balanced) topologies contain two symmetric traces (GSGSG) carrying currents of equal magnitude that are 180° out of phase; the transmitted signal is effectively the difference of the currents. Differential signals are less susceptible to cross-talk and common-mode noise. On the other hand, single-ended topologies contain a single trace (GSG) where the transmitted signal is relative to the fixed ground traces.

3.3.3 Active Device Integration and On-wafer Probing

The ability to easily integrate active devices and probe on-wafer structures are a result of the CPW conductors being on the same dielectric surface. Active devices can be connected directly to CPW conductors because the signal and ground contacts are on the same plane. Other integrated transmission lines require transition vias to make the necessary connections to active devices, adding complexity to the integration.

Likewise, on-wafer probing of CPW components is easy due to the conductors being on the same surface. The ability to measure RF components on-wafer provides accurate component performance assessment without having to package the component with connectorized input and output ports. This is accomplished using microwave probes that establish the signal and ground configurations (GSG for single ended, GSGSG for differential) for each port to be measured. Coplanar probes can be used to make on-wafer measurements on circuits up to W-band and beyond. A picture of coplanar probes on both ends of a CPW line is shown in Figure 3.6. It should be noted that other planar transmission lines (microstrip etc.) must include a transition to CPW in order to make coplanar on-wafer measurements.

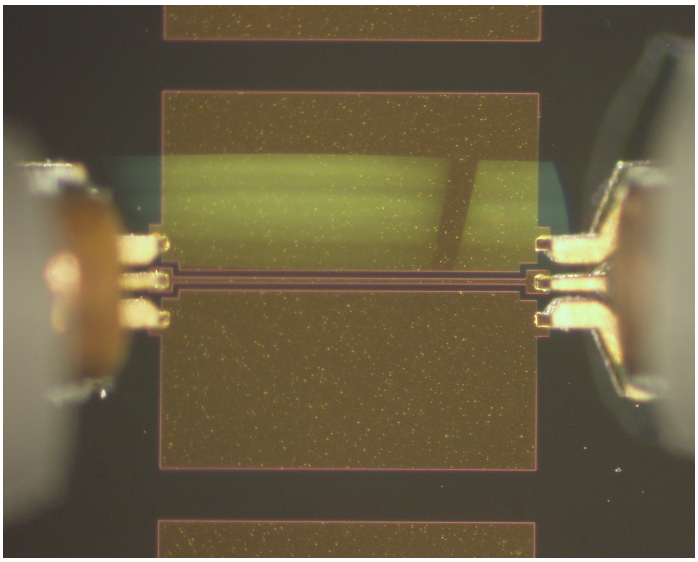


Figure 3.6: Coplanar Waveguide with GSG probes on both ports

3.3.4 Characteristic Impedance of Coplanar Waveguide

In order to prevent reflections within the system, it is important to properly match the impedance of cascaded components. Assuming the substrate permittivity and thickness are set by the technology, the characteristic impedance of a CPW line can be modified by changing either the signal conductor width or the signal-ground gap width as will be shown in the following discussion.

Assuming the materials and geometry have little effect on the magnetic permeability μ of the line, the characteristic impedance Z_0 can be determined from the baseline capacitance of the line C (calculated using ϵ_0) and the effective permittivity ϵ_{eff} of the combination of the dielectrics above and below the conductors. As such, the characteristic impedance is given by[16]:

$$Z_0 = \frac{1}{c_0 \left(\sqrt{\epsilon_{eff}}\right) C} \tag{3.4}$$

where c_0 is the speed of light in free space. With traditional CPW line impedance calculators (such as ADS LineCalc), the dielectric above the line is always assumed to be air. However in the case of three-dimensional transitions and face-down assembly

(as discussed in the next chapter), the air-dielectric assumption could lead to incorrect characteristic impedance values. Therefore, the following equations are useful for determining the characteristic impedance of a CPW line that is in close proximity to other dielectrics.

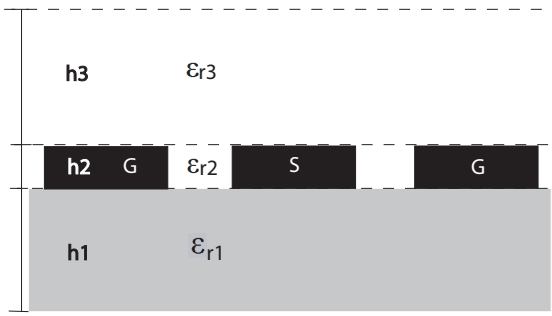


Figure 3.7: Dielectric sections for computing CPW capacitance

The total capacitance in free space C is the sum of the capacitances of each section (see Figure 3.7) where each section capacitance is given by [16]:

$$C_i = 2\epsilon_0(\epsilon_i - 1)F(k_i) \tag{3.5}$$

where ϵ_i is the permittivity of each layer, k_i defines the electric field geometry given by [16]:

$$k_i = \frac{\sinh\left(\frac{\pi S}{4h_i}\right)}{\sinh\left\{\frac{[\pi(S+2W)]}{4h_i}\right\}} \tag{3.6}$$

and $F(k)$ is the complete elliptic integral, approximated by [17]:

$$F(k) = \begin{cases} \frac{1}{\pi}\ln\left[\frac{2(1+\sqrt{k})}{(1-\sqrt{k}}\right] & , \quad 0.5 \leq k^2 \leq 1 \\ \frac{\pi}{\ln\left[\frac{2(1+\sqrt{k'})}{(1-\sqrt{k'}}\right]} & , \quad 0 \leq k^2 \leq 0.5 \end{cases} \tag{3.7}$$

$$k_i' = \sqrt{1 - k_i^2} \tag{3.8}$$

The effective permittivity of the CPW structure is given by [17]:

$$\epsilon_{eff} = \sum q_i \epsilon_i \tag{3.9}$$

where q_i is a filling factor representing the fraction of field energy traveling through each media.

The filling factor is determined by [16]:

$$q_i = F(k_i) \tag{3.10}$$

It is worth noting that a simple approximation of the effective permittivity for a CPW line with a substrate permittivity of ϵ_r in free space is given by:

$$\epsilon_{eff} \approx \frac{\epsilon_r + 1}{2} \tag{3.11}$$

which is simply the average of the two dielectrics.

The complete method of characteristic impedance calculation in equation 3.4 considers the effects of stacked substrates and dielectrics between them as will be presented in the following chapters.

3.3.5 Coplanar Waveguide Odd Mode Suppression

Since the CPW configuration includes three conductors, it is important to note that it can support both even and odd mode signals. The even mode is preferred since it can operate at higher frequencies with less dispersive effects. In even mode operation, the

two ground conductors are held at the same electric potential (ground). The electric fields are then coupled between the center conductor and the equipotential conductors on either side in typical CPW operation as shown in Figure 3.1(b). On the other hand, odd mode operation occurs when currents of equal magnitude and opposite direction propagate through the outer conductors (not equipotential in this case) similar to the coplanar stripline of Figure 3.1(c). Nearly zero current flows through the center conductor in odd modes [17]. In order to prevent parasitic energy loss, it is advantageous to suppress the odd mode by electrically connecting the ground planes on either side of the signal conductor. This is often done using wirebond connections, an air-bridge connections, or via strap connections when using a multi-layered process technology.

3.4 Summary

Transmission lines and planar waveguides that propagate waves in the 2-D plane on MMICs and carriers have been discussed in this chapter. The features of each type discussed are summarized in Table 3.1.

Table 3.1: Summary of Transmission Lines and Planar Waveguides.

	Metal Layers	Dispersion	Isolation	Power
Microstrip	2	High	Poor	Low
Coplanar Stripline	1	Medium	Medium	Very Low
Coplanar Waveguide	1	Medium	Medium	Very Low
Stripline	≥ 3	Very Low	Good	High
Micro-Coaxial	≥ 3	Very Low	Very Good	High

The ability to couple these 2-D transmission lines together with heterogeneous system components requires 3-D transitions. Vertical transitions that make the stacked RF systems possible are discussed in the next chapter.

Chapter 4

Vertical Interconnection and Assembly

Vertical interconnects link the transmission lines on the planar chip level to lines on the carrier/system level. To couple high frequency signals between integration levels, the vertical interconnect section must adequately match the wave confinement of the planar transmission line sections that are being interconnected. This transition from the chip level to the carrier level also requires mechanically assembling the various chip components together. This interface between the chip and carrier is commonly referred to as chip scale packaging or first level integration. In a traditional MCM, all of the chips of the system are bonded directly to the carrier using assembly techniques that will be discussed later in this chapter. However in more advanced integrated systems such as SiP, chips are stacked on top of adjacent chips and bonded together. There have been major advances in the technology at this level of integration that have led to significant reductions in size and power consumption in recent years. This chapter introduces previous work on vertical interconnects in the microwave/millimeter-wave regime and compares them to the proposed interconnects of this research.

4.1 Vertical Microwave/Millimeter-wave Interconnects

This section presents vertical transition strategies between various transmission lines and planar waveguides. As mentioned in Chapter 3, on-chip microwave interconnects tend to be planar (microstrip, CPS or CPW) while carrier-level interconnects can be either planar or three-dimensional (stripline or micro-coaxial). Therefore, assembling chips to carriers (or other chips) requires matching the transmission line on both sides of the structure with a suitable transition.

The implementation of the transition is dependent on the location of the conductors as well as whether the top chip is assembled face up or face down. For example, CPW-CPW transitions where the top chip is face down are common due to their simplicity since all of the conductors are on the same side of the respective substrate media. However, most other configurations require either through-substrate vias (discussed in Chapter 5) or wirebonds (discussed in section 4.2) to bridge across the thickness of the substrate. Several notable transitions are discussed in the following sub-sections.

4.1.1 CPW-CPW Transition

In this transition scheme, all of the conductors are on the same side of the assembled chips (assuming the top chip is face down) as shown in Figure 4.1. A spacer material is often used to separate the chip and carrier while metallized bumps extend through the spacer to connect the top and bottom conductors [18]. Due to its simplicity, the proposed interconnect methods of this research are variations of the CPW-CPW transition. The top chip is flipped makes this transition scheme closely resemble flip chip bonding, a common assembly method of digital CMOS ICs. Flip chip considerations that apply to CPW-CPW transitions are discussed in section 4.2.

The performance of this transition scheme is based on the geometry and materials of the spacer and the bumps. The height of the bumps should be sufficiently tall to separate the chip and carrier such that the carrier does not de-tune the circuit performance of the chip. It has been noted that the CPW bumps should be at least 30% of the gap separation between the signal and ground conductors [16][19].

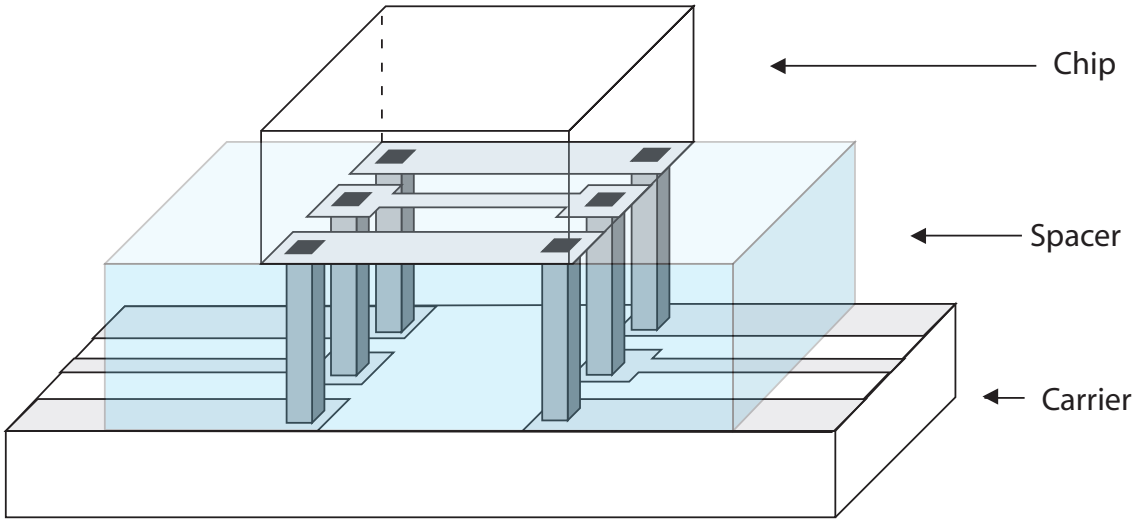


Figure 4.1: CPW-CPW transition in Flip-Chip style

Impedance matching can be performed through changing the conductor or gap width of the signal line for a small section [20]. Since the bumps typically introduce parasitic capacitance, the signal conductor can be made thinner or the gap width can be made wider in CPW to make a compensating inductance [21].

4.1.2 CPW-Microstrip

This transition scheme commonly involves a CPW carrier with a face up microstrip chip. In this way, both sides can share a common ground plane as shown in Figure 4.2. Since the signal conductor of the microstrip is on the top of the chip, an inter-layer connection must link it to the signal conductor of the CPW.

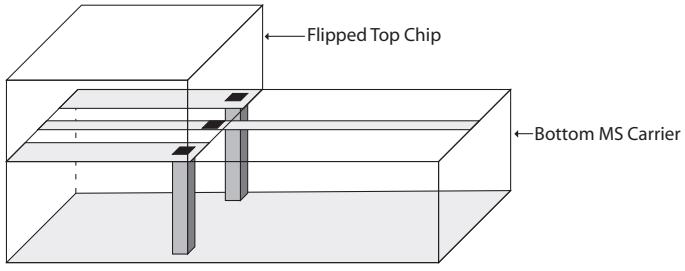


Figure 4.2: CPW-Microstrip transition

4.1.3 Microstrip-Microstrip

A novel transition approach proposed by Lahiji *et.al.* links two microstrip layers (both face up) with vias connecting signal and ground conductors [22].

The characteristic impedance of the transition is modified by using tapered vias formed by wet etching as opposed to straight vias formed by dry etching. Etching techniques will be discussed further in Chapter 5.

4.1.4 CPW-Stripline

An example of a transition between a planar waveguide and a multi-layered carrier is the CPW-SL interconnect as shown in Figure 4.3 [14]. Since the signal conductor of the stripline is embedded within the dielectric stack (typically LTCC, as will be discussed in Chapter 5), vertical vias are needed to transition the signal conductor up to the top plane for assembly with other circuits. When the top chip CPW is flipped face down on the stripline vertical signal via, it is possible for the ground plane of the CPW to be common with the top stripline ground plane.

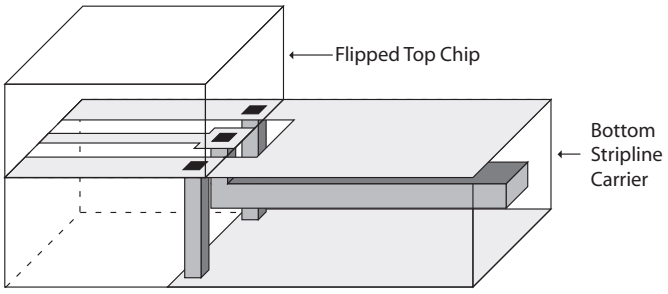


Figure 4.3: CPW-Stripline transition

4.2 Vertical Assembly

In order to realize the transitions described in the previous section, assembly methods are needed to connect the conductors on the different chip levels. These assembly techniques closely resemble the chip scale packaging used to interconnect chips at the module level. A critical aspect of chip scale packaging for RF systems is the ability

to match impedances in order to effectively propagate signals from chip to system. The chip scale packaging techniques used commonly are wirebonding and flip chip bonding.

4.2.1 Wirebonding

To date, the most prevalent interconnection scheme for MMICs is wire bonding. It is a simple, well-understood process that is easily adaptable to different configurations. The die to be wirebonded is placed face up in its package, and wires, typically made of gold or copper, are attached to respective bond pads on both the die and carrier. The process starts by mounting the chip onto the carrier, using thermally conductive epoxies to aid in sinking heat away from the chip. Next, each of the wires are bonded to the pads using a placement tool that applies heat and pressure to force the joint to weld. Ultrasonic excitation enables welding to occur at lower temperatures and pressures.

Wire bonding has been popular due to its fabrication simplicity and its flexibility with different chip layouts and pad frames, but it has some performance drawbacks that are beginning to limit its use, especially in higher frequency applications. Large bond pads must be used, introducing parasitic capacitance and the wires must be relatively long to reach from the connecting chip to the package lead frame, introducing parasitic resistance and inductance that degrade the device performance and limit the bandwidth of the transition to around 20 GHz [23]. The inductance of a wire with length, L [mm] and diameter D [mm] is given by [24]:

$$L[pH] = 0.129 * L * \left[\ln\left(4\frac{L}{D}\right) - 1\right] \tag{4.1}$$

In addition, the bond pads must be along the periphery of the bonded chip, limiting the number of connections that can be made. The pad footprints for wirebonding on the chip are quite large and significantly contribute to the overall size of the chip. This inefficiency in real estate drives the need for space-saving assembly methods in future high density systems.

4.2.2 Flip Chip Bonding

An emerging bonding technique that is closely related to this work is flip chip bonding. Flip chip bonding is quickly replacing wire bonding as the approach of choice, especially in high frequency applications [19]. Traditional flip chip bonding includes depositing solder bumps on the chip and then mounting it face down onto carrier. The bumps are typically plated onto pads on the chip and then a reflow cycle melts the bumps so that they adhere to corresponding pads on the carrier. In order to protect the bumps from thermal stress, underfill polymers are often injected under the chip after bonding.

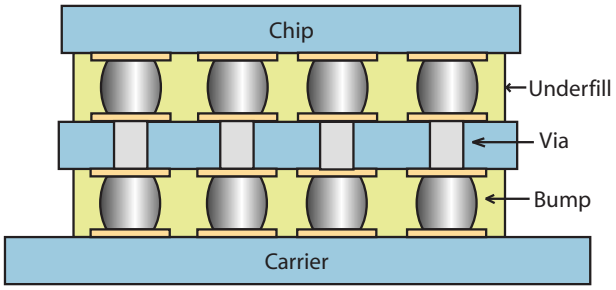


Figure 4.4: Stacked Flip Chip Bonding - Chip bonded face down on metal bumps with underfill in between

In this case, the interconnects extend vertically and are typically much shorter than wire bonds (flip chip bonds are typically 5-50um while wire bonds are usually 1-10mm). The reduced length makes flip chip connections suitable up to bandwidths of 100 GHz or more [23]. Also since the bonding bumps are underneath the chip, less carrier real estate is required compared to the wirebonding case. Also, the bumps can be integrated at any location on the face of the chip, opening up the possibility to shorten intra-chip global traces by stacking chips and connecting circuitry vertically. The main concern of flip chip bonding is managing the heat produced by chips mounted closely together. Also, the close proximity of the chip to the carrier can couple electromagnetic fields at high frequencies which can cause unwanted interference between circuit blocks.

Table 4.1: Comparison of Assembly Approaches.

Assembly	Wirebonding	Flip Chip
Interconnect Length	Long	Short
Carrier Area Required	High	Low
Interconnect Fab	Serial	Parallel
Interconnect Location	Periphery	Array

The key consideration for using flip chip strategies at high frequencies is making the bumps small enough in cross-section to maintain the characteristic impedance of the transmission lines that are being connected together. In terms of reflection, the width of the bumps determines the return loss due to the capacitance between the bumps [25].

The above packaging and bonding techniques have been demonstrated and used with success in the microelectronics industry for microprocessors, memories and other digital devices. Adapting flip chip assembly to the microwave/mm-wave regimes requires further consideration and one of is the focuses of this work. The next section describes the process involved and the materials used in flip chip assembly

4.3 Flip Chip Bonding Methods

Flip Chip assembly is becoming increasingly favorable over wirebonding in microwave/mm-wave applications because the parasitic inductance, resistance, and capacitance are greatly reduced because the interconnections are much shorter and have smaller footprints. This section includes discussion on the structure of an individual flip chip bump, common flip chip materials, and underfill materials used to protect the bumps.

4.3.1 Solder Bump Components

There are four components to traditional solder bump assembly: the under bump metallurgy (UBM), the top surface metallurgy (TSM), the solder bumps themselves, and the underfill encapsulant [26]. The UBM is patterned on the die to ensure that the solder bump firmly adheres to the metallization pads on the die, while the TSM ensures adhesion with the pads on the carrier. The UBM and TSM are usually

fabricated in a three step process: an adhesion layer approximately 100 nm thick (commonly Ti, Cr, Ni, W, and Zn), then a wetting layer approximately 1 μm thick (commonly Cu), and finally an oxidation passivation layer approximately 200 nm (commonly Au). These layers allow for a strong bond by promoting solder wetting as well as preventing joint oxidation that can create cracks in the interface.

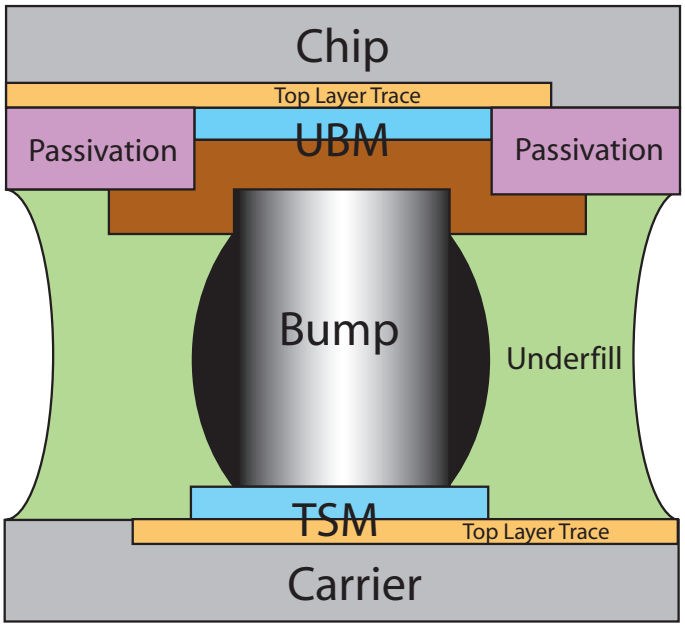


Figure 4.5: Diagram of the components of a single flip chip solder bump

4.3.2 Solder Bump Materials

Solders are usually differentiated by their melting temperature. High melting point solders generally have high yield strength and therefore only experience elastic deformation during operation. Low melting point solders, on the other hand, have lower yield strengths and experience plastic deformation during operation. While the ductile low melting point solders can better discharge stresses, they exhibit thermal fatigue that leads to failure after long periods of operation [27]. The commonly accepted practice is to choose a solder bump material that has a higher melting point than any subsequent thermal packaging steps and operating temperatures. This is important in traditional solder bump technology because most of the mechanical support for the chip comes from the solder bumps. The thermal budget of the overall

packaging process should be minimized to prevent stresses caused by the differences in coefficient of thermal expansion (CTE) of heterogeneous substrates, as well as to prevent damage or compromise performance of active devices. Once the bumps have endured their original reflow to create the electrical and mechanical connections, the bumps should remain solid [28].

The materials that are combined to form the solder bump alloys significantly affect the overall characteristics. In the past, most solders were made of varying concentrations of lead and tin, mainly due to the low cost, ease of use, and acceptable performance [26]. The higher the lead content (up to roughly 97% Pb), the higher the melting temperature. The addition of tin in the alloy enhances the overall solder wettability. Lead alloys containing indium tend have high thermal fatigue reliability [27].

More recently, lead-free solder alloys are becoming prevalent due to environmental concerns. A major issue when switching to lead-free alloys is the ability to prevent the molten solder from oxidizing and creating poor joints [28]. Oxidation was overcome when using lead solder by using polymer fluxes to isolate the molten solder from air which could be cleaned after the solder was cooled. From an RF perspective, the introduction of fluxes and cleaners could leave residues that could detune sensitive circuitry and cause deterioration and failure. Therefore, lead-free fluxless solders are highly desirable with the most common to date being AuSn. AuSn solder can be evaporated in layers; the layers then diffuse together during the thermocompression bonding. The drawback to using AuSn solders is the high reflow temperature necessary (>300C). Current bump materials research seeks lead-free low-temperature solder materials.

Adding Indium and Bismuth to lead-free alloys tends to reduce the overall melting temperature. However, these are reserved for speciality applications due to the cost of indium and the brittleness of bismuth alloys [29]. Tin is still a major constituent in lead-free alloys due to its low cost, low melting point, strength, and wettability. Silver is sometimes used, but only in small quantities (due to its cost and high melting point), to improve the conductivity of the solder. Properties of common solder materials and alloys are shown in Table 2.1.

Table 4.2: Properties of Common Solder Bump Materials.

Material	Ratio[%]	Melt. Pt [C]	Tensile Strength. [MPa]	Elec. Cond. [S/um]
In	100	157	1.88	13.92
Sn	100	232	13.1	8.7
Pb	100	327	12.4	4.97
InSn	52/48	118	11.85	6.78
InAg	97/3	143	5.52	13.35
SnAg	96.5/3.5	221	18.6	9.62
AuSn	10/90	217	50.2	5.68
AuSn	80/20	280	278	
SnPb	63/37	183	51.7	6.94
SnPb	5/95	310	27.6	5.13

4.3.3 Underfill

Underfill materials are polymeric adhesives that are used to mechanically isolate the bumps from stress generated through Coefficient of Thermal Expansion (CTE) mismatch. The underfill adheres to both the chip and carrier and couples them mechanically, reducing the stress on the bumps and increasingly reliability [30]. Because of this, underfill materials can increase the solder bump reliability by an order of magnitude over bumps without it.

Underfill materials must be considered not only on mechanical qualities, but also electrical properties such as dielectric permittivity and loss tangent. The effective dielectric constant of planar transmission lines is affected by the presence of underfill dielectric materials (discussed in Chapter 3) and their insertion loss increases if the underfill is exceptionally lossy. A study was conducted using a flip chip CPW chip with an underfill to determine the affects the underfill had on the RF performance [31]. The result was that epoxy underfills generate an additional loss of less than 1dB/mm through 40 GHz, proving the flip chip assembly method can be extended to high frequencies.

Another study proposed a method of tailoring the properties of the underfill material by modifying the ratio of epoxy resin to silica filler in the composition [32]. For example, the elastic modulus can be increased, thus stiffening the material, by increasing the concentration of the silica filler. The silica filler is generally less lossy compared to the epoxy resin, so the material flexibility and dielectric loss can be optimized for

a given application.

Underfills also serve as a semi-hermetic encapsulation to protect the bumps from environmental issues such as oxidation and corrosion. Typical underfill materials are polymeric adhesives that can be deposited either through capillary flow after the chip has been bonded, or by applying as liquid in place before bonding such that the bumps can press through it.

4.3.4 Coefficient of Thermal Expansion Mismatch

Materials generally expand when exposed to increased temperatures, and the rate of this change is known as the Coefficient of Thermal Expansion. When materials with different CTEs are bonded together, stress is created at the interface as the material with higher CTE expands more readily than the other material. This is known as CTE mismatch. This is particularly problematic with flip chip bonding as the bonded chips expand laterally and impose shear strain (elongation parallel to the material face) on the bumps as shown in Figure 4.6.

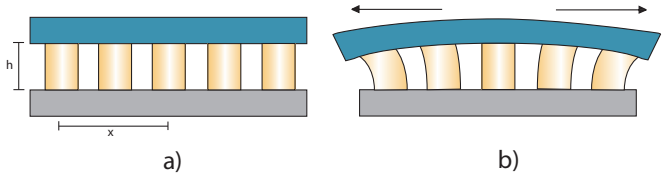


Figure 4.6: CTE mismatch - a) Assembled chip and carrier with no thermal excitation. b) Assembled chip and carrier with high thermal excitation.

The shear strain on a bump due to CTE mismatch without underfill is given by [30]:

$$\gamma = \frac{(\Delta CTE)(\Delta T)(x)}{h} \tag{4.2}$$

where ΔCTE is the difference in CTE between the dissimilar materials, ΔT is the change in temperature, x is the distance from the center of the chip, and h is the bump height. Therefore, bumps on the periphery of large chips experience the most shear strain and are most susceptible to breakage. Equation 4.2 also shows that the bump height reduces the effects of CTE shear stress.

The shear strain on a bump due to CTE mismatch with an underfill layer is given by [33]:

$$\gamma = (\Delta CTE)(\Delta T)\frac{2k\sinh(kx)}{3G\lambda\cosh(kl)} \tag{4.3}$$

where $k = \sqrt{\frac{\lambda}{\kappa}}$ and λ is the axial compliance and κ is the interfacial compliance. The axial compliance, a measure of stiffness in the z-direction, between the stacked substrates is given by [33]:

$$\lambda = \frac{(1-v_1^2)}{E_1 h_1} + \frac{(1-v_3^2)}{E_3 h_3} + \frac{h^2}{4D} \tag{4.4}$$

where E_i is the Young's modulus of each layer, v_i is the Poisson ratio of each layer, h_i is the thickness of each layer, and l is the distance from the center to edge of the chip . The flexual rigidity, a measure of the force required to bend a material, of each layer is given by [33]:

$$D_i = \frac{E_i h_i^3}{12(1-v_i^2)} \tag{4.5}$$

with the stack rigidity being the sum of all of the layers. The shear modulus, the ratio of applied shear force to shear deformation of the material, of each layer is given by [33]:

$$G_i = \frac{E_i}{2(1+v_i)} \tag{4.6}$$

with the stack shear modulus being the sum of all the layers.

The interfacial compliance, a measure of how well the stacked materials adhere to each other when the stack is bent, is given by [33]:

$$\kappa = \frac{t_1}{3G_1} + \frac{2t_2}{3G_2} + \frac{t_3}{3G_3} \tag{4.7}$$

Young's moduli and Poisson ratios of common flip chip materials are given in Table 4.3.

Table 4.3: Mechanical Properties of Common Flip Chip Materials.

Material	Young's Modulus [GPa]	Poisson Ratio	CTE [ppm/K]
Silicon	160	0.3	2.8
GaAs	82.68	0.31	5.7
Underfill	2.5-74	0.19-0.4	0.5-87
SU-8	2	0.22	52
FR-4	22	0.28	18
Alumina	300	0.21	6.5

For example, epoxy-based photoresist SU-8 adds almost 2 orders of magnitude of strain relief to flip chip bumps when used as an underfill material. When using the previous model for flip chip bump strain without an underfill material, a 100°C temperature change creates approximately 250000 μm/ μm of strain. Under the same conditions except for adding an underfill material, the resulting strain is approximately 8000 μm/ μm. The strain reduction is further reduced with materials with higher elastic (Young's) modulus. Therefore, underfill materials are mechanically necessary for reliable flip chip bonds.

4.4 Summary

This chapter has addressed some of the common RF transmission line integration schemes between chips and carriers as well as assembly techniques used in these

transitions. CPW-CPW transitions are used in this work due to their simplicity in fabrication and bonding. Flip chip bonding was discussed because of its potential it has for W-band integration and beyond.

Chapter 5

Vertical Fabrication Technologies

The ability to fabricate three-dimensional circuit layers and vertical interconnects saves lateral space and allows systems to be realized in a much more dense and efficient manner. The vertical interconnect strategies discussed in the previous chapters require several specialized techniques in order to be manufactured. This chapter discusses fabrication technologies that are needed for 3-D microwave/millimeter-wave integration, as well as the assembly technologies that combine the different components.

Wafer-level fabrication processes that can be employed in vertical integration include bulk and surface micromachining. Bulk micromachining involves wet or dry etching of semiconductor substrates in order to create three-dimensional features, for example through-substrate vias (TSVs) that can electrically connect circuits at the top and bottom surfaces of the substrate [34]. Surface micromachining involves dielectric film processing and metal deposition to create three-dimensional features, for example LIGA[1]-like metallic waveguide structures [35].

[1]LIGA is a German acronym that stands for Lithographie, Galvanoformung, Abformung (Lithography, Electroplating, and Molding)

5.1 Bulk Micromachining

Both crystalline and non-crystalline substrates can be etched to create three-dimensional features. There are two general methods of creating three-dimensional cavities: wet chemical etching and dry plasma etching. Wet etching involves immersing the substrate in a chemical bath that reacts with the substrate surface. Dry etching involves placing the substrate into a chamber containing an RF-excited plasma whose ions physically bombard and/or chemically react with the substrate surface.

A key consideration in bulk micromachining is the isotropy of the etch, which dictates the topography of the sidewalls and overall shape of the etched cavity. Wet etching in silicon is generally anisotropic and selective to different crystal planes. For example, the etch rate of the <111> plane in silicon is much slower than other planes, creating angled sidewalls based on the surface crystallography of the wafer as shown in Figure 5.1. Dry etching is generally isotropic and etches equally in both the vertical and lateral directions. This creates cavities with nearly vertical sidewalls, regardless of the wafer crystallography. These differences must be accounted for in the mask design in order for the desired structure to be realized.

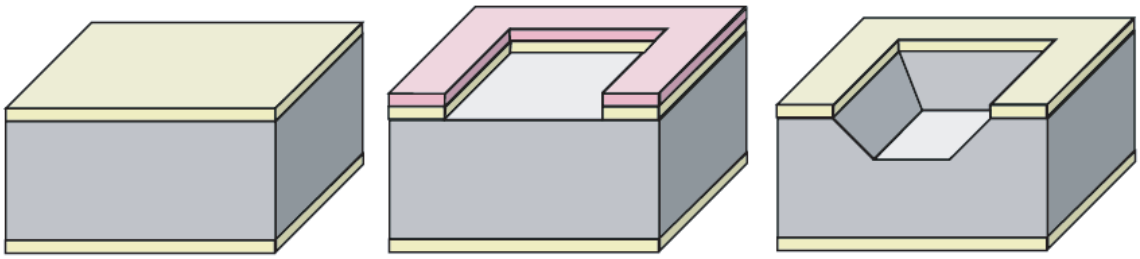


Figure 5.1: Anisotropic Etching Process: a) Mask Layer Deposition. b) Mask Layer Patterning c) Aniostropic Etching

Bulk silicon wet etching is most commonly performed using baths of potassium hydroxide (KOH), ethylenediamine pyrocatechol (EDP), or tetramethyl ammonium hydroxide (TMAH). Each of these etchants has properties that make it suitable for different applications. In all three cases, the bath concentration poses a trade-off between etch rate and surface roughness. A higher concentration of the etchant yields a smoother etch surface at the cost of slower etch rate. KOH has the fastest etch rate (roughly 1.5 μm/min), but has poor selectivity to SiO_2 and can be difficult to work with due to potential health hazards [36]. EDP has superior selectivity to a

wide range of mask materials including SiO_2, but is extremely dangerous to work with due to both physical and health hazards, and can easily become unusable due to precipitates in the etching solution. Despite the slower etch rate, TMAH is the etchant of choice in this work due to its superior SiO_2 selectivity and relative ease of use.

Advances in dry (reactive ion) etching have created the ability to etch high aspect ratio vertical trenches. While standard dry etching can be excited to etch mostly vertical, it is still isotropic. Vertically etched sidewalls can be obtained by alternating steps of passivation and etching in a process known as Deep Reactive Ion Etching (DRIE). The passivation step slows the lateral etch rate, resulting in nearly vertical cavity with minimal lateral mask undercutting.

5.1.1 Bulk Etching Evaluation Experiments

Bulk silicon micromachining experiments were conducted for use in processing steps in this work discussed further in Chapter 6. The important issues in comparing wet and dry etching methods include cost, processing time, and masking. Wet etching methods are generally much simpler and cheaper because they only require a heated and stirred chemical bath. Dry etching techniques require expensive tools operated under high vacuum with precision gas controls and RF power to generate etching plasma. As far as processing time, dry etching generally etches an order of magnitude faster than wet etching. As for masking layers, both approaches can typically be patterned using oxide layers as a mask; however dry etching requires a thicker mask layer due to its poorer oxide selectivity.

The experiments compared TMAH and DRIE etching approaches using <100> silicon wafers. Since TMAH etches the <100> plane considerably faster than the <111> plane, it forms slanted sidewalls at roughly a 54° angle and this must be accommodated to ensure the cavity feature is large enough in area at the bottom. A 20% concentration of TMAH was used as a compromise between etch rate and surface smoothness as suggested by [36]. The wet etch was performed in a large beaker with mechanical stirring at 250 RPM and a solution temperature of 140°F [37].

The DRIE etch was performed in an Alcatel 100 SDE chamber using SF_6 for etching

and C_4F_8 for passivation, known as a Bosch process. The results of the etching experiments are shown in Table 5.1.

Table 5.1: Comparison of DRIE and TMAH for bulk silicon etching.

Si Etching	DRIE	TMAH
Rate	4 μm/min	0.5 μm/min
Sidewall	Vertical	Slanted
SiO_2 Selectivity	100:1	1000:1
Cavity Surface	Rough	Smooth

5.1.2 Through-Substrate Vias

An important application of bulk micromachining that enables vertical integration is the fabrication of through substrate vias (TSVs). TSVs form the electrical connections between surfaces of wafers in a bonded stack, and are necessary in order to fabricate stacks higher than a single level without requiring all of the I/O pads to be along the periphery of each chip. These vias are generally fabricated by etching a vertical hole completely through the wafer and then filling the hole with metal [34]. Isolation layers of silicon oxide or nitride are generally used to electrically separate the via metallization from the bulk substrate. These dielectric materials are typically deposited through low pressure chemical vapor deposition (LPCVD). The metal filling is a two step process: a seed layer is sputtered in the cavity to coat the sidewalls and then metal is electroplated onto of the seed layer, eventually filling the hole. Copper is a popular metal choice for vias due to its ability to be electroplated, high conductivity, and relatively lower cost. As this technology has matured, isolating dielectric layers, such as silicon nitride, have been used to separate the metallized via from a conductive bulk substrate [34][38].

5.2 Surface Micromachining

Surface micromachining techniques build up components layer by layer on top of the substrate. The specific surface micromachining techniques used in this work are

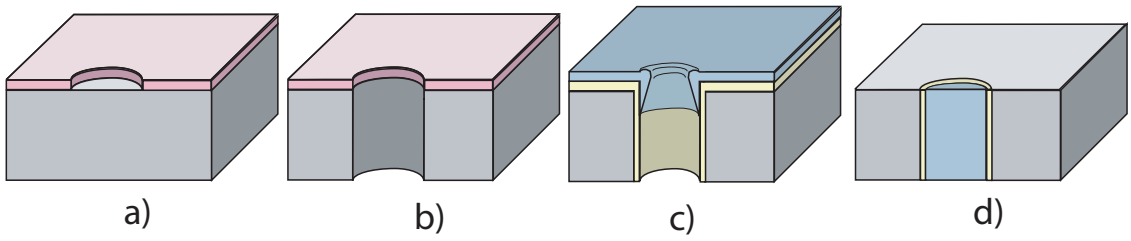


Figure 5.2: Through Wafer Via process steps: a) Photoresist mask pattern. b) Through Wafer Deep RIE. c) Isolation and metal sputtering. d) Metal plating and Chemical Mechanical Polishing(CMP)

LIGA-like processes, including thick-film processing and electroplating.

5.2.1 LIGA

LIGA is a well-known process for creating high aspect ratio metal structures from lithographically-defined molds [39]. LIGA-like steps include using thick film photoresists as electroplating molds on top of a conductive seed layer, electroplating, and then subsequently removing the mold to expose the free-standing metal. In this way, vertical metal interconnections can be made much taller than is possible using common, thin-film deposition systems such as sputterers and evaporators. The height and the aspect ratio of the resulting metal structures are dependent on the properties of the material used for the mold. PMMA is widely used in LIGA processing due to its ability to create tall, high aspect ratio features. It is usually applied in a two step process: first, a thin, liquid adhesion layer is spun on to the wafer; and second, a thick solid layer is bonded on top [40]. The solid layer can then be polished down to the desired height of the structures using a flywheel. The PMMA can be patterned through exposure by electron-beam or deep UV lithography [41]. While PMMA performs quite well when properly applied (40:1 aspect ratio for $>$ 1mm tall structures), alternative resists, such as SU-8, are of great interest since they can be processed similar to thin film photoresists (spin-coating, UV exposure), yet have comparable performance to PMMA [42]. These resists will be further discussed in the next sections.

A notable multi-layer LIGA-like process for creating micro-coaxial components (Fig.

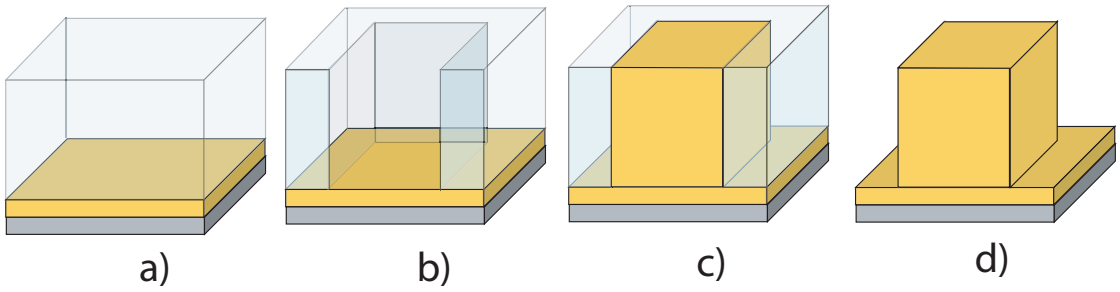


Figure 5.3: LIGA process steps: a) Mold deposition. b) Mold patterning. c) Electroplating. d) Mold Removal.

3.4) is the Polystrata process developed by Nuvotronics[2][15]. These three dimensional structures are fabricated in thin layers through a series of photoresist molding, copper electroplating, and chemical mechanical polishing (CMP) steps. After the final polishing step, the photoresist is removed, leaving the free-standing copper structure (free-standing coaxial transmission lines with air dielectric for low loss). Each layer is roughly 100um thick with currently up to 15 layers in the process.

5.2.2 Electroplating

Electroplating is a common metal deposition technique for creating films or structures that are thicker than can be practically done with physical vapor deposition (PVD) and is critical to the LIGA process described above. Given that PVD deposition rates are generally on the order of 5 Å/s, and 1 gram of metal roughly produces films 1000 Å thick, the practical limit for films produced by PVD is generally 0.5 um. Electroplated films, on the other hand, can be as thick as 1 mm.

Typical electroplating methods involve supplying an electric current between an anode and cathode that are submerged in an electrolytic bath. The current causes the metal ions suspended in the solution to be drawn toward the cathode. Samples can be plated by connecting them as the cathode in the electrolyte bath. This can be done by coating the sample with a thin, electrically-continuous layer known as a seed layer. In a LIGA style process, a thick photoresist mask is patterned on top of the seed layer in order to plate high aspect ratio (HAR) metal structures. The characteristics of the

[2]Formerly Rohm and Haas Electronic Materials

HAR structures are directly related to the plating conditions of the electrolyte bath set up.

Gold is widely used in the RF microelectronics industry due to its low thermal and electrical resistance, low reactivity, and ease of deposition. These qualities make it very suitable as an interconnect and bonding metal. Since gold is less reactive than other metals, it is less likely to corrode and oxidize; therefore, it is more able to maintain mechanical strength and electrical continuity. Gold is easily deposited using both slow, uniform physical vapor deposition (PVD) methods, and through faster electroplating methods.

The most widely used gold electroplating solutions are cyanide-based, thiosulfate-based, and sulfite-based electrolytes. Cyanide solutions generally have the fastest deposition rate, but are toxic and tend to be incompatible with many photoresists. Positive resists have been noted to crack and lose adherence to the substrate, but experiments have shown that negative resists can also be adversely affected by cyanide electrolytes as well. Thiosulfate solutions have not been extensively used based on their instability. Sulfite baths are non-toxic and tend to exhibit better bump thickness uniformity than cyanide solutions [43]. For these reasons, a sulfite solution was used as the electrolyte for gold bumps in this research.

5.2.3 SU-8

SU-8 is a negative tone epoxy-based photoresist that is capable of producing thick films up to several millimeters thick with high aspect ratio sidewalls [44]. As a negative photoresist, the polymer cross-links when exposed to UV light and is therefore patterned with dark field masks. A key feature of SU-8 is that cross-linked SU-8 is very durable and virtually insoluble in acids, bases, and solvents. Because of this, applications in which the SU-8 can be left as a permanent structure are best suited for its use.

SU-8 is commonly used as a substitute for PMMA in LIGA processes because of its thickness and high aspect ratio. SU-8 can be spun on to the sample surface and exposed using UV sources, making the process flow much simpler and inexpensive compared to PMMA. Also, since cured SU-8 is impervious to most chemical treatments, it

is suitable as a mold in electroplating baths. This same quality, however, makes SU-8 quite difficult to remove after the metal structures have been electroplated. While SU-8 can be removed through heated N-Methyl-2-pyrrolidone (NMP)-based solvents and harsh plasma etches, these processes generally destroy the plated metal as well. Therefore, it is often best to keep the SU-8 as a permanent mold after electroplating instead of trying to remove it.

Several applications for SU-8 as a low-k dielectric material have emerged in the RF realm. In these regards, it should be compared to polyimide and Benzocyclobutene (BCB) as suitable insulating polymers. In a study by Jeon *et al*, thick dielectric layers were tested for their capacitive properties based on the quality factor of inductors built on top of the layers. Despite its higher loss, SU-8 had a higher quality factor for test inductors at 8 GHz [45].

Further investigations were conducted by constructing CPW lines on top of low-resistivity (LR) silicon using these insulating polymer layers as isolation [46][47]. Without proper isolation, much of the electromagnetic energy is absorbed in the lossy substrate in a CPW configuration directly on low-resistivity silicon, leading to poor transmission. Polyimide and BCB show reasonable improvement over direct contact with the LR silicon, but the CPW performance is also related to the amount of energy contained in air above the line. The ability to make ultra-thick films allows SU-8 to create more insulating space between the CPW conductors and the lossy substrate reducing the insertion loss of the line.

In summary, SU-8 has the following key strengths: very thick films with nearly vertical sidewalls; simplified processing compared to other thick films; and good mechanical stability and adhesion when cured. The Mechanical Fit strategy to be presented in Chapter 6 exploits each of these desirable characteristics when using SU-8 as the interfacing structure between a mounted chip and carrier.

5.2.4 KMPR

While SU-8 has several qualities that make it a suitable choice for electroplating molds (10 to 1000 μm thick films with 10:1 aspect ratio), removing it after plating can be very difficult and this therefore limits its use as a sacrificial layer. For this

reason, a new epoxy-based photoresist, KMPR, was developed with many of the same properties of SU-8 that is also easily strippable [48]. KMPR is an ideal alternative in applications in which free-standing electroplated metal structures with high aspect ratio are desired.

The processing requirements of KMPR are very similar to those of SU-8. Both materials are spun on as very viscous liquids that release their liquefying solvents during a soft bake step. Both are patterned through exposure to i-line (365 nm) UV radiation, although KMPR requires a significantly stronger exposure dose (roughly 5x) than SU-8. The photolithographic process is concluded with a post-exposure bake, followed by development for both materials. An organic solvent (propylene glycol monomethyl ether acetate sold as SU-8 developer) can be used to develop both SU-8 and KMPR. After lithography, both thick films are ready for electroplating. After electroplating however, KMPR can be removed through either solvent baths or RIE etching while SU-8 remains impervious to these agents.

The removal of KMPR in solvent baths is a three-part process. The first step is an NMP-based solution (sold as Remover PG) that causes the sacrificial KMPR to expand and swell, producing cracks on the surface of the material. The second step is a combination of organic solvents (sold as Remover K) that help break down the adhesion between the photoresist and the electroplated sample, lifting off the unwanted sacrificial layer. The last step is a neutralizing acid that removes residues left by the KMPR and the Remover K.

A crucial step in the use of KMPR is that a de-scum step must be performed after development of the photoresist. This completely cleans the seed layer surface so that electroplated metal will adhere well and create a strong mechanical bond with the seed metal. Otherwise, residual photoresist could block the electroplated metal formation and severely weaken the bond. These weakened bonds typically separate from the seed layer when the KMPR swells during removal. The typical de-scum cycle required is an RF plasma of 100 watts in 100 sccm of O_2.

In addition, the thickness of the KMPR film makes it susceptible to delamination during thermal cycles, particularly during heated plating baths. Therefore in order to keep the mold from peeling off during the electroplating run, it is necessary to keep the bath at a lower temperature. For the processing in this work, the electroplating

bath was kept at 40°C instead of the 80°C typically used with thin film plating molds. This significantly slows the deposition rate, but is necessary for successful processing with KMPR.

5.3 Summary

This chapter has discussed three-dimensional fabrication techniques, specifically bulk and surface micromachining. These techniques have evolved through MEMS research. TMAH etching is used in Chapter 6 for bulk silicon processing. Electroplating is used to create gold flip chip bumps in both Chapters 6 and 7. Thick film processing of SU-8 to create underfill-like structures for flip chip assembly is also used in Chapters 6 and 7. KMPR is used as a sacrificial HAR electroplating mold in Chapter 7.

Chapter 6

Mechanical Fit

In a vertical SiP configuration, the bonding and stability of adjacent levels of the chip stack is of prime importance. In order to maintain optimal signal and structural integrity of the interconnects, it is important to minimize the number of stressful thermal cycles imposed on the system during assembly. For example, if standard solder bumps are used to connect each level of the stack, then a new thermal reflow cycle is required to add each new level. This introduces considerable stress on previously reflowed solder bumps and on the stacked devices, and can jeopardize the reliability of the overall system, particularly when different substrate technologies are used. The proposed Mechanical Fit approach solves this problem by allowing each level to snap together and be held in place through interlocking structural layer so that one reflow cycle can wet the interconnect metal at each level and bond the system together.

6.1 Introduction

As a proof of concept of the proposed Mechanical Fit strategy, a passive chip is flipped on a carrier substrate with vertical interconnections [49]. A diagram of the passive transmission line chip demonstration of the Mechanical Fit approach is shown in Figure 6.1. The interconnections are made through tall (~50 μm) electroplated gold bumps that mate with the pads of the stacked chip. The gold plating is facilitated through a thick photoresist mold fabricated using SU-8. In contrast to typical approaches, this plating mold is designed to be permanent and interlock with a matching

SU-8 structure on the target chip to be bonded. The interlocking SU-8 structure on the target chip is patterned to avoid electromagnetically sensitive areas that could be de-tuned in the presence of the additional dielectric.

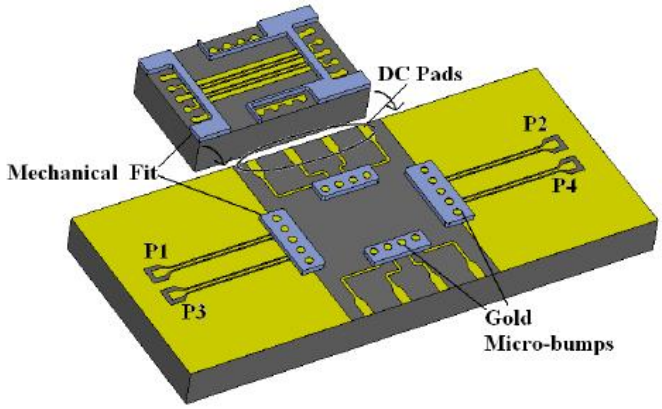


Figure 6.1: Mechanical Fit diagram showing interlocking structures between chip and substrate

The advantages of the proposed Mechanical Fit scheme include: easier and more accurate flip chip bonding; microbump protection against thermo-mechanical stress; and a larger gap between stacked circuitry to prevent cross-talk and de-tuning. Highly accurate flip chip bonding requires precisely calibrated machinery to ensure that the top chip is properly aligned with the underlying carrier. The Mechanical Fit strategy improves alignment accuracy by setting alignment tolerances with photolithography. Consequently, alignment comparable to that of typical flip chip bonders can be achieved in a more cost effective manner.

Mechanical Fit is also beneficial in providing structural support for the microbumps. In addition to serving as a mold for the electroplating process that creates the microbumps, the SU-8 remains as a permanent structure to strengthen the vertical interconnection. This support structure allows gold to be used as a bump material; which otherwise is malleable to be considered. Since the SU-8 structure compensates for the poor mechanical properties of gold, gold's resistance to oxidation and excellent electrical conductivity can be utilized.

Another advantage of using the Mechanical Fit strategy is the separation that the tall microbumps provide. As discussed in the Chapter 4, taller bumps reduce the stress caused by CTE mismatch. Also, isolating the top chip from the substrate to which it is bonded to helps prevent both thermal and electromagnetic coupling between the

two circuits. Cross-talk is directly related to the distance between coupling lines, so the taller space between chips would reduce unwanted radiation coupling in either direction. This space also offers the potential for the use of microfluidic cooling channels within the SU-8 to help dissipate heat in active circuits.

The design considerations of the proposed Mechanical Fit strategy are discussed in the next section, followed by discussion on the necessary fabrication procedures including SU-8 deposition and silicon micro-machining. This chapter concludes with RF measurements of a test chip assembled with Mechanical Fit and discussion of the results.

6.2 Mechanical Fit Structure and Process

The test structure for prototyping the Mechanical Fit strategy includes a carrier substrate with SU-8 patterns and electroplated Au bumps as well as a top chip with matching SU-8 interlocking patterns. The layout was based on the integration of a SiGe HBT 30 GHz power amplifier test chip [50] into the vertical stacking structure . The layout of the power amplifier along with the Mechanical Fit pattern is shown in Figure 6.2. The red areas shows where the SU-8 is patterned on the previously foundry-fabricated PA chip. The placement of the gold bumps and the interlocking SU-8 structures was based on the pad layout of the PA chip. All of the RF and DC bias electrical connections are provided to the chip through the electroplated bumps on the carrier substrate.

The carrier substrate was designed such that the probe pads matched the GSGSG RF probe layout (150 μm pitch) of the PA chip. The layout of the carrier substrate is shown in Figure 6.3. The gray areas show the SU-8 interlocking structures on the bottom carrier. The input and output differential CPW traces were laid out such that when the chip is mounted in position, it does not block access to the pads.

The carrier substrate process flow begins by depositing a uniform Ti layer through electron-beam evaporation on the wafer as an adhesion layer for the Au signal traces as well as a seed layer for electroplating. Photoresist is deposited and developed in order to pattern the subsequent Au conductor layer through lift-off. Then, the initial Ti layer is selectively etched to remove metal from areas that would ultimately be

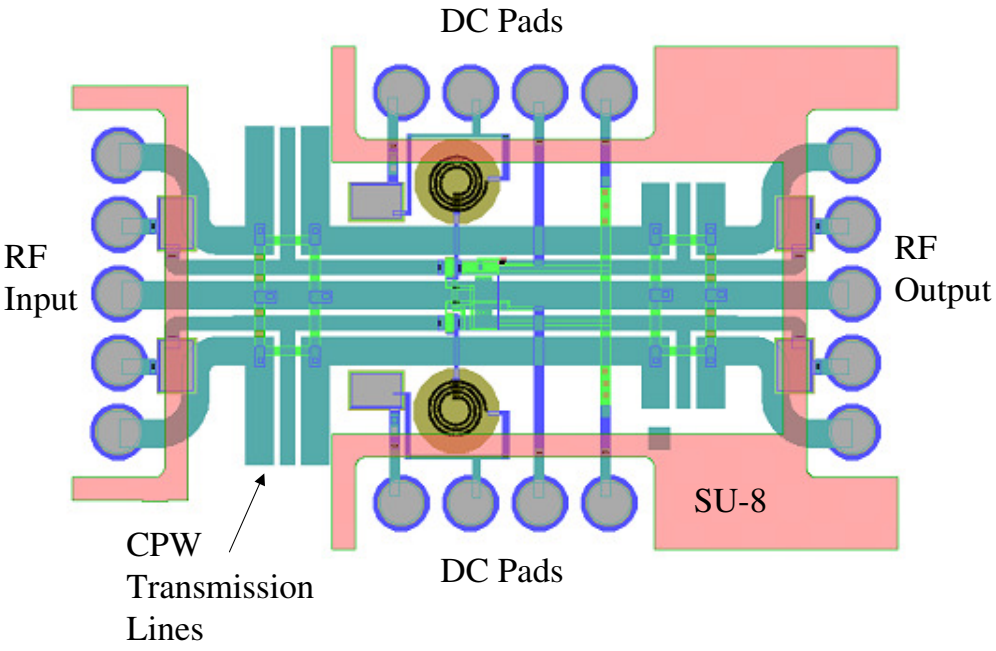


Figure 6.2: Layout of Power Amplifier with SU-8 Mechanical Fit in red

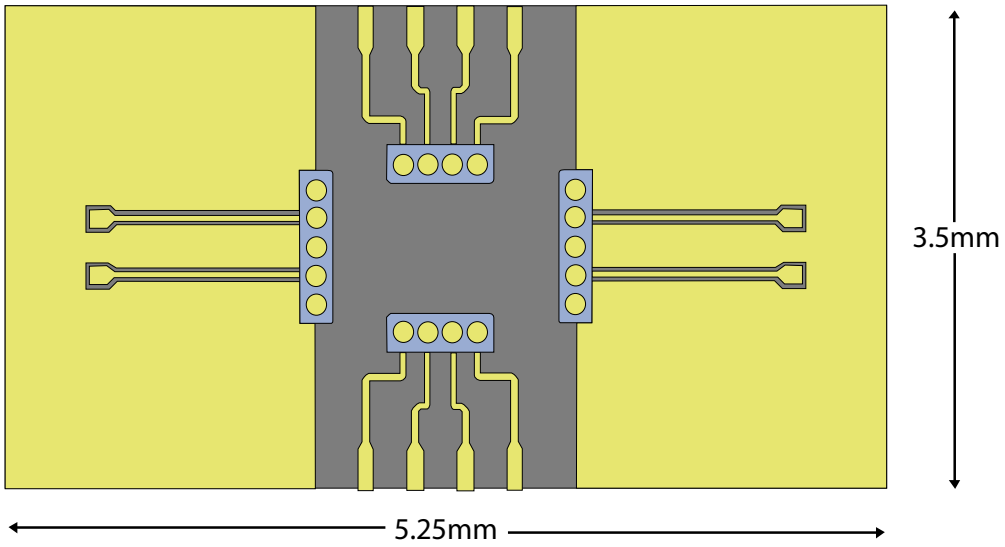


Figure 6.3: Layout of Carrier Substrate with SU-8 Mechanical Fit in gray

under the permanent SU-8 structures. The Au traces provide the conductive path from the Ti seed layer to the electroplating sites. Next, the SU-8 mold is spun-on and developed to form the bottom side of the interlocking mechanism. After the SU-8 deposition, an insulating nitride layer is used to cover the exposed Au traces to prevent unwanted electroplating. The nitride is deposited through plasma-enhanced chemical vapor deposition (PECVD). The bumps are then electroplated up through the SU-8 mold. Once the bumps are fabricated, the nitride layer and the exposed Ti layer are removed to finish the process. Completed bumps with the SU-8 structure are shown in Figure 6.5.

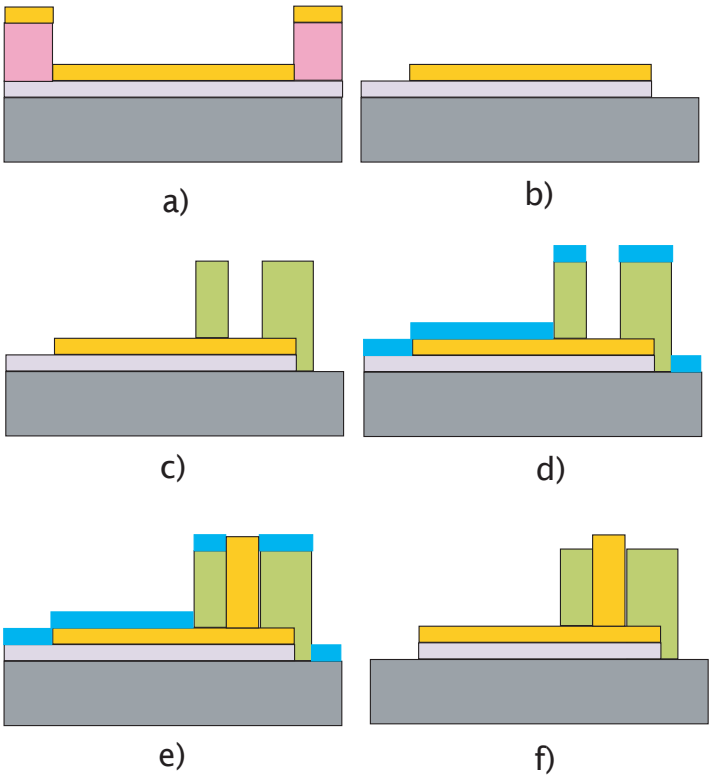


Figure 6.4: Process Flow for Mechanical Fit carrier substrate: a) Deposit Ti (gray) and photoresist (pink), b) Pattern Au (gold) through lift-off, c) Pattern SU-8 (green), d) Deposit and pattern nitride barrier layer (blue), e) Electroplate Au bumps, f) Remove nitride and remaining Ti seed layer

Passive dummy chips (no PA circuitry) were also fabricated for testing purposes as shown in Figure 6.1. These consisted of differential CPW lines with pads matching those on the PA test chip. The Ti-Au metallization is the same as the carrier. The SU-

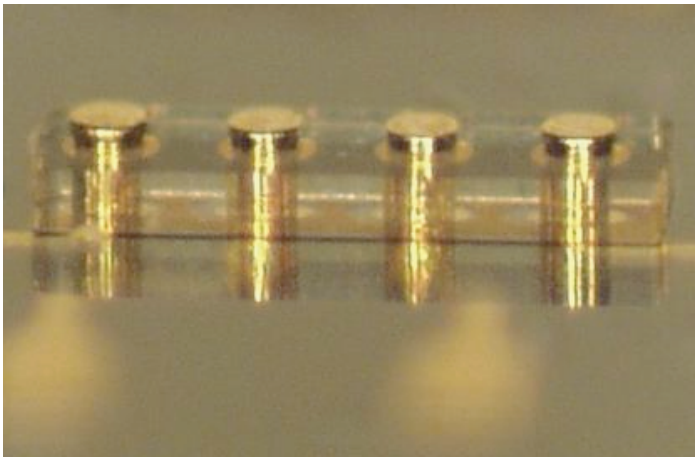


Figure 6.5: Mechanical Fit post with SU-8 and electroplated Au bumps

8 pattern is the same as that of the PA test chip in order to prototype the interlocking and bonding process.

Processing for the PA chip uses a sacrificial wafer to temporarily embed the previously fabricated PA chips so that SU-8 can be spin-coated on a planar surface. It should be noted that the use of this sacrificial wafer is only necessary to handle the diced chip for spin-coating. If the Mechanical Fit approach is implemented prior to dicing of the ICs, the SU-8 could be deposited without using a sacrificial wafer. The process for adding the SU-8 onto the diced PA chips begins by etching a cavity into the sacrificial wafer as shown in Figure 6.6. The etch rate was monitored through thickness measurements of the wafer to ensure that cavity was etched to the desired depth. The PA chip is then inserted into the cavity so that the PA chip surface is planar with the sacrificial wafer surface. Next, SU-8 is spin-coated and patterned through photolithography. Finally, the PA chip is removed from the cavity through ultra-sonic agitation during the SU-8 development. The next section discusses the processing development of the sacrificial wafer.

6.2.1 Sacrificial Wafer Processing

The sacrificial wafer was micro-machined to be compatible with the dimensions of the power amplifier chips. Cavities were etched in the sacrificial wafer so that the diced chips could be dropped into the cavity and planarized to the wafer surface. This enables spin coating as if the chip was part of a full wafer.

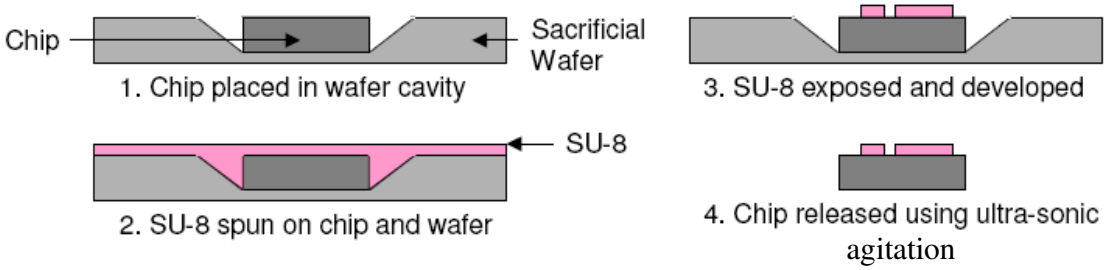


Figure 6.6: Process Flow for Mechanical Fit chip

Experiments were conducted to determine the best bulk silicon etching method as discussed in Chapter 5. Anisotropic TMAH etching was ultimately chosen because the angled sidewalls simplified the removal of the PA chip after SU-8 processing.

Samples were prepared for TMAH etching by first establishing a mask to pattern the cavity. Thermal oxidation was used to grow an oxide mask layer to ensure that both sides of the wafer would be protected from the etchant. A photoresist pattern was deposited through standard lithographic techniques to pattern the oxide on the front side of the wafer. A reactive ion etcher was used to define the pattern so that only the oxide on the front side of the wafer was etched. The cavities were then etched in the sacrificial wafers. A cross-sectional image of an etched cavity is shown in Figure 6.7 where the angled sidewalls are displayed. Figure 6.8 shows an etched cavity with an inserted chip after SU-8 coating showing the planarity of the sacrificial wafer process.

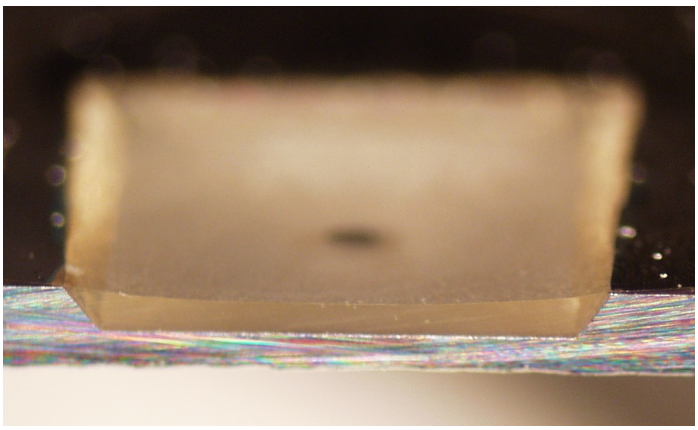


Figure 6.7: Profile of TMAH etched cavity filled with SU-8

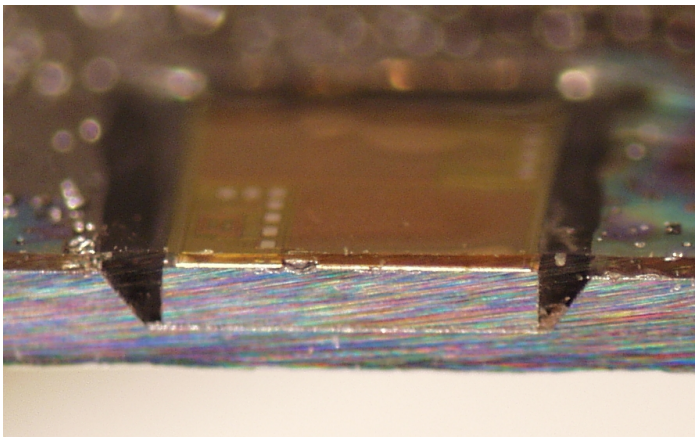


Figure 6.8: Profile of cavity with dummy chip covered with SU-8

6.2.2 SU-8 Processing on MMIC Chip within Sacrificial Wafer

To fabricate the mating SU-8 structure on the MMIC test chip, the chip is placed into the sacrificial wafer cavity and then the sacrificial wafer is spun with SU-8. The viscosity of the liquid SU-8 holds the chip in the sacrificial wafer cavity during processing. When SU-8 is initially poured on the processing wafer, an air pocket usually forms under the chip in the cavity. It is important to remove this bubble by pressing down on the chip with tweezers while it is covered with the SU-8 to ensure a uniform height of the developed structure and to keep the chip from ejecting from the carrier during spinning.

SU-8 processing recipes for the mating structures were based on the previous research into multi-layer SU-8 waveguides [51] and recommendations from MicroChem [44]. This recipe is detailed in Appendix D.

During the SU-8 spinning, exposure and development, the chip is held in place by the SU-8 surrounding the chip in the cavity. After development of the interlocking structure, ultrasonic excitation is used to remove the chip from the cavity. The angled sidewalls of the cavity from the anisotropic TMAH wet etch facilitate release of the chip. A photograph of a PA chip with the fabricated SU-8 mechanical fit structure is shown in Figure 6.9.

With matching structures on both the top and bottom, the MMIC chips can be straightforwardly positioned on top of the carrier bonding site. The structure on the top chip is patterned such that the SU-8 is outside of the corresponding SU-8 areas on

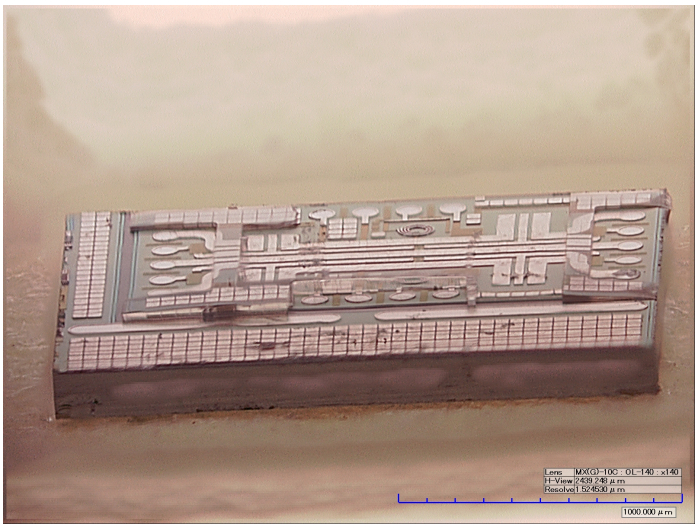


Figure 6.9: Power Amplifier chip with SU-8 Mechanical Fit structure in place

the bottom carrier, and avoids components on the chip that are sensitive to detuning.

6.2.3 Bonding

The ultimate goal of this project is to develop strategies to simplify the vertical stacking of RF components and therefore thermocompression is the ideal choice for bonding. Thermocompression only requires heat and pressure to facilitate the bonding of the interconnect metals. However, the available power amplifier test chip had aluminum pads which are difficult to directly bond to gold. Aluminum and gold do not form a eutectic alloy at the joint as is the case with normal solders; instead, they form intermetallics that can more easily degrade and fracture the joint, and cause the interconnection to fail. In typical bonding procedures, interface metal layers are used between aluminum and gold to aid the bonding process.

Despite the challenges involved in bonding gold to aluminum, studies show that it is possible. Aluminum layers readily form an isolating oxide layer that must be overcome in order to establish a proper electrical connection. There are two primary options for overcoming the aluminum oxide: use an etching step immediately followed by a thin film cap of gold to seal the pad [52] or apply enough energy through heat, pressure, and ultrasonic vibration to break through the oxide [53]. Given the added difficulty in further processing metallization layers on a 1x1mm chip, experiments were conducted by attempting to bond the gold microbumps directly to the aluminum pads through

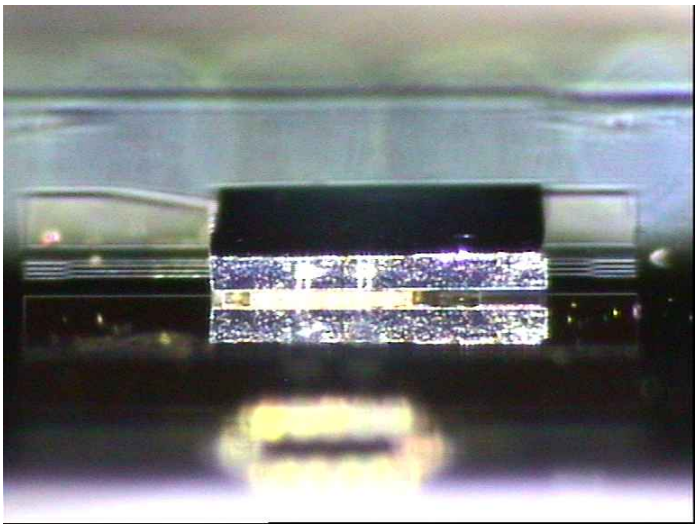


Figure 6.10: Assembled Mechanical Fit structure

high bonding energy. The bonding cycle was 320C with 20N of pressure for 45 seconds based on the process in [53]. While this high temperature cycle was necessary for this particular combination of metallurgy, future work should include work with MMIC chip pads with metals that are more compatible with gold. The final assembled structure is shown in Figure 6.10.

6.3 Power Amplifier Design

The MMIC amplifier used to demonstrate Mechanical Fit integration was designed to have high linearity for use in millimeter wave wireless networking (WLAN) and inter-vehicle communications (IVC) where the transmit power requirements are relatively low [1]. It was fabricated in a fully differential topology on a SiGe substrate using the Atmel SiGe2RF process. The zeroth level connections on this chip are Finite Ground CPW lines using transmission line stubs as matching networks for both the RF input and RF output. A circuit diagram of the power amplifier chip is shown in 6.11.

A layout of the chip with each of the pads labeled is shown in Figure 6.12.

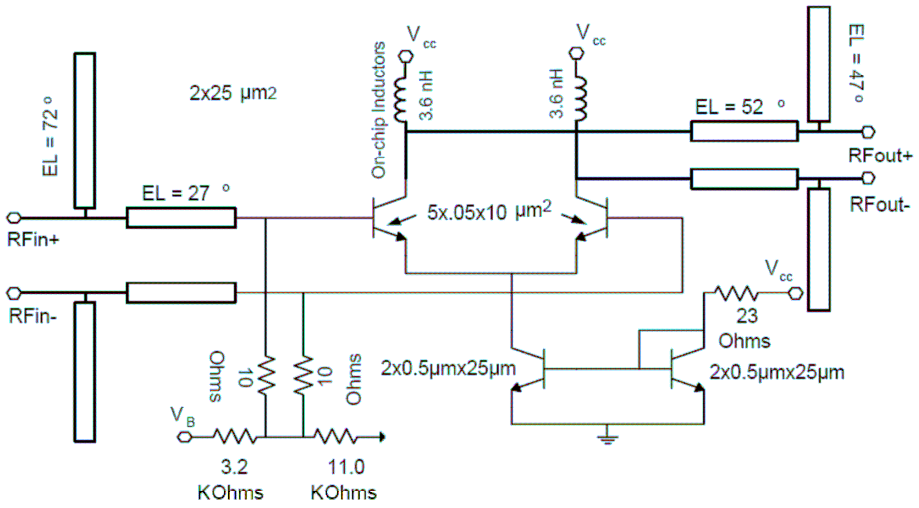


Figure 6.11: Circuit diagram of 30 GHz SiGe HBT Power Amplifier [1]

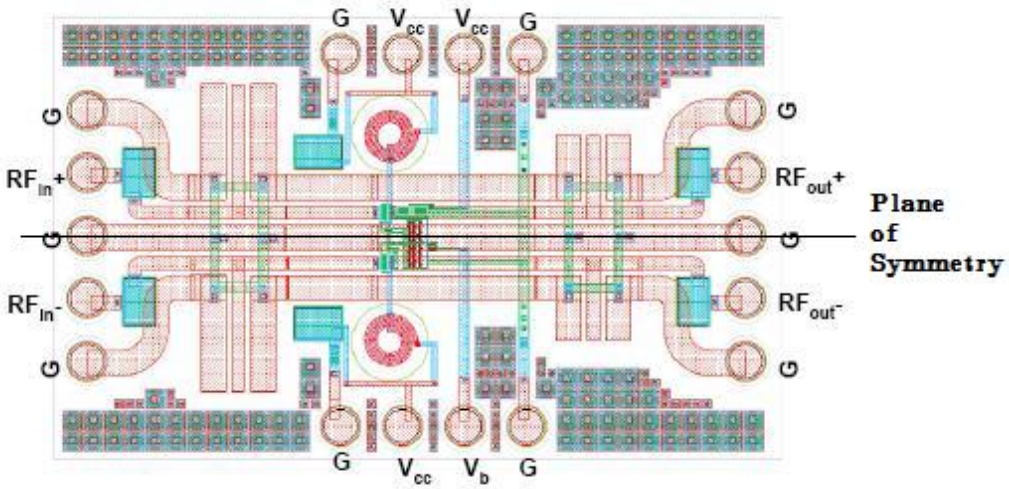


Figure 6.12: Layout of 30 GHz SiGe HBT Power Amplifier [1] showing pad connections

6.4 Measured Performance

In order to evaluate the performance of the Mechanical Fit structure, measurements were taken on both the passive CPW chip and the power amplifier chip. In both cases, the chips were measured before assembly (directly on the aluminum IC pads) and after assembly (on the pads on the carrier) in order to isolate the effects of the Mechanical Fit posts from the overall measurements. The small signal measurements were made using the same parameters defined in [1]. The Agilent 8364B Vector Network Analyzer was used to measure the 2-port S-parameters. The cables used were 2.92mm and the probes were Cascade Microtech ACP50 GSG 150um pitch. A Short-Open-Load-Thru (SOLT) calibration from 20 to 40 GHz was used to match the previous measurements on the power amplifiers.

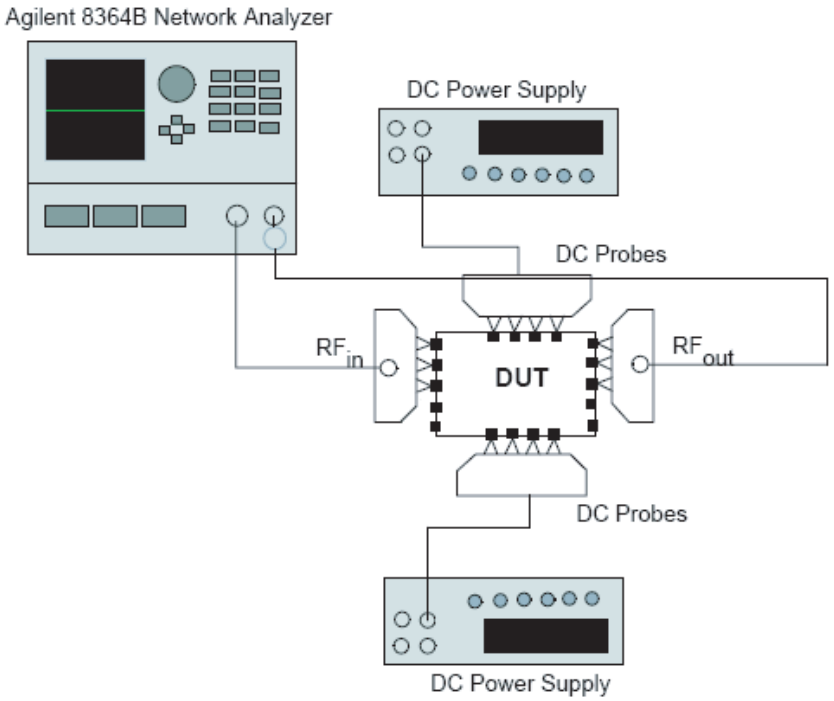


Figure 6.13: S-Parameter Measurement System

6.4.1 Passive CPW Chip

In order to characterize the Mechanical Fit structure alone, a Through-Reflect-Line (TRL) calibration routine was conducted to move the reference place of the mea-

surements up to the point at which the SU-8 begins. TRL calibration is performed by measuring through, reflect, and line standards fabricated on the same substrate material as the measured structures. The TRL standards fabricated on the high resistivity carrier substrate are shown in Figure 6.14. The reflect (short) standard length is equal to the distance the reference plane is offset from the probe pads. The through line standard is twice the reference plane offset. The two line standards calibrate for the band between 1 to 40 GHz. The reflect, through, and line standards are 600 μm, 1200 μm, 3475 μm, and 8150 μm in length, respectively.

Figure 6.14: Line and Reflect (short) TRL standards used in the Mechanical Fit calibration.

The insertion loss and reflection loss of the passive CPW transition, shown in Figure 6.1, are compared with HFSS[1] simulations in Figure 6.15 [49].

6.4.2 Power Amplifier Chip

The differential amplifier was measured on the single-ended VNA by measuring each channel (RF+ and RF- in Fig. 6.12) individually about the horizontal plane of symmetry. These single-ended measurements were transformed to differential mode using an ideal balun component within ADS. The voltage biasing was set to match the previous work [1]. 4-pin DC probes and power supplies were used to provide V_{CC} and V_B. The V_{CC} voltage was set to 2V and the V_B voltage was set to 1.5V. Under these bias voltages, the current drawn from the chip was approximately 30 mA. The

[1] High Frequency Structural Simulator is a 3-D finite element analysis simulation tool from Ansoft Corporation.

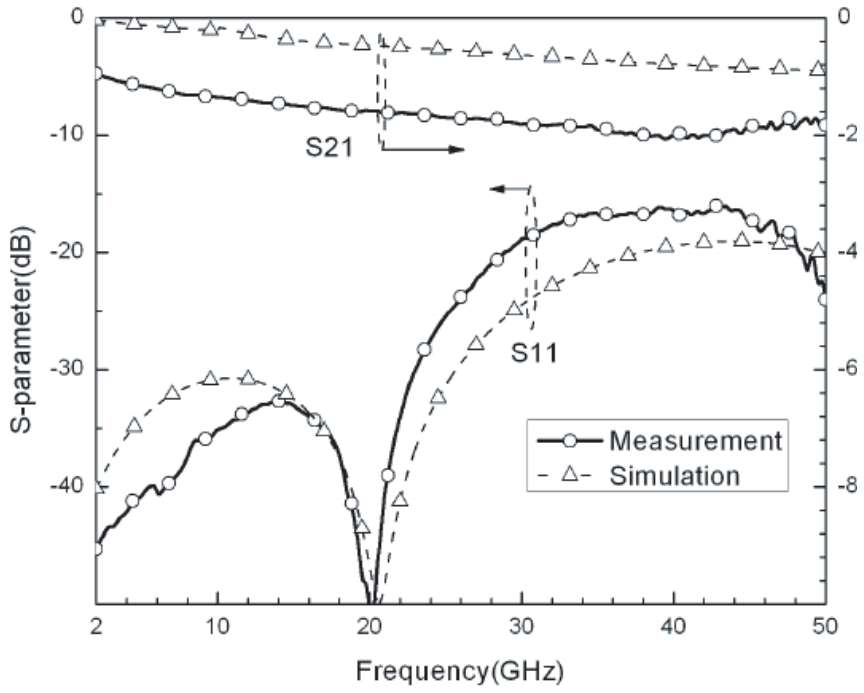


Figure 6.15: Passive CPW Chip S-Parameter Measurements

transmitted power (S21) and the reflected power for input and output (S11, S22) are shown in the measurements taken of the chips prior to Mechanical Fit processing (Fig. 6.16) and the measurements taken after mounting on carrier substrate with Mechanical Fit (Fig. 6.17).

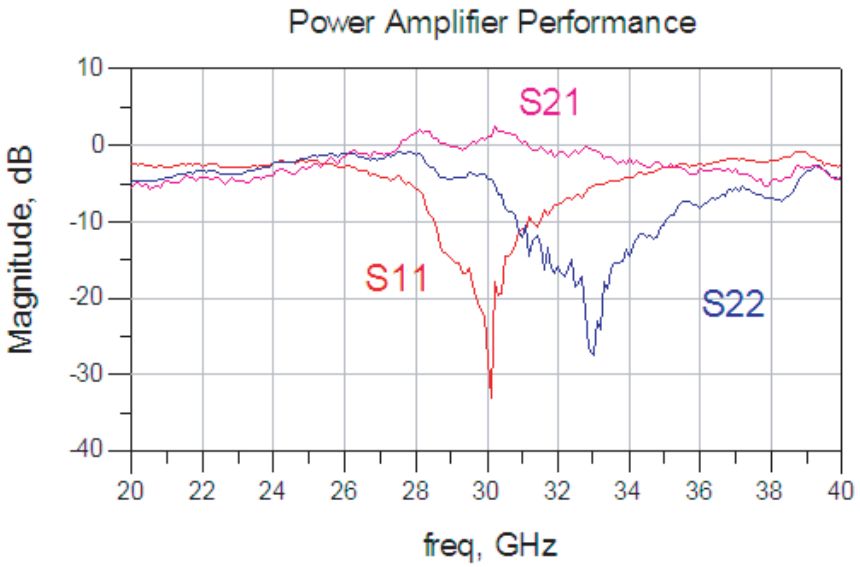


Figure 6.16: Power Amplifier Performance before mounting in Mechanical Fit

As can be seen, significant transmission loss was experienced in the Mechanical Fit case. Further discussion of these results is provided in section 6.6.

6.5 Transition Modeling

In order to further characterize the RF performance, simulations were conducted to model the transmission lines and posts. Lumped element models were created to determine the RF characteristics of the mechanical fit structure that could be contributing to the loss in transmission. The system was divided into the subsections shown in Figure 6.18: the carrier CPW sections, the vertical posts, and the power amplifier itself. The power amplifier block is an .s2p (Touchstone) file of the measured data for the PA chip before Mechanical Fit integration.

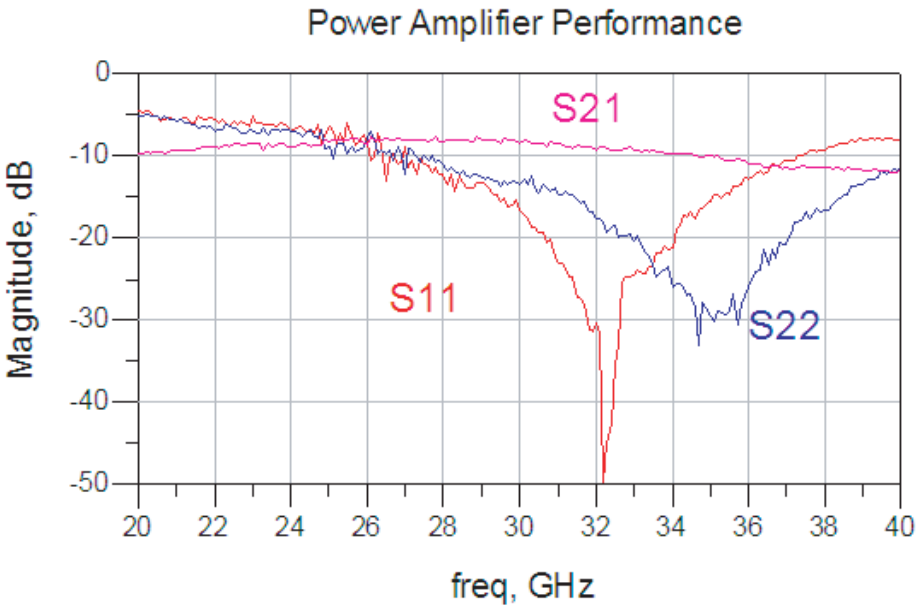


Figure 6.17: Power Amplifier Performance after mounting in Mechanical Fit

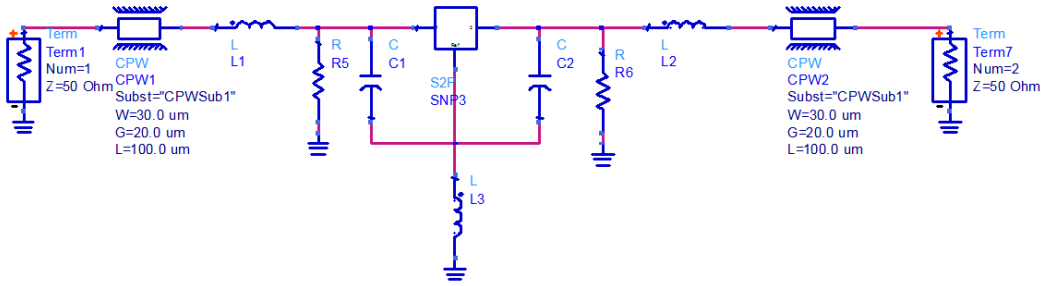


Figure 6.18: ADS schematic of total Mechanical Fit model

The Mechanical Fit vertical bumps were modeled as shown in Figure 6.19. The gold sections represent the electroplated gold bumps and the surrounding blue sections represent the SU-8. This model shows inductance and resistance intrinsic to the height of the bumps as well as the parasitic capacitance in between the bumps.

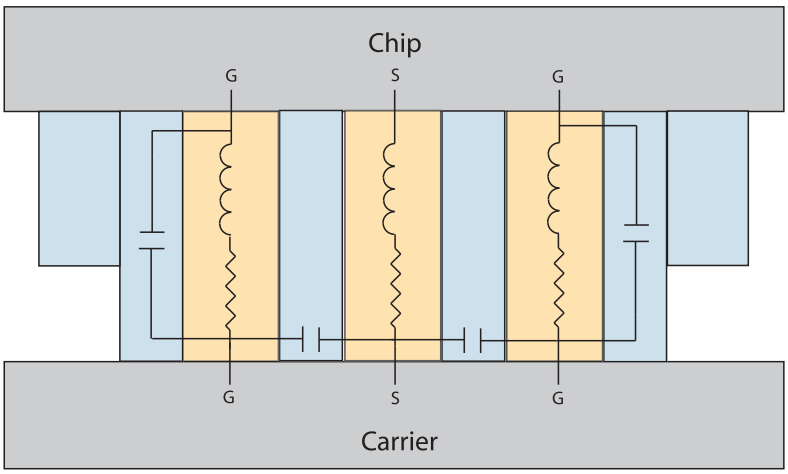


Figure 6.19: Lumped element electrical model of Mechanical Fit bump structure

The optimization was carried out by using ADS CPW models for the carrier sections, lumped elements for the Mechanical Fit elements (from Fig. 6.19), and a S2P data block for the chip data prior to SU-8 processing. The lumped element values were optimized until the overall S-parameters matched those of the Mechanical Fit data $after$ assembly. The values for each of the elements in the Mechanical Fit model are given in Table 6.1.

Table 6.1: Mechanical Fit Lumped Element Model Values.

Element	Res. [Ohms]	Cap. [fF]	Ind. [pH]
M. F. Signal	7	60	80
M. F. Ground	10	20	35

This overall lumped element model after optimization is compared to the measured data of the whole structure in Figure 6.20.

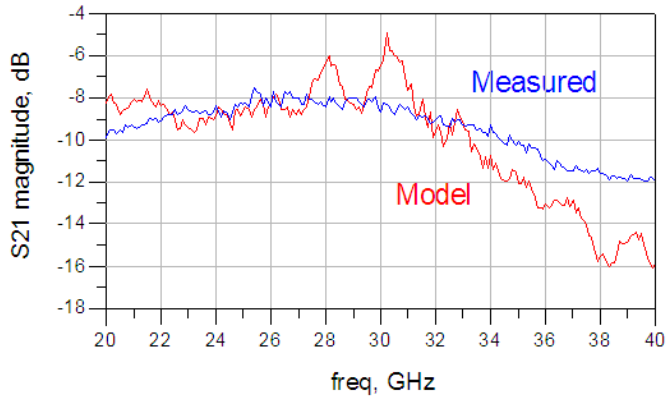
Further analysis of this Mechanical Fit transition model is given in the next section.

6.6 Discussion

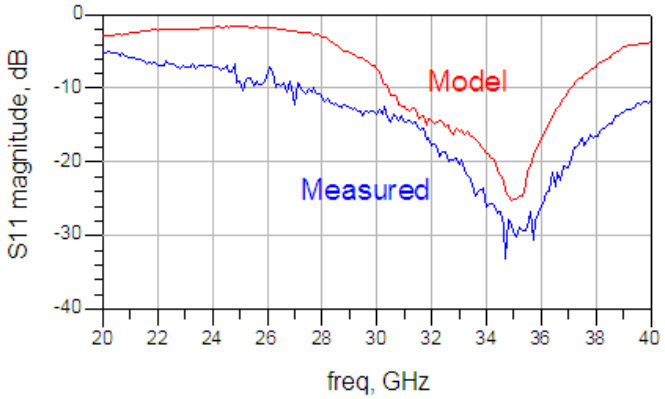
The proposed Mechanical Fit strategy for simplifying the vertical integration process through interlocking flip chip connectors has several potential benefits such as simplified flip chip assembly with improved alignment and bump mechanical support. This work has demonstrated a fabrication process for implementing the Mechanical Fit strategy and has uncovered some of the challenges that still must be resolved.

The electrical performance of the mounted power amplifier chip suffered from significant attenuation in the transmitted signal as well as shifts in the input and output impedance match. The lumped element model used to investigate these problems includes large resistances, capacitances and inductances, representing a poor joint in between one of more of the plated bumps and the power amplifier MMIC. A possible reason for this could be that the low thermal conductivity of the silicon ($1.3\ \frac{W}{cm \cdot K}$) could prevent heat from traveling to the joint during bonding. In the bonding set-up, heat was applied from the top of the chip and the bottom of the substrate. Therefore, more work is required to optimize the heating mechanism and bonding cycle. This is especially important due to the metallurgical junction between bare gold and aluminum used in this work. If the chip pads were coated with an UBM metal stack, such as indium or tin to promote metal wetting as defined in Chapter 4, prior to the bonding, it is possible that reflow could have taken place at a lower temperature and produced more robust joints.

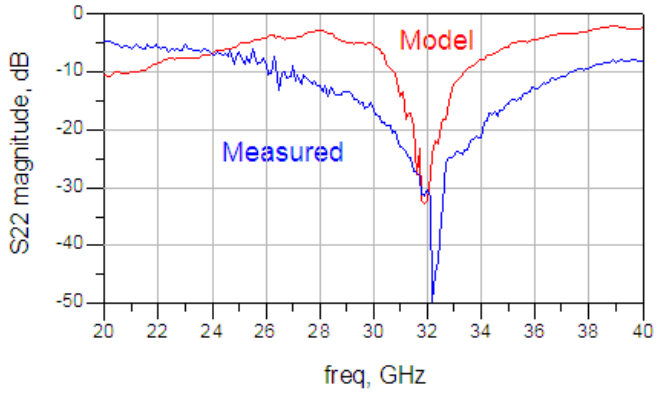
Another issue is that the Mechanical Fit interconnects contribute a significant impedance loading that must be compensated for in the matching network of the power amplifiers. The close proximity of the signal and ground flip chip bumps adds additional capacitance as well as the height of the transitions adds additional inductance to the power amplifier ports. Therefore in the future, this proposed Mechanical Fit interconnect process would need to be accounted for during design of the amplifiers themselves.



(a) S21 Insertion Loss



(b) S11 Input Reflection Loss



(c) S22 Output Reflection Loss

Figure 6.20: S-Parameters comparing simulated model and measurements

Chapter 7

Liquid Metal Interconnects

The objective of the liquid metal effort in this thesis is to demonstrate the use of low melting point metals in vertical RF transitions. Room temperature liquid metal connections can be advantageous in several ways: they can maintain electrical continuity during a wide range of thermo-mechanical stress, adapt to flexible substrates, and do not require elevated temperature processing steps.

CTE mismatch is the main contributor to failure in systems of heterogeneous materials. This issue arises due to adjacent components expanding at different rates due to material properties under temperature variations. When the two mismatched materials are in direct contact, as in the case of an underfill dielectric between stacked chips, the high-CTE material will exert a tensile stress on the low-CTE material at the interface, eventually leading to delamination. A similar situation occurs when the mismatched materials are mechanically bonded with solder bumps as in Figure 4.6. The high-CTE material bends and causes the bump to flex and often crack when cooled. A commonly used method to circumvent the CTE mismatch issue has been to use ceramic carriers whose CTE closely matches silicon. However, there are problems with this method when mounting components fabricated from materials other than silicon on the same ceramic carrier.

There has also been much interest in the ability to mount chips onto flexible carriers and this presents new challenges for flip chip packaging. Plastic or polymer carrier substrates are typically much lighter in weight than semiconductor or ceramic carriers and can be flexed and bent into various shapes for different applications [54]. For

example, polyimide carriers are being used to create space-saving, high-density folded packages that are becoming the standard in biomedical systems such as hearing aids and pacemakers [55]. These creative packaging schemes require interconnects that can reliably maintain contact despite the order of magnitude differences in CTE possible between the polymer carrier and the mounted semiconductor chip.

There is also a critical need for low temperature bonding processes. In many cases with standard solder bump flip chip bonding, the bonding cycle can be more stressful than operational thermal cycling. Therefore, low temperature bonding is advantageous when working with temperature sensitive components. This includes polymeric flexible substrates, active devices in MEMS and optical systems, large substrates that could bow and warp, and other components whose performance would be compromised by exposure to a high reflow temperature.

7.1 Liquid Metal Qualities and Applications

There are two main families of metal alloys that are liquid state at room temperature: mercury-based and gallium-based. Despite their reduced conductivity compared to other solid microelectronic metals, the fluid nature of these metals at room temperature opens up the potential for new applications. The thermal and electrical conductivities of these liquid metals are compared to other common microelectronics metals in Table 7.1.

Mercury has been historically used in various electrical applications [56][57]; however, its toxicity requires alternatives. Gallium alloys have emerged as a non-toxic alternative to mercury. The eutectic 62.5% Ga - 21.5% In - 16% Sn (commonly referred to as Galinstan) is liquid at room temperature, has slightly better conductive properties, and is much less toxic, making it a popular choice for conductive liquids. Much research has been conducted into new applications for Galinstan.

Since liquid metals can flow and wet to most solid metal surfaces, there has been much interest in their use as contacts for switches and relays. The conformality of

Table 7.1: Common metals and their melting points and conductivies.

Metal	Melt Point [°C]	Elec. Cond. [S/um]	Therm. Cond. [W/mK]
Mercury	-38.7	1.0	8.34
Ga Eutectic	10	3.46	55
Gallium	29.9	6.7	40.6
Indium	156.6	12.0	81.8
60 % Sn 40 % Pb	187	19.8	49
Tin	232	9.2	66.6
95 % Pb 5 % Sn	310	15.1	23
Aluminum	660	37.7	237
Silver	961	63	429
Titanium	1660	2.3	21.9
Gold	1065	45.2	317
Copper	1085	59.6	401

the solid-liquid metal interface reduces the contact resistance and can improve power handling due to reduced risk of electromigration [58]. Similarly, a recent study has investigated the ability to manipulate Galinstan droplets using magnetic fields to potentially make waveguide slot switches [59].

Another common application for liquid conductive metal alloys is chip cooling for heat management. Metal alloys have much higher thermal conductivities than water, oils, and other liquids. The conductivity can be further improved by suspending nanoparticles within the liquid solution. By using carbon nanotubes in a solution of 20%, the thermal conductivity can be more than doubled [60].

As interconnect materials, low melting point metals have been investigated to reduce the reflow/curing temperature cycle. Gallium solutions with solid metal suspensions have been demonstrated in a method similar to solder paste [61]. The suspension can be stencil patterned and then cured to harden the material. The solid and liquid metals react during the curing process and create strong intermetallic solids. Another approach is to use metals that transition back to the liquid phase at high temperatures [62]. A key consideration with this approach is using interface metals between the bumps and the substrate that wet well and also prevent metal diffusion that could damage the joint as the interconnects continually melt and harden.

7.2 Liquid Metal Transition Design

There are several novel techniques used in the demonstration of liquid metal chip interconnections in this work. These include high aspect ratio gold pin plating, solidified epoxy underfill that defines the shape of the interconnections, and low melting point gallium alloys as the bump material. A diagram of the completed structure is shown in Figure 7.1.

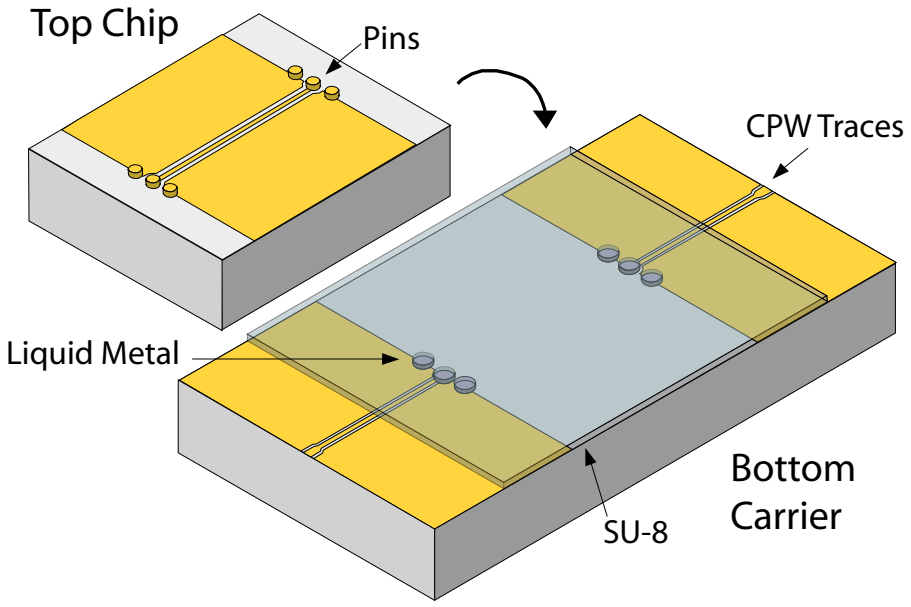


Figure 7.1: Diagram of Liquid Metal Flip Chip Interconnect Scheme

The test chip and carrier were designed to demonstrate these new techniques using a well-known coplanar waveguide (CPW) to CPW transition scheme [11][18]. The test chip in this study includes short gold pins that fit into sockets on the carrier. The sockets on the carrier are filled with the liquid metal, allowing the top chip to "float" in place when mounted. The pins on the top chip are feed coplanar waveguide (CPW) traces. The sockets on the carrier are also connected to the probe pads through CPW traces. In this way, the transitions can be characterized by their electrical characteristics between the probe pads. The layout and profile of the liquid metal structure is shown in Figure 7.2.

In Figure 7.1, the gold traces on the bottom carrier represent CPW transmission

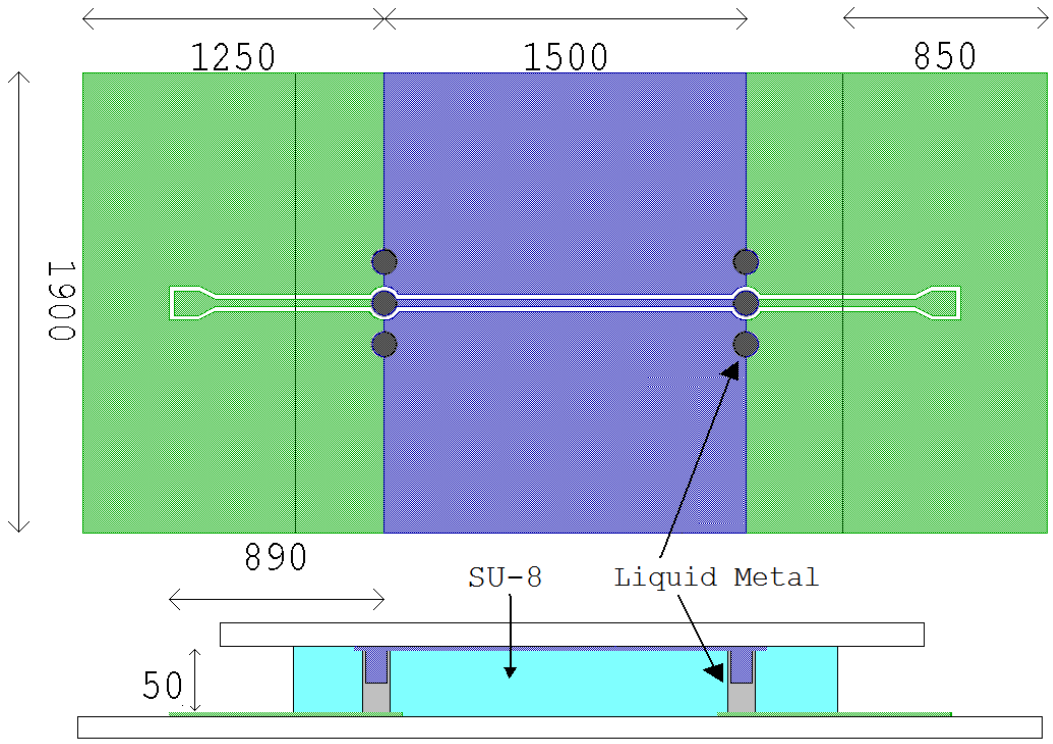


Figure 7.2: Top view layout and side view profile of the Liquid Metal structure

lines that can be probed using GSG probes. The SU-8 layer is patterned such that the probe pads are accessible to the probes. The electrical connection is extended vertically through the gray liquid metal cavities in the SU-8. CPW lines continue on the top chip to form the completed circuit.

7.2.1 Process Flow

Liquid metal test structures were fabricated on low resistivity silicon substrates for initial process development runs. Low resistivity (20 ohm-cm) silicon is easily available, inexpensive, and convenient for experimentation. Subsequent runs to demonstrate the RF performance of the interconnect scheme were fabricated on high resistivity (500 ohm-cm) silicon.

To ensure uniform CPW traces on the chip and carrier sections, the initial metal deposition is performed on a single wafer before dicing the wafer into top and bottom sections. The process flow begins for both the top and bottom parts of the interconnect structure by evaporating a thin layer (500 Å) of titanium and a thicker layer (5000 Å) of gold onto the wafer surface (Fig 7.3a). On the top chip side, the Ti layer serves as an adhesion layer for the gold coplanar traces as well as a seed layer for the gold pin plating. Next, a positive tone photoresist (S1813) is used to create a 2 μm thick pattern for etching the gold layer to form the CPW traces (Figs 7.3a and 7.4b). With the metal patterned, the top and bottom parts are separated because of their different further processing steps.

The bottom carrier is then spun with SU-8 and patterned to form the underfill dielectric that will hold the liquid metal (Fig 7.3b). The SU-8 remains as a permanent socket in which the top chip fits. After SU-8 deposition, additional S1813 photoresist is used to protect the exposed gold probe pads from the liquid metal deposition. Because this photoresist is intended to cover the probe pads and it is undesirable to get into the liquid metal cavities, the photoresist is selectively deposited using a micro-syringe instead of a typical spin on procedure. With the permanent SU-8 and the sacrificial S1813 in place, the liquid metal is dispensed using methods discussed in the next section (Fig 7.3c). The liquid metal typically only adheres to other metal surfaces, making any residual liquid metal easily removable by cleaning with acetone. This cleaning also removes the sacrificial photoresist, leaving only the intended SU-8

with liquid metal in the cavities.

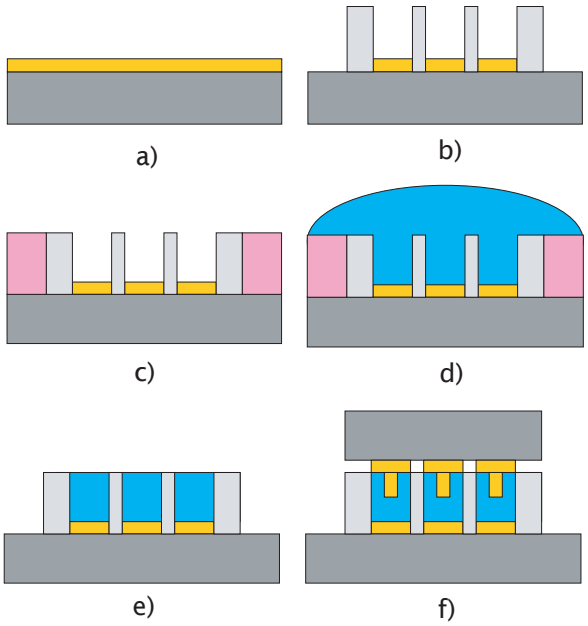


Figure 7.3: Liquid Metal Bottom Carrier Process Flow

The top chip processing is continued by spinning on the sacrificial thick film KMPR that serves as a mold for the gold pins (Fig 7.4c). The gold pins are then electroplated to be tall enough (roughly 20-30 μm) to hold the top chip into position when mounting onto the carrier (Fig 7.4d). With the pins fabricated, the wafer is diced to separate individual chips with the KMPR still intact (Fig 7.4d). The mold protects the bumps from damage by the dicing saw. To allow for continued batch processing, the wafer is not completely separated by the saw. The blade is kept roughly 100 μm from the tape while passing across the wafer. This permits the whole wafer to be further processed, and then each chip can be snapped out when ready. After dicing, the KMPR mold is removed through a chemical stripping bath recipe (Fig 7.4e), described in Appendix C. To complete the top chip processing, the Ti seed layer is etched away and the individual chips are snapped apart (Fig. 7.4e).

The ability to create such free standing metal pins is crucial to fitting the top chip into the bottom carrier socket. In order to create moderately tall, straight posts (~20

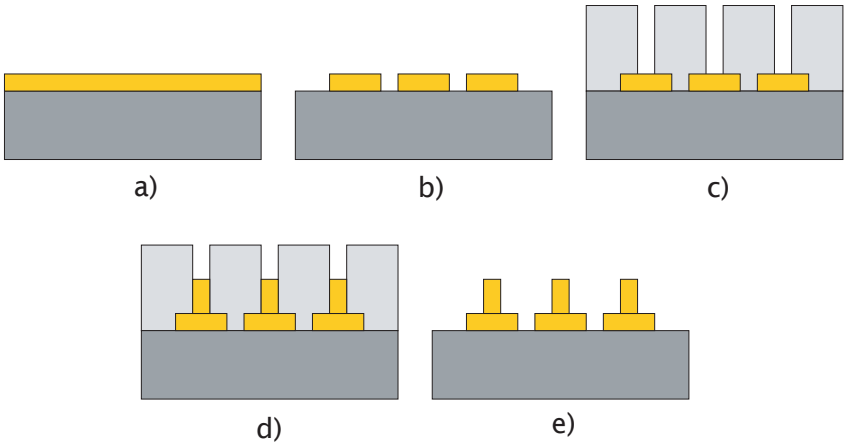


Figure 7.4: Liquid Metal Top Chip Process Flow

um), a thick film mold is required that can be deposited thicker than desired height of the posts so that the posts do not over-plate and mushroom out of the post hole. The other main processing steps, such as thick film processing and electroplating, were described in Chapter 5. Step by step instructions for the different procedures are included in Appendix A-C.

In this study, the fabricated gold pins showed extended vertical sidewalls, with an open center as shown in Figure 7.5. It is believed that this odd structure is caused by sputtering of the seed layer during the de-scum of the KMPR mold. The RF plasma causes a very small amount of the gold seed layer to redistribute along the sidewalls of the mold cavity, extending the seed layer vertically. In this situation, the sidewalls begin to plate at an equal rate as the base. If carried out long enough, this leads to completely filled mold cavities and tall gold bumps equal to the mold height. However, this is undesirable in this experiment because the gold bumps are not intended to displace large amounts of the liquid metal volume. As it turns out, the resulting open center bumps prove to be beneficial because the sharp sidewalls can penetrate any oxidation on the liquid metal surface while allowing the liquid to fill the hollow center of the bump. If desired, however, the de-scum step can be altered to use Inductively Coupled Plasma (ICP) instead of RIE plasma to remove the residual photoresist without sputtering the underlying seed metal.

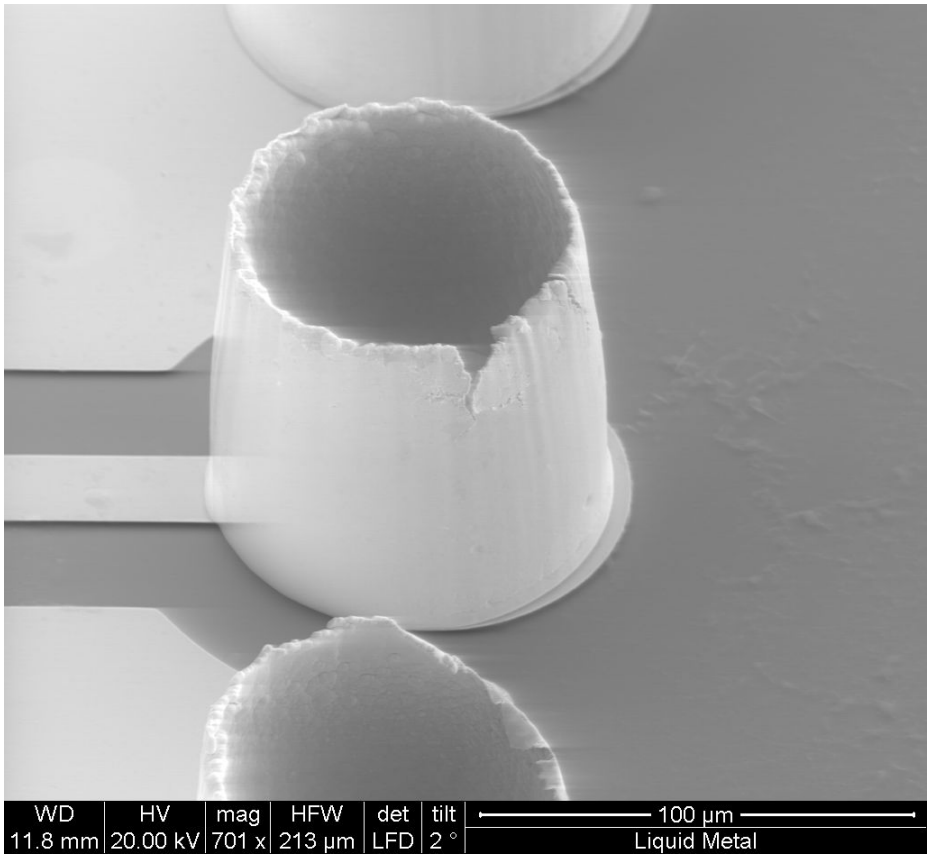


Figure 7.5: SEM of Single Pin Electroplated Using KMPR Mold

After processing, the top chips are mounted onto the carrier using a flip chip bonder to align the pins with the cavities. The bonder uses a vacuum tool to pick up the top chip from its backside and then place it in position on top of the carrier. The bonding only requires enough pressure to insert the bumps into the liquid (> 5 Newtons).

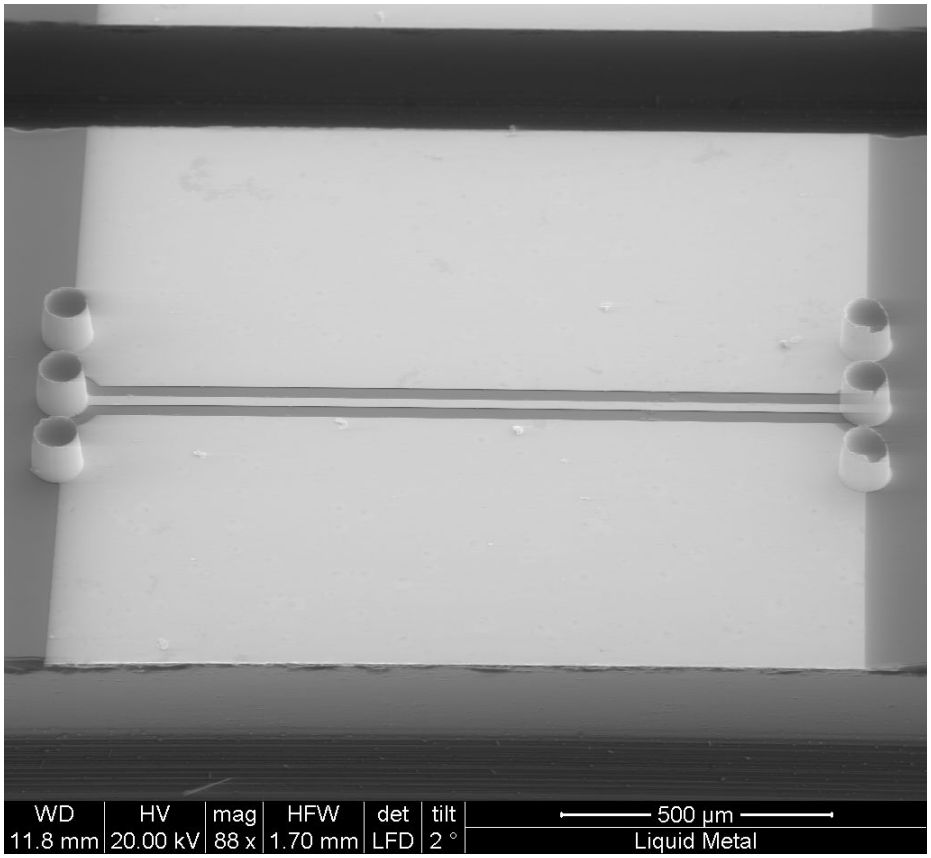


Figure 7.6: SEM of of CPW top chip with electroplated pins

The process of depositing the micro-scale liquid is described in more detail in the following sections. This process could easily be adapted to other materials as all of the metallization and processing is on the substrate surface.

7.3 Liquid Metal Deposition

Considering the small volume of the liquid metal sockets, special techniques are required to deposit a consistent amount of liquid in each cavity. In this work, the

Table 7.2: Liquid Metal Deposition Methods.

Method	Liquid in Socket	Consistency	Complexity
Micro-Pipette	Variable	Low	Low
Pin Dip	Little	Medium	Low
Squeegee	Full	Medium	Low
Evaporation	Little	High	High
Electrostatic	Full	Medium	High
Ink-Jet	Variable	High	High

sockets are 100 x 100 μm in area and 50 μm tall for a volume of 0.5 x 10^{-6} mL. This size represents a balance between a size that is physically possible to fabricate and a size that is comparable to the feeding coplanar traces.

Several techniques were investigated for the deposition of the liquid metal: using a micro-pipette to deposit small droplets in the cavities; dipping the gold pins into the liquid metal prior to the mounting; and using a stencil-like pattern to "squeegee" the liquid into the cavities. More exotic methods include evaporating the liquid metal in a vacuum chamber, electrostatically attracting the liquid into the cavities, and using an ink-jet system to squirt small amounts of the liquid into the cavity. These deposition techniques are compared in terms of the volume of liquid that is deposited into the socket, the precision of the liquid volume in each socket, and complexity in Table 7.2.

This project was mainly concerned with demonstrating the feasibility of using liquid metals as RF interconnect materials, so only the techniques that could easily be performed were tested. The first strategy tested the ability to drop small liquid volumes from a pipette. A Hamilton 0.5 μL syringe was used to test this micro-pipette strategy. While this was the smallest syringe generally available, the tip still produced droplets that were too large for the given cavity size. A critical problem with this strategy on this size scale was that the surface tension of the liquid metal prevents small droplets from forming and therefore makes it difficult to dispense. Another strategy that was attempted was to dip the gold pins into a liquid metal reservoir so that drops could adhere to the ends of the pins. The difficulty in this strategy was ensuring that the reservoir of liquid was flat enough on the surface such that all of the pins could contact the liquid without the liquid touching the CPW traces on the chip surface.

The most promising liquid metal deposition technique was to "squeegee" the liquid into the cavities in a similar manner as screen printed solder paste. In order for this method to work, a permanent SU-8 stencil was used to pattern the liquid into the SU-8 cavities. Additional sacrificial S1813 photoresist is used to keep the liquid from adhering to unintended areas, namely the gold CPW probe pads. Drops of the liquid metal were broadly deposited from a dropper onto the wafer surface. The drops were then swept into the cavities using a rubber squeegee. The liquid slides across the polymeric SU-8 and is forced into contact with the gold in the bottom of the cavities. With the liquid in place, acetone is used to clean off excess liquid metal as well as to remove the sacrificial S1813 photoresist. A completed bottom carrier with the liquid metal in the cavities is shown in Figure 7.7.

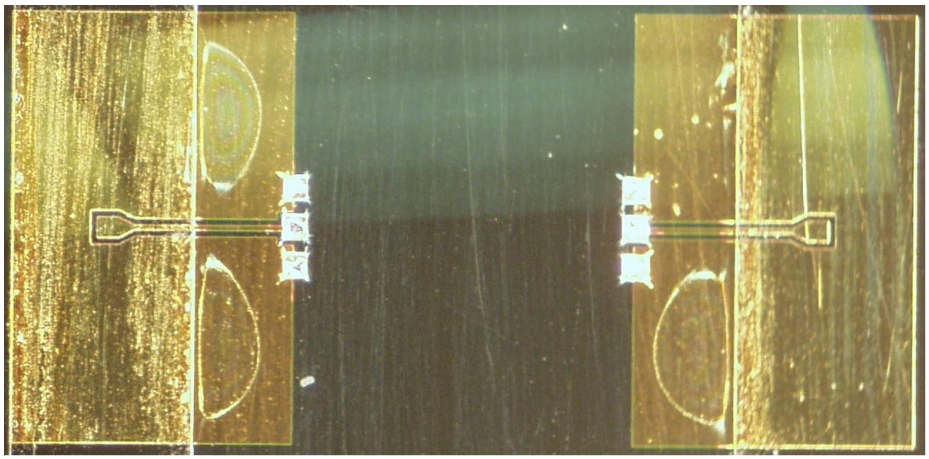
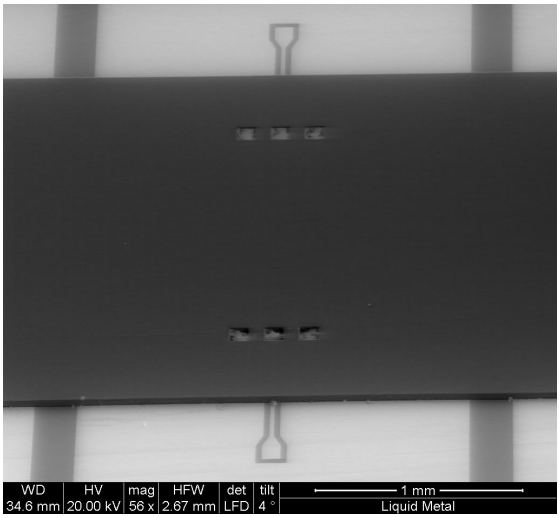


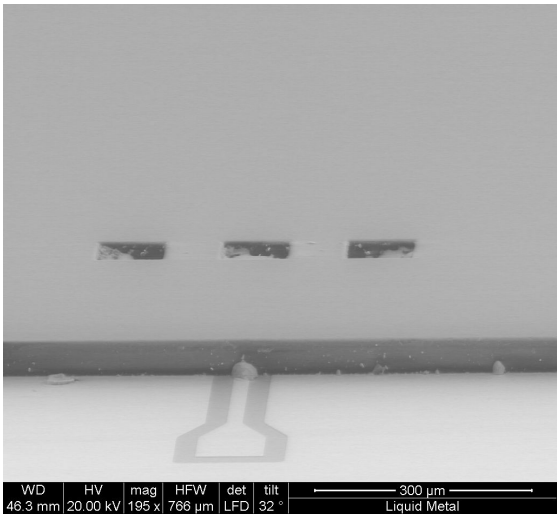
Figure 7.7: Optical camera image of bottom carrier showing liquid metal in SU-8 cavities

This method completely fills the cavities. SEM images of the surface of the liquid metal in the cavities are shown in Figure 7.8.

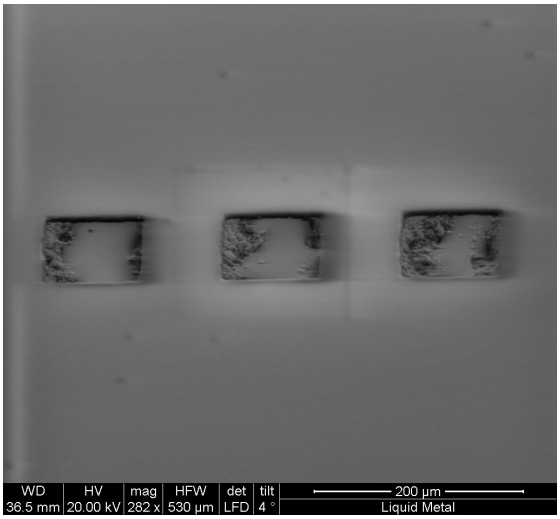
Figure 7.8(d) shows some oxidation of the gallium alloy along the edges of the surface. While the gold posts can generally break through this oxidized surface, other deposition techniques discussed in section 7.3 could prevent oxidation so that the liquid surface is smooth and oxide free. The oxide could be a factor in the somewhat high DC resistance of the liquid metal vertical interconnects, to be discussed further in the next section.



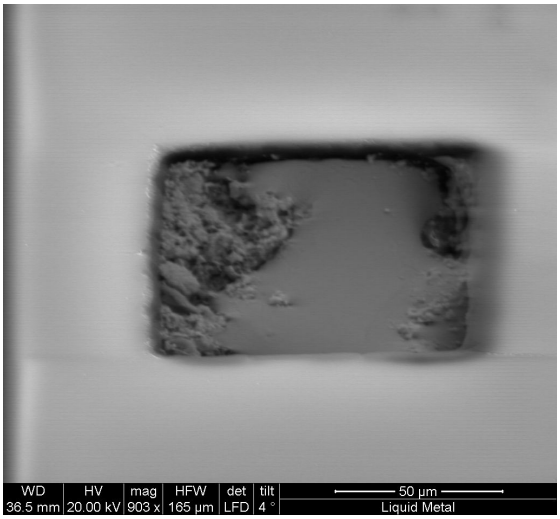
(a) SEM of total bottom carrier



(b) SEM of one side of bottom carrier at 75 degree tilt



(c) SEM of one side of bottom carrier at 45 degree tilt



(d) SEM of single cavity at 45 degree tilt

Figure 7.8: SEM images of bottom carrier with liquid metal

7.4 Measurements, Simulations and Analysis

The liquid metal interconnects were characterized using RF and DC measurements. The RF measurements were used to determine the loss per transition using the Galinstan alloy as the conductor material. The DC measurements were used to determine the contact resistance of the electrical path.

7.4.1 RF Measurements

The RF performance of the vertical transition was measured using the same test setup as used for the Mechanical Fit structures in Figure 6.13. The calibration routine for the liquid metal measurements was the same TRL procedure used on the passive Mechanical Fit structures (Fig. 6.14). In this way, most of the losses from the bottom carrier are accounted for in the calibration. TRL is performed using standards defined on the silicon substrates themselves. The necessary standards included a thru section, short sections for both ports, and three line sections to calibrate over the band of 1 to 40 GHz.

An overall measurement of insertion loss, including 200 μm of CPW on the low-resistivity carrier after TRL calibration, liquid metal vertical transition, and 1500 μm of CPW on the high-resistivity top chip, is shown in Figure 7.9. The transitions were also simulated using HFSS, a three dimensional Finite Element Analysis tool for modeling RF components, to compare the measured values to theoretical calculations. A 3-D model representation was drawn to match the physical properties and the material properties used are given in Table 7.3. The resulting insertion loss of the simulated structure is also shown in Figure 7.9.

Sections of CPW with known lengths (1500 μm) were fabricated on both low and high resistivity silicon substrates in order to determine their respective attenuation constants, α. Figure 7.10 shows α vs. frequency for both substrates.

Given these results, calculations were performed to isolate the effects of the vertical liquid metal transition alone. Assuming the total insertion loss is a sum of the insertion loss of each of the components as in 7.1, the individual transition loss can be

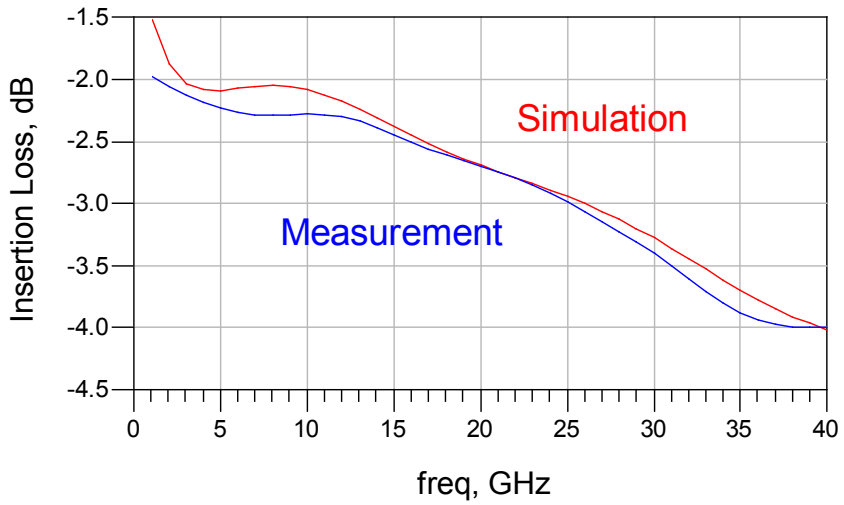


Figure 7.9: Insertion loss of complete liquid metal assembly

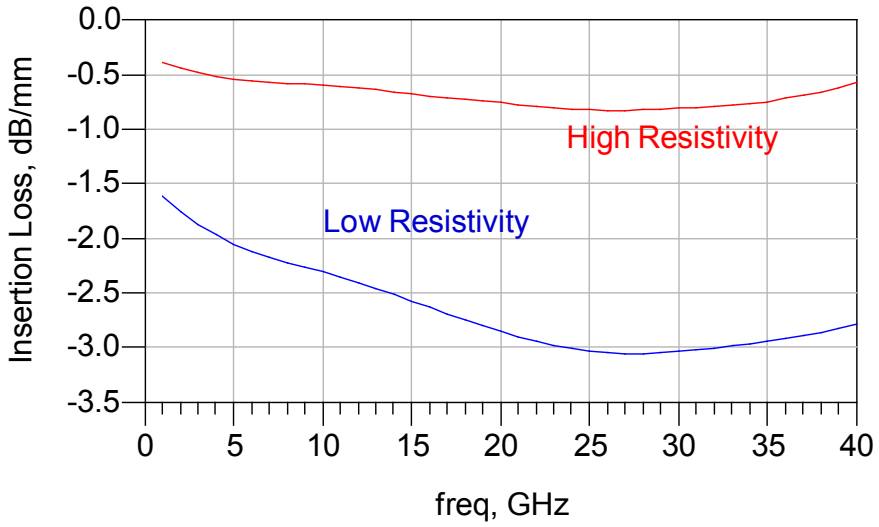


Figure 7.10: Insertion loss of CPW on silicon, measured on 1.5mm line. High resistivity = 500 Ω/cm and Low resistivity = 20 Ω/cm

Table 7.3: HFSS Simulation Material Properties.

Material	ϵ_r	Loss Tangent	Conductivity[S/m]
Galinstan	-	-	500000
SU-8	4.0	0.08	-
High Res. Silicon	10.5	0.02	0.8
Low Res. Silicon	10.5	0.02	8

determined through 7.2.

$$\text{Total Loss} = 2 \times \text{Carrier Loss} + 2 \times \text{Transition Loss} + \text{Top Chip Loss} \tag{7.1}$$

$$2 \times \text{Transition Loss} = \text{-}10 \cdot \log\left(\frac{|S_{21}|^2}{1-|S_{11}|^2}\right) - \alpha_{chip} \cdot L_{chip} - \alpha_{carrier} \cdot L_{carrier} \tag{7.2}$$

In 7.2, α is the attenuation constant of the CPW transmission line and L is the length of the line.

The measured transition loss of the de-embedded liquid metal interconnect as well as the simulated HFSS transition loss are shown in Figure 7.11.

The measurements shown exhibit acceptable loss considering the proof-of-concept materials used. In all of these structures, low resistivity silicon is used as the carrier substrate material. While most of the loss associated with the low resistivity CPW lines is removed through TRL calibration, some of the remaining loss can still be attributed to it. These results show that the liquid metal interconnects themselves do not contribute a prohibitively large loss factor and the results could likely be improved through more insulative substrate materials.

7.4.2 DC Measurements

The DC electrical resistance was also measured for the liquid metal transitions. DC probes were put down onto the pads to source a DC current through the metal traces and the corresponding voltage was measured. The signal and ground traces were measured independently.

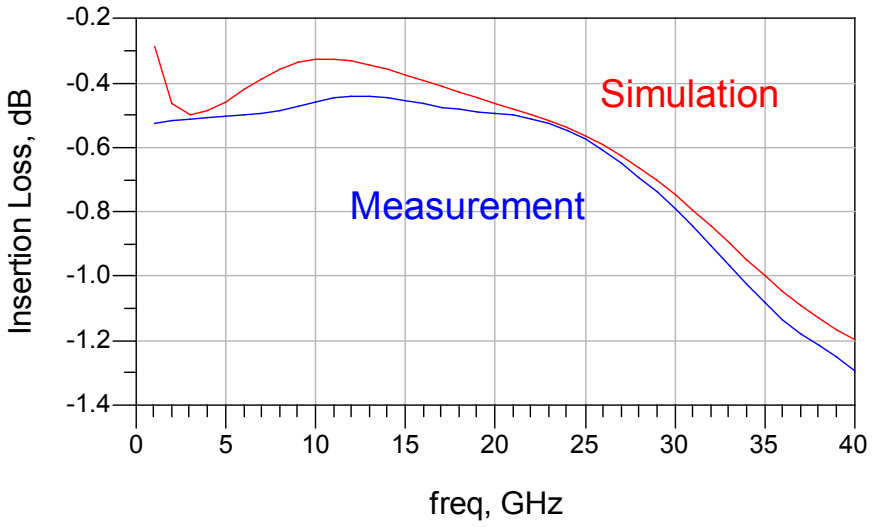


Figure 7.11: Insertion loss of single liquid metal transition

Interestingly, it was observed that the DC resistance of the traces varied with time and the initial excitation current applied. This behavior is shown in Figure 7.12. For each curve on the graph, DC current was applied for 1 minute and then the resistance was measured (using a significantly smaller sense current) over time.

This change in resistance is believed to be due to I^2R heating that causes the liquid to expand within the cavity as shown in Figure 7.13. This liquid expansion creates more contact surface area between the liquid metal and the gold bumps, thus lowering the measured resistance.

7.5 Summary

An approach for using a room temperature liquid metal as the interconnect between stacked chips has been discussed. The advantage of a liquid transition is that the structure will not experience fatigue under continued thermo-mechanical stress (CTE mismatch) like traditional solid solder transitions. The liquid metal used in this work is a gallium eutectic alloy (Galinstan) with a melting point of 10°C. Since the vertical transitions are liquid, they require a solid structure to maintain volumetric

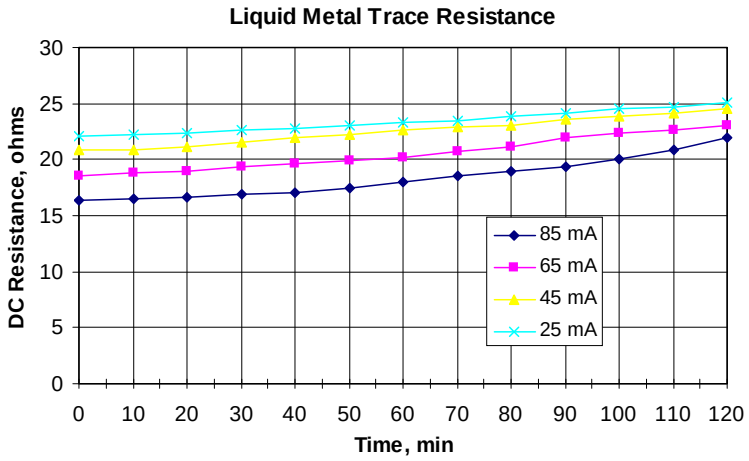


Figure 7.12: DC resistance vs. time after current was turned off for varying magnitude current

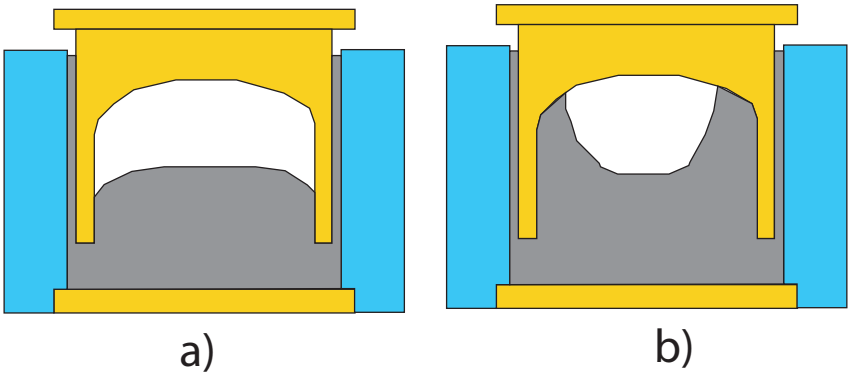


Figure 7.13: Liquid expansion due to heating from DC current

shape. This solid structure, fabricated in SU-8, was formed into a socket and filled with the liquid metal. Pins on the top chip were inserted into the socket, making contact with the liquid metal. A process flow for this liquid metal interconnect was discussed. This included liquid metal deposition into the SU-8 socket, electroplating of pins on the top chip to fit into the socket, and a special dicing procedure to protect the pins from breakage by preserving the electroplating mold until dicing is complete. The assembled structures with chips in the carrier sockets were measured using RF and DC tests. The RF measurements showed that the liquid metal interconnects contribute an insertion loss of < 0.5dB to 20 GHz. The DC measurements showed that the conductance of the transition increased with a higher applied DC current. This effect is believed to be due to thermal expansion of the liquid, causing greater surface contact between the liquid metal and the solid gold pins.

Chapter 8

Conclusion

The objective of this thesis was to develop new strategies for vertical heterogeneous integration for RF microwave/mm-wave applications. These applications include automotive radar, remote sensing, wideband terrestrial and satellite communications, and imaging. It has been shown that vertical integration allows reduced size and weight electronic systems while maintaining optimal performance through heterogeneous semiconductor material integration and minimal length interconnects.

Vertical interconnects tend to be much shorter than lateral interconnects and therefore have reduced parasitic resistance, capacitance, and inductance. This is especially important at higher frequencies where these parasitics become more influential. The power consumption of the system can also be reduced through vertical interconnects. In 2-D CMOS circuits, up to 50% of the chip power goes into driving long, global interconnects and this can be significantly reduced by stacking active circuitry with short, vertical interconnects.

Heterogeneous integration allows each system component to be fabricated in its optimal technology, thereby maintaining optimal system performance. While monolithic SoC integration strategies yield the smallest overall size, they sacrifice performance as, for example, the RF components may have higher gain and efficiency in III-V semiconductor technologies as opposed to CMOS Si. Also, the planarity of SoC on-chip passives limits their quality factor and size compared to off-chip three-dimensional passives that are available in other heterogeneous integration strategies. The most efficient integration technique for heterogeneous systems is to vertically stack the sys-

tem component chips on top of each other. In this way, the interconnections between chips are minimized to mitigate parasitics, and lateral real estate is conserved.

In order for vertical heterogeneous integration to be successful up to 100 GHz and beyond, chip scale packaging must combine various system components and assemble them to a carrier with very little impact on individual component performance. Flip-chip bonding has the greatest potential for use in the microwave/millimeter-wave regime to due its short, vertical metallized bumps that can be fabricated on size scales that maintain the characteristic impedance of the signal paths. Flip chip bonding also enables efficient chip stacking and connection between multiple substrate layers with through-substrate vias.

8.1 Summary

This thesis focused on structural and material methods for improving flip chip bonding for use in vertical, heterogeneous integration strategies. The first method presented is an interlocking structure, referred to as Mechanical Fit, that aids in stacking assembly and mechanically supports the mounted chip. The second method presented, referred to as Liquid Metal Interconnects, employs low melting point metals as the interconnecting vertical conductors.

8.1.1 Mechanical Fit

The interlocking structure is fabricated from SU-8, a thick film epoxy photoresist that can be photolithographically patterned with high aspect ratio (>10:1). A prototype process flow for adding the SU-8 structure to previously fabricated, diced chips was developed including bulk micromachining of a sacrificial wafer to allow planarized spin-coating on the few mm^2 chips. However, it should be noted that the proposed structures could be added as final back-end of line steps of the IC process flow prior to wafer dicing.

This Mechanical Fit strategy was employed in the integration of a 30 GHz SiGe HBT power amplifier. SU-8 was added to the power amplifier chip to demonstrate the potential of Mechanical Fit with active devices. A passive chip Mechanical Fit

structure was also fabricated and tested. RF measurements were performed and a lumped-element model was created to characterize the interconnects. On the passive structures, the Mechanical Fit contributed less than 0.25 dB of insertion loss at 40 GHz. However, the structure integrated with the power amplifier chip added 8 dB of insertion loss at 30 GHz.

8.1.2 Liquid Metal Interconnects

A fabrication technique for depositing gallium alloys such as Galinstan that are liquid at room temperature as vertical interconnects in a coplanar waveguide transition scheme was developed. The advantage of liquid interconnects is that will not experience stress and fatigue due to CTE mismatch and thermal cycling like traditional solid metal (solder) interconnects. Another key feature of this proposed method is that assembly can be performed at room temperature.

SU-8 was used on the carrier side as a mold to form cavities that shape the liquid metal. A passive chip with CPW lines and released gold pins was fabricated and plugged into the liquid metal-filled cavities on the carrier. Electrical measurements, both DC and RF, were made on the assembly. The RF measurements showed that the Liquid Metal Interconnects contribute less than 0.5 dB of insertion loss up to 40 GHz as well as led to the characterization of the Galinstan and SU-8 materials used in this work. The DC measurements showed that the interconnect resistance could vary from 16 to 25 Ω based on the DC current heating and expanding the conductive liquid.

8.2 Future Work

Several fabrication improvements can be made to enhance the assembly and performance of the proposed strategies.

8.2.1 Mechanical Fit

The insertion loss of the proof-of-concept amplifier structure was significantly higher than expected. This is most likely due to a poor aluminum-gold junction that prevents proper contact between the chip pads and carrier bumps. Possible resolutions for this include: metallurgical interface layers, such as In or Sn, to enhance the fusion of the chip pads to the gold microbumps; cleaning of the pad metal prior to assembly; and an improved bonding cycle that focuses the energy at the metal junction.

As described in Chapter 5, interface metals are used to transition between the metals of the chip pads and solder bumps. These layers isolate the pads from metal diffusion, promote adhesion, and enhance the ability of the bump to wet to the pad metals. In this application, a metallization stack of Al-Ti-Sn-Au on the chip pads is recommended. The Ti layer prevents diffusion, the Sn layer promotes wetting, and the Au layer promotes bonding and adhesion to the gold bumps.

A cleaning cycle prior to assembly could help remove any contaminants from the metal surfaces. This will likely improve the electrical continuity of the bond. This cleaning procedure could either be a short acid rinse or an O_2 RIE cycle.

A further issue with the flip-chip assembly cycle is that the heat must travel through the semiconductor substrate to reach the bonding junction. This can be remedied through ultra-sonic excitation. Using ultra-sonic excitation can add energy to the bond without increasing the temperature or pressure. However, mechanical robustness of the SU-8 and bump structure must be verified through thermal cycling experiments.

8.2.2 Liquid Metal Interconnects

As a proof-of-concept implementation, the liquid metal interconnects show reasonable electrical performance. Mechanical and thermal tests have yet to be performed.

The liquid metal deposition method employed was very simple in order to evaluate the liquid metal functionality. As shown in the SEM images (Fig. 7.8), there were signs of oxidation around the edges of the SU-8 cavities. This could possibly be avoided through alternative deposition methods described in section 7.3. Also, the

conductivity of the liquid metal could be improved through the addition of metallic nanoparticles [60].

In addition, the openness of the electroplated Au pins could be improved through a pulsed electroplating process that could help evenly distribute the Au solution within the electroplating mold. A long period of forward DC current followed by a short period of reverse DC current could help with the electroplating uniformity.

While there are still a number of process improvements that could be made, the liquid metal interconnect strategy was found to be promising and viable. In the future, active circuits (e.g. microwave PA) demonstrating this technique should be performed.

Appendix A

Photolithography Recipe for S1813

S1813 is a thin film, positive tone photoresist used in this work to pattern deposited thin film metal and oxide layers. This recipe is based on the S1813 datasheet[63].

1. Wafer cleaning. Dip wafer in HF for 15 seconds, DI water rinse
2. Spray 5 seconds of Acetone followed by 5 seconds of Methanol followed by 5 seconds of Isopropal Alcohol. Continue spinning for 1 additional minute.
3. Dehydration bake at 120°C for at least 1 minute.
4. Pour S1813 photoresist onto wafer such that 2/3 of wafer is covered.
5. Spin wafer at 3000 RPM for 45 seconds to obtain a film thickness of 1.5 μm. Ensure that there are no streaks or bubbles in the film.
6. Soft bake the wafer at 110°C for 1 minute.
7. Expose the wafer in the Karl Suss MA-6 for 10 seconds at 12 mW/cm^2 (120 mJ/cm^2).
8. Bake the wafer at 110°C for 1 minute to promote adhesion.
9. Develop for 45 seconds in MF-319 developer.
10. Rinse wafer in DI water and blow dry with N_2.

After the photoresist has served its masking purpose, it can be easily removed by soaking or spraying acetone, methanol, followed by IPA. It can also be removed in a short de-scum cycle under 10 sccm of O_2 plasma.

Appendix B

Photolithography Recipe for SU-8

The following recipe for SU-8 2025 used in this research was based on the SU-8 datasheet[44].

1. Make sure SU-8 has been warming to room temperature for several hours.
2. Clean wafer by spraying 5 seconds of Acetone, 5 seconds of Methanol, followed by 5 seconds of IPA and then spin dry for 1 additional minute.
3. Pour SU-8 directly from bottle onto center of wafer so that 1/3 of wafer is covered.
4. Spin at 300 RPM for 1 minute. Ensure SU-8 is evenly spreading across wafer.
5. Spin at 2000 RPM for 45 seconds for thickness of 50 μm. While spinning, lightly spray SU-8 thinner at the edge of the wafer to prevent beading due to the resist viscoscity.
6. Place wafer on hotplate while it heats to 65°C. At 65°C, wait 1 minute.
7. Ramp hotplate to 100°C. At 100°C, wait 10 minutes.
8. Expose the wafer in the Karl Suss MA-6 for 30 seconds at 12 mW/cm^2 (360 mJ/cm^2).
9. Place wafer on hotplate while it heats to 65°C. At 65°C, wait 1 minute.

10. Ramp hotplate to 100°C. At 100°C, wait 7 minutes. Turn the hotplate off and let the wafer cool back to room temperature.

11. Develop in SU-8 Developer for 6 minutes. For the last 1-2 minutes of development, use ultra-sonic agitation.

12. Rinse in IPA and lightly blow dry with N_2.

Appendix C

Photolithography and Removal Recipe for KMPR

The following recipe for KMPR 1025 used in this research was based on the KMPR datasheet[48].

C.1 Photolithography

1. Make sure KMPR has been warming to room temperature for several hours.
2. Clean wafer by spraying 5 seconds of Acetone, 5 seconds of Methanol, followed by 5 seconds of IPA and then spin dry for 1 additional minute.
3. Pour KMPR directly from bottle onto center of wafer so that 1/3 of wafer is covered.
4. Spin at 300 RPM for 1 minute. Ensure KMPR is evenly spreading across wafer.
5. Spin at 1500 RPM for 45 seconds for thickness of 50 μm. While spinning, lightly spray SU-8 thinner at the edge of the wafer to prevent beading due to the resist viscoscity.
6. Place wafer on hotplate while it heats to 65°C. At 65°C, wait 3 minute.
7. Ramp hotplate to 100°C. At 100°C, wait 15 minutes.

8. Expose the wafer in the Karl Suss MA-6 for 85 seconds at 12 mW/cm^2 (1020 mJ/cm^2) for Si areas, 125 seconds (1500 mJ/cm^2) for metallized areas.

9. Place wafer on hotplate while it heats to 65°C. At 65°C, wait 1 minute.

10. Ramp hotplate to 100°C. At 100°C, wait 4 minutes. Turn the hotplate off and let the wafer cool back to room temperature.

11. Develop in SU-8 Developer for 6 minutes. For the last 1-2 minutes of development, use ultra-sonic agitation.

12. Rinse in IPA and lightly blow dry with N_2. If white residues emerge from cavities, develop for a few more minutes.

13. If electroplating, perform a de-scum cycle of 100W of ICP power for 2 minutes in 10 sccm O_2.

C.2 Removal

1. Immerse the KMPR in Remover PG bath heated to 80°C for 5 minutes. KMPR should begin to wrinkle and curl up.

2. Rinse in DI water.

3. Immerse the KMPR in Remover K mixture heated to 80°C for 5 minutes. KMPR should detach from metal and wafer.

4. Rinse in DI water.

5. Immerse the sample in Neutralizer K at room temperature until all dark KMPR residue disappears.

6. Rinse in DI water.

Appendix D

Recipe for TMAH Wet Etching

The following recipe was used for bulk silicon etching using TMAH.

1. Using a container large enough to fit the wafers to be processed, mix a 4:1 concentration solution of DI water:TMAH.
2. Heat solution on a hotplate to 90°C. Depending on container size, hotplate may need to be set well above desired temperature (For 1 gallon of solution, hotplate was set to 170°C).
3. Use magnetic stirrer to agitate the solution at least at 250 RPM.
4. When temperature is reached, immerse samples in solution. Ensure that magnetic stirrer is able to move solution around sample.
5. Wait for desired time based on 0.5 μm/ min etch rate.
6. Rinse sample in DI water.

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